

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.
and APPLE INC.
Petitioners,

v.

MARLIN SEMICONDUCTOR LTD.,
Patent Owner.

Case No. IPR2025-00879
U.S. Patent No. 9,093,473 B2

**PATENT OWNER'S PRELIMINARY RESPONSE
PURSUANT TO 37 C.F.R. § 42.107(a)**

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TABLE OF EXHIBITS

Exhibit	Description
2001	Declaration of Joseph McAlexander
2002	Peter Van Zant, <i>Microchip Fabrication, A Practical Guide to Semiconductor Processing</i> , (4 th ed. 2000)

I. Summary

The Petition should be denied because none of its grounds establishes a reasonable likelihood that Petitioners will be able to prove that any of the asserted references or combinations teach or make obvious each limitation in any challenged claim.

Each of the challenged claims is directed to a method for fabricating a semiconductor transistor that includes, among others, two steps: (1) forming an epitaxial layer adjacent two sides of a gate pattern; and (2) forming a slot in the gate pattern to separate the gate pattern into individual gates. Critically, each claim requires that the slot must be formed **after** the epitaxial layer is formed.

But Grounds 1-4 do not identify—or even purport to identify—**any** reference that teaches forming the claimed slot after forming the claimed epitaxial layer. Indeed, the Petition does not identify (and does even allege to identify) any reference that teaches both slot and epitaxial layer formation in **any order**, much less the claimed one.

Instead, the Petition relies on two categories of references: (1) references (*Okuno* and *Mandelman*) that allegedly form a slot to separate a gate pattern into individual gates but do not teach, mention or use the claimed forming of an epitaxial layer; and (2) references (*Shin* and *Chong*) that form individual gates in a

conventional manner—without forming a slot in a gate pattern—and then allegedly form an epitaxial layer.

The Petition's grounds mix and match these different and disparate references in an attempt to make up for the fact that Petitioners could not find any reference that teaches forming the claimed slot after forming the claimed epitaxial layer. But these attempts fail.

Although the grounds alternately rely on *Okuno* (Grounds 1 & 3) and *Mandelman* (Grounds 2 & 4) as teaching the claimed slot formation, these references do not teach forming the slot after forming the epitaxial layer. They cannot because they do not disclose or suggest forming an epitaxial layer at all, much less forming an epitaxial layer before forming the slot.

So the grounds instead turn to *Shin* (combined with *Okuno* in Ground 1 and with *Mandelman* in Ground 3) and *Chong* (combined with *Okuno* in Ground 2 and with *Mandelman* in 4) as purportedly teaching the formation of an epitaxial layer. But this cannot save the Petition because *Shin* and *Chong* likewise fail to teach forming the slot after forming the epitaxial layer. They cannot because they do not disclose or suggest forming a slot at all, much less doing so after forming an epitaxial layer.

Accordingly, the Petition itself invents (or rather, copies from the challenged claims) the order of steps in its proposed reference combinations. After asserting (incorrectly) that a POSITA would combine the disparate and incompatible approaches of the two categories of references to arrive at a fabrication method that includes both forming of an epitaxial layer and forming a slot to separate an extended gate pattern into individual gates, the Petition simply presumes that a POSITA would and could perform these steps in the claimed order.

But the Petition's self-serving presumption has no reasonable basis. The Petition does not identify any teaching or suggestion of forming the epitaxial layer before forming the slot. To the contrary, the references that the Petition cites to—*Shin* and *Chong*—teach away from the Petition's presumed order. Each of those references teaches how to form an epitaxial layer after individual gates have already been formed. Following these teachings would necessarily lead a POSITA to likewise form the epitaxial layer after the slot is formed to divide the gate pattern create individual gates, which is the exact opposite of the claimed order here.

For at least these reasons, the Petition fails to establish the required likelihood of success and should be denied.

II. Semiconductor Transistor Technology Primer

The '473 Patent generally discloses and claims improved methods for fabricating semiconductor transistors. The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; and (2) common process steps for creating transistors.

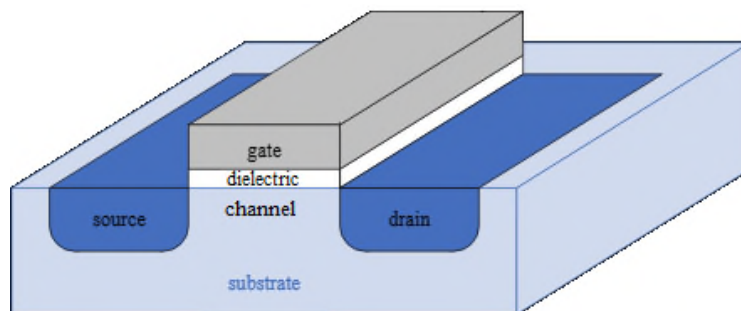
A. Basic Transistor Components

Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (i.e., turning electrical current on and off) and amplification (i.e., increasing the amplitude of a signal while retaining its electrical characteristics). (EX2002 at 1-2). Where earlier tube devices used a vacuum to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. (EX2002 at 3; EX2001, ¶6).

One type of transistor typically used in an integrated circuit (or "chip") is a "field effect transistor," or FET. The '473 Patent describes different types of transistors and FETs, including a Metal Oxide Semiconductor FET ("MOS"). (*E.g.*, EX1001 at 1:18-42).

Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. (EX2002 at 29-34). In a conductor (e.g., a metal), electric current can flow freely. (EX2002 at 29). A dielectric (e.g., silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. (EX2002 at 30). Semiconductors (e.g., silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. (EX2002 at 31-34; EX2001, ¶7).

The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. (See, e.g., EX2002 at 510-511). The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.

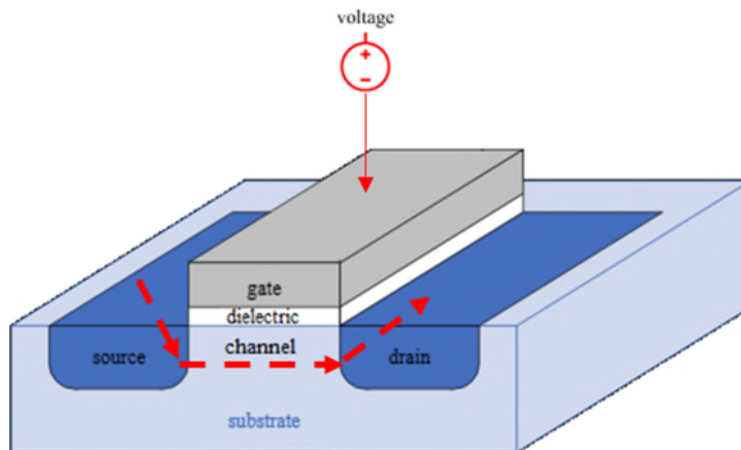


(See, e.g., EX2002 at 510-511; EX2001, ¶8).

The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). (EX2002 at 34-36, 510-511). The channel is a region under the gate and between the source and drain and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). (EX2002 at 510-511; EX2001, ¶9).

The gate is a conductor located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. (EX2002 at 510-511). When a voltage is applied to the gate, the dielectric prevents the flow of current from the gate to the channel, but the applied voltage results in the creation of a “field effect” in the channel. (EX2002 at 510-511). This “field effect” either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). (EX2002 at 510-511; EX2001, ¶10).

As illustrated below, this field effect allows electrical current to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping the flow of electrical current. (EX2001, ¶11).



B. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging. (EX2001, ¶17).

In the first stage, the semiconductor material itself is created. (EX2002 at 13). For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. (EX2002 at 13; EX2001, ¶18).

In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” (EX2002 at 13-14). A wafer acts as a semiconductor substrate on and in which transistors may be formed. (EX2001, ¶19).

The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. (EX2002 at 14). Thousands of integrated circuits can be formed on the substrate of a single wafer. (EX2002 at 14; EX2001, ¶20).

In the packaging stage, the wafer is separated into individual chips. (EX2002 at 14-15; EX2001, ¶21).

2. The Wafer Fabrication Stage

The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in the wafer's substrate. (EX2002 at 14). These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). (See EX2002 at 29-31, 71). For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning. (EX2001, ¶22).

Layering is the operation used to add thin layers to the semiconductor substrate. (EX2002 at 72). The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. (EX2002 at 72; EX2001, ¶23).

For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to the semiconductor substrate additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. (EX2002 at 72; EX2001, ¶24).

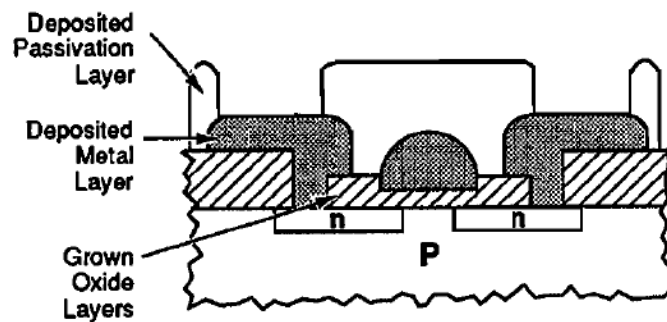


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

Patterning is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. (EX2002 at 72-73). This creates a pattern on the wafer surface. (EX2002 at 72-73; EX2001, ¶25).

The patterning may result in one or more holes in the layered material or one or more remaining islands of material. (EX2002 at 72-73; EX2001, ¶26). For

example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

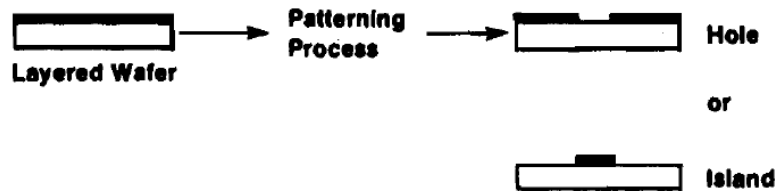


Figure 4.7 Patterning.

The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

(EX2002 at 73; EX2001, ¶27).

III. The Challenged '473 Patent

The '473 Patent describes and claims improved methods for fabricating semiconductor transistors that resolve certain problems associated with conventional methods, such as relatively low yields of acceptable gates. (EX1001 at 1:43-63). For example, the patent discloses creating a gate pattern on a substrate

and subsequently forming a slot in that gate pattern, thereby separating the pattern into two gates, with at least one gate on each side of the slot. (*E.g.*, EX1001 at 1:64-2:7, 2:44-62, 3:46-55). The '473 Patent further describes including an epitaxial layer in the fabricated transistor. (*E.g.*, EX1001 at 2:3-4, 3:19-21; EX2001, ¶37).

An “epitaxial layer” is a high purity layer of semiconducting material. (Van Zandt at 18, 380). The '473 Patent describes that correctly ordering the formation of the epitaxial layer is critical. Specifically, the patent discloses an inventive approach where, among other things, an epitaxial layer is formed adjacent a gate pattern **before**—rather than after—forming the slot separating the gate pattern into two gates. (*E.g.*, EX1001 at 2:3-7, 3:19-55, 4:27-31, 5:7-11, 5:24-29). According to the patent, this specific sequence and approach substantially avoids problems such as the formation of shallow, incomplete slots, “line end bridge of epitaxial layer[,] and growth of epitaxial layer on sidewall of the gate.” (*E.g.*, EX1001 at 1:44-63, 2:3-7, 3:19-55, 4:27-31, 5:7-11, 5:24-29; EX2001, ¶38).

A. The '473 Patent's Inventive Method Includes Forming The Epitaxial Layer Before The Slot

The '473 Patent describes an exemplary inventive fabrication method, starting with the formation of a gate pattern 24. (EX1001 at 2:34-3:3). That gate

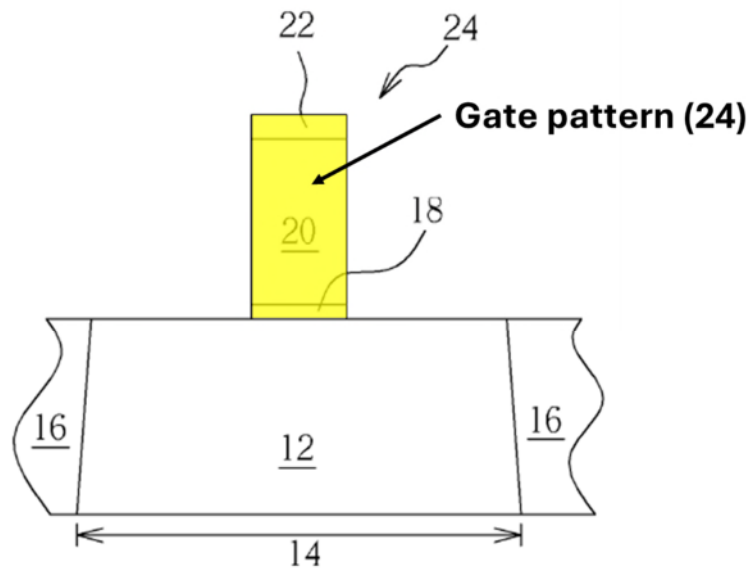
pattern formation starts with sequentially adding three layers on a substrate 12 (such as a silicon substrate):

(1) first, a gate insulating layer 18 (such as an oxide or nitride dielectric material) is deposited on the substrate 12;

(2) then a silicon layer (such as polysilicon layer 20) is formed on the gate insulating layer 18; and

(3) finally, a hard mask 22 (such as silicon dioxide or silicon nitride) is formed on the silicon layer. (*E.g.*, EX1001 at Fig. 1, 2:42-51; EX2001, ¶39).

These layers are then patterned (using a photo-etching process including one or more etchings to selectively remove portions of the layers) to form one or more gate patterns 24. (EX1001 at Fig. 1, 2:52-3:3). Annotated Figure 1 shows the layers in cross section, after etching was performed to form the gate pattern 24 (annotated in yellow):



1

(EX1001 at Fig. 1, 2:34-3:3). In Figure 1, the gate is running into or out of the page. (EX2001, ¶40). Annotated Figure 2 shows a top view of three of these gate patterns 24 on top of the substrate:

¹ Unless otherwise indicated, all colors and annotations to the challenged patent's figures are added.

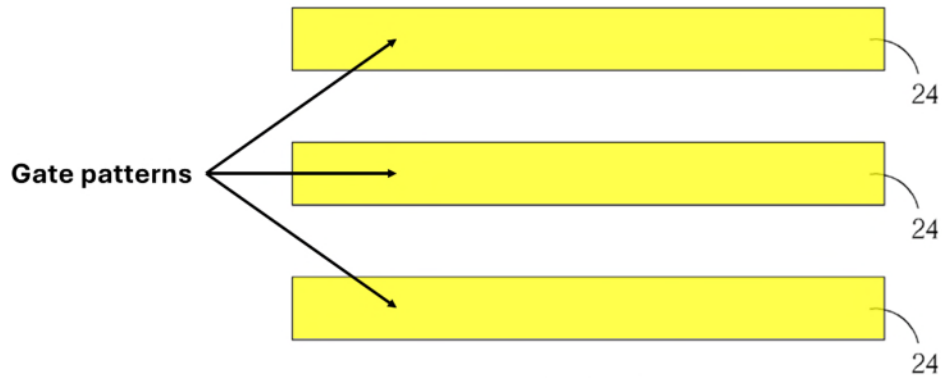
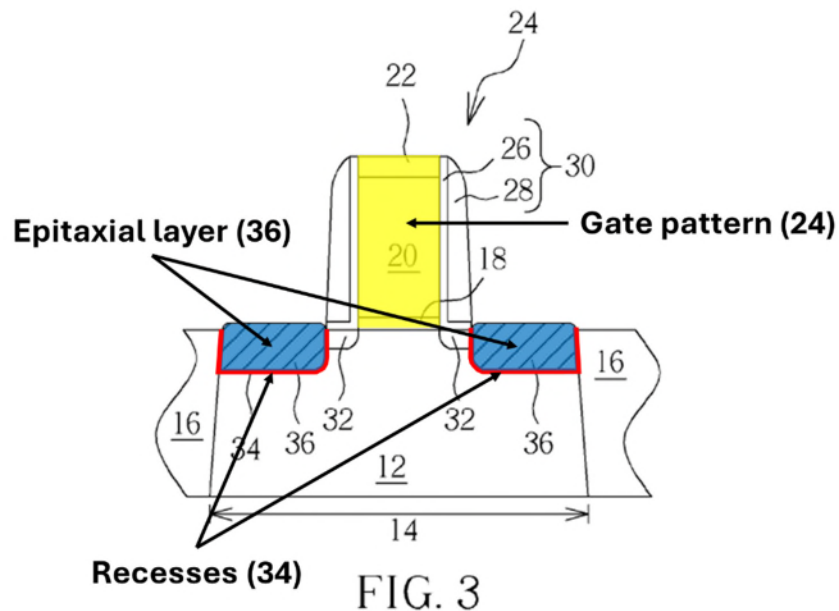


FIG. 2

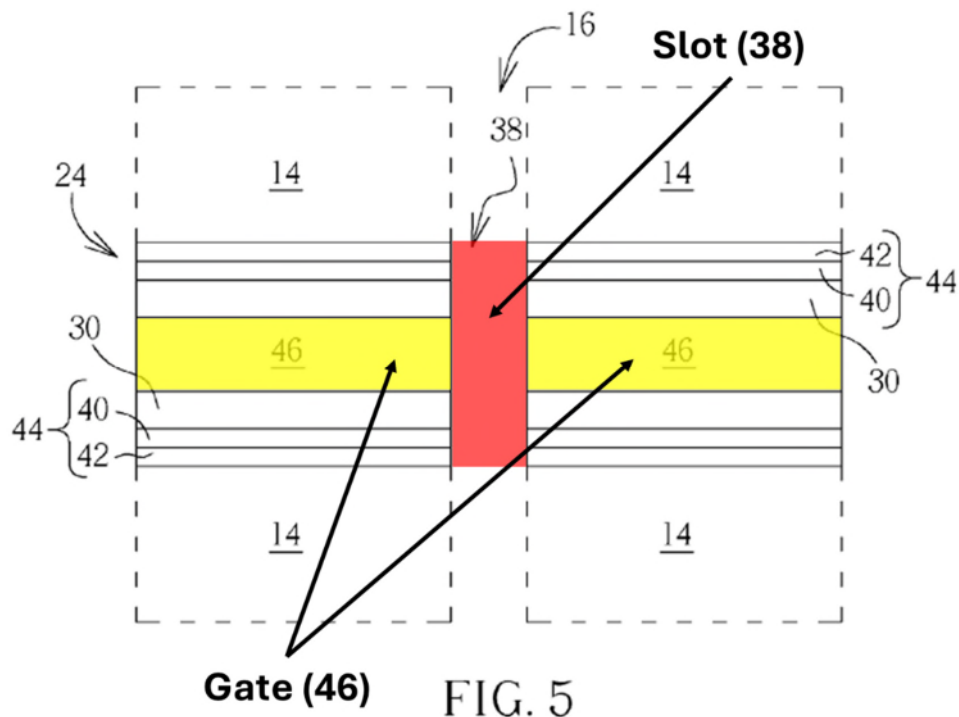
(EX1001 at Fig. 2, 2:63-3:3; EX2001, ¶41).

The '473 Patent describes subsequently forming epitaxial layers adjacent these gate patterns. (EX1001 at 3:11-28). For example, the patent describes patterning the substrate to form recesses 34 (illustrated below in annotated Figure 3) in the substrate and adjacent to two sides of the gate pattern 24. (EX1001 at 3:13-16). The patent further describes substantially filling these recesses with epitaxial growth, thereby forming an epitaxial layer 36 (annotated in blue below) that is in the substrate and adjacent to two sides of the gate pattern 24:



(EX1001 at Fig. 3, 3:13-21; EX2001, ¶42).

The '473 Patent describes forming a slot in the gate pattern after first forming the foregoing epitaxial layer. For example, the patent describes using another photo-etching process on the gate pattern, selectively removing material from the gate pattern to form a slot 38 therein. Annotated Figure 5 below is a top view illustrating this slot 38 (shown in red) in gate pattern 24. As the patent describes, this slot separates a gate pattern 24 into two independent gates 46:



(EX1001 at Fig. 5, 3:39-55; EX2001, ¶43).

B. The Challenged '473 Patent Claims

The Petition challenges all of the '473 Patent claims, namely independent claim 1 and dependent claims 2-10. Consistent with the foregoing, each of these claims is directed to a method for fabricating a semiconductor transistor and requires that a slot be formed in the gate pattern after an epitaxial layer is formed adjacent the gate pattern. (EX2001, ¶44).

For example, exemplary independent claim 1 recites:

1. A method for fabricating a metal-oxide semiconductor (MOS) transistor, comprising:
providing a semiconductor substrate;

forming a silicon layer on the semiconductor substrate;
performing a first photo-etching process on the silicon layer
for forming a gate pattern;
forming an epitaxial layer in the semiconductor substrate
adjacent to two sides of the gate pattern; and
**after forming the epitaxial layer, performing a second
photo-etching process on the gate pattern to form a slot
in the gate pattern** while using the gate pattern to
physically separate the gate pattern into two gates.

(EX1001 at claim 1; EX2001, ¶45).²

IV. PTAB Should Deny The Petition Because It Fails To Establish The Required Likelihood Of Success

The Petition asserts four independent grounds against various selections of claims:

Ground	Challenged Claim(s)	35 U.S.C. §¹	Reference(s)
1	1, 3	103	Okuno, Shin
2	1-10	103	Chong, Okuno
3	1, 3	103	Mandelman, Shin
4	1-6	103	Chong, Mandelman

The Petition should be denied because none of these grounds establishes a reasonable likelihood that Petitioners will be able to prove that any of the asserted

² Unless otherwise indicated, all emphases in quotations is added.

references or combinations teach or make obvious each limitation in any challenged claim. (EX2001, ¶47).

For example, the Grounds do not identify—or even purport to identify—**any** reference that teaches forming the claimed slot after forming the claimed epitaxial layer, as required by every challenged claim. Indeed, the Petition does not identify (and does even allege to identify) any reference that teaches both slot and epitaxial layer formation in **any order**, much less the claimed one. (EX2001, ¶48).

Instead, the Petition relies on two categories of references: (1) references (*Okuno* and *Mandelman*) that allegedly form a slot to separate a gate pattern into individual gates but do not teach, mention or use the claimed formation of an epitaxial layer; and (2) references (*Shin* and *Chong*) that form individual gates in a conventional manner—without forming the claimed slot in a gate pattern—and then allegedly form an epitaxial layer. (EX2001, ¶49).

The Petition’s grounds mix and match these different and disparate references in attempt to make up for the fact that Petitioners could not find any reference that teaches forming the claimed slot after forming the claimed epitaxial layer. But these attempts fail. (EX2001, ¶50).

Although the grounds alternately rely on *Okuno* (Grounds 1 & 3) and *Mandelman* (Grounds 2 & 4) as teaching the claimed slot formation, these

references do not teach forming the slot after forming the epitaxial layer. They cannot because they do not disclose or suggest forming an epitaxial layer at all, much less before forming the slot. (EX2001, ¶51).

So the grounds instead turn to *Shin* (combined with *Okuno* in Ground 1 and with *Mandelman* in Ground 3) and *Chong* (combined with *Okuno* in Ground 2 and with *Mandelman* in 4) as purportedly teaching the formation of an epitaxial layer. But this cannot save the Petition because *Shin* and *Chong* likewise fail to teach forming the slot after forming the epitaxial layer. They cannot because they do not disclose or suggest forming a slot at all, much less doing so after forming an epitaxial layer. (EX2001, ¶52).

Accordingly, the Petition itself invents (or rather, copies from the challenged claims) the order of steps in its proposed reference combinations. After asserting (incorrectly) that a POSITA would combine the disparate and incompatible approaches of the two categories of references to arrive at a fabrication method that includes both forming of an epitaxial layer and forming a slot to separate an extended gate pattern into individual gates, the Petition simply presumes that a POSITA would and could perform these steps in the claimed order. (EX2001, ¶53).

But the Petition's self-serving presumption has no reasonable basis. The Petition does not identify any teaching or suggestion of forming the epitaxial layer before forming the slot. To the contrary, the references that the Petition cites to—*Shin* and *Chong*—teach away from the Petition's presumed order. Each of those references teaches how to form an epitaxial layer **after** individual gates have already been formed. Following these teachings would necessarily lead a POSITA to likewise form the epitaxial layer **after** the slot is formed to divide the gate pattern create individual gates, which is the exact opposite of the claimed order here. (EX2001, ¶54).

For at least these reasons, the Petition should be denied.

A. The *Okuno* Grounds 1 & 2 Fail To Disclose Or Suggest Forming The Slot After Forming The Epitaxial Layer

Each challenged claim requires that a slot be formed in the gate pattern **after** an epitaxial layer is formed adjacent the gate pattern.

forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and

after forming the epitaxial layer, performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.

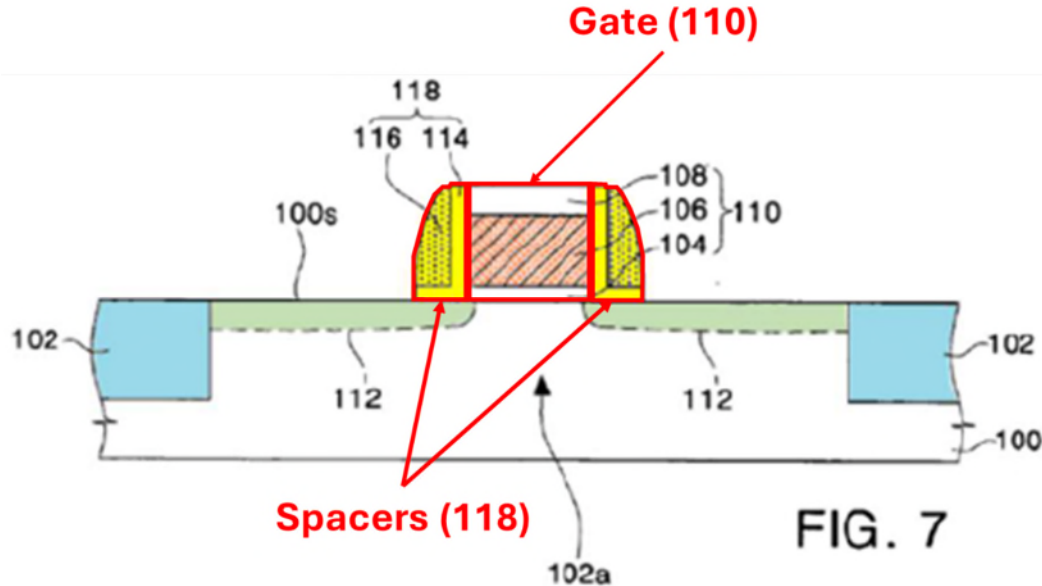
(EX1001 at claim 1; EX2001, ¶55).

Grounds 1 and 2 each rely on *Okuno* as allegedly teaching the claimed forming a slot to separate the gate pattern into individual gates. (Petition at 23-24, 44). But because *Okuno* does not teach forming this slot **after** forming an epitaxial layer as claimed (or forming an epitaxial layer at all), the Petition tries to combine *Okuno* with *Shin* (Ground 1) or *Chong* (Ground 2) to cure this fatal defect. But *Shin* and *Chong* likewise do not teach or suggest this missing limitation. (EX2001, ¶56).

1. Ground 1: *Shin* Does Not Teach Or Suggest Forming The Slot After Forming The Epitaxial Layer

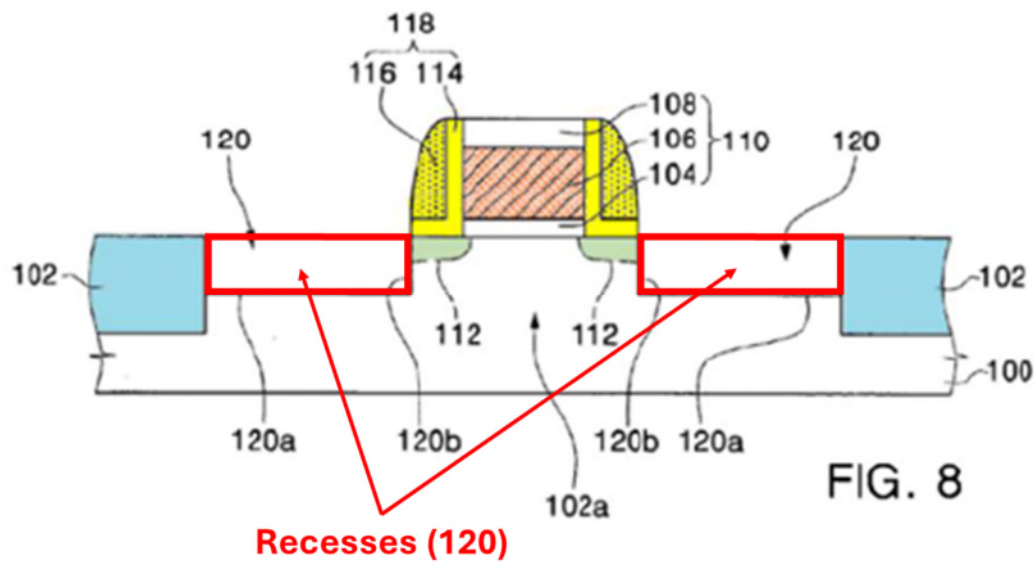
Shin cannot save Ground 1 because, like *Okuno*, it fails to teach or suggest forming the slot after forming the epitaxial layer. The Petition does not assert otherwise. It could not because *Shin* indisputably does not teach forming a slot at all, in any order. (EX2001, ¶57).

Instead, as the Petition concedes, rather than using a slot to separate a gate pattern into individual gates, *Shin* uses conventional layering and patterning to pattern individual gates, including the individual gate depicted in the Petition's annotated *Shin* Figure 7:



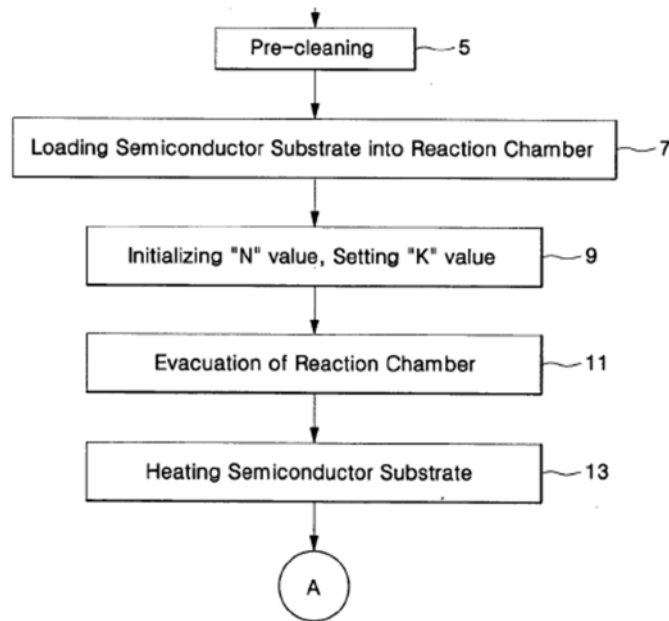
(Petition at 18; EX1006 at Fig. 7 (annotations from Petition except for red labels), ¶¶ 80-82). Because the gates are formed in the desired pattern from the start, there is no need to cut them into separate gates using a slot. (EX2001, ¶58).

According to the Petition and *Shin*, after this individual gate is formed, *Shin* teaches subsequently using the gate and its spacer to selectively pattern recesses 120 in the substrate, as shown in the Petition's annotated Figure 8:



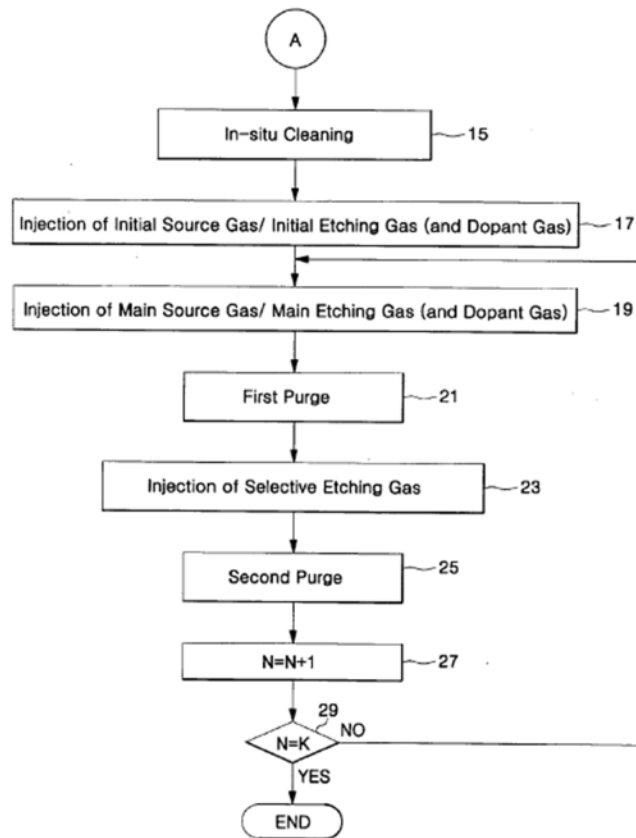
(Petition at 18; EX1006 at Fig. 8 (annotations from Petition except for red label), ¶¶ 80-82; EX2001, ¶59).

The Petition asserts that *Shin* teaches next forming epitaxial layers in the recesses. (Petition at 18). *Shin* describes that the initial steps of this process include the below steps 5, 7, 9, 11, and 13, described in detail in *Shin* (but ignored by the Petition and its obviousness allegations):



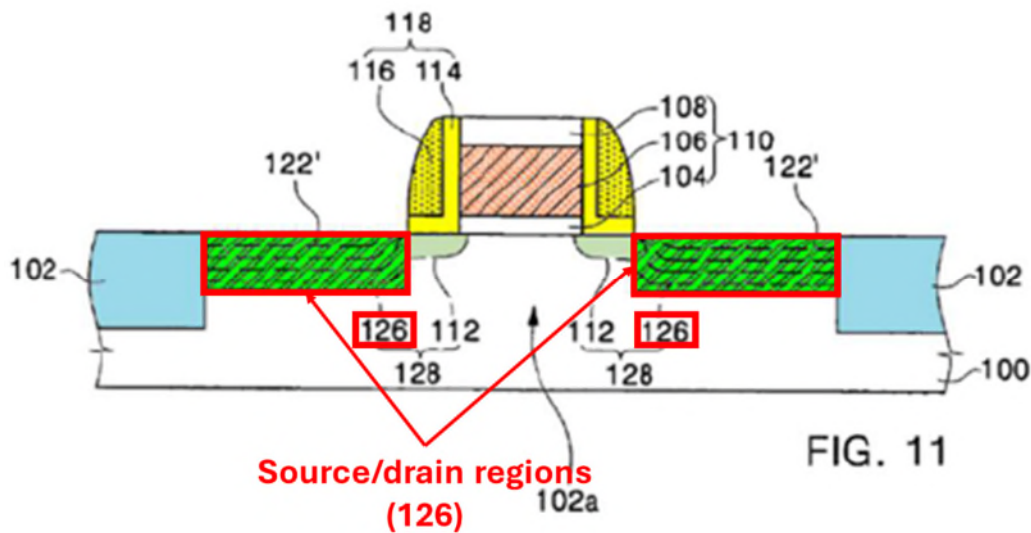
(EX1006 at Fig. 1A, ¶¶ 58-59, 84-85; EX2001, ¶60).

Shin further describes (but the Petition again ignores) that the formation of the final epitaxial layers further includes steps 15-29 illustrated below, which include a repeated series of gas injections and purges within a reaction chamber, including the steps identified below, which are repeatedly performed until the epitaxial layer meets its final thickness:



(EX1006 at Fig. 1B, ¶¶ 58-59, 84-85; EX2001, ¶61).

The Petition asserts that once the epitaxial layers are formed, *Shin* describes doping those epitaxial layers and create source/drain regions 126 at either side of the gate, as depicted in the Petition's annotated Figure 11, thereby concluding the formation of the transistor:



(Petition at 18; EX1006 at Fig. 11 (annotations from Petition except for red labels), ¶ 90; EX2001, ¶62).

Thus, *Shin* cannot save Ground 1 because it indisputably does not disclose or suggest forming a slot at all, much less doing so after forming the epitaxial layer. (EX2001, ¶63).

The Petition's argument that *Shin* nonetheless teaches this missing limitation because, according to the Petition, it was obvious to incorporate *Shin*'s method of forming source/drain region into *Okuno* is wrong for at least two additional reasons. (*E.g.*, Petition at 23; EX2001, ¶64).

First, the Petition never even addresses *Shin*'s disclosed method for forming its source/drain regions (including steps 5-29), nor does it assert, much less provide evidence establishing, that this method would have worked and been compatible with *Okuno*'s materially different fabrication process. Instead, the Petition just

presumes that any source/drain fabrication method may be substituted for any other source/drain fabricate method, a presumption that is both totally unsupported and wholly false. (EX2001, ¶65).

Second, even if it were obvious to incorporate *Shin*'s method for fabricating source/drain regions into *Okuno*—which the Petition does not come close to proving—that incorporation would not result in the claimed order. The claims require that the slot be formed to separate the gate pattern into individual gates **after** the formation of the epitaxial layer. *Shin* teaches the opposite—*Shin*'s method for fabricating source-drain regions teaches performing all of the steps, including the detailed and complex formation of epitaxial layers, after the individual gates were already formed. Thus, incorporating this method into *Okuno* would result in the epitaxial layers being formed after the individual gates were formed. Accordingly, in the proposed combination, the slot would be formed to separate the gate pattern into individual gates **before** the formation of any epitaxial layer, not after. (EX2001, ¶¶66-68).

For each and any of the foregoing reasons, Ground 1 fails.

2. Ground 2: Chong Does Not Teach Or Suggest Forming The Slot After Forming The Epitaxial Layer

Chong likewise cannot cure *Okuno*'s deficiencies because, like *Okuno*, it too fails to teach or suggest forming the slot after forming the epitaxial layer. Rather,

just like *Shin*, *Chong* could not possibly teach this missing limitation because it is undisputed that *Chong* does not teach forming a slot at all, in any order. (EX2001, ¶70).

As with *Shin*, rather than using a slot to separate a gate pattern into individual gates, *Chong* uses conventional layering and patterning to pattern individual gates, including the individual gate 122 depicted in the Petition's annotated *Chong* Figure 1:

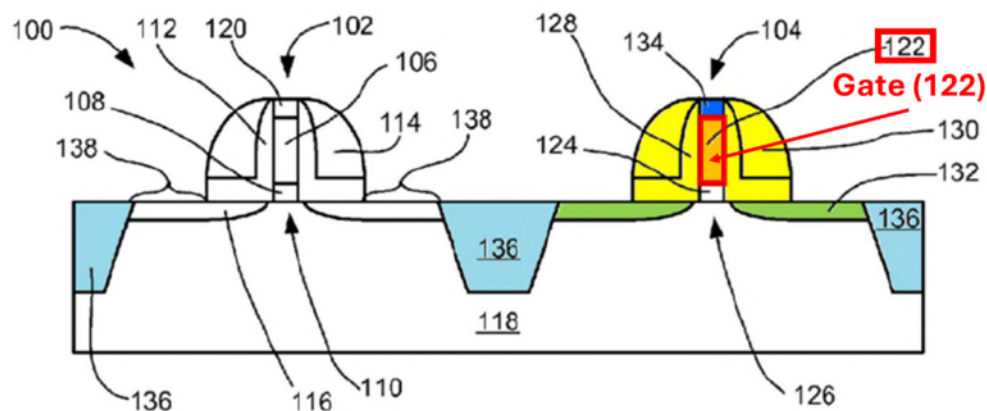


FIG. 1

(Petition at 27; EX1007 at Fig. 1 (annotations from Petition except for red label), ¶¶ 28-31). As with the *Shin* gates, because the *Chong* gates are formed in the desired pattern from the start, there is no need to cut them into separate gates using a slot. (EX2001, ¶71).

And as the Petition describes, *Chong* teaches the formation of recesses 400 only after this individual gate has already been formed:

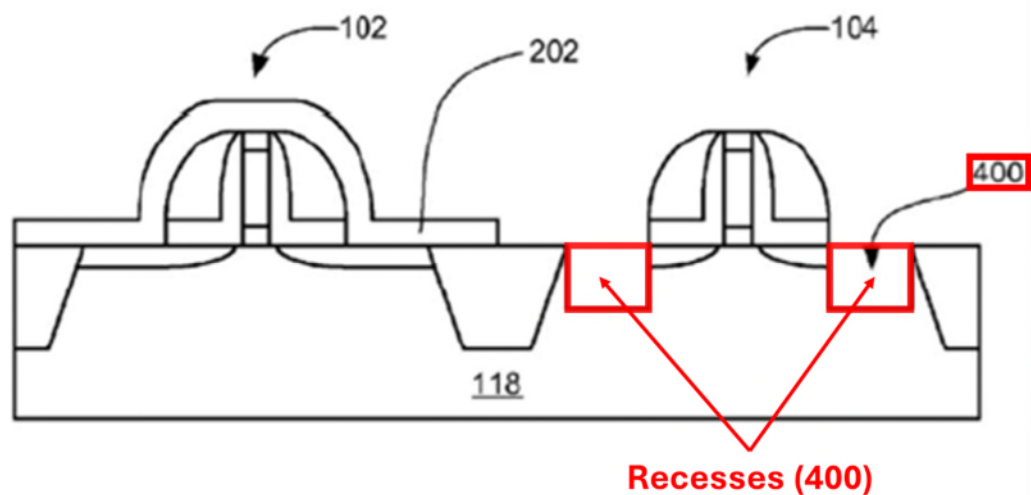


FIG. 4

(Petition at 27; EX1007 at Fig. 4, ¶38; EX2001, ¶72).

After numerous other steps, *Chong* eventually describes forming source/drains 502 in recesses 400 and the alleged epitaxial layers in those source/drains 502:

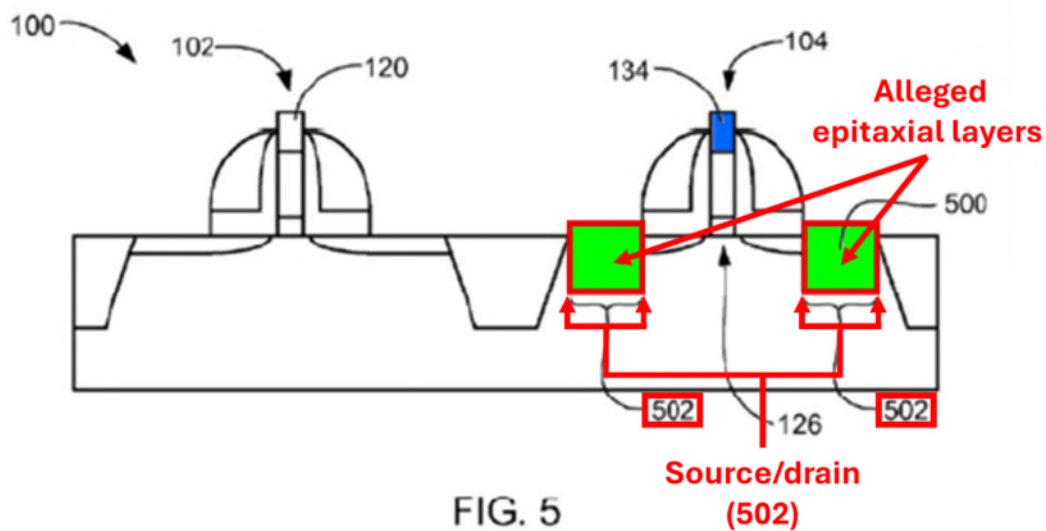


FIG. 5

(Petition at 27; EX1007 at Fig. 1 (annotations from Petition except for red labels), ¶¶ 40-44; EX2001, ¶73).

Thus, *Chong* cannot save Ground 2 because it indisputably does not disclose or suggest forming a slot at all, much less doing so after forming the epitaxial layer. (EX2001, ¶74).

The Petition's argument that *Chong* nonetheless teaches this missing limitation because, according to the Petition, it was obvious to use *Okuno*'s slot to form the individual gates in *Chong* make no sense. (*E.g.*, Petition at 44). *Chong* admittedly and explicitly teaches creating its individual gates **before** then forming its source/drain regions and alleged epitaxial layers. (Petition at 27; EX1007 at ¶¶ 28-31, 38, 40-44). Thus, if creating those *Chong* gates by forming a notch to separate gate pattern into individual gates was just a design choice as the Petition alleges (Petition at 30), then applying that design choice to *Chong* would result in the slot being formed to separate the gate pattern into individual gates **before** the formation of the alleged epitaxial layer, **not after** as required by the claims. EX2001, ¶¶75-76).

For each and any of the foregoing reasons, Ground 2 fails.

B. The *Mandelman* Grounds 3 & 4 Fail To Disclose Or Suggest Forming The Slot After Forming The Epitaxial Layer

Grounds 3 and 4 mirror Grounds 1 and 2 and fail for the same foregoing reasons. These grounds simply substitute the similarly defective *Mandelman* reference for *Okuno* and then make substantively the same arguments about allegedly curing that fatal defect with either *Shin* (Ground 3) or *Chong* (Ground 4). These arguments fail for all the same reasons discussed above in connection with Grounds 1 and 2. (EX2001, ¶78).

Specifically, *Mandelman*—like *Okuno*—allegedly discloses forming a slot in a gate pattern to separate it into individual gates. (*E.g.*, Petition at 70-71, 78). But *Mandelman* does not teach forming the slot after forming the epitaxial layer. It cannot because they do not disclose or suggest forming an epitaxial layer at all, much less before forming the slot. The Petition does not argue otherwise. (EX2001, ¶79).

Instead, the Petition attempts to cure *Mandelman*'s deficiency—substantively identical to *Okuno*'s identified deficiency—with the same arguments concerning *Shin* or *Chong*. (EX2001, ¶80).

But *Shin* cannot save Ground 3 for all the same reasons it cannot save Ground 1, including:

(1) *Shin* cannot provide the missing but required forming of the slot after forming the epitaxial layer because *Shin* indisputably does not disclose or suggest forming a slot at all, much less doing so after forming the epitaxial layer.

(2) The Petition once again does not even attempt to establish that *Shin*'s disclosed method for forming its source/drain regions (including steps 5-29) would have been operable, compatible, and obvious to use with *Mandelman*'s materially different fabrication process, but just baselessly and wrongly presumes that any source/drain fabrication method may be substituted for any other source/drain fabricate method. (*E.g.*, Petition at 66).

(3) Even if it were obvious to incorporate *Shin*'s method for fabricating source/drain regions into *Mandelman*—and it is not—that incorporation would not result the claimed order. The claims requires that the slot be formed to separate the gate pattern into individual gates **after** the formation of the epitaxial layer. *Shin* teaches the opposite—*Shin*'s method for fabricating source-drain regions teaches performing all of the steps, including the detailed and complex formation of epitaxial layers, after the individual gates were already formed. Thus, incorporating this method into *Mandelman* would result in the epitaxial layers being formed after the individual gates were formed. Accordingly, in the proposed

combination, the slot would be formed to separate the gate pattern into individual gates **before** the formation of any epitaxial layer, not after. (EX2001, ¶81).

And *Chong* cannot save Ground 4 for all the same reasons it cannot save Ground 2, including:

(1) *Chong* cannot provide the missing but required order of forming of the slot after the forming epitaxial layer because *Chong* indisputably does not disclose or suggest forming a slot at all, much less doing so after forming the epitaxial layer.

(2) *Chong* admittedly and explicitly teaches creating its individual gates **before** then forming its source/drain regions and alleged epitaxial layers. (Petition at 27; EX1007 at ¶¶ 28-31, 38, 40-44). Thus, if creating those *Chong* gates by forming a notch to separate gate pattern into individual gates (as taught in *Mandelman*) was just a design choice as the Petition alleges (Petition at 73), then applying that design choice to *Chong* would result in the slot being formed to separate the gate pattern into individual gates **before** the formation of the alleged epitaxial layer, **not after** as required by the claims. (EX2001, ¶82).

For each and any of the foregoing reasons, Grounds 3 and 4 fail along with Grounds 1 and 2. (EX2001, ¶83).

V. Conclusion

For the foregoing reasons, the Board should deny institution of the Petition.

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner hereby certifies, in reliance on the word count of the word-processing system (Microsoft Office Word 2010) used to prepare this preliminary response, that the number of words in this paper is 5,136. This word count excludes the tables of contents, tables of authorities, certificate of word count, certificate of service, and table of exhibits.

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CERTIFICATE OF SERVICE

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