

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY LTD.
and APPLE INC.

Petitioners,

v.

MARLIN SEMICONDUCTOR LTD.,
Patent Owner.

Case No. IPR2025-00879
U.S. Patent No. 9,093,473 B2

**DECLARATION OF JOSEPH C. MCALEXANDER III REGARDING
PATENT OWNER'S PRELIMINARY RESPONSE FOR *INTER PARTES*
REVIEW OF U.S. PATENT NO. 9,093,473**

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TABLE OF EXHIBITS

Exhibit	Description
2002	Peter Van Zant, <i>Microchip Fabrication, A Practical Guide to Semiconductor Processing</i> , (4 th ed. 2000)

I. Qualifications

1. I am a Registered Professional Engineer (#79454) and the President of McAlexander Sound, Inc. I hold a Bachelor of Science degree in Electrical Engineering from North Carolina State University. I have been associated with the integrated circuit and electronics industry as a designer and consultant for the past 53 years and am a named inventor on 31 U.S. patents and a number of foreign patents, many of which are directly related to the design and operation of transistors and circuits incorporating transistors, including control, addressing, comparing and sensing, and fabrication.

2. My skills and experience are in areas of circuit design and analysis, device and board fabrication and assembly, testing, marketing, control system design and analysis, manufacturing operations, and respective areas of quality, reliability, and defect/failure analysis. Specifically, I have:

- designed memories, including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant (incorporating both non-volatile EPROM and random access memory components), parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs;
- managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing,

analysis, and control involved use of mechanical calibration and measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and FFT for HARI applications;

- taught courses in solid-state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;
- provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, volatile and non-volatile memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), and consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other); and
- designed and managed development, testing, and evaluation of memory devices and systems incorporating such devices, including simulation of operation. I have also had experience in programming, erasing, and wearout of electrically programmable and erasable non-volatile memories.

3. Because of my background, training, and experience, I am qualified as an expert to opine on the challenged patent. A more detailed account of my work experience and other qualifications is listed in my Curriculum Vitae attached to this Declaration.

II. Materials Considered

4. In preparing this declaration, I have reviewed the Petition and the declaration of Petitioner's expert, as well as the material that they cite, including the asserted prior art.

III. Semiconductor Transistor Technology Primer

5. The following is a brief primer of semiconductor transistors to establish a foundation of common terms and concepts that can be used in addressing the defects in the Petition. These terms and concepts focus on: (1) the basic components of transistors; (2) the difference between planar and three-dimensional (e.g., fin) transistors; and (3) common process steps for creating transistors.

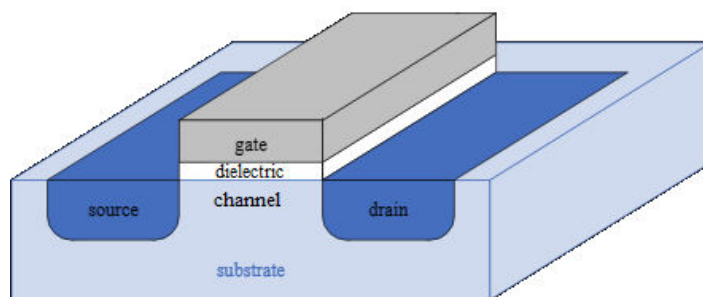
A. Basic Transistor Components

6. Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions: switching (i.e., turning electrical current on and off) and amplification (i.e., increasing the amplitude of a signal while retaining its electrical characteristics). (EX2002 at 1-2). Where earlier tube devices used a vacuum to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors. (EX2002 at 3).

7. One type of transistor typically used in an integrated circuit (or "chip") is a "field effect transistor," or FET. The '473 Patent describes different types of transistors and FETS, including a Metal Oxide Semiconductor FET ("MOS"). (E.g., EX1001 at 1:18-42). Materials used to build such transistors are divided into three categories based on their ability to conduct electrical current: conductors, dielectrics, and semiconductors. (EX2002 at 29-34). In a conductor (e.g., a metal), electric

current can flow freely. (EX2002 at 29). A dielectric (e.g., silicon dioxide) is an insulative material at the opposite end of the conductivity spectrum and has a high resistance to the flow of current. (EX2002 at 30). Semiconductors (e.g., silicon) fall between conductors and dielectrics and have some conducting and some resisting ability. (EX2002 at 31-34).

8. The simplified FET below illustrates how these materials may be used to create a semiconductor transistor device. As shown, the transistor is built on a semiconductor substrate and comprises a source, a drain, a gate, and a channel. (*See, e.g.,* EX2002 at 510-511). The source, drain and channel comprise semiconductor material, the gate comprises a conductor, and the gate and channel are separated by a thin dielectric layer.



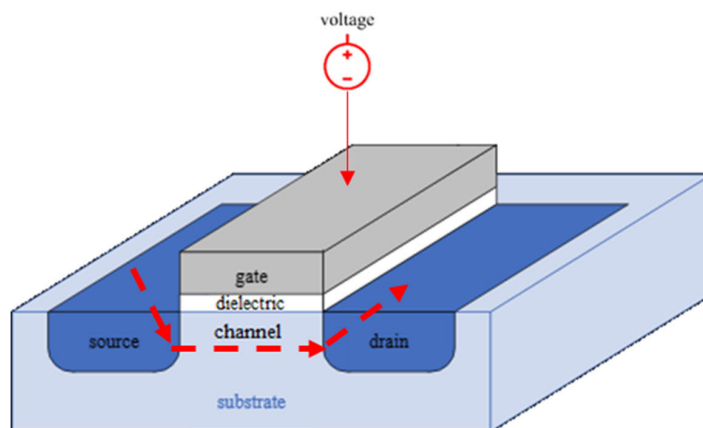
(*See, e.g.,* EX2002 at 510-511).

9. The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in holes (a positive, or p-type, region). (EX2002 at 34-36, 510-511). The channel is a region under the gate

and between the source and drain and is of the opposite type to that of the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa). (EX2002 at 510-511).

10. The gate is a conductor located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. (EX2002 at 510-511). When a voltage is applied to the gate, the dielectric prevents the flow of current from the gate to the channel, but the applied voltage results in the creation of a “field effect” in the channel. (EX2002 at 510-511). This “field effect” either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). (EX2002 at 510-511).

11. As illustrated below, this field effect allows electrical current to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate switches the transistor on and off, starting and stopping the flow of electrical current.

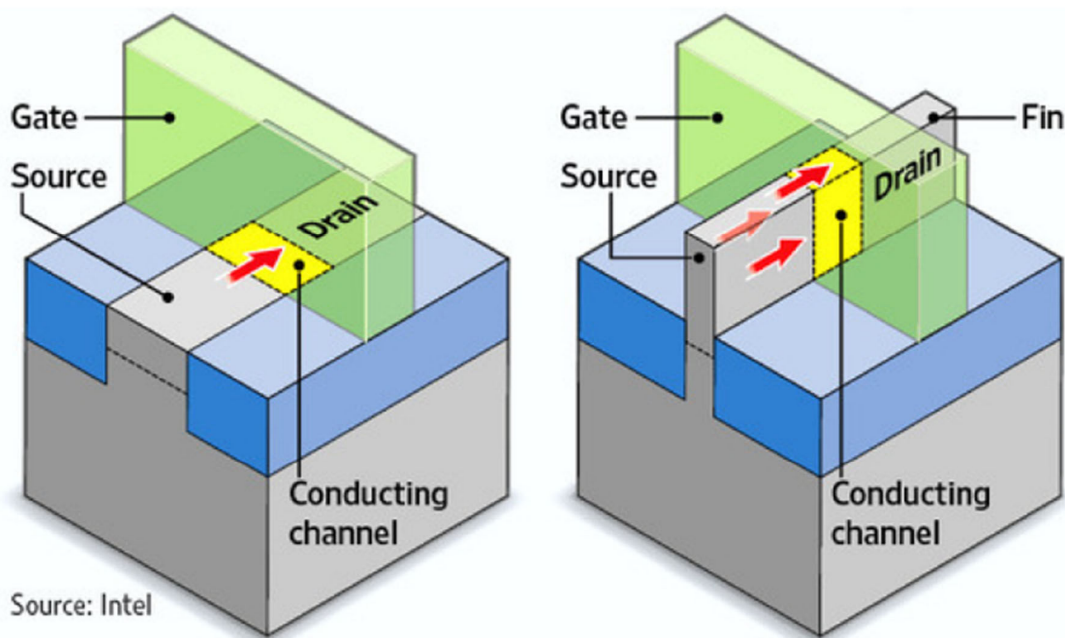


B. Planar vs. Three-Dimensional Transistors

12. Integrated circuit chips in modern computer systems are typically composed of millions and even billions of transistors. The first transistor prototypes in 1947 were several inches in size, and implementing even the simplest early computers required tens of thousands of gates or transistors. Given those numbers, and the correlation between an increased number of transistors and increased computing power, the desire to shrink transistor sizes to fit more transistors on a chip has been consistent and widespread in industry. This desire led to the development of a new type of transistor, a “FinFET.”

13. The simplified illustrative FET transistors illustrated in the previous section all feature a gate structure built on a flat semiconductor substrate; in other words, a “planar” FET. In the early 2010s, however, commercial gates evolved from such two-dimensional (2D) planar transistors to three-dimensional (3D) FinFET transistors.

14. In the below image, the figure on the left illustrates a 2D planar transistor built on a flat silicon substrate. In this traditional 2D planar transistor, the transistor forms a conducting channel in the silicon region under the gate.



15. In contrast, as illustrated above in the right figure, an exemplary 3D fin transistor design features a vertical semiconductor fin structure above the substrate that acts as a channel between the source and drain regions. In the resulting fin field effect transistor (“FinFET”), the source and drain regions are formed at opposing regions of the fin, and the gate is wrapped over the fin surrounding the fin on the top and two sides.

16. Thus, where a planar gate has only a horizontal dimension, the FinFET gate has both horizontal and vertical dimensions, thereby allowing a FinFET transistor to take up less surface area than a planar transistor. This alone means that more FinFET transistors may fit on an integrated circuit chip compared to that of the planar transistor. In addition, because FinFETs typically leak less current than

planar FET transistors, FinFETs may be more tightly packed on an integrated circuit chip. This, too, increases the number of FinFET transistors that may fit onto a single chip.

C. Processes For Manufacturing Integrated Circuits And Transistors

1. The Four Stages Of Fabricating Integrated Circuits

17. The intricate, complex manufacturing process developed over the years for achieving such highly-dense integrated circuits can be divided into four distinct stages: (1) material preparation; (2) wafer preparation; (3) wafer fabrication; and (4) packaging.

18. In the first stage, the semiconductor material itself is created. (EX2002 at 13). For a silicon semiconductor, the raw starting material is sand, which is converted to pure silicon with a polysilicon structure. (EX2002 at 13).

19. In the second stage, the semiconductor material is first formed into a silicon crystal with specific electrical and structural parameters, and it is then sliced into thin disks called “wafers.” (EX2002 at 13-14). A wafer acts as a semiconductor substrate on and in which transistors may be formed.

20. The third stage is wafer fabrication, during which individual integrated circuits are formed in and on the wafer semiconductor substrate. (EX2002 at 14). Thousands of integrated circuits can be formed on the substrate of a single wafer. (EX2002 at 14).

21. In the packaging stage, the wafer is separated into individual chips. (EX2002 at 14-15).

2. The Wafer Fabrication Stage

22. The third manufacturing stage, wafer fabrication, is the one most relevant here, and it can take several thousand steps, during which transistors and other devices are formed in the wafer's substrate. (EX2002 at 14). These steps are generally performed using three categories of materials (conductors, semiconductors, and dielectrics) in four basic operations (layering, patterning, doping, and heat treatments). (See EX2002 at 29-31, 71). For purposes of understanding the Petition and its deficiencies, the two most important basic operations are layering and patterning.

23. **Layering** is the operation used to add thin layers to the semiconductor substrate. (EX2002 at 72). The layers may be conductors, semiconductors, or dielectrics; and they can have a variety of functions and be made in a variety of ways. (EX2002 at 72).

24. For example, one way of adding a layer of material is to deposit that material onto the semiconductor substrate. Another way of adding a layer of material is to grow the material on the semiconductor substrate. After an initial layer is added to the semiconductor substrate additional layers may be added to the earlier layers using similar growth or deposition processes. To illustrate, the transistor

structure shown below shows a number of layers that have been added to the wafer's semiconductor substrate, some deposited, some grown. (EX2002 at 72).

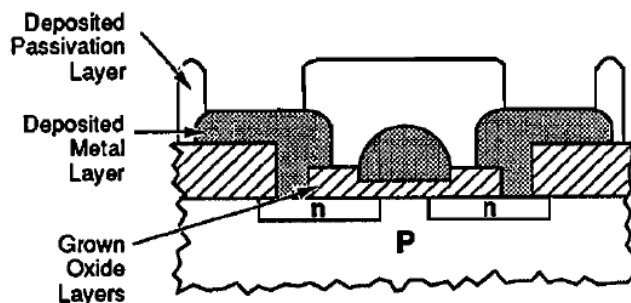


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

25. **Patterning** is the series of steps to remove (etch away) selected portions of the semiconductor substrate or one or more layers of materials that were added during one or more prior layering operations. (EX2002 at 72-73). This creates a pattern on the wafer surface. (EX2002 at 72-73).

26. The patterning may result in one or more holes in the layered material or one or more remaining islands of material. (EX2002 at 72-73). For example, the following figures illustrate the use of patterning to make (1) a hole in a previously formed layer: and (2) an island from a previously formed layer:

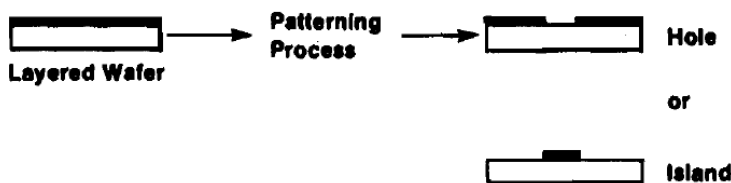


Figure 4.7 Patterning.

27. The repeated combination of layering and patterning in different sequences and variations is critical to the formation of transistors in and on the semiconductor wafer:

These parts are created one layer at a time by the combination of putting a layer on the surface and removing a portion, with a patterning process, to leave a specific shape. The goal of the patterning operations is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other parts.

(EX2002 at 73).

IV. Understanding Of The Law

28. In preparing and expressing my opinions and considering the subject matter of the challenged patent, I am relying on certain basic legal principles that counsel have explained to me. These principles are discussed below.

A. Claim Construction

29. I understand that the scope of a patent is defined by its claims. I understand that a claim can be:

- a. a method claim, which covers a process/activity, or
- b. an apparatus claim, which covers a physical machine, etc.

30. I understand that the first step in determining the validity of a claim is for the claim to be properly construed. I have been further advised that, in an inter partes review proceeding, the claims of a patent are typically given their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the claims and the patent disclosure (specification).

31. I further understand that an inventor can provide special definitions for specific claim term(s) within the patent. However, any special definition for a claim term must be set forth in the specification with reasonable clarity and precision.

B. Invalidity

32. I have been informed that a claim may be invalid as obvious if the subject matter described by the claim, as a whole, would have been obvious to a POSITA at the time the claimed invention was made. I understand that the standard for obviousness in an inter partes review proceeding is by a preponderance of the evidence.

33. I have also been informed that a determination of obviousness involves an analysis of the scope and content of the prior art, the similarities between the claimed invention and the prior art, and the level of ordinary skill in the art. I have been informed and understand that a prior art reference should be viewed as a whole.

34. I have been informed that in considering whether an invention for a claimed combination would have been obvious, I may assess whether there are

apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the market place, and/or the background knowledge possessed by a POSITA. I also understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious.

35. I have been informed that, in making a determination as to whether or not the claimed invention would have been obvious to a POSITA, one may consider certain objective indicators of non-obviousness if they are present, such as: commercial success of product(s) practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. I understand that for such objective evidence to be relevant to the non-obviousness of claim, however, there must be a causal relationship (called a “nexus”) between the claim and the evidence. I also understand that this nexus must be based on a novel element of the claim rather than something available in the prior art.

36. I have also been informed and understand that, when considering the obviousness of a patent claim, one should consider whether a reason or motivation existed for combining the elements of the references in the manner claimed, and that

the prior art must create a reasonable expectation of success in producing the claimed subject matter.

V. The Challenged '473 Patent

37. The '473 Patent describes and claims improved methods for fabricating semiconductor transistors that resolve certain problems associated with conventional methods, such as relatively low yields of acceptable gates. (EX1001 at 1:43-63). For example, the patent discloses creating a gate pattern on a substrate and subsequently forming a slot in that gate pattern, thereby separating the pattern into two gates, with at least one gate on each side of the slot. (E.g., EX1001 at 1:64-2:7, 2:44-62, 3:46-55). The '473 Patent further describes including an epitaxial layer in the fabricated transistor. (E.g., EX1001 at 2:3-4, 3:19-21).

38. An “epitaxial layer” is a high purity layer of semiconducting material. (Van Zandt at 18, 380). The '473 Patent describes that correctly ordering the formation of the epitaxial layer is critical. Specifically, the patent discloses a novel approach where, among other things, an epitaxial layer is formed adjacent a gate pattern **before**—rather than after—forming the slot separating the gate pattern into two gates. (E.g., EX1001 at 2:3-7, 3:19-55, 4:27-31, 5:7-11, 5:24-29). According to the patent, this specific sequence and approach substantially avoids problems such as the formation of shallow, incomplete slots, “line end bridge of

epitaxial layer[,] and growth of epitaxial layer on sidewall of the gate.” (*E.g.*, EX1001 at 1:44-63, 2:3-7, 3:19-55, 4:27-31, 5:7-11, 5:24-29).

A. The '473 Patent's Inventive Method Includes Forming The Epitaxial Layer Before The Slot

39. The '473 Patent describes an exemplary inventive fabrication method, starting with the formation of a gate pattern 24. (EX1001 at 2:34-3:3). That gate pattern formation starts with sequentially adding three layers on a substrate 12 (such as a silicon substrate):

- (1) first, a gate insulating layer 18 (such as an oxide or nitride dielectric material) is deposited on the substrate 12;
- (2) then a silicon layer (such as polysilicon layer 20) is formed on the gate insulating layer 18; and
- (3) finally, a hard mask 22 (such as silicon dioxide or silicon nitride) is formed on the silicon layer. (*E.g.*, EX1001 at Fig. 1, 2:42-51).

40. These layers are then patterned (using a photo-etching process including one or more etchings to selectively remove portions of the layers) to form one or more gate patterns 24. (EX1001 at Fig. 1, 2:52-3:3). Annotated Figure 1 shows the layers in cross section, after etching was performed to form the gate pattern 24 (annotated in yellow):

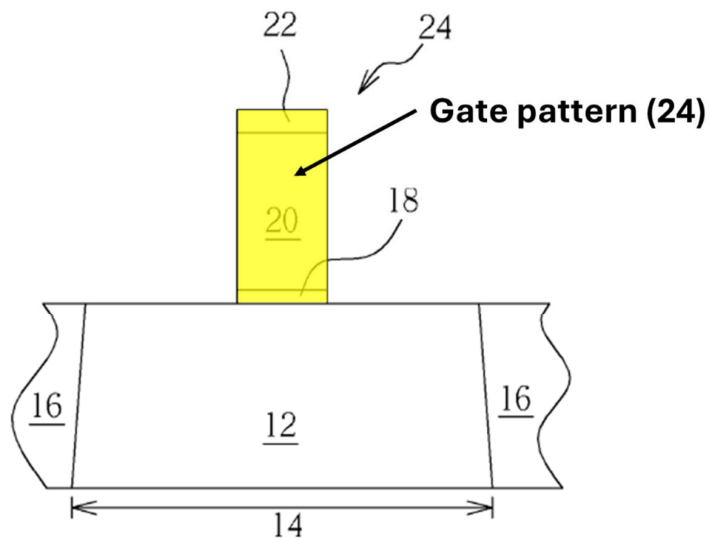


FIG. 1

1

(EX1001 at Fig. 1, 2:34-3:3). In Figure 1, the gate is running into or out of the page.

41. Annotated Figure 2 shows a top view of three of these gate patterns 24 on top of the substrate:

¹ Unless otherwise indicated, all colors and annotations to the challenged patent's figures are added.

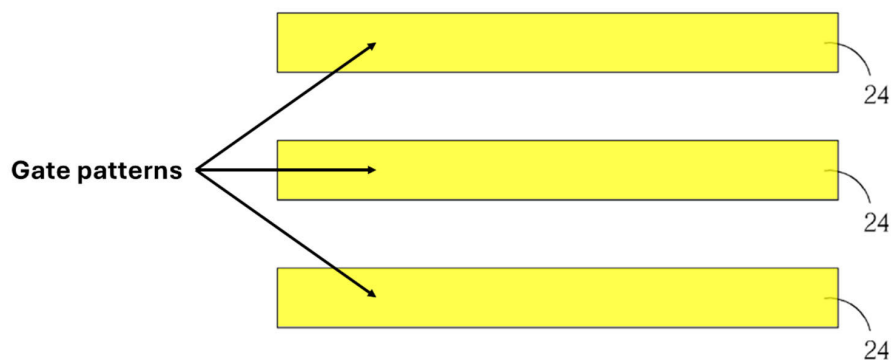
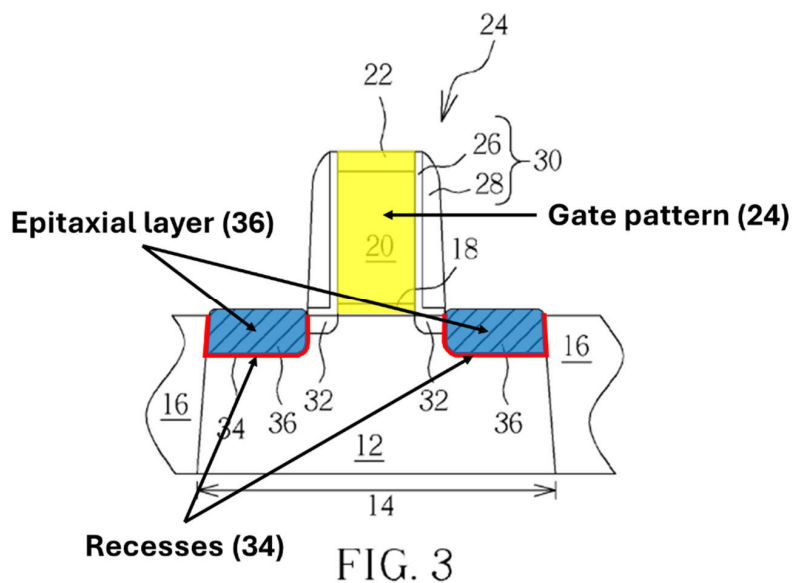


FIG. 2

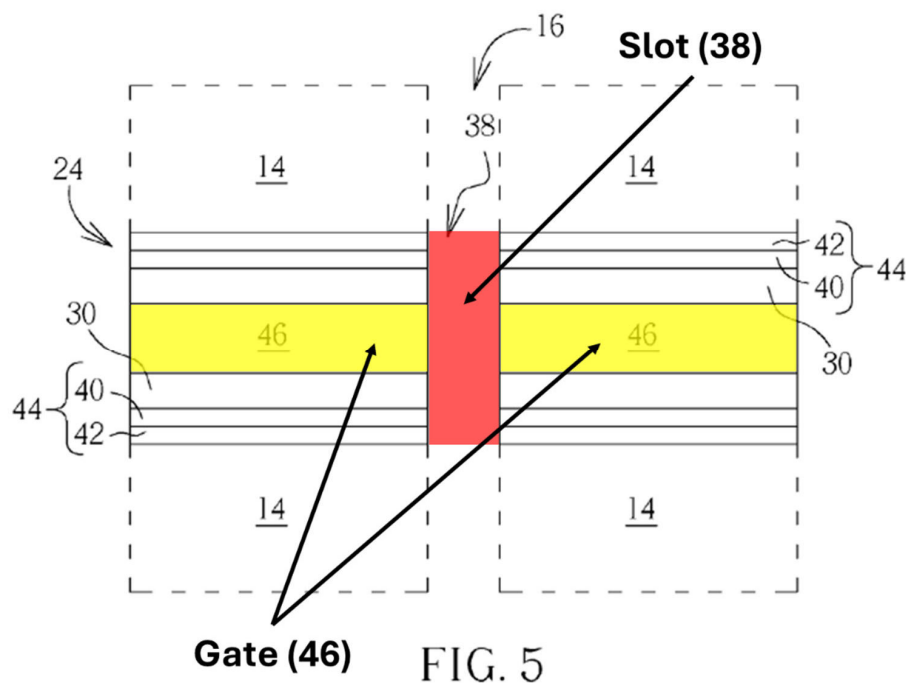
(EX1001 at Fig. 2, 2:63-3:3).

42. The '473 Patent describes subsequently forming epitaxial layers adjacent these gate patterns. (EX1001 at 3:11-28). For example, the patent describes patterning the substrate to form recesses 34 (illustrated below in annotated Figure 3) in the substrate and adjacent to two sides of the gate pattern 24. (EX1001 at 3:13-16). The patent further describes substantially filling these recesses with epitaxial growth, thereby forming an epitaxial layer 36 (annotated in blue below) that is in the substrate and adjacent to two sides of the gate pattern 24:



(EX1001 at Fig. 3, 3:13-21).

43. The '473 Patent describes forming a slot in the gate pattern after first forming the foregoing epitaxial layer. For example, the patent describes using another photo-etching process on the gate pattern, selectively removing material from the gate pattern to form a slot 38 therein. Annotated Figure 5 below is a top view illustrating this slot 38 (shown in red) in gate pattern 24. As the patent describes, this slot separates a gate pattern 24 into two independent gates 46:



(EX1001 at Fig. 5, 3:39-55).

B. The Challenged '473 Patent Claims

44. The Petition challenges all of the '473 Patent claims, specifically independent claim 1 and dependent claims 2-10. Consistent with the foregoing, each of these claims is directed to a method for fabricating a semiconductor transistor and requires that a slot be formed in the gate pattern after an epitaxial layer is formed adjacent the gate pattern.

45. For example, exemplary independent claim 1 recites:

1. A method for fabricating a metal-oxide semiconductor (MOS) transistor, comprising:
providing a semiconductor substrate;

forming a silicon layer on the semiconductor substrate;
performing a first photo-etching process on the silicon layer
for forming a gate pattern;
forming an epitaxial layer in the semiconductor substrate
adjacent to two sides of the gate pattern; and
**after forming the epitaxial layer, performing a second
photo-etching process on the gate pattern to form a slot
in the gate pattern** while using the gate pattern to
physically separate the gate pattern into two gates.

(EX1001 at claim 1).²

VI. The Asserted Grounds Fail To Demonstrate Invalidity

46. The Petition asserts four independent grounds against various selections of claims:

Ground	Challenged Claim(s)	35 U.S.C. § ¹	Reference(s)
1	1, 3	103	Okuno, Shin
2	1-10	103	Chong, Okuno
3	1, 3	103	Mandelman, Shin
4	1-6	103	Chong, Mandelman

47. In my opinion, the Petition fails to show that any of the asserted references or combinations teaches or renders obvious each limitation in any challenged claim.

² Unless otherwise indicated, all emphases in quotations is added.

48. For example, the Grounds do not identify—or even purport to identify—any reference that teaches forming the claimed slot after forming the claimed epitaxial layer, as required by every challenged claim. Indeed, the Petition does not identify (and does even allege to identify) any reference that teaches both slot and epitaxial layer formation in any order, much less the claimed one.

49. Instead, the Petition relies on two categories of references: (1) references (*Okuno* and *Mandelman*) that allegedly form a slot to separate a gate pattern into individual gates but do not teach, mention or use the claimed formation of an epitaxial layer; and (2) references (*Shin* and *Chong*) that form individual gates in a conventional manner—without forming the claimed slot in a gate pattern—and then allegedly form an epitaxial layer.

50. The Petition's grounds mix and match these different and disparate references in attempt to make up for the fact that Petitioners could not find any reference that teaches forming the claimed slot after forming the claimed epitaxial layer. But these attempts fail.

51. Although the grounds alternately rely on *Okuno* (Grounds 1 & 3) and *Mandelman* (Grounds 2 & 4) as teaching the claimed slot formation, these references do not teach forming the slot after forming the epitaxial layer. They cannot because

they do not disclose or suggest forming an epitaxial layer at all, much less before forming the slot.

52. So the grounds instead turn to *Shin* (combined with *Okuno* in Ground 1 and with *Mandelman* in Ground 3) and *Chong* (combined with *Okuno* in Ground 2 and with *Mandelman* in 4) as purportedly teaching the formation of an epitaxial layer. But this argument does not cure the deficiencies of the Petition because *Shin* and *Chong* likewise fail to teach forming the slot after forming the epitaxial layer. They cannot because they do not disclose or suggest forming a slot at all, much less doing so after forming an epitaxial layer.

53. Accordingly, the Petition itself concocts (or rather, copies from the challenged claims) the order of steps in its proposed reference combinations. After incorrectly asserting that a POSITA would combine the disparate and incompatible approaches of the two categories of references to arrive at a fabrication method that includes both forming of an epitaxial layer and forming a slot to separate an extended gate pattern into individual gates, the Petition simply presumes that a POSITA would and could perform these steps in the claimed order.

54. In my opinion, this presumption is entirely incorrect and has no reasonable basis. The Petition (and the supporting expert declaration) does not identify any teaching or suggestion of forming the epitaxial layer before forming the

slot. To the contrary, the references that the Petition cites to—*Shin* and *Chong*—counsel against the Petition’s presumed order. Each of those references teaches how to form an epitaxial layer **after** individual gates have already been formed. Following these teachings would necessarily lead a POSITA to likewise form the epitaxial layer **after** the slot is formed to divide the gate pattern create individual gates, which is the exact opposite of the claimed order here. Accordingly, the Petition thus fails to demonstrate invalidity.

A. The *Okuno* Grounds 1 & 2 Fail To Disclose Or Suggest Forming The Slot After Forming The Epitaxial Layer

55. Each challenged claim requires that a slot be formed in the gate pattern **after** an epitaxial layer is formed adjacent the gate pattern.

forming an epitaxial layer in the semiconductor substrate adjacent to two sides of the gate pattern; and

after forming the epitaxial layer, performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.

(EX1001 at claim 1).

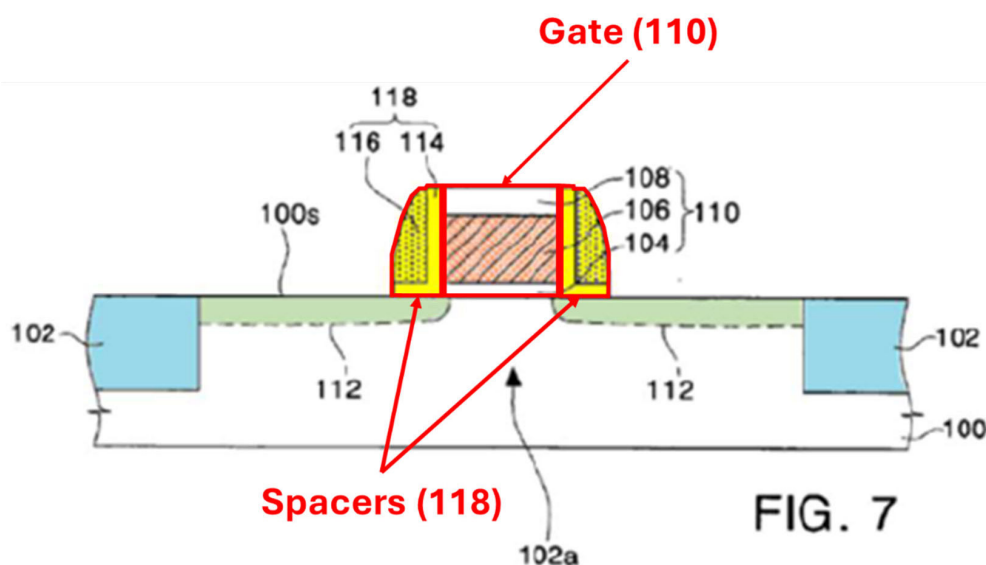
56. Grounds 1 and 2 each rely on *Okuno* as allegedly teaching the claimed forming a slot to separate the gate pattern into individual gates. (Petition at 23-24, 44). But because *Okuno* does not teach forming this slot **after** forming an epitaxial

layer as claimed (or forming an epitaxial layer at all), the Petition tries to combine Okuno with *Shin* (Ground 1) or *Chong* (Ground 2) to cure this fatal defect. But *Shin* and *Chong* likewise do not teach or suggest this missing limitation.

1. Ground 1: *Shin* Does Not Teach Or Suggest Forming The Slot After Forming The Epitaxial Layer

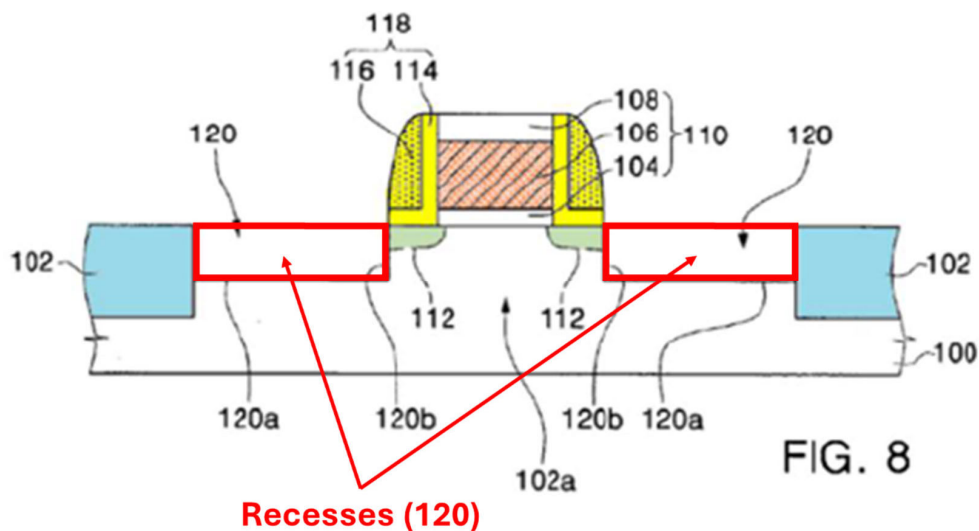
57. *Shin* cannot save Ground 1 because, like *Okuno*, it fails to teach or suggest forming the slot after forming the epitaxial layer. The Petition does not assert otherwise. It could not because *Shin* indisputably does not teach forming a slot at all, in any order.

58. Instead, as the Petition concedes, rather than using a slot to separate a gate pattern into individual gates, *Shin* uses conventional layering and patterning to pattern individual gates, including the individual gate depicted in the Petition's annotated *Shin* Figure 7:



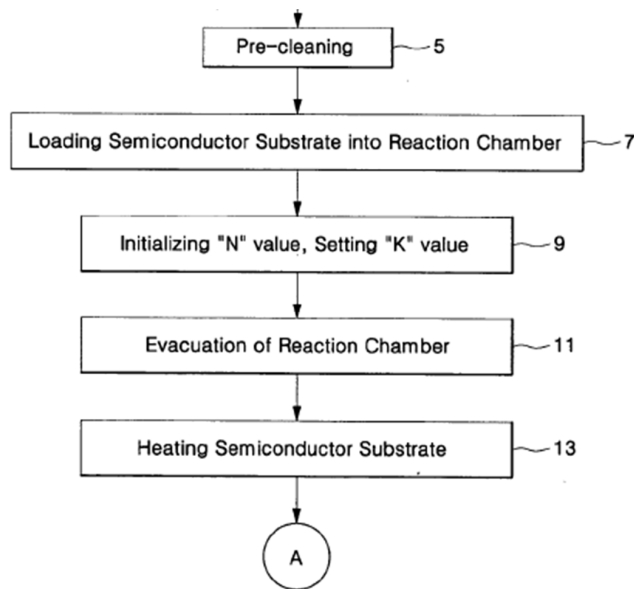
(Petition at 18; EX1006 at Fig. 7 (annotations from Petition except for red labels), ¶¶ 80-82). Because the gates are formed in the desired pattern from the start, there is no need to cut them into separate gates using a slot.

59. According to the Petition and *Shin*, after this individual gate is formed, *Shin* teaches subsequently using the gate and its spacer to selectively pattern recesses 120 in the substrate, as shown in the Petition's annotated Figure 8:



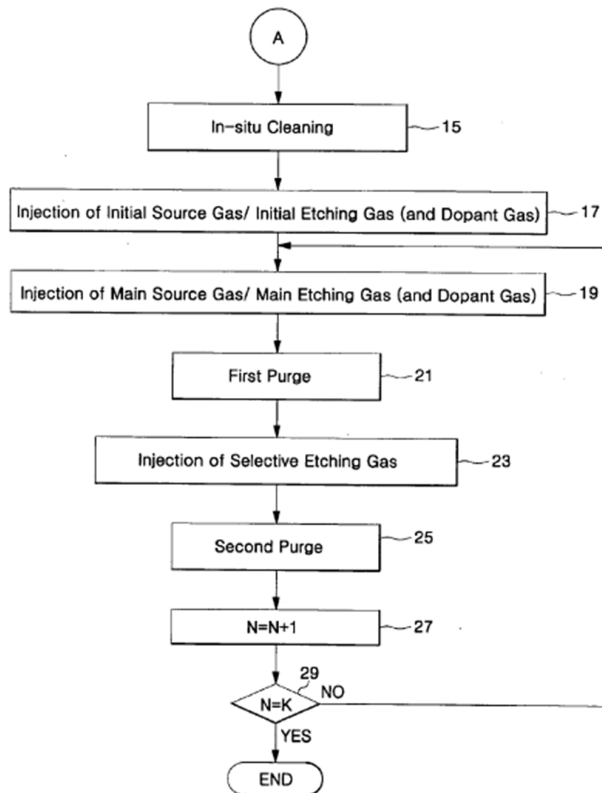
(Petition at 18; EX1006 at Fig. 8 (annotations from Petition except for red label), ¶¶ 80-82).

60. The Petition asserts that *Shin* teaches next forming epitaxial layers in the recesses. (Petition at 18). *Shin* describes that the initial steps of this process include the below steps 5, 7, 9, 11, and 13, described in detail in *Shin* (but ignored by the Petition and its accompanying expert declaration):



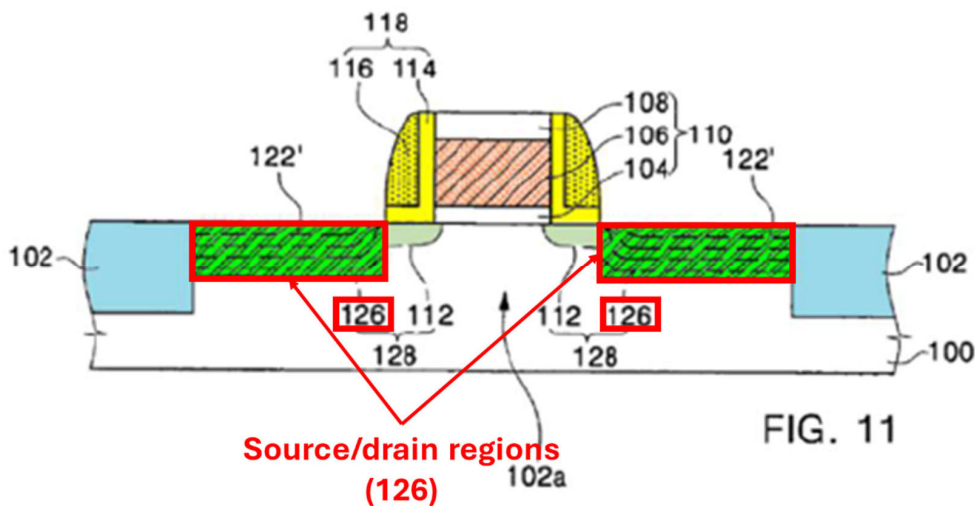
(EX1006 at Fig. 1A, ¶¶ 58-59, 84-85).

61. *Shin* further describes (but the Petition and supporting expert declaration again ignore) that the formation of the final epitaxial layers further includes steps 15-29 illustrated below, which include a repeated series of gas injections and purges within a reaction chamber, including the steps identified below, which are repeatedly performed until the epitaxial layer meets its final thickness:



(EX1006 at Fig. 1B, ¶¶ 58-59, 84-85).

62. The Petition asserts that once the epitaxial layers are formed, *Shin* describes doping those epitaxial layers and create source/drain regions 126 at either side of the gate, as depicted in the Petition’s annotated Figure 11, thereby concluding the formation of the transistor:



(Petition at 18; EX1006 at Fig. 11 (annotations from Petition except for red labels), ¶ 90).

63. Thus, *Shin* cannot save Ground 1 because it indisputably does not disclose or suggest forming a slot at all, much less doing so after forming the epitaxial layer.

64. The Petition's argument that *Shin* nonetheless teaches this missing limitation because, according to the Petition, it was obvious to incorporate *Shin*'s method of forming source/drain region into *Okuno* is wrong for at least two additional reasons. (*E.g.*, Petition at 23).

65. First, neither the Petition nor the supporting expert declaration even address Shin's disclosed method for forming its source/drain regions (including steps 5-29), nor do they assert, much less provide evidence establishing, that this method would have worked and been compatible with *Okuno's* materially different

fabrication process. Instead, the Petition and expert declaration just presume that any source/drain fabrication method may be substituted for any other source/drain fabricate method, a presumption that is both totally unsupported and wholly false.

66. Second, even if it were obvious to incorporate *Shin*'s method for fabricating source/drain regions into *Okuno*—which neither the Petition nor the supporting expert declaration come close to proving—that incorporation would not result in the claimed order.

67. The claims require that the slot be formed to separate the gate pattern into individual gates **after** the formation of the epitaxial layer. *Shin* teaches the opposite—*Shin*'s method for fabricating source-drain regions teaches performing all of the steps, including the detailed and complex formation of epitaxial layers, after the individual gates were already formed. Thus, incorporating this method into *Okuno* would result in the epitaxial layers being formed after the individual gates were formed.

68. Accordingly, in the proposed combination, the slot would be formed to separate the gate pattern into individual gates **before** the formation of any epitaxial layer, not after.

69. For each and any of the foregoing reasons, Ground 1 fails to demonstrate invalidity.

2. Ground 2: *Chong* Does Not Teach Or Suggest Forming The Slot After Forming The Epitaxial Layer

70. *Chong* likewise cannot cure *Okuno*'s deficiencies because, like *Okuno*, it too fails to teach or suggest forming the slot after forming the epitaxial layer. Rather, just like *Shin*, *Chong* could not possibly teach this missing limitation because it is undisputed that *Chong* does not teach forming a slot at all, in any order.

71. As with *Shin*, rather than using a slot to separate a gate pattern into individual gates, *Chong* uses conventional layering and patterning to pattern individual gates, including the individual gate 122 depicted in the Petition's annotated *Chong* Figure 1:

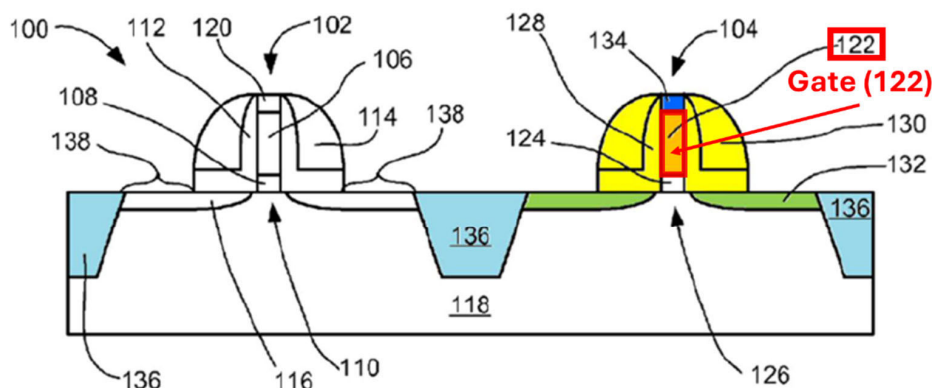


FIG. 1

(Petition at 27; EX1007 at Fig. 1 (annotations from Petition except for red label),

¶¶ 28-31). As with the *Shin* gates, because the *Chong* gates are formed in the desired pattern from the start, there is no need to cut them into separate gates using a slot.

72. And as the Petition describes, *Chong* teaches the formation of recesses 400 only after this individual gate has already been formed:

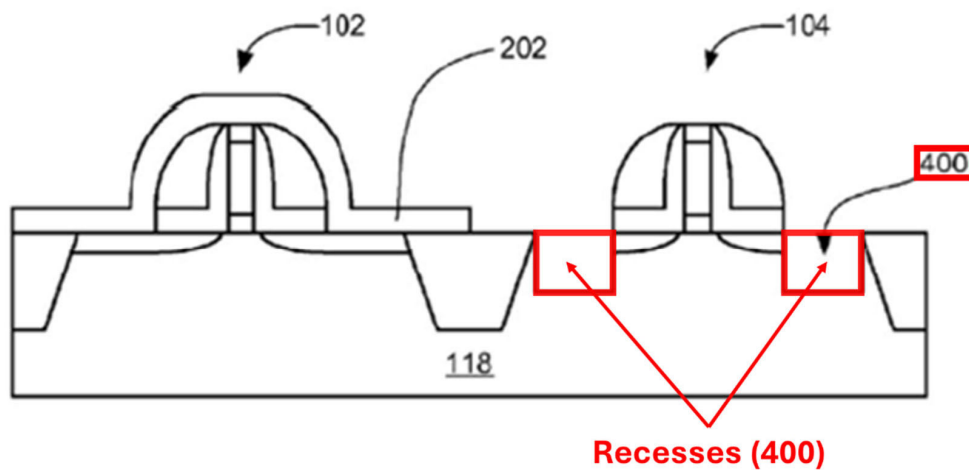
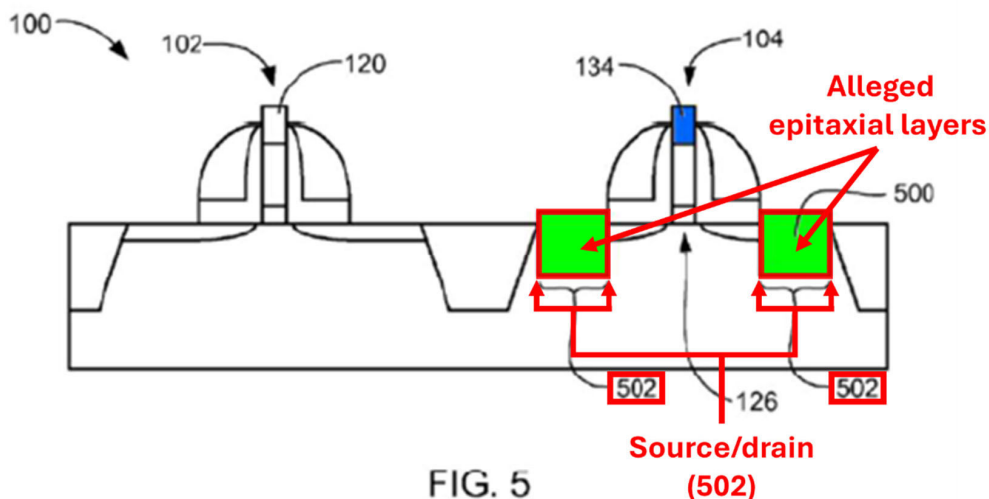


FIG. 4

(Petition at 27; EX1007 at Fig. 4, ¶38).

73. After numerous other steps, *Chong* eventually describes forming source/drains 502 in recesses 400 and the alleged epitaxial layers in those source/drains 502:



(Petition at 27; EX1007 at Fig. 1, ¶¶ 40-44 (annotations from Petition except for red labels)).

74. Thus, *Chong* cannot save Ground 2 because it indisputably does not disclose or suggest forming a slot at all, much less doing so after forming the epitaxial layer.

75. The Petition's argument that *Chong* nonetheless teaches this missing limitation because, according to the Petition, it was obvious to use *Okuno*'s slot to form the individual gates in *Chong* makes no sense. (*E.g.*, Petition at 44).

76. *Chong* admittedly and explicitly teaches creating its individual gates **before** then forming its source/drain regions and alleged epitaxial layers. (Petition at 27; EX1007 at ¶¶ 28-31, 38, 40-44). Thus, if creating those *Chong* gates by forming a notch to separate gate pattern into individual gates was just a design choice

as the Petition alleges (Petition at 30), then applying that design choice to *Chong* would result in the slot being formed to separate the gate pattern into individual gates **before** the formation of the alleged epitaxial layer, **not after** as required by the claims.

77. For each and any of the foregoing reasons, Ground 2 also fails to demonstrate invalidity.

B. The *Mandelman* Grounds 3 & 4 Fail To Disclose Or Suggest Forming The Slot After Forming The Epitaxial Layer

78. Grounds 3 and 4 mirror Grounds 1 and 2 and fail for the same reasons. These grounds simply substitute the similarly defective *Mandelman* reference for *Okuno* and then make substantively the same arguments about allegedly curing that fatal defect with either *Shin* (Ground 3) or *Chong* (Ground 4). These arguments fail for all the same reasons discussed above in connection with Grounds 1 and 2.

79. Specifically, *Mandelman*—like *Okuno*—allegedly discloses forming a slot in a gate pattern to separate it into individual gates. (*E.g.*, Petition at 70-71, 78). But *Mandelman* does not teach forming the slot after forming the epitaxial layer. It cannot because they do not disclose or suggest forming an epitaxial layer at all, much less before forming the slot. Neither the Petition nor the supporting expert declaration argues otherwise.

80. Instead, the Petition attempts to cure *Mandelman*'s deficiency—substantively identical to *Okuno*'s identified deficiency—with the same arguments concerning *Shin* or *Chong*.

81. But *Shin* cannot save Ground 3 for all the same reasons it cannot save Ground 1, including:

- (1) *Shin* cannot provide the missing but required forming of the slot after forming the epitaxial layer because *Shin* indisputably does not disclose or suggest forming a slot at all, much less doing so after forming the epitaxial layer.
- (2) The Petition once again does not even attempt to establish that *Shin*'s disclosed method for forming its source/drain regions (including steps 5-29) would have been operable, compatible, and obvious to use with *Mandelman*'s materially different fabrication process, but just baselessly and wrongly presumes that any source/drain fabrication method may be substituted for any other source/drain fabricate method. (*E.g.*, Petition at 66).
- (3) Even if it were obvious to incorporate *Shin*'s method for fabricating source/drain regions into *Mandelman*—and it is not—that incorporation would not result the claimed order. The claims requires

that the slot be formed to separate the gate pattern into individual gates **after** the formation of the epitaxial layer. *Shin* teaches the opposite—*Shin*'s method for fabricating source-drain regions teaches performing all of the steps, including the detailed and complex formation of epitaxial layers, after the individual gates were already formed. Thus, incorporating this method into *Mandelman* would result in the epitaxial layers being formed after the individual gates were formed. Accordingly, in the proposed combination, the slot would be formed to separate the gate pattern into individual gates **before** the formation of any epitaxial layer, not after.

82. And *Chong* cannot save Ground 4 for all the same reasons it cannot save Ground 2, including:

- (1) *Chong* cannot provide the missing but required order of forming of the slot after the forming epitaxial layer because *Chong* indisputably does not disclose or suggest forming a slot at all, much less doing so after forming the epitaxial layer.
- (2) *Chong* admittedly and explicitly teaches creating its individual gates **before** then forming its source/drain regions and alleged epitaxial layers. (Petition at 27; EX1007 at ¶¶ 28-31, 38, 40-44). Thus, if

creating those *Chong* gates by forming a notch to separate gate pattern into individual gates (as taught in *Mandelman*) was just a design choice as the Petition alleges (Petition at 73), then applying that design choice to *Chong* would result in the slot being formed to separate the gate pattern into individual gates **before** the formation of the alleged epitaxial layer, **not after** as required by the claims.

83. For each and any of the foregoing reasons, Grounds 3 and 4 fail to demonstrate invalidity, along with Grounds 1 and 2.

Dated: August 15, 2025



Joseph C. McAlexander, III

PROFESSIONAL SUMMARY

Currently a Registered Professional Engineer (#79454) and recognized as an inventor on 31 US and a number of foreign patents, I am President of M^cAlexander Sound, Inc., and the Managing Director of M^cAlexander Sound Pte Ltd. I have focused my expertise to support a number of clients in product, process, and operations analysis and investigation. Fifty-two years of experience in microcircuit and semiconductor technologies has developed my skills in areas of circuit design and analysis, device fabrication and assembly, testing, marketing, control system design and analysis, manufacturing operations and respective areas of quality, reliability, and defect / failure analysis. I am also the President and CEO of MDFHoldings, Inc., an IP holding company currently engaged in the field of GPS Tracking, and was formerly, among others, a Manager with QM Partners, LP, supporting clients in IP management and licensing. I have:

- designed and managed development, testing, and evaluation of devices including Dynamic Random Access Memories (DRAMs), Static Random Access Memories (SRAMs), Charge Coupled Devices (CCDs), Shift Registers (SRs), and functional circuits including I/O buffers for address and data, decoders, clocks, sense amplifiers, fault tolerant, parallel-to-serial data paths for video applications, level shifters, converters, pumps, and logic, as well as wireless communication systems and MEMs applications;
- designed, built, and managed 4 physical / chemical analysis laboratories to assess cause of defect and reliability of products, including nanostructure integrated circuits, systems, and product packaging;
- managed operations including engineering, training, and quality assurance for device fabrication, assembly, test, analysis, and reliability assessment, as well as manufacturing control, each of which involved both volatile and non-volatile memory; testing, analysis, and control involving use of mechanical calibration and measuring equipment, including optical, scanning e-beam, IR, capacitive, and laser using phase contrast and Fast Fourier Transform (FFT) for High Aspect Ratio Inspection (HARI) applications; audio and video system design and installation;
- taught courses in solid state device physics, integrated circuit design, integrated circuit fabrication, and statistical control;
- provided expert services, investigating both process and design technologies of various devices (microprocessor and controller, memory, programmable logic, card, tag, module, mixed signal, custom, and other), systems (PC and peripheral, computer, control, laser measurement, switch, architecture, software, and other), and consumer products (medical, TV, telephone, VCR, facsimile, copier, lighting, game, and other);
- provided nuclear radiation hardness testing services for military and space clients; and

PROFESSIONAL SUMMARY

- managed the design and installation of audio sound and video systems for private and commercial enterprises.

From 1986-1990, I was Executive Vice President of EPI Technologies, Inc., prior to joining the staff at Cochran Consulting, Inc. where I served as senior managing consultant from 1991-2002. From 1972 to 1986, I was employed by Texas Instruments Incorporated.

EXPERIENCE PROFILE

1988-present

McAlexander Sound, Inc. (McASI) - Richardson, TX
President

- o System, Product, and Process investigation, expert witness services for protection of intellectual property;
- o Patent portfolio development and valuation;
- o Product liability and insurance claim investigation, expert witness services for matters involving such claims;
- o Quality Systems consulting and engineering;
- o Radiation Hardness Testing Technical Representative;
- o Acoustic system design/installation
- o Technical Advisor in High Aspect Ratio and Surface Contour Measurement using Direct-to-Digital Holography.

2005-present

McAlexander Sound Pte Ltd - Singapore
Managing Director

- o System, Product, and Process investigation, expert witness services for protection of intellectual property;
- o Patent portfolio development and valuation;
- o Contract consultation;
- o Not assigned any patents and is not engaged in any IP related licensing or litigation activities.

2002-present

MDFHoldings, Inc. – Las Vegas, NV
CEO

- o IP holding and licensing company;
- o Assigned U.S. Patent Nos. 7,340,260 and 7,657,265 and EP 1 557 058 B1, each related to an object locating system;
- o Has not been and is not engaged in any IP related litigation or licensing activities.

2006-2020

QM Partners, L.P. – Texas
Manager

- o Management of development, licensing, prosecution and exploitation of assigned intellectual property;
- o Not assigned any patents and is not engaged in any IP related licensing or litigation activities.

EXPERIENCE PROFILE (continued)

2006-2020

Guardian Technologies, LLC – Texas
Manager

- o IP holding and licensing company;
- o Litigated U.S. Patent No. 5,657,076 related to security surveillance 2009-2011 (patent expired 2015);
- o Assigned U.S. Patent No. 8,334,775 related to RFID tracking (reassigned 2020 to personal);
- o Not engaged in any IP related licensing or litigation activities.

2006-2020

Appropriate Holdings, LLC – Delaware
Manager

- o IP holding company;
- o Not assigned any patents, has not been and is not engaged in any IP related licensing or litigation activities.

1996-2010

RMC Management, LLP - Plano, TX
Partner

- o Asset management.

1991-2002

Cochran Consulting, Inc. (CCI) - Richardson, TX
Managing Consultant

- o System, Product, and Process investigation, expert witness services for protection of intellectual property;
- o Design, process, and product reliability;
- o Defect and failure analysis.

1986-Nov'90

EPI Technologies, Inc. - Richardson, TX
Executive Vice President and Company Officer

- o Managed Advanced Technology Div., QA, and Engineering, including software program development;
- o Developed strategic, space/energy market growth plans;
- o Negotiated the acquisition of and managed a radiation company;
- o Designed and managed physical analysis, radiation effects, and environmental stress laboratories, including optical and e-beam measurement;
- o Achieved > 30% annual revenue growth and profitability for each laboratory the first 12 months;

EXPERIENCE PROFILE (continued)

- o Product and Process investigation services for protection of intellectual property.

1972 – 1986 **Texas Instruments, Inc.** - Dallas/Houston, TX; Singapore

'84 - '86 **Quality/Reliability Assurance Manager, TI Dallas** Advanced DRAM semiconductor wafer fabrication facility

- o Developed/implemented on-line, computerized SPC software tools for dimensioning analysis and control and pattern recognition;
- o Coordinated people development, design-of-experiments;
- o Managed chemical and physical analysis laboratories;
- o Implemented control systems to assure product, process, material, equipment, and facility compliance, including Cost of Quality analysis.

'82 - '84 **Quality/Reliability Assurance and Engineering Manager, TI Singapore** assembly/test facility

- o Developed, implemented, and operated an effective Quality/Reliability Assurance program for assembly processing including optical pattern recognition for equipment registration;
- o Supervised 225 people for 7 day/week operation, including QRA, Computer Systems software development, and Training;
- o Trained engineers in Solid State Physics, device fabrication, and statistical process control.

'81 - '82 **Engineering Operations Manager, TI Houston**

- o Managed DRAM memory product cost center;
- o Responsible for division test software generation, product assembly and test quality / yield, cost reduction and quality improvement;
- o Provided technical customer interface for marketing;
- o Coordinated TI Singapore engineering test/assembly.

'79 - '81 **Product Engineering Manager, TI Houston**

- o Responsible for yield improvement, technical customer interface, quality improvement, design evaluation, and device characterization for DRAM and CCD products;
- o Developed device specifications and test software.

EXPERIENCE PROFILE (continued)

'72 - '79

Design Section Manager / Engineer, TI Houston

- o Responsible for design and development, process compatibility, production introduction of Dynamic Ram products;
- o Activities included electrical and physical layout, SPICE model simulation, test program generation, and product implementation for MOS Dynamic Ram products.

1969 - 1972

U. S. Army - Coventry, Rhode Island; Seoul, Korea
Captain, Air Defense Artillery

- o Served one year as Communications Officer in Korea;
- o Served two years as Tactical Officer, New England Defense.

ORGANIZATIONS, PUBLICATIONS, EDUCATIONPROFESSIONAL ORGANIZATIONS AND AWARDS

- 1 - Institute of Electrical and Electronics Engineers, Inc. (IEEE), Senior Member. Societies:
Computer, Electron Devices, Solid State Circuits
- 2 - Licensing Executives Society (LES)
- 3 - National Society of Professional Engineers
- 4 - Texas Board of Professional Engineers, Registered License #79454
- 5 - American Society of Civil Engineers
- 6 - Architectural Engineering Institute
- 7 - 2000/2001 Nationwide Register's Who's Who in Executives and Businesses
- 8 - 1996/1997 Strathmore's Who's Who Registry of Business Leaders

PUBLICATIONS

- 1- NUS Proceedings of Engineering Convention '83, Aug '83, pgs. 139-142, The Memory Challenge.
- 2- Archives of Biochemistry and Biophysics, Dec'81, Vol. 212, No. 2, Equilibrium Constants under Physiological Conditions for the Reactions of D-3-Phosphoglycerate Dehydrogenase and L-Phosphoserine Aminotransferase.
- 3- International Electron Devices Meeting, Dec '79, pgs. 355-357, Sub 100ns 16K x 1 MOS Dynamic RAM Using a Grounded Substrate.

EDUCATION PROFILE

1980 - 1985	Taught Solid State Device Physics, Semiconductor Processing, Circuit Design Techniques, and Statistical Quality Control Methods Effectiveness Training and Japanese Manufacturing Techniques, Participative Problem Solving courses
1975 - 1976	1.5 years Graduate Study in Neural Science, the University of Texas Graduate School of Biomedical Science
1965 - 1969	BSEE, North Carolina State University

PATENTS (US-31, Foreign-8)

4,239,993	(1980) High Performance Dynamic Sense Amplifier with Active Loads
4,280,070	(1981) Balanced Input Buffer Circuit for Semiconductor Memory
4,288,706	(1981) Noise Immunity in Input Buffer Circuit for Semiconductor Memory
4,370,575	(1983) High Performance Dynamic Sense Amplifier with Active Loads
4,418,293	(1983) High Performance Dynamic Sense Amplifier with Multiple Column Outputs
4,533,843	(1985) High Performance Dynamic Sense Amplifier with Voltage Boost for Row Address Lines
4,543,500	(1985) High Performance Dynamic Sense Amplifier Voltage Boost for Row Address Lines
4,543,501	(1985) High Performance Dynamic Sense Amplifier with Dual Channel Grounding Transistor
4,748,349	(1988) High Performance Dynamic Sense Amplifier with Voltage Boost for Row Address Lines
6,172,640 B1	(2001) Pet Locator
6,236,358 B1	(2001) Mobile Object Locator
6,421,001 B1	(2002) Object Locator
6,441,778 B1	(2002) Pet Locator
6,480,147 B2	(2002) Portable Position Determining Device
6,518,919 B1	(2003) Mobile Object Locator
6,771,213 B2	(2004) Object Locator
6,859,171 B2	(2005) Mobile Object Locator

PATENTS (continued)

7,113,126 B2	(2006) Portable Positioning Determining Device
7,179,674 B2	(2007) Bi-Directional Released-Beam Sensor
7,209,075 B2	(2007) Mobile Object Locator
7,324,044 B2	(2008) Object Locator
7,336,227 B2	(2008) Portable Position Determining Device
7,340,260 B2	(2008) System and Method for Tracking the Location of Multiple Mobile Radio Transceiver Units (assigned to MDFHoldings, Inc.)
7,353,706 B2	(2008) Weighted Released-Beam Sensor
7,397,097 B2	(2008) Integrated Released Beam Layer Structure Fabricated in Trenches and Manufacturing Method Thereof
7,564,405 B2	(2009) Object Locator
7,657,265 B2	(2010) System and Method for Tracking the Location of Multiple Mobile Radio Transceiver Units (assigned to MDFHoldings, Inc.)
7,760,137 B2	(2010) Portable Positioning Determining Device
7,764,228 B2	(2010) Portable Positioning Determining Device
7,989,906 B2	(2011) Bi-Directional released-Beam Sensor
8,334,775 B2	(2012) RFID-Based Asset Security and Tracking System, Apparatus and Method (assigned to personal)
JP 55-053640 B4	(1980) Defect Resistant Semiconductor Memory Cell
JP 59-044720 B4	(1984) Semiconductor High Speed Read/Write Memory Unit
DE2935121 C2	(1980) Clock Voltage Generator for Semiconductor Memory with Reduced Power Dissipation
DE3043651 A1	(1981) Clock Voltage Generator for Semiconductor Memory with Reduced Power Dissipation

PATENTS (continued)

- GB2032211 B2 (1980) High Performance Dynamic MOS Read/Write Memory
- EP 1 557 058 B1 (2011) System and method for tracking the location of multiple mobile radio transceiver units (assigned to MDFHoldings, Inc.)
[States: AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PT RO SE SI SK TR]
- EP 1 676 809 B1 (2010) Weighted released-beam sensor
[States: DE FR GB IT]
- EP 1 676 810 B1 (2010) Bi-directional released-beam sensor
[States: DE FR GB IT]

CASES

Cases over at least the past 7 years, either active or closed, in which I have signed a Protective Order, have testified as an expert either at a trial, hearing, or deposition, or have submitted statements / opinions by declaration, affidavit, or report, are:

CASE¹	CASE NUMBER	LOCATION	YEAR	TYPE²
Kangaroo Media* v. Immersion Entertainment (*firm: Kenyon & Kenyon)	2:12-cv-00382-JFC, 2:14-cv-01536-JFC	WD PA	2012 - 2016	P,t
(Audio/Video Entertainment System patent)				
Securus* v. Global (*firm: Gruber)	3:13-CV-03009-K	ND TX	2014 - 2017	P,t
(Patents related to telecom systems)				
Global v. Securus* (*firm: Gruber)	3:14-CV-0829-K, 3:13-CV-00713-JRS	ND TX / ED VA	2014 - 2017	P
(Patents related to telecom systems)				
Advanced Audio Devices* (*firm: Clark Hill PLC)	IPR2014-01155	USPTO PTAB	2014 - 2016	P,t
(Patent 7,289,393 related to music jukebox)				
Advanced Audio Devices* (*firm: Clark Hill PLC)	IPR2014-01156	USPTO PTAB	2014 - 2016	P,t
(Patent 7,817,502 related to a personal digital stereo player)				
Advanced Audio Devices* (*firm: Clark Hill PLC)	IPR2014-01157	USPTO PTAB	2014 - 2016	P,t
(Patent 7,933,171 related to a personal digital stereo player)				
Advanced Audio Devices* (*firm: Clark Hill PLC)	IPR2014-01158	USPTO PTAB	2014 - 2016	P,t
(Patent 8,400,888 related to a personal digital stereo player)				

¹ * = Client

² P=Patent, C=Contract, ©=Copyright, TS=Trade Secret, AT=Antitrust; CA=Class Action; t=testified, TH=Trial/Hearing

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
One-E-Way* v. Sony, Sennheiser, BlueAnt, Creative Tech, Beats, Jawbone, Jabra (*firm: Knobbe Marten, Olson & Bear)	337-TA-943	ITC (Pender)	2014 - 2018	P,t
(Patents related to bluetooth configured headphones)				
Omega* v. Calamp	6:13-cv-1950-Orl-31DAB	MD, FL	2015 - 2016	P,t,TH
(Patents related to vehicular control systems and tracking)				
AVM* v. Intel (*firm: Boies, Schiller & Flexner)	1:15-cv-00033-RGA	DE	2015 - 2016	P,t,TH
(Patent related to dynamic logic circuits)				
Allure Energy* v. Honeywell (*firm: McKool Smith)	1:15-cv-00079-RP	WDTX, Austin	2015 - 2017	P
(Smart Thermostat)				
IV* v. Toshiba (*firm: Desmarais)	13-cv-453-SLR-SRF	DE	2015 - 2017	P,t,TH
(NAND Flash)				
IMS v. Micron* (*Weil Gotchal/ Orrick)	1:14-cv-01480-RGA	DE	2015 - 2022	P,t
(Patents related to flash memory)				
Honeywell v. Allure* (*firm: Dickinson Wright)	IPR201501248, 01251,01253	USPTO PTAB	2015 - 2017	P
(Smart Thermostat)				
Blitzsafe* v Honda (*firm: Brown Rudnick)	2:15-cv-01274-JRG-RSP	EDTX, Marshall	2015 - 2017	P,t
(Patents related to audio device integration systems)				
Blitzsafe* v Hyundai (*firm: Brown Rudnick)	2:15-cv-01275-JRG-RSP	EDTX, Marshall	2015 - 2017	P,t
(Patents related to audio device integration systems)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Blitzsafe* v Nissan (*firm: Brown Rudnick)	2:15-cv-01276- JRG-RSP	EDTX, Marshall	2015 - 2017	P,t
(Patents related to audio device integration systems)				
Blitzsafe* v Toyota (*firm: Brown Rudnick)	2:15-cv-01277- JRG-RSP	EDTX, Marshall	2015 - 2017	P,t
(Patents related to audio device integration systems)				
Blitzsafe* v VW (*firm: Brown Rudnick)	2:15-cv-01278- JRG-RSP	EDTX, Marshall	2015 - 2017	P,t
(Patents related to audio device integration systems)				
3rd Eye Surveillance* v Stealth (*firm: Kennedy Law)	6:14-cv-00162 JDL	EDTX, Tyler	2015 - 2016	P
(Patents related to real-time image processing to response agency)				
3rd Eye Surveillance* v Vision Video (*firm: Kennedy Law)	6:14-cv-00161- JDL	EDTX, Tyler	2015 - 2016	P
(Patents related to real-time image processing to response agency)				
3rd Eye Surveillance* v Ft Worth / e-Watch (*firm: Kennedy Law)	6:14-cv-00725	EDTX, Tyler	2015 - 2017	P,t,TH
(Patents related to real-time image processing to response agency)				
3rd Eye Surveillance* v United States (*firm: Kennedy Law)	1:15-cv-00501- CFL	Court of Federal Claims, DC	2015 -	P,t,TH
(Patents related to real-time image processing to response agency)				
Hitachi v TPV* (*firm: O'Melveny & Myers)	2:14-cv-1121- JRG-RSP	EDTX, Marshall	2015 - 2016	P
(Patent related to LCD power and signal board arrangement)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Nidec Motor v Broad Ocean Motor* (*firm: Locke Lord)	2:15-cv-00443	EDTX, Marshall	2016	P
(Patent related to blower motor control for HVAC)				
TracBeam* v T-Mobile (*firm: Dovel & Luner)	6:14-cv-678-RWS	EDTX, Tyler	2016	P,t
(Patents related to geographic location estimates)				
SMS v Emerson* (*firm: Davidson Berquist)	2:15-cv-00032-RWS-RSP	EDTX, Marshall	2016	P
(Patent related to a method of monitoring a protected space)				
Prong v Sorias* (*firm: Gottlieb, Rackman & Reisman)	IPR2015-01317	USPTO PTAB	2016	P
(Patent related to attachable mobile charger)				
Skyline Software Systems v Duane Morris* (*firm: Venable)	2015-08868	Circuit Court Fairfax County	2016	P
(3D mapping technology)				
SignalQuest v Oncque* (*firm: Duane Morris)	11-cv-00392-JL	NH	2016	P
(Patents related to vibration switches)				
TiVo v Samsung* (*firm: Fish & Richardson)	2:15-CV-1503	EDTX, Marshall	2016	P
(Patent related to multimedia signal processing)				
Richtek v uPi* (*firm: Hogan Lovells)	C 09-05659 WHA LB	NDCA, SF	2016	P
(Patents related to converter channel current balance and PWM circuit)				
Paice* v VW, Porsche, Audi (*firm: Fish & Richardson)	337-TA-998	ITC	2016 – 2017	P
(Patents related to hybrid vehicle technology)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Biosonix v Hydrowave* (*firm: Bradley)	4:16-cv-00139-RC	EDTX, Sherman	2016 - 2017	P
(Patent related to underwater sound listening and generation)				
Univ of S FL* v Fujifilm (*firm: Dickinson Wright)	8:16-cv-01194-MSS-TGW	MDFL, Tampa	2017	P
(Patent related to Workstation Interface – Digital Mammography)				
Univ of S FL * v BRIT (*firm: Dickinson Wright)	8:16-cv-03109-MSS-TGW	MDFL, Tampa	2017	P,t
(Patent related to Workstation Interface – Digital Mammography)				
Nokia v Apple	337-TA-1038	ITC	2017	P
(Patent related to controllable bias mode oscillator)				
Univ of IL v Micron* (*firm: Fish & Richardson)	2:11-cv-02288-SLD-JAG	CDIL, Rock Falls	2017	P, C
(Patents and contract related to use of deuterium in semiconductor processing)				
ZiiLabs v AMD* (*firm: O'Melveny & Myers)	337-TA-1037	ITC-Shaw	2017	P
(Patents related to graphics processors)				
MTL* v Sandisk (*firm: Tensegrity)	337-TA-1034	ITC-Lord	2017	P,t
(Patents related to flash memory)				
Razberi v Dynacolor* (*firm: McDole Williams)	01-16-0003-3734	AAA	2017 - 2018	C,TS,t, TH
(Arbitration related to contractual obligations)				
Seed Spring* v Microsoft (*firm: Dovel)	6:17-cv-427-RWS	EDTX, Tyler	2017	P
(Patents related to Wirelss Location)				
TracBeam* v Microsoft (*firm: Dovel)	6:17-cv-426-RWS	EDTX, Tyler	2017	P
(Patents related to Wirelss Location)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
TracBeam* v Cisco (*firm: Dovel)	6:17-cv-525-RWS	EDTX, Tyler	2017 - 2018	P
(Patents related to Wirelss Location)				
Arris* v Sony (*firm: Fish & Richardson)	337-TA-1060	ITC-Lord	2017	P,t
(Patent related to Broadcast Signals)				
Vivint* v Alarm.com (*firm: Weil)	2:15-cv-00392- CW-BCW	UT	2017 - 2023	P,t
(Patents related to Electronic Message Delivery)				
Blitzsafe* v Bosch (*firm: Brown Rudnick)	2:17-cv-00105- JRG	EDTX, Marshall	2017 - 2019	P,t
(Patents related to audio device integration systems)				
Blitzsafe* v Daimler & Mercedes (*firm: Brown Rudnick)	2:17-cv-00422- JRG	EDTX, Marshall	2017 - 2019	P
(Patents related to audio device integration systems)				
Blitzsafe* v BMW (*firm: Brown Rudnick)	2:17-cv-00418- JRG	EDTX, Marshall	2017 - 2019	P
(Patents related to audio device integration systems)				
Blitzsafe* v Mazda (*firm: Brown Rudnick)	2:17-cv-00423- JRG	EDTX, Marshall	2017 - 2019	P
(Patents related to audio device integration systems)				
Blitzsafe* v Mitsubishi (*firm: Brown Rudnick)	2:17-cv-00430- JRG	EDTX, Marshall	2017 - 2019	P
(Patents related to audio device integration systems)				
Blitzsafe* v Subaru (*firm: Brown Rudnick)	2:17-cv-00421- JRG	EDTX, Marshall	2017 - 2019	P,t
(Patents related to audio device integration systems)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Blitzsafe* v Tata & Jaguar (*firm: Brown Rudnick)	2:17-cv-00424-JRG	EDTX, Marshall	2017 - 2019	P
(Patents related to audio device integration systems)				
Blitzsafe* v Volvo (*firm: Brown Rudnick)	2:17-cv-00420-JRG	EDTX, Marshall	2017 - 2019	P
(Patents related to audio device integration systems)				
AGIS* v Huawei (*firm: Brown Rudnick)	2:17-00513-JRG	EDTX, Marshall	2017 - 2018	P,t
(Patents related to Patents related to interactive remote communications)				
AGIS* v HTC (*firm: Brown Rudnick)	2:17-00514-JRG	EDTX, Marshall	2017 - 2019	P,t
(Patents related to Patents related to interactive remote communications)				
AGIS* v LG (*firm: Brown Rudnick)	2:17-00515-JRG	EDTX, Marshall	2017 - 2019	P,t
(Patents related to Patents related to interactive remote communications)				
AGIS* v Apple (*firm: Brown Rudnick)	2:17-00516-JRG	EDTX, Marshall	2017 - 2019	P,t
(Patents related to Patents related to interactive remote communications)				
AGIS* v ZTE (*firm: Brown Rudnick)	2:17-00517-JRG	EDTX, Marshall	2017 - 2019	P
(Patents related to Patents related to interactive remote communications)				
Arya v Dufossat* (*firm: Robert Sueiro)	4:16-cv-03595	SDYX, Houston	2017 -	TS,C,t
(Dispute related to Trade Secrets)				
Seven Networks v Samsung* (*firm: Fish & Richardson)	2:17-cv-00441-JRG	EDTX, Marshall	2017 - 2018	P,t
(Patents related to Power Management of Mobile Networks)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
ZF Micro Solutions* v. Tat Investment (*firm: Berger)	1-09-CV-134970	Santa Clara County	2018	C,t,TH
(Business tort, unfair practice)				
Univ of S FL* v Fujifilm (*firm: Dickinson Wright)	3:18-cv-00215-AVC	Connecticut	2018	P,t
(Patent related to Workstation Interface – Digital Mammography)				
Univ of S FL* v BRIT (*firm: Dickinson Wright)	3:18-CV-0250-K	NDTX, Dallas	2018 - 2019	P,t
(Patent related to Workstation Interface – Digital Mammography)				
Cypress Insurance v Hynix* (*firm: Bird Marella)	C17-467 RAJ	WDWA, Seattle	2018 - 2019	C,t,TH
(Contract dispute related to product delivery)				
Belliveau* v BARCO (*firm: McKool)	1:17-CV-00379-SS	WDTX, Austin	2018	C,t
(Patent portfolio licensing dispute)				
MPS* v Intersil (*firm: Perkins)	16-1125-LPS	DE	2018 - 2021	TS,t
(Trade Secret dispute)				
GoGo v Squire Patton Boggs* (*firm: Cozen O'Connor)	2016-L-007789	Cook County, IL	2018 - 2019	P
(Patent Malpractice claim)				
X2Y* v Intel (*firm: Dovel)	3:18-cv-1394-HZ	DOR, Portland	2018 - 2020	P
(Patents related to package layer metalization)				
Power Integration* v ON Semi (*firm: Fish & Richardson)	5:16-cv-06371-BLF	NDCA, San Jose	2019	P,t
(Patents related to power converter regulation)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
ON Semi v Power Integration* (*firm: Fish & Richardson)	1:17-cv-00247-LPS-CJB	DE	2019	P,t
(Patents related to power converter regulation)				
Semcon* v Amazon (*firm: Brown Rudnick)	2:18-CV-00192-JRG	EDTX, Marshall	2019	P
(Patent related to Adaptive Power Control)				
Semcon* v Asustek (*firm: Brown Rudnick)	2:18-CV-00193-JRG	EDTX, Marshall	2019	P
(Patent related to adaptive power control)				
Semcon* v Kyocera (*firm: Brown Rudnick)	2:18-CV-00197-JRG	EDTX, Marshall	2019	P
(Patent related to adaptive power control)				
Innovation Sciences* v Amazon (*firm: Davidson Berquist)	4:18-cv-00474-ALM	EDTX, Sherman	2019 - 2020	P,t,TH
(Patent related to Internet communication)				
Innovation Sciences* v HTC (*firm: Davidson Berquist)	4:18-cv-00476-ALM	EDTX, Sherman	2019 - 2020	P,t
(Patent related to Internet communication)				
Innovation Sciences* v Resideo (*firm: Davidson Berquist)	4:18-cv-00475-ALM	EDTX, Sherman	2019 - 2020	P,t
(Patent related to Internet communication)				
Innovation Sciences* v Vector (*firm: Davidson Berquist)	4:18-cv-00477-ALM	EDTX, Sherman	2019	P
(Patent related to Internet communication)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
CXT* v JC Penny (*firm: Brown Rudnick)	2:18-cv-00171- RWS-RSP (lead) 2:18-CV-233- RWS-RSP	EDTX, Marshall	2019 - 2020	P,t
(Patents related to storage management and information distribution)				
Photonics* v Lenovo (*firm: Brown Rudnick)	1:18-cv-00489- MN	DE	2019	P
(Patents related to GDS-II Layout)				
Quest NetTech Corp* v Apple (*firm: Brown Rudnick)	2:19-CV-00118- JRG	EDTX, Marshall	2019 - 2020	P
(Patent related to programmable credit card system)				
Pilot, Inc.* v Schumacher (*firm: Bradford)	1:19-cv-05982- EEC	NDIL, Eastern Div	2019 - 2921	P
(Patents related to battery chargers)				
Vocalife* v Amazon (*firm: Brown Rudnick)	2:19-cv-00123- JRG	EDTX, Marshall	2019 - 2020	P,t,TH
(Patent related to microphone array)				
Semcon* v Vuitton (*firm: Brown Rudnick)	2:19-CV-00122- JRG	EDTX, Marshall	2019	P,t
(Patent related to adaptive power control)				
Semcon* v Shenzhen (*firm: Brown Rudnick)	2:18-CV-00196- JRG	EDTX, Marshall	2019	P,t
(Patent related to adaptive power control)				
Ultravision* v GoVision (*firm: Brown Rudnick)	2:18-cv-00100- JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				
Ultravision* v Shenzhen (*firm: Brown Rudnick)	2:18-cv-00103- JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Ultravision* v Aoto (*firm: Brown Rudnick)	2:18-cv-00113-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				
Ultravision* v Leyard (*firm: Brown Rudnick)	2:18-cv-00102-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				
Ultravision* v NEC (*firm: Brown Rudnick)	2:18-cv-00150-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to Modular Display Panels and LED lighting)				
Ultravision* v Prismaflex (*firm: Brown Rudnick)	2:18-cv-00108-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				
Ultravision* v Unilumin (*firm: Brown Rudnick)	2:18-cv-00116-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				
Ultravision* v Yaham (*firm: Brown Rudnick)	2:18-cv-00118-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				
Ultravision* v Absen (*firm: Brown Rudnick)	2:18-cv-00112-JRG-RSP	EDTX, Marshall	2019	P
(Patents related to modular display panels and LED lighting)				
Birchett* v City of Fort Worth (*firm: Kennedy Law)	DC-19-06941	Dallas County	2019	C,t
(Whistleblower)				
Innovation Sciences* v HTC (*firm: Davidson Berquist)	337-TA-1180	ITC	2020 - 2021	P,t
(Patent related to wireless communication)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Innovation Sciences* v Resideo (*firm: Davidson Berquist)	337-TA-1180	ITC	2020	P,t
(Patent related to Internet communication)				
CXT* v Neiman Marcus (*firm: Brown Rudnick)	2:19-cv-00270-RWS-RSP	EDTX, Marshall	2020	P
(Patents related to storage management and information distribution)				
CXT* v General Nutrition (*firm: Brown Rudnick)	2:19-cv-00271-RWS-RSP	EDTX, Marshall	2020	P
(Patents related to storage management and information distribution)				
CXT* v Steven Madden (*firm: Brown Rudnick)	2:19-cv-00272-RWS-RSP	EDTX, Marshall	2020	P
(Patents related to storage management and information distribution)				
Consolidated* v Amazon (*firm: Devlin Law)	1:19-cv-01715-RGA	DE	2020 – 2021	P,t
(Patents related to on-line shopping)				
Consolidated* v Ford (*firm: Devlin Law)	1:19-cv-01916-RGA	DE	2020 - 2021	P,t
(Patents related to on-line shopping)				
Consolidated* v JC Penney (*firm: Devlin Law)	1:19-cv-01918-RGA	DE	2020 - 2021	P,t
(Patents related to on-line shopping)				
Consolidated* v Ebay (*firm: Devlin Law)	1:19-cv-01580-RGA	DE	2020 - 2021	P,t
(Patents related to on-line shopping)				
Consolidated* v Walmart (*firm: Devlin Law)	1:19-cv-01581-RGA	DE	2020 - 2021	P,t
(Patents related to on-line shopping)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Semcon* v TCT Mobile (*firm: Brown Rudnick)	2:18-CV-00194-JRG	EDTX, Marshall	2020	P
(Patent related to adaptive power control)				
BNR v Samsung* (*firm: Fish & Richardson)	2:19-cv-00286-JRG	EDTX, Marshall	2020	P
(Patents related to portable communication devices)				
AGIS* v Google (*firm: BRudnick, Fabricant)	2:19-cv-00361-JRG	EDTX, Marshall	2020 - 2022	P,t
(Patents related to interactive remote communications)				
AGIS* v Waze (*firm: BRudnick, Fabricant)	2:19-cv-00359-JRG	EDTX, Marshall	2020 - 2022	P,t
(Patents related to interactive remote communications)				
Burke* v City of Fort Worth (*firm: Kennedy Law)	DC-19-07239	Dallas County	2020	C,t
(Whistleblower)				
Infinera v Oyster Optics* (*firm: Davidson Berquist)	IPR2020-00325	PTAB	2020	P,t
(Patent related to fiber optic telecommunications)				
Blitzsafe* v GM (*firm: Fabricant)	2:19-cv-00377-JRG	EDTX, Marshall	2020	P,t
(Patents related to audio device integration systems)				
Blitzsafe* v FCA (*firm: Fabricant)	2:19-cv-00378-JRG	EDTX, Marshall	2020	P,t
(Patents related to audio device integration systems)				
Kuster v Western Digital* (*firm: Shearman & Sterling)	6:20-cv-00563	WDTX, Waco	2020	P,t
(Patent related to memory stack storage)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
TruSun* v Eaton (*firm: Duane Morris)	6:19-cv-00656- ADA	WDTX, Waco	2020 - 2022	P,t
(Patent related to a light-generating system)				
RJR v PMI* (*firm: Latham Watkins)	1:20-cv-00393- LO-TCB	EDVA, Alexandria	2020 - 2022	P,t,TH
(Patents related to e-cigarette controls)				
Koss* v Apple et al (*firm: K L Gates)	6:20-cv-00665	WDTX, Waco	2020 - 2022	P,t
(Patents related to Wireless Headphones)				
Koss* v Bose (*firm: K L Gates)	6:20-cv-00661	WDTX, Waco	2020	P
(Patents related to Wireless Headphones)				
Ipcom v Sprint et al (Nokia*) (*Alston Bird)	2:20-cv-321	EDTX, Marshall	2020 - 2022	P
(Patents related to CDMA communication)				
Ipcom v Verizon et al (Nokia*) (*Alston Bird)	2:20-cv-323	EDTX, Marshall	2020 - 2022	P
(Patents related to CDMA communication)				
Pilot* v CarKu (*firm: Bradford / Sheridan)	7131799991	Amazon Arbitration	2020	P,t
(Patent related to jump starters)				
MPS* v Meraki (*firm: Perkins Coie)	6:2020cv00876- ADA	WDTX, Waco	2020 - 2022	P,TS,C
(Patents related to synchronous rectifier control)				
AGIS* v Uber (*firm: Fabricant)	2:21-cv-00026- JRG-RSP)	EDTX, Marshall	2021	P
(Patents related to interactive remote communications)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
AGIS* v WhatsApp (*firm: Fabricant)	2:21-cv-00029- JRG-RSP)	EDTX, Marshall	2021	P
(Patents related to interactive remote communications)				
One E-Way* v Apple (*firm: Knobbe Martin)	2:20-cv-06339- JSK-PD	CDCA	2021 - 2023	P,t
(Patent related to Bluetooth Headphones)				
BMW v Omega Patents* (*firm: Allen Dyer)	IPR2021-00181	PTAB	2021 -	P,t
(Patent related to remote start)				
Pilot* v The NOCO Co (*firm: Bradford / Sheridan)	2:20-cv-01452- SRB	AZ	2021 - 2023	P,t
(Patents related to auto chargers)				
Express Mobile* v Atlassian (*firm: Mololamken)	6:20-cv-00805- ADA	WDTX, Austin	2021	P
(Patents related to browser-based web site generation)				
AGIS* v Lyft (*firm: Fabricant)	2:21-cv-00024- JRG-RSP	EDTX, Marshall NDCA	2021 - 2022	P
(Patents related to interactive remote communications)				
AGIS* v T-Mobile (*firm: Fabricant)	2:21-cv-00072- JRG-RSP	EDTX, Marshall	2021	P
(Patents related to interactive remote communications)				
Altria* v RJR (*firm: Weil Gotshal)	1:20-cv-00472	MDNC	2021 - 2022	P,t,TH
(Patents related to e-cig)				
One E-Way* v Apple (*firm: Knobbe Martin)	IPR2021-00283 IPR2021-00286	PTAB	2021 - 2022	P,t
(Patent related to Bluetooth Headphones)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Altria* v RJR (*firm: Weil Gotshal)	IPR2021-00650 IPR2021-00652 IPR2021-00725 IPR2021-00744 IPR2021-00745 IPR2021-00746 IPR2021-00747 IPR2021-00793	PTAB	2021 - 2022	P,t,TH
(Patents related to e-cig control)				
Kiwi Connection* v Anker (*firm: Bradford)	8519300821	Amazon Arbitration	2021	P,t
(Patent related to bidirectional connector)				
Kiwi Connection* v JBL (*firm: Bradford)	8674855301	Amazon Arbitration	2021	P,t
(Patent related to bidirectional connector)				
Platform Science v Omnitracs* (*firm: Kirkland & Ellis)	IPR2020-0187 IPR2020-1517 IPR2020-1518	PTAB	2021 – 2022	P,t
(Patent related to critical event reporting)				
Netlist v Samsung* (*firm: Bird Marella)	8:20-cv-993-MCS	CDCA, Southern	2021	C,t
(Contract dispute)				
Monterey Research* v (*firm: Desmarais)	IPR 2021-00119 IPR 2021-00120 IPR 2021-00172	PTAB	2021 - 2022	P,t
(Patents related to semiconductor processing)				
Apple / Bose v Koss* (*firm: K L Gates)	IPR2021-00255 IPR2021-00297 IPR2021-00305 IPR2021-00381 IPR2021-00592	PTAB	2021 - 2022	P,t
(Patents related to Wireless Headphones)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Vocalife* v Amazon2 (*firm: Fabricant)	2 :20-cv-00401- JRG-RSP	EDTX, Marshall	2021 - 2023	P,t
(Patent related to microphone array)				
Vocalife* v Google (*firm: Fabricant)	2 :21-cv-00124- JRG-RSP	EDTX, Marshall	2021 - 2023	P,t
(Patent related to microphone array)				
Luxshare* v Amphenol (*firm: K L Gates)	IPR2022-00132	PTAB	2021 - 2022	P,t
(Patent related to high performance connector)				
Vervain v Micron* (*firm: Orrick)	6:20-cv-487- ADA	WDTX, Waco	2021 - 2023	P,t
(Patents related to MLC & SLC endurance)				
Express Mobile* v Dropbox (*firm: Mololamken)	3:21-cv-01145	NDCA	2021	P
(Patents related to browser-based web site generation)				
Lexmark v Universal Imaging* (*firm: Allen Dyer)	8:18-cv-1047-T- 17AEP	MDFL, Tampa	2021 - 2023	P
(Patents related to printer cartridge authentication)				
Pilot* v The NOCO Co (*firm: Bradford / Sheridan)	IPR2021-00777 IPR2021-01232 IPR2023-00167 IPR2023-00810	PTAB	2021	P,t
(Patents related to auto chargers)				
Delta T* v MacroAir (*firm: Latham/VedderPrice)	5:20-cv-00728- GW-GJS	CDCA, LA	2022 - 2023	P
(Patents related to fan sensors and control)				
MPS* v Dong & Sheng (*firm: Perkins Coie)	4 :20-cv-6752- JSW	NCCA, Oakland	2022 - 2023	P, TS
(Patents related to synchronous rectifier control)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Vocalife* v Sonos (*firm: Fabricant)	2 :21-cv-00129-JRG	EDTX, Marshall	2022	P,t
(Patent related to microphone array)				
Vocalife* v Bose (*firm: Fabricant)	2 :21-cv-00128-JRG	EDTX, Marshall	2022	P,t
(Patent related to microphone array)				
Enovsys* v T-Mobile (*firm: Eichmann)	2:21-cv-00368-JRG	EDTX, Marshall	2022	P,t
(Patents related to precise location determination and secure disclosure)				
Enovsys* v Verizon (*firm: Eichmann)	2:21-cv-00315-JRG-RSP	EDTX, Marshall	2022	P,t
(Patents related to precise location determination and secure disclosure)				
Lyft v AGIS* (*firm: Fabricant)	5 :21-cv-04653-BLF	NDCA, San Jose	2022 - 2023	P
(Patents related to interactive remote communications)				
Vocalife* v Amazon (*firm: Fabricant)	IPR2021-01331	PTAB	2022	P,t
(Patent related to microphone array)				
MPS* v Meraki (*firm: Perkins Coie)	4:22-cv-01986-JSW	NDCA, Oakland	2022 - 2023	P,TS,C
(Patents related to synchronous rectifier control)				
Signode v Polychem* (*firm: Latham)	1 :22-cv-00519-UNA	DE	2022	P
(Patents related to a strapping apparatus)				
Pilot* v Hulkman (*firm: BRADFORD)	10427111251	Amazon Arbitration	2022	P,t
(Patent related to jump starters)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Netlist v Samsung* (*firm: Fish & Richardson)	2:21-cv-463	EDTX, Marshall	2022 - 2024	P,t,TH
(Patents related to DIMM DDR3 signal timing, power management, and rank multiplication)				
Orange* v Autel (*firm: Sughrue Mion)	2 :21-cv-240	EDTX, Marshall	2022 - 2023	P,t,TH
(Patent related to Tire Pressure Monitoring Systems)				
Bell Power v MPS* (*firm: Perkins Coie)	6 :21-cv-00655-ADA	WDTX, Waco	2022 -	P
(Patents related to power converter/regulator control)				
VPR v Jupiter* (*firm: Noroozi PC)	2:20-CV-02185-DJH	AZ	2023 -	P,t
(Patent related to electronic vape device with air flow sensor)				
Multimodal* v Guangdong (*firm: Fabricant)	2:21-cv-00436-JRG-RSP	EDTX, Marshall	2023	P
(Patents related to communication over a network, call completion)				
Multimodal v ZTE (*firm: Fabricant)	2:21-cv-00437-JRG-RSP	EDTX, Marshall	2023	P
(Patents related to communication over a network, call completion)				
Entropic* v Charter Communications et al. (*firm: K L Gates)	2 :22-cv-00125-JRG	EDTX, Marshall	2022	P
(Patents related to modems and broadband content distribution)				
Oasis Tooling* v Global Foundries U.S. (*firm: Kramer Levin)	22-00312-CJB	DE	2022 - 2024	P,t
(Patents related to chip design process workflow)				
Oasis Tooling* v Siemens Industry Software (*firm: Kramer Levin)	22-00151-CJB	DE	2022 - 2024	P,t
(Patents related to chip design process workflow)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
AGIS* ITC (*firm: Fabricant)	337-TA-1347	ITC	2023	P
(Patents related to Location-Sharing Systems)				
Monterey* v Nanya (*firm: Desmarais)	19-2090-NIQA-LAS	DE	2023 – 2024	P
(Patents directed to semiconductor technology)				
Geotab v Omega* (*firm: Allen Dyer)	IPR2023-00504	PTAB	2023	P,t
(Patent related to multi-vehicle communication)				
Adv Lighting Concepts* v mate (*firm: Munsch)	IPR2023-01264	PTAB	2023	P
(Patent related to LED drivers)				
SitePro* v Waterbridge (*firm: Perkins Coie)	6:23-cv-00115-ADA-DTG	WDTX, Waco	2023	P,TS,C
(Patents and Trade Secrets related to remote delivery control)				
Nanya v Monterey* (*firm: Botos Churchill)	EPR 6,825,526C1 EPR 6,680,516	USPTO	2023	P,t
(Patents directed to semiconductor technology)				
ICPillar* v ARM (*firm: Eichmann)	6_23-cv-00115-ADA-DTG	WDTX, Austin	2023 - 2024	P
(Patents related to computer method for IC design)				
GoTV Streaming v Netflix* (*firm: Wilkie Farr)	EPR 8478245 EPR 8989715	USPTO	2023	P,t
(Patent related to rendering content on a wireless device)				
Greenthread v MPS* (*firm: Perkins Coie)	23-579-RGA	DE	2024	P
(Patents related to semiconductor structure with graded doping)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
MPS* v REED (*firm: Perkins Coie)	23-1155-JFM	DE	2023 -	P,t
(Patent related to bootstrap refresh control)				
Verizon v Omega* (*firm: Allen Dyer)	IPR2023--01162	PTAB	2023 -	P,t
(Patent related to multi-vehicle communication)				
MOSAID v MediaTek* (*firm: Fish & Richardson)	2:23-cv-00129- JRG-RSP	EDTX, Marshall	2023 - 2024	P
(Patents related to IC Power Management)				
GoTV Streaming v Netflix* (*firm: Wilkie Farr)	2 :22-cv-07556- RGK-SHK	CDCA	2023	P
(Patent related to rendering content on a wireless device)				
Lifetime* v Qima (*firm: Fabricant)	2:23-cv-00216- JRG	EDTX, Marshall	2024	P,t
(Patents related to Quality Management)				
Stellar* v Motorola Solutions (*firm: Devlin)	4:23-cv-00750- SDJ	EDTX, Sherman	2024 -	P
(Patents related to write protect recording)				
Enovsys* v Lyft (*firm: Seth Law)	23-cv-05157-EJD	NDCA, San Jose	2024	P
(Patents related to mobile unit tracking)				
ARM v ICPillar* (*firm: Lowenstein)	IPR2024-00476 IPR2024-00566	PTAB	2024	P,t
(Patents related to computer method for IC design)				
Maxell v TCL* (*firm: King & Spalding)	5:23-CV-00108- RWS-JBB	EDTX, Texarkana	2024 -	P,t
(Patents related to image display apparatus)				
Enovsys* v Uber (*firm: Seth Law)	23-cv-04549-EJD	NDCA, San Jose	2024	P
(Patents related to mobile unit tracking)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
Uber v Enovsys* (*firm: Seth Law)	IPR2024-00825 IPR2024-00826 IPR2024-00827	PTAB	2024 -	P,t
(Patents related to mobile unit tracking)				
JUUL v NJOY* (*firm: Weil Gotshal)	337-TA-1368 IPR2024-00231	ITC PTAB	2024	P,t,TH
(Patent related to vaping devices)				
RJR v Guangdong et al.* (*firm: Mei & Mark)	337-TA-1410	ITC	2024 -	P,t
(Patent related to vaping devices)				
RJR v Kangvape* (*firm: Fish & Richardson)	337-TA-1410	ITC	2024 -	P,t
(Patent related to vaping devices)				
RJR v Breeze et al.* (*firm: Goodwin Procter)	337-TA-1410	ITC	2024 -	P,t
(Patent related to vaping devices)				
RJR v Pastel et al.* (*firm: Keller Heckman)	337-TA-1410	ITC	2024 -	P,t
(Patent related to vaping devices)				
RJR v Shenzhen Yanyang et al.* (*firm: Rimon)	337-TA-1410	ITC	2024 -	P,t
(Patent related to vaping devices)				
RJR v Maduro* (*firm: Thompson Hine)	337-TA-1410	ITC	2024 -	P,t
(Patent related to vaping devices)				
RJR v TheSy* (*firm: Thompson Hine)	337-TA-1410	ITC	2024 -	P,t
(Patent related to vaping devices)				

Cases (continued)

CASE ¹	CASE NUMBER	LOCATION	YEAR	TYPE ²
RJR v SV3* (*firm: Sterne Kessler)	337-TA-1410	ITC	2024 -	P,t
(Patent related to vaping devices)				
REED v MPS* (*firm: Perkins Coie)	IPR2024-00871	PTAB	2024 -	P,t
(Patent related to bootstrap refresh control)				
Phenix* v AU Optronics (*firm: Womble Bond)	2:23-cv-00477- RWS-RSP	EDTX, Marshall	2024 -	P
(Patents related to Gamma reference generation)				
Phenix* v Innolux (*firm: Womble Bond)	2:23-cv-00478- RWS-RSP	EDTX, Marshall	2024 -	P
(Patents related to Gamma reference generation)				

Cases (continued)

I have worked with other clients in various areas of my expertise, including “system, product, and process investigation,” “patent valuation,” “product liability and insurance claim investigation,” “quality systems consulting and engineering,” and “IP licensing.” This work generally relates to patents and/or trade secrets and may involve analysis of products either defensively or offensively. In no case does any of the work involve design of circuits, processes, packaging, software, or systems.

Non-confidentially, I have represented a radiation effects testing company, ICS Radiation Technology. Further, I have worked with investment companies, such as Hatcreek Partners, reviewing potential investment opportunities, and have participated as a technical advisor to nLine Corporation, a company that developed a product for semiconductor wafer inspection using holographic High Aspect Ratio Inspection (HARI) technology. Work associated with each of these matters occurred more than 10 years ago.

These and other non-confidentially related companies are:

The Aspire International Foundation (2019-present)

- Partner;
- Rediscovering and redefining identity and purpose through experiential equine learning programs;
- Not assigned any patents and not engaged in any IP related activities.

Casualty Consulting Group of America (2013-present)

- Partner;
- Assessment of structural damage caused by extreme weather events;
- Not assigned any patents and not engaged in any IP related activities.

VCSY (2013-2020)

- Advisory board Member;
- Technology related to encrypted communication.

Bethel Cannon Group / Bethel Cannon Holdings (2011-present)

- Partner;
- Counseling / Event / Retreat Center / Hunting Lodge;
- Not assigned any patents and not engaged in any IP related activities.

Spirit Song Youth Equestrian Academy / Spirit Song Holdings (2011-present)

- CEO;
- Equine Assisted Learning Program for abused / traumatized youth, families, corporations, and churches;
- Not assigned any patents and not engaged in any IP related activities.

Cases (continued)

E³A (2016-present)

- President (2018-2023);
- Certification training of Equine Practitioners;
- Not assigned any patents and not engaged in any IP related activities.

Novo Tellus Capital Partners (2016-2017)

- Novo Tellus is an investment firm. I served as a technical advisor in reviewing the technology and contracts of investment opportunities.

UTAC (2008-2016)

- Technical consultant in matters related to packaging test and assembly, patents, and contracts.

ICS Radiation Technology (1988-2009)

- Consulting work related to nuclear radiation effects testing.

Creative Management Consultants (CMC) (2003-2004)

- Consulting work related to Internet services, such as access service to clients and web site hosting services; providing business co-op services and internet product purchasing sites.

Hatcreek Partners (1999-2003)

- Hatcreek Partners is an investment firm. I served as a technical advisor in reviewing the technology of investment opportunities.

nLine Corporation (1999-2003)

- Member of Technical Advisory Board;
- nLine Corp.'s business related to semiconductor holographic High Aspect Ratio Inspection (HARI) technology.

Texas Instruments (pre 2002)

- Patent evaluation and application consulting.

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