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FOURTH EDITION

Microchip Fabrication

A Practical Guide to
SEMICONDUCTOR PROCESSING

PETER VAN ZANT

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A Practical Guide to Semiconductor Processing

Peter Van Zant

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The Semiconductor Industry

Overview

In this chapter, you will be introduced to the Semiconductor industry via a brief history, as well as by the importance of the industry in the world economy, an overview of the significant technical developments, and the trends that have made the industry the world's leading industrial segment. The major manufacturing stages are introduced by product types, and transistor building structures along with integration levels will be explained.

Objectives

Upon completion of this chapter you should be able to:

1. Describe the difference between discrete devices and integrated circuits.
2. Define the terms "solid state," "planar processing" and "N" and "P" type semiconducting materials.
3. List the four major stages of semiconductor processing.
4. Explain the Integration Scale and the implications of processing circuits of different levels of integration.
5. List the major process and device trends in semiconductor processing.

Birth of an Industry

The electronic signal processing industry got its jump start with the discovery of the audion vacuum tube in the 1906 by Lee DeForest.¹ It

2 Chapter One

made possible the radio, television, and other consumer electronics. It also was the brains of the world's first electronic computer, named the Electronic Numeric Integrator and Calculator (ENIAC), first demonstrated at the Moore School of Engineering in Pennsylvania in 1947.

This ENIAC hardly fits the modern picture of a computer. It occupied some 1500 square feet, weighed 30 tons, generated large quantities of heat, required the services of a small power station, and cost \$400,000 in 1940 dollars. The ENIAC was based on 19000 vacuum tubes along with thousands of resistors and capacitors (Fig. 1.1).

A vacuum tube consists of three elements, two electrodes separated by a grid in a glass enclosure (Fig. 1.2). Inside the enclosure is a vacuum, required to prevent the elements from burning up, and to allow the easy transfer of electrons.

Tubes perform two important electrical functions, switching and amplification. Switching refers to the ability of an electrical device to turn a current on or off. Amplification is a little more complicated. It is the ability of a device to receive a small signal (or current) and amplify it while retaining its electrical characteristics.

Vacuum tubes suffer from a number of drawbacks. They are bulky, prone to loose connections and vacuum leaks, fragile, require rela-

Size, ft	30 x 50
Weight, tons	30
Vacuum Tubes	18,000
Resistors	70,000
Capacitors	10,000
Switches	6000
Power Requirements, W	150,000
Cost (in 1940)	\$400,000

Figure 1.1 Eniac statistics. (*Foundations of Computer Technology*, J. G. Giarratano, Howard W. Sams & Co., Indianapolis, Ind., 1983.)

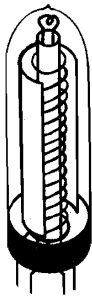


Figure 1.2 Vacuum tube.

tively large amounts of power to operate, and their elements deteriorate rather rapidly. One of the major drawbacks to the ENIAC and other tube-based computers was a limited operating time due to tube burn-out.

These problems were the impetus leading many laboratories around the country to seek a replacement for the vacuum tube. That effort came to fruition on Dec. 23, 1947 when three Bell Lab scientists demonstrated an electrical amplifier formed from the semiconducting material Germanium (Fig. 1.3).

This device offered the electrical functioning of a vacuum tube, but with the advantages of the solid state (no vacuum), small and light weight, low power requirements and long lifetime. First named a transfer resistor, the new device soon became known as the *transistor*.

The three scientists, John Bardeen, Walter Brattin and William Shockley were awarded the 1956 Nobel Prize in physics for their invention.

The Solid State Era

That first transistor was a far distance from the high density integrated circuit of today. But it was the component that gave birth to the solid state electronics era with all its famous progeny. Besides transistors, solid state technology is also used to create diodes, resistors and capacitors. Diodes are two-element devices that function in a circuit as a switch. Resistors are one-element devices that serve to limit current flow. Capacitors are two-element devices that store charge in a circuit. In some circuits, the technology is used to create fuses. Refer to Chapter 14 for an explanation of these concepts and a explanation of how these devices work.

These devices, containing only one device per chip, are called discrete devices (Fig 1.4). Most discrete devices have less demanding operational and fabrication requirements than integrated circuits. In

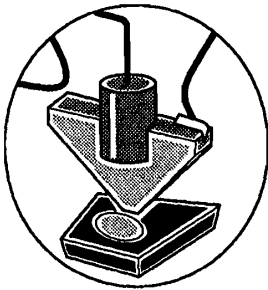


Figure 1.3 The first transistor.

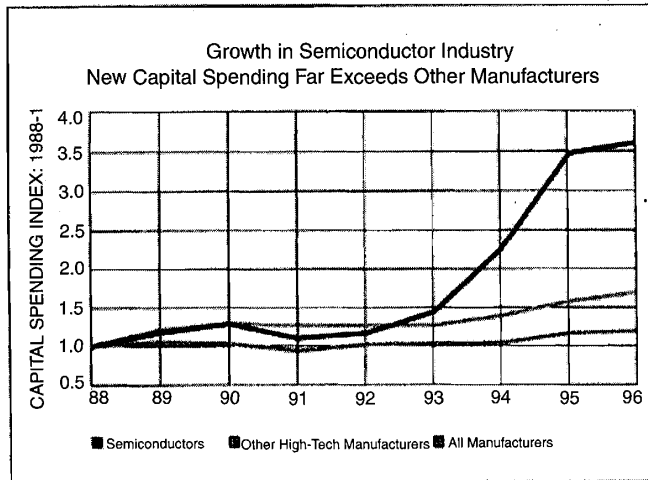


Figure 1.18 Growth of semiconductor industry-capital spending (Courtesy of Semiconductor Industry Association)

ket. Captive suppliers are firms whose final product is a computer, communications system, etc., and produce chips in-house for their own products. Some firms produce chips for in-house use and also sell on the open market, and others produce specialty chips in-house and buy others on the open market. During the 1980's, the trend has been to a greater percentage of chips being fabricated in captive fab areas.

Stages of Manufacturing

Solid state devices are manufactured in four distinct stages (Fig. 1.19). They are: material preparation, crystal growing and wafer preparation, wafer fabrication, and packaging.

In the first stage, material preparation (see Chapter 2), the raw semiconducting materials are mined and purified to meet semiconductor standards. For silicon, the starting material is sand, which is converted to pure silicon with a polysilicon structure. (Fig. 1.21).

In stage two, the material is formed into a crystal with specific electrical and structural parameters. Next, thin disks called wafers, are cut from the crystal and surface treated (Fig. 1.21) in a process called

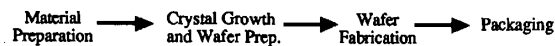


Figure 1.19 Stages of semiconductor manufacturing.

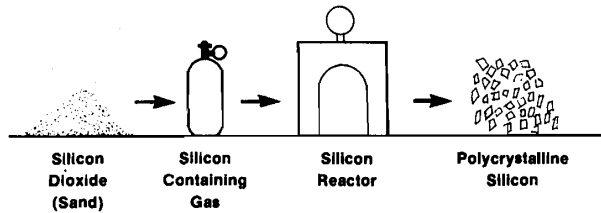


Figure 1.20 Conversion of silicon dioxide to semiconductor grade silicon.

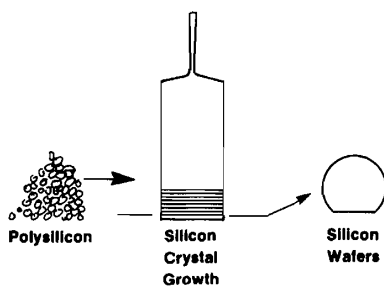


Figure 1.21 Crystal growth and wafer preparation.

crystal growth and wafer preparation (see Chapter 3). The industry also makes devices and circuits from germanium, and compounds of different semiconductor materials.

It is in stage three (Fig. 1.22), wafer fabrication, that the devices or integrated circuits are actually formed in and on the wafer surface. Up to several thousand identical devices can be formed on each wafer, although two to three hundred is a more common number. The area on the wafer occupied by the discrete device or integrated circuit is called a chip or die. The wafer fabrication process is also called fabrication, fab, chip fabrication or microchip fabrication. While a wafer fabrication operation may take several thousand individual steps there are two major activities. In the front end of the line (FEOL), the transistors and other devices are formed in the wafer surface. In the back end of the line (BEOL), the devices are wired together with metalization processes and the circuit is protected with a final sealing layer.

Following wafer fabrication, the chips on the wafer are complete, but untested and still in wafer form. Next comes an electrical test (called wafer sort) of every chip to identify those that meet customer specifications. Wafer sort may be the last step in the wafer fabrication or the first step in the *packaging* process.

Packaging (Fig. 1.23) is the series of processes that separates the wafer into individual die, and places them into protective packages. A

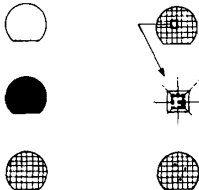
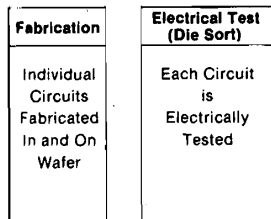


Figure 1.22 Wafer fabrication (and electrical test).

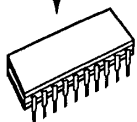
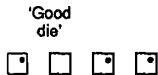


Figure 1.23 Packaging stage.

protective chip package is necessary to protect the chip from contamination and abuse, and to provide a durable and substantial electrical lead system to allow connection of the chip onto a printed circuit board or directly into an electronic product. Packaging takes place in a dif-

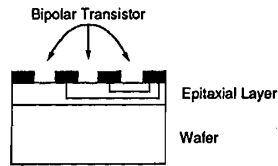


Figure 1.26 Double diffused bipolar transistor formed in epitaxial layer.

Bell Labs conceived of forming transistors in a high purity layer of semiconducting material deposited on top of the wafer (Fig. 1.27). Called an epitaxial layer, this discovery allowed higher speed devices and provided a scheme for the closer packing of components in a bipolar circuit.

The 1950's was indeed the golden age of semiconductor development. During this incredibly short time almost all of the basic processes and materials were discovered. The decade opened with the knowledge of manufacturing small volumes of crude devices in germanium and ended with the first integrated circuit and the material silicon firmly established as the semiconductor of the future.

The Processing Decade (1961–1970)

The 1960's was the decade of the process engineer and start-up companies. The chip price erosion trend of the industry was well established in the 1950's. In the 1960's, many new chip manufacturers opened their doors and established firms to solidify their positions. It fell to the process engineers to develop high-yield volume processes to crank out the needed chips at ever lower prices. In this decade, the

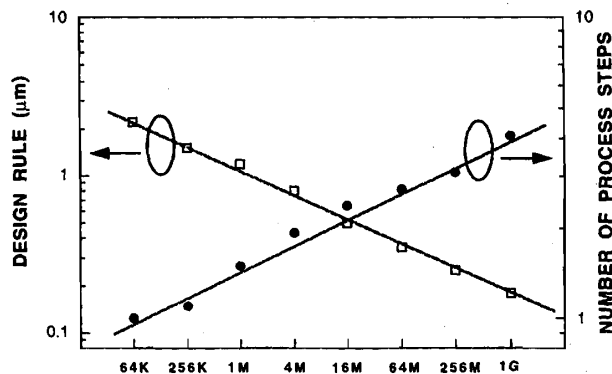


Figure 1.27 DRAM growth design rule and number of process steps. (SEMI 1995 ISS Conference)

represents the number of electrons in the outer ring and all of the elements in each column share similar properties.

It is no accident that the three best electrical conductors (copper, silver and gold) all appear in the same column (Ib) (Fig. 2.4) of the periodic table.

There are two more rules of atomic structure relevant to the understanding of semiconductors.

4. Elements are stable with a filled outer ring or with eight electrons in the outer ring. These atoms tend to be more chemically stable than atoms with partially filled rings.

5. Atoms seek to combine with other atoms to create the stable condition of full orbits or eight electrons in their outer ring.

Rules 4 and 5 influence the creation of N- and P-type semiconductor materials as explained in the section on doped semiconductors.

Electrical Conduction

Conductors

An important property of many materials is the ability to conduct electricity or support an electrical current flow. An electrical current is simply a flow of electrons. Electrical conduction takes place in elements and materials where the attractive hold of the protons on the outer ring electrons is relatively weak. In such a material, these electrons can be easily moved and set up an electrical current. This condition exists in most metals.

The property of materials to conduct electricity is measured by a factor known as conductivity. The higher the conductivity, the better the conductor. Conducting ability is also measured by the reciprocal of the conductivity which is resistivity. The lower the resistivity of a material, the better the conducting ability.

$$C = 1/\rho$$

29	Cu
	Copper
47	Ag
	Silver
79	Au
	Gold

Figure 2.4 The three best electrical conductors.

where C = conductivity
 ρ = resistivity in ohms-centimeter (Ω -cm)

Dielectrics and Capacitors

At the opposite end of the conductivity scale are materials that exhibit a large attractive force between the nucleus and the orbiting electrons. The net effect is a great deal of resistance to the movement of electrons. These materials are known as dielectrics. They have low conductivity and high resistivity. In electrical circuits and products, dielectric materials such as silicon dioxide (glass) are used as insulators.

An electrical device known as a *capacitor* is formed whenever a dielectric layer is sandwiched between two conductors. In semiconductor structures, capacitors are formed in MOS gate structures, between metal layers and silicon substrates separated by dielectric layers, and other structures (see Chapter 16). The practical effect of a capacitor is that it stores electrical charges. Capacitors are used for information storage in memory devices to prevent unwanted charges to build up in conductors and silicon surfaces, and to form the working parts of field effect (MOS) transistors. Capacitance ability of a film is relative to the area and thickness and a property parameter known as the dielectric constant. Semiconductor metal conduction systems need high conductivity and, therefore, low resistance and low capacitance materials. These are referred to as low- k dielectrics. Dielectric layers used as insulators between conducting layers need high capacitances or high- k dielectrics.

$$C = \frac{k E_0 A}{t}$$

C = capacitance
 k = dielectric constant of material
 E_0 = permittivity of free space (free space has the highest "capacitance")
 A = area of capacitor
 t = thickness of dielectric material

Resistors

An electrical factor related to the degree of conductivity (and resistivity) of a material is the electrical resistance of a specific volume of the material. The resistance is a factor of the resistivity and dimensions of the material. Resistance to electrical flow is measured in ohms as illustrated in Fig. 2.5.

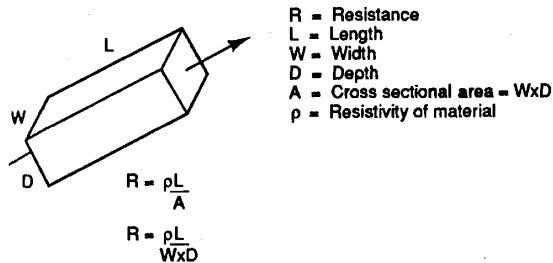


Figure 2.5 Resistance of rectangular bar.

The formula defines the electrical resistance of a specific volume of a specific material (in this illustration, the volume is a rectangular bar with dimensions X, Y and Z). The relationship is analogous to density and weight, *density* being a material property and *weight* being the force exerted by a specific volume of the material.

Electric current flow is analogous to water flowing in a hose. For a given hose diameter and water pressure, only a given amount of water will flow out of the hose. The resistance to flow can be reduced by increasing the hose diameter, shortening the hose, and/or increasing the pressure. In an electrical system, the electron flow can be increased by increasing the cross section of the material, shortening the length of the piece, increasing the voltage (analogous to pressure), and/or decreasing the resistivity of the material.

Intrinsic Semiconductors

Semiconducting materials, as the name implies, are materials that have some natural electrical conducting ability. There are two elemental semiconductors—silicon and germanium—both found in column IV (Fig. 2.6) of the periodic table. In addition, there are some tens of material compounds (a compound is a material containing two or more chemically bound elements) that also exhibit semiconducting properties. These compounds come from elements found in columns III and V, such as gallium arsenide and gallium phosphide. Others are compounds from elements shown in columns II and VI.

The term intrinsic refers to these materials in their purified state and not contaminated with impurities or other substances.

Doped Semiconductors

Semiconducting materials, in their intrinsic state, are not useful in solid state devices. However, through a process called doping, specific

IIIA	IVA	VA
5 10.811 B Boron	6 12.01115 C Carbon	7 14.0067 N Nitrogen
13 26.9815 Al Aluminum	14 28.086 Si Silicon	15 30.9738 P Phosphorus
31 69.72 Ga Gallium	32 72.64 Ge Germanium	33 74.922 As Arsenic
49 114.82 In Indium	50 118.69 Sn Tin	51 121.75 Sb Antimony
81 204.37 Tl Thallium	82 207.19 Pb Lead	83 208.980 Bi Bismuth

Elemental Semiconductors

III - V Compound Semiconductors

Figure 2.6 Semiconductor materials.

elements can be introduced into intrinsic semiconductor materials. These elements increase the conductivity of the intrinsic semiconductor material. The doped material displays two unique properties that are the basis of solid state electronics. The two properties are:

1. Precise resistivity control through doping
2. Electron and hole conduction

Resistivity of doped semiconductors

Metals have a conductivity range limited to 10^4 to 10^6 /ohm-cm. The implications of this limit is illustrated by an examination of the resistor represented in Fig. 2.5. Given a specific metal with a specific resistivity, the only way to change the resistance of a given volume is to change the dimensions. In a semiconducting material, the resistivity can be changed, giving another degree of freedom in the design of the resistor. Semiconductors are such a material. Their resistivity can be extended over the range of 10^{-3} to 10^3 by the addition of dopant atoms.

Semiconducting materials can be doped into a useful resistivity range by elements that make the material either electron rich (N-type) or hole rich (P-type).

Figure 2.7 shows the relationship of the doping level to the resistivity of silicon. The x-axis is labeled the carrier concentration because the electrons or holes in the material are called carriers. Note that there are two curves: N-type and P-type. That is due to the different amount of energies required to move an electron or a hole through the material. As the curves indicate, it takes less of a concentration of N-type dopants than P-type dopants to create a given resistivity in silicon. Another way to express this phenomenon is that it takes less energy to move an electron than move a hole.

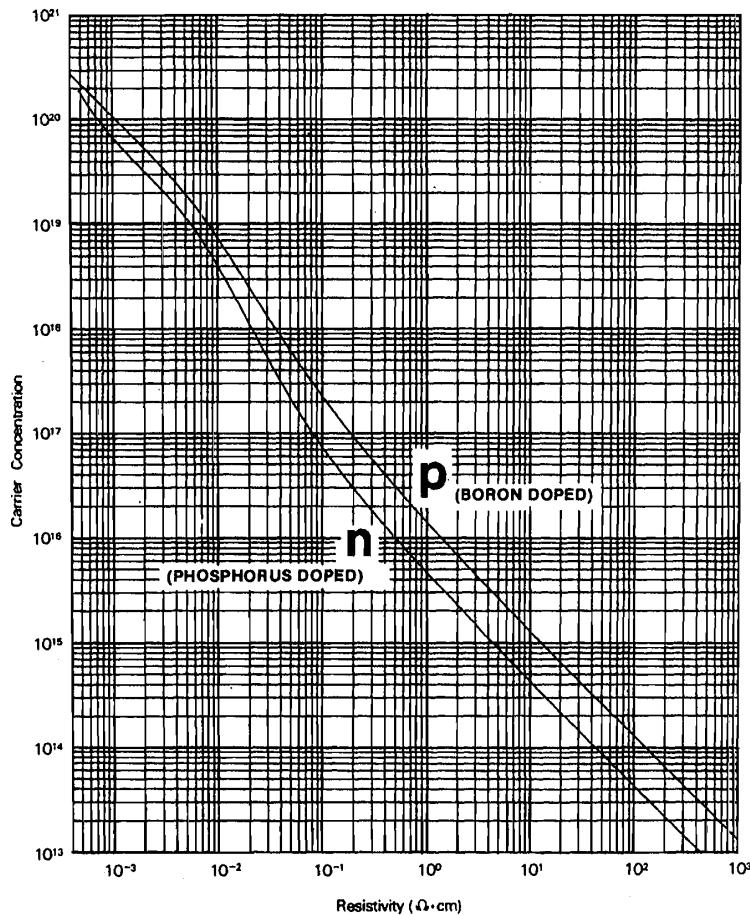


Figure 2.7 Silicon resistivity versus doping (carrier) concentration. (After Thurber *et al.*, *Natl. Bur Standards Spec. Publ.* 400-64, May 1981, tables 10 and 14.)

It takes only 0.000001% to 0.1% of a dopant to bring a semiconductor material into a useful resistivity range. This property of semiconductors allows the creation of regions of very precise resistivity values in the material.

Electron and Hole Conduction

Another limit of a metal conductor is that it conducts electricity only through the movement of electrons. Metals are permanently N-type. Semiconductors can be made either N- and P-type by doping with specific dopant elements. N- and P-type semiconductors can conduct electricity by either electrons or holes. Before examining the conduction mechanism, it is instructive to examine the creation of free (or extra) electrons or holes in a semiconductor structure.

To understand the situation of N-type semiconductors, consider a piece of silicon (Si) doped with a very small amount of arsenic (As) as shown in Fig. 2.8. Assuming even mixing, each of the arsenic atoms would be surrounded by silicon atoms. Applying the rule from section 2.3.2 that atoms attempt to stabilize by having eight electrons in their outer ring, the atom is shown sharing four electrons from its neighboring silicon atoms. However, arsenic is from column V which means it has five electrons in its outer ring. The net result is that four of them pair up with electrons from the silicon atoms, leaving one left over. This one electron is available for electrical conduction.

Considering that a crystal of silicon has millions of atoms per cm^3 , there are lots of electrons available to conduct an electrical current. In silicon, the elements arsenic, phosphorus and antimony create N-type conditions.

An understanding of P-type material is approached in the same manner (Fig. 2.9). The difference is that only boron, from column III of the periodic table, is used to make silicon P-type. When mixed into the silicon, it too borrows electrons from silicon atoms. However, having only three outer electrons, there is a place in the outer ring that is not filled by an electron. It is this unfilled position that is defined as a hole.

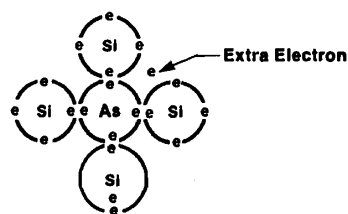


Figure 2.8 N-type doping of silicon with arsenic.

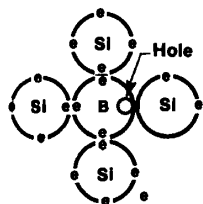


Figure 2.9 P-type doping of silicon with boron.

Within a doped semiconductor material there is a great deal of activity: holes and electrons are constantly being created. The electrons are attracted to the unfilled holes, in turn, leaving an unfilled position, which creates another hole.

How the holes contribute to electrical conduction is illustrated in Fig. 2.10. When a voltage is applied across a piece of conducting or semiconducting material, the negative electrons move towards the positive pole of the voltage source, such as a battery.

In P-type material (Fig. 2.11), an electron will move towards the positive pole by jumping into a hole along the direction of route (t_1). Of course when it leaves its position, it leaves a new hole. As it continues towards the positive pole, it creates a succession of holes. The effect to someone measuring this process with a current meter is that the material is supporting a positive current, when actually it is a negative current moving in the opposite direction. This phenomenon is called *hole flow* and is unique to semiconducting materials.

The dopants that create a P-type conductivity in a semiconductor material are called *acceptors*. Dopants that create N-type conditions

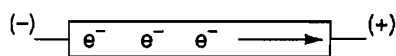


Figure 2.10 Electron conduction in N-type semiconductor material.

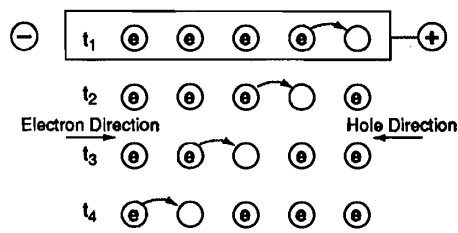


Figure 2.11 Hole conduction in P-type semiconductor material.

are called *donors*. An easy way to keep these terms straight is that acceptor has a p and donor is spelled with an n.

The electrical characteristics of conductors, insulators and semiconductors is summarized in Fig. 2.12 The particular characteristics of doped semiconductors is summarized in Fig. 2.13.

N- and P-type conditions are also created in germanium and compound semiconductors with specific dopant elements.

Carrier Mobility

It was mentioned in section 2.5.6 that it takes “less energy” to move an electron than a hole through a piece of semiconducting material. In a circuit we are interested in both the energy required to move these carriers (holes and electrons) and the speed at which they move. The speed of movement is called the “carrier mobility” with holes having a lower mobility than electrons. This factor is an important consideration in selecting a particular semiconducting material for a circuit.

Classification	Electrons	Examples	Conductivity
1. Conductor	Free to Move	Gold Copper Silver	10^4 – 10^8 /ohm-cm
2. Insulator (Dielectric)	Bound	Glass Plastic	10^{-22} – 10^{-10} /ohm-cm
3. Semiconductor a. Intrinsic	Some Available	Germanium Silicon III-IV	10^{-9} – 10^3 /ohm-cm
b. Doped	Controlled Amount Available	N-type Semiconductor P-type Semiconductor	

Figure 2.12 Electrical classification of materials.

	N-TYPE	P-TYPE
1. Conduction	Electrons	Holes
2. Polarity	Negative	Positive
3. Dopant Term	Donor	Acceptor
4. Doping Elements in Silicon	Arsenic Phosphorus Antimony	Boron

Figure 2.13 Characteristics of doped semiconductors.

1. Chip, die, device, circuit, microchip, or bar. All of these terms are used to identify the microchip patterns covering the majority of the wafer surface.

2. Scribe lines, saw lines, streets, and avenues. These areas are spaces between the chips that allow separation of the chip from the wafer. Generally the scribe lines are blank, but some companies place alignment targets, or test structures (see photomasking) in them.

3. Engineering die, test die. These chips are different from the regular device or circuit die. They contain special devices and circuit elements that allow electrical testing during the fabrication processing.

4. Edge die. The edges of the wafer contain partial die patterns that are wasted space. The trend to increasing die sizes leads to more wasted space that is compensated by manufacturing larger diameter wafers. One of the driving forces behind larger wafer diameters is to minimize the area occupied by the edge die.

5. Wafer crystal planes. The cutaway section illustrates the crystal structure of the wafer under the circuit layers. The diagram shows that the chip edges are oriented to the wafer crystal structure.

6. Wafer flats/notches. The depicted wafer has a major and minor flat, indicating that it is a P-type $\langle 100 \rangle$ oriented wafer (see Chapter 3 for the flat code). 300mm diameter wafers use notches as crystal orientation indicators.

Basic Wafer-Fabrication Operations

There are hundreds of thousands of different microchip types and functions. However, they are made with a small number of basic structures (primarily bipolar or MOS structures, see Chapter 16) and manufacturing processes. An analogy is the auto industry. This industry produces a wide variety of products, from sedans to bulldozers. Yet the processes of metal forming, welding, painting, etc. are common to all plants. Within the plant, these basic processes are applied in different ways to produce the desired product.

The same is true in microchip fabrication. Companies use four basic operations in an infinite number of sequences and variations to produce specific microchips. They are layering, patterning, doping, and heat treatments (Fig. 4.3).

- Layering
- Patterning
- Doping
- Heat Treatments

Figure 4.3 Basic wafer-fabrication operations.

Layering

Layering is the operation used to add thin layers to the wafer surface. An examination of the simple MOS transistor structure in Fig. 4.4 shows a number of layers that have been added to the wafer surface. These layers could be insulators, semiconductors, or conductors. They are of different materials and are grown or deposited by a variety of processes.

The major techniques are grown silicon dioxide layers and deposition (Fig. 4.5) of a variety of materials. Common deposition techniques are chemical vapor deposition (CVD), evaporation, and sputtering. Figure 4.6 lists common layer materials and layering processes. The details of each are explained in the process chapters. The role of the different layers in the structures is explained in Chapter 16.

Patterning

Patterning is the series of steps that results in the removal of selected portions of the added surface layers (Fig. 4.7). After removal, a *pattern* of the layer is left on the wafer surface. The material removed may be in the form of a hole in the layer or just a remaining island of the material.

The patterning process is known by the names photomasking, masking, photolithography, and microlithography. During the wafer fabri-

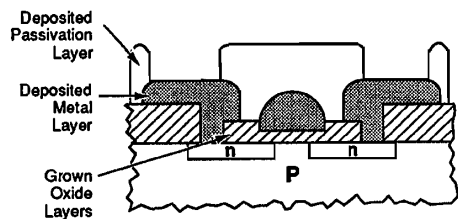


Figure 4.4 Cross section of completed metal gate MOS transistor with grown and deposited layers.

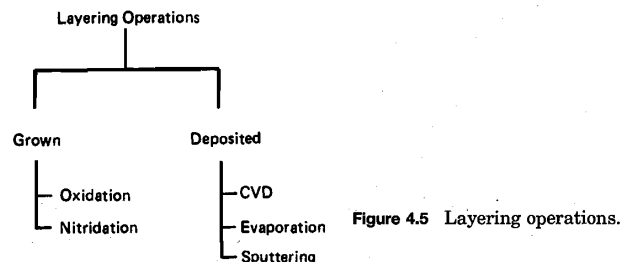


Figure 4.5 Layering operations.

Layers	Thermal Oxidation	Chemical Vapor Deposition	Evaporation	Sputtering
Insulators	Silicon Dioxide	Silicon Dioxide Silicon Nitrides		Silicon Dioxide Silicon Monoxide
Semiconductors		Epitaxial Silicon Poly Silicon		
Conductors			Aluminum Aluminum/Silicon Aluminum/Copper Nichrome Gold	Tungsten Titanium Molybdenum Aluminum Aluminum/Silicon Aluminum/Copper

Figure 4.6 Table of layers, processes, and materials.

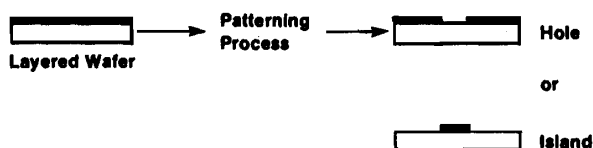


Figure 4.7 Patterning.

cation process, the various physical *parts* of the transistors, diodes, capacitors, resistors and metal conduction system are formed in and on the wafer surface. These parts are created one layer at a time by the combination of putting a layer on the surface and removing portions, with a patterning process, to leave a specific shape. The goal of the patterning operation is to create the desired shapes in the exact dimensions (feature size) required by the circuit design, and to locate them in their proper location on the wafer surface and in relation to the other *parts*.

Patterning is the most critical of the four basic operations. This operation sets the critical dimensions of the devices. Errors in the patterning process can cause distorted or misplaced patterns that result in changes in the electrical functioning of the device/circuit. Misplacement of the pattern can have the same bad results. Another problem is defects. Patterning is a high tech version of photography, but performed at incredibly small dimensions. Contamination in the process steps can introduce defects. This contamination problem is magnified by the fact that patterning operations are performed on the wafer from five to twenty or more times in the course of the wafer-fabrication process.

Doping

Doping is the process that puts specific amounts of dopants in the wafer surface through openings in the surface layers (Fig. 4.8). The

use. The uses are treated in general. For a more detailed explanation of film roles in particular devices, see Chapter 16. Deposition methods for conductive metal films is discussed in Chapter 13.

Deposited Semiconductors

So far in this text we have discussed the formation of wafers as the base of semiconductor devices and circuits. However there are several drawbacks to using bulk wafers for high quality devices and circuits. Crystal quality, doping ranges, and doping control all limit bulk wafer use. These factors placed a limit on the fabrication of high-performance bipolar transistors. A solution was found by the development of a deposited silicon layer, called an *epitaxial layer*. It is one of the major advances in the industry. Epitaxial layers were a part of the technology as early as 1950.¹⁷ Since then deposited silicon layers have found additional uses in advanced bipolar device design, a high-quality base for CMOS circuits, and silicon epitaxial layers deposited on sapphire and other substrates (Chapter 14). Gallium arsenide and other III–IV and II–VI films are also deposited in epitaxial films. Epitaxial films that are the same material as the substrate (silicon on silicon) are *homoepitaxial*. When the deposited material is different than the substrate (GaAs on silicon), the film is called *heteroepitaxial*.

Epitaxial Silicon

The term *epitaxial* comes from the Greek word meaning “arranged upon.” In semiconductor technology, it refers to the single crystalline structure of the film. The structure comes about when silicon atoms are deposited on a bare silicon wafer in a CVD reactor (Fig. 12.27). When the chemical reactants are controlled and the system parameters set correctly, the depositing atoms arrive at the wafer surface with sufficient energy to move around on the surface and orient themselves to the crystal arrangement of the wafer atoms. Thus an epitaxial film deposited on a $\langle 111 \rangle$ -oriented wafer will take on a $\langle 111 \rangle$ orientation.

If, on the other hand, the wafer surface has a thin layer of silicon dioxide, an amorphous surface layer, or contamination the depositing atoms have no structure to align to. The resulting film structure is polysilicon. This condition is useful for some applications, such as MOS gates, and is unwanted if the goal is to grow a single-crystal film structure.

Silicon tetrachloride source chemistry. A number of different sources are used for the deposition of epitaxial silicon (Fig. 12.28). Deposition temperature, film quality, growth rate, and compatibility with a par-

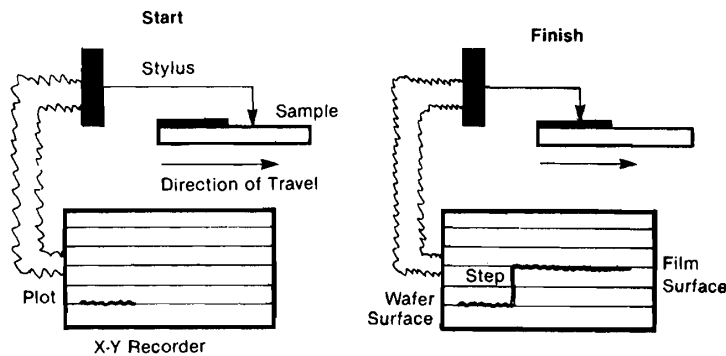


Figure 14.12 Step height measurement.

face step, it changes position, causing a change in the signal output. This change is evidenced by a change of pen position on the x - y chart trace. The change in position is relative to the step height, which is read directly from the calibrated x - y chart.

Junction Depth

A critical device parameter is the junction depth of the various doped regions. This parameter is measured after each of the doping steps. The measurement methods described are all performed off-line; that is, the test wafers or device wafers have to be taken to a measurement station or laboratory for the measurement.

Groove and stain

The traditional method of junction depth measurement is by the groove (or bevel) and stain technique. Grooving or beveling is a mechanical method of exposing the junction for viewing and measurement from the horizontal plane (Fig. 14.13). The extreme shallow depth of the junction requires either grooving or beveling of the wafer to expose the junction.

The junction itself is not visible to the naked eye. Two techniques, called *junction delineation*, are available to make it visible. Both techniques utilize the electrical differences between N-type and P-type regions. The first technique, the etch technique, starts with the placement of a drop of hydrofluoric acid and water mixture over the junction (Fig. 14.14). A heat lamp is directed onto the exposed junction. The heat and light cause holes or electrons to flow in each region. As a result of the flowing current, the etch rate of the $\text{HF-H}_2\text{O}$ mixture is higher on the N-type region, making it appear darker.

the transistor on and off (switching speed) is critical when millions of transistors are operating.

Field-effect transistors (FETs)

Metal-gate MOSFET. As early as 1948 William Shockley noted another type of transistor operation, a field-effect-actuated transistor current flow. That effect was developed into the field-effect transistor, with the MOS structure now the most popular design. An MOS transistor, like a bipolar (Fig. 16.18), has three regions, three contacts, and two junctions but in a different structure. There is a similar analogy to the water system described previously. Current travels from the source region (tank), through the dielectric gate material (valve), and into the drain (bucket) before exiting the device.

An MOSFET gate controls current flow by a different mechanism than a bipolar base. The MOS structure shown in Fig. 16.19 is a simple metal-gate type capacitor and operates the same as a capacitor. When a voltage (the gate voltage) is applied to the gate through the gate metal a *field effect* takes place in the surface of the semiconductor. The effect is either a build-up of charge or a depletion of charges in

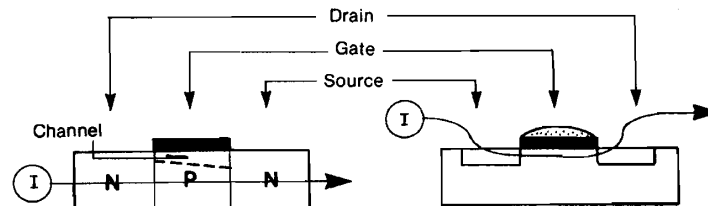


Figure 16.18 MOS transistor operation.

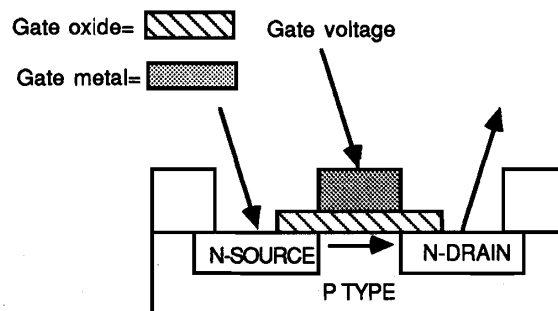


Figure 16.19 Metal gate MOS transistor.

the wafer surface under the top plate. Which event occurs depends on the doping conductivity type in the wafer under the gate and the polarity of the gate voltage.

The build-up or depletion of charge creates a channel under the gate which connects the source and drain. The surface of the semiconductor is said to be *inverted*. The source is biased with a voltage and the drain is grounded relative to the source. In this condition a current starts to flow as the inverted surface creates an electrically connecting channel. The source and drain are essentially shorted together. Applying more voltage to the gate increases the size of the channel, allowing more current to flow through the transistor (see Chapter 14). By controlling the gate voltage, an MOS transistor can be used as a switch (on/off) or as an amplifier. However, MOS transistors are voltage amplifiers, unlike the current amplification of bipolar transistors.

If the source and drain are N type formed in a P-type wafer, the channel must be of N type for conduction to occur. This type of MOS transistor is called N channel. MOS transistors with P-type sources and drains are P channel. Most high-performance MOS circuits are built around N-channel transistors due to the higher mobility of electrons in silicon. The mobility makes N-channel transistors faster and they consume less power than P-channel circuits. They often are referred to as NMOS transistors. Figure 16.20 shows the major steps in the formation of an N-channel metal-gate MOS transistor.

Silicon Gate MOS. A certain amount of voltage must be applied to the gate metal before the channel forms. This voltage is called the *threshold voltage* or V_t . The value of the threshold voltage is an important and critical circuit parameter. A lower V_t means less power supplies and faster circuits.

A primary parameter that determines the threshold voltage is the *work function* between the gate material and the doping level in the semiconductor. The work function can be thought of as a kind of electrical compatibility. The lower the work function, the lower the threshold voltage, the lower the power required to run the circuit, etc.

Deposited doped polysilicon has a lower work function than aluminum as an MOS gate material and has become the standard gate electrode material for MOS transistors. The formation of the transistor is shown in Fig. 16.21. The polysilicon is heavily doped N type to reduce its resistance. Thus doped it serves as the gate electrode and as a circuit conduction line. A polysilicon gate can withstand subsequent high-temperature processing without degradation.

An additional benefit of the silicon-gate process is the self-aligned gate. In the metal-gate process sequence, a hole for the gate oxide must be patterned between the source and drain. To ensure that the

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