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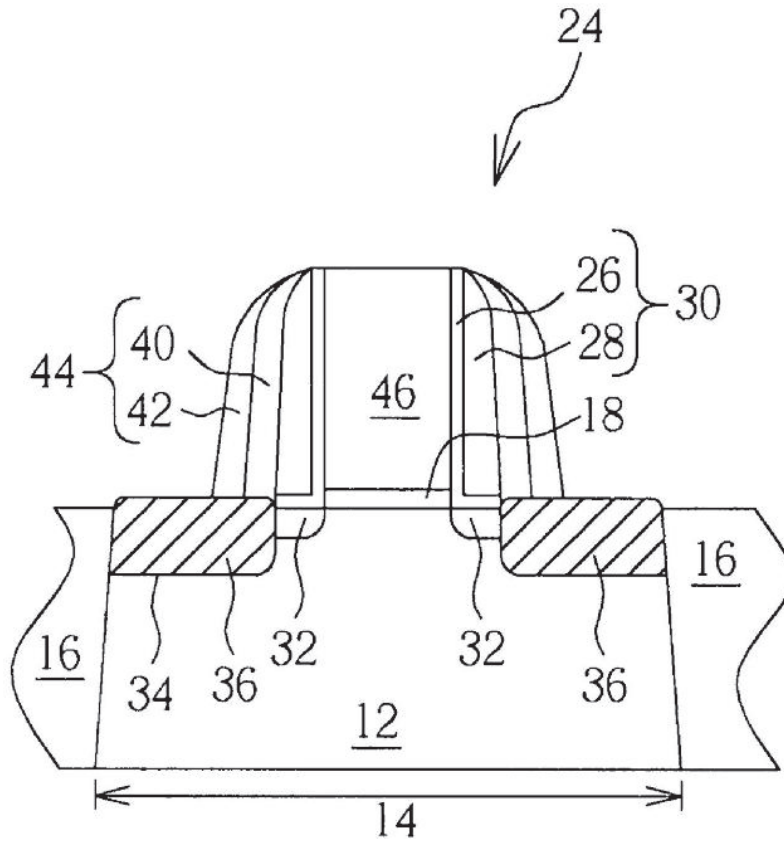
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Metal oxide semiconductor transistor and manufacturing method thereof

METAL-OXIDE SEMICONDUCTOR TRANSISTOR AND METHOD FOR FABRICATING THE
SAME

(57)Abstract

The present invention discloses a method for fabricating a metal oxide semiconductor (MOS) transistor. A semiconductor substrate is first provided, and a silicon layer is formed on the surface of the semiconductor substrate. A first lithography and etching process is then performed on the silicon layer to form a gate pattern. An epitaxial layer is then formed in the semiconductor substrate on both sides of the gate pattern. A second lithography and etching process is then performed on the gate pattern to form at least one opening (slot) in the gate pattern. The opening physically separates the gate pattern to form two gates.



12: Semiconductor substrate

14: Active area

16: Shallow Trench Isolation

18: Gate insulation layer

24: Gate

26: Silicon oxide layer

28: Silicon nitride layer

30: First side wall

32: Lightly doped drain

34: Groove

36: Epitaxial layer

40: Silicon oxide layer

42: Silicon nitride layer

44: Second side wall

46: Gate

6. Description of the invention:

[Technical field to which the invention belongs]

The present invention relates to a method for manufacturing a metal oxide semiconductor transistor, and more particularly to a method for forming an epitaxial layer before defining a polysilicon slot.

【Prior technology】

In the semiconductor industry, polysilicon is often used to form the gate electrode of typical metal-oxide-semiconductor (MOS) transistors due to its heat-resistance. This allows the source and drain regions to be annealed simultaneously at high temperatures. Furthermore, because polysilicon blocks ion-implanted doping atoms from entering the channel region, self-aligned source and drain regions can be easily formed at high temperatures after gate patterning.

As the size of semiconductor devices becomes smaller and smaller, the manufacturing process of transistors has also undergone many improvements to produce small and high-quality transistors. When manufacturing the gate of a conventional MOS transistor, a polysilicon layer and a hard mask are usually firstly applied to the entire surface of a semiconductor substrate. Then, the polysilicon layer and the hard mask are subjected to two photolithography and etching processes to pattern the polysilicon layer and the hard mask.

The transistor gates are formed. The first lithography and etching process preferably patterns the hard mask and polysilicon layer into a plurality of elongated polysilicon gate patterns. The second lithography and etching process forms polysilicon openings (poly slots) within each elongated gate pattern, separating each gate pattern into two gates via these openings. Sidewalls are then formed on the patterned gate sidewalls, and a lightly doped drain and epitaxial layer are formed in the semiconductor substrate on both sides of the sidewalls.

However, because conventional processes form the aforementioned polysilicon openings before growing the epitaxial layer, the etching rate of the polysilicon openings typically affects subsequent processes. For example, if the etching rate in the second lithography and etching process is low, the opening in the polysilicon gate typically cannot be completely etched, resulting in polysilicon residue, which in turn causes line end bridges in the subsequently grown epitaxial layer. Conversely, if the etching rate of the etching process is too high, the hard mask on the polysilicon layer will be over-consumed during the etching process, causing subsequent wear of the sidewalls of the gate sidewalls. As the sidewalls wear away, portions of the gate sidewalls are exposed, and thus, during the subsequent epitaxial growth process, unwanted epitaxial structures will grow on the gate sidewalls.

[Content of the invention]

Therefore, the present invention discloses a method for manufacturing a metal oxide semiconductor transistor to solve the above-mentioned problem of using two lithography and etching processes to manufacture polysilicon openings.

problem.

A preferred embodiment of the present invention discloses a method for fabricating a metal oxide semiconductor (MOS) transistor. A semiconductor substrate is first provided, and a silicon layer is formed on the surface of the semiconductor substrate. A first lithography and etching process is then performed on the silicon layer to form a gate pattern. An epitaxial layer is then formed in the semiconductor substrate on both sides of the gate pattern. A second lithography and etching process is then performed on the gate pattern to form at least one opening (slot) in the gate pattern. The opening physically separates the gate pattern to form two gates.

Another embodiment of the present invention discloses a metal oxide semiconductor transistor, which includes: a semiconductor substrate; a gate arranged on the semiconductor substrate, the gate having four sidewalls, and two opposite sidewalls of the four sidewalls have sidewall particles and the other two opposite sidewalls do not have sidewall particles; and an epitaxial layer arranged in the semiconductor substrate on both sides of the sidewall particles.

【Implementation】

Please refer to Figures 1 to 6, which are schematic diagrams of a preferred embodiment of the present invention for fabricating a metal oxide semiconductor transistor. As shown in Figure 1, a semiconductor substrate 12 is first provided, such as a silicon substrate or a silicon-on-insulator (SOI) substrate. Then, at least one active region 14 is defined on the semiconductor substrate 12, and a plurality of isolation regions 14 are formed.

Shallow trench isolation (STI) 16 structure.

A gate insulating layer (not shown) made of a dielectric material such as oxide or nitride is then formed on the surface of the semiconductor substrate 12. A polysilicon layer having a thickness of approximately 1000 angstroms and a hard mask are then sequentially formed on the gate insulating layer. In this embodiment, the hard mask can be made of materials such as silicon dioxide (SiO_2), silicon nitride, or silicon oxynitride (SiON), while the polysilicon layer can be made of either undoped polysilicon or N^{+} -doped polysilicon, all of which fall within the scope of the present invention.

The hard mask and polysilicon layer are then subjected to a photolithography and etching process. For example, a patterned photoresist layer (not shown) is first formed on the hard mask. A pattern transfer process is then performed using the patterned photoresist layer as a mask. A single etch or a series of etch steps are used to remove portions of the hard mask, polysilicon layer, and gate insulation layer. The patterned photoresist layer is then stripped to form a gate pattern 24 in the active region 14, which is composed of a patterned gate insulation layer 18, a patterned polysilicon layer 20, and a patterned hard mask 22.

Please also refer to FIG. 2, which is a top view of the gate after the first lithography and etching process in FIG. As shown in FIG. After the first lithography and etching process, a plurality of elongated gate patterns 24 are preferably formed on the semiconductor substrate 12 in this embodiment. Each gate pattern 24 is composed of a patterned gate insulation layer 18, a patterned polysilicon layer 20, and a patterned hard mask 22.

Then, as shown in FIG. 3, a first stage sidewall sub-process is performed. For example, a silicon oxide layer (not shown) and a silicon nitride layer (not shown) are sequentially formed on the semiconductor substrate 12. Then, portions of the silicon oxide layer and the silicon nitride layer are removed by etching back to form a first sidewall sub-process 30 composed of a silicon oxide layer 26 and a silicon nitride layer 28 on the sidewall of the gate pattern 24.

A selective epitaxial growth (SEG) process is then performed to form strained silicon in the semiconductor substrate 12. For example, a patterned photoresist layer (not shown) can be formed on the semiconductor substrate 12, and an etching process can be performed to form two recesses 34 in the semiconductor substrate 12 on both sides of the gate pattern 24. A surface cleaning process is then performed to completely remove native oxide and other impurities from the surface of the recesses 34. A selective epitaxial growth process is then used to substantially fill the two recesses 34 to form an epitaxial layer 36. In this embodiment, a shallow doping process can be performed before forming the first sidewalls 30 and the epitaxial layer 36 to implant N-type or P-type dopants into the semiconductor substrate 12 on both sides of the gate pattern 24 to form a lightly doped drain 32. In this embodiment, the material of the epitaxial layer 36 can be adjusted according to the characteristics of the transistor or process requirements, but is not limited thereto.

For example, if the transistor to be manufactured is a PMOS transistor, it is preferred to form an epitaxial layer 36 composed of silicon germanium in the groove 34, and the epitaxial layer 36 can apply a compressive stress to the channel region of the PMOS transistor.

Conversely, if the transistor being fabricated is an NMOS transistor, it is preferred to grow an epitaxial layer 36 made of silicon carbide (SiC) in the recess 34. This epitaxial layer applies tensile strain to the channel region of the NMOS transistor to enhance the electron mobility of the NMOS transistor.

Next, please refer to Figures 4 and 5 simultaneously. Figure 4 is a cross-sectional view continuing from Figure 3, and Figure 5 is a top view of the polysilicon gate of this embodiment. As shown in these figures, the hard mask 22 on the polysilicon layer 20 is first removed, and then a sidewall material layer is formed. For example, a silicon oxide layer (not shown) and a silicon nitride layer (not shown) are sequentially deposited on the semiconductor substrate 12. Next, a lithography and etching process is performed. For example, a patterned photoresist layer (not shown) is first formed on the polysilicon layer 20. An etching process is then performed using the patterned photoresist layer as a mask to remove only the polysilicon layer 20 located on the shallow trench isolation 16, such as the ends and the middle portion of the polysilicon layer 20. This removes at least one polysilicon opening (poly slot) 38 in the elongated gate pattern 24. This opening 38 physically separates the gate pattern 24 into two gates 46. The patterned photoresist layer is then removed and any residue remaining on the surface of the semiconductor substrate 12 is cleaned. An etch-back process is then performed on the silicon oxide layer (not shown) and the silicon nitride layer to form a second sidewall 44 composed of the silicon oxide layer 40 and the silicon nitride layer 42 on the sidewalls of the gate 46.

In this embodiment, FIG. 5 only takes a gate pattern 24 as an example and omits other doped regions, such as lightly doped drain and epitaxial layer structures.

As shown in FIG, the polysilicon opening 38 preferably separates the elongated gate pattern 24 into two portions. Furthermore, since this embodiment simultaneously removes portions of the silicon oxide layer 40 and the silicon nitride layer 42 during the formation of the polysilicon opening 38 to separate the two polysilicon gates 46, at least two opposing sidewalls of each polysilicon gate 46 after separation are free of any sidewall elements. In other words, two of the four sidewalls of the polysilicon gate 46 have second sidewall elements 44 formed of the silicon oxide layer 40 and the silicon nitride layer 42, while the other two opposing sidewalls are free of any sidewall elements.

It should be noted that the primary purpose of forming the polysilicon opening 38 after the hard mask is removed in this embodiment is to account for subsequent rework processes. Specifically, the photolithography process during the formation of the polysilicon opening 38 typically allows for rework. Prior to the rework process, the active region 14 on the semiconductor substrate 12 is exposed without any protection, as the hard mask 22 has already been removed in the previous process. However, since the oxygen introduced during rework to remove the patterned photoresist typically forms native oxide or recesses on the silicon substrate surface, it is preferable to first remove the hard mask 22 from the polysilicon layer 20 in this embodiment. The previously described silicon oxide and silicon nitride layers are then deposited on the semiconductor substrate 12. These layers serve as the material layer for the subsequent formation of the second sidewalls and also serve as a mask for etching the polysilicon opening and protecting the active region.

However, although the present embodiment takes the polysilicon opening 38 as an example after the hard mask is removed, the sequence is not limited to this. The present invention can also be used to form the polysilicon opening 38 after the hard mask is removed.

The polysilicon opening 38 may be formed at any time after the fabrication process, and this process selection also falls within the scope of the present invention.

It should also be noted that in the above-described embodiment, the process for forming the second sidewalls preferably involves sequentially depositing a silicon oxide layer and a silicon nitride layer before the etch-back process, and then performing a single etch-back to simultaneously remove portions of the silicon oxide and silicon nitride layers to form the second sidewalls. However, this approach is not limited to this approach. For example, the present invention can also deposit only a silicon oxide layer before forming the polysilicon opening, and then deposit a silicon nitride layer after the polysilicon opening is formed, thereby forming different metal oxide semiconductor transistor structures.

For example, after removing the hard mask, the present invention can first deposit a silicon oxide layer 40 on the semiconductor substrate 12, then form the polysilicon opening 38 according to the above-mentioned process, and then deposit a silicon nitride layer 42 on the semiconductor substrate 12. The silicon oxide layer 40 and the silicon nitride layer 42 are simultaneously removed by etching back to form the second sidewalls 44. As shown in FIG6, since part of the silicon oxide layer 40 is preferably removed when forming the polysilicon opening 38, the silicon oxide layer 40 of the second sidewalls 44 is only provided on two pairs of sidewalls of the gate 46. Since the silicon nitride layer 42 of the second sidewalls 44 is deposited after the polysilicon opening 38 is formed, it is preferably provided on all four sidewalls of the gate 46.

In addition, according to another embodiment of the present invention, after removing the hard mask, a silicon oxide layer 40 is first deposited on the semiconductor substrate 12, and then the silicon oxide layer 40 is deposited on the semiconductor substrate 12 according to the above method.

The above process forms a polysilicon opening 38. Next, a back-etch process is performed to remove a portion of the silicon oxide layer 40 to form a second sidewall. A silicon nitride layer 42 is then deposited on the semiconductor substrate 12. Another back-etch process is performed to remove a portion of the silicon nitride layer 42 to form a third sidewall. Although the sequence of this process differs slightly from the above embodiment, the transistor structure shown in FIG. 6 can still be fabricated.

In summary, compared to the conventional method of creating polysilicon openings before forming the epitaxial layer, the present invention preferably first defines a long polysilicon gate pattern using a first lithography and etching process, then forms the epitaxial layer on both sides of the polysilicon gate pattern, and then uses a second lithography and etching process to define the polysilicon opening and physically separate the polysilicon gate to form two gates. Because the polysilicon opening definition step is performed after the epitaxial layer is formed, the present invention avoids the aforementioned problem of epitaxial layer growth on the gate sidewalls due to low etching rates. When opening polysilicon, the etching rate is too high, which may cause epitaxial layer bridging or etching.

The above description is only a preferred embodiment of the present invention. All equivalent changes and modifications made according to the scope of the patent application of the present invention should fall within the scope of the present invention.

[Simple explanation of the diagram]

Figures 1 to 6 are schematic diagrams of manufacturing a metal oxide semiconductor transistor according to a preferred embodiment of the present invention.

[Description of main component symbols]

12	Semiconductor substrate	14	active area
16	shallow trench isolation	18	Gate insulation layer
20	polysilicon layer	22	hard mask
24	gate pattern	26	silicon oxide layer
28	Silicon nitride layer	30	first side wall
32	Lightly doped drain	34	groove
36	epitaxial layer	38	Polysilicon opening
40	silicon oxide layer	42	Silicon nitride layer
44	Second side wall	46	Gate

Invention Patent Specification

(Please do not change the format and order of this manual at will. Please do not fill in the marked parts.)

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99123277

※ Application date:

20. 7. 13

※ IPC classification:

H01L 21/336 H2006.01

H01L 21/28 H2006.01

H01L 29/18 H2006.01

1. Title of invention: (Chinese/English)

Metal-Oxide Semiconductor Transistor and Method for Fabricating the Same

2. Abstract of the invention in Chinese:

The present invention discloses a method for fabricating a metal oxide semiconductor (MOS) transistor. A semiconductor substrate is first provided, and a silicon layer is formed on the surface of the semiconductor substrate. A first lithography and etching process is then performed on the silicon layer to form a gate pattern. An epitaxial layer is then formed in the semiconductor substrate on both sides of the gate pattern. A second lithography and etching process is then performed on the gate pattern to form at least one opening (slot) in the gate pattern. The opening physically separates the gate pattern to form two gates.

3. Invention abstract in English:

A method for fabricating a metal-oxide semiconductor (MOS) transistor is disclosed. The method includes the steps of: providing a semiconductor substrate; forming a silicon layer on the semiconductor substrate; performing a first photo-etching process on the silicon layer for forming a gate pattern; forming an epitaxial layer in the

semiconductor substrate adjacent to two sides of the gate pattern; and performing a second photo-etching process on the gate pattern to form a slot in the gate pattern while using the gate pattern to physically separate the gate pattern into two gates.

7. Scope of patent application:

1. A method for manufacturing a metal oxide semiconductor transistor, comprising:

providing a semiconductor substrate;

forming a silicon layer on the surface of the semiconductor substrate;

Perform a first lithography and etching process on the silicon layer to form a gate pattern

case;

forming an epitaxial layer in the semiconductor substrate on both sides of the gate pattern;

and

After forming the epitaxial layer, a second lithography and etching process is performed

on the gate pattern to form at least one opening (slot) in the gate pattern and the gate pattern

is physically separated by the opening to form two gates.

2. The method as described in claim 1, wherein after forming the silicon layer

Also included:

forming a hard mask on the surface of the silicon layer;

The first lithography and etching process is performed on the hard mask and the silicon layer to form

Into the gate pattern;

forming a first sidewall around the gate pattern;

Form a lightly doped drain on the semiconductor substrate on both sides of the gate pattern

middle;

at least one recess in the semiconductor substrate on both sides of the first sidewall;

forming

forming the epitaxial layer in the groove;

Removing the hard mask from the surface of the silicon layer;

Form a first dielectric layer on the semiconductor substrate and cover the gate pattern case;

The second photolithography and etching process is performed on the gate pattern, the first sidewall and the first dielectric layer to form the opening in the gate pattern; and a portion of the first dielectric layer is removed to form a second sidewall.

3. The method of claim 1, wherein the semiconductor substrate further comprises at least one shallow trench isolation, and the step of forming the opening in the gate pattern further comprises removing the silicon layer on the shallow trench isolation.

4. The method of claim 2, wherein the hard mask comprises silicon nitride.

5. The method as described in claim 2, wherein the step of forming the first sidewall comprises:

forming a silicon oxide layer and a silicon nitride layer on the surface of the semiconductor substrate;

and

The silicon oxide layer and the silicon nitride layer are etched back to form the first sidewall.

6. The method of claim 2, wherein the first dielectric layer comprises a silicon oxide layer and a silicon nitride layer.

7. The method of claim 2, further comprising:

forming a second dielectric layer on the semiconductor substrate; and

Parts of the first dielectric layer and the second dielectric layer are removed to form the second sidewall.

8. The method of claim 7, wherein the first dielectric layer

The second dielectric layer comprises a silicon oxide layer and the second dielectric layer comprises a silicon nitride layer.

9. The method as described in claim 2, wherein after forming the second sidewall, the

method further comprises:

forming a second dielectric layer on the semiconductor substrate; and

A portion of the second dielectric layer is removed to form a third sidewall.

10. The method of claim 9, wherein the first dielectric layer comprises a silicon oxide layer and the second dielectric layer comprises a silicon nitride layer.

11. A metal oxide semiconductor transistor comprising:

a semiconductor substrate;

A gate is provided on the semiconductor substrate, the gate having four sidewalls, two of the four sidewalls facing each other having sidewall segments and the other two facing each other having no sidewall segments; and

An epitaxial layer is arranged on the semiconductor substrate at both sides of the sidewall.

12. The metal oxide semiconductor transistor as described in item 11 of the patent application, wherein the sidewall comprises a first sidewall and a second sidewall.

13. The metal oxide semiconductor transistor as described in item 12 of the patent application, wherein the first sidewall and the second sidewall each comprise silicon oxide and silicon nitride.

14. The metal oxide semiconductor transistor as described in item 11 of the patent application, wherein the epitaxial layer comprises silicon germanium or silicon carbide.

8. Schema:

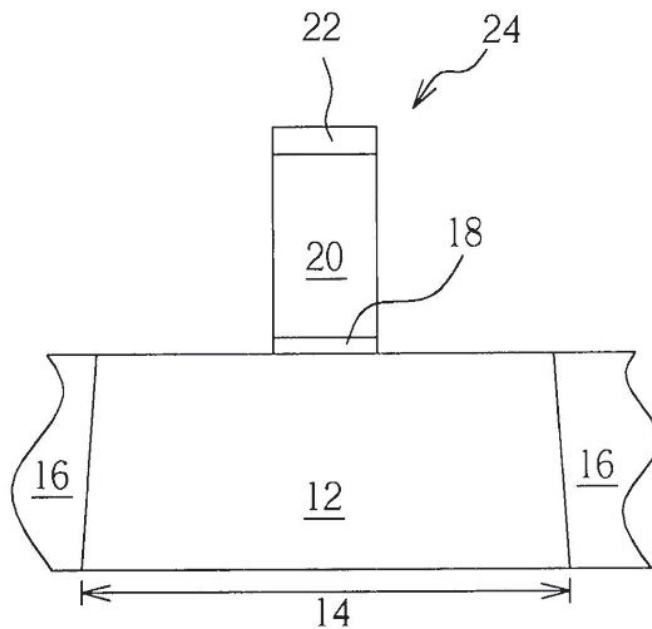
An epitaxial layer is arranged on the semiconductor substrate at both sides of the sidewall.

12. The metal oxide semiconductor transistor as described in item 11 of the patent application, wherein the sidewall comprises a first sidewall and a second sidewall.

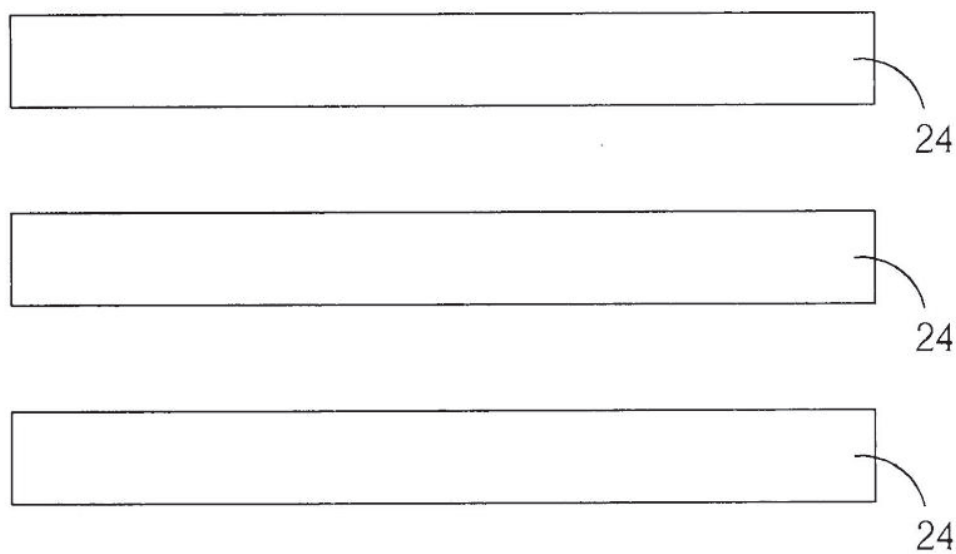
13. The metal oxide semiconductor transistor as described in item 12 of the patent application, wherein the first sidewall and the second sidewall each comprise silicon oxide and silicon nitride.

14. The metal oxide semiconductor transistor as described in item 11 of the patent application, wherein the epitaxial layer comprises silicon germanium or silicon carbide.

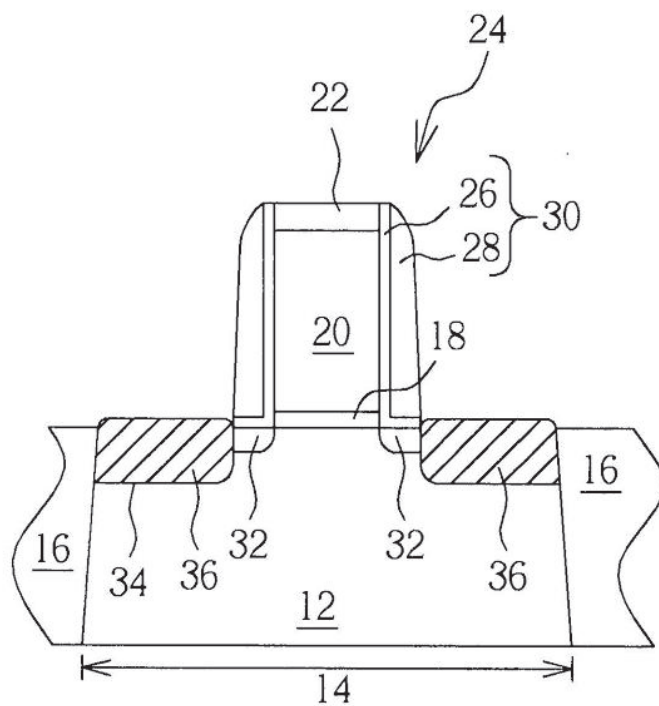
8. Schema:



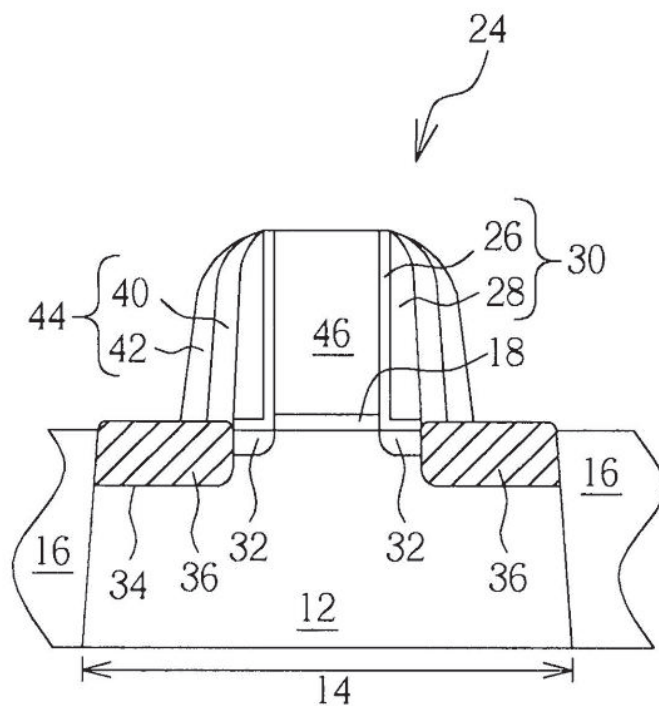
Picture 1



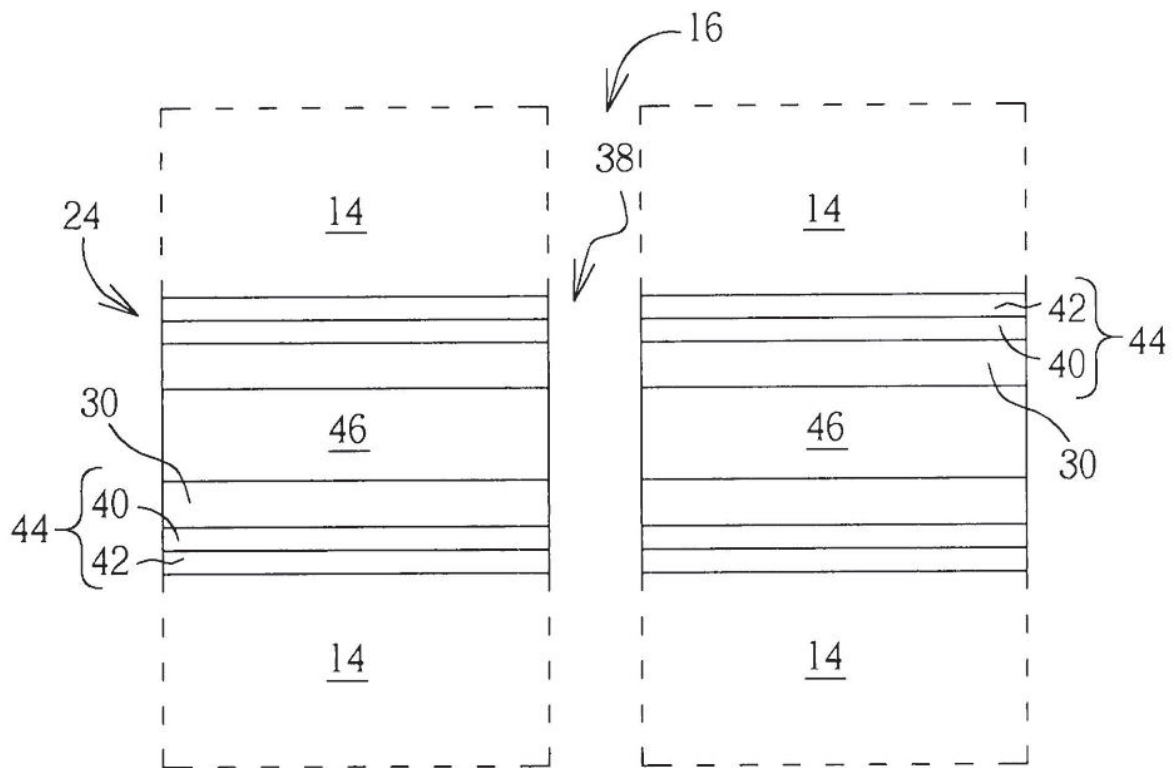
Picture 2



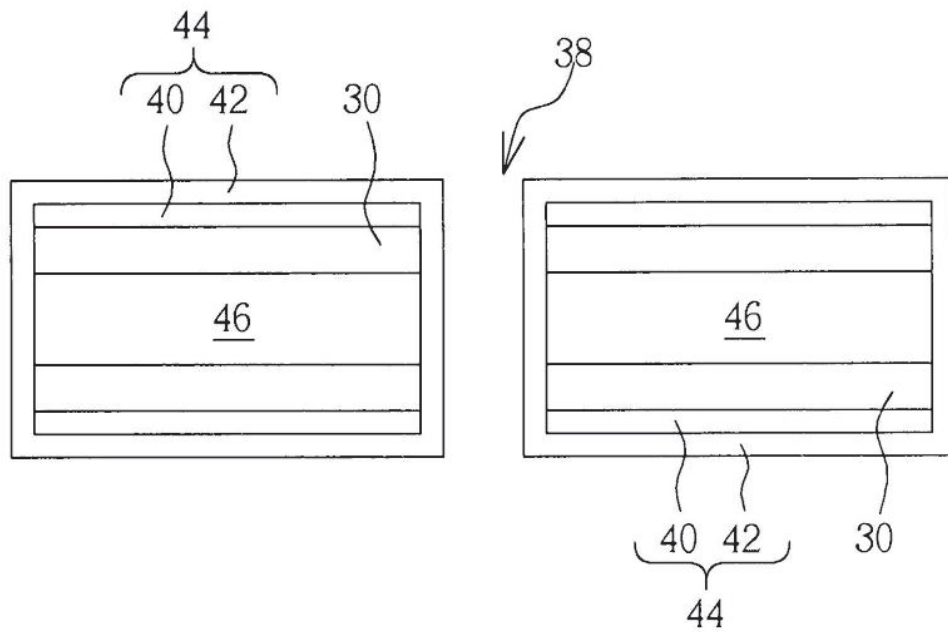
Picture 3



Picture 4



Picture 5



Picture 6

4. Designated representative picture:

(1) The designated representative figure in this case is Figure (4).

(2) Brief description of the component symbols in this diagram:

12	Semiconductor substrate	14	active area
16	shallow trench isolation	18	Gate insulation layer
24	Gate	26	silicon oxide layer
28	Silicon nitride layer	30	First side wall
32	Lightly doped drain	34	groove
36	epitaxial layer	40	silicon oxide layer
42	Silicon nitride layer	44	Second side wall
46	Gate		

5. If there is a chemical formula for this invention, please disclose the formula that best demonstrates the characteristics of the invention.

Chemical formula:

none