

071305

17712

U.S. PTO

UTILITY
PATENT APPLICATION
TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.

3771P003C

First Inventor

Daniel E. Grupp, et al.

Title

Method For Depinning The Fermi Level Of A Semiconductor At An Electrical Junction And Devices Incorporating Such Junctions

Express Mail Label No.

EV633422970US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ☒ Applicant claims small entity status.
See 37 CFR 1.27.
3. ☒ Specification [Total Pages 34]
(preferred arrangement set forth below)
- Descriptive title of the invention
 - Cross References to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference to sequence listing, a table, or a computer program listing appendix
 - Background of the invention
 - Brief Summary of the invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
4. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 6]
5. Oath or Declaration (signed) [Total Pages 5]
- a. ☐ Newly executed (original or copy)
 - b. ☒ Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 18 completed)
 - i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. ☐ Application Data Sheet. See 37 CFR 1.76

7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
- a. ☐ Computer Readable Form (CRF)
 - b. Specification Sequence Listing on:
 - i. ☐ CD-ROM or CD-R (2 copies); or
 - ii. ☐ paper
 - c. ☐ Statements verifying identity of above copies

9. ☐ Assignment Papers (cover sheet & document(s))
10. ☐ 37 C.F.R. § 3.73(b) Statement ☐ Power of Attorney
(when there is an assignee)
11. ☐ English Translation Document (if applicable)
12. ☒ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
13. ☐ Preliminary Amendment ☐ Application Amended to Reflect Claim of Priority
14. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
15. ☐ Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. ☐ Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i).
Applicant must attach form PTO/SB/35 or its equivalent.
17. ☐ Other: _____

18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76:

☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP)of prior application No: 10/217,758Prior application Information: Examiner 10/217,758Group/Art Unit: 2818

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

☒ Customer Number

08791

or ☒ Correspondence address below

Name

Tarek N. Fahmi
Blakely, Sokoloff, Taylor & Zafman LLP

Address

12400 Wilshire Boulevard, 7th Floor

City

Los Angeles

State

California

Zip Code

90025

Country

USA

Telephone

(408) 947-8200

Fax

(408) 947-8280

Name (Print/Type)

Tarek N. Fahmi

Registration No. (Attorney/Agent)

41,402

Signature

Date

07/13/05

Effective 12/08/2004
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818)

FEE TRANSMITTAL for FY 2005

Complete if Known

☒ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT (\$) 500.00

Application Number	Unknown
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Examiner Name	Unknown
Art Unit	Unknown
Attorney Docket No.	3771P003C

METHOD OF PAYMENT (check all that apply)

☒ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below

☐ Charge fee(s) indicated below, except for the filing fee

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.

☒ Credit any overpayments

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fee(s) Paid (\$)
	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	
Utility	300	150	500	250	200	100	500.00
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description

Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent

Each independent claim over 3 or, Reissues, each independent claim more than in the original patent

Multiple independent claims

Total Claims	Extra Claims	Fee (\$)	Fee Paid	Multiple Dependent Claims
1 - 20 or HP = 0	X	25.00	= \$0.00	Fee (\$)

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee (\$)	Fee Paid
1 - 3 or HP = 0	X	100.00	= \$0.00

HP = highest number of independent claims paid for, if greater than 3

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
40	- 100 = -60	/ 50 = (round up to a whole number) X		

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)

Other: _____

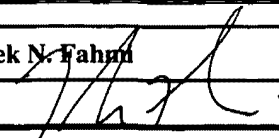
Recording of a patent assignment _____

5. TOTAL AMOUNT OF PAYMENT

(\$) 500.00

SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Tarek N. Fahmy	Registration No. (Attorney/Agent)	41,402	Telephone	(408) 947-8200
Signature				Date	07/13/05

Based on PTO/SB/17 (10-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 02/10/2004.
SEND TO: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL
JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS**

INVENTORS

**DANIEL E. GRUPP
DANIEL J. CONNELLY**

Prepared by

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1026
408-947-8200

Attorney Docket No.: 03771P003C

"Express Mail" mailing label number: EV633422970US

Date of Deposit: July 13, 2005

I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450

Geneva Walls

(Typed or printed name of person mailing paper or fee)

(Signature of person mailing paper or fee)

July 13, 2005

(Date signed)

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

RELATED APPLICATIONS

[0001] The present application is a CONTINUATION of U.S. Patent Application 10/217,758, filed August 12, 2002, incorporated herein by reference, which is related to U.S. Patent Application No. 10/342,578, filed January 14, 2003, now U.S. Patent 6,833,556, issued December 21, 2004, incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0002] The invention relates generally to semiconductor processing and semiconductor devices. More particularly, the invention relates to a process for depinning the Fermi level of a semiconductor at a metal-interface layer-semiconductor junction and to devices that employ such a junction.

BACKGROUND

[0003] One of the most basic electrical junctions used in modern devices is the metal-semiconductor junction. In these junctions, a metal (such as aluminum) is brought in contact with a semiconductor (such as silicon). This forms a device (a diode) which can be inherently rectifying; that is, the junction will tend to conduct current in one direction more favorably than in the other direction. In other cases, depending on the materials used, the junction may be ohmic in nature (i.e., the contact may have negligible resistance regardless of the direction

of current flow). Grondahl and Geiger first studied the rectifying form of these junctions in 1926, and by 1938 Schottky had developed a theoretical explanation for the rectification that was observed.

[0004] Schottky's theory explained the rectifying behavior of a metal-semiconductor contact as depending on a barrier at the surface of contact between the metal and the semiconductor. In this model, the height of the barrier (as measured by the potential necessary for an electron to pass from the metal to the semiconductor) was postulated as the difference between the work function of the metal (the work function is the energy required to free an electron at the Fermi level of the metal, the Fermi level being the highest occupied energy state of the metal at $T = 0$) and the electron affinity of the semiconductor (the electron affinity is the difference between the energy of a free electron and the conduction band edge of the semiconductor).

Expressed mathematically:

$$\phi_B = \phi_M - \chi_S \quad [1]$$

where Φ_B is the barrier height, Φ_M is the work function of the metal and χ_S is the electron affinity of the semiconductor.

[0005] Not surprisingly, many attempts were made to verify this theory experimentally. If the theory is correct, one should be able to observe direct variations in barrier heights for metals of different work functions when put in contact with a common semiconductor. What is observed, however, is not direct scaling, but instead only a much weaker variation of barrier height with work function than implied by the model.

[0006] Bardeen sought to explain this difference between theoretical prediction and experimental observation by introducing the concept that surface states of the semiconductor play a role in determining the barrier height. Surface states are energy states (within the bandgap between the valence and conduction bands) at the edge of the semiconductor crystal that arise from incomplete covalent bonds, impurities, and other effects of crystal termination.

Figure 1 shows a cross-section of an un-passivated silicon surface labeled 100. The particular silicon surface shown is an Si(100) 2x1 surface. As shown, the silicon atoms at the surface,

such as atom 110, are not fully coordinated and contain un-satisfied dangling bonds, such as dangling bond 120. These dangling bonds may be responsible for surface states that trap electrical charges.

[0007] Bardeen's model assumes that surface states are sufficient to pin the Fermi level in the semiconductor at a point between the valence and conduction bands. If true, the barrier height at a metal-semiconductor junction should be independent of the metal's work function. This condition is rarely observed experimentally, however, and so Bardeen's model (like Schottky's) is best considered as a limiting case.

[0008] For many years, the cause underlying the Fermi level pinning of the semiconductor at a metal-semiconductor junction remained unexplained. Indeed, to this day no one explanation satisfies all experimental observations regarding such junctions. Nevertheless, in 1984, Tersoff proposed a model that goes a long way towards explaining the physics of such junctions. See J. Tersoff, "Schottky Barrier Heights and the Continuum of Gap States," Phys. Rev. Lett. 52 (6), Feb. 6, 1984.

[0009] Tersoff's model (which is built on work by Heine and Flores & Tejedor, and see also Louie, Chelikowsky, and Cohen, "Ionicity and the theory of Schottky barriers," Phys. Rev. B 15, 2154 (1977)) proposes that the Fermi level of a semiconductor at a metal-semiconductor interface is pinned near an effective "gap center", which is related to the bulk semiconductor energy band structure. The pinning is due to so-called metal induced gap states (MIGS), which are energy states in the bandgap of the semiconductor that become populated due to the proximity of the metal. That is, the wave functions of the electrons in the metal do not terminate abruptly at the surface of the metal, but rather decay in proportion to the distance from that surface (i.e., extending inside the semiconductor). To maintain the sum rule on the density of states in the semiconductor, electrons near the surface occupy energy states in the gap derived from the valence band such that the density of states in the valence band is reduced. To maintain charge neutrality, the highest occupied state (which defines the Fermi level of the semiconductor) will then lie at the crossover point from states derived from the

valence band to those derived from the conduction band. This crossover occurs at the branch point of the band structure. Although calculations of barrier heights based on Tersoff's model do not satisfy all experimentally observed barrier heights for all metal-semiconductor junctions, there is generally good agreement for a number of such junctions.

[0010] One final source of surface effects on diode characteristics is inhomogeneity. That is, if factors affecting the barrier height (e.g., density of surface states) vary across the plane of the junction, the resulting properties of the junction are found not to be a linear combination of the properties of the different regions. In summary then, a classic metal-semiconductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, MIGS and inhomogeneities.

[0011] The importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction. Thus, if one were able to control or adjust the barrier height of a metal-semiconductor junction, one could produce electrical devices of desired characteristics. Such barrier height tuning may become even more important as device sizes shrink even further. Before one can tune the barrier height, however, one must depin the Fermi level of the semiconductor. As discussed in detail below, the present inventors have achieved this goal in a device that still permits substantial current flow between the metal and the semiconductor.

SUMMARY OF THE INVENTION

[0012] The present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal – interface layer – semiconductor junction, there exist corresponding minimum specific contact resistances. The interface layer thickness corresponding to this minimum specific contact resistance will vary depending upon the materials used, however, it is a thickness that allows for depinning the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor when the junction is biased (e.g., forward or reverse biased). By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the effect of MIGS has been overcome, or at least reduced, by displacing the semiconductor a sufficient distance from the metal. Minimum specific contact resistances of less than or equal to approximately $10 \Omega - \mu m^2$ or even less than or equal to approximately $1 \Omega - \mu m^2$ may be achieved for such junctions in accordance with the present invention.

[0013] Thus, in one embodiment, the present invention provides an electrical device in which an interface layer is disposed between and in contact with a metal and a silicon-based semiconductor and is configured to depin the Fermi level of the semiconductor while still permitting current flow between the metal and the semiconductor when the electrical device is biased. The specific contact resistance of the electrical device is less than approximately $10 \Omega - \mu m^2$. The interface layer may include a passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and sometimes also includes a separation layer. In some cases, the interface layer may be essentially a monolayer (or several monolayers) of a semiconductor passivating material.

[0014] In another embodiment, the interface layer is made up of a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material, for example ammonia

(NH₃), nitrogen (N₂) or unbound gaseous nitrogen (N) generated from a plasma process. In such cases, the interface layer may be fabricated by heating the semiconductor while in a vacuum chamber and exposing the semiconductor to the nitrogenous material.

[0015] A further embodiment of the present invention provides for depinning the Fermi level of a semiconductor in an electrical junction through the use of an interface layer disposed between a surface of the semiconductor and a conductor. The interface layer preferably (i) is of a thickness sufficient to reduce effects of MIGS in the semiconductor, and (ii) passivates the surface of the semiconductor. Despite the presence of the interface layer, significant current may flow between the conductor and the semiconductor because the thickness of the interface layer may be chosen to provide a minimum (or near minimum) specific contact resistance for the junction. As indicated above, the interface layer may include a passivating material such as a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride.

[0016] Further embodiments of the present invention provide a junction between a semiconductor and a conductor separated from the semiconductor by an interface layer configured to allow a Fermi level of the conductor to (i) align with a conduction band of the semiconductor, (ii) align with a valence band of the semiconductor, or (iii) to be independent of the Fermi level of the semiconductor. In some or all of these cases, current may flow between the conductor and the semiconductor when the junction is biased because the interface layer has a thickness corresponding to a minimum or near minimum specific contact resistance for the junction. For example, specific contact resistances of less than or equal to approximately $2500\ \Omega - \mu m^2$, $1000\ \Omega - \mu m^2$, $100\ \Omega - \mu m^2$, $50\ \Omega - \mu m^2$, $10\ \Omega - \mu m^2$ or even less than or equal to $1\ \Omega - \mu m^2$ may be achieved.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0017] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0018] **Figure 1** shows a cross-section of an un-passivated silicon surface containing surface silicon atoms with dangling bonds.

[0019] **Figure 2** illustrates various energy levels for metals and semiconductors and is labeled to show the work function of a metal and the electron affinity of a semiconductor.

[0020] **Figure 3** shows an energy band diagram for a conventional metal – *n*-type semiconductor junction and also illustrates the concept of a depletion region formed in the semiconductor when the materials are brought into contact with one another.

[0021] **Figure 4** illustrates band bending at a conventional metal – *n*-type semiconductor junction.

[0022] **Figure 5** shows a semiconductor device containing a semiconductor material having a surface across which electrical current flows during operation of the semiconductor device, and containing an interface layer formed on the surface according to one embodiment of the present invention.

[0023] **Figure 6** shows an electrical junction containing an interface layer that is disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

[0024] **Figures 7a, 7b, 7c and 7d** show relationships between Fermi energy, conduction-band energy, and valence-band energy for an unpassivated Schottky diode, a passivated Schottky diode in which MIGS are not removed, an unpassivated Schottky diode in which

MIGS are removed and a passivated Schottky diode in which MIGS are removed according to one embodiment of the present invention, respectively.

[0025] **Figure 8** shows a curve of interface layer resistance versus interface layer thickness for an electrical junction containing an interface layer disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0026] Described herein are processes for depinning the Fermi level of a silicon-based semiconductor (e.g., Si, SiC or SiGe) at a metal-semiconductor junction as well as devices that use such a junction. As more fully discussed below, an interface layer is introduced between the semiconductor and the metal. The interface layer functions to passivate the semiconductor surface (that is, terminate dangling bonds that may otherwise be present at the semiconductor surface so as to assure chemical stability of the surface) and to displace the semiconductor from the metal so as to reduce the effect of MIGS.

[0027] As discussed more fully below, the present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal – interface layer – semiconductor junction, there exist corresponding minimum specific contact resistances. Indeed, minimum specific contact resistances of less than or equal to approximately $10 \, \Omega - \mu m^2$ or even less than or equal to approximately $1 \, \Omega - \mu m^2$ may be achieved for such junctions in accordance with the present invention. To achieve such low contact resistances, a metal that has a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function that is near the valence band for p-type semiconductors, is selected.

[0028] The Schottky barrier in such junctions is already minimized, meaning that it is much less than the Schottky barrier presented by a junction in which the Fermi level is pinned, generally near the middle of the semiconductor's bandgap. The current versus voltage (IV) characteristic of these junctions is non-linear, generally having a slope that increases as the voltage increases, such that the derivative of current with respect to voltage is increasing with voltage. This results in a decreasing differential resistance (dV/dI) and a decreasing resistance (V/I). Thus, a junction that has high resistance or high differential resistance near the origin of the IV characteristic (zero volts) may have significantly lower resistance or lower differential resistance at higher voltages.

[0029] The present invention achieves low resistance and low differential resistance near the origin of the current-voltage characteristic for a metal – interface layer – semiconductor junction. Generally, the voltage around the origin should be less than about 100 mV, or more preferably less than about 10 mV for purposes of measuring, determining, or utilizing such junctions of low resistance. At higher voltages, the junction resistance will be even lower. It is thus a feature of the present invention to set an upper bound on the resistance of a contact, where the upper bound occurs at low voltages.

[0030] It is further noted that in junctions where the Schottky barrier is minimized as described above, such that the Fermi level at the junction interface at zero volts lies at or near the conduction band edge or valence band edge (for *n*- and *p*-type semiconductors, respectively), the *IV* characteristic will be nearly symmetric, especially at low voltage. In this case, the term “forward bias” is not defined in the usual sense of a diode wherein forward bias corresponds to the direction of bias for which greater current flows. Thus, in determining or utilizing low resistance junctions of the present invention, the voltage may be either positive or negative.

[0031] It is also possible (in accordance with a further embodiment of the present invention) to make junctions where the Schottky barrier is higher than it would be if the Fermi level at the junction interface were pinned, usually around mid-gap of the semiconductor. Such junctions are formed in the present invention between a metal with a workfunction near or substantially equal to the conduction band edge of a *p*-type semiconductor, or between a metal with a workfunction near or substantially equal to the valence band edge of an *n*-type semiconductor. These junctions are diodes, in that little current will flow if the *n*-type (*p*-type) semiconductor is biased positive (negative) with respect to the metal, and large currents will flow if the voltage is reversed. The low-current flow state is referred to as reverse bias, and the high-current flow state is referred to as positive bias.

[0032] Low resistance in the case of a diode is only relevant in forward bias conditions. In junctions created in accordance with the present invention the resistance contribution of the

interface layer is smaller than the resistance due to the Schottky barrier. That is, in forward bias conditions for junctions created in accordance with the present invention, the transport of charge is limited mainly by the thermal emission of carriers from the semiconductor over the barrier at the interface, and not by the tunneling through the interface dielectric. Thus, low resistance in the case of a diode refers to a resistance lower than the resistance presented by the Schottky barrier.

[0033] In certain applications of diodes, the ability to withstand high reverse biases may be more desirable than high current flow in forward bias. These applications would be considered high voltage/low power applications. In such cases, a low resistance is not essential, and junctions created in accordance with still another embodiment of the present invention provide high-voltage diodes capable of withstanding voltages higher than could otherwise be achieved if the Fermi level of the semiconductor in the junction were pinned.

[0034] The present invention is discussed below in terms of presently preferred embodiments thereof, however, this discussion is not meant to limit the scope of the invention. By studying the present disclosure, others of ordinary skill in the art may recognize equivalent procedures, materials or structures that can be substituted for those described herein to achieve the same effect. The reader is advised and reminded that the use of such equivalents is deemed to be within the scope of the present invention. For example, where the discussion refers to well-known structures and devices, block diagrams are used, in part to demonstrate the broad applicability of the present invention to a wide range of such structures and devices.

I. Introduction and Definitions

[0035] The present discussion makes use of terms that, although well known in the art, may not be familiar to all readers. Therefore, before beginning a detailed discussion of the present invention, it is helpful to define certain terms and concepts. To understand the properties of metal-semiconductor junctions and the impact of the present invention, one must refer to some important energy scales, which are shown graphically in **Figure 2**. The so-called vacuum

level (E_0) represents the minimum energy that an electron needs to possess in order to completely free itself from a metal or semiconductor. For a metal, the Fermi level (E_F) represents the highest occupied energy level for the material. That is, nearly all energy states below the Fermi level are filled, while nearly all states above the Fermi level are empty. The work function of the metal (Φ_M) is then defined as the energy required to free an electron at the Fermi level and mathematically it is the difference between the vacuum level and the Fermi level. The work function is an invariant bulk property of the metal.

[0036] As illustrated in the diagram, semiconductors also have a Fermi level (E_F) and a work function (Φ_S), however, the work function is not an invariant property of the semiconductor. Because the Fermi level varies depending on the doping level in the semiconductor (i.e., the relative amounts of impurities introduced into the semiconductor crystal which change the electron and hole carrier concentrations), a separate parameter, the electron affinity (χ_S), is defined. The electron affinity is an invariant property of the semiconductor and is the difference between the vacuum level and the conduction band edge of the semiconductor. In a semiconductor, almost all energy states are filled in the valence band (E_V) while the conduction band (E_C) is almost empty.

[0037] Now consider a conventional junction between a metal and an *n*-type semiconductor that has a work function smaller than the work function of the metal (i.e., $\Phi_S < \Phi_M$). An *n*-type semiconductor is one in which electrons are the majority charge carriers (in *p*-type semiconductors, holes are the majority charge carrier). As shown in **Figure 3**, because the Fermi level in the semiconductor is higher than the Fermi level in the metal, electrons transfer from the semiconductor 310 to the metal 320 when the materials are brought into contact. Thus, a depletion region (i.e., a region in which there are no free charge carriers) 330 forms near the junction interface 340.

[0038] The formation of the depletion region gives rise to an electric field and so-called “band bending”, as one approaches the junction interface from the semiconductor side (see **Figure 4**). The band bending creates an energy barrier (discussed above) that blocks further

transfer of electrons into or out of the semiconductor. Similar barriers are formed for a junction between a metal and a *p*-type semiconductor when the work function of the metal is less than the work function of the semiconductor. However, in the case of a metal-*n*-type semiconductor junction in which the work function of the semiconductor is greater than that of the metal or a metal-*p*-type semiconductor junction in which the work function of the semiconductor is less than that of the metal, no such energy barriers are created and the contact is said to be ohmic in nature.

[0039] As discussed above, although Schottky first postulated that the height of the energy barrier (Φ_b) formed at a metal-semiconductor junction was simply the difference between the work function of the metal and the electron affinity of the semiconductor, experiments have not verified this relationship. Instead a more complex explanation that takes into account the effects of surface defect states, inhomogeneities and MIGS appears to provide more accurate estimates of barrier heights by explaining the pinning of the Fermi level in the semiconductor. The present inventors have created a technique which is believed to depin the Fermi level of a Si-based semiconductor at a junction with a metal (and thus allow for control or tuning of the barrier height) by both passivating the semiconductor surface (to eliminate or at least reduce the effects of surface states and possibly inhomogeneities) and displacing the metal from the semiconductor (to eliminate or at least reduce the effects of MIGS). This depinning is achieved by introducing an interface layer between the semiconductor and the metal to create a semiconductor -- interface layer -- metal junction, which still permits significant current to flow between the metal and the semiconductor when the junction is forward biased.

[0040] This latter point is important. As discussed further below, for contacts where the energy bands of the semiconductor and the conductor align (i.e., where the Fermi level of the conductor aligns with the conduction or valence band of the semiconductor depending on semiconductor type and/or contact application), if the interface layer is too thin, the specific contact resistance of the junction increases because of the presence of MIGS, resulting in an increased barrier height; thus, current flow is hampered. Conversely, if the interface layer is

too thick, the specific contact resistance is again increased and one gets low current across the junction because of tunneling limitations. The present invention achieves an interface layer that is thick enough to reduce or eliminate the effect of MIGS, while still thin enough to permit significant current flow.

II. Passivation of Semiconductor Surfaces

[0041] A common processing operation performed during semiconductor device fabrication is silicon surface passivation. Surface passivation (whether by an oxide or another material) chemically neutralizes and physically protects the underlying silicon. For example, exposing a silicon surface to oxygen (under the appropriate conditions to grow a protective film of silicon dioxide) will allow the oxygen to react with the dangling bonds of the silicon surface to form covalent bonds that satisfy the surface silicon atoms' valency and render the surface fully coordinated. These covalent bonds provide chemical stability to the silicon surface. The covalent bonds also tie up unbound charges that exist on the silicon surface as a result of the discontinuation of the semiconductor crystal at the surface.

[0042] However, passivation with silicon dioxide has several significant disadvantages. For example, silicon dioxide is a dielectric insulator that poses a significant barrier to the flow of current. Accordingly, a layer of silicon dioxide deposited or grown on a silicon surface may significantly reduce the ability for electrical current to flow through that surface. As a result, the use of silicon dioxide has been limited in practicality to surfaces external to the active region of semiconductor devices through which current passes during device operation (e.g., as a gate oxide layer). This disadvantage is compounded by the fact that the silicon dioxide grows very rapidly and readily on the silicon surface so that it is difficult to limit the growth to a thin layer. Silicon dioxide is also a poor diffusion barrier to semiconductor dopants such as boron.

[0043] Instead of making use of silicon dioxide then, in one embodiment the present inventors utilize a nitrided semiconductor surface to provide chemical passivation. That is, a

nitride layer is introduced to passivate the semiconductor surface by eliminating or at least reducing the effects of surface states and possibly inhomogeneities. The nitride layer also displaces the metal from the semiconductor and eliminates or at least reduces the effects of MIGS. The result of introducing the nitride layer as an interface between the semiconductor and the metal is a depinning of the Fermi level of the semiconductor. When the Fermi level of the semiconductor is depinned, the Fermi level of the metal at the interface will be that of the bulk metal, and will not be dependent upon the interface. In addition to the above, the present inventors propose techniques for providing non-insulating, passivated semiconductor surfaces using materials other than nitrogen; for example, oxides, hydrides, arsenides and/or fluorides.

[0044] These developments have wide applicability in connection with the fabrication of Schottky diodes, Schottky-barrier transistors and other electrical components. For example, in Schottky diodes, the ability to control the energy barrier height at the diode junction is important if the device is to be tailored to specific applications. Use of the present techniques allows for tuning of the barrier height. Further, for other three-terminal devices with Schottky-barrier-isolated channels, control of device characteristics is made possible through the present invention by allowing *n*- and *p*-type devices to be fabricated without dopants, relying instead on the use of metals with different work functions.

[0045] **Figure 5** shows a semiconductor device 510 that contains a semiconductor 530 and an interface layer 520 formed on a surface 540 of the semiconductor in accordance with the present invention. The terms semiconductor device, microelectronic device, monolithic device, chip, and integrated circuit are often used interchangeably in this field. Any or all such devices may each contain an interface layer formed on a semiconductor surface in accordance with the present invention.

[0046] The semiconductor 530 contains a semiconductor material. The term semiconductor material refers to a material having a bandgap that is greater than about 0.1 eV and less than about 4 eV. The term bandgap refers to an energy gap of forbidden energy levels separating the conduction band, which is an upper energy band that is mostly devoid of electrons and

wherein electrons can conduct, and the valence band, which is an energy band that is mostly filled with electrons and wherein electrons cannot conduct. The semiconductor material may have a wide range of doping levels including no doping at all.

[0047] The semiconductor 530 has a surface 540 that is passivated by the interface layer 520. In this context (and as used elsewhere herein) the term passivation means the elimination or at least the reduction of the effects of surface states due to defects or dangling bonds of the semiconductor surface 540. Note that passivation does not, as a practical matter, require that all surface states be eliminated. Rather, it is the effect of surface states on the device properties that is limited or eliminated in passivation. Note further that the presence of MIGS may be regarded as a surface state, however, as used herein the term passivation is not meant to infer the elimination of MIGS (though in some cases, a passivation layer may have sufficient thickness to provide a separation layer between the semiconductor and the metal sufficient to reduce or eliminate MIGS). The semiconductor 530 is operable to be electrically coupled with a first voltage associated with the semiconductor device 510 and to conduct electrical current 550 across the passivated surface 540.

[0048] The interface layer 520 is formed on the semiconductor 530 and may contain a passivation material that bonds to the semiconductor material by way of a covalent (or other) bond formed between the passivation material and the semiconductor material. For example, an atom of passivation material may covalently bond with a dangling bond of a surface silicon atom to fully coordinate the silicon atom and thereby help passivate the silicon atom. In some cases, the passivation material may be the sole component of the interface layer 520, while in other cases the interface layer 520 may be a compound layer that includes both a passivation layer and a separation layer. That is, the interface layer serves to (i) chemically passivate the semiconductor surface 540, and (ii) displace the semiconductor from the metal sufficiently to eliminate or at least reduce the effect of MIGS. As explained below, this may necessitate including a separation layer in addition to a passivation layer within the interface layer, depending on the passivation material selected. Of course, the combination of the passivation

layer and the separation layer must be sufficiently thin to permit the low specific contact resistances described herein.

[0049] Different passivation materials are contemplated. According to one embodiment, the interface layer 520 is formed using a material that is preferably selected from the group consisting of hydrogen (H), oxygen (O), nitrogen (N), arsenic (As), and fluorine (F) (that is, the interface layer 520 may include a nitride, an oxide, a hydride, an arsenide and/or a fluoride). Other materials having chemical characteristics or valences similar to these materials may also be used. Note that distinct separation layers (i.e., in addition to the passivation layer(s)) may be needed where H, As, or F passivation layers are used, as these tend to form monolayer coverage, rather than a layer of a compound with Si of process-dependent thickness. In contrast, passivation layers made using N and/or O may not require distinct separation layers, as these elements may form a layer of a compound of Si with a thickness that can be varied depending on processing.

[0050] Different amounts of passivation material are contemplated to be useful for different embodiments of the present invention. Often, the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm. For example, depending upon the particular implementation, the thickness may be less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, may be the thickness corresponding to a single layer or monolayer of passivation material that is bonded to the semiconductor surface, or may even be the number of atoms of passivation material required to passivate substantially all the dangling bonds associated with the semiconductor surface 540.

[0051] In some cases, passivation of the semiconductor surface 540 will include removing (or terminating) dangling bonds located proximate to the surface of the semiconductor material, including those at the surface as well as those within a few molecular dimensions from the surface. This process may stabilize the surface of the semiconductor material and may improve the controllability of subsequent fabrication operations. Passivation may also reduce the density of surface states that may exist at the semiconductor surface as a result of the

discontinuation of the semiconductor crystal at the surface. This may improve consistency and performance of the semiconductor device, inasmuch as such states are known to interfere with proper device operation. For example, they may provide surface charge states that result in a pinning of the Fermi level.

III. Forming Interface Layers

[0052] Exemplary methods for forming interface layers to provide (i) passivation of semiconductor surfaces, and (ii) displacement of the semiconductor from the metal to eliminate or at least reduce of the effects of MIGS within the semiconductor when in the presence of the metal (collectively referred to herein as depinning the Fermi level of the semiconductor) with hydrogen, fluorine or nitrogen are presented below to further illustrate the concepts of the present invention. Other passivation materials may include arsenic, oxygen or an oxynitride, and in some cases such passivation layers are combined with separation layers (e.g., made of an oxide) to complete the interface layer.

A. Hydrogen And Fluorine

[0053] An interface layer may contain hydrogen, fluorine, or both hydrogen and fluorine (e.g., in the form of a hydride and/or a fluoride). One method for forming an interface layer on a semiconductor surface with hydrogen and fluorine includes cleaning the semiconductor substrate with a cleaning solution, immersing the cleaned substrate in a hydrogen fluoride solution (or other liquid containing hydrogen and fluorine ions) having an effective concentration typically between about 1%-50% by weight, waiting an effective period of time, typically between about several seconds and about 5 minutes, removing the substrate from the hydrogen fluoride solution, optionally rinsing the substrate in deionized water, and blow-drying the substrate with nitrogen. Such a method may form an interface layer containing hydrogen and fluorine that are bonded (e.g., covalently) to the semiconductor surface.

[0054] It should be noted that long rinses in deionized water, generally longer than about 30 seconds, might remove the hydrogen passivation. Thus, deionized water rinses might advantageously be kept to less than about 30 seconds to maintain the hydrogen passivation of the surface. Also, the higher the concentration of the hydrogen fluoride during the immersion, the greater the concentration of fluorine passivation. Finally, methods are also contemplated where the ratio of hydrogen to fluorine passivation is altered by removing either the hydrogen or the fluorine.

[0055] An interface layer formed in this fashion may be best suited for applications where a subsequent metal layer is deposited over the interface layer in a generally non-invasive fashion, for example using a thermally evaporated source. Experiments by the present inventors to date suggest that using other approaches (e.g., plasma deposition) may cause damage to the thin (e.g., monolayer thick) interface layer contemplated as part of the present invention.

B. Nitrogen

[0056] In a further embodiment, an interface layer may contain nitrogen (e.g., in the form of silicon nitride). One method for forming an interface over a semiconductor surface with nitrogen includes heating a substrate containing the semiconductor surface in the presence of a nitrogenous material (that is, a gas or other material containing nitrogen). For example, a substrate containing an exposed silicon surface may be annealed at a temperature between about 300°C and about 750°C, which is lower than temperatures conventionally used for Rapid Thermal Nitridation (RTN), under a gaseous ambient having, for example, ammonia (NH₃) at some effective partial pressure. By exposed, we mean a clean surface, free of everything except silicon. Such a method may form an interface layer containing nitrogen, often in the form of a nitride, bonded to the semiconductor surface. Note that the present inventors have observed indications suggesting that in these low temperature conditions interface layer growth is self-limiting, depending only on temperature.

[0057] According to another embodiment, an interface layer that includes nitrogen may be formed on an exposed surface of a semiconductor material by a method that includes heating a semiconductor material to a substantially high temperature under vacuum and exposing the semiconductor material to a substantially small amount of a nitrogenous material, such as ammonia. The method may include placing a semiconductor having an exposed semiconductor surface in a heating chamber, pulling a vacuum of less than about one millionth of a Torr, or more favorably an ultra high vacuum of less than 10^{-9} Torr, and then heating the semiconductor in the heating chamber to a substantially high temperature. The higher the vacuum, the longer the substrate may be heated without growth of an oxide from residual oxygen or water in the chamber. Thus, the process may include heating the semiconductor to a temperature that is between about 900°C and about 1000°C, or higher, in an inert ambient. As desired, the semiconductor may be exposed to hydrogen gas, or an equivalent, to reduce any native oxide on the semiconductor. These high temperatures may provide for greater passivation of the semiconductor surface as compared with results that may be achieved at lower temperatures.

[0058] Then, the heated semiconductor may be exposed to a substantially small amount of a nitrogenous material, such as ammonia. This may include exposing the semiconductor surface to ammonia for a substantially short period of time. For example, the surface may be subjected to a burst or pulse of ammonia lasting for a time period between about 0.5 seconds and about 5 seconds. Alternatively, the surface may be exposed to a controlled, small amount of ammonia over an arbitrarily longer period of time. In this way, the substantially small amount of ammonia will react with the surface to form a nitrogenous interface layer, such as a nitride layer, thereon and then further growth of the interface layer will cease. Then the semiconductor may be cooled from the substantially high temperature to ambient temperature and removed from the heating chamber. Further annealing of the substrate and the grown nitride layer may also be performed in the vacuum chamber before removal, at a substantially elevated temperature between about 700°C and 1000°C, or higher.

[0059] Advantageously, it has been unexpectedly observed that a process such as that described above and incorporating substantially high temperature exposure for substantially short periods may be used to controllably form thin yet effective interface layers. That is, the present inventors have observed that in the creation of thin interface layers that include nitrogenous materials, temperature appears to be a dominant factor in controlling thickness. For example, by such methods effective interface layers may be formed having a thickness that is less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the semiconductor surface.

[0060] Further, thin interface layers may be advantageously grown on a semiconductor in the presence of nitrogen gas, or other inert nitrogen-containing gas. The reaction rate of a semiconductor such as silicon with nitrogen gas is significantly lower than that of a reactive nitrogen-containing gas such as ammonia. The slow growth rate may be desirable for better control of the growth of films of nitrogen on a semiconductor of a thickness of less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the silicon surface.

IV. Diodes Containing Passivated Semiconductor Surfaces

[0061] Diodes made from Schottky barriers (i.e., asymmetric electrical potentials formed at a junction between a metal and a semiconductor) are widely used in rectifiers in power supply and control applications. As used herein, the terms Schottky diode, metal-semiconductor junction diode, diode, and rectifier are all related and appear in order from more specific at the left to more general at the right. Likewise, the terms Schottky barrier, metal-semiconductor barrier, conductor-semiconductor junction, and multi-material junction are all related and

appear in order from more specific at the left to more general at the right. The term Schottky diode will be used to refer to a diode containing a Schottky barrier.

[0062] As mentioned above, the present inventors have devised a scheme to control or adjust a Schottky barrier height by forming an interface layer (which includes or sometimes consists of a passivation layer that includes an oxide, oxynitride, nitride, arsenide, hydride, fluoride, or an equivalent) between a metal and a semiconductor. This scheme differs from past attempts by others to control barrier height, which attempts generally involved either using a silicide as a contact metal (and thus limiting the choices of available contact metals to those that can form silicides), or using esoteric substrates that exhibit wide bandgaps. Further, in previous devices the Fermi level of the semiconductor remains pinned, with the barrier height being virtually independent of the metal used. Finally, doping of substrates has also been attempted, however, it has not been shown to truly affect the barrier height of the substrate material. For example, PtSi contacts have reduced resistance due to high silicon doping such that the current across the junction is dominated by tunneling through the barrier. Doping may thus lead to cases where the top of the barrier may be so thin as to be essentially transparent to electrons, however, doping does not appear to allow actual tuning of the barrier height.

[0063] **Figure 6** shows an example of a diode 600 containing, according to one embodiment of the present invention, an interface layer 620 disposed between and attached to both a semiconductor 610 and a conductor 630. The conductor and the semiconductor are operable to be electrically coupled with different voltages associated with the operation of the diode 600 and to pass electrical current through a passivated semiconductor surface formed at the junction between the semiconductor 610 and the interface layer 620.

[0064] The conductor 630 contains a conductive material such as a metal or an alloy of a metal. The terms metal, conductive material, and conductor are all related and appear in order from specific at the left to general at the right. In general, the terms refer to a highly electrically conductive substance that has a Fermi energy level that sits in a partially filled band. Unless otherwise specified, conductors include metals (e.g., pure metals and alloys),

and other conductors such as doped polysilicon (a nonporous silicon containing randomly oriented crystallites), doped single crystal silicon, and metal silicides. Note that alloys may have workfunctions different than their constituents and may be designed to have specific workfunctions though selective use of ratios of the constituent metals.

[0065] Often, the conductor is a metal since metals may offer advantages over conductive semiconductors including lower resistance, higher carrier mobilities that provide superior high frequency performance and switching, favorable low power characteristics, and ease of manufacturing control. Use of metals may also avoid the need to perform semiconductor doping, which may simplify manufacturing and improve quality control.

[0066] Metals that are contemplated include pure metals, alloys, refractory metals, metals that do not form silicides, metals physically deposited by substantially non-invasive processes such as by condensation of a thermally evaporated metal vapor, and metals having a predetermined work function. The use of non-invasively deposited metals may allow for forming the metal on a thin interface layer without disrupting the passivation properties of the layer.

[0067] A metal having a predetermined work function may be a metal having a work function smaller or greater than that of the semiconductor, depending on the desired application. Often, the semiconductor will be silicon. In this case by the work function of a semiconductor or silicon we mean the energy in the middle of the semiconductor bandgap. Exemplary metals that have a work function smaller than silicon include Group 3A elements, aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum (Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn). Exemplary metals that have a work function greater than silicon include platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Co), and palladium (Pd).

[0068] The semiconductor-interface layer-conductor configuration illustrated in **Figure 6** defines what the present inventors have chosen to call a “passivated Schottky barrier”. The

passivated Schottky barrier is a naturally formed electrical potential barrier to an electron or hole at the Fermi energy (the electrochemical potential) in the conductor due to a depletion region formed in the semiconductor adjacent the conductor. The passivated Schottky barrier may deviate in barrier height from a standard un-passivated Schottky barrier that would form naturally at a contact junction between the semiconductor and the conductor without the interface layer disposed therebetween. That is, the passivated Schottky barrier may have a barrier height that depends predominantly upon the bulk characteristics of the semiconductor and the conductor, rather than on surface properties, and may depend in part on the characteristics of the interface layer.

[0069] Indeed, the present inventors have determined that changes in barrier height are approximately monotonic and continuous for variations in surface passivation thickness by nitridation of the semiconductor substrate. More specifically, experiments by the present inventors in a regime where the nitride layer is sufficiently thick to remove MIGS show that temperature of interface layer formation has the strongest effect on barrier height. In other regimes, thickness may be critical. Ideally, if all surface states are removed, barrier height should be controllable simply by the choice of metal used.

[0070] To understand why thickness of the interface layer is important, refer briefly to **Figure 8** where a graph of interface-specific contact resistance versus interface thickness is shown. The graph is for a structure where the workfunction of the metal is the same as the electron affinity in the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the semiconductor. At large thicknesses, the interface layer poses significant resistance to current. As thickness decreases, resistance falls due to increased tunneling current. However, there comes a point where even as the interface layer continues to get thinner, resistance increases. This is due to the effect of MIGS, which increasingly pull the Fermi level of the metal down towards mid-gap of the semiconductor, creating a Schottky barrier. The present inventors have discovered that this competition results in an optimum thickness, as shown in the illustration, where the resistance is a minimum. At this thickness

the effect of MIGS has been sufficiently reduced to depin the metal and lower the Schottky barrier, and the layer is still sufficiently thin to allow significant current flow across the interface layer. Contact resistances of less than or equal to approximately $2500\ \Omega\text{-}\mu\text{m}^2$, $1000\ \Omega\text{-}\mu\text{m}^2$, $100\ \Omega\text{-}\mu\text{m}^2$, $50\ \Omega\text{-}\mu\text{m}^2$, $10\ \Omega\text{-}\mu\text{m}^2$ or even less than or equal to $1\ \Omega\text{-}\mu\text{m}^2$ may be achieved.

[0071] Characteristics that may be adjusted to provide a desired barrier height thus include the passivation material used (e.g., selection based on bandgap), the interface layer thickness (e.g., especially where the interface layer is a compound layer formed of a passivation layer and a separation layer), the method of forming the interface layer (e.g., control of parameters such as temperature), the interface layer thickness that is substantially similar to a penetration depth of MIGS formed at a metal interface, the metal used for the source and/or drain, and other characteristics.

[0072] One advantage of the ability to adjust the Schottky barrier height with the introduction of interface layer 620 is the ability to form a substantially high barrier height. For example, an interface layer may be used to create a Schottky barrier having a barrier height that is greater than can be achieved through the use of metal silicides, greater than about 2.0 eV, or greater than about 2.5 eV (using a semiconductor with a bandgap at least this large), or nearly 1.0 V using silicon. Such high barrier heights imply the ability to withstand high voltages before breakdown occurs. Thus, Schottky barriers having such high barrier heights may be particularly useful in high-voltage Schottky diodes.

[0073] Another advantage achieved through the use of the interface layer 620 is greater flexibility afforded in selecting a conductor 630. Typically, metals chosen for application in classic Schottky diodes are those that can form a silicide with a silicon semiconductor. The formation of the silicide helps to reduce surface states (resulting from dangling bonds), but not the effects of MIGS. Thus, the Fermi level at the semiconductor surface is still pinned. Using metals that form silicides upon contact with silicon may thus help to make the devices more

reproducible in a manufacturing environment, but such devices still suffer from the drawback of having a barrier height that is fixed.

[0074] According to one embodiment of the present invention, however, one may select a conductor that is not able (or not readily able) to form a silicide with the semiconductor. The metal silicide is not needed because the interface layer provided in accordance with the present invention passivates the semiconductor surface and also reduces or eliminates the effect of MIGS. This may allow for selection of a metal that has properties such as a desirable work function or Fermi level energy, even though that metal may not form a metal silicide.

[0075] For example, to make large-barrier diodes, for an *n*-type doped silicon semiconductor, a metal may be selected that has a work function that is either substantially equal to the valence band energy of the semiconductor or that is within about 0.1 eV to about 0.3 eV of the valence band energy of the semiconductor. Similarly, for a *p*-type doped silicon semiconductor, a metal may be selected that has a work function substantially equal to the conduction band energy of the semiconductor. For Schottky diodes configured in accordance with the present invention, the Fermi level of the metal may lie anywhere in the bandgap of the semiconductor when an interface layer is disposed within the junction, resulting in diodes of various barrier heights. The Fermi level of the metal may also lie in the conduction or valence band of the semiconductor.

[0076] The use of interface layer 620 thus provides a way to tune, adjust, or control the height of the barrier between the conductor and the semiconductor. Without the interface layer 620, the barrier height would be substantially un-tunable, un-adjustable, and fixed (as discussed above).

[0077] The role played by interface layer 620 in tuning, adjusting, or controlling the height of the barrier between the conductor 630 and the semiconductor 610 may be understood as a depinning of the Fermi level of the semiconductor. That is, the interface layer may reduce surface states by bonding to the semiconductor material to consume dangling bonds.

Additionally, the interface layer may reduce the formation of MIGS in the semiconductor by

providing a thickness and bandgap that prevent the electron wave function (of the metal) from penetrating into the semiconductor. The electron wave function may instead penetrate into the interface layer and form MIGS within the interface layer at an energy related to the states of the interface layer material. As desired, the density of the MIGS and the depth of MIGS penetration into the interface layer may be reduced by choosing an interface layer material or materials having a larger bandgap or higher effective mass than the semiconductor.

[0078] According to one embodiment of the present invention then, the interface layer 620 is incorporated into a device operable to pass current through the semiconductor surface and the interface layer during device operation. In such an embodiment, it may be desirable to use an interface layer having a thickness of a monolayer, or, for example between about 0.1 nm and about 0.3 nm, and also having a wide bandgap (as compared to that of the semiconductor) so that the interface layer both de-pins the Fermi level (so that the barrier height depends predominantly on bulk properties of the junction materials) and allows sufficient current transfer across it. Advantageously, such interface layers may be sufficiently thin to provide low impedance to current flow (due to the exponential dependence of direct tunneling on barrier thickness), which is desirable for many semiconductor devices, while also providing sufficient semiconductor surface passivation to allow an adjustable barrier height. That is, the interface layer may allow passivation of surface states and reduction (or elimination) of MIGS in the semiconductor to allow for an adjustable barrier height with a substantially thin layer that allows sufficient current to be transferred across the interface layer.

[0079] There are several methods by which the barrier height can be made adjustable. For example, adjustment may be made by tuning the degree of Fermi level pinning. In other words, some embodiments may allow for a sufficiently thin interface layer so that not all of the effects of MIGS in the Si are eliminated. Further, the pinning may be varied by combinations of thickness of the interface layer and the choice of interface material. The metal in contact with the interface layer may be pinned by MIGS at different levels in different materials. Conversely, or in addition, the passivation may be left incomplete to allow for an

effective level of unpassivated states. Complete depinning of the Fermi level (that is removal of all surface states in Si including MIGS) is another option, in which case one could tune the barrier height simply by choosing a pure metal or an alloy that possesses the desired workfunction. In that case, the barrier height is determined by Equation (1), which until now has been an unrealizable idealization. Note that the type of tuning being discussed here is adjustment of the barrier height by altering the structure of the junction at the time of manufacture, not by varying an externally applied condition during junction operation.

[0080] **Figure 7a – 7d** show relationships between Fermi energy, conduction band energy, and valence band energy for various Schottky barriers containing a metal in contact with (or in close proximity to) a semiconductor, where the bandgap (E_g) of the semiconductor exists between the conduction band (E_c) and the valence band (E_v). In this example, the work function of the metal Φ_M is chosen to be approximately equal to the electron affinity χ_s of the semiconductor. In **Figure 7a**, an unpassivated Schottky barrier 700 is shown. In this example, the Fermi level (E_F) of the metal 730 is pinned in the bandgap of the semiconductor 710. This results in a discontinuity in the vacuum level caused by a charged dipole at the interface.

[0081] In **Figure 7b**, the interface layer 720b is thick enough to passivate dangling bonds at the surface of the semiconductor 710, but not thick enough to eliminate or sufficiently reduce the effect of MIGS. As a result, the band structure is largely unaltered from that seen in the previous illustration. Similarly, in **Figure 7c**, when the interface layer 720c is sufficiently thick to eliminate or reduce the effect of MIGS but not to passivate the semiconductor surface, little change in the energy band structure is observed. However, as shown in **Figure 7d**, when the interface layer 720d is sufficient to both eliminate or reduce the effect of MIGS and to passivate the semiconductor surface, we see the Fermi level of the metal aligning with the conduction band of the semiconductor (i.e., the Fermi level of the semiconductor has been depinned and no longer lines up with the Fermi level of the metal). The vacuum level is now continuous as there is no charged dipole at the interface. Thus, the band structure of a device

constructed in this fashion is a result of only bulk material properties, not properties of the surface. By way of example, the materials in such cases may be Al and Si, with a work function for Al of approximately $\Phi_M = 4.1$ eV and the electron affinity for Si of approximately $\chi_s = 4.05$ eV.

V. Transistors Containing Passivated Semiconductor Surfaces

[0082] The interface layers described herein may be used in connection with a semiconductor surface of a channel in a field effect transistor. That is, an interface layer may be disposed between a source and a channel, a channel and a drain, or both of an insulated gate field effect transistor. Such use of an interface layer is described in detail in co-pending U.S. Patent Application No.: 10/342,578 entitled "INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL", filed January 14, 2003 by the present inventors, and assigned to the assignee of the present invention.

[0083] The source and drain contacts at the channel of a field effect transistor are examples of a broader category of metal-interface layer-semiconductor contacts that make up the present invention. In the past, such contacts generally comprised a silicide- n^+ -Si junction, which formed a somewhat "leaky" Schottky diode, with a Fermi level of the semiconductor pinned at the midgap. In contrast, the present invention provides a contact wherein the Fermi level of the metal is aligned with the conduction band of the semiconductor (e.g., as shown in Figure 7d). Note that in other cases, depending on the type of semiconductor material and conductors used, the Fermi level of the metal may align with the valence band of the semiconductor.

[0084] Although both types of junctions (i.e., the new passivated Schottky barrier junction and the conventional silicide-semiconductor junction) permit tunneling currents, the present junction can be fabricated with a much thinner interface layer as compared to the thickness of the silicide layer used previously. Indeed, thickness of an order of magnitude less than the silicide thickness can be expected. In a conventional silicide – semiconductor junction a Schottky barrier is formed which is comprised of a depletion layer. The tunnel barrier

presented by such a depletion layer may be an order of magnitude thicker than the dielectric tunnel barrier in the present invention. The thinner interface layers provided by the present invention permit higher current across the junction (i.e., lower junction specific contact resistance).

[0085] Two other properties of the dielectric deserve mention. First is the property of the height of the barrier compared to the semiconductor conduction band (for electrons). In making the barrier thinner than a silicide barrier, the tradeoff may be a higher tunnel barrier (e.g., 2 eV for nitride, compared with about half the gap of 0.6 eV for silicide). Spacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV). Nevertheless, even with the higher barrier to electrons, the present inventors have determined that the resistance can still be one hundred times lower than a contact to silicon with a silicide barrier.

[0086] The second property is the effective mass of electrons in the dielectric. Larger mass electrons will not penetrate as far (i.e., because of their shorter wavelength) from the metal into the semiconductor. The less the electrons penetrate into the dielectric, the less the effect of MIGS in the dielectric. Thus, MIGS in the dielectric are reduced with larger bandgap and larger effective mass.

[0087] In addition the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility). The high doping profiles were required in the past in order to keep the junction depletion layer relatively thin, so as to increase the tunneling current, thus reducing the junction resistance. However, it is becoming increasingly difficult to increase doping profiles in order to provide low resistance junctions. It may be possible to reach the same level of resistance with a lower doping concentration using the present invention. It may further be possible to achieve much lower resistance even with lower doping concentration. When the present invention is used with high doping levels, the resistance will be further reduced.

[0088] Thus, methods and applications for semiconductor-interface layer-metal junctions have been described. Although described with reference to specific embodiments it should be remembered that various modifications and changes may be made to the techniques described herein without departing from the broader spirit and scope of the invention. The specification and drawings are accordingly to be regarded in an illustrative rather than a restrictive sense and the invention measured only in terms of the claims, which follow.

CLAIMS

What is claimed is:

1. An electrical device comprising an interface layer disposed between and in contact with both a metal and a semiconductor, the interface layer being configured to depin a Fermi level of the semiconductor, and wherein the electrical device has a specific contact resistance of less than or equal to approximately $1000 \Omega - \mu m^2$.

ABSTRACT

[0089] An electrical device in which an interface layer is disposed between and in contact with a metal and a Si-based semiconductor, the interface layer being of a thickness effective to depin of the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor. The interface layer may include a layer of a passivating material (e.g., made from nitrogen, oxygen, oxynitride, arsenic, hydrogen and/or fluorine) and sometimes also includes a separation layer. In some cases, the interface layer may be a monolayer of a semiconductor passivating material. The interface layer thickness corresponds to a minimum specific contact resistance of less than or equal to $10\ \Omega\text{-}\mu\text{m}^2$ or even less than or equal to $1\ \Omega\text{-}\mu\text{m}^2$ for the electrical device.

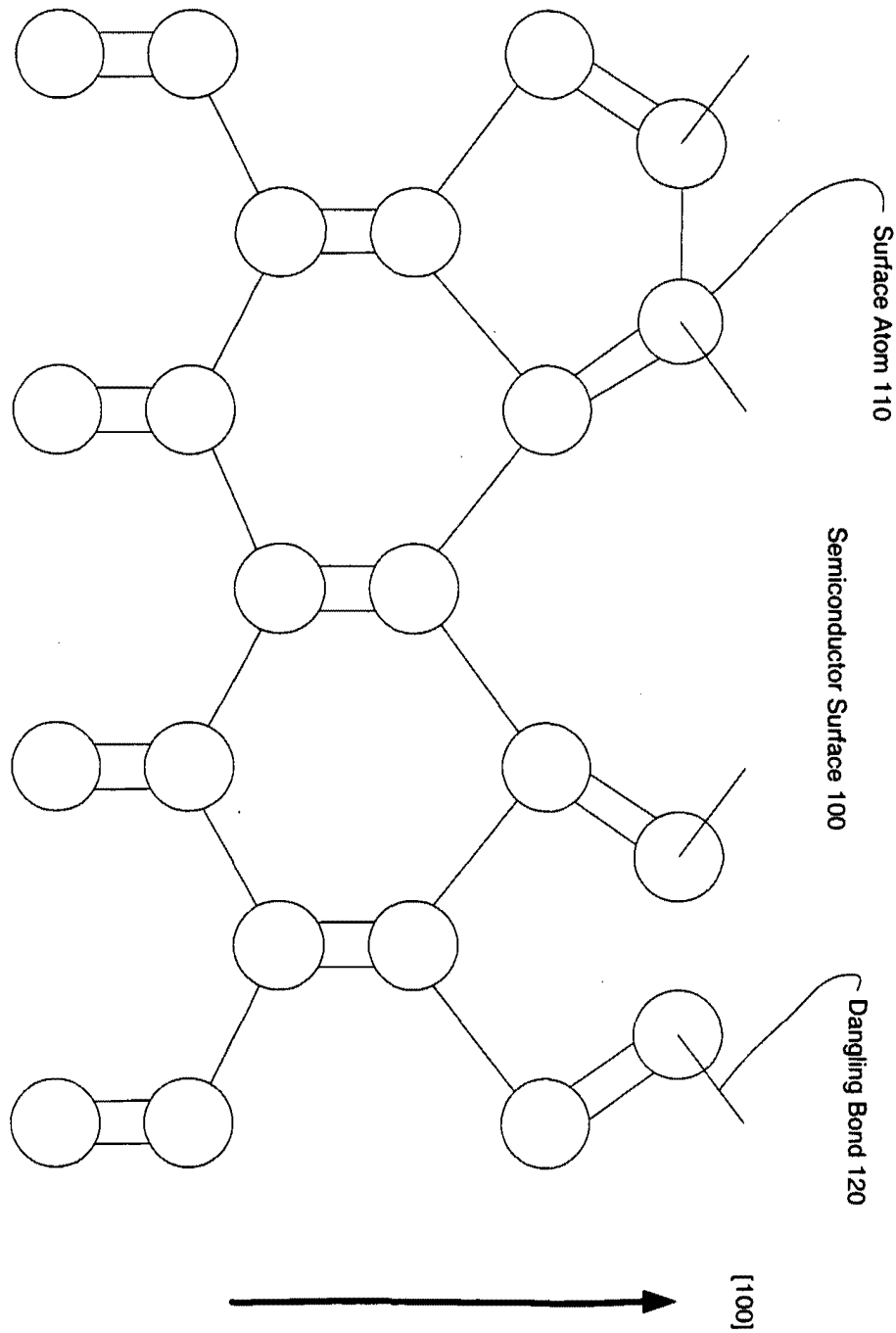


Fig. 1

Energy Scales for Metal - Semiconductor Junctions

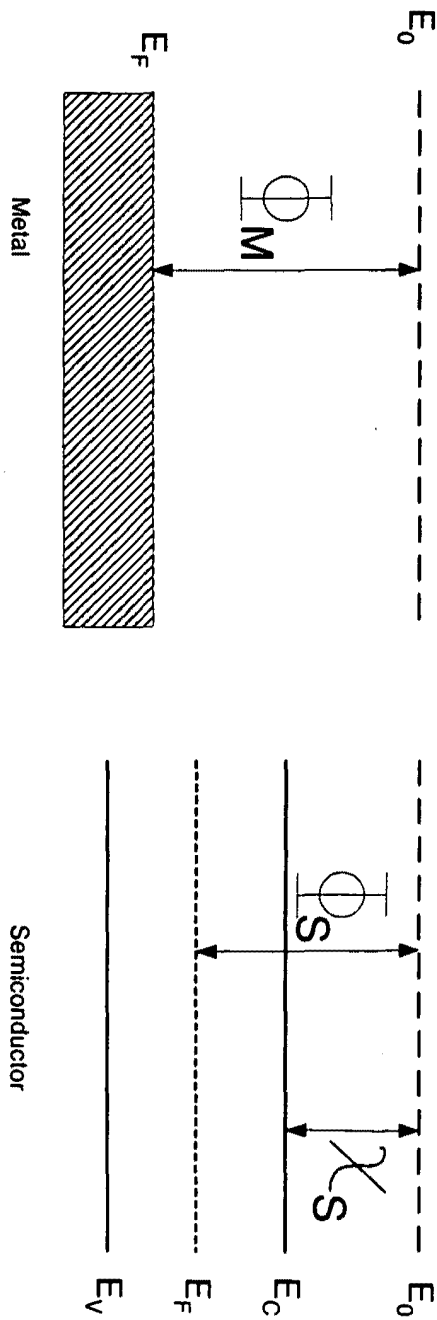


Fig. 2

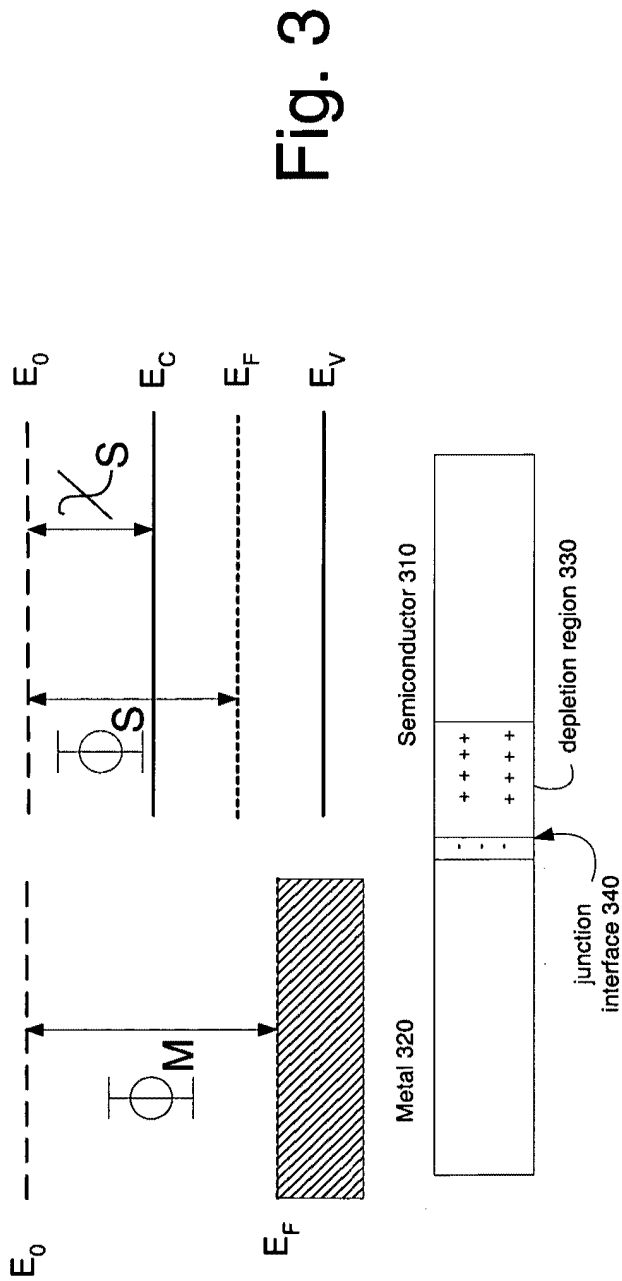


Fig. 3

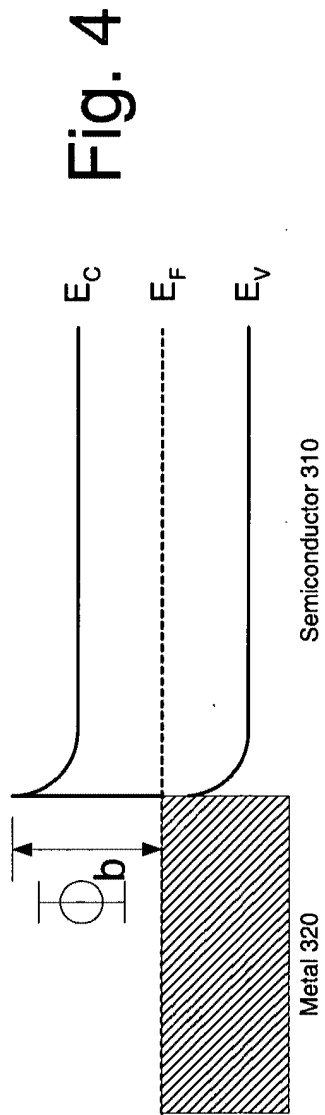


Fig. 4

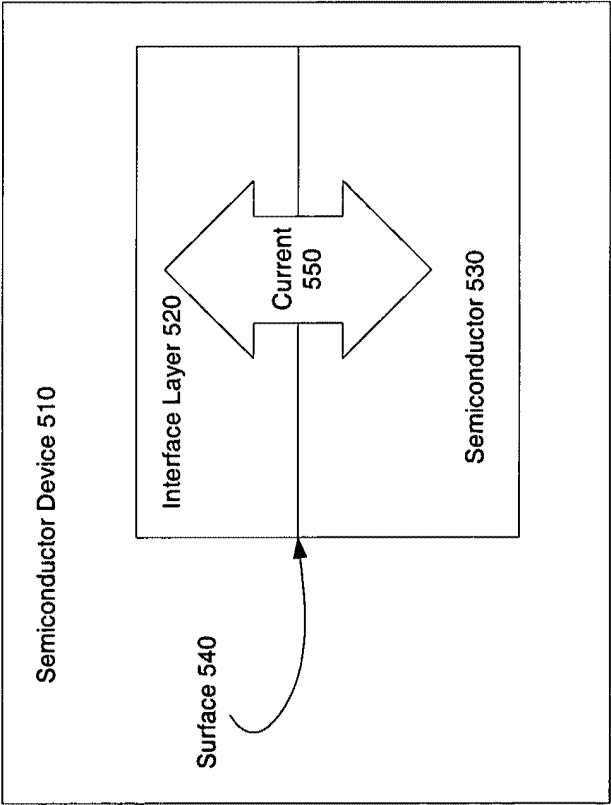


Fig. 5

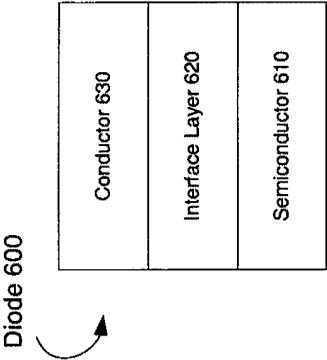
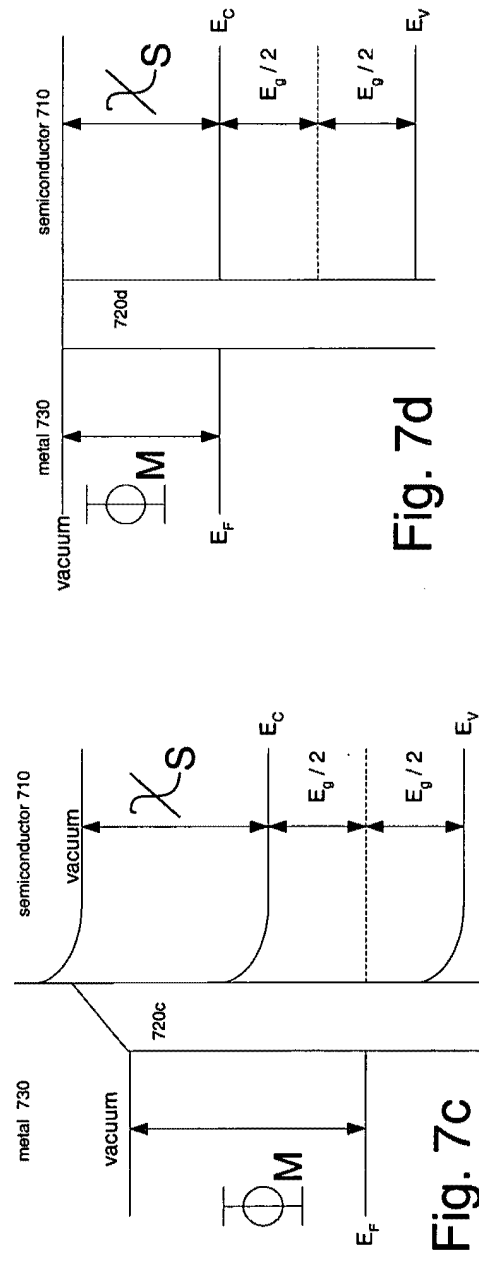
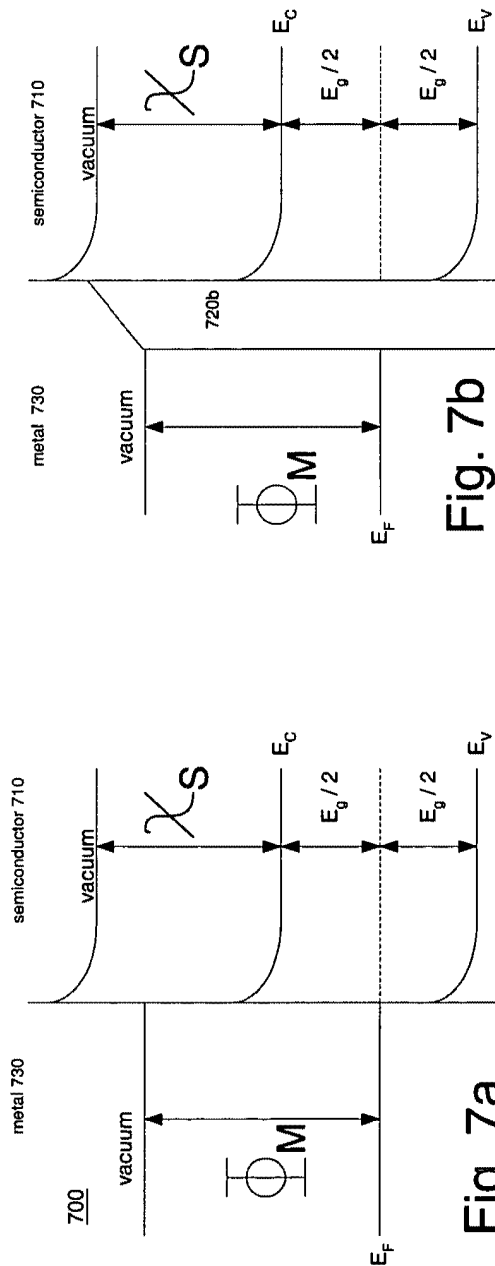


Fig. 6



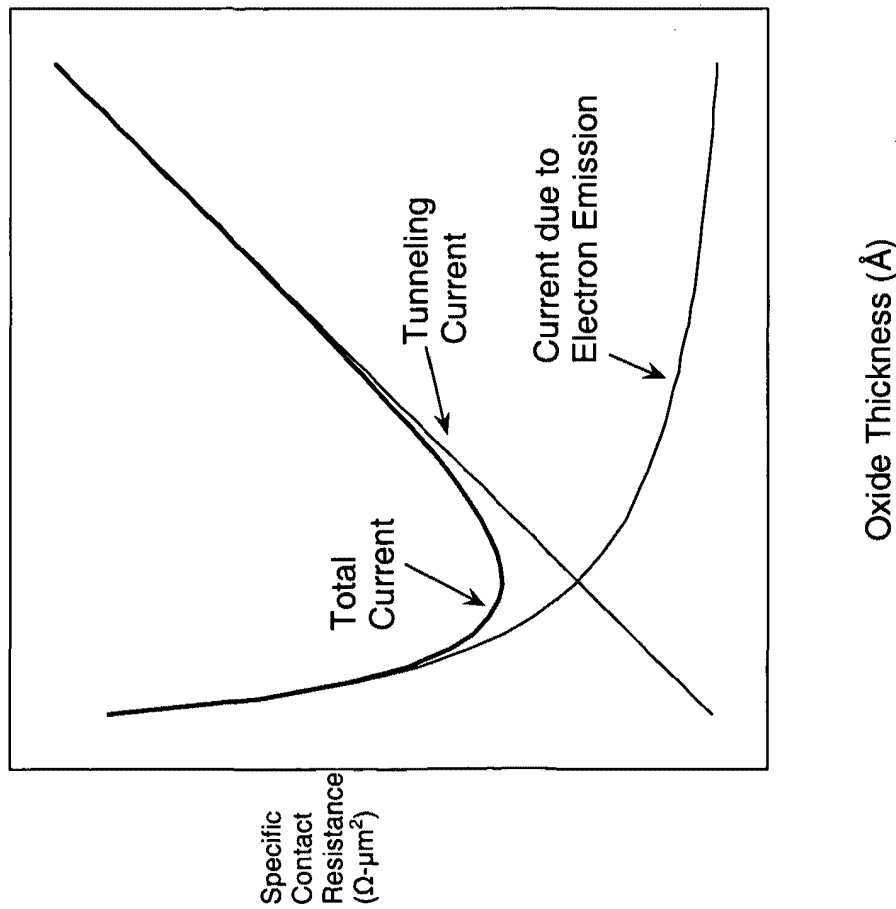


Fig. 8

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

the specification of which

 X is attached hereto.

_____ was filed on (MM/DD/YYYY) _____

_____ as

United States Application Number _____

or PCT International Application Number _____

and was amended on (MM/DD/YYYY) _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application. I do not know and do not believe that the claimed invention was in public use or on sale in the United States of America more than one year prior to this application, nor do I know or believe that the invention has been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

BEST AVAILABLE COPY

Prior Foreign Application(s)

Priority
Claimed

(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

(Application Number) (Filing Date – MM/DD/YYYY)

(Application Number) (Filing Date – MM/DD/YYYY)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number) (Filing Date – MM/DD/YYYY) (Status -- patented,
pending, abandoned)

(Application Number) (Filing Date – MM/DD/YYYY) (Status -- patented,
pending, abandoned)

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence Tarek N. Fahmi, Reg. No. 41,402, BLAKELY,
SOKOLOFF, TAYLOR &

(Name of Attorney or Agent)

ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California
90025 and direct telephone calls to Tarek N. Fahmi, (408) 720-
8300.

(Name of Attorney or Agent)

BEST AVAILABLE COPY

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor DANIEL E. GRUPP

Inventor's Signature DEG - TG Date 8/7/02

Residence PALO ALTO, CA Citizenship USA
(City, State) (Country)

Post Office Address 334 LELAND AVE.
94306-1127

Full Name of Second/Joint Inventor DANIEL J. CONNELLY

Inventor's Signature Daniel Connelly Date 8 Aug 2002

Residence REDWOOD CITY CA Citizenship USA
(City, State) (Country)

Post Office Address 525 RUTHERFORD AVE
94061-4215

BEST AVAILABLE COPY

APPENDIX A

Ramin Aghevli, Reg. No. 43,462; William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. 42,261; W. Thomas Babbitt, Reg. No. 39,591; Jordan M. Becker, Reg. No. 39,602; Michael A. Bernadidou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; R. Alan Burnett, Reg. No. 46,149; Daniel J. Burns, Reg. No. 50,222; Gregory D. Caldwell, Reg. No. 39,926; Thomas M. Coester, Reg. No. 39,637; Robert P. Cogan, Reg. No. 25,049; Donna Jo Coningsby, Reg. No. 41,684; Florin A. Corie, Reg. No. 46,244; Mimi D. Dao, Reg. No. 45,628; Stephen M. De Klerk, Reg. No. 46,503; Daniel M. De Vos, Reg. No. 37,813; Justin M. Dillon, Reg. No. 42,486; Sanjeet Dutta, Reg. No. 46,145; Tarek N. Fahmi, Reg. No. 41,402; Mark C. Farrell, Reg. No. 45,988; Thomas S. Ferrill, Reg. No. 42,532; Kyle H. Flindt, Reg. No. 42,539; George L. Fountain, Reg. No. 37,374; Andre M. Gibbs, Reg. No. 47,593; James Y. Go, Reg. No. 40,621; Mark A. Goldstein, Reg. No. 50,759; Alan E. Heimlich, Reg. No. 48,808; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. 41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W. Hoover II, Reg. No. 32,992; Libby H. Hope, Reg. No. 46,774; Eric S. Hyman, Reg. No. 30,139; William W. Kidd, Reg. No. 31,772; Walter T. Kim, Reg. No. 42,731; Eric T. King, Reg. No. 44,188; Steve Laut, Reg. No. 47,736; Suk S. Lee, Reg. No. 47,745; Gordon R. Lindeen III, Reg. No. 33,192; Jan C. Little, Reg. No. 41,181; Julio Loza, Reg. No. 47,758; Joseph Lutz, Reg. No. 43,765; Lawrence Lycke, Reg. No. 38,540; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, Reg. No. 48,095; Raul D. Martinez, Reg. No. 46,904; Paul A. Mendonsa, Reg. No. 42,879; Clive D. Menezes, Reg. No. 45,493; Jonathan S. Miller, Reg. No. 48,534; Richard A. Nakashima, Reg. No. 42,023; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Robert B. O'Rourke, Reg. No. 46,972; Daniel E. Ovanezian, Reg. No. 41,236; Gregg A. Peacock, Reg. No. 45,001; Marina Portnova, Reg. No. 45,750; Michael A. Proksch, Reg. No. 43,021; William F. Ryann, Reg. No. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey S. Schubert, Reg. No. 43,098; Saina S. Shamilov, Reg. No. 48,266; Kevin G. Shao, Reg. No. 45,095; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Ronald S. Tamura, Reg. No. 43,179; Edwin H. Taylor, Reg. No. 25,129; Lance A. Termes, Reg. No. 43,184; John F. Travis, Reg. No. 43,203; Thomas J. Treutler, Reg. No. 51,126; Kerry D. Tweet, Reg. No. 45,959; Mark C. Van Ness, Reg. No. 39,865; Thomas A. Van Zandt, Reg. No. 43,219; Lester J. Vincent, Reg. No. 31,460; Archana B. Vittal, Reg. No. 45,182; Glenn E. Von Tersch, Reg. No. 41,364; John P. Ward, Reg. No. 40,216; Mark L. Watson, Reg. No. 46,322; Thomas C. Webster, Reg. No. 46,154; Linda S. Zachariah, Reg. No. 48,057; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and William E. Hickman, Reg. No. 46,771, Brent E. Vecchia, Reg. No. 48,011, and Lehua Wang, Reg. No. 48,023; my patent agents, of BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and James R. Thein, Reg. No. 31,710, my patent attorney with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

BEST AVAILABLE COPY

APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56 Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

(e) In any continuation-in-part application, the duty under this section includes the duty to disclose to the Office all information known to the person to be material to patentability, as defined in paragraph (b) of this section, which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

BEST AVAILABLE COPY

GF Exhibit 1006 - 47/161

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875 Effective December 8, 2004

Application or Docket Number

11181217

APPLICATION AS FILED - PART I

(Column 1)

(Column 2)

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1 16(a), (b), or (c))	N/A	N/A
SEARCH FEE (37 CFR 1 16(k), (l), or (m))	N/A	N/A
EXAMINATION FEE (37 CFR 1 16(o), (p), or (q))	N/A	N/A
TOTAL CLAIMS (37 CFR 1 16(j))	1 minus 20 =	• —
INDEPENDENT CLAIMS (37 CFR 1 16(h))	1 minus 3 =	• —
APPLICATION SIZE FEE (37 CFR 1 16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))		

RATE (\$)	FEE (\$)
N/A	150.00
N/A	\$250
N/A	\$100
X\$ 25 =	
X100 =	
+180=	
TOTAL	500

OR

RATE (\$)	FEE (\$)
N/A	300.00
N/A	\$500
N/A	\$200
X\$50 =	
X200 =	
+360=	
TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

(Column 1)

(Column 2)

(Column 3)

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(j))	•	Minus **	=
Independent (37 CFR 1.16(h))	•	Minus ***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25 =	
X100 =	
+180=	
TOTAL ADD'L FEE	

OR

OR

OR

OR

OR

RATE (\$)	ADDITIONAL FEE (\$)
X\$50 =	
X200 =	
+360=	
TOTAL ADD'L FEE	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(j))	•	Minus **	=
Independent (37 CFR 1.16(h))	•	Minus ***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

RATE (\$)	ADDITIONAL FEE (\$)
X\$ 25 =	
X100 =	
+180=	
TOTAL ADD'L FEE	

OR

OR

OR

OR

OR

RATE (\$)	ADDITIONAL FEE (\$)
X\$50 =	
X200 =	
+360=	
TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

07/18/2005 CNGUYEN2 00000001 11181217

01 FC:2011	150.00 OP
02 FC:2111	250.00 OP
03 FC:2311	100.00 OP

PTO-1556

(5/87)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

DANIEL E. GRUPP, ET AL.

Application No.: Unknown

Filed: July 13, 2005

For: **Method For Depinning The Fermi Level Of
A Semiconductor At An Electrical Junction
And Devices Incorporating Such Junctions**

Art Group: Unknown

Examiner: Unknown

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In accordance with the duty of disclosure, enclosed is a copy of IDS Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted concurrently with the Continuation Application. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s). Some or all of the references listed on the enclosed PTO/SB/08 were previously identified in the parent application (Application No. 10/217,758, filed August 12, 2002) and copies of the references were furnished at that time. Accordingly, per 37 CFR §1.98(d)(1) additional copies of those references are not submitted herewith.

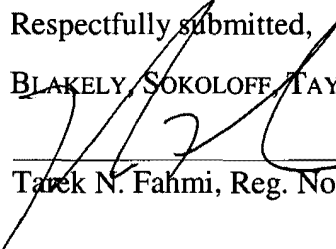
The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

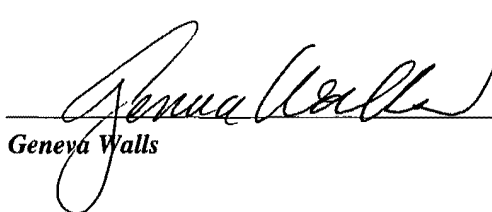
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: July 13, 2005


Tarek N. Fahmi, Reg. No. 41,402

12400 Wilshire Boulevard, 7th Floor
Los Angeles, CA 90025
Telephone: (408) 947-8200

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.


Geneva Walls

Date

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 1 of 1

Attorney Docket No: 3771P003C

US PATENT DOCUMENTS

Examiner Initial *	Cite No. *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-0,789,388	08/13/1997	Hara, Shiro, et al.	
		US-3,590,471	07/06/1971	Lepselter, et al.	
		US-3,708,360	01/02/1973	Wakefield, Jr., et al.	
		US-3,983,264	09/28/1976	Schroen, Walter H., et al.	
		US-4,056,642	11/01/1977	Saxena, Arjun N., et al.	
		US-4,300,152	11/10/1981	Lepselter,	
		US-4,485,550	12/04/1984	Koeneke, et al.	
		US-5,021,365	06/04/1991	Kirchner, et al.	
		US-5,399,206	03/21/1995	de Lyon,	
		US-5,578,848	11/26/1996	Kwong, et al.	
		US-5,596,218	01/21/1997	Soleimani, et al.	
		US-5,612,567	03/18/1997	Baliga,	
		US-5,663,584	09/02/1997	Welch,	
		US-5,801,398	09/01/1998	Hebiguchi,	
		US-5,888,891	03/30/1999	Gould,	
		US-5,939,763	08/17/1999	Hao, et al.	
		US-6,037,605	03/14/2000	Yoshimura,	
		US-6,096,590	08/01/2000	Chan, et al.	
		US-6,150,286	11/21/2000	Sun, et al.	
		US-6,198,113	03/06/2001	Grupp, Daniel E.	
		US-6,207,976	03/27/2001	Takshashi, et al.	
		US-6,261,932	07/17/2001	Hulfachor,	
		US-6,291,866	09/18/2001	Wallace, et al.	
		US-6,291,867	09/18/2001	Wallace, et al.	
		US-6,303,479	10/16/2001	Snyder,	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. *	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
		Country Code - Number - Kind Code (if known)				
		EP-0295490	12/21/1988	Fowler, Alan B., et al.		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
--------------------	-----------------------	---	----------------

EXAMINER**DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
 STATEMENT BY APPLICANT**
 (Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 2 of 2

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		ABERLE, ARMIN G., et al., "Injection-Level Dependent Surface Recombination Velocities at The Silicon-Plasma Silicon Nitride Interface", <u>Institut fur Solaenergieforschung, ISFH, D-3 1860 Emmerthal, Germany, (3/9/95), pp. 2828-2830</u>	
		B. J. ZHANG, et al., "Schottky Diodes of Ni/Au on n-GaN Grown on Sapphire and SiC Substrates", <u>Applied Physics Letters, Vol. 79, No. 16, (10/15/01), pp. 2567-2569</u>	
		B.R. WEINBERGER, et al., "Surface Chemistry of HF Passivation Silicon: X-Ray Photoelectron And Ion Scattering Spectroscopy Results", <u>J. Appl. Phys. 60(9), (11/186), pp. 3232-3234</u>	
		C.L. CHEN, et al., "High Quality Native-Oxide-Free Ultrathin Oxide Grown by In-Situ HF-Vapor Treatment", <u>Electronic Letters, Vol. 36, No. 11, (5/25/00), pp. 981-983</u>	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number

Unknown

Filing Date

July 13, 2005

First Named Inventor

Daniel E. Grupp

Group Art Unit

Unknown

Examiner Name

Unknown

Sheet 3 of 3

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		CHUNG-KUANG, HUANG, et al., "Two-Dimensional Numerical Simulation of Schottky Barrier MOSFET with Channel Length to 10 nm", <u>IEEE</u> , pp. 842-848	
		D. J. CHADI, et al., "Fermi-Level-Pinning Defects in Highly n-Doped Silicon", <u>Physical Review Letters</u> , Vol. 79, No. 24, NEC Research Institute, Princeton New Jersey 08540-6634, (12/97), pp. 4834-4837	
		E. YABLONOVITCH, et al., "Unusually Low Surface-Recombination Velocity on Silicon and Germanium Surfaces", <u>Physical Review Letters</u> , Vol. 57, No. 2, (7/14/86), pp. 249-252	
		F. A. PADOVANI, "Forward Voltage-Current Characteristics of Metal-Silicon Schottky Barriers", <u>Texas Instruments, Inc., Dallas Texas</u> , (9/15/66), pp. 892-892	

EXAMINER**DATE CONSIDERED**

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
 STATEMENT BY APPLICANT**
 (Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 4 of 4

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		G.B. AKERS, et al., "Effects of Thermal Stability and Roughness on Electrical Properties of Tantalus Oxide Gates", <u>Mat. Res., Soc. Symp. Proc., Vol. 567, Materials Research Society, (1999),pp. 391-395</u>	
		HASEGAWA, HIDEKI , et al., "Upinning of Fermi Level in Nanometer-Sized Schottky Contacts on GaAs and InP", <u>Research Center For Interface Quantum Electronics And Graduate School of Electronics And Info. Eng, Hokkaido Univ, Japan, (2000),pp. 92-96</u>	
		HEINE, VOKKER , "Theory of Surface States", <u>Physical Review Letters, Vol. 138, No. 6A, Tell Telephone Lab., Murphy Jill, New Jersey, (6/4/65),</u>	
		HUANG, FENG-JUNG , "Metal-Oxide Semiconductor Field-Effect Transistors Using Schottky Barrier Drains", <u>Electronics Letters, Vol. 33, No. 15, (7/17/97),pp. 1341-1342</u>	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Complete if Known	
	Application Number	Unknown
	Filing Date	July 13, 2005
	First Named Inventor	Daniel E. Grupp
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 5 of 5	Attorney Docket No: 3771P003C	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		I. SHALISH, et al., "Yellow Luminescence And Fermi Level Pinning in GaN Layers", <u>American Institute of Physics, Vol. 77, No. 7, (8/14/00), pp. 987-989</u>	
		INTERNET, <u>http://www.rciqu.hokudai.ac.jp/RCIQEold/ReseacjAcjoeve.emts/jt</u> , <u>downloaded on, (4/12/02),</u>	
		IZUMI, HIROT, et al., "43 Hydrogen Termination: The Ideally Finished Silicon Surface", <u>Ultraclean Surface Processing of Silicon Wafers: Secrets of Vlsi Manufacturing http://halloftechnology.com/electrical_optical/986.shtml</u> , (11/98),	
		J. HILSENBECK, et al., "Aging Behavior of Algan HFETs With Advanced Ohmic And Schottky Contacts", <u>Electronic letters, Vol. 36, No. 11, (5/25/00), pp. 980-981</u>	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number Unknown**Filing Date** July 13, 2005**First Named Inventor** Daniel E. Grupp**Group Art Unit** Unknown**Examiner Name** Unknown

Sheet 6 of 6

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		J. TERSOFF, "Schottky Barrier Heights and The Continuum of Gap States", <u>Physical Review Letters</u> , Vol. 52, No. 6, AT&T Bell Lab., Murphy Jill, New Jersey 07974, (2/6/84),	
		J.R. PATEL, et al., "Arsenic Atom Location on Passive Silicon (111) Surfaces", <u>Physical Review B</u> , Vol. 36, No. 14, (11/15/87), pp. 7715-7717	
		K. NAUKA, et al., "Surface Photovoltage Measurement of Hydrogen-Treated Si Surfaces", <u>Journal of Electrochemical Society</u> 146(1), (1999), pp. 292-295	
		KAMIYAMA, SATOSHI, et al., "Ultrathin Tantalum Oxide Capacitor DIELECTRIC Layers Fabricated Using Rapid Thermal Nitridation Prior to Low Pressure Chemical Vapor Deposition", <u>J. Electrochem Soc.</u> , Vol. 140, No. 6, The Electrochemical Society, Inc., (6/6/93), pp. 1617	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Complete if Known	
	Application Number	Unknown
	Filing Date	July 13, 2005
	First Named Inventor	Daniel E. Grupp
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 7 of 7	Attorney Docket No: 3771P003C	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		KINURA, MITSUTERU , et al., "A New Type of Schottky Tunnel Transistor", <u>IEEE Electron Device Letters</u> , Vol. 15, No. 10, (10/94),pp. 412-414	
		L. CAI, et al., "Investigation of The Properties of Plasma-Enhanced Chemical Vapor Deposition Silicon Nitride And its Effect on Silicon Surface Passivation", <u>Journal of Applied Physics</u> , Vol. 83, No. 11, (6/1/98),pp. 5885-5889	
		LEE, TAKHEE , et al., "Electronic Property of Metallic Nanoclusters on Semiconductor Surfaces: Implications For Nanoelectronic Device Applications", <u>Journal of Nanoparticle Research</u> 2, (2000),pp. 345-362	
		LOUIE, STEVEN G., et al., "Ionicity And The Theory of Schottky Barriers", <u>Physical Review Letters</u> , Vol. 15, No. 4, Dept. of Phys. Univ. of California, and Materials and Molecular Research Div., Lawrence Berkeley Lab., Berkley, CA 94720,	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Complete if Known <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Application Number</td> <td style="width: 50%;">Unknown</td> </tr> <tr> <td>Filing Date</td> <td>July 13, 2005</td> </tr> <tr> <td>First Named Inventor</td> <td>Daniel E. Grupp</td> </tr> <tr> <td>Group Art Unit</td> <td>Unknown</td> </tr> <tr> <td>Examiner Name</td> <td>Unknown</td> </tr> </table>		Application Number	Unknown	Filing Date	July 13, 2005	First Named Inventor	Daniel E. Grupp	Group Art Unit	Unknown	Examiner Name	Unknown
Application Number	Unknown											
Filing Date	July 13, 2005											
First Named Inventor	Daniel E. Grupp											
Group Art Unit	Unknown											
Examiner Name	Unknown											
Sheet 8 of 8	Attorney Docket No: 3771P003C											

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		M. A. SOBOLEWSKI, et al., "Properties of Ultrathin Thermal Nitrides in Silicon Schottky Barrier Structures", <u>Applied Physics Letters</u> , American Institute of Physics, Vol 54, No. 7, (2/13/89), pp. 638-640	
		M. MIYAWAK, et al., "Improvement of Aluminum-Si Contact Performance in Native-Oxide-Free Processing", <u>IEEE Electron Device Letters</u> , Vol. 11, No. 10, (10/90), pp. 448-450	
		M.C. GILMER, et al., "Process and Manufacturing Challenges For High-K Gate Stack Systems", <u>Mat. Res. Soc. Symp. Proc. Vol. 567</u> , (1999), pp. 323-341	
		MANDELIS, ANDREAS, et al., "Evidence of a Surface Acceptor State in Undoped Semi-Insulating GaAs by Photothermal Radiometric Deep Level Transient Spectroscopy", <u>Sociedad Mexicana de Ciencias de Superficies y de Vacio</u> , (1999), pp. 13-17	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Complete if Known	
	Application Number	Unknown
	Filing Date	July 13, 2005
	First Named Inventor	Daniel E. Grupp
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 9 of 9		Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		NOSHIOKA, YASUSHIRO , et al., "Dielectric Characteristics of Forinated Ultradry SiO ₂ ", <u>Appl. Phy. Letters</u> 54(12), (3/20/89),pp. 1127-1129	
		OKAMOTO, NAOYA , et al., "Near-Ohmic Contact of n-GaAs with Ga/Ga/GaAs Quasi-Metal-Insulator-Semiconductor Structure", <u>Jpn. J. Appl. Phys.</u> , Vol. 37, (1998),pp. 32483251	
		P. BAUERNSCHMITT, et al., "Yb-SiO ₂ -Si Tunneling Junctions", <u>Elsevier Publishers B.V.</u> , (1993),pp. 105-108	
		PORTER, LISA M., et al., "A Critical Review of Ohmic and Rectifying Contacts For Silicon Carbide", <u>Material Science and Engineering</u> , Vol. 34, No. 2, (11/1/95),pp. 83-105	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 608. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Complete if Known	
	Application Number	Unknown
	Filing Date	July 13, 2005
	First Named Inventor	Daniel E. Grupp
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 10 of 10	Attorney Docket No: 3771P003C	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		R.A. MCKEE, et al., "Physical Structure And Inversion Chargeat a Semiconductor Interface With a Crystalline Oxide", <u>www.sciencemag.org</u> , Vol. 293, (7/20/01),pp. 468-469	
		R.D. BRINGANSS, "Arsenic Passivation of Si and Ge Surfaces", <u>Critical Reviews in Solid State and Materials Sciences</u> , 17(4): 353-395, (1992),pp. 353-395	
		R.M.C. DE ALMEIDA, et al., "Reaction-Diffusion Model For Thermal Growth of Silicon Nitrite Films on Si", <u>Physical Review B</u> , Vol. 62, No. 24, (12/1500),pp. R16 255-R16 258	
		R.T. TUNG, "Electron Transport of Inhomogeneous Schottky Barriers", <u>AT&T Bell Lab., Murray Hill, New Jersey 07974</u> , (3/21/91),pp. 3832-3834	

EXAMINER

DATE CONSIDERED

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Complete if Known <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; border: 1px solid black;">Application Number</td> <td style="width: 50%; border: 1px solid black;">Unknown</td> </tr> <tr> <td style="border: 1px solid black;">Filing Date</td> <td style="border: 1px solid black;">July 13, 2005</td> </tr> <tr> <td style="border: 1px solid black;">First Named Inventor</td> <td style="border: 1px solid black;">Daniel E. Grupp</td> </tr> <tr> <td style="border: 1px solid black;">Group Art Unit</td> <td style="border: 1px solid black;">Unknown</td> </tr> <tr> <td style="border: 1px solid black;">Examiner Name</td> <td style="border: 1px solid black;">Unknown</td> </tr> </table>		Application Number	Unknown	Filing Date	July 13, 2005	First Named Inventor	Daniel E. Grupp	Group Art Unit	Unknown	Examiner Name	Unknown
Application Number	Unknown											
Filing Date	July 13, 2005											
First Named Inventor	Daniel E. Grupp											
Group Art Unit	Unknown											
Examiner Name	Unknown											
Sheet 11 of 11	Attorney Docket No: 3771P003C											

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		S. HARA, et al., "Control of Schoffky And Ohmic Interfaces by Unpinning Fermi Level", <u>Elsevier Science B.V.</u> , pp. 394-399	
		S. HARA, et al., "Pinning-Controlled Metal/Semiconductor Interfaces", <u>Electrotechnical Laboratory</u> , pp. 802-807	
		S. HARA, et al., "Pinning-Controlled Ohmic Contacts: Application to SiC(0001)", <u>Elsevier Science B.V.</u> , pp. 218-221	
		S. VERHACEBEKE, et al., "Surface Characterization of Si After HF Treatments and its Influence in the Dielectric Breakdown of Thermal Oxides", <u>Research Aspirant of the Belgium National Fund for Scientific Research; Mat. Res. Soc. Symp. Proc., Vol. 259, Material Research Society</u> , (1992),pp. 391-399	

EXAMINER

DATE CONSIDERED

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Complete if Known <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; border: 1px solid black;">Application Number</td> <td style="width: 50%; border: 1px solid black;">Unknown</td> </tr> <tr> <td style="border: 1px solid black;">Filing Date</td> <td style="border: 1px solid black;">July 13, 2005</td> </tr> <tr> <td style="border: 1px solid black;">First Named Inventor</td> <td style="border: 1px solid black;">Daniel E. Grupp</td> </tr> <tr> <td style="border: 1px solid black;">Group Art Unit</td> <td style="border: 1px solid black;">Unknown</td> </tr> <tr> <td style="border: 1px solid black;">Examiner Name</td> <td style="border: 1px solid black;">Unknown</td> </tr> </table>		Application Number	Unknown	Filing Date	July 13, 2005	First Named Inventor	Daniel E. Grupp	Group Art Unit	Unknown	Examiner Name	Unknown
Application Number	Unknown											
Filing Date	July 13, 2005											
First Named Inventor	Daniel E. Grupp											
Group Art Unit	Unknown											
Examiner Name	Unknown											
Sheet 12 of 12	Attorney Docket No: 3771P003C											

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		S.A. WOLF, et al., "Spintronics: A Spin-Based Vision For The Future", <u>www.sciencemag.or</u> , Vol.294, (11/6/01),pp. 1488	
		S.M. SZE, "Metal-Semiconductor Contacts", <u>Physics of Semiconductor Devices</u> , John Wiley & Sons, (1981),	
		SCHMIDT, JAN , et al., "Carrier Recombination at Silicon-Silicon Nitride Interfaces Fabricated by Plasma-Enhanced Chemical Vapor Deposition", <u>Journal of Applied Physics</u> , Vol. 85, No. 7, (4/1/99),pp. 3626-3633	
		SEARCH REPORT, "International Searching Authority", <u>PCT/US03/25054</u> , (12/3/03),pp. 8	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Complete if Known	
	Application Number	Unknown
	Filing Date	July 13, 2005
	First Named Inventor	Daniel E. Grupp
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 13 of 13	Attorney Docket No: 3771P003C	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		SHAIK, LAHIR , et al., "Experimental Identification of Nitrogen-Vacancy Complexes in Nitrogen Implanted Silicon", <u>Applied Physics Letters</u> , Vol. 79, No. 5, (7/30/01),pp. 623-625	
		SNYDER, JOHN P., et al., "Experimental Investigation of a PtSi Source And Drain Field Emission Transister", <u>American Institute of Physics</u> , pp. 1-3	
		T.I. KAMINS, et al., "Effect of Hydrogen on p-Type Epitaxial Silicon Sheet-Resistance Measurements", <u>Electrochemical and Solid-State Letters</u> 1(2), (1998),pp. 100-101	
		TERAJI, TOKUYUKI , et al., "Ohmic Contacts To n-Type 6H-SiC Without Post-Annealing", <u>Material Research Society Symposium Proceeding</u> , (4/8/96),pp. 149-154	

EXAMINER

DATE CONSIDERED

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	<i>Complete if Known</i>	
	Application Number	Unknown
	Filing Date	July 13, 2005
	First Named Inventor	Daniel E. Grupp
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 14 of 14	Attorney Docket No: 3771P003C	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		U.J.R. BAUMVOL, "Atomic Transport During Growth of Ultrathin Dielectrics on Silicon", <u>Surface Science Reports</u> 36 , (1999),pp. 1-166	
		W.E. SPICER, et al., "Unified Mechanism For Schottky-Barrier Formation And III-V Oxide Interface States", <u>Physical Review Letters</u> , Vol. 44, No. 6, <u>Stanford Electronics Lab., Stanford Univ., Stanford, CA 94305</u> , (2/11/80),pp. 420-423	
		WANG, LIE , et al., "High Barrier GaN Schottky Diodes: Pt/GaN and Pd/GaN", <u>Dept. of Electrical Eng., Univ. of Minnesota, Minneapolis, Minnesota 55455; Appl. Phys. Letters</u> , Vol. 68(9) , (2/26/96),pp. 1267-1270	
		WIDJAJA, YUNIARTO , et al., "Ab Initio Study and Decomposition of NH3 on Si(100)-(2x1)", <u>J. Phy. Chem B</u> , (2000),pp. 2527-2533	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Complete if Known <table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; border: 1px solid black; padding: 2px;">Application Number</td> <td style="width: 50%; border: 1px solid black; padding: 2px;">Unknown</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">Filing Date</td> <td style="border: 1px solid black; padding: 2px;">July 13, 2005</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">First Named Inventor</td> <td style="border: 1px solid black; padding: 2px;">Daniel E. Grupp</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">Group Art Unit</td> <td style="border: 1px solid black; padding: 2px;">Unknown</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">Examiner Name</td> <td style="border: 1px solid black; padding: 2px;">Unknown</td> </tr> </table>	Application Number	Unknown	Filing Date	July 13, 2005	First Named Inventor	Daniel E. Grupp	Group Art Unit	Unknown	Examiner Name	Unknown
Application Number	Unknown										
Filing Date	July 13, 2005										
First Named Inventor	Daniel E. Grupp										
Group Art Unit	Unknown										
Examiner Name	Unknown										
Sheet 15 of 15	Attorney Docket No: 3771P003C										

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		WRIGHT, PETER J., et al., "Hot-Electron Immunity of SiO ₂ Dielectrics with Fluorine Incorporation", <u>IEEE Electron Device Letters</u> , Vol. 10, No. 8, (8/8/89),pp. 347-348	
		Y. HAYAFUJI, et al., "Nitridation of Silicon and Oxidized-Silicon", <u>Sony Corp. Research Center, 174 Fujitsuka-Cho, Hodogaya-Ku, Yokohama, 240 Japan; J. Electrochem. Soc.: Solid State Science and Technology</u> , (9/82),	
		Y. K. KIM, et al., "Metal-Dependent Fermi-Level Movement in The Metal/Sulfur-Passivated InGaP Contact", <u>J. Vac Sci. Technology A</u> 15(3), (1997),pp. 1124-1128	
		YANG, HANYANG , et al., "The Effects of Interfacial Sub-Oxide Transition Regions and Monolayer Level Nitridation on Tunneling Currents in Silicon Devices", <u>IEEE Electron Device Letters</u> , Vol. 21, No. 2, (2/2/00),pp. 76-78	

EXAMINER

DATE CONSIDERED

Effective 12/03/2004 Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818) FEE TRANSMITTAL for FY 2005		Complete if Known	
☒ Applicant claims small entity status. See 37 CFR 1.27.		Application Number	Unknown
		Filing Date	July 13, 2005
		First Named Inventor	Daniel E. Grupp
		Examiner Name	Unknown
		Art Unit	Unknown
TOTAL AMOUNT OF PAYMENT (\$) 500.00		Attorney Docket No.	3771P003C

METHOD OF PAYMENT (check all that apply)

☒ Check
 ☐ Credit card
 ☐ Money Order
 ☐ None
 ☐ Other (please identify): _____

☒ Deposit Account
 Deposit Account Number: 02-2666
 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below
 ☐ Charge fee(s) indicated below, except for the filing fee
☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.
 ☒ Credit any overpayments

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fee(s) Paid (\$)
	Small Entity	Small Entity	Small Entity	Small Entity	Small Entity	Small Entity	
	Fee (\$)	Fee (\$)	Fee (\$)	Fee (\$)	Fee (\$)	Fee (\$)	
Utility	300	150	500	250	200	100	500.00
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description
 Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent
 Each independent claim over 3 or, Reissues, each independent claim more than in the original patent
 Multiple independent claims

Total Claims	Extra Claims	Fee (\$)	Fee Paid	Multiple Dependent Claims	Fee (\$)	Fee Paid
1 - 20 or HP = 0	X	25.00	\$0.00			
HP = highest number of total claims paid for, if greater than 20						
Indep. Claims	Extra Claims	Fee (\$)	Fee Paid			
1 - 3 or HP = 0	X	100.00	\$0.00			
HP = highest number of independent claims paid for, if greater than 3						

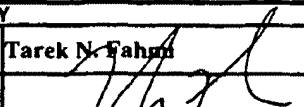
3. APPLICATION SIZE FEE
 If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets of sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
40	100 = -60	/ 50 = (round up to a whole number) X		

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)
 Other: _____
 Recording of a patent assignment _____

5. TOTAL AMOUNT OF PAYMENT (\$) **500.00**

SUBMITTED BY		Complete (if applicable)	
Name (Print/Type)	Tarek N. Fahmy	Registration No. (Attorney/Agent)	41,402
Signature		Telephone	(408) 947-8200
		Date	07/13/05

Based on PTO/SB/17 (10-03) as modified by Blakely, Sokoloff, Taylor & Zafman (wtr) 02/10/2004.
 SEND TO: Mail Stop Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450



IFW

TRANSMITTAL FORM (to be used for all correspondence after initial filing)		Application No.	11/181,217
		Filing Date	July 13, 2005
		First Named Inventor	Daniel E. Grupp
		Art Unit	2811
		Examiner Name	Unknown
Total Number of Pages in This Submission	7	Attorney Docket Number	3771P003C

ENCLOSURES (check all that apply)		
☒ Fee Transmittal Form ☐ Fee Attached ☐ Amendment / Response ☐ After Final ☐ Affidavits/declaration(s) ☐ Extension of Time Request ☐ Express Abandonment Request ☒ Information Disclosure Statement ☒ PTO/SB/08 ☐ Certified Copy of Priority Document(s) ☐ Response to Missing Parts/Incomplete Application ☐ Basic Filing Fee ☐ Declaration/POA ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53	☐ Drawing(s) ☐ Licensing-related Papers ☐ Petition ☐ Petition to Convert a Provisional Application ☐ Power of Attorney, Revocation Change of Correspondence Address ☐ Terminal Disclaimer ☐ Request for Refund ☐ CD, Number of CD(s)	☐ After Allowance Communication to Group ☐ Appeal Communication to Board of Appeals and Interferences ☐ Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) ☐ Proprietary Information ☐ Status Letter ☒ Other Enclosure(s) (please identify below): Eight (8) References Cited; Postcard.
Remarks		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	Tarek N. Fahmi, Reg. No. 41,402 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	August 22, 2005

CERTIFICATE OF MAILING/TRANSMISSION			
I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.			
Typed or printed name	Geneva Walls		
Signature		Date	August 22, 2005

Based on PTO/SB/21 (04-04) as modified by Blakely, Solokoff, Taylor & Zafman (wlr) 06/04/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450



FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

Complete if Known

Application Number	11/181,217
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Examiner Name	Unknown
Art Unit	2811
Attorney Docket No.	3771P003C

☒ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT (\$)

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit card ☐ Money Order ☒ None ☐ Other (please identify):

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below

☐ Charge fee(s) indicated below, except for the filing fee

☒ Charge any additional fee(s) or underpayment of fee(s)

☒ Credit any overpayments

under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.

FEE CALCULATION

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	
Other fee (specify)					
SUBTOTAL (2)				(\$)	

SUBMITTED BY

Name (Print/Type)	Tarek N. Fahmi	Registration No. (Attorney/Agent)	41,402	Telephone	(408) 947-8200
Signature		Date	08/22/05		

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450



UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

DANIEL E. GRUPP, ET AL.

Application No.: 11/181,217

Filed: July 13, 2005

For: **Method For Depinning The Fermi Level Of
A Semiconductor At An Electrical Junction
And Devices Incorporating Such Junctions**

Art Group: 2811

Examiner: Unknown

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In accordance with the duty of disclosure, enclosed is a copy of IDS Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of a first Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s). Some or all of the references listed on the enclosed PTO/SB/08 were previously identified in the parent application (Application No. 10/217,758, filed August 12, 2002) and copies of the references were furnished at that time. Accordingly, per 37 CFR §1.98(d)(1) additional copies of those references are not submitted herewith.

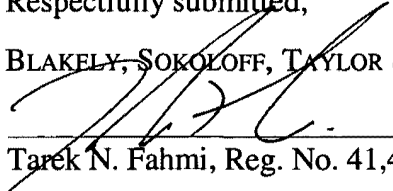
The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 02-2666. A duplicate copy of the Fee Transmittal (PTO/SB/17) is enclosed for this purpose.

Respectfully submitted,

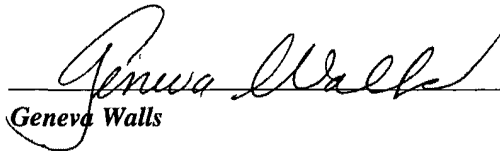
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: August 22, 2005


Tarek N. Fahmi, Reg. No. 41,402

12400 Wilshire Boulevard, 7th Floor
Los Angeles, CA 90025
Telephone: (408) 947-8200

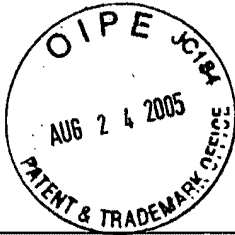
I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.


Geneva Walls

08-22-05

Date

Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Use as many sheets as necessary)



Complete if Known

Application Number	11/181,217
Filing Date	July 13, 2005
First Named Inventor	Grupp, Daniel E.
Group Art Unit	2811
Examiner Name	Unknown

Sheet 1 of 2

Attorney Docket No: 3771P003C

		BLOSSE, A., et al., "A Novel Low Cost 65nm CMOS Process Architecture With Self Aligned Isolation and W Cladded Source/Drain", <u>IEEE, Transactions of 2004 International Electron Device Meeting</u> , pp. 669-672	
		CONNELLY, DANIEL, et al., "Optimizing Schottky S/D Offset for 25-nm Dual-Gate CMOS Performance", <u>IEEE Trans. Electron Devices, Vol. 47 No. 5, (2003)</u> , pp. 1028-1034	
		EDELSTEIN, D., et al., "Full Copper Wiring in a Sub-0.25 mm CMOS ULSI Technology", <u>Proceedings of the IEEE International Electron Device Meeting, (12/1997)</u> , pp. 773-776	
		GOPALAKRISHNAN, KAILASH, et al., "Impact Ionization MOS (I-MOS)-Part I: Device and Circuit Simulations", <u>IEEE Transactions Electron Devices, Vol. 52, No. 1, (2005)</u> , pp. 69-76	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
 STATEMENT BY APPLICANT**
 (Use as many sheets as necessary)



Complete if Known

Application Number	11/181,217
Filing Date	July 13, 2005
First Named Inventor	Grupp, Daniel E.
Group Art Unit	2811
Examiner Name	Unknown

Sheet 2 of 2

Attorney Docket No: 3771P003C

		KEDZIERSKI, JAKUB, et al., "Extension and Source/Drain Design for High-Performance FinFET Devices", <u>IEEE Trans. Electron Devices</u> , Vol. 50, No. 4, (4/2003), pp. 952-958	
		THOMPSON, SCOTT E., et al., "A Logic Nanotechnology Featuring Strained-Silicon", <u>IEEE Electron Device Letters</u> , Vol. 25, No. 4, (2004), pp. 191-193	
		WEI, C.S., et al., "The Use of Selective Electroless Metal Deposition For Micron Size Contact Fill", <u>IEEE TInternational Electron Device Meeting Technical Digest</u> , (1988), pp. 446-449	
		YAGISHITA, ATSUSHI, et al., "High Performance Damascene Metal Gate MOSFET's for 0.1 mm Regime", <u>IEEE Trans. Electron Devices</u> , Vol. 47, No. 5, (2000), pp. 1028-1034	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2	("7084423").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/07/06 21:14
L2	149	depin or de-pin or de adj pin	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/06 22:02

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	11/181217	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/05 22:42
L2	12	10/217758	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/05 22:48
L3	15	(depin near5 fermi adj level) and resistance	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/05 22:54
L4	15	depin near5 fermi adj level	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/05 22:54
L5	15	depin near5 fermi	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/05 22:54
L6	15	depin and fermi	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/05 22:58
L7	88	depin	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/05 22:59
L8	73	l7 not l6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/06 00:14
L9	4085	fermi and interface	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/06 00:14

EAST Search History

L10	66	I9 and de-pin or de adj pin	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/07/06 00:15
-----	----	-----------------------------	---	----	----	------------------



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/181,217	07/13/2005	Daniel E. Grupp	3771P003C	6623

8791 7590 07/13/2007
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER

NGO, NGAN V

ART UNIT	PAPER NUMBER
----------	--------------

2818

MAIL DATE	DELIVERY MODE
-----------	---------------

07/13/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

11/181,217

Applicant(s)

GRUPP ET AL.

Examiner

Ngan Ngo

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 0805 and 0705.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: ____.

Art Unit: 2818

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

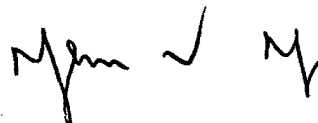
Claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. &,084,423 B2.

Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 in this application inherently has a thickness of less than 1nm in order to depin a Fermi level of the semiconductor and the Fermi level of the metal. It is well known that silicon is used as semiconductor. Therefore, claim 1 in this application is obvious over claim 1 of the U.S. Patent No. &,084,423 B2.

Art Unit: 2818

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Ngan Van Ngo
Primary Examiner

Ngan Ngo

July 6, 2007

Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
 STATEMENT BY APPLICANT**
 (Use as many sheets as necessary)



Complete if Known

Application Number	11/181,217
Filing Date	July 13, 2005
First Named Inventor	Grupp, Daniel E.
Group Art Unit	2811 2818
Examiner Name	Unknown NGAN NGO

Sheet 1 of 2

Attorney Docket No: 3771P003C

/NN/	BLOSSE, A., et al., "A Novel Low Cost 65nm CMOS Process Architecture With Self Aligned Isolation and W Cladded Source/Drain", <u>IEEE, Transactions of 2004 International Electron Device Meeting</u> , pp. 669-672
/NN/	CONNELLY, DANIEL, et al., "Optimizing Schottky S/D Offset for 25-nm Dual-Gate CMOS Performance", <u>IEEE Trans. Electron Devices</u> , Vol. 47 No. 5, (2003), pp. 1028-1034
/NN/	EDELSTEIN, D., et al., "Full Copper Wiring in a Sub-0.25 mm CMOS ULSI Technology", <u>Proceedings of the IEEE International Electron Device Meeting</u> , (12/1997), pp. 773-776
/NN/	GOPALAKRISHNAN, KAILASH, et al., "Impact Ionization MOS (I-MOS)-Part I: Device and Circuit Simulations", <u>IEEE Transactions Electron Devices</u> , Vol. 52, No. 1, (2005), pp. 69-76

EXAMINER

/Ngan Ngo/

DATE CONSIDERED

07/06/2007

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
 STATEMENT BY APPLICANT**

(Use as many sheets as necessary)



Complete if Known

Application Number	11/181,217
Filing Date	July 13, 2005
First Named Inventor	Grupp, Daniel E.
Group Art Unit	2811 2818
Examiner Name	Unknown NGAN NGO

Sheet 2 of 2

Attorney Docket No: 3771P003C

/NN/	KEDZIERSKI, JAKUB, et al., "Extension and Source/Drain Design for High-Performance FinFET Devices", <u>IEEE Trans. Electron Devices</u> , Vol. 50, No. 4, (4/2003), pp. 952-958
/NN/	THOMPSON, SCOTT E., et al., "A Logic Nanotechnology Featuring Strained-Silicon", <u>IEEE Electron Device Letters</u> , Vol. 25, No. 4, (2004), pp. 191-193
/NN/	WEI, C.S., et al., "The Use of Selective Electroless Metal Deposition For Micron Size Contact Fill", <u>IEEE International Electron Device Meeting Technical Digest</u> , (1988), pp. 446-449
/NN/	YAGISHITA, ATSUSHI, et al., "High Performance Damascene Metal Gate MOSFET's for 0.1 mm Regime", <u>IEEE Trans. Electron Devices</u> , Vol. 47, No. 5, (2000), pp. 1028-1034

EXAMINER

/Ngan Ngo/

DATE CONSIDERED

07/06/2007

Substitute Disclosure Statement Form (PTO-1449)

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Use as many sheets as necessary)

Complete if Known

Application Number	Unknown 11/181217
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Group Art Unit	Unknown 2818
Examiner Name	Unknown NGAN NGO

Sheet 1 of 1

Attorney Docket No: 3771P003C

US PATENT DOCUMENTS

Examiner Initial *	Cite No. *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/NN/		US-0,789,388	08/13/1997	Hara, Shiro, et al.	
		US-3,590,471	07/06/1971	Lepseter, , et al.	
		US-3,708,360	01/02/1973	Wakefield, Jr., , et al.	
		US-3,983,264	09/28/1976	Schroen, Walter H., et al.	
		US-4,056,642	11/01/1977	Saxena, Arjun N., et al.	
		US-4,300,152	11/10/1981	Lepseter,	
		US-4,485,550	12/04/1984	Koeneke, , et al.	
		US-5,021,365	06/04/1991	Kirchner, , et al.	
		US-5,399,206	03/21/1995	de Lyon,	
		US-5,578,848	11/26/1996	Kwong, , et al.	
		US-5,596,218	01/21/1997	Soleimani, , et al.	
		US-5,612,567	03/18/1997	Baliga,	
		US-5,663,584	09/02/1997	Welch,	
		US-5,801,398	09/01/1998	Hebiguchi,	
		US-5,888,891	03/30/1999	Gould,	
		US-5,939,763	08/17/1999	Hao, , et al.	
		US-6,037,605	03/14/2000	Yoshimura,	
		US-6,096,590	08/01/2000	Chan, , et al.	
		US-6,150,286	11/21/2000	Sun, , et al.	
		US-6,198,113	03/06/2001	Grupp, Daniel E.	
		US-6,207,976	03/27/2001	Takshashi, , et al.	
		US-6,261,932	07/17/2001	Hulfachor,	
		US-6,291,866	09/18/2001	Wallace, , et al.	
		US-6,291,867	09/18/2001	Wallace, , et al.	
/NN/		US-6,303,479	10/16/2001	Snyder,	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. *	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
/NN/		Country Code - Number - Kind Code (If known) EP-0295490	12/21/1988	Fowler, Alan B., et al.		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No *	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
---------------------	-----------	---	----------------

EXAMINER

/Ngan Ngo/

DATE CONSIDERED

07/06/2007

Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
 STATEMENT BY APPLICANT**
 (Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 2 of 2

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/NN/		ABERLE, ARMIN G., et al., "Injection-Level Dependent Surface Recombination Velocities at The Silicon-Plasma Silicon Nitride Interface", <u>Institut fur Solaenergieforschung, ISFH, D-3 1860 Emmerthal, Germany, (3/9/95), pp. 2828-2830</u>	
/NN/		B. J. ZHANG, et al., "Schottky Diodes of Ni/Au on n-GaN Grown on Sapphire and SiC Substrates", <u>Applied Physics Letters, Vol. 79, No. 16, (10/15/01), pp. 2567-2569</u>	
/NN/		B.R. WEINBERGER, et al., "Surface Chemistry of HF Passivation Silicon: X-Ray Photoelectron And Ion Scattering Spectroscopy Results", <u>J. Appl. Phys. 60(9), (11/186), pp. 3232-3234</u>	
/NN/		C.L. CHEN, et al., "High Quality Native-Oxide-Free Ultrathin Oxide Grown by In-Situ HF-Vapor Treatment", <u>Electronic Letters, Vol. 36, No. 11, (5/25/00), pp. 981-983</u>	

EXAMINER /Ngan Ngo/

DATE CONSIDERED

07/06/2007

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 608. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449/APTO
**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 3 of 3

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/NN/		CHUNG-KUANG, HUANG , et al., "Two-Dimensional Numerical Simulation of Schottky Barrier MOSFET with Channel Length to 10 nm", <u>IEEE</u> , pp. 842-848	
/NN/		D. J. CHADI, et al., "Fermi-Level-Pinning Defects in Highly n-Doped Silicon", <u>Physical Review Letters</u> , Vol. 79, No. 24, NEC Research Institute, Princeton New Jersey 08540-6634, (12/97),pp. 4834-4837	
/NN/		E. YABLONOVITCH, et al., "Unusually Low Surface-Recombination Velocity on Silicon and Germanium Surfaces", <u>Physical Review Letters</u> , Vol. 57, No. 2, (7/14/86),pp. 249-252	
/NN/		F. A. PADOVANI, "Forward Voltage-Current Characteristics of Metal-Silicon Schottky Barriers", <u>Texas Instruments, Inc., Dallas Texas</u> , (9/15/66),pp. 892-892	

EXAMINER

/Ngan Ngo/

DATE CONSIDERED

07/06/2007

Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 4 of 4

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/NN/		G.B. AKERS, et al., "Effects of Thermal Stability and Roughness on Electrical Properties of Tantalus Oxide Gates", <u>Mat. Res., Soc. Symp. Proc., Vol. 567, Materials Research Society, (1999),pp. 391-395</u>	
/NN/		HASEGAWA, HIDEKI , et al., "Upping of Fermi Level in Nanometer-Sized Schottky Contacts on GaAs and InP", <u>Research Center For Interface Quantum Electronics And Graduate School of Electronics And Info. Eng, Hokkaido Univ, Japan, (2000),pp. 92-96</u>	
/NN/		HEINE, VOKKER , "Theory of Surface States", <u>Physical Review Letters, Vol. 138, No. 6A, Tell Telephone Lab., Murphy Jill, New Jersey, (6/4/65),</u>	
/NN/		HUANG, FENG-JUNG , "Metal-Oxide Semiconductor Field-Effect Transistors Using Schottky Barrier Drains", <u>Electronics Letters, Vol. 33, No. 15, (7/17/97),pp. 1341-1342</u>	

EXAMINER /Ngan Ngo/

DATE CONSIDERED 07/06/2007

Substitute Disclosure Statement Form (PTO-1448)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number Unknown

Filing Date July 13, 2005

First Named Inventor Daniel E. Grupp

Group Art Unit Unknown

Examiner Name Unknown

Sheet 5 of 5

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/NN/		I. SHALISH, et al., "Yellow Luminescence And Fermi Level Pinning in GaN Layers", <u>American Institute of Physics, Vol. 77, No. 7, (8/14/00), pp. 987-989</u>	
/NN/		INTERNET, <u>http://www.rciqu.hokudai.ac.jp/RCIQEold/ReseacjAcjoeve.emts/it</u> , <u>downloaded on, (4/12/02),</u>	
/NN/		IZUMI, HIROT, et al., "43 Hydrogen Termination: The Ideally Finished Silicon Surface", <u>Ultraclean Surface Processing of Silicon Wafers: Secrets of Vlsi Manufacturing http://halloftechnology.com/electrical_optical/986.shtml</u> , (11/98),	
/NN/		J. HILSENBECK, et al., "Aging Behavior of Algan HFETs With Advanced Ohmic And Schottky Contacts", <u>Electronic letters, Vol. 36, No. 11, (5/25/00), pp. 980-981</u>	

EXAMINER

/Ngan Ngo/

DATE CONSIDERED

07/06/2007

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Complete if Known	
	Application Number	Unknown
	Filing Date	July 13, 2005
	First Named Inventor	Daniel E. Grupp
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 6 of 6	Attorney Docket No: 3771P003C	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/NN/		J. TERSOFF, "Schottky Barrier Heights and The Continuum of Gap States", <u>Physical Review Letters</u> , Vol. 52, No. 6, AT&T Bell Lab., Murphy Hill, New Jersey 07974, (2/6/84),	
/NN/		J.R. PATEL, et al., "Arsenic Atom Location on Passive Silicon (111) Surfaces", <u>Physical Review B</u> , Vol. 36, No. 14, (11/15/87), pp. 7715-7717	
/NN/		K. NAUKA, et al., "Surface Photovoltage Measurement of Hydrogen-Treated Si Surfaces", <u>Journal of Electrochemical Society</u> 146(1), (1999), pp. 292-295	
/NN/		KAMIYAMA, SATOSHI, et al., "Ultrathin Tantalum Oxide Capacitor DIELECTRIC Layers Fabricated Using Rapid Thermal Nitridation Prior to Low Pressure Chemical Vapor Deposition", <u>J. Electrochem Soc.</u> , Vol. 140, No. 6, The Electrochemical Society, Inc., (6/6/93), pp. 1617	

EXAMINER

/Ngan Ngo/

DATE CONSIDERED

07/06/2007

Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 7 of 7

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/NN/		KINURA, MITSUTERU , et al., "A New Type of Schottky Tunnel Transistor", <u>IEEE Electron Device Letters</u> , Vol. 15, No. 10, (10/94),pp. 412-414	
/NN/		L. CAI, et al., "Investigation of The Properties of Plasma-Enhanced Chemical Vapor Deposition Silicon Nitride And its Effect on Silicon Surface Passivation", <u>Journal of Applied Physics</u> , Vol. 83, No. 11, (6/1/98),pp. 5885-5889	
/NN/		LEE, TAKHEE , et al., "Electronic Property of Metallic Nanoclusters on Semiconductor Surfaces: Implications For Nanoelectronic Device Applications", <u>Journal of Nanoparticle Research 2</u> , (2000),pp. 345-362	
/NN/		LOUIE, STEVEN G., et al., "Ionicity And The Theory of Schottky Barriers", <u>Physical Review Letters</u> , Vol. 15, No. 4, Dept. of Phys. Univ. of California, and Materials and Molecular Research Div., Lawrence Berkeley Lab., Berkley, CA 94720,	

EXAMINER

/Ngan Ngo/

DATE CONSIDERED

07/06/2007

Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 608. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. † Applicant's unique citation designation number (optional) ‡ Applicant is to place a check mark here if English language Translation is attached

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number Unknown

Filing Date July 13, 2005

First Named Inventor Daniel E. Grupp

Group Art Unit Unknown

Examiner Name Unknown

Sheet 8 of 8

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/NN/		M. A. SOBOLEWSKI, et al., "Properties of Ultrathin Thermal Nitrides in Silicon Schottky Barrier Structures", <u>Applied Physics Letters, American Institute of Physics, Vol 54, No. 7, (2/13/89),pp. 638-640</u>	
/NN/		M. MIYAWAK, et al., "Improvement of Aluminum-Si Contact Performance in Native-Oxide-Free Processing", <u>IEEE Electron Device Letters, Vol. 11, No. 10, (10/90),pp. 448-450</u>	
/NN/		M.C. GILMER, et al., "Process and Manufacturing Challenges For High-K Gate Stack Systems", <u>Mat. Res. Soc. Symp. Proc. Vol. 567, (1999),pp. 323-341</u>	
/NN/		MANDELIS, ANDREAS, et al., "Evidence of a Surface Acceptor State in Undoped Semi-Insulating GaAs by Photothermal Radiometric Deep Level Transient Spectroscopy", <u>Sociedad Mexicana de Ciencias de Superficies y de Vacio, (1999),pp. 13-17</u>	

EXAMINER

/Ngan Ngo/

DATE CONSIDERED

07/06/2007

Substitute Disclosure Statement Form (PTO-1448)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number Unknown

Filing Date July 13, 2005

First Named Inventor Daniel E. Grupp

Group Art Unit Unknown

Examiner Name Unknown

Sheet 9 of 9

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/NN/		NOSHIOKA, YASUSHIRO, et al., "Dielectric Characteristics of Forinated Ultradry SiO ₂ ", <u>Appl. Phy. Letters</u> 54(12), (3/20/89), pp. 1127-1129	
/NN/		OKAMOTO, NAOYA, et al., "Near-Ohmic Contact of n-GaAs with Ga/Ga/GaAs Quasi-Metal-Insulator-Semiconductor Structure", <u>Jpn. J. Appl. Phys.</u> , Vol. 37, (1998), pp. 32483251	
/NN/		P. BAUERNSCHMITT, et al., "Yb-SiO ₂ -Si Tunneling Junctions", <u>Elsevier Publishers B.V.</u> , (1993), pp. 105-108	
/NN/		PORTER, LISA M., et al., "A Critical Review of Ohmic and Rectifying Contacts For Silicon Carbide", <u>Material Science and Engineering</u> , Vol. 34, No. 2, (11/1/95), pp. 83-105	

EXAMINER

/Ngan Ngo/

DATE CONSIDERED

07/06/2007

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 608. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	<i>Complete if Known</i>	
	Application Number	Unknown
	Filing Date	July 13, 2005
	First Named Inventor	Daniel E. Grupp
	Group Art Unit	Unknown
	Examiner Name	Unknown
Sheet 10 of 10		Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/NN/		R.A. MCKEE, et al., "Physical Structure And Inversion Charge at a Semiconductor Interface With a Crystalline Oxide", <u>www.sciencemag.org</u> , Vol. 293, (7/20/01), pp. 468-469	
/NN/		R.D. BRINGANSS, "Arsenic Passivation of Si and Ge Surfaces", <u>Critical Reviews in Solid State and Materials Sciences</u> , 17(4): 353-395, (1992), pp. 353-395	
/NN/		R.M.C. DE ALMEIDA, et al., "Reaction-Diffusion Model For Thermal Growth of Silicon Nitride Films on Si", <u>Physical Review B</u> , Vol. 62, No. 24, (12/1500), pp. R16 255-R16 258	
/NN/		R.T. TUNG, "Electron Transport of Inhomogeneous Schottky Barriers", <u>AT&T Bell Lab., Murray Hill, New Jersey 07974</u> , (3/21/91), pp. 3832-3834	

EXAMINER /Ngan Ngo/

DATE CONSIDERED 07/06/2007

Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 808. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 11 of 11

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/NN/		S. HARA, et al., "Control of Schottky And Ohmic Interfaces by Unpinning Fermi Level", <u>Elsevier Science B.V.</u> , pp. 394-399	
/NN/		S. HARA, et al., "Pinning-Controlled Metal/Semiconductor Interfaces", <u>Electrotechnical Laboratory</u> , pp. 802-807	
/NN/		S. HARA, et al., "Pinning-Controlled Ohmic Contacts: Application to SiC(0001)", <u>Elsevier Science B.V.</u> , pp. 218-221	
/NN/		S. VERHACEBEKE, et al., "Surface Characterization of Si After HF Treatments and its Influence in the Dielectric Breakdown of Thermal Oxides", <u>Research Aspirant of the Belgium National Fund for Scientific Research; Mat. Res. Soc. Symp. Proc., Vol. 259, Material Research Society</u> , (1992), pp. 391-399	

EXAMINER

/Ngan Ngo/

DATE CONSIDERED

07/06/2007

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. * Applicant's unique citation designation number (optional) * Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 12 of 12

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/NN/		S.A. WOLF, et al., "Spintronics: A Spin-Based Vision For The Future", <u>www.sciencemag.or</u> , Vol.294, (11/6/01),pp. 1488	
/NN/		S.M. SZE, "Metal-Semiconductor Contacts", <u>Physics of Semiconductor Devices</u> , John Wiley & Sons, (1981),	
/NN/		SCHMIDT, JAN , et al., "Carrier Recombination at Silicon-Silicon Nitride Interfaces Fabricated by Plasma-Enhanced Chemical Vapor Deposition", <u>Journal of Applied Physics</u> , Vol. 85, No. 7, (4/1/99),pp. 3626-3633	
/NN/		SEARCH REPORT, "International Searching Authority", <u>PCT/US03/25054</u> , (12/3/03),pp. 8	

EXAMINER

/Ngan Ngo/

DATE CONSIDERED

07/06/2007

Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 13 of 13

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cita No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/NN/		SHAIK, LAHIR , et al., "Experimental Identification of Nitrogen-Vacancy Complexes in Nitrogen Implanted Silicon", <u>Applied Physics Letters</u> , Vol. 79, No. 5, (7/30/01),pp. 623-625	
/NN/		SNYDER, JOHN P., et al., "Experimental Investigation of a PtSi Source And Drain Field Emission Transister", <u>American Institute of Physics</u> , pp. 1-3	
/NN/		T.I. KAMINS, et al., "Effect of Hydrogen on p-Type Epitaxial Silicon Sheet-Resistance Measurements", <u>Electrochemical and Solid-State Letters</u> 1(2), (1998),pp. 100-101	
/NN/		TERAJI, TOKUYUKI , et al., "Ohmic Contacts To n-Type 6H-SiC Without Post-Annealing", <u>Material Research Society Symposium Proceeding</u> , (4/8/96),pp. 149-154	

EXAMINER /Ngan Ngo/

DATE CONSIDERED 07/06/2007

Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 14 of 14

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/NN/		U.J.R. BAUMVOL, "Atomic Transport During Growth of Ultrathin Dielectrics on Silicon", <u>Surface Science Reports</u> 36, (1999),pp. 1-166	
/NN/		W.E. SPICER, et al., "Unified Mechanism For Schottky-Barrier Formation And III-V Oxide Interface States", <u>Physical Review Letters</u> , Vol. 44, No. 6, <u>Stanford Electronics Lab., Stanford Univ., Stanford, CA 94305</u> , (2/11/80),pp. 420-423	
/NN/		WANG, LIE , et al., "High Barrier GaN Schottky Diodes: Pt/GaN and Pd/GaN", <u>Dept. of Electrical Eng., Univ. of Minnesota, Minneapolis, Minnesota 55455; Appl. Phys. Letters</u> , Vol. 68(9), (2/26/96),pp. 1267-1270	
/NN/		WIDJAJA, YUNIARTO , et al., "Ab Initio Study and Decomposition of NH3 on Si(100)-(2x1)", <u>J. Phy. Chem B</u> , (2000),pp. 2527-2533	

EXAMINER

/Ngan Ngo/

DATE CONSIDERED

07/06/2007

Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Use as many sheets as necessary)

Complete if Known

Application Number	Unknown
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Group Art Unit	Unknown
Examiner Name	Unknown

Sheet 15 of 15

Attorney Docket No: 3771P003C

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/NN/		WRIGHT, PETER J., et al., "Hot-Electron Immunity of SiO ₂ Dielectrics with Fluorine Incorporation", <u>IEEE Electron Device Letters</u> , Vol. 10, No. 8, (8/8/89), pp. 347-348	
/NN/		Y. HAYAFUJI, et al., "Nitridation of Silicon and Oxidized-Silicon", <u>Sony Corp. Research Center, 174 Fujitsuka-Cho, Hodogaya-Ku, Yokohama, 240 Japan; J. Electrochem. Soc.: Solid State Science and Technology</u> , (9/82),	
/NN/		Y. K. KIM, et al., "Metal-Dependent Fermi-Level Movement in The Metal/Sulfur-Passivated InGaP Contact", <u>J. Vac. Sci. Technology A</u> 15(3), (1997), pp. 1124-1128	
/NN/		YANG, HANYANG, et al., "The Effects of Interfacial Sub-Oxide Transition Regions and Monolayer Level Nitridation on Tunneling Currents in Silicon Devices", <u>IEEE Electron Device Letters</u> , Vol. 21, No. 2, (2/2/00), pp. 76-78	

EXAMINER /Ngan Ngo/

DATE CONSIDERED 07/06/2007

Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Notice of References Cited	Application/Control No. 11/181,217	Applicant(s)/Patent Under Reexamination GRUPP ET AL.	
	Examiner Ngan Ngo	Art Unit 2818	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-7,084,423 B2	08-2006	Grupp et al.	257/30
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims



Application/Control No.

11/181,217

Examiner

Ngan Ngo

Applicant(s)/Patent under Reexamination

GRUPP ET AL.

Art Unit

2818

✓	Rejected
=	Allowed

—	(Through numeral) Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

Claim		Date									
Final	Original										
	Original	7									
	9										
	6										
	7										
1											
2											
3											
4											
5											
6											
7											
8											
9											
10											
11											
12											
13											
14											
15											
16											
17											
18											
19											
20											
21											
22											
23											
24											
25											
26											
27											
28											
29											
30											
31											
32											
33											
34											
35											
36											
37											
38											
39											
40											
41											
42											
43											
44											
45											
46											
47											
48											
49											
50											

Claim		Date									
Final	Original										
	51										
	52										
	53										
	54										
	55										
	56										
	57										
	58										
	59										
	60										
	61										
	62										
	63										
	64										
	65										
	66										
	67										
	68										
	69										
	70										
	71										
	72										
	73										
	74										
	75										
	76										
	77										
	78										
	79										
	80										
	81										
	82										
	83										
	84										
	85										
	86										
	87										
	88										
	89										
	90										
	91										
	92										
	93										
	94										
	95										
	96										
	97										
	98										
	99										
	100										

Claim		Date									
Final	Original										
	101										
	102										
	103										
	104										
	105										
	106										
	107										
	108										
	109										
	110										
	111										
	112										
	113										
	114										
	115										
	116										
	117										
	118										
	119										
	120										
	121										
	122										
	123										
	124										
	125										
	126										
	127										
	128										
	129										
	130										
	131										
	132										
	133										
	134										
	135										
	136										
	137										
	138										
	139										
	140										
	141										
	142										
	143										
	144										
	145										
	146										
	147										
	148										
	149										
	150										

Search Notes

Application/Control No.

11/181,217

Examiner

Ngan Ngo

Applicant(s)/Patent under
Reexamination

GRUPP ET AL.

Art Unit

2818

SEARCHED

Class	Subclass	Date	Examiner

INTERFERENCE SEARCHED

Class	Subclass	Date	Examiner

**SEARCH NOTES
(INCLUDING SEARCH STRATEGY)**

	DATE	EXMR
BRS search using EAST See printout	7/5/2007	NN

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

CHANGE OF CORRESPONDENCE ADDRESS Application

Address to:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	11/181,217
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Art Unit	2818
Examiner Name	NGO, Ngan V.
Attorney Docket Number	40003771-0003-003

Please change the Correspondence Address for the above-identified patent application to:

☒ The address associated with
Customer Number:

26263

OR

☐ Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

I am the:

- ☐ Applicant/Inventor
- ☐ Assignee of record of the entire interest.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).
- ☒ Attorney or agent of record. Registration Number 41,402
- ☐ Registered practitioner named in the application transmittal letter in an application without an executed oath or declaration. See 37 CFR 1.33(a)(1). Registration Number _____

Signature s/Tarek N. Fahmi/

Typed or Printed
Name Tarek N. Fahmi

Date September 5, 2007Telephone 650.798.0320

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt

EFS ID:	2162036
Application Number:	11181217
International Application Number:	
Confirmation Number:	6623
Title of Invention:	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	8791
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-003
Receipt Date:	05-SEP-2007
Filing Date:	13-JUL-2005
Time Stamp:	18:33:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Change of Address	40003771-0003-003_change_of_Address.pdf	36194 e1b04826d43899688dfefa26e4f5e8f1362c96f8	no	1

Warnings:

Information:	
Total Files Size (in bytes):	36194
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	

Electronic Acknowledgement Receipt

EFS ID:	2322264
Application Number:	11181217
International Application Number:	
Confirmation Number:	6623
Title of Invention:	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	26263
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-003
Receipt Date:	15-OCT-2007
Filing Date:	13-JUL-2005
Time Stamp:	17:34:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		40003771-0003-003_ROA_Filed_10_15_07.pdf	346401 9c7d40817dbfe14e13ed30d1b7df21d14e6ddc43	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment - After Non-Final Rejection	1	1
	Specification	2	2
	Claims	3	4
	Applicant Arguments/Remarks Made in an Amendment	5	5

Warnings:

Information:

Total Files Size (in bytes):	346401
-------------------------------------	--------

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/181,217		Filing Date 07/13/2005		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☒ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)		RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	10/15/2007	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 9 Minus	** 20	= 0	X \$25 =	0	OR	X \$ =		
	Independent (37 CFR 1.16(h))	* 2 Minus	*** 3	= 0	X \$105 =	0	OR	X \$ =		
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
					TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE		
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* Minus	**	=	X \$ =		OR	X \$ =		
	Independent (37 CFR 1.16(h))	* Minus	***	=	X \$ =		OR	X \$ =		
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR			
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
Jacqueline E. Couplin

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 11/181,217

First named inventor: Grupp, Daniel E.

Filed: 07/13/2005

Art unit: 2818

Examiner: Ngo, Ngan V.

Docket No.: 40003771-0003-003

Customer No.: 26263

Confirmation No.: 6623

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450.

AMENDMENTS

Sir:

In response to the Office Action of 13 July 2007, please amend the above-identified application as follow:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks begin on page 5 of this paper.

Amendments to the Specification:

Please replace paragraph [0001] with the following amended paragraph:

[0001] The present application is a CONTINUATION of U.S. patent application Ser. No. 10/217,758, filed Aug. 12, 2002, now U.S. Patent 7,084,423, incorporated herein by reference, which is related to U.S. patent application Ser. No. 10/342,578, filed Jan. 14, 2003, now U.S. Pat. No. 6,833,556, issued Dec. 21, 2004, incorporated by reference in its entirety

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1. (Cancelled)
2. (New) A method, comprising cleaning a semiconductor substrate with a cleaning solution to form a cleaned substrate; immersing, for a period of time between several seconds and approximately five (5) minutes, the cleaned substrate in a solution containing hydrogen and fluorine ions of between approximately 1%-50% by weight; removing the substrate from the solution and blow-drying the substrate with nitrogen, thereby forming an interface layer containing hydrogen and fluorine on the semiconductor substrate, said interface layer being of sufficient thickness to passivate a surface of said semiconductor substrate in a vicinity of said interface layer; subsequently depositing a metal layer over the interface layer using a thermally evaporated source, thereby forming a junction having a metal layer disposed over the interface layer disposed over the semiconductor, said junction having a specific contact resistance of less than or equal to approximately $1000\ \Omega\text{-}\mu\text{m}^2$.
3. (New) The method of claim 2, wherein following removal of the substrate from the solution and prior to blow-drying the substrate with nitrogen, rinsing the substrate in deionized water for less than 30 sec.
4. (New) A method, comprising heating a substrate containing a semiconductor surface in the presence of a nitrogenous material thereby to form a nitride interface layer of sufficient thickness to passivate said semiconductor surface; cooling the semiconductor surface; subsequently depositing a metal layer over the interface layer using a thermally evaporated source, thereby forming a junction having a metal layer disposed over the interface layer disposed over the

semiconductor, said junction having a specific contact resistance of less than or equal to approximately $1000\ \Omega\text{-}\mu\text{m}^2$.

5. (New) The method of claim 4, wherein the nitrogenous material comprises a gas.

6. (New) The method of claim 5, wherein the gas comprises ammonia.

7. (New) The method of claim 4, wherein the substrate contains an exposed silicon surface and is annealed at a temperature between approximately 300°C . and approximately 750°C .

8. (New) The method of claim 4, the heating is performed in a heating chamber and prior to the heating, pulling a vacuum of less than approximately one millionth of a Torr in the heating chamber, and then heating the substrate in the heating chamber.

9. (New) The method of claim 4, wherein the substrate is heated to a temperature between approximately 900°C and approximately 1000°C in an inert ambient.

10. (New) The method of claim 4, wherein the semiconductor surface is exposed to a pulse of ammonia for a time period between approximately 0.5 seconds and approximately 5 seconds.

REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 2 - 10 find support in the specification as filed, for example at paragraphs 58-66.

The requirement for a terminal disclaimer with respect to previous claim 1 has been obviated by this amendment. If a terminal disclaimer is required for the present claims, the Examiner is invited to contact the undersigned by telephone to arrange for same.

If there are any additional fees due in connection with this communication, please charge Deposit Account No. 19-3140.

Respectfully submitted,
SONNENSCHNEIN NATH & ROSENTHAL LLP

Dated: October 15, 2007

/Tarek N. Fahmi/
Tarek N. Fahmi
Reg. No. 41,402

P.O. Box 061080
Wacker Drive Station
Scars Tower
Chicago, IL 60606-1080
650-798-0320



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/181,217	07/13/2005	Daniel E. Grupp	40003771-0003-003	6623

26263 7590 12/20/2007
SONNENSCHN NATH & ROSENTHAL LLP
P.O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606-1080

EXAMINER

NGO, NGAN V

ART UNIT	PAPER NUMBER
----------	--------------

2818

MAIL DATE	DELIVERY MODE
-----------	---------------

12/20/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

**UNITED STATES DEPARTMENT OF COMMERCE****U.S. Patent and Trademark Office**

Address: COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
11181217	7/13/05	GRUPP ET AL.	40003771-0003-003

SONNENSCHN NATH & ROSENTHAL LLP
P.O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606-1080

EXAMINER

Ngan Ngo

ART UNIT	PAPER
----------	-------

2818

20071216

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The amendment filed on October 15, 2007 canceling claim drawn to the elected invention and presenting only claims drawn to a non-elected invention is non-responsive (MPEP § 821.03). The new claims are not readable on the elected invention because the method claims 2-10 are different invention from the elected device claim 1. Since the above-mentioned amendment appears to be a bona fide attempt to reply, applicant is given a TIME PERIOD of ONE (1) MONTH or THIRTY (30) DAYS, whichever is longer, from the mailing date of this notice within which to supply the omission or correction in order to avoid abandonment. EXTENSIONS OF THIS TIME PERIOD UNDER 37 CFR 1.136(a) ARE AVAILABLE

Ngan Ngo
Primary Examiner
Art Unit: 2818

Electronic Acknowledgement Receipt

EFS ID:	2655844
Application Number:	11181217
International Application Number:	
Confirmation Number:	6623
Title of Invention:	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	26263
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-003
Receipt Date:	31-DEC-2007
Filing Date:	13-JUL-2005
Time Stamp:	14:22:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		40003771-0003-003_ROA_Filed_12_31_07.pdf	383040 a062ce9bfe81ba496084c67320bc9669c7c59b94	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment - After Non-Final Rejection	1	1
	Specification	2	2
	Claims	3	4
	Applicant Arguments/Remarks Made in an Amendment	5	5

Warnings:

Information:

Total Files Size (in bytes):	383040
-------------------------------------	--------

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 11/181,217

First named inventor: Grupp, Daniel E.

Filed: 07/13/2005

Art unit: 2818

Examiner: Ngo, Ngan V.

Docket No.: 40003771-0003-003

Customer No.: 26263

Confirmation No.: 6623

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450.

AMENDMENTS

Sir:

In response to the Office Actions of 13 July 2007 and 20 December 2007, please amend the above-identified application as follow:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks begin on page 5 of this paper.

Amendments to the Specification:

Please replace paragraph [0001] with the following amended paragraph:

[0001] The present application is a CONTINUATION of U.S. patent application Ser. No. 10/217,758, filed Aug. 12, 2002, now U.S. Patent 7,084,423, incorporated herein by reference, which is related to U.S. patent application Ser. No. 10/342,578, filed Jan. 14, 2003, now U.S. Pat. No. 6,833,556, issued Dec. 21, 2004, incorporated by reference in its entirety

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1. (Currently Amended) An electrical device comprising an interface layer disposed between and in contact with both a metal and a semiconductor, the metal being a conductor that is not able to form a silicide with the semiconductor, the interface layer being configured to depin a Fermi level of the semiconductor, and wherein the electrical device has a specific contact resistance of less than or equal to approximately $1000\ \Omega - \mu m^2$.
2. (New) A method, comprising cleaning a semiconductor substrate with a cleaning solution to form a cleaned substrate; immersing, for a period of time between several seconds and approximately five (5) minutes, the cleaned substrate in a solution containing hydrogen and fluorine ions of between approximately 1%-50% by weight; removing the substrate from the solution and blow-drying the substrate with nitrogen, thereby forming an interface layer containing hydrogen and fluorine on the semiconductor substrate, said interface layer being of sufficient thickness to passivate a surface of said semiconductor substrate in a vicinity of said interface layer; subsequently depositing a metal layer over the interface layer using a thermally evaporated source, thereby forming a junction having a metal layer disposed over the interface layer disposed over the semiconductor, said junction having a specific contact resistance of less than or equal to approximately $1000\ \Omega - \mu m^2$.
3. (New) The method of claim 2, wherein following removal of the substrate from the solution and prior to blow-drying the substrate with nitrogen, rinsing the substrate in deionized water for less than 30 sec.
4. (New) A method, comprising heating a substrate containing a semiconductor surface in the presence of a nitrogenous material thereby to form a nitride interface layer of sufficient thickness

to passivate said semiconductor surface; cooling the semiconductor surface; subsequently depositing a metal layer over the interface layer using a thermally evaporated source, thereby forming a junction having a metal layer disposed over the interface layer disposed over the semiconductor, said junction having a specific contact resistance of less than or equal to approximately $1000\ \Omega\text{-}\mu\text{m}^2$.

5. (New) The method of claim 4, wherein the nitrogenous material comprises a gas.

6. (New) The method of claim 5, wherein the gas comprises ammonia.

7. (New) The method of claim 4, wherein the substrate contains an exposed silicon surface and is annealed at a temperature between approximately 300°C . and approximately 750°C .

8. (New) The method of claim 4, the heating is performed in a heating chamber and prior to the heating, pulling a vacuum of less than approximately one millionth of a Torr in the heating chamber, and then heating the substrate in the heating chamber.

9. (New) The method of claim 4, wherein the substrate is heated to a temperature between approximately 900°C and approximately 1000°C in an inert ambient.

10. (New) The method of claim 4, wherein the semiconductor surface is exposed to a pulse of ammonia for a time period between approximately 0.5 seconds and approximately 5 seconds.

REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1 has been amended and new claims 2 - 10 added. Claims 2-10 find support in the specification as filed, for example at paragraphs 58-66. Support for the amendment to claim 1 is found at paragraph 74. No new matter is added.

The requirement for a terminal disclaimer with respect to previous claim 1 has been obviated by this amendment. If a terminal disclaimer is required for the present claims, the Examiner is invited to contact the undersigned by telephone to arrange for same.

If there are any additional fees due in connection with this communication, please charge Deposit Account No. 19-3140.

Respectfully submitted,
SONNENSCHN NATH & ROSENTHAL LLP

Dated: December 31, 2007

/Tarek N. Fahmi/
Tarek N. Fahmi
Reg. No. 41,402

P.O. Box 061080
Wacker Drive Station
Sears Tower
Chicago, IL 60606-1080
650-798-0320

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/181,217		Filing Date 07/13/2005		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☒ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)		RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=		X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=		X \$	=			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	12/31/2007	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 10	Minus	** 20	= 0	X \$25 =	0		X \$	=
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	X \$105 =	0		X \$	=
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE	0		TOTAL ADD'L FEE	
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=		X \$	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=		X \$	=
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/VIKKI SHORT/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/181,217	07/13/2005	Daniel E. Grupp	40003771-0003-003	6623
26263 7590 03/27/2008 SONNENSCHN NATH & ROSENTHAL LLP P.O. BOX 061080 WACKER DRIVE STATION, SEARS TOWER CHICAGO, IL 60606-1080			EXAMINER NGO, NGAN V	
			ART UNIT 2818	PAPER NUMBER
			MAIL DATE 03/27/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 11/181,217	Applicant(s) GRUPP ET AL.	
	Examiner Ngan Ngo	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 December 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) 2-10 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☐ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) ☐ Other: _____ |

The amendment filed December 31, 2007 has been entered and made of record as paper no. 1207.

Newly submitted claims 2-10 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

I. Claim 1, drawn to a semiconductor device, classified in Class 257, subclass 30.

II. Claims 2-10, drawn to a process for making a semiconductor device, classified in Class 438, subclass 1+.

The inventions are distinct, each from the other because of the following reasons:

Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (M.P.E.P. § 806.05(f)). In the instant case unpatentability of the group I invention would not necessarily imply unpatentability of the group II invention, since the device of the group I invention could be made by processes materially different than those of the group II invention. For example, the device in claim 1 can be formed without the step of cleaning a semiconductor substrate for a period of time as required by claim 2.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 2-10 are withdrawn from consideration

as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 1 stand rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. &,084,423 B2.

Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 in this application inherently has a thickness of less than 1nm in order to depin a Fermi level of the semiconductor and the Fermi level of the metal. It is well known that silicon is used as semiconductor. Since the interface layer is formed between the metal layer and the semiconductor layer, the interface layer inherently prevents the metal layer to form a silicide with the semiconductor. Therefore, claim 1 in this application is obvious over claim 1 of the U.S. Patent No. &,084,423 B2.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication should be directed to Examiner Ngan Ngo at telephone number (571) 272-1711. The fax phone number for the organization where this application or proceeding is assigned is (571)-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Application/Control Number: 11/181,217
Art Unit: 2818

Page 5

/Ngan Ngo/

Primary Examiner, Art Unit 2818

Ngan Ngo

March 27, 2008

<i>Index of Claims</i> 	Application/Control No. 11181217	Applicant(s)/Patent Under Reexamination GRUPP ET AL.
	Examiner Ngan Ngo	Art Unit 2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	03/21/2008								
	1	✓								
	2	N								
	3	N								
	4	N								
	5	N								
	6	N								
	7	N								
	8	N								
	9	N								
	10	N								

Electronic Patent Application Fee Transmittal

Application Number:	11181217			
Filing Date:	13-Jul-2005			
Title of Invention:	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions			
First Named Inventor/Applicant Name:	Daniel E. Grupp			
Filer:	Tarek N. Fahmi			
Attorney Docket Number:	40003771-0003-003			
Filed as Large Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Processing Fee, except for Provis. apps	1808	1	130	130
Total in USD (\$)				130

Electronic Acknowledgement Receipt

EFS ID:	3535615
Application Number:	11181217
International Application Number:	
Confirmation Number:	6623
Title of Invention:	Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	26263
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-003
Receipt Date:	27-JUN-2008
Filing Date:	13-JUL-2005
Time Stamp:	18:40:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 130
RAM confirmation Number	3949
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
-----------------	----------------------	-----------	----------------------------------	------------------	------------------

1	Terminal Disclaimer Filed	Terminal_Disclaimer_Filed_6_27_08.pdf	182192 dce4f7e71463c2c18809b1139fb975e436770530	no	1
Warnings:					
Information:					
2		40003771-0003-003_ROA_Filed_6_27_08.pdf	169894 7466d3132a0de2b68dd5510e88eb2471211bdc79	yes	3
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment After Final		1	1	
	Claims		2	2	
	Applicant Arguments/Remarks Made in an Amendment		3	3	
Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8231 a3726bc92554faf3d6d55df632a10d4a52d719d1	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			360317		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/181,217		Filing Date 07/13/2005		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)		SMALL ENTITY ☒ OR			OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=		X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=		X \$	=			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)		SMALL ENTITY OR			OTHER THAN SMALL ENTITY		
AMENDMENT	06/27/2008	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
Total (37 CFR 1.16(i))	* 1	Minus	** 20	= 0	X \$25 =	0		X \$	=	
Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0	X \$105 =	0		X \$	=	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE	0		TOTAL ADD'L FEE		
(Column 1)			(Column 2)		SMALL ENTITY OR			OTHER THAN SMALL ENTITY		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=		X \$	=	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=		X \$	=	
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE			TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/THERESA I. OKON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 11/181,217

First named inventor: Grupp, Daniel E.

Filed: 07/13/2005

Art unit: 2818

Examiner: Ngo, Ngan V.

Docket No.: 40003771-0003-003

Customer No.: 26263

Confirmation No.: 6623

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450.

AMENDMENTS

Sir:

In response to the Office Action of 27 March 2008, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 3 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of the claims in the application:

Listing of Claims:

1. (Previously Presented) An electrical device comprising an interface layer disposed between and in contact with both a metal and a semiconductor, the metal being a conductor that is not able to form a silicide with the semiconductor, the interface layer being configured to depin a Fermi level of the semiconductor, and wherein the electrical device has a specific contact resistance of less than or equal to approximately $1000 \Omega - \mu m^2$.

2-10. (Cancelled).

REMARKS

Reconsideration of this application, as amended, is respectfully requested.

The obviousness-type double patenting rejection in light of claim 1 of US Patent Number 7,084,423 is noted. A terminal disclaimer for the present claim is filed along with this amendment. Thus, removal of the obviousness-type double patenting rejection in light of claim 1 is respectfully requested.

If there are any additional fees due in connection with this communication, please charge Deposit Account No. 19-3140.

Respectfully submitted,
SONNENSCHNEIN NATH & ROSENTHAL LLP

Dated: June 27, 2008

/Tarek N. Fahmi/

Tarek N. Fahmi
Reg. No. 41,402

P.O. Box 061080
Wacker Drive Station
Sears Tower
Chicago, IL 60606-1080
650-798-0320

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING
REJECTION OVER A "PRIOR" PATENT**Docket Number (Optional)
40003771-0003-003

In re Application of: Grupp, Daniel E.

Application No.: 11/181,217

Filed: July 13, 2005

For: Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions

The owner*, Acorn Technologies, Inc., of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term **prior patent** No. 7,084,423 as the term of said prior patent is defined in 35 U.S.C. 154 and 173, and as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 and 173 of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ For submissions on behalf of a business/organization (e.g., corporation, partnership, university, government agency, etc.), the undersigned is empowered to act on behalf of the business/organization.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

2. ☒ The undersigned is an attorney or agent of record. Reg. No. 41,402

/Tarek N. Fahmi/
Signature

June 27, 2008
Date

Tarek N. Fahmi
Typed or printed name

650.798.0320
Telephone Number

- ☒ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Application Number 	Application No. 11/181,217	Applicant(s) GRUPP ET AL.	
	Terminal Disclaimer Filed: 06/27/08		

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Document Code - DISQ	This patent is subject to a Terminal Disclaimer	Reasons:
INTERNAL DOCUMENT – DO NOT MAIL		

U.S. Patent and Trademark Office

NOTE DISCLAIMER:

The term of this patent shall not extend
beyond the expiration date of Pat. No. 7,084,423,

☒ **SHARON S. HOPPE**
PARALEGAL SPECIALIST
TECHNOLOGY CENTER 2800

☐ **RENEE M. PRESTON**
PARALEGAL SPECIALIST
TECHNOLOGY CENTER 2800

☐ **TREDELLE D. JACKSON**
PARALEGAL SPECIALIST
TECHNOLOGY CENTER 2800

☐ **NOVA M. CHAPMAN**
PARALEGAL SPECIALIST
TECHNOLOGY CENTER 2800

☐ **CASSANDRA B. PARIS**
PARALEGAL SPECIALIST
TECHNOLOGY CENTER 2800



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

26263 7590 08/08/2008

SONNENSCHN NATH & ROSENTHAL LLP
P.O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606-1080

EXAMINER

NGO, NGAN V

ART UNIT

PAPER NUMBER

2893

DATE MAILED: 08/08/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

11/181,217

07/13/2005

Daniel E. Grupp

40003771-0003-003

6623

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$720	\$300	\$0	\$1020	11/10/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26263

7590

08/08/2008

SONNENSCHN NATH & ROSENTHAL LLP
P.O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606-1080

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

11/181,217

07/13/2005

Daniel E. Grupp

40003771-0003-003

6623

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$720	\$300	\$0	\$1020	11/10/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2893	257-030000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s); (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/181,217	07/13/2005	Daniel E. Grupp	40003771-0003-003	6623
26263	7590	08/08/2008	EXAMINER	
SONNENSCHN NATH & ROSENTHAL LLP P.O. BOX 061080 WACKER DRIVE STATION, SEARS TOWER CHICAGO, IL 60606-1080			NGO, NGAN V	
			ART UNIT	PAPER NUMBER
			2893	
DATE MAILED: 08/08/2008				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 301 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 301 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/181,217	GRUPP ET AL.	
	Examiner	Art Unit	
	Ngan Ngo	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment and the terminal disclaimer filed 6-27-08.
2. ☒ The allowed claim(s) is/are 1.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| <ol style="list-style-type: none"> 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date ____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | <ol style="list-style-type: none"> 5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date ____. 7. ☐ Examiner's Amendment/Comment 8. ☐ Examiner's Statement of Reasons for Allowance 9. ☐ Other ____. |
|--|---|

/Ngan Ngo/
Primary Examiner, Art Unit 2893



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 6623

SERIAL NUMBER 11/181,217	FILING or 371(c) DATE 07/13/2005 RULE	CLASS 257	GROUP ART UNIT 2893	ATTORNEY DOCKET NO. 40003771-0003-003		
APPLICANTS Daniel E. Grupp, Palo Alto, CA; Daniel J. Connelly, Redwood City, CA; ** CONTINUING DATA ***** This application is a CON of 10/217,758 08/12/2002 PAT 7,084,423 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** ** SMALL ENTITY ** 08/01/2005						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/NGAN V NGO/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 6	TOTAL CLAIMS 1	INDEPENDENT CLAIMS 1
ADDRESS SONNENSCHN NATH & ROSENTHAL LLP P.O. BOX 061080 WACKER DRIVE STATION, SEARS TOWER CHICAGO, IL 60606-1080 UNITED STATES						
TITLE Method for depinning the fermi level of a semiconductor at an electrical junction and devices incorporating such junctions						
FILING FEE RECEIVED 500	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4650	fermi and interface	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 12:19
L2	6	L1 and (de-pin or de adj pin)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/07/29 12:19
L3	2	("7084423").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/07/29 13:30
L4	2035	(257/30,485, E29.148,E29.338). OCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2008/07/29 13:50

7/ 29/ 08 1:51:05 PM

C:\Documents and Settings\NNgo\My Documents\ EAST\ workspaces\ 11181217.wsp

<i>Index of Claims</i> 	Application/Control No. 11181217	Applicant(s)/Patent Under Reexamination GRUPP ET AL.
	Examiner Ngan Ngo	Art Unit 2818

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	03/21/2008	07/29/2008						
	1	✓	=						
	2	N	-						
	3	N	-						
	4	N	-						
	5	N	-						
	6	N	-						
	7	N	-						
	8	N	-						
	9	N	-						
	10	N	-						

Search Notes 	Application/Control No. 11181217	Applicant(s)/Patent Under Reexamination GRUPP ET AL.
	Examiner Ngan Ngo	Art Unit 2893

SEARCHED			
Class	Subclass	Date	Examiner
257	30, 485, E29.148, E29.338	7-29-08	NN

SEARCH NOTES		
Search Notes	Date	Examiner
BRS search using EAST. See printout	7-29-08	NN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
257	30, 485, E29.148, E29.338	7-29-08	NN

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 11/181,217

First named inventor: Grupp, Daniel E.

Filed: 07/13/2005

Art unit: 2818

Examiner: Ngo, Ngan V.

Docket No.: 40003771-0003-003

Customer No.: 26263

Confirmation No.: 6623

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450.

AMENDMENTS

Sir:

In response to the Office Action of 27 March 2008, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 3 of this paper.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)

Complete if Known

Application Number	Unknown 11/181217
Filing Date	July 13, 2005
First Named Inventor	Daniel E. Grupp
Group Art Unit	Unknown 2818
Examiner Name	Unknown NGAN NGO

Sheet 1 of 1

Attorney Docket No: 3771P003C

US PATENT DOCUMENTS

Examiner Initial *	Cite No. *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/NN/		US-0,789,388	08/13/1997 EP	Hara, Shiro, et al.	
		US-3,590,471	07/06/1971	Lepseter, , et al.	
		US-3,708,360	01/02/1973	Wakefield, Jr., , et al.	
		US-3,983,264	09/28/1976	Schroen, Walter H., et al.	
		US-4,056,642	11/01/1977	Saxena, Arjun N., et al.	
		US-4,300,152	11/10/1981	Lepseter,	
		US-4,485,550	12/04/1984	Koenske, , et al.	
		US-5,021,365	06/04/1991	Kirchner, , et al.	
		US-5,399,208	03/21/1995	de Lyon,	
		US-5,578,848	11/26/1996	Kwong, , et al.	
		US-5,596,218	01/21/1997	Soleimani, , et al.	
		US-5,612,567	03/18/1997	Baliga,	
		US-5,663,584	09/02/1997	Welch,	
		US-5,801,398	09/01/1998	Hebiguchi,	
		US-5,888,891	03/30/1999	Gould,	
		US-5,939,783	08/17/1999	Hao, , et al.	
		US-6,037,605	03/14/2000	Yoshimura,	
		US-6,096,590	08/01/2000	Chan, , et al.	
		US-6,150,288	11/21/2000	Sun, , et al.	
		US-6,198,113	03/06/2001	Grupp, Daniel E.	
		US-6,207,976	03/27/2001	Takshashi, , et al.	
		US-6,261,932	07/17/2001	Hulfachor,	
		US-6,291,866	09/18/2001	Wallace, , et al.	
		US-6,291,867	09/18/2001	Wallace, , et al.	
/NN/		US-6,303,479	10/16/2001	Snyder,	

2X
8/20/08

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. *	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T*
/NN/		EP-0295490	12/21/1988	Fowler, Alan B., et al.		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No *	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issuue number(s), publisher, city and/or country where published.	T*
---------------------	-----------	--	----

EXAMINER

/Ngan Ngo/

DATE CONSIDERED

07/06/2007

Substitute Disclosure Statement Form (PTO-1449)
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 608. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. Applicant's unique citation designation number (optional) Applicant is to place a check mark here if English language Translation is attached

Electronic Patent Application Fee Transmittal				
Application Number:		11181217		
Filing Date:		13-Jul-2005		
Title of Invention:		METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS		
First Named Inventor/Applicant Name:		Daniel E. Grupp		
Filer:		Tarek N. Fahmi		
Attorney Docket Number:		40003771-0003-003		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	2501	1	755	755
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1055

Electronic Acknowledgement Receipt

EFS ID:	4255756
Application Number:	11181217
International Application Number:	
Confirmation Number:	6623
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	26263
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-003
Receipt Date:	07-NOV-2008
Filing Date:	13-JUL-2005
Time Stamp:	19:01:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 1055
RAM confirmation Number	3607
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
-----------------	----------------------	-----------	-------------------------------------	------------------	------------------

1	Issue Fee Payment (PTO-85B)	40003771-0003-003_Issue_Fee _Transmittal_Filed_11_7_08. pdf	249012 f9f483db7d8c47985ed6641905b7475f271a afb6	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	31539 3f9ec78cfd3031c588e64ce6bd72146962e b6eb	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			280551		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26263 7590 08/08/2008

SONNENSCHN NATH & ROSENTHAL LLP
P.O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606-1080

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/181.217	07/13/2005	Daniel E. Grupp	40003771-0003-003	6623

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$720	\$300	\$0	\$1020	11/10/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGO, NGAN V	2893	257-030000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

- 1 SONNENSCHN NATH &
- 2 ROSENTHAL LLP
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

ACORN TECHNOLOGIES, INC.

SANTA MONICA, CALIFORNIA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☒ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 19-3140 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Tarek N. Fahmi/

Date November 7, 2008

Typed or printed name Tarek N. Fahmi

Registration No. 41,402

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/181,217	12/09/2008	7462860	40003771-0003-003	6623

26263 7590 11/19/2008
SONNENSCHN NATH & ROSENTHAL LLP
P.O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606-1080

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 301 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Daniel E. Grupp, Palo Alto, CA;
Daniel J. Connelly, Redwood City, CA;

**REVOCATION OF PREVIOUS POWERS OF ATTORNEY WITH NEW
GENERAL POWER OF ATTORNEY TO PROSECUTE APPLICATIONS AND REEXAMINATION
PROCEEDINGS BEFORE THE UNITED STATES PATENT AND TRADEMARK OFFICE**

I hereby revoke all previous powers of attorney given in the application(s), reexamination proceeding(s) and/or patent(s) listed below and appoint:

Practitioners associated with the Customer Number

27571

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications and reexamination proceedings assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application(s), reexamination proceeding(s) and/or patent(s) listed below to the address associated with Customer Number 27571.

Assignee Name and Address:

Acom Technologies, Inc.
1200 Prospect Street, Suite 475
La Jolla, California 92037

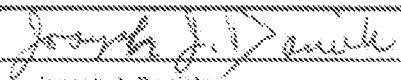
A statement under 37 CFR 3.73(b) is attached.

List of application(s), reexamination proceeding(s) and/or patent(s):

See Attached List

SIGNATURE OF ASSIGNEE OF RECORD

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date:	3/14/2012
Name	Joseph J. Daniele	Telephone:	858-551-1552
Title	Chief Operating Officer		

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Acorn Technologies, Inc.

States that it is:

1. ☒ The assignee of the entire right, title, and interest, or
2. ☐ an assignee of less than the entire right, title and interest
(The extent (by percentage) of its ownership interest is: _____ %)

in the patent applications/patents identified in the attached spreadsheet by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent applications/patents identified in the attached spreadsheet. The assignment was recorded in the United States Patent and Trademark Office at the Reel and Frame listed thereon.

OR

B. ☐ A chain of title from the inventor(s) of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark office at
Reel _____, Frame _____, or for which a copy thereof is attached.
2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark office at
Reel _____, Frame _____, or for which a copy thereof is attached.
3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark office at
Reel _____, Frame _____, or for which a copy thereof is attached.

Additional documents in the chain of title are listed on a supplemental sheet.

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Tarek N. Fahmi/
Signature

March 26, 2012
Date

Tarek N. Fahmi
Printed or Typed Name

866-377-4833
Telephone Number

Attorney of Record
Title

AppNumber	FileDate	AssignmentTo	Reel	Frame	Ref No
10/217758	12-Aug-02	Acom Technologies, Inc.	013195	0068	40003771-0003-002
11/181217	13-Jul-05	Acom Technologies, Inc.	13195	0068	40003771-0003-003
10/753504	07-Jan-04	Acom Technologies, Inc.	015453	0248	40003771-0003-005
10/753504	07-Jan-04	Acom Technologies, Inc.	016115	0318	40003771-0003-005
10/753504	07-Jan-04	Acom Technologies, Inc.	018401	0333	40003771-0003-005
12/197996	25-Aug-08	Acom Technologies, Inc.	022077	0447	40003771-0003-403
13/022522	07-Feb-11	Acom Technologies, Inc.	022077	0447	40003771-0003-453
10/342576	14-Jan-03	Acom Technologies, Inc.	016771	0810	40003771-0004-002
11/403185	11-Apr-06	Acom Technologies, Inc.	018181	0437	40003771-0004-403
10/754966	09-Jan-04	Acom Technologies, Inc.	18181	437	40003771-0004-004
13/022559	07-Feb-11	Acom Technologies, Inc.	018181	0437	40003771-0004-453
10/832576	26-Apr-04	Acom Technologies, Inc.	015846	0802	40003771-0005-002
11/010048	09-Dec-04	Acom Technologies, Inc.	016081	0879	40003771-0007-002
11/166286	23-Jun-05	Acom Technologies, Inc.	016729	0283	40003771-0008-002
13/019789	02-Feb-11	Acom Technologies, Inc.	016729	0283	40003771-0008-004
11/678397	23-Feb-07	Acom Technologies, Inc.	019424	0808	40003771-0009-002
12/878930	09-Sep-10	Acom Technologies, Inc.	019424	0808	40003771-0009-004
12/253769	17-Oct-08	Acom Technologies, Inc.	022058	0069	40003771-0010-002
12/253835	17-Oct-08	Acom Technologies, Inc.	022063	0521	40003771-0011-002
12/549227	27-Aug-09	Acom Technologies, Inc.	023159	0144	40003771-0014-002
61/537433	21-Sep-11	Acom Technologies, Inc.	027228	0055	40003771-0015-051

Electronic Acknowledgement Receipt

EFS ID:	12396256
Application Number:	11181217
International Application Number:	
Confirmation Number:	6623
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	26263
Filer:	Tarek N. Fahmi/Jennifer Stewart
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	40003771-0003-003
Receipt Date:	26-MAR-2012
Filing Date:	13-JUL-2005
Time Stamp:	19:02:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Acorn_executed_POA.pdf	325167 80c6d19a8e22bf29e157c34ec08b5aba90fe056d	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Power of Attorney	1	1
	Assignee showing of ownership per 37 CFR 3.73(b).	2	3
Warnings:			
Information:			
Total Files Size (in bytes):		325167	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/181,217	07/13/2005	Daniel E. Grupp	40003771-0003-003

CONFIRMATION NO. 6623

POA ACCEPTANCE LETTER



27571
TAREK N. FAHMI, APC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

Date Mailed: 04/04/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/26/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/kmoukdarath/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101