

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (37 CFR 1.63) ☐ Declaration Submitted with Initial Filing OR ☒ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16(e)) required)		Attorney Docket Number	40003771-0003-403
		First Named Inventor	Daniel E. Grupp
		COMPLETE IF KNOWN	
		Application Number	12/197,996
		Filing Date	August 25, 2008
		Art Unit	2811
		Examiner Name	Not Yet Assigned

As a below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below, next to my name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

the specification of which (Title of the Invention)

☐ is attached hereto.

OR

☒ was filed on (if applicable):

08/25/2008 as United States Application Number 12/197,996

as PCT International Application Number _____

and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment specifically referred to above.

I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application. I do not know and do not believe that the claimed invention was in public use or on sale in the United States of America more than one year prior to this application, nor do I know or believe that the invention has been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, or inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s):

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No

Appointment of Practitioners:

I hereby appoint the practitioners associated with Customer Number: 26263 as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected herewith.

If this patent application is assigned, then the undersigned hereby authorizes the patent attorneys and patent agents named herein to accept and follow instructions from the assignee(s) as to any action to be taken in the United States Patent and Trademark Office regarding this application without direct communication between the patent attorneys and patent agents and the undersigned. In the event of a change in the persons from whom instructions may be taken, at least one patent attorney or patent agent named herein will be so notified by the undersigned.

Correspondence:

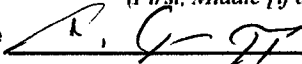
Direct all correspondence to Customer Number 26263

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR: ☐ A petition has been filed for this undersigned inventor

Full Name: Daniel E. Grupp

(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature 

Date 15 Dec 2008

Residence Palo Alto, California, USA
(City, State, Country)

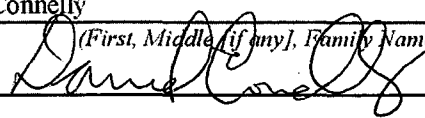
Citizenship USA
(Country)

Mailing Address 334 Leland Avenue
Palo Alto, California 94306

NAME OF SECOND INVENTOR: ☐ A petition has been filed for this undersigned inventor

Full Name: Daniel J. Connelly

(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature 

Date _____

Residence Redwood City, California, USA
(City, State, Country)

Citizenship USA
(Country)

Mailing Address ~~525 Rutherford Avenue~~
~~Redwood City, California 94061~~

653 KANSAS ST
SAN FRANCISCO CA 94107

NAME OF THIRD INVENTOR: ☐ A petition has been filed for this undersigned inventor

Full Name: _____

(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature _____

Date _____

Residence _____

(City, State, Country)

Citizenship _____

(Country)

Mailing Address _____

NAME OF FOURTH INVENTOR: ☐ A petition has been filed for this undersigned inventor

Full Name: _____

(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature _____

Date _____

Residence _____

(City, State, Country)

Citizenship _____

(Country)

Mailing Address _____

NAME OF FIFTH INVENTOR: ☐ A petition has been filed for this undersigned inventor

Full Name: _____

(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature _____

Date _____

Residence _____

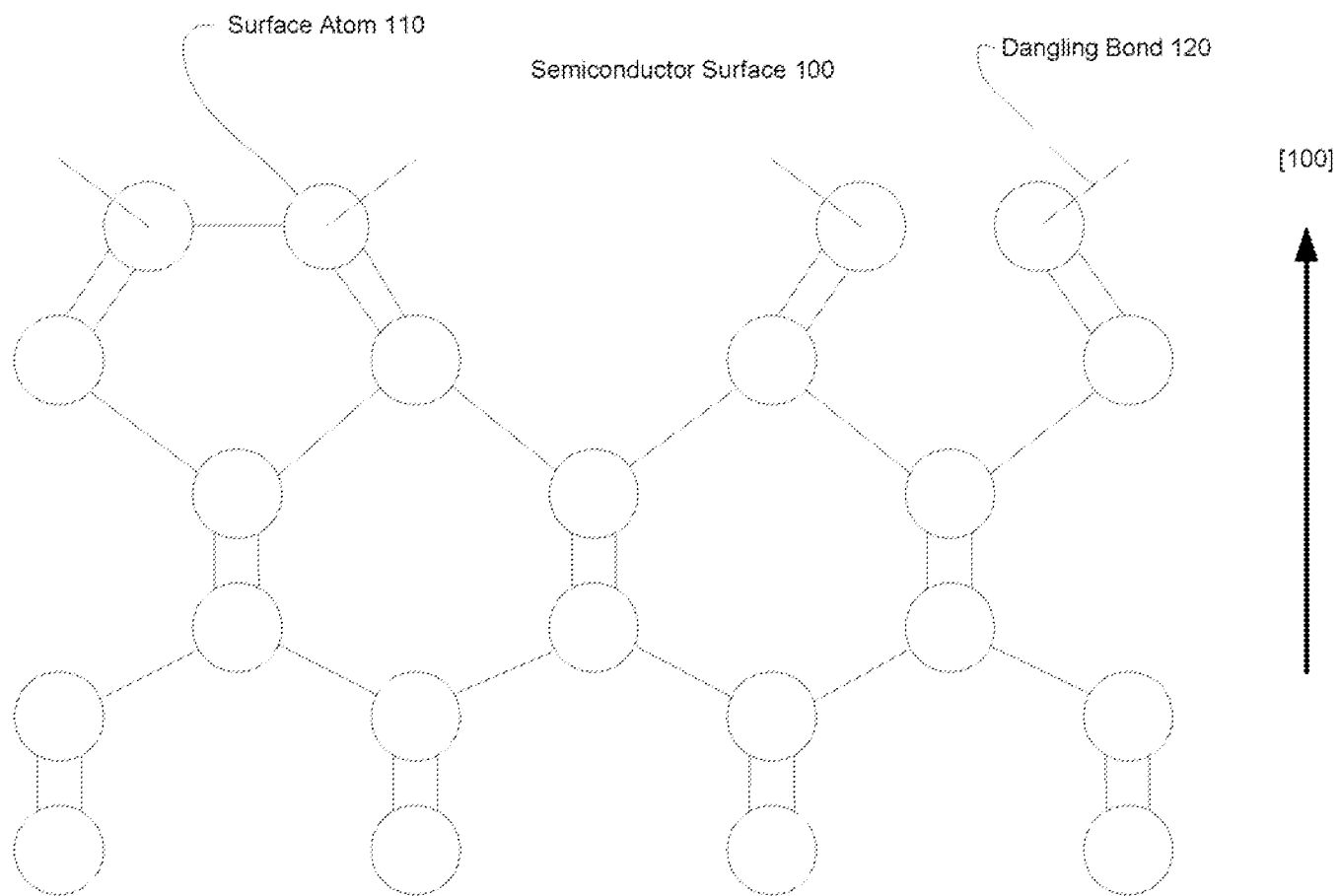
(City, State, Country)

Citizenship _____

(Country)

Mailing Address _____

Fig. 1



Energy Scales for Metal - Semiconductor Junctions

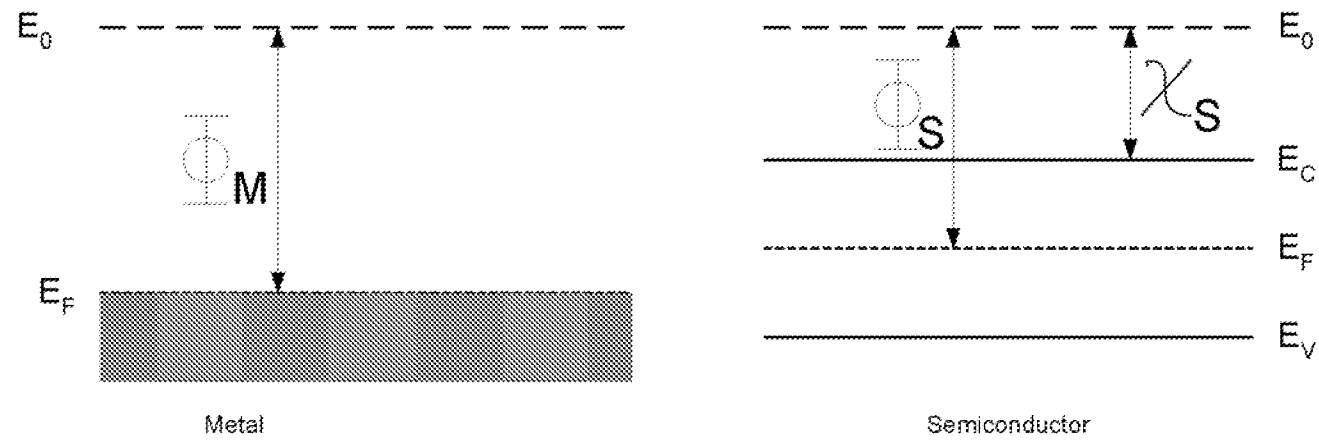


Fig. 2

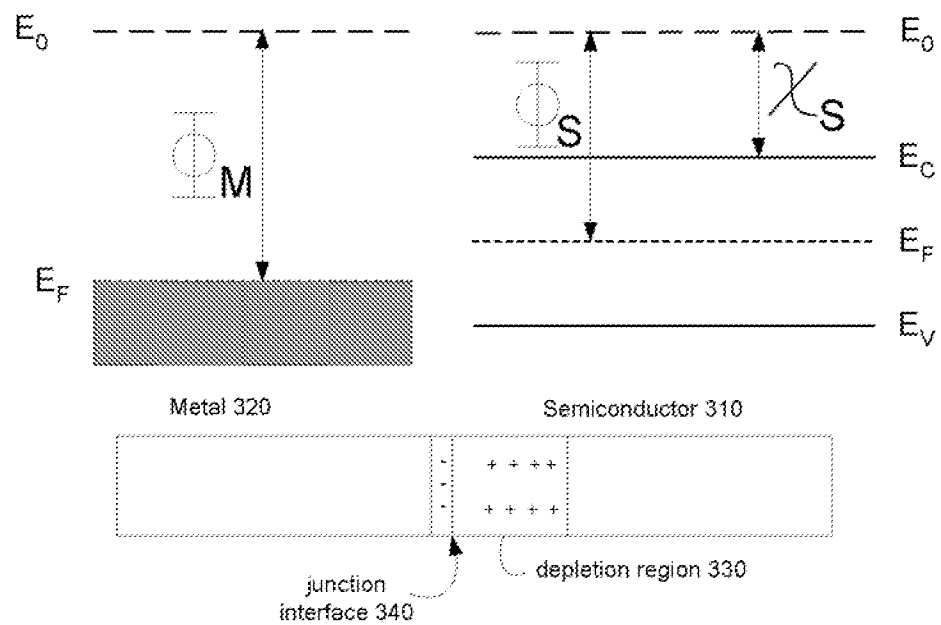


Fig. 3

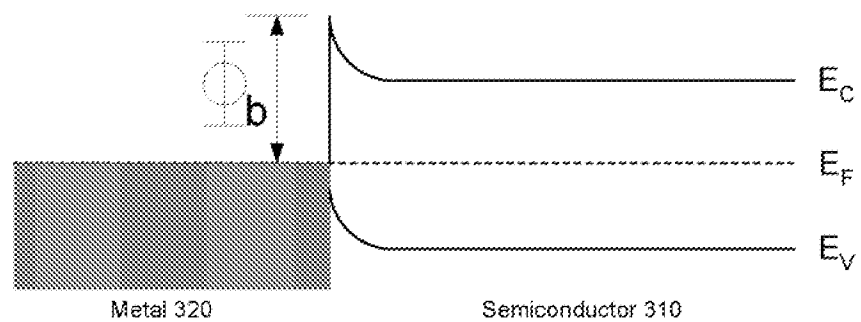


Fig. 4

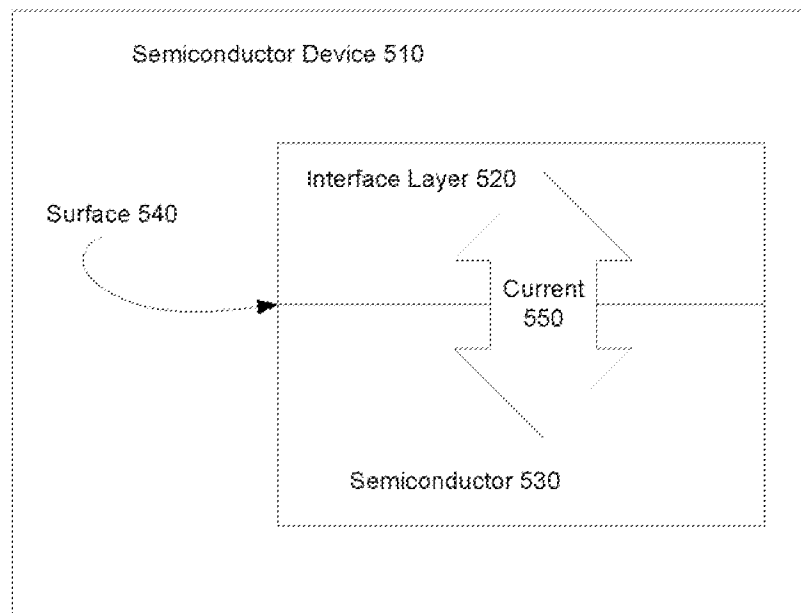


Fig. 5

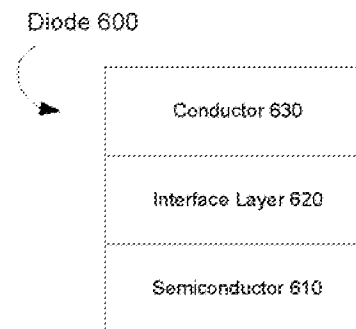


Fig. 6

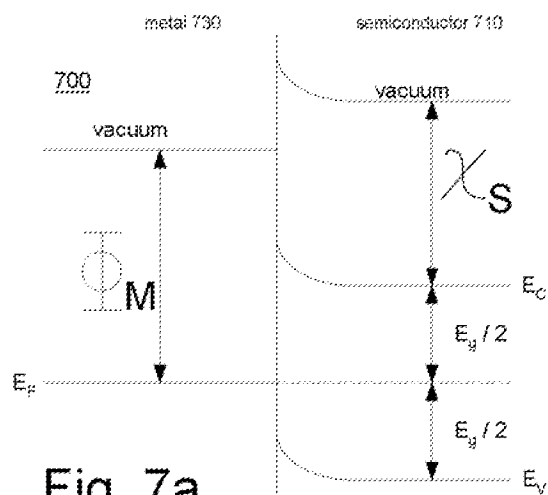


Fig. 7a

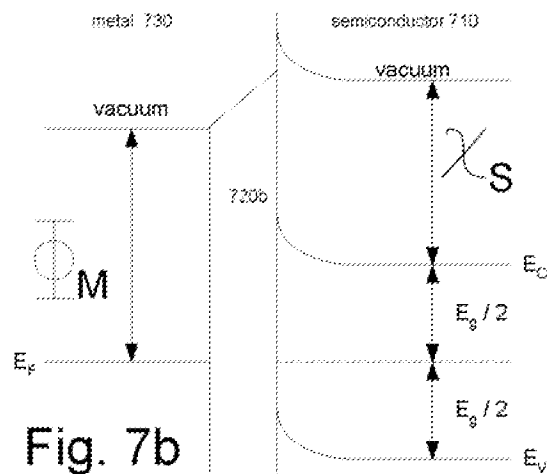


Fig. 7b

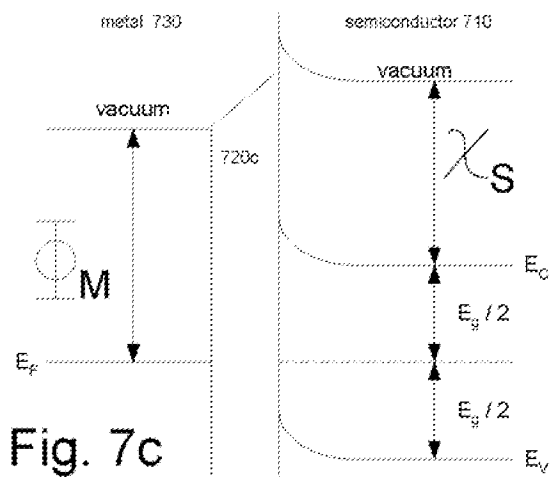


Fig. 7c

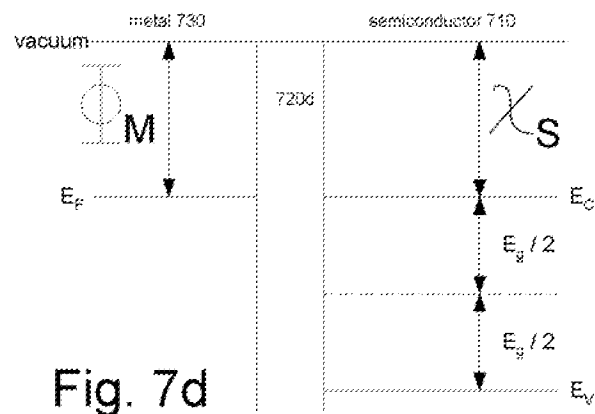


Fig. 7d

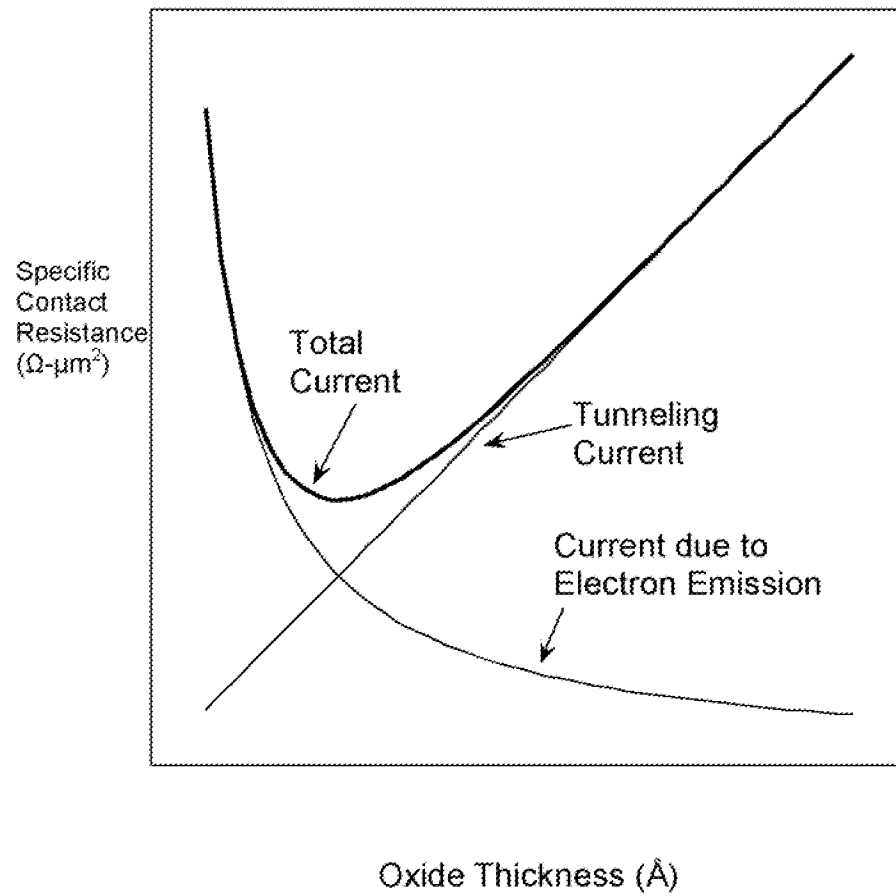


Fig. 8

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS		
First Named Inventor/Applicant Name:		Daniel E. Grupp		
Filer:		Tarek N. Fahmi		
Attorney Docket Number:		40003771-0003-453		
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	82	82
Utility Search Fee	2111	1	270	270
Utility Examination Fee	2311	1	110	110
Pages:				
Claims:				
Claims in excess of 20	2202	21	26	546
Multiple dependent claims	2203	1	195	195
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1203

Electronic Acknowledgement Receipt

EFS ID:	9393470
Application Number:	13022522
International Application Number:	
Confirmation Number:	6852
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	26263
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-453
Receipt Date:	07-FEB-2011
Filing Date:	
Time Stamp:	19:44:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1203
RAM confirmation Number	6007
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
-----------------	----------------------	-----------	-------------------------------------	------------------	------------------

1	Oath or Declaration filed	40003771-0003-453_executed_ Dec_and_POA.pdf	165794 3794697be566127b17f24c16a48492f2b96f 25bc	no	3
Warnings:					
Information:					
2		40003771-0003-453_APLN_File d_02_07_2011.pdf	4417245 478495262ee39df354293a2f901e28cba5b 6c1ca	yes	44
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	32	
	Claims		33	37	
	Abstract		38	38	
	Drawings-only black and white line drawings		39	44	
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	38092 c40f539189a1f4c075993cc2f9bbca5d09b9 ada0	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			4621131		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL
JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS**

INVENTORS

**DANIEL E. GRUPP
DANIEL J. CONNELLY**

Correspondence via: Customer No.: 26263

Attorney's Docket No.: 40003771-0003-453

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

RELATED APPLICATIONS

[0001] This is a Divisional of U.S. Patent Application 12/197,996, filed August 25, 2008, incorporated herein by reference, which is a Divisional of U.S. Patent Application No. 11/181,217 filed July 13, 2005, which is a Continuation of U.S. Patent Application No. 10/217,758, filed August 12, 2002, now U.S. Patent 7,084,423, incorporated herein by reference, which is related to U.S. Patent Application No. 10/342,578, filed January 14, 2003, now U.S. Pat. No. 6,833,556, issued Dec. 21, 2004, incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0002] The invention relates generally to semiconductor processing and semiconductor devices. More particularly, the invention relates to a process for depinning the Fermi level of a semiconductor at a metal-interface layer-semiconductor junction and to devices that employ such a junction.

BACKGROUND

[0003] One of the most basic electrical junctions used in modern devices is the metal-semiconductor junction. In these junctions, a metal (such as aluminum) is brought in contact with a semiconductor (such as silicon). This forms a device (a diode) which can be inherently rectifying; that is, the junction will tend to conduct current in one direction more favorably than in the other direction. In other cases, depending on the materials used, the junction may be ohmic in nature (i.e., the contact may have negligible resistance regardless of the direction of current flow). Grondahl and Geiger first studied the rectifying form of these junctions in 1926, and by 1938 Schottky had developed a theoretical explanation for the rectification that was observed.

[0004] Schottky's theory explained the rectifying behavior of a metal-semiconductor contact as depending on a barrier at the surface of contact between the metal and the semiconductor. In this model, the height of the barrier (as measured by the potential necessary for an electron to pass from the metal to the semiconductor) was postulated as the difference between the work function of the metal (the work function is the energy required to free an electron at the Fermi level of the metal, the Fermi level being the highest occupied energy state of the metal at $T = 0$) and the electron affinity of the semiconductor (the electron affinity is the difference between the energy of a free electron and the conduction band edge of the semiconductor). Expressed mathematically:

$$\phi_B = \phi_M - \chi_s \quad [1]$$

where Φ_B is the barrier height, Φ_M is the work function of the metal and χ_s is the electron affinity of the semiconductor.

[0005] Not surprisingly, many attempts were made to verify this theory experimentally. If the theory is correct, one should be able to observe direct variations in barrier heights for metals of different work functions when put in contact with a common semiconductor. What is observed, however, is not direct scaling, but instead only a much weaker variation of barrier height with work function than implied by the model.

[0006] Bardeen sought to explain this difference between theoretical prediction and experimental observation by introducing the concept that surface states of the semiconductor play a role in determining the barrier height. Surface states are energy states (within the bandgap between the valence and conduction bands) at the edge of the semiconductor crystal that arise from incomplete covalent bonds, impurities, and other effects of crystal termination.

Figure 1 shows a cross-section of an un-passivated silicon surface labeled 100. The particular silicon surface shown is an Si(100) 2x1 surface. As shown, the silicon atoms at the surface, such as atom 110, are not fully coordinated and contain un-satisfied dangling bonds, such as dangling bond 120. These dangling bonds may be responsible for surface states that trap electrical charges.

[0007] Bardeen's model assumes that surface states are sufficient to pin the Fermi level in the semiconductor at a point between the valence and conduction bands. If true, the barrier height at a metal-semiconductor junction should be independent of the metal's work function. This condition is rarely observed experimentally, however, and so Bardeen's model (like Schottky's) is best considered as a limiting case.

[0008] For many years, the cause underlying the Fermi level pinning of the semiconductor at a metal-semiconductor junction remained unexplained. Indeed, to this day no one explanation satisfies all experimental observations regarding such junctions. Nevertheless, in 1984, Tersoff proposed a model that goes a long way towards explaining the physics of such junctions. See J. Tersoff, "Schottky Barrier Heights and the Continuum of Gap States," Phys. Rev. Lett. 52 (6), Feb. 6, 1984.

[0009] Tersoff's model (which is built on work by Heine and Flores & Tejedor, and see also Louie, Chelikowsky, and Cohen, "Ionicity and the theory of Schottky barriers," Phys. Rev. B 15, 2154 (1977)) proposes that the Fermi level of a semiconductor at a metal-semiconductor interface is pinned near an effective "gap center", which is related to the bulk semiconductor energy band structure. The pinning is due to so-called metal induced gap states (MIGS), which are energy states in the bandgap of the semiconductor that become populated due to the proximity of the metal. That is, the wave functions of the electrons in the metal do not terminate abruptly at the surface of the metal, but rather decay in proportion to the distance from that surface (i.e., extending inside the semiconductor). To maintain the sum rule on the density of states in the semiconductor, electrons near the surface occupy energy states in the gap derived from the valence band such that the density of states in the valence band is reduced. To maintain charge neutrality, the highest occupied state (which defines the Fermi level of the semiconductor) will then lie at the crossover point from states derived from the valence band to those derived from the conduction band. This crossover occurs at the branch point of the band structure. Although calculations of barrier heights based on Tersoff's model

do not satisfy all experimentally observed barrier heights for all metal-semiconductor junctions, there is generally good agreement for a number of such junctions.

[0010] One final source of surface effects on diode characteristics is inhomogeneity. That is, if factors affecting the barrier height (e.g., density of surface states) vary across the plane of the junction, the resulting properties of the junction are found not to be a linear combination of the properties of the different regions. In summary then, a classic metal-semiconductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, MIGS and inhomogeneities.

[0011] The importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction. Thus, if one were able to control or adjust the barrier height of a metal-semiconductor junction, one could produce electrical devices of desired characteristics. Such barrier height tuning may become even more important as device sizes shrink even further. Before one can tune the barrier height, however, one must depin the Fermi level of the semiconductor. As discussed in detail below, the present inventors have achieved this goal in a device that still permits substantial current flow between the metal and the semiconductor.

SUMMARY OF THE INVENTION

[0012] The present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal – interface layer – semiconductor junction, there exist corresponding minimum specific contact resistances. The interface layer thickness corresponding to this minimum specific contact resistance will vary depending upon the materials used, however, it is a thickness that allows for depinning the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor when the junction is biased (e.g., forward or reverse biased). By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the effect of MIGS has been overcome, or at least reduced, by displacing the semiconductor a sufficient distance from the metal. Minimum specific contact resistances of less than or equal to approximately $10 \Omega - \mu m^2$ or even less than or equal to approximately $1 \Omega - \mu m^2$ may be achieved for such junctions in accordance with the present invention.

[0013] Thus, in one embodiment, the present invention provides an electrical device in which an interface layer is disposed between and in contact with a metal and a silicon-based semiconductor and is configured to depin the Fermi level of the semiconductor while still permitting current flow between the metal and the semiconductor when the electrical device is biased. The specific contact resistance of the electrical device is less than approximately $10 \Omega - \mu m^2$. The interface layer may include a passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and sometimes also includes a separation layer. In some cases, the interface layer may be essentially a monolayer (or several monolayers) of a semiconductor passivating material.

[0014] In another embodiment, the interface layer is made up of a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material, for example ammonia

(NH₃), nitrogen (N₂) or unbound gaseous nitrogen (N) generated from a plasma process. In such cases, the interface layer may be fabricated by heating the semiconductor while in a vacuum chamber and exposing the semiconductor to the nitrogenous material.

[0015] A further embodiment of the present invention provides for depinning the Fermi level of a semiconductor in an electrical junction through the use of an interface layer disposed between a surface of the semiconductor and a conductor. The interface layer preferably (i) is of a thickness sufficient to reduce effects of MIGS in the semiconductor, and (ii) passivates the surface of the semiconductor. Despite the presence of the interface layer, significant current may flow between the conductor and the semiconductor because the thickness of the interface layer may be chosen to provide a minimum (or near minimum) specific contact resistance for the junction. As indicated above, the interface layer may include a passivating material such as a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride.

[0016] Further embodiments of the present invention provide a junction between a semiconductor and a conductor separated from the semiconductor by an interface layer configured to allow a Fermi level of the conductor to (i) align with a conduction band of the semiconductor, (ii) align with a valence band of the semiconductor, or (iii) to be independent of the Fermi level of the semiconductor. In some or all of these cases, current may flow between the conductor and the semiconductor when the junction is biased because the interface layer has a thickness corresponding to a minimum or near minimum specific contact resistance for the junction. For example, specific contact resistances of less than or equal to approximately 2500 $\Omega-\mu m^2$, 1000 $\Omega-\mu m^2$, 100 $\Omega-\mu m^2$, 50 $\Omega-\mu m^2$, 10 $\Omega-\mu m^2$ or even less than or equal to 1 $\Omega-\mu m^2$ may be achieved.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0017] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0018] **Figure 1** shows a cross-section of an un-passivated silicon surface containing surface silicon atoms with dangling bonds.

[0019] **Figure 2** illustrates various energy levels for metals and semiconductors and is labeled to show the work function of a metal and the electron affinity of a semiconductor.

[0020] **Figure 3** shows an energy band diagram for a conventional metal – *n*-type semiconductor junction and also illustrates the concept of a depletion region formed in the semiconductor when the materials are brought into contact with one another.

[0021] **Figure 4** illustrates band bending at a conventional metal – *n*-type semiconductor junction.

[0022] **Figure 5** shows a semiconductor device containing a semiconductor material having a surface across which electrical current flows during operation of the semiconductor device, and containing an interface layer formed on the surface according to one embodiment of the present invention.

[0023] **Figure 6** shows an electrical junction containing an interface layer that is disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

[0024] **Figures 7a, 7b, 7c and 7d** show relationships between Fermi energy, conduction-band energy, and valence-band energy for an unpassivated Schottky diode, a passivated Schottky diode in which MIGS are not removed, an unpassivated Schottky diode in which

MIGS are removed and a passivated Schottky diode in which MIGS are removed according to one embodiment of the present invention, respectively.

[0025] Figure 8 shows a curve of interface layer resistance versus interface layer thickness for an electrical junction containing an interface layer disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0026] Described herein are processes for depinning the Fermi level of a silicon-based semiconductor (e.g., Si, SiC or SiGe) at a metal-semiconductor junction as well as devices that use such a junction. As more fully discussed below, an interface layer is introduced between the semiconductor and the metal. The interface layer functions to passivate the semiconductor surface (that is, terminate dangling bonds that may otherwise be present at the semiconductor surface so as to assure chemical stability of the surface) and to displace the semiconductor from the metal so as to reduce the effect of MIGS.

[0027] As discussed more fully below, the present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal – interface layer – semiconductor junction, there exist corresponding minimum specific contact resistances. Indeed, minimum specific contact resistances of less than or equal to approximately $10 \text{ } \Omega - \mu\text{m}^2$ or even less than or equal to approximately $1 \text{ } \Omega - \mu\text{m}^2$ may be achieved for such junctions in accordance with the present invention. To achieve such low contact resistances, a metal that has a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function that is near the valence band for p-type semiconductors, is selected.

[0028] The Schottky barrier in such junctions is already minimized, meaning that it is much less than the Schottky barrier presented by a junction in which the Fermi level is pinned, generally near the middle of the semiconductor's bandgap. The current versus voltage (IV) characteristic of these junctions is non-linear, generally having a slope that increases as the voltage increases, such that the derivative of current with respect to voltage is increasing with voltage. This results in a decreasing differential resistance (dV/dI) and a decreasing resistance (V/I). Thus, a junction that has high resistance or high differential resistance near the origin of the IV characteristic (zero volts) may have significantly lower resistance or lower differential resistance at higher voltages.

[0029] The present invention achieves low resistance and low differential resistance near the origin of the current-voltage characteristic for a metal – interface layer – semiconductor junction. Generally, the voltage around the origin should be less than about 100 mV, or more preferably less than about 10 mV for purposes of measuring, determining, or utilizing such junctions of low resistance. At higher voltages, the junction resistance will be even lower. It is thus a feature of the present invention to set an upper bound on the resistance of a contact, where the upper bound occurs at low voltages.

[0030] It is further noted that in junctions where the Schottky barrier is minimized as described above, such that the Fermi level at the junction interface at zero volts lies at or near the conduction band edge or valence band edge (for *n*- and *p*-type semiconductors, respectively), the *I/V* characteristic will be nearly symmetric, especially at low voltage. In this case, the term “forward bias” is not defined in the usual sense of a diode wherein forward bias corresponds to the direction of bias for which greater current flows. Thus, in determining or utilizing low resistance junctions of the present invention, the voltage may be either positive or negative.

[0031] It is also possible (in accordance with a further embodiment of the present invention) to make junctions where the Schottky barrier is higher than it would be if the Fermi level at the junction interface were pinned, usually around mid-gap of the semiconductor. Such junctions are formed in the present invention between a metal with a workfunction near or substantially equal to the conduction band edge of a *p*-type semiconductor, or between a metal with a workfunction near or substantially equal to the valence band edge of an *n*-type semiconductor. These junctions are diodes, in that little current will flow if the *n*-type (*p*-type) semiconductor is biased positive (negative) with respect to the metal, and large currents will flow if the voltage is reversed. The low-current flow state is referred to as reverse bias, and the high-current flow state is referred to as positive bias.

[0032] Low resistance in the case of a diode is only relevant in forward bias conditions. In junctions created in accordance with the present invention the resistance contribution of the

interface layer is smaller than the resistance due to the Schottky barrier. That is, in forward bias conditions for junctions created in accordance with the present invention, the transport of charge is limited mainly by the thermal emission of carriers from the semiconductor over the barrier at the interface, and not by the tunneling through the interface dielectric. Thus, low resistance in the case of a diode refers to a resistance lower than the resistance presented by the Schottky barrier.

[0033] In certain applications of diodes, the ability to withstand high reverse biases may be more desirable than high current flow in forward bias. These applications would be considered high voltage/low power applications. In such cases, a low resistance is not essential, and junctions created in accordance with still another embodiment of the present invention provide high-voltage diodes capable of withstanding voltages higher than could otherwise be achieved if the Fermi level of the semiconductor in the junction were pinned.

[0034] The present invention is discussed below in terms of presently preferred embodiments thereof, however, this discussion is not meant to limit the scope of the invention. By studying the present disclosure, others of ordinary skill in the art may recognize equivalent procedures, materials or structures that can be substituted for those described herein to achieve the same effect. The reader is advised and reminded that the use of such equivalents is deemed to be within the scope of the present invention. For example, where the discussion refers to well-known structures and devices, block diagrams are used, in part to demonstrate the broad applicability of the present invention to a wide range of such structures and devices.

1. Introduction and Definitions

[0035] The present discussion makes use of terms that, although well known in the art, may not be familiar to all readers. Therefore, before beginning a detailed discussion of the present invention, it is helpful to define certain terms and concepts. To understand the properties of metal-semiconductor junctions and the impact of the present invention, one must refer to some important energy scales, which are shown graphically in **Figure 2**. The so-called vacuum

level (E_0) represents the minimum energy that an electron needs to possess in order to completely free itself from a metal or semiconductor. For a metal, the Fermi level (E_F) represents the highest occupied energy level for the material. That is, nearly all energy states below the Fermi level are filled, while nearly all states above the Fermi level are empty. The work function of the metal (Φ_M) is then defined as the energy required to free an electron at the Fermi level and mathematically it is the difference between the vacuum level and the Fermi level. The work function is an invariant bulk property of the metal.

[0036] As illustrated in the diagram, semiconductors also have a Fermi level (E_F) and a work function (Φ_S). however, the work function is not an invariant property of the semiconductor. Because the Fermi level varies depending on the doping level in the semiconductor (i.e., the relative amounts of impurities introduced into the semiconductor crystal which change the electron and hole carrier concentrations), a separate parameter, the electron affinity (χ_S), is defined. The electron affinity is an invariant property of the semiconductor and is the difference between the vacuum level and the conduction band edge of the semiconductor. In a semiconductor, almost all energy states are filled in the valence band (E_V) while the conduction band (E_C) is almost empty.

[0037] Now consider a conventional junction between a metal and an n -type semiconductor that has a work function smaller than the work function of the metal (i.e., $\Phi_S < \Phi_M$). An n -type semiconductor is one in which electrons are the majority charge carriers (in p -type semiconductors, holes are the majority charge carrier). As shown in **Figure 3**, because the Fermi level in the semiconductor is higher than the Fermi level in the metal, electrons transfer from the semiconductor 310 to the metal 320 when the materials are brought into contact. Thus, a depletion region (i.e., a region in which there are no free charge carriers) 330 forms near the junction interface 340.

[0038] The formation of the depletion region gives rise to an electric field and so-called "band bending", as one approaches the junction interface from the semiconductor side (see **Figure 4**). The band bending creates an energy barrier (discussed above) that blocks further

transfer of electrons into or out of the semiconductor. Similar barriers are formed for a junction between a metal and a *p*-type semiconductor when the work function of the metal is less than the work function of the semiconductor. However, in the case of a metal-*n*-type semiconductor junction in which the work function of the semiconductor is greater than that of the metal or a metal-*p*-type semiconductor junction in which the work function of the semiconductor is less than that of the metal, no such energy barriers are created and the contact is said to be ohmic in nature.

[0039] As discussed above, although Schottky first postulated that the height of the energy barrier (Φ_b) formed at a metal-semiconductor junction was simply the difference between the work function of the metal and the electron affinity of the semiconductor, experiments have not verified this relationship. Instead a more complex explanation that takes into account the effects of surface defect states, inhomogeneities and MIGS appears to provide more accurate estimates of barrier heights by explaining the pinning of the Fermi level in the semiconductor. The present inventors have created a technique which is believed to depin the Fermi level of a Si-based semiconductor at a junction with a metal (and thus allow for control or tuning of the barrier height) by both passivating the semiconductor surface (to eliminate or at least reduce the effects of surface states and possibly inhomogeneities) and displacing the metal from the semiconductor (to eliminate or at least reduce the effects of MIGS). This depinning is achieved by introducing an interface layer between the semiconductor and the metal to create a semiconductor -- interface layer -- metal junction, which still permits significant current to flow between the metal and the semiconductor when the junction is forward biased.

[0040] This latter point is important. As discussed further below, for contacts where the energy bands of the semiconductor and the conductor align (i.e., where the Fermi level of the conductor aligns with the conduction or valence band of the semiconductor depending on semiconductor type and/or contact application), if the interface layer is too thin, the specific contact resistance of the junction increases because of the presence of MIGS, resulting in an increased barrier height; thus, current flow is hampered. Conversely, if the interface layer is

too thick, the specific contact resistance is again increased and one gets low current across the junction because of tunneling limitations. The present invention achieves an interface layer that is thick enough to reduce or eliminate the effect of MIGS, while still thin enough to permit significant current flow.

II. Passivation of Semiconductor Surfaces

[0041] A common processing operation performed during semiconductor device fabrication is silicon surface passivation. Surface passivation (whether by an oxide or another material) chemically neutralizes and physically protects the underlying silicon. For example, exposing a silicon surface to oxygen (under the appropriate conditions to grow a protective film of silicon dioxide) will allow the oxygen to react with the dangling bonds of the silicon surface to form covalent bonds that satisfy the surface silicon atoms' valency and render the surface fully coordinated. These covalent bonds provide chemical stability to the silicon surface. The covalent bonds also tie up unbound charges that exist on the silicon surface as a result of the discontinuation of the semiconductor crystal at the surface.

[0042] However, passivation with silicon dioxide has several significant disadvantages. For example, silicon dioxide is a dielectric insulator that poses a significant barrier to the flow of current. Accordingly, a layer of silicon dioxide deposited or grown on a silicon surface may significantly reduce the ability for electrical current to flow through that surface. As a result, the use of silicon dioxide has been limited in practicality to surfaces external to the active region of semiconductor devices through which current passes during device operation (e.g., as a gate oxide layer). This disadvantage is compounded by the fact that the silicon dioxide grows very rapidly and readily on the silicon surface so that it is difficult to limit the growth to a thin layer. Silicon dioxide is also a poor diffusion barrier to semiconductor dopants such as boron.

[0043] Instead of making use of silicon dioxide then, in one embodiment the present inventors utilize a nitrided semiconductor surface to provide chemical passivation. That is, a

nitride layer is introduced to passivate the semiconductor surface by eliminating or at least reducing the effects of surface states and possibly inhomogeneities. The nitride layer also displaces the metal from the semiconductor and eliminates or at least reduces the effects of MIGS. The result of introducing the nitride layer as an interface between the semiconductor and the metal is a depinning of the Fermi level of the semiconductor. When the Fermi level of the semiconductor is depinned, the Fermi level of the metal at the interface will be that of the bulk metal, and will not be dependent upon the interface. In addition to the above, the present inventors propose techniques for providing non-insulating, passivated semiconductor surfaces using materials other than nitrogen: for example, oxides, hydrides, arsenides and/or fluorides.

[0044] These developments have wide applicability in connection with the fabrication of Schottky diodes, Schottky-barrier transistors and other electrical components. For example, in Schottky diodes, the ability to control the energy barrier height at the diode junction is important if the device is to be tailored to specific applications. Use of the present techniques allows for tuning of the barrier height. Further, for other three-terminal devices with Schottky-barrier-isolated channels, control of device characteristics is made possible through the present invention by allowing *n*- and *p*-type devices to be fabricated without dopants, relying instead on the use of metals with different work functions.

[0045] Figure 5 shows a semiconductor device 510 that contains a semiconductor 530 and an interface layer 520 formed on a surface 540 of the semiconductor in accordance with the present invention. The terms semiconductor device, microelectronic device, monolithic device, chip, and integrated circuit are often used interchangeably in this field. Any or all such devices may each contain an interface layer formed on a semiconductor surface in accordance with the present invention.

[0046] The semiconductor 530 contains a semiconductor material. The term semiconductor material refers to a material having a bandgap that is greater than about 0.1 eV and less than about 4 eV. The term bandgap refers to an energy gap of forbidden energy levels separating the conduction band, which is an upper energy band that is mostly devoid of electrons and

wherein electrons can conduct, and the valence band, which is an energy band that is mostly filled with electrons and wherein electrons cannot conduct. The semiconductor material may have a wide range of doping levels including no doping at all.

[0047] The semiconductor 530 has a surface 540 that is passivated by the interface layer 520. In this context (and as used elsewhere herein) the term passivation means the elimination or at least the reduction of the effects of surface states due to defects or dangling bonds of the semiconductor surface 540. Note that passivation does not, as a practical matter, require that all surface states be eliminated. Rather, it is the effect of surface states on the device properties that is limited or eliminated in passivation. Note further that the presence of MIGS may be regarded as a surface state, however, as used herein the term passivation is not meant to infer the elimination of MIGS (though in some cases, a passivation layer may have sufficient thickness to provide a separation layer between the semiconductor and the metal sufficient to reduce or eliminate MIGS). The semiconductor 530 is operable to be electrically coupled with a first voltage associated with the semiconductor device 510 and to conduct electrical current 550 across the passivated surface 540.

[0048] The interface layer 520 is formed on the semiconductor 530 and may contain a passivation material that bonds to the semiconductor material by way of a covalent (or other) bond formed between the passivation material and the semiconductor material. For example, an atom of passivation material may covalently bond with a dangling bond of a surface silicon atom to fully coordinate the silicon atom and thereby help passivate the silicon atom. In some cases, the passivation material may be the sole component of the interface layer 520, while in other cases the interface layer 520 may be a compound layer that includes both a passivation layer and a separation layer. That is, the interface layer serves to (i) chemically passivate the semiconductor surface 540, and (ii) displace the semiconductor from the metal sufficiently to eliminate or at least reduce the effect of MIGS. As explained below, this may necessitate including a separation layer in addition to a passivation layer within the interface layer, depending on the passivation material selected. Of course, the combination of the passivation

layer and the separation layer must be sufficiently thin to permit the low specific contact resistances described herein.

[0049] Different passivation materials are contemplated. According to one embodiment, the interface layer 520 is formed using a material that is preferably selected from the group consisting of hydrogen (H), oxygen (O), nitrogen (N), arsenic (As), and fluorine (F) (that is, the interface layer 520 may include a nitride, an oxide, a hydride, an arsenide and/or a fluoride). Other materials having chemical characteristics or valences similar to these materials may also be used. Note that distinct separation layers (i.e., in addition to the passivation layer(s)) may be needed where H, As, or F passivation layers are used, as these tend to form monolayer coverage, rather than a layer of a compound with Si of process-dependent thickness. In contrast, passivation layers made using N and/or O may not require distinct separation layers, as these elements may form a layer of a compound of Si with a thickness that can be varied depending on processing.

[0050] Different amounts of passivation material are contemplated to be useful for different embodiments of the present invention. Often, the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm. For example, depending upon the particular implementation, the thickness may be less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, may be the thickness corresponding to a single layer or monolayer of passivation material that is bonded to the semiconductor surface, or may even be the number of atoms of passivation material required to passivate substantially all the dangling bonds associated with the semiconductor surface 540.

[0051] In some cases, passivation of the semiconductor surface 540 will include removing (or terminating) dangling bonds located proximate to the surface of the semiconductor material, including those at the surface as well as those within a few molecular dimensions from the surface. This process may stabilize the surface of the semiconductor material and may improve the controllability of subsequent fabrication operations. Passivation may also reduce the density of surface states that may exist at the semiconductor surface as a result of the

discontinuation of the semiconductor crystal at the surface. This may improve consistency and performance of the semiconductor device, inasmuch as such states are known to interfere with proper device operation. For example, they may provide surface charge states that result in a pinning of the Fermi level.

III. Forming Interface Layers

[0052] Exemplary methods for forming interface layers to provide (i) passivation of semiconductor surfaces, and (ii) displacement of the semiconductor from the metal to eliminate or at least reduce of the effects of MIGS within the semiconductor when in the presence of the metal (collectively referred to herein as depinning the Fermi level of the semiconductor) with hydrogen, fluorine or nitrogen are presented below to further illustrate the concepts of the present invention. Other passivation materials may include arsenic, oxygen or an oxynitride, and in some cases such passivation layers are combined with separation layers (e.g., made of an oxide) to complete the interface layer.

A. Hydrogen And Fluorine

[0053] An interface layer may contain hydrogen, fluorine, or both hydrogen and fluorine (e.g., in the form of a hydride and/or a fluoride). One method for forming an interface layer on a semiconductor surface with hydrogen and fluorine includes cleaning the semiconductor substrate with a cleaning solution, immersing the cleaned substrate in a hydrogen fluoride solution (or other liquid containing hydrogen and fluorine ions) having an effective concentration typically between about 1%-50% by weight, waiting an effective period of time, typically between about several seconds and about 5 minutes, removing the substrate from the hydrogen fluoride solution, optionally rinsing the substrate in deionized water, and blow-drying the substrate with nitrogen. Such a method may form an interface layer containing hydrogen and fluorine that are bonded (e.g., covalently) to the semiconductor surface.

[0054] It should be noted that long rinses in deionized water, generally longer than about 30 seconds, might remove the hydrogen passivation. Thus, deionized water rinses might advantageously be kept to less than about 30 seconds to maintain the hydrogen passivation of the surface. Also, the higher the concentration of the hydrogen fluoride during the immersion, the greater the concentration of fluorine passivation. Finally, methods are also contemplated where the ratio of hydrogen to fluorine passivation is altered by removing either the hydrogen or the fluorine.

[0055] An interface layer formed in this fashion may be best suited for applications where a subsequent metal layer is deposited over the interface layer in a generally non-invasive fashion, for example using a thermally evaporated source. Experiments by the present inventors to date suggest that using other approaches (e.g., plasma deposition) may cause damage to the thin (e.g., monolayer thick) interface layer contemplated as part of the present invention.

B. Nitrogen

[0056] In a further embodiment, an interface layer may contain nitrogen (e.g., in the form of silicon nitride). One method for forming an interface over a semiconductor surface with nitrogen includes heating a substrate containing the semiconductor surface in the presence of a nitrogenous material (that is, a gas or other material containing nitrogen). For example, a substrate containing an exposed silicon surface may be annealed at a temperature between about 300°C and about 750°C, which is lower than temperatures conventionally used for Rapid Thermal Nitridation (RTN), under a gaseous ambient having, for example, ammonia (NH₃) at some effective partial pressure. By exposed, we mean a clean surface, free of everything except silicon. Such a method may form an interface layer containing nitrogen, often in the form of a nitride, bonded to the semiconductor surface. Note that the present inventors have observed indications suggesting that in these low temperature conditions interface layer growth is self-limiting, depending only on temperature.

[0057] According to another embodiment, an interface layer that includes nitrogen may be formed on an exposed surface of a semiconductor material by a method that includes heating a semiconductor material to a substantially high temperature under vacuum and exposing the semiconductor material to a substantially small amount of a nitrogenous material, such as ammonia. The method may include placing a semiconductor having an exposed semiconductor surface in a heating chamber, pulling a vacuum of less than about one millionth of a Torr, or more favorably an ultra high vacuum of less than 10^{-9} Torr, and then heating the semiconductor in the heating chamber to a substantially high temperature. The higher the vacuum, the longer the substrate may be heated without growth of an oxide from residual oxygen or water in the chamber. Thus, the process may include heating the semiconductor to a temperature that is between about 900°C and about 1000°C, or higher, in an inert ambient. As desired, the semiconductor may be exposed to hydrogen gas, or an equivalent, to reduce any native oxide on the semiconductor. These high temperatures may provide for greater passivation of the semiconductor surface as compared with results that may be achieved at lower temperatures.

[0058] Then, the heated semiconductor may be exposed to a substantially small amount of a nitrogenous material, such as ammonia. This may include exposing the semiconductor surface to ammonia for a substantially short period of time. For example, the surface may be subjected to a burst or pulse of ammonia lasting for a time period between about 0.5 seconds and about 5 seconds. Alternatively, the surface may be exposed to a controlled, small amount of ammonia over an arbitrarily longer period of time. In this way, the substantially small amount of ammonia will react with the surface to form a nitrogenous interface layer, such as a nitride layer, thereon and then further growth of the interface layer will cease. Then the semiconductor may be cooled from the substantially high temperature to ambient temperature and removed from the heating chamber. Further annealing of the substrate and the grown nitride layer may also be performed in the vacuum chamber before removal, at a substantially elevated temperature between about 700°C and 1000°C, or higher.

[0059] Advantageously, it has been unexpectedly observed that a process such as that described above and incorporating substantially high temperature exposure for substantially short periods may be used to controllably form thin yet effective interface layers. That is, the present inventors have observed that in the creation of thin interface layers that include nitrogenous materials, temperature appears to be a dominant factor in controlling thickness. For example, by such methods effective interface layers may be formed having a thickness that is less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the semiconductor surface.

[0060] Further, thin interface layers may be advantageously grown on a semiconductor in the presence of nitrogen gas, or other inert nitrogen-containing gas. The reaction rate of a semiconductor such as silicon with nitrogen gas is significantly lower than that of a reactive nitrogen-containing gas such as ammonia. The slow growth rate may be desirable for better control of the growth of films of nitrogen on a semiconductor of a thickness of less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the silicon surface.

IV. Diodes Containing Passivated Semiconductor Surfaces

[0061] Diodes made from Schottky barriers (i.e., asymmetric electrical potentials formed at a junction between a metal and a semiconductor) are widely used in rectifiers in power supply and control applications. As used herein, the terms Schottky diode, metal-semiconductor junction diode, diode, and rectifier are all related and appear in order from more specific at the left to more general at the right. Likewise, the terms Schottky barrier, metal-semiconductor barrier, conductor-semiconductor junction, and multi-material junction are all related and appear in order from more specific at the left to more general at the right. The term Schottky diode will be used to refer to a diode containing a Schottky barrier.

[0062] As mentioned above, the present inventors have devised a scheme to control or adjust a Schottky barrier height by forming an interface layer (which includes or sometimes consists of a passivation layer that includes an oxide, oxynitride, nitride, arsenide, hydride, fluoride, or an equivalent) between a metal and a semiconductor. This scheme differs from past attempts by others to control barrier height, which attempts generally involved either using a silicide as a contact metal (and thus limiting the choices of available contact metals to those that can form silicides), or using esoteric substrates that exhibit wide bandgaps. Further, in previous devices the Fermi level of the semiconductor remains pinned, with the barrier height being virtually independent of the metal used. Finally, doping of substrates has also been attempted, however, it has not been shown to truly affect the barrier height of the substrate material. For example, PtSi contacts have reduced resistance due to high silicon doping such that the current across the junction is dominated by tunneling through the barrier. Doping may thus lead to cases where the top of the barrier may be so thin as to be essentially transparent to electrons, however, doping does not appear to allow actual tuning of the barrier height.

[0063] Figure 6 shows an example of a diode 600 containing, according to one embodiment of the present invention, an interface layer 620 disposed between and attached to both a semiconductor 610 and a conductor 630. The conductor and the semiconductor are operable to be electrically coupled with different voltages associated with the operation of the diode 600 and to pass electrical current through a passivated semiconductor surface formed at the junction between the semiconductor 610 and the interface layer 620.

[0064] The conductor 630 contains a conductive material such as a metal or an alloy of a metal. The terms metal, conductive material, and conductor are all related and appear in order from specific at the left to general at the right. In general, the terms refer to a highly electrically conductive substance that has a Fermi energy level that sits in a partially filled band. Unless otherwise specified, conductors include metals (e.g., pure metals and alloys), and other conductors such as doped polysilicon (a nonporous silicon containing randomly oriented crystallites), doped single crystal silicon, and metal silicides. Note that alloys may

have workfunctions different than their constituents and may be designed to have specific workfunctions though selective use of ratios of the constituent metals.

[0065] Often, the conductor is a metal since metals may offer advantages over conductive semiconductors including lower resistance, higher carrier mobilities that provide superior high frequency performance and switching, favorable low power characteristics, and ease of manufacturing control. Use of metals may also avoid the need to perform semiconductor doping, which may simplify manufacturing and improve quality control.

[0066] Metals that are contemplated include pure metals, alloys, refractory metals, metals that do not form silicides, metals physically deposited by substantially non-invasive processes such as by condensation of a thermally evaporated metal vapor, and metals having a predetermined work function. The use of non-invasively deposited metals may allow for forming the metal on a thin interface layer without disrupting the passivation properties of the layer.

[0067] A metal having a predetermined work function may be a metal having a work function smaller or greater than that of the semiconductor, depending on the desired application. Often, the semiconductor will be silicon. In this case by the work function of a semiconductor or silicon we mean the energy in the middle of the semiconductor bandgap. Exemplary metals that have a work function smaller than silicon include Group 3A elements, aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum (Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn). Exemplary metals that have a work function greater than silicon include platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Co), and palladium (Pd).

[0068] The semiconductor-interface layer-conductor configuration illustrated in **Figure 6** defines what the present inventors have chosen to call a "passivated Schottky barrier". The passivated Schottky barrier is a naturally formed electrical potential barrier to an electron or hole at the Fermi energy (the electrochemical potential) in the conductor due to a depletion

region formed in the semiconductor adjacent the conductor. The passivated Schottky barrier may deviate in barrier height from a standard un-passivated Schottky barrier that would form naturally at a contact junction between the semiconductor and the conductor without the interface layer disposed therebetween. That is, the passivated Schottky barrier may have a barrier height that depends predominantly upon the bulk characteristics of the semiconductor and the conductor, rather than on surface properties, and may depend in part on the characteristics of the interface layer.

[0069] Indeed, the present inventors have determined that changes in barrier height are approximately monotonic and continuous for variations in surface passivation thickness by nitridation of the semiconductor substrate. More specifically, experiments by the present inventors in a regime where the nitride layer is sufficiently thick to remove MIGS show that temperature of interface layer formation has the strongest effect on barrier height. In other regimes, thickness may be critical. Ideally, if all surface states are removed, barrier height should be controllable simply by the choice of metal used.

[0070] To understand why thickness of the interface layer is important, refer briefly to **Figure 8** where a graph of interface-specific contact resistance versus interface thickness is shown. The graph is for a structure where the workfunction of the metal is the same as the electron affinity in the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the semiconductor. At large thicknesses, the interface layer poses significant resistance to current. As thickness decreases, resistance falls due to increased tunneling current. However, there comes a point where even as the interface layer continues to get thinner, resistance increases. This is due to the effect of MIGS, which increasingly pull the Fermi level of the metal down towards mid-gap of the semiconductor, creating a Schottky barrier. The present inventors have discovered that this competition results in an optimum thickness, as shown in the illustration, where the resistance is a minimum. At this thickness the effect of MIGS has been sufficiently reduced to depin the metal and lower the Schottky barrier, and the layer is still sufficiently thin to allow significant current flow across the

interface layer. Contact resistances of less than or equal to approximately $2500 \text{ } \Omega\text{-}\mu\text{m}^2$, $1000 \text{ } \Omega\text{-}\mu\text{m}^2$, $100 \text{ } \Omega\text{-}\mu\text{m}^2$, $50 \text{ } \Omega\text{-}\mu\text{m}^2$, $10 \text{ } \Omega\text{-}\mu\text{m}^2$ or even less than or equal to $1 \text{ } \Omega\text{-}\mu\text{m}^2$ may be achieved.

[0071] Characteristics that may be adjusted to provide a desired barrier height thus include the passivation material used (e.g., selection based on bandgap), the interface layer thickness (e.g., especially where the interface layer is a compound layer formed of a passivation layer and a separation layer), the method of forming the interface layer (e.g., control of parameters such as temperature), the interface layer thickness that is substantially similar to a penetration depth of MIGS formed at a metal interface, the metal used for the source and/or drain, and other characteristics.

[0072] One advantage of the ability to adjust the Schottky barrier height with the introduction of interface layer 620 is the ability to form a substantially high barrier height. For example, an interface layer may be used to create a Schottky barrier having a barrier height that is greater than can be achieved through the use of metal silicides, greater than about 2.0 eV, or greater than about 2.5 eV (using a semiconductor with a bandgap at least this large), or nearly 1.0 V using silicon. Such high barrier heights imply the ability to withstand high voltages before breakdown occurs. Thus, Schottky barriers having such high barrier heights may be particularly useful in high-voltage Schottky diodes.

[0073] Another advantage achieved through the use of the interface layer 620 is greater flexibility afforded in selecting a conductor 630. Typically, metals chosen for application in classic Schottky diodes are those that can form a silicide with a silicon semiconductor. The formation of the silicide helps to reduce surface states (resulting from dangling bonds), but not the effects of MIGS. Thus, the Fermi level at the semiconductor surface is still pinned. Using metals that form silicides upon contact with silicon may thus help to make the devices more reproducible in a manufacturing environment, but such devices still suffer from the drawback of having a barrier height that is fixed.

[0074] According to one embodiment of the present invention, however, one may select a conductor that is not able (or not readily able) to form a silicide with the semiconductor. The metal silicide is not needed because the interface layer provided in accordance with the present invention passivates the semiconductor surface and also reduces or eliminates the effect of MIGS. This may allow for selection of a metal that has properties such as a desirable work function or Fermi level energy, even though that metal may not form a metal silicide.

[0075] For example, to make large-barrier diodes, for an *n*-type doped silicon semiconductor, a metal may be selected that has a work function that is either substantially equal to the valence band energy of the semiconductor or that is within about 0.1 eV to about 0.3 eV of the valence band energy of the semiconductor. Similarly, for a *p*-type doped silicon semiconductor, a metal may be selected that has a work function substantially equal to the conduction band energy of the semiconductor. For Schottky diodes configured in accordance with the present invention, the Fermi level of the metal may lie anywhere in the bandgap of the semiconductor when an interface layer is disposed within the junction, resulting in diodes of various barrier heights. The Fermi level of the metal may also lie in the conduction or valence band of the semiconductor.

[0076] The use of interface layer 620 thus provides a way to tune, adjust, or control the height of the barrier between the conductor and the semiconductor. Without the interface layer 620, the barrier height would be substantially un-tunable, un-adjustable, and fixed (as discussed above).

[0077] The role played by interface layer 620 in tuning, adjusting, or controlling the height of the barrier between the conductor 630 and the semiconductor 610 may be understood as a depinning of the Fermi level of the semiconductor. That is, the interface layer may reduce surface states by bonding to the semiconductor material to consume dangling bonds. Additionally, the interface layer may reduce the formation of MIGS in the semiconductor by providing a thickness and bandgap that prevent the electron wave function (of the metal) from penetrating into the semiconductor. The electron wave function may instead penetrate into the

interface layer and form MIGS within the interface layer at an energy related to the states of the interface layer material. As desired, the density of the MIGS and the depth of MIGS penetration into the interface layer may be reduced by choosing an interface layer material or materials having a larger bandgap or higher effective mass than the semiconductor.

[0078] According to one embodiment of the present invention then, the interface layer 620 is incorporated into a device operable to pass current through the semiconductor surface and the interface layer during device operation. In such an embodiment, it may be desirable to use an interface layer having a thickness of a monolayer, or, for example between about 0.1 nm and about 0.3 nm, and also having a wide bandgap (as compared to that of the semiconductor) so that the interface layer both de-pins the Fermi level (so that the barrier height depends predominantly on bulk properties of the junction materials) and allows sufficient current transfer across it. Advantageously, such interface layers may be sufficiently thin to provide low impedance to current flow (due to the exponential dependence of direct tunneling on barrier thickness), which is desirable for many semiconductor devices, while also providing sufficient semiconductor surface passivation to allow an adjustable barrier height. That is, the interface layer may allow passivation of surface states and reduction (or elimination) of MIGS in the semiconductor to allow for an adjustable barrier height with a substantially thin layer that allows sufficient current to be transferred across the interface layer.

[0079] There are several methods by which the barrier height can be made adjustable. For example, adjustment may be made by tuning the degree of Fermi level pinning. In other words, some embodiments may allow for a sufficiently thin interface layer so that not all of the effects of MIGS in the Si are eliminated. Further, the pinning may be varied by combinations of thickness of the interface layer and the choice of interface material. The metal in contact with the interface layer may be pinned by MIGS at different levels in different materials. Conversely, or in addition, the passivation may be left incomplete to allow for an effective level of unpassivated states. Complete depinning of the Fermi level (that is removal of all surface states in Si including MIGS) is another option, in which case one could tune the

barrier height simply by choosing a pure metal or an alloy that possesses the desired workfunction. In that case, the barrier height is determined by Equation (1), which until now has been an unrealizable idealization. Note that the type of tuning being discussed here is adjustment of the barrier height by altering the structure of the junction at the time of manufacture, not by varying an externally applied condition during junction operation.

[0080] Figure 7a – 7d show relationships between Fermi energy, conduction band energy, and valence band energy for various Schottky barriers containing a metal in contact with (or in close proximity to) a semiconductor, where the bandgap (E_g) of the semiconductor exists between the conduction band (E_c) and the valence band (E_v). In this example, the work function of the metal Φ_M is chosen to be approximately equal to the electron affinity χ_s of the semiconductor. In Figure 7a, an unpassivated Schottky barrier 700 is shown. In this example, the Fermi level (E_F) of the metal 730 is pinned in the bandgap of the semiconductor 710. This results in a discontinuity in the vacuum level caused by a charged dipole at the interface.

[0081] In Figure 7b, the interface layer 720b is thick enough to passivate dangling bonds at the surface of the semiconductor 710, but not thick enough to eliminate or sufficiently reduce the effect of MIGS. As a result, the band structure is largely unaltered from that seen in the previous illustration. Similarly, in Figure 7c, when the interface layer 720c is sufficiently thick to eliminate or reduce the effect of MIGS but not to passivate the semiconductor surface, little change in the energy band structure is observed. However, as shown in Figure 7d, when the interface layer 720d is sufficient to both eliminate or reduce the effect of MIGS and to passivate the semiconductor surface, we see the Fermi level of the metal aligning with the conduction band of the semiconductor (i.e., the Fermi level of the semiconductor has been depinned and no longer lines up with the Fermi level of the metal). The vacuum level is now continuous as there is no charged dipole at the interface. Thus, the band structure of a device constructed in this fashion is a result of only bulk material properties, not properties of the surface. By way of example, the materials in such cases may be Al and Si, with a work

function for Al of approximately $\Phi_M = 4.1$ eV and the electron affinity for Si of approximately $\chi_S = 4.05$ eV.

V. Transistors Containing Passivated Semiconductor Surfaces

[0082] The interface layers described herein may be used in connection with a semiconductor surface of a channel in a field effect transistor. That is, an interface layer may be disposed between a source and a channel, a channel and a drain, or both of an insulated gate field effect transistor. Such use of an interface layer is described in detail in U.S. Patent No.: 6,833,556, issued December 21, 2004, entitled "INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL," filed January 14, 2003, by the present inventors, and assigned to the assignee of the present invention.

[0083] The source and drain contacts at the channel of a field effect transistor are examples of a broader category of metal-interface layer-semiconductor contacts that make up the present invention. In the past, such contacts generally comprised a silicide-n⁺-Si junction, which formed a somewhat "leaky" Schottky diode, with a Fermi level of the semiconductor pinned at the midgap. In contrast, the present invention provides a contact wherein the Fermi level of the metal is aligned with the conduction band of the semiconductor (e.g., as shown in Figure 7d). Note that in other cases, depending on the type of semiconductor material and conductors used, the Fermi level of the metal may align with the valence band of the semiconductor.

[0084] Although both types of junctions (i.e., the new passivated Schottky barrier junction and the conventional silicide-semiconductor junction) permit tunneling currents, the present junction can be fabricated with a much thinner interface layer as compared to the thickness of the silicide layer used previously. Indeed, thickness of an order of magnitude less than the silicide thickness can be expected. In a conventional silicide – semiconductor junction a Schottky barrier is formed which is comprised of a depletion layer. The tunnel barrier presented by such a depletion layer may be an order of magnitude thicker than the dielectric tunnel barrier in the present invention. The thinner interface layers provided by the present

invention permit higher current across the junction (i.e., lower junction specific contact resistance).

[0085] Two other properties of the dielectric deserve mention. First is the property of the height of the barrier compared to the semiconductor conduction band (for electrons). In making the barrier thinner than a silicide barrier, the tradeoff may be a higher tunnel barrier (e.g., 2 eV for nitride, compared with about half the gap of 0.6 eV for silicide). Spacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV). Nevertheless, even with the higher barrier to electrons, the present inventors have determined that the resistance can still be one hundred times lower than a contact to silicon with a silicide barrier.

[0086] The second property is the effective mass of electrons in the dielectric. Larger mass electrons will not penetrate as far (i.e., because of their shorter wavelength) from the metal into the semiconductor. The less the electrons penetrate into the dielectric, the less the effect of MIGS in the dielectric. Thus, MIGS in the dielectric are reduced with larger bandgap and larger effective mass.

[0087] In addition the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility). The high doping profiles were required in the past in order to keep the junction depletion layer relatively thin, so as to increase the tunneling current, thus reducing the junction resistance. However, it is becoming increasingly difficult to increase doping profiles in order to provide low resistance junctions. It may be possible to reach the same level of resistance with a lower doping concentration using the present invention. It may further be possible to achieve much lower resistance even with lower doping concentration. When the present invention is used with high doping levels, the resistance will be further reduced.

[0088] Thus, methods and applications for semiconductor-interface layer-metal junctions have been described. Although described with reference to specific embodiments it should be

remembered that various modifications and changes may be made to the techniques described herein without departing from the broader spirit and scope of the invention. The specification and drawings are accordingly to be regarded in an illustrative rather than a restrictive sense and the invention measured only in terms of the claims, which follow.

CLAIMS

What is claimed is:

1. A method, comprising cleaning a semiconductor substrate with a cleaning solution to form a cleaned substrate; immersing, for a period of time between several seconds and approximately five (5) minutes, the cleaned substrate in a solution containing hydrogen and fluorine ions of between approximately 1%-50% by weight; removing the substrate from the solution and blow-drying the substrate with nitrogen, thereby forming an interface layer containing hydrogen and fluorine on the semiconductor substrate, said interface layer being of sufficient thickness to passivate a surface of said semiconductor substrate in a vicinity of said interface layer; subsequently depositing a metal layer over the interface layer, thereby forming a junction having a metal layer disposed over the interface layer disposed over the semiconductor, said junction having a specific contact resistance of less than or equal to approximately $1000 \Omega\text{-}\mu\text{m}^2$.
2. The method of claim 1, wherein following removal of the substrate from the solution and prior to blow-drying the substrate with nitrogen, rinsing the substrate in deionized water for less than 30 sec.
3. An electrical device, comprising a metal; a semiconductor; and an interface layer of less than 1 nm thickness disposed between and in contact with both the metal and the semiconductor, said interface layer configured to adjust a Schottky barrier height of the device, wherein the electrical device has a specific contact resistance of less than or equal to approximately $1000 \Omega\text{-}\mu\text{m}^2$.
4. The electrical device of claim 3, wherein the interface layer includes a passivating material.

5. The electrical device of claim 4, wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide.
6. The electrical device of claim 4, wherein the interface layer consists essentially of a monolayer of the passivating material.
7. The electrical device of claim 3, wherein the interface layer includes a separation layer and a passivating layer.
8. The electrical device of claim 7, wherein either or both of the passivating layer and the separation layer comprise a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide.
9. The electrical device of claim 3, wherein the metal comprises an alloy of a metal.
10. The electrical device of claim 9, wherein the interface layer includes a passivating material.
11. The electrical device of claim 10, wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide.
12. The electrical device of claim 10, wherein the interface layer consists essentially of a monolayer of the passivating material.
13. The electrical device of claim 9, wherein the interface layer includes a separation layer and a passivating layer.
14. The electrical device of claim 13, wherein either or both of the passivating layer and the separation layer comprise a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide.

15. The electrical device of claim 3, wherein the interface layer comprises a metal oxide.
16. The electrical device of claim 4, wherein the interface layer includes a metal oxide.
17. The electrical device of claim 13, wherein at least one of the passivating layer and the separation layer is a metal oxide.
18. The electrical device of claim 3, wherein the interface layer is configured to adjust the Schottky barrier height by reducing or eliminating metal induced gap states (MIGS).
19. The electrical device of claim 3, wherein the interface layer is configured to adjust the Schottky barrier height by reducing interface charge.
20. The electrical device of either one of claims 18 or 19, wherein the interface layer includes a passivating material.
21. The electrical device of either one of claims 18 or 19 wherein the interface layer comprises one or more of a metal oxide, a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide.
22. The electrical device of either one of claims 18 or 19, wherein the interface layer includes a separation layer and a passivating layer.
23. The electrical device of either one of claims 18 or 19, wherein the metal comprises an alloy of a metal.
24. The electrical device of either one of claims 18 or 19, wherein the interface layer includes a separation component and a passivation component, either or both of which

comprise a metal oxide, a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide.

25. A method, comprising adjusting a Schottky barrier height of a metal-semiconductor interface in an electrical device by introducing, during fabrication of the electrical device, an interface layer of less than 1 nm thickness between and in contact with both a metal and a semiconductor to form a metal-interface layer-semiconductor junction.

26. The method of claim 25, wherein the interface layer is configured to affect electrical dipoles between the metal and the semiconductor and thereby adjust the Schottky barrier height.

27. The method of claim 25, wherein the interface layer is introduced by deposition during fabrication of the electrical device.

28. The method of claim 25, wherein the interface layer includes a separation component and a passivating component.

29. The electrical device of claim 28, wherein either or both of the passivating component and the separation component comprise a metal oxide, a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide.

30. The method of claim 25, wherein the interface layer passivates and/or reduces the effect of metal induced gap states (MIGS).

31. A method, comprising forming, adjacent and in contact with a semiconductor channel surface, an interface layer of less than 1 nm thickness, and subsequently depositing a metal source/drain adjacent and in contact with the interface layer, wherein said metal is deposited in a noninvasive fashion so as not to disrupt passivation properties of the interface layer and said interface layer is configured to

adjust a Schottky barrier height of a metal-semiconductor interface which would exist if the interface layer were not present.

ABSTRACT

[0089] An electrical device in which an interface layer is disposed between and in contact with a metal and a Si-based semiconductor, the interface layer being of a thickness effective to depin of the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor. The interface layer may include a layer of a passivating material (e.g., made from nitrogen, oxygen, oxynitride, arsenic, hydrogen and/or fluorine) and sometimes also includes a separation layer. In some cases, the interface layer may be a monolayer of a semiconductor passivating material. The interface layer thickness corresponds to a minimum specific contact resistance of less than or equal to $10 \Omega\text{-}\mu\text{m}^2$ or even less than or equal to $1 \Omega\text{-}\mu\text{m}^2$ for the electrical device.

Electronic Acknowledgement Receipt

EFS ID:	9393470
Application Number:	13022522
International Application Number:	
Confirmation Number:	6852
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
Adjustment date: 02/22/2011 MNGUYEN 02/08/2011 INTEFSW 00006007 13022522 04 FC:2202 -546.00 DP 02/22/2011 MNGUYEN 00000013 13022522 01 FC:2201 110.00 DP 02 FC:2202 416.00 DP 03 FC:9998 20.00 DP	
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	26263
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-453
Receipt Date:	07-FEB-2011
Filing Date:	
Time Stamp:	19:44:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1203
RAM confirmation Number	6007
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
-----------------	----------------------	-----------	----------------------------------	------------------	------------------



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/022,522	02/07/2011	Daniel E. Grupp	40003771-0003-453

CONFIRMATION NO. 6852

FORMALITIES LETTER



OC000000046155958

26263
SNR DENTON US LLP
P.O. BOX 061080
CHICAGO, IL 60606-1080

Date Mailed: 02/24/2011

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given TWO MONTHS from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
 - Numbers, letters, and reference characters on the drawings must measure at least 0.32 cm (1/8 inch) in height. See Figure(s) 6-7d.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/hchin/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/022,522				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	82		N/A				
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	270		N/A				
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	110		N/A				
TOTAL CLAIMS (37 CFR 1.16(j))	36	minus 20 = *	16	x 26 =	416					
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4	minus 3 = *	1	x 110 =	110					
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				0.00					
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					195					
			TOTAL		1183	TOTAL				
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY,DOCKET,NO	TOT CLAIMS	IND CLAIMS
13/022,522	02/07/2011	2811	1183	40003771-0003-453	31	4

CONFIRMATION NO. 6852

26263
SNR DENTON US LLP
P.O. BOX 061080
CHICAGO, IL 60606-1080

FILING RECEIPT



Date Mailed: 02/24/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Daniel E. Grupp, Palo Alto, CA;
Daniel J. Connelly, Redwood City, CA;

Power of Attorney: The patent practitioners associated with Customer Number 26263

Domestic Priority data as claimed by applicant

This application is a DIV of 12/197,996 08/25/2008 PAT 7,884,003
which is a DIV of 11/181,217 07/13/2005 PAT 7,462,860
which is a CON of 10/217,758 08/12/2002 PAT 7,084,423

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

If Required, Foreign Filing License Granted: 02/16/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/022,522**

Projected Publication Date: To Be Determined - pending completion of Corrected Papers

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Preliminary Class

257

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER**Title 35, United States Code, Section 184****Title 37, Code of Federal Regulations, 5.11 & 5.15****GRANTED**

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where

the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

MULTIPLE DEPENDENT CLAIM FEE CALCULATION SHEET Substitute for Form PTO-1360 (For use with Form PTO/SB/06)							Application Number 13022522		Filing Date				
							Applicant(s) Daniel Grupp						
							* May be used for additional claims or amendments						
CLAIMS	AS FILED		AFTER FIRST AMENDMENT		AFTER SECOND AMENDMENT			*		*		*	
	Indep	Depend	Indep	Depend	Indep	Depend		Indep	Depend	Indep	Depend	Indep	Depend
1	1												
2		1											
3	1												
4		1											
5		1											
6		1											
7		1											
8		1											
9		1											
10		1											
11		1											
12		1											
13		1											
14		1											
15		1											
16		1											
17		1											
18		1											
19		1											
20		2											
21		2											
22		2											
23		2											
24		2											
25	1												
26		1											
27		1											
28		1											
29		1											
30		1											
31	1												
32													
33													
34													
35													
36													
37													
38													
39													
40													
41													
42													
43													
44													
45													
46													
47													
48													
49													
50													
Total Indep	4		0		0								
Total Depend	32	↙	0	↙	0	↙							
Total Claims	36		0		0								

51						
52						
53						
54						
55						
56						
57						
58						
59						
60						
61						
62						
63						
64						
65						
66						
67						
68						
69						
70						
71						
72						
73						
74						
75						
76						
77						
78						
79						
80						
81						
82						
83						
84						
85						
86						
87						
88						
89						
90						
91						
92						
93						
94						
95						
96						
97						
98						
99						
100						

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Daniel E. Grupp

Application No.: 13/022,522

Filed: February 7, 2011

Examiner: Not Yet Assigned

Art Unit: 2811

Docket No.: 40003771-0003-453

Confirmation No.: 6852

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

Sir:

In response to the Notice to File Corrected Application Papers mailed February 24, 2011, please find enclosed:

- Replacement Drawings 6-7D of the Formal Figures in compliance with 37 CFR 1.84 and 37 CFR 1.121(d);

If any additional fee is required, please charge Deposit Account No. 19-3140.

Respectfully submitted,

Date: March 25, 2011

/Tarek N. Fahmi/

Tarek N. Fahmi, Reg. No. 41,402

SNR DENTON US LLP
P.O. Box 061080
Wacker Drive Station, Willis Tower
Chicago, Illinois 60606-1080
(650) 798.0320

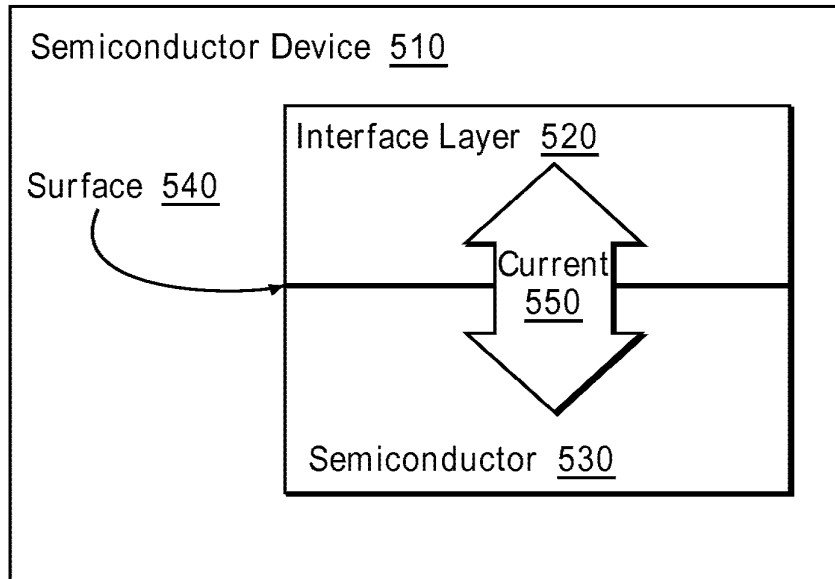


FIG. 5

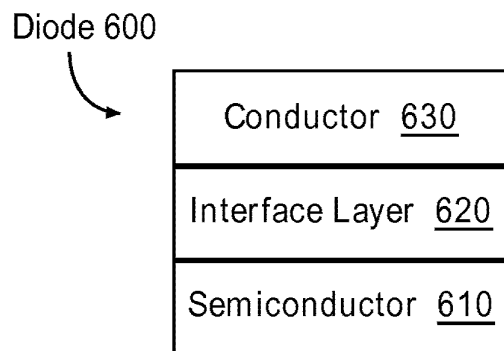
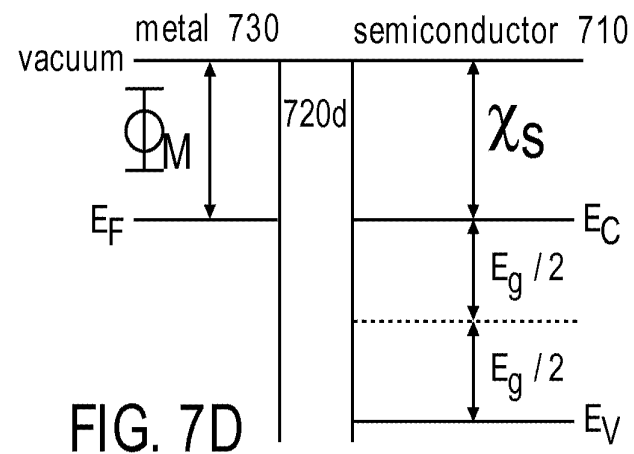
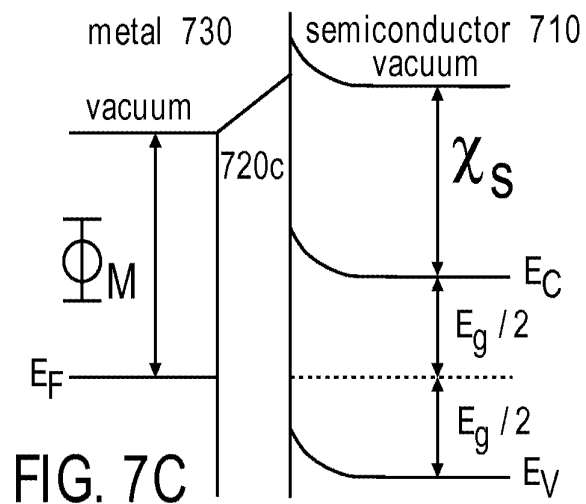
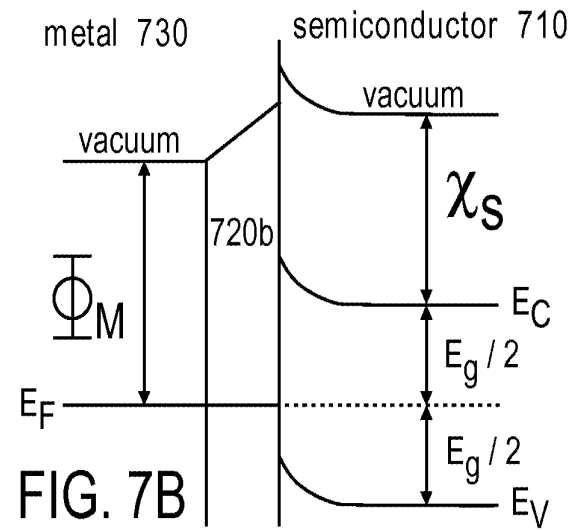
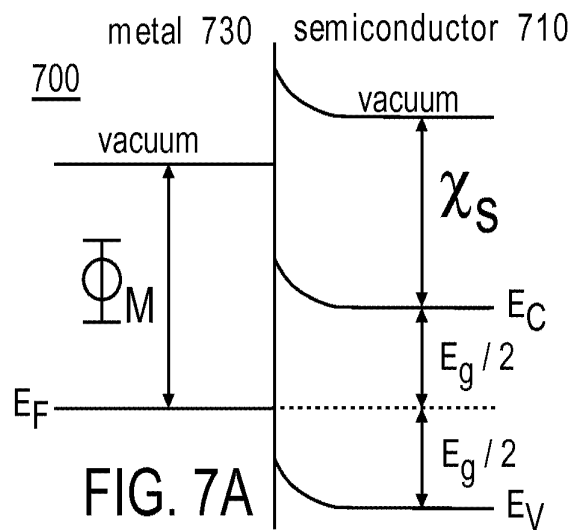


FIG. 6



Electronic Acknowledgement Receipt

EFS ID:	9745652
Application Number:	13022522
International Application Number:	
Confirmation Number:	6852
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	26263
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-453
Receipt Date:	25-MAR-2011
Filing Date:	07-FEB-2011
Time Stamp:	20:08:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		40003771-0003-453_Response_to_Notice_filed_03_25_2011.pdf	169393 bc423aabd121bd236841b7480e6e81a3fff577e4	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Applicant Response to Pre-Exam Formalities Notice	1	1
	Drawings-only black and white line drawings	2	3
Warnings:			
Information:			
Total Files Size (in bytes):		169393	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

Electronic Acknowledgement Receipt

EFS ID:	9745741
Application Number:	13022522
International Application Number:	
Confirmation Number:	6852
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	26263
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-453
Receipt Date:	25-MAR-2011
Filing Date:	07-FEB-2011
Time Stamp:	20:35:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	NPL Documents	BLOSSE_A_NOVEL_LOW_COST_65nm.pdf	219519 db76db36e1586dfbea07c7875db58ddb9e0ee9eb	no	4

Warnings:

Information:

2	NPL Documents	CONNELLY_OPTIMIZING_SCHOTT TKY_S_D_OFFSET.pdf	269616	no	3
			7b21c1e764f36cb485af968bbbaabb294bc1097c		
Warnings:					
Information:					
3	NPL Documents	EDELSTEIN_FULL_COPPER_WIR ING_IN_A_SUB.pdf	300637	no	4
			7a2e92f666f1d44126dc6c874e52e7eaf9d9f8ae		
Warnings:					
Information:					
4	NPL Documents	GOPALKRISHNAN_IMPACT_ION IZATION_MOS_I-MOS.pdf	723815	no	8
			835bac9a441e586283f6c3e63661e94904bf7b07		
Warnings:					
Information:					
5	NPL Documents	KEDZIERSKI_EXTENSION_AND_ SOURCE_DRAIN_DESIGN.pdf	638426	no	7
			03e76f01d1140908e62eb45e91b894553cfb33e1		
Warnings:					
Information:					
6	NPL Documents	THOMPSON_A_LOGIC_NANOTECHNOLOGY_FEATURING_STR AINED.pdf	289979	no	3
			ac2cabaa0a1834ba2770b53a6bf51e1d0ffa5efd		
Warnings:					
Information:					
7	NPL Documents	WEI_THE_USE_OF_SELECTIVE_ ELECTROLESS_METAL_DEPOSITION.pdf	268872	no	4
			d0b3c2635fb997d2e24f23e93bb8e8d642755a06		
Warnings:					
Information:					
8	NPL Documents	YAGISHITA_HIGH_PERFORMANCE_DAMASCENE_METAL_GATE .pdf	652510	no	7
			8698bfc9e3bbe4b15018326a833c8962804e9a96		
Warnings:					
Information:					
Total Files Size (in bytes):			3363374		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522
	Filing Date		2011-02-07
	First Named Inventor	Daniel E. Grupp	
	Art Unit	2811	
	Examiner Name		
	Attorney Docket Number	40003771-0003-453	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	3590471		1971-07-06	Lepselter, et al.	
	2	3708360		1973-01-02	Wakefield, Jr., et al.	
	3	3983264		1976-09-28	Schroen, Walter H., et al.	
	4	4056642		1977-11-01	Saxena, Arjun N. et al.	
	5	4300152		1981-11-10	Lepselter	
	6	4485550		1984-12-04	Koeneke, et al.	
	7	5021365		1991-06-04	Kirchner, et al.	
	8	5399206		1995-03-21	de Lyon	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		13022522
Filing Date		2011-02-07
First Named Inventor	Daniel E. Grupp	
Art Unit		2811
Examiner Name		
Attorney Docket Number		40003771-0003-453

9	5578848		1996-11-26	Kwong, et al.	
10	5596218		2009-04-10	Soleimani, et al.	
11	5612567		1997-03-18	Baliga	
12	5663584		1997-09-02	Welch	
13	5801398		1998-09-01	Hebiguchi	
14	5888891		1999-03-30	Gould	
15	5939763		1999-08-17	Hao, et al.	
16	6037605		2000-03-14	Yoshimura	
17	6096590		2000-08-01	Chan, et al.	
18	6150286		2000-11-21	Sun et al.	
19	6198113		2001-03-06	Grupp, Daniel E.	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		13022522
Filing Date		2011-02-07
First Named Inventor	Daniel E. Grupp	
Art Unit		2811
Examiner Name		
Attorney Docket Number		40003771-0003-453

20	6207976		2001-03-27	Takshashi et al.	
21	6261932		2001-07-17	Hulfachor	
22	6291866		2001-09-18	Wallace et al.	
23	6291867		2001-09-18	Wallace et al.	
24	6303479		2001-10-16	Snyder	
25	7084423		2006-08-01	Grupp et al.	
26	5801444		1998-09-01	Aboelfotoh et al.	
27	7176483		2007-02-13	Grupp et al.	

If you wish to add additional U.S. Patent citation information please click the Add button.

Add

U.S.PATENT APPLICATION PUBLICATIONS

Remove

Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	20030121468		2003-07-03	Boone et al.	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13022522
Filing Date	2011-02-07
First Named Inventor	Daniel E. Grupp
Art Unit	2811
Examiner Name	
Attorney Docket Number	40003771-0003-453

2	20040026687		2004-02-12	Grupp et al.	
3	20050093027		2005-05-05	Grupp et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. [Add](#)

FOREIGN PATENT DOCUMENTS

[Remove](#)

Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1	0295490	EP		1988-12-21	Fowler, Alan B. et al.		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button. [Add](#)

NON-PATENT LITERATURE DOCUMENTS

[Remove](#)

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	ABERLE, ARMIN G., et al., "Injection-Level Dependent Surface Recombination Velocities at The Silicon-Plasma Silicon Nitride Interface", Institut fur Solaenergieforschung, ISFH, D-3 1860 Emmerthal, Germany, (3/9/95), pp. 2828-2830	☐
	2	B. J. ZHANG, et al., "Schottky Diodes of Ni/Au on n-GaN Grown on Sapphire and SiC Substrates", Applied Physics Letters, Vol. 79, No. 16, (10/15/01), pp. 2567-2569	☐
	3	B.R. WEINBERGER, et al., "Surface Chemistry of HF Passivation Silicon: X-Ray Photoelectron And Ion Scattering Spectroscopy Results", J. Appl. Phys. 60(9), (11/186), pp. 3232-3234	☐
	4	C.L. CHEN, et al., "High Quality Native-Oxide-Free Ultrathin Oxide Grown by In-Situ HF-Vapor Treatment", Electronic Letters, Vol. 36, No. 11, (5/25/00), pp. 981-983	☐

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13022522
Filing Date	2011-02-07
First Named Inventor	Daniel E. Grupp
Art Unit	2811
Examiner Name	
Attorney Docket Number	40003771-0003-453

5	CHUNG-KUANG, HUANG , et al., "Two-Dimensional Numerical Simulation of Schottky Barrier MOSFET with Channel Length to 10 nm", IEEE, pp. 842-848	☐
6	D. J. CHADI, et al., "Fermi-Level-Pinning Defects in Highly n-Doped Silicon", Physical Review Letters, Vol. 79, No. 24, NEC Research Institute, Princeton New Jersey 08540-6634, (12/97),pp. 4834-4837	☐
7	E. YABLONOVITCH, et al., "Unusually Low Surface-Recombination Velocity on Silicon and Germanium Surfaces", Physical Review Letters, Vol. 57, No. 2, (7/14/86),pp. 249-252	☐
8	F. A. PADOVANI, "Forward Voltage-Current Characteristics of Metal-Silicon Schottky Barriers", Texas Instruments, Inc., Dallas Texas, (9/15/66),pp. 892-892	☐
9	G.B. AKERS, et al., "Effects of Thermal Stability and Roughness on Electrical Properties of Tantalus Oxide Gates", Mat. Res., Soc. Symp. Proc., Vol. 567, Materials Research Society, (1999),pp. 391-395	☐
10	HASEGAWA, HIDEKI , et al., "Upping of Fermi Level in Nanometer-Sized Schottky Contacts on GaAs and InP", Reseach Center For Interface Quantum Electronics And Graduate School of Electronics And Info. Eng, Hokkaido Univ, Japan, (2000),pp. 92-96	☐
11	HEINE, VOLKER , "Theory of Surface States", Physical Review Letters, Vol. 138, No. 6A, Tell Telephone Lab., Murphy Jill, New Jersey, (6/4/65),	☐
12	HUANG, FENG-JUNG , "Metal-Oxide Semiconductor Field-Effect Transistors Using Schottky Barrier Drains", Electronics Letters, Vol. 33, No. 15, (7/17/97),pp. 1341-1342	☐
13	I. SHALISH, et al., "Yellow Luminescence And Fermi Level Pinning in GaN Layers", American Institute of Physics, Vol. 77, No. 7, (8/14/00),pp. 987-989	☐
14	INTERNET, http://www.rciqe.hokudai.ac.jp/RCIQEold/ResearchAchievements.html , downloaded (4/12/02),	☐
15	IZUMI, HIROT , et al., "43 Hydrogen Termination: The Ideally Finished Silicon Surface", Ultraclean Surface Processing of Silicon Wafers: Secrets of Vlsi Manufacturing http://halloftechnology.com/electrical_optical/986.shtml , (11/98),	☐

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13022522
Filing Date	2011-02-07
First Named Inventor	Daniel E. Grupp
Art Unit	2811
Examiner Name	
Attorney Docket Number	40003771-0003-453

16	J. HILSENBECK, et al., "Aging Behavior of AlGaIn/GaN HFETs With Advanced Ohmic And Schottky Contacts", Electronic letters, Vol. 36, No. 11, (5/25/00),pp. 980-981	☐
17	J. TERSOFF, "Schottky Barrier Heights and The Continuum of Gap States", Physical Review Letters, Vol. 52, No. 6, AT&T Bell Lab., Murphy Hill, New Jersey 07974, (2/6/84),	☐
18	J.R. PATEL, et al., "Arsenic Atom Location on Passive Silicon (111) Surfaces", Physical Review B. Vol. 36, No. 14, (11/15/87),pp. 7715-7717	☐
19	K. NAUKA, et al., "Surface Photovoltage Measurement of Hydrogen-Treated Si Surfaces", Journal of Electrochemical Society 146(1), (1999),pp. 292-295	☐
20	KAMIYAMA, SATOSHI, et al., "Ultrathin Tantalum Oxide Capacitor Dielectric Layers Fabricated Using Rapid Thermal Nitridation Prior to Low Pressure Chemical Vapor Deposition", J. Electrochem Soc., Vol. 140, No. 6, The Electrochemical Society, Inc., (6/6/93),pp. 1617	☐
21	KIMURA, MITSUTERU, et al., "A New Type of Schottky Tunnel Transistor", IEEE Electron Device Letters, Vol. 15, No. 10, (10/94),pp. 412-41	☐
22	L. CAI, et al., "Investigation of The Properties of Plasma-Enhanced Chemical Vapor Deposition Silicon Nitride And its Effect on Silicon Surface Passivation", Journal of Applied Physics, Vol. 83, No. 11, (6/1/98),pp. 5885-5889	☐
23	LEE, TAKHEE, et al., "Electronic Property of Metallic Nanoclusters on Semiconductor Surfaces: Implications For Nanoelectronic Device Applications", Journal of Nanoparticle Research 2, (2000),pp. 345-362	☐
24	LOUIE, STEVEN G., et al., "Ionicity And The Theory of Schottky Barriers", Physical Review Letters, Vol. 15, No. 4, Dept. of Phys. Univ. of California, and Materials and Molecular Research Div., Lawrence Berkeley Lab., Berkeley, CA 94720,	☐
25	M. A. SOBOLEWSKI, et al., "Properties of Ultrathin Thermal Nitrides in Silicon Schottky Barrier Structures", Applied Physics Letters, American Institute of Physics, Vol 54, No. 7, (2/13/89),pp. 638-640	☐
26	M. MIYAWAKI, et al., "Improvement of Aluminum-Si Contact Performance in Native-Oxide-Free Processing", IEEE Electron Device Letters, Vol. 11, No. 10, (10/90),pp. 448-450	☐

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13022522
Filing Date	2011-02-07
First Named Inventor	Daniel E. Grupp
Art Unit	2811
Examiner Name	
Attorney Docket Number	40003771-0003-453

27	M.C. GILMER, et al., "Process and Manufacturing Challenges For High-K Gate Stack Systems", Mat. Res. Soc. Symp. Proc. Vol. 567, (1999),pp. 323-341	☐
28	MANDELIS, ANDREAS , et al., "Evidence of a Surface Acceptor State in Undoped Semi-Insulating GaAs by Photothermal Radiometric Deep Level Transient Spectroscopy", Sociedad Mexicana de Ciencias de Superficies y de Vacio, (1999),pp. 13-17	☐
29	NISHIOKA, YASUSHIRO , et al., "Dielectric Characteristics of Fluorinated Ultradry SiO2", Appl. Phy. Letters 54(12), (3/20/89),pp. 1127-112	☐
30	OKAMOTO, NAOYA , et al., "Near-Ohmic Contact of n-GaAs with Ga/Ga/GaAs Quasi-Metal-Insulator-Semiconductor Structure", Jpn. J. Appl. Phys., Vol. 37, (1998),pp. 32483251	☐
31	P. BAUERNSCHMITT, et al., "Yb-SiO2-Si Tunneling Junctions", Elsevier Publishers B.V., (1993),pp. 105-108	☐
32	PORTER, LISA M., et al., "A Critical Review of Ohmic and Rectifying Contacts For Silicon Carbide", Material Science and Engineering, Vol. 34, No. 2, (11/1/95),pp. 83-105	☐
33	R.A. MCKEE, et al., "Physical Structure And Inversion Charge at a Semiconductor Interface With a Crystalline Oxide", www.sciencemag.org, Vol. 293, (7/20/01),pp. 468-469	☐
34	R.D. BRINGANS, "Arsenic Passivation of Si and Ge Surfaces", Critical Reviews in Solid State and Materials Sciences, 17(4): 353-395, (1992),pp. 353-395	☐
35	R.M.C. DE ALMEIDA, et al., "Reaction-Diffusion Model For Thermal Growth of Silicon Nitride Films on Si", Physical Review B, Vol. 62, No. 24, (12/1500),pp. R16 255-R16 258	☐
36	R.T. TUNG, "Electron Transport of Inhomogeneous Schottky Barriers", AT&T Bell Lab., Murray Hill, New Jersey 07974, (3/21/91),pp. 3832-3834	☐
37	S. HARA, et al., "Control of Schottky And Ohmic Interfaces by Unpinning Fermi Level", Elsevier Science B.V., pp. 394-399	☐

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13022522
Filing Date	2011-02-07
First Named Inventor	Daniel E. Grupp
Art Unit	2811
Examiner Name	
Attorney Docket Number	40003771-0003-453

38	S. HARA, et al., "Pinning-Controlled Metal/Semiconductor Interfaces", Electrotechnical Laboratory, pp. 802-807	☐
39	S. HARA, et al., "Pinning-Controlled Ohmic Contacts: Application to SiC(0001)", Elsevier Science B.V., pp. 218-221	☐
40	S. VERHAVERBEKE, et al., "Surface Characterization of Si After HF Treatments and its Influence in the Dielectric Breakdown of Thermal Oxides", Research Aspirant of the Belgium National Fund for Scientific Research; Mat. Res. Soc. Symp. Proc., Vol. 259, Material Research Society, (1992),pp. 391-399	☐
41	S.A. WOLF, et al., "Spintronics: A Spin-Based Vision For The Future", www.sciencemag.or, Vol.294, (11/6/01),pp. 1488	☐
42	S.M. SZE, "Metal-Semiconductor Contacts", Physics of Semiconductor Devices, John Wiley & Sons, (1981),	☐
43	SCHMIDT, JAN , et al., "Carrier Recombination at Silicon-Silicon Nitride Interfaces Fabricated by Plasma-Enhanced Chemical Vapor Deposition", Journal of Applied Physics, Vol. 85, No. 7, (4/1/99),pp. 3626-3633	☐
44	ACORN TECHNOLOGIES, INC. PCT/US03/25054 filed 08 August 2003, International Search Report, International Searching Authority/US, (12/3/03),pp. 6	☐
45	SHAIK, LAHIR , et al., "Experimental Identification of Nitrogen-Vacancy Complexes in Nitrogen Implanted Silicon", Applied Physics Letters, Vol. 79, No. 5, (7/30/01),pp. 623-625	☐
46	SNYDER, JOHN P., et al., "Experimental Investigation of a PtSi Source And Drain Field Emission Transister", American Institute of Physics, pp. 1-3	☐
47	T.I. KAMINS, et al., "Effect of Hydrogen on p-Type Epitaxial Silicon Sheet-Resistance Measurements", Electrochemical and Solid-State Letters 1(2), (1998),pp. 100-101	☐
48	TERAJI, TOKUYUKI , et al., "Ohmic Contacts To n-Type 6H-SiC Without Post-Annealing", Material Research Society Symposium Proceeding, (4/8/96),pp. 149-154	☐

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13022522
Filing Date	2011-02-07
First Named Inventor	Daniel E. Grupp
Art Unit	2811
Examiner Name	
Attorney Docket Number	40003771-0003-453

49	U.J.R. BAUMVOL, "Atomic Transport During Growth of Ultrathin Dielectrics on Silicon", Surface Science Reports 36, (1999),pp. 1-166	☐
50	W.E. SPICER, et al., "Unified Mechanism For Schottky-Barrier Formation And III-V Oxide Interface States", Physical Review Letters, Vol. 44, No. 6, Stanford Electronics Lab., Stanford Univ., Stanford, CA 94305, (2/11/80),pp. 420-423	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13022522
Filing Date	2011-02-07
First Named Inventor	Daniel E. Grupp
Art Unit	2811
Examiner Name	
Attorney Docket Number	40003771-0003-453

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2011-03-25
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

U.S. PATENTS							Remove
---------------------	--	--	--	--	--	--	------------------------

Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button.

[Add](#)

U.S. PATENT APPLICATION PUBLICATIONS							Remove
---	--	--	--	--	--	--	------------------------

Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button.

[Add](#)

FOREIGN PATENT DOCUMENTS								Remove
---------------------------------	--	--	--	--	--	--	--	------------------------

Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

[Add](#)

NON-PATENT LITERATURE DOCUMENTS				Remove
--	--	--	--	------------------------

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13022522
Filing Date	2011-02-07
First Named Inventor	Daniel E. Grupp
Art Unit	2811
Examiner Name	
Attorney Docket Number	40003771-0003-453

1	WANG, LIE , et al., "High Barrier GaN Schottky Diodes: Pt/GaN and Pd/GaN", Dept. of Electrical Eng., Univ. of Minnesota, Minneapolis, Minnesota 55455; Appl. Phys. Letters, Vol. 68(9), (2/26/96),pp. 1267-1270	☐
2	WIDJAJA, YUNIARTO , et al., "Ab Initio Study and Decomposition of NH3 on Si(100)-(2x1)", J. Phy. Chem B, (2000), pp. 2527-2533	☐
3	WRIGHT, PETER J., et al., "Hot-Electron Immunity of SiO2 Dielectrics with Fluorine Incorporation", IEEE Electron Device Letters, Vol. 10, No. 8, (8/8/89),pp. 347-348	☐
4	Y. HAYAFUJI, et al., "Nitridation of Silicon and Oxidized-Silicon", Sony Corp. Research Center, 174 Fujitsuka-Cho, Hodogaya-Ku, Yokohama, 240 Japan; J. Electrochem. Soc.: Solid State Science and Technology, (9/82),	☐
5	Y. K. KIM, et al., "Metal-Dependent Fermi-Level Movement in The Metal/Sulfur-Passivated InGaP Contact", J. Vac Sci. Technology A 15(3), (1997),pp. 1124-1128	☐
6	YANG, HANYANG , et al., "The Effects of Interfacial Sub-Oxide Transition Regions and Monolayer Level Nitridation on Tunneling Currents in Silicon Devices", IEEE Electron Device Letters, Vol. 21, No. 2, (2/2/00),pp. 76-78	☐
7	BLOSSE, A., et al., "A Novel Low Cost 65nm CMOS Process Architecture With Self Aligned Isolation and W Cladded Source/Drain", IEEE, Transactions of 2004 International Electron Device Meeting, pp. 669-672	☐
8	CONNELLY, DANIEL, et al., "Optimizing Schottky S/D Offset for 25-nm Dual-Gate CMOS Performance", IEEE Trans. Electron Devices, Vol. 47 No. 5, (2003), pp. 1028-1034	☐
9	EDELSTEIN, D., et al., "Full Copper Wiring in a Sub-0.25 mm CMOS ULSI Technology", Proceedings of the IEEE International Electron Device Meeting, (12/1997), pp. 773-776	☐
10	GOPALAKRISHNAN, KAILASH, et al., "Impact Ionization MOS (I-MOS)-Part I: Device and Circuit Simulations", IEEE Transactions Electron Devices, Vol. 52, No. 1, (2005), pp. 69-76	☐
11	KEDZIERSKI, JAKUB, et al., "Extension and Source/Drain Design for High-Performance FinFET Devices", IEEE Trans. Electron Devices, Vol. 50, No. 4, (4/2003), pp. 952-958	☐

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13022522
Filing Date	2011-02-07
First Named Inventor	Daniel E. Grupp
Art Unit	2811
Examiner Name	
Attorney Docket Number	40003771-0003-453

12	THOMPSON, SCOTT E., et al., "A Logic Nanotechnology Featuring Strained-Silicon", IEEE Electron Device Letters, Vol. 25, No. 4, (2004), pp. 191-193	☐
13	WEI, C.S., et al., "The Use of Selective Electroless Metal Deposition For Micron Size Contact Fill", IEEE International Electron Device Meeting Technical Digest, (1988), pp. 446-449	☐
14	YAGISHITA, ATSUSHI, et al., "High Performance Damascene Metal Gate MOSFET's for 0.1 mm Regime", IEEE Trans. Electron Devices, Vol. 47, No. 5, (2000), pp. 1028-1034	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13022522
Filing Date	2011-02-07
First Named Inventor	Daniel E. Grupp
Art Unit	2811
Examiner Name	
Attorney Docket Number	40003771-0003-453

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2011-03-25
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

(19)



Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number:

**0 295 490
A1**

(12)

EUROPEAN PATENT APPLICATION

(21) Application number: 88108684.7

(51) Int. Cl. 4: **H01L 21/314 , H01L 29/40 ,
H01L 21/285**

(22) Date of filing: 31.05.88

(30) Priority: 18.06.87 US 64414

(43) Date of publication of application:
21.12.88 Bulletin 88/51

(84) Designated Contracting States:
DE FR GB

(71) Applicant: International Business Machines
Corporation
Old Orchard Road
Armonk, N.Y. 10504(US)

(72) Inventor: Fowler, Alan B.
3511 Kamhi Drive
Yorktown Heights New York 10598(US)
Inventor: Freeouf, John L.
East Mountain, Lake Katonah, Route 3
Katonah New York 10536(US)
Inventor: Kirchner, Peter D.
RR1, Box 156A
Putnam Valley New York 10579(US)
Inventor: Warren, Alan C.
150 Overlook Avenue, Apt. 7A
Peekskill New York 10566(US)
Inventor: Woodall, Jerry M.
336 Cherry Street
Katonah New York 10507(US)

(74) Representative: Kreidler, Eva-Maria, Dr. rer.
nat.
IBM Deutschland GmbH Patentwesen und
Urheberrecht Schönaicher Strasse 220
D-7030 Böblingen(DE)

(54) Compound semiconductor surface termination.

EP 0 295 490 A1

(57) A surface termination of a compound semiconductor is provided wherein conditions are provided for a pristine surface to be retained in an unpinned condition and a surface layer of a non-metallic material is provided. A GaAs substrate is heated in an oxygen-free atmosphere at high temperature with hydrogen sulfide, producing a pristine surface with a coating of gallium sulfide covered with a 1,000 nanometer covering of low temperature plasma enhanced chemical vapor deposited silicon dioxide.

COMPOUND SEMICONDUCTOR SURFACE TERMINATION

The invention relates to semiconductor devices fabricated of compound semiconductor materials and to the surfaces of those semiconductor materials that influence the fabrication of devices.

The design and operation of compound semiconductor devices are influenced by a number of factors, a principal one being the properties of the exposed semiconductor surface and of interfaces between the semiconductor crystal and metals or insulators.

In such compound semiconductor devices, on the surface of the semiconductor crystal, the Fermi level is pinned at some characteristic energy and this produces the undesirable effect of both carrier recombination at the surface and an inherent barrier. The development of a number of otherwise possible and useful devices and device structures have been prevented by these conditions and a more nearly ideal interface, that is one whose Fermi level may be moved freely and has low recombination velocity is required.

There has been effort directed to the problem. The effort usually is called passivation and the result is the providing of a covering member over the compound semiconductor crystal surface.

The work in the art indicates responsiveness to the presence of the element sulfur.

In U.S. Patent 4,354,198, it is taught that on a Group III-V compound semiconductor, such as GaAs, a Group II-VI semiconductor operates to passivate the surface, with the preferred Group II-VI compound being ZnS.

Further work indicates a need for care in the field. In an article in the Journal of Vacuum Science & Technology, Volume 17, No. 5, p.1134, Sept./Oct. 1980, there is described the fact that exposure of GaAs to H_2S in vacuum unpins the Fermi level and that this effect persists after the adding of Al. In another article in the Journal of Vacuum Science & Technology, Vol. B3, No. 4, July/Aug. 1985, p.1197, studies and data indicate the fact that for GaAs, arsenic must be removed or the results become unpredictable. In yet another article, in the Journal of Vacuum Science and Technology, Vol. 19, 1981, p.794, it is shown that native oxides of Ga and As which form in the presence of O are associated with Fermi level pinning. Thus, O behaves in a detrimental way.

The use of sulfur compounds to passivate Group III-V compound semiconductors has been reported Applied Physics Letters, July 1987, wherein data is advanced that lithium sulfide, ammonium sulfide and sodium sulfide provide improvement in the GaAs surface recombination property.

The sulfur compound type further passivation work is reported in Applied Physics Letters, July 1987, describing the use of sodium sulfide in an aqueous solution applied at surface electrode locations to provide passivation.

FIG. 1 is a schematic view of a compound semiconductor crystal illustrating a surface with the elements of the invention.

FIG. 2 is an illustration of a band diagram of a tunneling type contact achievable with the invention.

FIG. 3 is an illustration of a variable barrier height contact achievable with the invention.

FIG. 4 is an illustration of passivation in a planar structure where a p-n junction is at the surface.

FIG. 5 is a schematic illustration of the application of the invention to a metal oxide semiconductor field effect transistor.

FIG. 6 is a schematic illustration of the application of the invention to the passivation of a bipolar transistor.

FIG. 7 is a schematic illustration of the application of the invention to the passivation of a light emitting device.

FIG. 8 is a schematic illustration of the application of the invention to the passivation of a semiconductor structure employing a small dimension, quantum wire type feature.

The invention provides a surface termination capability for a variety of compound semiconductor device structures in which there is recognized that there are several interdependent factors that are responsible and that useful termination properties include compatibility with the device being fabricated.

The invention structurally employs a very thin Fermi level pinning control layer of a material that unpins the Fermi level of the compound semiconductor material at the surface. This layer should be on the order of a monolayer in thickness. A monolayer layer of a material may be defined as one surface atom for each surface atom of the material on which it is positioned. The quantity needed for coverage is sensitive to crystallographic orientation. For compatibility with device fabricating the pinning control layer would preferably be thin enough not to attenuate light and permit tunneling for ohmic contact performance. A quantum mechanical tunneling thickness of the order of 2 nm would be satisfactory. The term pristine crystal surface refers to a damage-free uncontaminated crystal surface. The layer of unpinning material is covered with a second layer of a non-metallic material. The non-metallic material is selected for dielectric ambient

reaction inertness and translucence properties.

The resulting compound semiconductor crystal with the surface termination structure of the invention can serve as an intermediate manufacturing product in the fabrication of compound semiconductor devices.

The factors influencing the surface problem may be viewed in the light of the following principles. In order to facilitate communication, the III-V compound GaAs has been selected for illustration although in the light of the principles involved, translation to other semiconductor materials will be readily apparent.

The first factor is that there exists at a compound semiconductor surface an agent responsible for moving the Fermi level away from the normal which is the position in the absence of any surface charge and producing the phenomenon in the art known as Fermi level pinning. In the case of GaAs, this agent appears to be an excess of one or more of the components of the compound semiconductor crystal. In view of this, surface termination for practical device purposes will require the removal of any such agent at that surface. The semiconductor surface is to be pristine.

A second factor is that the compound semiconductor surface will react with the ambient and become contaminated unless steps are taken by protecting with a coating of material that insures that the Fermi level remain in an unpinned condition both on the shelf and in conditions of use, such as in the presence of the materials at the device interface.

The third factor is that generally materials that will control the pinning condition must be able to be compatible with other functional purposes in device fabrication and there may be conditions of material properties and layer thickness incompatibility. In accordance with the invention where such conditions are encountered, a layer is applied to provide the required properties.

The resulting multilayer termination structure of the invention is capable of being employed in a variety of compound semiconductor device structures because the elimination of the Fermi level pinning condition enables the formation of ideal interfaces where barrier height to conduction is no longer constant but depends on the relative work functions of the materials. This in turn provides the ability to selectably form such interfaces as ohmic contacts, selectable barrier height rectifying contacts, and selectable threshold inversion channel carrier control in devices.

Referring to FIG. 1, on a compound semiconductor substrate 1, at a pristine surface 2, that is at a surface 2 where there is essentially no damage and essentially no extraneous material, there will be no pinning agent species, a layer of material

that retains the Fermi level in the normal position is applied. The layer for device fabrication and performance compatibility is a very thin, of the order of a monolayer in thickness layer of a material 3 for coverage and is preferably for tunneling purposes of less than tunneling thickness.

Over the layer 3, a layer 4 is provided. The layer 4 is selected to provide dielectric, ambient reaction inertness and translucence properties. It is non-metallic and may be a semiconductor or an insulator.

In accordance with the invention, the compound semiconductor may be a compound of Ga, Al or In with As or Sb or ternary and quaternary alloys thereof.

The layer 3 is a compound of a cation ingredient with respect to the compound semiconductor together with one of S, Se and Te. In a compound semiconductor, the element of the lower group of the periodic table is the cationic ingredient. For one example, a compound of Ga with S. For another example, the layer 3 can be a cation oxide such as Ga_2O_3 for a GaAs crystal, if the anion oxide which for GaAs would be As_2O_3 plus any excess anion such as As are removed before or during formation of the unpinning layer.

The layer 4 is non-metallic and may be such materials as low temperature plasma enhanced SiO_2 , CaF_2 , NaS, ZnS, GaP, GaSe and polyimides.

In the fabrication of the invention, the substrate 1 may be rendered pristine and free of the pinning producing species in, as examples, the following ways, using GaAs as the example:

- by heating the crystal with an arsenic coating at about $400^\circ C$ for about 10 seconds in vacuum. This procedure produces a surface reconstruction such that the surface unit cell is equivalent to the bulk unit cell and removes the cause of the Fermi level pinning;
- by treatment with zinc selenide in a beam that tends to strip the arsenic from the surface;
- by exposure to an ambient of hydrogen sulfide at high temperatures;
- by the etching of the surface with acids and bases; and
- by photo-washing under conditions where the crystal surface is subjected to water in the presence of light.

All of these operations provide a compound semiconductor crystal with pristine surface that does not have any of the pinning causing species thereon. Such a surface requires protection so that in accordance with the invention a very thin material that will retain the Fermi level in the free

position is applied. This material is a compound of the cation of the compound semiconductor crystal and is a member taken from the group of S, Se and Te, which for GaAs is gallium sulfide, gallium selenide and gallium telluride.

The application of the layer 4 may employ such techniques as exposing the crystal 1 in FIG. 1 with the layer 3 in place to an ambient of H_2S , to an evaporation of sodium sulfide, gallium sulfide or gallium selenide, and by the technique of photo-washing.

The technique of photo-washing is described in European patent application Serial No. 87 107 476.1. The surface produced by that technique may be used as the structure of Fig. 1 on which the layer 4 is to be applied.

The layer 4 is then applied in a thickness of up to approximately 1,000 nanometers.

The surface termination of the invention is useful in a variety of device structures.

Referring next to FIG. 2, there is shown a band energy diagram illustrating an interface suitable for ohmic contact performance where the layer 3 at the pristine surface 2 results in the Fermi level E_f being unpinned at the surface 2 and the dielectric layer 4 is made sufficiently thin to permit quantum mechanical tunneling so that a contact through a low work function metal, such as In for the metal 5 will demonstrate on a GaAs crystal essentially ohmic conduction performance. The layer 3 being of a monolayer order is thin enough not to interfere with the tunneling mechanism and the layer 4 is of the proper thickness which for most applications is of the order of 2 nm generally achieved in connection with the positioning of the metal contact 5.

In the fabricating of different types of device structures, it is desirable to have a barrier to electrical conduction that is selectable. The selectability provides controllable performance rectifying contacts and the ability to control carrier flow in an inversion channel in a device.

Referring next to FIG. 3, a band energy diagram is shown where the layer 4 is sufficiently thin to permit quantum mechanical tunneling so that when a higher work function metal, such as Au is used for the metal 5, the performance is that of a selectable Schottky barrier height. This is useful in threshold control of field effect transistors.

In FIGS. 4 through 8, the application of the invention to various types of semiconductor structures is illustrated.

Referring next to FIG. 4, there is illustrated a device wherein there is a p-n junction 6 that terminates at the surface. Where such a structural condition occurs, the carrier recombination is aggravated by the presence of very high fields illustrated at one intersection as element 7. In accordance with the invention, the layers 3 and 4 under these

conditions operate to prevent both carrier recombination and the effects of the field.

In FIG. 5, a field effect transistor semiconductor device known as a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is illustrated wherein the semiconductor substrate 1 has positioned thereon source and drain ohmic contacts 8 and 9 that go through the layer 3 on the surface 2 and dielectric layer 4 is in a shape modified to accommodate the other requirements of the device. The thin essentially monolayer thickness of the layer 3 permits the ohmic contacts 8 and 9 to be merely positioned on the layer 3 which in turn doesn't interfere with their electrical performance. The layer 4 serves as the insulator of gate 10 with the layer 4 being provided with appropriate thickness and dielectric strength to have the threshold properties for the inversion of a channel between contacts 8 and 9 at the interface of the crystal 1.

With the structural principles of the invention, it will be readily apparent that the type of selectability of the barrier shown in FIG. 3 provides flexibility in imparting characteristics to a device being fabricated.

Referring next to FIG. 6, a bipolar transistor type structure is illustrated vertically oriented with respect to the substrate wherein the substrate 1, appropriately doped, serves as the collector, with an opposite conductivity type appropriately doped base region 11 positioned adjacent the interface 2. On the layer 3 at interface 2, a circular ohmic electrode 12 is positioned separated from and surrounding a mesa semiconductor region 13 epitaxially joined at the interface 2 serving as the emitter which in turn has a contact facilitating semiconductor region 14 serving as the interface to the metal emitter contact 15.

The features of the invention are employed in this type of structure to facilitate prevention of leakage problems that occur with respect to closely positioned contacts, interfaces terminating at the surface, and ohmic performance. The two layer termination structure on pristine surface of the invention is applied around the emitter 13 shown as element 16. The layer 4 is removed in the positioning of ohmic contact 12 and the layer 3 due to the thin dimension thereof does not affect the ohmic performance of contact 12.

The principles of the invention are further applicable to facilitate construction of electro-optical conversion devices.

Referring next to FIG. 7, one of the serious problems in the electro-optical conversion field has been the translucent passivation of pn junctions that radiate light.

Referring to FIG. 7, a light emitting diode type device is shown wherein on a substrate 1, there is a high conductivity extrinsic n+ layer 18, an n-type

layer 19 and a p-type layer 20 in a mesa type configuration, with the pn junction between elements 19 and 20 serving as the light emitting source in a mesa type configuration. The light emitting junction at the surface is indicated as having a field with the circle at 21. The termination structure of the invention is shown as element 22 applied over the mesa. The ohmic contacts 23 to the n+ region 18 and 24 to the p region 20 are made by removing the layer 4, the ohmic performance being unaffected by the thin layer 3.

In this type of structure, the layers 3 and 4 in the termination of the invention are sufficiently thin not to attenuate the emitted light, yet they serve in passivation and facilitate contacting.

Referring to FIG. 8, a typical, very small, of the order of 5 to 10nm dimension active region device is shown. Such a device has come to be known in the art as a quantum wire structure. In FIG. 8, on the substrate 25 of a first band gap semiconductor material, such as GaAs, a region 26 of an atomically compatible different band gap high mobility semiconductor, such as InGaAs, is sandwiched between another layer 27 of a different band gap lower mobility semiconductor material such as GaAs in a mesa configuration. In accordance with the invention, the surface at both sides of the mesa and the substrate is coated with the termination structure comprising layer 3 on a pristine surface covered by layer 4.

The termination operates to passivate the surfaces including the hetero-interfaces between different semiconductor materials. Ohmic contacts 28 and 29 are illustrated showing the presence of the layer 3 which due to thickness does not affect ohmic contact performance. The structure of FIG. 8 would have a contact to the quantum wire region 26, not shown.

The preferred embodiment for fabrication of the structure of FIG. 1 would employ a GaAs crystal 1 which is heated with surface 2 exposed in an oxygen-free atmosphere in H₂S at 700 °C for 30 seconds to render the surface 2 pristine and forms a thin, of the order of a monolayer, coating 3 of gallium sulfide. The GaS coated structure is then provided with a 1-1,000 nanometer dielectric coating 4 of low temperature plasma enhanced chemical vapor deposited silicon dioxide.

What has been described is the fact that surface termination of compound semiconductor material for device use involves insuring the absence of an agent that causes the pinning, the presence of a material that prevents the pinning, and the protection of that material with a non-metallic layer that provides capability for dielectric, ambient reaction inertness and translucence properties.

Claims

1. Compound semiconductor crystal intermediate manufacturing product comprising in combination on a pristine crystal interface of a monocrystalline compound semiconductor material taken from the group of Ga or Al or In and As or Sb and monocrystalline ternary and quaternary alloys thereof,

a Fermi level pinning control layer of a compound of a cation ingredient of said compound semiconductor and a member taken from the group of S, Se and Te in a thickness compatible with electrical current conduction through said layer, and a surface layer of a non-metallic material.

2. Intermediate manufacturing product of claim 1 wherein said compound semiconductor crystal is GaAs and said Fermi level pinning control layer is a Ga compound.

3. Intermediate manufacturing product of claim 1 wherein said non-metallic material is taken from the group of SiO₂, CaF₂, NaS, ZnS, GaP, GaSe and polyimides.

4. Intermediate manufacturing product of claim 1 wherein said Fermi level pinning layer thickness is in a range of one monolayer to approximately 2 nm.

5. Intermediate manufacturing product of claim 1 where the surface layer is in the range of 1 to 1000 nanometers thick.

6. In the fabrication of compound semiconductor device structures, the improvement in providing a compound semiconductor crystal with a device fabrication compatible surface termination, the intermediate manufacturing product comprising on a pristine crystal interface of a monocrystalline compound semiconductor material taken from the group of Ga or Al or In and As or Sb and monocrystalline ternary and quaternary alloys thereof, a Fermi level pinning control layer of a compound of a cation ingredient of said compound semiconductor and a member taken from the group of S, Se and Te in a thickness compatible with electrical current conduction through said layer, and a surface layer of a non-metallic material.

7. Intermediate manufacturing product of claim 6 wherein said compound semiconductor crystal is GaAs and said Fermi level pinning control layer is a Ga compound.

8. Intermediate manufacturing product of claim 6 wherein said non-metallic material is taken from the group of SiO₂, CaF₂, NaS, ZnS, GaP, GaSe and polyimides.

9. Intermediate manufacturing product of claim 6 wherein said Fermi level pinning layer thickness is in a range of the order of one monolayer to approximately 2 nm.

10. Intermediate manufacturing product of claim 6 where the surface layer is in the range of 1 to 1000 nanometers thick.

5

10

15

20

25

30

35

40

45

50

55

FIG. 1

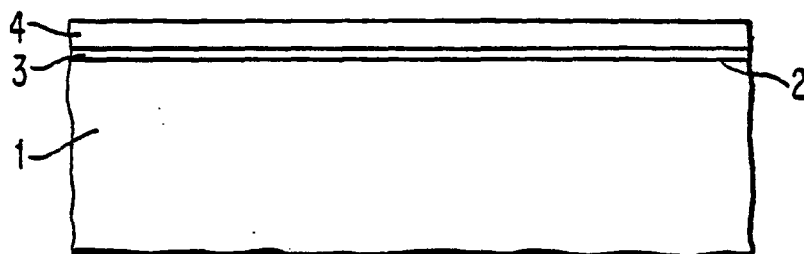


FIG. 2

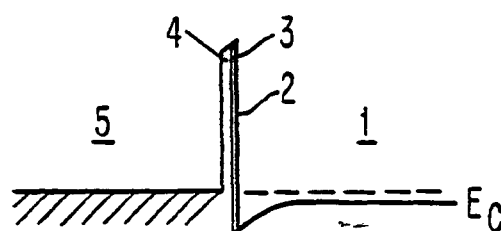


FIG. 3

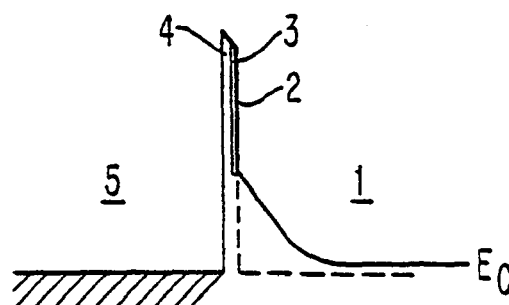


FIG. 4

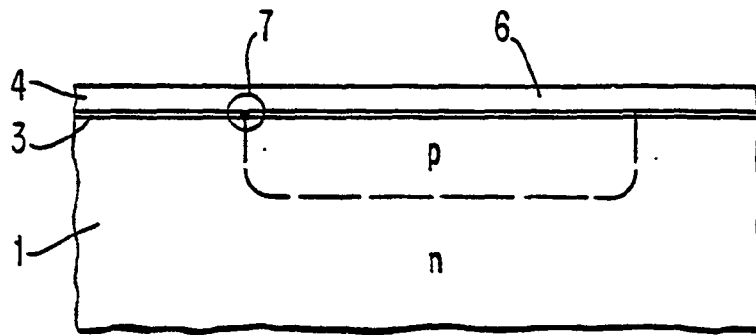


FIG. 5

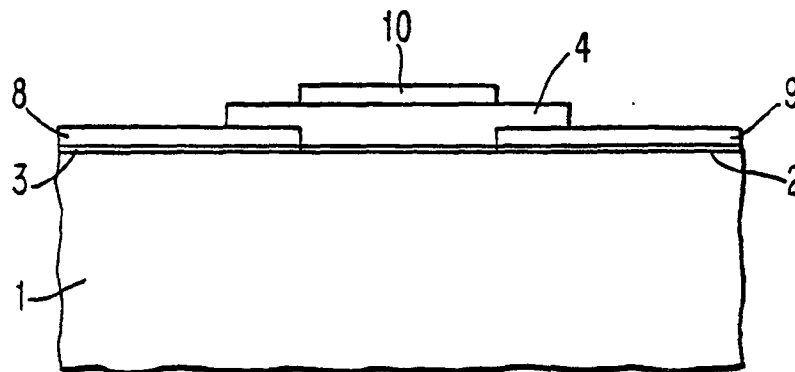


FIG. 6

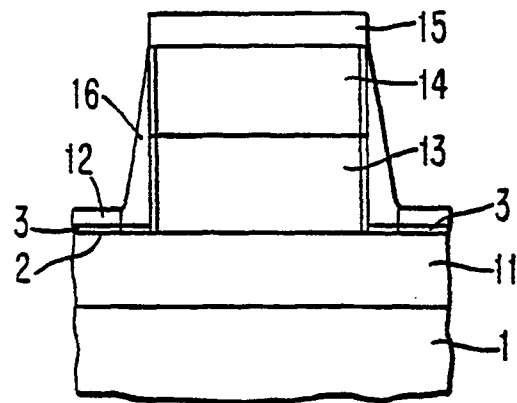


FIG. 7

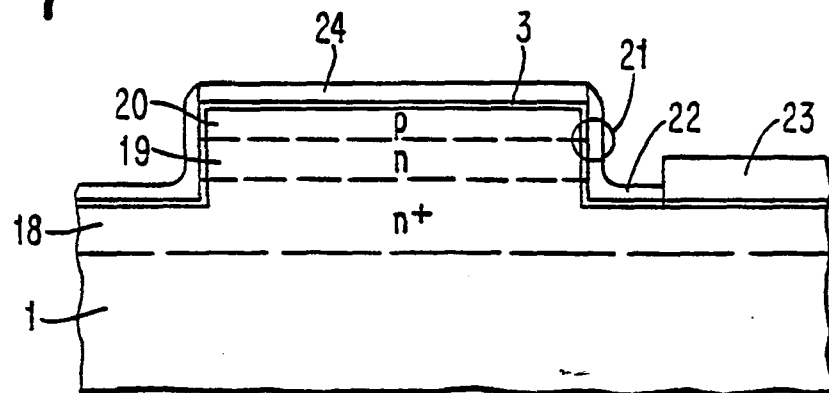
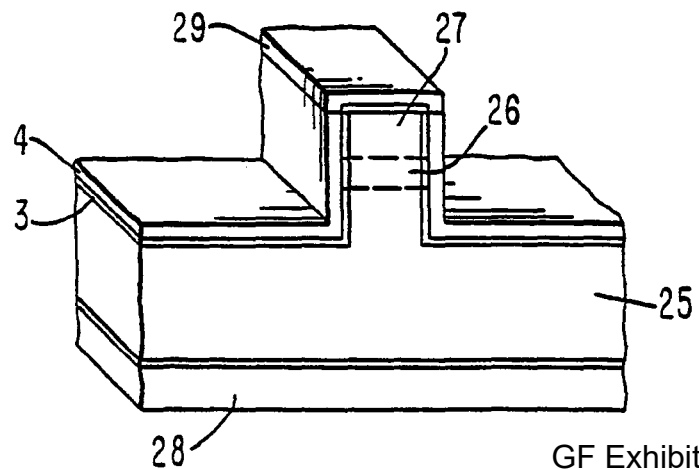


FIG. 8





DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 4)
P,X	EP-A-0 265 314 (CNET/CNRS) * Page 2, line 37 - page 3, line 36 *	1-3	H 01 L 21/314 H 01 L 29/40 H 01 L 21/285
Y	APPLIED PHYSICS LETTERS, vol. 38, no. 9, 1st May 1981, pages 693-695, American Institute of Physics, New York, US; J. MASSIES et al.: "Monocrystalline aluminium ohmic contact to n-GaAs by H ₂ S adsorption" * Abstract; page 695 *	6,7,9	
A	IDEM	1,2,4	
X	WO-A-8 304 420 (HUGHES AIRCRAFT CO.) * Page 12, line 24; page 15, lines 26-34; page 24, line 4 - page 26, line 30; page 27, line 1 - page 28, line 1 *	1,2,4	
Y		6,7,9	
A	US-A-3 983 264 (TEXAS INSTRUMENTS INC.) * Page 3, lines 1-39 *	1,2,4,6 7,9	TECHNICAL FIELDS SEARCHED (Int. Cl.4)
A	GB-A-2 046 994 (D. CHEMLA et al.) * Abstract *	1,2,6,7	H 01 L
D,A	JOURNAL OF VACUUM SCIENCE & TECHNOLOGY, vol. B3, no. 4, July/August 1985, pages 1197-1201, American Vacuum Society, New York, US; J.R. WALDROP: "Influence of S and Se on the schottky-barrier height and interface chemistry of Au contacts to GaAs" * Abstract; page 1197, right-hand column - page 1198, left-hand column *	1,6	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 30-09-1988	Examiner GELEBART J.F.M.
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	



DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 4)
A	JOURNAL OF THE ELECTROCHEMICAL SOCIETY, vol. 134, no. 2, February 1987, pages 437-439, Manchester, NH, US; T. NARUSAWA et al.: "Structural study of GaAs-dielectric film (CaF ₂ , Al ₂ O ₃) interfaces by high-energy ion scattering" * Abstract *	3,8	
D,A	JOURNAL OF VACUUM SCIENCE & TECHNOLOGY, vol. 17, no. 5, September/October 1980, pages 1134-1140, American Vacuum Society; J. MASSIES et al.: "Effects of H ₂ S adsorption on surface properties of GaAs (100) grown in situ by MBE"		
			TECHNICAL FIELDS SEARCHED (Int. Cl. 4)
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 30-09-1988	Examiner GELEBART J.F.M.
CATEGORY OF CITED DOCUMENTS			
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons ----- & : member of the same patent family, corresponding document	

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

PCT

TNE
03771P003

To:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN
LLP
Attn. Fahmi, Tarek
12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025
UNITED STATES OF AMERICA

DEC 10 2003

RECEIVED

DEC 04 2003

NOTIFICATION OF TRANSMITTAL OF
STATUS OF THE INTERNATIONAL SEARCH REPORT
OR THE DECLARATION

(PCT Rule 44.1)

DEC 11 2003

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
LOS ANGELES

Date of mailing
(day/month/year)

03/12/2003

LA FIF DEPT

Applicant's or agent's file reference

3771P003PCT

FOR FURTHER ACTION

See paragraphs 1 and 4 below

International application No.

PCT/US 03/25054

International filing date
(day/month/year)

08/08/2003

Applicant

ACORN TECHNOLOGIES, INC.

1. ☒ The applicant is hereby notified that the International Search Report has been established and is transmitted herewith.

Filing of amendments and statement under Article 19:

The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

When? The time limit for filing such amendments is normally 2 months from the date of transmittal of the International Search Report; however, for more details, see the notes on the accompanying sheet.

Where? Directly to the International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland
Fascimile No.: (41-22) 740.14.35

Entered in FIP on: 12/10

By: NA

Docketing Department

For more detailed instructions, see the notes on the accompanying sheet.

2. ☐ The applicant is hereby notified that no International Search Report will be established and that the declaration under Article 17(2)(a) to that effect is transmitted herewith.

3. ☐ **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Further action(s):** The applicant is reminded of the following:

Shortly after **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90bis.1 and 90bis.3, respectively, before the completion of the technical preparations for international publication.

Within **19 months** from the priority date, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase until 30 months from the priority date (in some Offices even later).

Within **20 months** from the priority date, the applicant must perform the prescribed acts for entry into the national phase before all designated Offices which have not been elected in the demand or in a later election within 19 months from the priority date or could not be elected because they are not bound by Chapter II.

Name and mailing address of the International Searching Authority



European Patent Office, P.B. 5818 Patentlaan 2
NL-2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Jacinta Reddy

ENTERED INTO CALENDAR

BY: A

DATE: 1/10/04

FORWARDED TO

1010 - 95/229

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 3771P003PCT	FOR FURTHER ACTION see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
International application No. PCT/US 03/ 25054	International filing date (day/month/year) 08/08/2003	(Earliest) Priority Date (day/month/year) 12/08/2002
Applicant ACORN TECHNOLOGIES, INC.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 5 sheets.



It is also accompanied by a copy of each prior art document cited in this report.

1. Basis of the report

- a. With regard to the **language**, the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.



the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

- b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :



contained in the international application in written form.



filed together with the international application in computer readable form.



furnished subsequently to this Authority in written form.



furnished subsequently to this Authority in computer readable form.



the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.



the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. ☐ **Certain claims were found unsearchable** (See Box I).

3. ☐ **Unity of invention is lacking** (see Box II).

4. With regard to the **title**,

the text is approved as submitted by the applicant.



the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

the text is approved as submitted by the applicant.



the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No.

5



as suggested by the applicant.



None of the figures.



because the applicant failed to suggest a figure.



because this figure better characterizes the invention.

INTERNATIONAL SEARCH REPORT

international application No.

PCT/US 03/25054

Box III TEXT OF THE ABSTRACT (Continuation of item 5 of the first sheet)

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L29/45 H01L21/285 H01L29/47 H01L21/329 H01L29/872

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, COMPENDEX, IBM-TDB, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 3 983 264 A (PADOVANI FRANCOIS A ET AL) 28 September 1976 (1976-09-28) column 2, line 49 -column 6, line 29; figure 2 ---	1-26, 31-54, 57-61
X	US 5 021 365 A (WARREN ALAN C ET AL) 4 June 1991 (1991-06-04) column 5, line 64 -column 6, line 49; figures 2,4,9 ---	1-26, 31-54, 57-61
X	EP 0 295 490 A (IBM) 21 December 1988 (1988-12-21) column 5, line 19 -column 6, line 24; figures 2-5 --- -/--	1-26, 31-54, 57-61



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
- *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
- *G* document member of the same patent family

Date of the actual completion of the international search

25 November 2003

Date of mailing of the international search report

03/12/2003

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Berthold, K

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 0 789 388 A (AGENCY IND SCIENCE TECHN) 13 August 1997 (1997-08-13) page 8, line 37 -page 13, line 6; figure 2 ----	1-61
Y	TERAJI T ET AL: "OHMIC CONTACTS TO N.TYPE 6H.SIC WITHOUT POST-ANNEALING" MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS, MATERIALS RESEARCH SOCIETY, PITTSBURG, PA, US, 8 April 1996 (1996-04-08), pages 149-154, XP002068069 ISSN: 0272-9172 page 150 -page 153 ----	1-61
Y	SOBOLEWSKI M A ET AL: "PROPERTIES OF ULTRATHIN THERMAL NITRIDES IN SILICON SCHOTTKY BARRIER STRUCTURES" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 54, no. 7, 13 February 1989 (1989-02-13), pages 638-640, XP000048508 ISSN: 0003-6951 column 638 ----	27-29, 55,56
A	SZE S M: "METAL-SEMICONDUCTOR CONTACTS" PHYSICS OF SEMICONDUCTOR DEVICES, NEW YORK, JOHN WILEY & SONS, US, 1981, pages 245-311, XP002068071 ISBN: 0-471-05661-8 page 304 -page 306; figures 43,44 ----	1-61
A	US 4 056 642 A (SAXENA ARJUN N ET AL) 1 November 1977 (1977-11-01) column 5, line 59 -column 6, line 28 ----	1-61
A	PORTER L M ET AL: "A critical review of ohmic and rectifying contacts for silicon carbide" MATERIALS SCIENCE AND ENGINEERING B, ELSEVIER SEQUOIA, LAUSANNE, CH, vol. 34, no. 2, 1 November 1995 (1995-11-01), pages 83-105, XP004000935 ISSN: 0921-5107 page 100, right-hand column -page 102 -----	1-61

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 3983264	A	28-09-1976	NONE		
US 5021365	A	04-06-1991	US	4843450 A	27-06-1989
			EP	0249768 A2	23-12-1987
			JP	62299077 A	26-12-1987
EP 0295490	A	21-12-1988	US	4811077 A	07-03-1989
			DE	3880019 D1	13-05-1993
			DE	3880019 T2	28-10-1993
			EP	0295490 A1	21-12-1988
			JP	1008613 A	12-01-1989
			JP	1977501 C	17-10-1995
			JP	7009914 B	01-02-1995
EP 0789388	A	13-08-1997	JP	2995284 B2	27-12-1999
			JP	9129901 A	16-05-1997
			EP	0789388 A2	13-08-1997
US 4056642	A	01-11-1977	CA	1061915 A1	04-09-1979
			DE	2720893 A1	17-11-1977
			FR	2351500 A1	09-12-1977
			GB	1530237 A	25-10-1978
			JP	52139366 A	21-11-1977
			NL	7705316 A	16-11-1977

Electronic Acknowledgement Receipt

EFS ID:	9745730
Application Number:	13022522
International Application Number:	
Confirmation Number:	6852
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	26263
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-453
Receipt Date:	25-MAR-2011
Filing Date:	07-FEB-2011
Time Stamp:	20:32:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	40003771-0003-453_IDS_State ment_03_25_2011.pdf	203257 eb6d8fa55c30ccb063806dab397c/d59c19 2c1d0	no	2

Warnings:

Information:

2	Information Disclosure Statement (IDS) Filed (SB/08)	40003771-0003-453_IDS_pt_1_ Filed_03_25_2011.pdf	1347958	no	11
			6616c3abf340d70ac6dda00f25ba9a70ec7888c0		
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Filed (SB/08)	40003771-0003-453_IDS_pt_2_ Filed_03_25_2011.pdf	840731	no	5
			0fdcd583426008a41951859cc7686e99a310eb3e		
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
4	NPL Documents	ABERLE_INJECTION- LEVEL_DEPENDENT_SURFACE_ RECOMBINATION.pdf	293308	no	3
			ac4d6b4ffe2f679201fddb9680b0dbc6971a85e		
Warnings:					
Information:					
5	Foreign Reference	EP0295490.pdf	550702	no	11
			6c6c7bb4dd7fb012ac1eae4b707bc68d8315254b		
Warnings:					
Information:					
6	NPL Documents	ZHANG_SCHOTTKY_DIODES_O F_Ni_Au.pdf	384757	no	3
			7efb20e4946f3ff9fb7aed8d19fd0d4d7ad1d5b2		
Warnings:					
Information:					
7	NPL Documents	WEINBERGER_SURFACE- CHEMISTRY-OF_HF.pdf	328710	no	3
			f36b705d6424c35710b9e9a718874ffefee5c9c1		
Warnings:					
Information:					
8	NPL Documents	CHEN_HIGH-QUALITY_NATIVE- OXIDE-FREE.pdf	272322	no	3
			9b7f6f0617de09f4794a6f1fd52d96f5673c7b71		
Warnings:					
Information:					
9	NPL Documents	HUANG_TWO- DIMENSIONAL_NUMERICAL_SI MULATION_OF_SCHOTTKY.pdf	2227083	no	7
			b8c85b967b0aac621b3afe6103de6712dd335d93		
Warnings:					
Information:					

10	NPL Documents	CHADI_FERMI-LEVEL-PINNING_DEFECTS_IN_HIGHLY.pdf	403618	no	4
			7670a986992c2883e6d78921e662502ca5e20375		
Warnings:					
Information:					
11	NPL Documents	YABLONOVITCH_UNUSUALLY_LOW_SURFACE-RECOMBINATION.pdf	279917	no	4
			4ae1c379c538d3c638c5523476796bda611d61a3		
Warnings:					
Information:					
12	NPL Documents	PADOVANI_FORWARD_VOLTAGE-CURRENT_CHARACTERISTICS.pdf	209928	no	2
			67e041be803bf00601158b42aaa9b638eb88ae7e		
Warnings:					
Information:					
13	NPL Documents	ALERS_EFFECT_OF_THERMAL_STABILITY_AND_ROUGHNESS.pdf	214848	no	3
			8562c49693a153b81a03b5bcfeaf81c9b4231aba		
Warnings:					
Information:					
14	NPL Documents	HASEGAWA_UNPINNING_OF_FERMI_LEVEL_IN_NANOMETER-SIZED.pdf	315065	no	5
			75f1ffc06f06c445b21df7ce70eace52bdefcb88		
Warnings:					
Information:					
15	NPL Documents	HEINE_THEORY_OF_SURFACE_STATES.pdf	677692	no	8
			309c896e3e3a379224155f5a188861abc06d2478		
Warnings:					
Information:					
16	NPL Documents	HUANG_METAL_OXIDE_SEMICONDUCTOR_FIELD_EFFECT.pdf	188022	no	2
			7b6bab15ab84875b2f7498a1adb0c685a4adc11		
Warnings:					
Information:					
17	NPL Documents	SHALISH_YELLOW_LUMINESCENCE_AND_FERMI_LEVEL.pdf	311410	no	3
			c04084ea70aec034901400647114f2f5cb6cd524		
Warnings:					
Information:					
18	NPL Documents	INTERNET_RESEARCH_ACHIEVEMENTS.pdf	537914	no	9
			85203707e2cf7b2afd4892d38a95c530295cd0941		
Warnings:					
Information:					

19	NPL Documents	IZUMI_HYDROGEN_TERMINATION.pdf	329881	no	4
			f2b0a3b664deaaebb2002c31dee3b89fe7883641		
Warnings:					
Information:					
20	NPL Documents	HILSENBECK_AGING_BEHAVIOR_OF_AIGaN.pdf	177841	no	2
			d4363829cc508351d2532bcf2c1f2634a8a3832b		
Warnings:					
Information:					
21	NPL Documents	TERSOFF_SCHOTTKY_BARRIER_HEIGHTS_AND_THE_CONTINUUM.pdf	329272	no	4
			859ab132aefa8609e680028596367c095a11d1c2		
Warnings:					
Information:					
22	NPL Documents	PATEL_ARSENIC_ATOM_LOCATION_ON_PASSIVATED.pdf	264009	no	3
			1f3530b0283b1c8e1445855fdb4f1622b6fcfd0a		
Warnings:					
Information:					
23	NPL Documents	NAUKA_SURFACE_PHOTOVOLTAAGE_MEASUREMENT.pdf	344955	no	4
			112a3420b729ddb0a44c5706ef27a867481e769b		
Warnings:					
Information:					
24	NPL Documents	KAMIYAMA_ULTRATHIN_TANTALUM_OXIDE_CAPACITOR.pdf	1152498	no	9
			f7d63de441358613d9dd859b1c25dcecb5f91983		
Warnings:					
Information:					
25	NPL Documents	KIMURA_A_NEW_TYPE_OF_SCHOTTKY_TUNNEL.pdf	176814	no	3
			1b51686e36010bc057a3c60f79e619375b1b256c		
Warnings:					
Information:					
26	NPL Documents	CAI_INVESTIGATION_OF_THE_PROPERTIES_OF_PLASMA-ENHANCED.pdf	1561047	no	5
			4c793b2cd35d9e4898cae0f575d6fe6f71484890		
Warnings:					
Information:					
27	NPL Documents	LEE_ELECTRONIC_PROPERTIES_OF_METALLIC_NANOCLUSTERS.pdf	1391630	no	19
			1270125f5321bad5c243e9073f7bf66203db36f1		
Warnings:					
Information:					

28	NPL Documents	LOUIE_IONICITY_AND_THE_THEORY.pdf	662118	no	9
			f9202c508b52d47094d318ff75d476555027e3a6		
Warnings:					
Information:					
29	NPL Documents	SOBOLEWSKI_PROPERTIES_OF_ULTRATHIN_THERMAL_NITRIDES.pdf	246262	no	3
			32072f2f65852b58dc8aa29434e9ed33739412d6		
Warnings:					
Information:					
30	NPL Documents	MIYAWAKI_IMPROVEMENT_OF_ALUMINUM_Si_CONTACT.pdf	156507	no	3
			83dcf771bc13a128b21f34db7311f12cf064b123		
Warnings:					
Information:					
31	NPL Documents	GILMER_PROCESS_AND_MANUFACTURING_CHALLENGES_FOR.pdf	908341	no	10
			8c1340edb5588af577f625dd67f59276024e3da4		
Warnings:					
Information:					
32	NPL Documents	MANDELIS_EVIDENCE_OF_A_SURFACE_ACCEPTOR_STATE.pdf	366513	no	5
			1c2f2fceb4ce0862d45ef725150d52820c3c395		
Warnings:					
Information:					
33	NPL Documents	NISHIOKA_DIELECTRIC_CHARACTERISTICS.pdf	252338	no	3
			879e7653daeb43267d4b07a0a55608f3843beff3		
Warnings:					
Information:					
34	NPL Documents	OKAMOTO_NEAR-OHMIC_CONTACT_OF_.pdf	339545	no	4
			c4b1fea8296342ba1c9743f2304e3c8951ac2f25		
Warnings:					
Information:					
35	NPL Documents	BAUERNSCHMITT_TRANSITION_FROM_MOS_TO_SCHOTTKY-CONTACT_BEHAVIOUR.pdf	249367	no	4
			ebb0a8bfb3644de3687e3e4722abbc3804d7b9f4		
Warnings:					
Information:					
36	NPL Documents	PORTER_A_CRITICAL_REVIEW_OF_OHMIC_AND_RECTIFYING_CONTACTS.pdf	2176146	no	23
			a76feb3adb9313a883f523df2492f39144834c84		
Warnings:					
Information:					

37	NPL Documents	MCKEE_PHYSICAL_STRUCTURE _AND_INVERSION_CHARGE.pdf	244657 5578be0927dcfb4b02311b08332e84ce5e6 3815d	no	2
Warnings:					
Information:					
38	NPL Documents	BRINGANS_ARSENIC_PASSIVAT ION_OF_Si_and_Ge_SURFACES .pdf	2685615 4f6557f3abd1a8d850a901dc672f38a3ebdf 359a	no	43
Warnings:					
Information:					
39	NPL Documents	DE_ALMEIDA_REACTION- DIFFUSION_MODEL_FOR_THER MAL_GROWTH.pdf	331652 4d3e8cd6c1425b58fec342a01141ad6f5f25 d9ba	no	4
Warnings:					
Information:					
40	NPL Documents	TUNG_ELECTRON_TRANSPORT _OF_INHOMOGENEOUS_SCHOTTKY TTKY.pdf	303603 5c49a3ada3b21b00746bbebda6c493f9012 5b156	no	3
Warnings:					
Information:					
41	NPL Documents	HARA_CONTROL_OF_SCHOTTKY _AND_OHMIC_INTERFACES. pdf	541109 0a58e3573b032056726a0ce94ab4fcdab5 9b462	no	6
Warnings:					
Information:					
42	NPL Documents	HARA_PINNING- CONTROLLED_METAL_SEMICONDUCTOR _INTERFACES.pdf	410860 6e67599eef6606584b6fef915afeb56f9bdb 22e6	no	6
Warnings:					
Information:					
43	NPL Documents	HARA_PINNING- CONTROLLED_OHMIC_CONTACTS.pdf	342900 10eec6e0b5fd731dca75b395a03518927e5 855b3	no	4
Warnings:					
Information:					
44	NPL Documents	VERHAVERBEKE_SURFACE_CH ARACTERISATION_OF_Si_AFTER _HF.pdf	387098 9b1bf55f60f9d547bdae80842f341f37f2b3 fd2	no	5
Warnings:					
Information:					
45	NPL Documents	WOLF_SPINTRONICS.pdf	1273467 7089de1f27e39f22b43112e118bb0ae4acc 8ef24	no	8
Warnings:					
Information:					

46	NPL Documents	SZE_METAL_SEMICONDUCTOR_CONTACTS.pdf	2175850	no	67
			d639cebc8179615dee9882850f5f522de2999892		
Warnings:					
Information:					
47	NPL Documents	SCHMIDT_CARRIER_RECOMBINATION_AT_SILICON-SILICON_NITRIDE.pdf	757499	no	8
			7d14fb1d39424456ae12280ce73ebd22a0341733		
Warnings:					
Information:					
48	NPL Documents	PCT_US03_25054_ISR.pdf	255780	no	6
			d0543dc39bd586d81ab758e9b069abf4b8cabaee		
Warnings:					
Information:					
49	NPL Documents	SHAIK_EXPERIMENTAL_IDENTIFICATION_OF_NITROGEN.pdf	258513	no	3
			4b8613a5cd5c73d3d081269a4f2df3887ac8fbac		
Warnings:					
Information:					
50	NPL Documents	SNYDER_EXPERIMENTAL_INVESTIGATION_OF_A_PtSi_SOURCE.pdf	1371658	no	3
			8bcae4cc59396d38b1880700cb1bbb4ff976fae5		
Warnings:					
Information:					
51	NPL Documents	KAMINS_EFFECT_OF_HYDROGEN_ON_p-TYPE.pdf	207446	no	2
			a9bb220731d170436a93981637fccab7564d1e19		
Warnings:					
Information:					
52	NPL Documents	TERAJI_OHMIC_CONTACTS_TO_n-TYPE.pdf	327550	no	6
			c8c02ab51e175a523cd5bbdda50ff32554e7aeae		
Warnings:					
Information:					
53	NPL Documents	BAUMVOL_ATOMIC_TRANSPORT_DURING_GROWTH.pdf	1160521	no	25
			988f5bc92c8d3d4a6bc65f58d883fd01ea6dd1a52		
Warnings:					
Information:					
54	NPL Documents	SPICER_UNIFIED_MECHANISM_FOR_SCHOTTKY-BARRIER.pdf	335559	no	4
			3cd70610f02402b82072db7e3f979d15634446bf		
Warnings:					
Information:					

55	NPL Documents	WANG_HIGH_BARRIER_HEIGHT_GaN_SCHOTTKY.pdf	202756	no	4
			c7b8488a757ef884b0f5e8c53f923815bd08193d		
Warnings:					
Information:					
56	NPL Documents	WIDJAJA_AB_INITIO_STUDY_OF_ADSORBTION_AND_DECOMPOSITION.pdf	667319	no	7
			a616fbd359f407675a9886d72372bc221b06a4e9		
Warnings:					
Information:					
57	NPL Documents	WRIGHT_HOT-ELECTRON_IMMUNITY.pdf	145589	no	2
			e5443b6be5e005f123fc840ed266b0c5c471b3b		
Warnings:					
Information:					
58	NPL Documents	HAYAFUJI_NITRIDATION_OF_SILICON_AND_OXIDIZED-SILICON.pdf	717000	no	7
			00259459de66874279e90742281299fd4afe795		
Warnings:					
Information:					
59	NPL Documents	KIM_METAL-DEPENDENT_FERMI-LEVEL.pdf	409616	no	5
			ab38cbfedbad315f7d5768e9511515d49d4d22309		
Warnings:					
Information:					
60	NPL Documents	YANG_THE_EFFECTS_OF_INTERFACIAL_SUB-OXIDE.pdf	262934	no	3
			ce33b5daa96ed7b159383a50fdb318a76b5de387		
Warnings:					
Information:					
Total Files Size (in bytes):			36448877		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Daniel E. Grupp

Application No.: 13/022,522

Filed: February 7, 2011

Examiner: Not Yet Assigned

Art Unit: 2811

Docket No.: 40003771-0003-453

Confirmation No.: 6852

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.97

In accordance with the duty of disclosure, enclosed is a copy of IDS Citation Form PTO/SB/08, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g. copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS is being filed before the mailing of a First Office Action. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

Please charge any fees due to Deposit Account 19-3140.

Respectfully submitted,

SNR DENTON US LLP

Date: March 25, 2011

/Tarek N. Fahmi/

Tarek N. Fahmi, Reg. No. 41,402

P.O. Box 061080
Wacker Drive Station, Willis Tower
Chicago, Illinois 60606-1080
(650) 798-0320



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/022,522	02/07/2011	2811	1183	40003771-0003-453	31	4

CONFIRMATION NO. 6852

26263
SNR DENTON US LLP
P.O. BOX 061080
CHICAGO, IL 60606-1080

UPDATED FILING RECEIPT



Date Mailed: 04/07/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Daniel E. Grupp, Palo Alto, CA;
Daniel J. Connelly, Redwood City, CA;

Power of Attorney: The patent practitioners associated with Customer Number 26263

Domestic Priority data as claimed by applicant

This application is a DIV of 12/197,996 08/25/2008 PAT 7,884,003
which is a DIV of 11/181,217 07/13/2005 PAT 7,462,860
which is a CON of 10/217,758 08/12/2002 PAT 7,084,423

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

If Required, Foreign Filing License Granted: 02/16/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/022,522**

Projected Publication Date: 07/14/2011

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Preliminary Class

257

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER**Title 35, United States Code, Section 184****Title 37, Code of Federal Regulations, 5.11 & 5.15****GRANTED**

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where

the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/022,522	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	82		N/A	
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A	270		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	110		N/A	
TOTAL CLAIMS (37 CFR 1.16(j))	36	minus 20 = *	16	x 26 =	416		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4	minus 3 = *	1	x 110 =	110		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					195		
			TOTAL		1183	TOTAL	
* If the difference in column 1 is less than zero, enter "0" in column 2.							
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
				TOTAL ADD'L FEE		TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
				TOTAL ADD'L FEE		TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/022,522	02/07/2011	Daniel E. Grupp	40003771-0003-453

CONFIRMATION NO. 6852

26263
SNR DENTON US LLP
P.O. BOX 061080
CHICAGO, IL 60606-1080

PUBLICATION NOTICE



OC000000048764350

Title:METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Publication No.US-2011-0169124-A1

Publication Date:07/14/2011

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/022,522	02/07/2011	Daniel E. Grupp	40003771-0003-453	6852
26263	7590	10/07/2011	EXAMINER	
SNR DENTON US LLP			HARRISON, MONICA D	
P.O. BOX 061080				
CHICAGO, IL 60606-1080				
			ART UNIT	PAPER NUMBER
			2893	
			MAIL DATE	DELIVERY MODE
			10/07/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	13/022,522	GRUPP ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2893	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 February 2011.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 5) ☒ Claim(s) 1-31 is/are pending in the application.
- 5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☒ Claim(s) 1 and 2 is/are allowed.
- 7) ☒ Claim(s) 3-31 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 07 February 2011 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 12) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) ☒ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>3/25/11</u> . | 6) ☐ Other: ____. |

DETAILED ACTION

Priority

1. This application appears to be a division of Application No. 12/197,996, filed 8/25/08. A later application for a distinct or independent invention, carved out of a pending application and disclosing and claiming only subject matter disclosed in an earlier or parent application is known as a divisional application or "division." The divisional application should set forth the portion of the earlier disclosure that is germane to the invention as claimed in the divisional application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 3, 4, 6, 9, 10, 12, 19, 20, 23, 25 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Miura et al (6,452,244 B1).

2. Regarding claim 3, Miura et al discloses an electrical device, comprising a metal (Figure 1, reference 2); a semiconductor (Figure 1, reference 1); and an interface layer of less than 1 nm thickness disposed between and in contact with both the metal and the semiconductor (Figure 1, reference 3; column 6, lines 47-48), said interface layer configured to adjust a Schottky barrier height of the device, wherein the electrical device has a specific contact resistance of less than or equal to approximately 1000 f-- ,trot".

Art Unit: 2893

4. Regarding claim 4, Miura et al discloses wherein the interface layer includes a passivating material (Figure 1, reference 3; abstract).

5. Regarding claim 6, Miura et al discloses wherein the interface layer consists essentially of a monolayer of the passivating material (Figure 1, reference 3).

6. Regarding claim 9, Miura et al discloses wherein the metal comprises an alloy of a metal (Figure 1, reference 2).

7. Regarding claim 10, Miura et al discloses wherein the interlace layer includes a passivating material (Figure 1, reference 3; abstract).

8. Regarding claim 12, Miura et al discloses wherein the interface layer consists essentially of a monolayer of the passivating material (Figure 1, reference 3).

9. Regarding claim 19, Miura et al discloses wherein the interface layer is configured to adjust the Schottky barrier height by reducing interface charge (column 7, lines 14-40).

10. Regarding claim 20, Miura et al discloses wherein the interface layer includes a passivating material (Figure 1, reference 3; abstract).

11. Regarding claim 23, Miura et al discloses wherein the metal comprises an alloy of a metal (Figure 1, reference 2).

12. Regarding claim 25, Miura et al discloses a method, comprising adjusting a Schottky barrier height of a metal-semiconductor interface in an electrical device by introducing, during fabrication of the electrical device, an interface layer of less than 1 nm thickness between and in contact (Figure 1, reference 3; column 6, lines 47-48) with both a metal (Figure 1,

Art Unit: 2893

reference 2) and a semiconductor (Figure 1, reference 1) to form a metal-interface layer-semiconductor junction (column 7, lines 41-56).

13. Regarding claim 27, Miura et al discloses wherein the interface layer is introduced by deposition during fabrication of the electrical device (Figure 1, reference 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5, 11 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al (6,452,244 B1) in view of Clark (3,513,366).

14. Miura discloses all of the above claimed subject matter. However, Miura et al does not disclose wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide (claims 5, 11 and 21).

Clark discloses wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide (Figure 4, reference 13, oxide).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Miura et al with the teachings of Clark for the purpose of forming a passivating material comprising an oxide in order to minimize interruption in metallization in schottky barrier diodes.

Claims 7, 13, 22 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al (6,452,244 B1) in view of Takiar et al (4,723,197).

Art Unit: 2893

15. Miura et al discloses the above independently claimed subject matter. However, Miura et al does not disclose wherein the interface layer includes a separation layer and a passivating layer (claims 7, 13, 22 and 28).

Takiar et al discloses wherein the interface layer includes a separation layer and a passivating layer (Figure 2, references 16 and 18).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Miura et al with the teachings of Takiar et al, for the purpose of forming a separation and passivating layer in order to provide the necessary dielectric separation between devices in the active region and overlying metallization lines in semiconductor devices.

Claims 8, 14, 24 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al (6,452,244 B1) in view of Takiar et al (4,723,197)

16. Miura et al discloses the above independently claimed subject matter. However, Miura et al does not disclose wherein either or both of the passivating layer and the separation layer comprise a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide (claims 8, 14, 24 and 29).

Takiar et al discloses wherein either or both of the passivating layer and the separation layer comprise a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide (Figure 2, references 16 and 18; column 2, lines 63-68 thru column 3, lines 1-5).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Miura et al with the teachings of Takiar et al, for the purpose of forming a separation and passivating layer consisting of an oxide and nitride in order to provide

Art Unit: 2893

the necessary dielectric separation between devices in the active region and overlying metallization lines in semiconductor devices.

Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al (6,452,244 B1) in view of Ohtsuka et al (5,027,166).

17. Miura et al discloses the above independently claimed subject matter. However, Miura et al does not disclose wherein the interlace layer comprises a metal oxide (claim 15), wherein the interface layer includes a metal oxide (claim 16) nor wherein at least one of the passivating layer and the separation layer is a metal oxide (claim 17).

Ohtsuka et al discloses wherein the interlace layer comprises a metal oxide (column 4, lines 64-67), wherein the interface layer includes a metal oxide (column 4, lines 64-67) and wherein at least one of the passivating layer and the separation layer is a metal oxide (column 4, lines 64-67).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Miura et al with the teachings Ohtsuka et al, for the purpose of forming an interface of a metal oxide in order to be used as reference point in ascertaining schottky barrier height in semiconductor devices.

Claims 18 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al (6,452,244 B1) in view of Tang (6,462,931 B2).

18. Miura et al discloses the above independently claimed subject matter. However, Miura et al does not disclose wherein the interface layer is configured to adjust the Schottky barrier height by reducing or eliminating metal induced gap states (MIGS) (claims 18 and 30).

Art Unit: 2893

Tang discloses wherein the interface layer is configured to adjust the Schottky barrier height by reducing or eliminating metal induced gap states (MIGS) (column 6, lines 42-67).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Miura et al with the teachings of Tang for the purpose of using an interface to cause charge transfer which minimize gaps formed in the metal layers in semiconductor devices.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al (6,452,244 B1) in view of Liu et al (6,293,137).

19. Miura et al discloses the above independently claimed subject matter. However, Miura et al does not disclose wherein the interface layer is configured to affect electrical dipoles between the metal and the semiconductor and thereby adjust the Schottky barrier height (claim 26).

Liu et al discloses wherein the interface layer is configured to affect electrical dipoles between the metal and the semiconductor and thereby adjust the Schottky barrier height (column 4, lines 18-30).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Miura et al with the teachings of Liu et al, for the purpose of forming a dipole layer which will change the equilibrium of original charge distribution and reach a new one. The new equilibrium reduces the width of the depletion region of the semiconductor thereby reducing the Schottky barrier height in semiconductor devices.

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miura et al (6,452,244 B1) in view of Koeneke et al (4,485,550).

20. Regarding claim 31, Miura et al discloses a method, comprising forming, an interface layer of less than 1 nm thickness (Figure 1, reference 3). However, Miura et al does not disclose a semiconductor channel surface (),and subsequently depositing a metal source/drain adjacent and in contact with the interface layer, wherein said metal is deposited in a noninvasive fashion so as not to disrupt passivation properties of the interface layer and said interlace layer is configured to adjust a Schottky barrier height of a metal-semiconductor interface which would exist if the interface layer were not present.

Koencke et al discloses a semiconductor channel surface (Figure 8, between references 35 and 36, below reference 21), interface and subsequently depositing a metal source/drain adjacent and in contact with the interface layer (Figure 8, between references 21 and 20), wherein said metal is deposited in a noninvasive fashion so as not to disrupt passivation properties of the interface layer (Figure 8, reference 34) and said interface layer is configured to adjust a Schottky barrier height of a metal-semiconductor interface which would exist if the interface layer were not present (column 6, lines 5-42).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Miura et al with the teachings of Koencke et al , for the purpose of forming metal source and drain regions in a semiconductor substrate in order to result in a silicide to channel schottky barrier which minimizes current leakage in semiconductor devices.

Claim Objections

21. Claims 10, 13 and 20-24 are objected to because of the following informalities:
Claims 10 and 13 both refer to an interface which is not claimed in claim 9 from which both

Art Unit: 2893

claims 10 and 13 depend from. Also claims 20-24 are improper depending claims. Appropriate correction is required.

Allowable Subject Matter

22. Claims 1 and 2 are allowed over the prior art of record.

Reasons for Allowance

23. The following is an examiner's statement of reasons for allowance: The prior art does not disclose nor fairly suggest a method comprising cleaning a substrate and removing the substrate from the solution and blow-drying the substrate with nitrogen, thereby forming an interface layer containing hydrogen and fluorine on the semiconductor substrate, said interface layer being of sufficient thickness to passivate a surface of said semiconductor substrate in a vicinity of said interface layer as described in independent claim 1 and in the context of its recited process along with its depending claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is (571)272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

Art Unit: 2893

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Monica D. Harrison/
Examiner, Art Unit 2893

mdh
September 28, 2011

Notice of References Cited	Application/Control No. 13/022,522		Applicant(s)/Patent Under Reexamination GRUPP ET AL.	
	Examiner Monica D. Harrison		Art Unit 2893	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,452,244 B1	09-2002	Miura et al.	257/471
*	B	US-3,513,366	05-1970	CLARK LOWELL E	257/484
*	C	US-4,723,197	02-1988	Takiar et al.	361/771
*	D	US-6,293,137	09-2001	Liu et al.	73/31.06
*	E	US-6,462,931 B2	10-2002	Tang et al.	361/305
*	F	US-4,485,550	12-1984	Koeneke et al.	438/233
*	G	US-5,027,166	06-1991	Ohtsuka et al.	257/486
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 13022522	Applicant(s)/Patent Under Reexamination GRUPP ET AL.
	Examiner MONICA D HARRISON	Art Unit 2893

SEARCHED			
Class	Subclass	Date	Examiner
257	486,571,E21.192,E29.148	9/28/11	MDH

SEARCH NOTES		
Search Notes	Date	Examiner
East (USPAT, US-PGPUB, USOCR, EPO, JPO, DERWENT, IBM_TDB, FPRS)	9/28/11	MDH

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

/MONICA D HARRISON/ Examiner.Art Unit 2893	
---	--



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 6852

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
13/022,522	02/07/2011	438	2893	40003771-0003-453		
RULE						
APPLICANTS Daniel E. Grupp, Palo Alto, CA; MDH 9/28/11 Daniel J. Connelly, Redwood City, CA;						
** CONTINUING DATA ***** This application is a DIV of 12/197,996 08/25/2008 PAT 7,884,003 which is a DIV of 11/181,217 07/13/2005 PAT 7,462,860 MDH 9/28/11 which is a CON of 10/217,758 08/12/2002 PAT 7,084,423						
** FOREIGN APPLICATIONS ***** none MDH 9/28/11						
** IF REQUIRED, FOREIGN FILING LICENSE GRANTED *** SMALL ENTITY ** 02/16/2011						
Foreign Priority claimed	☐ Yes ☒ No	☐ Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	☐ Yes ☒ No		CA	6	31	4
Verified and	/MONICA D HARRISON/	Initials				
Acknowledged	Examiner's Signature					
ADDRESS SNR DENTON US LLP P.O. BOX 061080 CHICAGO, IL 60606-1080 UNITED STATES						
TITLE METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS						
FILING FEE RECEIVED 1183	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees		
				☐ 1.16 Fees (Filing)		
				☐ 1.17 Fees (Processing Ext. of time)		
				☐ 1.18 Fees (Issue)		
				☐ Other _____		
			☐ Credit			

Receipt date: 03/25/2011

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

13022522 - GAI: 2893

P10/05/05a (01-10)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522
	Filing Date		2011-02-07
	First Named Inventor	Daniel E. Grupp	
	Art Unit	2811	
	Examiner Name		
	Attorney Docket Number	40003771-0003-453	

U.S. PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
/M.D.H./	1	3590471		1971-07-06	Lepselter, et al.	
	2	3708360		1973-01-02	Wakefield, Jr., et al.	
	3	3983264		1976-09-28	Schroen, Walter H., et al.	
	4	4056642		1977-11-01	Saxena, Arjun N. et al.	
	5	4300152		1981-11-10	Lepselter	
	6	4485550		1984-12-04	Koeneke, et al.	
	7	5021365		1991-06-04	Kirchner, et al.	
	8	5399206		1995-03-21	de Lyon	

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2893
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit		2811	
	Examiner Name			
	Attorney Docket Number		40003771-0003-453	

/M.D.H./	9	5578848		1996-11-26	Kwong, et al.	
	10	5596218		2009-04-10	Soleimani, et al.	
	11	5612567		1997-03-18	Baliga	
	12	5663584		1997-09-02	Welch	
	13	5801398		1998-09-01	Hebiguchi	
	14	5888891		1999-03-30	Gould	
	15	5939763		1999-08-17	Hao, et al.	
	16	6037605		2000-03-14	Yoshimura	
	17	6096590		2000-08-01	Chan, et al.	
	18	6150286		2000-11-21	Sun et al.	
	19	6198113		2001-03-06	Grupp, Daniel E.	

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2893
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit		2811	
	Examiner Name			
	Attorney Docket Number		40003771-0003-453	

/M.D.H./	20	6207976		2001-03-27	Takshashi et al.	
	21	6261932		2001-07-17	Hulfachor	
	22	6291866		2001-09-18	Wallace et al.	
	23	6291867		2001-09-18	Wallace et al.	
	24	6303479		2001-10-16	Snyder	
	25	7084423		2006-08-01	Grupp et al.	
	26	5801444		1998-09-01	Aboelfotoh et al.	
	27	7176483		2007-02-13	Grupp et al.	

If you wish to add additional U.S. Patent citation information please click the Add button.

Add

U.S.PATENT APPLICATION PUBLICATIONS

Remove

Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/M.D.H./	1	20030121468		2003-07-03	Boone et al.	

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2893
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./	2	20040026687		2004-02-12	Grupp et al.	
/M.D.H./	3	20050093027		2005-05-05	Grupp et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
/M.D.H./	1	0295490	EP		1988-12-21	Fowler, Alan B. et al.		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button.

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
/M.D.H./	1	ABERLE, ARMIN G., et al., "Injection-Level Dependent Surface Recombination Velocities at The Silicon-Plasma Silicon Nitride Interface", Institut fur Solaernergieforchung, ISFH, D-3 1860 Emmerthal, Germany, (3/9/95), pp. 2828-2830	☐
	2	B. J. ZHANG, et al., "Schottky Diodes of Ni/Au on n-GaN Grown on Sapphire and SiC Substrates", Applied Physics Letters, Vol. 79, No. 16, (10/15/01), pp. 2567-2569	☐
	3	B.R. WEINBERGER, et al., "Surface Chemistry of HF Passivation Silicon: X-Ray Photoelectron And Ion Scattering Spectroscopy Results", J. Appl. Phys. 60(9), (11/186), pp. 3232-3234	☐
	4	C.L. CHEN, et al., "High Quality Native-Oxide-Free Ultrathin Oxide Grown by In-Situ HF-Vapor Treatment", Electronic Letters, Vol. 36, No. 11, (5/25/00), pp. 981-983	☐

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2893
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./	5	CHUNG-KUANG, HUANG , et al., "Two-Dimensional Numerical Simulation of Schottky Barrier MOSFET with Channel Length to 10 nm", IEEE, pp. 842-848	☐
	6	D. J. CHADI, et al., "Fermi-Level-Pinning Defects in Highly n-Doped Silicon", Physical Review Letters, Vol. 79, No. 24, NEC Research Institute, Princeton New Jersey 08540-6634, (12/97),pp. 4834-4837	☐
	7	E. YABLONOVITCH, et al., "Unusually Low Surface-Recombination Velocity on Silicon and Germanium Surfaces", Physical Review Letters, Vol. 57, No. 2, (7/14/86),pp. 249-252	☐
	8	F. A. PADOVANI, "Forward Voltage-Current Characteristics of Metal-Silicon Schottky Barriers", Texas Instruments, Inc., Dallas Texas, (9/15/66),pp. 892-892	☐
	9	G.B. AKERS, et al., "Effects of Thermal Stability and Roughness on Electrical Properties of Tantalus Oxide Gates", Mat. Res., Soc. Symp. Proc., Vol. 567, Materials Research Society, (1999),pp. 391-395	☐
	10	HASEGAWA, HIDEKI , et al., "Upping of Fermi Level in Nanometer-Sized Schottky Contacts on GaAs and InP", Reseach Center For Interface Quantum Electronics And Graduate School of Electronics And Info. Eng, Hokkaido Univ, Japan, (2000),pp. 92-96	☐
	11	HEINE, VOLKER , "Theory of Surface States", Physical Review Letters, Vol. 138, No. 6A, Tell Telephone Lab., Murphy Jill, New Jersey, (6/4/65),	☐
	12	HUANG, FENG-JUNG , "Metal-Oxide Semiconductor Field-Effect Transistors Using Schottky Barrier Drains", Electronics Letters, Vol. 33, No. 15, (7/17/97),pp. 1341-1342	☐
	13	I. SHALISH, et al., "Yellow Luminescence And Fermi Level Pinning in GaN Layers", American Institute of Physics, Vol. 77, No. 7, (8/14/00),pp. 987-989	☐
	14	INTERNET, http://www.rciqe.hokudai.ac.jp/RCIQEold/ResearchAchievements.html , downloaded (4/12/02),	☐
	15	IZUMI, HIROT , et al., "43 Hydrogen Termination: The Ideally Finished Silicon Surface", Ultraclean Surface Processing of Silicon Wafers: Secrets of Vlsi Manufacturing http://halloftechnology.com/electrical_optical/986.shtml , (11/98),	☐

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2893
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./	16	J. HILSENBECK, et al., "Aging Behavior of AlGaIn/GaN HFETs With Advanced Ohmic And Schottky Contacts", Electronic letters, Vol. 36, No. 11, (5/25/00),pp. 980-981	☐
	17	J. TERSOFF, "Schottky Barrier Heights and The Continuum of Gap States", Physical Review Letters, Vol. 52, No. 6, AT&T Bell Lab., Murphy Hill, New Jersey 07974, (2/6/84),	☐
	18	J.R. PATEL, et al., "Arsenic Atom Location on Passive Silicon (111) Surfaces", Physical Review B. Vol. 36, No. 14, (11/15/87),pp. 7715-7717	☐
	19	K. NAUKA, et al., "Surface Photovoltage Measurement of Hydrogen-Treated Si Surfaces", Journal of Electrochemical Society 146(1), (1999),pp. 292-295	☐
	20	KAMIYAMA, SATOSHI, et al., "Ultrathin Tantalum Oxide Capacitor Dielectric Layers Fabricated Using Rapid Thermal Nitridation Prior to Low Pressure Chemical Vapor Deposition", J. Electrochem Soc., Vol. 140, No. 6, The Electrochemical Society, Inc., (6/6/93),pp. 1617	☐
	21	KIMURA, MITSUTERU, et al., "A New Type of Schottky Tunnel Transistor", IEEE Electron Device Letters, Vol. 15, No. 10, (10/94),pp. 412-41	☐
	22	L. CAI, et al., "Investigation of The Properties of Plasma-Enhanced Chemical Vapor Deposition Silicon Nitride And its Effect on Silicon Surface Passivation", Journal of Applied Physics, Vol. 83, No. 11, (6/1/98),pp. 5885-5889	☐
	23	LEE, TAKHEE, et al., "Electronic Property of Metallic Nanoclusters on Semiconductor Surfaces: Implications For Nanoelectronic Device Applications", Journal of Nanoparticle Research 2, (2000),pp. 345-362	☐
	24	LOUIE, STEVEN G., et al., "Ionicity And The Theory of Schottky Barriers", Physical Review Letters, Vol. 15, No. 4, Dept. of Phys. Univ. of California, and Materials and Molecular Research Div., Lawrence Berkeley Lab., Berkeley, CA 94720,	☐
	25	M. A. SOBOLEWSKI, et al., "Properties of Ultrathin Thermal Nitrides in Silicon Schottky Barrier Structures", Applied Physics Letters, American Institute of Physics, Vol 54, No. 7, (2/13/89),pp. 638-640	☐
↓	26	M. MIYAWAKI, et al., "Improvement of Aluminum-Si Contact Performance in Native-Oxide-Free Processing", IEEE Electron Device Letters, Vol. 11, No. 10, (10/90),pp. 448-450	☐

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2893
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./	27	M.C. GILMER, et al., "Process and Manufacturing Challenges For High-K Gate Stack Systems", Mat. Res. Soc. Symp. Proc. Vol. 567, (1999),pp. 323-341	☐
	28	MANDELIS, ANDREAS , et al., "Evidence of a Surface Acceptor State in Undoped Semi-Insulating GaAs by Photothermal Radiometric Deep Level Transient Spectroscopy", Sociedad Mexicana de Ciencias de Superficies y de Vacio, (1999),pp. 13-17	☐
	29	NISHIOKA, YASUSHIRO , et al., "Dielectric Characteristics of Fluorinated Ultradry SiO2", Appl. Phy. Letters 54(12), (3/20/89),pp. 1127-112	☐
	30	OKAMOTO, NAOYA , et al., "Near-Ohmic Contact of n-GaAs with Ga/Ga/GaAs Quasi-Metal-Insulator-Semiconductor Structure", Jpn. J. Appl. Phys., Vol. 37, (1998),pp. 32483251	☐
	31	P. BAUERNSCHMITT, et al., "Yb-SiO2-Si Tunneling Junctions", Elsevier Publishers B.V., (1993),pp. 105-108	☐
	32	PORTER, LISA M., et al., "A Critical Review of Ohmic and Rectifying Contacts For Silicon Carbide", Material Science and Engineering, Vol. 34, No. 2, (11/1/95),pp. 83-105	☐
	33	R.A. MCKEE, et al., "Physical Structure And Inversion Charge at a Semiconductor Interface With a Crystalline Oxide", www.sciencemag.org, Vol. 293, (7/20/01),pp. 468-469	☐
	34	R.D. BRINGANS, "Arsenic Passivation of Si and Ge Surfaces", Critical Reviews in Solid State and Materials Sciences, 17(4): 353-395, (1992),pp. 353-395	☐
	35	R.M.C. DE ALMEIDA, et al., "Reaction-Diffusion Model For Thermal Growth of Silicon Nitride Films on Si", Physical Review B, Vol. 62, No. 24, (12/1500),pp. R16 255-R16 258	☐
	36	R.T. TUNG, "Electron Transport of Inhomogeneous Schottky Barriers", AT&T Bell Lab., Murray Hill, New Jersey 07974, (3/21/91),pp. 3832-3834	☐
↓	37	S. HARA, et al., "Control of Schottky And Ohmic Interfaces by Unpinning Fermi Level", Elsevier Science B.V., pp. 394-399	☐

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2893
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./	38	S. HARA, et al., "Pinning-Controlled Metal/Semiconductor Interfaces", Electrotechnical Laboratory, pp. 802-807	☐
	39	S. HARA, et al., "Pinning-Controlled Ohmic Contacts: Application to SiC(0001)", Elsevier Science B.V., pp. 218-221	☐
	40	S. VERHAVERBEKE, et al., "Surface Characterization of Si After HF Treatments and its Influence in the Dielectric Breakdown of Thermal Oxides", Research Aspirant of the Belgium National Fund for Scientific Research; Mat. Res. Soc. Symp. Proc., Vol. 259, Material Research Society, (1992),pp. 391-399	☐
	41	S.A. WOLF, et al., "Spintronics: A Spin-Based Vision For The Future", www.sciencemag.or, Vol.294, (11/6/01),pp. 1488	☐
	42	S.M. SZE, "Metal-Semiconductor Contacts", Physics of Semiconductor Devices, John Wiley & Sons, (1981),	☐
	43	SCHMIDT, JAN , et al., "Carrier Recombination at Silicon-Silicon Nitride Interfaces Fabricated by Plasma-Enhanced Chemical Vapor Deposition", Journal of Applied Physics, Vol. 85, No. 7, (4/1/99),pp. 3626-3633	☐
	44	ACORN TECHNOLOGIES, INC. PCT/US03/25054 filed 08 August 2003, International Search Report, International Searching Authority/US, (12/3/03),pp. 6	☐
	45	SHAIK, LAHIR , et al., "Experimental Identification of Nitrogen-Vacancy Complexes in Nitrogen Implanted Silicon", Applied Physics Letters, Vol. 79, No. 5, (7/30/01),pp. 623-625	☐
	46	SNYDER, JOHN P., et al., "Experimental Investigation of a PtSi Source And Drain Field Emission Transister", American Institute of Physics, pp. 1-3	☐
	47	T.I. KAMINS, et al., "Effect of Hydrogen on p-Type Epitaxial Silicon Sheet-Resistance Measurements", Electrochemical and Solid-State Letters 1(2), (1998),pp. 100-101	☐
↓	48	TERAJI, TOKUYUKI , et al., "Ohmic Contacts To n-Type 6H-SiC Without Post-Annealing", Material Research Society Symposium Proceeding, (4/8/96),pp. 149-154	☐

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2893
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./	49	U.J.R. BAUMVOL, "Atomic Transport During Growth of Ultrathin Dielectrics on Silicon", Surface Science Reports 36, (1999),pp. 1-166	☐
/M.D.H./	50	W.E. SPICER, et al., "Unified Mechanism For Schottky-Barrier Formation And III-V Oxide Interface States", Physical Review Letters, Vol. 44, No. 6, Stanford Electronics Lab., Stanford Univ., Stanford, CA 94305, (2/11/80),pp. 420-423	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/Monica D. Harrison/	Date Considered	09/27/2011
--------------------	----------------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	98	257/486,571,E21.192,E29.148.ccls. and (source drain) with interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:12
L2	48	257/486,571,E21.192,E29.148.ccls. and (source drain) with interface and (interface with metal) and (interface with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:19
L3	44	257/486,571,E21.192,E29.148.ccls. and (source drain) with interface and (interface with metal) and (interface with semiconductor) and schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:19
L6	2	"6462931".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:34
L7	3	"4723197".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:35
L8	2	"5027166".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:49
L9	2	"6293137".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 14:11
S1	1	13/022522	US-PGPUB;	OR	ON	2011/09/26

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			15:58
S2	2	"7884003".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 15:59
S3	2	"7462860".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:02
S4	2	"7084423".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:03
S5	1157	257/486,571,E21.192,E29.148.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:06
S6	465	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:06
S7	173	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier) with height	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:06
S8	84	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier) with height and (interface with metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:06
S9	68	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier) with height and (interface with metal) and (interface with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2011/09/26 16:07

			IBM_TDB			
S10	21	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier) with height and (interface with metal) and (interface with semiconductor) and (metal near interface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:07
S11	15	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier) with height and (interface with metal) and (interface with semiconductor) and (metal near interface) and (semiconductor near junction) with metal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:08
S12	28	257/486,571,E21.192,E29.148.ccls. and (interface near4 passivat\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:49
S13	15	257/486,571,E21.192,E29.148.ccls. and (interface near4 passivat\$4) and (interface near4 separat\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:50
S14	1	257/486,571,E21.192,E29.148.ccls. and (dual with passivat\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:52
S15	1	257/486,571,E21.192,E29.148.ccls. and (lower or bottom or below) near passivat\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:53
S16	809	257/'\$.ccls. and (lower or bottom or below) near passivat\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:53
S17	257	257/'\$.ccls. and (lower or bottom or below) near passivat\$4 and (upper or top or above) near passivat\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:53
S18	133	257/'\$.ccls. and (lower or bottom or below) near passivat\$4 and (upper or top or above) near passivat\$4 and (passivat\$4 with metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2011/09/27 14:54

			JPO; DERWENT; IBM_TDB			
S19	89	257/'\$.ccls. and (lower or bottom or below) near passivat\$4 and (upper or top or above) near passivat\$4 and (passivat\$4 with metal) and (passivat\$4 with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:54
S20	5	257/'\$.ccls. and (lower or bottom or below) near passivat\$4 and (upper or top or above) near passivat\$4 and (passivat\$4 with metal) and (passivat\$4 with semiconductor) and schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:55
S21	18	257/486,571,E21.192,E29.148.ccls. and (constant with resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:03
S22	5	257/486,571,E21.192,E29.148.ccls. and (constant near3 resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:04
S23	28	257/486,571,E21.192,E29.148.ccls. and (interface near3 passivat\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:14
S24	6	257/486,571,E21.192,E29.148.ccls. and (interface near3 (metal near oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:20
S25	0	257/486,571,E21.192,E29.148.ccls. and migd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:25
S26	12	257/486,571,E21.192,E29.148.ccls. and "MIGS"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:25
S27	94	257/'\$.ccls. and "MIGS"	US-PGPUB; USPAT;	OR	ON	2011/09/27 15:25

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S28	98	257/'\$.ccls. and ("MIGS" or (metal near induced near gap))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:27
S29	34	257/'\$.ccls. and (metal near induced near gap)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:27
S30	31715	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 11:58
S31	5316	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 11:59
S32	0	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and ((hydrogen and fluorine) near ion) with weight	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:00
S33	0	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (((hydrogen and fluorine) near ion) with weight)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:00
S34	4	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (blow near dry)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:02
S35	0	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (blow near dry) and (immers\$4 with (substrate or wafer or carrier or base or plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:02

S36	14	(substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (blow near dry) and (immers\$4 with (substrate or wafer or carrier or base or plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:03
S37	9	(substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (blow near dry) and (immers\$4 with (substrate or wafer or carrier or base or plate)) and metal and semiconductor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:04
S38	0	(substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (blow near dry) and (immers\$4 with (substrate or wafer or carrier or base or plate)) and metal and semiconductor and junction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:04
S39	2	"6293197".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:09
S40	15	257/486,571,E21.192,E29.148.ccls. and dipole	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:11
S41	2	257/486,571,E21.192,E29.148.ccls. and (dipole with metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:12
S42	2	257/486,571,E21.192,E29.148.ccls. and (dipole with metal) and (dipole with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:12
S43	67	257/'\$.ccls. and (dipole with metal) and (dipole with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:12

EAST Search History (I nterference)

< This search history is empty >

9/ 28/ 2011 2:44:32 PM

C:\Users\mharrison1\Documents\EAST\Workspaces\13022522.wsp

<i>Index of Claims</i> 	Application/Control No. 13022522	Applicant(s)/Patent Under Reexamination GRUPP ET AL.
	Examiner MONICA D HARRISON	Art Unit 2893

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	09/28/2011							
	1	=							
	2	=							
	3	✓							
	4	✓							
	5	✓							
	6	✓							
	7	✓							
	8	✓							
	9	✓							
	10	✓							
	11	✓							
	12	✓							
	13	✓							
	14	✓							
	15	✓							
	16	✓							
	17	✓							
	18	✓							
	19	✓							
	20	✓							
	21	✓							
	22	✓							
	23	✓							
	24	✓							
	25	✓							
	26	✓							
	27	✓							
	28	✓							
	29	✓							
	30	✓							
	31	✓							

Receipt date: 03/25/2011

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

13022522 - GALL: 2893

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

U.S.PATENTS							Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1						

If you wish to add additional U.S. Patent citation information please click the Add button.

Add

U.S.PATENT APPLICATION PUBLICATIONS							Remove
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1						

If you wish to add additional U.S. Published Application citation information please click the Add button.

Add

FOREIGN PATENT DOCUMENTS								Remove
Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

Add

NON-PATENT LITERATURE DOCUMENTS				Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵	

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2893
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./	1	WANG, LIE , et al., "High Barrier GaN Schottky Diodes: Pt/GaN and Pd/GaN", Dept. of Electrical Eng., Univ. of Minnesota, Minneapolis, Minnesota 55455; Appl. Phys. Letters, Vol. 68(9), (2/26/96),pp. 1267-1270	☐
	2	WIDJAJA, YUNIARTO , et al., "Ab Initio Study and Decomposition of NH3 on Si(100)-(2x1)", J. Phy. Chem B, (2000), pp. 2527-2533	☐
	3	WRIGHT, PETER J., et al., "Hot-Electron Immunity of SiO2 Dielectrics with Fluorine Incorporation", IEEE Electron Device Letters, Vol. 10, No. 8, (8/8/89),pp. 347-348	☐
	4	Y. HAYAFUJI, et al., "Nitridation of Silicon and Oxidized-Silicon", Sony Corp. Research Center, 174 Fujitsuka-Cho, Hodogaya-Ku, Yokohama, 240 Japan; J. Electrochem. Soc.: Solid State Science and Technology, (9/82),	☐
	5	Y. K. KIM, et al., "Metal-Dependent Fermi-Level Movement in The Metal/Sulfur-Passivated InGaP Contact", J. Vac Sci. Technology A 15(3), (1997),pp. 1124-1128	☐
	6	YANG, HANYANG , et al., "The Effects of Interfacial Sub-Oxide Transition Regions and Monolayer Level Nitridation on Tunneling Currents in Silicon Devices", IEEE Electron Device Letters, Vol. 21, No. 2, (2/2/00),pp. 76-78	☐
	7	BLOSSE, A., et al., "A Novel Low Cost 65nm CMOS Process Architecture With Self Aligned Isolation and W Cladded Source/Drain", IEEE, Transactions of 2004 International Electron Device Meeting, pp. 669-672	☐
	8	CONNELLY, DANIEL, et al., "Optimizing Schottky S/D Offset for 25-nm Dual-Gate CMOS Performance", IEEE Trans. Electron Devices, Vol. 47 No. 5, (2003), pp. 1028-1034	☐
	9	EDELSTEIN, D., et al., "Full Copper Wiring in a Sub-0.25 mm CMOS ULSI Technology", Proceedings of the IEEE International Electron Device Meeting, (12/1997), pp. 773-776	☐
	10	GOPALAKRISHNAN, KAILASH, et al., "Impact Ionization MOS (I-MOS)-Part I: Device and Circuit Simulations", IEEE Transactions Electron Devices, Vol. 52, No. 1, (2005), pp. 69-76	☐
↓	11	KEDZIERSKI, JAKUB, et al., "Extension and Source/Drain Design for High-Performance FinFET Devices", IEEE Trans. Electron Devices, Vol. 50, No. 4, (4/2003), pp. 952-958	☐

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2893
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./ 	12	THOMPSON, SCOTT E., et al., "A Logic Nanotechnology Featuring Strained-Silicon", IEEE Electron Device Letters, Vol. 25, No. 4, (2004), pp. 191-193	☐
	13	WEI, C.S., et al., "The Use of Selective Electroless Metal Deposition For Micron Size Contact Fill", IEEE International Electron Device Meeting Technical Digest, (1988), pp. 446-449	☐
	14	YAGISHITA, ATSUSHI, et al., "High Performance Damascene Metal Gate MOSFET's for 0.1 mm Regime", IEEE Trans. Electron Devices, Vol. 47, No. 5, (2000), pp. 1028-1034	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/Monica D. Harrison/	Date Considered	09/27/2011
--------------------	----------------------	-----------------	------------

***EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First named inventor: Daniel E. Grupp

Application No.: 13/022,522

Filed: February 7, 2011

Examiner: Harrison, Monica D.

Art Unit: 2893

Docket No.: 40003771-0003-453

Confirmation No.: 6852

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Madam:

In response to the Office Action dated October 7, 2011, reconsideration of the above-indicated application is respectfully requested in light of the following amendments and remarks.

REMARKS

Reconsideration of this application in light of the preceding amendments is respectfully requested.

With regard to the statement in the Office Action concerning "Priority", it is not required that a divisional application, such as the instant application, be redacted to include only that disclosure which is germane to the claimed subject matter.

Allowance of claims 1 and 2 is noted with appreciation. The claims have been amended to recite the subject matter indicated as being allowable.

Please charge any shortages and credit any overages to Deposit Account No. 19-3140. Any necessary extension of time for response not already requested is hereby requested. Please charge any corresponding fee to Deposit Account No. 19-3140.

Respectfully submitted,
SNR Denton US LLP

Date: January 23, 2012

/Tarek N. Fahmi/

Tarek N. Fahmi
Reg. No. 41,402

P.O. Box 061080
Wacker Drive Station, Willis Tower
Chicago, Illinois 60606-1080
650-798-0320

Electronic Patent Application Fee Transmittal

Application Number:	13022522			
Filing Date:	07-Feb-2011			
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS			
First Named Inventor/Applicant Name:	Daniel E. Grupp			
Filer:	Tarek N. Fahmi			
Attorney Docket Number:	40003771-0003-453			
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with \$0 paid	2251	1	75	75

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				75

Electronic Acknowledgement Receipt

EFS ID:	11897428
Application Number:	13022522
International Application Number:	
Confirmation Number:	6852
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	26263
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-453
Receipt Date:	23-JAN-2012
Filing Date:	07-FEB-2011
Time Stamp:	15:41:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$75
RAM confirmation Number	2388
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
-----------------	----------------------	-----------	-------------------------------------	------------------	------------------

1	Extension of Time	40003771-0003-453_EOT_Filed _01_23_2012.pdf	102809 7a4604d129eea9c581943e94c5db70a124ba5c94	no	1
Warnings:					
Information:					
2		40003771-0003-453_ROA_Filed _01_23_2012.pdf	213201 dcf6bb2cdd9eae653f0c59e2877324993ed66432	yes	3
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	2	
	Applicant Arguments/Remarks Made in an Amendment		3	3	
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30059 069d5c4932307017ce791437de059b578d737ea0	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			346069		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First named inventor: Daniel E. Grupp

Application No.: 13/022,522

Filed: February 7, 2011

Examiner: Harrison, Monica D.

Art Unit: 2893

Docket No.: 40003771-0003-453

Confirmation No.: 6852

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

PETITION FOR EXTENSION OF TIME PURSUANT TO 37 C.F.R. § 1.136(a)

Sir:

In accordance with 37 C.F.R. § 1.136(a), Applicants for the above-identified application respectfully request a one (1) month extension of time, extending the period for response to January 23, 2012 from the Non Final Office Action mailed October 7, 2011. The Petition filing fee of \$75.00 and a response are attached.

If it should be determined that a longer extension of time is required to prevent this application from being abandoned, please charge Deposit Account No. 19-3140.

Respectfully submitted,

SNR DENTON US LLP

Date: January 23, 2012

/Tarek N. Fahmi/

Tarek N. Fahmi

Reg. No. 41,402

P.O. Box 061080

Wacker Drive Station, Willis Tower

Chicago, Illinois 60606-1080

(650) 798.0320

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/022,522		Filing Date 02/07/2011		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☒ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(j))	minus 20 =	*	X \$	=	OR	X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=		X \$	=			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	01/23/2012	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 2	Minus	** 36	= 0	X \$30 =	0	OR	X \$ =	
	Independent (37 CFR 1.16(h))	* 1	Minus	***4	= 0	X \$125 =	0	OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/TAMARA DARKO/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

AMENDMENTS TO THE CLAIMS

The following listing of the claims shall replace all previous versions thereof.

1. (Original) A method, comprising cleaning a semiconductor substrate with a cleaning solution to form a cleaned substrate; immersing, for a period of time between several seconds and approximately five (5) minutes, the cleaned substrate in a solution containing hydrogen and fluorine ions of between approximately 1%-50% by weight; removing the substrate from the solution and blow-drying the substrate with nitrogen, thereby forming an interface layer containing hydrogen and fluorine on the semiconductor substrate, said interface layer being of sufficient thickness to passivate a surface of said semiconductor substrate in a vicinity of said interface layer; subsequently depositing a metal layer over the interface layer, thereby forming a junction having a metal layer disposed over the interface layer disposed over the semiconductor, said junction having a specific contact resistance of less than or equal to approximately $1000 \Omega\text{-}\mu\text{m}^2$.
2. (Original) The method of claim 1, wherein following removal of the substrate from the solution and prior to blow-drying the substrate with nitrogen, rinsing the substrate in deionized water for less than 30 sec.
- 3 - 31. (cancelled)

**REVOCATION OF PREVIOUS POWERS OF ATTORNEY WITH NEW
GENERAL POWER OF ATTORNEY TO PROSECUTE APPLICATIONS AND REEXAMINATION
PROCEEDINGS BEFORE THE UNITED STATES PATENT AND TRADEMARK OFFICE**

I hereby revoke all previous powers of attorney given in the application(s), reexamination proceeding(s) and/or patent(s) listed below and appoint:

Practitioners associated with the Customer Number

27571

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications and reexamination proceedings assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application(s), reexamination proceeding(s) and/or patent(s) listed below to the address associated with Customer Number 27571.

Assignee Name and Address:

Acom Technologies, Inc.
1200 Prospect Street, Suite 475
La Jolla, California 92037

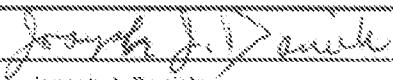
A statement under 37 CFR 3.73(b) is attached.

List of application(s), reexamination proceeding(s) and/or patent(s):

See Attached List

SIGNATURE OF ASSIGNEE OF RECORD

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date:	3/14/2012
Name	Joseph J. Daniele	Telephone:	858-551-1552
Title	Chief Operating Officer		

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Acorn Technologies, Inc.

States that it is:

1. ☒ The assignee of the entire right, title, and interest, or
2. ☐ an assignee of less than the entire right, title and interest
(The extent (by percentage) of its ownership interest is: _____ %)

in the patent applications/patents identified in the attached spreadsheet by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent applications/patents identified in the attached spreadsheet. The assignment was recorded in the United States Patent and Trademark Office at the Reel and Frame listed thereon.

OR

B. ☐ A chain of title from the inventor(s) of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark office at
Reel _____, Frame _____, or for which a copy thereof is attached.
2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark office at
Reel _____, Frame _____, or for which a copy thereof is attached.
3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark office at
Reel _____, Frame _____, or for which a copy thereof is attached.

Additional documents in the chain of title are listed on a supplemental sheet.

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Tarek N. Fahmi/
Signature

March 26, 2012
Date

Tarek N. Fahmi
Printed or Typed Name

866-377-4833
Telephone Number

Attorney of Record
Title

AppNumber	FileDate	AssignmentTo	Reel	Frame	Ref No
10/217758	12-Aug-02	Acom Technologies, Inc.	013195	0068	40003771-0003-002
11/181217	13-Jul-05	Acom Technologies, Inc.	13195	0068	40003771-0003-003
10/753504	07-Jan-04	Acom Technologies, Inc.	015453	0248	40003771-0003-005
10/753504	07-Jan-04	Acom Technologies, Inc.	016115	0318	40003771-0003-005
10/753504	07-Jan-04	Acom Technologies, Inc.	018401	0333	40003771-0003-005
12/197996	25-Aug-08	Acom Technologies, Inc.	022077	0447	40003771-0003-403
13/022522	07-Feb-11	Acom Technologies, Inc.	022077	0447	40003771-0003-453
10/342576	14-Jan-03	Acom Technologies, Inc.	016771	0810	40003771-0004-002
11/403185	11-Apr-06	Acom Technologies, Inc.	018181	0437	40003771-0004-403
10/754966	09-Jan-04	Acom Technologies, Inc.	18181	437	40003771-0004-004
13/022559	07-Feb-11	Acom Technologies, Inc.	018181	0437	40003771-0004-453
10/832576	26-Apr-04	Acom Technologies, Inc.	015846	0802	40003771-0005-002
11/010048	09-Dec-04	Acom Technologies, Inc.	016081	0879	40003771-0007-002
11/166286	23-Jun-05	Acom Technologies, Inc.	016729	0283	40003771-0008-002
13/019789	02-Feb-11	Acom Technologies, Inc.	016729	0283	40003771-0008-004
11/678397	23-Feb-07	Acom Technologies, Inc.	019424	0808	40003771-0009-002
12/878930	09-Sep-10	Acom Technologies, Inc.	019424	0808	40003771-0009-004
12/253769	17-Oct-08	Acom Technologies, Inc.	022058	0069	40003771-0010-002
12/253835	17-Oct-08	Acom Technologies, Inc.	022063	0521	40003771-0011-002
12/549227	27-Aug-09	Acom Technologies, Inc.	023159	0144	40003771-0014-002
61/537433	21-Sep-11	Acom Technologies, Inc.	027228	0055	40003771-0015-051

Electronic Acknowledgement Receipt

EFS ID:	12396365
Application Number:	13022522
International Application Number:	
Confirmation Number:	6852
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	26263
Filer:	Tarek N. Fahmi/jennifer Stewart
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	40003771-0003-453
Receipt Date:	26-MAR-2012
Filing Date:	07-FEB-2011
Time Stamp:	19:14:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Acorn_executed_POA.pdf	325167 80c6d19a8e22bf29e157c34ec08b5aba90fe056d	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Power of Attorney	1	1
	Assignee showing of ownership per 37 CFR 3.73(b).	2	3
Warnings:			
Information:			
Total Files Size (in bytes):		325167	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/022,522	02/07/2011	Daniel E. Grupp	40003771-0003-453

CONFIRMATION NO. 6852

POA ACCEPTANCE LETTER



27571
TAREK N. FAHMI, APC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

Date Mailed: 04/04/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/26/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/tkim/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/022,522	02/07/2011	Daniel E. Grupp	40003771-0003-453

26263
SNR DENTON US LLP
P.O. BOX 061080
CHICAGO, IL 60606-1080

CONFIRMATION NO. 6852
POWER OF ATTORNEY NOTICE



Date Mailed: 04/04/2012

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/26/2012.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/ttkim/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/022,522	02/07/2011	Daniel E. Grupp	40003771-0003-453	6852
27571	7590	05/31/2012		
TAREK N. FAHMI, APC 84 W. Santa Clara St. Suite 550 San Jose, CA 95113			EXAMINER HARRISON, MONICA D	
			ART UNIT 2896	PAPER NUMBER
			NOTIFICATION DATE 05/31/2012	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@tnfip.com
tarek.fahmi@tnfip.com

Office Action Summary	Application No.	Applicant(s)	
	13/022,522	GRUPP ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2896	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 January 2012.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 5) ☒ Claim(s) 1 and 2 is/are pending in the application.
- 5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1 and 2 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 12) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) ☐ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date ____. | 6) ☐ Other: ____. |

DETAILED ACTION

1. Applicant's amendment filed 1/23/12 has been entered. Examiner acknowledges claims 3-31 are cancelled.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyawaki et al "Improvement of Aluminum-Si Contact Performance in Native Oxide Free Processing", IEEE Electron Device Letters Vol. 11, NO.10, October 1990, pp. 448-450 and Takahagi et al "The formation of hydrogen passivated silicon single crystal surface using ultraviolet cleaning and HF etching", Journal of Applied Physics, Vol.64, No.7 1 October 1988, pp. 3516-3521 in view of Wittmer et al "Ideal Schottky Diodes on Passivated Silicon", Physical Review Letters, Vol.69 No.18, 2 November 1992, pp. 2701-2704.

2. Regarding claim 1, Miyawaki et al discloses a method comprising immersing a semiconductor substrate into a solution of HF, which contains hydrogen and fluorine ions (p. 448, left col., lines 20-21 in introduction section), removing the substrate from the solution and blow drying with nitrogen (p. 448, left col., lines 23-24 in introduction section) which passivates the semiconductor substrate with an interface layer containing hydrogen and fluorine (*Takahagi*

Art Unit: 2896

et al provides evidence by way of FIG. 7 and associated text that HF solution dipping a silicon substrate leads to the formation of a hydrogen and fluorine terminated passivating monolayer on a silicon substrate), which is of sufficient thickness to passivate the surface of the semiconductor substrate. Miyawaki et al also discloses an aluminum metal layer is subsequently deposited over the interfacial layer (p. 449, left col., lines 1-5) forming a junction which has a specific contact resistance of less than $1000 \Omega\text{-}\mu\text{m}^2$ (p. 449, left col., lines 9-11; $0.4 \mu\Omega\text{-cm}^2$ converts to $40 \Omega\text{-}\mu\text{m}^2$).

Although Miyawaki et al discloses the conditions of the HF immersion generally, Miyawaki et al does not disclose cleaning the semiconductor substrate with a cleaning solution, immersing in HF for several seconds to 5 minutes with a 1-50% by weight concentration.

Wittmer et al discloses an HF immersion technique for forming hydrogen-fluorine passivation monolayers on silicon substrates including cleaning the semiconductor substrate with a cleaning solution, such as RCA clean (p. 2702, left col., line 8) and using a 10:1 diluted HF immersion for 30 seconds (p. 2702, left col., lines 10-11 and 28-29).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art to use the HF immersion technique of Wittmer et al in the method of Miyawaki et al since the RCA clean was an industrial standard in the semiconductor field for removing contaminants from wafer surfaces, and the conditions of the HF concentration and immersion time are sufficient to effectively passivate the silicon substrate surface for the formation of an ideal diode.

Art Unit: 2896

3. Regarding claim 2, Miyawaki et al discloses rinsing with water after blow drying with nitrogen and Wittmer et al teaches using deionized water so for 30 seconds and it would have been obvious at the time the invention was made to use less than 30 seconds given these teachings in order to save processing time. Additionally, a prima facie case of obviousness exists where the claimed ranges and prior art ranges do not overlap but are close enough that one skilled in the art would have expected them to have the same properties. *Titanium Metals Corp. of America v. Banner*, 778 F.2d 775, 227 USPQ 773. See MPEP § 2144.05.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is (571)272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Such can be reached on 571-272-8895. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2896

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Monica D. Harrison/
Examiner, Art Unit 2896

mdh
May 15, 2012

/Matthew W. Such/
Supervisory Patent Examiner, Art Unit 2896

Notice of References Cited	Application/Control No. 13/022,522	Applicant(s)/Patent Under Reexamination GRUPP ET AL.	
	Examiner Monica D. Harrison	Art Unit 2896	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Miyakawi et al, "Improvement of Aluminum-Si Contact Performance in Native Oxide Free Processing", October 1990, IEEE Electron Device Letters, Vol. 11 No. 10, pp.448-450.
	V	Takahagi et al, "The formation of hydrogen passivated silicon single crystal surface using ultraviolet cleaning and HF etching", 1 October 1988, Journal of Applied Physics, Vol.64 No.7, pp.3516-3521.
	W	Wittmer et al, "Ideal Schottky Diodes on Passivated Silicon", 2 November 1992, Physical Review Letters, Vol.69 No.18, pp.2701-2704.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Receipt date: 03/25/2011

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

13022522 - GAI: 2896

PFO/05/05a (01-10)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522
	Filing Date		2011-02-07
	First Named Inventor	Daniel E. Grupp	
	Art Unit	2811	
	Examiner Name		
	Attorney Docket Number	40003771-0003-453	

U.S. PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
/M.D.H./	1	3590471		1971-07-06	Lepselter, et al.	
	2	3708360		1973-01-02	Wakefield, Jr., et al.	
	3	3983264		1976-09-28	Schroen, Walter H., et al.	
	4	4056642		1977-11-01	Saxena, Arjun N. et al.	
	5	4300152		1981-11-10	Lepselter	
	6	4485550		1984-12-04	Koeneke, et al.	
	7	5021365		1991-06-04	Kirchner, et al.	
	8	5399206		1995-03-21	de Lyon	

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2896
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit		2811	
	Examiner Name			
	Attorney Docket Number		40003771-0003-453	

/M.D.H./	9	5578848		1996-11-26	Kwong, et al.	
	10	5596218		2009-04-10	Soleimani, et al.	
	11	5612567		1997-03-18	Baliga	
	12	5663584		1997-09-02	Welch	
	13	5801398		1998-09-01	Hebiguchi	
	14	5888891		1999-03-30	Gould	
	15	5939763		1999-08-17	Hao, et al.	
	16	6037605		2000-03-14	Yoshimura	
	17	6096590		2000-08-01	Chan, et al.	
	18	6150286		2000-11-21	Sun et al.	
	19	6198113		2001-03-06	Grupp, Daniel E.	

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2896
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit		2811	
	Examiner Name			
	Attorney Docket Number		40003771-0003-453	

/M.D.H./	20	6207976		2001-03-27	Takshashi et al.	
	21	6261932		2001-07-17	Hulfachor	
	22	6291866		2001-09-18	Wallace et al.	
	23	6291867		2001-09-18	Wallace et al.	
	24	6303479		2001-10-16	Snyder	
	25	7084423		2006-08-01	Grupp et al.	
	26	5801444		1998-09-01	Aboelfotoh et al.	
	27	7176483		2007-02-13	Grupp et al.	

If you wish to add additional U.S. Patent citation information please click the Add button.

Add

U.S.PATENT APPLICATION PUBLICATIONS

Remove

Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/M.D.H./	1	20030121468		2003-07-03	Boone et al.	

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2896
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./	2	20040026687		2004-02-12	Grupp et al.	
/M.D.H./	3	20050093027		2005-05-05	Grupp et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
/M.D.H./	1	0295490	EP		1988-12-21	Fowler, Alan B. et al.		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button.

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
/M.D.H./	1	ABERLE, ARMIN G., et al., "Injection-Level Dependent Surface Recombination Velocities at The Silicon-Plasma Silicon Nitride Interface", Institut fur Solaernergieforchung, ISFH, D-3 1860 Emmerthal, Germany, (3/9/95), pp. 2828-2830	☐
	2	B. J. ZHANG, et al., "Schottky Diodes of Ni/Au on n-GaN Grown on Sapphire and SiC Substrates", Applied Physics Letters, Vol. 79, No. 16, (10/15/01), pp. 2567-2569	☐
	3	B.R. WEINBERGER, et al., "Surface Chemistry of HF Passivation Silicon: X-Ray Photoelectron And Ion Scattering Spectroscopy Results", J. Appl. Phys. 60(9), (11/186), pp. 3232-3234	☐
	4	C.L. CHEN, et al., "High Quality Native-Oxide-Free Ultrathin Oxide Grown by In-Situ HF-Vapor Treatment", Electronic Letters, Vol. 36, No. 11, (5/25/00), pp. 981-983	☐

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2896
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./	5	CHUNG-KUANG, HUANG , et al., "Two-Dimensional Numerical Simulation of Schottky Barrier MOSFET with Channel Length to 10 nn", IEEE, pp. 842-848	☐
	6	D. J. CHADI, et al., "Fermi-Level-Pinning Defects in Highly n-Doped Silicon", Physical Review Letters, Vol. 79, No. 24, NEC Research Institute, Princeton New Jersey 08540-6634, (12/97),pp. 4834-4837	☐
	7	E. YABLONOVITCH, et al., "Unusually Low Surface-Recombination Velocity on Silicon and Germanium Surfaces", Physical Review Letters, Vol. 57, No. 2, (7/14/86),pp. 249-252	☐
	8	F. A. PADOVANI, "Forward Voltage-Current Characteristics of Metal-Silicon Schottky Barriers", Texas Instruments, Inc., Dallas Texas, (9/15/66),pp. 892-892	☐
	9	G.B. AKERS, et al., "Effects of Thermal Stability and Roughness on Electrical Properties of Tantalus Oxide Gates", Mat. Res., Soc. Symp. Proc., Vol. 567, Materials Research Society, (1999),pp. 391-395	☐
	10	HASEGAWA, HIDEKI , et al., "Upping of Fermi Level in Nanometer-Sized Schottky Contacts on GaAs and InP", Reseach Center For Interface Quantum Electronics And Graduate School of Electronics And Info. Eng, Hokkaido Univ, Japan, (2000),pp. 92-96	☐
	11	HEINE, VOLKER , "Theory of Surface States", Physical Review Letters, Vol. 138, No. 6A, Tell Telephone Lab., Murphy Jill, New Jersey, (6/4/65),	☐
	12	HUANG, FENG-JUNG , "Metal-Oxide Semiconductor Field-Effect Transistors Using Schottky Barrier Drains", Electronics Letters, Vol. 33, No. 15, (7/17/97),pp. 1341-1342	☐
	13	I. SHALISH, et al., "Yellow Luminescence And Fermi Level Pinning in GaN Layers", American Institute of Physics, Vol. 77, No. 7, (8/14/00),pp. 987-989	☐
	14	INTERNET, http://www.rciqe.hokudai.ac.jp/RCIQEold/ResearchAchievements.html , downloaded (4/12/02),	☐
	15	IZUMI, HIROT , et al., "43 Hydrogen Termination: The Ideally Finished Silicon Surface", Ultraclean Surface Processing of Silicon Wafers: Secrets of Vlsi Manufacturing http://halloftechnology.com/electrical_optical/986.shtml , (11/98),	☐

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2896
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./	16	J. HILSENBECK, et al., "Aging Behavior of AlGaIn/GaN HFETs With Advanced Ohmic And Schottky Contacts", Electronic letters, Vol. 36, No. 11, (5/25/00),pp. 980-981	☐
	17	J. TERSOFF, "Schottky Barrier Heights and The Continuum of Gap States", Physical Review Letters, Vol. 52, No. 6, AT&T Bell Lab., Murphy Hill, New Jersey 07974, (2/6/84),	☐
	18	J.R. PATEL, et al., "Arsenic Atom Location on Passive Silicon (111) Surfaces", Physical Review B. Vol. 36, No. 14, (11/15/87),pp. 7715-7717	☐
	19	K. NAUKA, et al., "Surface Photovoltage Measurement of Hydrogen-Treated Si Surfaces", Journal of Electrochemical Society 146(1), (1999),pp. 292-295	☐
	20	KAMIYAMA, SATOSHI, et al., "Ultrathin Tantalum Oxide Capacitor Dielectric Layers Fabricated Using Rapid Thermal Nitridation Prior to Low Pressure Chemical Vapor Deposition", J. Electrochem Soc., Vol. 140, No. 6, The Electrochemical Society, Inc., (6/6/93),pp. 1617	☐
	21	KIMURA, MITSUTERU, et al., "A New Type of Schottky Tunnel Transistor", IEEE Electron Device Letters, Vol. 15, No. 10, (10/94),pp. 412-41	☐
	22	L. CAI, et al., "Investigation of The Properties of Plasma-Enhanced Chemical Vapor Deposition Silicon Nitride And its Effect on Silicon Surface Passivation", Journal of Applied Physics, Vol. 83, No. 11, (6/1/98),pp. 5885-5889	☐
	23	LEE, TAKHEE, et al., "Electronic Property of Metallic Nanoclusters on Semiconductor Surfaces: Implications For Nanoelectronic Device Applications", Journal of Nanoparticle Research 2, (2000),pp. 345-362	☐
	24	LOUIE, STEVEN G., et al., "Ionicity And The Theory of Schottky Barriers", Physical Review Letters, Vol. 15, No. 4, Dept. of Phys. Univ. of California, and Materials and Molecular Research Div., Lawrence Berkeley Lab., Berkeley, CA 94720,	☐
	25	M. A. SOBOLEWSKI, et al., "Properties of Ultrathin Thermal Nitrides in Silicon Schottky Barrier Structures", Applied Physics Letters, American Institute of Physics, Vol 54, No. 7, (2/13/89),pp. 638-640	☐
↓	26	M. MIYAWAKI, et al., "Improvement of Aluminum-Si Contact Performance in Native-Oxide-Free Processing", IEEE Electron Device Letters, Vol. 11, No. 10, (10/90),pp. 448-450	☐

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2896
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./	27	M.C. GILMER, et al., "Process and Manufacturing Challenges For High-K Gate Stack Systems", Mat. Res. Soc. Symp. Proc. Vol. 567, (1999),pp. 323-341	☐
	28	MANDELIS, ANDREAS , et al., "Evidence of a Surface Acceptor State in Undoped Semi-Insulating GaAs by Photothermal Radiometric Deep Level Transient Spectroscopy", Sociedad Mexicana de Ciencias de Superficies y de Vacio, (1999),pp. 13-17	☐
	29	NISHIOKA, YASUSHIRO , et al., "Dielectric Characteristics of Fluorinated Ultradry SiO2", Appl. Phy. Letters 54(12), (3/20/89),pp. 1127-112	☐
	30	OKAMOTO, NAOYA , et al., "Near-Ohmic Contact of n-GaAs with Ga/Ga/GaAs Quasi-Metal-Insulator-Semiconductor Structure", Jpn. J. Appl. Phys., Vol. 37, (1998),pp. 32483251	☐
	31	P. BAUERNSCHMITT, et al., "Yb-SiO2-Si Tunneling Junctions", Elsevier Publishers B.V., (1993),pp. 105-108	☐
	32	PORTER, LISA M., et al., "A Critical Review of Ohmic and Rectifying Contacts For Silicon Carbide", Material Science and Engineering, Vol. 34, No. 2, (11/1/95),pp. 83-105	☐
	33	R.A. MCKEE, et al., "Physical Structure And Inversion Charge at a Semiconductor Interface With a Crystalline Oxide", www.sciencemag.org, Vol. 293, (7/20/01),pp. 468-469	☐
	34	R.D. BRINGANS, "Arsenic Passivation of Si and Ge Surfaces", Critical Reviews in Solid State and Materials Sciences, 17(4): 353-395, (1992),pp. 353-395	☐
	35	R.M.C. DE ALMEIDA, et al., "Reaction-Diffusion Model For Thermal Growth of Silicon Nitride Films on Si", Physical Review B, Vol. 62, No. 24, (12/1500),pp. R16 255-R16 258	☐
	36	R.T. TUNG, "Electron Transport of Inhomogeneous Schottky Barriers", AT&T Bell Lab., Murray Hill, New Jersey 07974, (3/21/91),pp. 3832-3834	☐
↓	37	S. HARA, et al., "Control of Schottky And Ohmic Interfaces by Unpinning Fermi Level", Elsevier Science B.V., pp. 394-399	☐

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2896
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./	38	S. HARA, et al., "Pinning-Controlled Metal/Semiconductor Interfaces", Electrotechnical Laboratory, pp. 802-807	☐
	39	S. HARA, et al., "Pinning-Controlled Ohmic Contacts: Application to SiC(0001)", Elsevier Science B.V., pp. 218-221	☐
	40	S. VERHAVERBEKE, et al., "Surface Characterization of Si After HF Treatments and its Influence in the Dielectric Breakdown of Thermal Oxides", Research Aspirant of the Belgium National Fund for Scientific Research; Mat. Res. Soc. Symp. Proc., Vol. 259, Material Research Society, (1992),pp. 391-399	☐
	41	S.A. WOLF, et al., "Spintronics: A Spin-Based Vision For The Future", www.sciencemag.or, Vol.294, (11/6/01),pp. 1488	☐
	42	S.M. SZE, "Metal-Semiconductor Contacts", Physics of Semiconductor Devices, John Wiley & Sons, (1981),	☐
	43	SCHMIDT, JAN , et al., "Carrier Recombination at Silicon-Silicon Nitride Interfaces Fabricated by Plasma-Enhanced Chemical Vapor Deposition", Journal of Applied Physics, Vol. 85, No. 7, (4/1/99),pp. 3626-3633	☐
	44	ACORN TECHNOLOGIES, INC. PCT/US03/25054 filed 08 August 2003, International Search Report, International Searching Authority/US, (12/3/03),pp. 6	☐
	45	SHAIK, LAHIR , et al., "Experimental Identification of Nitrogen-Vacancy Complexes in Nitrogen Implanted Silicon", Applied Physics Letters, Vol. 79, No. 5, (7/30/01),pp. 623-625	☐
	46	SNYDER, JOHN P., et al., "Experimental Investigation of a PtSi Source And Drain Field Emission Transister", American Institute of Physics, pp. 1-3	☐
	47	T.I. KAMINS, et al., "Effect of Hydrogen on p-Type Epitaxial Silicon Sheet-Resistance Measurements", Electrochemical and Solid-State Letters 1(2), (1998),pp. 100-101	☐
↓	48	TERAJI, TOKUYUKI , et al., "Ohmic Contacts To n-Type 6H-SiC Without Post-Annealing", Material Research Society Symposium Proceeding, (4/8/96),pp. 149-154	☐

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2896
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./	49	U.J.R. BAUMVOL, "Atomic Transport During Growth of Ultrathin Dielectrics on Silicon", Surface Science Reports 36, (1999),pp. 1-166	☐
/M.D.H./	50	W.E. SPICER, et al., "Unified Mechanism For Schottky-Barrier Formation And III-V Oxide Interface States", Physical Review Letters, Vol. 44, No. 6, Stanford Electronics Lab., Stanford Univ., Stanford, CA 94305, (2/11/80),pp. 420-423	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/Monica D. Harrison/	Date Considered	05/14/2012
--------------------	----------------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

Receipt date: 03/25/2011

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

13022522 - GALL: 2896

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

U.S.PATENTS							Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1						

If you wish to add additional U.S. Patent citation information please click the Add button.

Add

U.S.PATENT APPLICATION PUBLICATIONS							Remove
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
	1						

If you wish to add additional U.S. Published Application citation information please click the Add button.

Add

FOREIGN PATENT DOCUMENTS								Remove
Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

Add

NON-PATENT LITERATURE DOCUMENTS				Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵	

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2896
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./	1	WANG, LIE , et al., "High Barrier GaN Schottky Diodes: Pt/GaN and Pd/GaN", Dept. of Electrical Eng., Univ. of Minnesota, Minneapolis, Minnesota 55455; Appl. Phys. Letters, Vol. 68(9), (2/26/96),pp. 1267-1270	☐
	2	WIDJAJA, YUNIARTO , et al., "Ab Initio Study and Decomposition of NH3 on Si(100)-(2x1)", J. Phy. Chem B, (2000), pp. 2527-2533	☐
	3	WRIGHT, PETER J., et al., "Hot-Electron Immunity of SiO2 Dielectrics with Fluorine Incorporation", IEEE Electron Device Letters, Vol. 10, No. 8, (8/8/89),pp. 347-348	☐
	4	Y. HAYAFUJI, et al., "Nitridation of Silicon and Oxidized-Silicon", Sony Corp. Research Center, 174 Fujitsuka-Cho, Hodogaya-Ku, Yokohama, 240 Japan; J. Electrochem. Soc.: Solid State Science and Technology, (9/82),	☐
	5	Y. K. KIM, et al., "Metal-Dependent Fermi-Level Movement in The Metal/Sulfur-Passivated InGaP Contact", J. Vac Sci. Technology A 15(3), (1997),pp. 1124-1128	☐
	6	YANG, HANYANG , et al., "The Effects of Interfacial Sub-Oxide Transition Regions and Monolayer Level Nitridation on Tunneling Currents in Silicon Devices", IEEE Electron Device Letters, Vol. 21, No. 2, (2/2/00),pp. 76-78	☐
	7	BLOSSE, A., et al., "A Novel Low Cost 65nm CMOS Process Architecture With Self Aligned Isolation and W Cladded Source/Drain", IEEE, Transactions of 2004 International Electron Device Meeting, pp. 669-672	☐
	8	CONNELLY, DANIEL, et al., "Optimizing Schottky S/D Offset for 25-nm Dual-Gate CMOS Performance", IEEE Trans. Electron Devices, Vol. 47 No. 5, (2003), pp. 1028-1034	☐
	9	EDELSTEIN, D., et al., "Full Copper Wiring in a Sub-0.25 mm CMOS ULSI Technology", Proceedings of the IEEE International Electron Device Meeting, (12/1997), pp. 773-776	☐
	10	GOPALAKRISHNAN, KAILASH, et al., "Impact Ionization MOS (I-MOS)-Part I: Device and Circuit Simulations", IEEE Transactions Electron Devices, Vol. 52, No. 1, (2005), pp. 69-76	☐
↓	11	KEDZIERSKI, JAKUB, et al., "Extension and Source/Drain Design for High-Performance FinFET Devices", IEEE Trans. Electron Devices, Vol. 50, No. 4, (4/2003), pp. 952-958	☐

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2896
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit	2811		
	Examiner Name			
	Attorney Docket Number	40003771-0003-453		

/M.D.H./ 	12	THOMPSON, SCOTT E., et al., "A Logic Nanotechnology Featuring Strained-Silicon", IEEE Electron Device Letters, Vol. 25, No. 4, (2004), pp. 191-193	☐
	13	WEI, C.S., et al., "The Use of Selective Electroless Metal Deposition For Micron Size Contact Fill", IEEE International Electron Device Meeting Technical Digest, (1988), pp. 446-449	☐
	14	YAGISHITA, ATSUSHI, et al., "High Performance Damascene Metal Gate MOSFET's for 0.1 mm Regime", IEEE Trans. Electron Devices, Vol. 47, No. 5, (2000), pp. 1028-1034	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/Monica D. Harrison/	Date Considered	05/14/2012
--------------------	----------------------	-----------------	------------

***EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

Search Notes 	Application/Control No. 13022522	Applicant(s)/Patent Under Reexamination GRUPP ET AL.
	Examiner MONICA D HARRISON	Art Unit 2893

SEARCHED			
Class	Subclass	Date	Examiner
257	486,571,E21.192,E29.148	9/28/11	MDH
438	571	5/15/12	MDH

SEARCH NOTES		
Search Notes	Date	Examiner
East (USPAT, US-PGPUB, USOCR, EPO, JPO, DERWENT, IBM_TDB, FPRS)	9/28/11	MDH
East updated	5/15/12	MDH
GRUPP et al .inv.	5/15/12	MDH
USPAT, US-PGPUB, UPAD txt .clm.	5/15/12	MDH

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

/MONICA D HARRISON/ Examiner.Art Unit 2893	
---	--

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	13/022522	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 15:58
S2	2	"7884003".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 15:59
S3	2	"7462860".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:02
S4	2	"7084423".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:03
S5	1157	257/486,571,E21.192,E29.148.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:06
S6	465	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:06
S7	173	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier) with height	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:06
S8	84	257/486,571,E21.192,E29.148.ccls. and	US-PGPUB;	OR	ON	2011/09/26

		(schottky near barrier) with height and (interface with metal)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			16:06
S9	68	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier) with height and (interface with metal) and (interface with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:07
S10	21	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier) with height and (interface with metal) and (interface with semiconductor) and (metal near interface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:07
S11	15	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier) with height and (interface with metal) and (interface with semiconductor) and (metal near interface) and (semiconductor near junction) with metal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:08
S12	28	257/486,571,E21.192,E29.148.ccls. and (interface near4 passivat\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:49
S13	15	257/486,571,E21.192,E29.148.ccls. and (interface near4 passivat\$4) and (interface near4 separat\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:50
S14	1	257/486,571,E21.192,E29.148.ccls. and (dual with passivat\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:52
S15	1	257/486,571,E21.192,E29.148.ccls. and (lower or bottom or below) near passivat\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:53
S16	809	257/'\$.ccls. and (lower or bottom or below) near passivat\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2011/09/27 14:53

			IBM_TDB			
S17	257	257/'\$.ccls. and (lower or bottom or below) near passivat\$4 and (upper or top or above) near passivat\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:53
S18	133	257/'\$.ccls. and (lower or bottom or below) near passivat\$4 and (upper or top or above) near passivat\$4 and (passivat\$4 with metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:54
S19	89	257/'\$.ccls. and (lower or bottom or below) near passivat\$4 and (upper or top or above) near passivat\$4 and (passivat\$4 with metal) and (passivat\$4 with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:54
S20	5	257/'\$.ccls. and (lower or bottom or below) near passivat\$4 and (upper or top or above) near passivat\$4 and (passivat\$4 with metal) and (passivat\$4 with semiconductor) and schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:55
S21	18	257/486,571,E21.192,E29.148.ccls. and (constant with resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:03
S22	5	257/486,571,E21.192,E29.148.ccls. and (constant near3 resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:04
S23	28	257/486,571,E21.192,E29.148.ccls. and (interface near3 passivat\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:14
S24	6	257/486,571,E21.192,E29.148.ccls. and (interface near3 (metal near oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:20
S25	0	257/486,571,E21.192,E29.148.ccls. and migd	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2011/09/27 15:25

			JPO; DERWENT; IBM_TDB			
S26	12	257/486,571,E21.192,E29.148.ccls. and "MIGS"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:25
S27	94	257/'\$.ccls. and "MIGS"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:25
S28	98	257/'\$.ccls. and ("MIGS" or (metal near induced near gap))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:27
S29	34	257/'\$.ccls. and (metal near induced near gap)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:27
S30	31715	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 11:58
S31	5316	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 11:59
S32	0	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and ((hydrogen and fluorine) near ion) with weight	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:00
S33	0	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (((hydrogen and fluorine) near ion) with weight)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:00
S34	4	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or	US-PGPUB; USPAT;	OR	ON	2011/09/28 12:02

		clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (blow near dry)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S35	0	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (blow near dry) and (immers\$4 with (substrate or wafer or carrier or base or plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:02
S36	14	(substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (blow near dry) and (immers\$4 with (substrate or wafer or carrier or base or plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:03
S37	9	(substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (blow near dry) and (immers\$4 with (substrate or wafer or carrier or base or plate)) and metal and semiconductor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:04
S38	0	(substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (blow near dry) and (immers\$4 with (substrate or wafer or carrier or base or plate)) and metal and semiconductor and junction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:04
S39	2	"6293197".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:09
S40	15	257/486,571,E21.192,E29.148.ccls. and dipole	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:11
S41	2	257/486,571,E21.192,E29.148.ccls. and (dipole with metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:12
S42	2	257/486,571,E21.192,E29.148.ccls. and (dipole with metal) and (dipole with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:12

S43	67	257/'\$.ccls. and (dipole with metal) and (dipole with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:12
S44	98	257/486,571,E21.192,E29.148.ccls. and (source drain) with interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:12
S45	48	257/486,571,E21.192,E29.148.ccls. and (source drain) with interface and (interface with metal) and (interface with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:19
S46	44	257/486,571,E21.192,E29.148.ccls. and (source drain) with interface and (interface with metal) and (interface with semiconductor) and schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:19
S47	2	"6462931".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:34
S48	3	"4723197".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:35
S49	2	"5027166".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:49
S50	2	"6293137".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 14:11
S51	1	"13022522"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2012/05/14 15:15

			DERWENT; IBM_TDB			
S52	1724	438/571.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:16
S53	70	438/571.ccls. and (substrate wafer carrier base plate) with (clean\$4 ash\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:16
S54	15	438/571.ccls. and (substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:17
S55	3	438/571.ccls. and (substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:17
S56	3	438/571.ccls. and (substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:18
S57	877	S54(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:26
S58	865	(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:26
S59	16	(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine) and (blow near dry\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:27
S60	13	(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and	US-PGPUB; USPAT; USOCR;	OR	ON	2012/05/14 15:28

		(substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine) and ((blow near dry\$4) with nitrogen)	FPRS; EPO; JPO; DERWENT; IBM_TDB			
S61	11	(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine) and ((blow near dry\$4) with nitrogen) and (interface with hydrogen)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:29
S62	11	(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine) and ((blow near dry\$4) with nitrogen) and (interface with hydrogen) and (interface with fluor\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:30
S63	11	(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine) and ((blow near dry\$4) with nitrogen) and (interface with hydrogen) and (interface with fluor\$4) and (grupp connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:33

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S64	4	(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine) and ((blow near dry\$4) with nitrogen) and (interface with hydrogen) and (interface with fluor\$4).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2012/05/14 15:34

5/ 15/ 2012 10:09:04 AM
C:\ Users\ mharrison1\ Documents\ EAST\ Workspaces\ 13022522.wsp

<i>Index of Claims</i> 	Application/Control No. 13022522	Applicant(s)/Patent Under Reexamination GRUPP ET AL.
	Examiner MONICA D HARRISON	Art Unit 2896

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE							
Final	Original	09/28/2011	05/15/2012						
	1	=	✓						
	2	=	✓						
	3	✓	-						
	4	✓	-						
	5	✓	-						
	6	✓	-						
	7	✓	-						
	8	✓	-						
	9	✓	-						
	10	✓	-						
	11	✓	-						
	12	✓	-						
	13	✓	-						
	14	✓	-						
	15	✓	-						
	16	✓	-						
	17	✓	-						
	18	✓	-						
	19	✓	-						
	20	✓	-						
	21	✓	-						
	22	✓	-						
	23	✓	-						
	24	✓	-						
	25	✓	-						
	26	✓	-						
	27	✓	-						
	28	✓	-						
	29	✓	-						
	30	✓	-						
	31	✓	-						

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Daniel E. Grupp

Application No.: 13/022,522

Filed: February 7, 2011

Examiner: Harrison, Monica D.

Art Unit: 2896

Docket No.: 40003771-0003-453

Confirmation No.: 6852

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Madam:

In response to the Office Action dated May 31, 2012, reconsideration of the above-indicated application is respectfully requested in light of the following amendments and remarks.

AMENDMENTS TO THE CLAIMS

The following listing of the claims shall replace all previous versions thereof.

1. (Original) A method, comprising cleaning a semiconductor substrate with a cleaning solution to form a cleaned substrate; immersing, for a period of time between several seconds and approximately five (5) minutes, the cleaned substrate in a solution containing hydrogen and fluorine ions of between approximately 1%-50% by weight; removing the substrate from the solution and blow-drying the substrate with nitrogen, thereby forming an interface layer containing hydrogen and fluorine on the semiconductor substrate, said interface layer being of sufficient thickness to passivate a surface of said semiconductor substrate in a vicinity of said interface layer; subsequently depositing a metal layer over the interface layer through thermal evaporation of a source, thereby forming a junction having a metal layer disposed over the interface layer disposed over the semiconductor, said junction having a specific contact resistance of less than or equal to approximately $1000\ \Omega\text{-}\mu\text{m}^2$.
2. (Original) The method of claim 1, wherein following removal of the substrate from the solution and prior to blow-drying the substrate with nitrogen, rinsing the substrate in deionized water for less than 30 sec.
- 3 – 31. (Cancelled)

REMARKS

Reconsideration of this application in light of the preceding amendments and the following remarks is respectfully requested. Claim 1 is amended to clarify that a thermally evaporated source is used for the metal deposition. Support for the amendments is provided in, for example, paragraph 55 of the originally filed specification and, as such, no new matter has been added.

The combination of Miyawaki, Takahagi and Wittmer fails to obviate the present invention. In particular, Miyawaki teaches the use of sputter deposition, contrary to the use of a thermally evaporated source, as claimed. Accordingly, the claims are patentable over the combination of cited references.

Please charge any additional fee due in connection with this communication to Deposit Account No. 50-5798.

Respectfully submitted,

Date: August 30, 2012

/Tarek N. Fahmi/

Tarek N. Fahmi
Reg. No. 41,402

Tarek N. Fahmi, APC
84 W. Santa Clara St., Suite 550
San Jose, CA 95113
866-877-4883

Electronic Acknowledgement Receipt

EFS ID:	13633078
Application Number:	13022522
International Application Number:	
Confirmation Number:	6852
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-453
Receipt Date:	30-AUG-2012
Filing Date:	07-FEB-2011
Time Stamp:	21:18:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		40003771-0003-453_R-OA_8-30-12.pdf	89028 0f2c88d6db5b5fa979a338c9aa7483ab9b4b2dd6	yes	3

Multipart Description/PDF files in .zip description			
Document Description		Start	End
Amendment/Req. Reconsideration-After Non-Final Reject		1	1
Claims		2	2
Applicant Arguments/Remarks Made in an Amendment		3	3

Warnings:

Information:

Total Files Size (in bytes):	89028
-------------------------------------	-------

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/022,522		Filing Date 02/07/2011		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☒ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(j))	minus 20 =	*	X \$	=	OR	X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=		X \$	=			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL				
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	08/30/2012	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 2	Minus	** 36	= 0	X \$30 =	0	OR	X \$	=
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 4	= 0	X \$125 =	0	OR	X \$	=
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=	OR	X \$	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=	OR	X \$	=
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/VERNON TOWLER/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

27571 7590 01/02/2013
TAREK N. FAHMI, APC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

EXAMINER

HARRISON, MONICA D

ART UNIT

PAPER NUMBER

2896

DATE MAILED: 01/02/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

13/022,522

02/07/2011

Daniel E. Grupp

40003771-0003-453

6852

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$885	\$300	\$0	\$1185	04/02/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

27571 7590 01/02/2013
TAREK N. FAHMI, APC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

13/022,522 02/07/2011 Daniel E. Grupp 40003771-0003-453 6852

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$885	\$300	\$0	\$1185	04/02/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
HARRISON, MONICA D	2896	438-571000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a **Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s); (Please first reapply any previously paid issue fee shown above)

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/022,522	02/07/2011	Daniel E. Grupp	40003771-0003-453	6852

27571 7590 01/02/2013
TAREK N. FAHMI, APC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

EXAMINER

HARRISON, MONICA D

ART UNIT PAPER NUMBER

2896

DATE MAILED: 01/02/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	13/022,522	GRUPP ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2896	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 8/30/2012 (Amendment).
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1 and 2. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|---|
| <ol style="list-style-type: none"> 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date ____ 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date ____ | <ol style="list-style-type: none"> 5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other ____. |
|---|---|

/Monica D. Harrison/
Assistant Examiner

/Calvin Lee/
Primary Examiner, Art Unit 2896

OFFICE ACTION

1. Applicant's amendment filed 8/30/12 has been entered.

Allowable Subject Matter

2. Claims 1 and 2 are allowed over the prior art.

Reasons for Allowance

3. The following is an examiner's statement of reasons for allowance:

After consideration of applicant's arguments, amendments and a further search of the prior art, examiner has concluded that the prior art does not disclose nor fairly suggest a method, comprising cleaning a semiconductor substrate with a cleaning solution to form a cleaned substrate; removing the substrate from the solution and blow-drying the substrate with nitrogen, thereby forming an interface layer containing hydrogen and fluorine on the semiconductor substrate, said interface layer being of sufficient thickness to passivate a surface of said semiconductor substrate in a vicinity of said interface layer; subsequently depositing a metal layer over the interface layer through thermal evaporation of a source, thereby forming a junction having a metal layer disposed over the interface layer disposed over the semiconductor, said junction having a specific contact resistance of less than or equal to approximately $1000\ \Omega\text{-}\mu\text{m}^2$, as described in the independent claim and in the context of its recited process along with its depending claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Application Number: 13/022,522
Docket No: 40003771-0003-453

A.U.2896 (Page 3)
GRUPP, et al.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Monica D. Harrison* whose telephone number is (571) 272-1959. The examiner can normally be reached on Monday-Friday 7:00AM-3:30PM EST. If attempts to reach the examiner by telephone are unsuccessful, Art Unit 2896's Supervisory Patent Examiner *Matthew Such* can be reached at (571) 272-8895. The fax phone number for the organization is (571) 273-8300.

Information regarding the status of this application may be obtained from either Public Patent Application Information Retrieval (PAIR) or Private PAIR system at <http://pair-direct.uspto.gov>. Should you have questions on access to the PAIR, contact Electronic Board Center at (866) 217-9197. For assistance from a USPTO Customer Service system, call toll free (800) 786-9199 or (571) 272-1000

/Monica D. Harrison/
Assistant Examiner

December 14, 2012

Date

/Calvin Lee/

Primary Patent Examiner, A.U.2896

Search Notes 	Application/Control No. 13022522	Applicant(s)/Patent Under Reexamination GRUPP ET AL.
	Examiner MONICA D HARRISON	Art Unit 2893

SEARCHED			
Class	Subclass	Date	Examiner
257	486,571,E21.192,E29.148	9/28/11	MDH
438	571	5/15/12	MDH

SEARCH NOTES		
Search Notes	Date	Examiner
East (USPAT, US-PGPUB, USOCR, EPO, JPO, DERWENT, IBM_TDB, FPRS)	9/28/11	MDH
East updated	5/15/12	MDH
GRUPP et al .inv.	5/15/12	MDH
USPAT, US-PGPUB, UPAD txt .clm.	5/15/12	MDH
East updated	12/13/12	MDH

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	USPAT, US-PGPUB, UPAD txt .clm.	12/13/12	MDH

/MONICA D HARRISON/ Examiner.Art Unit 2893	
---	--

<i>Index of Claims</i> 	Application/Control No. 13022522	Applicant(s)/Patent Under Reexamination GRUPP ET AL.
	Examiner MONICA D HARRISON	Art Unit 2896

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant					☐ CPA		☐ T.D.		☐ R.1.47	
CLAIM		DATE								
Final	Original	09/28/2011	05/15/2012	12/14/2012						
	1	=	✓	=						
	2	=	✓	=						
	3	✓	---							
	4	✓	---							
	5	✓	---							
	6	✓	---							
	7	✓	---							
	8	✓	---							
	9	✓	---							
	10	✓	---							
	11	✓	---							
	12	✓	---							
	13	✓	---							
	14	✓	---							
	15	✓	---							
	16	✓	---							
	17	✓	---							
	18	✓	---							
	19	✓	---							
	20	✓	---							
	21	✓	---							
	22	✓	---							
	23	✓	---							
	24	✓	---							
	25	✓	---							
	26	✓	---							
	27	✓	---							
	28	✓	---							
	29	✓	---							
	30	✓	---							
	31	✓	---							

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3	"3983264".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 12:34
L2	3	"5021365".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 12:44
L3	2	"13022522"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 12:54
L4	9553	257/288,E29.255.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 12:54
L5	651	257/288,E29.255.ccls. and (substrate wafer carrier base plate) with (clean\$4 wash\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 12:55
L6	151	257/288,E29.255.ccls. and (substrate wafer carrier base plate) with (clean\$4 wash\$4) and (clean\$4 wash\$4) with (fluor\$4 hydrogen)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 12:56
L7	0	257/288,E29.255.ccls. and (substrate wafer carrier base plate) with (clean\$4 wash\$4) and (clean\$4 wash\$4) with (fluor\$4 hydrogen) and (substrate wafer carrier base plate) with (blow near dry)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 12:56
L8	4	257/288,E29.255.ccls. and (substrate	US-PGPUB;	OR	ON	2012/12/13

		wafer carrier base plate) with (clean\$4 wash\$4) and (clean\$4 wash\$4) with (fluor\$4 hydrogen) and (dry\$4 with nitrogen)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			12:57
L9	7635	257/'\$.ccls. and (substrate wafer carrier base plate) with (clean\$4 wash\$4) and (clean\$4 wash\$4) with (fluor\$4 hydrogen)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 13:01
L10	4861	257/'\$.ccls. and (substrate wafer carrier base plate) with (clean\$4 wash\$4) and (clean\$4 wash\$4) with (fluor\$4 hydrogen) and nitrogen	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 13:04
L11	2623	(Grupp Connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 13:09
L12	86	(Grupp Connelly).inv. and (substrate wafer carrier base plate) with (clean\$4 wash\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 13:10
L13	12	(Grupp Connelly).inv. and (substrate wafer carrier base plate) with (clean\$4 wash\$4 ash\$4) and (clean\$4 wash\$4 ash\$4) with (hydrogen fluorine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 13:11
L14	35265	(substrate wafer carrier base plate) with (clean\$4 wash\$4 ash\$4) and (clean\$4 wash\$4 ash\$4) with (hydrogen fluorine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 13:21
L15	447	(substrate wafer carrier base plate) with (clean\$4 wash\$4 ash\$4) and (clean\$4 wash\$4 ash\$4) with (hydrogen fluorine) and (blow\$4 near dry\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 13:22
L16	203	(substrate wafer carrier base plate) with (clean\$4 wash\$4 ash\$4) and (clean\$4 wash\$4 ash\$4) with (hydrogen fluorine) and ((blow\$4 near dry\$4) with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2012/12/13 13:22

			IBM_TDB			
L17	169	(substrate wafer carrier base plate) with (clean\$4 wash\$4 ash\$4) and (clean\$4 wash\$4 ash\$4) with (hydrogen fluorine) and ((blow\$4 near dry\$4) with (substrate wafer carrier base plate)) and ((hydrogen fluorine) with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 13:24
L18	109	(substrate wafer carrier base plate) with (clean\$4 wash\$4 ash\$4) and (clean\$4 wash\$4 ash\$4) with (hydrogen fluorine) and ((blow\$4 near dry\$4) with (substrate wafer carrier base plate)) and ((hydrogen fluorine) with (substrate wafer carrier base plate)) and ((oxide insulat\$4 passivat\$4 dielectric) with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 13:26
L19	81	(substrate wafer carrier base plate) with (clean\$4 wash\$4 ash\$4) and (clean\$4 wash\$4 ash\$4) with (hydrogen fluorine) and ((blow\$4 near dry\$4) with (substrate wafer carrier base plate)) and ((hydrogen fluorine) with (substrate wafer carrier base plate)) and ((oxide insulat\$4 passivat\$4 dielectric) with (substrate wafer carrier base plate)) and ((metal conduct\$4) with (oxide insulat\$4 passivat\$4 dielectric))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 13:28
L20	29	(substrate wafer carrier base plate) with (clean\$4 wash\$4 ash\$4) and (clean\$4 wash\$4 ash\$4) with (hydrogen fluorine) and ((blow\$4 near dry\$4) with (substrate wafer carrier base plate)) and ((hydrogen fluorine) with (substrate wafer carrier base plate)) and ((oxide insulat\$4 passivat\$4 dielectric) with (substrate wafer carrier base plate)) and ((metal conduct\$4) with (oxide insulat\$4 passivat\$4 dielectric)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/13 13:31
S1	1	13/022522	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 15:58
S2	2	"7884003".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 15:59
S3	2	"7462860".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:02
S4	2	"7084423".pn.	US-PGPUB;	OR	ON	2011/09/26

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			16:03
S5	1157	257/486,571,E21.192,E29.148.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:06
S6	465	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:06
S7	173	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier) with height	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:06
S8	84	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier) with height and (interface with metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:06
S9	68	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier) with height and (interface with metal) and (interface with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:07
S10	21	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier) with height and (interface with metal) and (interface with semiconductor) and (metal near interface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:07
S11	15	257/486,571,E21.192,E29.148.ccls. and (schottky near barrier) with height and (interface with metal) and (interface with semiconductor) and (metal near interface) and (semiconductor near junction) with metal	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/26 16:08
S12	28	257/486,571,E21.192,E29.148.ccls. and (interface near4 passivat\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2011/09/27 14:49

			IBM_TDB			
S13	15	257/486,571,E21.192,E29.148.ccls. and (interface near4 passivat\$4) and (interface near4 separat\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:50
S14	1	257/486,571,E21.192,E29.148.ccls. and (dual with passivat\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:52
S15	1	257/486,571,E21.192,E29.148.ccls. and (lower or bottom or below) near passivat\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:53
S16	809	257/'\$.ccls. and (lower or bottom or below) near passivat\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:53
S17	257	257/'\$.ccls. and (lower or bottom or below) near passivat\$4 and (upper or top or above) near passivat\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:53
S18	133	257/'\$.ccls. and (lower or bottom or below) near passivat\$4 and (upper or top or above) near passivat\$4 and (passivat\$4 with metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:54
S19	89	257/'\$.ccls. and (lower or bottom or below) near passivat\$4 and (upper or top or above) near passivat\$4 and (passivat\$4 with metal) and (passivat\$4 with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:54
S20	5	257/'\$.ccls. and (lower or bottom or below) near passivat\$4 and (upper or top or above) near passivat\$4 and (passivat\$4 with metal) and (passivat\$4 with semiconductor) and schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 14:55
S21	18	257/486,571,E21.192,E29.148.ccls. and (constant with resistance)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2011/09/27 15:03

			EPO; JPO; DERWENT; IBM_TDB			
S22	5	257/486,571,E21.192,E29.148.ccls. and (constant near3 resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:04
S23	28	257/486,571,E21.192,E29.148.ccls. and (interface near3 passivat\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:14
S24	6	257/486,571,E21.192,E29.148.ccls. and (interface near3 (metal near oxide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:20
S25	0	257/486,571,E21.192,E29.148.ccls. and migd	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:25
S26	12	257/486,571,E21.192,E29.148.ccls. and "MIGS"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:25
S27	94	257/'\$.ccls. and "MIGS"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:25
S28	98	257/'\$.ccls. and ("MIGS" or (metal near induced near gap))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:27
S29	34	257/'\$.ccls. and (metal near induced near gap)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/27 15:27
S30	31715	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or	US-PGPUB; USPAT;	OR	ON	2011/09/28 11:58

		clean\$4)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S31	5316	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 11:59
S32	0	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and ((hydrogen and fluorine) near ion) with weight	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:00
S33	0	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (((hydrogen and fluorine) near ion) with weight)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:00
S34	4	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (blow near dry)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:02
S35	0	438/'\$.ccls. and (substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (blow near dry) and (immers\$4 with (substrate or wafer or carrier or base or plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:02
S36	14	(substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (blow near dry) and (immers\$4 with (substrate or wafer or carrier or base or plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:03
S37	9	(substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (blow near dry) and (immers\$4 with (substrate or wafer or carrier or base or plate)) and metal and semiconductor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:04
S38	0	(substrate or wafer or carrier or base or plate) with (wash\$4 or clean\$4) and ((wash\$4 or clean\$4) with (hydrogen fluorine)) and (blow near dry) and (immers\$4 with (substrate or wafer or carrier or base or plate)) and metal and semiconductor and junction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:04

S39	2	"6293197".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:09
S40	15	257/486,571,E21.192,E29.148.ccls. and dipole	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:11
S41	2	257/486,571,E21.192,E29.148.ccls. and (dipole with metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:12
S42	2	257/486,571,E21.192,E29.148.ccls. and (dipole with metal) and (dipole with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:12
S43	67	257/'\$.ccls. and (dipole with metal) and (dipole with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 12:12
S44	98	257/486,571,E21.192,E29.148.ccls. and (source drain) with interface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:12
S45	48	257/486,571,E21.192,E29.148.ccls. and (source drain) with interface and (interface with metal) and (interface with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:19
S46	44	257/486,571,E21.192,E29.148.ccls. and (source drain) with interface and (interface with metal) and (interface with semiconductor) and schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:19
S47	2	"6462931".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2011/09/28 13:34

			DERWENT; IBM_TDB			
S48	3	"4723197".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:35
S49	2	"5027166".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 13:49
S50	2	"6293137".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2011/09/28 14:11
S51	1	"13022522"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:15
S52	1724	438/571.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:16
S53	70	438/571.ccls. and (substrate wafer carrier base plate) with (clean\$4 ash\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:16
S54	15	438/571.ccls. and (substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:17
S55	3	438/571.ccls. and (substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:17
S56	3	438/571.ccls. and (substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with	US-PGPUB; USPAT; USOCR;	OR	ON	2012/05/14 15:18

		hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine)	FPRS; EPO; JPO; DERWENT; IBM_TDB			
S57	877	S54(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:26
S58	865	(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:26
S59	16	(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine) and (blow near dry\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:27
S60	13	(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine) and ((blow near dry\$4) with nitrogen)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:28
S61	11	(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine) and ((blow near dry\$4) with nitrogen) and (interface with hydrogen)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:29
S62	11	(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine) and ((blow near dry\$4) with nitrogen) and (interface with hydrogen) and (interface with fluor\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:30
S63	11	(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine) and ((blow near dry\$4) with nitrogen) and (interface with hydrogen) and (interface with fluor\$4) and (grupp connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/14 15:33

EAST Search History (I nterference)

Ref	Hits	Search Query	DBs	Default	Plurals	Time
-----	------	--------------	-----	---------	---------	------

#				Operator		Stamp
S64	4	(substrate wafer carrier base plate) with (clean\$4 ash\$4) and (substrate wafer carrier base plate) with hydrogen and (substrate wafer carrier base plate) with fluorine and (metal conduct\$4) with (hydrogen fluorine) and ((blow near dry\$4) with nitrogen) and (interface with hydrogen) and (interface with fluor\$4).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2012/05/14 15:34

12/ 13/ 2012 1:53:10 PM
C:\ Users\ mharrison1\ Documents\ EAST\ Workspaces\ 13022522.wsp

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

27571 7590 01/02/2013
TAREK N. FAHMI, APC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

13/022,522 02/07/2011 Daniel E. Grupp 40003771-0003-453 6852

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$885	\$300	\$0	\$1185	04/02/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
HARRISON, MONICA D	2896	438-571000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

1 Tarek N. Fahmi, APC

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Acorn Technologies, Inc.

La Jolla, California

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 505798 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Tarek N. Fahmi/

Date April 2, 2013

Typed or printed name Tarek N. Fahmi

Registration No. 41,402

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal

Application Number:	13022522			
Filing Date:	07-Feb-2011			
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS			
First Named Inventor/Applicant Name:	Daniel E. Grupp			
Filer:	Tarek N. Fahmi			
Attorney Docket Number:	40003771-0003-453			
Filed as Small Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	2501	1	890	890
Publ. Fee- Early, Voluntary, or Normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1190

Electronic Acknowledgement Receipt

EFS ID:	15414902
Application Number:	13022522
International Application Number:	
Confirmation Number:	6852
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-453
Receipt Date:	02-APR-2013
Filing Date:	07-FEB-2011
Time Stamp:	17:38:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1190
RAM confirmation Number	4561
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
-----------------	----------------------	-----------	-------------------------------------	------------------	------------------

1	Issue Fee Payment (PTO-85B)	40003771-0003- DC2_Issue_Fee_Transmittal_04 _02_2013.pdf	102904 0ff27d74ba1d9c0b64d7916562d537113a4a 009b	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31657 ea149ef33211e789e9287cde5873b4402f54 3af9	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			134561		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Receipt date: 03/25/2011 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13022522	13022522 - GAU: 2896
	Filing Date		2011-02-07	
	First Named Inventor	Daniel E. Grupp		
	Art Unit		2811	
	Examiner Name			
	Attorney Docket Number		40003771-0003-453	

/M.D.H./	9	5578848		1996-11-26	Kwong, et al.	
	10	5596218		~~01-21-1997~~ ~~2000-04-10~~	Soleimani, et al.	
Change(s) applied	11	5612567		1997-03-18	Baliga	
to document,	12	5663584		1997-09-02	Welch	
/D.G./	13	5801398		1998-09-01	Hebiguchi	
2/12/2013	14	5888891		1999-03-30	Gould	
	15	5939763		1999-08-17	Hao, et al.	
	16	6037605		2000-03-14	Yoshimura	
	17	6096590		2000-08-01	Chan, et al.	
	18	6150286		2000-11-21	Sun et al.	
	19	6198113		2001-03-06	Grupp, Daniel E.	



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/022,522	04/30/2013	8431469	40003771-0003-453	6852

27571 7590 04/10/2013
TAREK N. FAHMI, APC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Daniel E. Grupp, Palo Alto, CA;
Daniel J. Connelly, Redwood City, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.