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	Practitioners associated with the Customer Number	27571	

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications and reexamination proceedings assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application(s), reexamination proceeding(s) and/or patent(s) listed below to the address associated with Customer Number 27571

Assignee Name and Address:

Arcam Technologies, Inc.
1250 Prospect Street, Suite 475
La Jolla, California 92037

A statement under 37 CFR 3.73(b) is attached.

List of application(s), reexamination proceeding(s) and/or patent(s).

See Attached List

SIGNATURE OF ASSIGNEE OF RECORD

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	Joseph J. Daniele	Date: 3/14/2012
Name	Joseph J. Daniele	Telephone: 858-861-1582
Title	Chief Operating Officer	

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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: ACORN TECHNOLOGIES, INC.

Application No./Patent No.: 7,884,003 Filed/Issue Date: February 8, 2011

Titled: Method for Depinning the Fermi Level of a Semiconductor at an Electrical Junction and Devices Incorporating Such Junctions

ACORN TECHNOLOGIES, INC. , a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. [X] the assignee of the entire right, title, and interest in;

2. [ ] an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or

3. [ ] the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. [X] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 022077, Frame 0447, or for which a copy therefore is attached.

OR

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

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[ ] Additional documents in the chain of title are listed on a supplemental sheet(s).

[X] As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Tarek N. Fahmi/ 2012-07-18
Signature Date

Attorney of Record
Printed or Typed Name Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION (37 CFR 1.63)

☐ Declaration Submitted with Initial Filing

OR

☒ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16(e)) required)

Attorney Docket Number	40003771-0003-403
First Named Inventor	Daniel E. Grupp
COMPLETE IF KNOWN	
Application Number	12/197,996
Filing Date	August 25, 2008
Art Unit	2811
Examiner Name	Not Yet Assigned

As a below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below, next to my name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

(Title of the Invention)

the specification of which

☐ is attached hereto.

OR

☒ was filed on (if applicable):

08/25/2008 as United States Application Number 12/197,996

as PCT International Application Number

and was amended on (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment specifically referred to above.

I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application. I do not know and do not believe that the claimed invention was in public use or on sale in the United States of America more than one year prior to this application, nor do I know or believe that the invention has been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

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I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, or inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s):

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No
			☐	☐ Yes ☐ No

Appointment of Practitioners:
I hereby appoint the practitioners associated with Customer Number: 26263 as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the U.S. Patent and Trademark Office connected herewith.

If this patent application is assigned, then the undersigned hereby authorizes the patent attorneys and patent agents named herein to accept and follow instructions from the assignee(s) as to any action to be taken in the United States Patent and Trademark Office regarding this application without direct communication between the patent attorneys and patent agents and the undersigned. In the event of a change in the persons from whom instructions may be taken, at least one patent attorney or patent agent named herein will be so notified by the undersigned.

Correspondence:
Direct all correspondence to Customer Number 26263

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR: ☐ A petition has been filed for this undersigned inventor

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Inventor's Signature [signature] Date 12 DEC 2005

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NAME OF SECOND INVENTOR: ☐ A petition has been filed for this undersigned inventor

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Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State, Country) *(Country)*

Mailing Address _____

NAME OF FOURTH INVENTOR: ☐ A petition has been filed for this undersigned inventor

Full Name: _____
(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State, Country) *(Country)*

Mailing Address _____

NAME OF FIFTH INVENTOR: ☐ A petition has been filed for this undersigned inventor

Full Name: _____
(First, Middle [if any], Family Name (or Surname), and Suffix [if any])

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____
(City, State, Country) *(Country)*

Mailing Address _____

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

INVENTORS

DANIEL E. GRUPP

DANIEL J. CONNELLY

Attorney Docket No.: 40003771-0003-463

Correspondence via: Customer No. 27571
866-877-4883

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

RELATED APPLICATIONS

[0001] The present application is a CONTINUATION of co-pending U.S. Patent Application No. 13/022,522, filed 2/7/2011, which is a DIVISIONAL of U.S. Patent Application 12/197,966, filed 8/25/2008, now U.S. Patent 7,884,003, which is a DIVISIONAL of U.S. Patent Application 11/181,217, filed 7/13/2005, now U.S. Patent 7,462,860, which is a CONTINUATION of U.S. Patent Application 10/217,758, filed 8/12/2002, now U.S. Patent 7,084,423, which is related to U.S. Patent Application 10/342,576, filed 1/14/2003, now U.S. Patent 6,833,556, all of which are hereby incorporated by reference.

FIELD OF THE INVENTION

[0002] The invention relates generally to semiconductor processing and semiconductor devices. More particularly, the invention relates to a process for depinning the Fermi level of a semiconductor at a metal-interface layer-semiconductor junction and to devices that employ such a junction.

BACKGROUND

[0003] One of the most basic electrical junctions used in modern devices is the metal-semiconductor junction. In these junctions, a metal (such as aluminum) is brought in contact with a semiconductor (such as silicon). This forms a device (a diode) which can be inherently rectifying; that is, the junction will tend to conduct current in one direction more favorably than in the other direction. In other cases, depending on the materials used, the junction may

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be ohmic in nature (i.e., the contact may have negligible resistance regardless of the direction of current flow). Grondahl and Geiger first studied the rectifying form of these junctions in 1926, and by 1938 Schottky had developed a theoretical explanation for the rectification that was observed.

[0004] Schottky's theory explained the rectifying behavior of a metal-semiconductor contact as depending on a barrier at the surface of contact between the metal and the semiconductor. In this model, the height of the barrier (as measured by the potential necessary for an electron to pass from the metal to the semiconductor) was postulated as the difference between the work function of the metal (the work function is the energy required to free an electron at the Fermi level of the metal, the Fermi level being the highest occupied energy state of the metal at T = 0) and the electron affinity of the semiconductor (the electron affinity is the difference between the energy of a free electron and the conduction band edge of the semiconductor). Expressed mathematically:

$$\phi_B = \phi_M - \chi_S \qquad [1]$$

where Φ_B is the barrier height, Φ_M is the work function of the metal and χ_S is the electron affinity of the semiconductor.

[0005] Not surprisingly, many attempts were made to verify this theory experimentally. If the theory is correct, one should be able to observe direct variations in barrier heights for metals of different work functions when put in contact with a common semiconductor. What is observed, however, is not direct scaling, but instead only a much weaker variation of barrier height with work function than implied by the model.

[0006] Bardeen sought to explain this difference between theoretical prediction and experimental observation by introducing the concept that surface states of the semiconductor play a role in determining the barrier height. Surface states are energy states (within the bandgap between the valence and conduction bands) at the edge of the semiconductor crystal that arise from incomplete covalent bonds, impurities, and other effects of crystal termination. **Figure 1** shows a cross-section of an un-passivated silicon surface labeled 100. The particular

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silicon surface shown is an Si(100) 2x1 surface. As shown, the silicon atoms at the surface, such as atom 110, are not fully coordinated and contain un-satisfied dangling bonds, such as dangling bond 120. These dangling bonds may be responsible for surface states that trap electrical charges.

[0007] Bardeen's model assumes that surface states are sufficient to pin the Fermi level in the semiconductor at a point between the valence and conduction bands. If true, the barrier height at a metal-semiconductor junction should be independent of the metal's work function. This condition is rarely observed experimentally, however, and so Bardeen's model (like Schottky's) is best considered as a limiting case.

[0008] For many years, the cause underlying the Fermi level pinning of the semiconductor at a metal-semiconductor junction remained unexplained. Indeed, to this day no one explanation satisfies all experimental observations regarding such junctions. Nevertheless, in 1984, Tersoff proposed a model that goes a long way towards explaining the physics of such junctions. See J. Tersoff, "Schottky Barrier Heights and the Continuum of Gap States," Phys. Rev. Lett. 52 (6), Feb. 6, 1984.

[0009] Tersoff's model (which is built on work by Heine and Flores & Tejedor, and see also Louie, Chelikowsky, and Cohen, "Ionicity and the theory of Schottky barriers," Phys. Rev. B 15, 2154 (1977)) proposes that the Fermi level of a semiconductor at a metal-semiconductor interface is pinned near an effective "gap center", which is related to the bulk semiconductor energy band structure. The pinning is due to so-called metal induced gap states (MIGS), which are energy states in the bandgap of the semiconductor that become populated due to the proximity of the metal. That is, the wave functions of the electrons in the metal do not terminate abruptly at the surface of the metal, but rather decay in proportion to the distance from that surface (i.e., extending inside the semiconductor). To maintain the sum rule on the density of states in the semiconductor, electrons near the surface occupy energy states in the gap derived from the valence band such that the density of states in the valence band is reduced. To maintain charge neutrality, the highest occupied state (which defines the Fermi

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level of the semiconductor) will then lie at the crossover point from states derived from the valence band to those derived from the conduction band. This crossover occurs at the branch point of the band structure. Although calculations of barrier heights based on Tersoff's model do not satisfy all experimentally observed barrier heights for all metal-semiconductor junctions, there is generally good agreement for a number of such junctions.

[0010] One final source of surface effects on diode characteristics is inhomogeneity. That is, if factors affecting the barrier height (e.g., density of surface states) vary across the plane of the junction, the resulting properties of the junction are found not to be a linear combination of the properties of the different regions. In summary then, a classic metal-semiconductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, MIGS and inhomogeneities.

[0011] The importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction. Thus, if one were able to control or adjust the barrier height of a metal-semiconductor junction, one could produce electrical devices of desired characteristics. Such barrier height tuning may become even more important as device sizes shrink even further. Before one can tune the barrier height, however, one must depin the Fermi level of the semiconductor. As discussed in detail below, the present inventors have achieved this goal in a device that still permits substantial current flow between the metal and the semiconductor.

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SUMMARY OF THE INVENTION

[0012] The present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal – interface layer – semiconductor junction, there exist corresponding minimum specific contact resistances. The interface layer thickness corresponding to this minimum specific contact resistance will vary depending upon the materials used, however, it is a thickness that allows for depinning the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor when the junction is biased (e.g., forward or reverse biased). By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the effect of MIGS has been overcome, or at least reduced, by displacing the semiconductor a sufficient distance from the metal. Minimum specific contact resistances of less than or equal to approximately 10 $\Omega - \mu m^2$ or even less than or equal to approximately 1 $\Omega - \mu m^2$ may be achieved for such junctions in accordance with the present invention.

[0013] Thus, in one embodiment, the present invention provides an electrical device in which an interface layer is disposed between and in contact with a metal and a silicon-based semiconductor and is configured to depin the Fermi level of the semiconductor while still permitting current flow between the metal and the semiconductor when the electrical device is biased. The specific contact resistance of the electrical device is less than approximately 10 $\Omega - \mu m^2$. The interface layer may include a passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and sometimes also includes a separation layer. In some cases, the interface layer may be essentially a monolayer (or several monolayers) of a semiconductor passivating material.

[0014] In another embodiment, the interface layer is made up of a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material, for example ammonia

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(NH_3), nitrogen (N_2) or unbound gaseous nitrogen (N) generated from a plasma process. In such cases, the interface layer may be fabricated by heating the semiconductor while in a vacuum chamber and exposing the semiconductor to the nitrogenous material.

[0015] A further embodiment of the present invention provides for depinning the Fermi level of a semiconductor in an electrical junction through the use of an interface layer disposed between a surface of the semiconductor and a conductor. The interface layer preferably (i) is of a thickness sufficient to reduce effects of MIGS in the semiconductor, and (ii) passivates the surface of the semiconductor. Despite the presence of the interface layer, significant current may flow between the conductor and the semiconductor because the thickness of the interface layer may be chosen to provide a minimum (or near minimum) specific contact resistance for the junction. As indicated above, the interface layer may include a passivating material such as a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride.

[0016] Further embodiments of the present invention provide a junction between a semiconductor and a conductor separated from the semiconductor by an interface layer configured to allow a Fermi level of the conductor to (i) align with a conduction band of the semiconductor, (ii) align with a valence band of the semiconductor, or (iii) to be independent of the Fermi level of the semiconductor. In some or all of these cases, current may flow between the conductor and the semiconductor when the junction is biased because the interface layer has a thickness corresponding to a minimum or near minimum specific contact resistance for the junction. For example, specific contact resistances of less than or equal to approximately 2500 $\Omega-\mu m^2$, 1000 $\Omega-\mu m^2$, 100 $\Omega-\mu m^2$, 50 $\Omega-\mu m^2$, 10 $\Omega-\mu m^2$ or even less than or equal to 1 $\Omega-\mu m^2$ may be achieved.

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BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0017] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0018] **Figure 1** shows a cross-section of an un-passivated silicon surface containing surface silicon atoms with dangling bonds.

[0019] **Figure 2** illustrates various energy levels for metals and semiconductors and is labeled to show the work function of a metal and the electron affinity of a semiconductor.

[0020] **Figure 3** shows an energy band diagram for a conventional metal – *n*-type semiconductor junction and also illustrates the concept of a depletion region formed in the semiconductor when the materials are brought into contact with one another.

[0021] **Figure 4** illustrates band bending at a conventional metal – *n*-type semiconductor junction.

[0022] **Figure 5** shows a semiconductor device containing a semiconductor material having a surface across which electrical current flows during operation of the semiconductor device, and containing an interface layer formed on the surface according to one embodiment of the present invention.

[0023] **Figure 6** shows an electrical junction containing an interface layer that is disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

[0024] **Figures 7a, 7b, 7c and 7d** show relationships between Fermi energy, conduction-band energy, and valence-band energy for an unpassivated Schottky diode, a passivated Schottky diode in which MIGS are not removed, an unpassivated Schottky diode in which

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MIGS are removed and a passivated Schottky diode in which MIGS are removed according to one embodiment of the present invention, respectively.

[0025] **Figure 8** shows a curve of interface layer resistance versus interface layer thickness for an electrical junction containing an interface layer disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

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DETAILED DESCRIPTION

[0026] Described herein are processes for depinning the Fermi level of a silicon-based semiconductor (e.g., Si, SiC or SiGe) at a metal-semiconductor junction as well as devices that use such a junction. As more fully discussed below, an interface layer is introduced between the semiconductor and the metal. The interface layer functions to passivate the semiconductor surface (that is, terminate dangling bonds that may otherwise be present at the semiconductor surface so as to assure chemical stability of the surface) and to displace the semiconductor from the metal so as to reduce the effect of MIGS.

[0027] As discussed more fully below, the present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal – interface layer – semiconductor junction, there exist corresponding minimum specific contact resistances. Indeed, minimum specific contact resistances of less than or equal to approximately 10 $\Omega - \mu m^2$ or even less than or equal to approximately 1 $\Omega - \mu m^2$ may be achieved for such junctions in accordance with the present invention. To achieve such low contact resistances, a metal that has a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function that is near the valence band for p-type semiconductors, is selected.

[0028] The Schottky barrier in such junctions is already minimized, meaning that it is much less than the Schottky barrier presented by a junction in which the Fermi level is pinned, generally near the middle of the semiconductor's bandgap. The current versus voltage (IV) characteristic of these junctions is non-linear, generally having a slope that increases as the voltage increases, such that the derivative of current with respect to voltage is increasing with voltage. This results in a decreasing differential resistance *(dV/dI)* and a decreasing resistance *(V/I)*. Thus, a junction that has high resistance or high differential resistance near the origin of the IV characteristic (zero volts) may have significantly lower resistance or lower differential resistance at higher voltages.

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[0029] The present invention achieves low resistance and low differential resistance near the origin of the current-voltage characteristic for a metal – interface layer – semiconductor junction. Generally, the voltage around the origin should be less than about 100 mV, or more preferably less than about 10 mV for purposes of measuring, determining, or utilizing such junctions of low resistance. At higher voltages, the junction resistance will be even lower. It is thus a feature of the present invention to set an upper bound on the resistance of a contact, where the upper bound occurs at low voltages.

[0030] It is further noted that in junctions where the Schottky barrier is minimized as described above, such that the Fermi level at the junction interface at zero volts lies at or near the conduction band edge or valence band edge (for *n*- and *p*-type semiconductors, respectively), the *IV* characteristic will be nearly symmetric, especially at low voltage. In this case, the term "forward bias" is not defined in the usual sense of a diode wherein forward bias corresponds to the direction of bias for which greater current flows. Thus, in determining or utilizing low resistance junctions of the present invention, the voltage may be either positive or negative.

[0031] It is also possible (in accordance with a further embodiment of the present invention) to make junctions where the Schottky barrier is higher than it would be if the Fermi level at the junction interface were pinned, usually around mid-gap of the semiconductor. Such junctions are formed in the present invention between a metal with a workfunction near or substantially equal to the conduction band edge of a *p*-type semiconductor, or between a metal with a workfunction near or substantially equal to the valence band edge of an *n*-type semiconductor. These junctions are diodes, in that little current will flow if the *n*-type (*p*-type) semiconductor is biased positive (negative) with respect to the metal, and large currents will flow if the voltage is reversed. The low-current flow state is referred to as reverse bias, and the high-current flow state is referred to as positive bias.

[0032] Low resistance in the case of a diode is only relevant in forward bias conditions. In junctions created in accordance with the present invention the resistance contribution of the

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interface layer is smaller than the resistance due to the Schottky barrier. That is, in forward bias conditions for junctions created in accordance with the present invention, the transport of charge is limited mainly by the thermal emission of carriers from the semiconductor over the barrier at the interface, and not by the tunneling through the interface dielectric. Thus, low resistance in the case of a diode refers to a resistance lower than the resistance presented by the Schottky barrier.

[0033] In certain applications of diodes, the ability to withstand high reverse biases may be more desirable than high current flow in forward bias. These applications would be considered high voltage/low power applications. In such cases, a low resistance is not essential, and junctions created in accordance with still another embodiment of the present invention provide high-voltage diodes capable of withstanding voltages higher than could otherwise be achieved if the Fermi level of the semiconductor in the junction were pinned.

[0034] The present invention is discussed below in terms of presently preferred embodiments thereof, however, this discussion is not meant to limit the scope of the invention. By studying the present disclosure, others of ordinary skill in the art may recognize equivalent procedures, materials or structures that can be substituted for those described herein to achieve the same effect. The reader is advised and reminded that the use of such equivalents is deemed to be within the scope of the present invention. For example, where the discussion refers to well-known structures and devices, block diagrams are used, in part to demonstrate the broad applicability of the present invention to a wide range of such structures and devices.

I. Introduction and Definitions

[0035] The present discussion makes use of terms that, although well known in the art, may not be familiar to all readers. Therefore, before beginning a detailed discussion of the present invention, it is helpful to define certain terms and concepts. To understand the properties of metal-semiconductor junctions and the impact of the present invention, one must refer to some important energy scales, which are shown graphically in **Figure 2**. The so-called vacuum

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level (E_0) represents the minimum energy that an electron needs to possess in order to completely free itself from a metal or semiconductor. For a metal, the Fermi level (E_F) represents the highest occupied energy level for the material. That is, nearly all energy states below the Fermi level are filled, while nearly all states above the Fermi level are empty. The work function of the metal (Φ_M) is then defined as the energy required to free an electron at the Fermi level and mathematically it is the difference between the vacuum level and the Fermi level. The work function is an invariant bulk property of the metal.

[0036] As illustrated in the diagram, semiconductors also have a Fermi level (E_F) and a work function (Φ_S), however, the work function is not an invariant property of the semiconductor. Because the Fermi level varies depending on the doping level in the semiconductor (i.e., the relative amounts of impurities introduced into the semiconductor crystal which change the electron and hole carrier concentrations), a separate parameter, the electron affinity (χ_S), is defined. The electron affinity is an invariant property of the semiconductor and is the difference between the vacuum level and the conduction band edge of the semiconductor. In a semiconductor, almost all energy states are filled in the valence band (E_V) while the conduction band (E_C) is almost empty.

[0037] Now consider a conventional junction between a metal and an *n*-type semiconductor that has a work function smaller than the work function of the metal (i.e., $\Phi_S < \Phi_M$). An *n*-type semiconductor is one in which electrons are the majority charge carriers (in *p*-type semiconductors, holes are the majority charge carrier). As shown in **Figure 3**, because the Fermi level in the semiconductor is higher than the Fermi level in the metal, electrons transfer from the semiconductor 310 to the metal 320 when the materials are brought into contact. Thus, a depletion region (i.e., a region in which there are no free charge carriers) 330 forms near the junction interface 340.

[0038] The formation of the depletion region gives rise to an electric field and so-called "band bending", as one approaches the junction interface from the semiconductor side (see **Figure 4**). The band bending creates an energy barrier (discussed above) that blocks further

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transfer of electrons into or out of the semiconductor. Similar barriers are formed for a junction between a metal and a *p*-type semiconductor when the work function of the metal is less than the work function of the semiconductor. However, in the case of a metal– *n*-type semiconductor junction in which the work function of the semiconductor is greater than that of the metal or a metal–*p*-type semiconductor junction in which the work function of the semiconductor is less than that of the metal, no such energy barriers are created and the contact is said to be ohmic in nature.

[0039] As discussed above, although Schottky first postulated that the height of the energy barrier (Φ_b) formed at a metal-semiconductor junction was simply the difference between the work function of the metal and the electron affinity of the semiconductor, experiments have not verified this relationship. Instead a more complex explanation that takes into account the effects of surface defect states, inhomogeneities and MIGS appears to provide more accurate estimates of barrier heights by explaining the pinning of the Fermi level in the semiconductor. The present inventors have created a technique which is believed to depin the Fermi level of a Si-based semiconductor at a junction with a metal (and thus allow for control or tuning of the barrier height) by both passivating the semiconductor surface (to eliminate or at least reduce the effects of surface states and possibly inhomogeneities) and displacing the metal from the semiconductor (to eliminate or at least reduce the effects of MIGS). This depinning is achieved by introducing an interface layer between the semiconductor and the metal to create a semiconductor -- interface layer -- metal junction, which still permits significant current to flow between the metal and the semiconductor when the junction is forward biased.

[0040] This latter point is important. As discussed further below, for contacts where the energy bands of the semiconductor and the conductor align (i.e., where the Fermi level of the conductor aligns with the conduction or valence band of the semiconductor depending on semiconductor type and/or contact application), if the interface layer is too thin, the specific contact resistance of the junction increases because of the presence of MIGS, resulting in an increased barrier height; thus, current flow is hampered. Conversely, if the interface layer is

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too thick, the specific contact resistance is again increased and one gets low current across the junction because of tunneling limitations. The present invention achieves an interface layer that is thick enough to reduce or eliminate the effect of MIGS, while still thin enough to permit significant current flow.

II. Passivation of Semiconductor Surfaces

[0041] A common processing operation performed during semiconductor device fabrication is silicon surface passivation. Surface passivation (whether by an oxide or another material) chemically neutralizes and physically protects the underlying silicon. For example, exposing a silicon surface to oxygen (under the appropriate conditions to grow a protective film of silicon dioxide) will allow the oxygen to react with the dangling bonds of the silicon surface to form covalent bonds that satisfy the surface silicon atoms' valency and render the surface fully coordinated. These covalent bonds provide chemical stability to the silicon surface. The covalent bonds also tie up unbound charges that exist on the silicon surface as a result of the discontinuation of the semiconductor crystal at the surface.

[0042] However, passivation with silicon dioxide has several significant disadvantages. For example, silicon dioxide is a dielectric insulator that poses a significant barrier to the flow of current. Accordingly, a layer of silicon dioxide deposited or grown on a silicon surface may significantly reduce the ability for electrical current to flow through that surface. As a result, the use of silicon dioxide has been limited in practicality to surfaces external to the active region of semiconductor devices through which current passes during device operation (e.g., as a gate oxide layer). This disadvantage is compounded by the fact that the silicon dioxide grows very rapidly and readily on the silicon surface so that it is difficult to limit the growth to a thin layer. Silicon dioxide is also a poor diffusion barrier to semiconductor dopants such as boron.

[0043] Instead of making use of silicon dioxide then, in one embodiment the present inventors utilize a nitrided semiconductor surface to provide chemical passivation. That is, a

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nitride layer is introduced to passivate the semiconductor surface by eliminating or at least reducing the effects of surface states and possibly inhomogeneities. The nitride layer also displaces the metal from the semiconductor and eliminates or at least reduces the effects of MIGS. The result of introducing the nitride layer as an interface between the semiconductor and the metal is a depinning of the Fermi level of the semiconductor. When the Fermi level of the semiconductor is depinned, the Fermi level of the metal at the interface will be that of the bulk metal, and will not be dependent upon the interface. In addition to the above, the present inventors propose techniques for providing non-insulating, passivated semiconductor surfaces using materials other than nitrogen; for example, oxides, hydrides, arsenides and/or fluorides.

[0044] These developments have wide applicability in connection with the fabrication of Schottky diodes, Schottky-barrier transistors and other electrical components. For example, in Schottky diodes, the ability to control the energy barrier height at the diode junction is important if the device is to be tailored to specific applications. Use of the present techniques allows for tuning of the barrier height. Further, for other three-terminal devices with Schottky-barrier-isolated channels, control of device characteristics is made possible through the present invention by allowing *n*- and *p*-type devices to be fabricated without dopants, relying instead on the use of metals with different work functions.

[0045] **Figure 5** shows a semiconductor device 510 that contains a semiconductor 530 and an interface layer 520 formed on a surface 540 of the semiconductor in accordance with the present invention. The terms semiconductor device, microelectronic device, monolithic device, chip, and integrated circuit are often used interchangeably in this field. Any or all such devices may each contain an interface layer formed on a semiconductor surface in accordance with the present invention.

[0046] The semiconductor 530 contains a semiconductor material. The term semiconductor material refers to a material having a bandgap that is greater than about 0.1 eV and less than about 4 eV. The term bandgap refers to an energy gap of forbidden energy levels separating the conduction band, which is an upper energy band that is mostly devoid of electrons and

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wherein electrons can conduct, and the valence band, which is an energy band that is mostly filled with electrons and wherein electrons cannot conduct. The semiconductor material may have a wide range of doping levels including no doping at all.

[0047] The semiconductor 530 has a surface 540 that is passivated by the interface layer 520. In this context (and as used elsewhere herein) the term passivation means the elimination or at least the reduction of the effects of surface states due to defects or dangling bonds of the semiconductor surface 540. Note that passivation does not, as a practical matter, require that all surface states be eliminated. Rather, it is the effect of surface states on the device properties that is limited or eliminated in passivation. Note further that the presence of MIGS may be regarded as a surface state, however, as used herein the term passivation is not meant to infer the elimination of MIGS (though in some cases, a passivation layer may have sufficient thickness to provide a separation layer between the semiconductor and the metal sufficient to reduce or eliminate MIGS). The semiconductor 530 is operable to be electrically coupled with a first voltage associated with the semiconductor device 510 and to conduct electrical current 550 across the passivated surface 540.

[0048] The interface layer 520 is formed on the semiconductor 530 and may contain a passivation material that bonds to the semiconductor material by way of a covalent (or other) bond formed between the passivation material and the semiconductor material. For example, an atom of passivation material may covalently bond with a dangling bond of a surface silicon atom to fully coordinate the silicon atom and thereby help passivate the silicon atom. In some cases, the passivation material may be the sole component of the interface layer 520, while in other cases the interface layer 520 may be a compound layer that includes both a passivation layer and a separation layer. That is, the interface layer serves to (i) chemically passivate the semiconductor surface 540, and (ii) displace the semiconductor from the metal sufficiently to eliminate or at least reduce the effect of MIGS. As explained below, this may necessitate including a separation layer in addition to a passivation layer within the interface layer, depending on the passivation material selected. Of course, the combination of the passivation

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layer and the separation layer must be sufficiently thin to permit the low specific contact resistances described herein.

[0049] Different passivation materials are contemplated. According to one embodiment, the interface layer 520 is formed using a material that is preferably selected from the group consisting of hydrogen (H), oxygen (O), nitrogen (N), arsenic (As), and fluorine (F) (that is, the interface layer 520 may include a nitride, an oxide, a hydride, an arsenide and/or a fluoride). Other materials having chemical characteristics or valences similar to these materials may also be used. Note that distinct separation layers (i.e., in addition to the passivation layer(s)) may be needed where H, As, or F passivation layers are used, as these tend to form monolayer coverage, rather than a layer of a compound with Si of process-dependent thickness. In contrast, passivation layers made using N and/or O may not require distinct separation layers, as these elements may form a layer of a compound of Si with a thickness that can be varied depending on processing.

[0050] Different amounts of passivation material are contemplated to be useful for different embodiments of the present invention. Often, the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm. For example, depending upon the particular implementation, the thickness may be less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, may be the thickness corresponding to a single layer or monolayer of passivation material that is bonded to the semiconductor surface, or may even be the number of atoms of passivation material required to passivate substantially all the dangling bonds associated with the semiconductor surface 540.

[0051] In some cases, passivation of the semiconductor surface 540 will include removing (or terminating) dangling bonds located proximate to the surface of the semiconductor material, including those at the surface as well as those within a few molecular dimensions from the surface. This process may stabilize the surface of the semiconductor material and may improve the controllability of subsequent fabrication operations. Passivation may also reduce the density of surface states that may exist at the semiconductor surface as a result of the

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discontinuation of the semiconductor crystal at the surface. This may improve consistency and performance of the semiconductor device, inasmuch as such states are known to interfere with proper device operation. For example, they may provide surface charge states that result in a pinning of the Fermi level.

III. Forming Interface Layers

[0052] Exemplary methods for forming interface layers to provide (i) passivation of semiconductor surfaces, and (ii) displacement of the semiconductor from the metal to eliminate or at least reduce of the effects of MIGS within the semiconductor when in the presence of the metal (collectively referred to herein as depinning the Fermi level of the semiconductor) with hydrogen, fluorine or nitrogen are presented below to further illustrate the concepts of the present invention. Other passivation materials may include arsenic, oxygen or an oxynitride, and in some cases such passivation layers are combined with separation layers (e.g., made of an oxide) to complete the interface layer.

A. Hydrogen And Fluorine

[0053] An interface layer may contain hydrogen, fluorine, or both hydrogen and fluorine (e.g., in the form of a hydride and/or a fluoride). One method for forming an interface layer on a semiconductor surface with hydrogen and fluorine includes cleaning the semiconductor substrate with a cleaning solution, immersing the cleaned substrate in a hydrogen fluoride solution (or other liquid containing hydrogen and fluorine ions) having an effective concentration typically between about 1%-50% by weight, waiting an effective period of time, typically between about several seconds and about 5 minutes, removing the substrate from the hydrogen fluoride solution, optionally rinsing the substrate in deionized water, and blow-drying the substrate with nitrogen. Such a method may form an interface layer containing hydrogen and fluorine that are bonded (e.g., covalently) to the semiconductor surface.

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[0054] It should be noted that long rinses in deionized water, generally longer than about 30 seconds, might remove the hydrogen passivation. Thus, deionized water rinses might advantageously be kept to less than about 30 seconds to maintain the hydrogen passivation of the surface. Also, the higher the concentration of the hydrogen fluoride during the immersion, the greater the concentration of fluorine passivation. Finally, methods are also contemplated where the ratio of hydrogen to fluorine passivation is altered by removing either the hydrogen or the fluorine.

[0055] An interface layer formed in this fashion may be best suited for applications where a subsequent metal layer is deposited over the interface layer in a generally non-invasive fashion, for example using a thermally evaporated source. Experiments by the present inventors to date suggest that using other approaches (e.g., plasma deposition) may cause damage to the thin (e.g., monolayer thick) interface layer contemplated as part of the present invention.

B. Nitrogen

[0056] In a further embodiment, an interface layer may contain nitrogen (e.g., in the form of silicon nitride). One method for forming an interface over a semiconductor surface with nitrogen includes heating a substrate containing the semiconductor surface in the presence of a nitrogenous material (that is, a gas or other material containing nitrogen). For example, a substrate containing an exposed silicon surface may be annealed at a temperature between about 300°C and about 750°C, which is lower than temperatures conventionally used for Rapid Thermal Nitridation (RTN), under a gaseous ambient having, for example, ammonia (NH_3) at some effective partial pressure. By exposed, we mean a clean surface, free of everything except silicon. Such a method may form an interface layer containing nitrogen, often in the form of a nitride, bonded to the semiconductor surface. Note that the present inventors have observed indications suggesting that in these low temperature conditions interface layer growth is self-limiting, depending only on temperature.

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[0057] According to another embodiment, an interface layer that includes nitrogen may be formed on an exposed surface of a semiconductor material by a method that includes heating a semiconductor material to a substantially high temperature under vacuum and exposing the semiconductor material to a substantially small amount of a nitrogenous material, such as ammonia. The method may include placing a semiconductor having an exposed semiconductor surface in a heating chamber, pulling a vacuum of less than about one millionth of a Torr, or more favorably an ultra high vacuum of less than 10^{-9} Torr, and then heating the semiconductor in the heating chamber to a substantially high temperature. The higher the vacuum, the longer the substrate may be heated without growth of an oxide from residual oxygen or water in the chamber. Thus, the process may include heating the semiconductor to a temperature that is between about 900°C and about 1000°C, or higher, in an inert ambient. As desired, the semiconductor may be exposed to hydrogen gas, or an equivalent, to reduce any native oxide on the semiconductor. These high temperatures may provide for greater passivation of the semiconductor surface as compared with results that may be achieved at lower temperatures.

[0058] Then, the heated semiconductor may be exposed to a substantially small amount of a nitrogenous material, such as ammonia. This may include exposing the semiconductor surface to ammonia for a substantially short period of time. For example, the surface may be subjected to a burst or pulse of ammonia lasting for a time period between about 0.5 seconds and about 5 seconds. Alternatively, the surface may be exposed to a controlled, small amount of ammonia over an arbitrarily longer period of time. In this way, the substantially small amount of ammonia will react with the surface to form a nitrogenous interface layer, such as a nitride layer, thereon and then further growth of the interface layer will cease. Then the semiconductor may be cooled from the substantially high temperature to ambient temperature and removed from the heating chamber. Further annealing of the substrate and the grown nitride layer may also be performed in the vacuum chamber before removal, at a substantially elevated temperature between about 700°C and 1000°C, or higher.

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[0059] Advantageously, it has been unexpectedly observed that a process such as that described above and incorporating substantially high temperature exposure for substantially short periods may be used to controllably form thin yet effective interface layers. That is, the present inventors have observed that in the creation of thin interface layers that include nitrogenous materials, temperature appears to be a dominant factor in controlling thickness. For example, by such methods effective interface layers may be formed having a thickness that is less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the semiconductor surface.

[0060] Further, thin interface layers may be advantageously grown on a semiconductor in the presence of nitrogen gas, or other inert nitrogen-containing gas. The reaction rate of a semiconductor such as silicon with nitrogen gas is significantly lower than that of a reactive nitrogen-containing gas such as ammonia. The slow growth rate may be desirable for better control of the growth of films of nitrogen on a semiconductor of a thickness of less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the silicon surface.

IV. Diodes Containing Passivated Semiconductor Surfaces

[0061] Diodes made from Schottky barriers (i.e., asymmetric electrical potentials formed at a junction between a metal and a semiconductor) are widely used in rectifiers in power supply and control applications. As used herein, the terms Schottky diode, metal-semiconductor junction diode, diode, and rectifier are all related and appear in order from more specific at the left to more general at the right. Likewise, the terms Schottky barrier, metal-semiconductor barrier, conductor-semiconductor junction, and multi-material junction are all related and

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appear in order from more specific at the left to more general at the right. The term Schottky diode will be used to refer to a diode containing a Schottky barrier.

[0062] As mentioned above, the present inventors have devised a scheme to control or adjust a Schottky barrier height by forming an interface layer (which includes or sometimes consists of a passivation layer that includes an oxide, oxynitride, nitride, arsenide, hydride, fluoride, or an equivalent) between a metal and a semiconductor. This scheme differs from past attempts by others to control barrier height, which attempts generally involved either using a silicide as a contact metal (and thus limiting the choices of available contact metals to those that can form silicides), or using esoteric substrates that exhibit wide bandgaps. Further, in previous devices the Fermi level of the semiconductor remains pinned, with the barrier height being virtually independent of the metal used. Finally, doping of substrates has also been attempted, however, it has not been shown to truly affect the barrier height of the substrate material. For example, PtSi contacts have reduced resistance due to high silicon doping such that the current across the junction is dominated by tunneling through the barrier. Doping may thus lead to cases where the top of the barrier may be so thin as to be essentially transparent to electrons, however, doping does not appear to allow actual tuning of the barrier height.

[0063] **Figure 6** shows an example of a diode 600 containing, according to one embodiment of the present invention, an interface layer 620 disposed between and attached to both a semiconductor 610 and a conductor 630. The conductor and the semiconductor are operable to be electrically coupled with different voltages associated with the operation of the diode 600 and to pass electrical current through a passivated semiconductor surface formed at the junction between the semiconductor 610 and the interface layer 620.

[0064] The conductor 630 contains a conductive material such as a metal or an alloy of a metal. The terms metal, conductive material, and conductor are all related and appear in order from specific at the left to general at the right. In general, the terms refer to a highly electrically conductive substance that has a Fermi energy level that sits in a partially filled band. Unless otherwise specified, conductors include metals (e.g., pure metals and alloys),

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and other conductors such as doped polysilicon (a nonporous silicon containing randomly oriented crystallites), doped single crystal silicon, and metal silicides. Note that alloys may have workfunctions different than their constituents and may be designed to have specific workfunctions though selective use of ratios of the constituent metals.

[0065] Often, the conductor is a metal since metals may offer advantages over conductive semiconductors including lower resistance, higher carrier mobilities that provide superior high frequency performance and switching, favorable low power characteristics, and ease of manufacturing control. Use of metals may also avoid the need to perform semiconductor doping, which may simplify manufacturing and improve quality control.

[0066] Metals that are contemplated include pure metals, alloys, refractory metals, metals that do not form silicides, metals physically deposited by substantially non-invasive processes such as by condensation of a thermally evaporated metal vapor, and metals having a predetermined work function. The use of non-invasively deposited metals may allow for forming the metal on a thin interface layer without disrupting the passivation properties of the layer.

[0067] A metal having a predetermined work function may be a metal having a work function smaller or greater than that of the semiconductor, depending on the desired application. Often, the semiconductor will be silicon. In this case by the work function of a semiconductor or silicon we mean the energy in the middle of the semiconductor bandgap. Exemplary metals that have a work function smaller than silicon include Group 3A elements, aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum (Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn). Exemplary metals that have a work function greater than silicon include platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Co), and palladium (Pd).

[0068] The semiconductor-interface layer-conductor configuration illustrated in **Figure 6** defines what the present inventors have chosen to call a "passivated Schottky barrier". The

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passivated Schottky barrier is a naturally formed electrical potential barrier to an electron or hole at the Fermi energy (the electrochemical potential) in the conductor due to a depletion region formed in the semiconductor adjacent the conductor. The passivated Schottky barrier may deviate in barrier height from a standard un-passivated Schottky barrier that would form naturally at a contact junction between the semiconductor and the conductor without the interface layer disposed therebetween. That is, the passivated Schottky barrier may have a barrier height that depends predominantly upon the bulk characteristics of the semiconductor and the conductor, rather than on surface properties, and may depend in part on the characteristics of the interface layer.

[0069] Indeed, the present inventors have determined that changes in barrier height are approximately monotonic and continuous for variations in surface passivation thickness by nitridation of the semiconductor substrate. More specifically, experiments by the present inventors in a regime where the nitride layer is sufficiently thick to remove MIGS show that temperature of interface layer formation has the strongest effect on barrier height. In other regimes, thickness may be critical. Ideally, if all surface states are removed, barrier height should be controllable simply by the choice of metal used.

[0070] To understand why thickness of the interface layer is important, refer briefly to **Figure 8** where a graph of interface-specific contact resistance versus interface thickness is shown. The graph is for a structure where the workfunction of the metal is the same as the electron affinity in the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the semiconductor. At large thicknesses, the interface layer poses significant resistance to current. As thickness decreases, resistance falls due to increased tunneling current. However, there comes a point where even as the interface layer continues to get thinner, resistance increases. This is due to the effect of MIGS, which increasingly pull the Fermi level of the metal down towards mid-gap of the semiconductor, creating a Schottky barrier. The present inventors have discovered that this competition results in an optimum thickness, as shown in the illustration, where the resistance is a minimum. At this thickness

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the effect of MIGS has been sufficiently reduced to depin the metal and lower the Schottky barrier, and the layer is still sufficiently thin to allow significant current flow across the interface layer. Contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 Ω-μm^2, 100 Ω-μm^2, 50 Ω-μm^2, 10 Ω-μm^2 or even less than or equal to 1 Ω-μm^2 may be achieved.

[0071] Characteristics that may be adjusted to provide a desired barrier height thus include the passivation material used (e.g., selection based on bandgap), the interface layer thickness (e.g., especially where the interface layer is a compound layer formed of a passivation layer and a separation layer), the method of forming the interface layer (e.g., control of parameters such as temperature), the interface layer thickness that is substantially similar to a penetration depth of MIGS formed at a metal interface, the metal used for the source and/or drain, and other characteristics.

[0072] One advantage of the ability to adjust the Schottky barrier height with the introduction of interface layer 620 is the ability to form a substantially high barrier height. For example, an interface layer may be used to create a Schottky barrier having a barrier height that is greater than can be achieved through the use of metal silicides, greater than about 2.0 eV, or greater than about 2.5 eV (using a semiconductor with a bandgap at least this large), or nearly 1.0 V using silicon. Such high barrier heights imply the ability to withstand high voltages before breakdown occurs. Thus, Schottky barriers having such high barrier heights may be particularly useful in high-voltage Schottky diodes.

[0073] Another advantage achieved through the use of the interface layer 620 is greater flexibility afforded in selecting a conductor 630. Typically, metals chosen for application in classic Schottky diodes are those that can form a silicide with a silicon semiconductor. The formation of the silicide helps to reduce surface states (resulting from dangling bonds), but not the effects of MIGS. Thus, the Fermi level at the semiconductor surface is still pinned. Using metals that form silicides upon contact with silicon may thus help to make the devices more

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reproducible in a manufacturing environment, but such devices still suffer from the drawback of having a barrier height that is fixed.

[0074] According to one embodiment of the present invention, however, one may select a conductor that is not able (or not readily able) to form a silicide with the semiconductor. The metal silicide is not needed because the interface layer provided in accordance with the present invention passivates the semiconductor surface and also reduces or eliminates the effect of MIGS. This may allow for selection of a metal that has properties such as a desirable work function or Fermi level energy, even though that metal may not form a metal silicide.

[0075] For example, to make large-barrier diodes, for an *n*-type doped silicon semiconductor, a metal may be selected that has a work function that is either substantially equal to the valence band energy of the semiconductor or that is within about 0.1 eV to about 0.3 eV of the valence band energy of the semiconductor. Similarly, for a *p*-type doped silicon semiconductor, a metal may be selected that has a work function substantially equal to the conduction band energy of the semiconductor. For Schottky diodes configured in accordance with the present invention, the Fermi level of the metal may lie anywhere in the bandgap of the semiconductor when an interface layer is disposed within the junction, resulting in diodes of various barrier heights. The Fermi level of the metal may also lie in the conduction or valence band of the semiconductor.

[0076] The use of interface layer 620 thus provides a way to tune, adjust, or control the height of the barrier between the conductor and the semiconductor. Without the interface layer 620, the barrier height would be substantially un-tunable, un-adjustable, and fixed (as discussed above).

[0077] The role played by interface layer 620 in tuning, adjusting, or controlling the height of the barrier between the conductor 630 and the semiconductor 610 may be understood as a depinning of the Fermi level of the semiconductor. That is, the interface layer may reduce surface states by bonding to the semiconductor material to consume dangling bonds. Additionally, the interface layer may reduce the formation of MIGS in the semiconductor by

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providing a thickness and bandgap that prevent the electron wave function (of the metal) from penetrating into the semiconductor. The electron wave function may instead penetrate into the interface layer and form MIGS within the interface layer at an energy related to the states of the interface layer material. As desired, the density of the MIGS and the depth of MIGS penetration into the interface layer may be reduced by choosing an interface layer material or materials having a larger bandgap or higher effective mass than the semiconductor.

[0078] According to one embodiment of the present invention then, the interface layer 620 is incorporated into a device operable to pass current through the semiconductor surface and the interface layer during device operation. In such an embodiment, it may be desirable to use an interface layer having a thickness of a monolayer, or, for example between about 0.1 nm and about 0.3 nm, and also having a wide bandgap (as compared to that of the semiconductor) so that the interface layer both de-pins the Fermi level (so that the barrier height depends predominantly on bulk properties of the junction materials) and allows sufficient current transfer across it. Advantageously, such interface layers may be sufficiently thin to provide low impedance to current flow (due to the exponential dependence of direct tunneling on barrier thickness), which is desirable for many semiconductor devices, while also providing sufficient semiconductor surface passivation to allow an adjustable barrier height. That is, the interface layer may allow passivation of surface states and reduction (or elimination) of MIGS in the semiconductor to allow for an adjustable barrier height with a substantially thin layer that allows sufficient current to be transferred across the interface layer.

[0079] There are several methods by which the barrier height can be made adjustable. For example, adjustment may be made by tuning the degree of Fermi level pinning. In other words, some embodiments may allow for a sufficiently thin interface layer so that not all of the effects of MIGS in the Si are eliminated. Further, the pinning may be varied by combinations of thickness of the interface layer and the choice of interface material. The metal in contact with the interface layer may be pinned by MIGS at different levels in different materials. Conversely, or in addition, the passivation may be left incomplete to allow for an

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effective level of unpassivated states. Complete depinning of the Fermi level (that is removal of all surface states in Si including MIGS) is another option, in which case one could tune the barrier height simply by choosing a pure metal or an alloy that possesses the desired workfunction. In that case, the barrier height is determined by Equation (1), which until now has been an unrealizable idealization. Note that the type of tuning being discussed here is adjustment of the barrier height by altering the structure of the junction at the time of manufacture, not by varying an externally applied condition during junction operation.

[0080] **Figure 7a – 7d** show relationships between Fermi energy, conduction band energy, and valence band energy for various Schottky barriers containing a metal in contact with (or in close proximity to) a semiconductor, where the bandgap (E_g) of the semiconductor exists between the conduction band (E_c) and the valence band (E_v). In this example, the work function of the metal Φ_M is chosen to be approximately equal to the electron affinity χ_S of the semiconductor. In **Figure 7a**, an unpassivated Schottky barrier 700 is shown. In this example, the Fermi level (E_F) of the metal 730 is pinned in the bandgap of the semiconductor 710. This results in a discontinuity in the vacuum level caused by a charged dipole at the interface.

[0081] In **Figure 7b**, the interface layer 720b is thick enough to passivate dangling bonds at the surface of the semiconductor 710, but not thick enough to eliminate or sufficiently reduce the effect of MIGS. As a result, the band structure is largely unaltered from that seen in the previous illustration. Similarly, in **Figure 7c**, when the interface layer 720c is sufficiently thick to eliminate or reduce the effect of MIGS but not to passivate the semiconductor surface, little change in the energy band structure is observed. However, as shown in **Figure 7d**, when the interface layer 720d is sufficient to both eliminate or reduce the effect of MIGS and to passivate the semiconductor surface, we see the Fermi level of the metal aligning with the conduction band of the semiconductor (i.e., the Fermi level of the semiconductor has been depinned and no longer lines up with the Fermi level of the metal). The vacuum level is now continuous as there is no charged dipole at the interface. Thus, the band structure of a device

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constructed in this fashion is a result of only bulk material properties, not properties of the surface. By way of example, the materials in such cases may be Al and Si, with a work function for Al of approximately $\Phi_M = 4.1$ eV and the electron affinity for Si of approximately $\chi_S = 4.05$ eV.

V. Transistors Containing Passivated Semiconductor Surfaces

[0082] The interface layers described herein may be used in connection with a semiconductor surface of a channel in a field effect transistor. That is, an interface layer may be disposed between a source and a channel, a channel and a drain, or both of an insulated gate field effect transistor. Such use of an interface layer is described in detail in co-pending U.S. Patent No. 6,833,556, issued December 21, 2004, entitled "INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL", filed January 14, 2003 by the present inventors, and assigned to the assignee of the present invention.

[0083] The source and drain contacts at the channel of a field effect transistor are examples of a broader category of metal-interface layer-semiconductor contacts that make up the present invention. In the past, such contacts generally comprised a silicide-n^+-Si junction, which formed a somewhat "leaky" Schottky diode, with a Fermi level of the semiconductor pinned at the midgap. In contrast, the present invention provides a contact wherein the Fermi level of the metal is aligned with the conduction band of the semiconductor (e.g., as shown in Figure 7d). Note that in other cases, depending on the type of semiconductor material and conductors used, the Fermi level of the metal may align with the valence band of the semiconductor.

[0084] Although both types of junctions (i.e., the new passivated Schottky barrier junction and the conventional silicide-semiconductor junction) permit tunneling currents, the present junction can be fabricated with a much thinner interface layer as compared to the thickness of the silicide layer used previously. Indeed, thickness of an order of magnitude less than the silicide thickness can be expected. In a conventional silicide – semiconductor junction a

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Schottky barrier is formed which is comprised of a depletion layer. The tunnel barrier presented by such a depletion layer may be an order of magnitude thicker than the dielectric tunnel barrier in the present invention. The thinner interface layers provided by the present invention permit higher current across the junction (i.e., lower junction specific contact resistance).

[0085] Two other properties of the dielectric deserve mention. First is the property of the height of the barrier compared to the semiconductor conduction band (for electrons). In making the barrier thinner than a silicide barrier, the tradeoff may be a higher tunnel barrier (e.g., 2 eV for nitride, compared with about half the gap of 0.6 eV for silicide). Spacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV). Nevertheless, even with the higher barrier to electrons, the present inventors have determined that the resistance can still be one hundred times lower than a contact to silicon with a silicide barrier.

[0086] The second property is the effective mass of electrons in the dielectric. Larger mass electrons will not penetrate as far (i.e., because of their shorter wavelength) from the metal into the semiconductor. The less the electrons penetrate into the dielectric, the less the effect of MIGS in the dielectric. Thus, MIGS in the dielectric are reduced with larger bandgap and larger effective mass.

[0087] In addition the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility). The high doping profiles were required in the past in order to keep the junction depletion layer relatively thin, so as to increase the tunneling current, thus reducing the junction resistance. However, it is becoming increasingly difficult to increase doping profiles in order to provide low resistance junctions. It may be possible to reach the same level of resistance with a lower doping concentration using the present invention. It may further be possible to achieve much lower resistance even with lower doping concentration. When the present invention is used with high doping levels, the resistance will be further reduced.

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[0088] Thus, methods and applications for semiconductor-interface layer-metal junctions have been described. Although described with reference to specific embodiments it should be remembered that various modifications and changes may be made to the techniques described herein without departing from the broader spirit and scope of the invention. The specification and drawings are accordingly to be regarded in an illustrative rather than a restrictive sense and the invention measured only in terms of the claims, which follow.

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CLAIMS

What is claimed is:

1. An electrical junction, comprising an interface layer disposed between and in contact with a conductor and a semiconductor, the interface layer comprising arsenic.

2. The electrical junction of claim 1, wherein the conductor comprises a metal silicide.

3. The electrical junction of claim 1, wherein the interface layer comprises a monolayer of arsenic.

4. The electrical junction of claim 3, wherein the conductor comprises a metal silicide.

5. The electrical junction of claim 4, wherein the semiconductor comprises silicon.

6. The electrical junction of claim 4, wherein the semiconductor comprises germanium.

7. The electrical junction of claim 1, wherein the conductor comprises a source of a transistor.

8. The electrical junction of claim 1, wherein the conductor comprises a drain of a transistor.

9. The electrical junction of claim 1, wherein the conductor has a work function substantially equal to a conduction band energy of the semiconductor.

10. A field effect transistor, comprising a source, a drain, a semiconductor channel

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region between the source and the drain, a gate proximate the semiconductor channel region, and an interface layer comprising arsenic between the source and the semiconductor channel region.

11. The field effect transistor of claim 10, wherein the source comprises a metal silicide.

12. The field effect transistor of claim 10, wherein the interface layer comprises a monolayer of arsenic.

13. The field effect transistor of claim 12, wherein the source comprises a metal silicide.

14. The field effect transistor of claim 10, wherein the semiconductor channel region comprises silicon.

15. The field effect transistor of claim 10, wherein the semiconductor channel region comprises silicon germanium.

16. The field effect transistor of claim 10, wherein the semiconductor channel region comprises germanium.

17. The field effect transistor of claim 10, wherein the source comprises a material having a work function substantially equal to a conduction band energy of the semiconductor channel region.

18. A field effect transistor, comprising a source, a drain, a semiconductor channel region between the source and the drain, a gate proximate the semiconductor channel region, and an interface layer comprising arsenic between the drain and the semiconductor channel region.

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ABSTRACT

An electrical device in which an interface layer comprising arsenic is disposed between and in contact with a conductor and a semiconductor. In some cases, the interface layer may be a monolayer of arsenic.

GF Exhibit 1012 - 40/439

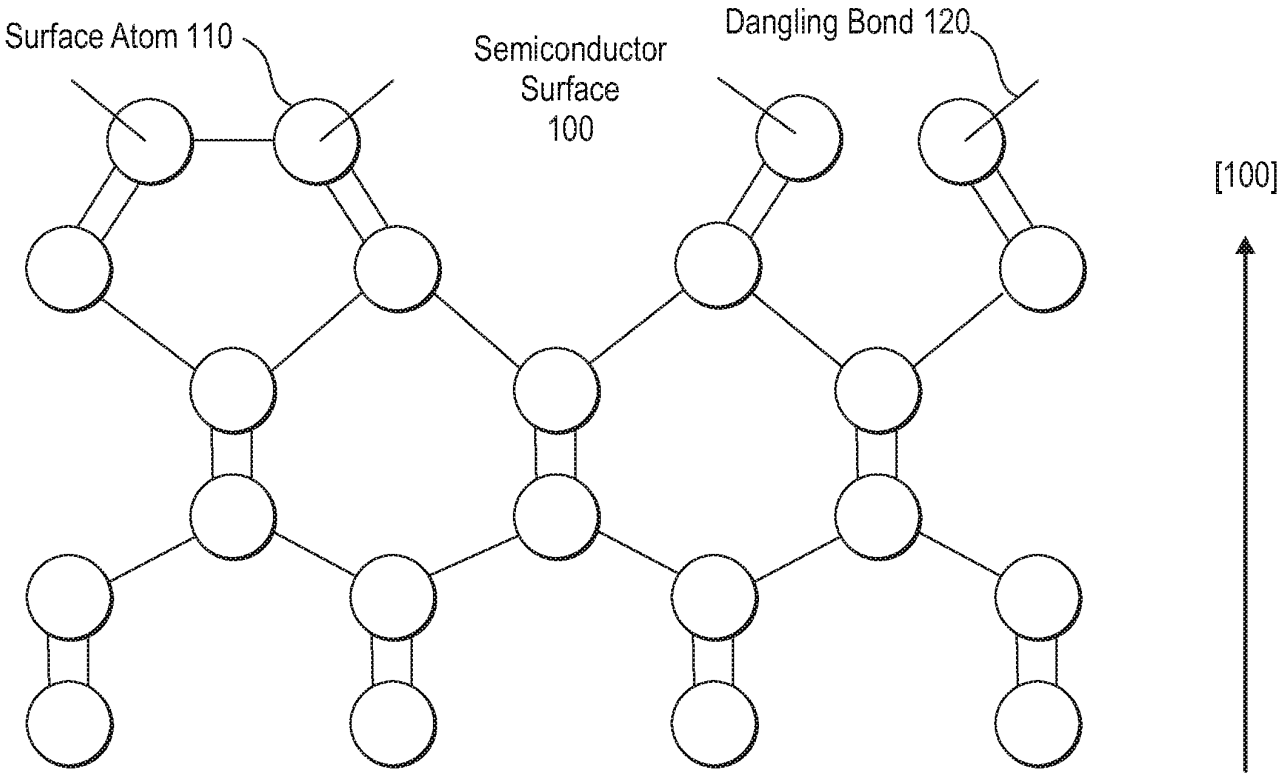


Fig. 1

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Energy Scales for Metal - Semiconductor Junctions

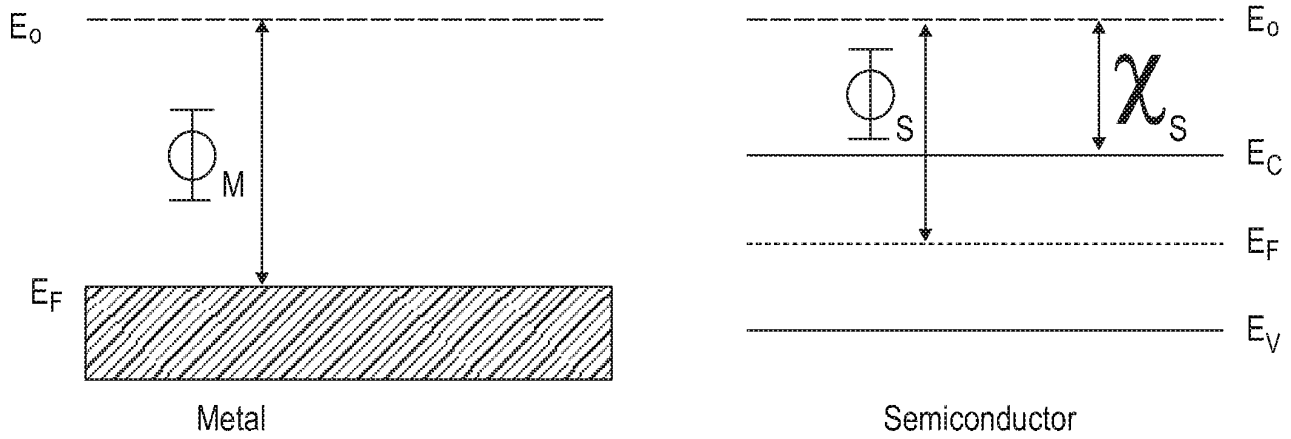


Fig. 2

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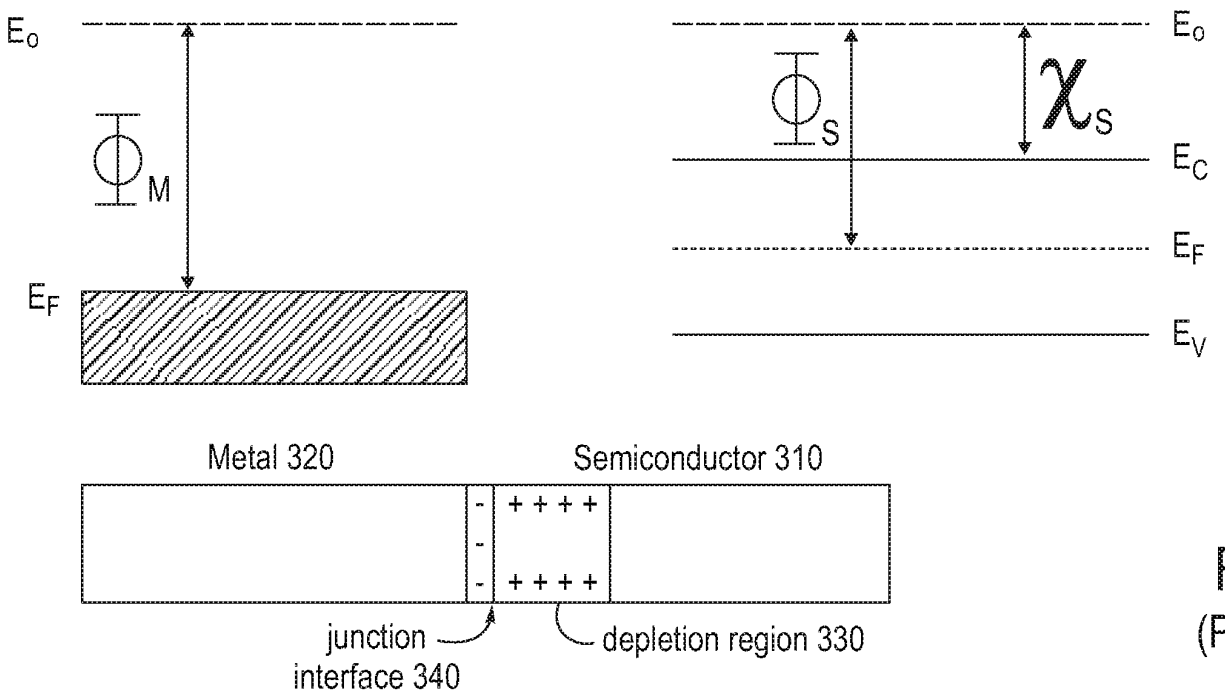


Fig. 3
(Prior Art)

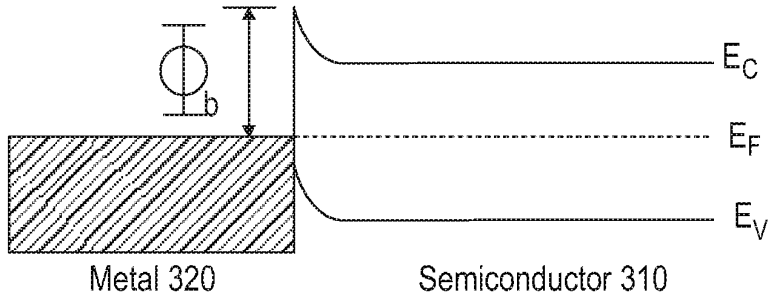


Fig. 4
(Prior Art)

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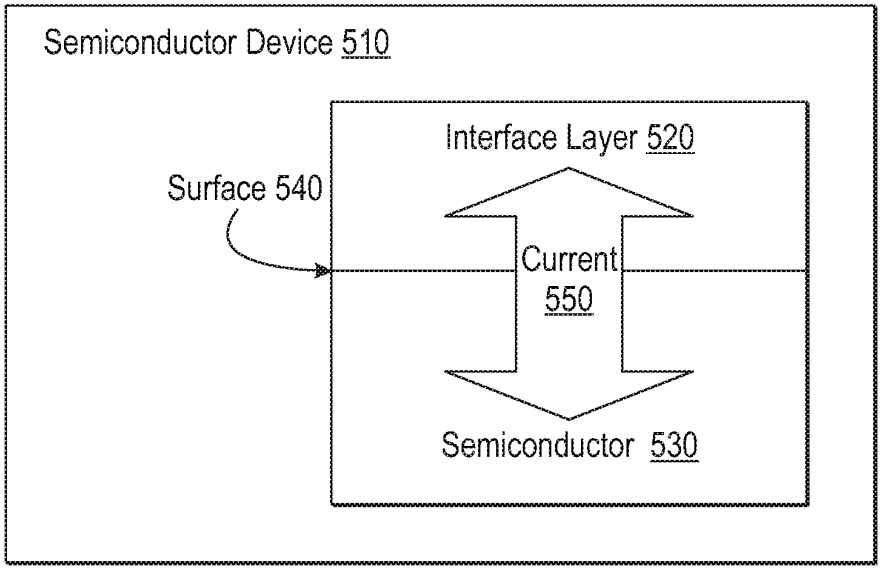


Fig. 5

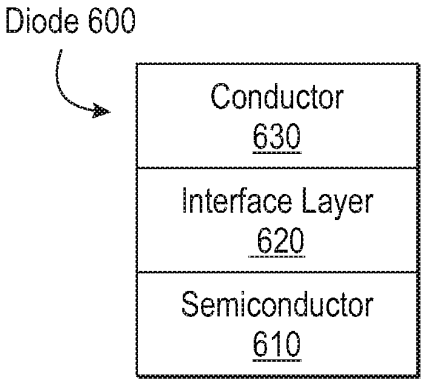


Fig.6

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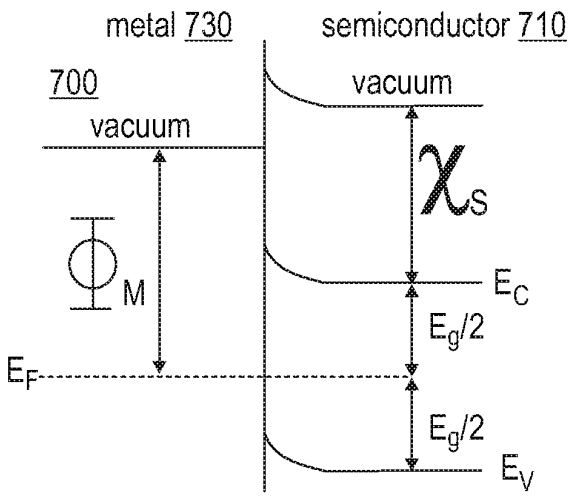


Fig. 7a

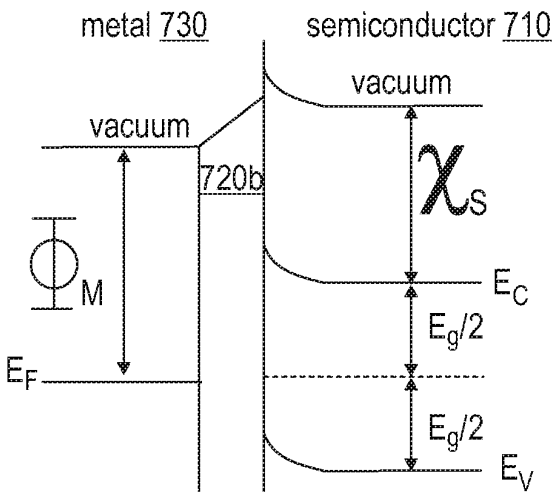


Fig. 7b

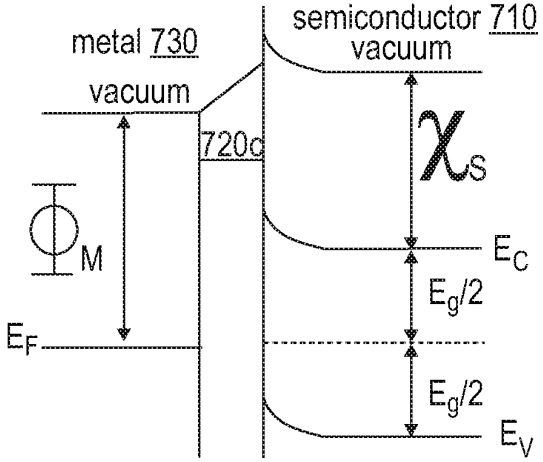


Fig. 7c

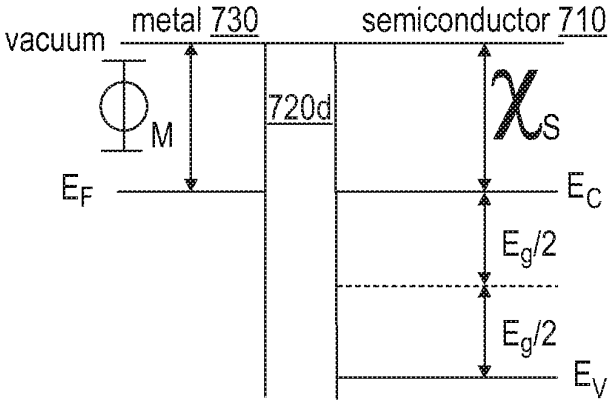


Fig. 7d

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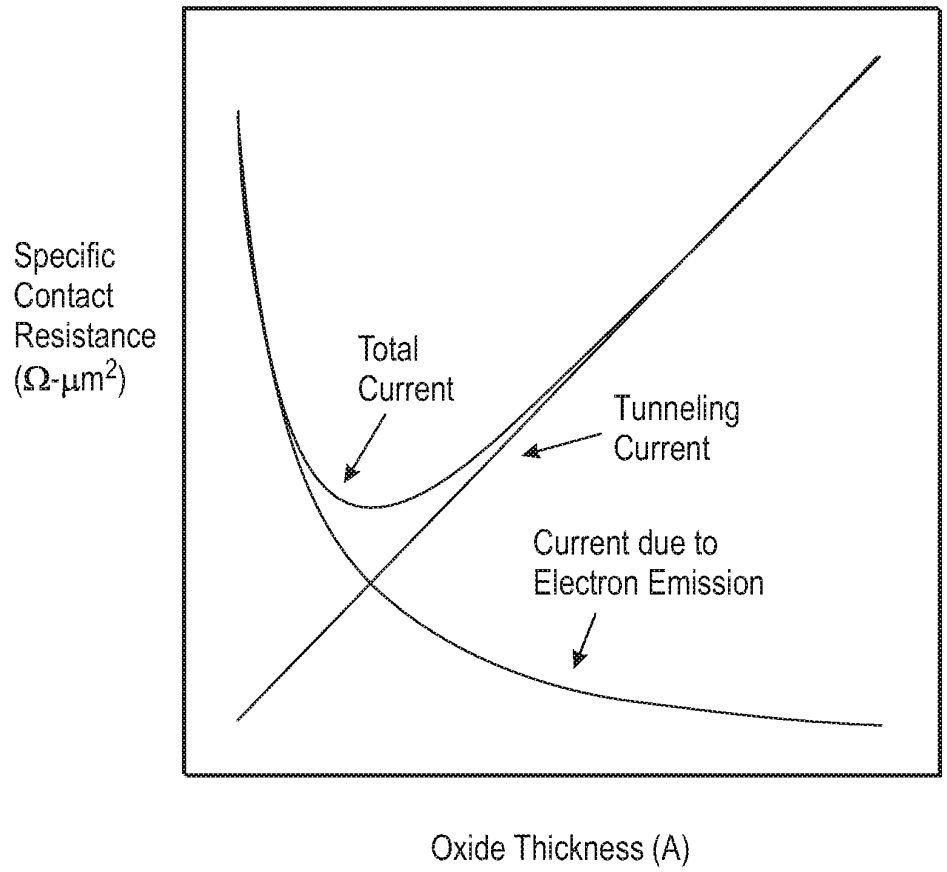


Fig. 8

GF Exhibit 1012 - 46/439

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Filer:	Tarek N. Fahmi
Attorney Docket Number:	40003771-0003-463

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility filing Fee (Electronic filing)	4011	1	95	95
Utility Search Fee	2111	1	310	310
Utility Examination Fee	2311	1	125	125
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**530**

Electronic Acknowledgement Receipt

EFS ID:	13286879
Application Number:	13552556
International Application Number:	
Confirmation Number:	8045
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-463
Receipt Date:	18-JUL-2012
Filing Date:	
Time Stamp:	20:20:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$530
RAM confirmation Number	8385
Deposit Account	
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1		40003771-0003-463_executed_POA_and_Dec.pdf	975083 d0e735f5303e6180855955b97d664c20263c0814	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Power of Attorney	1	1
	Assignee showing of ownership per 37 CFR 3.73(b).	2	2
	Oath or Declaration filed	3	5

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2		40003771-0003-463_Apln_filed_07_18_2012.pdf	364414 4489e640b4783457b209807adefc614326f2b13f	yes	41

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	32
	Claims	33	34
	Abstract	35	35
	Drawings-only black and white line drawings	36	41

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3	Fee Worksheet (SB06)	fee-info.pdf	33083 a6a3ceef730f42ae1a2b0615cad7b1acec0374f3	no	2

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/552,556	07/18/2012	2811	530	40003771-0003-463	18	3

CONFIRMATION NO. 8045

27571
TAREK N. FAHMI, APC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

FILING RECEIPT



Date Mailed: 08/01/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Daniel E. Grupp, Palo Alto, CA;
Daniel J. Connelly, Redwood City, CA;

Power of Attorney: The patent practitioners associated with Customer Number 27571

Domestic Priority data as claimed by applicant

This application is a CON of 13/022,522 02/07/2011
which is a DIV of 12/197,966 08/25/2008 ABN
which is a DIV of 11/181,217 07/13/2005 PAT 7462860
which is a CON of 10/217,758 08/12/2002 PAT 7084423

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

If Required, Foreign Filing License Granted: 07/30/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/552,556**

Projected Publication Date: 11/08/2012

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****

Title

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Preliminary Class

257

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/552,556

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	95		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	310		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	125		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	18 minus 20 =	*	x 30 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 125 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	530		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/552,556	07/18/2012	Daniel E. Grupp	40003771-0003-463

CONFIRMATION NO. 8045

27571
TAREK N. FAHMI, APC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

POA ACCEPTANCE LETTER

OC000000055663097

Date Mailed: 08/01/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/18/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/agoitom/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/552,556	07/18/2012	Daniel E. Grupp	40003771-0003-463	8045

27571 7590 10/04/2012

TAREK N. FAHMI, APC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

EXAMINER	
HARRISON, MONICA D	
ART UNIT	**PAPER NUMBER**
2896	

NOTIFICATION DATE	DELIVERY MODE
10/04/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@tnfip.com
tarek.fahmi@tnfip.com

Office Action Summary	Application No.	Applicant(s)	
	13/552,556	GRUPP ET AL.	
	Examiner	Art Unit	
	Monica D. Harrison	2896	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

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- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) 1-18 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) 10-18 is/are allowed.

7)☒ Claim(s) 1-9 is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on 18 July 2012 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

OFFICE ACTION

Priority

1. This application discloses and claims only subject matter disclosed in prior Application No. 13/022,522, filed 2/7/11, and names an inventor or inventors named in the prior application. Accordingly, this application may constitute a continuation or division. Should applicant desire to obtain the benefit of the filing date of the prior application, attention is directed to 35 U.S.C. 120 and 37 CFR 1.78.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4 and 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Long et al (U.S. Patent No. 6,608,352).

2. Regarding claim 1, Long et al discloses an electrical junction, comprising an interface layer (Figure 3, references 156 and 158) disposed between and in contact with a conductor (Figure 3, reference 118) and a semiconductor (Figure 3, references 154, 152, 102), the interface layer comprising arsenic (Figure 3, references 156 and 158; column 5, lines 12-16).

3. Regarding claim 2, Long et al discloses wherein the conductor comprises a metal silicide (Figure 1, reference 120).

4. Regarding claim 3, Long et al discloses wherein the interface layer comprises a monolayer of arsenic (Figure 3, references 156 and 158; column 5, lines 12-16).

5. Regarding claim 4, Long et al discloses wherein the conductor comprises a metal silicide (Figure 1, reference 120).

6. Regarding claim 7, Long et al discloses wherein the conductor (Figure 6, reference 118) comprises a source (Figure 6, reference 158) of a transistor (Figure 6).

7. Regarding claim 8, Long et al discloses wherein the conductor (Figure 4, reference 118) comprises a drain (Figure 4, reference 156) of a transistor (Figure 4).

8. Regarding claim 9, Long et al discloses wherein the conductor (Figure 3, reference 118) has a work function substantially equal to conduction band energy of the semiconductor (Figure 3, references 154, 152 and 102).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al (U.S. Patent No. 6,608,352) in view of Sakuma et al (U.S. Patent No. 6,011,271).

9. Long et al discloses all of the above claimed subject matter.

However, Long et al does not disclose wherein the semiconductor comprises silicon (claim 5) nor wherein the semiconductor comprises germanium (claim 6).

Sakuma et al discloses wherein the semiconductor comprises silicon (column 21, lines 17-18) and wherein the semiconductor comprises germanium (column 31, lines 17-18).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art to modify Long et al with teachings of Sakuma et al for the purpose of forming the semiconductor of silicon or germanium because silicon and germanium are well known in the art to be used a foundation for semiconductor devices.

Allowable Subject Matter

10. Claims 10-18 are allowed over the prior art of record.

Reasons for Allowance

11. The following is an examiner's statement of reasons for allowance: After further search of the prior art, examiner has concluded that the prior art does not disclose nor fairly suggest a field effect transistor comprising: an interface layer comprising arsenic between the source and the semiconductor channel region (claim 10) nor an interface layer comprising arsenic between the drain and the semiconductor channel region (claim 18) as described in the independent claims and in the context of their recited apparatus along with their depending claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Monica D. Harrison* whose telephone number is (571) 272-1959. The examiner can normally be reached on Monday-Friday 7:00AM-3:30PM EST. If attempts to reach the examiner by telephone are unsuccessful, Art Unit 2896's Supervisory Patent Examiner *Matthew Such* can be reached at (571) 272-8895. The fax phone number for the organization is (571) 273-8300.

Information regarding the status of this application may be obtained from either Private Patent Application Information Retrieval (PAIR) or Public PAIR system at http://pair-direct.uspto.gov. Should you have questions on access to the PAIR, contact Electronic Board Center at (866) 217-9197. For assistance from a USPTO Customer Service system, call toll free (800) 786-9199 or (571) 272-1000.

/Monica D. Harrison/
Assistant Examiner

September 27, 2012 /Calvin Lee/

Date Primary Patent Examiner, A.U.2896

Notice of References Cited	Application/Control No. 13/552,556	Applicant(s)/Patent Under Reexamination GRUPP ET AL.	
	Examiner Monica D. Harrison	Art Unit 2896	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,608,352 B1	08-2003	Long et al.	257/347
*	B	US-6,011,271	01-2000	Sakuma et al.	257/14
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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BIB DATA SHEET

CONFIRMATION NO. 8045

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/552,556	07/18/2012	257	2896	40003771-0003-463

APPLICANTS

Daniel E. Grupp, Palo Alto, CA;
Daniel J. Connelly, Redwood City, CA;

MDH 9/25/12

**** CONTINUING DATA ***************************

This application is a CON of 13/022,522 02/07/2011
which is a DIV of 12/197,966 08/25/2008 ABN
which is a DIV of 11/181,217 07/13/2005 PAT 7,462,860
which is a CON of 10/217,758 08/12/2002 PAT 7,084,423

MDH 9/25/12

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
07/30/2012

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /MONICA D HARRISON/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		CA	6	18	3

ADDRESS

TAREK N. FAHMI, APC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113
UNITED STATES

TITLE

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

FILING FEE RECEIVED		
530	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13552556	GRUPP ET AL.
	Examiner	**Art Unit**
	MONICA D HARRISON	2896

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
257	30-35,56,62,65,288,471-475,483	9/25/12	MDH

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
East (USPAT, US-PGPUB, USOCR, EPO, JPO, DERWENT, IBM_TDB, FPRS)	9/25/12	MDH
GRUPP et al. .inv.	9/25/12	MDH

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**

/MONICA D HARRISON/ Examiner.Art Unit 2896	

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	13/552556	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:52
L2	1	13/022522	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:53
L3	2	"7884003".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:53
L4	2	"7462860".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:54
L5	2	"7084423".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:55
L6	2	"6833556".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:00
L7	3697	257/288.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:09
L8	30	257/288.ccls. and ((conductor metal)	US-PGPUB;	OR	ON	2012/09/25

		with arsenic)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:09
L9	12	257/288.ccls. and ((conductor metal) with arsenic) and (arsenic with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:10
L10	2609	(grupp connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:18
L11	25	(grupp connelly).inv. and arsenic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:18
L12	17	(grupp connelly).inv. and (arsenic with interface) and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:19
L13	8062	257/30-35,56,62,65,288,471-475,483.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:27
L14	123	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:27
L15	86	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:29
L16	77	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2012/09/25 11:29

			IBM_TDB			
L17	74	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:29
L18	56	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:30
L19	56	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:30
L20	47	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel and gate and (semiconductor with silicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 12:15
L21	17	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel and gate and (semiconductor with silicon) and (semiconductor with germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 12:15
L22	386	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:20
L23	150	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface) and (interface with metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:20
L24	225	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface) and (interface with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:20
L25	5	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface) and (interface with	US-PGPUB; USPAT; USOCR;	OR	ON	2012/09/25 13:21

		semiconductor) and (interface with arsenic)	FPRS; EPO; JPO; DERWENT; IBM_TDB			
L26	97	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface with arsenic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:21
L27	46	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:21
L28	0	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 siicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:22
L29	44	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 silicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:22
L30	1	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 silicon) and (semiconductor near5 germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:23
L31	2	(conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 silicon) and (semiconductor near5 germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:23
L32	4222	257/30-35,56,62,65,288,471-475,483.ccls. and (substrate wafer semiconductor) near6 silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:27
L33	901	257/30-35,56,62,65,288,471-475,483.ccls. and (substrate wafer semiconductor) near6 silicon and (substrate wafer semiconductor) near6 germanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:27
L34	16	257/30-35,56,62,65,288,471-	US-PGPUB;	OR	ON	2012/09/25

		475,483.ccls. and (substrate wafer semiconductor) near6 silicon and (substrate wafer semiconductor) near6 germanium and (conduct$4 with arsenic)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			13:28

EAST Search History (Interference)

<This search history is empty>

9/25/2012 1:52:16 PM
C:\Users\mharrison1\Documents\EAST\Workspaces\13552556.wsp

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13552556	GRUPP ET AL.
	Examiner	**Art Unit**
	MONICA D HARRISON	2896

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/27/2012								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
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	15	=								
	16	=								
	17	=								
	18	=								

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/552,556	07/18/2012	Daniel E. Grupp	40003771-0003-463

CONFIRMATION NO. 8045

27571
TAREK N. FAHMI, APC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

PUBLICATION NOTICE

OC000000057511038

Title:METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Publication No.US-2012-0280294-A1
Publication Date:11/08/2012

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 13/552,556

First Named Inventor: Daniel E. Grupp

Filed: July 18, 2012

Art unit: 2896

Examiner: Harrison, Monica D.

Docket No.: 40003771-0003-463

Confirmation No.: 8045

Commissioner for Patents
P.O. Box 1450
Alexandria VA, 22313-1450

RESPONSE TO OFFICE ACTION

Sir:

In Response to the Office Action mailed on October 4, 2012, reconsideration of the above-identified application is respectfully requested in light of the following remarks.

REMARKS

The Examiner is thanked for indicating that claims 10-18 are allowable. Reconsideration of the remaining claims pending in this application in light of the following remarks is respectfully requested.

Claim 1 recites:

> An electrical junction, comprising an interface layer disposed between and in contact with a conductor and a semiconductor, the interface layer comprising arsenic.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of Californi*a, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), see also MPEP § 2131.02. The identical invention must be shown in as complete detail as is contained in the … claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, (Fed. Cir. 1989). Therefore, the present rejection of claim 1 as being anticipated by Long, US Patent No. 6,608,352, is appropriate only if Long teaches all of the elements recited in claim 1.

In rejecting claim 1, the Office Action refers primarily to Long's Figure 3 (reproduced below) and attempts to map the elements of claim 1 onto this illustration as follows:

Claim element	Long Fig 3 reference
Interface layer	156, 158
Conductor	118
Semiconductor	154, 152, 102
Arsenic	156, 158 (as explained at 5:12-16)

However, an examination of Long's Fig 3 shows how these mappings fail to support the present rejections.

Although not specified in Fig. 3, Long does indicate that a gate structure (referenced as 118 in Long's Fig. 1) is separated from the channel and the source/drain regions by a gate dielectric 116. Long at 1:46-47. As is well-known in the semiconductor arts, a gate dielectric is an electrical insulator, not a conductor. Moreover, the masking structure 202 shown in Long's Fig 3 is a temporary artifice formed of a photoresist and

GF Exhibit 1012 - 74/439

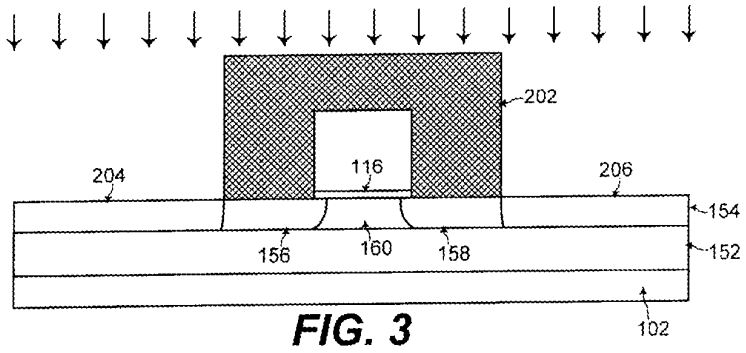


FIG. 3

does not form part of any electrical junction. See Long at 5:41-45.

Thus, if for purposes of argument one assumes that the interface layer recited in claim 1 is equivalent to Long's source/drain regions 156, 158, it is apparent that these regions are in contact with doped semiconductor regions 204, 206 (formed from semiconductor layer 154), semiconductor channel 160 and gate dielectric 116. However, the source/drain regions 156, 158 are not in contact with gate 118, and therefore Long does not teach an interface layer (comprising Arsenic) disposed between and in contact with a conductor and a semiconductor, as claimed. Stated differently, Long cannot anticipate claim 1 or any claims dependent therefrom. Accordingly, the rejections of claims 1-4 and 7-9 as being anticipated by Long should be withdrawn.

The rejection of claims 5 and 6 for obviousness in view of the combination of Long and Sakuma, US Patent 6,011,271, suffers from the same underlying deficiencies in Long noted above. Hence, claims 5 and 6 are patentable over these references.

Please charge any fees due to Deposit Account 50-5798.

Respectfully submitted,

TAREK N. FAHMI, APC

Date: December 31, 2012

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GF Exhibit 1012 - 75/439

REMARKS

The Examiner is thanked for indicating that claims 10-18 are allowable. Reconsideration of the remaining claims pending in this application in light of the following remarks is respectfully requested.

Claim 1 recites:

> An electrical junction, comprising an interface layer disposed between and in contact with a conductor and a semiconductor, the interface layer comprising arsenic.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of Californi*a, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), see also MPEP § 2131.02. The identical invention must be shown in as complete detail as is contained in the … claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, (Fed. Cir. 1989). Therefore, the present rejection of claim 1 as being anticipated by Long, US Patent No. 6,608,352, is appropriate only if Long teaches all of the elements recited in claim 1.

In rejecting claim 1, the Office Action refers primarily to Long's Figure 3 (reproduced below) and attempts to map the elements of claim 1 onto this illustration as follows:

Claim element	Long Fig 3 reference
Interface layer	156, 158
Conductor	118
Semiconductor	154, 152, 102
Arsenic	156, 158 (as explained at 5:12-16)

However, an examination of Long's Fig 3 shows how these mappings fail to support the present rejections.

Although not specified in Fig. 3, Long does indicate that a gate structure (referenced as 118 in Long's Fig. 1) is separated from the channel and the source/drain regions by a gate dielectric 116. Long at 1:46-47. As is well-known in the semiconductor arts, a gate dielectric is an electrical insulator, not a conductor. Moreover, the masking structure 202 shown in Long's Fig 3 is a temporary artifice formed of a photoresist and

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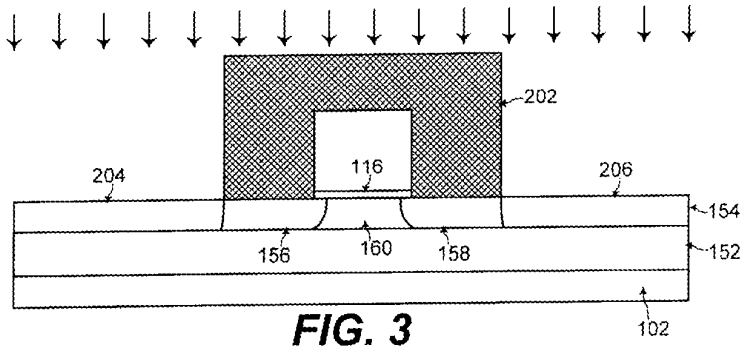


FIG. 3

does not form part of any electrical junction. See Long at 5:41-45.

Thus, if for purposes of argument one assumes that the interface layer recited in claim 1 is equivalent to Long's source/drain regions 156, 158, it is apparent that these regions are in contact with doped semiconductor regions 204, 206 (formed from semiconductor layer 154), semiconductor channel 160 and gate dielectric 116. However, the source/drain regions 156, 158 are not in contact with gate 118, and therefore Long does not teach an interface layer (comprising Arsenic) disposed between and in contact with a conductor and a semiconductor, as claimed. Stated differently, Long cannot anticipate claim 1 or any claims dependent therefrom. Accordingly, the rejections of claims 1-4 and 7-9 as being anticipated by Long should be withdrawn.

The rejection of claims 5 and 6 for obviousness in view of the combination of Long and Sakuma, US Patent 6,011,271, suffers from the same underlying deficiencies in Long noted above. Hence, claims 5 and 6 are patentable over these references.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Daniel E. Grupp

Application No.: 13/552,556
Filed: July 18, 2012

Examiner: Harrison, Monica D.
Art Unit: 2896

Docket No.: 40003771-0003-463

Customer No.: 27571

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
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Application Number	13552556
Filing Date	2012-07-18
First Named Inventor	Daniel E. Grupp
Art Unit	2896
Examiner Name	Harrison, Monica D.
Attorney Docket Number	40003771-0003-463

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	1	3590471		1971-07-06	Lepselter, et al.	
	2	3708360		1973-01-02	Wakefield, Jr., et al.	
	3	3983264		1976-09-28	Schroen, Walter H., et al.	
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	8	5399206		1995-03-21	de Lyon	

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	Attorney Docket Number	40003771-0003-463

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	2	20040026687		2004-02-12	Grupp et al.	
	3	20050093027		2005-05-05	Grupp et al.	

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	Attorney Docket Number	40003771-0003-463

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Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	13552556
Filing Date:	18-Jul-2012
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Filer:	Tarek N. Fahmi
Attorney Docket Number:	40003771-0003-DC3

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
Total in USD ($)				**180**

Electronic Acknowledgement Receipt

EFS ID:	14591246
Application Number:	13552556
International Application Number:	
Confirmation Number:	8045
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-DC3
Receipt Date:	31-DEC-2012
Filing Date:	18-JUL-2012
Time Stamp:	19:21:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$180
RAM confirmation Number	4460
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1		40003771-0003-DC3_ROA_Filed_12_31_2012.pdf	178214 48c370a6be98834cf49affbf1ea073be2bcc39a2	yes	3
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Applicant Arguments/Remarks Made in an Amendment		2	3	
Warnings:					
Information:					
2	Transmittal Letter	40003771-0003-DC3_IDS_Statement_12_31_2012.pdf	74135 1dcde49de0372e424f948197858265f07d92f550	no	2
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	40003771-0003-DC3_IDS_Filed_12_31_2012.pdf	619960 0e6905537740d0eb431db652dd4d19486d2b9365	no	11
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30435 9e16b1fa11abf16113fe3e6c560fc10ca666cc75	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	902744		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
13/552,556	07/18/2012	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☒		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	12/31/2012	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $31 =	0	OR	X $ =	
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $125 =	0	OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE	

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/JOY J. DOBBS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/552,556	07/18/2012	Daniel E. Grupp	40003771-0003-DC3	8045

27571 7590 04/15/2013

TAREK N. FAHMI, APC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

EXAMINER	
HARRISON, MONICA D	
ART UNIT	**PAPER NUMBER**
2896	

NOTIFICATION DATE	DELIVERY MODE
04/15/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@tnfip.com
tarek.fahmi@tnfip.com

Office Action Summary	Application No. 13/552,556	Applicant(s) GRUPP ET AL.	
	Examiner Monica D. Harrison	Art Unit 2896	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2012*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-18* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *10-18* is/are allowed.

7)☒ Claim(s) *1-9* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *18 July 2012* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some * c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Interim copies:

a)☐ All b)☐ Some c)☐ None of the: Interim copies of the priority documents have been received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/31/2012*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

FINAL ACTION

1. Applicant's arguments filed 12/31/12 have been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4 and 7-9 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,608,352 to *Long et al.*

Regarding claim 1, Long et al discloses an electrical junction, comprising an interface layer (Figure 3, references 156 and 158) disposed between and in contact with a conductor (Figure 3, reference 118) and a semiconductor (Figure 3, references 154, 152, 102), the interface layer comprising arsenic (Figure 3, references 156 and 158; column 5, lines 12-16).

Regarding claim 2, Long et al discloses wherein the conductor comprises a metal silicide (Figure 1, reference 120).

Regarding claim 3, Long et al discloses wherein the interface layer comprises a monolayer of arsenic (Figure 3, references 156 and 158; column 5, lines 12-16).

Regarding claim 4, Long et al discloses wherein the conductor comprises a metal silicide (Figure 1, reference 120).

Regarding claim 7, Long et al discloses wherein the conductor (Figure 6, reference 118) comprises a source (Figure 6, reference 158) of a transistor (Figure 6).

Regarding claim 8, Long et al discloses wherein the conductor (Figure 4, reference 118) comprises a drain (Figure 4, reference 156) of a transistor (Figure 4).

Regarding claim 9, Long et al discloses wherein the conductor (Figure 3, reference 118) has a work function substantially equal to conduction band energy of the semiconductor (Figure 3, references 154, 152 and 102).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al (U.S. Patent No. 6,608,352) in view of Sakuma et al (U.S. Patent No. 6,011,271).

Long et al discloses all of the above claimed subject matter. However, Long et al does not disclose wherein the semiconductor comprises silicon (claim 5) nor wherein the semiconductor comprises germanium (claim 6). Sakuma et al discloses wherein the semiconductor comprises silicon (column 21, lines 17-18) and wherein the semiconductor comprises germanium (col. 31, lines 17-18).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art to modify Long et al with teachings of Sakuma et al for the purpose of forming the semiconductor of silicon or germanium because silicon and germanium are well known in the art to be used as a foundation for semiconductor devices.

Allowable Subject Matter

6. Claims 10-18 are allowed. Following is an examiner's statement of reasons for allowance:

After further search of the prior art, the Examiner has concluded that the prior art does not disclose nor fairly suggest a field effect transistor comprising: an interface layer comprising arsenic between the source and the semiconductor channel region (claim 10) nor an interface layer comprising arsenic between the drain and the semiconductor channel region (claim 18) as described in the independent claims and in the context of their recited apparatus along with their depending claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

7. Applicant's arguments filed 12/31/12 have been fully considered but they are not persuasive. Applicant argues that *Long et al* does not disclose an interface layer comprising arsenic between and in contact with a conductor and semiconductor. Examiner disagrees. The gate structure, which includes the gate oxide (116) and gate electrode (118) are in contact with the doped source (156) and drains (158) regions which comprise arsenic that are formed within the SOI substrate (102, 152 and 154). The elements of the entire stacked structure are all in contact with one another. That is how the FET device is formed. Thus, claimed limitations have been met.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing

date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Monica D. Harrison* whose telephone number is (571) 272-1959. The examiner can normally be reached on Monday-Friday 7:00AM-3:30PM EST. If attempts to reach the examiner by telephone are unsuccessful, Art Unit 2896's Supervisory Patent Examiner *Matthew Such* can be reached at (571) 272-8895. The fax phone number for the organization is (571) 273-8300.

Information regarding the status of this application may be obtained from either Public Patent Application Information Retrieval (PAIR) or Private PAIR system at http://pair-direct.uspto.gov. Should you have questions on access to the PAIR, contact Electronic Board Center at (866) 217-9197. For assistance from a USPTO Customer Service system, call toll free (800) 786-9199 or (571) 272-1000

/M. D. Harrison/
Patent Examiner

April 5, 2013 /Calvin Lee/

Date Primary Patent Examiner, A.U.2896

Notice of References Cited	Application/Control No. 13/552,556	Applicant(s)/Patent Under Reexamination GRUPP ET AL.	
	Examiner Monica D. Harrison	Art Unit 2896	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,608,352 B1	08-2003	Long et al.	257/347
*	B	US-6,011,271	01-2000	Sakuma et al.	257/14
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13552556	GRUPP ET AL.
	Examiner	**Art Unit**
	MONICA D HARRISON	2896

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/27/2012	04/05/2013							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	=	=							
	11	=	=							
	12	=	=							
	13	=	=							
	14	=	=							
	15	=	=							
	16	=	=							
	17	=	=							
	18	=	=							

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13552556
	Filing Date	2012-07-18
	First Named Inventor	Daniel E. Grupp
	Art Unit	2896
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	40003771-0003-463

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/M.D.H./	1	3590471		1971-07-06	Lepselter, et al.	
	2	3708360		1973-01-02	Wakefield, Jr., et al.	
	3	3983264		1976-09-28	Schroen, Walter H., et al.	
	4	4056642		1977-11-01	Saxena, Arjun N. et al.	
	5	4300152		1981-11-10	Lepselter	
	6	4485550		1984-12-04	Koeneke, et al.	
	7	5021365		1991-06-04	Kirchner, et al.	
	8	5399206		1995-03-21	de Lyon	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H/

Receipt date: 12/31/2012	Application Number	13552556	13552556 - GAU: 2896
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2012-07-18	
(Not for submission under 37 CFR 1.99)	First Named Inventor	Daniel E. Grupp	
	Art Unit	2896	
	Examiner Name	Harrison, Monica D.	
	Attorney Docket Number	40003771-0003-463	

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Receipt date: 12/31/2012	Application Number	13552556 13552556 - GAU: 2896
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/M.D.H./	1	20030121468		2003-07-03	Boone et al.	

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/M.D.H./	1	0295490	EP		1988-12-21	Fowler, Alan B. et al.		☐

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	Art Unit	2896	
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13552556	GRUPP ET AL.
	Examiner	Art Unit
	MONICA D HARRISON	2896

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
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US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	30-35,56,62,65,288,471-475,483	9/25/12	MDH
257	288,E29.255	4/4/13	MDH

SEARCH NOTES		
Search Notes	Date	Examiner
East (USPAT, US-PGPUB, USOCR, EPO, JPO, DERWENT, IBM_TDB, FPRS)	9/25/12	MDH
GRUPP et al. .inv.	9/25/12	MDH
East updated	4/4/13	MDH

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EAST Search History (Prior Art)

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L1	70	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" | "7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:06
L2	39	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" | "7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As") with (gate electrode conduct$4 metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:07
L3	23	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" | "7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As") with (gate electrode conduct$4 metal) and (arsenic "As") with (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:08
L4	9	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" | "7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As") with (gate electrode conduct$4 metal) and (arsenic "As") with (substrate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:08

		wafer carrier base plate) and (arsenic "As") with channel				
L5	4445	257/'$'.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:14
L6	177	257/'$'.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and (arsenic near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:14
L7	29	257/'$'.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and (arsenic near (layer film)) and fet	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:15
S1	0	13/552556	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:52
S2	1	13/022522	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:53
S3	2	"7884003".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:53
S4	2	"7462860".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:54
S5	2	"7084423".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:55
S6	2	"6833556".pn.	US-PGPUB; USPAT; USOCR;	OR	ON	2012/09/25 11:00

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S7	3697	257/288.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:09
S8	30	257/288.ccls. and ((conductor metal) with arsenic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:09
S9	12	257/288.ccls. and ((conductor metal) with arsenic) and (arsenic with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:10
S10	2609	(grupp connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:18
S11	25	(grupp connelly).inv. and arsenic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:18
S12	17	(grupp connelly).inv. and (arsenic with interface) and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:19
S13	8062	257/30-35,56,62,65,288,471-475,483.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:27
S14	123	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:27
S15	86	257/30-35,56,62,65,288,471-475,483.ccls.	US-PGPUB;	OR	ON	2012/09/25

		and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide))	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:29
S16	77	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:29
S17	74	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:29
S18	56	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:30
S19	56	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:30
S20	47	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel and gate and (semiconductor with silicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 12:15
S21	17	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel and gate and (semiconductor with silicon) and (semiconductor with germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 12:15
S22	386	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:20
S23	150	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface) and (interface with metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2012/09/25 13:20

			IBM_TDB			
S24	225	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface) and (interface with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:20
S25	5	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface with arsenic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:21
S26	97	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface with arsenic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:21
S27	46	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:21
S28	0	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 siicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:22
S29	44	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 silicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:22
S30	1	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 silicon) and (semiconductor near5 germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:23
S31	2	(conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 silicon) and (semiconductor near5 germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:23
S32	4222	257/30-35,56,62,65,288,471-475,483.ccls. and (substrate wafer semiconductor) near6 silicon	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2012/09/25 13:27

			EPO; JPO; DERWENT; IBM_TDB			
S33	901	257/30-35,56,62,65,288,471-475,483.ccls. and (substrate wafer semiconductor) near6 silicon and (substrate wafer semiconductor) near6 germanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:27
S34	16	257/30-35,56,62,65,288,471-475,483.ccls. and (substrate wafer semiconductor) near6 silicon and (substrate wafer semiconductor) near6 germanium and (conduct$4 with arsenic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:28
S35	3	"6608352".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:38
S36	1	"13552556"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:47
S37	9867	257/288,E29.255.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:48
S38	0	257/288,E29.255.ccls. and (electrical near juction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:48
S39	16	257/288,E29.255.ccls. and (electrical near junction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:48
S40	5	257/288,E29.255.ccls. and (electrical near junction) and (arsenic "Ar")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:49
S41	535	257/288,E29.255.ccls. and (gate electrode) with arsenic	US-PGPUB; USPAT;	OR	ON	2013/04/04 20:58

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S42	218	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:58
S43	109	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and junction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:58
S44	1	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and junction and (arsenic near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:59
S45	1	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and junction and ((arsenic arsenide)near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 21:02
S46	1	257/288,E29.255.ccls. and (gate electrode) with (arsenic arsenide) and (arsenic with (substrate wafer carrier base plate)) and junction and ((arsenic arsenide)near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 21:02
S47	7	257/288,E29.255.ccls. and (gate electrode) with (arsenic arsenide) and ((arsenic arsenide) with (substrate wafer carrier base plate)) and junction and ((arsenic arsenide)near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 21:02

EAST Search History (Interference)

<This search history is empty>

4/4/2013 10:51:21 PM
C:\Users\mharrison1\Documents\EAST\Workspaces\13552556.wsp

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Courtesy Reminder for
Application Serial No: 13/552,556

Attorney Docket No: 40003771-0003-DC3
Customer Number: 27571
Date of Electronic Notification: 04/15/2013

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 13/552,556

First Named Inventor: Daniel E. Grupp

Filed: July 18, 2012

Art unit: 2896

Examiner: Harrison, Monica D.

Docket No.: 40003771-0003-463

Confirmation No.: 8045

Commissioner for Patents
P.O. Box 1450
Alexandria VA, 22313-1450

PRE-APPEAL REQUEST FOR REVIEW

Dear Commissioner:

Applicants request review of the final rejection in the above-identified application. No amendments are being filed with this request. The review is requested for the reason(s) stated on the attached sheet(s).

This request is being filed with a notice of appeal.

If there are any additional fees due in connection with this communication, please charge Deposit Account No. 50-5798.

Respectfully submitted,
FAHMI, SELLERS, EMBERT & DAVITZ

Dated: August 23, 2013

/Tarek N. Fahmi/
Tarek N. Fahmi
Reg. No. 41,402

84 W. Santa Clara St.
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San Jose, CA 95113-1812
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STATEMENT IN SUPPORT OF PRE-APPEAL BRIEF REQUEST FOR REVIEW

I. STATUS OF CLAIMS

Claims 1-18 are presently pending. Claim 1-9 have been finally rejected, and are the subject of this pre-appeal brief request for review. Claims 10-18 have been indicated as allowable.

II. GROUNDS OF REJECTIONS TO BE REVIEWED

1) Claims 1-4 and 7-9 are rejected under 35 U.S.C. § 102(e) as being anticipated by *Long* (US 6,608,352).

2) Claims 5 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Long* in view of *Sakuma* (US 6,011,271).

III. ARGUMENT

1. Claims 1-4 and 7-9 are patentable over *Long*.

In the Final Office Action mailed on April 15, 2013, claim 1 was rejected as being anticipated by Long. The structure cited in the Office Action, Long's Fig. 3, is shown below.

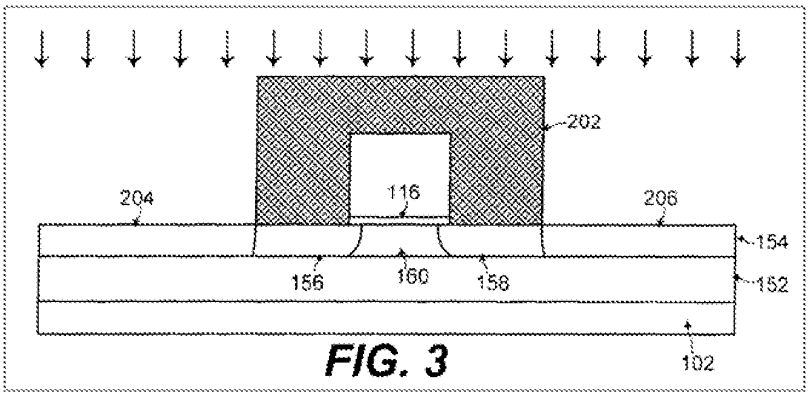


FIG. 3

Referring to this figure, Long describes the various elements as follows:

116: "gate dielectric"

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118: "gate electrode"

152: "buried insulating material"

154: "layer of semiconductor material"

156: "drain region"

158: "source region"

160: "channel region of a MOSFET"

202: "masking structure"

204: "first doped region"

206: "second doped region"

Claim 1 recites:

> An electrical junction, comprising an interface layer disposed between and in contact with a conductor and a semiconductor, the interface layer comprising arsenic.

In rejecting claim 1, the Office Action maps the elements of Long's Figure 3 onto the claim as follows:

Claim element	Long Fig 3 reference
Interface layer	156, 158
Conductor	118
Semiconductor	154, 152, 102
Arsenic	156, 158 (as explained at 5:12-16)

In explaining the rejection, the Office Action states, "The gate structure, which includes the gate oxide (116) and gate electrode (118) are in contact with the doped source (156) and drains (158) regions which comprise arsenic that are formed within the SOI substrate (102, 152 and 154). The elements of the entire stacked structure are all in contact with one another."

This analysis is flawed. Claim 1 specifically recites "an interface layer . . . in contact with a conductor". The Office Action reads source and drain regions 156, 158 as the claimed interface layer. It is apparent from Long's figure 3 and the admission set forth in the office Action that these regions are in contact with the gate dielectric 116 and not the gate electrode 118. Gate dielectric 116 is not a conductor; it is an electrical

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insulator. Hence, in Long, the source and drain regions 156, 158 are in contact with an insulator, not a conductor.

Interpreting the gate electrode 118 and gate dielectric 116 as somehow being one structure that is a conductor ignores the actual teachings of Long. A gate dielectric is an important element of the MOSFET described by Long and is critical to its operation. If the source and drain regions were in direct contact with the gate electrode, a short circuit would result. It is the gate dielectric 116 that prevents such a short circuit and allows the gate to control current flow between the source and drain. Its presence, role and composition cannot be ignored.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of Californi*a, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), see also MPEP § 2131.02. The identical invention must be shown in as complete detail as is contained in the … claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, (Fed. Cir. 1989). Therefore, the present rejection of claim 1 as being anticipated by Long, US Patent No. 6,608,352, is inappropriate because Long does not teach the elements recited in claim 1. Claims 2-4 and 7-9 depend, directly or indirectly, from claim 1 and are therefore patentable over Long for the same reasons as claim 1.

2. Claims 5 and 6 are patentable over *Long* in view of *Sakuma*.

Sakuma is cited for teaching a semiconductors that are silicon and germanium. Office Action at p. 3, para. 5. Even if true, such teachings do not cure the underlying deficiencies of Long, therefore the combination of Long and Sakuma would suffer from such deficiencies. Accordingly, claims 5 and 6, which depend indirectly from claim 1, are patentable over the combination of Long and Sakuma.

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Electronic Patent Application Fee Transmittal

Application Number:	13552556
Filing Date:	18-Jul-2012
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Filer:	Tarek N. Fahmi
Attorney Docket Number:	40003771-0003-DC3

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Notice of Appeal	2401	1	400	400
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 2 months with $0 paid	2252	1	300	300
Miscellaneous:				
		Total in USD ($)		**700**

Electronic Acknowledgement Receipt

EFS ID:	16668764
Application Number:	13552556
International Application Number:	
Confirmation Number:	8045
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	40003771-0003-DC3
Receipt Date:	23-AUG-2013
Filing Date:	18-JUL-2012
Time Stamp:	12:05:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$700
RAM confirmation Number	9600
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Notice of Appeal Filed	40003771-0003-DC3_sb0031_8-23-2013.pdf	215873 8b9288b5a4e164ac545409994c7adc287aa1620b	no	2
Warnings:					
Information:					
2	Pre-Brief Conference request	40003771-0003-DC3_Pre-Appeal_request_8-23-2013.pdf	154437 95d0cf4f30cf1c5041d3e5161739c1bf8ab3da3b	no	4
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	32072 618522398c4187c7a903005cb11fc5bc512c0440	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	402382		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/31 (09-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

NOTICE OF APPEAL FROM THE EXAMINER TO THE PATENT TRIAL AND APPEAL BOARD

Docket Number (Optional): 40003771-0003-DC3

I hereby certify that this correspondence is being facsimile transmitted to the USPTO EFS-Web transmitted to the USPTO, or or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on _____

Signature _____

Typed or printed name _____

In re Application of: Daniel E. Grupp

Application Number	Filed
13/552,556	07/18/2012

For: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES

Art Unit	Examiner
2896	Monica D. Harrison

Applicant hereby **appeals** to the Patent Trial and Appeal Board from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 41.20(b)(1)) $ 800.00

☑ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is: $ 400.00

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 50-5798 .

☑ A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☑ attorney or agent of record. Registration number 41402.

☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____

/Tarek N. Fahmi/
Signature

Tarek N. Fahmi
Typed or printed name

866-877-4883
Telephone number

_____
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 41.31. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/552,556	07/18/2012	Daniel E. Grupp	40003771-0003-DC3	8045

27571 7590 10/07/2013

Fahmi, Sellers, Embert & Davitz
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

EXAMINER	
HARRISON, MONICA D	
ART UNIT	PAPER NUMBER
2896	
MAIL DATE	DELIVERY MODE
10/07/2013	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of Panel Decision from Pre-Appeal Brief Review	Application No. 13/552,556	Applicant(s) GRUPP ET AL.
	Examiner Monica D. Harrison	Art Unit 2896

This is in response to the Pre-Appeal Brief Request for Review filed 23 August, 2013.

1. ☐ **Improper Request** – The Request is improper and a conference will not be held for the following reason(s):

☐ The Notice of Appeal has not been filed concurrent with the Pre-Appeal Brief Request.
☐ The request does not include reasons why a review is appropriate.
☐ A proposed amendment is included with the Pre-Appeal Brief request.
☐ Other: .

The time period for filing a response continues to run from the receipt date of the Notice of Appeal or from the mail date of the last Office communication, if no Notice of Appeal has been received.

2. ☒ **Proceed to Board of Patent Appeals and Interferences** – A Pre-Appeal Brief conference has been held. The application remains under appeal because there is at least one actual issue for appeal. Applicant is required to submit an appeal brief in accordance with 37 CFR 41.37. The time period for filing an appeal brief will be reset to be one month from mailing this decision, or the balance of the two-month time period running from the receipt of the notice of appeal, whichever is greater. Further, the time period for filing of the appeal brief is extendible under 37 CFR 1.136 based upon the mail date of this decision or the receipt date of the notice of appeal, as applicable.

☒ The panel has determined the status of the claim(s) is as follows:
Claim(s) allowed: *10-18*.
Claim(s) objected to: _____.
Claim(s) rejected: *1-9*.
Claim(s) withdrawn from consideration: _____.

3. ☐ **Allowable application** – A conference has been held. The rejection is withdrawn and a Notice of Allowance will be mailed. Prosecution on the merits remains closed. No further action is required by applicant at this time.

4. ☐ **Reopen Prosecution** – A conference has been held. The rejection is withdrawn and a new Office action will be mailed. No further action is required by applicant at this time.

All participants:

(1) *Monica D. Harrison*.	(3) *Hien Phan*.
(2) *Matthew W. Such*.	(4)_____.

/Monica D. Harrison/ Examiner, Art Unit 2896	/Hien Phan/ Hien H. Phan, TQAS TC 2800	/Matthew W. Such/ Supervisory Patent Examiner, Art Unit 2896

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	13/552,556	Filing Date	2012-07-18	Docket Number (if applicable)	3771-0003-DC3	Art Unit	2176
First Named Inventor	Daniel E. Grupp			Examiner Name	Harrison, Monica D.		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 505798

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2013-11-19
Name	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 13/552,556

First Named Inventor: Daniel E. Grupp

Filed: July 18, 2012

Art unit: 2896

Examiner: Harrison, Monica D.

Docket No.: 3771-0003-DC3

Confirmation No.: 8045

Commissioner for Patents
P.O. Box 1450
Alexandria VA, 22313-1450

AMENDMENT

Dear Commissioner:

Reconsideration of this application in view of the following amendments is respectfully requested. This amendment is being filed with a request for continued examination (RCE).

Amendments to the Claims are set forth in the listing of the claims that begins on page 2.

Remarks begin on page 5.

AMENDMENTS TO THE CLAIMS

The following listing of the claims shall replace all previous versions thereof:

1. (Currently Amended) An electrical junction, comprising an interface layer disposed between and in contact with a conductor and a semiconductor, the interface layer comprising arsenic and configured to reduce a height of a Schottky barrier between the conductor and the semiconductor from that which would exist at a junction between the conductor and the semiconductor without the interface layer disposed therebetween, and wherein the electrical junction has a specific contact resistance of less than or equal to approximately 100 $\Omega - \mu m^2$.

2. (Original) The electrical junction of claim 1, wherein the conductor comprises a metal silicide.

3. (Original) The electrical junction of claim 1, wherein the interface layer comprises a monolayer of arsenic.

4. (Original) The electrical junction of claim 3, wherein the conductor comprises a metal silicide.

5. (Currently Amended) The electrical junction of claim [[4]] 1, wherein the semiconductor comprises n-type doped silicon.

6. (Currently Amended) The electrical junction of claim [[4]] 1, wherein the semiconductor comprises n-type doped germanium.

7. (Original) The electrical junction of claim 1, wherein the conductor comprises a source of a transistor.

8. (Original) The electrical junction of claim 1, wherein the conductor comprises a drain of a transistor.

GF Exhibit 1012 - 140/439

9. (Cancelled)

10. (Original) A field effect transistor, comprising a source, a drain, a semiconductor channel region between the source and the drain, a gate proximate the semiconductor channel region, and an interface layer comprising arsenic between the source and the semiconductor channel region.

11. (Original) The field effect transistor of claim 10, wherein the source comprises a metal silicide.

12. (Original) The field effect transistor of claim 10, wherein the interface layer comprises a monolayer of arsenic.

13. (Original) The field effect transistor of claim 12, wherein the source comprises a metal silicide.

14. (Original) The field effect transistor of claim 10, wherein the semiconductor channel region comprises silicon.

15. (Original) The field effect transistor of claim 10, wherein the semiconductor channel region comprises silicon germanium.

16. (Original) The field effect transistor of claim 10, wherein the semiconductor channel region comprises germanium.

17. (Original) The field effect transistor of claim 10, wherein the source comprises a material having a work function substantially equal to a conduction band energy of the semiconductor channel region.

18. (Original) A field effect transistor, comprising a source, a drain, a semiconductor

GF Exhibit 1012 - 141/439

channel region between the source and the drain, a gate proximate the semiconductor channel region, and an interface layer comprising arsenic between the drain and the semiconductor channel region.

19. (New) The electrical junction of claim 1, wherein the electrical junction has a specific contact resistance of less than or equal to approximately 10 $\Omega - \mu m^2$.

20. (New) The electrical junction of claim 1, wherein the electrical junction has a specific contact resistance of less than or equal to approximately 1 $\Omega - \mu m^2$.

GF Exhibit 1012 - 142/439

REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claim 1 has been amended to clarify that the interface layer is configured to reduce a height of a Schottky barrier between the conductor and the semiconductor from that which would exist at a junction between the conductor and the semiconductor without the interface layer disposed therebetween, and wherein the electrical junction has a specific contact resistance of less than or equal to approximately 100 $\Omega - \mu m^2$. Support for these amendments, and for new claims 19 and 20, is found in the specification as originally filed, for example at [0012], [0027], [0049], [0070], etc. As amended, the claims are patentable over *Long*.

In the Final Office Action, claim 1 was rejected as being anticipated by *Long*, US Patent No. 6,608,352. In explaining the rejection, the Office Action states, "The gate structure, which includes the gate oxide (116) and gate electrode (118) are in contact with the doped source (156) and drains (158) regions which comprise arsenic that are formed within the SOI substrate (102, 152 and 154). The elements of the entire stacked structure are all in contact with one another."

Whether or not this analysis is correct,[1] *Long* fails to teach or suggest an As interface layer in contact with a conductor and a semiconductor, which interface layer is configured to reduce a height of a Schottky barrier between the conductor and the semiconductor from that which would exist at a junction between the conductor and the semiconductor without the interface layer disposed therebetween, and wherein the electrical junction has a specific contact resistance as recited in the claims. The Office Action reads source and drain regions 156, 158 as the claimed interface layer. It is apparent from *Long's* figure 3 and the admission set forth in the Office Action that these

[1] Interpreting the gate electrode 118 and gate dielectric 116 as somehow being one structure that is a conductor ignores the actual teachings of *Long*. A gate dielectric is an important element of the MOSFET described by *Long* and is critical to its operation. If the source and drain regions were in direct contact with the gate electrode, a short circuit would result. It is the gate dielectric 116 that prevents such a short circuit and allows the gate to control current flow between the source and drain. Its presence, role and composition cannot be ignored.

GF Exhibit 1012 - 143/439

regions are in contact with the gate dielectric 116 and not the gate electrode 118. Gate dielectric 116 is not a conductor; it is an electrical insulator. But even if the gate dielectric and gate electrode are considered together, the source and drain regions 156, 158 (the alleged interface layer) are not configured to reduce a height of a Schottky barrier to this gate structure. Nor is the source/drain – gate junction configured to have a specific contact resistance as recited in claim 1. Indeed, nowhere does *Long* ever discuss reduction of a Schottky barrier or achieving a specific contact resistance value.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of Californi*a, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), see also MPEP § 2131.02. The identical invention must be shown in as complete detail as is contained in the … claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, (Fed. Cir. 1989). As demonstrated above, *Long* fails to meet these requirements, hence, claim 1 is not anticipated by *Long*. Claims 2-9 and 19-20 depend, directly or indirectly, from claim 1 and are therefore patentable over *Long* for the same reasons as claim 1.

Sakuma is cited for teaching semiconductors that are silicon and germanium. Even if true, such teachings do not cure the underlying deficiencies of *Long*, therefore the combination of *Long* and *Sakuma* would suffer from such deficiencies. Accordingly, claims 5 and 6, which depend indirectly from claim 1, are patentable over the combination of *Long* and *Sakuma*.

If there are any additional fees due in connection with this communication, please charge Deposit Account No. 50-5798.

Respectfully submitted,
FAHMI, SELLERS, EMBERT & DAVITZ

Dated: November 19, 2013

/Tarek N. Fahmi/
Tarek N. Fahmi
Reg. No. 41,402

84 W. Santa Clara St., Suite 550
San Jose, CA 95113-1812
(866) 877-4883

GF Exhibit 1012 - 144/439

Electronic Patent Application Fee Transmittal

Application Number:	13552556
Filing Date:	18-Jul-2012
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Filer:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC3

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with $0 paid	2251	1	100	100

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for Continued Examination	2801	1	600	600
		Total in USD ($)		**700**

Electronic Acknowledgement Receipt

EFS ID:	17448545
Application Number:	13552556
International Application Number:	
Confirmation Number:	8045
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	3771-0003-DC3
Receipt Date:	19-NOV-2013
Filing Date:	18-JUL-2012
Time Stamp:	19:49:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$700
RAM confirmation Number	6836
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Extension of Time	3771-0003-DC3_EOT_Filed_11-19-2013.pdf	68136 fbb2f8b37d95947fb19e9d4032a0664936ec5471	no	1
Warnings:					
Information:					
2	Request for Continued Examination (RCE)	3771-0003-DC3_RCE_Filed_11_19_2013.pdf	697784 bbb3de2b5f116961cf91a905cd359258c334d974	no	3
Warnings:					
Information:					
3		40003771-0003-DC3_Amend_11-19-2013.pdf	130507 39f39ece34d2ceebf1be32d952ef3468cf15acb3	yes	6

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment Submitted/Entered with Filing of CPA/RCE	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	6

Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	31970 c0011bbbf47f187e137c6623cce62e3ba04a983f	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	928397	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 13/552,556

First Named Inventor: Daniel E. Grupp

Filed: July 18, 2012

Art unit: 2896

Examiner: Harrison, Monica D.

Docket No.: 3771-0003-DC3

Confirmation No.: 8045

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION FOR EXTENSION OF TIME PURSUANT TO 37 C.F.R. § 1.136(a)

Sir:

In accordance with 37 C.F.R. § 1.136(a), Applicants for the above-identified application respectfully Petition the Commissioner for a one (1) month extension of time, extending the period for response to November 19, 2013 from the Notice of Panel Decision from Pre-Appeal Brief Review mailed October 7, 2013. The Petition filing fee of $100.00 and a response are included.

Respectfully submitted,

Date: November 19, 2013

/Tarek N. Fahmi/
Tarek N. Fahmi
Reg. No. 41,402

FAHMI, SELLERS, EMBERT & DAVITZ
84 W. Santa Clara St., Ste. 550
San Jose, CA 95113
(866) 877-4883

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/552,556	Filing Date 07/18/2012	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	11/19/2013	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	X $40 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $210 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**0**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/DOROTHY BELL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/552,556	07/18/2012	Daniel E. Grupp	3771-0003-DC3	8045

27571 7590 02/26/2014

Ascenda Law Group, PC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

EXAMINER	
HARRISON, MONICA D	
ART UNIT	PAPER NUMBER
2896	

NOTIFICATION DATE	DELIVERY MODE
02/26/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@ascendalaw.com
tarek.fahmi@ascendalaw.com

Office Action Summary	Application No. 13/552,556	Applicant(s) GRUPP ET AL.	
	Examiner Monica D. Harrison	Art Unit 2896	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/19/13*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-8 and 10-20* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *1-8,19 and 20* is/are allowed.

7)☒ Claim(s) *10-16 and 18* is/are rejected.

8)☒ Claim(s) *17* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

1. Applicant's request for continued examination (RCE) filed 11/19/13 has been entered. Claim 9 is cancelled.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 10, 12, 14 and 18 are rejected under pre-AIA 35 U.S.C. 102(e) as being anticipated by Wang et al (6,380,021 B1).

2. Regarding claim 10, Wang et al discloses a field effect transistor (Figure 9, PMOS), comprising a source (Figure 9, reference 44, *left side*), a drain (Figure 9, reference 44, *right side*), a semiconductor channel region (Figure 9, reference 10, *upper region directly below gate 16*) between the source ((Figure 9, reference 44, *left side*) and the drain (Figure 9, reference 44, *right side*), a gate (Figure 9, reference 16) proximate the semiconductor channel region (Figure 9, reference 10, *upper region directly below gate 16*), and an interface layer comprising arsenic (Figure 9, references 34, *left side*) between the source (Figure 9, reference 44, *left side*) and the semiconductor channel region (Figure 9, reference 10, *upper region directly below gate 16*).

3. Regarding claim 12, Wang et al discloses wherein the interface layer comprises a monolayer of arsenic (Figure 9, reference 34).

4. Regarding claim 14, Wang et al discloses wherein the semiconductor channel region comprises silicon (Figure 9, reference 10).

5. Regarding claim 18, Wang et al discloses a field effect transistor (Figure 9, PMOS), comprising a source (Figure 9, reference 44, *left side*), a drain (Figure 9, reference 44, *right side*), a semiconductor channel region (Figure 9, reference 10, *upper region directly below gate 16*) between the source ((Figure 9, reference 44, *left side*) and the drain (Figure 9, reference 44, *right side*), a gate (Figure 9, reference 16) proximate the semiconductor channel region (Figure 9, reference 10, *upper region directly below gate 16*), and an interface layer comprising arsenic (Figure 9, references 34, *right side*) between the drain (Figure 9, reference 44, *right side*) and the semiconductor channel region (Figure 9, reference 10, *upper region directly below gate 16*).

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11, 13, 15 and 16 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Wang et al (6,380,021 B1) in view of Agnello et al (5,608,266).

6. Wang et al discloses all of the above claimed subject matter.

However, Wang et al does not disclose wherein the source comprises a metal silicide (claims 11 and 13), wherein the semiconductor channel region comprises silicon germanium (claim 15) nor wherein the semiconductor channel region comprises germanium (claim 16).

Agnello et al discloses wherein the source comprises a metal silicide (Figure 7(b), reference 72), wherein the semiconductor channel region comprises silicon germanium (Figure 7(b), reference 11; column 5, line 18) and wherein the semiconductor channel region comprises germanium (Figure 7(b), reference 11; column 5, line 6).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Wang et al with the teachings of Agnello et al for the purpose of forming the source with a metal silicide and the semiconductor channel region with silicon germanium or germanium because silicon germanium and germanium as well as amorphous silicon, single crystal silicon, polycrystalline silicon, amorphous germanium, single crystalline germanium, polycrystalline germanium, or semiconductors or compound semiconductors of columns IIb, IIIa, IVa, Va, and VIa of the periodic table are known substrates used to form the thin film metal silicide which is thermally stable and resistant to agglomeration and layer inversion during elevated thermal cycles in a multi-layer semiconductor device.

Allowable Subject Matter

7. Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose nor fairly suggest wherein the source comprises a

material having a work function substantially equal to a conduction band energy of the semiconductor channel region (claim 17) as incorporated within the independent claim 10 and in the context of its recited apparatus along with its depending claims.

9. Claims 1-8, 19 and 20 are allowed over the prior art of record.

10. The following is an examiner's statement of reasons for allowance:

After further consideration of applicant's arguments, amendments and a further search of the prior art, examiner has concluded that the prior art does not disclose nor fairly suggest an electrical junction comprising: the interface layer comprising arsenic and configured to reduce a height of a Schottky barrier between the conductor and the semiconductor from that which would exist at a junction between the conductor and the semiconductor without the interface layer disposed there between, and wherein the electrical junction has a specific contact resistance of less than or equal to approximately $100\Omega\text{-}\mu m^2$ as described in the independent claim 1 and in the context of their recited apparatus along with its depending claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is (571)272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Such can be reached on 571-272-8895. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Monica D. Harrison/
Examiner, Art Unit 2896

mdh
February 19, 2014

Notice of References Cited	Application/Control No. 13/552,556	Applicant(s)/Patent Under Reexamination GRUPP ET AL.	
	Examiner Monica D. Harrison	Art Unit 2896	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,380,021 B2	04-2002	Wang et al.	438/232
*	B	US-5,608,266	03-1997	Agnello et al.	257/768
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13552556	GRUPP ET AL.
	Examiner	**Art Unit**
	MONICA D HARRISON	2896

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/27/2012	04/05/2013	11/26/2013						
1	1	✓	✓	=						
2	2	✓	✓	=						
3	3	✓	✓	=						
4	4	✓	✓	=						
5	5	✓	✓	=						
6	6	✓	✓	=						
7	7	✓	✓	=						
8	8	✓	✓	=						
	9	✓	✓	-						
11	10	=	=	✓						
12	11	=	=	✓						
13	12	=	=	✓						
14	13	=	=	✓						
15	14	=	=	✓						
16	15	=	=	✓						
17	16	=	=	✓						
18	17	=	=	O						
19	18	=	=	✓						
9	19			=						
10	20			=						

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13552556	GRUPP ET AL.
	Examiner	Art Unit
	MONICA D HARRISON	2896

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	30-35,56,62,65,288,471-475,483	9/25/12	MDH
257	288,E29.255	4/4/13	MDH
257	486,E21.192,E29.148	11/26/13	MDH

SEARCH NOTES		
Search Notes	Date	Examiner
East (USPAT, US-PGPUB, USOCR, EPO, JPO, DERWENT, IBM_TDB, FPRS)	9/25/12	MDH
GRUPP et al. .inv.	9/25/12	MDH
East updated	4/4/13	MDH
East updated	11/26/13	MDH
GRUPP et al. .inv.	11/26/13	MDH
USPAT, US-PGPUB, UPAD txt .clm.	11/26/13	MDH
East updated	2/19/14	MDH

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	USPAT, US-PGPUB, UPAD txt .clm.	11/26/13	MDH

/MONICA D HARRISON/ Examiner.Art Unit 2896	

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	13/552556	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:52
S2	1	13/022522	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:53
S3	2	"7884003".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:53
S4	2	"7462860".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:54
S5	2	"7084423".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:55
S6	2	"6833556".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:00
S7	3697	257/288.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:09
S8	30	257/288.ccls. and ((conductor metal) with	US-PGPUB;	OR	ON	2012/09/25

		arsenic)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:09
S9	12	257/288.ccls. and ((conductor metal) with arsenic) and (arsenic with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:10
S10	2609	(grupp connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:18
S11	25	(grupp connelly).inv. and arsenic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:18
S12	17	(grupp connelly).inv. and (arsenic with interface) and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:19
S13	8062	257/30-35,56,62,65,288,471-475,483.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:27
S14	123	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:27
S15	86	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:29
S16	77	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2012/09/25 11:29

			IBM_TDB			
S17	74	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:29
S18	56	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:30
S19	56	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:30
S20	47	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel and gate and (semiconductor with silicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 12:15
S21	17	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel and gate and (semiconductor with silicon) and (semiconductor with germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 12:15
S22	386	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:20
S23	150	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface) and (interface with metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:20
S24	225	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface) and (interface with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:20
S25	5	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface) and (interface with	US-PGPUB; USPAT; USOCR;	OR	ON	2012/09/25 13:21

		semiconductor) and (interface with arsenic)	FPRS; EPO; JPO; DERWENT; IBM_TDB			
S26	97	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface with arsenic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:21
S27	46	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:21
S28	0	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 siicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:22
S29	44	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 silicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:22
S30	1	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 silicon) and (semiconductor near5 germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:23
S31	2	(conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 silicon) and (semiconductor near5 germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:23
S32	4222	257/30-35,56,62,65,288,471-475,483.ccls. and (substrate wafer semiconductor) near6 silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:27
S33	901	257/30-35,56,62,65,288,471-475,483.ccls. and (substrate wafer semiconductor) near6 silicon and (substrate wafer semiconductor) near6 germanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:27
S34	16	257/30-35,56,62,65,288,471-	US-PGPUB;	OR	ON	2012/09/25

		475,483.ccls. and (substrate wafer semiconductor) near6 silicon and (substrate wafer semiconductor) near6 germanium and (conduct$4 with arsenic)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			13:28
S35	3	"6608352".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:38
S36	1	"13552556"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:47
S37	9867	257/288,E29.255.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:48
S38	0	257/288,E29.255.ccls. and (electrical near juction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:48
S39	16	257/288,E29.255.ccls. and (electrical near junction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:48
S40	5	257/288,E29.255.ccls. and (electrical near junction) and (arsenic "Ar")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:49
S41	535	257/288,E29.255.ccls. and (gate electrode) with arsenic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:58
S42	218	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2013/04/04 20:58

			IBM_TDB			
S43	109	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and junction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:58
S44	1	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and junction and (arsenic near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:59
S45	1	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and junction and ((arsenic arsenide)near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 21:02
S46	1	257/288,E29.255.ccls. and (gate electrode) with (arsenic arsenide) and (arsenic with (substrate wafer carrier base plate)) and junction and ((arsenic arsenide)near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 21:02
S47	7	257/288,E29.255.ccls. and (gate electrode) with (arsenic arsenide) and ((arsenic arsenide) with (substrate wafer carrier base plate)) and junction and ((arsenic arsenide)near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 21:02
S48	70	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" | "7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:06
S49	39	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" | "7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As") with (gate electrode conduct$4 metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:07

S50	23	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" | "7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As") with (gate electrode conduct$4 metal) and (arsenic "As") with (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:08
S51	9	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" | "7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As") with (gate electrode conduct$4 metal) and (arsenic "As") with (substrate wafer carrier base plate) and (arsenic "As") with channel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:08
S52	4445	257/'$'.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:14
S53	177	257/'$'.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and (arsenic near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:14
S54	29	257/'$'.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and (arsenic near (layer film)) and fet	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:15
S55	0	257/486,E21.192,E29.148.ccls. and arsenic near (conduct$4 metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:33
S56	11	257/486,E21.192,E29.148.ccls. and arsenic near9 (conduct$4 metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2013/11/26 16:33

			DERWENT; IBM_TDB			
S57	7	257/486,E21.192,E29.148.ccls. and arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:34
S58	1	257/486,E21.192,E29.148.ccls. and arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:35
S59	18	257/'$'.ccls. and arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:37
S60	25	arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:39
S61	0	arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky and (grupp connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:43
S62	3	arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:43
S64	2	"13552556"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 12:45
S65	2	"6380021".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 12:46
S66	12364	257/288,E29.255.ccls.	US-PGPUB; USPAT; USOCR;	OR	ON	2014/02/18 13:23

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S67	57	257/288,E29.255.ccls. and gate and source and drain and (LDD near7 arsenic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:24
S68	36	257/288,E29.255.ccls. and gate and source and drain and (LDD near7 arsenic) and (silicide salicide) near7 (source drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:24
S69	22	257/288,E29.255.ccls. and gate and source and drain and (LDD near7 arsenic) and (silicide salicide) near7 (source drain) and germanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:37
S70	19	257/288,E29.255.ccls. and gate and source and drain and (LDD near4 arsenic) and (silicide salicide) near7 (source drain) and germanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:37
S71	5	"6608352".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:41
S72	0	257/288,E29.255.ccls. and gate and source and drain and (LDD near4 arsenic) and (metal near (silicide salicide)) near7 (source drain) and germanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:50
S73	1853	257/288,E29.255.ccls. and (metal near silicide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:50
S74	535	257/288,E29.255.ccls. and (metal near silicide) near7 (source drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:52
S75	535	257/288,E29.255.ccls. and (metal near	US-PGPUB;	OR	ON	2014/02/18

		silicide) near7 (source drain) and gate	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			13:55
S76	81	257/288,E29.255.ccls. and (metal near silicide) near7 (source drain) and gate and (arsenic with (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:58
S77	48	257/288,E29.255.ccls. and (metal near silicide) near7 (source drain) and gate and (arsenic with (source drain)) and (germanium "SiGe")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 14:16
S78	969	257/288,E29.255.ccls. and (germanium "SiGe") with channel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 14:40
S79	962	257/288,E29.255.ccls. and (germanium "SiGe") with channel and (gate electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 14:40
S80	386	257/288,E29.255.ccls. and (germanium "SiGe") with channel and (gate electrode) and (silicide with (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 14:41
S81	1981	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:25
S82	161	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:27
S83	107	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2014/02/19 10:27

			IBM_TDB			
S84	107	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide and (gate electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:27
S85	32	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide and (gate electrode) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:28
S86	9	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide and (gate electrode) and (work near function) and (conduction near band)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:28
S87	32	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide and (gate electrode) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:29
S88	107	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide and (gate electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:32
S89	1132	257/288,E29.255.ccls. and germanium near9 (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near9 (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:37
S90	1104	257/288,E29.255.ccls. and germanium near9 (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near9 (substrate wafer carrier base plate) and (gate electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:37
S91	99	257/288,E29.255.ccls. and germanium near9 (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near9 (substrate wafer carrier base plate) and (gate electrode) and (arsenic near9 (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:37
S92	15	257/288,E29.255.ccls. and germanium near(substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near9 (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2014/02/19 10:43

		and (gate electrode) and (arsenic near9 (source drain))	EPO; JPO; DERWENT; IBM_TDB			
S93	169	257/288,E29.255.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:44
S94	164	257/288,E29.255.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:44
S95	154	257/288,E29.255.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate) and gate and source and drain	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:44
S96	61	257/288,E29.255.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate) and gate and source and drain and arsenic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:44
S97	3466	257/'$'.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:50
S98	229	257/'$'.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate) and (gate electrode) and source and drain and arsenic and (metal near silicide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:50
S99	56	257/'$'.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate) and (gate electrode) and source and drain and arsenic and (metal near silicide) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:51

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S63	3	arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky.clm.	US-PGPUB; USPAT; UPAD	OR	ON	2013/11/26 16:48

2/19/2014 2:12:01 PM
C:\Users\mharrison1\Documents\EAST\Workspaces\13552556.wsp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 13/552,556

First Named Inventor: Daniel E. Grupp

Filed: July 18, 2012

Art unit: 2896

Examiner: Harrison, Monica D.

Docket No.: 3771-0003-DC3

Confirmation No.: 8045

Commissioner for Patents
P.O. Box 1450
Alexandria VA, 22313-1450

AMENDMENT

Dear Commissioner:

Reconsideration of this application in view of the following amendments is respectfully requested.

Amendments to the Claims are set forth in the listing of the claims that begins on page 2.

Remarks begin on page 5.

AMENDMENTS TO THE CLAIMS

The following listing of the claims shall replace all previous versions thereof:

1. (Previously Presented) An electrical junction, comprising an interface layer disposed between and in contact with a conductor and a semiconductor, the interface layer comprising arsenic and configured to reduce a height of a Schottky barrier between the conductor and the semiconductor from that which would exist at a junction between the conductor and the semiconductor without the interface layer disposed therebetween, and wherein the electrical junction has a specific contact resistance of less than or equal to approximately 100 $\Omega - \mu m^2$.

2. (Original) The electrical junction of claim 1, wherein the conductor comprises a metal silicide.

3. (Original) The electrical junction of claim 1, wherein the interface layer comprises a monolayer of arsenic.

4. (Original) The electrical junction of claim 3, wherein the conductor comprises a metal silicide.

5. (Previously Presented) The electrical junction of claim 1, wherein the semiconductor comprises n-type doped silicon.

6. (Previously Presented) The electrical junction of claim 1, wherein the semiconductor comprises n-type doped germanium.

7. (Original) The electrical junction of claim 1, wherein the conductor comprises a source of a transistor.

8. (Original) The electrical junction of claim 1, wherein the conductor comprises a drain of a transistor.

GF Exhibit 1012 - 176/439

9. (Cancelled)

10. (Currently Amended) A field effect transistor, comprising a source, a drain, ~~a~~ an n-type semiconductor channel region between the source and the drain, a gate proximate the semiconductor channel region, and an interface layer comprising arsenic between the source and the n-type semiconductor channel region.

11. (Original) The field effect transistor of claim 10, wherein the source comprises a metal silicide.

12. (Original) The field effect transistor of claim 10, wherein the interface layer comprises a monolayer of arsenic.

13. (Original) The field effect transistor of claim 12, wherein the source comprises a metal silicide.

14. (Original) The field effect transistor of claim 10, wherein the semiconductor channel region comprises silicon.

15. (Original) The field effect transistor of claim 10, wherein the semiconductor channel region comprises silicon germanium.

16. (Original) The field effect transistor of claim 10, wherein the semiconductor channel region comprises germanium.

17. (Original) The field effect transistor of claim 10, wherein the source comprises a material having a work function substantially equal to a conduction band energy of the semiconductor channel region.

18. (Cancelled)

GF Exhibit 1012 - 177/439

19. (Previously Presented) The electrical junction of claim 1, wherein the electrical junction has a specific contact resistance of less than or equal to approximately 10 $\Omega - \mu m^2$.

20. (Previously Presented) The electrical junction of claim 1, wherein the electrical junction has a specific contact resistance of less than or equal to approximately 1 $\Omega - \mu m^2$.

21. (New) An electrical junction, comprising an interface layer disposed between and in contact with a conductor and an n-type semiconductor, the interface layer comprising arsenic and a titanium oxide.

GF Exhibit 1012 - 178/439

REMARKS

Reconsideration of this application, as amended, is respectfully requested. The amendments to claim 10 find support in the specification as originally filed, for example at [0075]. New claim 21 finds support in the specification as originally filed, for example at [0027], [0029], [0043]-[0044], [0048]-[0049] and [0075], and Figures 5 and 6.

As amended, claim 10 specifies an arsenic interface layer between a source and an n-type semiconductor channel region. Wang fails to teach or suggest such a device. Instead, Wang teaches the use of an arsenic pocket implant in a p-type semiconductor region. Pocket implants, such as those described by Wang, are similar to halo implants and are used to suppress short channel effects by reducing the extension of the depletion layer into the channel region at source/drain junctions. Importantly for purposes of the present review, pocket implant dopants are always of opposite type to the source/drain dopant. Considering arsenic pocket implants, being n-type, these are applied in p-channel transistors (PFETs), as taught by Wang. Claim 10 recites an arsenic interface layer and an n-type channel. Accordingly, claim 10 and its dependent claims are patentable over Wang.

Moreover, a pocket implant cannot be characterized as a monolayer, as recited in claim 12. Pocket implants are regions (volumes) of doped semiconductor, not associated with a semiconductor interface.

The teachings of Agnello are cited for reasons unconnected with the above reasons for patentability, hence, the claims would remain patentable over the combination of Wang and Agnello.

If there are any additional fees due in connection with this communication, please charge Deposit Account No. 50-5798.

Respectfully submitted,
Ascenda Law Group, PC

Dated: June 5, 2014

/Tarek N. Fahmi/
Tarek N. Fahmi
Reg. No. 41,402

84 W. Santa Clara St., Suite 550
San Jose, CA 95113-1812
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GF Exhibit 1012 - 179/439

Electronic Patent Application Fee Transmittal

Application Number:	13552556
Filing Date:	18-Jul-2012
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Filer:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC3

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with $0 paid	2251	1	100	100

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**100**

Electronic Acknowledgement Receipt

EFS ID:	19228126
Application Number:	13552556
International Application Number:	
Confirmation Number:	8045
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi
Filer Authorized By:	
Attorney Docket Number:	3771-0003-DC3
Receipt Date:	05-JUN-2014
Filing Date:	18-JUL-2012
Time Stamp:	19:57:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$100
RAM confirmation Number	5485
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Extension of Time	3771-0003-DC3_EOT_Filed_06-05-2014.pdf	67585 d8781951d9cd729278cc37e6be07b864da175257	no	1
Warnings:					
Information:					
2		3771-0003-DC3_ROA_Filed_06-05-2014.pdf	114824 5d55fca3fae03ea3d57c3b67b41017e3068fdc3a	yes	5

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	4
	Applicant Arguments/Remarks Made in an Amendment	5	5

Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30169 950b1079d1b76120be6d119ebddcddd65cb12bf5	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	212578		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 13/552,556

First Named Inventor: Daniel E. Grupp

Filed: July 18, 2012

Art unit: 2896

Examiner: Harrison, Monica D.

Docket No.: 3771-0003-DC3

Confirmation No.: 8045

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION FOR EXTENSION OF TIME PURSUANT TO 37 C.F.R. § 1.136(a)

Sir:

In accordance with 37 C.F.R. § 1.136(a), Applicants for the above-identified application respectfully Petition the Commissioner for a one (1) month extension of time, extending the period for response to June 5, 2014 from the Non Final Office Action mailed February 26, 2014. The Petition filing fee of $100.00 and a response are included.

Respectfully submitted,

Date: June 5, 2014

/Tarek N. Fahmi/
Tarek N. Fahmi
Reg. No. 41,402

ASCENDA LAW GROUP, PC
84 W. Santa Clara St., Ste. 550
San Jose, CA 95113
(866) 877-4883

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/552,556	Filing Date 07/18/2012	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	06/05/2014	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	X $40 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $210 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**0**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/MARQUITA JONES/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/552,556	07/18/2012	Daniel E. Grupp	3771-0003-DC3	8045

27571 7590 10/24/2014

Ascenda Law Group, PC
84 W. Santa Clara St.
Suite 550
San Jose, CA 95113

EXAMINER	
HARRISON, MONICA D	
ART UNIT	PAPER NUMBER
2896	

NOTIFICATION DATE	DELIVERY MODE
10/24/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patents@ascendalaw.com
tarek.fahmi@ascendalaw.com

Office Action Summary	Application No. 13/552,556	Applicant(s) GRUPP ET AL.	
	Examiner Monica D. Harrison	Art Unit 2896	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/5/14*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-8,10-17 and 19-21* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *1-8,19 and 20* is/are allowed.

7)☒ Claim(s) *10-16 and 21* is/are rejected.

8)☒ Claim(s) *17* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

1. Applicant's amendment filed 6/5/14 has been entered. Claims 9 and 18 are cancelled.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope

of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit http://www.uspto.gov/forms/. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

3. Claim 21 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim 21 of U.S. Patent No. 8,766,336 B2. Although the claims at issue are not identical, they are not patentably distinct from each other because the subject matter of claim 21 of the instant application is found in claim 21 of the patent.

4. Regarding claim 21, Grupp et al 336' discloses an electrical junction, comprising an interface layer disposed between and in contact with a conductor and an n-type semiconductor, the interface layer comprising arsenic and a titanium oxide (claim 21).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the

> international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 10, 12 and 14 are rejected under pre-AIA 35 U.S.C. 102(e) as being anticipated by Wang et al (6,380,021 B 1).

7. Regarding claim 10, Wang et al discloses a field effect transistor (Figure 9, PMOS), comprising a source (Figure 9, reference 44, left side), a drain (Figure 9, reference 44, right side), an n-type semiconductor channel region (Figure 9, reference 10, upper region directly below gate 16; column 1, lines 66-67 thru column 2, line 1) between the source (Figure 9, reference 44, left side) and the drain (Figure 9, reference 44, right side), a gate (Figure 9, reference 16) proximate the semiconductor channel region (Figure 9, reference 10, upper region directly below gate 16), and an interface layer comprising arsenic (Figure 9, references 34, left side) between the source (Figure 9, reference 44, left side) and the n-type semiconductor channel region (Figure 9, reference 10, upper region directly below gate 16; column 1, lines 66-67 thru column 2, line 1).

8. Regarding claim 12, Wang et al discloses wherein the interface layer comprises a monolayer of arsenic (Figure 9, reference 34).

9. Regarding claim 14, Wang et al discloses wherein the semiconductor channel region comprises silicon (Figure 9, reference 10).

Claim Rejections - 35 USC § 103

10. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 11, 13, 15 and 16 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Wang et al (6,380,021 B 1) in view of Agnello et al (5,608,266).

12. Wang et al discloses all of the above claimed subject matter.

However, Wang et al does not disclose wherein the source comprises a metal silicide (claims 11 and 13), wherein the semiconductor channel region comprises silicon germanium (claim 15) nor wherein the semiconductor channel region comprises germanium (claim 16).

Agnello et al discloses wherein the source comprises a metal silicide (Figure 7(b), reference 72), wherein the semiconductor channel region comprises silicon germanium (Figure 7(b), reference 11; column 5, line 18) and wherein the semiconductor channel region comprises germanium (Figure 7(b), reference 11; column 5, line 6).

It would have been obvious, at the time the invention was made, for one having ordinary skill in the art, to modify Wang et al with the teachings of Agnello et al for the purpose of forming the source with a metal silicide and the semiconductor channel region with silicon germanium or germanium because silicon germanium and germanium as well as amorphous silicon, single crystal silicon, polycrystalline silicon, amorphous germanium, single crystalline germanium, polycrystalline germanium, or semiconductors or compound semiconductors of columns IIb, IIIa, IVa, Va, and Via of the periodic table are known substrates used to form the thin film metal silicide which is thermally stable and resistant to agglomeration and layer inversion during elevated thermal cycles in a multi-layer semiconductor device.

Allowable Subject Matter

13. Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not disclose nor fairly suggest wherein the source comprises a material having a work function substantially equal to a conduction band energy of the semiconductor channel region (claim 17) as incorporated within the independent claim 10 and in the context of its recited apparatus along with its depending claims.

15. Claims 1-8, 19 and 20 are allowed over the prior art of record.

16. The following is an examiner's statement of reasons for allowance:

After further consideration of applicant's arguments, amendments and a further search of the prior art, examiner has concluded that the prior art does not disclose nor fairly suggest an electrical junction comprising: the interface layer comprising arsenic and configured to reduce a height of a Schottky barrier between the conductor and the semiconductor from that which would exist at a junction between the conductor and the semiconductor without the interface layer disposed there between, and wherein the electrical junction has a specific contact resistance of less than or equal to approximately $100\Omega\text{-}\mu m^2$ as described in the independent claim 1 and in the context of their recited apparatus along with its depending claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

17. Applicant's arguments filed 6/5/14 have been fully considered but they are not persuasive.

Applicant argues that the pocket implant cannot be categorized as interface layer. Examiner disagrees. Merriam Webster's definition of an interface is the place or area at which different things meet and communicate with or affect each other. The pocket implant is formed at an interface of the substrate (top surface). The pocket implant is a monolayer formed on the substrate. Thus, claimed limitations have been met.

Related Prior Art

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Ren (Electrochemical Society Proceedings) teaches a Schottky diode with interface layer of arsenic which reduces a height of a Schottky barrier between the conductor metal and the semiconductor from that which would exist at a junction between the conductor and the semiconductor without the interface layer disposed there between. However, since claim 1 sets forth a specific contact resistance value, the structural characteristics are distinguished from Ren since the contact structure must be ohmic in nature. As noted by Berger (J. Electrochem. Soc.), since the device of Ren is a Schottky diode, meaningful specific contact resistance values cannot be determined (see Page 512, Left Col., Lines 7-10), such values are only obtainable for ohmic contacts.

Conclusion

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is (571)272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Such can be reached on 571-272-8895. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Monica D. Harrison/
Examiner, Art Unit 2896

mdh
September 22, 2014

/Matthew W. Such/
Supervisory Patent Examiner, Art Unit 2896

Notice of References Cited	Application/Control No. 13/552,556	Applicant(s)/Patent Under Reexamination GRUPP ET AL.	
	Examiner Monica D. Harrison	Art Unit 2896	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,380,021 B2	04-2002	Wang et al.	438/232
*	B	US-5,608,266	03-1997	Agnello et al.	257/768
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Ren, Q.W., et al. "Metal / Silicon Schottky Barrier Lowering By RTCVD Interface Passivation." Electrochemical Society Proceedings, Vol. 2000-9 (2000): pp. 161-166.
	V	Berger, H.H. "Contact Resistance and Contact Resistivity." J. Electrochem. Soc.: Solid-State Science and Technology. Vol. 119, No. 4 (April 1972): pp. 507-514.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13552556	GRUPP ET AL.
	Examiner	Art Unit
	MONICA D HARRISON	2896

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	30-35,56,62,65,288,471-475,483	9/25/12	MDH
257	288,E29.255	4/4/13	MDH
257	486,E21.192,E29.148	11/26/13	MDH

SEARCH NOTES		
Search Notes	Date	Examiner
East (USPAT, US-PGPUB, USOCR, EPO, JPO, DERWENT, IBM_TDB, FPRS)	9/25/12	MDH
GRUPP et al. .inv.	9/25/12	MDH
East updated	4/4/13	MDH
East updated	11/26/13	MDH
GRUPP et al. .inv.	11/26/13	MDH
USPAT, US-PGPUB, UPAD txt .clm.	11/26/13	MDH
East updated	2/19/14	MDH
East updated	9/22/14	MDH

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	USPAT, US-PGPUB, UPAD txt .clm.	11/26/13	MDH

/MONICA D HARRISON/ Examiner.Art Unit 2896	

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	13/552556	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:52
S2	1	13/022522	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:53
S3	2	"7884003".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:53
S4	2	"7462860".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:54
S5	2	"7084423".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:55
S6	2	"6833556".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:00
S7	3697	257/288.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:09
S8	30	257/288.ccls. and ((conductor metal)	US-PGPUB;	OR	ON	2012/09/25

		with arsenic)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:09
S9	12	257/288.ccls. and ((conductor metal) with arsenic) and (arsenic with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:10
S10	2609	(grupp connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:18
S11	25	(grupp connelly).inv. and arsenic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:18
S12	17	(grupp connelly).inv. and (arsenic with interface) and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:19
S13	8062	257/30-35,56,62,65,288,471-475,483.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:27
S14	123	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:27
S15	86	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:29
S16	77	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2012/09/25 11:29

			IBM_TDB			
S17	74	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:29
S18	56	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:30
S19	56	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:30
S20	47	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel and gate and (semiconductor with silicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 12:15
S21	17	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel and gate and (semiconductor with silicon) and (semiconductor with germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 12:15
S22	386	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:20
S23	150	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface) and (interface with metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:20
S24	225	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface) and (interface with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:20
S25	5	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface) and (interface with	US-PGPUB; USPAT; USOCR;	OR	ON	2012/09/25 13:21

		semiconductor) and (interface with arsenic)	FPRS; EPO; JPO; DERWENT; IBM_TDB			
S26	97	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface with arsenic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:21
S27	46	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:21
S28	0	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 siicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:22
S29	44	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 silicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:22
S30	1	257/'$'.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 silicon) and (semiconductor near5 germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:23
S31	2	(conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 silicon) and (semiconductor near5 germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:23
S32	4222	257/30-35,56,62,65,288,471-475,483.ccls. and (substrate wafer semiconductor) near6 silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:27
S33	901	257/30-35,56,62,65,288,471-475,483.ccls. and (substrate wafer semiconductor) near6 silicon and (substrate wafer semiconductor) near6 germanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:27
S34	16	257/30-35,56,62,65,288,471-	US-PGPUB;	OR	ON	2012/09/25

GF Exhibit 1012 - 201/439

		475,483.ccls. and (substrate wafer semiconductor) near6 silicon and (substrate wafer semiconductor) near6 germanium and (conduct$4 with arsenic)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			13:28
S35	3	"6608352".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:38
S36	1	"13552556"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:47
S37	9867	257/288,E29.255.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:48
S38	0	257/288,E29.255.ccls. and (electrical near juction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:48
S39	16	257/288,E29.255.ccls. and (electrical near junction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:48
S40	5	257/288,E29.255.ccls. and (electrical near junction) and (arsenic "Ar")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:49
S41	535	257/288,E29.255.ccls. and (gate electrode) with arsenic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:58
S42	218	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2013/04/04 20:58

			IBM_TDB			
S43	109	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and junction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:58
S44	1	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and junction and (arsenic near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:59
S45	1	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and junction and ((arsenic arsenide)near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 21:02
S46	1	257/288,E29.255.ccls. and (gate electrode) with (arsenic arsenide) and (arsenic with (substrate wafer carrier base plate)) and junction and ((arsenic arsenide)near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 21:02
S47	7	257/288,E29.255.ccls. and (gate electrode) with (arsenic arsenide) and ((arsenic arsenide) with (substrate wafer carrier base plate)) and junction and ((arsenic arsenide)near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 21:02
S48	70	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" | "7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:06
S49	39	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" | "7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As") with (gate electrode conduct$4 metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:07

S50	23	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" | "7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As") with (gate electrode conduct$4 metal) and (arsenic "As") with (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:08
S51	9	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" | "7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As") with (gate electrode conduct$4 metal) and (arsenic "As") with (substrate wafer carrier base plate) and (arsenic "As") with channel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:08
S52	4445	257/'$'.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:14
S53	177	257/'$'.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and (arsenic near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:14
S54	29	257/'$'.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and (arsenic near (layer film)) and fet	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:15
S55	0	257/486,E21.192,E29.148.ccls. and arsenic near (conduct$4 metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:33
S56	11	257/486,E21.192,E29.148.ccls. and arsenic near9 (conduct$4 metal)	US-PGPUB; USPAT; USOCR;	OR	ON	2013/11/26 16:33

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S57	7	257/486,E21.192,E29.148.ccls. and arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:34
S58	1	257/486,E21.192,E29.148.ccls. and arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:35
S59	18	257/'$'.ccls. and arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:37
S60	25	arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:39
S61	0	arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky and (grupp connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:43
S62	3	arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:43
S64	2	"13552556"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 12:45
S65	2	"6380021".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 12:46
S66	12364	257/288,E29.255.ccls.	US-PGPUB;	OR	ON	2014/02/18

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			13:23
S67	57	257/288,E29.255.ccls. and gate and source and drain and (LDD near7 arsenic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:24
S68	36	257/288,E29.255.ccls. and gate and source and drain and (LDD near7 arsenic) and (silicide salicide) near7 (source drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:24
S69	22	257/288,E29.255.ccls. and gate and source and drain and (LDD near7 arsenic) and (silicide salicide) near7 (source drain) and germanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:37
S70	19	257/288,E29.255.ccls. and gate and source and drain and (LDD near4 arsenic) and (silicide salicide) near7 (source drain) and germanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:37
S71	5	"6608352".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:41
S72	0	257/288,E29.255.ccls. and gate and source and drain and (LDD near4 arsenic) and (metal near (silicide salicide)) near7 (source drain) and germanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:50
S73	1853	257/288,E29.255.ccls. and (metal near silicide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:50
S74	535	257/288,E29.255.ccls. and (metal near silicide) near7 (source drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2014/02/18 13:52

			IBM_TDB			
S75	535	257/288,E29.255.ccls. and (metal near silicide) near7 (source drain) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:55
S76	81	257/288,E29.255.ccls. and (metal near silicide) near7 (source drain) and gate and (arsenic with (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:58
S77	48	257/288,E29.255.ccls. and (metal near silicide) near7 (source drain) and gate and (arsenic with (source drain)) and (germanium "SiGe")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 14:16
S78	969	257/288,E29.255.ccls. and (germanium "SiGe") with channel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 14:40
S79	962	257/288,E29.255.ccls. and (germanium "SiGe") with channel and (gate electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 14:40
S80	386	257/288,E29.255.ccls. and (germanium "SiGe") with channel and (gate electrode) and (silicide with (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 14:41
S81	1981	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:25
S82	161	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:27
S83	107	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2014/02/19 10:27

		source and drain and silicide	EPO; JPO; DERWENT; IBM_TDB			
S84	107	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide and (gate electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:27
S85	32	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide and (gate electrode) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:28
S86	9	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide and (gate electrode) and (work near function) and (conduction near band)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:28
S87	32	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide and (gate electrode) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:29
S88	107	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide and (gate electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:32
S89	1132	257/288,E29.255.ccls. and germanium near9 (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near9 (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:37
S90	1104	257/288,E29.255.ccls. and germanium near9 (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near9 (substrate wafer carrier base plate) and (gate electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:37
S91	99	257/288,E29.255.ccls. and germanium near9 (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near9 (substrate wafer carrier base plate) and (gate electrode) and (arsenic near9 (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:37
S92	15	257/288,E29.255.ccls. and germanium near(substrate wafer carrier base plate)	US-PGPUB; USPAT;	OR	ON	2014/02/19 10:43

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		and ("SiGe" (silicon near germanium)) near9 (substrate wafer carrier base plate) and (gate electrode) and (arsenic near9 (source drain))	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S93	169	257/288,E29.255.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:44
S94	164	257/288,E29.255.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:44
S95	154	257/288,E29.255.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate) and gate and source and drain	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:44
S96	61	257/288,E29.255.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate) and gate and source and drain and arsenic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:44
S97	3466	257/'$'.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:50
S98	229	257/'$'.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate) and (gate electrode) and source and drain and arsenic and (metal near silicide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:50
S99	56	257/'$'.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate) and (gate electrode) and source and drain and arsenic and (metal near silicide) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:51
S100	3	"13552556"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/09/22 09:54

S101	6204	257/288.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/09/22 09:57
S102	2	"6380021".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/09/22 11:12

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S63	3	arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky.clm.	US-PGPUB; USPAT; UPAD	OR	ON	2013/11/26 16:48

9/22/2014 12:30:20 PM
C:\Users\mharrison1\Documents\EAST\Workspaces\13552556.wsp

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13552556	GRUPP ET AL.
	Examiner	**Art Unit**
	MONICA D HARRISON	2896

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/27/2012	04/05/2013	11/26/2013	09/22/2014					
1	1	✓	✓	=	=					
2	2	✓	✓	=	=					
3	3	✓	✓	=	=					
4	4	✓	✓	=	=					
5	5	✓	✓	=	=					
6	6	✓	✓	=	=					
7	7	✓	✓	=	=					
8	8	✓	✓	=	=					
	9	✓	✓	-	-					
11	10	=	=	✓	=					
12	11	=	=	✓	=					
13	12	=	=	✓	=					
14	13	=	=	✓	=					
15	14	=	=	✓	=					
16	15	=	=	✓	=					
17	16	=	=	✓	=					
18	17	=	=	O	O					
19	18	=	=	✓	-					
9	19			=	=					
10	20			=	=					
	21				✓					

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	13552556	Filing Date	2012-07-18	Docket Number (if applicable)	3771-0003-DC3	Art Unit	2896
First Named Inventor	Daniel E. Grupp			Examiner Name	Harrison, Monica D.		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☒ Amendment/Reply

☒ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☒ Other Terminal Disclaimer

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 505798

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Signature of Registered U.S. Patent Practitioner			
Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2015-02-24
Name	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 13/552,556

First Named Inventor: Daniel E. Grupp

Filed: July 18, 2012

Art unit: 2896

Examiner: Harrison, Monica D.

Docket No.: 3771-0003-DC3

Confirmation No.: 8045

Commissioner for Patents
P.O. Box 1450
Alexandria VA, 22313-1450

AMENDMENT

Dear Commissioner:

Reconsideration of this application in view of the following amendments is respectfully requested.

Amendments to the Claims are set forth in the listing of the claims that begins on page 2.

Remarks begin on page 5.

AMENDMENTS TO THE CLAIMS

The following listing of the claims shall replace all previous versions thereof:

1. (Previously Presented) An electrical junction, comprising an interface layer disposed between and in contact with a conductor and a semiconductor, the interface layer comprising arsenic and configured to reduce a height of a Schottky barrier between the conductor and the semiconductor from that which would exist at a junction between the conductor and the semiconductor without the interface layer disposed therebetween, and wherein the electrical junction has a specific contact resistance of less than or equal to approximately 100 $\Omega - \mu m^2$.

2. (Original) The electrical junction of claim 1, wherein the conductor comprises a metal silicide.

3. (Original) The electrical junction of claim 1, wherein the interface layer comprises a monolayer of arsenic.

4. (Original) The electrical junction of claim 3, wherein the conductor comprises a metal silicide.

5. (Previously Presented) The electrical junction of claim 1, wherein the semiconductor comprises n-type doped silicon.

6. (Previously Presented) The electrical junction of claim 1, wherein the semiconductor comprises n-type doped germanium.

7. (Original) The electrical junction of claim 1, wherein the conductor comprises a source of a transistor.

8. (Original) The electrical junction of claim 1, wherein the conductor comprises a drain of a transistor.

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9. (Cancelled)

10. (Currently Amended) A field effect transistor, comprising a source, a drain, an n-type semiconductor channel region between the source and the drain, a gate proximate the semiconductor channel region, and an interface layer comprising arsenic between the source and the n-type semiconductor channel region, wherein the source comprises a material having a work function substantially equal to a conduction band energy of the semiconductor channel region.

11. (Original) The field effect transistor of claim 10, wherein the source comprises a metal silicide.

12. (Original) The field effect transistor of claim 10, wherein the interface layer comprises a monolayer of arsenic.

13. (Original) The field effect transistor of claim 12, wherein the source comprises a metal silicide.

14. (Original) The field effect transistor of claim 10, wherein the semiconductor channel region comprises silicon.

15. (Original) The field effect transistor of claim 10, wherein the semiconductor channel region comprises silicon germanium.

16. (Original) The field effect transistor of claim 10, wherein the semiconductor channel region comprises germanium.

17. (Cancelled)

18. (Cancelled)

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19. (Previously Presented) The electrical junction of claim 1, wherein the electrical junction has a specific contact resistance of less than or equal to approximately 10 $\Omega - \mu m^2$.

20. (Previously Presented) The electrical junction of claim 1, wherein the electrical junction has a specific contact resistance of less than or equal to approximately 1 $\Omega - \mu m^2$.

21. (Previously Presented) An electrical junction, comprising an interface layer disposed between and in contact with a conductor and an n-type semiconductor, the interface layer comprising arsenic and a titanium oxide.

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REMARKS

Reconsideration of this application, as amended, is respectfully requested. Claim 10 has been amended to incorporate the subject matter of former claim 17.

A terminal disclaimer with respect to US 8,766,336 is included herewith.

In view of the forgoing amendments and the terminal disclaimer, all claims should be in condition for allowance as specified in the Office Action.

If there are any additional fees due in connection with this communication, please charge Deposit Account No. 50-5798.

Respectfully submitted,
Ascenda Law Group, PC

Dated: February 24, 2015

/Tarek N. Fahmi/
Tarek N. Fahmi
Reg. No. 41,402

333 W San Carlos, St., Ste. 200
San Jose, CA 95110
(866) 877-4883

GF Exhibit 1012 - 219/439

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	13552556
Filing Date	2012-07-18
First Named Inventor	Daniel E. Grupp
Art Unit	2896
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC3

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	3513366		1970-05-19	CLARK	
	2	4019113		1977-04-19	HARTMAN	
	3	4422090		1983-12-20	SHEPHERD; et al.	
	4	4583110		1986-04-15	JACKSON; et al.	
	5	4723197		1988-02-02	TAKIAR; et al.	
	6	4811077		1969-03-07	FOWLER; et al.	
	7	5027166		1991-06-25	OHTSUKA; et al.	
	8	5098859		1992-03-24	JACKSON; et al.	

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	First Named Inventor	Daniel E. Grupp
	Art Unit	2896
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC3

	9	5308998		1994-05-03	YAMAZAKI; et al.	
	10	5438210		1995-08-01	WORLEY	
	11	5908313		1999-06-01	CHAU; et al.	
	12	5943575		1999-08-24	CHUNG; et al.	
	13	6064082		2000-05-16	KAWAI; et al.	
	14	6071783		2000-06-06	LIANG; et al.	
	15	6091076		2000-07-18	DELEONIBUS; et al.	
	16	6117781		2000-09-12	LUKANC; et al.	
	17	6291282		2001-09-18	WILK; et al.	
	18	6293137		2001-09-25	LIU; et al.	
	19	6326294		2001-12-04	JANG HA SOON; et al.	

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	Application Number	13552556
	Filing Date	2012-07-18
	First Named Inventor	Daniel E. Grupp
	Art Unit	2896
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC3

	20	6339232		2002-01-15	TAKAGI	
	21	6452244		2002-09-17	MIURA; et al.	
	22	6462931		2002-10-08	TANG; et al.	
	23	6548875		2003-04-15	NISHIYAMA	
	24	6680224		2004-01-20	SHIN; et al.	
	25	5943575		1999-08-24	CHUNG; et al.	

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	2	2004/015782	WO	A1	2004-02-19	ACORN TECHNOLOGIES, INC.		☐

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	3	2004/030104	WO	A1	2004-04-08	ACORN TECHNOLOGIES, INC.		☐

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(54) Structure and fabrication method for schottky and ohmic electrodes onto semiconductor devices

(57) A novel electrode structure for Schottky electrodes and Ohmic electrodes and novel methods of fabricating electrodes by freely controlling electric characteristics of electrodes on semiconductors. Interface states density of a semiconductor (11) after deposition of an electrode metal (13, 14) is decreased by flattening the surface of the semiconductor on an atomic level to freely control the Schottky barrier height. The method can realize an ideal Ohmic electrode having a Schottky barrier height of substantially zero. The Schottky barrier height is varied freely by decreasing the interface level density and selecting work function of the electrode metal. The method can provide stable Schottky and Ohmic electrodes (13, 14) without need of heat treatment. Further, the method can provide Ohmic electrodes without high concentration doping.

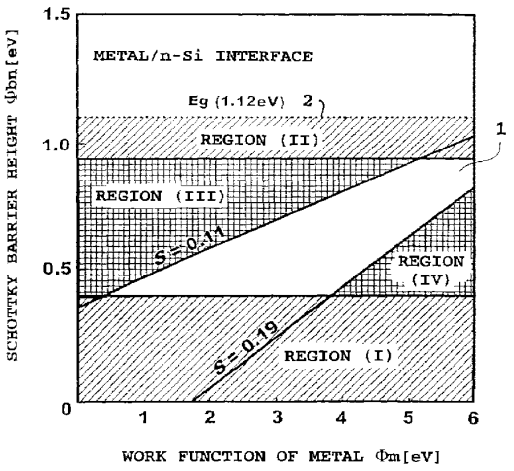


FIG.2

EP 0 789 388 A2

GF Exhibit 1012 - 230/439

Description

The present invention relates to an electrode provided on a semiconductor and a method for fabricating an electrode on a semiconductor. The present invention is applicable to various fields of industry which involve fabrication of electrodes on semiconductors. For example, the present invention can be applied to various semiconductor devices such as microprocessors, memories, power devices and the like.

In conventional fabrication methods of electrodes on semiconductors, rectifying potential barriers, i.e., Schottky barriers, which will appear on the interfaces between electrode metals and semiconductors, have been impossible to control their magnitude. Hence, it has been impossible to artificially control the rectifying properties and conductivities of all the electrodes including not only those semiconductor devices whose performance depends directly on the heights of Schottky barriers, such as Schottky diodes as typical examples, but also those electrodes in the semiconductor devices thus far fabricated. The Schottky barrier height and leakage current, which is an indicator of important performance of interface on the device, inconveniently vary to a greater extent depending on combination of metals and semiconductors as well as on the process in which the interface is formed. Conventionally, this problem has been solved empirically. That is, when a new semiconductor has been developed, a method for fabricating an electrode on the semiconductor has been investigated and developed for each metal one after another until a suitable one is obtained. In other words, going into detail, there have conventionally been developed unique fabrication methods for fabricating electrodes adapted for respective combinations of semiconductors and electrode metal materials. Because of having had to resort to empirical rule, methods for fabricating electrodes differ from institution to institution or from manufacturer to manufacturer. There has been established no fabrication method for fabricating electrodes which method can be uniformly applied to any or most of electrode metal/semiconductor combinations. Under the circumstances, development of electrodes has needed much human and monetary resources for investigation. In all the semiconductor device fabrication technology inclusive of technologies for fabricating integrated semiconductor devices such as VLSIs and the like, only the technology for forming electrodes has remained as a unit technology that is out of reach of successful efforts for free designing.

More specific explanation will be made as to how to fabricate electrodes for Schottky electrodes and Ohmic electrodes, respectively.

First, in the case of Schottky electrodes, it was almost impossible to control their Schottky barrier height and, hence there was no other way than accept such non-controlled values as they are. For example, silicon Schottky diodes have almost fixed barrier heights on the order of about 0.5 to about 0.7 eV. While use of different metals or application of heat to cause interface reaction will vary barrier height to some extent, the width of change in barrier height is at most about 0.2 eV. Thus, in Schottky devices, the Schottky barrier height, which is the most important indicator for the device characteristics, cannot be controlled freely.

In the case of Ohmic electrodes, a severer problem arises. That is, electrode fabrication inevitably results in the formation of a Schottky barrier whose interface usually shows rectifying resistance. As a result, formation of a conductive Ohmic electrode, which is contrary to the fabrication of an electrode having a rectifying resistance, requires in principle a very difficult technique. Practically, in fabrication of almost all of the Ohmic electrodes fabricators have presupposed presence of a Schottky barrier in the interface between the electrode metal and semiconductor and then taken a measure to allow a leakage current to flow in the barrier.

There have been known several methods for increasing a leakage current. For example, a method for fabricating a device in which impurity ions are doped to extremely increase the concentration of electrons or holes which contribute to conductivity in the vicinity of the surface of the semiconductor (cf., e.g., E.H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988, M.Murakami: Materials Science Reports, 5, 273 (1990), P.A. Barnes and A.Y. Cho, Appl. Phys. Lett, 33, 651 (1978), and T. Uemoto: Jpn. J. Appl. Phys., 34, L7 (995)). This reduces the width of the Schottky barrier, i.e., decreases the thickness of the depletion layer and, hence, a leakage current in the form of tunneling current, can be flown in the thin depletion layer. However, in the case of SiC, GaN and the like new semiconductor materials that are under development are usually difficult to dope with impurities at high concentrations so that electrodes having sufficiently low resistance cannot be obtained in most cases. The above-described method is not simple nor convenient in some cases since it requires an ion implanting apparatus or an electric oven for diffusing impurities in gaseous phases. Furthermore, the concentration of impurities has an upper limit at about $10^{20}cm^{-3}$. This automatically determines the minimum width of the depletion layer and, hence, sets technical limits to the interface resistance of an Ohmic electrode to be realized. Theoretically, this approach is unsuccessful in making the interface resistance of the Ohmic electrode to be zero. In addition, there may occur reflection of electrons or holes between the high concentration doped region and the low concentration doped substrate. This reflection of carriers increases the resistance of the electrode. From these, the interface resistance of an Ohmic electrode fabricated on a silicon substrate is limited to about $10^{-8}\ \Omega cm^2$ based on the technical restrictions as described above.

Another method for fabricating an Ohmic electrode is to heat the electrode to decrease its resistance (cf., e.g., E. H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988, M.

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Murakami: Materials Science Reports, 5, 273 (1990), H.C. Card: IEEE Trans. Electron Devices, ED-23, 538 (1976), T.C. Shen, G.B. Gao, and H. Morkoç: J. Vac. Sci. Technol., B10, 2113 (1992), N. Braslau, J.B. Gunn, and J.L. Staples: Solid-State Electronics, 10, 381 (1967), J. Appl. Phys., 77, 1317 (1967), and J. Crofton, P.G. McMullin, J.R. Williams, and M.J. Bozack: J. Appl. Phys., 77, 1317 (1995)). In this method, after the electrode metal is deposited, heat treatment is carried out so that there occurs interface chemical reaction between the metal and the semiconductor and metallization of the semiconductor proceeds in the vicinity of the interface. This induces impurity level or defect level in the depletion layer of the Schottky barrier. These levels generate leakage current. This method is simple and can be used in combination with high concentration doping. Because of the advantages, the method is used without fail in the conventional process of fabricating electrodes. However, interface reaction is complicated since it differs from a metal/semiconductor system to another and the mode of reaction varies widely depending on temperature and time of heat treatment. In some reaction systems, it is often the case that heating results in the formation of good Schottky barrier, which means heating does not always enhance Ohmicity (cf., e.g., S. Zaima, T. Yamauchi, Y. Koide, and Y. Yasuda: Appl. Surf. Sci., 70, 624 (1993)). This is a decisive defect of the above-described heating method.

Still another approach is to grow on a first semiconductor a crystal of a second semiconductor having a bandgap smaller than that of the first semiconductor so that the highest possible Schottky barrier height can be decreased to facilitate the formation of Ohmic contact (cf., e.g., E.H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988, M.Murakami: Materials Science Reports, 5, 273 (1990), and T.C. Shen, G.B. Gao, and H. Morkoç: J. Vac. Sci. Technol., B10, 2113 (1992)). This method involves heteroepitaxy of a semiconductor and, hence, its application is limited to semiconductor systems which allow heteroepitaxy.

Further, heteroepitaxy itself is a high technology which requires a complicated manufacturing process, which increases production costs. Therefore, the method is suited to a very limited range of semiconductor materials, more particularly, new semiconductor materials having wide bandgaps, such as GaN and the like, which are difficult to dope impurities with high concentration doping of impurities.

The above-described three methods use large process apparatus suitable for fabricating devices and thus are not simple. Accordingly, in early stages of research and development for evaluating electric properties of materials or developing various devices, simpler means such as scratching of semiconductor or the like is used (here, by the term "scratching" is meant to hurt the surface of a semiconductor with a diamond needle or the like to coarsen it (cf., e.g., E.H. Rhoderick and R.H. Williams: "Metal-Semiconductor Contacts, 2nd Ed.," Oxford Science Publications, 1988). On a coarse surface, a lot of structural defects are induced which increase leakage current. This method is quite inconvenient for making fine structures in the fabrication of semiconductor devices. In most cases, no good interface resistance can be obtained.

As described above, electrodes have been fabricated based on empirical rules. The primary reason for this is a lack of common or uniform understanding of the mechanism in forming a metal/semiconductor interface potential barrier. Uncontrollability of Schottky barriers and complexity of the mechanism of Ohmic contact formation which is attributable thereto would be due to the fact that Schottky barrier height is by nature fixed to a certain level. Fixation of Schottky barrier height of a semiconductor is equivalent to the fact that the Fermi level is fixed in the bandgap of the semiconductor on the metal/semiconductor interface. The fixation of Fermi level is usually referred to pinning of the Fermi level. The pinning of the Fermi level occurs as a result of generation of electron level in the bandgap of a semiconductor on the interface between the metal and the semiconductor. Carriers flow from bulk to the interface, i.e., electrons in the case of n-type semiconductor or holes in the case of p-type semiconductor flow from the bulk semiconductor to the interface and the carriers are trapped therein to create an electric double layer of the semiconductor bulk and the interface, i.e., a potential barrier or Schottky barrier.

Reviewing the development of Schottky barrier, in 1947, J. Bardeen stated that the interface level is caused by electronic level due to dangling bonds and the like existing on the surface of the semiconductor (cf. J. Bardeen: Phys. Rev., 71, 717 (1947)). Thereafter, however, in view of the impossibility of controlling the surface level density accurately by the technology available at that time, the leading view was that surface level density was uncontrollable and intrinsic to the material concerned, and interface electron level embedded in a solid should be an essential electron level that was more difficult to control than the surface level. The belief that pinning was intrinsic to materials and cannot be controlled artificially has led to a theory of MIGS (Metal-induced Gap States) which explains a cause of generation of interface levels (cf. V. Heine: Phys. Rev., 138, A1689 (1965)). According to this theory, interface levels are induced when a metal approaches toward the semiconductor. Since 1965 when V. Heine proposed it, the MIGS theory has been leading to date. The MIGS theory has inhibited research of a technology which controls the height of Schottky barrier. In fact, regardless of theories, there have been unavailable high technologies that can control interface level density in actual semiconductor devices.

Concerning numerical consideration of pinning, the work which referred to Schottky barrier for the first time was by W. Schottky (cf. W. Schottky: Naturwissenschaften, 26, 843 (1938) and N.F. Mott: Proc. Camb. Philos. Soc., 34, 568 (1938)). According to Schottky, the Schottky barrier height, φbn, of a n-type semiconductor is given by the following equation (1):

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$$\varphi bn=\varphi m-\chi S+C \quad (1)$$

wherein φm is a work function of the metal, χS is electron affinity of the semiconductor, C is a constant no greater than several meV. On the other hand, the Schottky barrier height of a p-type semiconductor in a pinning-free state is given by the following equation (2):

$$\varphi bp=Eg-(\varphi m-\chi S+C) \quad (2)$$

wherein Eg is a bandgap.

The equations (1) and (2) are called Schottky models. However, no interface has been realized that meets these equations. The actual interface is expressed by the following equation (3):

$$\varphi bn=S(\varphi m-\chi S)+C \quad (3)$$

wherein S is a coefficient which indicates a dependence of φbn on φm and $0 \leq S \leq 1$.

When S=0, φbn is constant and the interface is pinned strongly. This state is called a Bardeen barrier. On the contrary, when S=1, the equation (3) is the same as the equation (3) and represents a pinning-free interface according to the Schottky-Mott model. Actual interfaces fall between the both states. Heretofore, the S factor has been believed to be a physical property specific to the material concerned and, hence, beyond control.

Table 1 below summarizes values of S factor and maximum and minimum values of Schottky barrier height of representative semiconductors.

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Table 1

PINNING RATIOS S OF VARIOUS KNOWN SEMICONDUCTORS AND RANGE OF SCHOTTKY BARRIER HEIGHT

SEMI-CONDUCTOR	S FACTOR	INTERCEPT PARAMETER	MINIMUM SCHOTTKY BARRIER HEIGHT [eV]	MAXIMUM SCHOTTKY BARRIER HEIGHT [eV]
Ge	$0.18 \geq S \geq 0.05$[1]	$-0.23 \leq C_2 \leq 0.11$[1]		
Si(001)	$0.19 \geq S \geq 0.11$[1]	$-0.34 \leq C_2 \leq 0.35$[1]	0.37($GdSi_2/HoSi_2$)[2]	0.94(IrSi3)[3]
GaAs(001)	$0.22 \geq S \geq 0.06$[1]	$-0.40 \leq C_2 \leq 0.075$[1]	0.62(Mg)[4]	0.96(Cu)[4]
GaP	$0.21 \geq S \geq 0.07$[1]	$0.45 \leq C_2 \leq 0.80$[1]		
InP	$0.37 \geq S \geq 0.24$[1]	$-1.00 \leq C_2 \leq 0.81$[1]		
ZnS	$0.66 \geq S \geq 0.21$[1]	$-1.63 \leq C_2 \leq 0.91$[1]		
ZnSe	$0.24 \geq S \geq 0.17$[1]	$-0.25 \leq C_2 \leq 0.57$[1]		
6H-SiC(0001)	$0.25 \geq S \geq 0.23$[5-10]	$-3.5 \leq C_2 \leq 0.15$[5-10]	0.73(Ti)[6]	1.37(Au)[5]

1. B.L. Sharma and S.C. Gupta, Solid State Technology, 23(6), 90 (1980).
2. K.N. Tu, R.D. Thompson, and B.Y.Tsaur, Appl. Phys. Lett. 38, 626(1981).
3. C.S. Petersson, et al., J. Appl. Phys., 50, 3357 (1979).
4. J.R. Waldrop, J. Vac. Sci. Technol., B2, 445 (1984).
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7. L.M. Porter, et al., Mat. Res. Soc. Symp. Proc., 287, 471 (1993).
8. L.M. Porter, et al., J. Mat. Res., 10, 26 (1995).
9. L.M. Porter, et al., J. Mat. Res., 10, 668 (1995).
10. L.M. Porter, et al., M. Mat. Res. 10, 2336 (1995).

Fig. 1 is a graphical presentation of the data in Table 1, plotting Schottky barrier height (ϕ_{Bn} [eV]) against work function of a metal (ϕ_m [eV]) taking as an example of an n-type Si(001) semiconductor substrate. Fig. 1 shows that the Schottky barrier height was limited within a certain range for various metals. In Fig. 1, reference numeral 1 denotes an area representing the range in which the Schottky barrier heights of conventionally fabricated metal/n-Si interfaces fall and 2 denotes a line which represents an absolute upper limit of the Schottky barrier height of metal/n-Si interfaces corresponding to the bandgap Eg=1.12 eV. With different metals, there are always upper and lower limits of the Schottky

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barrier heights.

Consequently, it has heretofore been impossible to freely control the Schottky height of metal/semiconductor interfaces.

The present invention is directed to overcoming the problem of uncontrollability of the Schottky barrier height between an electrode metal and a semiconductor, which problem has been an important subject since a transistor was invented.

Also, the present invention is aimed at solving the scientific and technological problem of uncontrollability of Ohmic electrodes, which has heretofore been considered a different problem from the uncontrollability of Schottky barrier height.

Further, the present invention is intended to provide a systematic technology which can control both Schottky electrodes and Ohmic electrodes, that have been treated separately one from another, based on a single principle that allows understanding them consistently. More specifically, the present invention is directed to overcoming the problem of uncontrollability of pinning of Fermi level of the interface of metal/semiconductor that has been impossible to control conventionally.

Therefore, an object of the present invention is to provide a method for fabricating Schottky electrode or Ohmic electrode formed at the interface between an electrode metal/semiconductor, which enables freely controlling electric properties of the electrode formed on the semiconductor.

Another object of the present invention is to provide an electrode structure comprising an electrode having a controlled Schottky barrier height of the interface between the electrode metal and the semiconductor.

According to a first aspect of the present invention, there is provided a method of fabricating a layer of an electrode metal on a surface of a semiconductor, comprising the step of:

decreasing a surface states density of the surface of the semiconductor.

According to a second aspect of the present invention, there is provided a method of fabricating a layer of an electrode metal on a surface of a semiconductor, comprising the step of:

controlling a Schottky barrier height of a rectifying Schottky electrode formed on the surface of the semiconductor.

Here, the control of the Schottky barrier height of the Schottky electrode may be carried out by controlling flatness of an electrode metal/semiconductor interface.

The control of the Schottky barrier height of the Schottky electrode may be carried out by controlling a step density on an atomic level of an electrode metal/semiconductor interface.

The control of the Schottky barrier height of the Schottky electrode may be carried out by controlling selecting a work function of the metal.

The control of the Schottky barrier height of the Schottky electrode may be carried out by controlling the Schottky barrier height of the Schottky electrode under conditions without giving thermal hysteresis.

According to a third aspect of the present invention, there is provided a method of fabricating a layer of an electrode metal on a surface of a semiconductor, comprising the step of:

fabricating a Schottky electrode from a metal having a high work function, and fabricating an Ohmic electrode from a metal having a low work function, for an n-type semiconductor, or

fabricating a Schottky electrode form a metal having a low work function and an Ohmic electrode from a metal having a high work function, for a p-type semiconductor.

Here, the method may further comprise the step of heating.

According to a fourth aspect of the present invention, there is provided a method of fabricating an Ohmic electrode, comprising the step of: forming flat electrode metal/semiconductor interface on an atomic level.

According to a fifth aspect of the present invention, there is provided a method of fabricating an Ohmic electrode, comprising the step of: forming an electrode metal/semiconductor interface having a low step density on an atomic level.

According to a sixth aspect of the present invention, there is provided a method of fabricating an electrode, comprising the step of:

fabricating an Ohmic electrode as described above in a highly integrated electronic device.

Here, the semiconductor may be made of a semiconductor selected from the group consisting of Si and SiC.

The electrode metal may be selected from the group consisting of Al, Au, Mo and Ti.

According to a seventh aspect of the present invention, there is provided a Schottky electrode structure provided on a semiconductor having an interface portion which is flat on an atomic level.

According to an eighth aspect of the present invention, there is provided a Schottky electrode structure provided on a semiconductor having a Schottky barrier height which is impossible to realize by conventional method.

According to a ninth aspect of the present invention, there is provided a Schottky electrode structure provided on a semiconductor containing no high concentration impurity.

According to a tenth aspect of the present invention, there is provide an Ohmic electrode structure having a Schottky barrier height which is substantially zero.

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Here, the semiconductor may be made of a semiconductor selected from the group consisting of Si and SiC.

The electrode metal may be selected from the group consisting of Al, Au, Mo and Ti.

According to an eleventh aspect of the present invention, there is provided a method of fabricating an electrode, comprising the step of:

oxidizing a surface layer of silicon or silicon carbide on a surface of a semiconductor and removing the resulting oxide film.

Here, the oxidizing of the silicon or silicon carbide may be carried out by heating the silicon or silicon carbide in an oxidative gaseous atmosphere.

Removing the oxide film may be carried out by reacting the oxide film with a reducing liquid or gas.

The silicon or silicon carbide may be n-type silicon or n-type silicon carbide, and wherein the electrode metal is a metal having a work function lower than that of noble metals.

The silicon carbide may be p-type silicon carbide, and wherein the electrode material is a noble metal or a metal having a work function of a level substantially equal to that of noble metals.

The electrode material may be titanium (Ti).

The electrode material may be aluminum (Al).

The above and other objects, effects, features and advantages of the present invention will become more apparent from the following description of the embodiment thereof taken in conjunction with the accompanying drawings.

Fig. 1 is a graph plotting Schottky barrier height of a Schottky electrode fabricated on an n-type Si(001) substrate by a conventional method against the work function of the electrode metal;

Fig. 2 is a graph illustrating regions representing Schottky barrier heights realized by the fabrication method of the present invention;

Fig. 3 is a graph illustrating current-voltage characteristics of Ti electrodes on SiC according to examples of the present invention;

Fig. 4 is a graph illustrating current-voltage characteristics of a Ti electrode on SiC which has been subjected to a conventional treatment with 5% hydrofluoric acid;

Fig. 5 is a graph illustrating current-voltage characteristics of an Al electrode on SiC according to the present invention;

Fig. 6 is a graph illustrating current-voltage characteristics of Al electrodes on SiC according to the present invention;

Fig. 7 is a graph illustrating current-voltage characteristics of an Al electrode on Si(111) which has been subjected to a conventional treatment with 5% hydrofluoric acid;

Fig. 8A is a sketch prepared based on an optical micrograph of the surface of a Ti electrode fabricated by the fabrication method according to EXAMPLE 4 of the present invention;

Fig. 8B is a schematic cross sectional view showing the Ti electrode illustrated in Fig. 8A;

Fig. 9A is a sketch prepared based on an optical micrograph of the surface of an Ni electrode fabricated by a conventional fabrication method;

Fig. 9B is a schematic cross sectional view showing the Ti electrode illustrated in Fig. 9A;

Fig. 10 is a graph illustrating logarithmic current-voltage characteristics of Au electrodes on 6H-SiC(0001) substrates according to EXAMPLE 7 of the present invention;

Fig. 11 is a graph plotting Schottky barrier height of electrode metals fabricated on 6H-SiC(0001) substrates against the work function of the electrode metals; and

Fig. 12 is a graph illustrating new areas for Schottky barrier heights of electrode metals fabricated on 6H-SiC(0001) substrates using the techniques of the present invention.

In order to solve the problem of uncontrollability of Schottky barrier height, it is only necessary to decrease the interface states density of the interface between an electrode metal and a semiconductor on which the electrode metal layer is formed. According to the present invention, a decrease in the interface states density is realized by decreasing the surface states density of the semiconductor before deposition of a metal thereon. The decrease in the surface states density can be realized primarily by flattening the surface of a semiconductor on an atomic level.

Flattening of the surface of a semiconductor results in a decrease in an atomic step density which generates dangling bond density which is a cause of surface states and in an amount of unstable atoms adsorbed on the surface of the semiconductor. According to the present invention, it has been found for the first time that flattening of the surface of a semiconductor on an atomic level decreases the surface states density of the semiconductor and that a decrease in the surface states density is effective for decreasing the interface states density of the electrode metal/semiconductor structure.

Recently, the technology of flattening the surface of semiconductors on an atomic level has developed rapidly and a variety of methods have been proposed. The present invention uses the newest known atomic level surface flattening

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technologies to demonstrate the above effect. However, the present invention should not be construed as being limited to specific atomic level surface flattening techniques. There have been known several important techniques for flattening surfaces of semiconductors on an atomic level, all of which have been proved useful in decreasing interface level density according to the present invention.

The present invention is based on a principle contrary to the conventional method in which particularly in the case of Ohmic contact, the desired Ohmic contact has been realized by intentionally decreasing ideality of interface, i.e., abruptness of structural connection.

Description will be made on how to flatten the surface of a semiconductor on an atomic level. An example of such a method is to set up conditions of oxidation appropriately so that oxidation can proceed flat on an atomic level, thus making the surface of the semiconductor after etching more flattened than the original surface.

Another method is a treatment with dilute hydrofluoric acid adjusted to have an appropriate pH. The pH of the solution can be rendered alkaline with ammonia water. Such a solution has an activity of flattening the surface of a semiconductor on an atomic level by means of a weak etching action of a lot of OH groups contained in the solution. Similarly, a semiconductor may be immersed in boiling water. This method can flatten the surface of a semiconductor on an atomic level by means of a weak etching action of deionized water.

High temperature heat treatment in hydrogen gas is also effective for flattening the surface of a semiconductor. Homoepitaxial growth can accelerate surface migration of atoms at relatively low growth rates to flatten the surface of crystal growth. As the last example, a method utilizing electromigration can also be used for flattening the surface of a semiconductor on an atomic level. Electromigration is a phenomenon in which upon application of electric current to a sample, surface atoms will migrate in a direction the same as or opposite to the direction in which electric current flows. Use of this method semiconductor surfaces can be flattened depending on the conditions. The present invention is not limited to the above-described specific methods. Instead, any method that can flatten semiconductor surfaces on an atomic level may be used similarly and will be effective for decreasing interface levels.

Hereinbelow, the idea of flattening semiconductor surfaces on an atomic level will be described in more detail. To be flat on an atomic level means existence of wide flat terraces when viewed on an atomic level. This directly indicates that an atomic step density is low in the surface concerned. Atoms at a step generally have more dangling bonds than atoms on a terrace. While the dangling bonds on a terrace will disappear after the formation of an interface with a metal due to bonding with the metal, the dangling bonds at a step will not disappear completely because of the step or difference in height as high as the thickness of one atomic layer. Therefore, after the formation of an interface, a main cause of generation of interface states is dangling bonds at steps. In other words, a decrease in a step density will result in a decrease in an interface level density. Hence, in order to decrease an interface states density, it is sufficient to flatten the surface of a semiconductor so that its step density can be decreased. Thus, even if the surface is not flattened when viewed on a scale on the order of micrometers, existence of wide terraces in more minute regions will suffice for decreasing interface states. Therefore, electrode structures with an interface having wide terraces on an atomic level, even though they have uneven or rough surfaces when viewed in a broader region, will cause a decrease in surface states density and, hence, fall within the scope of the present invention as defined below in appended claims.

If the interface states density is reduced enough by one of the above-described methods, the pinning of Fermi level will disappear. On such a pinning-free interface, what determines its potential barrier is merely a difference between respective Fermi levels, i.e., a difference between respective work functions, of the metal and the semiconductor. In this case, Schottky-Mott model expressed by equations (1) and (2) above is followed. Therefore, in the case of an n-type semiconductor, use of a metal having a high work function results in the formation of a Schottky barrier while use of a metal having a low work function gives rise to an Ohmic contact. To control the Schottky barrier height, it is only necessary to select an appropriate metal with regard to work function. For p-type semiconductors, the same idea as that for n-type semiconductors can be applied except that relationship of the magnitudes of the work functions should be reversed.

According to the present invention, the Schottky barrier height of a semiconductor can be expanded to a minimum value of 0 eV (cf. Fig. 2, region (I)) and a maximum value equivalent to the bandgap (cf. Fig. 2, region (II)).

Also, controlling the degree of pinning will in effect vary the Schottky height and, hence, controlling interface level density will enable the Schottky barrier height even when the same metal is used. That pinning can be controlled means that the Schottky barrier height can be controlled at will for each metal. As a result, the region where the Schottky barrier height can be controlled is expanded to regions (III) and (IV) in Fig. 2.

As described above, the present invention has made it possible to expand the region where the Schottky barrier height can appear from region (1) to regions (I) to (IV) in Fig. 2. Therefore, for a given metal, electrodes having the Schottky barrier heights within one of the regions (I) to (IV) also fall within the scope of the present invention. The present invention is generally applicable and operable regardless of the kind of metal and for all n-type and p-type semiconductor substrates, can be set up the regions (I) to (IV) as illustrated in Fig. 2 according to the present invention. Table 1 above indicates the Schottky barrier height regions of the present invention for representative semiconductor materials.

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Another important feature of the present invention is that control of Schottky/Ohmic property can be performed without heat treatment. However, if heat treatment is carried out after the deposition of electrode metals, still a flat interface can be obtained since originally a flat surface on an atomic level is provided, an interface reaction between the metal and the semiconductor occurs uniformly in the interface therebetween. Therefore, the present invention is also effective to electrodes which are subjected to heat treatment.

While not intended to be bound thereto, the present invention can be applied suitably to fabrication of electrodes on silicon carbide (SiC). While SiC is a material with which p- and n-type semiconductors can be used with ease, they have various excellent physical properties such as large a large bandgap. The present invention will be explained further taking SiC as an example. Since in the present invention, processes are used that do not involve heat treatment, no appreciable interface chemical reaction does occur between the metal and the semiconductor. Therefore, the resulting interface receives the conditions of the surface of the semiconductor without any change, and the interface has electrical characteristics which depend on structural and chemical properties of the surface of SiC before the deposition of the electrode metal. In other words, control of the conditions of the surface of SiC makes it possible to control electric properties freely.

When no treatment is performed on the surface of SiC, a natural oxide film is formed thereon. Also, a lot of water and/or impurity atoms are adsorbed on the SiC surface. Further, in the case of as ground surfaces, there are near the surface a lot of impurity atoms contaminating or defects induced upon grinding. Such conditions depend strongly on the process by which the SiC surface is fabricated so that the resulting surface does not always have the same surface atomic conditions and surface electronic state and then unstable.

In the present invention, a method is used which depends strongly on the conditions of surface atoms as described above. Therefore, such an unstable surface layer must be removed. For this purpose, SiC is oxidized and then the resulting oxide film is removed. The oxidation and removal of the oxide film may be performed simultaneously.

As a specific example of oxidation method for oxidizing silicon carbide (SiC), there can be used a method in which SiC is heated in an oxidizing gas atmosphere. The oxidation can be carried out at a heating temperature within the range of usually 800 to 1,250°C, preferably 950 to 1,150°C.

Concerning the selection of metals for use as an electrode material, a lot of metal materials with which Ohmic electrodes have not been realized by the conventional high temperature heat treatment can be used for forming Ohmic electrodes according to surface condition controlling technique in the fabrication method for fabricating electrodes on SiC according to the present invention. Properly speaking, a theoretical approach for realizing an Ohmic contact for n-type semiconductors is to use metal materials having a low work function. However, conventionally, Ohmic contacts were obtained by coarsening or roughening the interface by means of high temperature heat treatment to provide the interface with a non-ideal (non-uniform) structure and metal materials having a high work function which are difficult to oxidize were used in order to prevent the high temperature oxidation. On the contrary, in the present invention, heat treatment does not have to be done so that the interface is abrupt enough to be ideal one and then it is possible to realize an Ohmic contact for those metal materials which do not have high work function naturally. Here, metals which do not have high work functions are those metal materials composed mainly of elements other than noble metals (Ni, Pd, Pt, Cu, Ag, and Au) having high work functions, such as Ni which has been used conventionally. More specifically, a wide variety of metals can be used, including, for example, Mg, Ca, Sr, Ba, Sc, Y, La, Ti, Zr, Hf, V, Nb, Ta, Cr, Mn, Re, Fe, Al, Ga, In, Tl and the like. Among these, those metals having not so high an oxidizing capability, e.g., Ti and Al, are preferred.

In order to realize Ohmic contacts with p-type semiconductors, theoretically, metal materials having high work functions should be used. Conventionally, however, Ohmic contacts were formed by addition of impurities in high concentrations and, hence, aluminum (Al) has been used as an electrode metal because it can serve as a p-type impurity. However, Al has a low work function and is not suited as a metal for p-type metals. In the present invention, metals having high work functions are used. More specifically, metals which can be used for p-type semiconductors for forming Ohmic contacts include noble metals such as Ni, Pd, Pt, Cu, Ag, and Al and metals having approximately the same work function as the noble metals, such as Co, Rh, Ir, Ru, Os, and Re.

In the case of n-type SiC, if heat treatment is required after the formation of electrodes, a metal which is resistant to oxidation and has a high work function can be deposited on the above-described electrode metals having low work functions to prevent oxidation of the electrode portions. Similar effects can be obtained by depositing two or more metals having low work functions on a metal forming a metal semiconductor interface. Therefore, if heating is needed or desired, the above-described effect of the present invention cannot be deteriorated. What is important in the present invention is to use a metal having a low work function for an n-type SiC and a metal having a high work function for a p-type SiC. Practically, metals are divided into low and high work function metals when they have work functions up to 4.5 eV or higher than 4.5 eV. However, 4.5 eV is not a strict threshold value. This is because when a metal is deposited on SiC at ambient (room) temperature, e.g., about 20°C, mutual diffusion of the atoms constituting the metal and the atoms constituting the SiC semiconductor may occur on the metal/semiconductor interface and effective work function alters, if the metal used is highly reactive. So, 4.5 eV is to be understood to be a practical standard for classifying

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metals.

More specifically, the present invention comprises an oxidation process using an oxidative gas. Usually, a sample is placed in an oxidative atmosphere in an apparatus which enables heating of the sample, such as electric oven, and the sample is heated at a temperature within the range of 800 to 1,250°C. With this treatment, the surface of the sample becomes insulating due to formation of an oxide film thereon and a sufficient electric contact is not achieved. Then, the oxide film is removed with a reducing liquid or gas. It is often the case that the atoms on the surface of SiC are arranged or accumulate in a manner different from that the atoms in the bulk of the SiC. The oxidation process in an oxidative gaseous atmosphere is meant to oxidize such a denatured surface layer and make the surface layer ready to be removed by a liquid process including dissolving the surface oxide layer with a reducing liquid to remove it, or gaseous process involving reducing the surface oxide layer with a reducing gas to convert the oxide layer to a semiconductor of non-oxidized state.

In conventional processes for fabricating electrodes, immersion or dipping of a semiconductor in a dilute hydrofluoric acid has been conducted to remove spontaneous oxide film on the surface of SiC. However, no intentional or artificial oxidation of SiC has been performed so that the unstable surface layer has not been removed completely, thus failing to provide stable Ohmic contacts.

According to the present invention, development of Schottky and Ohmic electrodes, which has heretofore been made relying on experience or empirical rules, can be made in a shorter time than before since the present invention is based on a systematized knowledge. Thus, efforts for the development of electrodes can be minimized. The method for fabricating electrodes according to the present invention does not need heat treatment, which makes a great increase in stability of the electrode structure as compared with the conventional method in which heat treatment is essential. Further, In the case of fabricating Ohmic electrodes, conventional methods use doping semiconductors with impurities in high concentrations. In the present invention, however, high concentration doping is unnecessary so that Ohmic electrodes can be fabricated simply and conveniently. In contrast to the conventional methods in which leakage current in the Schottky barrier is used, the method for fabricating electrodes according to the present invention can reduce the Schottky barrier height to zero so that high performance Ohmic electrodes having theoretically no interface resistance that has not been achieved conventionally.

According to the present invention, Schottky barrier heights, that have been almost impossible to control by conventional methods, can be controlled freely by controlling interface level density and selecting work function of metals.

In practicing the present invention, it is only necessary to make the surface of a semiconductor as flat as possible on an atomic level. There are various kinds of known techniques for flattening the surface of a semiconductor on an atomic level and all such techniques can be used in the present invention. Therefore, there is no technical difficulty in practicing the present invention and the present invention can be applied to various metals and semiconductors simply and conveniently.

Hereinafter, the present invention will be described in greater detail by examples with reference to the attached drawings. However, the present invention should not be construed as being limited thereto.

EXAMPLE 1 Confirmation of Ohmic Property (SiC-Ti Structure)

In the instant example, vacuum sublimated n-type 6H-SiC was used as a semiconductor substrate immediately after it was ground. The substrate had a carrier density of about $1x10^{17}$ cm^{-3}. At this carrier density, usually, the semiconductor was not metallic and it was difficult to produce an Ohmic contact. The substrate was cleaned using methanol and trichloroethylene, and then placed in an electric oven filled with an oxygen gas atmosphere and oxidized at 300 °C for 30 minutes, followed by 800°C for 10 minutes. Thus an oxide film of about 5 nm thick was formed. The substrate was dipped in 5% hydrofluoric acid to remove the oxide film.

On the thus-obtained SiC substrate was deposited titanium (Ti), which is a representative high melting metal and has a low work function. The work function of Ti was 4.4 eV, which is by 0.9 eV lower than Ni, which has conventionally been used as an Ohmic electrode and has a work function of 5.3 eV. The SiC substrate used was not heated previously. The thickness of deposited film was about 500 nm. Deposition was not carried out on the entire surface of the semiconductor but through a metal mask formed with a round hole of 0.30 mm in diameter for subsequent electrical measurements.

Fig. 3 is a graph illustrating current-voltage (I-V) characteristics of the sample taken out of the vacuum apparatus (cf. line 3a). As apparent from Fig. 3, the line 3a is a straight line. Lack of nonlinearity as shown by the straight line 3a in Fig. 3 clearly indicates that the electrode obtained is Ohmic, that is, current is proportional to voltage. The interface resistance of the resulting electrode was $6.7x10^{-2}$ Ωcm^2. The electrode made of a SiC material having a low carrier density as low as $2x10^{17}$ cm^{-3} had an Ohmic contact which had theoretically the lowest resistance.

An electrode structure was fabricated in the same manner as in EXAMPLE 1 except that no oxidative etching was conducted but only dipping in 5% hydrofluoric acid was performed (COMPARATIVE EXAMPLE 1). The comparative electrode structure showed no Ohmic property but exhibited Schottky property (Fig. 4). In Fig. 4, curves 4a and 4b

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show normal and reverse direction leakage currents, respectively.

EXAMPLE 2 Confirmation of Ohmic Property (SiC-Al structure)

Next, an electrode structure was fabricated in the same manner as in EXAMPLE 1 except that instead of Ti was used aluminum (Al), which is a non-transient, low melting metal and belonging to the group (III) of the periodic table. In this case, too, was obtained an Ohmic contact similar to that fabricated in EXAMPLE 1. The work function of Al is 4.3 eV. Fig. 5 shows current-voltage characteristics of the aluminum electrode fabricated under the same conditions as the Ti electrode. Similarly to EXAMPLE 1, a line 5 representing the current-voltage characteristics of the Al electrode showed linearity and the interface resistance was about 1.4×10^{-2} Ωcm^2. The electrode made of a SiC material having a low carrier density as low as 2×10^{17} cm^{-3} had an Ohmic contact which had theoretically the lowest resistance.

What is common between EXAMPLE 1 and EXAMPLE 2 is that the both metals used have work functions by about 1 eV lower than those of noble metals used as electrode metal for SiC in the conventional methods. The both metals tested here exhibited effects which attain the objects of the present invention.

EXAMPLE 3 Confirmation of Ohmic Property (Si-Al structure)

The instant example is to show that the present invention is applicable to Si substrates and also realize Ohmic contacts. As a semiconductor substrate was used an n-type Si substrate having a carrier density of 7×10^{16} cm^{-3}. The substrate was cleaned using methanol and trichloroethylene, and then placed in an electric oven filled with an oxygen gas atmosphere and oxidized at 300°C for 30 minutes, followed by 800°C for 10 minutes. Thus an oxide film of about 50 nm thick was formed. The substrate was dipped in 5% hydrofluoric acid to remove the oxide film. The substrate thus obtained was dipped in hot water to make the surface of the semiconductor substrate flat on an atomic level. Thereafter, aluminum was deposited on the surface as an electrode metal. Fig. 6 illustrates current-voltage characteristics of the resulting electrode structure. A line 6a, which is a straight line, represents the sample with 5% hydrofluoric acid treatment. A line 6b, which is also a straight line, represents the sample with hot water treatment after 5% hydrofluoric acid treatment. A line 6c, which is also a straight line, represents the sample with 5% hydrofluoric acid treatment followed by hot water treatment. Here, by the term "hot water treatment" is meant a treatment with heated deionized water at a temperature below 100°C. From Fig. 6, it is apparent that the electrode fabricated according to the present invention has an Ohmic contact having a good linearity of current-voltage characteristics (the line 6c). Heretofore, as illustrated in Fig. 1, no metal could provide an Ohmic contact for Si substrates without high concentration doping. In fact, a comparative sample having an Si(111) substrate which did not subjected to high concentration doping and having a carrier density of 7×10^{16} cm^{-3} (COMPARATIVE EXAMPLE 2) gave a Schottky barrier whose φbn was 0.69 eV after receiving the same 5% hydrofluoric acid treatment as in the instant example (Fig. 7). In Fig. 7, curves 7a and 7b denote current flows in normal and reverse directions, respectively. Comparing the lines 6a to 6c in Fig. 6, it is observed that according as flattening processes are added or flatness increases, current increases and contact resistance decreases. In the instant example (the line 6c in Fig. 6), the doping concentration was 7×10^{16} cm^{-3}, at which the width of the depletion layer is sufficiently thick and no tunneling will occur theoretically. Therefore, the Ohmic property observed in the sample of the instant example is considered to be attributable to a sufficiently decreased Schottky barrier.

EXAMPLE 4 Structural Uniformity of Electrode Structure

A Ti electrode was fabricated in the same manner as in EXAMPLE 1. Fig. 8A is an illustrative view prepared based on an optical micrograph of the surface of the Ti electrode. Fig. 8B is an expanded schematic cross sectional view showing the Ti electrode shown in Fig. 8A. As COMPARATIVE EXAMPLE 3, was prepared an Ni electrode by a conventional heat treatment method. The Ni electrode fabricated by cleaning using methanol and trichloroethylene, the same n-type SiC substrate as used in EXAMPLE 1, depositing Ni thereon by vapor deposition and then heating the substrate at 1,000°C for 60 minutes. Fig. 9A is an illustrative view prepared based on an optical micrograph of the surface of the Ni electrode. Fig. 9B is an expanded schematic cross sectional view showing the Ni electrode shown in Fig. 8A. In Figs. 8A and 9A, reference numeral 11 denotes an SiC substrate, 12 is an outline contour line of the electrode, 13 is an Ni electrode, and 14 is a Ti electrode. The both Ni and Ti electrodes were in the form of a disk of 0.3 mm in diameter. From Figs. 8A, 8B, 9A and 9B, it is apparent that the Ti electrode fabricated on SiC fabricated without heat treatment in accordance with the present invention has a high flatness in surface. The Ni electrode 13 shown in Fig. 9A has a rough surface, clearly lacking structural uniformity. In contrast, in the Ti electrode 14 of the present invention, no region is observed where surface conditions are different, and the area inside a contour line 12 of the electrode 14 is uniform in appearance and highly flat, thus presenting excellent structure for Ohmic structure. The electrode fabricated according to the method of the present invention (Fig. 8B) had a surface with an unevenness (X1) of 5 nm or

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less. On the contrary, the electrode fabricated by the conventional method (Fig. 9B) had a surface with an unevenness (X2) of about 200 nm. This clearly indicates that the electrode fabricated by the method of the present invention had a surface flatness much superior to the electrode fabricated by the conventional method.

EXAMPLE 5 Dependence on Atomic Level Flattening Treatment - Epitaxial Growth

The same SiC substrate immediately after grinding as used in EXAMPLE 1 was dipped in boiling water (100°C) for 10 minutes. On the other hand, a sample was prepared by homoepitaxially growing SiC on the same SiC substrate after grinding as used in EXAMPLE 1. The sample was dipped in boiling water (100°C) for 10 minutes. Then, difference in current-voltage characteristics between the epitaxial SiC substrate and the SiC substrate immediately after grinding were examined. In the case of the epitaxial SiC substrate, an expectation will be made that flattening in surface proceeds sufficiently so that the interface level density decreases and as a result, the Schottky barrier height decreased and Ohmic property increases. In fact, the SiC substrate immediately after grinding had an interface resistance of 1.2×10^{-2} Ωcm^2 (the line 3c in Fig. 3) while the epitaxial SiC substrate had an improved interface resistance of 6×10^{-3} Ωcm^2 (the line 3d in Fig. 3). From this it follows that epitaxial growth is effective for flattening on an atomic level the surface of a semiconductor and for decreasing interface level density of the semiconductor.

EXAMPLE 6 Dependence on Atomic Level Flattening Treatment - pH Adjusted Dilute Hydrofluoric Acid Treatment

An oxidized/etched substrate having a current-voltage characteristics represented by the line 3a in Fig. 3 as used in EXAMPLE 1 was dipped in a pH adjusted dilute hydrofluoric acid for 10 minutes. Then, a metal was deposited on the surface of the thus obtained substrate. In Fig. 3, the line 3b represents the current-voltage characteristics of the electrode sample. In this case, the dilute hydrofluoric acid was adjusted to pH 10. Comparison of the line 3b with the line 3a shows that the interface resistance is improved to 1.5×10^{-2} Ωcm^2. As demonstrated in the instant example, pH adjusted dilute hydrofluoric acid treatment is also effective in decreasing interface level density.

EXAMPLE 7 Fabrication of a Schottky Electrode Showing Less Leakage

Fig. 10 illustrates current-voltage characteristics of gold (Au) electrode on 6H-SiC(0001) face. Lines 10a, 10b and 10c show normal direction leakage currents and 10a', 10b' and 10c' show reverse direction leakage currents. In the case of SiC surface with usual 5% hydrofluoric acid treatment, the reverse direction leakage current was on the order of 10^{-7} A/cm^2 (line 10a'). When oxidation/etching treatment was conducted, the reverse direction leakage current was decreased to 10^{-19} A/cm^2 or less (line 10b'), thus showing a drastically improvement in leakage characteristics by 12 digits. Furthermore, with additional boiling water treatment, the reverse direction leakage current was further improved by 2 digits to 10^{-21} A/cm^2 (line 10c'). This indicates that oxidation/etching treatment and boiling water treatment which accelerate flattening of the surface of the semiconductor weaken the pinning of the Schottky barrier. To note, in the instant example, the electrode itself was subjected to no heat treatment. Therefore, the instant example clearly shows that high quality Schottky electrode can be fabricated without heat treatment of the electrode.

EXAMPLE 8 Control of Pinning and Schottky Barrier Height

Fig. 11 illustrate Schottky barrier height for various metals deposited on 6H-SiC(0001) face. The horizontal axis indicates work function of the metal. In the case of usual pretreatment with 5% hydrofluoric acid, the Schottky barrier height does not substantially depend on the work function of the metal and S factor which indicates an inclination of the line is about 0.2 (line 11a). Then, atomic level flattening of SiC was conducted by oxidation/etching treatment, S=0.8 was obtained, which indicates almost pinning free state (line 11b). Further, boiling water treatment gives rise to S=1.0, which indicates no pinning is observed (line 11c). Thus, the present invention realized pinning free state for those semiconductors which inherently show pinning. As a result, the Schottky barrier height can be freely changed merely by changing the work function of the metal as illustrated in Fig. 11 clearly. When the same metal is used, change in the process of atomic level flattening of the surface of the semiconductor results in varied Schottky barrier height. Note that for Ti electrodes, Schottky barrier heights were theoretically estimated from contact resistance values.

Fig. 12 illustrates Schottky barrier heights of Schottky electrodes fabricated on 6H-SC(0001) substrates by the conventional method and by the methods of the examples of the present invention. For strict comparison, conventional electrodes were fabricated on clean surfaces and I-V characteristics values measured at room temperature were used. The data of the conventional electrodes exist in the region (0). Ti, Mo and Au electrodes subjected to oxidation/etching treatment and boiling water treatment according to the present invention are plotted in regions (I), (IV) and (II), respectively. The data show that the present invention made it possible to realize Schottky barrier heights beyond the lower limit (region (I)) and beyond the upper limit (region (II) that were impossible to achieve by the conventional method.

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The Mo electrode plotted in region (IV) gives the same Schottky barrier height as that of the conventional Ti electrode having lower work function. This means that to give a certain Schottky barrier height, those metals that were considered inappropriate in view of pinning action can be used in the method of the present invention.

As described above, Schottky barrier height of semiconductors can be freely controlled according to the present invention.

Table 2 summarizes the results of examples and Comparative examples above.

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Table 2

	Substrate	Electrode Metal	Treatment	Figure	Interface Resistance ($10^{-2}\Omega cm^2$)	Reverse Direction Leakage Current (A/cm^2)	Surface Unevenness (nm)
Ex. 1	SiC	Ti	A+B	Fig. 3 Line (a)	6.7		
C.Ex.1	SiC	Ti	B	Fig. 4			
Ex. 2	SiC	Al	A+B	Fig. 5	1.4		
Ex. 3	Si	Al	A+B	Fig. 6 Line (a)			
	Si	Al	B+C	Fig. 6 Line (b)			
	Si	Al	A+B+C	Fig. 6 Line (c)			
C.Ex.2	Si	Al	B	Fig. 7			
Ex. 4	SiC	Ti	A+B	Fig. 8A, Fig. 8B			5≥
C.Ex.3	SiC	Ni	Cleaning* Heating 1,000°C	Fig. 9A, Fig. 9B			200

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Table 2 (Continued)

	Substrate	Electrode Metal	Treatment	Figure	Interface Resistance ($10^{-2}\Omega cm^2$)	Reverse Direction Leakage Current (A/cm^2)	Surface Unevenness (nm)
Ex. 5	SiC (Bulk)	Ti	A+B+C	Fig. 3 Line (c)	1.2		
	SiC-SiC (Epitaxial)	Ti	A+B+C	Fig. 3 Line (d)	0.6		
Ex. 6	SiC	Ti	A+B'	Fig. 3 Line (b)	1.5		
Ex. 7	6H-SiC (0001)	Au	A+B	Fig. 10		10^{-19}	
	6H-SiC (0001)	Au	A+B+C	Fig. 10		10^{-21}	
C.Ex.4	6H-SiC (0001)	Au	B	Fig. 10		10^{-7}	
Ex. 8	6H-SiC (0001)	Ti, Mo, Ni	A+B+C	Fig. 11			

*: with methanol and trichloroethylene

The present invention has been described in detail with respect to an embodiment, and it will now be apparent

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from the foregoing to those skilled in the art that changes and modifications may be made without departing from the invention in its broader aspects, and it is the intention, therefore, in the appended claims to cover all such changes and modifications as fall within the true spirit of the invention.

Claims

1. A method of fabricating a layer of an electrode metal on a surface of a semiconductor, characterized by comprising the step of:
   decreasing a surface states density of said surface of said semiconductor.

2. A method of fabricating a layer of an electrode metal on a surface of a semiconductor, characterized by comprising the step of:
   controlling a Schottky barrier height of a rectifying Schottky electrode formed on said surface of said semiconductor.

3. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling flatness of an electrode metal/semiconductor interface.

4. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling a step density on an atomic level of an electrode metal/semiconductor interface.

5. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling selecting a work function of the metal.

6. The method as claimed in claim 2, characterized in that said control of the Schottky barrier height of said Schottky electrode is carried out by controlling the Schottky barrier height of the Schottky electrode under conditions without giving thermal hysteresis.

7. A method of fabricating a layer of an electrode metal on a surface of a semiconductor, characterized by comprising the step of:

   fabricating a Schottky electrode from a metal having a high work function, and fabricating an Ohmic electrode from a metal having a low work function, for an n-type semiconductor, or
   fabricating a Schottky electrode form a metal having a low work function and an Ohmic electrode from a metal having a high work function, for a p-type semiconductor.

8. The method as claimed in any one of claims 2 to 7, characterized by further comprising the step of heating.

9. A method of fabricating an Ohmic electrode, characterized by comprising the step of: forming flat electrode metal/semiconductor interface on an atomic level.

10. A method of fabricating an Ohmic electrode, characterized by comprising the step of: forming an electrode metal/semiconductor interface having a low step density on an atomic level.

11. A method of fabricating an electrode,
    characterized by comprising the step of:
    fabricating an Ohmic electrode as claimed in any one of claim 1 to 10 in a highly integrated electronic device.

12. The method as claimed in any one of claims 1 to 11, characterized in that said semiconductor is made of a semiconductor selected from the group consisting of Si and SiC.

13. The method as claimed in any one of claims 1 to 12, characterized in that said electrode metal is selected from the group consisting of Al, Au, Mo and Ti.

14. A Schottky electrode structure provided on a semiconductor characterized by having an interface portion which is flat on an atomic level.

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15. A Schottky electrode structure provided on a semiconductor characterized by having a Schottky barrier height which is impossible to realize by conventional method.

16. An Ohmic electrode structure provided on a semiconductor characterized by containing no high concentration impurity.

17. An Ohmic electrode structure characterized by having a Schottky barrier height which is substantially zero.

18. The electrode structure as claimed in any one of claims 14 to 17, characterized in that said semiconductor is made of a semiconductor selected from the group consisting of Si and SiC.

19. The electrode structure as claimed in any one of claims 14 to 17, characterized in that said electrode metal is selected from the group consisting of Al, Au, Mo and Ti.

20. A method of fabricating an electrode,
characterized by comprising the step of:
oxidizing a surface layer of silicon or silicon carbide and removing the resulting oxide film.

21. The method as claimed in claim 20, characterized in that said oxidizing of the silicon or silicon carbide is carried out by heating the silicon or silicon carbide in an oxidative gaseous atmosphere.

22. The method as claimed in claim 20, characterized in that said removing the oxide film is carried out by reacting the oxide film with a reducing liquid or gas.

23. The method as claimed in any one of claims 20 to 22, characterized in that said silicon or silicon carbide is n-type silicon or n-type silicon carbide, and wherein said electrode metal is a metal having a work function lower than that of noble metals.

24. The method as claimed in any one of claims 20 to 22, characterized in that said silicon carbide is p-type silicon carbide, and wherein said electrode material is a noble metal or a metal having a work function of a level substantially equal to that of noble metals.

25. The method as claimed in claim 23, characterized in that said electrode material is titanium (Ti).

26. The method as claimed in claim 23, characterized in that said electrode material is aluminum (Al).

27. A method of producing a Schottky diode or other semiconductor device having electrodes which includes fabricating electrodes by any method or combination of methods as claimed in any of claims 9 to 13 or 20 to 26 or which includes fabricating electrodes by patterning or fabricating in a pattern a layer of electrode metal produced by any method claimed in claims 1 to 8.

28. A semiconductor device having at least two metal electrodes formed on a semiconductor surface and wherein the flatness of the semiconductor surface is different at each interface with said two respective metal electrodes.

29. A device according to claim 28 wherein the electrodes are ohmic and Schottky electrodes respectively, and the interfaces therewith are atomically flat and other than atomically flat respectively.

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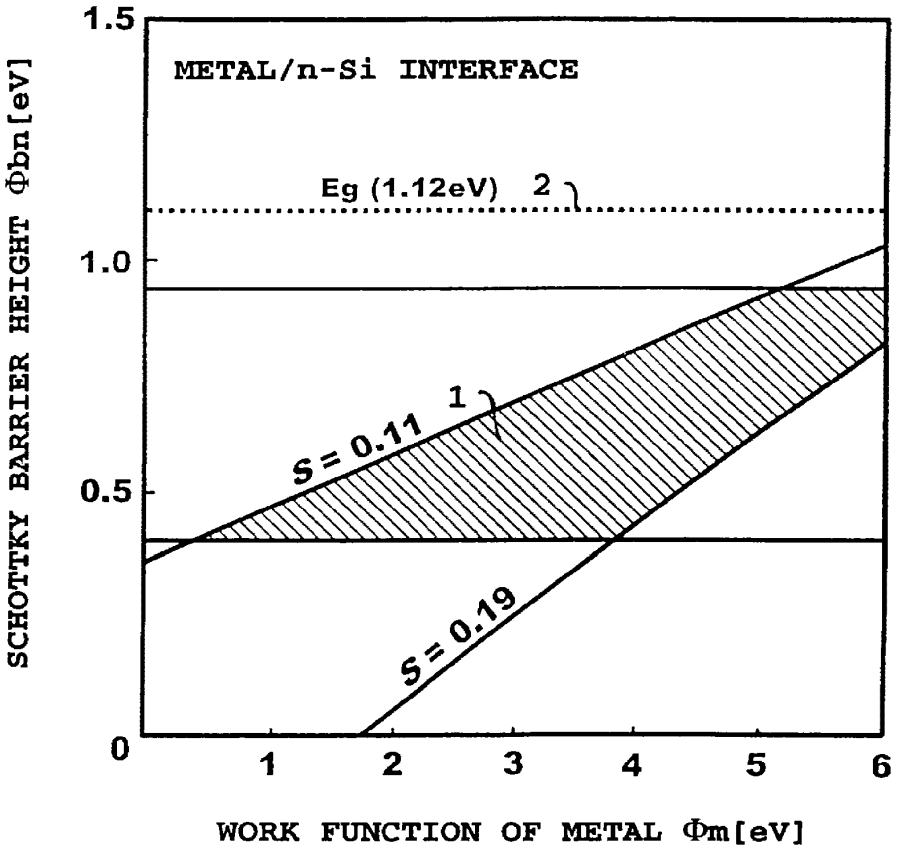


FIG. 1
(PRIOR ART)

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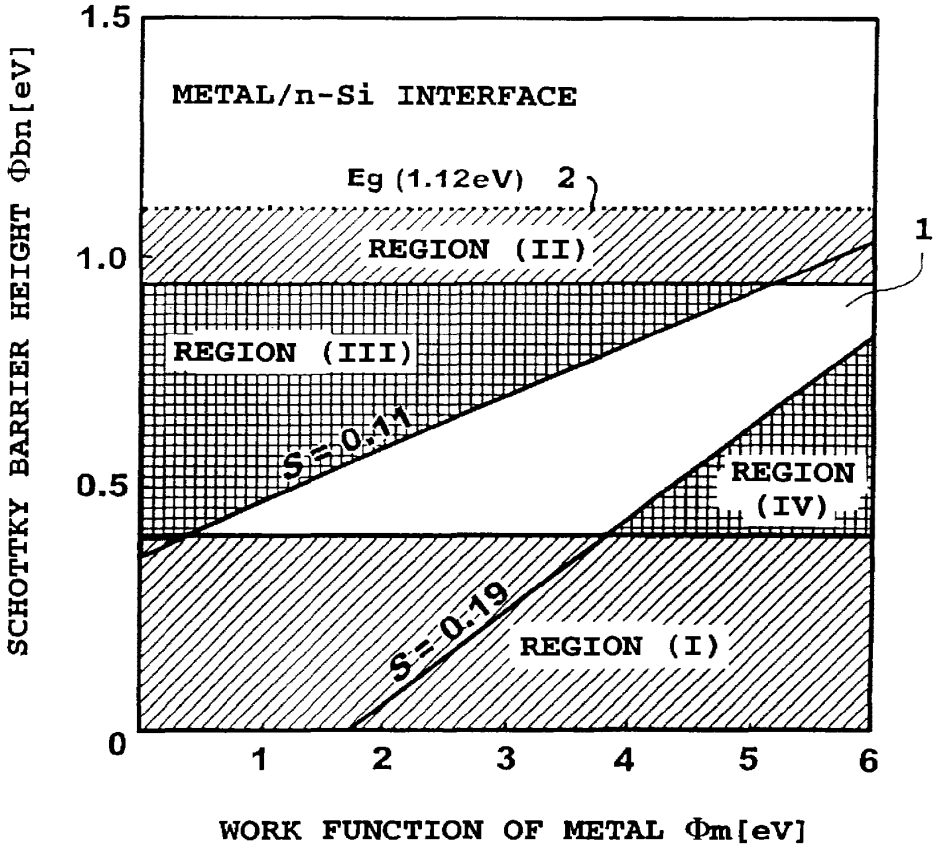


FIG.2

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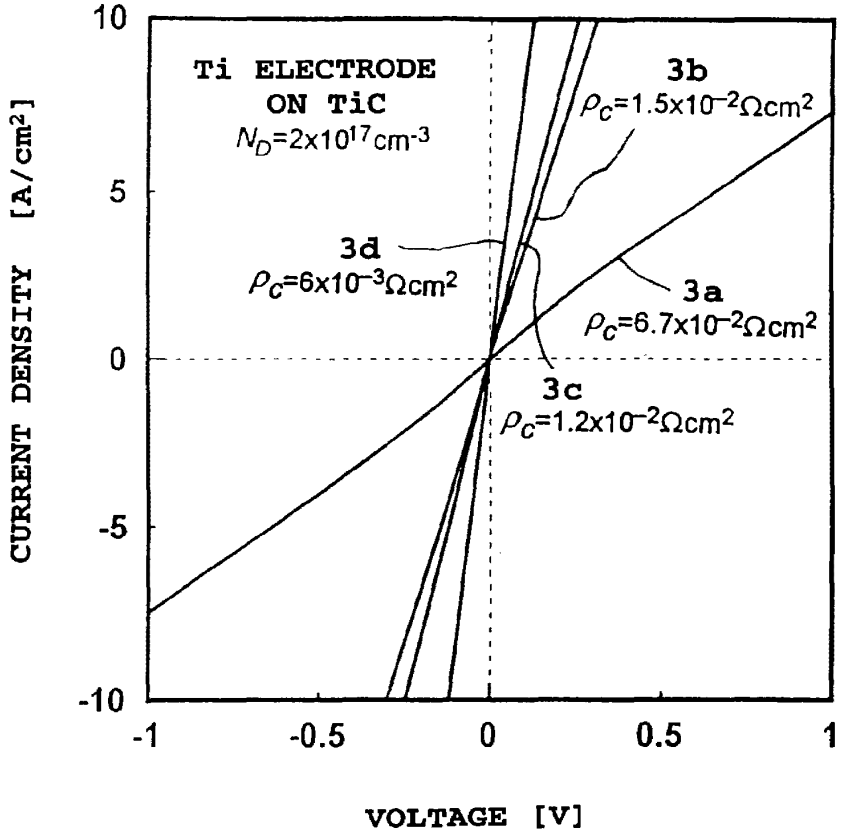


FIG.3

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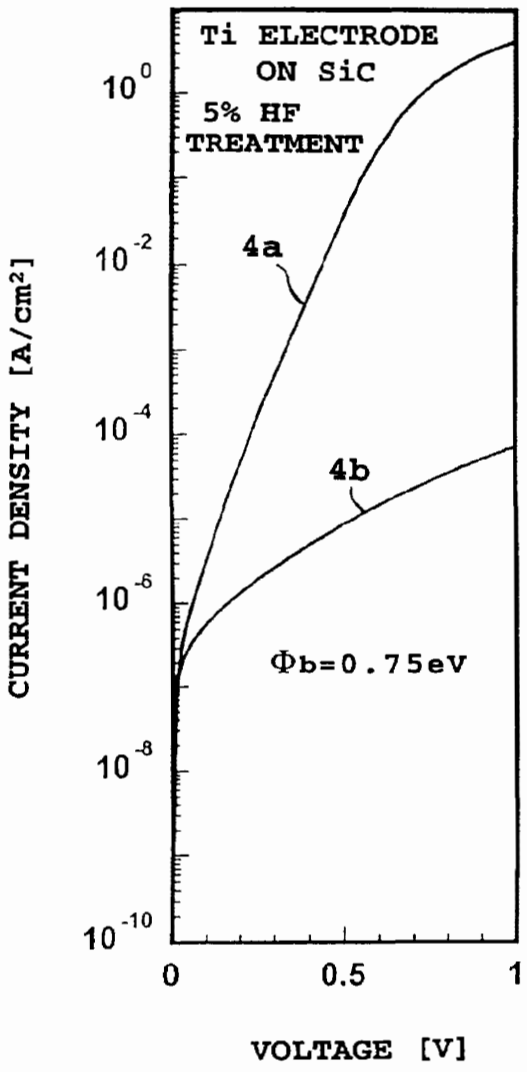


FIG.4

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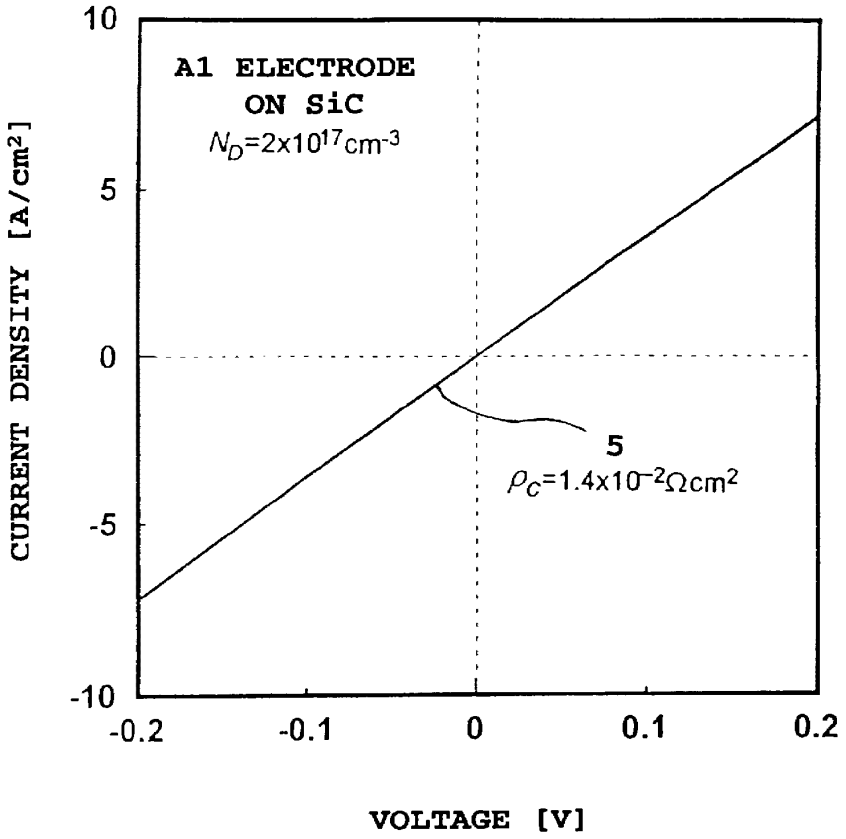


FIG.5

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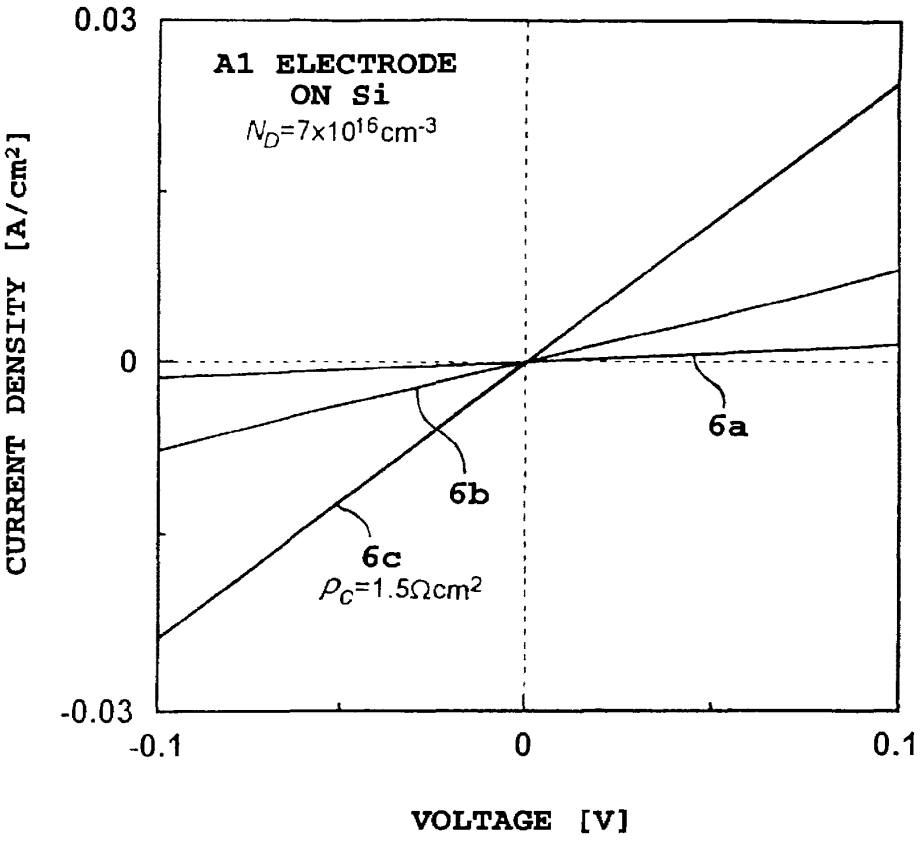


FIG. 6

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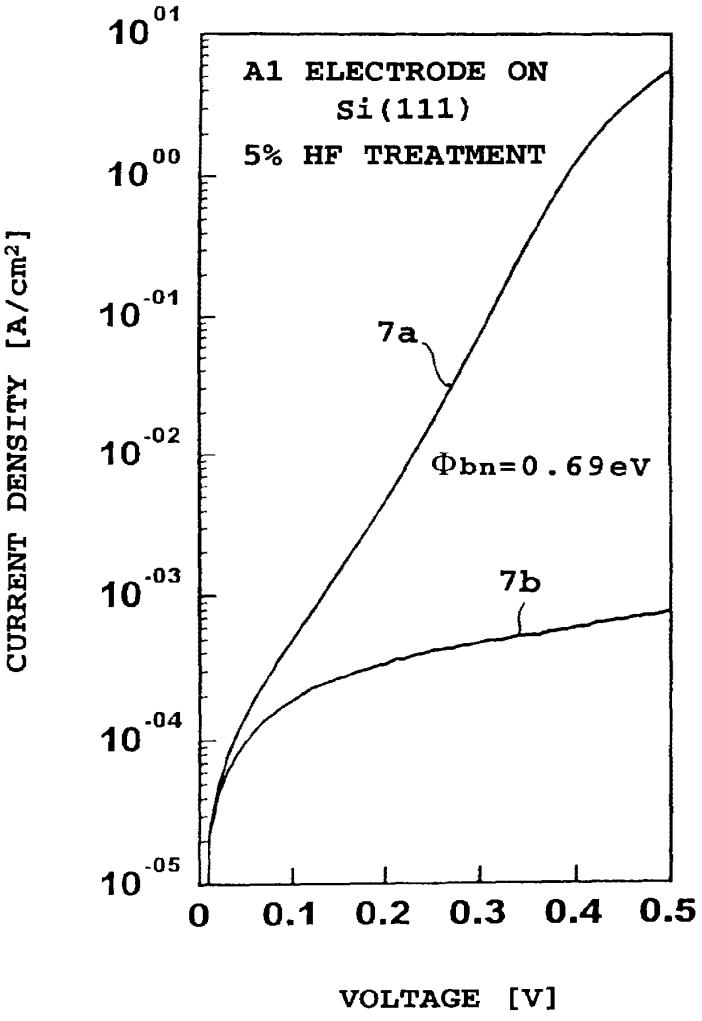


FIG.7

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FIG.8A

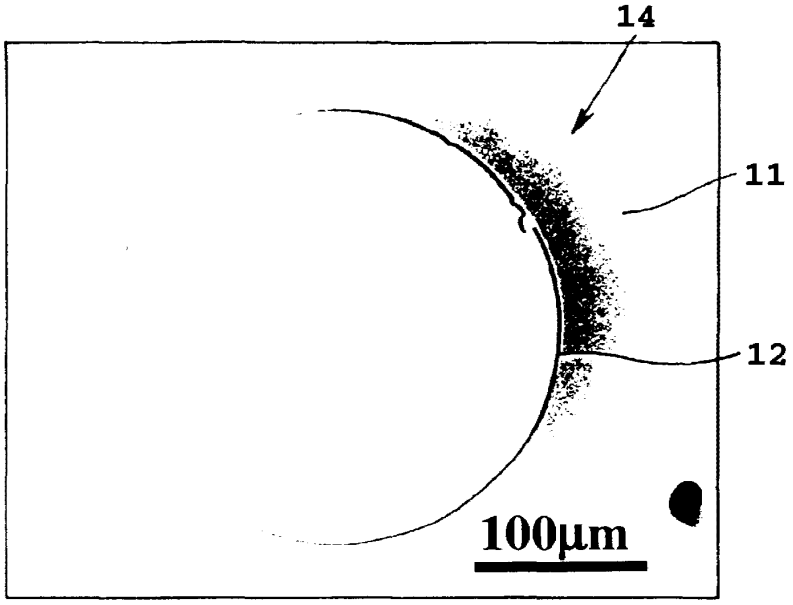
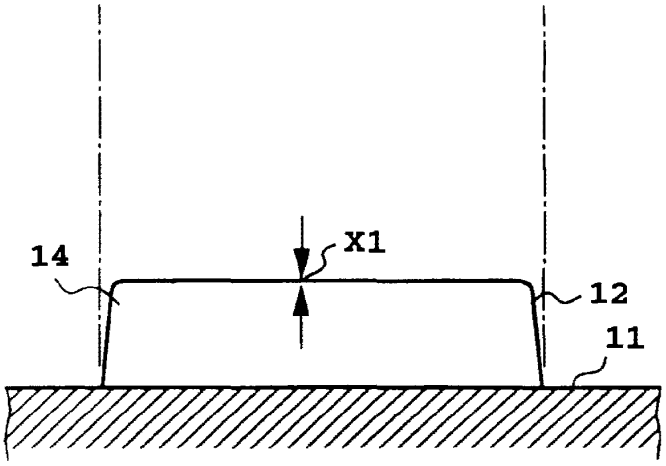


FIG.8B



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FIG.9A

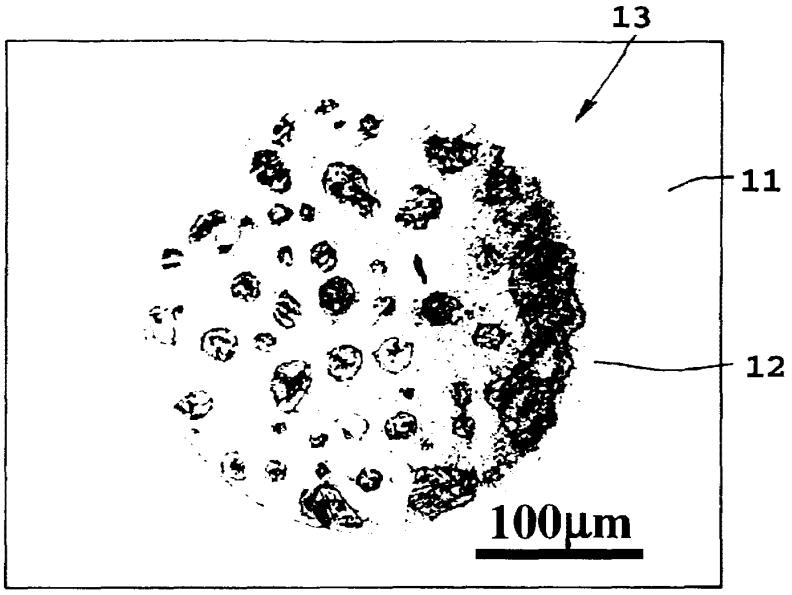
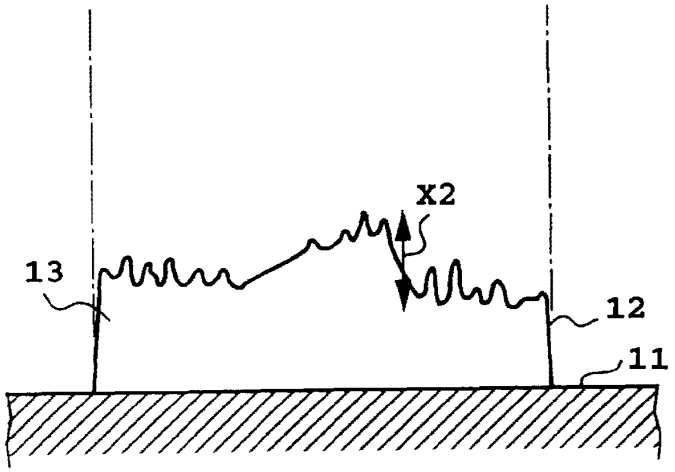


FIG.9B



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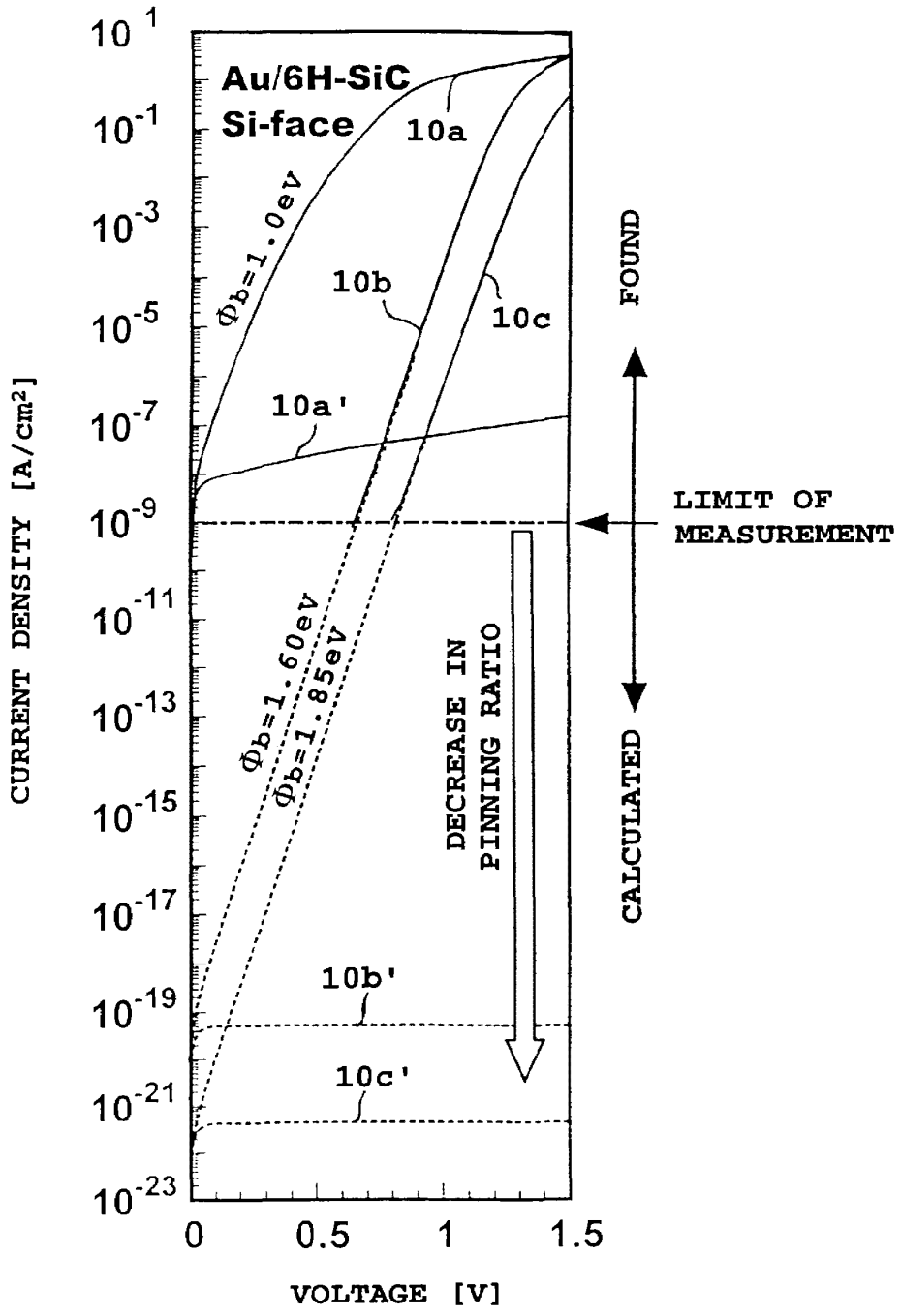


FIG.10

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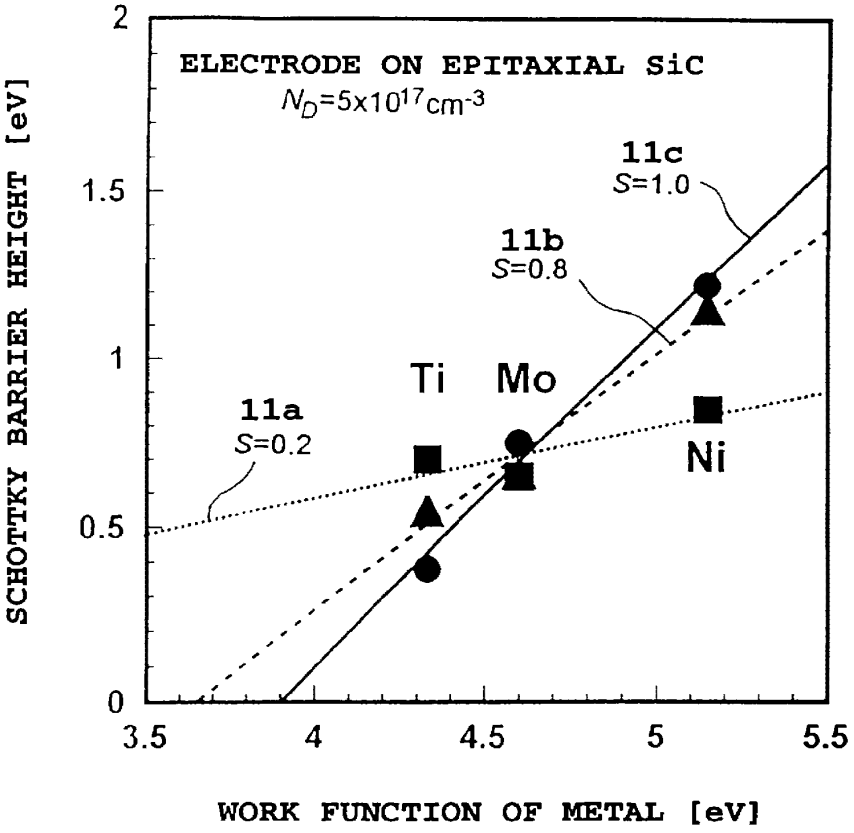


FIG.11

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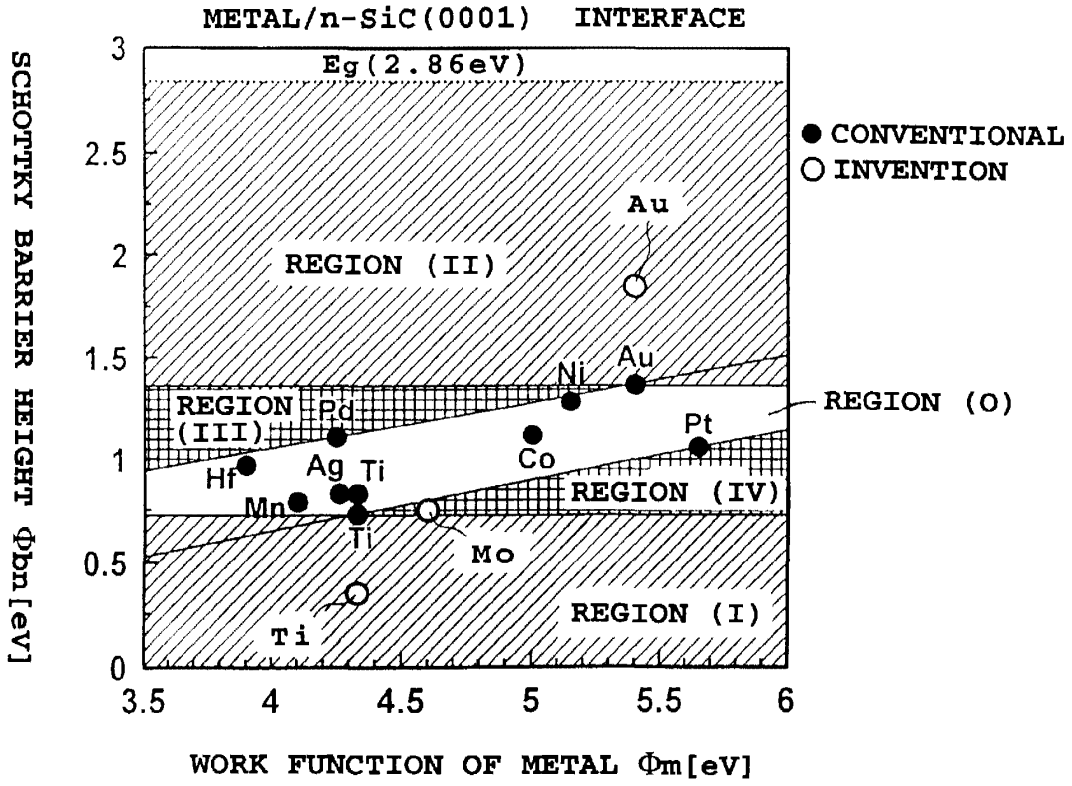


FIG.12

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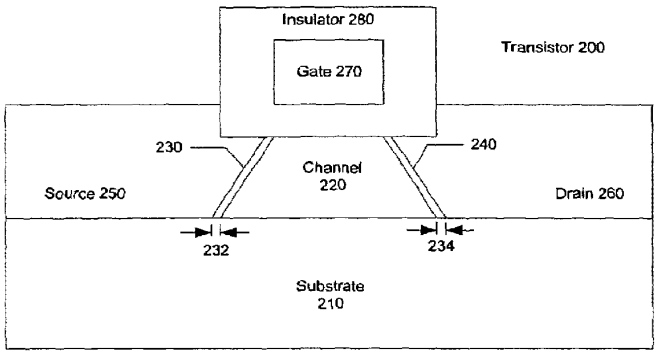
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(54) Title: INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL



(57) Abstract: A transistor includes a semiconductor channel (220) disposed nearby a gate (270) and in an electrical path between a source (250) and a drain (260), wherein the channel and at least one of the source or the drain are separated by an interface layer (230, 240) so as to form a channel - interface layer - source/drain junction in which a Fermi level of the semiconductor channel is depinned in a region near the junction and the junction has a specific contact resistance of less than approximately 1000 Ω-μm^2. The interface layer may include a passivating material such as a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of the semiconductor of the channel. In some cases, the interface layer consists essentially of a monolayer configured to depin the Fermi level of the semiconductor of the channel, or an amount of passivation material sufficient to terminate all or a sufficient number of dangling bonds of the semiconductor channel to achieve chemical stability of the surface. Also, the interface layer may include a separation layer of a material different than the passivating material. Where used, the separation layer has a thickness sufficient to reduce effects of metal-induced gap states in the semiconductor channel.

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INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL

RELATED APPLICATIONS

[0001] The present application is a continuation-in-part of co-pending U.S. Patent Application No.10/217,758, entitled "Method for Depinning the Fermi Level of a Semiconductor at an Electrical Junction and Devices Incorporating Such Junctions", by Daniel Grupp and Daniel J. Connelly, filed on August 12, 2002, and assigned to the same assignee as the present application. This patent application is hereby incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0002] The invention relates generally to solid-state switching and amplification devices. More particularly, the invention relates to a transistor having passivated metal-semiconductor junctions from the source to the channel and/or from the channel to the drain and at which the Fermi level of a semiconductor which comprises the channel is depinned.

BACKGROUND

[0003] One of the most basic electrical junctions used in modern devices is the metal-semiconductor junction. In these junctions, a metal (such as aluminum) is brought into contact with a semiconductor (such as silicon). This forms a device (a diode) which can be inherently rectifying; that is, the junction will tend to conduct current in one direction more favorably than in the other direction. In other cases, depending on the materials used, the junction may be ohmic in nature (i.e., the contact may have negligible resistance regardless of the direction of current flow). In addition to diodes, such metal – semiconductor junctions are also present at source/drain – channel interfaces within a class of transistors known as MOSFETs (metal oxide semiconductor field effect transistors).

[0004] As explained in the above-cited patent application, there exists at a metal-semiconductor contact a so-called Schottky barrier. The Schottky barrier at a conventional metal – semiconductor junction is characterized by Fermi level pinning of the semiconductor, due to both extrinsic and intrinsic surface states. The extrinsic states may arise from defects in the crystal structure of the interface. The intrinsic states arise from the quantum-mechanical penetration of the electrons in the metal into the bandgap of the semiconductor. These so-called metal-induced gap states (MIGS) appear to be of fundamental importance in explaining the physics of such

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junctions. See J. Tersoff, "Schottky Barrier Heights and the Continuum of Gap States," Phys. Rev. Lett. 52 (6), Feb. 6, 1984.

[0005] The Schottky barrier height at a metal–semiconductor interface determines the electrical properties of the junction. Thus, if it were possible to control or adjust the barrier height of a metal – semiconductor junction, electrical devices of desired characteristics could be produced. To tune the barrier height, the Fermi level of the semiconductor must be depinned. As discussed in detail in the above-cited patent application, the present inventors have achieved this goal in a device that still permits substantial current flow between the metal and the semiconductor. Below, the inventors present an application of this technology to MOSFET devices.

[0006] MOSFETs which incorporate Schottky junctions have a long—and largely unfruitful—history. In 1966, Lepselter and Kahng were investigating Schottky diodes. In that year they received U.S. Patent 3,290,127 directed to a device with a PtSi/Si interface. Use of the silicide was found to be an improvement over previous metal/Si contacts. The diodes were reproducible and stable, in part because the interface was sealed, as noted by the inventors at the time. The silicide also may reduce the extrinsic surface states (defects). The remaining pinning is most likely due to intrinsic surface states (MIGS), although this was not recognized at the time. Shortly thereafter, Lepselter and Sze incorporated the Schottky barrier into a MOSFET (see M. P. Lepselter and S. M. Sze, "SB-IGFET: An insulated-gate field-effect transistor using Schottky barrier contacts as source and drain", Proc. IEEE 56, 1088 (1968)). U.S. Patent 3,590,471 to Lepselter discussed the incorporation of the Schottky barriers, but the channel was still essentially isolated by implanted regions. The first patent for a channel isolated by Schottky barriers (U.S. Patent 3,708,360) was issued to Wakefield and Cunningham in 1973. This device also utilized silicided junctions.

[0007] In U.S. Patent 4,300,152, Lepselter described a Schottky barrier MOSFET. By eliminating the pn-junction in the source-substrate region, Lepselter showed that the parasitic pnpn structure responsible for latch-up could be eliminated. The proposed devices still utilized PtSi for the source and drain metal, however.

[0008] An extension of Lepselter's early work is found in U.S. Patent 4,485,550 to Koeneke et al. In these devices, an extra implant is added to extend beyond the source metal. This is similar to modern CMOS halo implants. The extra implant improves the drive current capabilities of the transistor by bringing the channel edge under the gate. The channel isolation in this device is from a pn-junction, not the PtSi source metal. An attempt to bring the source under the gate was

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investigated by recessing the source/drain contacts by etching (see C.J. Koeneke et al., "Schottky MOSFET for VLSI", IEDM, 367 (1981)). Sidewall spacers were still a limiting factor, however. This was improved by Snyder as described in US Patent 6,303,479, which also disclosed the ability to control vertical doping profiles without regard to horizontal profile control. The contacts were again made from PtSi.

[0009] U.S. Patent 6,096,590 to Chan et al. describes a device in which the PtSi/Si junctions are not recessed. This yields a poor sub-threshold slope from reduced coupling of the gate at the edge of the channel. Exponential turn-on, indicative of the Schottky barrier being too high, is seen in measurements presented in the patent. Further, the gate-source capacitance will be high.

[0010] Recently, MOSFET devices having metal – semiconductor junctions between a source/drain and a channel have been demonstrated with sub-50 nm channel-lengths, using $PtSi_2$ (see, e.g., C. Wang et al., "Sub-40 nm PtSi Schottky source/drain metal-oxide field-effect transistors", Appl. Phys. Lett. 74, 1174 (1999); and A. Itoh et al., "A 25-nm-long channel metal-gate p-type Schottky source/drain metal-oxide-semiconductor field-effect transistor on separation-by-implanted-oxygen substrate", J. Journal Appl. Phys. Part 1 39, 4757 (2000)), $ErSi_2$ (see, e.g., J. Kedzierski et al., "Complementary silicide source/drain thin-body MOSFETs for the 20 nm gate length regime", IEDM Tech. Dig., International Electron Devices Meeting 2000, San Francisco, CA, p. 00-57 (2000); and W. Saitoh et al., "Analysis of short-channel Schottky source/drain metal-oxide-semiconductor field-effect transistor on silicon-on-insulator substrate and demonstration of sub-50-nm n-type devices with metal gate", J. Journal Appl. Phys. Part 1 38, 6226 (1999)), and $CoSi_2$ (see, e.g., U. K. Matsuzawa et al., "Enhancement of hot-electron generation rate in Schottky source metal-oxide-semiconductor field-effect transistors", Appl. Phys. Lett. 76, 3992 (2000)) for the source/drain metal. Also, simulations have been performed all the way down to channel lengths of 10 nm (see, e.g., C. K. Huang et al., "Two-dimensional numerical simulation of Schottky barrier MOSFET with channel length to 10 nm", IEEE Trans. on Elect. Dev. 45, 842 (1998)), although a poor choice of device parameters limited the performance results, e.g., a large Φ_B. The performance of all of these devices is limited in part by the inability to control, and especially to lower, the height of the Shottkky barrier at the source and drain interfaces to the channel.

[0011] Only two disclosures of a non-silicide pure-metal/Si contact embodiment of a Schottky-barrier MOSFET have been found by the present inventors. Welch, U.S. Patent 5,663,584, seems to describe Schottky barrier MOSFET systems and fabrication thereof; however, a contact of

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"metal or metal silicide" is mentioned. This is inappropriate for fabrication of a device with a controlled barrier height. That is, there is no surface treatment or interface dielectric disclosed.

[0012] The disclosure by Hebiguchi in U.S. Patent 5,801,398 is perhaps more practical, and a method for manufacturing a thin-film transistor such as for use in displays is presented. In this device (which is a field effect transistor or FET), the source/drain contacts to the Si channel are metal (a list of possibilities is presented), but again, no surface preparation is mentioned.

[0013] **Figure 1** shows the FET 100 that was discussed by Hebiguchi. The transistor contains a glass substrate 110, a gate electrode 120, a gate insulating film 130, a drain electrode 140, a source electrode 150, and a semiconductor active film 160. During operation, voltage is applied to the source electrode 150 and to the gate electrode 120. The voltage applied to the gate electrode 120 changes the electrical properties of the semiconductor active film 160 allowing current to flow from the source electrode 150 to the drain electrode 140. In particular, the voltage applied to the gate electrode 120 creates a channel-generating region 170, in the semiconductor active film 160 a short distance from the gate insulating film 130, through which current may flow.

[0014] Hebiguchi describes the semiconductor active film 160 as being hydrogenated amorphous silicon, the drain and source electrodes 140 and 150 are formed of conductive materials (metals) such as chromium (Cr), aluminum (Al), tantalum (Ta), platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), or certain mixtures of these materials, and the junctions between the semiconductor active film 160 and the source and drain electrodes 150 and 140 are insulating Schottky barriers. The metal selected for an n-channel thin film transistor is chosen on the basis of having a workfunction that is smaller than that of silicon and the metal selected for a p-channel thin film transistor has a workfunction that is larger than that of silicon.

[0015] A significant limitation with the transistor discussed in Hebiguchi, is the generally poor control over the Schottky barrier height. As is well known, use of different metals with widely varying work functions tends to result in Schottky barriers which vary in height over a dramatically reduced range. Further, no special effort is made in Hebiguchi to control or reduce extrinsic surface states.

[0016] Another type of junction to the channel is introduced by Yoshimura in U.S. Patent 6,037,605,with the stated goal being to reduce short-channel effects. An oxide or nitride is disposed between Si source and drain contacts and a Si channel. The oxide is thicker farther away from the channel (down into the Si) to reduce currents not controlled by the gate. The

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thickness of the oxide is "sufficiently thin to permit charge tunneling", and is disclosed to be 0.5 to 2.0 nm. This differs from the present invention, which is described in detail below, in several ways, for example the use of Si as a source/drain, as opposed to a metal.

SUMMARY OF THE INVENTION

[0017] A transistor includes a semiconductor channel disposed nearby a gate (e.g., separated therefrom by a dielectric) and disposed in an electrical path between a source and a drain, wherein the channel and at least one of the source or the drain are separated by an interface layer so as to form a channel – interface layer – source/drain junction in which a Fermi level of the semiconductor channel is depinned in a region near the junction and the junction has a specific contact resistance of less than approximately 1000 Ω-μm^2. The interface layer may include a passivating material such as a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of the semiconductor of the channel. In some cases, the interface layer consists essentially of a monolayer configured to depin the Fermi level of the semiconductor of the channel, or an amount of passivation material sufficient to terminate all or a sufficient number of dangling bonds of the semiconductor channel to achieve chemical stability of the surface. Also, the interface layer may include a separation layer of a material different than the passivating material. Where used, the separation layer has a thickness sufficient to reduce the effects of intrinsic surface states in the semiconductor channel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The present invention is illustrated by way of example, and not limitation, in the figures of the accompanying drawings, in which like reference numerals refer to similar elements.

[0019] **Figure 1** shows a conventional FET having metal – semiconductor Schottky junctions between the source and the channel and the channel and the drain.

[0020] **Figure 2** shows a FET having passivated metal – semiconductor junctions from the source to the channel and from the channel to the drain, according to one embodiment of the present invention.

[0021] **Figure 3** shows a method for fabricating a transistor having passivated metal – semiconductor junctions from the source to the channel and from the channel to the drain, according to one embodiment of the present invention.

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[0022] **Figures 4A-4I** show intermediate substrates representing fabrication of a transistor having passivated aluminum-silicon junctions formed from an aluminum source to a silicon channel and from the silicon channel to an aluminum drain, according to one embodiment of the present invention.

[0023] **Figure 5A** illustrates portions of a conventional FinFET device.

[0024] **Figure 5B** illustrates portions of a FinFET device having interface layers between the source/drain and the channel in accordance with an embodiment of the present invention.

[0025] **Figure 6A** illustrates portions of a conventional vertical MOSFET device.

[0026] **Figure 6B** illustrates portions of a vertical MOSFET device having interface layers between the source/drain and the channel in accordance with an embodiment of the present invention.

[0027] **Figure 7A** illustrates portions of a conventional MESFET device.

[0028] **Figure 7B** illustrates portions of a MESFET device having an interface layer between the gate and the channel in accordance with an embodiment of the present invention.

[0029] **Figure 8** illustrates the operation of different n-type devices having tunnel barriers in accordance with an embodiment of the present invention under various gate voltage conditions.

DETAILED DESCRIPTION OF THE INVENTION

[0030] The above-cited co-pending patent application describes processes for depinning the Fermi level of a silicon-based or germanium semiconductor (e.g., Si, SiC, SiGe, SiGeC,or Ge) at a metal-semiconductor junction as well as devices that use such a junction. As more fully discussed in that application, an interface layer is introduced between the semiconductor and the metal. The interface layer functions to passivate the semiconductor surface (that is, terminate dangling bonds that may otherwise be present at the semiconductor surface so as to assure chemical stability of the surface) and to displace the semiconductor from the metal so as to reduce the effect of MIGS.

[0031] As discussed more fully below, the present inventors have determined that for thin interface layers disposed between a metal and a silicon-based or germanium semiconductor (e.g., Si, SiC, SiGe, SIGeC, or Ge), so as to form a metal – interface layer – semiconductor junction, there exist corresponding minimum specific contact resistances. Indeed, minimum specific

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contact resistances of less than or equal to approximately 1000 $\Omega-\mu m^2$ or less than or equal to approximately 100 $\Omega-\mu m^2$ or less than or equal to approximately 50 $\Omega-\mu m^2$ or less than or equal to approximately 10 $\Omega-\mu m^2$ or even less than or equal to approximately 1 $\Omega-\mu m^2$ may be achieved for such junctions in accordance with the present invention. To achieve such low contact resistances, a metal that has a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function that is near the valence band for p-type semiconductors, is selected.

[0032] The effect of (and reason for) using such metals may be understood with reference to **Figure 8**. Shown in the illustration is a 2x2 grid of band diagrams. The upper two diagrams illustrate the operation of an n-type device having tunnel barriers (in the form of an interface layer configured in accordance with the present invention) and a metal source/drain in which the workfunction is aligned to the semiconductor channel conduction band under different gate voltages. Notice that the device is OFF (i.e., not conducting current) when the gate-to-source voltage (V_{GS}) is 0. The device is ON (i.e., conducting current) when $V_{GS} > 0$. The lower two diagrams illustrate the operation of the n-type device having a metal source/drain in which the workfunction is aligned to the semiconductor channel mid-gap. Notice that even in the ON state ON (i.e., $V_{GS} > 0$) a barrier to current flow exists due to band bending. This results in a higher contact resistance.

[0033] The interface layers described in the above-cited patent application may be used in connection with a semiconductor surface of a channel in a FET, as discussed below. That is, an interface layer may be disposed between a source and a channel, a channel and a drain, or both of an insulated gate field effect transistor. Such use of an interface layer is described in detail herein. The present invention provides a source – channel and/or channel – drain contact wherein the Fermi level of the source and/or drain metal is aligned (or approximately aligned) with the conduction or valence band of the semiconductor, depending on the type of semiconductor material and metals used.

[0034] In addition, the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility). The high doping profiles were required in the past in order to keep the junction depletion layer relatively thin, so as to increase the tunneling current, thus reducing the junction resistance. However, it is becoming increasingly difficult to increase doping profiles in order to provide low resistance junctions. It may be possible to reach the same level of resistance with a lower doping concentration using the present invention. It may further be possible to achieve much lower resistance even with lower

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doping concentration. When the present invention is used with high doping levels, the resistance will be further reduced.

[0035] To aid in the understanding of the present invention, the following description provides specific details of presently preferred embodiments of the invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without some of these specific details, for example by substituting well-known equivalent materials in place of those described herein for semiconductors, passivation layers and/or conductors. Where the discussion refers to well-known structures and devices, block diagrams are used, in part to demonstrate the broad applicability of the present invention to a wide range of such structures and devices.

[0036] The present inventors have devised a scheme to passivate a semiconductor surface such as a channel surface within a Schottky barrier transistor. The scheme involves forming a passivation layer which is a nitride, hydride, oxide, arsenide and/or fluoride of the semiconductor that makes up the channel. In some cases (e.g., when the passivating layer is a hydride or fluoride of the semiconductor of the channel), it may be necessary to include a separation layer between the semiconductor and the metal source/drain to reduce or eliminate the effect of intrinsic surface states in the semiconductor channel. The term interface layer will be used in connection with the present invention to include passivation layers alone and passivation layers in combination with separation layers, where such separation layers are appropriate.

[0037] The interface layer chemically neutralizes and physically protects the semiconductor channel surface. The interface layer also allows for a tunable Schottky barrier, having a height that depends on bulk characteristics of the channel semiconductor and the source/drain metal, rather than on surface properties. This allows greater control over the barrier height to meet the operational characteristics that are desired for the transistor. This scheme differs from past attempts by others to insulate channel surfaces and provide adjustable Schottky barriers in that the passivation materials used for the interface layer are not limited to metals that readily form silicides with the semiconductor channel. In other words, the present invention decouples the need for semiconductor passivation from other considerations used to select the source/drain metal, such as the desirability of a particular workfunction. It further provides for greater control of the Schottky-barrier height than previously possible.

I. An Exemplary Transistor

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[0038] **Figure 2** shows a transistor 200 formed on a substrate 210 (e.g., a semiconductor substrate such as Si or a compound substrate such as SOI) and configured in accordance with an embodiment of the present invention. The transistor 200 contains a channel 220 that is separated from a source 250 and a drain 260 by interface layers 230 and 240, respectively, each of which form passivated Schottky barriers. The particular transistor 200 shown, which is one example of a switching device, is an Insulated Gate FET. The interface layers 230 and 240 passivate the surfaces of channel 220 in the regions of the source/drain – channel junctions by chemically stabilizing the channel surface. The interface layers 230 and 240 also reduce or eliminate the effect of MIGS in the region of the source/drain – channel junctions by displacing the source/drain (250/260) away from the channel 220. The result of introducing the interface layers 230 and 240 between the semiconductor channel 220 and the metal source/drain 250/260 is a depinning of the Fermi level of the semiconductor that makes up channel 220. When the Fermi level of the semiconductor is depinned, the height of the Schottky barrier will depend only on the difference of the bulk workfunctions of the metal and the semiconductor in contact at the junction, and will not be dependent upon the interface. The reduction in the effectiveness of the MIGS to pin the Fermi level depends on the choice of interface dielectric. There will be MIGS at the interface between the metal and the dielectric. In general, dielectrics have much weaker MIGS than semiconductors, primarily due to larger bandgaps. Thus the choice of dielectric is important in determining the final electrical characteristics of the Schottky barrier junction.

[0039] The transistor 200 also includes a gate 270 surrounded by an insulator 280. The terms gate, source and drain each refer to terminals of a three terminal Insulated Gate FET. The source 250 and drain 260 are the terminals between which conduction occurs under the influence of an electric field resulting from a voltage applied to the gate 270. The source 250 and the drain 260 are provided at opposite ends of the channel 220 so that the channel 220 is disposed between the source 250 and the drain 260. Often, though it is not a requirement of the present invention, the source 250 and drain 260 are fabricated such that they are geometrically symmetrical. Symmetrical source and drain terminals may be referred to as source/drain terminals. A particular terminal may be designated a source or a drain on the basis of the voltage to be applied to that terminal when the FET is operated in an electrical circuit. In the particular transistor 200 shown, the source 250 is provided at a left-hand side of the channel 220 and the drain 260 is provided at a right-hand side of the channel 220, although another embodiment is contemplated wherein the source 250 and the drain 260 are interchanged.

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[0040] The source 250 and the drain 250 may each contain a conductor, preferably a metal. Examples of metals that may be used include pure metals, alloys, refractory metals, metals that do not form silicides, and metals having a predetermined work function. The gate 270, which may also preferably contain a conductor, such as a metal, is located above the channel 220 and is capacitively coupled to the channel 220 through the insulator 280. Note, in other embodiments the transistor's three terminals may be co-planar or the gate 270 may be disposed below the level of the source 250 and/or the drain 260 in the substrate 210.

[0041] The insulator 280 (which may be made of a dielectric such as an oxide of the metal gate or an oxide of a semiconductor) surrounds the gate 270 and separates the gate 270 from the source 250, the drain 260, the channel 220, and the interface layers 230 and 240. The insulator 280 is of a sufficient thickness to provide a high resistance between the gate 270 and the channel 220 such that essentially no current flows between the gate 270 and the channel 220. For example, the resistance may be between about 10^8 Ohms and about 10^{12} Ohms, or greater. Such a resistance may allow the gate 270 and the channel 220 to be capacitively coupled, while preventing current from flowing between the gate 270 and the channel 220.

[0042] The insulator 280 may also or alternatively contain a high-k dielectric material that has a higher dielectric constant than that of silicon dioxide (i.e., higher than about 4.0). The high-k material may allow the same charge induced in the channel 220 under the gate 270 to be achieved at the same gate voltage in a thicker layer. That is, the higher dielectric constant may allow the insulator 280 to have a greater layer thickness than a corresponding layer of silicon dioxide that provides the same amount of insulation. The increased thickness may simplify fabrication of the transistor 200. The thicker layer may also have less leakage current than a thinner SiO_2 layer. Exemplary high-k dielectric materials that are contemplated include materials having a dielectric constant greater than about 4 (e.g., zinc oxide, ZnO), greater than about 10 (e.g., aluminum oxide, Al_2O_3), greater than about 20 (e.g., zirconium oxide, ZrO_2), and greater than about 40 (e.g., hafnium oxide, HfO).

[0043] As discussed above, the channel 220 contains a semiconductor material. The term semiconductor is used to refer to a material having a bandgap that is greater than about 0.1 electron volts and less than about 4 electron volts. Exemplary semiconductors that are contemplated include Si, Ge, SiGe or SiC. The semiconductor material may have a wide range of doping levels including no doping at all. The interface layers 230 and 240 each contain a passivation material that provides passivation to the channel 220 by covalently bonding with a dangling bond of a surface semiconductor atom to fully coordinate the semiconductor atom and

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thereby help passivate the semiconductor atom. The passivation material is preferably selected from the group consisting of a hydride, a nitride, an arsenide, an oxide and a fluoride of the semiconductor channel 220. Depending on the passivation material selected (e.g., where H, As or F are used as passivation materials), a separation layer in addition to a passivation layer within the interface layers 230 and 240 may be needed. Of course, the combination of the passivation layer and the separation layer must be sufficiently thin to permit the low specific contact resistances described in the above-cited patent application. Further details regarding the formation of an interface layer may be found in the above-cited patent application and will not be repeated herein.

II. Fabricating a Transistor Having Passivated Schottky Barriers to the Channel

[0044] **Figure 3** shows a method 300 for fabricating a transistor having passivated metal – semiconductor junctions from the source to the channel and from the channel to the drain, according to one embodiment of the present invention. The method starts at block 301 and then proceeds to block 310 where a substrate is provided. At block 320 an insulated gate structure is formed on the substrate. The insulated gate structure may contain a gate having a conductive material (e.g., a metal) and a gate insulator having an insulating material beneath the conductive material. Then at block 330 a channel is formed under the insulated gate. The channel may include undercut void regions subjacent the gate dielectric and extending into the channel on both ends of the insulated gate structure. The method advances to block 340 where an interface layer is formed on the channel sides. Forming the interface layer may include creating a passivating layer and (where necessary) a separation layer using one or more of the materials discussed above. The method then advances to block 350 where a source and drain are formed on opposite sides of the channel, including on the interface layer, and within any undercut regions. Depending upon the interface layer thickness and robustness, the source and drain may be formed by substantially non-invasive approaches. The method terminates at block 360.

[0045] An alternative procedure does not use the undercut described above. Instead, there is an "underlap". That is, in the alternative process the width of the gate is intentionally made less than the width of the channel so that the gate underlaps the channel.

III. Exemplary Process For Fabricating a Transistor

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[0046] **Figures 4A-I** show intermediate substrates, representing fabrication of the transistor shown in Figure 4I, according to one embodiment of the present invention. The particular transistor shown in Figure 4I contains passivated aluminum-silicon junctions 482I and 484I formed from the aluminum source 492I to the silicon channel 430I and from the silicon channel 430I to the aluminum drain 494I. However, this is merely one example of a transistor configured in accordance with the present invention. For example, planar devices, wherein the gate, source and drain are co-planar in or above the substrate are also within the scope of the present invention, as are embodiments where the gate is disposed in a plane below the source and/or drain. Likewise, embodiments wherein the width of the gate is less than the width of the channel are included within the present invention.

[0047] **Figures 4A-I** therefore show one embodiment of fabricating a transistor, according to the method 300. **Figures 4A-4C** show providing a substrate and forming an insulated gate on the substrate. **Figures 4D-4E** show forming a channel beneath the insulated gate, such that the channel and the insulated gate define a first and a second undercut void region that extend underneath the insulated gate toward the channel from a first and a second side of the insulated gate. **Figure 4G** shows forming an interface layer on exposed sidewall surfaces of the channel. Finally, **Figures 4F, 4G, and 4H** show forming a source and a drain terminal on a first and a second side of the channel including on the interface layers, and forming extension tips within the undercut voids beneath the insulated gate.

[0048] **Figure 4A** shows a first intermediate substrate 400A containing a silicon substrate 410A, a layer of buried oxide of silicon 420A, a layer of silicon on insulator 430A, a layer of an oxide of silicon 440A, and an aluminum gate 450A. The layers 410A-430A represent a conventional Silicon On Insulator (SOI) substrate. The SOI substrate includes the buried layer 440A to help isolate proximate semiconductor devices formed in the layer of silicon on insulator. This isolation may help reduce short-channel effects, as compared to semiconductor devices formed in a bulk wafer. The buried oxide layer may have a thickness that is effective to isolate the silicon on insulator, preferably greater than about 10 nm. The layer of silicon on insulator may have a thickness of about 20 nm, or slightly less.

[0049] As will be understood by a person having an ordinary level of skill in the art and the benefit of the present disclosure, the SOI substrate is not a limitation of the present invention. Other substrates are contemplated to replace the SOI substrate. For example, the SOI substrate may be replaced by a Silicon-On-Sapphire substrate, although this may increase the cost of fabrication, or the SOI substrate may be replaced by a plain silicon wafer, although this may

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provide inferior electrical isolation of semiconductor devices and poor short-channel characteristics.

[0050] The layer of oxide of silicon 440A, in one embodiment silicon dioxide (SiO_2), may be formed by wet or dry oxidation of the silicon on insulator, as is common in the semiconductor processing arts. The layer may be sufficiently thin to serve as a gate oxide and have a thickness between about 1 nm and about 10 nm.

[0051] The aluminum gate 450A is formed on the oxide 440A. The aluminum gate has a width 451A that is about equal to, or slightly larger than the intended channel length, which in one embodiment is less than about 50 nm and in another embodiment is less than about 20 nm. More than slight increases of the width over the channel length may increase the extent and angle of a subsequent undercut etch, which may complicate fabrication. The gate450A may be formed by depositing a layer of aluminum on the oxide 440A, depositing a photoresist layer on the deposited aluminum layer, exposing a pattern including the width 451A in the photoresist using conventional high-resolution lithography, removing a portion of the photoresist according to the exposed pattern, wet or dry etching a portion of the deposited layer of aluminum according to the patterned photoresist, and removing the remaining photoresist.

[0052] **Figure 4B** shows a second intermediate substrate 400B containing an oxide of aluminum insulator 460B formed on exposed portions, including the top and sides, of the aluminum gate 450B. The oxide of aluminum layer 460B may have a thickness between about 1 nm and about 20 nm. The thickness may be about equivalent to the thickness of the layer 440B, or slightly larger. Larger thickness may improve performance by reducing capacitance between the gate and the source, however the additional thickness may also increase fabrication complexity by increasing undercut. Forming the oxide of aluminum layer 460B may include oxidizing the aluminum gate 450A in an oxygen plasma etcher that provides a suitable oxidizing atmosphere, or by other methods known in the semiconductor processing arts.

[0053] **Figure 4C** shows a third intermediate substrate 400C containing a gate oxide 440C formed by removing a portion of the layer 440B that is not beneath aluminum gate 450B or aluminum oxide 460B. The removal may include using the oxidized aluminum gate 450B-460B as a mask for the layer 440B and etching portions of the layer 440B that are not subjacent to and concealed by the oxidized aluminum gate 450B-460B. This removal leaves a portion of the silicon on insulator layer 430C that is not subjacent to the gate oxide 440C, aluminum gate 450C, or oxide 460C exposed. Etching may include Reactive Ion Etching (RIE) to encourage etching

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preferentially in the direction normal or perpendicular to the surface of the layer 440B. RIE is a dry-etch process wherein the intermediate substrate 400B is placed on a radio frequency powered electrode and provided with a potential that helps ionize and accelerate ion bombardment of etching species extracted from plasma toward the etched surface.

[0054] Figure 4D shows a fourth intermediate substrate 400D containing a silicon channel 430D formed by removing a portion of the silicon on insulator layer 430C that is substantially not subjacent and concealed by the gate oxide 440C. Removal may include etching silicon on insulator that has a standard Si-100 orientation with tetramethylammonium hydroxide (TMAH) to form angled sidewalls that slope inward toward the gate 450D, as shown. Alternatively, comparatively straight sidewalls aligned with the gate oxide 440D may be formed by a self-limiting etch in TMAH if the silicon on insulator has a Si-110 orientation. Such comparatively straight sidewalls may also be formed by RIE.

[0055] Figure 4E shows a fifth intermediate substrate 400E containing an undercut silicon channel 430E formed by removing a portion of the channel 430D that is subjacent and aligned with the gate oxide 440D. The undercut silicon channel 430E contains an undercut region wherein the silicon is removed from the channel 430D at a left and right-hand edge of the gate oxide 440D to allow a subsequent formation of source and drain material vertically under the gate oxide 440E. Removal may be by a non-directional or isotropic wet silicon etch with TMAH wherein etching takes place in substantial uniform amounts along the sidewall. If the crystal axis of the silicon on insulator are not aligned precisely with the lithography, the TMAH etch may not be completely self-limiting and may form an undercut due to the vertical ridges or stair steps of crystal structure. Alternatively, removal may be by an isotropic RIE.

[0056] Figure 4F shows a sixth intermediate substrate 400F containing a seed layer 476F, 472F, and 474F formed respectively on a top surface of the insulated gate and on a left and right-hand side of the insulated gate. The seed layer facilitates subsequent formation of a metal source and drain. The seed layer may be deposited anisotropically so that no significant seed layer material is deposited on the vertical sidewalls of the aluminum oxide 460F, gate oxide 440F, or channel 430F and essentially no metal is deposited on the underside of the undercut overhang of the gate oxide 440F. This is desired to electrically isolate the seed layer portion 476F from the seed layer portion 472F and 474F. In one embodiment, the seed layer contains chromium deposited from a thermal source. Chromium provides desirable electrochemistry and is well suited for formation of ultra-thin films.

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[0057] Figure 4G shows a seventh intermediate substrate 400G containing a modified seed layer 472G-474G formed by selectively removing the layer portion 476F from the top surface of the insulated gate. Removal of the portion 476F is desirable to allow depositing the source and drain materials superjacent the layer portions 472G and 476G without depositing the source and drain materials atop the oxidized aluminum gate structure. Since the seed layer portion 476F is electrically isolated from the seed layer portions 472F and 476F, the portion 476F may be removed electrochemically by a Cerric Ammonium Nitrate (CAN) chrome etch. For example, the seed layer portions 472F and 474F but not the seed layer portion 476F may be electrically coupled with a copper electrical probe at the edge of the substrate to etch the seed layer portion 476F but not the portions 472F-474F. It should be noted however, that another embodiment is contemplated wherein patterning may be used to form chromium layers 472F and 474F without forming chromium layer 476F. This may avoid a subsequent removal of the chromium layer 476F.

[0058] Figure 4H shows an eighth intermediate substrate 400H containing interface layers 482H and 484H formed on the sidewall surfaces of the channel 430H. The interface layers may be a monolayer, slightly more than a monolayer, less than about 0.3 nm, less than about 0.5 nm or less than about 1 nm (depending upon the desired Schottky barrier characteristics). That is, in some cases an amount of passivation material sufficient to terminate all or a sufficient number of dangling bonds of the semiconductor channel to achieve chemical stability of the surface may be used. The interface layers may be grown in accordance with the techniques discussed in the above-cited patent application. Passivation materials that are contemplated include arsenic, hydrogen, fluorine, oxygen, and nitrogen, as discussed above, and the interface layers 482H and 484H may be made up of both a passivation layer and a separation layer.

[0059] Figure 4I shows a ninth intermediate substrate 400I containing a source 492I formed superjacent upon the seed material 472H and beneath the left undercut overhang and a drain 494I formed superjacent upon the seed material 474H and beneath the right undercut overhang. The source and drain have a thickness that extends above the gate insulator 440I. Desirably, the thickness may be precisely controlled. Forming may include plating the potentially different source/drain materials on the seed layers 472H and 474H. This may include depositing a photoresist, irradiating the photoresist to expose a channel width pattern, removing a portion of the photoresist to expose the seed layers 472H and 474H, plating the source/drain materials on the seed layers 472H and 474H, and removing the remainder of the photoresist. According to

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one embodiment, the source and drain materials are aluminum. Alternatively, the source and drain materials may be another desired and potentially different metal or alloy.

[0060] The transistor shown in **Figure 4I** has a number of advantages. In general, the transistor provides a simple construction. This may allow extending transistor fabrication below 50 nm channel lengths, below 20 nm channel lengths, or even below 10 nm channel lengths. Another advantage is greater control over the Schottky barrier height provided by the interface layers. The barrier height may be controlled by the properties of the interface layer such as passivation material, layer thickness, and layer formation conditions, in addition to difference in workfunctions between the source/drain and the channel. This ability to control the barrier height is further increased by greater flexibility in selecting source/drain materials, since, due to the interface layers, the source/drain materials do not have to readily form silicides with the silicon channel. Yet another advantage is low resistance in the source due to the use of a high conductivity metal rather than doped silicon. Removal of dopants in the junctions in general may be attractive from an Ultra-Large-Scale-Integration (ULSI) manufacturing perspective, since application of such dopants is posing a limit to process controllability.

[0061] The channel – interface layer – source/drain junction(s) of the transistor shown in **Figure 4I** are unique in that the Fermi level of the semiconductor channel is depinned in a region near the junction and the junction has a specific contact resistance of less than approximately 1000 Ω-μm^2. This is true of all transistors configured in accordance with the present invention. Indeed, minimum specific contact resistances of less than or equal to approximately 10 $\Omega - \mu m^2$ or even less than or equal to approximately 1 $\Omega - \mu m^2$ may be achieved for such junctions in accordance with the present invention. To achieve such low contact resistances, a source/drain metal that has a work function near the conduction band of the semiconductor for n-type semiconductors, or a work function that is near the valence band for p-type semiconductors, is selected. The depinning role played by the interface layer in tuning, adjusting, or controlling the height of the barrier between the source/drain and the semiconductor channel involves both a reduction in surface states of the channel, by bonding to the semiconductor material to consume dangling bonds, a reduction in the formation of MIGS in the semiconductor channel, by providing a thickness and bandgap that prevent the electron wave function (of the source/drain metal) from penetrating into the semiconductor channel. The electron wave function may instead penetrate into the interface layer and form MIGS within the interface layer at an energy related to the states of the interface layer material. As desired, the density of the MIGS and the depth of MIGS penetration into the interface layer may be reduced by choosing an interface layer material

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or materials having a larger bandgap or higher effective mass than the semiconductor of the channel. The interface layer is operable to pass current to/from the semiconductor channel during device operation.

[0062] In some embodiments, it may be desirable to use an interface layer having a thickness of a monolayer, or, for example between about 0.1 nm and about 0.3 nm, and also having a wide bandgap (as compared to that of the semiconductor of the channel) so that the interface layer both depins the Fermi level (so that the barrier height depends predominantly on bulk properties of the junction materials) and allows sufficient current transfer across it. In some cases the interface layer may include only an amount of passivation material sufficient to terminate all or a sufficient number of dangling bonds of the semiconductor channel to achieve chemical stability of the surface. Advantageously, such interface layers may be sufficiently thin to provide low impedance to current flow (due to the exponential dependence of direct tunneling on barrier thickness), which is desirable for many semiconductor devices, while also providing sufficient semiconductor surface passivation to allow an adjustable barrier height. That is, the interface layer may allow passivation of surface states and reduction (or elimination) of MIGS in the semiconductor to allow for an adjustable barrier height with a substantially thin layer that allows sufficient current to be transferred across the interface layer.

[0063] As explained in the above-cited patent application, there are several methods by which the barrier height can be made adjustable. For example, adjustment may be made by tuning the degree of Fermi level pinning. In other words, some embodiments may allow for a sufficiently thin interface layer so that not all of the effects of MIGS in the semiconductor channel are eliminated. Further, the pinning may be varied by combinations of thickness of the interface layer and the choice of interface material. The metal in contact with the interface layer may be pinned by MIGS at different levels in different materials. Conversely, or in addition, the semiconductor channel passivation may be left incomplete to allow for an effective level of unpassivated states. Complete depinning of the Fermi level (that is removal of all surface states in the semiconductor channel including MIGS) is another option, in which case one could tune the barrier height simply by choosing a pure metal or an alloy that possesses the desired workfunction.

[0064] In summary then, one embodiment for fabricating a transistor on a semiconductor substrate includes: (1) forming a semiconductor oxide dielectric layer on a semiconductor substrate by oxidizing the semiconductor substrate; (2) forming a metal gate on the semiconductor oxide layer by depositing a layer of metal on the semiconductor oxide and

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removing a portion of the deposited layer of metal based on a lithographic exposure; (3) forming a metal oxide dielectric layer on exposed portions of the metal gate by oxidizing the metal gate; (4) forming a gate oxide dielectric by removing a portion of the semiconductor oxide layer that is protected by the metal oxide formed on the metal gate; (5) forming a semiconductor channel structure by removing a portion of the semiconductor substrate that is not protected by the metal oxide formed on the metal gate; (6) forming an undercut semiconductor channel containing a source undercut region for a source tip and a drain undercut region for a drain tip by removing a source tip portion of the semiconductor channel structure that is subjacent to a left-hand end of the gate oxide and extends underneath the gate oxide toward the channel top interior and removing a drain tip portion of the semiconductor channel structure that is subjacent to a right-hand end of the gate oxide and extends underneath the gate oxide toward the channel top interior; (7) forming a source seed layer on a left-hand side of the undercut semiconductor channel and forming a drain seed layer on a right-hand side of the undercut semiconductor channel by anisotropically depositing seed layer material so that seed layer material is not deposited on exposed sidewall surfaces of the undercut semiconductor channel and removing a portion of deposited seed layer material that is above the undercut semiconductor channel; (8) forming an interface layer on the exposed sidewall surfaces of the undercut semiconductor channel by covalently bonding at least a monolayer (or less) of passivation material to semiconductor atoms of the exposed sidewall surfaces of the undercut semiconductor channel; and (9) forming a source on a first side of the channel including on the passivation layer and within a first undercut corresponding to the removal of the first portion of the semiconductor channel structure and forming a drain on a second side of the channel including on the interface layer and within a second undercut corresponding to the removal of the second portion of the semiconductor channel structure.

IV. Alternative Arrangements

[0065] The transistor illustrated in Figure 4I is but one example of the types of FETs that can benefit from the present invention. Other FETs known in the art may also realize such benefits by incorporating the present interface layers into source/drain – channel junctions. For example, so-called FinFETs may incorporate such interface layers. A FinFET is an example of a thin-body SOI device and is the name given to a class of FETs developed by researchers at the University of California, Berkely. Conventional FinFETs are described in detail in Yang-Kyu Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era", IEEE Electron Device

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Letters, vol. 25, no. 1 (Jan. 2002), incorporated herein by reference, and an example of such a device 500 is illustrated in **Figure 5A**. As shown, the channel of a finFET is formed by spacer-defined semiconductor fins.

[0066] **Figure 5B** shows a Fin-FET 520 modified to incorporate interface layers 522 in accordance with an embodiment of the present invention. In this embodiment, the semiconductor source and/or drain are replaced with a metal source and/or drain. The semiconductor fins (i.e., the channel) contact these source/drain regions through an interface layer.

[0067] Another transistor where the present invention may find application is the so-called vertical MOSFET, e.g., as described in E. Josse et al., "High performance 40 nm vertical MOSFET within a conventional CMOS process flow", 2001 Symposium on VLSI Technology Digest of Technical Papers. Paper No. 5B-2, pages 55 – 56 (2001), incorporated herein by reference. Vertical MOSFETs are characterized by a pillar-like channel sandwiched between a double gate. The source and drain are located at the ends of the channel pillar. An example of such a structure 600 is shown in **Figure 6A**.

[0068] **Figure 6B** shows a vertical MOSFET 620 modified to incorporate interface layers in accordance with an embodiment of the present invention. This transistor is similar to the MOSFET illustrated in Figure 6A but the upper Si n-region (the drain in this example) has been replace with a metal drain and contact to the channel is through an interface layer 622. Thus, such devices may be asymmetric, having a passivated Si/metal tunnel junction at the top contact, and a Si p-n junction at the bottom of the device on the substrate side. Complementary devices may be fabricated on the same substrate by first implanting p and n regions for the bottom contacts, and then employing two different metals, each with work functions chosen to yield p-type or n-type devices, as the top contacts to the channel.

[0069] **Figure 7A** illustrates yet another type of transistor 700, the MESFET. A MESFET (Metal Semiconductor FET) replaces the gate/insulator/semiconductor stack adjacent to the channel with a metal/semiconductor contact, intentionally forming a Schottky barrier. The conductance of the channel is modulated when an applied gate voltage results in a change in the depletion width of the Schottky barrier into the channel. The channel as shown may be a thin Si layer, as in an SOI substrate.

[0070] For optimizing the utility of a particular MESFET application, it may be desirable to either raise or lower the Schottky barrier. This may be achieved as shown in **Figure 7B** by implementation of the present invention in a transistor 720 wherein a particular interface

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dielectric and contact metal may be appropriately chosen. The interface dielectric forms an interface layer 722 between the gate and the channel. In other embodiments, the gate may be poly Si instead of a metal.

V. Use of Transistor In Electrical Systems

[0071] Transistors such as those described herein may be used in chips, integrated circuits, monolithic devices, semiconductor devices, microelectronic devices, and the like within a number of electrical systems. Electrical systems that are contemplated include computer systems (e.g., portable, laptop, desktop, server, mainframe, etc.), hard copy equipment (e.g., printer, plotter, fax machine, etc.), and other electrical systems. For example, in one embodiment a computer system may comprise a microprocessor having such a transistor to help execute instructions. The computer system may contain other conventional components including but not limited to a bus or other communication means to communicate information, a memory to store information (e.g., a dynamic memory such as RAM or a static memory such as ROM), a display device, a data input device, and a communication device such as a modem, as will be appreciated by a person having an ordinary level of skill in the art and the benefit of the present disclosure. Any or all of these devices may include transistors configured in accordance with the present invention.

[0072] Thus, a transistor having passivated junctions from the source to the channel and/or from the channel to the drain, and a method for forming such a transistor have been described. Although described with reference to specific embodiments it should be remembered that various modifications and changes may be made to the techniques described herein without departing from the broader spirit and scope of the invention. For example, metals other than aluminum may be used in transistors configured in accordance with the present invention. Low work function metals that may be so used include Er, Eu, Ba, Cs, Ca, Ce, Rb, Sm, Y, and Yb. All have workfunctions less than 3 eV. High work function metals (for aligning to valence bands) which may be used include Pt, Ir, Pd, Re, Ni, Co, and Au. The specification and drawings are accordingly to be regarded in an illustrative rather than a restrictive sense and the invention measured only in terms of the claims, which follow.

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CLAIMS

What is claimed is:

1. A transistor, comprising a semiconductor channel disposed (i) nearby a gate configured to control conductance within the channel and (ii) in an electrical path between a source and a drain, at least one of which is made of a metal, wherein the channel and whichever of the source and/or the drain is/are made of the metal is/are separated by an interface layer so as to form a channel – interface layer – source/drain junction in which a Fermi level of the semiconductor channel is depinned in a region near the junction and the junction has a specific contact resistance of less than approximately 1000 Ω-μm^2.

2. The transistor of claim 1 wherein the semiconductor channel is made of one of Si, Ge, SiGe, SiGeC, or SiC.

3. The transistor of claim 1 wherein the metal comprises one of a pure metal, an alloy, or a refractory metal.

4. The transistor of claim 1 wherein the metal comprises aluminum.

5. The transistor of claim 1 wherein the specific contact resistance is less than or equal to approximately 100 $\Omega - \mu m^2$.

6. The transistor of claim 1 wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

7. The transistor of claim 1 wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

8. The transistor of claim 1 wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

9. The transistor of claim 1 wherein the interface layer includes a passivating material.

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10. The transistor of claim 9 wherein the passivating material comprises one or more of a nitride of the semiconductor of the channel, a fluoride of the semiconductor of the channel, an oxide of the semiconductor of the channel, an oxynitride of the semiconductor of the channel, a hydride of the semiconductor of the channel and/or an arsenide of the semiconductor of the channel.

11. The transistor of claim 10 wherein the interface layer consists essentially of an amount of passivating material sufficient to terminate enough dangling bonds of a surface of the semiconductor channel so as to achieve chemical stability of the surface.

12. The transistor of claim 10 wherein the interface layer consists essentially of a monolayer configured to depin the Fermi level of the semiconductor of the channel.

13. The transistor of claim 12 wherein the interface layer has a thickness sufficient to reduce effects of metal-induced gap states in the semiconductor channel.

14. The transistor of claim 9 wherein the interface layer further includes a separation layer.

15. The transistor of claim 14 wherein the separation layer has a thickness sufficient to reduce effects of metal-induced gap states in the semiconductor channel.

16. The transistor of claim 1 wherein the semiconductor channel is separated from the gate by a dielectric.

17. A method , comprising:

forming, on one or more surfaces of a semiconductor channel of a transistor, an interface layer; and

forming, on one or more surfaces of the interface layer opposite the semiconductor channel, a source or drain terminal for the transistor so as to create a channel – interface layer – source/drain junction in which a Fermi level of the semiconductor channel is depinned in a region near the junction and the junction has a specific contact resistance of less than approximately 1000 Ω-μm^2.

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18. The method of claim 17 wherein the semiconductor channel is formed by removing a portion of a semiconductor substrate that is not protected by a mask created at least in part by a gate structure formed above the semiconductor channel.

19. The method of claim 17 wherein the specific contact resistance is less than or equal to approximately 100 $\Omega - \mu m^2$.

20. The method of claim 17 wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

21. The method of claim 17 wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

22. The method of claim 17 wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

23. The method of claim 17 wherein the semiconductor channel is made of one of Si, Ge, SiGe, SiGeC, or SiC.

24. The method of claim 23 wherein the gate is formed on a oxide layer disposed over the semiconductor channel.

25. The method of claim 24 wherein the oxide layer comprises a dielectric layer sufficiently thick enough to provide only capacitive coupling between the gate and the semiconductor channel.

26. The method of claim 24 wherein the oxide layer is formed over the semiconductor substrate by oxidizing the substrate.

27. The method of claim 26 wherein the gate is formed on the oxide layer by depositing a layer of metal on the oxide layer and removing a portion of the deposited layer of metal based on a lithographic exposure.

28. The method of claim 25 wherein the source or drain terminal is formed from a seed layer created by anisotropically depositing seed layer material on the semiconductor substrate.

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29. The method of claim 27 wherein the interface layer is formed by covalently bonding at least a monolayer of a passivation material to the semiconductor channel.

30. The method of claim 29 wherein the passivation material comprises one or more of a nitride of the semiconductor channel, a fluoride of the semiconductor channel, an oxide of the semiconductor channel, an oxynitride of the semiconductor channel, a hydride of the semiconductor channel and/or an arsenide of the semiconductor channel.

31. The method of claim 29 wherein the interface layer includes a separation layer comprising a material different than the passivation material.

32. The method of claim 31 wherein the material that makes up the separation layer comprises an oxide of the semiconductor channel.

33. The method of claim 17 wherein the interface layer comprises an amount of a passivation material sufficient to terminate all or a sufficient number of dangling bonds of the one or more surfaces of the semiconductor channel to achieve chemical stability of the one or more surfaces.

34. An electrical system comprising a circuit coupled to a transistor having a semiconductor channel disposed nearby a gate and in an electrical path between a source and a drain, at least one of which is made of a metal, wherein the channel and whichever of the source and/or the drain is/are made of the metal is/are separated by an interface layer so as to form a channel – interface layer – source/drain junction in which a Fermi level of the semiconductor channel is depinned in a region near the junction and the junction has a specific contact resistance of less than approximately 1000 Ω-μm^2.

35. The electrical system of claim 34 wherein the semiconductor channel is separated from the gate by a dielectric.

36. The electrical system of claim 35 wherein the specific contact resistance is less than or equal to approximately 100 $\Omega - \mu m^2$.

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37. The electrical system of claim 35 wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

38. The electrical system of claim 35 wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

39. The electrical system of claim 35 wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

40. The electrical system of claim 35 wherein the semiconductor channel is made of one of Si,Ge, SiGe, SiGeC, or SiC.

41. The electrical system of claim 35 wherein the interface layer includes a passivating material.

42. The electrical system of claim 41 wherein the interface layer includes a separation layer comprising a material different than the passivation material.

43. The electrical system of claim 41 wherein the interface layer has a thickness sufficient to reduce effects of metal-induced gap states in the semiconductor channel.

44. The electrical system of claim 41 wherein the interface layer comprises an amount of passivating material sufficient to terminate all or a sufficient number of dangling bonds of the semiconductor channel to achieve chemical stability of a surface of the semiconductor channel in the region near the junction.

45. The electrical system of claim 44 wherein amount of passivating material comprises a monolayer.

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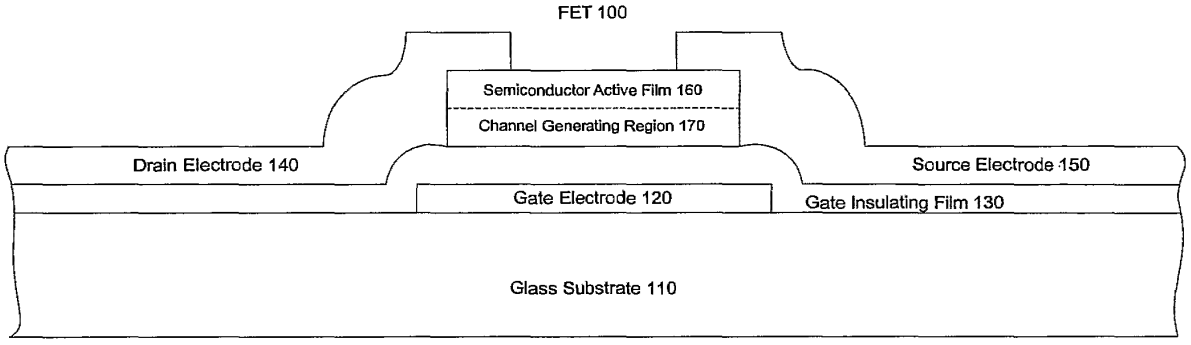


Fig. 1
(Prior Art)

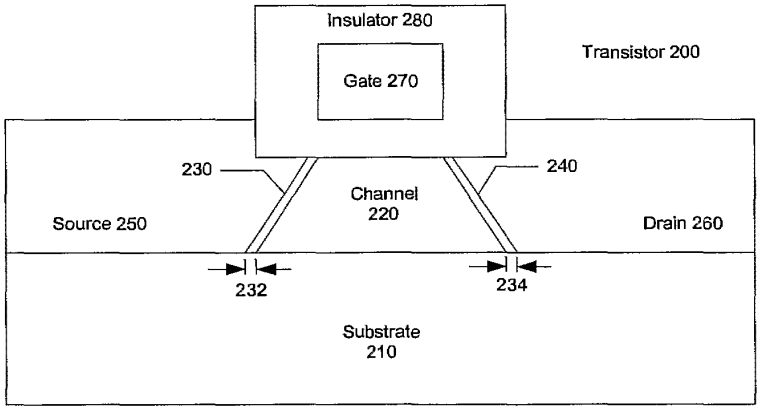


Fig. 2

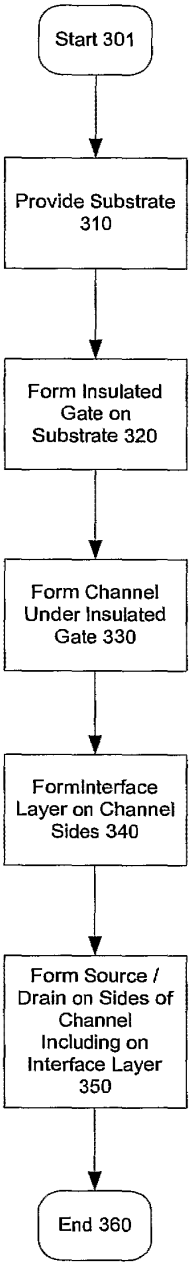

Start 301
300
Provide Substrate 310
Form Insulated Gate on Substrate 320
Form Channel Under Insulated Gate 330
FormInterface Layer on Channel Sides 340
Form Source / Drain on Sides of Channel Including on Interface Layer 350
End 360

Fig. 3

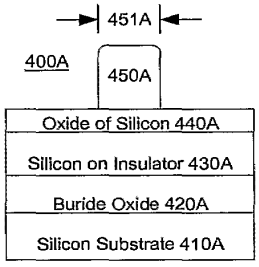


Fig. 4A

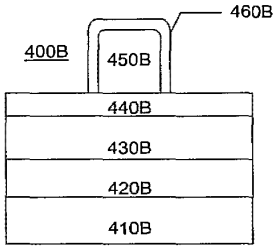


Fig. 4B

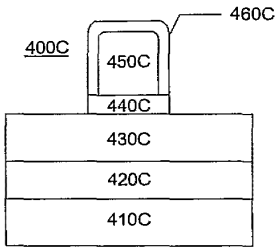


Fig. 4C

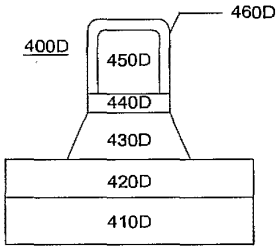


Fig. 4D

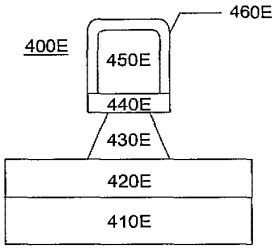


Fig. 4E

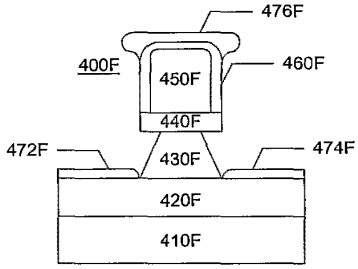


Fig. 4F

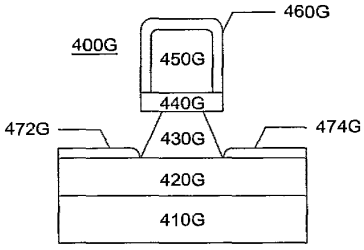


Fig. 4G

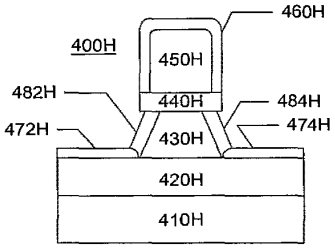


Fig. 4H

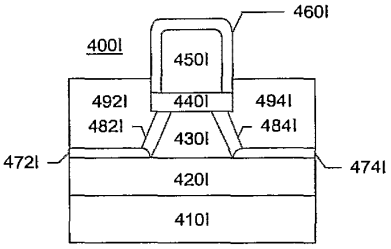


Fig. 4I

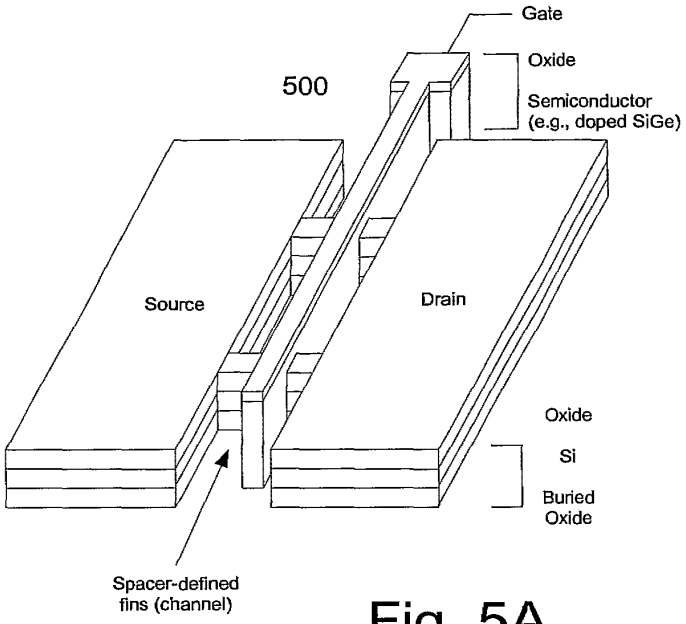

Gate
Oxide
500
Semiconductor
(e.g., doped SiGe)
Source
Drain
Oxide
Si
Buried
Oxide
Spacer-defined
fins (channel)

Fig. 5A

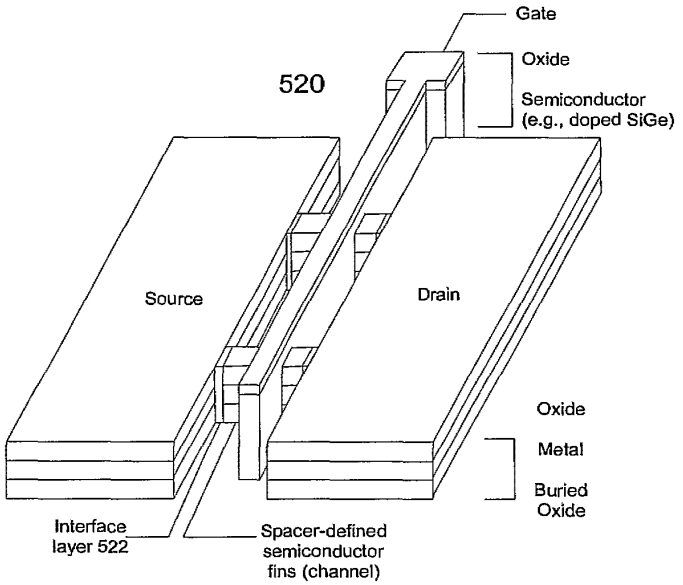

Gate
Oxide
520
Semiconductor
(e.g., doped SiGe)
Source
Drain
Oxide
Metal
Buried
Oxide
Interface
layer 522
Spacer-defined
semiconductor
fins (channel)

Fig. 5B

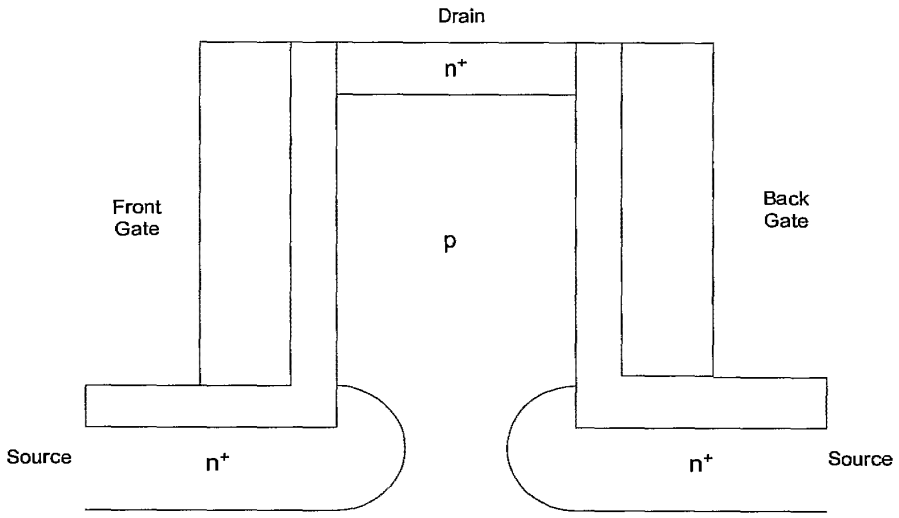

Drain
n+
Front Gate
p
Back Gate
Source
n+
n+
Source
600

Fig. 6A

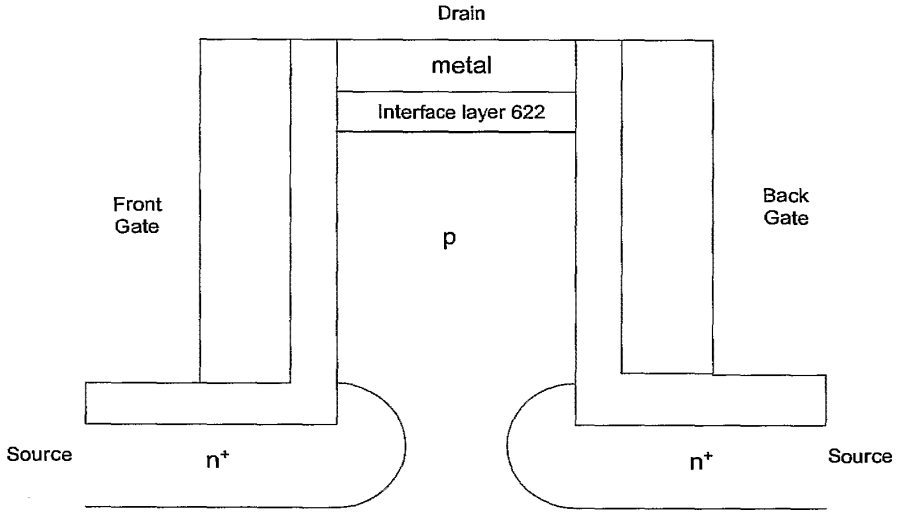

Drain
metal
Interface layer 622
Front Gate
p
Back Gate
Source
n+
n+
Source
620

Fig. 6B

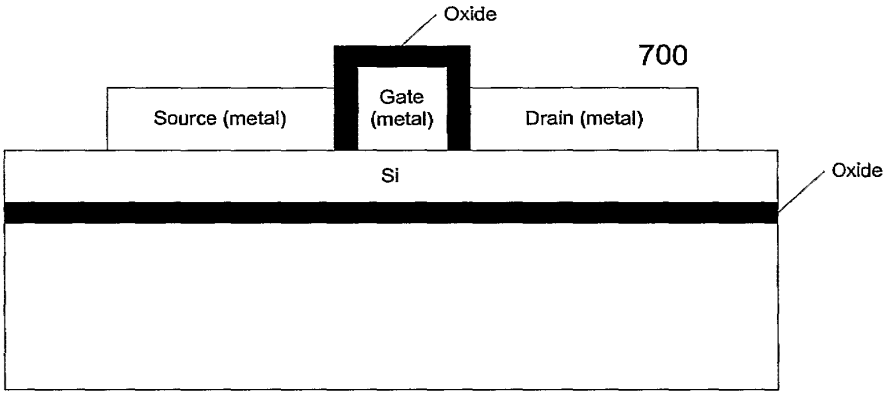

Oxide
700
Source (metal)
Gate
(metal)
Drain (metal)
Si
Oxide

Fig. 7A

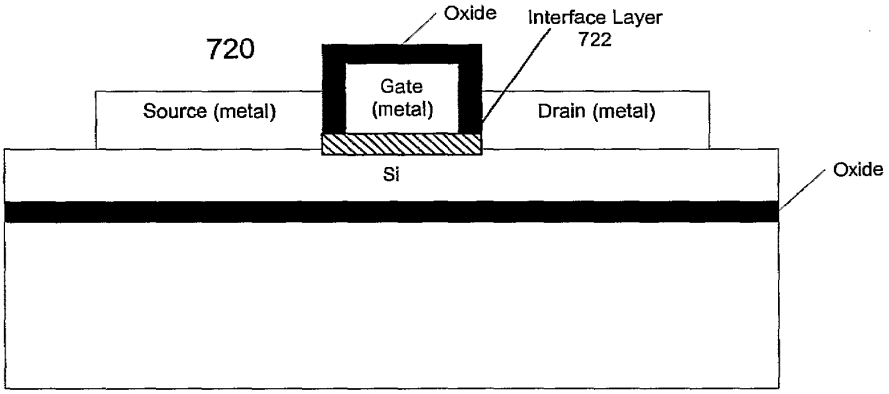

Oxide
Interface Layer
722
720
Source (metal)
Gate
(metal)
Drain (metal)
Si
Oxide

Fig. 7B

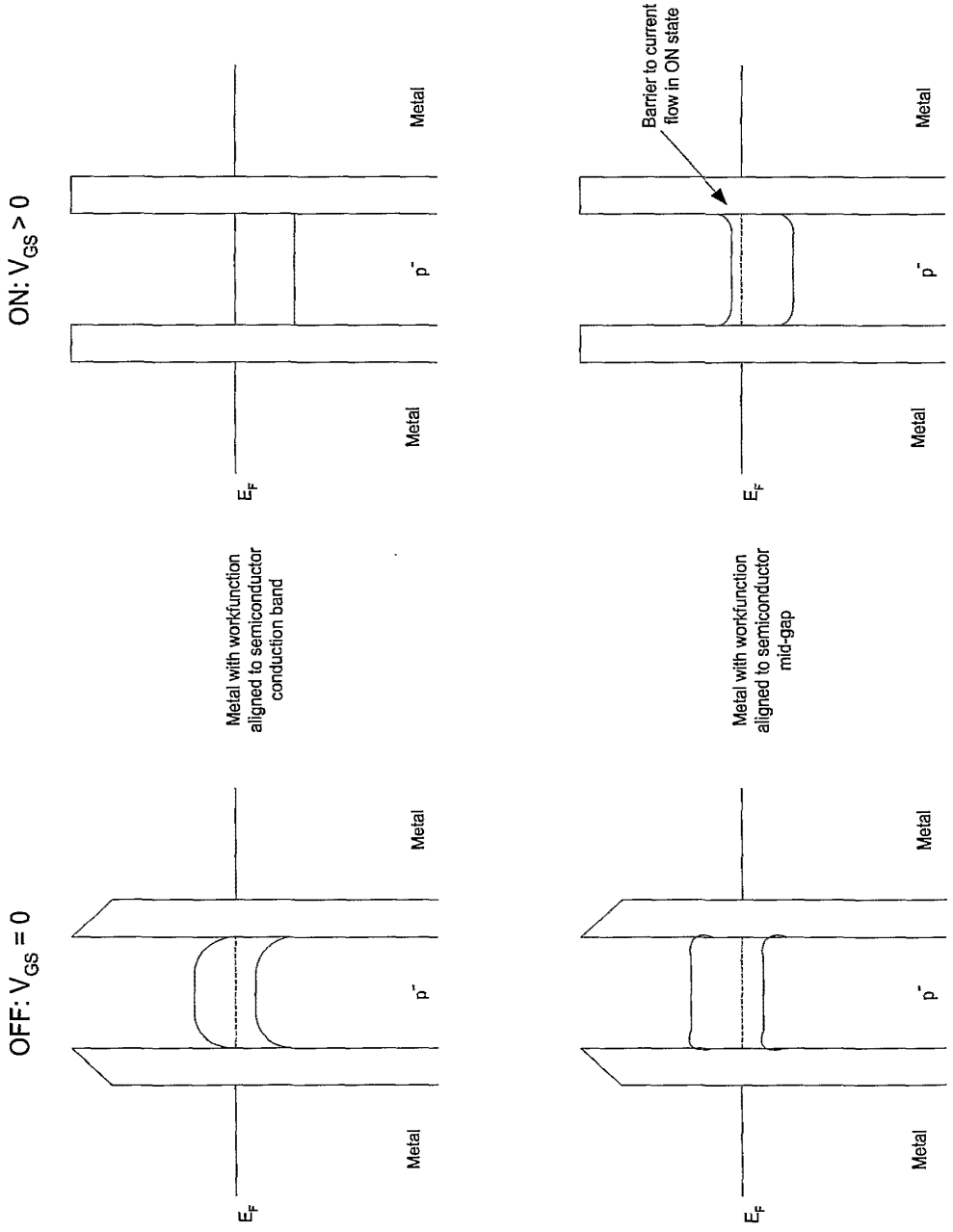


Fig. 8

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/25057

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/78 H01L21/336 H01L29/49 H01L29/45 H01L29/51

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, COMPENDEX, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 3 983 264 A (PADOVANI FRANCOIS A ET AL) 28 September 1976 (1976-09-28) column 2, line 49 -column 6, line 29; figure 2	1-45
X	US 5 021 365 A (WARREN ALAN C ET AL) 4 June 1991 (1991-06-04) column 5, line 64 -column 6, line 49; figures 2,4,9	1-45
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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/25057

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US 03/25057

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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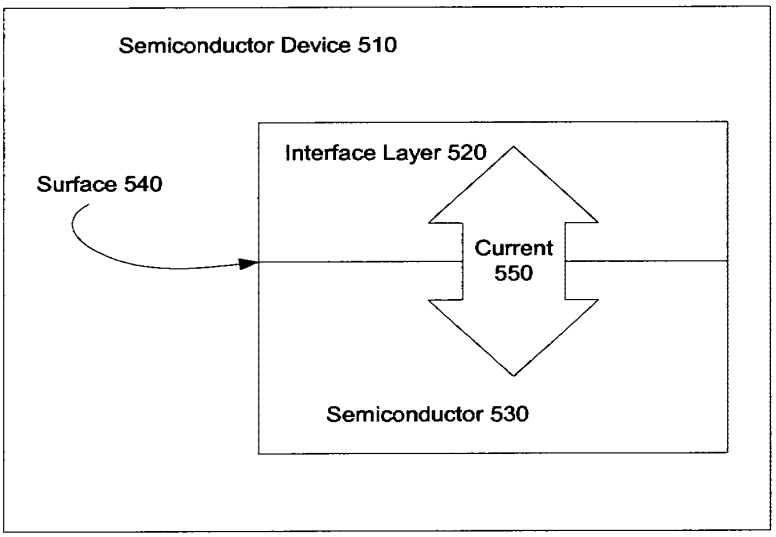
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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS



(57) Abstract: An electrical device in which an interface layer (520) is disposed between and in contact with a metal and a Si-based semiconductor, the interface layer being of a thickness effective to depin of the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor. The interface layer may include a layer of a passivating material (e.g., made from nitrogen, oxygen, oxynitride, arsenic, hydrogen and/or fluorine) and sometimes also includes a separation layer. In some cases, the interface layer may be a monolayer of a semiconductor passivating material. The interface layer thickness corresponds to a minimum specific contact resistance of less than or equal to 10 O-μm2 or even less than or equal to 1 O-μm2 for the electrical device.

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METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

RELATED APPLICATIONS

[0001] The present application is related to co-pending U.S. Patent Application No. 10/342,576 entitled "INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL", filed on January 14, 2003, by the present inventors and assigned to the same assignee as the present application. This related patent application is hereby incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0002] The invention relates generally to semiconductor processing and semiconductor devices. More particularly, the invention relates to a process for depinning the Fermi level of a semiconductor at a metal-interface layer-semiconductor junction and to devices that employ such a junction.

BACKGROUND

[0003] One of the most basic electrical junctions used in modern devices is the metal-semiconductor junction. In these junctions, a metal (such as aluminum) is brought in contact with a semiconductor (such as silicon). This forms a device (a diode) which can be inherently rectifying; that is, the junction will tend to conduct current in one direction more favorably than in the other direction. In other cases, depending on the materials used, the junction may be ohmic in nature (i.e., the contact may have negligible resistance regardless of the direction of current flow). Grondahl and Geiger first studied the rectifying form of these junctions in 1926, and by 1938 Schottky had developed a theoretical explanation for the rectification that was observed.

[0004] Schottky's theory explained the rectifying behavior of a metal-semiconductor contact as depending on a barrier at the surface of contact between the metal and the semiconductor. In this model, the height of the barrier (as measured by the potential necessary for an electron to pass from the metal to the semiconductor) was postulated as the difference between the work function of the metal (the work function is the energy required to free an electron at the Fermi level of the metal, the Fermi level being the highest occupied energy state of the metal at $T = 0$) and the electron affinity of

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the semiconductor (the electron affinity is the difference between the energy of a free electron and the conduction band edge of the semiconductor). Expressed mathematically:

$$\phi_B = \phi_M - \chi_S \qquad [1]$$

where Φ_B is the barrier height, Φ_M is the work function of the metal and χ_S is the electron affinity of the semiconductor.

[0005] Not surprisingly, many attempts were made to verify this theory experimentally. If the theory is correct, one should be able to observe direct variations in barrier heights for metals of different work functions when put in contact with a common semiconductor. What is observed, however, is not direct scaling, but instead only a much weaker variation of barrier height with work function than implied by the model.

[0006] Bardeen sought to explain this difference between theoretical prediction and experimental observation by introducing the concept that surface states of the semiconductor play a role in determining the barrier height. Surface states are energy states (within the bandgap between the valence and conduction bands) at the edge of the semiconductor crystal that arise from incomplete covalent bonds, impurities, and other effects of crystal termination. **Figure 1** shows a cross-section of an un-passivated silicon surface labeled 100. The particular silicon surface shown is an Si(100) 2x1 surface. As shown, the silicon atoms at the surface, such as atom 110, are not fully coordinated and contain un-satisfied dangling bonds, such as dangling bond 120. These dangling bonds may be responsible for surface states that trap electrical charges.

[0007] Bardeen's model assumes that surface states are sufficient to pin the Fermi level in the semiconductor at a point between the valence and conduction bands. If true, the barrier height at a metal-semiconductor junction should be independent of the metal's work function. This condition is rarely observed experimentally, however, and so Bardeen's model (like Schottky's) is best considered as a limiting case.

[0008] For many years, the cause underlying the Fermi level pinning of the semiconductor at a metal-semiconductor junction remained unexplained. Indeed, to this day no one explanation satisfies all experimental observations regarding such junctions. Nevertheless, in 1984, Tersoff proposed a model that goes a long way towards explaining the physics of such junctions. See J. Tersoff, "Schottky Barrier Heights and the Continuum of Gap States," Phys. Rev. Lett. 52 (6), Feb. 6, 1984.

[0009] Tersoff's model (which is built on work by Heine and Flores & Tejedor, and see also Louie, Chelikowsky, and Cohen, "Ionicity and the theory of Schottky barriers," Phys. Rev. B 15, 2154

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(1977)) proposes that the Fermi level of a semiconductor at a metal-semiconductor interface is pinned near an effective "gap center", which is related to the bulk semiconductor energy band structure. The pinning is due to so-called metal induced gap states (MIGS), which are energy states in the bandgap of the semiconductor that become populated due to the proximity of the metal. That is, the wave functions of the electrons in the metal do not terminate abruptly at the surface of the metal, but rather decay in proportion to the distance from that surface (i.e., extending inside the semiconductor). To maintain the sum rule on the density of states in the semiconductor, electrons near the surface occupy energy states in the gap derived from the valence band such that the density of states in the valence band is reduced. To maintain charge neutrality, the highest occupied state (which defines the Fermi level of the semiconductor) will then lie at the crossover point from states derived from the valence band to those derived from the conduction band. This crossover occurs at the branch point of the band structure. Although calculations of barrier heights based on Tersoff's model do not satisfy all experimentally observed barrier heights for all metal-semiconductor junctions, there is generally good agreement for a number of such junctions.

[0010] One final source of surface effects on diode characteristics is inhomogeneity. That is, if factors affecting the barrier height (e.g., density of surface states) vary across the plane of the junction, the resulting properties of the junction are found not to be a linear combination of the properties of the different regions. In summary then, a classic metal-semiconductor junction is characterized by a Schottky barrier, the properties of which (e.g., barrier height) depend on surface states, MIGS and inhomogeneities.

[0011] The importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction. Thus, if one were able to control or adjust the barrier height of a metal-semiconductor junction, one could produce electrical devices of desired characteristics. Such barrier height tuning may become even more important as device sizes shrink even further. Before one can tune the barrier height, however, one must depin the Fermi level of the semiconductor. As discussed in detail below, the present inventors have achieved this goal in a device that still permits substantial current flow between the metal and the semiconductor.

SUMMARY OF THE INVENTION

[0012] The present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal – interface

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layer – semiconductor junction, there exist corresponding minimum specific contact resistances. The interface layer thickness corresponding to this minimum specific contact resistance will vary depending upon the materials used, however, it is a thickness that allows for depinning the Fermi level of the semiconductor while still permitting current to flow between the metal and the semiconductor when the junction is biased (e.g., forward or reverse biased). By depinning the Fermi level, the present inventors mean a condition wherein all, or substantially all, dangling bonds that may otherwise be present at the semiconductor surface have been terminated, and the effect of MIGS has been overcome, or at least reduced, by displacing the semiconductor a sufficient distance from the metal. Minimum specific contact resistances of less than or equal to approximately 10 $\Omega-\mu m^2$ or even less than or equal to approximately 1 $\Omega-\mu m^2$ may be achieved for such junctions in accordance with the present invention.

[0013] Thus, in one embodiment, the present invention provides an electrical device in which an interface layer is disposed between and in contact with a metal and a silicon-based semiconductor and is configured to depin the Fermi level of the semiconductor while still permitting current flow between the metal and the semiconductor when the electrical device is biased. The specific contact resistance of the electrical device is less than approximately 10 $\Omega-\mu m^2$. The interface layer may include a passivating material (e.g., a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride) and sometimes also includes a separation layer. In some cases, the interface layer may be essentially a monolayer (or several monolayers) of a semiconductor passivating material.

[0014] In another embodiment, the interface layer is made up of a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material, for example ammonia (NH_3), nitrogen (N_2) or unbound gaseous nitrogen (N) generated from a plasma process. In such cases, the interface layer may be fabricated by heating the semiconductor while in a vacuum chamber and exposing the semiconductor to the nitrogenous material.

[0015] A further embodiment of the present invention provides for depinning the Fermi level of a semiconductor in an electrical junction through the use of an interface layer disposed between a surface of the semiconductor and a conductor. The interface layer preferably (i) is of a thickness sufficient to reduce effects of MIGS in the semiconductor, and (ii) passivates the surface of the semiconductor. Despite the presence of the interface layer, significant current may flow between the conductor and the semiconductor because the thickness of the interface layer may be chosen to

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provide a minimum (or near minimum) specific contact resistance for the junction. As indicated above, the interface layer may include a passivating material such as a nitride, oxide, oxynitride, arsenide, hydride and/or fluoride.

[0016] Further embodiments of the present invention provide a junction between a semiconductor and a conductor separated from the semiconductor by an interface layer configured to allow a Fermi level of the conductor to (i) align with a conduction band of the semiconductor, (ii) align with a valence band of the semiconductor, or (iii) to be independent of the Fermi level of the semiconductor. In some or all of these cases, current may flow between the conductor and the semiconductor when the junction is biased because the interface layer has a thickness corresponding to a minimum or near minimum specific contact resistance for the junction. For example, specific contact resistances of less than or equal to approximately 2500 $\Omega-\mu m^2$, 1000 $\Omega-\mu m^2$, 100 $\Omega-\mu m^2$, 50 $\Omega-\mu m^2$, 10 $\Omega-\mu m^2$ or even less than or equal to 1 $\Omega-\mu m^2$ may be achieved.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0017] The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

[0018] **Figure 1** shows a cross-section of an un-passivated silicon surface containing surface silicon atoms with dangling bonds.

[0019] **Figure 2** illustrates various energy levels for metals and semiconductors and is labeled to show the work function of a metal and the electron affinity of a semiconductor.

[0020] **Figure 3** shows an energy band diagram for a conventional metal – *n*-type semiconductor junction and also illustrates the concept of a depletion region formed in the semiconductor when the materials are brought into contact with one another.

[0021] **Figure 4** illustrates band bending at a conventional metal – *n*-type semiconductor junction.

[0022] **Figure 5** shows a semiconductor device containing a semiconductor material having a surface across which electrical current flows during operation of the semiconductor device, and

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containing an interface layer formed on the surface according to one embodiment of the present invention.

[0023] **Figure 6** shows an electrical junction containing an interface layer that is disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

[0024] **Figures 7a, 7b, 7c and 7d** show relationships between Fermi energy, conduction-band energy, and valence-band energy for an unpassivated Schottky diode, a passivated Schottky diode in which MIGS are not removed, an unpassivated Schottky diode in which MIGS are removed and a passivated Schottky diode in which MIGS are removed according to one embodiment of the present invention, respectively.

[0025] **Figure 8** shows a curve of interface layer resistance versus interface layer thickness for an electrical junction containing an interface layer disposed between a semiconductor and a conductor in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0026] Described herein are processes for depinning the Fermi level of a silicon-based semiconductor (e.g., Si, SiC or SiGe) at a metal-semiconductor junction as well as devices that use such a junction. As more fully discussed below, an interface layer is introduced between the semiconductor and the metal. The interface layer functions to passivate the semiconductor surface (that is, terminate dangling bonds that may otherwise be present at the semiconductor surface so as to assure chemical stability of the surface) and to displace the semiconductor from the metal so as to reduce the effect of MIGS.

[0027] As discussed more fully below, the present inventors have determined that for thin interface layers disposed between a metal and a silicon-based semiconductor (e.g., Si, SiC and SiGe), so as to form a metal – interface layer – semiconductor junction, there exist corresponding minimum specific contact resistances. Indeed, minimum specific contact resistances of less than or equal to approximately 10 $\Omega - \mu m^2$ or even less than or equal to approximately 1 $\Omega - \mu m^2$ may be achieved for such junctions in accordance with the present invention. To achieve such low contact resistances, a metal that has a work function near the conduction band of the semiconductor for n-

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type semiconductors, or a work function that is near the valence band for p-type semiconductors, is selected.

[0028] The Schottky barrier in such junctions is already minimized, meaning that it is much less than the Schottky barrier presented by a junction in which the Fermi level is pinned, generally near the middle of the semiconductor's bandgap. The current versus voltage (IV) characteristic of these junctions is non-linear, generally having a slope that increases as the voltage increases, such that the derivative of current with respect to voltage is increasing with voltage. This results in a decreasing differential resistance (*dV/dI)* and a decreasing resistance (*V/I)*. Thus, a junction that has high resistance or high differential resistance near the origin of the IV characteristic (zero volts) may have significantly lower resistance or lower differential resistance at higher voltages.

[0029] The present invention achieves low resistance and low differential resistance near the origin of the current-voltage characteristic for a metal – interface layer – semiconductor junction. Generally, the voltage around the origin should be less than about 100 mV, or more preferably less than about 10 mV for purposes of measuring, determining, or utilizing such junctions of low resistance. At higher voltages, the junction resistance will be even lower. It is thus a feature of the present invention to set an upper bound on the resistance of a contact, where the upper bound occurs at low voltages.

[0030] It is further noted that in junctions where the Schottky barrier is minimized as described above, such that the Fermi level at the junction interface at zero volts lies at or near the conduction band edge or valence band edge (for *n*- and *p*-type semiconductors, respectively), the *IV* characteristic will be nearly symmetric, especially at low voltage. In this case, the term "forward bias" is not defined in the usual sense of a diode wherein forward bias corresponds to the direction of bias for which greater current flows. Thus, in determining or utilizing low resistance junctions of the present invention, the voltage may be either positive or negative.

[0031] It is also possible (in accordance with a further embodiment of the present invention) to make junctions where the Schottky barrier is higher than it would be if the Fermi level at the junction interface were pinned, usually around mid-gap of the semiconductor. Such junctions are formed in the present invention between a metal with a workfunction near or substantially equal to the conduction band edge of a *p*-type semiconductor, or between a metal with a workfunction near or substantially equal to the valence band edge of an *n*-type semiconductor. These junctions are diodes, in that little current will flow if the *n*-type (*p*-type) semiconductor is biased positive (negative) with

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respect to the metal, and large currents will flow if the voltage is reversed. The low-current flow state is referred to as reverse bias, and the high-current flow state is referred to as positive bias.

[0032] Low resistance in the case of a diode is only relevant in forward bias conditions. In junctions created in accordance with the present invention the resistance contribution of the interface layer is smaller than the resistance due to the Schottky barrier. That is, in forward bias conditions for junctions created in accordance with the present invention, the transport of charge is limited mainly by the thermal emission of carriers from the semiconductor over the barrier at the interface, and not by the tunneling through the interface dielectric. Thus, low resistance in the case of a diode refers to a resistance lower than the resistance presented by the Schottky barrier.

[0033] In certain applications of diodes, the ability to withstand high reverse biases may be more desirable than high current flow in forward bias. These applications would be considered high voltage/low power applications. In such cases, a low resistance is not essential, and junctions created in accordance with still another embodiment of the present invention provide high-voltage diodes capable of withstanding voltages higher than could otherwise be achieved if the Fermi level of the semiconductor in the junction were pinned.

[0034] The present invention is discussed below in terms of presently preferred embodiments thereof, however, this discussion is not meant to limit the scope of the invention. By studying the present disclosure, others of ordinary skill in the art may recognize equivalent procedures, materials or structures that can be substituted for those described herein to achieve the same effect. The reader is advised and reminded that the use of such equivalents is deemed to be within the scope of the present invention. For example, where the discussion refers to well-known structures and devices, block diagrams are used, in part to demonstrate the broad applicability of the present invention to a wide range of such structures and devices.

I. Introduction and Definitions

[0035] The present discussion makes use of terms that, although well known in the art, may not be familiar to all readers. Therefore, before beginning a detailed discussion of the present invention, it is helpful to define certain terms and concepts. To understand the properties of metal-semiconductor junctions and the impact of the present invention, one must refer to some important energy scales, which are shown graphically in **Figure 2**. The so-called vacuum level (E_0) represents the minimum energy that an electron needs to possess in order to completely free itself from a metal or

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semiconductor. For a metal, the Fermi level (E_F) represents the highest occupied energy level for the material. That is, nearly all energy states below the Fermi level are filled, while nearly all states above the Fermi level are empty. The work function of the metal (Φ_M) is then defined as the energy required to free an electron at the Fermi level and mathematically it is the difference between the vacuum level and the Fermi level. The work function is an invariant bulk property of the metal.

[0036] As illustrated in the diagram, semiconductors also have a Fermi level (E_F) and a work function (Φ_S), however, the work function is not an invariant property of the semiconductor. Because the Fermi level varies depending on the doping level in the semiconductor (i.e., the relative amounts of impurities introduced into the semiconductor crystal which change the electron and hole carrier concentrations), a separate parameter, the electron affinity (χ_S), is defined. The electron affinity is an invariant property of the semiconductor and is the difference between the vacuum level and the conduction band edge of the semiconductor. In a semiconductor, almost all energy states are filled in the valence band (E_V) while the conduction band (E_C) is almost empty.

[0037] Now consider a conventional junction between a metal and an *n*-type semiconductor that has a work function smaller than the work function of the metal (i.e., $\Phi_S < \Phi_M$). An *n*-type semiconductor is one in which electrons are the majority charge carriers (in *p*-type semiconductors, holes are the majority charge carrier). As shown in **Figure 3**, because the Fermi level in the semiconductor is higher than the Fermi level in the metal, electrons transfer from the semiconductor 310 to the metal 320 when the materials are brought into contact. Thus, a depletion region (i.e., a region in which there are no free charge carriers) 330 forms near the junction interface 340.

[0038] The formation of the depletion region gives rise to an electric field and so-called "band bending", as one approaches the junction interface from the semiconductor side (see **Figure 4**). The band bending creates an energy barrier (discussed above) that blocks further transfer of electrons into or out of the semiconductor. Similar barriers are formed for a junction between a metal and a *p*-type semiconductor when the work function of the metal is less than the work function of the semiconductor. However, in the case of a metal– *n*-type semiconductor junction in which the work function of the semiconductor is greater than that of the metal or a metal–*p*-type semiconductor junction in which the work function of the semiconductor is less than that of the metal, no such energy barriers are created and the contact is said to be ohmic in nature.

[0039] As discussed above, although Schottky first postulated that the height of the energy barrier (Φ_b) formed at a metal-semiconductor junction was simply the difference between the work function

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of the metal and the electron affinity of the semiconductor, experiments have not verified this relationship. Instead a more complex explanation that takes into account the effects of surface defect states, inhomogeneities and MIGS appears to provide more accurate estimates of barrier heights by explaining the pinning of the Fermi level in the semiconductor. The present inventors have created a technique which is believed to depin the Fermi level of a Si-based semiconductor at a junction with a metal (and thus allow for control or tuning of the barrier height) by both passivating the semiconductor surface (to eliminate or at least reduce the effects of surface states and possibly inhomogeneities) and displacing the metal from the semiconductor (to eliminate or at least reduce the effects of MIGS). This depinning is achieved by introducing an interface layer between the semiconductor and the metal to create a semiconductor -- interface layer -- metal junction, which still permits significant current to flow between the metal and the semiconductor when the junction is forward biased.

[0040] This latter point is important. As discussed further below, for contacts where the energy bands of the semiconductor and the conductor align (i.e., where the Fermi level of the conductor aligns with the conduction or valence band of the semiconductor depending on semiconductor type and/or contact application), if the interface layer is too thin, the specific contact resistance of the junction increases because of the presence of MIGS, resulting in an increased barrier height; thus, current flow is hampered. Conversely, if the interface layer is too thick, the specific contact resistance is again increased and one gets low current across the junction because of tunneling limitations. The present invention achieves an interface layer that is thick enough to reduce or eliminate the effect of MIGS, while still thin enough to permit significant current flow.

II. Passivation of Semiconductor Surfaces

[0041] A common processing operation performed during semiconductor device fabrication is silicon surface passivation. Surface passivation (whether by an oxide or another material) chemically neutralizes and physically protects the underlying silicon. For example, exposing a silicon surface to oxygen (under the appropriate conditions to grow a protective film of silicon dioxide) will allow the oxygen to react with the dangling bonds of the silicon surface to form covalent bonds that satisfy the surface silicon atoms' valency and render the surface fully coordinated. These covalent bonds provide chemical stability to the silicon surface. The covalent

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bonds also tie up unbound charges that exist on the silicon surface as a result of the discontinuation of the semiconductor crystal at the surface.

[0042] However, passivation with silicon dioxide has several significant disadvantages. For example, silicon dioxide is a dielectric insulator that poses a significant barrier to the flow of current. Accordingly, a layer of silicon dioxide deposited or grown on a silicon surface may significantly reduce the ability for electrical current to flow through that surface. As a result, the use of silicon dioxide has been limited in practicality to surfaces external to the active region of semiconductor devices through which current passes during device operation (e.g., as a gate oxide layer). This disadvantage is compounded by the fact that the silicon dioxide grows very rapidly and readily on the silicon surface so that it is difficult to limit the growth to a thin layer. Silicon dioxide is also a poor diffusion barrier to semiconductor dopants such as boron.

[0043] Instead of making use of silicon dioxide then, in one embodiment the present inventors utilize a nitrided semiconductor surface to provide chemical passivation. That is, a nitride layer is introduced to passivate the semiconductor surface by eliminating or at least reducing the effects of surface states and possibly inhomogeneities. The nitride layer also displaces the metal from the semiconductor and eliminates or at least reduces the effects of MIGS. The result of introducing the nitride layer as an interface between the semiconductor and the metal is a depinning of the Fermi level of the semiconductor. When the Fermi level of the semiconductor is depinned, the Fermi level of the metal at the interface will be that of the bulk metal, and will not be dependent upon the interface. In addition to the above, the present inventors propose techniques for providing non-insulating, passivated semiconductor surfaces using materials other than nitrogen; for example, oxides, hydrides, arsenides and/or fluorides.

[0044] These developments have wide applicability in connection with the fabrication of Schottky diodes, Schottky-barrier transistors and other electrical components. For example, in Schottky diodes, the ability to control the energy barrier height at the diode junction is important if the device is to be tailored to specific applications. Use of the present techniques allows for tuning of the barrier height. Further, for other three-terminal devices with Schottky-barrier-isolated channels, control of device characteristics is made possible through the present invention by allowing *n*- and *p*-type devices to be fabricated without dopants, relying instead on the use of metals with different work functions.

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[0045] **Figure 5** shows a semiconductor device 510 that contains a semiconductor 530 and an interface layer 520 formed on a surface 540 of the semiconductor in accordance with the present invention. The terms semiconductor device, microelectronic device, monolithic device, chip, and integrated circuit are often used interchangeably in this field. Any or all such devices may each contain an interface layer formed on a semiconductor surface in accordance with the present invention.

[0046] The semiconductor 530 contains a semiconductor material. The term semiconductor material refers to a material having a bandgap that is greater than about 0.1 eV and less than about 4 eV. The term bandgap refers to an energy gap of forbidden energy levels separating the conduction band, which is an upper energy band that is mostly devoid of electrons and wherein electrons can conduct, and the valence band, which is an energy band that is mostly filled with electrons and wherein electrons cannot conduct. The semiconductor material may have a wide range of doping levels including no doping at all.

[0047] The semiconductor 530 has a surface 540 that is passivated by the interface layer 520. In this context (and as used elsewhere herein) the term passivation means the elimination or at least the reduction of the effects of surface states due to defects or dangling bonds of the semiconductor surface 540. Note that passivation does not, as a practical matter, require that all surface states be eliminated. Rather, it is the effect of surface states on the device properties that is limited or eliminated in passivation. Note further that the presence of MIGS may be regarded as a surface state, however, as used herein the term passivation is not meant to infer the elimination of MIGS (though in some cases, a passivation layer may have sufficient thickness to provide a separation layer between the semiconductor and the metal sufficient to reduce or eliminate MIGS). The semiconductor 530 is operable to be electrically coupled with a first voltage associated with the semiconductor device 510 and to conduct electrical current 550 across the passivated surface 540.

[0048] The interface layer 520 is formed on the semiconductor 530 and may contain a passivation material that bonds to the semiconductor material by way of a covalent (or other) bond formed between the passivation material and the semiconductor material. For example, an atom of passivation material may covalently bond with a dangling bond of a surface silicon atom to fully coordinate the silicon atom and thereby help passivate the silicon atom. In some cases, the passivation material may be the sole component of the interface layer 520, while in other cases the interface layer 520 may be a compound layer that includes both a passivation layer and a separation

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layer. That is, the interface layer serves to (i) chemically passivate the semiconductor surface 540, and (ii) displace the semiconductor from the metal sufficiently to eliminate or at least reduce the effect of MIGS. As explained below, this may necessitate including a separation layer in addition to a passivation layer within the interface layer, depending on the passivation material selected. Of course, the combination of the passivation layer and the separation layer must be sufficiently thin to permit the low specific contact resistances described herein.

[0049] Different passivation materials are contemplated. According to one embodiment, the interface layer 520 is formed using a material that is preferably selected from the group consisting of hydrogen (H), oxygen (O), nitrogen (N), arsenic (As), and fluorine (F) (that is, the interface layer 520 may include a nitride, an oxide, a hydride, an arsenide and/or a fluoride). Other materials having chemical characteristics or valences similar to these materials may also be used. Note that distinct separation layers (i.e., in addition to the passivation layer(s)) may be needed where H, As, or F passivation layers are used, as these tend to form monolayer coverage, rather than a layer of a compound with Si of process-dependent thickness. In contrast, passivation layers made using N and/or O may not require distinct separation layers, as these elements may form a layer of a compound of Si with a thickness that can be varied depending on processing.

[0050] Different amounts of passivation material are contemplated to be useful for different embodiments of the present invention. Often, the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm. For example, depending upon the particular implementation, the thickness may be less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, may be the thickness corresponding to a single layer or monolayer of passivation material that is bonded to the semiconductor surface, or may even be the number of atoms of passivation material required to passivate substantially all the dangling bonds associated with the semiconductor surface 540.

[0051] In some cases, passivation of the semiconductor surface 540 will include removing (or terminating) dangling bonds located proximate to the surface of the semiconductor material, including those at the surface as well as those within a few molecular dimensions from the surface. This process may stabilize the surface of the semiconductor material and may improve the controllability of subsequent fabrication operations. Passivation may also reduce the density of surface states that may exist at the semiconductor surface as a result of the discontinuation of the semiconductor crystal at the surface. This may improve consistency and performance of the

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semiconductor device, inasmuch as such states are known to interfere with proper device operation. For example, they may provide surface charge states that result in a pinning of the Fermi level.

III. Forming Interface Layers

[0052] Exemplary methods for forming interface layers to provide (i) passivation of semiconductor surfaces, and (ii) displacement of the semiconductor from the metal to eliminate or at least reduce of the effects of MIGS within the semiconductor when in the presence of the metal (collectively referred to herein as depinning the Fermi level of the semiconductor) with hydrogen, fluorine or nitrogen are presented below to further illustrate the concepts of the present invention. Other passivation materials may include arsenic, oxygen or an oxynitride, and in some cases such passivation layers are combined with separation layers (e.g., made of an oxide) to complete the interface layer.

A. Hydrogen And Fluorine

[0053] An interface layer may contain hydrogen, fluorine, or both hydrogen and fluorine (e.g., in the form of a hydride and/or a fluoride). One method for forming an interface layer on a semiconductor surface with hydrogen and fluorine includes cleaning the semiconductor substrate with a cleaning solution, immersing the cleaned substrate in a hydrogen fluoride solution (or other liquid containing hydrogen and fluorine ions) having an effective concentration typically between about 1%-50% by weight, waiting an effective period of time, typically between about several seconds and about 5 minutes, removing the substrate from the hydrogen fluoride solution, optionally rinsing the substrate in deionized water, and blow-drying the substrate with nitrogen. Such a method may form an interface layer containing hydrogen and fluorine that are bonded (e.g., covalently) to the semiconductor surface.

[0054] It should be noted that long rinses in deionized water, generally longer than about 30 seconds, might remove the hydrogen passivation. Thus, deionized water rinses might advantageously be kept to less than about 30 seconds to maintain the hydrogen passivation of the surface. Also, the higher the concentration of the hydrogen fluoride during the immersion, the greater the concentration of fluorine passivation. Finally, methods are also contemplated where the ratio of hydrogen to fluorine passivation is altered by removing either the hydrogen or the fluorine.

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[0055] An interface layer formed in this fashion may be best suited for applications where a subsequent metal layer is deposited over the interface layer in a generally non-invasive fashion, for example using a thermally evaporated source. Experiments by the present inventors to date suggest that using other approaches (e.g., plasma deposition) may cause damage to the thin (e.g., monolayer thick) interface layer contemplated as part of the present invention.

B. Nitrogen

[0056] In a further embodiment, an interface layer may contain nitrogen (e.g., in the form of silicon nitride). One method for forming an interface over a semiconductor surface with nitrogen includes heating a substrate containing the semiconductor surface in the presence of a nitrogenous material (that is, a gas or other material containing nitrogen). For example, a substrate containing an exposed silicon surface may be annealed at a temperature between about 300°C and about 750°C, which is lower than temperatures conventionally used for Rapid Thermal Nitridation (RTN), under a gaseous ambient having, for example, ammonia (NH_3) at some effective partial pressure. By exposed, we mean a clean surface, free of everything except silicon. Such a method may form an interface layer containing nitrogen, often in the form of a nitride, bonded to the semiconductor surface. Note that the present inventors have observed indications suggesting that in these low temperature conditions interface layer growth is self-limiting, depending only on temperature.

[0057] According to another embodiment, an interface layer that includes nitrogen may be formed on an exposed surface of a semiconductor material by a method that includes heating a semiconductor material to a substantially high temperature under vacuum and exposing the semiconductor material to a substantially small amount of a nitrogenous material, such as ammonia. The method may include placing a semiconductor having an exposed semiconductor surface in a heating chamber, pulling a vacuum of less than about one millionth of a Torr, or more favorably an ultra high vacuum of less than 10^{-9} Torr, and then heating the semiconductor in the heating chamber to a substantially high temperature. The higher the vacuum, the longer the substrate may be heated without growth of an oxide from residual oxygen or water in the chamber. Thus, the process may include heating the semiconductor to a temperature that is between about 900°C and about 1000°C, or higher, in an inert ambient. As desired, the semiconductor may be exposed to hydrogen gas, or an equivalent, to reduce any native oxide on the semiconductor. These high temperatures may provide

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for greater passivation of the semiconductor surface as compared with results that may be achieved at lower temperatures.

[0058] Then, the heated semiconductor may be exposed to a substantially small amount of a nitrogenous material, such as ammonia. This may include exposing the semiconductor surface to ammonia for a substantially short period of time. For example, the surface may be subjected to a burst or pulse of ammonia lasting for a time period between about 0.5 seconds and about 5 seconds. Alternatively, the surface may be exposed to a controlled, small amount of ammonia over an arbitrarily longer period of time. In this way, the substantially small amount of ammonia will react with the surface to form a nitrogenous interface layer, such as a nitride layer, thereon and then further growth of the interface layer will cease. Then the semiconductor may be cooled from the substantially high temperature to ambient temperature and removed from the heating chamber. Further annealing of the substrate and the grown nitride layer may also be performed in the vacuum chamber before removal, at a substantially elevated temperature between about 700°C and 1000°C, or higher.

[0059] Advantageously, it has been unexpectedly observed that a process such as that described above and incorporating substantially high temperature exposure for substantially short periods may be used to controllably form thin yet effective interface layers. That is, the present inventors have observed that in the creation of thin interface layers that include nitrogenous materials, temperature appears to be a dominant factor in controlling thickness. For example, by such methods effective interface layers may be formed having a thickness that is less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the semiconductor surface.

[0060] Further, thin interface layers may be advantageously grown on a semiconductor in the presence of nitrogen gas, or other inert nitrogen-containing gas. The reaction rate of a semiconductor such as silicon with nitrogen gas is significantly lower than that of a reactive nitrogen-containing gas such as ammonia. The slow growth rate may be desirable for better control of the growth of films of nitrogen on a semiconductor of a thickness of less than about 1 nm, less than about 0.5 nm, less than about 0.2 nm, or having a thickness that corresponds to essentially a single monolayer sufficient to passivate essentially all dangling bonds proximate the silicon surface.

IV. Diodes Containing Passivated Semiconductor Surfaces

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[0061] Diodes made from Schottky barriers (i.e., asymmetric electrical potentials formed at a junction between a metal and a semiconductor) are widely used in rectifiers in power supply and control applications. As used herein, the terms Schottky diode, metal-semiconductor junction diode, diode, and rectifier are all related and appear in order from more specific at the left to more general at the right. Likewise, the terms Schottky barrier, metal-semiconductor barrier, conductor-semiconductor junction, and multi-material junction are all related and appear in order from more specific at the left to more general at the right. The term Schottky diode will be used to refer to a diode containing a Schottky barrier.

[0062] As mentioned above, the present inventors have devised a scheme to control or adjust a Schottky barrier height by forming an interface layer (which includes or sometimes consists of a passivation layer that includes an oxide, oxynitride, nitride, arsenide, hydride, fluoride, or an equivalent) between a metal and a semiconductor. This scheme differs from past attempts by others to control barrier height, which attempts generally involved either using a silicide as a contact metal (and thus limiting the choices of available contact metals to those that can form silicides), or using esoteric substrates that exhibit wide bandgaps. Further, in previous devices the Fermi level of the semiconductor remains pinned, with the barrier height being virtually independent of the metal used. Finally, doping of substrates has also been attempted, however, it has not been shown to truly affect the barrier height of the substrate material. For example, PtSi contacts have reduced resistance due to high silicon doping such that the current across the junction is dominated by tunneling through the barrier. Doping may thus lead to cases where the top of the barrier may be so thin as to be essentially transparent to electrons, however, doping does not appear to allow actual tuning of the barrier height.

[0063] **Figure 6** shows an example of a diode 600 containing, according to one embodiment of the present invention, an interface layer 620 disposed between and attached to both a semiconductor 610 and a conductor 630. The conductor and the semiconductor are operable to be electrically coupled with different voltages associated with the operation of the diode 600 and to pass electrical current through a passivated semiconductor surface formed at the junction between the semiconductor 610 and the interface layer 620.

[0064] The conductor 630 contains a conductive material such as a metal or an alloy of a metal. The terms metal, conductive material, and conductor are all related and appear in order from specific at the left to general at the right. In general, the terms refer to a highly electrically conductive

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substance that has a Fermi energy level that sits in a partially filled band. Unless otherwise specified, conductors include metals (e.g., pure metals and alloys), and other conductors such as doped polysilicon (a nonporous silicon containing randomly oriented crystallites), doped single crystal silicon, and metal silicides. Note that alloys may have workfunctions different than their constituents and may be designed to have specific workfunctions though selective use of ratios of the constituent metals.

[0065] Often, the conductor is a metal since metals may offer advantages over conductive semiconductors including lower resistance, higher carrier mobilities that provide superior high frequency performance and switching, favorable low power characteristics, and ease of manufacturing control. Use of metals may also avoid the need to perform semiconductor doping, which may simplify manufacturing and improve quality control.

[0066] Metals that are contemplated include pure metals, alloys, refractory metals, metals that do not form silicides, metals physically deposited by substantially non-invasive processes such as by condensation of a thermally evaporated metal vapor, and metals having a predetermined work function. The use of non-invasively deposited metals may allow for forming the metal on a thin interface layer without disrupting the passivation properties of the layer.

[0067] A metal having a predetermined work function may be a metal having a work function smaller or greater than that of the semiconductor, depending on the desired application. Often, the semiconductor will be silicon. In this case by the work function of a semiconductor or silicon we mean the energy in the middle of the semiconductor bandgap. Exemplary metals that have a work function smaller than silicon include Group 3A elements, aluminum (Al), indium (In), titanium (Ti), chromium (Cr), tantalum (Ta), cesium (Cs), magnesium (Mg), erbium (Er), ytterbium (Yb), manganese (Mn), lead (Pb), silver (Ag), yttrium (Y), and zinc (Zn). Exemplary metals that have a work function greater than silicon include platinum (Pt), gold (Au), tungsten (W), nickel (Ni), molybdenum (Mo), copper (Cu), cobalt (Co), and palladium (Pd).

[0068] The semiconductor-interface layer-conductor configuration illustrated in **Figure 6** defines what the present inventors have chosen to call a "passivated Schottky barrier". The passivated Schottky barrier is a naturally formed electrical potential barrier to an electron or hole at the Fermi energy (the electrochemical potential) in the conductor due to a depletion region formed in the semiconductor adjacent the conductor. The passivated Schottky barrier may deviate in barrier height from a standard un-passivated Schottky barrier that would form naturally at a contact junction

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between the semiconductor and the conductor without the interface layer disposed therebetween. That is, the passivated Schottky barrier may have a barrier height that depends predominantly upon the bulk characteristics of the semiconductor and the conductor, rather than on surface properties, and may depend in part on the characteristics of the interface layer.

[0069] Indeed, the present inventors have determined that changes in barrier height are approximately monotonic and continuous for variations in surface passivation thickness by nitridation of the semiconductor substrate. More specifically, experiments by the present inventors in a regime where the nitride layer is sufficiently thick to remove MIGS show that temperature of interface layer formation has the strongest effect on barrier height. In other regimes, thickness may be critical. Ideally, if all surface states are removed, barrier height should be controllable simply by the choice of metal used.

[0070] To understand why thickness of the interface layer is important, refer briefly to **Figure 8** where a graph of interface-specific contact resistance versus interface thickness is shown. The graph is for a structure where the workfunction of the metal is the same as the electron affinity in the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the semiconductor. At large thicknesses, the interface layer poses significant resistance to current. As thickness decreases, resistance falls due to increased tunneling current. However, there comes a point where even as the interface layer continues to get thinner, resistance increases. This is due to the effect of MIGS, which increasingly pull the Fermi level of the metal down towards mid-gap of the semiconductor, creating a Schottky barrier. The present inventors have discovered that this competition results in an optimum thickness, as shown in the illustration, where the resistance is a minimum. At this thickness the effect of MIGS has been sufficiently reduced to depin the metal and lower the Schottky barrier, and the layer is still sufficiently thin to allow significant current flow across the interface layer. Contact resistances of less than or equal to approximately 2500 Ω-μm^2, 1000 Ω-μm^2, 100 Ω-μm^2, 50 Ω-μm^2, 10 Ω-μm^2 or even less than or equal to 1 Ω-μm^2 may be achieved.

[0071] Characteristics that may be adjusted to provide a desired barrier height thus include the passivation material used (e.g., selection based on bandgap), the interface layer thickness (e.g., especially where the interface layer is a compound layer formed of a passivation layer and a separation layer), the method of forming the interface layer (e.g., control of parameters such as

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temperature), the interface layer thickness that is substantially similar to a penetration depth of MIGS formed at a metal interface, the metal used for the source and/or drain, and other characteristics.

[0072] One advantage of the ability to adjust the Schottky barrier height with the introduction of interface layer 620 is the ability to form a substantially high barrier height. For example, an interface layer may be used to create a Schottky barrier having a barrier height that is greater than can be achieved through the use of metal silicides, greater than about 2.0 eV, or greater than about 2.5 eV (using a semiconductor with a bandgap at least this large), or nearly 1.0 V using silicon. Such high barrier heights imply the ability to withstand high voltages before breakdown occurs. Thus, Schottky barriers having such high barrier heights may be particularly useful in high-voltage Schottky diodes.

[0073] Another advantage achieved through the use of the interface layer 620 is greater flexibility afforded in selecting a conductor 630. Typically, metals chosen for application in classic Schottky diodes are those that can form a silicide with a silicon semiconductor. The formation of the silicide helps to reduce surface states (resulting from dangling bonds), but not the effects of MIGS. Thus, the Fermi level at the semiconductor surface is still pinned. Using metals that form silicides upon contact with silicon may thus help to make the devices more reproducible in a manufacturing environment, but such devices still suffer from the drawback of having a barrier height that is fixed.

[0074] According to one embodiment of the present invention, however, one may select a conductor that is not able (or not readily able) to form a silicide with the semiconductor. The metal silicide is not needed because the interface layer provided in accordance with the present invention passivates the semiconductor surface and also reduces or eliminates the effect of MIGS. This may allow for selection of a metal that has properties such as a desirable work function or Fermi level energy, even though that metal may not form a metal silicide.

[0075] For example, to make large-barrier diodes, for an *n*-type doped silicon semiconductor, a metal may be selected that has a work function that is either substantially equal to the valence band energy of the semiconductor or that is within about 0.1 eV to about 0.3 eV of the valence band energy of the semiconductor. Similarly, for a *p*-type doped silicon semiconductor, a metal may be selected that has a work function substantially equal to the conduction band energy of the semiconductor. For Schottky diodes configured in accordance with the present invention, the Fermi level of the metal may lie anywhere in the bandgap of the semiconductor when an interface layer is

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disposed within the junction, resulting in diodes of various barrier heights. The Fermi level of the metal may also lie in the conduction or valence band of the semiconductor.

[0076] The use of interface layer 620 thus provides a way to tune, adjust, or control the height of the barrier between the conductor and the semiconductor. Without the interface layer 620, the barrier height would be substantially un-tunable, un-adjustable, and fixed (as discussed above).

[0077] The role played by interface layer 620 in tuning, adjusting, or controlling the height of the barrier between the conductor 630 and the semiconductor 610 may be understood as a depinning of the Fermi level of the semiconductor. That is, the interface layer may reduce surface states by bonding to the semiconductor material to consume dangling bonds. Additionally, the interface layer may reduce the formation of MIGS in the semiconductor by providing a thickness and bandgap that prevent the electron wave function (of the metal) from penetrating into the semiconductor. The electron wave function may instead penetrate into the interface layer and form MIGS within the interface layer at an energy related to the states of the interface layer material. As desired, the density of the MIGS and the depth of MIGS penetration into the interface layer may be reduced by choosing an interface layer material or materials having a larger bandgap or higher effective mass than the semiconductor.

[0078] According to one embodiment of the present invention then, the interface layer 620 is incorporated into a device operable to pass current through the semiconductor surface and the interface layer during device operation. In such an embodiment, it may be desirable to use an interface layer having a thickness of a monolayer, or, for example between about 0.1 nm and about 0.3 nm, and also having a wide bandgap (as compared to that of the semiconductor) so that the interface layer both de-pins the Fermi level (so that the barrier height depends predominantly on bulk properties of the junction materials) and allows sufficient current transfer across it. Advantageously, such interface layers may be sufficiently thin to provide low impedance to current flow (due to the exponential dependence of direct tunneling on barrier thickness), which is desirable for many semiconductor devices, while also providing sufficient semiconductor surface passivation to allow an adjustable barrier height. That is, the interface layer may allow passivation of surface states and reduction (or elimination) of MIGS in the semiconductor to allow for an adjustable barrier height with a substantially thin layer that allows sufficient current to be transferred across the interface layer.

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[0079] There are several methods by which the barrier height can be made adjustable. For example, adjustment may be made by tuning the degree of Fermi level pinning. In other words, some embodiments may allow for a sufficiently thin interface layer so that not all of the effects of MIGS in the Si are eliminated. Further, the pinning may be varied by combinations of thickness of the interface layer and the choice of interface material. The metal in contact with the interface layer may be pinned by MIGS at different levels in different materials. Conversely, or in addition, the passivation may be left incomplete to allow for an effective level of unpassivated states. Complete depinning of the Fermi level (that is removal of all surface states in Si including MIGS) is another option, in which case one could tune the barrier height simply by choosing a pure metal or an alloy that possesses the desired workfunction. In that case, the barrier height is determined by Equation (1), which until now has been an unrealizable idealization. Note that the type of tuning being discussed here is adjustment of the barrier height by altering the structure of the junction at the time of manufacture, not by varying an externally applied condition during junction operation.

[0080] **Figure 7a – 7d** show relationships between Fermi energy, conduction band energy, and valence band energy for various Schottky barriers containing a metal in contact with (or in close proximity to) a semiconductor, where the bandgap (E_g) of the semiconductor exists between the conduction band (E_c) and the valence band (E_v). In this example, the work function of the metal Φ_M is chosen to be approximately equal to the electron affinity χ_S of the semiconductor. In **Figure 7a**, an unpassivated Schottky barrier 700 is shown. In this example, the Fermi level (E_F) of the metal 730 is pinned in the bandgap of the semiconductor 710. This results in a discontinuity in the vacuum level caused by a charged dipole at the interface.

[0081] In **Figure 7b**, the interface layer 720b is thick enough to passivate dangling bonds at the surface of the semiconductor 710, but not thick enough to eliminate or sufficiently reduce the effect of MIGS. As a result, the band structure is largely unaltered from that seen in the previous illustration. Similarly, in **Figure 7c**, when the interface layer 720c is sufficiently thick to eliminate or reduce the effect of MIGS but not to passivate the semiconductor surface, little change in the energy band structure is observed. However, as shown in **Figure 7d**, when the interface layer 720d is sufficient to both eliminate or reduce the effect of MIGS and to passivate the semiconductor surface, we see the Fermi level of the metal aligning with the conduction band of the semiconductor (i.e., the Fermi level of the semiconductor has been depinned and no longer lines up with the Fermi level of the metal). The vacuum level is now continuous as there is no charged dipole at the

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interface. Thus, the band structure of a device constructed in this fashion is a result of only bulk material properties, not properties of the surface. By way of example, the materials in such cases may be Al and Si, with a work function for Al of approximately $\Phi_M = 4.1$ eV and the electron affinity for Si of approximately $\chi_S = 4.05$ eV.

V. Transistors Containing Passivated Semiconductor Surfaces

[0082] The interface layers described herein may be used in connection with a semiconductor surface of a channel in a field effect transistor. That is, an interface layer may be disposed between a source and a channel, a channel and a drain, or both of an insulated gate field effect transistor. Such use of an interface layer is described in detail in co-pending U.S. Patent Application No.: _____ _____ entitled "INSULATED GATE FIELD EFFECT TRANSISTOR HAVING PASSIVATED SCHOTTKY BARRIERS TO THE CHANNEL", filed _____, 2002 by the present inventors, and assigned to the assignee of the present invention.

[0083] The source and drain contacts at the channel of a field effect transistor are examples of a broader category of metal-interface layer-semiconductor contacts that make up the present invention. In the past, such contacts generally comprised a silicide-n^+-Si junction, which formed a somewhat "leaky" Schottky diode, with a Fermi level of the semiconductor pinned at the midgap. In contrast, the present invention provides a contact wherein the Fermi level of the metal is aligned with the conduction band of the semiconductor (e.g., as shown in Figure 7d). Note that in other cases, depending on the type of semiconductor material and conductors used, the Fermi level of the metal may align with the valence band of the semiconductor.

[0084] Although both types of junctions (i.e., the new passivated Schottky barrier junction and the conventional silicide-semiconductor junction) permit tunneling currents, the present junction can be fabricated with a much thinner interface layer as compared to the thickness of the silicide layer used previously. Indeed, thickness of an order of magnitude less than the silicide thickness can be expected. In a conventional silicide – semiconductor junction a Schottky barrier is formed which is comprised of a depletion layer. The tunnel barrier presented by such a depletion layer may be an order of magnitude thicker than the dielectric tunnel barrier in the present invention. The thinner interface layers provided by the present invention permit higher current across the junction (i.e., lower junction specific contact resistance).

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[0085] Two other properties of the dielectric deserve mention. First is the property of the height of the barrier compared to the semiconductor conduction band (for electrons). In making the barrier thinner than a silicide barrier, the tradeoff may be a higher tunnel barrier (e.g., 2 eV for nitride, compared with about half the gap of 0.6 eV for silicide). Spacer layers may be used with lower barriers (e.g., TiO_2 has a barrier of less than 1 eV). Nevertheless, even with the higher barrier to electrons, the present inventors have determined that the resistance can still be one hundred times lower than a contact to silicon with a silicide barrier.

[0086] The second property is the effective mass of electrons in the dielectric. Larger mass electrons will not penetrate as far (i.e., because of their shorter wavelength) from the metal into the semiconductor. The less the electrons penetrate into the dielectric, the less the effect of MIGS in the dielectric. Thus, MIGS in the dielectric are reduced with larger bandgap and larger effective mass.

[0087] In addition the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility). The high doping profiles were required in the past in order to keep the junction depletion layer relatively thin, so as to increase the tunneling current, thus reducing the junction resistance. However, it is becoming increasingly difficult to increase doping profiles in order to provide low resistance junctions. It may be possible to reach the same level of resistance with a lower doping concentration using the present invention. It may further be possible to achieve much lower resistance even with lower doping concentration. When the present invention is used with high doping levels, the resistance will be further reduced.

[0088] Thus, methods and applications for semiconductor-interface layer-metal junctions have been described. Although described with reference to specific embodiments it should be remembered that various modifications and changes may be made to the techniques described herein without departing from the broader spirit and scope of the invention. The specification and drawings are accordingly to be regarded in an illustrative rather than a restrictive sense and the invention measured only in terms of the claims, which follow.

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CLAIMS

What is claimed is:

1. An electrical device, comprising:

a metal;

a silicon-based semiconductor having a Fermi level; and

an interface layer disposed between and in contact with both the metal and the semiconductor and configured to depin the Fermi level of the semiconductor,

wherein the electrical device has a specific contact resistance of less than or equal to approximately 1000 $\Omega - \mu m^2$.

2. The electrical device of claim 1 wherein the interface layer includes a passivating material.

3. The electrical device of claim 2 wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.

4. The electrical device of claim 3 wherein the interface layer consists essentially of a monolayer configured to depin the Fermi level of the semiconductor.

5. The electrical device of claim 2 wherein the interface layer further includes a separation layer.

6. The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately 100 $\Omega - \mu m^2$.

7. The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

8. The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

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9. The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

10. The electrical device of claim 1 wherein the interface layer comprises a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material.

11. The electrical device of claim 10 wherein the nitrogenous material comprises at least one of ammonia (NH_3), nitrogen (N_2) or unbound nitrogen (N).

12. An electrical device, comprising a metal – interface layer – Si-based semiconductor junction in which the interface layer includes a passivating material and the electrical device has a specific contact resistance of less than approximately 1000 Ω-μm^2.

13. The electrical device of claim 12 wherein the specific contact resistance is less than or equal to approximately 100 Ω-μm^2.

14. The electrical device of claim 12 wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

15. The electrical device of claim 12 wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

16. The electrical device of claim 1 wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

17. The electrical device of claim 12, wherein the passivating material comprises one or more of a nitride, an oxide, an oxynitride a hydride, a fluoride and/or an arsenide of silicon.

18. The electrical device of claim 17, wherein the interface layer comprises a passivation layer and a separation layer.

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19. A method, comprising depinning a Fermi level of a silicon-based semiconductor in an electrical junction through the use of an interface layer disposed between a surface of the semiconductor and a conductor, wherein the interface layer (i) has a thickness sufficient to reduce effects of metal-induced gap states in the semiconductor while providing the junction with a specific contact resistance of less than approximately 1000 $\Omega - \mu m^2$, and (ii) passivates the surface of the semiconductor.

20. The method of claim 19 wherein the specific contact resistance is less than or equal to approximately 100 Ω-μm^2.

21. The method of claim 19 wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

22. The method of claim 19 wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

23. The method of claim 19 wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

24. The method of claim 19 wherein the interface layer has a thickness sufficient to provide a specific contact resistance of the electrical junction of less than or equal to approximately 1 Ω-μm^2.

25. The method of claim 19 wherein the interface layer includes a passivating material selected from the list comprising: an arsenide, a hydride, a fluoride, an oxide, an oxynitride and a nitride of silicon.

26. The method of claim 25 wherein the interface layer consists essentially of a monolayer.

27. The method of claim 19 wherein the interface layer is grown on the semiconductor surface at temperatures above approximately 300 °C.

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28. The method of claim 27 wherein the interface layer is grown in the presence of a nitrogenous material.

29. The method of claim 28 wherein the nitrogenous material comprises one of ammonia (NH_3), nitrogen (N_2), or unbound nitrogen (N).

30. The method of claim 19 wherein the interface layer includes a passivation layer grown by immersion of the semiconductor in a liquid containing hydrogen and fluorine ions.

31. An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness that allows a Fermi level of the conductor to align with a conduction band of the semiconductor, wherein the electrical device has a specific contact resistance less than approximately 1000 Ω-μm^2.

32. The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately 100 Ω-μm^2.

33. The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

34. The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

35. The electrical device of claim 31 wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

36. An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness that allows a Fermi level of the conductor to align with a valence band of the semiconductor, wherein the electrical device has a specific contact resistance less than approximately 1000 Ω-μm^2.

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37. The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately 100 Ω-μm^2.

38. The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

39. The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

40. The electrical device of claim 36 wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

41. An electrical device, comprising a junction between a Si-based semiconductor and a conductor separated from the semiconductor by an interface layer having a thickness that allows a Fermi level of the semiconductor to be independent of a Fermi level of the conductor, wherein the electrical device has a specific contact resistance less than approximately 1000 Ω-μm^2.

42. The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately 100 Ω-μm^2.

43. The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

44. The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

45. The electrical device of claim 41 wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

46. *An electrical device, comprising:*

a silicon-based semiconductor of either *n*-type or *p*-type semiconductor material;

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a metal having a workfunction approximately equal to a conduction band of the semiconductor if the semiconductor is of *n*-type semiconductor material or having a workfunction approximately equal to a valence band of the semiconductor if the semiconductor is of *p*-type semiconductor material; and

an interface layer disposed between and in contact with both the semiconductor and the metal, wherein the electrical device has a specific contact resistance of less than or approximately equal to 1000 Ω-μm^2.

47. The electrical device of claim 46 wherein the interface layer includes a passivating material.

48. The electrical device of claim 47 wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.

49. The electrical device of claim 48 wherein the interface layer consists essentially of a monolayer configured to depin a Fermi level of the semiconductor.

50. The electrical device of claim 47 wherein the interface layer further includes a separation layer.

51. The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately 100 $\Omega - \mu m^2$.

52. The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately 50 Ω-μm^2.

53. The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately 10 Ω-μm^2.

54. The electrical device of claim 46 wherein the specific contact resistance is less than or equal to approximately 1 Ω-μm^2.

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55. The electrical device of claim 46 wherein the interface layer comprises a passivation layer fabricated by heating the semiconductor in the presence of nitrogenous material.

56. The electrical device of claim 55 wherein the nitrogenous material comprises at least one of ammonia (NH_3), nitrogen (N_2) or unbound nitrogen (N).

57. An electrical device, comprising:

a silicon-based semiconductor of either *n*-type or *p*-type semiconductor material;

a metal having a workfunction near or substantially equal to a conduction band edge of the semiconductor if the semiconductor is of *p*-type semiconductor material, or having a workfunction near or substantially equal to a valence band edge of the semiconductor if the semiconductor is of *n*-type semiconductor material; and

an interface layer disposed between and in contact with both the semiconductor and the metal and configured to depin a Fermi level of the semiconductor.

58. The electrical device of claim 57 wherein the interface layer includes a passivating material.

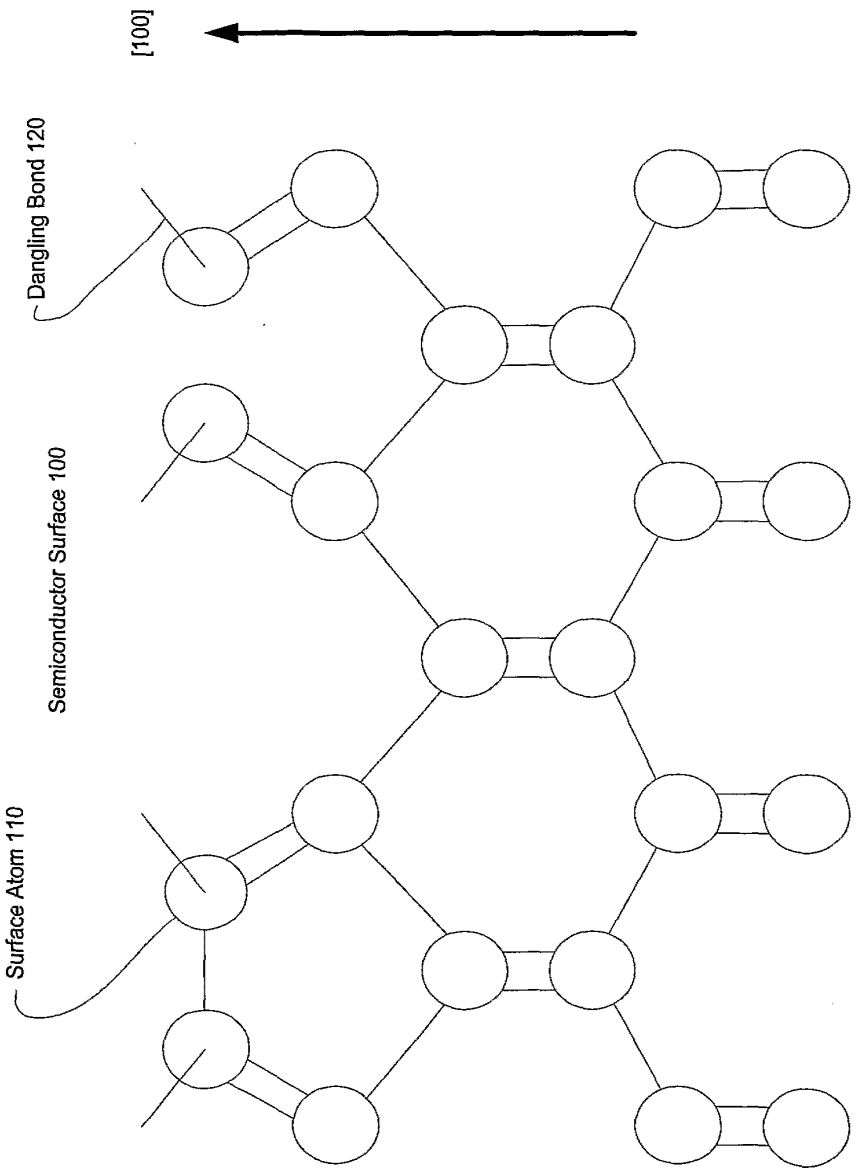
59. The electrical device of claim 58 wherein the passivating material comprises one or more of a nitride, a fluoride, an oxide, an oxynitride, a hydride and/or an arsenide of silicon.

60. The electrical device of claim 57 wherein the interface layer consists essentially of a monolayer configured to depin a Fermi level of the semiconductor.

61. The electrical device of claim 57 wherein the interface layer further includes a separation layer.

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Fig. 1



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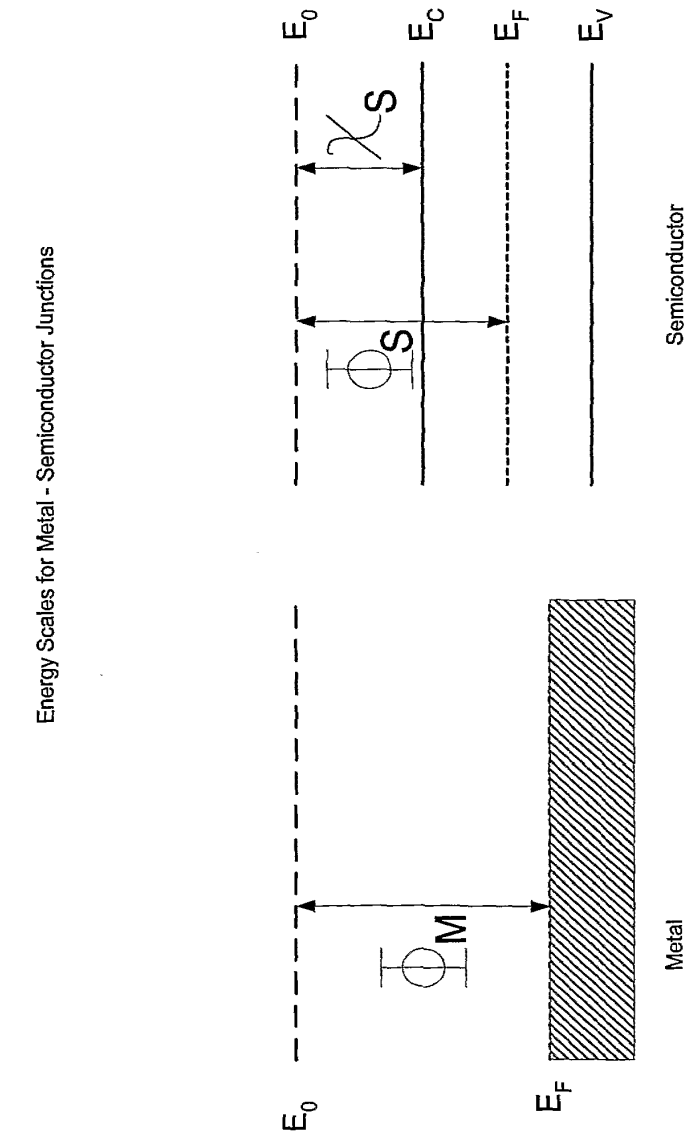


Fig. 2

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Fig. 3

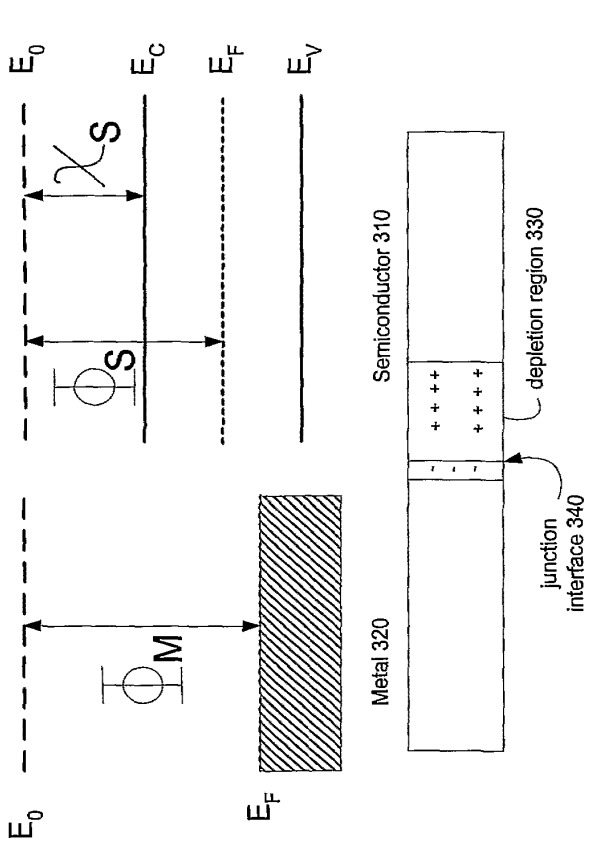
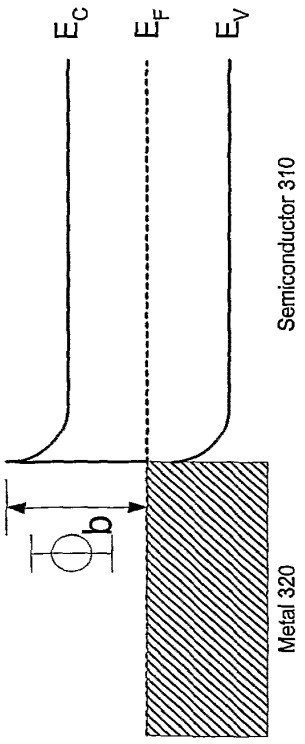


Fig. 4



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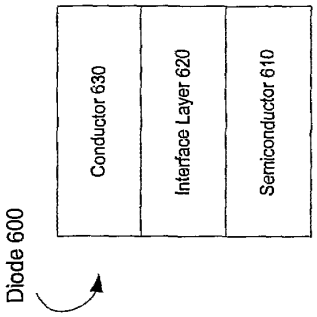


Fig. 6

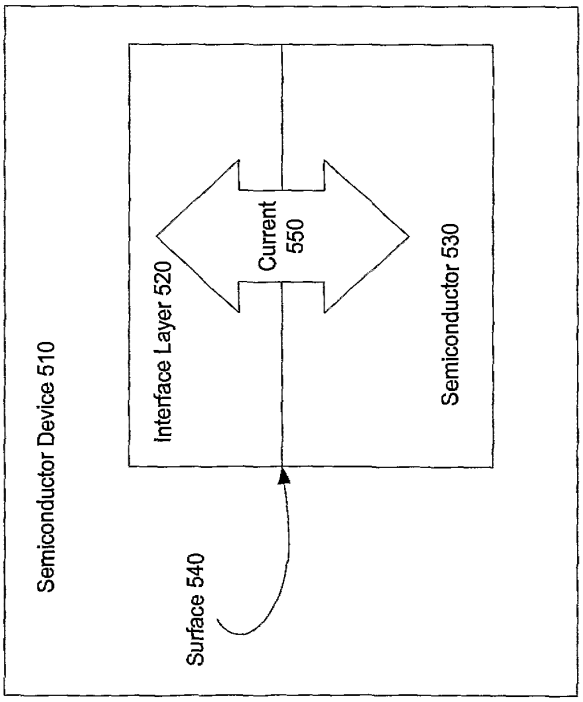


Fig. 5

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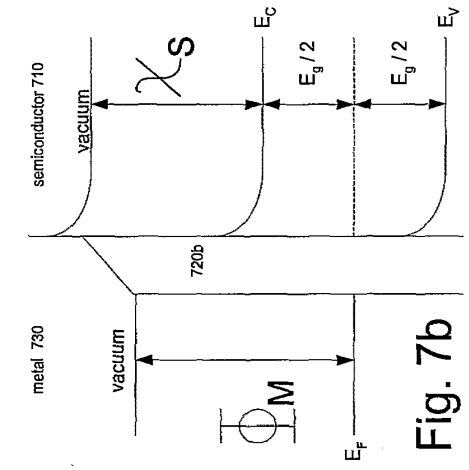


Fig. 7b

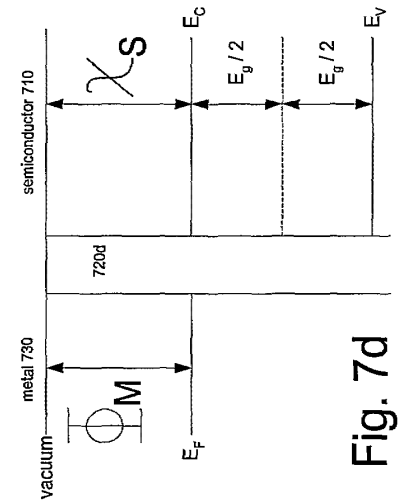


Fig. 7d

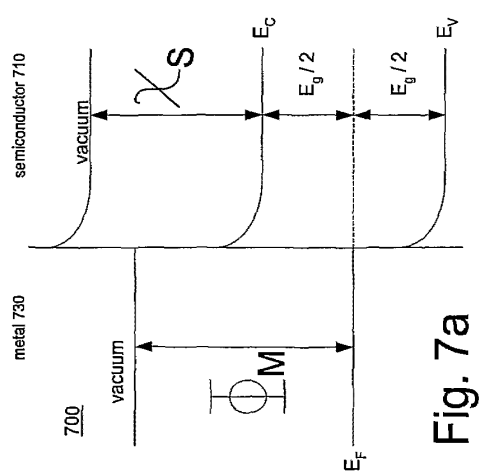


Fig. 7a

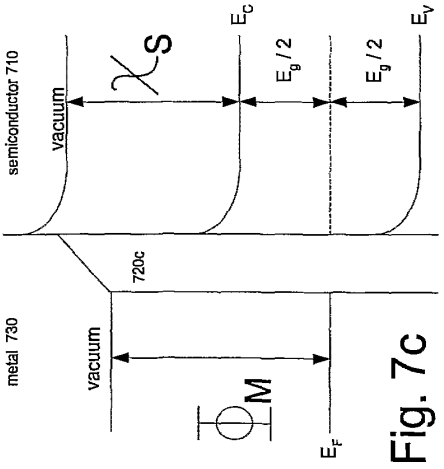
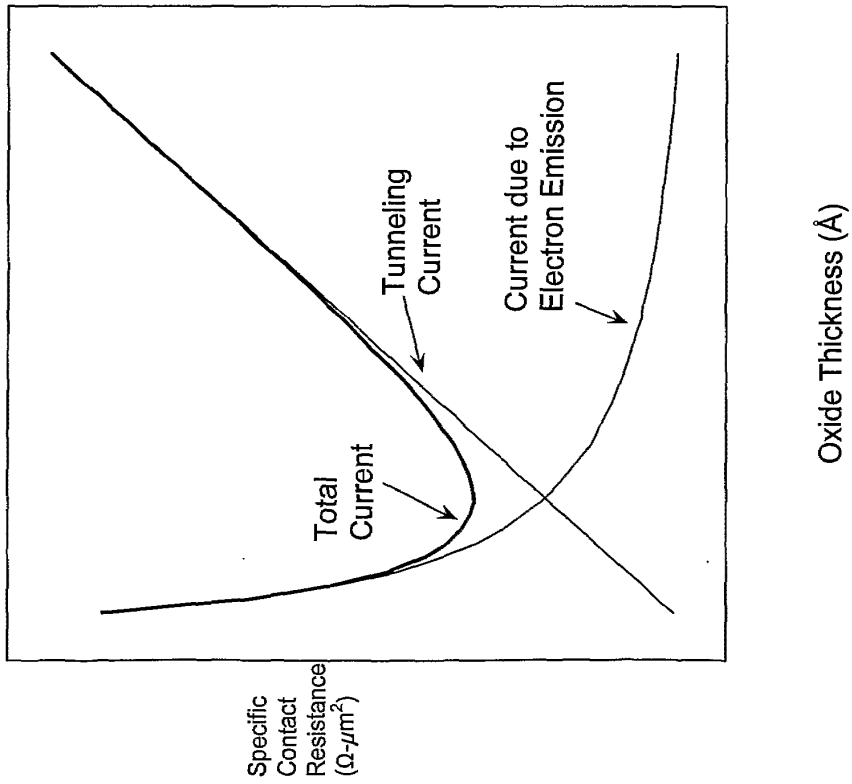


Fig. 7c

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Fig. 8



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INTERNATIONAL SEARCH REPORT

International application No
PCT/US 03/25054

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/45 H01L21/285 H01L29/47 H01L21/329 H01L29/872

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, COMPENDEX, IBM-TDB, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 3 983 264 A (PADOVANI FRANCOIS A ET AL) 28 September 1976 (1976-09-28) column 2, line 49 -column 6, line 29; figure 2 ---	1-26, 31-54, 57-61
X	US 5 021 365 A (WARREN ALAN C ET AL) 4 June 1991 (1991-06-04) column 5, line 64 -column 6, line 49; figures 2,4,9 ---	1-26, 31-54, 57-61
X	EP 0 295 490 A (IBM) 21 December 1988 (1988-12-21) column 5, line 19 -column 6, line 24; figures 2-5 --- -/--	1-26, 31-54, 57-61

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 November 2003	03/12/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Berthold, K

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US 03/25054

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
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Y	TERAJI T ET AL: "OHMIC CONTACTS TO N.TYPE 6H.SIC WITHOUT POST-ANNEALING" MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS, MATERIALS RESEARCH SOCIETY, PITTSBURG, PA, US, 8 April 1996 (1996-04-08), pages 149-154, XP002068069 ISSN: 0272-9172 page 150 -page 153	1-61
Y	SOBOLEWSKI M A ET AL: "PROPERTIES OF ULTRATHIN THERMAL NITRIDES IN SILICON SCHOTTKY BARRIER STRUCTURES" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 54, no. 7, 13 February 1989 (1989-02-13), pages 638-640, XP000048508 ISSN: 0003-6951 column 638	27-29, 55,56
A	SZE S M: "METAL-SEMICONDUCTOR CONTACTS" PHYSICS OF SEMICONDUCTOR DEVICES, NEW YORK, JOHN WILEY & SONS, US, 1981, pages 245-311, XP002068071 ISBN: 0-471-05661-8 page 304 -page 306; figures 43,44	1-61
A	US 4 056 642 A (SAXENA ARJUN N ET AL) 1 November 1977 (1977-11-01) column 5, line 59 -column 6, line 28	1-61
A	PORTER L M ET AL: "A critical review of ohmic and rectifying contacts for silicon carbide" MATERIALS SCIENCE AND ENGINEERING B, ELSEVIER SEQUOIA, LAUSANNE, CH, vol. 34, no. 2, 1 November 1995 (1995-11-01), pages 83-105, XP004000935 ISSN: 0921-5107 page 100, right-hand column -page 102	1-61

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US 03/25054

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			JP	52139366 A	21-11-1977
			NL	7705316 A	16-11-1977

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/25057

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/78 H01L21/336 H01L29/49 H01L29/45 H01L29/51

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, COMPENDEX, INSPEC, IBM-TDB

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X	US 5 021 365 A (WARREN ALAN C ET AL) 4 June 1991 (1991-06-04) column 5, line 64 -column 6, line 49; figures 2,4,9	1-45
X	EP 0 295 490 A (IBM) 21 December 1988 (1988-12-21) column 5, line 19 -column 6, line 24; figures 2-5	1-45

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 November 2003	18/12/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Berthold, K

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/25057

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	EP 0 789 388 A (AGENCY IND SCIENCE TECHN) 13 August 1997 (1997-08-13) page 8, line 37 -page 11, line 40; figures 6,7 ---	1-45
Y	SZE S M: "METAL-SEMICONDUCTOR CONTACTS" PHYSICS OF SEMICONDUCTOR DEVICES, NEW YORK, JOHN WILEY & SONS, US, 1981, pages 245-311, XP002068071 ISBN: 0-471-05661-8 page 304 -page 306; figures 43,44 ---	1-45
A	TERAJI T ET AL: "OHMIC CONTACTS TO N.TYPE 6H.SIC WITHOUT POST-ANNEALING" MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS, MATERIALS RESEARCH SOCIETY, PITTSBURG, PA, US, 8 April 1996 (1996-04-08), pages 149-154, XP002068069 ISSN: 0272-9172 page 150 -page 153 ---	1-45
A	BANNIKOV V S ET AL: "FIELD-EFFECT TRANSISTOR WITH METAL-(TUNNELING-INSULATOR)- SEMICONSUCTOR CONTACTS AND A GATE INSULATOR MADE OF A LANGMUIR-BLODGETT FILM" SOVIET TECHNICAL PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 15, no. 3, 1 March 1989 (1989-03-01), pages 211-212, XP000102701 the whole document ---	1,17,34
A	US 5 801 398 A (HEBIGUCHI HIROYUKI) 1 September 1998 (1998-09-01) cited in the application page 11, line 18 -page 11, line 40; figures 7-14 ---	18
A	PORTER L M ET AL: "A critical review of ohmic and rectifying contacts for silicon carbide" MATERIALS SCIENCE AND ENGINEERING B, ELSEVIER SEQUOIA, LAUSANNE, CH, vol. 34, no. 2, 1 November 1995 (1995-11-01), pages 83-105, XP004000935 ISSN: 0921-5107 page 88, left-hand column, paragraph 2 --- -/--	1-45

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/25057

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	HARA S ET AL: "PINNING-CONTROLLED METAL/SEMICONDUCTOR INTERFACES" PROCEEDINGS OF THE SPIE, SPIE, BELLINGHAM, VA, US, vol. 2779, 3 June 1996 (1996-06-03), pages 802-806, XP002068070 ISSN: 0277-786X page 803 ---	1-45
A	US 2002/061646 A1 (NARAYANAN VENKATASUBRAMAN ET AL) 23 May 2002 (2002-05-23) paragraph '0002! - paragraph '0004! -----	1-45

Form PCT/ISA/210 (continuation of second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US 03/25057

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 3983264	A	28-09-1976	NONE		
US 5021365	A	04-06-1991	US	4843450 A	27-06-1989
			EP	0249768 A2	23-12-1987
			JP	62299077 A	26-12-1987
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US 5801398	A	01-09-1998	JP	2938351 B2	23-08-1999
			JP	8116060 A	07-05-1996
US 2002061646	A1	23-05-2002	WO	02089178 A2	07-11-2002
			US	2002192949 A1	19-12-2002

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/030209

A. CLASSIFICATION OF SUBJECT MATTER
H01L21/336 H01L29/786

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2004/142524 A1 (GRUPP DANIEL E ET AL) 22 July 2004 (2004-07-22) figures 4,5	1-6, 10-46 7-9
X	US 5 943 575 A (CHUNG ET AL) 24 August 1999 (1999-08-24) figure 3	1-3
X	US 6 091 076 A (DELEONIBUS ET AL) 18 July 2000 (2000-07-18) paragraph '0061!; figures 9,14	1-3

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 February 2006	02/03/2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Juhl, A

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2005/030209

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004142524 A1	22-07-2004	AU 2003255257 A1	25-02-2004
		CN 1675778 A	28-09-2005
		EP 1535343 A1	01-06-2005
		JP 2005536047 T	24-11-2005
		WO 2004015782 A1	19-02-2004
US 5943575 A	24-08-1999	JP 3094293 B2	03-10-2000
		JP 11330454 A	30-11-1999
		KR 261170 B1	01-07-2000
US 6091076 A	18-07-2000	DE 69715802 D1	31-10-2002
		DE 69715802 T2	15-05-2003
		EP 0852814 A1	15-07-1998
		FR 2749977 A1	19-12-1997
		WO 9748135 A1	18-12-1997
		JP 11510967 T	21-09-1999

PATENT COOPERATION TREATY

REC'D 28 FEB 2006
WIPO PCT

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

see form PCT/ISA/220

PT04

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY
(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)* see form PCT/ISA/210 (second sheet)	
Applicant's or agent's file reference see form PCT/ISA/220	**FOR FURTHER ACTION** See paragraph 2 below
International application No. PCT/US2005/030209	International filing date *(day/month/year)* 24.08.2005
Priority date *(day/month/year)* 26.08.2004	
International Patent Classification (IPC) or both national classification and IPC H01L21/336, H01L29/786	
Applicant ACORN TECHNOLOGIES, INC.	

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☒ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will usually be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA"). However, this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notifed the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of three months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA: European Patent Office - Gitschiner Str. 103 D-10958 Berlin Tel. +49 30 25901 - 0 Fax: +49 30 25901 - 840	Authorized Officer Juhl, A Telephone No. +49 30 25901-768

Form (PCT/ISA/237) (Cover Sheet) (January 2004)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US2005/030209

Box No. I Basis of the opinion

1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This opinion has been established on the basis of a translation from the original language into the following language , which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material:

   ☐ a sequence listing

   ☐ table(s) related to the sequence listing

   b. format of material:

   ☐ in written format

   ☐ in computer readable form

   c. time of filing/furnishing:

   ☐ contained in the international application as filed.

   ☐ filed together with the international application in computer readable form.

   ☐ furnished subsequently to this Authority for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

Box No. II Priority

1. ☒ The validity of the priority claim has not been considered because the International Searching Authority does not have in its possession a copy of the earlier application whose priority has been claimed or, where required, a translation of that earlier application. This opinion has nevertheless been established on the assumption that the relevant date (Rules 43*bis*.1 and 64.1) is the claimed priority date.

2. ☐ This opinion has been established as if no priority had been claimed due to the fact that the priority claim has been found invalid (Rules 43*bis*.1 and 64.1). Thus for the purposes of this opinion, the international filing date indicated above is considered to be the relevant date.

3. Additional observations, if necessary:

Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	6-10,22-28,30-36,38-46
	No:	Claims	1-5,11-21,29,37
Inventive step (IS)	Yes:	Claims	7-9
	No:	Claims	1-6,10-46
Industrial applicability (IA)	Yes:	Claims	1-46
	No:	Claims	

2. Citations and explanations

see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Reference is made to the following document:

D1 = US-2004/0142524 (D.E. Grupp et al.) (22 July 2004).

2. The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of claims 1-5,11-21,29,37 is not new in the sense of Article 33(2) PCT.

2.1 The document D1 discloses(cf. Figs.4,5 and corresponding text) a method comprising a gate (450), creating a recess (Fig.4D) and depositing a source/drain conducting material (494) in the recess (cf. Fig.4I); relevant to claims 1-3,11-21,29,37.

2.2 In D1 a seed layer (472F;474F) (cf. Fig.4F; § [0055]) is used to selectively deposit the source/drain material; relevant to claim 4.

2.3 In particular passivation layers (482;484) are selectively deposited within the recess (cf. Fig.4H); relevant to claim 4.

3. The additional subject matter of dependent claims 6,10,22-28,30-36,38-46 is well known in the field of TFT technology and cannot contribute to inventive step (Article 33(3) PCT).

4. It would appear that the subject matter of claims 7-9 is not suggested the available prior art.

GF Exhibit 1012 - 347/439

Electronic Patent Application Fee Transmittal

Application Number:	13552556
Filing Date:	18-Jul-2012
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Filer:	Tarek N. Fahmi/Sarah Zizzo
Attorney Docket Number:	3771-0003-DC3

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 1 month with $0 paid	2251	1	100	100
Miscellaneous:				
RCE- 2nd and Subsequent Request	2820	1	850	850
		Total in USD ($)		**950**

Electronic Acknowledgement Receipt

EFS ID:	21589482
Application Number:	13552556
International Application Number:	
Confirmation Number:	8045
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC3
Receipt Date:	24-FEB-2015
Filing Date:	18-JUL-2012
Time Stamp:	18:38:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$950
RAM confirmation Number	5193
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	3771-0003-DC3_RCE_filed_2-24-15.pdf	697804 4bb9c30811bedf56244446f322ae769fa08a872c	no	3
Warnings:					
Information:					
2		3771-0003-DC3_Amend_filed_2-24-15.pdf	111997 3002559313c3ee3def948e056c99a3797d420178	yes	5
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Amendment Submitted/Entered with Filing of CPA/RCE		1	1	
	Claims		2	4	
	Applicant Arguments/Remarks Made in an Amendment		5	5	
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	3771-0003-DC3_IDS_filed_2-24-15.pdf	616570 c3aacaaf79afd2921b0e6f97cc9b14574d873a00	no	10
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4	Foreign Reference	EP0789388A2.pdf	1286148 eb21f9223882fbd756db487a4d009a7deed93325	no	29
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Information:					
5	Foreign Reference	WO2004015782.pdf	1746183 5118345633460 21a9a8e3ad1b3c77a4a739b9c7a	no	38
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Information:					
6	Foreign Reference	WO2004030104.pdf	1946665 8e86a92c4397b67d343674297b80f6272d6bbb08	no	41

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Information:					
7	Non Patent Literature	ISR_12-18-03_PCTUS0325057.pdf	148419 e6b41e4f822e053dda03e415228eec268272b6e3	no	4
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Information:					
8	Non Patent Literature	ISR_WO_3-2-06_PCTUS0530209.pdf	228679 c36a652b30aa430000db5eba847a34102163a8c0	no	6
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Information:					
9	Non Patent Literature	ABOELFOTOH_1989.pdf	701772 e625ef20b52aef2eafa3f0c0c4b17af3eb746c1d	no	9
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Information:					
10	Non Patent Literature	BANNIKOV_1989.pdf	167912 f396b0ab8963ef3c1d13998aec341cce0fb89ff8	no	2
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Information:					
11	Non Patent Literature	BLOSSE_2004.pdf	495453 5c8cf3799fc7086620895779febcac35653770e6	no	7
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12	Non Patent Literature	CARD_1971.pdf	1068378 2eee1e7d39692c293c9300822cdf0ea9777cec9e	no	13
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13	Non Patent Literature	Chaneliere.pdf	299200 ed1ed60b28b25c7b702f6e44354c906d855fc680	no	4
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14	Non Patent Literature	CONNELLY_2003.pdf	316577 d549c7804c9c4d61a9e20166329f664a7d60c7c7	no	3
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15	Non Patent Literature	EDELSTEIN_1997.pdf	617003 bb894ecd9e12845a480ce7705d4fb81193ffb300	no	4

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17	Non Patent Literature	HAYAFUJI_1982.pdf	683467 870cee79e02ca02c796315be39c6d086bf7e3883	no	7
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19	Non Patent Literature	KEDZIERSKI_2003.pdf	633817 fd22971f65b550e0ce4d43aae1b6508dbac7cfc7	no	7
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20	Non Patent Literature	KELLER_1992.pdf	558589 b0769e22b1b4b5c9901ef30fe1bfda3510a5f431	no	6
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Information:					
21	Non Patent Literature	KIM_1997.pdf	391579 36a61e29fd1f778f18124e105ce6fff95588438b	no	5
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Information:					
22	Non Patent Literature	MARTEL_2001.pdf	428646 e54cd12257b30a461bcc1f444ba84d59da973a44	no	5
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23	Non Patent Literature	PARK_1991.pdf	688386 f7f98cc5dcf63ececc0688d29c2bc469788888ac	no	5
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24	Non Patent Literature	RUZYLLO_2004.pdf	907374 a70f00a29907d930054bcb3cc83474d075f35f03	no	3

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28	Non Patent Literature	TAO_2004.pdf	335433 68f7919c91a4538e1405a3d1bc7c34ad43f96b90	no	4
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29	Non Patent Literature	TAUBENBLATT_1984.pdf	332531 fc8a9e796ee8fb56343c8571227722b556ad530e	no	3
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30	Non Patent Literature	THANAILAKIS_1976.pdf	548894 d8b510f90a25647f277edfdb4831a0aae5650b15	no	7
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31	Non Patent Literature	THOMSON_2004.pdf	310866 bef09afb5070e811af59db75dfe95a9a681599f4	no	3
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32	Non Patent Literature	UDESHI_2004.pdf	275553 e74ac2043eea5677abec375eaf521952360424c7	no	4
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34	Non Patent Literature	WANG_1996.pdf	188993 338fb7eb751e1dfffa2b36e7ef56b10c6f4a6fa6	no	3
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35	Non Patent Literature	WEI_1988.pdf	405291 4f59d1a6a4b2ca71ee97b8807d8eff8df61326e6	no	4
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36	Non Patent Literature	WIDJAJA_2000.pdf	637393 196628f01f2e9d30a636c1caa299122408a90245	no	7
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41	Non Patent Literature	ZHU_2005.pdf	324245 99c3e05c5285763258b4f7989fd524302450a3bb	no	4
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Warnings:					
Information:					
			Total Files Size (in bytes):	24257729	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	13552556
Filing Date	18-Jul-2012
First Named Inventor	Daniel Grupp
Attorney Docket Number	3771-0003-DC3
Title of Invention	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
ACORN TECHNOLOGIES, INC.	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

8766336

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

○	I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

◉ Small Entity

○ Micro Entity

○ Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

◉ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

Registration Number 41402

○ A sole inventor

○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application

○ A joint inventor; all of whom are signing this request

Signature	/Tarek N. Fahmi/
Name	Tarek N. Fahmi

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	13552556
Filing Date:	18-Jul-2012
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Filer:	Tarek N. Fahmi/Sarah Zizzo
Attorney Docket Number:	3771-0003-DC3

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Statutory or Terminal Disclaimer	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**160**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 13552556

Filing Date: 18-Jul-2012

Applicant/Patent under Reexamination: Grupp et al.

Electronic Terminal Disclaimer filed on February 24, 2015

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	21589592
Application Number:	13552556
International Application Number:	
Confirmation Number:	8045
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC3
Receipt Date:	24-FEB-2015
Filing Date:	18-JUL-2012
Time Stamp:	18:49:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$160
RAM confirmation Number	5282
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Electronic Terminal Disclaimer-Filed	eTerminal-Disclaimer.pdf	33463 3a0f9f22f5461083cd23e59ccba28e7320b60d48	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30508 7b326302af386dcbc5209f25436bd0f56d74c82a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	63971		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/552,556	Filing Date 07/18/2012	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	02/24/2015	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $40 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $210 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**0**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/LAJUAN HICKSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13552556
	Filing Date	2012-07-18
	First Named Inventor	Daniel E. Grupp
	Art Unit	2896
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC3

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6724068		2004-04-20	MATSUYAMA	
	2	8110877		2012-02-07	MUKHERJEE; et al.	
	3	8952541		2015-02-10	MUKHERJEE; et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

EFS Web 2.1.17

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13552556
	Filing Date	2012-07-18
	First Named Inventor	Daniel E. Grupp
	Art Unit	2896
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC3

If you wish to add additional Foreign Patent Document citation information please click the Add button Add			
NON-PATENT LITERATURE DOCUMENTS Remove			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐
If you wish to add additional non-patent literature document citation information please click the Add button Add			

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13552556
	Filing Date	2012-07-18
	First Named Inventor	Daniel E. Grupp
	Art Unit	2896
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2015-05-13
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	22332961
Application Number:	13552556
International Application Number:	
Confirmation Number:	8045
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC3
Receipt Date:	13-MAY-2015
Filing Date:	18-JUL-2012
Time Stamp:	12:32:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	3771-0003-DC3_IDS_filed_5-13-15.pdf	612263 8f7f38e86725f75c588155d7e9395d2bc6ce3e5b	no	4

Warnings:	
Information:	

Total Files Size (in bytes):	612263

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13552556
	Filing Date	2012-07-18
	First Named Inventor	Daniel E. Grupp
	Art Unit	2896
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC3

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6724088		2004-04-20	JAMMY; et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13552556
	Filing Date	2012-07-18
	First Named Inventor	Daniel E. Grupp
	Art Unit	2896
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC3

	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13552556
	Filing Date	2012-07-18
	First Named Inventor	Daniel E. Grupp
	Art Unit	2896
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2015-06-19
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	22689138
Application Number:	13552556
International Application Number:	
Confirmation Number:	8045
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC3
Receipt Date:	19-JUN-2015
Filing Date:	18-JUL-2012
Time Stamp:	17:15:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	3771-0003-DC3_IDS_filed_6-19-15.pdf	612154 3ecf252dfbd768d24b7154851e63df9b43041791	no	4

Warnings:	
Information:	

Total Files Size (in bytes):	612154

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 13/552,556

First Named Inventor: Daniel E. Grupp

Filed: July 18, 2012

Art unit: 2896

Examiner: Harrison, Monica D.

Docket No.: 3771-0003-DC3

Confirmation No.: 8045

Commissioner for Patents
P.O. Box 1450
Alexandria VA, 22313-1450

AMENDMENT

Dear Commissioner:

Reconsideration of this application in view of the following amendments is respectfully requested.

Amendments to the Specification begins on page 2.

Remarks begin on page 3.

Amendments to the Specification

Page 1, paragraph **[0001]**, please amend as follows:

[0001] The present application is a CONTINUATION of co-pending U.S. Patent Application No. 13/022,522, filed 2/7/2011, which is a DIVISIONAL of U.S. Patent Application ~~12/197,966~~ 12/197,996, filed 8/25/2008, now U.S. Patent 7,884,003, which is a DIVISIONAL of U.S. Patent Application 11/181,217, filed 7/13/2005, now U.S. Patent 7,462,860, which is a CONTINUATION of U.S. Patent Application 10/217,758, filed 8/12/2002, now U.S. Patent 7,084,423, which is related to U.S. Patent Application 10/342,576, filed 1/14/2003, now U.S. Patent 6,833,556, all of which are hereby incorporated by reference.

GF Exhibit 1012 - 378/439

REMARKS

Reconsideration of this application, as amended, is respectfully requested. The specification has been amended to correct a typographical error in the related applications information. No new matter has been added.

If there are any additional fees due in connection with this communication, please charge Deposit Account No. 50-5798.

Respectfully submitted,
Ascenda Law Group, PC

Dated: August 28, 2015

/Tarek N. Fahmi/
Tarek N. Fahmi
Reg. No. 41,402

333 W San Carlos, St., Ste. 200
San Jose, CA 95110
(866) 877-4883

GF Exhibit 1012 - 379/439

Electronic Acknowledgement Receipt

EFS ID:	23348877
Application Number:	13552556
International Application Number:	
Confirmation Number:	8045
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC3
Receipt Date:	28-AUG-2015
Filing Date:	18-JUL-2012
Time Stamp:	19:29:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		3771-0003-DC3_Amendment_filed_8-28-15.pdf	84978 cbd4e5078e11af48e5feb2cd3a4c5bded79ae9d5	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Supplemental Response or Supplemental Amendment	1	1
	Specification	2	2
	Applicant Arguments/Remarks Made in an Amendment	3	3
Warnings:			
Information:			
	Total Files Size (in bytes):	84978	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
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National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

CORRECTED
NOTICE OF ALLOWANCE AND FEE(S) DUE

27571 7590 04/26/2016

Ascenda Law Group, PC
333 W San Carlos St.
Suite 200
San Jose, CA 95110

EXAMINER
HARRISON, MONICA D

ART UNIT	PAPER NUMBER
2896	

DATE MAILED: 04/26/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/552,556	07/18/2012	Daniel E. Grupp	3771-0003-DC3	8045

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	07/26/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

GF Exhibit 1012 - 382/439

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27571 7590 04/26/2016

Ascenda Law Group, PC
333 W San Carlos St.
Suite 200
San Jose, CA 95110

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/552,556	07/18/2012	Daniel E. Grupp	3771-0003-DC3	8045

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	07/26/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
HARRISON, MONICA D	2896	257-288000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

GF Exhibit 1012 - 383/439

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/552,556	07/18/2012	Daniel E. Grupp	3771-0003-DC3	8045

27571 7590 04/26/2016

Ascenda Law Group, PC
333 W San Carlos St.
Suite 200
San Jose, CA 95110

EXAMINER	
HARRISON, MONICA D	

ART UNIT	PAPER NUMBER
2896	

DATE MAILED: 04/26/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

GF Exhibit 1012 - 384/439

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/552,556	Applicant(s) GRUPP ET AL.	
	Examiner Monica D. Harrison	Art Unit 2896	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *2/24/15*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-8,10-16 and 19-21*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/Monica D. Harrison/
Primary Examiner, Art Unit 2896

GF Exhibit 1012 - 386/439

Continuation of Attachment(s) 2. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 2/24/15, 5/13/15 and 6/19/15.

GF Exhibit 1012 - 387/439

The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

1. Applicant's request for continued examination filed 2/24/15 has been entered. Claims 9, 17 and 18 are cancelled.

Terminal Disclaimer

2. The terminal disclaimer filed on 2/24/15 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of 8,766,366 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Allowable Subject Matter

3. Claims 1-8, 10-16 and 19-21 are allowed over the prior art of record.

Reasons for Allowance

4. The following is an examiner's statement of reasons for allowance:

After consideration of applicant's arguments, amendments, approval of applicant's terminal disclaimer and a further search of the prior art of record, examiner has concluded that the prior art does not disclose nor fairly suggest an electrical junction comprising: the interface layer comprising arsenic and configured to reduce a height of a Schottky barrier between the conductor and the semiconductor from that which would exist at a junction between the conductor and the semiconductor without the interface layer disposed there between, and wherein the electrical junction has a specific contact resistance of less than or equal to approximately $100\Omega\text{-}\mu m^2$ (claim 1), a field effect transistor comprising: wherein the source comprises a material having a work function substantially equal to a conduction band energy of the semiconductor channel region (claim 10) nor an electrical junction comprising: the interface

layer comprising arsenic and a titanium oxide (claim 21) as described in the independent claims and in the context of their recited apparatus' along with their depending claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica D. Harrison whose telephone number is (571)272-1959. The examiner can normally be reached on M-F 7:00am-3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Such can be reached on 571-272-8895. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Monica D. Harrison/
Primary Examiner, Art Unit 2896

mdh
April 14, 2016

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	13552556
Filing Date	2012-07-18
First Named Inventor	Daniel E. Grupp
Art Unit	2896
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC3

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/M.D.H./	1	6724088		2004-04-20	JAMMY; et al.	

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	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC3

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EXAMINER SIGNATURE

Examiner Signature	/Monica D. Harrison/	Date Considered	04/14/2016

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2015-06-19
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13552556	GRUPP ET AL.
	Examiner	**Art Unit**
	MONICA D HARRISON	2896

CPC						
Symbol					**Type**	**Version**
H01L		29	/	45	F	2013-01-01
H01L		21	/	28537	I	2013-01-01
H01L		29	/	0895	I	2013-01-01
H01L		29	/	456	I	2013-01-01
H01L		29	/	47	I	2013-01-01
H01L		29	/	66143	I	2013-01-01
H01L		29	/	78	I	2013-01-01
H01L		29	/	7839	A	2013-01-01
H01L		29	/	785	A	2013-01-01
H01L		29	/	812	I	2013-01-01
H01L		29	/	16	I	2013-01-01
H01L		29	/	161	I	2013-01-01
H01L		29	/	66643	I	2013-01-01
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Symbol				**Type**	**Set**	**Ranking**	**Version**
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(Assistant Examiner)	(Date)	**Total Claims Allowed:** 18	
/MONICA D HARRISON/ Primary Examiner.Art Unit 2896	04/14/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5, 7D

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	MONICA D HARRISON	2896

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
257	288	H	0	1	L	29 / 78 (2006.01.01)						
CROSS REFERENCE(S)		H	0	1	L	21 / 82 (2006.01.01)						

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	E21.192	E29.148			

(Assistant Examiner)	(Date)	Total Claims Allowed: 18	
/MONICA D HARRISON/ Primary Examiner.Art Unit 2896	04/14/2016	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5, 7D

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	Examiner	**Art Unit**
	MONICA D HARRISON	2896

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1		17												
2	2		18												
3	3	9	19												
4	4	10	20												
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13552556	GRUPP ET AL.
	Examiner	Art Unit
	MONICA D HARRISON	2896

CPC- SEARCHED		
Symbol	Date	Examiner
H01L29/6659,7833,665,6656	4/14/16	MDH

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	30-35,56,62,65,288,471-475,483	9/25/12	MDH
257	288,E29.255	4/4/13	MDH
257	486,E21.192,E29.148	11/26/13	MDH

SEARCH NOTES		
Search Notes	Date	Examiner
East (USPAT, US-PGPUB, USOCR, EPO, JPO, DERWENT, IBM_TDB, FPRS)	9/25/12	MDH
GRUPP et al. .inv.	9/25/12	MDH
East updated	4/4/13	MDH
East updated	11/26/13	MDH
GRUPP et al. .inv.	11/26/13	MDH
USPAT, US-PGPUB, UPAD txt .clm.	11/26/13	MDH
East updated	2/19/14	MDH
East updated	9/22/14	MDH
East updated	4/14/16	MDH

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US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
	USPAT, US-PGPUB, UPAD txt .clm.	4/14/16	MDH

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	2	4019113		1977-04-19	HARTMAN	
	3	4422090		1983-12-20	SHEPHERD; et al.	
	4	4583110		1986-04-15	JACKSON; et al.	
	5	4723197		1988-02-02	TAKIAR; et al.	
	6	4811077		1969-03-07	FOWLER; et al.	
	7	5027166		1991-06-25	OHTSUKA; et al.	
	8	5098859		1992-03-24	JACKSON; et al.	

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/M.D.H./	9	5308998		1994-05-03	YAMAZAKI; et al.	
	10	5438210		1995-08-01	WORLEY	
	11	5908313		1999-06-01	CHAU; et al.	
	12	5943575		1999-08-24	CHUNG; et al.	
	13	6064082		2000-05-16	KAWAI; et al.	
	14	6071783		2000-06-06	LIANG; et al.	
	15	6091076		2000-07-18	DELEONIBUS; et al.	
	16	6117781		2000-09-12	LUKANC; et al.	
	17	6291282		2001-09-18	WILK; et al.	
	18	6293137		2001-09-25	LIU; et al.	
	19	6326294		2001-12-04	JANG HA SOON; et al.	

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/M.D.H./	20	6339232		2002-01-15	TAKAGI	
	21	6452244		2002-09-17	MIURA; et al.	
	22	6462931		2002-10-08	TANG; et al.	
	23	6548875		2003-04-15	NISHIYAMA	
	24	6680224		2004-01-20	SHIN; et al.	
	25	5943575		1999-08-24	CHUNG; et al.	

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/M.D.H./	1	20010028067		2001-10-11	AWANO	
	2	20020061646		2002-05-22	KAN; et al.	
	3	20030009463		2003-01-09	GALLANT	

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/M.D.H./	4	20030012146		2003-01-16	NOVAES		
	5	20030127700		2003-07-10	MODDEL; et al.		
	6	20030132466		2003-07-17	SHIN; et al.		
	7	20030235936		2003-12-25	SNYDER; et al.		
	8	20040142524		2004-07-22	GRUPP; et al.		
	9	20050009302		2005-01-13	WAKUI; et al.		
	10	20050037557		2005-02-17	DOCZY; et al.		

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/M.D.H./	1	0789388	EP	A1	1997-08-13	AGENCY INDUSTRIAL SCIENCE AND TECHNOLOGY		☐
/M.D.H./	2	2004/015782	WO	A1	2004-02-19	ACORN TECHNOLOGIES, INC.		☐

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/M.D.H./	3	2004/030104	WO	A1	2004-04-08	ACORN TECHNOLOGIES, INC.		☐

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/M.D.H./	1	"International Search Report and Written Opinion of the International Searching Authority", Patent Cooperation Treaty (02 March 2006), PCT/US2005/030209, 6 pgs.	☐
	2	"International Search Report", Patent Cooperation Treaty (18 December 2003), PCT/US03/25057, 4 pgs.	☐
	3	ABOELFOTOH, "Influence of thin interfacial silicon oxide layers on the Schottky-barrier behavior of Ti on Si(100)", Phys Rev B Condens Matter (Mar. 1989), 39(8):5070-5078.	☐
	4	BANNIKOV; et al., "Field-Effect Transistor With Metal-(Tunneling-Insulator)-Semiconductor Contacts and a Gate Insulator Made of A Mangmuir-Blodgett Film", Soviet Technical Physics Letters (Mar. 1989), 15(3):211-212.	☐
	5	BLOSSE; et al., "A Novel Low Cost 65nm CMOS Process Architecture With Self Aligned Isolation and W Cladded Source/Drain", IEEE, Transactions of 2004 International Electron Device Meeting (Jan. 2005), pp. 669-672.	☐
	6	CARD; et al., "Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes", Journal of Physics D: Applied Physics (1971), 4(10):1589-1601.	☐
	7	CHANELIERE; et al., "Tantalum Pentoxide (Ta2O5) Thin Films for Advanced Dielectric Applications"; Materials Science and Engineering, R: Reports (May 1998), 22(6):269-322.	☐
	8	CONNELLY; et al., "Optimizing Schottky S/D Offset for 25-nm Dual-Gate CMOS Performance", Electron Device Letters, IEEE (Jun. 2003), 24(6)411-413.	☐

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/M.D.H./	9	EDELSTEIN; et al., "Full Copper Wiring in a Sub-0.25 mm CMOS ULSI Technology", Proceedings of the IEEE International Electron Device Meeting (1997), pp. 773-776.	☐
	10	GOPALAKRISHNAN; et al., "Impact Ionization MOS (I-MOS)-Part I: Device and Circuit Simulations", IEEE Transactions Electron Devices (Jan. 2005), 52(1):69-76.	☐
	11	HAYAFUJI; et al., "Nitridation of Silicon and Oxidized-Silicon", J. Electrochem. Soc. (1982), 129(9):2102-2108.	☐
	12	KAXIRAS, "Efthimios. Semiconductor-surface restoration by valence-mending adsorbates: Application to Si (100): S and Si (100): Se", Phys Rev B Condens Matter (Mar. 1991), 43(18):6824-6827.	☐
	13	KEDZIERSKI; et al., "Extension and Source/Drain Design for High-Performance FinFET Devices", IEEE Trans. Electron Devices (Apr. 2003), 50(4):952-958.	☐
	14	KELLER; et al., "Calculations of the barrier height and charge distribution of a metal-dielectric interface", Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films (Jul. 1992), 10(4):775-780.	☐
	15	KIM; et al., "Metal-Dependent Fermi-Level Movement in The Metal/Sulfer-Passivated InGaP Contact", Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films (1997), 15(3):1124-1128.	☐
	16	MARTEL; et al., "Ambipolar Single-Wall Carbon Nanotube Transistors and Inverters", AIP Conference Proceedings (Mar. 2001). 591:543-547.	☐
	17	PARK; et al., "Thermal stability of molybdenum-silicon nitride-silicon Schottky diodes", Journal of Applied Physics (Mar. 1991), 69(5):3149-3153.	☐
	18	RUZYLLO; et al., "Semiconductor Glossary An Introduction to Semiconductor Terminology", Prosto Multimedia Publishing (2004), pp. 26.	☐
	19	SOBOLEWSKI; et al., "Studies of barrier height mechanisms in metal-silicon nitride-silicon Schottky barrier diodes", Journal of Vacuum Science & Technology B (1989), 7:971-979.	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13552556
	Filing Date	2012-07-18
	First Named Inventor	Daniel E. Grupp
	Art Unit	2896
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC3

/M.D.H./	20	TAKAHAGI; et al., "The formation of hydrogen passivated silicon singlecrystal surfaces using ultraviolet cleaning and HF etching", J Appl Phys (1988), 64(7):3516-21.	☐
	21	TAO; et al., "Removal of dangling bonds and surface states on silicon (001) with a monolayer of selenium", Applied Physics Letters (Mar. 2003), 82(10)1559-1561.	☐
	22	TAO; et al., "Suppression of silicon (001) surface reactivity using a valence-mending technique", Solid State Communications (Oct. 2004), 132(2):89-92.	☐
	23	TAUBENBLATT; et al., "Interface effects in titanium and hafnium Schottky barriers on silicon", Appl Phys Lett (May 1984), 44:895-897.	☐
	24	THANAILAKIS; et al., "Transition-metal contacts to atomically clean silicon, Department of Electrical Engineering and Electronics", Journal of Physics C: Solid State Physics (1976), 9:337-343.	☐
	25	THOMPSON; et al., "A Logic Nanotechnology Featuring Strained-Silicon", IEEE Electron Device Letters (Apr. 2004),25 (4):191-193.	☐
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	27	UEMOTO, "Reduction of Ohmic Contact Resistance on N-Type 6H-SIC By Heavy Doping", Japanese Journal of Applied Physics (Jan. 1995), 34(Parts 2, Number 1A).	☐
	28	WANG; et al., "High Barrier GaN Schottky Diodes: Pt/GaN and Pd/GaN", Appl. Phys. Letters (Feb. 1996), 68 (9):1267-1270.	☐
	29	WEI; et al., "The Use of Selective Electroless Metal Deposition For Micron Size Contact Fill", IEEE International Electron Device Meeting Technical Digest (1988), pp. 446-449.	☐
	30	WIDJAJA; et al., "Ab Initio Study and Decomposition of NH3 on Si(100)-(2x1)", J. Phy. Chem B, (2000), 104:2527-2533.	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13552556
	Filing Date	2012-07-18
	First Named Inventor	Daniel E. Grupp
	Art Unit	2896
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC3

/M.D.H./	31	WITTMER; et al., "Ideal Schottky diodes on passivated silicon", Phys Rev Lett (Nov. 1992), 69(18):2701-2704.	☐
	32	WRIGHT; et al., "Hot-Electron Immunity of SiO2 Dielectrics with Fluorine Incorporation", IEEE Electron Device Letters (1989), 10(8):347-348.	☐
	33	YAGISHITA; et al., "High Performance Damascene Metal Gate MOSFET's for 0.1 mm Regime", IEEE Trans. Electron Devices (2000), 47(5):1028-1034.	☐
	34	YANG; et al., "The Effects of Interfacial Sub-Oxide Transition Regions and Monolayer Level Nitridation on Tunneling Currents in Silicon Devices", IEEE Electron Device Letters (2000), 21(2):76-78.	☐
	35	ZHU; et al., "Low-Resistance Ti/n-Type Si(100) Contacts by Monolayer Se Passivation", ECS Trans (2006), 2 (2):401-409.	☐
	36	ZHU; et al., "Stability of Se passivation layers on Si(001) surfaces characterized by time-of-flight positron annihilation induced Auger electron spectroscopy", Journal of Applied Physics (2005), 97(10):103510-1103510-4.	☐

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EXAMINER SIGNATURE

Examiner Signature	/Monica D. Harrison/	Date Considered	04/14/2016

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Application Number	13552556
	Filing Date	2012-07-18
	First Named Inventor	Daniel E. Grupp
	Art Unit	2896
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2015-02-24
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5	"13552556"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/14 15:00
L2	127	257/288,E29.255.ccls. and (conduct$4 metal) near9 arsenic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/14 15:08
L3	3	257/288,E29.255.ccls. and (conduct$4 metal) near9 arsenic and (conduct$4 metal) near9 (titanium near oxide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/14 15:08
L4	3	257/288,E29.255.ccls. and (conduct$4 metal) near9 arsenic and (conduct$4 metal) near9 (titanium near oxide) and (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/14 15:08
L5	0	H01L29/6659,7833,665,6656.cpc. and (conduct$4 metal) near9 arsenic and (conduct$4 metal) near9 (titanium near oxide) and (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/14 15:12
L6	22	H01L29/'$'.cpc. and (conduct$4 metal) near9 arsenic and (conduct$4 metal) near9 (titanium near oxide) and (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/14 15:12
L7	768	H01L29/6659,7833,665,6656.cpc. and transistor and source and drain and (channel near9 arsenic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/14 15:17
L8	2	H01L29/6659,7833,665,6656.cpc. and	US-PGPUB;	OR	ON	2016/04/14

		transistor and source and drain and (channel near9 arsenic)and (arsenic near interface)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			15:17
L9	35	H01L29/6659,7833,665,6656.cpc. and transistor and source and drain and (channel near9 arsenic)and (arsenic near (interface layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/14 15:20
L10	5	H01L29/6659,7833,665,6656.cpc. and transistor and source and drain and (channel near9 arsenic)and (arsenic near (interface layer film)) and (conduction near band) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/14 15:20
L11	9	H01L29/'$'.cpc. and transistor and source and drain and (channel near9 arsenic)and (arsenic near (interface layer film)) and (conduction near band) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/14 15:22
L12	9	transistor and source and drain and (channel near9 arsenic)and (arsenic near (interface layer film)) and (conduction near band) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/14 15:24
L13	1	transistor and source and drain and (channel near9 arsenic)and (arsenic near (interface layer film)) and (conduction near band) and (work near function)and (grupp connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/14 15:26
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L15	1	transistor and source and drain and (channel near9 arsenic)and (arsenic near (interface layer film)) and (conduction near band) and (work near function).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/04/14 15:47
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S2	1	13/022522	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:53
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S4	2	"7462860".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:54
S5	2	"7084423".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 10:55
S6	2	"6833556".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:00
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			DERWENT; IBM_TDB			
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S10	2609	(grupp connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:18
S11	25	(grupp connelly).inv. and arsenic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:18
S12	17	(grupp connelly).inv. and (arsenic with interface) and transistor	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:19
S13	8062	257/30-35,56,62,65,288,471-475,483.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:27
S14	123	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:27
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		(semiconductor silicon germanium gallium carbide)) and transistor	FPRS; EPO; JPO; DERWENT; IBM_TDB			
S17	74	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:29
S18	56	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:30
S19	56	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 11:30
S20	47	257/30-35,56,62,65,288,471-475,483.ccls. and (arsenic with (metal conduct$4)) and (arsenic with (semiconductor silicon germanium gallium carbide)) and transistor and source and drain and channel and gate and (semiconductor with silicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 12:15
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S23	150	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface) and (interface with metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:20
S24	225	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface) and (interface with semiconductor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:20

S25	5	257/30-35,56,62,65,288,471-475,483.ccls. and (conduct$4 with interface) and (interface with semiconductor) and (interface with arsenic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:21
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S31	2	(conduct$4 with interface) and (interface with semiconductor) and (interface near5 arsenic) and transistor and (semiconductor near5 silicon) and (semiconductor near5 germanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:23
S32	4222	257/30-35,56,62,65,288,471-475,483.ccls. and (substrate wafer semiconductor) near6 silicon	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/09/25 13:27
S33	901	257/30-35,56,62,65,288,471-475,483.ccls. and (substrate wafer semiconductor) near6 silicon and (substrate wafer semiconductor) near6 germanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2012/09/25 13:27

			DERWENT; IBM_TDB			
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S36	1	"13552556"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:47
S37	9867	257/288,E29.255.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:48
S38	0	257/288,E29.255.ccls. and (electrical near juction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:48
S39	16	257/288,E29.255.ccls. and (electrical near junction)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:48
S40	5	257/288,E29.255.ccls. and (electrical near junction) and (arsenic "Ar")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:49
S41	535	257/288,E29.255.ccls. and (gate electrode) with arsenic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:58
S42	218	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR;	OR	ON	2013/04/04 20:58

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S43	109	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and junction	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:58
S44	1	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and junction and (arsenic near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 20:59
S45	1	257/288,E29.255.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and junction and ((arsenic arsenide)near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 21:02
S46	1	257/288,E29.255.ccls. and (gate electrode) with (arsenic arsenide) and (arsenic with (substrate wafer carrier base plate)) and junction and ((arsenic arsenide)near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 21:02
S47	7	257/288,E29.255.ccls. and (gate electrode) with (arsenic arsenide) and ((arsenic arsenide) with (substrate wafer carrier base plate)) and junction and ((arsenic arsenide)near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 21:02
S48	70	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" | "7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:06
S49	39	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" |	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:07

		"7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As") with (gate electrode conduct$4 metal)				
S50	23	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" | "7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As") with (gate electrode conduct$4 metal) and (arsenic "As") with (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:08
S51	9	("3708360" | "6198113" | "20030121468" | "6011271" | "20040026687" | "5399206" | "5596218" | "5801444" | "5888891" | "6303479" | "4300152" | "4485550" | "5578848" | "5801398" | "3983264" | "20050093027" | "6037605" | "6261932" | "6608352" | "4056642" | "5021365" | "5663584" | "5939763" | "6150286" | "6207976" | "6291866" | "7084423" | "7176483" | "3590471" | "5612567" | "6096590" | "6291867").PN. and (arsenic "As") with (gate electrode conduct$4 metal) and (arsenic "As") with (substrate wafer carrier base plate) and (arsenic "As") with channel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:08
S52	4445	257/'$'.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:14
S53	177	257/'$'.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and (arsenic near (layer film))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:14
S54	29	257/'$'.ccls. and (gate electrode) with arsenic and (arsenic with (substrate wafer carrier base plate)) and (arsenic near (layer film)) and fet	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/04 22:15
S55	0	257/486,E21.192,E29.148.ccls. and arsenic near (conduct$4 metal)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2013/11/26 16:33

			EPO; JPO; DERWENT; IBM_TDB			
S56	11	257/486,E21.192,E29.148.ccls. and arsenic near9 (conduct$4 metal)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:33
S57	7	257/486,E21.192,E29.148.ccls. and arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:34
S58	1	257/486,E21.192,E29.148.ccls. and arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:35
S59	18	257/'$'.ccls. and arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:37
S60	25	arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:39
S61	0	arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky and (grupp connelly).inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:43
S62	3	arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/11/26 16:43
S64	2	"13552556"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 12:45
S65	2	"6380021".pn.	US-PGPUB; USPAT;	OR	ON	2014/02/18 12:46

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S66	12364	257/288,E29.255.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:23
S67	57	257/288,E29.255.ccls. and gate and source and drain and (LDD near7 arsenic)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:24
S68	36	257/288,E29.255.ccls. and gate and source and drain and (LDD near7 arsenic) and (silicide salicide) near7 (source drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:24
S69	22	257/288,E29.255.ccls. and gate and source and drain and (LDD near7 arsenic) and (silicide salicide) near7 (source drain) and germanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:37
S70	19	257/288,E29.255.ccls. and gate and source and drain and (LDD near4 arsenic) and (silicide salicide) near7 (source drain) and germanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:37
S71	5	"6608352".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:41
S72	0	257/288,E29.255.ccls. and gate and source and drain and (LDD near4 arsenic) and (metal near (silicide salicide)) near7 (source drain) and germanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:50
S73	1853	257/288,E29.255.ccls. and (metal near silicide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:50

S74	535	257/288,E29.255.ccls. and (metal near silicide) near7 (source drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:52
S75	535	257/288,E29.255.ccls. and (metal near silicide) near7 (source drain) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:55
S76	81	257/288,E29.255.ccls. and (metal near silicide) near7 (source drain) and gate and (arsenic with (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 13:58
S77	48	257/288,E29.255.ccls. and (metal near silicide) near7 (source drain) and gate and (arsenic with (source drain)) and (germanium "SiGe")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 14:16
S78	969	257/288,E29.255.ccls. and (germanium "SiGe") with channel	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 14:40
S79	962	257/288,E29.255.ccls. and (germanium "SiGe") with channel and (gate electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 14:40
S80	386	257/288,E29.255.ccls. and (germanium "SiGe") with channel and (gate electrode) and (silicide with (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/18 14:41
S81	1981	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:25
S82	161	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2014/02/19 10:27

			DERWENT; IBM_TDB			
S83	107	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:27
S84	107	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide and (gate electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:27
S85	32	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide and (gate electrode) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:28
S86	9	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide and (gate electrode) and (work near function) and (conduction near band)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:28
S87	32	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide and (gate electrode) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:29
S88	107	257/288,E29.255.ccls. and (germanium "SiGe") near9 (substrate wafer carrier base plate) and (arsenic near9 (substrate wafer carrier base plate)) and source and drain and silicide and (gate electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:32
S89	1132	257/288,E29.255.ccls. and germanium near9 (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near9 (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:37
S90	1104	257/288,E29.255.ccls. and germanium near9 (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near9 (substrate wafer carrier base plate) and (gate electrode)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:37
S91	99	257/288,E29.255.ccls. and germanium near9 (substrate wafer carrier base plate) and ("SiGe" (silicon near	US-PGPUB; USPAT; USOCR;	OR	ON	2014/02/19 10:37

		germanium)) near9 (substrate wafer carrier base plate) and (gate electrode) and (arsenic near9 (source drain))	FPRS; EPO; JPO; DERWENT; IBM_TDB			
S92	15	257/288,E29.255.ccls. and germanium near(substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near9 (substrate wafer carrier base plate) and (gate electrode) and (arsenic near9 (source drain))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:43
S93	169	257/288,E29.255.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:44
S94	164	257/288,E29.255.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate) and gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:44
S95	154	257/288,E29.255.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate) and gate and source and drain	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:44
S96	61	257/288,E29.255.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate) and gate and source and drain and arsenic	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:44
S97	3466	257/'$'.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:50
S98	229	257/'$'.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate) and (gate electrode) and source and drain and arsenic and (metal near silicide)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:50
S99	56	257/'$'.ccls. and germanium near (substrate wafer carrier base plate) and ("SiGe" (silicon near germanium)) near (substrate wafer carrier base plate) and (gate electrode) and source and drain and arsenic and (metal near silicide) and (work near function)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/02/19 10:51
S100	3	"13552556"	US-PGPUB;	OR	ON	2014/09/22

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			09:54
S101	6204	257/288.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/09/22 09:57
S102	2	"6380021".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/09/22 11:12

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S63	3	arsenic near9 (conduct$4 metal) and (arsenic near9 (semiconductor substrate silicon base wafer carrier germanium)) and arsenic with schottky.clm.	US-PGPUB; USPAT; * No UPAD	OR	ON	2013/11/26 16:48

4/14/2016 3:58:53 PM
C:\Users\mharrison1\Documents\EAST\Workspaces\13552556.wsp

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	13552556
Filing Date	2012-07-18
First Named Inventor	Daniel E. Grupp
Art Unit	2896
Examiner Name	Harrison, Monica D.
Attorney Docket Number	3771-0003-DC3

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
/M.D.H./	1	6724068		2004-04-20	MATSUYAMA	
/M.D.H./	2	8110877		2012-02-07	MUKHERJEE; et al.	
/M.D.H./	3	8952541		2015-02-10	MUKHERJEE; et al.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13552556
	Filing Date	2012-07-18
	First Named Inventor	Daniel E. Grupp
	Art Unit	2896
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC3

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Examiner Signature	/Monica D. Harrison/	Date Considered	04/14/2016

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Application Number	13552556
	Filing Date	2012-07-18
	First Named Inventor	Daniel E. Grupp
	Art Unit	2896
	Examiner Name	Harrison, Monica D.
	Attorney Docket Number	3771-0003-DC3

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Tarek N. Fahmi/	Date (YYYY-MM-DD)	2015-05-13
Name/Print	Tarek N. Fahmi	Registration Number	41402

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H./

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H./

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13552556	GRUPP ET AL.
	Examiner	**Art Unit**
	MONICA D HARRISON	2896

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/27/2012	04/05/2013	11/26/2013	09/22/2014	04/14/2016				
1	1	✓	✓	=	=	=				
2	2	✓	✓	=	=	=				
3	3	✓	✓	=	=	=				
4	4	✓	✓	=	=	=				
5	5	✓	✓	=	=	=				
6	6	✓	✓	=	=	=				
7	7	✓	✓	=	=	=				
8	8	✓	✓	=	=	=				
	9	✓	✓	-	-	-				
11	10	=	=	✓	=	=				
12	11	=	=	✓	=	=				
13	12	=	=	✓	=	=				
14	13	=	=	✓	=	=				
15	14	=	=	✓	=	=				
16	15	=	=	✓	=	=				
17	16	=	=	✓	=	=				
	17	=	=	O	O	-				
	18	=	=	✓	-	-				
9	19			=	=	=				
10	20			=	=	=				
18	21				✓	=				

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/552,556	07/18/2012	2896	530	3771-0003-DC3	18	3

CONFIRMATION NO. 8045

CORRECTED FILING RECEIPT

27571
Ascenda Law Group, PC
333 W San Carlos St.
Suite 200
San Jose, CA 95110



Date Mailed: 04/29/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Daniel E. Grupp, Palo Alto, CA;
Daniel J. Connelly, Redwood City, CA;

Applicant(s)

Daniel E. Grupp, Palo Alto, CA;
Daniel J. Connelly, Redwood City, CA;

Power of Attorney: The patent practitioners associated with Customer Number 27571

Domestic Priority data as claimed by applicant

This application is a CON of 13/022,522 02/07/2011 PAT 8431469
which is a DIV of 12/197,996 08/25/2008 PAT 7884003
which is a DIV of 11/181,217 07/13/2005 PAT 7462860
which is a CON of 10/217,758 08/12/2002 PAT 7084423

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 07/30/2012
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/552,556**
Projected Publication Date: Not Applicable
Non-Publication Request: No
Early Publication Request: No
**** SMALL ENTITY ****
Title

METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications:

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

27571 7590 04/26/2016

Ascenda Law Group, PC
333 W San Carlos St.
Suite 200
San Jose, CA 95110

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/552,556	07/18/2012	Daniel E. Grupp	3771-0003-DC3	8045

TITLE OF INVENTION: METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	07/26/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
HARRISON, MONICA D	2896	257-288000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Ascenda Law Group, PC
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Acorn Technologies, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): La Jolla, California

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.
☒ Payment by credit card. Form PTO-2038 is attached.
☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 50-5798 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Tarek N. Fahmi/ Date July 22, 2016

Typed or printed name Tarek N. Fahmi Registration No. 41,402

PTOL-85 Part B (10-13) Approved for use through 10/31/2013 OMB 0651-0033 U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

GF Exhibit 1012 - 433/439

Electronic Patent Application Fee Transmittal

Application Number:	13552556
Filing Date:	18-Jul-2012
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Filer:	Tarek N. Fahmi/Sarah Zizzo
Attorney Docket Number:	3771-0003-DC3

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	2501	1	480	480

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**480**

Electronic Acknowledgement Receipt

EFS ID:	26434883
Application Number:	13552556
International Application Number:	
Confirmation Number:	8045
Title of Invention:	METHOD FOR DEPINNING THE FERMI LEVEL OF A SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES INCORPORATING SUCH JUNCTIONS
First Named Inventor/Applicant Name:	Daniel E. Grupp
Customer Number:	27571
Filer:	Tarek N. Fahmi/Sarah Zizzo
Filer Authorized By:	Tarek N. Fahmi
Attorney Docket Number:	3771-0003-DC3
Receipt Date:	22-JUL-2016
Filing Date:	18-JUL-2012
Time Stamp:	17:43:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$480
RAM confirmation Number	4487
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2016-07-22_3771-0003-DC3_Issue_Fee.pdf	145743 6ad02a2ce2e28698db30ab4997e34dc230a0dbf9	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30521 2081669fadf7b18bcbbd0ea681882c35727f0967	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	176264		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Receipt date: 12/31/2012	Application Number	13552556	13552556 - GAU: 2896
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Filing Date	2012-07-18	
(Not for submission under 37 CFR 1.99)	First Named Inventor	Daniel E. Grupp	
	Art Unit	2896	
	Examiner Name	Harrison, Monica D.	
	Attorney Docket Number	40003771-0003-463	

/M.D.H./	9	5578848		1996-11-26	Kwong, et al.	
Change(s) applied to document, /S.X.R./ 5/6/2016	10	5596218		01/1997 ~~2009-04-18~~	Soleimani, et al.	
	11	5612567		1997-03-18	Baliga	
	12	5663584		1997-09-02	Welch	
	13	5801398		1998-09-01	Hebiguchi	
	14	5888891		1999-03-30	Gould	
	15	5939763		1999-08-17	Hao, et al.	
	16	6037605		2000-03-14	Yoshimura	
	17	6096590		2000-08-01	Chan, et al.	
	18	6150286		2000-11-21	Sun et al.	
	19	6198113		2001-03-06	Grupp, Daniel E.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /M.D.H

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/552,556	08/23/2016	9425277	3771-0003-DC3	8045

27571 7590 08/03/2016

Ascenda Law Group, PC
333 W San Carlos St.
Suite 200
San Jose, CA 95110

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 130 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Daniel E. Grupp, Palo Alto, CA;
Daniel J. Connelly, Redwood City, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.