

Petition for *Inter Partes* Review
U.S. Patent No. 10,090,395

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner

v.

ACORN SEMI, LLC,
Patent Owner

Case IPR2020-_____

U.S. Patent No. 10,090,395

Title: METHOD FOR DEPINNING THE FERMI LEVEL OF A
SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES
INCORPORATING SUCH JUNCTIONS

Issue Date: October 2, 2018

PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 10,090,395

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All citations to 35 U.S.C. §§ 102 and 112 in this paper refer to the pre-AIA statute unless otherwise noted.

All emphases are added unless otherwise noted.

This paper includes color illustrations and should be viewed in color.

PETITIONER'S EXHIBIT LIST

Petitioner Exhibit No.	DESCRIPTION
1001	U.S. Patent No. 10,090,395
1002	File History of U.S. Patent No. 7,084,423.
1003	U.S. Patent No. 7,084,423.
1004	File History of U.S. Patent No. 6,833,556.
1005	U.S. Patent No. 6,833,556.
1006	File History of U.S. Patent No. 7,462,860.
1007	U.S. Patent No. 7,462,860.
1008	File History of U.S. Patent No. 7,884,003.
1009	U.S. Patent No. 7,884,003.
1010	File History of U.S. Patent No. 8,431,469.
1011	U.S. Patent No. 8,431,469.
1012	File History of U.S. Patent No. 9,425,277.
1013	U.S. Patent No. 9,425,277.
1014	File History of U.S. Patent No. 9,905,691.
1015	U.S. Patent No. 9,905,691.
1016	File History of U.S. Patent No. 9,812,542
1017	U.S. Patent No. 9,812,542.
1018	File History of U.S. Patent No. 10,388,748.
1019	U.S. Patent No. 10,388,748.
1020	File History of U.S. Patent No. 10,090,395.
1021	U.S. Patent No. 7,176,483 (cited as "Grupp '483").
1022	Declaration of Dr. E. Fred Schubert (cited as "Schubert Decl.").
1023	E.H. Rhoderick, <i>Metal-semiconductor contacts</i> , 129 IEE REV. 1 (Feb. 1982) (cited as "Rhoderick").
1024	C.Y. Chang et al., <i>Specific contact resistance of metal-semiconductor barriers</i> , 15 SOLID STATE ELECS. 541 (1971) (cited as "Chang").
1025	S.M. Goodnick et al., <i>Effects of a thin SiO₂ layer on the formation of metal-silicon contacts</i> , 18 J. VAC. SCI. & TECH. 949 (Apr. 1981) (cited as "Goodnick").
1026	M.A. Sobolewski and C.R. Helms, <i>Studies of barrier height mechanisms in metal-silicon nitride-silicon Schottky barrier diodes</i> , J. VAC. SCI. & TECH. B 971 (Jul./Aug. 1989) (cited as "Sobolewski").
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1030	U.S. Patent No. 4,845,050 (cited as “Kim”).
1031	Japanese Laid-Open App. No. JPH11162874A (June 18, 1999).
1032	Certified Translation of Japanese Laid-Open App. No. JPH11162874A (June 18, 1999) (cited as “Iwaguro”).
1033	Gary P. Carver et al., <i>Specific Contact Resistivity of Metal-Semiconductor Contacts—A New, Accurate Method Linked to Spreading Resistance</i> , 35 IEEE TRANS. ELECTRON DEVICES 489 (Apr. 1988) (cited as “Carver”).
1034	Redline of Specification of U.S. Patent No. 7,176,483 Against Specification of U.S. Patent No. 7,084,423.
1035	N.D. Lang and W. Kohn, <i>Theory of Metal Surfaces: Work Function</i> , 3 PHYS. REV. B 1215 (1971) (cited as “Lang”).
1036	W. Zheng et al., <i>Electronic Structure Differences in ZrO₂ vs. HfO₂</i> , 109 J. PHYS. CHEM. A 109 (2005) (cited as “Zheng”).
1037	U.S. Patent App. Pub. No. 2014/0117465.
1038	Complaint in <i>Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.</i> , Case No. 2:19-cv-00347, ECF No. 1 (E.D. Tex. Oct. 23, 2019).
1039	Summons and Return of Service in <i>Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.</i> , No. 2:19-cv-00347, ECF No. 8 (E.D. Tex. Oct. 29, 2019).
1040	Second Amended Docket Control Order, <i>Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.</i> , No. 2:19-cv-00347, ECF No. 39 (E.D. Tex. Apr. 21, 2020).
1041	Cover Pleading to Acorn’s Preliminary Infringement Contentions in <i>Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.</i> , No. 2:19-cv-00347 (Mar. 9, 2020).
1042	Exhibit F to Acorn’s Preliminary Infringement Contentions in <i>Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.</i> , No. 2:19-cv-00347 (Mar. 9, 2020).

All citations to specific pages of exhibits follow the pagination added to those exhibits per 37 C.F.R. § 42.63(d)(2)(i).

I. Introduction

Petitioner Samsung Electronics Co., Ltd. (“Petitioner”) requests *inter partes* review and cancellation of Claims 1-6, 8-12, and 14-16 (“the challenged claims”) of U.S. Patent No. 10,090,395 (“the ’395 Patent”), assigned to Acorn Semi, LLC (“Acorn”). The ’395 Patent purports to claim a priority date of August 12, 2002 through a series of parent applications, the earliest of which issued as U.S. Patent No. 7,084,423. (’395 Patent at Cover, 1:8-27; Ex. 1003.)

The ’395 Patent and the challenged claims generally relate to metal-semiconductor junctions with an interface layer between the metal and the semiconductor. (’395 Patent at 1:31-35.) The interface layer includes both a semiconductor oxide and a generic metal oxide. (*Id.* at Claims 1-6, 8-12, and 14-16.) But not all of the parent applications of the ’395 Patent describe the genus of metal oxides. Indeed, the first time the patentee even arguably described a generic metal oxide in an interface layer was in the originally filed claims of parent application U.S. Patent App. No. 13/022,522—which was not filed until February 7, 2011. (Ex. 1010, at 48.) As a result, no challenged claim can possibly obtain a priority date earlier than February 7, 2011.

Claim 6 cannot even obtain that February 7, 2011 date: none of the ’395 Patent’s parent applications enables the full scope of Claim 6’s open-ended recitation of “wherein said interface layer is configured to provide a specific contact

resistivity between the metal electrical contact and the region in the semiconductor of less than $10\ \Omega\text{-}\mu\text{m}^2$.” Specific contact resistivity is also called specific contact resistance. (Carver at 2.) Although the specification that the ’395 Patent shares with its parent applications purports to describe achieving some “minimum specific contact resistance,” that shared specification does not put a lower bound on that “minimum specific contact resistance.” (’395 Patent at 4:16-30.) Nor does it describe how to achieve specific contact resistances (resistivities) down to and including approximately zero.

That, however, did not stop the patentee from attempting to tie up future efforts to reduce specific contact resistivity via open-ended claiming. Instead of claiming, for instance, an electrical junction with “a specific contact resistivity between approximately $1000\ \Omega\text{-}\mu\text{m}^2$ and $10\ \Omega\text{-}\mu\text{m}^2$,” the inventors drafted unbounded claims whose specific contact resistivity is “less than $10\ \Omega\text{-}\mu\text{m}^2$.” With no lower bound to that specific contact resistivity limitation, no parent application can enable the *full* scope of Claim 6, including specific contact resistivities down to and including approximately zero. Thus, Claim 6 cannot obtain a filing date any earlier than that of the ’395 Patent: January 23, 2018.

Under either the February 7, 2011 or the January 23, 2018 priority date, U.S. Patent No. 7,176,483 (Ex. 1021, “Grupp ’483”)—which issued in 2007 and which has the same ancestor as the ’395 Patent—qualifies as prior art to the challenged

claims. As shown herein and as further explained in the declaration of Dr. E. Fred Schubert, an expert in metal-semiconductor junctions with more than thirty years of experience (Schubert Decl. ¶¶ 8-21), Grupp '483 anticipates every challenged claim. Petitioner therefore respectfully requests that the Board institute *inter partes* review, hold the challenged claims unpatentable, and cancel the challenged claims.

II. Mandatory Notices

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner identifies itself; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC as real parties-in-interest.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

1. Judicial Matters

The following judicial matters may affect or be affected by this proceeding: *Acorn Semi, LLC v. Samsung Electronics Co. Ltd.*, Civil Action No. 2:19-cv-347 (E.D. Tex.) (“the Acorn Litigation”), in which Patent Owner Acorn Semi, LLC (“Acorn”) filed a complaint alleging that Petitioner and its real parties-in-interest infringe the '395 Patent. (Ex. 1038 ¶¶ 108-117.) Acorn first served that complaint on October 24, 2019. (Ex. 1039.)

2. Administrative Matters

Public PAIR lists the following patents and applications that purport to claim the benefit of the priority of the filing date of the '395 Patent:

Patent or Application No.	Filing Date
U.S. Patent No. 10,186,592	May 16, 2018
U.S. Patent App. No. 16/506,022	July 9, 2019

Petitioner will be filing one or more petitions for *inter partes* review against the following patents related to the '395 Patent: U.S. Patent No. 7,084,423; U.S. Patent No. 8,766,336; U.S. Patent No. 9,209,261; U.S. Patent No. 9,461,167; and U.S. Patent No. 9,905,691. Those proceedings may affect or be affected by this proceeding. Further, Acorn has asserted those five other patents against Petitioner and its real parties-in-interest in the Acorn Litigation. (Ex. 1038 ¶¶ 58-107.)

C. Designation of Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))

With this petition, Petitioner is filing a power of attorney appointing the practitioners associated with Customer Number 132,593. Petitioner designates the following lead and back-up counsel:

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D. Service Information (37 C.F.R. § 42.8(b)(4))

Please direct all correspondence to lead and back-up counsel at the addresses listed above. Petitioner consents to electronic service at the following email addresses: jdesmarais@desmaraisllp.com; kkm-ptab@desmaraisllp.com; cmaier@desmaraisllp.com; and tkonstantakopoulos@desmaraisllp.com.

III. Fees

Petitioner is concurrently electronically submitting the required fees for this Petition. The Board is authorized to charge Desmarais LLP's deposit account, No. 50-6822, for any fee deficiency.

IV. Grounds for Standing

Petitioner certifies that the '395 Patent is available for *inter partes* review. Petitioner further certifies that neither Petitioner nor any real party-in-interest or privy is estopped or barred from requesting *inter partes* review of the challenged claims on the grounds identified in this petition.

V. Identification of Challenge and Relief Requested

Petitioner requests *inter partes* review and cancellation of Claims 1-6, 8-12, and 14-16 of the '395 Patent.

A. Identification of Prior Art

1. Grupp '483 (Ex. 1021)

As discussed in detail below in **Section IX**, no challenged claim is entitled to a priority date earlier than February 7, 2011, the filing date of U.S. Patent App. No. 13/022,522. U.S. Patent No. 7,176,483 to Grupp et al. (Ex. 1021, "Grupp '483"), issued on February 13, 2007, qualifies as prior art to all challenged claims either at least pre-AIA 35 U.S.C. § 102(b). Further, Claim 6 cannot even obtain that February 7, 2011 priority date; instead, Claim 6's priority date can be no earlier than the filing date of the '395 Patent on January 23, 2018. Grupp '483 also qualifies as prior art to Claim 6 under AIA 35 U.S.C. § 102(a)(1).

B. Statutory Grounds of Unpatentability

Ground 1: Grupp '483 anticipates Claims 1-6, 8-12, and 14-16 under at least pre-AIA 35 U.S.C. § 102(b). Because Claim 6 cannot obtain a priority date earlier than the January 23, 2018 filing date of the '395 Patent, Grupp '483 also anticipates Claim 6 under AIA 35 U.S.C. § 102(a)(1).

VI. Overview of the '395 Patent

A. Technical Background

Metal-semiconductor junctions are a basic electronic component. (Schubert Decl. ¶¶ 34-35; '395 Patent at 1:39-40.) Those junctions are generally characterized by a barrier to the movement of charge carriers at the interface between the metal and the semiconductor, called a Schottky barrier. (Rhoderick at 1; '395 Patent at 1:52-54; Schubert Decl. ¶ 36.) The barrier's width and its height each affect the junction's specific contact resistance. (Chang at 5-6; Schubert Decl. ¶¶ 37-43.)

The Schottky barrier height of a metal-semiconductor junction can become fixed at a particular height in a phenomenon known as Fermi-level pinning. ('395 Patent at 2:10-67, 5:35-38, 7:55-59; Schubert Decl. ¶¶ 44-48.) Electron states, including Bardeen states (such as dangling bonds at the semiconductor surface) and metal-induced gap states (energy states in the bandgap of the semiconductor that become populated due to the proximity of the metal), can cause the Fermi level to become pinned between the semiconductor's conduction and valence bands,

typically at or near the midgap. ('395 Patent at 2:41-3:9, 16:66-17:1; Schubert Decl.

¶¶ 48-49.) Fig. 7a shows a metal-semiconductor junction with a pinned Fermi level:

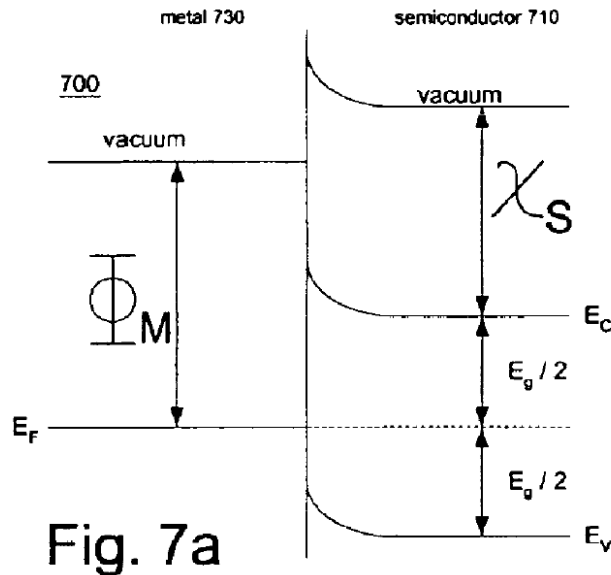


Fig. 7a

('395 Patent at Fig. 7a, 16:65-17:1.)

As Fig. 7a depicts, the pinned Fermi level E_F is not aligned with the conduction band edge E_C of the semiconductor at the interface. For an n-type semiconductor, the difference between the Fermi level E_F and the conduction band edge of the semiconductor E_C at the interface produces a barrier to the flow of electrons of height Φ_b , as shown in Fig. 4 of the '395 Patent:

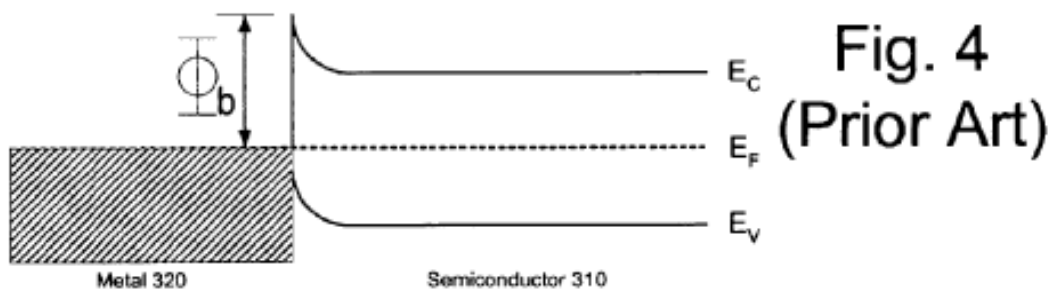


**Fig. 4
(Prior Art)**

('395 Patent at Fig. 4, 4:49-50, 7:35-59; Schubert Decl. ¶ 49.)

“The importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction. Thus, if one were able to control or adjust the barrier height of a metal-semiconductor junction, one could produce electrical devices of desired characteristics.” (’395 Patent at 3:10-14.) According to the ’395 Patent, depinning a Fermi level is one technique for accomplishing that. (*Id.* at 16:36-57, Schubert Decl. ¶ 50.) But even before the earliest alleged priority date of the ’395 Patent, techniques for depinning a Fermi level and controlling barrier height were well-known, as were techniques for reducing specific contact resistance. (Schubert Decl. ¶¶ 51-53.)

Indeed, even before the earliest alleged priority date of the challenged claims in August 2002, the prior art was replete with examples of interface layers that depin a Fermi level by passivating the semiconductor surface (thereby satisfying dangling bonds and reducing Bardeen states) and reducing the effects of metal-induced gap states, including the examples described in the Goodnick, Rhoderick, and Sobolewski references. (Schubert Decl. ¶¶ 52-55; Goodnick at 1; Rhoderick at 3, Sobolewski at 1.) It was similarly known that an interfacial oxide could reduce the barrier height of a metal-semiconductor junction. (Schubert Decl. ¶¶ 56-58; Risko at 1:43-50; Taubenblatt 1984 at 3.) Likewise, prior art spanning three decades taught that an interface layer could reduce the specific contact resistance of a metal-semiconductor junction: for example, the 1976 Schroen patent, the 1989 Kim

patent, and the 1999 Iwaguro patent application publication. (Schubert Decl. ¶¶ 59-63; Schroen at Abstract; Kim at 4:63-5:1, 5:27-30; Iwaguro at [0005]-[0006], [0012]-[0014].)

B. The Purported Invention of the '395 Patent

The purported invention of the '395 Patent, like the prior art, involves providing an interface layer between the metal and the semiconductor in a metal-semiconductor junction. ('395 Patent at 1:31-35.) Claim 1, the only independent challenged claim, illustrates that un inventive approach:

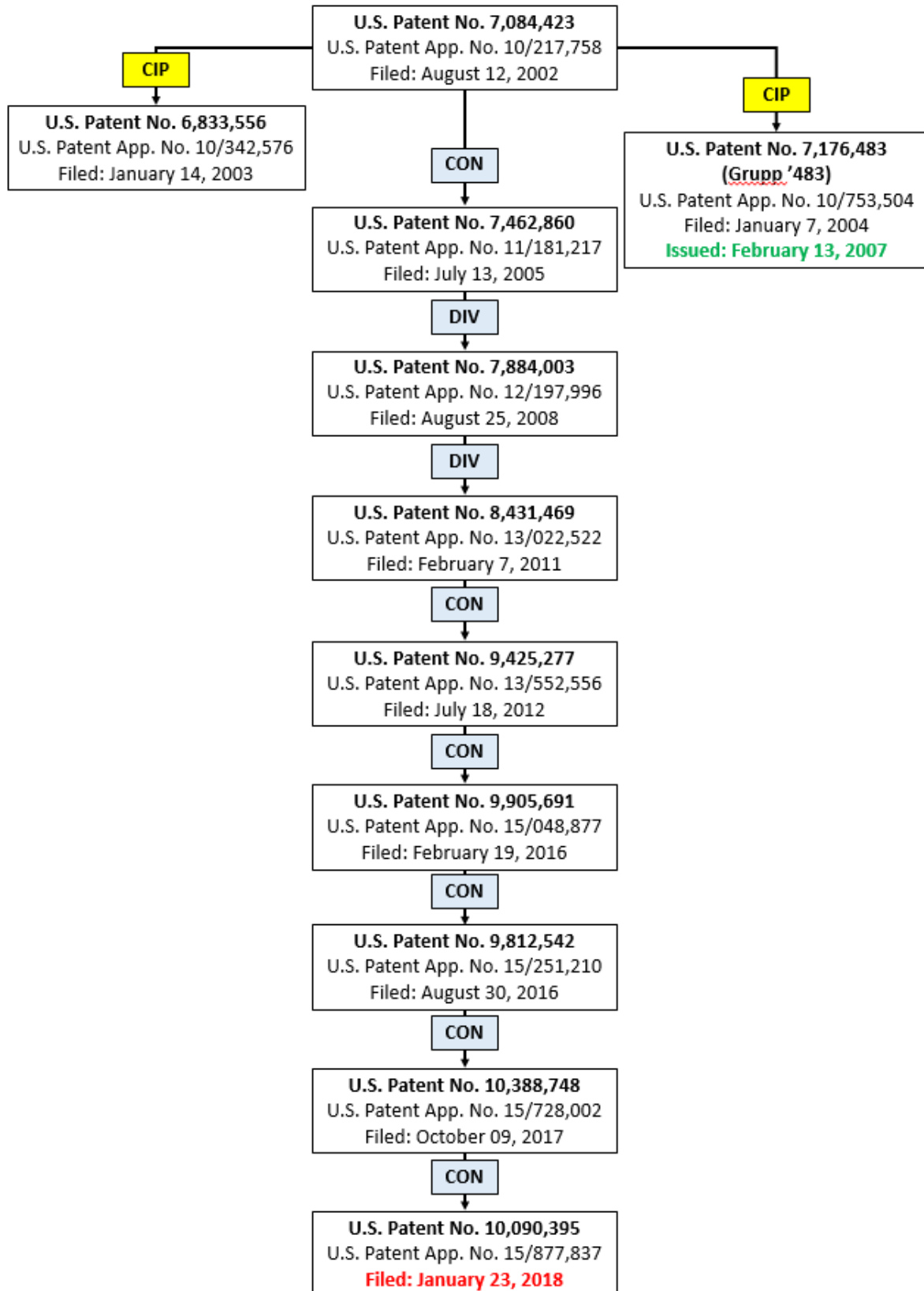
An electrical junction, comprising a region in a semiconductor substrate, a metal electrical contact to said region, and an interface layer between said region and said metal electrical contact, said region being electrically connected to said metal electrical contact through said interface layer and said interface layer comprising a metal oxide and a semiconductor oxide, and being in contact with said region in the semiconductor substrate and said metal electrical contact.

C. Prosecution History

The '395 Patent began as U.S. Patent App. No. 15/877,837 ("the '837 Application," filed on January 23, 2018. (Ex. 1020, at 3-49.) The '395 Patent purports to claim a priority date of August 12, 2002 through a series of parent applications, as shown in the partial family tree below:

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(Ex. 1005, at Cover; Ex. 1020, at 5; Grupp '483 at Cover, 1:8-19.)

Each challenged claim was among the originally filed claims of the '837 Application. (Ex. 1020, at 39-42.) In the Examiner's first office action, the Examiner contended that the '837 Application, styled as a continuation, was "actually a Continuation-In-Part." (*Id.* at 121.) According to the Examiner, "[a]ll of the independent claims recite either a semiconductor oxide or oxide of the semiconductor and a metal oxide or oxide of titanium in the interface layer, ***the pairing*** of which is not found or contemplated in the parent applications." (Ex. 1020, at 121.) Thus, the Examiner stated that "the subject matter of independent claim 1 of 'said interface layer comprising a metal oxide in contact with said electrical contact and a semiconductor oxide in contact with said region in the semiconductor substrate' is not supported by any of the parent applications from which the present application claims priority to." (*Id.*) The Examiner then rejected all of the challenged claims over U.S. Patent App. Pub. No. 2014/0117465 to Huang, either by itself or in combination with another reference. (*Id.* at 122-129; Ex. 1037.)

In response, the applicants contended that the parent applications describe an interface layer that includes a passivation layer and a separation layer, and that the parent applications describe titanium dioxide separation layer. (Ex. 1020, at 162-163.) "Thus, the specification provides written description support for semiconductor-interface layer-metal contact junctions in which the interface layer includes both a semiconductor oxide and a metal oxide and the interface layer is in

contact with both the semiconductor and the metal contact, as recited in the present claims.” (*Id.* at 163.) According to the applicants, the pending claims were entitled to a priority date of August 12, 2002, disqualifying Huang as prior art. (*Id.*)

The Examiner allowed the claims on the next action. (Ex. 1020, at 174.) But the Examiner’s statements on the reasons for allowance did not actually ascribe any specific priority date to the challenged claims. (*Id.*) Instead, the Examiner merely stated that “[a]fter consideration and persuasion of applicant’s arguments, amendments and a further search of the prior art of record, examiner has concluded that the prior art does not disclose nor fairly suggest the electrical junctions as described in the independent claims 1, 17 and 29.” (*Id.*) Notably, Huang’s earliest possible prior art date is its 35 U.S.C. § 102(e) prior art date, which fell in 2012. (Ex. 1037.) Thus, the Examiner’s decision to allow the claims over Huang does not necessarily indicate that the Examiner found that the claims are entitled to a priority date as early as August 12, 2002. In any event, the ’837 Application then issued as the ’395 Patent. (*Id.* at 196.)

VII. Level of Ordinary Skill in the Art

Any of the following combinations of education and experience would have qualified someone as an ordinarily skilled artisan in the field of the ’395 Patent:

- a Ph.D. in electrical engineering, physics, materials science, or chemical engineering, with two years of practical experience with semiconductor research and design;

- a Master's degree in electrical engineering, physics, materials science, or chemical engineering, with four years of practical experience with semiconductor research and design; or
- a Bachelor's degree in electrical engineering, physics, materials science, or chemical engineering, with six to eight years of practical experience with semiconductor research and design.

(Schubert Decl. ¶¶ 70-71.)

Further, additional education could make up for less practical experience, and vice versa. (*Id.*) The same level of ordinary skill would have been applicable in August 2002, February 2011, or January 2018. (*Id.*)

VIII. Claim Construction

For petitions filed after November 13, 2018, the Board “constru[es] the claim in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b); *see also Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). The Board need only construe claim terms to the extent necessary to resolve a controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Below, Petitioner construes the term “specific contact resistivity.” As for all remaining claim terms, the challenged claims are unpatentable under those terms’

ordinary and customary meanings, as explained in detail below. The Board need not expressly construe any other term at this stage.¹

A. Claim 6: “a specific contact resistivity between the metal electrical contact and the region in the semiconductor of less than $10\ \Omega\text{-}\mu\text{m}^2$ ”

The term “specific contact resistivity” appears in Claim 6. Ordinarily skilled artisans commonly (if not universally) used the terms “specific contact resistivity” and “specific contact resistance” interchangeably. (Carver at 2; *see also* Schubert Decl. ¶¶ 74-76.) The ’395 Patent’s use of “specific contact resistivity” in Claim 6 tracks that common interchangeable use: the specification of the ’395 Patent never uses the phrase “specific contact resistivity,” but it does discuss specific contact resistance as part of the invention. (*E.g.*, ’395 Patent at 3:25-29, 3:42-45, 3:52-53, 4:22-30.) Thus, an ordinarily skilled artisan would have understood Claim 6’s “specific contact resistivity” to refer to specific contact resistance.

¹ Petitioner reserves all rights to raise claim construction arguments and other arguments in the Acorn Litigation or other proceedings involving the ’395 Patent. For example, Petitioner has not raised all of its challenges to the ’395 Patent here, including invalidity under 35 U.S.C. § 112. Further, comparing the claims to the accused products in the Acorn Litigation may raise controversies that require claim construction in that litigation, but not here.

IX. The challenged claims are not entitled to any priority date earlier than February 7, 2011.

The '395 Patent purports to claim priority to August 12, 2002, the filing date of the application that issued as U.S. Patent No. 7,084,423. ('395 Patent at Cover, 1:8-27; Ex. 1003, at Cover.) For the challenged claims to receive the benefit of the priority of that August 12, 2002 filing date, every application in the priority chain leading to the application that issued as the '395 Patent must support every limitation of the challenged claims under 35 U.S.C. § 112 ¶ 1. *In re NTP, Inc.*, 654 F.3d 1268, 1277 (Fed. Cir. 2011). Thus, every parent application of the '395 Patent must both enable and describe every limitation of every challenged claim. *Id.*; *Fiers v. Revel*, 984 F.2d 1164, 1169-70 (Fed. Cir. 1993).

But the challenged claims have at least two limitations that the parent applications fail to support: (1) the generic “metal oxide” in the limitation “said interface layer comprising a metal oxide and a semiconductor oxide” in every challenged claim; and (2) “wherein said interface layer is configured to provide a specific contact resistivity between the metal electrical contact and the region in the semiconductor of less than $10\ \Omega\text{-}\mu\text{m}^2$ ” in Claim 6. Those unsupported limitations are discussed below with reference to the '395 Patent's disclosure, including incorporated-by-reference U.S. Patent No. 6,833,556. (Ex. 1005.) The parent applications' specifications and figures are substantively identical to the '395 Patent, including in their incorporation by reference of U.S. Patent No. 6,833,556. Thus, if

a limitation lacks support in the '395 Patent's disclosure, it also lacks support in the parent applications' disclosures, and vice versa. (Ex. 1002, at 5-52; Ex. 1003; Ex. 1006, at 3-42; Ex. 1007; Ex. 1008, at 8-49; Ex. 1009; Ex. 1010, at 14-51; Ex. 1011; Ex. 1012, at 6-46; Ex. 1013; Ex. 1014, at 12-17, 35-65; Ex. 1015; Ex. 1016, at 12-48; Ex. 1017; Ex. 1018, at 51-87; Ex. 1019; Schubert Decl. ¶¶ 86-88, 100-102.)

The only differences among the parent applications and the '395 Patent are their respective abstracts and claims. But, even those abstracts and claims cannot provide the challenged claims with any priority date earlier than February 7, 2011. In particular, the patentee did not even arguably disclose a generic "metal oxide" as in the limitation "said interface layer comprising a metal oxide and a semiconductor oxide" until February 7, 2011, in the originally filed claims of U.S. Patent App. No. 13/022,522. (Ex. 1010, at 48; Schubert Decl. ¶¶ 89-90.)

Thus, no challenged claim can possibly obtain a priority date earlier than February 7, 2011. *In re NTP*, 654 F.3d at 1276-77. And Claim 6 fares even worse than that: **no** parent application enables the full scope of the limitation "wherein said interface layer is configured to provide a specific contact resistivity between the metal electrical contact and the region in the semiconductor of less than 10 $\Omega\text{-}\mu\text{m}^2$." That leaves Claim 6 with a priority date no earlier than January 23, 2018, the filing date of the '395 Patent. Grupp '483, which issued in 2007, qualifies as prior art

under 35 U.S.C. § 102(b) in even the best-case scenario for the challenged claims, and it also qualifies as prior art under AIA 35 U.S.C. § 102(a)(1) to Claim 6.

A. Claims 1-6, 8-12, and 14-16 are not entitled to any priority date earlier than February 7, 2011 because no earlier parent application describes an interface layer including a generic “metal oxide.”

As discussed above, the challenged claims cannot obtain their alleged August 12, 2002 priority date unless all of the '395 Patent's parent applications provide written description support for every limitation of the challenged claims. *In re NTP*, 654 F.3d at 1277. “[T]he test for sufficiency is whether the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). Thus, “[a] disclosure in a parent application that merely renders the later-claimed invention obvious is not sufficient to meet the written description requirement; the disclosure must describe the claimed invention with all its limitations.” *Tronzo v. Biomet, Inc.*, 156 F.3d 1154, 1158 (Fed. Cir. 1998).

To support a claim to a genus, the specification must disclose “either a representative number of species falling within the scope of the genus or structural features common to the members of the genus so that one of skill in the art can ‘visualize or recognize’ the members of the genus.” *Ariad*, 598 F.3d at 1350. Here, every challenged claim includes a generic “metal oxide” for an interface layer by

virtue of Claim 1's "interface layer comprising a metal oxide and a semiconductor oxide." The first time that the patentee even arguably disclosed a generic "metal oxide" for an interface layer is in the originally filed claims of U.S. Patent App. No. 13/022,522, filed on February 7, 2011. (Ex. 1010, at 48; Schubert Decl. ¶ 89.) The only possible example of a metal oxide for an interface layer described in any earlier parent application is a TiO₂ spacer layer: "[s]pacer layers may be used with lower barriers (e.g., TiO₂ has a barrier of less than 1 eV)." ('395 Patent at 18:6-8; Schubert Decl. ¶ 90.)

Although incorporated-by-reference U.S. Patent No. 6,833,556 describes a generic metal oxide and four example metal oxides, those metal oxides are only used to electrically isolate a transistor's gate from its channel "such that essentially no current flows between the gate 270 and the channel 220"—not for an interface layer through which current does flow, as is claimed. (Ex. 1005, at 7:60-8:22; *see also id.* at 13:44-14:20; '395 Patent at 14:58-65; Schubert Decl. ¶ 91.) Even if Acorn contends that those metal oxides could have been suitable for use as the claimed interface layers, U.S. Patent No. 6,833,556 does not describe using them for that purpose. (Schubert Decl. ¶¶ 92-93; Ex. 1005, at 7:60-8:22, 13:44-14:20.) And even if it would have been obvious to use them for that purpose, that still would not have satisfied the written description requirement. *Tronzo*, 156 F.3d at 1158.

Thus, the relevant question is whether the earlier parent applications' statement that "[s]pacer layers may be used with lower barriers (e.g., TiO₂ has a barrier of less than 1 eV)" provides written description of the entire genus of metal oxide interface layers. ('395 Patent at 18:6-8.) And the answer is no: some metal oxides present considerably higher barriers than the "barrier of less than 1 eV" ascribed to TiO₂. For example, hafnium oxide and zirconium oxide are metal oxides with barriers to aluminum of 2 eV and 2.43 eV, respectively—well above the "less than 1 eV" presented by TiO₂ as described in the '395 Patent's parent applications. ('395 Patent at 18:6-8; Lang at 4; Zheng at 1; Schubert Decl. ¶ 94.) Moreover, aluminum is identified as a low workfunction metal in the '261 Patent's parent applications. ('395 Patent at 14:4-9.) Hafnium oxide and zirconium oxide present even higher barriers to metals with high workfunctions. (*Id.* at 14:10-13; Schubert Decl. ¶ 95.)

That discrepancy shows that neither TiO₂ nor "lower barriers" represents the full genus of metal oxides. Those disclosures, whether taken alone or together, do not reflect the full variation across the genus of metal oxide interface layers, including the variation in barrier heights across the genus of metal oxide interface layers. Thus, no application prior to U.S. Patent App. No. 13/022,522 provides written description of a generic "metal oxide" interface layer.

Indeed, “[a] patentee will not be deemed to have invented species sufficient to constitute the genus by virtue of having disclosed a single species when, as is the case here, the evidence indicates ordinary artisans could not predict the operability in the invention of any species other than the one disclosed.” *In re Curtis*, 354 F.3d 1347, 1358 (Fed. Cir. 2004). *In re Curtis* involved claims directed to PTFE dental floss reciting a genus of friction-enhancing coatings, but the specification only identified only one friction-enhancing coating: microcrystalline wax (MCW). *Id.* at 1349, 1358. Because neither the specification nor any other evidence conveyed that any other coating was suitable as a friction-enhancing coating for PTFE dental floss, the Federal Circuit held that the lone disclosed example could not support a claim to a genus of friction-enhancing coatings. *Id.* at 1358.

Like the lone example in *In re Curtis*, TiO₂ is the only metal oxide interface layer disclosed in the parent applications predating U.S. Patent App. No. 13/022,522. Finally, Acorn’s own complaint alleges that the operability of the claimed interface layers was unpredictable; indeed, it alleges that using *any* interface layer was “counter-intuitive.” (Ex. 1038 ¶¶ 6, 48; Schubert Decl. ¶ 96.) Thus, just as the lone example of MCW in *In re Curtis* could not support a claim to the genus of friction-enhancing coatings, the previous parent applications’ lone example of TiO₂ as a spacer layer cannot support claims to a generic “metal oxide” for an interface layer. Accordingly, no challenged claim can possibly obtain a priority date earlier than

February 7, 2011, the filing date of U.S. Patent App. No. 13/022,522. (Schubert Decl. ¶ 97.)

B. Claim 6 is not entitled to any priority date earlier than January 23, 2018 because the parent applications of the '395 Patent fail to enable the full scope of Claim 6.

“The enablement requirement asks whether ‘the specification teach[es] those in the art to make and use the invention without undue experimentation.’” *Enzo Life Scis., Inc. v. Roche Molecular Sys., Inc.*, 928 F.3d 1340, 1345 (Fed. Cir. 2019), *cert. denied*, 589 U.S. ____ (Mar. 30, 2020) (quoting *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988)). “This important doctrine prevents both inadequate disclosure of an invention and overbroad claiming that might otherwise attempt to cover more than was actually invented.” *Magsil Corp. v. Hitachi Global Storage Techs., Inc.*, 687 F.3d 1377, 1380-81 (Fed. Cir. 2012). Thus, “the specification must teach those of skill in the art how to make and how to use the invention as broadly as it is claimed.” *In re Goodman*, 11 F.3d 1046, 1050 (Fed. Cir. 1993).

The disclosure that the '395 Patent shares with its parent applications falls well short of that mark. Claim 6 broadly recites an interface layer “configured to provide a specific contact resistivity between the metal electrical contact and the region in the semiconductor of less than 10 $\Omega\text{-}\mu\text{m}^2$ ” As written, that claim limitation has no lower bound on specific contact resistivity. The specification imposes no lower bound on specific contact resistivity, either, as it does not quantify or describe

any lower bound for the “minimum specific contact resistance” that it purports to describe. (’395 Patent at Fig. 8, 4:16-30, 14:42-62.) Thus, the “less than $10 \Omega\text{-}\mu\text{m}^2$ ” part of that limitation encompasses specific contact resistivities down to and including approximately zero.

But specific contact resistivities down to and including approximately zero cannot be achieved according to the teachings of the ’395 Patent and its parent applications. Their shared disclosure purports to describe an interface layer that minimizes the total specific contact resistance (specific contact resistivity) of a metal-semiconductor junction, represented below by the “total current” curve that sums (1) resistance to tunneling current and (2) resistance to current by electron emission:

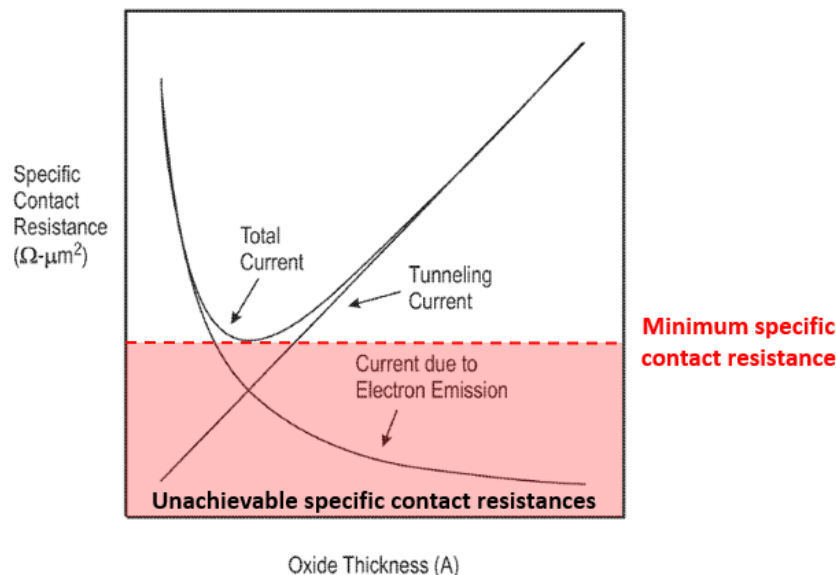


Fig. 8

(’395 Patent at Fig. 8 (annotations added), 14:42-62; Schubert Decl. ¶¶ 103-105.)

As can be seen from the annotated figure above, the nadir of Fig. 8's "total current" curve indicates a range of specific contact resistivities down to and including approximately zero that an ordinarily skilled artisan could not have attained by following the teachings of the '395 Patent and its parent applications. Thus, those parent applications fail to enable the *full* scope of Claim 6's "configured to provide a specific contact resistivity between the metal electrical contact and the region in the semiconductor of less than $10\ \Omega\text{-}\mu\text{m}^2$."

Nor should the Board constrain "less than $10\ \Omega\text{-}\mu\text{m}^2$ " to some lower bound in order to enable Claim 6. That would be tantamount to redrafting it, and the Federal Circuit "repeatedly and consistently has recognized that courts may not redraft claims, whether to make them operable or to sustain their validity." *Chef America, Inc. v. Lamb-Weston, Inc.*, 358 F.3d 1371, 1374 (Fed. Cir. 2004). Rather, "a patentee chooses broad claim language at the peril of losing any claim that cannot be enabled across its full scope of coverage." *Magsil*, 687 at 1381.

Indeed, Claim 6 closely resembles the non-enabled claims in *Magsil*. *Magsil* involved claims to a tri-layer tunnel junction "wherein applying a small magnitude of electromagnetic energy to the junction reverses at least one of the magnetization directions and causes a change in the resistance by at least 10% at room temperature." 687 F.3d at 1379. While the patent at issue described certain resistance change values within that range—"as much as 11.8% change was seen"—

the inventors did not attain even an 18% change until after the filing date. *Id.* at 1381-82. The district court nonetheless followed the plain language of the claims in construing them to cover from a 10% change to an infinite percentage change in resistance. *Id.* at 1382. It then granted the defendant summary judgment that the claims were not enabled. *Id.* at 1380.

The Federal Circuit affirmed both the district court's claim construction and its enablement decision. *Magsil*, 687 F.3d at 1382-85. Noting that the patentee chose to draft open-ended claims, it held the patentee to the consequences of that choice: "MagSil's difficulty in enabling the asserted claims is a problem of its own making." *Id.* at 1384. The Court emphasized the lack of working examples in the specification, and further noted that junctions with even a 100% to 120% change in resistance had not been developed until twelve years after the patent's filing date. *Id.* at 1381-82. That led the Federal Circuit to uphold the district court's summary judgment of non-enablement. *Id.* at 1382.

Claim 6 is no better off than the non-enabled claims in *Magsil*. The disclosure that the '395 Patent shares with its parent applications does not describe **any** working examples of an electrical junction with a specific contact resistivity under $10\ \Omega\text{-}\mu\text{m}^2$, down to and including approximately zero—a range encompassed by every challenged claim. Worse still, despite the '395 Patent and its parent applications expressly teaching that the disclosed techniques cannot reduce specific contact

resistivity below some unspecified minimum, the patentee nonetheless drafted open-ended claims with no lower bound on specific contact resistivity. ('395 Patent at Fig. 8, 14:42-62; Schubert Decl. ¶¶ 103-106.)

Because Claim 6 encompasses a range of specific contact resistivities down to and including approximately zero that cannot be achieved according to the '395 Patent's parent applications, those parent applications cannot enable the full scope of the challenged claims. *Magsil*, 687 F.3d at 1382. And when the breadth of a claim alone indicates that the claim is not enabled—as is the case here—that disposes of the enablement issue in its entirety, as it did in *Magsil*. *CommVault Sys., Inc. v. Realtime Data, LLC*, Case IPR2017-01710, Paper 11, at 20 (PTAB Jan. 18, 2018) (citing *Magsil*, 687 F.3d at 1382). Because no parent application enables the full scope of Claim 6, its priority date is the filing date of the '395 Patent: January 23, 2018.

X. The challenged claims are unpatentable.

A. Ground 1: Grupp '483 anticipates Claims 1-6, 8-12, and 14-16.

1. Overview of Grupp '483

Grupp '483 is a continuation-in-part of an August 2002 application that issued as U.S. Patent No. 7,084,423. (Grupp '483 at Cover, 1:8-19.) The '395 Patent purports to claim priority to that same August 2002 application through a chain of parent applications. ('395 Patent at Cover, 1:8-29.) Thus, Grupp '483 (on the one

hand) and the '395 Patent and its parent applications (on the other hand) have significantly overlapping disclosures. Unsurprisingly, Grupp '483 anticipates every challenged claim.

2. Claim 1

i. An electrical junction, comprising

To the extent the preamble is limiting, Grupp '483 discloses it. (Schubert Decl. ¶ 108.) For example, “[i]n one embodiment, the present invention provides an electrical junction that includes a semiconductor (e.g., C, Ge, or an Si-based semiconductor), a conductor, and an interface layer disposed therebetween.” (Grupp '483 at 3:44-47; *see also id.* at 3:18-22, 5:49-58, 19:26-27.)

ii. a region in a semiconductor substrate,

Grupp '483 discloses this limitation. (Schubert Decl. ¶¶ 109-110.) For example, “[t]he present inventors have determined that for thin interface layers disposed between a metal and a semiconductor (e.g., C, Ge, Si, SiC and SiGe), so as to form a metal—interface layer—semiconductor junction, there exist corresponding minimum specific contact resistances.” (Grupp '483 at 3:18-22.) “In one embodiment, the present invention provides an electrical junction that includes a semiconductor (e.g., C, Ge, or an Si-based semiconductor), a conductor, and an interface layer disposed therebetween.” (*Id.* at 3:44-47.)

One example of a region in a semiconductor substrate that Grupp '483 discloses is a source or drain of a transistor. (Schubert Decl. ¶ 110.) In a section on “Transistors Containing Passivated Semiconductor Surfaces,” Grupp '483 discloses that “the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility).” (Grupp '483 at 18:19-20, 19:11-15.) As Dr. Schubert explains, “in a transistor, a ‘well’ is a doped region of a semiconductor in which source and drain regions are formed by implanting dopants; the source and drain regions have a doping opposite that of the well.” (Schubert Decl. ¶ 110.)

iii. a metal electrical contact to said region, and

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 111.) For example, “[i]n further embodiments the present invention provides an electrical device in which an interface layer is disposed between and in *contact with a metal* and a semiconductor” (Grupp '483 at 4:21-23; *see also id.* at Fig. 7d, 3:18-22, 3:44-47, 5:49-58, 18:4-17 (describing an interface layer between silicon and aluminum).)

iv. an interface layer between said region and said metal electrical contact,

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 112.) For example, “[i]n further embodiments the present invention provides an electrical device in which *an interface layer is disposed between and in contact with a metal and a*

semiconductor” (Grupp ’483 at 4:21-23; *see also id.* at Fig. 7d, 3:18-22, 3:44-47, 5:49-58, 18:4-17 (describing an interface layer between silicon and aluminum); Schubert Decl. ¶ 112.)

v. said region being electrically connected to said metal electrical contact through said interface layer and

Grupp ’483 discloses this limitation. (Schubert Decl. ¶ 113.) For example, “the present invention provides an electrical device in which an interface layer is disposed between and in contact with a metal and a semiconductor and is configured to depin the Fermi level of the semiconductor while still *permitting current flow between the metal and the semiconductor* when the electrical device is biased.” (Grupp ’483 at 4:21-26.)

vi. said interface layer comprising a metal oxide and a semiconductor oxide, and

Grupp ’483 discloses this limitation. (Schubert Decl. ¶¶ 114-117.) Grupp ’483 discloses an interface layer that includes (1) a passivation layer, which can be a semiconductor oxide; and (2) a separation layer, which can be titanium dioxide, a metal oxide. (*Id.* ¶ 114.) “The interface layer includes a passivating material, for example, a nitride, a fluoride, an *oxide*, an oxynitride, a hydride and/or an arsenide *of the semiconductor*, and in some cases may also include a separation layer.” (Grupp ’483 at 3:53-56; *see also id.* at 4:28-31, 4:53-55, 8:64-9:10, 9:39-43, 10:34-44, 10:48-54, 10:60-63, 11:35-38, 13:41-46.)

In turn, the separation layer can be an oxide. (Grupp '483 at 11:35-38.) More specifically, the separation layer can be a “spacer layer” of TiO₂, which is titanium dioxide: “[s]pacer layers may be used with lower barriers (e.g., TiO₂ has a barrier of less than 1 eV).” (*Id.* at 18:65-67; *see also id.* at 18:45-65; Schubert Decl. ¶ 116.) Thus, Grupp '483 discloses an interface layer comprising a metal oxide (titanium dioxide) and an oxide of the semiconductor. (Schubert Decl. ¶ 117.)

vii. being in contact with said region in the semiconductor substrate and said metal electrical contact.

Grupp '483 discloses this limitation. (Schubert Decl. ¶¶ 118-119.) For example, “[i]n further embodiments the present invention provides an electrical device in which an *interface layer is disposed between and in contact with a metal and a semiconductor . . .*.” (Grupp '483 at 4:21-23.)

3. Claim 2

i. The electrical junction of claim 1,

Grupp '483 discloses the electrical junction of Claim 1, as discussed above in **Section X.A.2.** (Schubert Decl. ¶ 121.)

ii. wherein the semiconductor oxide comprises an oxide of the region in the semiconductor substrate.

Grupp '483 discloses this limitation. (Schubert Decl. ¶¶ 122-125.) As discussed above in **Section X.A.2.vi**, Grupp '483 discloses an interface layer that includes a semiconductor oxide as a passivating material.

Grupp '483 further discloses using an oxide of a region of a silicon semiconductor substrate as that passivating material. (Grupp '483 at 10:27-34, 10:48-54, 10:60-63; Schubert Decl. ¶¶ 122-124.) Grupp '483 discloses that “passivation layers made using N and/or *O* [oxygen] may not require distinct separation layers, as *these elements may form a layer of a compound of Si* [silicon] with a thickness that can be varied depending on processing.” (*Id.* at 10:60-63.) Although that excerpt discusses examples that “may not require distinct separation layers,” Grupp '483 expressly discloses using a separation layer when the passivating material is an oxide. (*Id.* at 11:35-38.) Finally, Grupp '483 also discloses silicon dioxide, another oxide of silicon, as a passivating material. (*Id.* at 8:64-9:10; Schubert Decl. ¶ 125.)

4. Claim 3

i. The electrical junction of claim 2,

Grupp '483 discloses the electrical junction of Claim 2, as discussed above in **Section X.A.3.** (Schubert Decl. ¶ 127.)

ii. wherein the semiconductor oxide has a thickness of approximately 0.1 nm to 5 nm.

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 128.) “The interface layer includes a passivating material, for example, a nitride, a fluoride, an *oxide*, an oxynitride, a hydride and/or an arsenide *of the semiconductor*, and in some cases may also include a separation layer.” (Grupp '483 at 3:53-56; *see also id.* at 4:28-

31, 4:53-55, 8:64-9:10, 9:39-43, 10:34-38, 10:48-54, 10:60-63, 11:35-38, 13:41-46.)

Grupp further discloses that the interface layer's passivating material—*i.e.*, the semiconductor oxide—can be 0.1 nm to 5 nm thick: “the interface layer 520 includes or is made up of a passivation layer with a thickness of between approximately 0.1 nm and about 5 nm.” (Grupp '483 at 10:66-11:1; *see also id.* at 11:1-4.)

5. Claim 4

i. The electrical junction of claim 1,

Grupp '483 discloses the electrical junction of Claim 1, as discussed above in **Section X.A.2.** (Schubert Decl. ¶ 130.)

ii. wherein said region in the semiconductor substrate comprises a source or drain of a transistor.

Grupp '483 discloses this limitation. (Schubert Decl. ¶¶ 131-132.) Grupp '483 states that its invention encompasses a broad category of metal-interface layer-semiconductor contacts. (Grupp '483 at 18:32-35.) Further, in a section entitled “Transistors Containing Passivated Semiconductor Surfaces,” Grupp '483 discloses that “the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility).” (Grupp '483 at 18:19-20, 19:11-15.) As Dr. Schubert explains, “[i]n a transistor, a ‘well’ is a doped region of a semiconductor in which source and drain regions are formed by implanting dopants; the source and drain regions have a doping opposite that of the

well.” (Schubert Decl. ¶ 132.) Accordingly, Grupp ’483 discloses “source or drain” semiconductor regions of a transistor. (Grupp ’483 at 18:19-20, 19:11-15.)

6. Claim 5

i. The electrical junction of claim 1,

Grupp ’483 discloses the electrical junction of Claim 1, as discussed above in **Section X.A.2.** (Schubert Decl. ¶ 134.)

ii. wherein said interface layer has a thickness sufficient to depin a Fermi level of the metal electrical contact in a vicinity of the junction

Grupp ’483 discloses this limitation. (Schubert Decl. ¶¶ 136-137.) Discussing the optimum thickness of an interface layer for depinning a Fermi level of a conductor in a metal-semiconductor junction (Grupp ’483 at 15:34-54), Grupp ’483 discloses that “[a]t this thickness the effect of MIGS has been sufficiently reduced to *depin the metal* and lower the Schottky barrier, and the layer is still sufficiently thin to allow significant current flow across the interface layer.” (*Id.* at 15:50-54.) Accordingly, Grupp ’483 discloses an interface layer having a thickness sufficient to depin a Fermi level of the conductor in a vicinity of the junction.

* * *

In a related proceeding involving U.S. Patent No. 7,084,423, a parent of the ’395 Patent, Petitioner has construed the related term “depin a Fermi level of the conductor in a vicinity of the junction” to mean “passivate the semiconductor surface

and reduce the effects of metal-induced gap states in the semiconductor.” Applying that construction here to the term “depin a Fermi level of the metal electrical contact in a vicinity of the junction,” Grupp ’483 discloses that “[t]he interface layer preferably (i) is of a thickness sufficient to reduce effects of MIGS in the semiconductor, and (ii) passivates the surface of the semiconductor.” (Grupp ’483 at 4:46-48; *see also id.* at 18:5-10.)

- iii. **yet thin enough to provide the junction with a specific contact resistivity that is generally dependent on: a workfunction of the metal electrical contact, a Fermi energy of the semiconductor in the region, or both the workfunction of the metal electrical contact and the Fermi energy of the semiconductor in the region.**

Grupp ’483 discloses this limitation. (Schubert Decl. ¶¶ 138-141.) In particular, Grupp ’483 discloses an interface layer thin enough to provide the junction with a specific contact resistivity that is generally dependent on a workfunction of the metal electrical contact.

“There are several methods by which the barrier height can be made adjustable. For example, adjustment may be made by tuning the degree of Fermi level pinning.” (Grupp ’483 at 17:28-30.) “[T]he pinning may be varied by combinations of thickness of the interface layer and the choice of interface material.” (*Id.* at 17:33-35.) “Complete depinning of the Fermi level (that is removal of all surface states in Si including MIGS is another option, in which case one could tune the barrier height simply by choosing a pure metal or an alloy that possesses the

desired workfunction.” (*Id.* at 17:39-43.) “Ideally, if all surface states are removed, barrier height should be controllable simply by the choice of metal used.” (*Id.* at 15:31-33.) Thus, Grupp ’483 discloses an interface layer of an appropriate thickness (*i.e.*, “thin enough”) to provide the junction with a barrier height that generally depends on the workfunction of the metal electrical contact. (Schubert Decl. ¶ 139.)

“The importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction.” (Grupp ’483 at 3:3-5.) In particular, specific contact resistivity generally depends on barrier height. (Chang at 5-6.) As Dr. Schubert explains, “[b]ecause Grupp ’483’s interface layer is thin enough to provide a barrier height that generally depends on the workfunction of the metal electrical contact, it follows that Grupp ’483’s interface layer is also thin enough to provide a specific contact resistivity that generally depends on the workfunction of the metal electrical contact.” (Schubert Decl. ¶ 140.)

In that regard, Grupp ’483 discloses an example of specific contact resistivity generally depending on a workfunction of the metal when the interface layer’s thickness is optimized. (Schubert Decl. ¶ 141.) Referring to Fig. 8, Grupp ’483 discloses that “[t]he graph is for a structure where the *workfunction of the metal* is the same as the electron affinity in the semiconductor, such that the Fermi level of the metal lines up with the conduction band of the semiconductor.” (Grupp ’483 at 15:34-40.) When the interface layer’s thickness is optimized, the alignment of the

metal's Fermi level and the semiconductor's conduction band—which alignment generally depends on the workfunction of the metal—minimizes specific contact resistivity. (*Id.* at 15:40-57.) Accordingly, Grupp '483 discloses an interface layer thin enough to provide the junction with a specific contact resistivity that is generally dependent on the workfunction of the metal electrical contact.

Finally, the Board should reject any argument Acorn might make that Grupp '483 fails to disclose this limitation. During the prosecution of the parent U.S. Patent No. 7,084,423, the patentee argued that the same disclosure cited above supports the limitation “yet thin enough to provide the junction with a specific contact resistance that is generally dependent on the work function of the conductor” in then-pending Claim 62 of that parent. (Ex. 1002, at 245.) “Support for this claim may be found, for example at paragraph 70 et seq. of the specification as originally filed.” (*Id.*) That paragraph 70 is identical to the disclosure of Grupp '483 cited above in this petition. (*Compare* Ex. 1002, at 29-30 *with* Grupp '483 at 15:34-57.)

7. Claim 6

i. The electrical junction of claim 1,

Grupp '483 discloses the electrical junction of Claim 1, as discussed above in **Section X.A.2.** (Schubert Decl. ¶ 143.)

- ii. **wherein said interface layer is configured to provide a specific contact resistivity between the metal electrical contact and the region in the semiconductor of less than $10\ \Omega\text{-}\mu\text{m}^2$.**

Grupp '483 provides presumptively enabling disclosure of an interface layer configured to provide a specific contact resistivity between the metal electrical contact and the region in the semiconductor within the specified range, thereby satisfying this limitation. (Schubert Decl. ¶¶ 144-145.) As discussed above in **Section VIII.A**, “specific contact resistivity” is interchangeable with “specific contact resistance,” so the analysis for this limitation focuses on specific contact resistance.

Grupp '483 discloses that “the present inventors have determined that for thin interface layers disposed between a metal and a semiconductor, so as to form a metal-interface layer-semiconductor junction, there exist corresponding minimum specific contact resistances.” (Grupp '483 at 5:64-6:1.) “Indeed, minimum specific contact resistances of less than or equal to approximately $10\ \Omega\text{-}\mu\text{m}^2$ or even less than or equal to approximately $1\ \Omega\text{-}\mu\text{m}^2$ may be achieved for such junctions in accordance with the present invention.” (Grupp '483 at 6:1-5; *see also id.* at 3:40-43, 5:64-6:1, 8:58-61, 10:44-47; 15:52-57.) Grupp '483 therefore discloses an interface layer configured to provide some non-zero specific contact resistivity of less than $10\ \Omega\text{-}\mu\text{m}^2$, such as a specific contact resistivity of $1\ \Omega\text{-}\mu\text{m}^2$ or just under

10 $\Omega\text{-}\mu\text{m}^2$, between the metal electrical contact and the region of the semiconductor.

(Schubert Decl. ¶ 144.)

Grupp '483's disclosure of a non-zero, but less than 10 $\Omega\text{-}\mu\text{m}^2$ specific contact resistivity is presumed enabling. *Amgen, Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1355 (Fed. Cir. 2003) (“[W]e hold a presumption arises that both the claimed and unclaimed disclosures in a prior art patent are enabled.”). Further, Grupp '483's presumptively enabled non-zero, but less than 10 $\Omega\text{-}\mu\text{m}^2$ specific contact resistivity suffices to satisfy this limitation for anticipation: “[w]hen a patent claims a range, as in this case, that range is anticipated by a prior art reference if the reference discloses a point within the range.” *Ineos USA LLC v. Berry Plastics Corp.*, 783 F.3d 865, 869 (Fed. Cir. 2015) (citing *Titanium Metals Corp. v. Banner*, 778 F.3d 775, 782 (Fed. Cir. 1985)). So, while Grupp '483 may not enable a specific contact resistivity all the way down to and including approximately zero, it does not need to. Its disclosure of a non-zero, but less than 10 $\Omega\text{-}\mu\text{m}^2$ specific contact resistivity (such as a specific contact resistivity of 1 $\Omega\text{-}\mu\text{m}^2$ just under 10 $\Omega\text{-}\mu\text{m}^2$) is presumed enabling, and that disclosure satisfies this limitation for anticipation.

(Schubert Decl. ¶ 145.)

8. Claim 8

i. The electrical junction of claim 1,

Grupp '483 discloses the electrical junction of Claim 1, as discussed above in **Section X.A.2.** (Schubert Decl. ¶ 147.)

ii. wherein said metal oxide comprises an oxide of said metal electrical contact.

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 148.) As discussed above in **Section X.A.2.iii**, Grupp '483 discloses a metal electrical contact. Further, Grupp '483 discloses using titanium (Ti) as the metal electrical contact. (Grupp '483 at 4:13-20, 14:58-15:2, Claim 7.) Finally, as discussed above in **Section X.A.2.vi**, Grupp '483 describes an interface layer that includes a titanium dioxide spacer layer: “[s]pacer layers may be used with lower barriers (e.g., TiO₂ has a barrier of less than 1 eV).” (*Id.* at 18:65-67.) Thus, Grupp '483 discloses titanium as a metal electrical contact, and titanium dioxide is an oxide of that titanium metal electrical contact. (Schubert Decl. ¶ 148.)

9. Claims 9 and 10

Claims 9 and 10 are identical and are treated together below.

i. The electrical junction of claim 8,

Grupp '483 discloses the electrical junction of Claim 8, as discussed above in **Section X.A.8.** (Schubert Decl. ¶ 150.)

- ii. **wherein said semiconductor oxide comprises an oxide of the region in the semiconductor substrate.**

This limitation also appears in Claim 2. Grupp '483 discloses this limitation for the reasons discussed above in **Section X.A.3.ii.** (Schubert Decl. ¶ 151.)

10. Claim 11

- i. **The electrical junction of claim 1,**

Grupp '483 discloses the electrical junction of Claim 1, as discussed above in **Section X.A.2.** (Schubert Decl. ¶ 153.)

- ii. **wherein said metal oxide comprises an oxide of titanium.**

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 154.) As discussed above in **Section X.A.2.vi**, Grupp '483 discloses a titanium dioxide (TiO₂) spacer layer: “Spacer layers may be used with lower barriers (e.g., TiO₂ has a barrier of less than 1 eV).” (Grupp '483 at 18:65-67.)

11. Claim 12

- i. **The electrical junction of claim 11,**

Grupp '483 discloses the electrical junction of Claim 11, as discussed above in **Section X.A.10.** (Schubert Decl. ¶ 156.)

- ii. **wherein said semiconductor oxide comprises an oxide of silicon.**

Grupp '483 discloses this limitation. (Schubert Decl. ¶¶ 157-159.) As discussed above in **Section X.A.2.vi**, Grupp '483 discloses using a semiconductor

oxide as a passivating material. Further, Grupp '483 discloses using either an oxide of silicon (Grupp '483 at 10:27-34, 10:48-54, 10:60-63) or silicon dioxide (*id.* at 8:64-9:10) as the passivating semiconductor oxide. (Schubert Decl. ¶¶ 157-159.)

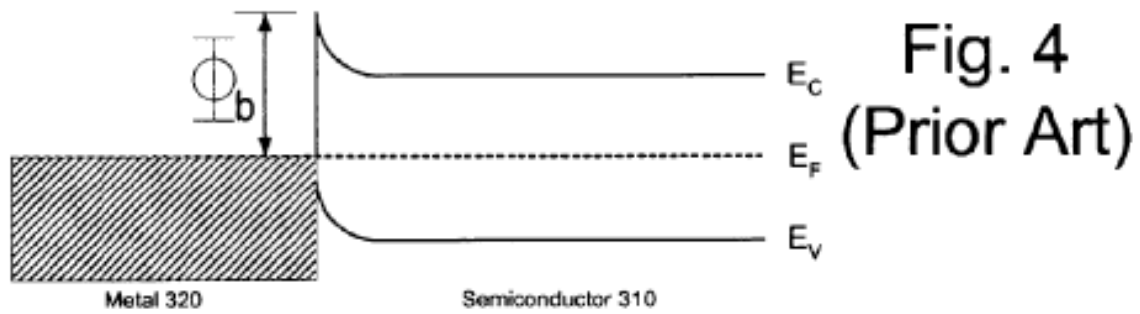
12. Claim 14

i. The electrical junction of claim 12,

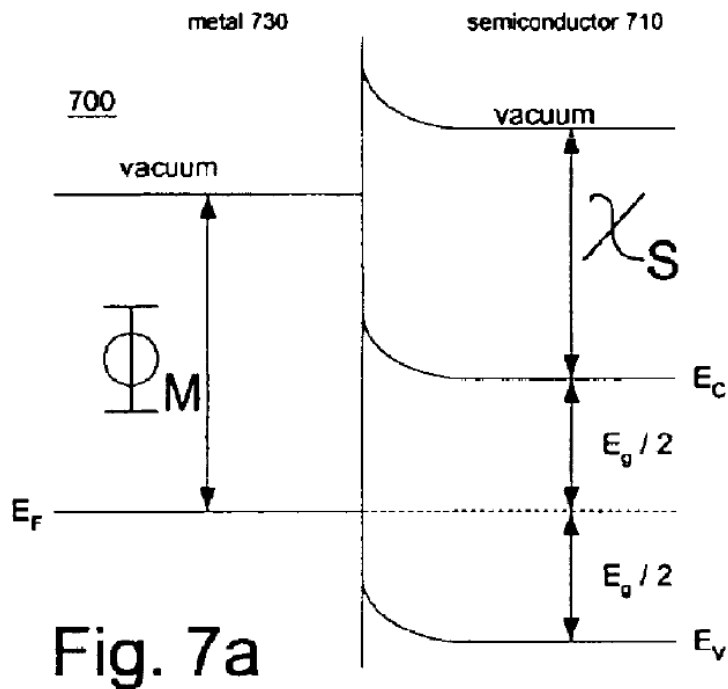
Grupp '483 discloses the electrical junction of Claim 12, as discussed above in **Section X.A.11**. (Schubert Decl. ¶ 161.)

ii. wherein said region in the semiconductor substrate comprises an n-type doped source or drain of a transistor.

Grupp '483 discloses this limitation. (Schubert Decl. ¶¶ 162-169.) Grupp '483 discloses that the semiconductor can be an n-type doped semiconductor. (Grupp '483 at 6:5-9; Schubert Decl. ¶ 163.) Further, Grupp '483's Fig. 7d depicts a junction between a metal and an n-type doped semiconductor with an interface layer in accordance with the invention. (Grupp '483 at Fig. 7d; *see also id.* at Fig. 4, Fig. 7a, 5:37-40, 18:4-10; Schubert Decl. ¶¶ 164-166.) As Dr. Schubert explains, Grupp '483's Fig. 7a depicts the same band bending as Grupp '483's Fig. 4, which is described as a junction between a metal and an n-type semiconductor:

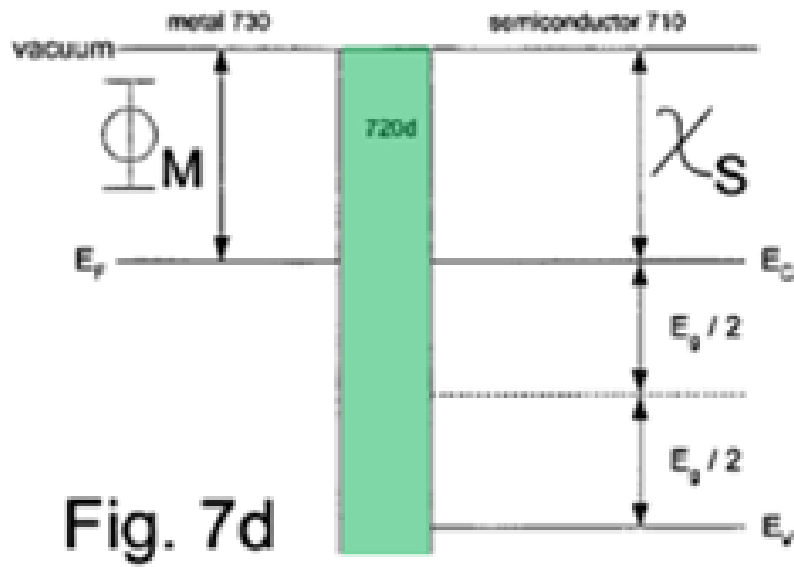


(Grupp '483 at Fig. 4, 5:22-23, 8:10-15; Schubert Decl. ¶¶ 164-166.)



(Grupp '483 at Fig. 7a, 17:57-60; Schubert Decl. ¶¶ 164-166.)

Fig. 7d depicts that n-type semiconductor in a metal-semiconductor junction with an interface layer and a depinned Fermi level in accordance with the invention:



(Grupp '483 at Fig. 7d (annotation added), 18:4-17; Schubert Decl. ¶¶ 164-166.)

Further, in a section entitled “Transistors Containing Passivated Semiconductor Surfaces,” Grupp '483 discloses that “the junction of the present invention can be used in making contacts to source or drain implanted wells and will have the advantage of reducing the need for high doping levels (which are now reaching their limits of solid solubility).” (Grupp '483 at 18:19-20, 19:11-15; *see also id.* at 18:32-35; Schubert Decl. ¶¶ 167-168.) As Dr. Schubert explains, “[i]n a transistor, a ‘well’ is a doped region of a semiconductor in which source and drain regions are formed by implanting dopants; the source and drain regions have a doping opposite that of the well.” (Schubert Decl. ¶ 168.)

In sum, Grupp '483 discloses that the region in the semiconductor substrate can be both (1) n-type doped and (2) the source or drain of a transistor. Accordingly,

Grupp '483 discloses the limitation “wherein the semiconductor comprises an n-type doped source or drain of a transistor.”

13. Claim 15

i. The electrical junction of claim 1,

Grupp '483 discloses the electrical junction of Claim 1, as discussed above in **Section X.A.2.** (Schubert Decl. ¶ 171.)

ii. wherein said metal electrical contact comprises titanium.

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 172.) As discussed above in **Section X.A.2.iii**, Grupp '483 discloses a metal electrical contact. Further, Grupp '483 discloses using titanium (Ti) as the metal electrical contact. (Grupp '483 at 4:13-20, 14:58-15:2, Claim 7.)

14. Claim 16

i. The electrical junction of claim 1,

Grupp '483 discloses the electrical junction of Claim 1, as discussed above in **Section X.A.2.** (Schubert Decl. ¶ 174.)

ii. wherein said metal electrical contact comprises tungsten.

Grupp '483 discloses this limitation. (Schubert Decl. ¶ 175.) As discussed above in **Section X.A.2.iii**, Grupp '483 discloses a metal electrical contact. Further, Grupp '483 discloses using tungsten (W) as the metal electrical contact. (Grupp '483 at 4:13-20, 14:58-15:5, Claim 8.)

XI. The discretionary factors favor instituting trial.

A. 35 U.S.C. § 325(d)

The Board employs a two-part framework in assessing whether to institute trial in light of 35 U.S.C. § 325(d): (1) whether the Office has been presented with the same or substantially the same prior art or arguments; and (2) if so, whether the Office erred in a manner material to the patentability of the challenged claims. *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, Case IPR2019-01469, Paper 6, at 8 (PTAB Feb. 13, 2020) (designated precedential). That framework favors institution for every ground here.

To start, the record of the Office's previous consideration of Grupp '483 with respect to the '395 Patent consists of the Examiner signing off on it in an information disclosure statement. (Ex. 1020, at 146.) The record of the Office's consideration of Grupp '483 in the '395 Patent's parent applications is similarly limited: it consisted of (1) the Examiner of one parent application identifying Grupp '483 as a pertinent reference; and (2) the Examiners of other parent applications signing off on Grupp '483 in information disclosure statements. (Ex. 1008, at 127-133; Ex. 1010, at 133; Ex. 1012, at 106; Ex. 1014, at 144; Ex. 1016, at 118; Ex. 1018, at 139.)

Crucially, no Examiner cited Grupp '483 against any claim of the '395 Patent or of any parent application. And merely signing an information disclosure statement or identifying a reference as pertinent does not warrant denying institution.

E.g., Zip Top, LLC v. Stasher, Inc., Case IPR2018-01216, Paper 14, at 35-36 (PTAB Jan. 17, 2019); *Navistar, Inc. v. Fatigue Fracture Tech., LLC*, Case IPR2018-00853, Paper 13, at 16-17 (PTAB Sept. 12, 2018).

Further, while the prosecution history of the '395 Patent includes some limited discussion of the priority date of the challenged claims, this petition presents a different priority issue than that discussed during prosecution. (Ex. 1020, at 121-122.) The issue discussed during prosecution was whether the parent applications described an interface layer that paired a semiconductor oxide with a metal oxide or oxide of titanium: “[a]ll of the independent claims recite either a semiconductor oxide or oxide of the semiconductor and a metal oxide or oxide of titanium in the interface layer, *the pairing* of which is not found or contemplated in the parent applications.” (*Id.* at 121; *see also id.* at 162-163.) That pairing issue is separate from whether the parent applications’ lone titanium dioxide spacer layer could support claims to *any* metal oxide for an interface layer. (Schubert Decl. ¶ 98.) And that lone example is inadequate for the reasons discussed above in **Section IX.A**.

Moreover, the Examiner did not expressly ascribe any particular priority date to the challenged claims in the statement on reasons for allowance. (Ex. 1020, at 174.) Notably, the Examiner would not have needed to ascribe an August 12, 2002 priority date to the pending claims to find them allowable over the Huang reference used in all of the Examiner’s rejections. (*Id.* at 162-169.) Indeed, Huang’s 2012

priority date is *after* the applicants first introduced a generic “metal oxide” for an interface layer in the originally filed claims of U.S. Patent App. No. 13/022,522 on February 7, 2011. (Ex. 1010, at 48; Ex. 1037, at Cover.) Thus, the Examiner’s decision to allow the challenged claims over Huang could have been based on an implicit determination that the challenged claims’ priority date is February 7, 2011. That February 7, 2011 priority date would have disqualified Huang as prior art—but it would not have disqualified Grupp ’483. In any event, even if the Examiner did tacitly determine that the challenged claims are entitled to an August 12, 2002 priority date or any other priority date earlier than February 7, 2011, the Examiner erred for the reasons discussed above in **Section IX**.

* * *

In sum, the Office has only minimally considered Grupp ’483 as it pertains to the ’395 Patent, and does not appear to have considered the priority issues raised herein. To the extent the Office considered either but allowed the challenged claims anyway, it erred: under the correct priority date of the challenged claims, Grupp ’483 anticipates all of them. The Board should therefore institute trial.

B. 35 U.S.C. § 314(a)

1. *General Plastic*

This is Petitioner’s first petition against the ’395 Patent. Further, this petition involves only one reference and one ground. The *General Plastic* factors therefore

do not weigh against institution here. *General Plastic Indus. Co., Ltd. v. Canon Kabushiki Kaisha*, Case IPR2016-01357, Paper 19, at 9-10 (PTAB Sept. 6, 2017) (designated precedential).

2. *NHK Spring / Apple*

Despite concurrent litigation involving the '395 Patent, discretionary denial of institution under *NHK Spring Co., Ltd. v. Intri-Plex Techs., Inc.*, Case IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018) (designated precedential) is unwarranted. Denying institution based on the presence or stage of concurrent litigation thwarts Congress's deliberate decision to provide *inter partes* review petitioners with a full year to file a petition after service of an infringement complaint. 35 U.S.C. § 315(b). Indeed, Congress initially considered giving *inter partes* review petitioners only six months. Joe Matal, *A Guide to the Legislative History of the America Invents Act: Part II of II*, 21 FED. CIR. B.J. 539, 611-612 (2012). But Congress instead decided to grant *inter partes* review petitioners a full year, and with good reason: Congress recognized that petitioners deserved a "reasonable opportunity to identify and understand the patent claims that are relevant to the litigation" when a patent owner asserts "multiple patents with large numbers of vague claims." *Id.* (citing 157 Cong. Rec. S5429 (daily ed. Sept. 8, 2011) (statement of Sen. Kyl)).

Here, Acorn has asserted ***108 claims across six patents*** in the Acorn Litigation, including ***25 claims of the '395 Patent***—precisely the scenario that

prompted Congress to give *inter partes* review petitioners a full year to file. (Ex. 1041; Ex. 1042.) Thus, denying institution because of concurrent litigation involving the '395 Patent would contradict Congress's intent in enacting the AIA. In any event, the six factors in *Apple Inc. v. Fintiv, Inc.*, Case IPR2020-00019, Paper 11, at 6 (PTAB Mar. 20, 2020) (designated precedential) that guide the Board's discretion collectively favor instituting trial, as explained below.

i. *Apple* factor 1: whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted

This factor favors instituting trial. Petitioner will be promptly moving to stay the Acorn Litigation. Although the Court presiding over the Acorn Litigation infrequently grants pre-institution motions to stay, it nonetheless invites defendants to renew their motions to stay once the Board institutes trial. And it has granted those renewed motions to stay even when the stage of the case has significantly advanced in the interim—even after claim construction has occurred.

For example, in *Image Processing Techs. LLC v. Samsung Elecs. Co., Ltd.*, the Court denied Samsung's pre-institution motion to stay, but invited Samsung to renew its motion to stay if the Board instituted trial. Case No. 2:16-cv-505-JRG, 2017 WL 10185855, at *1 (E.D. Tex. Feb. 17, 2017). The litigation proceeded in the interim, and the Court construed the claims four months later. 2017 WL 2672616 (E.D. Tex. June 21, 2017). Four months after that claim construction order, the

Court granted Samsung's renewed motion to stay after the Board instituted trial. 2017 WL 7051628, at *1 (E.D. Tex. Oct. 25, 2017). While the Court noted that decisions on motions to stay are by nature fact-dependent, it concluded that a stay was appropriate—despite the advanced stage of the case—because the Board instituted *inter partes* review on all but one asserted claim. *Id.*

Thus, even if the Acorn Litigation reaches an advanced stage by the time the Board decides whether to institute trial—indeed, even if claim construction has already taken place—the Acorn Litigation Court could still stay that litigation in view of a favorable institution decision. This factor therefore favors institution.

ii. *Apple* factor 2: proximity of the court's trial date to the Board's projected statutory deadline for a final written decision

Although the district court's trial date is currently ahead of the Board's projected statutory deadline for the final written decision, that trial date does not favor denying institution here. While the Acorn Litigation is scheduled for trial in April 2021 (Ex. 1040), jury trial dates—to say nothing of dates for post-trial briefing—are inherently subject to change. *Precision Planting, LLC v. Deere & Co.*, Case IPR2019-01044, Paper 17, at 15 (PTAB Dec. 2, 2019). The inherent uncertainty in any district court schedule weighs against denying institution. And it weighs especially heavily against denying institution here given the Acorn Litigation

Court’s willingness to stay advanced cases when the Board has instituted trial on the asserted claims. *Image Processing Techs.*, 2017 WL 7051628, at *1.

iii. *Apple* factor 3: investment in the parallel proceeding by the court and the parties

This factor largely overlaps with factor 2; for similar reasons, it does not favor denying institution. Whatever investment in the Acorn Litigation that the parties and Court might make between now and the Board’s institution decision, the Acorn Litigation Court has shown a willingness to stay cases for instituted *inter partes* reviews—even four months after a claim construction order. *Image Processing Techs.*, 2017 WL 7051628, at *1.

Further, the Board has held “that it is often reasonable for a petitioner to wait to file its petition until it learns which claims are being asserted against it in the parallel proceeding.” *Apple*, Case IPR2020-00019, Paper 11, at 11. Here, Acorn identified only one representative claim for each of six patents in its October 2019 complaint, including only one claim of the ’395 Patent, Claim 1. (Ex. 1038 ¶¶ 63, 73, 83, 93, 103, 113.) Later, in March 2020, Acorn served its infringement contentions—which collectively span **108 claims** across those six patents, including 24 previously unidentified claims of the ’395 Patent. (Ex. 1041; Ex. 1042.) Petitioner promptly filed this petition (and will be promptly filing its petitions against the asserted claims in other patents) after receiving those infringement contentions.

iv. *Apple* factor 4: overlap between issues raised in the petition and in the parallel proceeding

Although Petitioner is also challenging the validity of Claims 1-6, 8-9, 11-12, and 14-16 in the Acorn Litigation, that does not favor denying institution here. Instituting trial would make it possible for the Acorn Litigation Court to stay the Acorn Litigation, reducing the overlap of issues between the petition and the Acorn Litigation.

Further, it is unlikely that the Acorn Litigation will resolve the validity of every claim challenged here. While Acorn may commit to bringing all of those claims to trial, the far more likely outcome is that some claims will drop out before trial, leaving the Board as the only tribunal to assess them. Finally, to reduce overlap, if the Board institutes trial here, Petitioner will promptly cease asserting Grupp '483 and its pre-grant publication as prior art references to Claims 1-6, 8-9, 11-12, and 14-16 in the Acorn Litigation. Thus, this factor favors institution.

v. *Apple* factor 5: whether the petitioner and the defendant in the parallel proceeding are the same party

Petitioner and its real parties-in-interest are the defendants in the Acorn Litigation. But, that does not automatically favor denying institution. Rather, the Board principally considers this factor to avoid duplicating another tribunal's work. *Apple*, Case IPR2020-00019, Paper 11, at 13-14. And, as discussed above for factors 1-4, there is minimal risk of that happening here given (1) the Acorn Litigation

Court's willingness to grant stays where the Board has instituted trial on the asserted claims; and (2) Petitioner's willingness to cease asserting Grupp '483 and its pre-grant publication against Claims 1-6, 8-9, 11-12, and 14-16 in the Acorn Litigation if the Board institutes trial.

vi. *Apple* factor 6: other circumstances that impact the Board's exercise of discretion, including the merits

This factor favors institution: Petitioner has presented a compelling anticipation ground using Grupp '483. Further, *Apple* states that considerations similar to those under 35 U.S.C. § 325(d) are relevant. Case IPR2020-00019, Paper 11, at 16. As discussed above in **Section XI.A**, the prosecution history of the '395 Patent does not indicate that the Office has addressed the precise priority date issue raised herein or cited Grupp '483 against the claims. That favors instituting trial.

* * *

In conclusion, the district court's willingness to grant stays, Petitioner's diligence in preparing petitions against six patents spanning 108 asserted claims, the minimum likelihood of overlap, and Petitioner's strong merits case based on a previously unaddressed priority challenge collectively favor instituting trial. Moreover, the Acorn Litigation trial date is not set in stone, and even if it were, that trial date would only be "an additional factor" for the Board to consider. *NHK Spring*, Case IPR2018-00752, Paper 8, at 19-29. Indeed, "*NHK Spring* does not suggest, much less hold, that *inter partes* review should be denied under § 314(a)

solely because a district court is scheduled to consider the same validity issues before the *inter partes* review would be complete.” *Intuitive Surgical, Inc. v. Ethicon LLC*, Case IPR2018-01703, Paper 7, at 13 (PTAB Feb. 19, 2019). The Board should therefore institute trial.

XII. Conclusion

Petitioner respectfully requests that the Board institute *inter partes* review, hold the challenged claims unpatentable, and cancel the challenged claims.

Dated: June 29, 2020

Respectfully submitted,

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CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

I hereby certify that this paper, excluding the portions exempted under 37 C.F.R. § 42.24(a), has:

- 11,078 words as counted by Microsoft Word 2016, the word-processing system used to prepare this paper; and
- 277 words in the illustrations, counted manually.

This paper's total word count, excluding the portions exempted under 37 C.F.R. § 42.24(a), is **11,355** words.

Dated: June 29, 2020

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CERTIFICATE OF SERVICE

Under 37 C.F.R. § 42.6(e), the undersigned certifies that on June 29, 2020, a complete copy of the foregoing and all accompanying papers and exhibits were served via Federal Express Priority Overnight shipping, which is at least as fast and reliable as U.S. Priority Mail Express, on counsel of record for Acorn at the correspondence address indicated in PAIR:

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