

Petition for *Inter Partes* Review
U.S. Patent No. 10,090,395

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner

v.

ACORN SEMI, LLC,
Patent Owner

Case IPR2020-01282

U.S. Patent No. 10,090,395
Title: METHOD FOR DEPINNING THE FERMI LEVEL OF A
SEMICONDUCTOR AT AN ELECTRICAL JUNCTION AND DEVICES
INCORPORATING SUCH JUNCTIONS
Issue Date: October 2, 2018

PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 10,090,395

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PETITIONER'S EXHIBIT LIST

Petitioner Exhibit No.	DESCRIPTION
1101	U.S. Patent No. 10,090,395
1102	File History of U.S. Patent No. 7,084,423.
1103	U.S. Patent No. 7,084,423.
1104	File History of U.S. Patent No. 6,833,556.
1105	U.S. Patent No. 6,833,556.
1106	File History of U.S. Patent No. 7,462,860.
1107	U.S. Patent No. 7,462,860.
1108	File History of U.S. Patent No. 7,884,003.
1109	U.S. Patent No. 7,884,003.
1110	File History of U.S. Patent No. 8,431,469.
1111	U.S. Patent No. 8,431,469.
1112	File History of U.S. Patent No. 9,425,277.
1113	U.S. Patent No. 9,425,277.
1114	File History of U.S. Patent No. 9,905,691.
1115	U.S. Patent No. 9,905,691.
1116	File History of U.S. Patent No. 9,812,542
1117	U.S. Patent No. 9,812,542.
1118	File History of U.S. Patent No. 10,388,748.
1119	U.S. Patent No. 10,388,748.
1120	File History of U.S. Patent No. 10,090,395.
1121	S.M. Goodnick et al., <i>Effects of a thin SiO₂ layer on the formation of metal-silicon contacts</i> , 18 J. VAC. SCI. & TECH. 949 (Apr. 1981) (cited as "Goodnick").
1122	U.S. Patent No. 6,724,088 (cited as "Jammy").
1123	M.A. Taubenblatt and C.R. Helms, <i>Silicide and Schottky barrier formation in the Ti-Si and the Ti-SiO_x-Si systems</i> , 53 J. APPLIED PHYS. 6308 (Sept.1982) (cited as "Taubenblatt 1982").
1124	C.Y. Chang et al., <i>Specific contact resistance of metal-semiconductor barriers</i> , 14 SOLID STATE ELECS. 541 (1971) (cited as "Chang").
1125	U.S. Patent No. 4,845,050 (cited as "Kim").
1126	Declaration of Dr. E. Fred Schubert (cited as "Schubert Decl.").
1127	E.H. Rhoderick, <i>Metal-semiconductor contacts</i> , 129 IEE REV. 1 (Feb. 1982) (cited as "Rhoderick").

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1128	M.A. Sobolewski and C.R. Helms, <i>Studies of barrier height mechanisms in metal-silicon nitride-silicon Schottky barrier diodes</i> , 7 J. VAC. SCI. & TECH. B 971 (July/Aug. 1989) (cited as “Sobolewski”).
1129	U.S. Patent No. 4,110,488 (cited as “Risko”).
1130	M.A. Taubenblatt et al., <i>Interface effects in titanium and hafnium Schottky barriers on silicon</i> , 44 APPLIED PHYS. LETTERS 895 (cited as “Taubenblatt 1984”).
1131	U.S. Patent No. 3,983,264 (cited as “Schroen”).
1132	Japanese Laid-Open App. No. JPH11162874A (June 18, 1999).
1133	Certified Translation of Japanese Laid-Open App. No. JPH11162874A (June 18, 1999) (cited as “Iwaguro”).
1134	Gary P. Carver et al., <i>Specific Contact Resistivity of Metal-Semiconductor Contacts—A New, Accurate Method Linked to Spreading Resistance</i> , 35 IEEE TRANS. ELECTRON DEVICES 489 (Apr. 1988) (cited as “Carver”).
1135	U.S. Patent No. 5,216,282 (cited as “Cote”).
1136	A. Rohatgi et al., <i>Comprehensive Study of Rapid, Low-Cost Silicon Surface Passivation Technologies</i> , 47 IEEE Trans. Electron Devices 987 (May 2000) (cited as “Rohatgi”).
1137	European Patent App. Pub. No. EP0789388A2 to Hara et al. (cited as “Hara”).
1138	U.S. Patent No. 6,521,502 (cited as “Yu”).
1139	T. Sakurai et al., <i>Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas</i> , 25 IEEE SOLID STATE CIRCUITS 584 (Apr. 1990) (cited as “Sakurai”).
1140	U.S. Patent No. 4,304,042 (cited as “Yeh”).
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1142	U.S. Patent App. Pub. No. 2006/0178015 (cited as “Verhaverbeke”).
1143	T.H. DiStefano and D.E. Eastman, <i>The band edge of amorphous SiO₂ by photoinjection and photoconductivity measurements</i> , 9 SOLID STATE COMM. 2259 (1971) (cited as “DiStefano”).
1144	M.L. Bortz et al., <i>Temperature dependence of the electronic structure of oxides: MgO, MgAl₂O₄ and Al₂O₃</i> , 41 PHYSICA SCRIPTA 537 (1990) (cited as “Bortz”).

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1145	H.-J. Fitting et al., <i>Monte-Carlo Approach of Electron Emission from SiO₂</i> , 81 PHYSICA STATUS SOLIDI (a) 323 (1984) (cited as “Fitting”).
1146	Edet F. Archibong and Alain St-Amant, <i>On the Structure of Al₂O₃ and Photoelectron Spectra of Al₂O₂⁻ and Al₂O₃⁻</i> , 103 J. PHYS. CHEM. A 1109 (1999) (cited as “Archibong”).
1147	N.D. Lang and W. Kohn, <i>Theory of Metal Surfaces: Work Function</i> , 3 PHYS. REV. B 1215 (Feb. 1971) (cited as “Lang”).
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1149	John G. Simmons, <i>Generalized Formula for the Electric Tunnel Effect Between Similar Electrodes Separated by a Thin Insulating Film</i> , 34 J. APP. PHYS. 1793 (June 1963) (cited as “Simmons”).
1150	I. Polishchuk et al., <i>Dual work function metal gate CMOS technology using metal interdiffusion</i> , 22 IEEE ELECTRON DEVICE LETTERS 444 (Sept. 2001) (cited as “Polishchuk”).
1151	N. Szydlo and R. Poirier, <i>I-V and C-V Characteristics of Au/TiO₂ Schottky diodes</i> , 51 J. APPLIED PHYS. 3310 (June 1980) (cited as “Szydlo”).
1152	S.S. Cohen et al., <i>Chapter 6 – Practical Ohmic Contacts to Silicon</i> , 13 VLSI ELECS. MICROSTRUCTURE SCI. 213 (1986) (cited as “Cohen”).
1153	Declaration of Dr. Sylvia D. Hall-Ellis (cited as “Hall-Ellis Decl.”).
1154	U.S. Patent No. 4,583,110.
1155	U.S. Patent No. 4,801,984.
1156	U.S. Patent No. 5,614,745.
1157	Complaint in <i>Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.</i> , Case No. 2:19-cv-00347, ECF No. 1 (E.D. Tex. Oct. 23, 2019).
1158	Summons and Return of Service in <i>Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.</i> , No. 2:19-cv-00347, ECF No. 8 (E.D. Tex. Oct. 29, 2019).
1159	Second Amended Docket Control Order, <i>Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.</i> , No. 2:19-cv-00347, ECF No. 39 (E.D. Tex. Apr. 21, 2020).
1160	Cover Pleading to Acorn’s Preliminary Infringement Contentions in <i>Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.</i> , No. 2:19-cv-00347 (Mar. 9, 2020).

Petition for *Inter Partes* Review

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Petitioner Exhibit No.	DESCRIPTION
1161	Exhibit F to Acorn's Preliminary Infringement Contentions in <i>Acorn Semi, LLC v. Samsung Elecs. Co., Ltd.</i> , No. 2:19-cv-00347 (Mar. 9, 2020).

All citations to specific pages of exhibits follow the pagination added to those exhibits per 37 C.F.R. § 42.63(d)(2)(i).

I. Introduction

Petitioner Samsung Electronics Co., Ltd. (“Petitioner”) requests *inter partes* review and cancellation of Claims 1-6, 8-12, and 14-28 (“the challenged claims”) of U.S. Patent No. 10,090,395 (“the ’395 Patent”), assigned to Acorn Semi, LLC (“Acorn”). The ’395 Patent purports to claim a priority date of August 12, 2002 through its parent applications. (’395 Patent at Cover, 1:8-27.)

The ’395 Patent and the challenged claims generally relate to metal-semiconductor junctions with an interface layer between the metal and the semiconductor. (’395 Patent at 1:31-35.) The interface layer includes both a semiconductor oxide and either a generic metal oxide or an oxide of titanium. (*Id.* at Claims 1-6, 8-12, and 14-28.) But junctions like those were well-known in the prior art, even before August 2002. For example, the Goodnick reference, a 1981 journal article, describes a junction that includes aluminum, a silicon substrate, and an interface layer of aluminum oxide and silicon dioxide in between. (Goodnick at 1-2, 5.) Likewise, the Taubenblatt 1982 reference describes a structure that includes titanium, a silicon substrate, and an interface layer including titanium oxide and silicon dioxide in between. (Taubenblatt 1982 at 7-8.) And

While some challenged claims require a particular type of semiconductor (such as a source or drain of a transistor), a particular metal (such as tungsten), the Jammy and Kim references taught those features, and it would have been obvious to

combine them with Goodnick, Taubenblatt 1982, or both. (Jammy at 4:32-33; Kim at 4:59-5:4.) Likewise, while Claim 6 requires a specific contact resistivity of less than $10\ \Omega\text{-}\mu\text{m}^2$, an ordinarily skilled artisan could have and would have achieved that specific contact resistivity for a junction of titanium; a titanium oxide-silicon dioxide interface layer; and an n-type doped silicon source or drain of a transistor as in Jammy, doped to the high doping concentrations described in the Chang reference. (Chang at 7 (Fig. 5, describing a doping concentration of 10^{21} dopant atoms / cm^3 for n-type silicon).)

In sum, an ordinarily skilled artisan would have found the challenged claims obvious over the prior art discussed herein, as explained by Dr. E. Fred Schubert, an expert in metal-semiconductor junctions with more than thirty years of experience. (Schubert Decl. ¶¶ 8-21.) Because the challenged claims are unpatentable, Petitioner respectfully requests that the Board institute *inter partes* review, hold the challenged claims unpatentable, and cancel the challenged claims.

II. Mandatory Notices

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner identifies itself; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor, LLC as real parties-in-interest.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

1. Judicial Matters

The following judicial matters may affect or be affected by this proceeding:
Acorn Semi, LLC v. Samsung Electronics Co. Ltd., Civil Action No. 2:19-cv-347 (E.D. Tex.) (“the Acorn Litigation”), in which Patent Owner Acorn Semi, LLC (“Acorn”) filed a complaint alleging that Petitioner and its real parties-in-interest infringe the ’395 Patent. (Ex. 1157 ¶¶ 108-117.) Acorn first served that complaint on October 24, 2019. (Ex. 1158.)

2. Administrative Matters

The ’395 Patent is also involved in Case IPR2020-01207.

Petitioner has filed one or more petitions for *inter partes* review against the following patents related to the ’395 Patent: U.S. Patent No. 7,084,423; U.S. Patent No. 8,766,336; U.S. Patent No. 9,209,261; U.S. Patent No. 9,461,167; and U.S. Patent No. 9,905,691. Those proceedings may affect or be affected by this proceeding. Further, Acorn has asserted those five other patents against Petitioner and its real parties-in-interest in the Acorn Litigation. (Ex. 1157 ¶¶ 58-107.)

C. Designation of Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))

With this petition, Petitioner is filing a power of attorney appointing the practitioners associated with Customer Number 132,593. Petitioner designates the following lead and back-up counsel:

Lead Counsel	Back-up Counsel
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D. Service Information (37 C.F.R. § 42.8(b)(4))

Please direct all correspondence to lead and back-up counsel at the addresses listed above. Petitioner consents to electronic service at the following email addresses: jdesmarais@desmaraisllp.com; kkm-ptab@desmaraisllp.com; cmaier@desmaraisllp.com; and tkonstantakopoulos@desmaraisllp.com.

III. Fees

Petitioner is concurrently electronically submitting the required fees for this Petition. The Board is authorized to charge Desmarais LLP's deposit account, No. 50-6822, for any fee deficiency.

IV. Grounds for Standing

Petitioner certifies that the '395 Patent is available for *inter partes* review. Petitioner further certifies that neither Petitioner nor any real party-in-interest or privy is estopped or barred from requesting *inter partes* review of the challenged claims on the grounds identified in this petition.

V. Identification of Challenge and Relief Requested

Petitioner requests *inter partes* review and cancellation of Claims 1-6, 8-12, and 14-28 of the '395 Patent.

A. Identification of Prior Art

The references identified below were prior art even as of the earliest alleged priority date of the challenged claims in August 12, 2002. Petitioner reserves the right to challenge the priority date of the challenged claims in its reply in this proceeding, or in any other proceeding.

1. Goodnick (Ex. 1121)

S.M. Goodnick et al., *Effects of a thin SiO₂ layer on the formation of metal-silicon contacts*, 18 J. VAC. SCI. & TECH. 949 (Apr. 1981) (Ex. 1121, "Goodnick"),

published in print in 1981 and again online in 1998. Because Goodnick became a prior art printed publication more than a year before August 12, 2002, Goodnick is prior art under at least 35 U.S.C. § 102(b).

On its face, Goodnick states that it is a publication of the Journal of Vacuum Science and Technology. (Goodnick at Cover, 1.) The Journal of Vacuum Science and Technology, the official publication of the AVS Science and Technology Society, was a well-known journal that split into two journals in 1983. (Schubert Decl. ¶ 76; Hall-Ellis Decl. ¶ 72.) That Goodnick published in the Journal of Vacuum Science and Technology—instead of either of its post-1983 successor journals—demonstrates that Goodnick first published before 1983, more than a year before August 12, 2002. Further, Goodnick bears a copyright date of 1981 and a printing date of April 1981. (Goodnick at Cover, 1.) Goodnick also indicates that it published again online in June 1998. (*Id.* at Cover; Hall-Ellis Decl. ¶ 68.)

Further, the declaration testimony of Dr. Sylvia Hall-Ellis, an expert librarian, confirms that Goodnick was publicly accessible more than a year before August 12, 2002. As Dr. Hall-Ellis explains, MARC and OCLC records, as well as other records of the King Library at San José State University and the University of Minnesota Library, indicate that Goodnick was cataloged, indexed, and publicly available through at least the King Library on or shortly after April 30, 1981. (Hall-Ellis Decl. ¶¶ 69-76, Attachments 3a-3d.) Finally, the American Vacuum Society's records

indicate that at least fourteen publications cited Goodnick more than a year before August 12, 2002. (Hall-Ellis Decl. ¶ 77, Attachment 3e (Citations 12-25).)

2. Jammy (Ex. 1122)

U.S. Patent No. 6,724,088 to Jammy et al., (Ex. 1122, “Jammy”), filed on April 20, 1999, qualifies as prior art under at least 35 U.S.C. § 102(e).

3. Taubenblatt 1982 (Ex. 1123)

M.A. Taubenblatt and C.R. Helms, *Silicide and Schottky barrier formation in the Ti-Si and the Ti-SiO_x-Si systems*, 58 J. APPLIED PHYS. 6308 (1982) (Ex. 1123, “Taubenblatt 1982”), published in 1982. Because Taubenblatt 1982 became a prior art printed publication more than a year before August 12, 2002, Taubenblatt 1982 is prior art under at least 35 U.S.C. § 102(b).

Taubenblatt 1982 states that it is a publication of the Journal of Applied Physics. (Taubenblatt 1982 at 1.) Further, Taubenblatt 1982 states that it was “accepted for publication 27 May 1982” and published in September 1982. (*Id.*; see also Hall-Ellis Decl. ¶¶ 45-46 (confirming that Taubenblatt 1982 published in the September 1982 issue of the Journal of Applied Physics).) Taubenblatt 1982 also bears a copyright date of 1982 to the American Institute of Physics. (Taubenblatt 1982 at 1.) And, records of the American Institute of Physics indicate that Taubenblatt 1982 published again online in August 1998. (Hall-Ellis Decl. ¶ 46.)

Further, as Dr. Hall-Ellis explains, MARC and OCLC records, as well as other records of the King Library at San José State University and the University of Minnesota Library, indicate that Taubenblatt 1982 was cataloged, indexed, and publicly available through at least the King Library on or shortly after September 30, 1982. (Hall-Ellis Decl. ¶¶ 47-54, Attachments 1a-1c.) Finally, subsequent citations to Taubenblatt 1982, as indicated by Google Scholar, further confirm its public accessibility. (Hall-Ellis Decl. ¶ 55, Attachment 1d.)

4. Chang (Ex. 1124)

C.Y. Chang et al., *Specific contact resistance of metal-semiconductor barriers*, 15 SOLID STATE ELECS. 541 (1971) (Ex. 1124, “Chang”) published in 1971. Because Chang became a prior art printed publication more than a year before August 12, 2002, Chang is prior art under at least 35 U.S.C. § 102(b).

Chang states that it is a publication of the journal *Solid-State Electronics* by Pergamon Press that was “Printed in Great Britain” in 1971. (Chang at 1; see also Hall-Ellis Decl. ¶¶ 56-57 (confirming that Chang published in the July 1971 issue of the journal *Solid-State Electronics*.) Further, as Dr. Hall-Ellis explains, MARC and OCLC records, as well as other records of the King Library at San José State University and the Library of Congress, indicate that Chang was cataloged, indexed, and publicly available through at least the King Library on or shortly after July 31, 1971. (Hall-Ellis Decl. ¶¶ 56-65, Attachments 2a-2c.) And, subsequent citations to

Chang, as indicated by Google Scholar, further confirm Chang's public accessibility.

(Hall-Ellis Decl. ¶ 66, Attachment 2d.)

Finally, Chang is cited on the faces of three semiconductor patents that issued more than a year before August 12, 2002: U.S. Patent No. 4,583,110 (Ex. 1154), issued in 1986; U.S. Patent No. 4,801,984 (Ex. 1155), issued in 1989; and U.S. Patent No. 5,614,745 (Ex. 1156), issued in 1997. Each citation both (1) confirms Chang's public accessibility during the prosecution of those patents; and (2) makes those patents "research aids" directing ordinarily skilled artisans to Chang. *Bruckelmyer v. Ground Heaters, Inc.*, 445 F.3d 1374, 1379 (Fed. Cir. 2006); *see also Cornell Univ. v. Hewlett-Packard Co.*, No. 01-cv-1974, 2008 WL 11274580, at *5-7 (N.D.N.Y. May 14, 2008).

5. Kim (Ex. 1125)

U.S. Patent No. 4,845,050 to Kim et al. (Ex. 1125, "Kim"), filed on November 16, 1987 and issued on July 4, 1989, is prior art under at least 35 U.S.C. § 102(b).

B. Statutory Grounds of Unpatentability

Ground 1: Goodnick anticipates Claims 1-3 and 8-10 under at least 35 U.S.C. § 102(b).

Ground 2: Goodnick in view of Jammy renders Claim 4 obvious under 35 U.S.C. § 103(a).

Ground 3: Goodnick renders Claim 5 obvious under 35 U.S.C. § 103(a).

Ground 4: Goodnick in view of Taubenblatt 1982 renders Claims 1, 11, 12, 15, 23-25, and 28 obvious under 35 U.S.C. § 103(a).

Ground 5: Goodnick in view of Jammy and Taubenblatt 1982 renders Claims 14, 17-19 and 22 obvious under 35 U.S.C. § 103(a).

Ground 6: Goodnick in view of Jammy, Taubenblatt 1982, and Chang renders Claim 6 obvious under 35 U.S.C. § 103(a).

Ground 7: Goodnick in view of Taubenblatt 1982 and Kim renders Claims 16, 26, and 27 obvious under 35 U.S.C. § 103(a).

Ground 8: Goodnick in view of Jammy, Taubenblatt 1982, and Kim renders Claims 20 and 21 obvious under 35 U.S.C. § 103(a).

VI. Overview of the '395 Patent

A. Technical Background

Metal-semiconductor junctions are a basic electronic component. (Schubert Decl. ¶¶ 34-35; '395 Patent at 1:39-40.) Those junctions are generally characterized by a barrier to the movement of charge carriers at the interface between the metal and the semiconductor, called a Schottky barrier. (Rhoderick at 1; '395 Patent at 1:52-54; Schubert Decl. ¶ 36.) The barrier's width and its height each affect the junction's specific contact resistance. (Chang at 5-6; Schubert Decl. ¶¶ 37-43.)

The Schottky barrier height of a metal-semiconductor junction can become fixed at a particular height in a phenomenon known as Fermi-level pinning. ('395

Patent at 2:10-67, 5:35-38, 7:55-59; Schubert Decl. ¶¶ 44-48.) Electron states, including Bardeen states (such as dangling bonds at the semiconductor surface) and metal-induced gap states (energy states in the bandgap of the semiconductor that become populated due to the proximity of the metal), can cause the Fermi level to become pinned between the semiconductor's conduction and valence bands, typically at or near the midgap. ('395 Patent at 2:41-3:9, 16:66-17:1; Schubert Decl. ¶¶ 48-49.) Fig. 7a shows a metal-semiconductor junction with a pinned Fermi level:

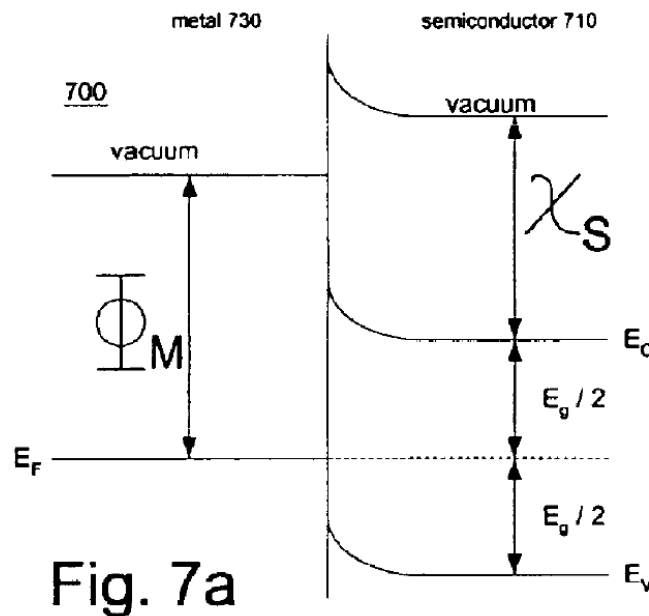
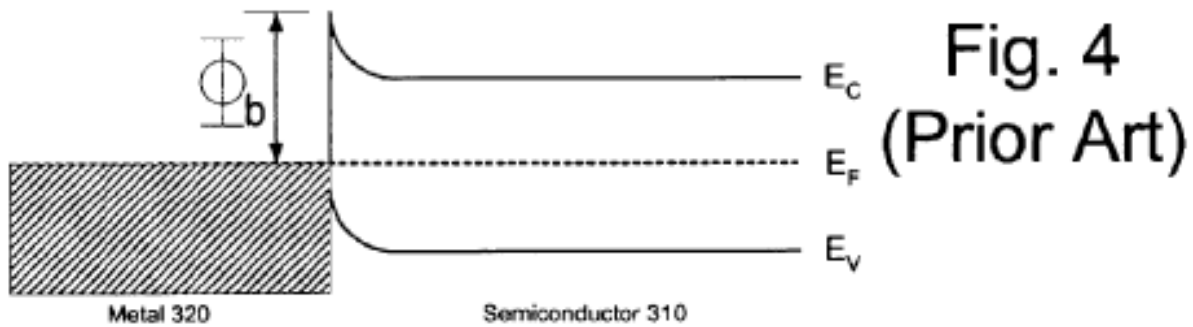


Fig. 7a

('395 Patent at Fig. 7a, 16:65-17:1.)

As Fig. 7a depicts, the pinned Fermi level E_F is not aligned with the conduction band edge E_C of the semiconductor at the interface. For an n-type semiconductor, the difference between the Fermi level E_F and the conduction band edge of the semiconductor E_C at the interface produces a barrier to the flow of electrons of height Φ_b , as shown in Fig. 4 of the '395 Patent:



(’395 Patent at Fig. 4, 4:49-50, 7:35-59; Schubert Decl. ¶ 49.)

“The importance of the barrier height at a metal-semiconductor interface is that it determines the electrical properties of the junction. Thus, if one were able to control or adjust the barrier height of a metal-semiconductor junction, one could produce electrical devices of desired characteristics.” (’395 Patent at 3:10-14.) According to the ’395 Patent, depinning a Fermi level is one technique for accomplishing that. (*Id.* at 16:36-57, Schubert Decl. ¶ 50.) But even before the earliest alleged priority date of the ’395 Patent, techniques for depinning a Fermi level and controlling barrier height were well-known, as were techniques for reducing specific contact resistance. (Schubert Decl. ¶¶ 51-53.)

Indeed, even before the earliest alleged priority date of the challenged claims in August 2002, the prior art was replete with examples of interface layers that depin a Fermi level by passivating the semiconductor surface (thereby satisfying dangling bonds and reducing Bardeen states) and reducing the effects of metal-induced gap states, including the examples described in the Goodnick, Rhoderick, and

Sobolewski references. (Schubert Decl. ¶¶ 52-55; Goodnick at 1; Rhoderick at 3, Sobolewski at 1.) It was similarly known that an interfacial oxide could reduce the barrier height of a metal-semiconductor junction. (Schubert Decl. ¶¶ 56-58; Risko at 1:43-50; Taubenblatt 1984 at 3.) Likewise, the prior art taught that an interface layer could reduce the specific contact resistance of a metal-semiconductor junction: for example, the 1976 Schroen patent, the 1989 Kim patent, and the 1999 Iwaguro patent application publication. (Schubert Decl. ¶¶ 59-63; Schroen at Abstract; Kim at 4:63-5:1, 5:27-30; Iwaguro at [0005]-[0006], [0012]-[0014].)

B. The Purported Invention of the '395 Patent

The purported invention of the '395 Patent, like the prior art, involves providing an interface layer between the metal and the semiconductor in a metal-semiconductor junction. ('395 Patent at 1:31-35.)

C. Prosecution History

The '395 Patent began as U.S. Patent App. No. 15/877,837 ("the '837 Application,") filed on January 23, 2018. (Ex. 1120, at 3-49.) It purports to claim a priority date of August 12, 2002 through a series of parent applications. ('395 Patent, at Cover, 1:8-27.) Each challenged claim was among the '837 Application's original claims. (Ex. 1120, at 39-42.) The Examiner initially rejected the claims over U.S. Patent App. Pub. No. 2014/0117465 to Huang and other references combined with Huang. (*Id.* at 122-129.) The Examiner said that Huang qualified as prior art

because the parent applications of the '395 Patent did not describe the pairing of “a semiconductor oxide or oxide of the semiconductor and a metal oxide or oxide of titanium in the interface layer.” (Ex. 1120, at 121.) The applicants disagreed, responding that the parent applications allegedly described pairing a titanium dioxide spacer layer with a passivation layer of a semiconductor oxide. (Ex. 1120, at 162-163.) The Examiner then allowed the claims, and the '837 Application then issued as the '395 Patent. (*Id.* at 174, 196.)

VII. Level of Ordinary Skill in the Art

Any of the following combinations of education and experience would have qualified someone as an ordinarily skilled artisan in the field of the '395 Patent:

- a Ph.D. in electrical engineering, physics, materials science, or chemical engineering, with two years of practical experience with semiconductor research and design;
 - a Master's degree in electrical engineering, physics, materials science, or chemical engineering, with four years of practical experience with semiconductor research and design; or
 - a Bachelor's degree in electrical engineering, physics, materials science, or chemical engineering, with six to eight years of practical experience with semiconductor research and design.
- (Schubert Decl. ¶¶ 70-71.)

Further, additional education could make up for less practical experience, and vice versa. (*Id.*)

VIII. Claim Construction

Petitioner construes two claim terms below. As for the remaining claim terms, the challenged claims are unpatentable under those remaining terms' ordinary and customary meanings. 37 C.F.R. § 42.100(b). The Board need not expressly construe any other term at this stage.¹

A. Claim 5: “depin a Fermi level of the metal electrical contact in the vicinity of the junction”

The term “depin a Fermi level of the metal electrical contact in the vicinity of the junction” in Claim 5 means “passivate the semiconductor surface and reduce the effects of metal-induced gap states in the semiconductor.” The specification consistently describes that depinning a Fermi level involves passivating the semiconductor surface and reducing the effects of metal-induced gap states in the semiconductor. ('395 Patent at 3:36-41, 10:56-64, 14:56-62, 15:27-42, 16:45-51, 17:12-20.)

¹ Petitioner reserves all rights to raise claim construction arguments and other arguments in the Acorn Litigation or other proceedings involving the '395 Patent. For example, Petitioner has not raised all of its challenges to the '395 Patent here, including invalidity under 35 U.S.C. § 112. Further, comparing the claims to the accused products in the Acorn Litigation may raise controversies that require claim construction in that litigation, but not here.

Although the specification often discusses those two features in the context of depinning a Fermi level of the **semiconductor**, the applicants indicated during prosecution of a parent application that those features also relate to depinning a Fermi level of a **conductor**, such as a metal. (Ex. 1102, at 245.) In remarks accompanying a claim amendment that changed “depin a Fermi level of the semiconductor” to “depin a Fermi level of the conductor,” the applicants stated: “the phrase ‘Fermi level of the semiconductor’ has been revised to read ‘Fermi level of the metal/conductor’ in claims 1, 19 and 57 to clarify the nature of the physics as explained at paragraph 70 of the specification as originally filed.” (*Id.*; *see also id.* at 29-30 (originally filed paragraph 70); Ex. 1103, at 14:27-50.) Original paragraph 70, in turn, describes reducing metal-induced gap states “to depin the metal and lower the Schottky barrier.” (Ex. 1102, at 29-30.) The original specification’s next paragraph states that Schottky barrier height can be adjusted by the selection of an appropriate passivation material. (*Id.* at 30; *see also* Ex. 1103, at 14:51-60.)

B. Claims 5 and 6: “specific contact resistivity”

An ordinarily skilled artisan would have understood that “specific contact resistivity” and “specific contact resistance” are interchangeable in the context of the ’395 Patent. Indeed, the ’395 Patent appears to use those terms interchangeably: the specification discusses specific contact resistance, but the claims recite specific contact resistivities. (*E.g.*, ’395 Patent at 3:25-29, 3:42-45, 3:52-53, 4:22-30.) The

interchangeable use of those terms was also common (if not universal) in the field.

(Carver at 2; *see also* Schubert Decl. ¶¶ 74-76.)

IX. Overview of the Prior Art

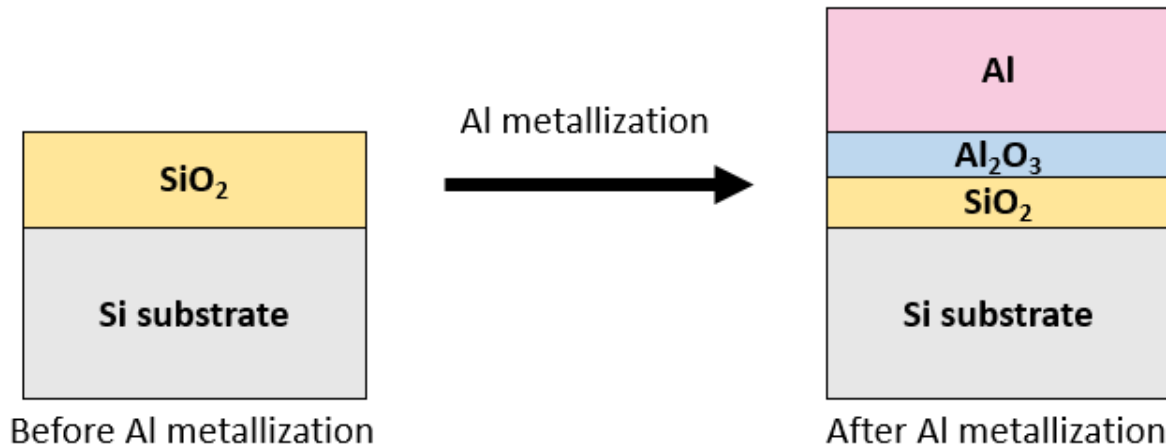
A. Goodnick (Ex. 1121)

Goodnick describes a series of experiments “to observe the influence of thin SiO₂ layers on the chemical formation of metal-silicon contacts.” (Goodnick at 1.)

Goodnick discloses that a thin interfacial oxide can satisfy dangling silicon bonds, thereby depinning a Fermi level. (*Id.*) Goodnick also teaches that “the presence of a thin oxide at the interface acts as a passivating influence, both from an electronic and a chemical standpoint.” (*Id.*)

Goodnick also describes forming an Al – Al₂O₃ – SiO₂ – Si contact by thermally evaporating aluminum onto a 30 Å silicon dioxide (SiO₂) layer grown on an n-type doped silicon (Si) substrate. (Goodnick at 1-2, 5.)² The aluminum (Al) partially reduces the SiO₂ to form Al₂O₃ and free silicon in a self-limiting reaction, yielding an Al₂O₃ – SiO₂ interface layer between the aluminum and the silicon substrate. (*Id.* at 5.) A schematic depiction of Goodnick’s metallization process and the resulting Al – Al₂O₃ – SiO₂ – Si contact appears below:

² One angstrom (Å) is equal to 0.1 nanometers (nm). Thus, 30 Å converts to 3 nm.



(Goodnick at 1-2, 5; Schubert Decl. ¶¶ 80-86.)

B. Jammy (Ex. 1122)

Jammy generally describes a MOSFET (metal oxide semiconductor field effect transistor) that incorporates a “quantum conductive barrier” interface layer between a conductive stud and a semiconductor substrate, as depicted below:

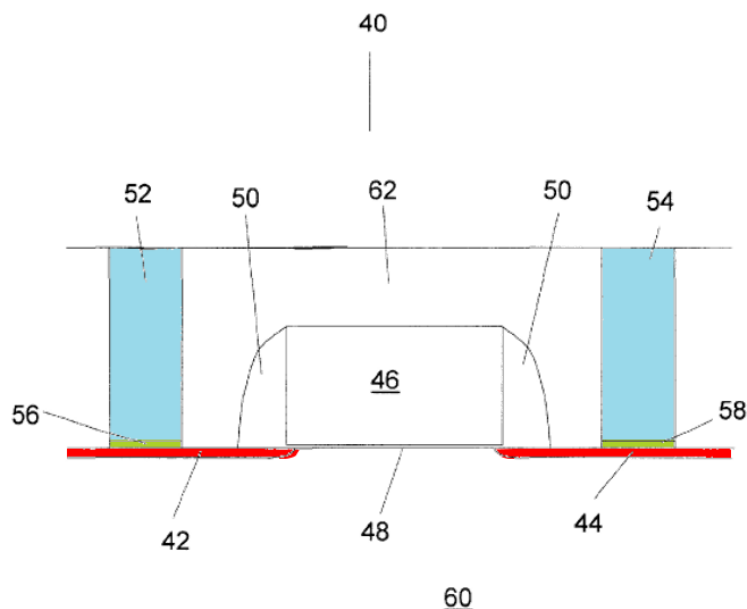


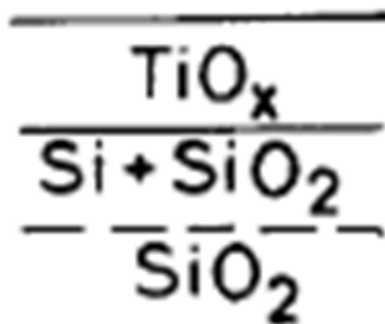
Figure 1

(Jammy at Fig. 1 (annotations added) Jammy at 2:42-53; 3:16-22.)

Jammy states that “FIG. 1 shows a schematic side view of a MOSFET 40 in a substrate 60. Shallow **source/drain diffusions (doped regions) 42 and 44** are formed in substrate 60. . . . **Conductive studs 52 and 54** contact **diffusions 42 and 44** through **quantum conductive barrier layers 56 and 58** respectively.” (Jammy at 4:9-17.) Jammy discloses forming those **source/drain diffusions** by implanting n-type dopants into a silicon substrate. (Jammy at 4:33-38.)

C. Taubenblatt 1982 (Ex. 1123)

Taubenblatt 1982 describes the interface layers that form when titanium is deposited on layer of SiO₂ (silicon dioxide) on an n-type silicon substrate and annealed. (Taubenblatt 1982 at 2, 7-8.) Taubenblatt 1982 discloses that when titanium is deposited on top of a layer of SiO₂ thicker than 20 Å, and the resulting structure is annealed at 700°C – 900°C, the TiO_x (titanium oxide) – SiO₂ interface layer depicted below forms between the titanium and the silicon:



(Taubenblatt 1982 at 7; *see also id.* at 8.)

As Taubenblatt 1982 describes, “in the reaction of Ti with a thicker SiO₂ layer, Ti oxide forms, which can act as a diffusion barrier to prevent further reduction of

the oxide by unreacted Ti metal or in the formation of silicide.” (Taubenblatt 1982 at 8.) Thus, once the TiO_x layer forms, it prevents subsequent reactions between the titanium and the SiO_2 , leaving a layer of unreacted Ti metal atop the TiO_x layer. (*Id.*; Schubert Decl. ¶¶ 94-97.)

D. Chang (Ex. 1124)

Chang generally addresses specific contact resistance for “various metals on silicon samples” (Chang at 1.) Chang describes that at doping levels above 10^{18} dopant atoms / cm^3 , specific contact resistance “becomes a strong function of doping,” decreasing as doping increases. (*Id.* at 4-5.) Chang also explains that the specific contact resistance of an electrical junction decreases as its barrier height decreases. (*Id.* at 6.) Finally, Chang describes a doping concentration as high as 10^{21} dopant atoms / cm^3 for n-type doped silicon. (*Id.* at 7 (Fig. 5).)

E. Kim (Ex. 1125)

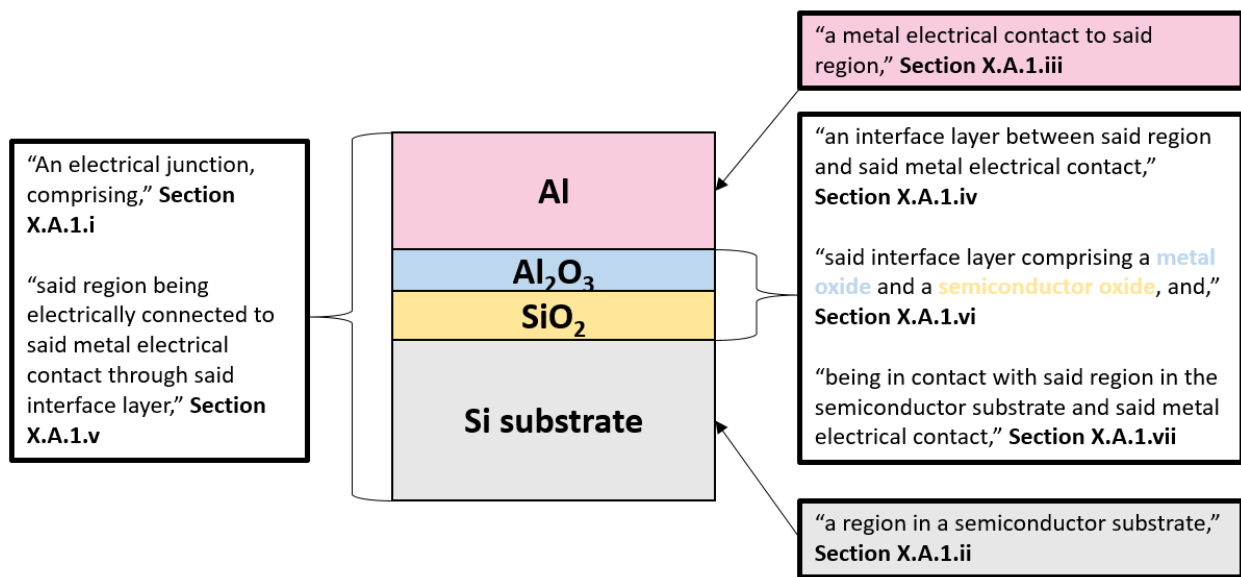
Kim generally describes a low resistance contact between a titanium-tungsten alloy and silicon with an interface layer therebetween, the interface layer including titanium dioxide. (Kim at 4:59-5:4.) The titanium in the tungsten-titanium alloy reduces native silicon dioxide present on the silicon to form silicon and titanium dioxide, which reduces the interface resistance. (*Id.* at 4:63-5:4.) Kim describes achieving a specific contact resistance as low as $8 \Omega\text{-}\mu\text{m}^2$ for a junction between that alloy and n-type doped silicon. (*Id.* at 5:27-30.)

X. The challenged claims are unpatentable.

A. Ground 1: Goodnick anticipates Claims 1-3 and 8-10.

1. Claim 1

As discussed above in **Section IX.A**, Goodnick discloses an Al – Al₂O₃ – SiO₂ – Si contact. (Goodnick at 1-2, 5.) That contact meets every limitation of Claim 1, as summarized by the below graphic:



(Goodnick at 1-2, 5; Schubert Decl. ¶ 118.)

i. An electrical junction, comprising

To the extent the preamble is limiting, Goodnick discloses it. (Schubert Decl. ¶ 119.) As discussed above in **Section IX.A**, Goodnick discloses an Al – Al₂O₃ – SiO₂ – Si contact. (Goodnick at 1-2, 5.) That contact is an electrical junction as described and claimed in the '395 Patent. Indeed, the specification of the '395 Patent

uses the terms “contact” and “junction” broadly and interchangeably. (*E.g.*, ’395 Patent at 1:45-48, 8:5-20, 13:20-23, 17:41-44.)

ii. a region in a semiconductor substrate,

Goodnick discloses this limitation. (Schubert Decl. ¶ 122.) In particular, Goodnick discloses a silicon substrate. (Goodnick at 1; Schubert Decl. ¶ 122.) “The silicon substrates used in this study were commercial single crystal (100) wafers, phosphorous doped to 10^{15} cm^{-3} .” (Goodnick at 1.)

iii. a metal electrical contact to said region, and

Goodnick discloses this limitation. (Schubert Decl. ¶ 123.) In particular, Goodnick addresses the “chemical formation of metal-silicon contacts” and Goodnick discloses aluminum as an example of a metal electrical contact. (Goodnick at 1; Schubert Decl. ¶ 123.) Specifically, Goodnick describes forming a metal-silicon contact by evaporating aluminum (Al) onto a 30 Å layer of SiO₂ grown on a cleaned silicon substrate. (Goodnick at 1-2, 5.)

iv. an interface layer between said region and said metal electrical contact,

Goodnick discloses this limitation. (Schubert Decl. ¶ 124.) Goodnick describes forming a metal-silicon contact by evaporating aluminum (Al) onto a 30 Å layer of SiO₂ grown on a cleaned silicon substrate. (Goodnick at 1-2.) According to Goodnick, that process produced an Al₂O₃ - SiO₂ interface layer between the silicon substrate and the aluminum. (Goodnick at 5; Schubert Decl. ¶ 124.)

v. said region being electrically connected to said metal electrical contact through said interface layer and

Goodnick discloses this limitation. (Schubert Decl. ¶ 125.) “The focus of the present investigation has been to observe the influence of thin SiO₂ layers on the chemical formation of metal-silicon contacts.” (Goodnick at 1.) For its aluminum metallization, Goodnick discloses that “both SiO₂ and Al₂O₃ existed simultaneously at the interface” (*Id.* at 5.) That Goodnick characterizes its Al – Al₂O₃ – SiO₂ – Si contact as a “metal-silicon contact” indicates that the silicon substrate (semiconductor region) is electrically connected to the aluminum (metal electrical contact) through the Al₂O₃ – SiO₂ interface layer. (Schubert Decl. ¶ 126.) Confirming that electrical connection, Goodnick describes its interfacial oxide layers as “thin,” and states that “an oxide layer that is sufficiently thin may sustain considerable current via tunneling.” (Goodnick at 1; Schubert Decl. ¶ 126.)

vi. said interface layer comprising a metal oxide and a semiconductor oxide, and

Goodnick discloses this limitation. (Schubert Decl. ¶ 127.) “The results indicated that both SiO₂ and Al₂O₃ existed simultaneously at the interface, implying that the reaction is self-limiting, even at elevated temperatures. This is probably a result of the diffusion barrier formed by the Al₂O₃ layer to the transport of Al to the SiO₂ layer.” (Goodnick at 5.)

vii. being in contact with said region in the semiconductor substrate and said metal electrical contact.

Goodnick discloses this limitation. (Schubert Decl. ¶ 128.) Goodnick describes thermally evaporating aluminum (a metal electrical contact) onto an SiO₂ layer grown on a silicon substrate (semiconductor region). (Goodnick at 1-2, 5; Schubert Decl. ¶ 128.) Although the aluminum partially reduced the SiO₂ to produce Al₂O₃, some of the SiO₂ layer grown on the silicon surface remained, “probably a result of the diffusion barrier formed by the Al₂O₃ layer to the transport of Al to the SiO₂ layer.” (Goodnick at 5.) The remaining portion of the SiO₂ layer grown on the silicon substrate would have been in contact with the silicon substrate. (*Id.* at 1-2; Schubert Decl. ¶ 129.) And, because the interface layer’s Al₂O₃ layer forms a diffusion barrier against the “the transport of Al to the SiO₂ layer,” evaporated aluminum would have remained atop and in contact with the interface layer’s Al₂O₃ layer. (Goodnick at 5; Schubert Decl. ¶ 130.)

2. Claim 2

i. The electrical junction of claim 1,

See **Section X.A.1.** (Schubert Decl. ¶ 132.)

ii. wherein the semiconductor oxide comprises an oxide of the region in the semiconductor substrate.

Goodnick discloses this limitation. (Schubert Decl. ¶ 133.) As discussed above in **Sections X.A.1.iv, X.A.1.vi, and X.A.1.vii**, Goodnick discloses thermally

growing a layer of SiO₂ on a silicon substrate. (Goodnick at 1-2.) After metallization, “[t]he results indicated that both SiO₂ and Al₂O₃ existed simultaneously at the interface, implying that the reaction is self-limiting, even at elevated temperatures.” (*Id.* at 5.) The SiO₂ remaining on the silicon substrate is an oxide of that silicon substrate, *i.e.*, of that semiconductor region. (Schubert Decl. ¶ 133.)

3. Claim 3

i. The electrical junction of claim 2,

See **Section X.A.2.** (Schubert Decl. ¶ 135.)

ii. wherein the semiconductor oxide has a thickness of approximately 0.1 nm to 5 nm.

Goodnick discloses this limitation. (Schubert Decl. ¶ 136.) Goodnick describes thermally growing a 30 Å (3 nm)³ thick layer of SiO₂ on a silicon substrate. (Goodnick at 1-2.) As discussed above with respect to Claim 2 in **Section X.A.2.ii**, some of that SiO₂ layer is partially reduced by aluminum to produce Al₂O₃, but an SiO₂ layer nonetheless remains on the silicon substrate. (*Id.* at 5.) The minimum possible thickness of the remaining SiO₂ layer is 0.2 nm, which is the thickness of a monolayer of SiO₂, *i.e.*, a layer one SiO₂ molecule thick. (Verhaverbeke at [0004];

³ One Angstrom (Å) is equivalent to 0.1 nanometers (nm).

Schubert Decl. ¶ 136.) Thus, the thickness of Goodnick's post-metallization SiO₂ layer is between 0.2 nm and its original 3 nm, satisfying this limitation.

4. Claim 8

i. The electrical junction of claim 1,

See **Section X.A.1.** (Schubert Decl. ¶ 138.)

ii. wherein said metal oxide comprises an oxide of said metal electrical contact.

Goodnick discloses this limitation. (Schubert Decl. ¶ 139.) Goodnick describes forming a metal-silicon contact by evaporating aluminum (Al) onto a 30 Å layer of SiO₂ grown on a cleaned silicon substrate. (Goodnick at 1-2.) That produced an interface layer that includes aluminum oxide (Al₂O₃), an oxide of Goodnick's aluminum metal electrical contact as discussed above in **Sections X.A.1.iii and X.A.1.iv.** (*Id.* at 5; Schubert Decl. ¶ 139.)

5. Claims 9 and 10

Claims 9 and 10 are identical and addressed together below.

i. The electrical junction of claim 8,

See **Section X.A.4.** (Schubert Decl. ¶ 141.)

ii. wherein said semiconductor oxide comprises an oxide of the region in the semiconductor substrate.

See **Section X.A.2.ii.** (Schubert Decl. ¶ 142.)

B. Ground 2: Goodnick in view of Jammy renders Claim 4 obvious.

1. Combination of Goodnick and Jammy

As discussed above in **Section X.A.1.ii**, Goodnick discloses a semiconductor region in a substrate. (Goodnick at 1.) Further, Goodnick discloses growing a thin SiO₂ layer on a cleaned, phosphorus-doped silicon substrate, which is an n-type doped silicon semiconductor region. (*Id.* at 1-2; Yu at 1:53-55, 4:19-21; Schubert Decl. ¶ 143.) But, Goodnick does not expressly disclose that its silicon substrate “comprises a source or drain of a transistor” as recited in Claim 4.

Jammy, on the other hand, discloses a source or drain of a transistor formed in a silicon substrate. Jammy describes a semiconductor device called a MOSFET, which is a metal oxide semiconductor field effect transistor. (Jammy at 4:1-4, 4:9-11; Schubert Decl. ¶ 144.) The MOSFET includes a silicon substrate in which source/drain diffusions (doped regions) are formed. (Jammy at 4:9-12, 4:36-38.) Similar to Goodnick’s disclosure of growing an SiO₂ layer on a cleaned silicon substrate, Jammy discloses cleaning the exposed source/drain diffusions regions on the silicon substrate before forming an interface layer thereon. (Jammy at 5:32-37.)

An ordinarily skilled artisan would have found it obvious to form Goodnick’s Al – Al₂O₃ – SiO₂ – Si contact as described for Claim 1 in **Section X.A.1** using Jammy’s silicon source or drain of a transistor as the semiconductor region. (Schubert Decl. ¶ 145.) That combination would have involved growing Goodnick’s

30 Å thick layer of SiO₂ on Jammy's cleaned source/drain diffusion regions, then depositing aluminum on the SiO₂ layer as described in Goodnick. (Goodnick at 1-2, 5; Jammy at 4:9-12, 4:36-38, 5:32-37.) An ordinarily skilled artisan would have expected that combination to produce the same Al – Al₂O₃ – SiO₂ – Si structure described in Goodnick; swapping Goodnick's silicon substrate for Jammy's source or drain of a transistor in a silicon substrate would not have changed the structure or function of the resulting Al₂O₃ – SiO₂ interface layer. (Schubert Decl. ¶ 145.) And, that substrate swap would have been a simple substitution with a predictable result, a recognized rationale for combining references. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 418 (2007).

Further, an ordinarily skilled artisan would have combined Goodnick and Jammy because their teachings fit “together like pieces of a puzzle.” *KSR*, 550 U.S. at 420-421. (Schubert Decl. ¶ 146.) Goodnick describes contact metallization processes that it suggests for use in semiconductor devices, and Jammy describes a semiconductor device. (Goodnick at 1; Jammy at 4:1-4, 4:9-11.) Jammy identifies alumina (aluminum oxide) as an example of a suitable interface layer, and Goodnick discloses a technique for forming an aluminum oxide interface layer, as discussed above in **Section X.A.1.vi**. (Ex. 1122 [Jammy] at 3:55-58; Goodnick at 1-2, 5.) Jammy also suggests the use of an interface layer that “prevent[s] or slow[s] diffusion of chemical species from one side of the layer to the other,” and

Goodnick's aluminum oxide layer forms a diffusion barrier that prevents aluminum on one side of that layer from penetrating through to silicon dioxide and silicon on the other side. (Jammy at 3:27-29; Goodnick at 5; Schubert Decl. ¶ 146.) Each of those reasons also would have prompted an ordinarily skilled artisan to combine Goodnick and Jammy as described above. And, that combination teaches every limitation of Claim 4.

2. Claim 4

i. The electrical junction of claim 1,

See **Section X.A.1.** (Schubert Decl. ¶ 149.)

ii. wherein said region in the semiconductor substrate comprises a source or drain of a transistor.

Jammy discloses this limitation. (Schubert Decl. ¶ 150.) Jammy describes a MOSFET (metal oxide semiconductor field effect transistor) that includes a silicon substrate in which source/drain diffusions (doped regions) are formed, such as by diffusing an n-type dopant into the substrate. (Jammy at 4:1-4, 4:9-12, 4:36-38.)

C. Ground 3: Goodnick renders Claim 5 obvious.

1. Claim 5

i. The electrical junction of claim 1,

See **Section X.A.1.** (Schubert Decl. ¶ 152.)

ii. wherein said interface layer has a thickness sufficient to depin a Fermi level of the metal electrical contact in a vicinity of the junction

Goodnick discloses this limitation. (Schubert Decl. ¶ 153.) An interface layer that depins a Fermi level of the metal electrical contact in a vicinity of the junction by definition has “a thickness sufficient to depin a Fermi level of a metal electrical contact in a vicinity of the junction.” See *Geneva Pharm., Inc. v. GlaxoSmithKline PLC*, 349 F.3d 1373, 1384 (Fed. Cir. 2003) (“[A] functional limitation covers all embodiments performing the recited function.”). And Goodnick discloses an interface layer that depins a Fermi level of the metal electrical contact in a vicinity of the junction. (Schubert Decl. ¶¶ 153-154.)

According to Goodnick, even “a thin interfacial oxide” can cause the Fermi level to become unpinned. (Goodnick at 1; Schubert Decl. ¶ 155.) The $\text{Al}_2\text{O}_3 - \text{SiO}_2$ interface layer in Goodnick’s $\text{Al} - \text{Al}_2\text{O}_3 - \text{SiO}_2 - \text{Si}$ contact indeed “depin[s] a Fermi level of the metal electrical contact in a vicinity of the junction” as construed.

Goodnick discloses an interface layer that passivates the surface of the semiconductor.

As discussed above in **Section X.A.1.iv**, Goodnick’s $\text{Al} - \text{Al}_2\text{O}_3 - \text{SiO}_2 - \text{Si}$ contact has a thin $\text{Al}_2\text{O}_3 - \text{SiO}_2$ interfacial oxide layer that includes a layer of thermally grown SiO_2 on the silicon substrate. (Goodnick at 1-2, 5; Schubert Decl. ¶ 156.) Goodnick discloses that “the presence of a thin oxide at the interface acts as a passivating influence, both from an electronic and a chemical standpoint.”

(Goodnick at 1.) Goodnick discloses that “[a] thin interfacial oxide also may significantly reduce the density of interface states by satisfying silicon dangling bonds,” which is an example of passivation in the ’395 Patent. (Goodnick at 1; ’395 Patent at 7:59-67; 9:37-42.) And, it was known that growing SiO₂ on a silicon surface, as in Goodnick, would passivate that silicon surface by satisfying dangling bonds, as even the ’395 Patent admits. (’395 Patent at 8:24-37; Goodnick at 1-2; Taubenblatt 1984 at 3; Schubert Decl. ¶¶ 157-161.) Thus, Goodnick discloses an Al₂O₃ – SiO₂ interfacial oxide layer, whose SiO₂ passivates the surface of the silicon substrate. (Schubert Decl. ¶ 162.)

Goodnick’ interface layer also reduces the effect of metal-induced gap states in the semiconductor.

Goodnick’s Al₂O₃ – SiO₂ interfacial oxide layer would have reduced the probability of an aluminum electron’s wave function penetrating from the aluminum through the interface layer and into the semiconductor—which penetration is the cause of metal-induced gap states—to less than 1 in 703 million, as Dr. Schubert has calculated. (Schubert Decl. ¶¶ 163-179.) That would have reduced if not substantially eliminated the effects of metal-induced gap states in the semiconductor. (*Id.*) Further, it was known that interfacial oxide layers reduce the influence of metal electron wave functions on states in the semiconductor. (Rhoderick at 3; Sobolewski at 1; Schubert Decl. ¶¶ 180-182.)

* * *

Thus, Goodnick discloses an $\text{Al}_2\text{O}_3 - \text{SiO}_2$ interface layer that both passivates the silicon substrate's surface and reduces the effects of metal-induced gap states in the silicon substrate, thereby "depin[ning] a Fermi level of the metal electrical contact in a vicinity of the junction" as construed herein. (*Id.* at 1; Rhoderick at 3; Sobolewski at 1; Taubenblatt 1984 at 3.) Goodnick therefore discloses an interface layer having a thickness sufficient to depin a Fermi level of the metal electrical contact in a vicinity of the junction. (Schubert Decl. ¶¶ 182-183.)

- iii. **yet thin enough to provide the junction with a specific contact resistivity that is generally dependent on: a workfunction of the metal electrical contact, a Fermi energy of the semiconductor in the region, or both the workfunction of the metal electrical contact and the Fermi energy of the semiconductor in the region.**

This limitation would have been obvious over Goodnick. (Schubert Decl. ¶ 184.) Because this limitation recites a list of alternatives, it is satisfied by prior art addressing any alternative. Here, Goodnick renders obvious an interface layer thin enough to provide the junction with a specific contact resistivity that is generally dependent on a workfunction of the metal electrical contact.

Goodnick discloses an $\text{Al} - \text{Al}_2\text{O}_3 - \text{SiO}_2 - \text{Si}$ contact whose barrier height generally depends on the workfunction of the aluminum. As discussed above in **Section X.C.1.ii**, Goodnick's $\text{Al}_2\text{O}_3 - \text{SiO}_2$ interface layer depins the Fermi level of the conductor, such that Goodnick's $\text{Al}_2\text{O}_3 - \text{SiO}_2$ interface layer provides a "barrier

height [that] is more directly determined by the metal work function.” (Goodnick at 1; *see also* Sobolewski at 1; Taubenblatt 1984 at 3; Schubert Decl. ¶¶ 185-186.)

Because the barrier height of that contact generally depends on the workfunction of the aluminum, an ordinarily skilled artisan would have inferred that the contact’s specific contact resistivity also generally depends on the workfunction of the aluminum, as specific contact resistivity depends on barrier height. (Schubert Decl. ¶¶ 186-195; Chang at 2, 4.) Finally, because “a functional limitation covers all embodiments performing the recited function,” an ordinarily skilled artisan would have inferred that the interface layer is by definition thin enough to provide the junction with a specific contact resistivity that is generally dependent on a workfunction of the metal electrical contact. *Geneva Pharm.*, 349 F.3d at 1384; *see also In re Preda*, 401 F.2d 825, 826 (CCPA 1968) (holding that an obviousness encompasses an ordinarily skilled artisan’s inferences about a reference).

Even if Goodnick purportedly must teach some specific thinness to satisfy this limitation—*Geneva Pharmaceuticals* notwithstanding—Goodnick discloses that “[i]f the oxide is too thick, current flow in the resulting device may be severely suppressed, accompanied by a loss of rectifying characteristics. However, an oxide layer that is sufficiently thin may sustain considerable current via tunneling.” (Goodnick at 1; *see also* Schubert Decl. ¶ 196.) That disclosure, coupled with the fact that Goodnick renders obvious an interface layer that actually provides “a

specific contact resistivity that is generally dependent on a workfunction of the metal electrical contact,” confirms the obviousness of an interface layer “yet thin enough to provide the junction with a specific contact resistance that is generally dependent on the workfunction of the conductor.”

Finally, to the extent the Board finds that limitation inherent in Goodnick in addition to or instead of obvious over Goodnick—which would mean that Goodnick fully discloses every limitation of Claim 5—it would remain appropriate to hold Claim 5 at least obvious over Goodnick. Indeed, “anticipation is the epitome of obviousness.” *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1373 (Fed. Cir. 2019) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)).

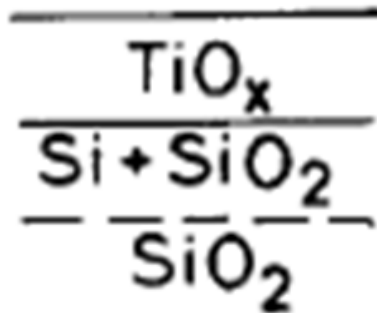
D. Ground 4: Goodnick in view of Taubenblatt 1982 renders Claims 1, 11, 12, 15, 23-25, and 28 obvious.

1. Combination of Goodnick and Taubenblatt 1982

As discussed above in **Sections IX.A and X.A.1**, Goodnick describes growing a 30 Å layer of SiO₂ on an n-type silicon substrate, then depositing aluminum on that layer of SiO₂ to form an Al – Al₂O₃ – SiO₂ – Si contact. (Goodnick at 1-2, 5) Goodnick, however, does not expressly disclose an interface layer that includes a titanium oxide (as in Claims 11, 23, and their dependent claims) or a metal electrical contact that includes titanium (as in Claims 15, 24, and their dependent claims)

But, an ordinarily skilled artisan could have provided and would have been motivated to provide Goodnick with an interface layer that includes both titanium oxide and silicon dioxide using the combined teachings of Goodnick and Taubenblatt 1982. Below, Petitioner first explains **how** to form that interface layer using Goodnick and Taubenblatt 1982, and then **why** an ordinarily skilled artisan would have been motivated to do so.

Starting with the “how,” Taubenblatt 1982 discloses a technique for forming an interface layer between titanium and silicon, which interface layer includes both a titanium oxide (TiO_x), which is a metal oxide, and silicon dioxide (SiO_2), which is a semiconductor oxide:



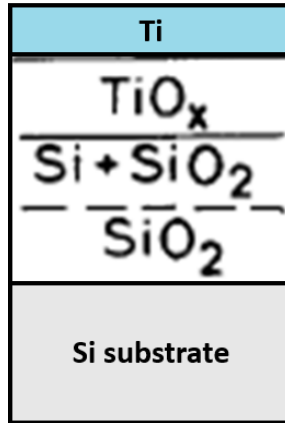
(Taubenblatt 1982 at 7; *see also id.* at 8.)

In particular, Taubenblatt 1982 discloses that when titanium is deposited on a layer of SiO_2 thicker than 20 Å (2 nm) and annealed at temperatures between 700°C – 900°C, the TiO_x – SiO_2 interface layer depicted above forms. (Taubenblatt 1982 at 7-8; Schubert Decl. ¶¶ 198-201.) Taubenblatt 1982 describes that “in the reaction of Ti with a thicker SiO_2 layer, Ti oxide forms, which can act as a diffusion barrier

to prevent further reduction of the oxide by unreacted Ti metal or in the formation of silicide.” (Taubenblatt 1982 at 8.) Thus, once the TiO_x layer forms, it prevents subsequent reactions between the titanium and the SiO_2 , leaving a layer of unreacted Ti metal atop the TiO_x layer. (*Id.*; Schubert Decl. ¶ 202.)

To provide the initial layer of SiO_2 thicker than 20 Å for the Taubenblatt 1982 technique, Goodnick teaches thermally growing a 30 Å-thick layer of SiO_2 on a silicon substrate. (Goodnick at 1-2.) And to provide the titanium, Taubenblatt 1982 describes depositing titanium on a silicon dioxide layer. (Taubenblatt 1982 at 7-8.) With Taubenblatt 1982’s titanium deposited on Goodnick’s 30 Å-thick layer of thermally grown SiO_2 , all that it would have taken to form a TiO_x – SiO_2 interface layer is annealing at 700°C – 900°C as described in Taubenblatt 1982. (Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 203.) And annealing was a common and necessary processing step for semiconductor devices; indeed, the prior art describes “[p]ost-deposition processing, such as annealing” as “critical for typical device fabrication” (Taubenblatt 1984 at 1; Schubert Decl. ¶ 203.)

In sum, an ordinarily skilled artisan could have readily applied the teachings of Goodnick and Taubenblatt 1982 to form a TiO_x – SiO_2 interface layer as taught in Taubenblatt 1982 between Goodnick’s silicon substrate and Taubenblatt 1982’s titanium. The result of that combination is depicted schematically below:



(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 204.)

As for “why,” an ordinarily skilled artisan would have been motivated to form the $\text{TiO}_x - \text{SiO}_2$ interface layer according to the combined teachings of Goodnick and Taubenblatt 1982 as an interface layer between Taubenblatt 1982’s titanium and Goodnick’s n-type silicon substrate because that interface layer would have been expected to reduce the specific contact resistivity of that junction. (Schubert Decl. ¶¶ 205-206.) Indeed, the prior art was replete with examples of interface layers that reduce specific contact resistivity. (*Id.* ¶ 206; Schroen at Abstract; Kim at 4:63-5:1, 5:27-30; Iwaguro at [0005]-[0006], [0012]-[0014].)

The $\text{TiO}_x - \text{SiO}_2$ interface layer formed according to the combined teachings of Goodnick and Taubenblatt 1982 would have been yet another entry in the canon of interface layers that reduce specific contact resistivity. In particular, it was known that an SiO_2 interface layer grown on silicon will passivate the surface of the silicon. (Goodnick at 1; Taubenblatt 1984 at 3; Schubert Decl. ¶ 207.) That passivation would have reduced the barrier height of a titanium to n-type silicon junction, such

as the junction between Taubenblatt's titanium Goodnick's n-type source/drain silicon substrate. (Taubenblatt 1984 at 3; Goodnick at 1-2; Schubert Decl. ¶ 207.)

For a junction between titanium and n-type silicon with an SiO₂ interface layer, the SiO₂ interface layer produces a net reduction of barrier height of more than 0.1 eV owing to the passivation that the SiO₂ interface layer provides. (Taubenblatt 1984 at 3.) And, reducing the barrier height of a junction reduces its specific contact resistivity. (Chang at 5-6; Schubert Decl. ¶ 207.)

By depositing titanium on the SiO₂ layer and annealing to convert part of that SiO₂ interface layer to a titanium oxide—while still leaving enough SiO₂ to passivate the silicon surface—specific contact resistivity will decrease further. (Schubert Decl. ¶ 208.) While titanium oxides modestly passivate silicon surfaces—and therefore modestly reduce the junction's barrier height—they present less resistance to current than SiO₂ does. (Rohatgi at 2-3; Kim at 4:63-5:1; Schubert Decl. ¶ 208.) Thus, converting some of the interface layer's SiO₂ to a titanium oxide would have decreased specific contact resistivity further. (Kim at 4:63-5:1; Schubert Decl. ¶ 208.) But, an ordinarily skilled artisan still would have wanted to leave **some** SiO₂ remaining in the interface layer to obtain the barrier-height reducing benefits of a passivating layer of SiO₂. (Taubenblatt 1984 at 3; Schubert Decl. ¶ 209.)

The desire to provide a low-resistance interface layer that also passivates the surface of the silicon would have led an ordinarily skilled artisan to the TiO_x – SiO₂

layer in Taubenblatt 1982. (Schubert Decl. ¶ 210.) In particular, Taubenblatt 1982 discloses an interface layer with an SiO₂ passivating layer that remains in contact with the silicon after titanium deposition and annealing at 700°C-900°C: “in the reaction of Ti with a thicker SiO₂ layer, Ti oxide forms, which can act as a diffusion barrier to prevent further reduction of the oxide by unreacted Ti metal or in the formation of silicide.” (Taubenblatt 1982 at 8.) And, the combination of a thicker (> 20 Å) silicon dioxide layer (such as the 30 Å layer taught in Goodnick) and annealing at 700°C-900°C was proven to produce a TiO_x – SiO₂ interface layer. (Taubenblatt 1982 at 7; *see also* Goodnick at 1-2; Schubert Decl. ¶ 210.)

That TiO_x – SiO₂ interface layer combines the barrier-height-lowering of a passivating layer of SiO₂ with the lower resistance of a layer of titanium oxide. (Taubenblatt 1982 at 7-8; Kim at 4:63-5:1; Schubert Decl. ¶ 211.) Thus, Taubenblatt 1982’s TiO_x – SiO₂ interface layer would have delivered the “best of both worlds” for reducing the specific contact resistivity of a junction between Taubenblatt 1982’s titanium and Goodnick’s n-type silicon substrate: the passivating benefits of silicon dioxide for reducing barrier height; and the lower resistance to electrical current of a titanium oxide.

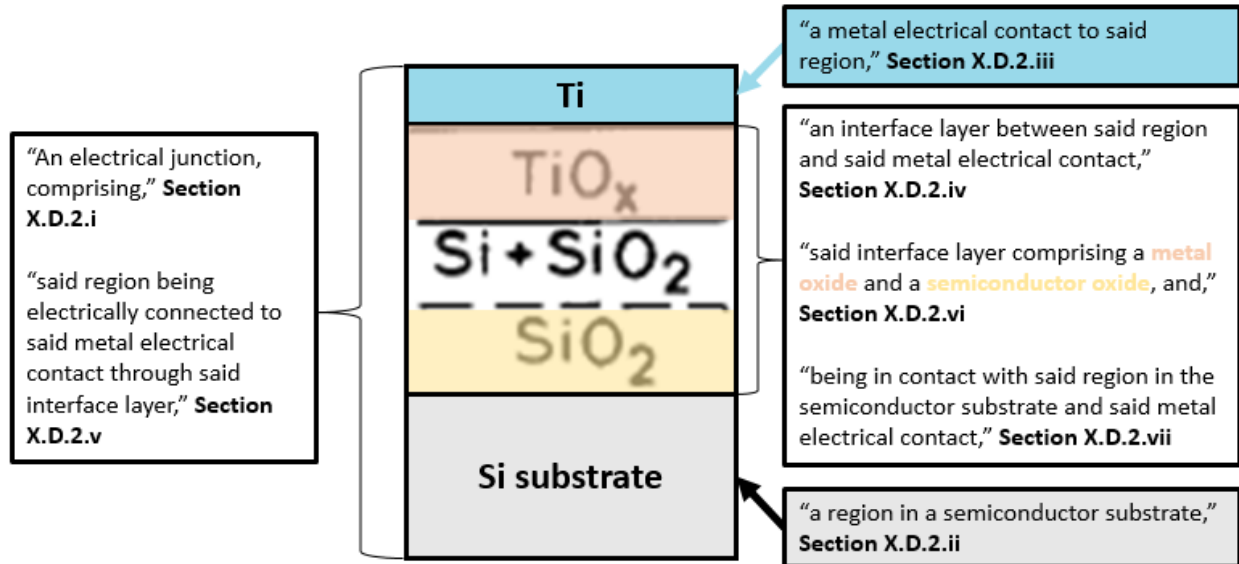
Further, an ordinarily skilled artisan would have expected that TiO_x – SiO₂ interface layer to present less electrical resistance than that presented by Goodnick’s Al₂O₃ – SiO₂ interface layer. (Schubert Decl. ¶ 213.) In particular, titanium

dioxide—the oxide of titanium most likely to form when titanium reacts with silicon dioxide—provides a lower resistance than aluminum oxide. (*Id.* ¶ 214.) And, an ordinarily skilled artisan would have sought to provide an interface layer that reduces specific contact resistivity to reduce the power consumption of a device incorporating a contact with that interface layer. (Takahashi at 4:57-59; Schubert Decl. ¶ 215.)

Finally, turning to reasonable expectation of success, forming a $\text{TiO}_x - \text{SiO}_2$ interface layer described in Taubenblatt 1982 by depositing titanium on the thermally grown 30 Å SiO_2 layer in Goodnick and annealing as described in Taubenblatt 1982 would have required nothing more than well-known, conventional semiconductor processing steps. (Schubert Decl. ¶ 216; Goodnick at 1; Taubenblatt 1982 at 7-8; Taubenblatt 1984 at 1.)

2. Claim 1

As discussed above in **Section X.D.1**, the combined teachings of Goodnick and Taubenblatt 1982 yield a $\text{Ti} - \text{TiO}_x - \text{SiO}_2 - \text{Si}$ contact. (Goodnick at 1-2, 5; Taubenblatt 1982 at 7-8.) That contact meets every limitation of Claim 1, as summarized by the below graphic:



(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 217.)

i. An electrical junction, comprising

To the extent the preamble is limiting, it is obvious over Goodnick in view of Taubenblatt 1982. (Schubert Decl. ¶ 218.) Goodnick in view of Taubenblatt 1982 renders obvious a Ti – TiO_x – SiO₂ – Si contact, as discussed above in **Section X.D.1**. (Schubert Decl. ¶ 218.) That contact is an electrical junction for the reasons discussed above in **Section X.A.1**: namely, the '395 Patent uses the terms “junction” and “contact” interchangeably. (*Id.*)

ii. a region in a semiconductor substrate,

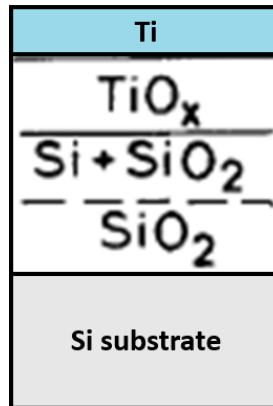
See **Section X.A.1.ii**. (Schubert Decl. ¶ 219.)

iii. a metal electrical contact to said region, and

This limitation would have been obvious over Goodnick in view of Taubenblatt 1982. (Schubert Decl. ¶ 220.) The combination discussed above in

Section X.D.1 would have yielded a **titanium** metal electrical contact as part of a

Ti – TiO_x – SiO₂ – Si contact:



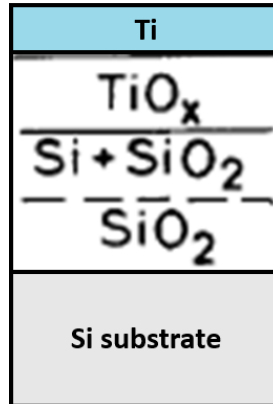
(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 220.)

Taubenblatt 1982 further explains that “in the reaction of Ti with a thicker SiO₂ layer, Ti oxide forms, which can act as a diffusion barrier to prevent further reduction of the oxide by *unreacted Ti metal* or in the formation of silicide.” (Taubenblatt 1982 at 8.) Because Taubenblatt 1982 discloses that the TiO_x layer forms a barrier between unreacted Ti and the SiO₂ layer, an ordinarily skilled artisan would have understood that unreacted titanium remained on top of the TiO_x layer, providing a titanium electrical contact. (*Id.*; Schubert Decl. ¶ 221.)

iv. an interface layer between said region and said metal electrical contact,

This limitation would have been obvious over Goodnick in view of Taubenblatt 1982. (Schubert Decl. ¶ 222.) As discussed above in **Section X.D.1**, that combination would have yielded a TiO_x – SiO₂ interface layer between a region

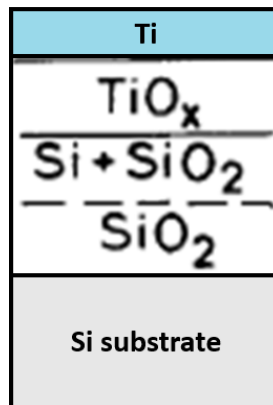
in a semiconductor substrate (Goodnick's silicon substrate) and a metal electrical contact (titanium), as shown below:



(Goodnick at 1; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 222.)

- v. said region being electrically connected to said metal electrical contact through said interface layer and**

This limitation would have been obvious over Goodnick in view of Taubenblatt 1982. (Schubert Decl. ¶ 223.) The combination of Goodnick and Taubenblatt 1982 discussed above in **Section X.D.1** would have yielded the following junction:



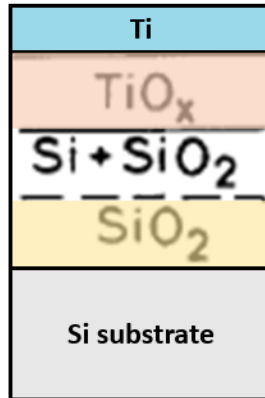
(Goodnick at 1; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 223.)

In that junction, the silicon substrate (region in a semiconductor substrate) is electrically connected to the titanium (metal electrical contact) through an SiO₂ layer (said passivating dielectric tunnel barrier layer) and a TiO_x layer (said metal oxide layer). Three features demonstrate that the silicon substrate and the titanium are electrically connected. *First*, Goodnick describes its interfacial oxide layers as “thin,” and states that “an oxide layer that is sufficiently thin may sustain considerable current via tunneling.” (Goodnick at 1; Schubert Decl. ¶¶ 224-225.) *Second*, an ordinarily skilled artisan would have known that converting some of the interfacial SiO₂ to a titanium oxide (as occurs during the annealing process) would have decreased the specific contact resistivity of the structure. (Kim at 4:63-5:1; Schubert Decl. ¶ 226.) *Third*, an ordinarily skilled artisan would have recognized that because Goodnick’s silicon substrate is n-type doped, the interfacial SiO₂ layer would have decreased the barrier height between that n-type doped silicon substrate and the titanium, further reducing the junction’s specific contact resistivity. (Goodnick at 1; Taubenblatt 1984 at 3; Schubert Decl. ¶ 227.)

vi. said interface layer comprising a metal oxide and a semiconductor oxide, and

This limitation would have been obvious over Goodnick in view of Taubenblatt 1982. (Schubert Decl. ¶ 229.) The combination of Goodnick and Taubenblatt 1982 discussed above in **Section X.D.1** would have yielded an interface

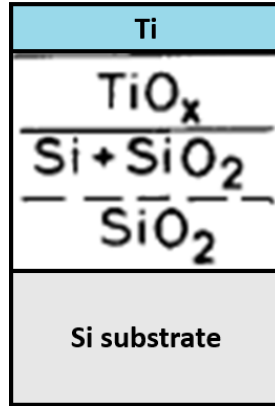
layer that includes titanium oxide (TiO_x), a metal oxide; and silicon dioxide (SiO_2),
a semiconductor oxide:



(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 229.)

vii. being in contact with said region in the semiconductor substrate and said metal electrical contact.

This limitation would have been obvious over Goodnick in view of Taubenblatt 1982. (Schubert Decl. ¶ 231.) The combination of Goodnick and Taubenblatt 1982 discussed above in **Section X.D.1** would have yielded an interface layer that includes silicon dioxide (SiO_2) in contact with the region in the semiconductor substrate and titanium oxide (TiO_x) in contact with the titanium metal electrical contact:



(Goodnick at 1; Taubenblatt 1982 at 7-8; Schubert Decl. ¶ 231.)

Turning to the SiO_2 layer, Taubenblatt 1982 explains that the titanium reduces the SiO_2 grown on the silicon substrate to form titanium oxide and free silicon, but leaves some SiO_2 remaining on the surface of the silicon: “in the reaction of Ti with a thicker SiO_2 layer, Ti oxide forms, which can act as a diffusion barrier to prevent further reduction of the oxide by unreacted Ti metal or in the formation of silicide.” (Goodnick at 1; Taubenblatt 1982 at 7.) And, once the TiO_x layer forms, it prevents subsequent reactions between the titanium and the SiO_2 grown on the silicon substrate, leaving a layer of unreacted Ti metal atop and in contact with the TiO_x layer. (Taubenblatt 1982 at 8; Schubert Decl. ¶ 232.)

3. Claims 11, 12, and 15

Claim 11 depends from Claim 1 and specifies that the metal oxide comprises an oxide of titanium; Claim 12 depends from Claim 11 and specifies that the semiconductor oxide comprises an oxide of silicon. The combination of Goodnick

and Taubenblatt 1982 teaches a TiO_x (titanium oxide) layer and an SiO_2 (silicon dioxide) layer, as discussed above in **Section X.D.2.vi**. (Schubert Decl. ¶¶ 233-235.)

Claim 15 depends from Claim 1 and specifies that the metal electrical contact comprises titanium; Taubenblatt 1982 describes a titanium electrical contact, as discussed above in **Section X.D.2.iii**. (Schubert Decl. ¶ 236.)

4. Claim 23

As discussed above in **Section X.D.1**, the combined teachings of Goodnick and Taubenblatt 1982 yield a $\text{Ti} - \text{TiO}_x - \text{SiO}_2 - \text{Si}$ contact. (Goodnick at 1-2, 5; Taubenblatt 1982 at 7-8.) As it did for Claim 1, that contact also meets every limitation of the similar Claim 23.

i. A semiconductor device, comprising:

The preamble is not limiting. Nevertheless, Goodnick in view of Taubenblatt 1982 renders obvious a semiconductor device. (Schubert Decl. ¶¶ 238-240.) In particular, Goodnick addresses contact metallizations for semiconductor devices. (Goodnick at 1; Schubert Decl. ¶ 241.) Further, as discussed above in **Section X.D.1**, an ordinarily skilled artisan would have combined Goodnick and Taubenblatt 1982 to produce a $\text{Ti} - \text{TiO}_x - \text{SiO}_2 - \text{Si}$ contact, which is a semiconductor device. (*Id.*) Accordingly, Goodnick in view of Taubenblatt 1982 renders obvious a semiconductor device. At the very least, an ordinarily skilled artisan would have found it obvious to form Goodnick's and Taubenblatt 1982's $\text{Ti} - \text{TiO}_x - \text{SiO}_2 - \text{Si}$

contact in a semiconductor device, as Goodnick expressly addresses contact metallizations for semiconductor devices. Goodnick at 1; Schubert Decl. ¶ 242.)

ii. a semiconductor region,

See **Section X.A.1.ii** (Goodnick’s silicon substrate). (Schubert Decl. ¶ 243.)

**iii. a metal electrical contact to said semiconductor region,
and**

See **Section X.D.2.iii** (Taubenblatt 1982’s titanium). (Schubert Decl. ¶ 244.)

**iv. an interface layer disposed between and in contact with
said semiconductor region and said metal electrical
contact,**

See **Sections X.D.2.iv** (“disposed between”) and **X.D.2.vii** (“and in contact with said semiconductor region and said metal electrical contact”). (Schubert Decl. ¶ 245.)

**v. said semiconductor region being electrically connected
to said metal electrical contact through said interface
layer and**

See **Section X.D.2.v** (electrical connection between Taubenblatt 1982’s titanium and Goodnick’s silicon substrate). (Schubert Decl. ¶ 246.)

**vi. said interface layer comprising an oxide of titanium
and an oxide of the semiconductor region.**

See **Section X.D.2.vi** (TiO_x – SiO₂ interface layer). (Schubert Decl. ¶¶ 247-248.)

5. Claims 24, 25, and 28

Claim 24 depends from Claim 23 and specifies that the metal electrical contact includes titanium; Goodnick in view of Taubenblatt 1982 renders obvious a titanium electrical contact, as discussed above in **Section X.D.2.iii.** (Schubert Decl. ¶¶ 249-250.)

Claim 25 depends from Claim 24; Claim 28 depends from Claim 23; and both specify that the semiconductor region comprises silicon. Goodnick discloses a semiconductor region comprising silicon as discussed above in **Section X.A.1.ii.** (*Id.* ¶ 251.)

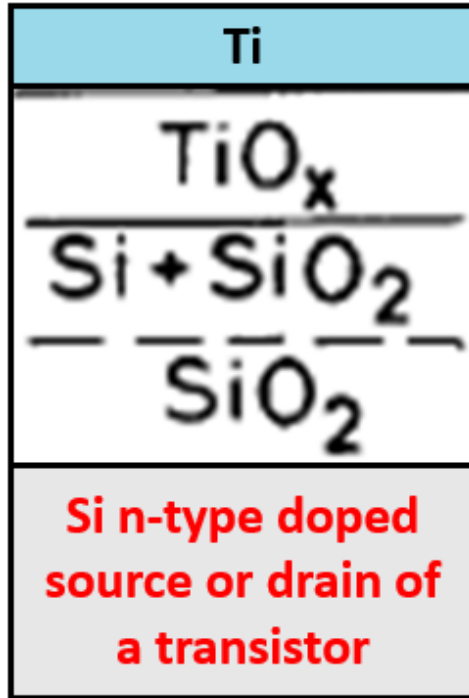
E. Ground 5: Goodnick in view of Jammy and Taubenblatt 1982 renders Claims 14, 17-19, and 22 obvious.

1. Combination of Goodnick, Jammy, and Taubenblatt 1982

As discussed above in **Section X.B.1**, an ordinarily skilled artisan would have found it obvious to grow a 30 Å SiO₂ layer as taught in Goodnick on Jammy's n-type doped source or drain of a transistor in a silicon substrate, then to deposit aluminum on that 30 Å SiO₂ layer. (Schubert Decl. ¶ 252.) As discussed above in **Section X.D.1**, it also would have been obvious both (1) to deposit Taubenblatt 1982's titanium on that 30 Å SiO₂ layer instead of Goodnick's aluminum; and (2) to anneal the resulting structure at 700°C - 900°C as taught by Taubenblatt 1982. (Schubert Decl. ¶ 253.)

Making both combinations would have yielded a contact materially identical to the Ti – TiO_x – SiO₂ – Si contact asserted in Ground 4 against Claims 1 and 12 (from which Claim 14 depends), and therefore would have yielded the same benefits for reducing specific contact resistance. (Schubert Decl. ¶ 254.) The only difference involves substituting Jammy's n-type doped silicon source or drain regions for Goodnick's n-type silicon substrate, which would not have materially altered the Ti – TiO_x – SiO₂ – Si structure or the desirability of using that structure to provide a contact with a low specific contact resistivity. (*Id.*)

In fact, in the context of a transistor like Jammy's, it would have been especially desirable to reduce specific contact resistivity by using a TiO_x – SiO₂ interface layer. That combination not only would have reduced the power consumption of Jammy's transistor, but it also would have advantageously avoided deteriorating Jammy's transistor's switching speed. (Schubert Decl. ¶ 255; Takahashi at 4:57-59; Sakurai at 6; Yeh at 2:54-64.) Thus, an ordinarily skilled artisan would have been motivated to combine Goodnick, Jammy, and Taubenblatt 1982 to provide a TiO_x – SiO₂ interface layer between a **titanium** metal electrical contact and Jammy's exposed n-type **source/drain diffusions** in its silicon substrate:



(Goodnick at 1-2, 5; Jammy at 4:1-4, 4:9-12, 4:36-38; Taubenblatt 1982 at 7-8.)

That contact meets every limitation of Claims 14, 17-19, and 22.⁴

2. Claim 14

i. The electrical junction of claim 12,

See **Section X.D.3** (addressing Claim 12). (Schubert Decl. ¶ 258.)

⁴ As an obvious alternative, Jammy describes depositing conductive studs on its “quantum conductive barrier,” and incorporates titanium conductive studs. (Jammy at Fig. 1, 4:5-8 (incorporating the Cote patent by reference); Cote at 8:24-28 (titanium conductive studs).) Depositing Jammy’s titanium conductive studs would have been equally suitable, and would have yielded the same $\text{TiO}_x - \text{SiO}_2$ interface layer. (Schubert Decl. ¶ 254 n.13; Taubenblatt 1982 at 8.)

- ii. wherein said region in the semiconductor substrate comprises an n-type doped source or drain of a transistor.**

See **Section X.B.2.ii** (Jammy's n-type doped source/drain diffusion regions formed in a silicon substrate). (Schubert Decl. ¶ 259.)

3. Claim 17

- i. An electrical junction, comprising:**

The preamble is not limiting. Nevertheless, it would have been obvious over Goodnick, Jammy, and Taubenblatt 1982. (Schubert Decl. ¶ 261.) As discussed above in **Sections X.D.1 and X.E.1**, the combined teachings of Goodnick, Jammy, and Taubenblatt 1982 yield a Ti – TiO_x – SiO₂ – Si contact, where the Si is an n-type doped source or drain of a transistor. (Goodnick at 1-2, 5; Jammy at 4:1-4, 4:9-12, 4:36-38; Taubenblatt 1982 at 7-8.) And, as discussed above in **Section X.A.1.i**, a contact is synonymous with an “electrical junction.” (Schubert Decl. ¶ 261.)

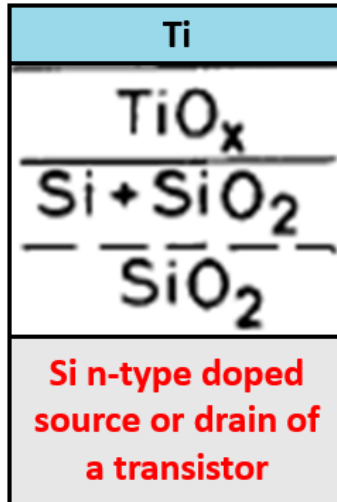
- ii. a source or drain of a transistor, said source or drain comprising a semiconductor,**

See **Section X.B.2.ii** (Jammy's n-type doped source/drain diffusion regions formed in a silicon substrate). (Schubert Decl. ¶ 262.)

- iii. a metal electrical contact to said source or drain, and**

This limitation would have been obvious over Goodnick in view of Jammy and Taubenblatt 1982. (Schubert Decl. ¶ 263.) As discussed above in **Section X.E.1**, the combination of Goodnick, Jammy, and Taubenblatt 1982 would have

yielded a layer of **titanium** as part of a Ti – TiO_x – SiO₂ – Si electrical contact, where the Si is Jammy's n-type source or drain of a transistor:



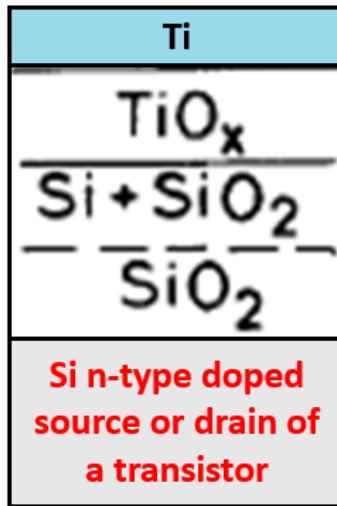
(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Jammy at 4:1-4, 4:9-12, 4:36-38; Schubert Decl. ¶ 263.)

Taubenblatt 1982 further explains that “in the reaction of Ti with a thicker SiO₂ layer, Ti oxide forms, which can act as a diffusion barrier to prevent further reduction of the oxide by **unreacted Ti metal** or in the formation of silicide.” (Taubenblatt 1982 at 8.) Because Taubenblatt 1982 discloses that the TiO_x layer forms a barrier between unreacted Ti and the SiO₂ layer, an ordinarily skilled artisan would have understood that unreacted titanium remained on top of the TiO_x layer, providing a titanium electrical contact. (*Id.*; Schubert Decl. ¶ 264.)

iv. an interface layer disposed between and in contact with said source or drain and said metal electrical contact,

This limitation would have been obvious over Goodnick in view of Jammy and Taubenblatt 1982. (Schubert Decl. ¶ 265.) As discussed above in **Section**

X.E.1, the combination of Goodnick, Jammy, and Taubenblatt would have yielded an interface layer whose SiO_2 is in contact with Jammy's source/drain diffusions in its silicon substrate and whose TiO_x is in contact with Taubenblatt 1982's titanium:

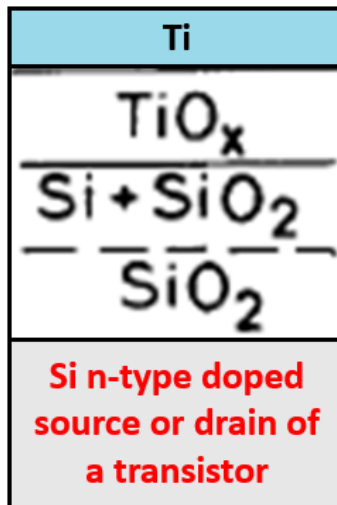


(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Jammy at 4:1-4, 4:9-12, 4:36-38; Schubert Decl. ¶ 265.)

Turning to the SiO_2 layer, Taubenblatt 1982 explains that the titanium reduces the SiO_2 grown on the silicon substrate to form titanium oxide (TiO_x) and free silicon, but leaves some SiO_2 remaining on the surface of the silicon: “in the reaction of Ti with a thicker SiO_2 layer, Ti oxide forms, which can act as a diffusion barrier to prevent further reduction of the oxide by unreacted Ti metal or in the formation of silicide.” (Goodnick at 1; Taubenblatt 1982 at 7.) And, once the TiO_x layer forms, it prevents subsequent reactions between the titanium and the SiO_2 grown on the silicon substrate, leaving a layer of unreacted Ti metal atop and in contact with the TiO_x layer. (Taubenblatt 1982 at 8; Schubert Decl. ¶ 266.)

- v. **said source or drain being electrically connected to said metal electrical contact through said interface layer and**

This limitation would have been obvious over Goodnick in view of Jammy and Taubenblatt 1982. (Schubert Decl. ¶ 267.) The combination of Goodnick, Jammy, and Taubenblatt 1982 discussed above in **Section X.E.1** would have yielded the following structure:

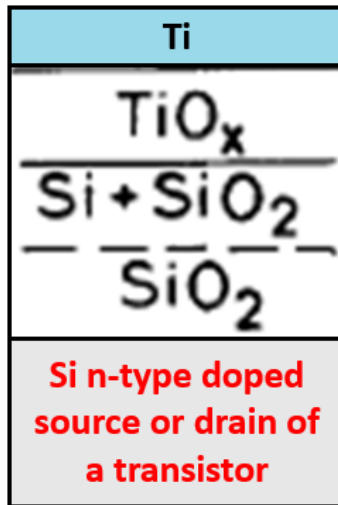


(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Jammy at 4:1-4, 4:9-12, 4:36-38; Schubert Decl. ¶ 267.)

In that structure, the source or drain in the silicon substrate is electrically connected to the titanium (metal electrical contact) through a TiO_x - SiO₂ layer (interface layer). (Schubert Decl. ¶ 268.) That TiO_x - SiO₂ layer provides an electrical connection between the titanium metal electrical contact and the silicon substrate substantially for the reasons discussed above in **Section X.D.2.v. (Id.)**

- vi. **said interface layer comprising an oxide of titanium and an oxide of the semiconductor.**

This limitation would have been obvious over Goodnick in view of Jammy and Taubenblatt 1982. (Schubert Decl. ¶ 273.) As discussed above in **Section X.E.3.iv**, that combination produces an interface layer that includes a titanium oxide (TiO_x) and silicon dioxide (SiO_2), a semiconductor oxide:



(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Jammy at 4:1-4, 4:9-12, 4:36-38; Schubert Decl. ¶ 273.)

4. **Claims 18, 19, and 22**

Claim 18 depends from Claim 17 and specifies that the metal electrical contact comprises titanium. Goodnick in view of Jammy and Taubenblatt 1982 renders obvious a titanium metal electrical contact, as discussed above in **Section X.E.3.iii**. (Schubert Decl. ¶¶ 275-276.)

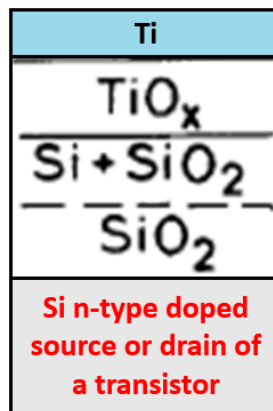
Claim 19 depends from Claim 18; Claim 22 depends from Claim 17; and both Claim 19 and Claim 22 specify that the semiconductor comprises silicon. Jammy

discloses n-type doped source/drain diffusions (doped regions) in a MOSFET's silicon substrate. (Jammy at 4:1-4, 4:9-12, 4:36-38; (Schubert Decl. ¶ 279.)

F. Ground 6: Goodnick in view of Jammy, Taubenblatt 1982, and Chang renders Claim 6 obvious.

1. Combination of Goodnick, Jammy, Taubenblatt 1982, and Chang

As discussed above in **Section X.E.1**, an ordinarily skilled artisan would have combined Goodnick, Jammy, and Taubenblatt 1982 to achieve the structure below:



(Goodnick at 1-2; Taubenblatt 1982 at 7-8; Jammy at 4:9-12, 4:33-38; Schubert Decl. ¶ 278.)

That combination of Goodnick, Jammy, and Taubenblatt 1982 does not expressly describe any specific contact resistivity. Nonetheless, an ordinarily skilled artisan could have and artisan would have been motivated to provide an interface layer configured to provide a specific contact resistivity between the metal electrical contact and the region in the semiconductor of less than 10 $\Omega\text{-}\mu\text{m}^2$ as in Claim 6 by using Chang's high doping concentrations for Jammy's n-type doped silicon source or drain of a transistor.

Jammy does not expressly disclose any doping level for its n-type silicon **source/drain diffusion region**. (Jammy at 4:33-38.) But, an ordinarily skilled artisan would have known that heavily doping that n-type silicon **source/drain diffusion region** would have reduced specific contact resistivity. (Schubert Decl. ¶ 280.) Indeed, at doping levels above 10^{18} dopant atoms / cm^3 , specific contact resistivity “becomes a strong function of doping,” with specific contact resistivity decreasing as doping increases. (Chang at 4-5.) Chang also describes doping levels for n-type silicon as high as 10^{21} dopant atoms / cm^3 . (*Id.* at 7 (Fig. 5).)

An ordinarily skilled artisan would have been motivated to use Chang’s high doping levels for Jammy’s n-type silicon source/drain diffusion regions to reduce specific contact resistivity further. (Schubert Decl. ¶ 282.) And, an ordinarily skilled artisan would have been motivated to reduce the specific contact resistivity of that contact to Jammy’s n-type doped silicon source or drain of a transistor to reduce the power consumption of Jammy’s transistor and to avoid deteriorating its switching speed, as discussed above in **Section X.E.1**. (*Id.*)

By both (1) increasing the doping levels of Jammy’s n-type doped source/drain to reduce specific contact resistivity and (2) disposing a specific-contact-resistivity-lowering TiO_x – SiO_2 interface layer between the titanium metal electrical contact and Jammy’s n-type doped silicon source/drain diffusions, an

ordinarily skilled artisan would have reasonably expected to achieve a specific contact resistivity of less than $10 \text{ } \Omega\text{-}\mu\text{m}^2$. (Schubert Decl. ¶ 283.)

Indeed, ordinarily skilled artisans had already succeeded in reducing specific contact resistivity below $10 \text{ } \Omega\text{-}\mu\text{m}^2$ with or without an interface layer:

Reference	Doping Concentration	Junction	Specific contact resistivity
Kim ⁵	3×10^{20} arsenic atoms / cm^3 for n-type doped silicon	Titanium-tungsten alloy to n-type silicon, with interface layer including TiO_2	$8 \text{ } \Omega\text{-}\mu\text{m}^2$
Hara ⁶	10^{20} atoms / cm^3 for silicon	Unspecified metal to silicon junction; no interface layer described	$1 \text{ } \Omega\text{-}\mu\text{m}^2$

(Schubert Decl. ¶¶ 284-285.)

Chang describes even higher doping concentrations for n-type doped silicon than those used in Kim or Hara: as high as 10^{21} dopant atoms / cm^3 . (Chang at 7 (Fig. 5).) And, an ordinarily skilled artisan would have reasonably expected to successfully n-type dope Jammy's silicon source or drain of a MOSFET to a concentration of 10^{21} dopant atoms / cm^3 . For example, U.S. Patent No. 6,521,502 to Yu, filed in August 2000, describes implanting n-type dopants into silicon source or drain regions of a MOSFET to a concentration of up to 10^{21} dopant atoms / cm^3 . (Yu at 4:4-12, 4:43-48; Schubert Decl. ¶¶ 286-287.)

⁵ Kim at 4:63-5:1, 5:27-30.

⁶ Hara at 2:50-56.

Using the higher doping concentration described in Chang in Jammy's n-type source or drain of a transistor gives the combination of Goodnick, Jammy, Taubenblatt 1982, and Chang a feature for reducing specific contact resistance that Kim and Hara lack: n-type silicon doped to a concentration as high as 10^{21} dopant atoms / cm^3 . And, when used with that higher doping concentration, the specific-contact-resistivity-minimizing $\text{TiO}_x - \text{SiO}_2$ interface layer described above would have given an ordinarily skilled artisan a reasonable expectation of successfully achieving a specific contact resistivity between the contact metal and the semiconductor of less than $10 \text{ } \Omega\text{-}\mu\text{m}^2$. (Schubert Decl. ¶ 288.)

2. Claim 6

i. The electrical junction of claim 1,

Goodnick in view of Taubenblatt 1982 renders obvious Claim 1, as discussed above in **Section X.D.2**. Goodnick in view of Jammy and Taubenblatt 1982 also renders the electrical junction of Claim 1 obvious. The only difference is that Jammy's n-type doped silicon source or drain of a transistor (instead of Goodnick's silicon substrate) would have been that the "Si" in the $\text{Ti} - \text{TiO}_x - \text{SiO}_2 - \text{Si}$ contact, which would have still met every limitation of Claim 1, and which would not have altered the combination. (Schubert Decl. ¶¶ 290-292.)

- ii. wherein said interface layer is configured to provide a specific contact resistivity between the metal electrical contact and the region in the semiconductor of less than $10\ \Omega\text{-}\mu\text{m}^2$.

As discussed above in **Section X.F.1**, an ordinarily skilled artisan would have been motivated to combine Jammy, Goodnick, Taubenblatt 1982, and Chang to provide a specific contact resistivity of less than $10\ \Omega\text{-}\mu\text{m}^2$ between Jammy's n-type doped silicon source or drain and a titanium metal electrical contact as described in Taubenblatt 1982, and would have had a reasonable expectation of successfully doing so. (Schubert Decl. ¶ 293.)

G. Ground 7: Goodnick in view of Taubenblatt 1982 and Kim renders Claims 16, 26, and 27 obvious.

1. Combination of Goodnick, Taubenblatt 1982, and Kim

As discussed above in **Sections X.D.1, X.D.2, and X.D.4**, the combination of Goodnick and Taubenblatt 1982 renders obvious both Claim 1 (from which Claim 16 depends) and Claim 23 (from which Claims 26 and 27 depend). But, neither Goodnick nor Taubenblatt 1982 expressly describe a metal electrical contact that comprises tungsten, as in Claims 16, 26, and 27.

Kim, on the other hand, describes a metal electrical contact that comprises tungsten: “[a]lloys in the range of about 10% to 40% by weight of titanium and the remainder tungsten are particularly suitable for providing low resistance contacts to

silicon.” (Kim at 5:2-4.) Kim also discloses that its titanium-tungsten alloy reduces silicon dioxide to form titanium dioxide when heated. (*Id.* at 4:63-5:1.)

An ordinarily skilled artisan would have found it obvious to substitute Kim’s titanium-tungsten alloy for Taubenblatt 1982’s titanium in the combination of Goodnick and Taubenblatt 1982 discussed above in **Section X.D.1**. An ordinarily skilled artisan would have expected that combination of Goodnick, Taubenblatt 1982, and Kim to yield an interface layer that includes a titanium oxide and SiO₂ just like the TiO_x – SiO₂ interface layer provided by the combination of Goodnick and Taubenblatt 1982 discussed above in **Section X.D.1**. (Schubert Decl. ¶ 296.) In particular, like the titanium in Taubenblatt 1982, the titanium-tungsten alloy in Kim reduces silicon dioxide to form a titanium oxide when heated, producing a desirable reduction in contact resistance. (Kim at 4:63-5:1; Taubenblatt 1982 at 8.)

Thus, substituting Kim’s titanium-tungsten alloy for Taubenblatt 1982’s titanium would have been nothing more than a substitution of one known prior art element (Taubenblatt 1982’s titanium) for another (Kim’s titanium-tungsten alloy), with the predictable result of a forming a metal-semiconductor contact with a TiO_x – SiO₂ interface layer. Further, an ordinarily skilled artisan would have been motivated to substitute Kim’s titanium-tungsten alloy for Taubenblatt 1982’s titanium to increase the temperature at which titanium silicide forms, which would have improved fabrication reliability. (Cohen at 82; Schubert Decl. ¶ 298.) And,

because that combination of Goodnick, Jammy, Taubenblatt 1982, and Kim would have only required conventional semiconductor processing steps, an ordinarily skilled artisan would have had a reasonable expectation of success. (*Id.* ¶ 299.)

2. Claim 16

i. The electrical junction of claim 1,

See **Section X.D.2.** (Schubert Decl. ¶ 301.)

ii. wherein said metal electrical contact comprises tungsten.

Kim discloses this limitation. (Schubert Decl. ¶ 302.) “Alloys in the range of about 10% to 40% by weight of titanium and the remainder tungsten are particularly suitable for providing low resistance contacts to silicon.” (Kim at 5:2-4.)

3. Claim 26

i. The semiconductor device of claim 23,

See **Section X.D.4.** (Schubert Decl. ¶ 303.)

ii. wherein said metal electrical contact includes tungsten.

See **Section X.G.2.ii.** (Schubert Decl. ¶ 304.)

4. Claim 27

i. The semiconductor device of claim 26,

See **Section X.G.3.** (Schubert Decl. ¶ 306.)

ii. wherein said semiconductor region comprises silicon.

Goodnick discloses a silicon substrate; see **Section X.A.1.ii.** (Schubert Decl. ¶ 307.)

H. Ground 8: Goodnick in view of Jammy, Taubenblatt 1982, and Kim renders obvious Claims 20 and 21.

1. Combination of Goodnick, Jammy, Taubenblatt 1982, and Kim

An ordinarily skilled artisan would have combined Goodnick with Jammy and Taubenblatt 1982 for the reasons discussed above in **Section X.E.1.** (Schubert Decl. ¶ 308.) And, although the combination of Goodnick, Jammy, and Taubenblatt 1982 does not expressly teach a metal electrical contact that includes tungsten, an ordinarily skilled artisan would have found it obvious to substitute Kim's titanium-tungsten metal electrical contact for Taubenblatt 1982's titanium for the reasons discussed above in **Section X.G.1.** (*Id.*)

2. Claim 20

i. The electrical junction of claim 17,

See **Section X.E.3.** (Schubert Decl. ¶ 310.)

ii. wherein said metal electrical contact includes tungsten.

See **Section X.G.2.ii.** (Schubert Decl. ¶ 311.)

3. Claim 21

i. The electrical junction of claim 20,

See **Section X.H.2.** (Schubert Decl. ¶ 313.)

ii. wherein said semiconductor comprises silicon.

See **Section X.B.2.ii** (Jammy's n-type doped source/drain diffusion regions formed in a silicon substrate). (Schubert Decl. ¶ 314.)

I. Alleged Secondary Considerations for Grounds 2-8

Petitioner addresses any alleged secondary considerations currently of record and reserves the right to address any secondary considerations that Acorn later presents.

Although the specification purports to describe unexpected results related to silicon nitride layers ('395 Patent at 12:30-37), no challenged claim has a silicon nitride layer. (Schubert Decl. ¶ 316.) Likewise, while Acorn's infringement complaint alleges unexpected results and industry recognition related to the inventors' purported achievement of low specific contact resistances using an interface layer, only Claim 6 specifies any particular specific contact resistivity. (Ex. 1157 ¶¶ 6, 48, 50, 51.) And, Acorn's complaint does not relate those alleged low specific contact resistances to any particular specific contact resistivity. (*Id.*)

Further, the prior art taught interface layers that reduced specific contact resistance. (Schubert Decl. ¶¶ 318-319; Schroen at Abstract; Iwaguro at [0005]-[0006], [0012]-[0014].) Indeed, the Iwaguro reference taught that an interface layer could reduce specific contact resistance by a factor of at least 100. (Schubert Decl. ¶ 319; Iwaguro at Fig. 3.) Moreover, both Kim and Hara taught specific contact

resistivities “less than 10 $\Omega\text{-}\mu\text{m}^2$ ” as in Claim 6, the only claim with any particular specific contact resistivity. (Kim at 4:63-5:1, 5:27-30; Hara at 2:55-56; Schubert Decl. ¶ 320.) And Kim obtained its 8 $\Omega\text{-}\mu\text{m}^2$ specific contact resistivity with an interface layer. (Kim at 4:63-5:1, 5:27-30.)

XI. The discretionary factors favor institution.

A. 35 U.S.C. § 325(d)

The Office did not consider any of Goodnick, Taubenblatt 1982, or Chang during the prosecution of the '395 Patent or its parent applications. And while Examiners signed information disclosure statements citing Jammy in the '395 Patent and parent applications, no further consideration of Jammy with respect to the '395 Patent is of record. (Ex. 1112, at 391-392; Ex. 1114, at 128; Ex. 1116, at 118; Ex. 1118, at 139; Ex. 1120, at 146.) Crucially, no Examiner cited Jammy against any claim of the '395 Patent or of any parent application; moreover, Jammy is being combined with new references here.

B. 35 U.S.C. § 314(a)

1. *General Plastic*

Petitioner also filed the petition in Case IPR2020-01207. But as of this petition's filing date, nothing has happened in Case IPR2020-01207. Thus, the *General Plastic* factors do not weigh against institution, especially if the Board elects to institute only one petition. *General Plastic Indus. Co., Ltd. v. Canon*

Kabushiki Kaisha, Case IPR2016-01357, Paper 19, at 9-10 (PTAB Sept. 6, 2017) (designated precedential).

2. *NHK Spring / Apple*

Despite concurrent litigation involving the '395 Patent, discretionary denial of institution under *NHK Spring Co., Ltd. v. Intri-Plex Techs., Inc.*, Case IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018) (designated precedential) is unwarranted. Congress deliberately gave *inter partes* review petitioners a full year to file a petition after service of an infringement complaint because petitioners deserve a “reasonable opportunity to identify and understand the patent claims that are relevant to the litigation” when a patent owner asserts “multiple patents with large numbers of vague claims.” Joe Matal, *A Guide to the Legislative History of the America Invents Act: Part II of II*, 21 FED. CIR. B.J. 539, 611-612 (2012) (quoting 157 Cong. Rec. S5429 (daily ed. Sept. 8, 2011) (statement of Sen. Kyl)); *see also* 35 U.S.C. § 315(b).

Here, Acorn has asserted **108 claims across six patents** in the Acorn Litigation, including **25 claims of the '395 Patent**—exactly what Congress envisioned. (Ex. 1160; Ex. 1161.) Thus, denying institution because of the Acorn Litigation would contradict Congress’s intent. Further, the six factors in *Apple Inc. v. Fintiv, Inc.*, Case IPR2020-00019, Paper 11, at 6 (PTAB Mar. 20, 2020) (designated precedential) collectively favor instituting trial.

i. Apple factor 1: whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted

This factor favors instituting trial. Petitioner will be promptly moving to stay the Acorn Litigation after filing this petition. Although the Court presiding over the Acorn Litigation infrequently grants pre-institution motions to stay, it nonetheless invites defendants to renew their motions to stay once the Board institutes trial, and grants stays even at advanced stages when the Board has instituted on the asserted claims. *Image Processing Techs. LLC v. Samsung Elecs. Co., Ltd.*, Case No. 2:16-cv-505-JRG, 2017 WL 10185855, at *1 (E.D. Tex. Feb. 17, 2017) (denying pre-institution motion to stay); 2017 WL 2672616 (E.D. Tex. June 21, 2017) (claim construction order); 2017 WL 7051628, at *1 (E.D. Tex. Oct. 25, 2017) (granting Samsung's renewed motion to stay after the Board instituted *inter partes* review, four months after the claim construction order).

ii. Apple factor 2: proximity of the court's trial date to the Board's projected statutory deadline for a final written decision

Although the Acorn Litigation trial date is currently scheduled for April 2021 (Ex. 1159) and ahead of the Board's projected final written decision date, jury trial dates—to say nothing of dates for post-trial briefing—are inherently subject to change. *Precision Planting, LLC v. Deere & Co.*, Case IPR2019-01044, Paper 17, at 15 (PTAB Dec. 2, 2019). That inherent uncertainty weighs against denying

institution, especially here given the Acorn Litigation Court’s willingness to stay when the Board has instituted on the asserted claims. *Image Processing Techs.*, 2017 WL 7051628, at *1.

iii. Apple factor 3: investment in the parallel proceeding by the court and the parties

This factor largely overlaps with factor 2; for similar reasons, it does not favor denying institution. However far the Acorn Litigation progresses between now and the institution decision, the Acorn Litigation Court has shown a willingness to stay cases for instituted *inter partes* reviews—even four months after a claim construction order. *Image Processing Techs.*, 2017 WL 7051628, at *1.

Further, “it is often reasonable for a petitioner to wait to file its petition until it learns which claims are being asserted against it in the parallel proceeding.” *Apple*, Case IPR2020-00019, Paper 11, at 11. Here, Acorn identified only one representative claim for each of six patents in its October 2019 complaint, including only one claim of the ’395 Patent. (Ex. 1157 ¶¶ 63, 73, 83, 93, 103, 113.) Later, in March 2020, Acorn served its infringement contentions—which collectively span **108 claims** across those six patents, including **24** previously unidentified claims of the ’395 Patent. (Ex. 1160; Ex. 1161.) Petitioner promptly filed its petitions against those 108 asserted claims thereafter.

iv. *Apple* factor 4: overlap between issues raised in the petition and in the parallel proceeding

Although Petitioner is also challenging Claims 1-6, 8-9, 11-12, and 14-28 in the Acorn Litigation, that does not favor denying institution here. Instituting would make a stay possible in the Acorn Litigation, reducing overlap. Further, it is unlikely that the Acorn Litigation will resolve the validity of every challenged claim of the '395 Patent. While Acorn may commit to trying all 25 asserted and challenged claims,⁷ some claims will likely drop out before trial, leaving the Board as the only tribunal to assess those claims. Finally, to reduce overlap, if the Board institutes, Petitioner will promptly cease asserting Jammy, Goodnick, Taubenblatt 1982, Chang, and Kim as prior art references to the challenged claims in the Acorn Litigation. Thus, this factor favors institution.

v. *Apple* factor 5: whether the petitioner and the defendant in the parallel proceeding are the same party

Although Petitioner and its real parties-in-interest are the defendants in the Acorn Litigation, that does not automatically favor denying institution. Rather, the Board principally considers this factor to avoid duplicating another tribunal's work. *Apple*, Case IPR2020-00019, Paper 11, at 13-14. And, as discussed above for factors 1-4, there is minimal risk of that happening here given (1) the Acorn Litigation

⁷ Acorn is not asserting Claim 10.

Court's willingness to grant stays where the Board has instituted; and (2) Petitioner's willingness to cease asserting Jammy, Goodnick, Taubenblatt 1982, Chang, and Kim against the challenged claims in the Acorn Litigation if the Board institutes.

vi. *Apple* factor 6: other circumstances that impact the Board's exercise of discretion, including the merits

This factor favors institution: Petitioner has presented well-supported anticipation and obviousness grounds based on Goodnick, Taubenblatt 1982, Jammy, Chang, and Kim. Further, considerations similar to those under 35 U.S.C. § 325(d) are relevant. *Apple*, Case IPR2020-00019, Paper 11, at 16. As discussed above in **Section XI.A**, the Office has not cited any of those references against the challenged claims. That too favors institution.

* * *

In conclusion, the *Apple* factors favor institution, despite the Acorn Litigation trial date. Indeed, “*NHK Spring* does not suggest, much less hold, that *inter partes* review should be denied under § 314(a) solely because a district court is scheduled to consider the same validity issues before the *inter partes* review would be complete.” *Intuitive Surgical, Inc. v. Ethicon LLC*, Case IPR2018-01703, Paper 7, at 13 (PTAB Feb. 19, 2019).

XII. Conclusion

Petitioner respectfully requests that the Board institute *inter partes* review, hold the challenged claims unpatentable, and cancel the challenged claims.

Petition for *Inter Partes* Review
U.S. Patent No. 10,030,395

Dated: July 13, 2020

Respectfully submitted,

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CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

I hereby certify that this paper, excluding the portions exempted under 37 C.F.R. § 42.24(a), has:

- 13,603 words as counted by Microsoft Word 2016, the word-processing system used to prepare this paper; and
- 378 words in the illustrations, counted manually.

This paper's total word count, excluding the portions exempted under 37 C.F.R. § 42.24(a), is **13,981** words.

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CERTIFICATE OF SERVICE

Under 37 C.F.R. § 42.6(e), the undersigned certifies that on July 13, 2020, a complete copy of the foregoing and all accompanying papers and exhibits were served via Federal Express Priority Overnight shipping, which is at least as fast and reliable as U.S. Priority Mail Express, on counsel of record for Acorn at the correspondence address indicated in PAIR:

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