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# **High-k Gate Dielectrics for Si CMOS Applications**

A Dissertation

Presented to the Faculty of the Graduate School

of

Yale University

in Candidacy for the Degree of

Doctor of Philosophy

By

**Zhijiong Luo**

Dissertation Director: Prof. Tso-Ping Ma

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## Abstract

# High-k Gate Dielectrics for Si CMOS Applications

Zhijiong Luo

2003

**This thesis focuses on the understanding of many fundamental properties of high-k gate dielectrics for Si CMOS gate applications, and on the development of ultra-thin  $\text{ZrO}_2/\text{Zr}$  silicate, titanium aluminates, and  $\text{TiO}_2/\text{SiN}$  gate dielectrics.**

**The results demonstrate that the ultra-thin  $\text{ZrO}_2/\text{Zr}$  silicate films deposited by the JVD process can have EOTs down to 1 nm, and possess high thermal stability, among other good electrical properties. The presence of a thermally stable Zr silicate interfacial layer may prevent the formation of interfacial silicon oxide during anneal.**

**Our results also reveal that either incorporating Al into  $\text{TiO}_2$ , or using a high-quality ultra-thin JVD SiN layer can improve the properties of the gate stack after high temperature annealing. The nano-crystallization of titanium aluminates results in considerable degradation of transconductance and reliability.**

**The barrier heights over Si conduction band edge and conduction mechanisms of several scientifically and technically important high-k materials have been studied. Our results reveal that (1) Though  $\text{Ta}_2\text{O}_5$  possesses a larger bandgap than that of  $\text{TiO}_2$ , due to its adverse band alignment to Si band,  $\text{Ta}_2\text{O}_5$  only has a barrier height of 0.28 eV over Si conduction band edge, which is much smaller than that of  $\text{TiO}_2$ . Therefore, Schottky emission or thermionic emission becomes the dominant conduction mechanism in over the  $\text{Ta}_2\text{O}_5$  barrier; (2) The high barrier height of 3.0 eV for ALD  $\text{Al}_2\text{O}_3$  over Si conduction band edge makes it attractive to block thermionic current at elevated temperatures; The barrier height of 2.1 eV for JVD  $\text{ZrO}_2/\text{Silicate}$  over the Si conduction band edge is sufficient to block thermionic current; (3) Incorporating Al into  $\text{TiO}_2$  increases the barrier height of**

**TiO<sub>2</sub> over the Si conduction band edge; (4) The work function of 4.7 eV for Tungsten makes its Fermi-level at the mid-gap of Si band.**

**Through the course of this dissertation study, we have found that (1) it is possible to make MOSFETs with high-k gate dielectrics with mobilities that fit closely to the universal mobility curve, (2) a major portion of the reduced transconductance or conductance can be attributed to trapping, (3) among MOSFET's with Hf silicate, HfO<sub>2</sub>, and Hf aluminate, the device with Hf silicate shows the highest transconductance and lowest trap densities.**

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## List of Abbreviations

|                  |                                                                        |
|------------------|------------------------------------------------------------------------|
| <b>AFM</b>       | <b>Atomic Force Microscopy</b>                                         |
| <b>ALD</b>       | <b>Atomic Layer Deposition</b>                                         |
| <b>CCS</b>       | <b>Constant-Current Stress</b>                                         |
| <b>CMOS</b>      | <b>Complementary Metal-Oxide-Semiconductor</b>                         |
| <b>CMOSFET</b>   | <b>Complementary Metal-Oxide-Semiconductor Field-Effect-Transistor</b> |
| <b>CV, C-V</b>   | <b>Capacitance-Voltage</b>                                             |
| <b>CVD</b>       | <b>Chemical Vapor Deposition</b>                                       |
| <b>DIBL</b>      | <b>Drain-Induced-Barrier-Lowering</b>                                  |
| <b>DG-MOSFET</b> | <b>Double-Gate Metal-Oxide-Semiconductor Field-Effect-Transistor</b>   |
| <b>D-T</b>       | <b>Direct-Tunneling</b>                                                |
| <b>EOT</b>       | <b>Equivalent Oxide Thickness</b>                                      |
| <b>F-N</b>       | <b>Fowler-Nordheim</b>                                                 |
| <b>HFCV</b>      | <b>High Frequency Capacitance-Voltage</b>                              |
| <b>IDM</b>       | <b>Integrated Device Manufacturer</b>                                  |
| <b>IV, I-V</b>   | <b>Current-Voltage</b>                                                 |
| <b>JVD</b>       | <b>Jet Vapor Deposition</b>                                            |
| <b>MEIS</b>      | <b>Medium Energy Ion Scattering</b>                                    |
| <b>MIS</b>       | <b>Metal-Insulator-Semiconductor</b>                                   |
| <b>N-MOSFET</b>  | <b>N-Channel MOSFET</b>                                                |
| <b>PDA</b>       | <b>Post-Deposition-Anneal</b>                                          |
| <b>PMA</b>       | <b>Post Metallization Anneal</b>                                       |

|                 |                                               |
|-----------------|-----------------------------------------------|
| <b>P-MOSFET</b> | <b>P-Channel MOSFET</b>                       |
| <b>RBS</b>      | <b>Rutherford backscattering spectroscopy</b> |
| <b>SIA</b>      | <b>Semiconductor Industries Association</b>   |
| <b>SOI</b>      | <b>Silicon-On-Insulator</b>                   |
| <b>TDB</b>      | <b>Time-Dependent-Breakdown</b>               |
| <b>TEM</b>      | <b>Transmission-Electron-Microscopy</b>       |
| <b>ULSI</b>     | <b>Ultra-Large-Scale-Integration</b>          |
| <b>WKB</b>      | <b>Wentzel-Kramer-Brillouin</b>               |
| <b>XPS</b>      | <b>X-ray Photoelectron Spectroscopy</b>       |
| <b>XRD</b>      | <b>X-Ray Diffraction Spectroscopy</b>         |

# List of Symbols

|                        |                                                  |
|------------------------|--------------------------------------------------|
| <b>c</b>               | <b>Capture Rate</b>                              |
| <b>C</b>               | <b>Capacitance</b>                               |
| <b>C<sub>ox</sub></b>  | <b>Oxide Capacitance</b>                         |
| <b>e</b>               | <b>Emission Rate</b>                             |
| <b>E</b>               | <b>Electric Field, or Energy</b>                 |
| <b>E<sub>c</sub></b>   | <b>Conduction Band Edge</b>                      |
| <b>E<sub>F</sub></b>   | <b>Fermi-level</b>                               |
| <b>E<sub>g</sub></b>   | <b>Band Gap</b>                                  |
| <b>E<sub>v</sub></b>   | <b>Valence Band Edge</b>                         |
| <b>F</b>               | <b>Occupancy Factor</b>                          |
| <b>EOT</b>             | <b>Equivalent Oxide Thickness</b>                |
| <b>G<sub>m</sub></b>   | <b>Transconductance</b>                          |
| <b>h</b>               | <b>Plank's Constant</b>                          |
| <b>I<sub>cp</sub></b>  | <b>Charge pumping Current</b>                    |
| <b>I<sub>d</sub></b>   | <b>Driving Current</b>                           |
| <b>I<sub>g</sub></b>   | <b>Gate Current</b>                              |
| <b>I<sub>d+s</sub></b> | <b>Source/Drain Current</b>                      |
| <b>I<sub>sub</sub></b> | <b>Substrate Current</b>                         |
| <b>J</b>               | <b>Current Density</b>                           |
| <b>J<sub>DT</sub></b>  | <b>Direct-Tunneling Current Density</b>          |
| <b>J<sub>FN</sub></b>  | <b>Fowler-Nordheim Tunneling Current Density</b> |
| <b>m*</b>              | <b>Effective Mass</b>                            |

|              |                                 |
|--------------|---------------------------------|
| $m_0$        | Electron Mass in Free Space     |
| $n$          | Electron                        |
| $N_{it}$     | Interface Trap Density Per Area |
| $p$          | Hole                            |
| $Q, q$       | Charge                          |
| $R$          | Resistance                      |
| $T_{ox}$     | Oxide Physical Thickness        |
| $V$          | Voltage                         |
| $V_{FB}$     | Flat-Band Voltage               |
| $V_{th}$     | Threshold Voltage               |
| $X$          | Distance                        |
| $\epsilon$   | Dielectric Constant             |
| $\epsilon_0$ | Vacuum Permittivity             |
| $\phi$       | Barrier Height                  |
| $\lambda$    | Attenuation Coefficient         |
| $\mu$        | Mobility                        |
| $\nu$        | Optical Frequency               |
| $\sigma$     | Capture Cross Section           |

# **Chapter 1**

## **The Evolution of CMOS Devices and Gate Dielectrics**

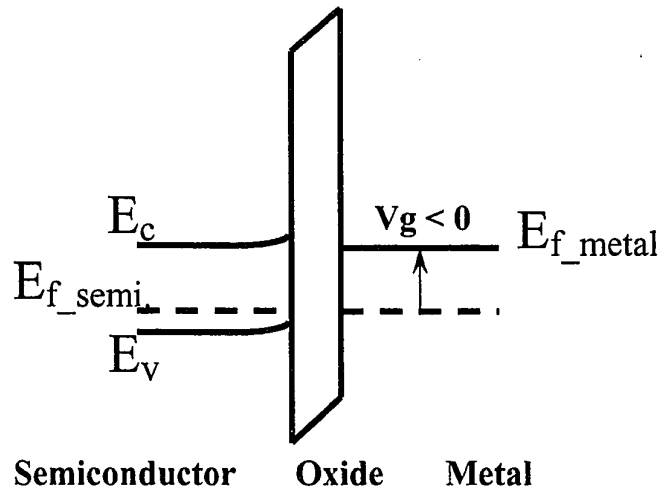
**This chapter provides an introduction of the evolution of Complementary-Metal-Oxide-Semiconductor (CMOS) devices and gate dielectrics for CMOS applications. First, the history of the evolution of CMOS will be presented, and the scaling theories will be introduced. Then, the current state of CMOS gate dielectric technology and the difficulties of continuing the scaling of silicon dioxide as gate dielectric will be discussed. Finally, a possible solution to continue the scaling of CMOS gate dielectric and possible candidates to succeed silicon dioxide will be reviewed. The criteria to select new high-k gate dielectrics to replace silicon dioxide as CMOS gate dielectric will be summarized.**

## 1. 1 CMOS

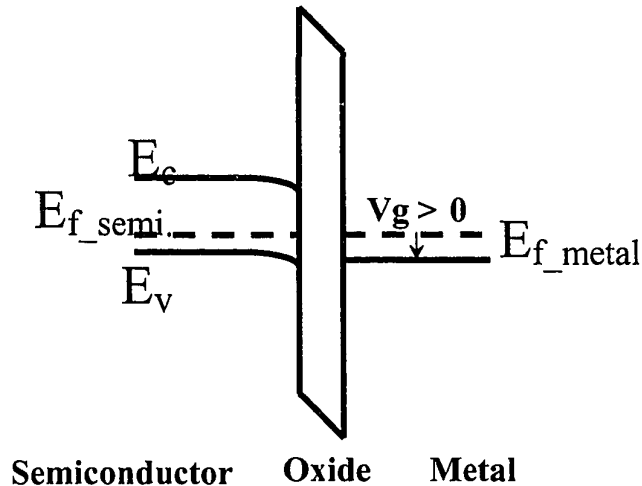
The human society is moving fast into the information age. From huge mainframe servers handling trillion bits of data in a second to tiny calculators, from the backbones of the telecommunication networks to cell phones, microchips are responsible for the generation, storage, and transmission of information, and they constitute brains and nerves of our society. In microchips, the most fundamental building block is the silicon Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET). MOSFET has greatly influenced the society since its birth, and it has become one of the most important inventions in human history.

### *1.1.1 MOS Structure and MOSFET*

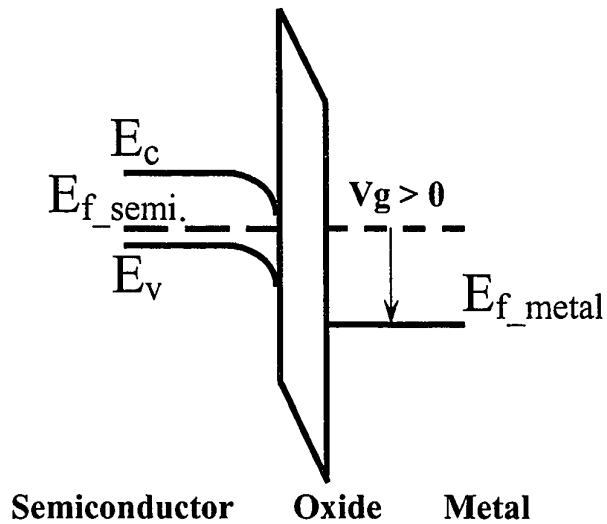
What is a MOSFET? First, a Metal-Oxide-Semiconductor (MOS) structure is composed of three important planar layers: one metal layer, one insulating layer, and one semiconductor layer. As illustrated in Figure 1.1, following the variation of the applied voltage or electric field, the surface of the semiconductor can be changed into three different conditions, accumulation, depletion, and inversion, respectively. Based on this effect, MOSFET was proposed. MOSFET is a four-terminal transistor as illustrated in Figure 1.2. For an enhancement mode N-type MOSFET, when the gate voltage is zero or negative, the device is off; Thus, there is no current flowing between the source and drain. However, when the gate voltage gradually increases and passes a threshold value, the semiconductor surface region underneath the gate is inverted. Therefore, a channel filled with free electrons is formed, which allows the current to conduct between the source and drain.



***Accumulation***

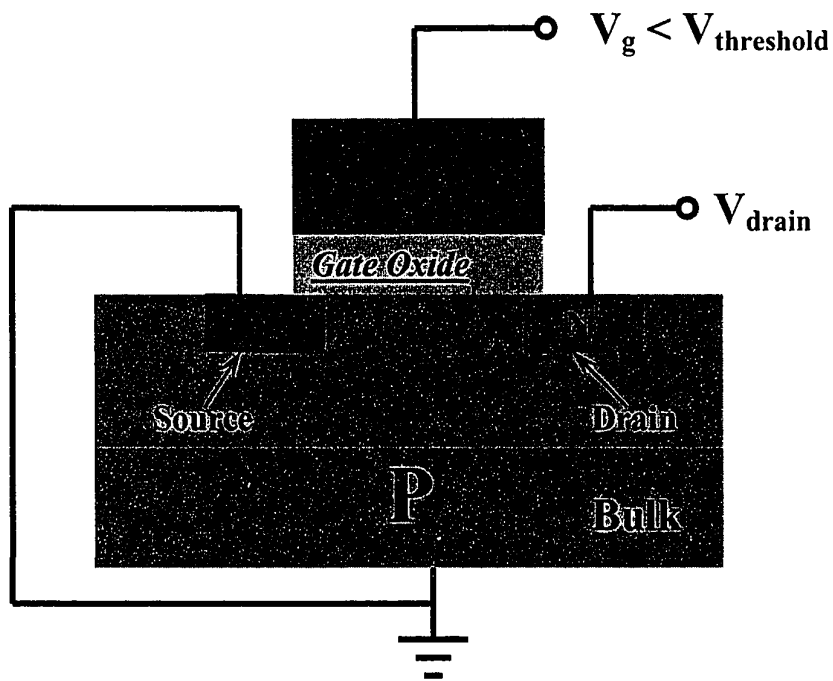


***Depletion***

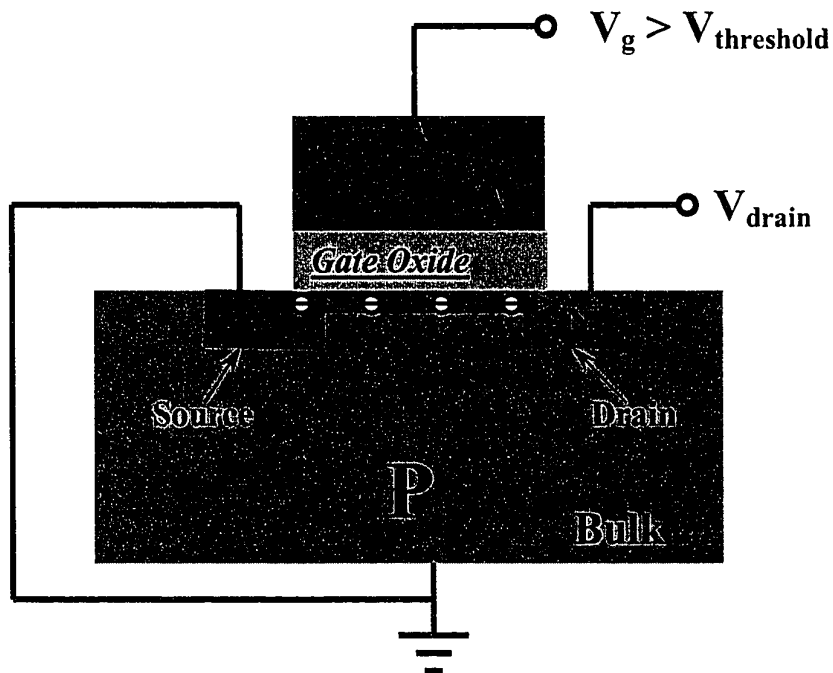


***Inversion***

Figure 1.1 Energy band diagrams for Metal-Oxide-Semiconductor system in accumulation, depletion and inversion. (Semiconductor in the figure is P-type; When  $V_g = 0$ , metal has the same Fermi-level as semiconductor.)



$V_g < V_{\text{threshold}}$ , MOSFET is OFF.



$V_g > V_{\text{threshold}}$ , MOSFET is ON.

Figure 1.2 The gate voltage controls the ON and OFF of MOSFET.

### ***1.1.2 Brief History of MOSFET***

A conceptually similar MOSFET structure was proposed and patented independently by Lilienfeld<sup>1</sup> and by Heil<sup>2</sup> in 1930, but was not successfully implemented until the early 1960s. Kahng at Bell Labs fabricated the first MOSFET in 1960<sup>3</sup>. In 1963, Wanlass and Sah at Fairchild Semiconductor originated and published the very idea of Complementary-Metal-Oxide-Semiconductor (CMOS)<sup>4</sup>. The circuitry based on CMOS structure shrank the stand-by power consumption significantly, reduced the device overlap capacitance, and improved frequency performance dramatically. By 1968, both CMOS structure and polysilicon gate technology with the gate to source/drain self-alignment technology had been successfully developed<sup>5</sup>. So, at that time, CMOS was poised to take over the world. Moreover, MOSFET found a perfect partner in silicon (Si). The low stand-by power of CMOS circuitry and the process prowess of Si together propelled the Si CMOS circuitry to the dominant role in modern electronics.

There are no better words to describe the phenomenal growth of the semiconductor industry than the famed Moore's law. In 1965, Gordon Moore, then director of research and development at Fairchild Semiconductor, wrote a paper for *Electronics* entitled "Cramming more components onto integrated circuits."<sup>6</sup> In the paper, Moore observed that "The complexity for minimum component has increased at a rate of roughly a factor of two per year." This observation became known as Moore's law: the number of components per Integrated Circuit (IC) doubles every year. Moore's law was later amended to that the number of components per IC doubles every 18 months. Moore's law holds to this day. Besides the growth of the density of the circuitry, the speed and function of circuitry are also growing at roughly the same rate. Figure 1.3 illustrates the growth of the memory capacity and MPU clock speed since the early 70s<sup>7</sup>. And Table 1.1 reveals the improvement of the recent CMOS technology generations<sup>8,9,10,11,12</sup>.

## 1. 2 MOSFET and Gate Dielectric Scaling

There is one driving force behind such astonishing growth: the scaling of MOSFET. At the birth of MOSFET, channel length, the critical feature of MOSFET, is on the scale of 100  $\mu\text{m}$ . Now the channel length of the state-of-the-art MOSFET is below 100 nm, which is a thousand-time smaller. Now hundreds of millions of MOSFETs can be integrated on one single chip economically.

### *1.2.1 Short Channel Effect*

However, the scaling of MOSFET is not a simple task. It takes a systematic approach to break numerous barriers. If the scaling is not conducted properly, instead of gaining benefits, it results in malfunctioned devices. With a shortened channel length, the gate faces a much stronger competition from the source and drain than that in device with longer channel. The gate has less influence on the channel region, which causes many adverse effects on the shortened channel. The short channel effect is characterized by a decrease of the MOSFET threshold voltage as the channel length reduces. When the distance between the source and drain are comparable to the depletion width of the source or drain, the space-charge region takes a significant part of the channel region. In this case, the MOSFET needs fewer carriers to invert the channel, which results in a lower threshold voltage. In the extreme case, the depletion regions for the source and drain connect, so carriers can move freely between source and drain without an inverted channel, and the device does not function at all. This extreme case is called punch through. Therefore, different scaling theories, such as the constant electric field scaling rules<sup>13</sup> and the constant voltage scaling rules<sup>14</sup> (see Appendix), were proposed to solve scaling related problems.

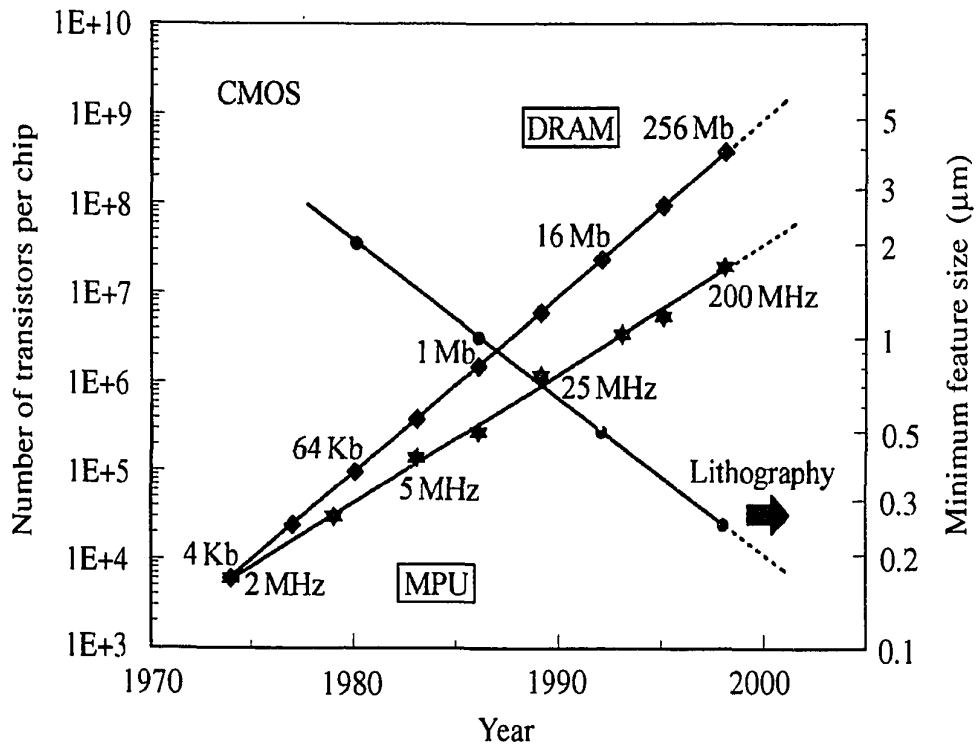


Figure 1.3 The evolution of DRAM capacity and MPU clock speed<sup>7</sup>.

| <i>Technology generation</i> | <i>Power-Supply Voltage (V)</i> | <i>Gate Oxide Thickness (nm)</i> | <i>Oxide Field (MV/cm)</i> | <i>Year of Initial Introduction</i> |
|------------------------------|---------------------------------|----------------------------------|----------------------------|-------------------------------------|
| <i>3μm</i>                   | 5                               | 70                               | 0.7                        | 1977                                |
| <i>2μm</i>                   | 5                               | 35                               | 1.4                        | 1980                                |
| <i>1.2μm</i>                 | 5                               | 25                               | 2.0                        | 1986                                |
| <i>0.8μm</i>                 | 5                               | 18                               | 2.8                        | 1989                                |
| <i>0.5μm</i>                 | 3.3                             | 12                               | 2.8                        | 1992                                |
| <i>0.35μm</i>                | 3.3                             | 10                               | 3.3                        | 1995                                |
| <i>0.25μm</i>                | 3.3-2.5                         | 6-4                              | 6                          | 1997                                |
| <i>0.18μm</i>                | 1.5                             | 2                                | 7.5                        | 1999                                |
| <i>0.13μm</i>                | 1.3                             | 1.5                              | 8.6                        | 2001                                |

Table1.1 CMOS VLSI technology generations<sup>9,10,11,12,13</sup>.

### ***1.2.2 The Scaling of Gate Dielectrics***

Among all the scaling parameters, the gate oxide thickness is probably the most important one. It's difficult to imagine any meaningful scaling of MOSFET without scaling the gate dielectric. That is mainly for two reasons: (1) the drive current of MOSFET is proportional to the gate capacitance per unit area,

$$I_{ds,sat} = \frac{W}{L} \mu C_{ox} \frac{V_{d,sat}^2}{2}, \quad (1.1)$$

where  $W$  is the channel width of MOSFET,  $L$  is the channel length,  $\mu$  is the channel carrier mobility, and  $C_{ox}$  is the gate capacitance per unit area. A thinner gate oxide or a larger gate capacitance per unit area provides a larger drive current; (2) a thinner gate oxide or a larger gate capacitance per unit area enables the gate to possess better control of the channel region. Therefore, it can minimize the short-channel effects. Table A.3 in Appendix reveals the requirements of the gate dielectric thickness for the future generations of Si CMOS technology<sup>15</sup>.

Since the birth of Si MOS devices, silicon dioxide (SiO<sub>2</sub>) has been used almost exclusively as the gate dielectrics. Its outstanding electrical properties and remarkable process compatibility with Si were unmatched by any other dielectric. Silicon dioxide is one of the most important reasons that Si is the dominant IC material. In the late 70s, the thickness of thermal silicon dioxide used in Si CMOS was about 50-70 nm, but now the gate oxide thickness is approaching 1 nm. Figure 1.4 shows the magnificent SEM images from a state-of-the-art research device presented by Intel Corporation<sup>16</sup>. In this MOSFET, the gate oxide thickness is only about 0.8 nm, and the gate oxide is only composed of three atomic layers. While it is a remarkable achievement, it also reveals that silicon dioxide is reaching its own limits.

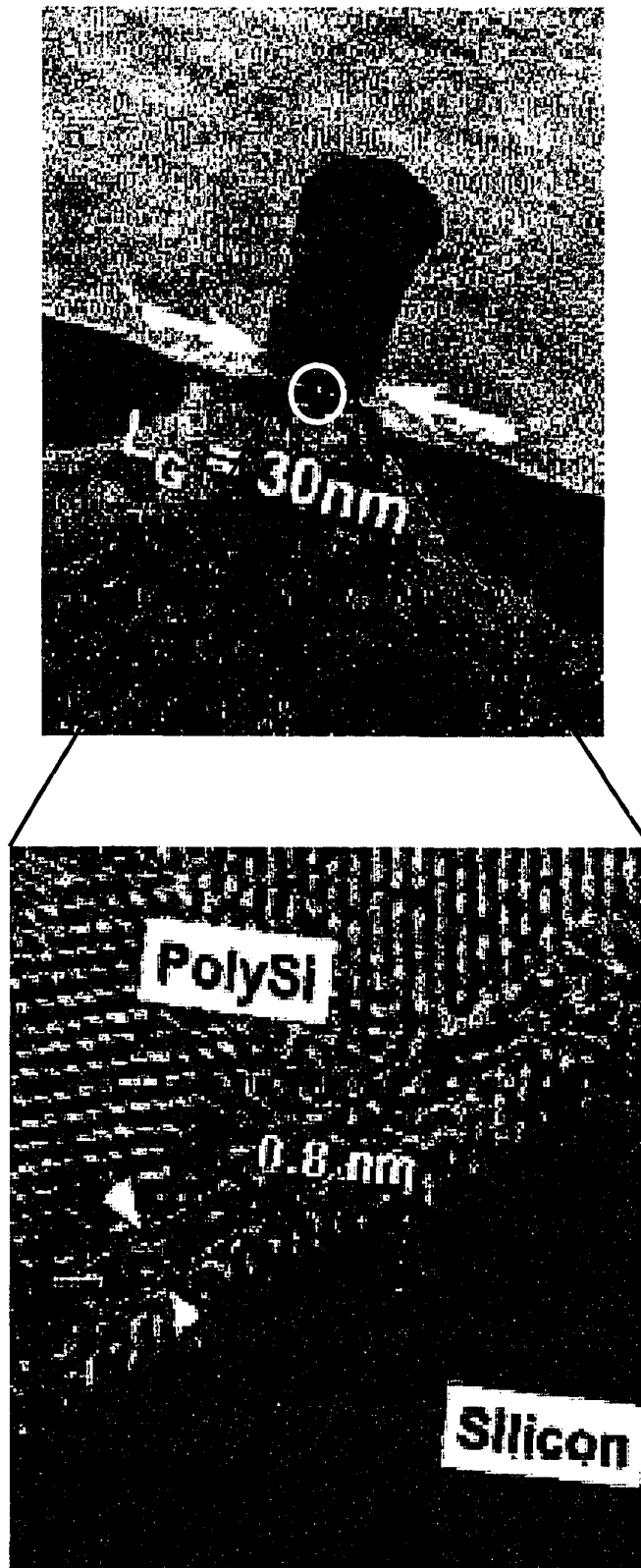


Figure 1.4 A 30nm gate length MOSFET with 0.8nm gate oxide<sup>16</sup>.

### ***1.2.3 High Tunneling Leakage Current***

Until the recent CMOS technology generations, most difficulties that we faced to scale down gate oxide were technical problems. However, now we are meeting some fundamental physics problems to scale down silicon dioxide. The tunneling current is the most severe physics problem raised when we scale down the silicon dioxide thickness below 2.0 nm. According to Quantum Mechanics, because of its wave character, an electron is able to penetrate through an energy barrier. The tunneling probability is related to the barrier height and barrier thickness<sup>17</sup>. The lower the barrier height and the thinner the barrier, the higher is the tunneling probability. With a 9.1eV bandgap, silicon dioxide enjoys a 3.15 eV barrier over the Si conduction band edge<sup>18</sup>. However, even with such a large barrier height, the tunneling current can be as high as 10 A/cm<sup>2</sup> for a 1.5nm thick silicon dioxide biased at 1 V<sup>19</sup>, as shown in Figure 1.5. Moreover, the tunneling leakage current will increase exponentially with the decrease of the silicon dioxide thickness. Every 0.2 nm reduction of the silicon dioxide thickness can result in about one order of magnitude increase of the tunneling leakage current. Such high tunneling leakage current causes serious consequences. First, it results in the standby power consumption increasing dramatically. If the gate silicon oxide thickness for a microchip is 1.5nm, and the chip operates at 1 V with an active area of 1 cm<sup>2</sup>, the standby power consumption will be at 10 W! And with further scaling of the gate oxide thickness, it can reach 100 W in one technology generation! Such a high standby power is more than we can bear, especially for portable devices. Second, silicon dioxide is no longer acting as an effective insulator with such a small thickness. It no longer can hold the channel carriers in the channel region. Thus a big portion of the channel carriers transports through silicon dioxide to the gate of MOSFET instead of conducting between the source and drain. At a minimum case, it degrades the drive current or transconductance ( $G_m$ ), and in a severe case, it could cause

failure of the device. For the same channel width, the MOSFET with a longer channel has a larger gate area and smaller drive current compared to the MOSFET with a shorter channel, which results in a larger gate leakage current to drive current ratio. So, there is a more severe problem with the gate leakage current in the MOSFET with a longer channel.

#### ***1.2.4 Boron Penetration***

One major breakthrough in CMOS technology is the invention of the dual-gate technology, in which  $n^+$  polysilicon and  $p^+$  polysilicon are used to form gate electrodes for nMOSFET and pMOSFET respectively<sup>5</sup>. Because the dual-gate technology brought us the convenience of the self-alignment of the gate to source/drain, it has become the standard technology for CMOS circuitry<sup>20</sup>. However, the dopant for  $p^+$  polysilicon gate, Boron (B) or  $BF_2$ , introduces one serious problem for thin gate oxide: boron penetration<sup>21,22,23</sup>. In the process flow, B or  $BF_2$  is implanted after the gate oxide and polysilicon deposition, and then dopants are activated by subsequent annealing at a high temperature: 950 °C – 1050 °C. Boron atom has high diffusion coefficient in both silicon and silicon dioxide, especially at elevated temperatures. For thin silicon dioxide, it is easy for boron atom to penetrate through thin silicon dioxide in the implant stage or the following annealing stage. The boron penetration causes serious consequences, such as degradation of gate oxide quality, unwanted shift of threshold voltage, and degradation of transconductance. Though we can reduce the degree of boron penetration by applying a lower implantation dose or a lower thermal budget during subsequent annealing, these solutions inevitably cause adverse effects, such as less than desirable doping concentration in  $p^+$  polysilicon gate, which results in severe poly depletion effect and large series resistance.

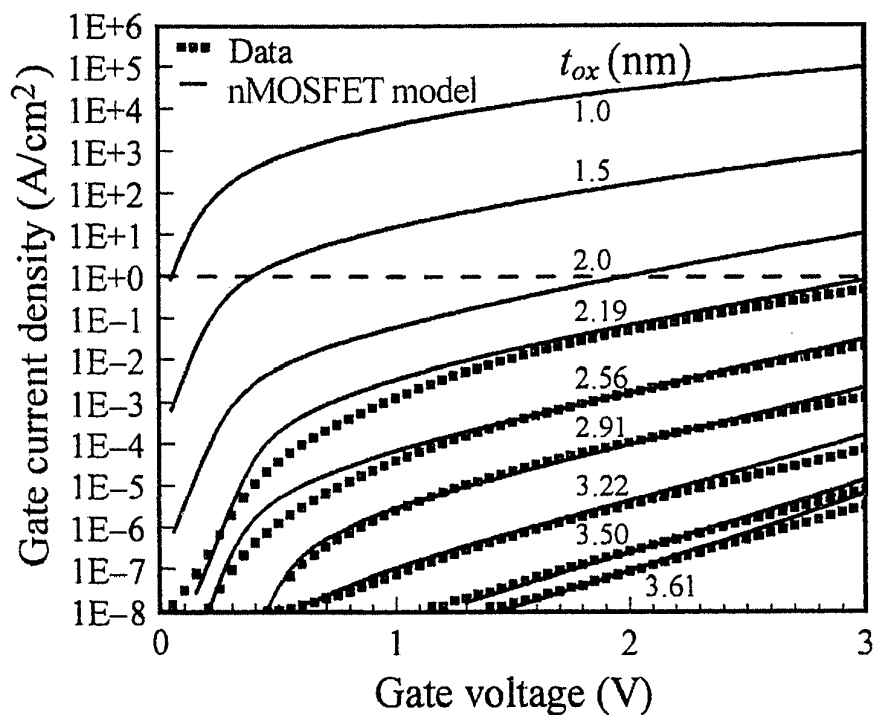


Figure 1.5 Tunneling Leakage Current in Ultra-thin Silicon Dioxide<sup>19</sup>.

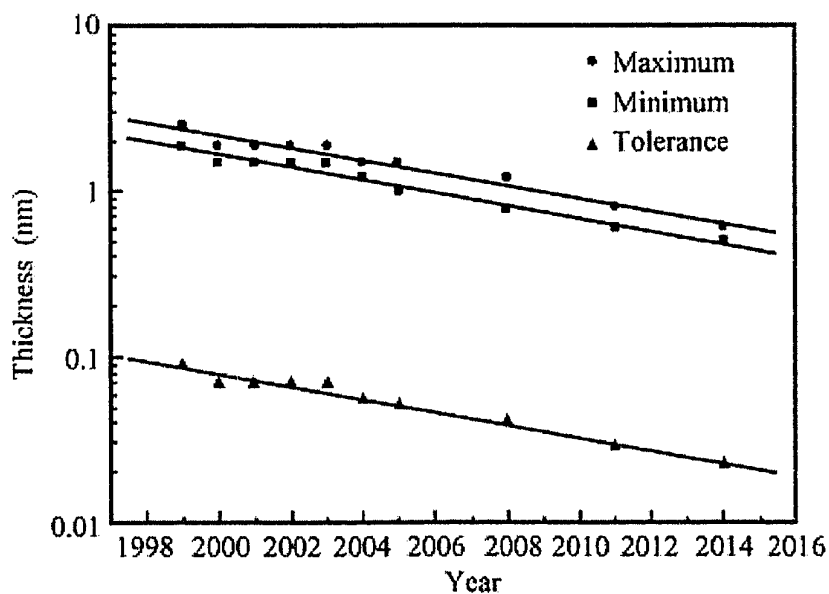


Figure 1.6 The projected gate dielectric thickness tolerance from 2002 update of the ITRS<sup>15</sup>.

### ***1.2.5 Silicon Dioxide Reliability and Life Time***

Not only is gate oxide one of the most important elements of MOSFET, its failure is also the main cause of device failure. Thus, the reliability of gate oxide is an extremely important factor that determines the device or chip lifetime. Though it may look straightforward at first, understanding the reliability and breakdown mechanisms of silicon dioxide is still a work in progress after more than three decades intensive research on this topic<sup>24,25,26,27,28,29</sup>. There are a few leading theories that address the reliability of silicon dioxide<sup>30,31,32,33,34,35</sup>. Most researchers acknowledge that the silicon dioxide breakdown is related to the magnitude of the electric field applied to it. And with the continuous CMOS scaling, the electric field across the gate oxide has been increasing. One leading theory, based on the anode hole-injection model, predicts a lifetime exponentially dependent on  $1/E^{30,31}$ . Another leading theory, the E model, predicts that the Time to Break Down (TBD) changes as  $\exp(-rE)^{32,33}$ , where  $r$  is a constant. Both theories predict that the lifetime of the gate silicon dioxide decreases with the increase of electric field. The percolation model<sup>34,35</sup> suggests that the breakdown happens when a continued path of defects formed as the results of defects generation before and during the electric stress. Clearly, with the thinner silicon dioxide, it's easier to form the continued path of defects inside the insulator. Thus, it also suggests a shortened lifetime for the ultra-thin gate oxide. Though there is no clear agreement on the limit of silicon dioxide thickness due to reliability concerns, a range between 1.5 nm to 2.5 nm was predicted by various groups as the final reliability limit of silicon dioxide<sup>36,37,38</sup>.

### ***1.2.6 Uniformity and Manufacturability***

For the semiconductor industry, manufacturability is one of the most important concerns for an Integrated Device Manufacturer (IDM), or a foundry. Now the whole

industry is shifting towards the 300 mm era, and in this new era, the requirement of manufacturability is raised to an unprecedented level. As an industry standard,  $3\sigma$  non-uniformity of less than 4% is required across the whole wafer<sup>15</sup>. Today's state-of-the-art technology of silicon dioxide realizes the tolerance of less than 0.01 nm for a 1.5-nm film<sup>39</sup>, which is phenomenal. A more detailed requirement for the future gate dielectric thickness and tolerance from ITRS<sup>15</sup> is shown in Figure 1.6. When considering the following two facts: (1) the wafer size is 300 mm in diameter, and (2) the thickness of one monolayer of silicon dioxide is about 0.2 to 0.3 nm, we realize that it requires remarkable sub-monolayer control of the growth of thin film to fulfill these requirements. Also, the pre-gate silicon surface cleaning techniques<sup>40</sup> and polysilicon intrusion and shallow trench isolation (STI) corner stress effects<sup>41</sup> have to be addressed as well in order to meet the stringent tolerance required.

## 1.3 Alternative Gate Dielectrics

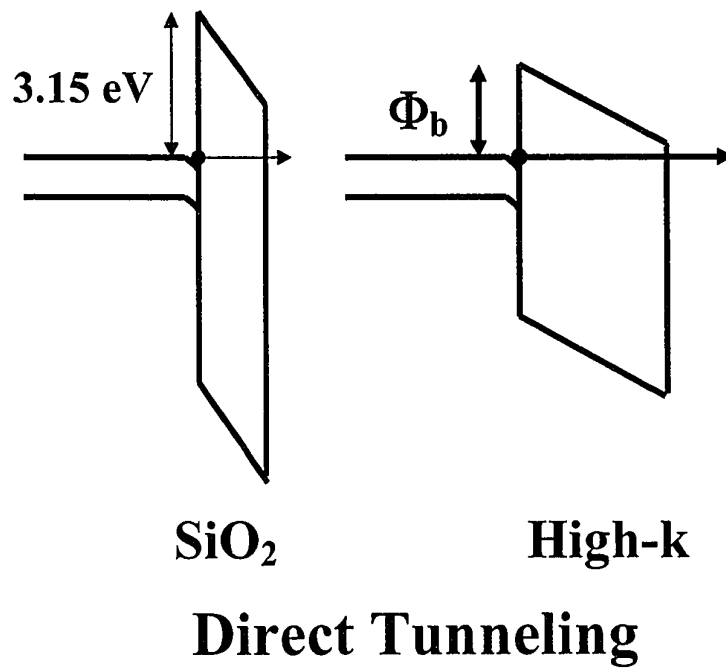
Silicon dioxide has been used as the gate dielectric for Si CMOS technology since the very first day of Si MOSFET, and it has been the driving force behind the dominance of Si CMOS technology. However, after several decades of scaling, clearly silicon dioxide is approaching its physical limits, and some aspects of that have been discussed in Section 1.3. A solution must be found to continue the CMOS scaling and the growth of the industry. Obviously most limits of silicon dioxide, from the leakage current to reliability issues, stem from the shrinking thickness of silicon dioxide. Is there a way to get around this thickness issue? The answer is YES. However, it's not an easy task. And most part of this thesis is dedicated to addressing this problem.

### 1.3.1 Fatter is Better

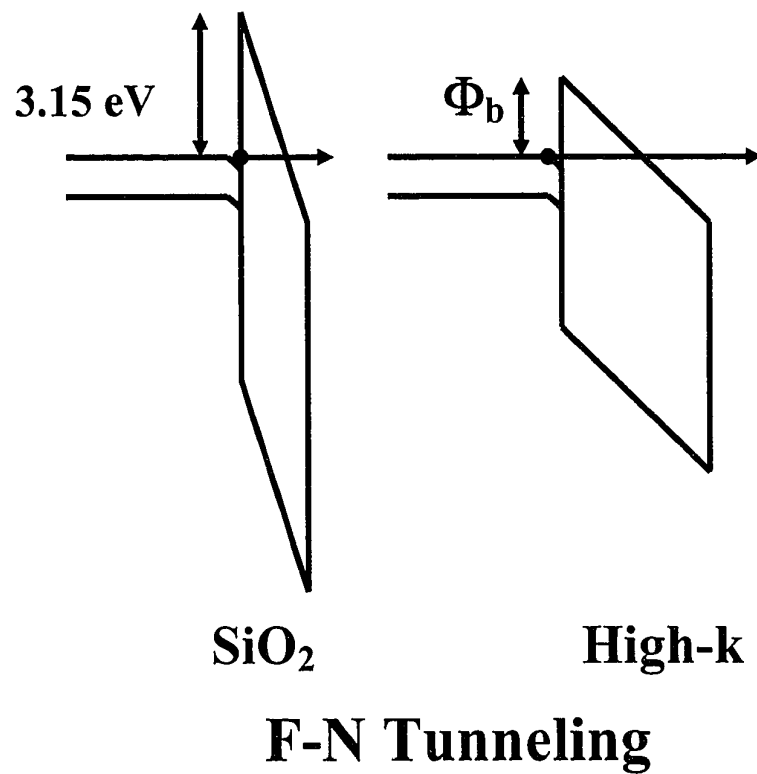
Device physics reveals that the real concern of the CMOS scaling is the gate oxide capacitance, not the gate oxide thickness. A large enough gate capacitance per unit area is necessary to improve the control over channel region by gate, and to reduce the short channel effect<sup>8</sup>. The capacitance is inversely proportional to the physical thickness for a certain dielectric material. However, the capacitance is also proportional to the dielectric constant of the material. Therefore, by finding a gate dielectric with higher dielectric constant (high-k) to replace silicon dioxide, we are able to get the same or higher gate capacitance per unit area with a larger thickness of the gate dielectric. By doing so, we can overcome many limits stemming from the thickness of silicon dioxide.

The most important limit of silicon dioxide is the large tunneling leakage current, which is a direct result of the shrunk thickness of silicon dioxide. Basically, the tunneling current through gate oxide can be divided into two regions. In the low electric field region, where the oxide voltage is smaller than the barrier height, as illustrated in Figure 1.7 (a), electrons tunnel through a trapezoidal barrier, and they tunnel into the other electrode directly. This process is called directly tunneling<sup>42,43,44</sup>. In the high electric field region, where the oxide voltage is larger than the barrier height, as illustrated in Figure 1.7 (b), electrons tunnel through a triangular barrier, and tunnel into the oxide conduction band first, before traveling towards the other electrode. This process is called Fowler-Nordheim tunneling<sup>45</sup>. The tunneling currents for direct tunneling condition and Fowler-Nordheim condition, respectively, are described as the following:

$$J_{DT} = \frac{q^2}{2\pi\hbar T_{ox}^2} \{ (\phi_b - V/2) \exp\left[-\frac{4\pi(2qm^*)^{1/2}}{h} T_{ox}(\phi_b - V/2)^{1/2}\right] - \phi_b \exp\left[-\frac{4\pi(2qm^*)^{1/2}}{h} T_{ox}\phi_b^{1/2}\right] \} \quad (1.2)$$



(a)



(b)

Figure 1.7 Direct tunneling and Fowler-Nordheim tunneling for silicon dioxide and high-k dielectrics.

and

$$J_{FN} = \frac{q^2}{8\pi\hbar\phi_b} E^2 \exp\left[-\frac{8\pi(2qm^*)^{1/2}}{3\hbar} \phi_b^{3/2} / E\right], \quad (1.3)$$

where  $\Phi_b$  is the barrier height,  $m^*$  is the effective mass of an electron, and  $T_{ox}$  is the gate oxide thickness.

For both cases, the reduction of tunneling current is exponentially dependent upon the increase of gate dielectric thickness. Most high-k materials have lower barrier heights than the barrier height of silicon dioxide, but for many high-k materials, the gain from the increase of thickness usually overcomes the loss from the decreased barrier heights.

To reduce tunneling leakage current is the foremost motivation to employ high-k gate dielectrics to replace silicon dioxide. Moreover, implementing high-k gate dielectrics also brings other possible benefits. Using a thicker gate dielectric is expected to suppress the possibility of boron penetration. A thicker gate dielectric reduces the electric field at a given voltage. Therefore, it may extend the lifetime of the gate dielectric. A thicker film also may relieve the stringent tolerance posed on the gate dielectric thickness with the same  $3\sigma$  standard.

### ***1.3.2 Potential Candidates to Succeed Silicon Dioxide***

Now we are going to discuss some possible candidates to succeed silicon dioxide. First, we will discuss silicon oxynitride/silicon nitride, then we will consider metal oxides, and last we will review ferroelectric materials. Table 1.2 lists the properties of many candidates.

|                                                                                                   | $ZrO_2$ | $HfO_2$ | $ZrSiO_4$ | $Al_2O_3$ | $TiO_2$ | $Ta_2O_5$ | $La_2O_3$ |
|---------------------------------------------------------------------------------------------------|---------|---------|-----------|-----------|---------|-----------|-----------|
| <b>Dielectric Constant</b>                                                                        | ~23     | ~20     | ~10-12    | ~10       | ~80     | ~25       | ~21       |
| <b>Band Gap (eV)</b>                                                                              | 5.8     | 6       | 6         | 8.8       | 3.25    | 4.65      | 6         |
| <b>Conduction Band Offset (eV)</b>                                                                | 1.9     | 1.5     | 2.1       | 3         | 0.9     | 0.28      | 2.3       |
| <b>Free energy of reaction, <math>Si + MO_x \rightarrow M + SiO_2</math> @ 727 °C (Kcal/mole)</b> | 42.3    | 47.6    | N/A       | 63.4      | 7.5     | -52.5     | N/A       |
| <b>Stability of Amorphous Phase at High Temp.</b>                                                 | Low     | Low     | High      | High      | Medium  | Low       | Low       |

Table 1.2 Properties of some high-k materials.

### **Silicon Oxynitride/Silicon Nitride**

Silicon oxynitride is the near-term solution to replace silicon dioxide. The employment of silicon oxynitride to replace silicon dioxide is in production now. Incorporation of a small amount of nitrogen into silicon dioxide has been a common practice to enhance silicon dioxide<sup>46</sup>, to reduce boron penetration<sup>47,48</sup>, channel hot electron degradation<sup>49</sup> and defect generation<sup>50</sup>, and to improve the uniformity control on the growth of sub-3.0 nm gate oxide<sup>51</sup>. However, usually only less than a few percent of nitrogen concentration is incorporated in silicon oxynitride to gain the above benefits without losing the other superb qualities of silicon dioxide. Such low nitrogen concentrations only have a small effect in increasing the dielectric constant. Therefore, the reduction of gate tunneling leakage current is marginal. Silicon nitride or high-nitrogen-concentration silicon oxynitride's dielectric constant can be as high as twice that of silicon dioxide. Thus, it has the potential to reduce the gate leakage current significantly. Moreover, silicon nitride is totally compatible with the conventional CMOS process flow, which makes it very attractive. However, until the appearance of Jet-Vapor-Deposition (JVD) silicon nitride<sup>52</sup>, the high density of traps and fixed charges in the silicon nitride or high-nitrogen-concentration silicon oxynitride produced by Chemical-Vapor-Deposition (CVD) prevented their practical usage as gate dielectrics<sup>53</sup>. The device-quality JVD silicon nitride, developed at Yale University, demonstrated for the first time that silicon nitride or high-nitrogen-concentration silicon oxynitride is a valid candidate to replace silicon dioxide as gate dielectric. Though the development of silicon nitride or high-nitrogen-concentration silicon oxynitride is still a work in progress, it is far ahead of the development of other candidates to replace silicon dioxide.

## *Metal Oxides*

Despite the significant progress in the development of silicon nitride or high-nitrogen-concentration silicon oxynitride, it is obvious that due to the mediocre dielectric constant, silicon nitride or high-nitrogen-concentration silicon oxynitride only can serve as an interim solution. We must look into other alternative dielectrics with higher dielectric constants. Many metal oxides have desirable dielectric constants. Therefore, it's natural for us to look into the big pool of metal oxides to search for the next viable gate dielectric to replace silicon dioxide. In principle, any non-radioactive metal oxide with a solid phase at room temperature is a potential candidate. However, the stringent requirements to succeed silicon dioxide have ruled out most of them, and later in this chapter, we will have a more detailed discussion about the requirements for the future high-k gate dielectrics. Originally, both  $\text{TiO}_2$ <sup>54,55,56,57,58</sup> and  $\text{Ta}_2\text{O}_5$ <sup>59,60,61</sup> were the leading candidates to succeed silicon dioxide. Both have large dielectric constants. The dielectric constant is about 25 for  $\text{Ta}_2\text{O}_5$ , and as high as 80 for  $\text{TiO}_2$ . Both have been used and researched for a while in the semiconductor industry, especially for memory applications. However, they are thermally unstable on Si<sup>62,63</sup>. Both tend to form silicon dioxide or possibly silicides when in contact with Si. Moreover, their low barrier heights over silicon make them less favorable to replace silicon dioxide<sup>64</sup>.  $\text{Al}_2\text{O}_3$ <sup>65,66,67</sup> was another leading candidate in the early stage. Its large band gap and high barrier height over silicon conduction band edge and thermal stability on Si make it very attractive to replace Si. However, its mediocre dielectric constant, about 9, causes serious concern.  $\text{ZrO}_2$ <sup>68,69,70</sup>,  $\text{HfO}_2$ <sup>71,72,73</sup> and their silicates<sup>70,74</sup> are the front-runners to become tomorrow's gate dielectric for Si CMOS technology.  $\text{ZrO}_2$  and  $\text{HfO}_2$  are very similar in many properties. Both have reasonably high dielectric constants, 20 to 25; large enough bandgap, about 5eV; and thermal stability with Si from the theoretical thermodynamic calculation<sup>69</sup>. All these desirable characteristics make these two

metal oxides very appealing. Some other materials, such as  $\text{La}_2\text{O}_3$ <sup>75,76</sup>,  $\text{Y}_2\text{O}_3$ <sup>76,77</sup>, and  $\text{Gd}_2\text{O}_3$ <sup>77</sup>, have been studied as well. Though every effort has been devoted to study many metal oxides, we are still facing an up hill battle to employ any metal oxide to replace silicon dioxide.

### **Ferroelectric Materials**

Ferroelectric materials are also considered to be possible long-term candidates for gate dielectrics. Many ferroelectric materials possess very high dielectric constants, from 200 to even 5000 in bulk form, though most of these materials show lower dielectric constants as thin films. Materials with a perovskite crystal structure, such as PZT<sup>78</sup> and SBT<sup>79</sup>, show the most promise. However, it's most likely that ferroelectric materials will be used in memory applications instead of for gate dielectric applications.

## **1.4 Other Issues with Ultra-thin Gate Dielectrics**

### ***1.4.1 Equivalent Oxide Thickness***

Two gate dielectrics with different dielectric constants can achieve the same capacitance per unit area with two corresponding physical thicknesses. Therefore, the physical thickness of a gate dielectric is no longer a useful parameter to compare against silicon dioxide in terms of the device performance. As described in Equation 1.4:

$$EOT = \frac{3.9}{K_{dielectric}} T_{physical}, \quad (1.4)$$

the Equivalent-Oxide-Thickness (EOT), a simple but useful concept, is derived from equating the capacitance per unit area achieved by an alternative gate dielectric to that of silicon dioxide to compare different gate dielectrics more directly.

However, quantum confinement effect<sup>80,81,82</sup>, polysilicon depletion effect<sup>7,83</sup>, leakage current, and series resistance further complicate the accurate measurement of EOT of ultra-thin gate dielectrics.

### ***1.4.2 Quantum Confinement Effect***

Quantum mechanics plays a significance role again. When a classical model, such as Maxwell-Boltzman (MB) model or Fermi-Dirac (FD) model, is employed to calculate the distribution of inversion charge in Si, it always predicts the maximum charge density appearing at the Si/dielectric interface, and it decays fast into the bulk Si region. However, quantum mechanics describes a drastically different picture<sup>80,81,82</sup>. As illustrated in Figure 1.8, the dielectric energy barrier and the bent Si conduction band under electric fields form a potential well to confine electrons, so the electrons must be treated as a 2-D gas, especially in the high electric field region. The calculated electron wave function gives rise to an electron density peak away from the interface, and goes to near zero at the interface, as shown in Figure 1.9. Because of such a distribution of electron density, it will add about 0.3 nm on top of the gate oxide thickness, which is quite significant, if the gate oxide thickness is below 3 nm.

### ***1.4.3 Polysilicon Depletion Effect***

Using polysilicon gate was a big step forward for Si CMOS technology<sup>5</sup>. However, being a semiconductor cannot avoid depletion, and thus the polysilicon depletion effect<sup>7,83</sup>.

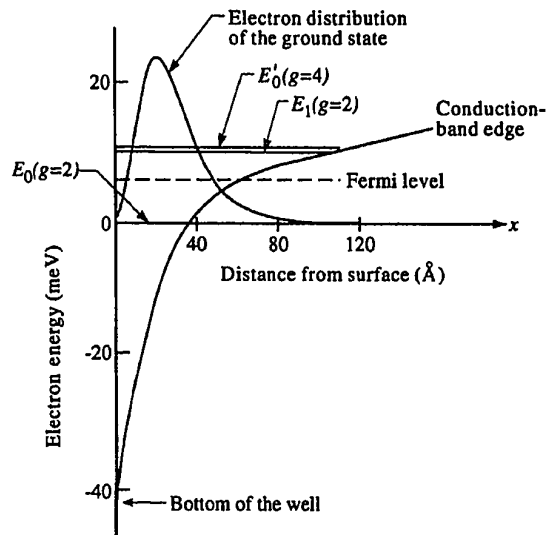


Figure 1.8 The electron distribution and energy levels in MOS system under inversion by quantum mechanical calculation<sup>81</sup>.

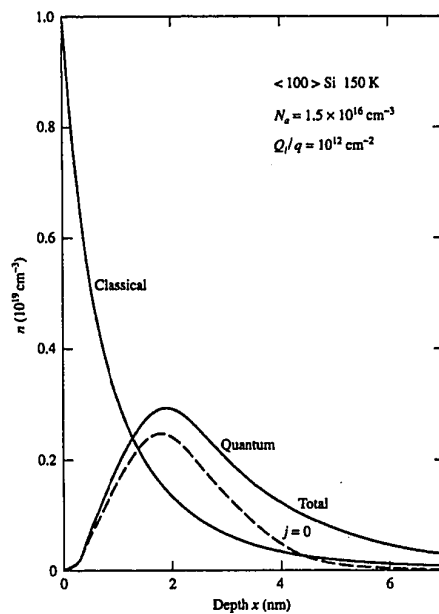
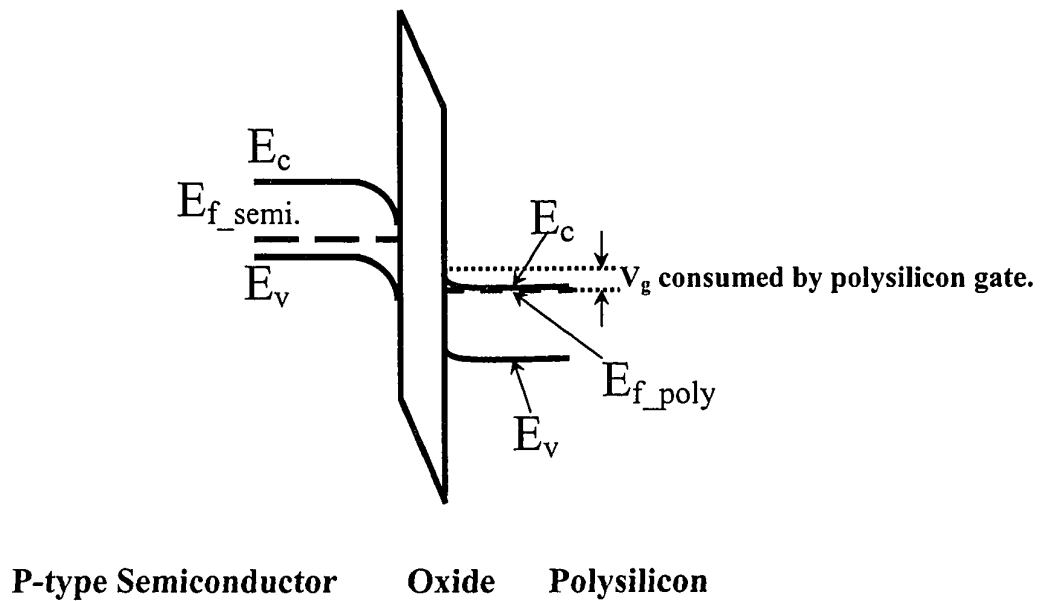


Figure 1.9 The comparison of classically and quantum mechanically calculated electron distribution in MOS system under inversion<sup>80</sup>.



## PolySilicon Depletion

Figure 1.10 The energy band diagram for Polysilicon-Oxide-p-type Semiconductor system in inversion reveals the cause of polysilicon depletion effect.

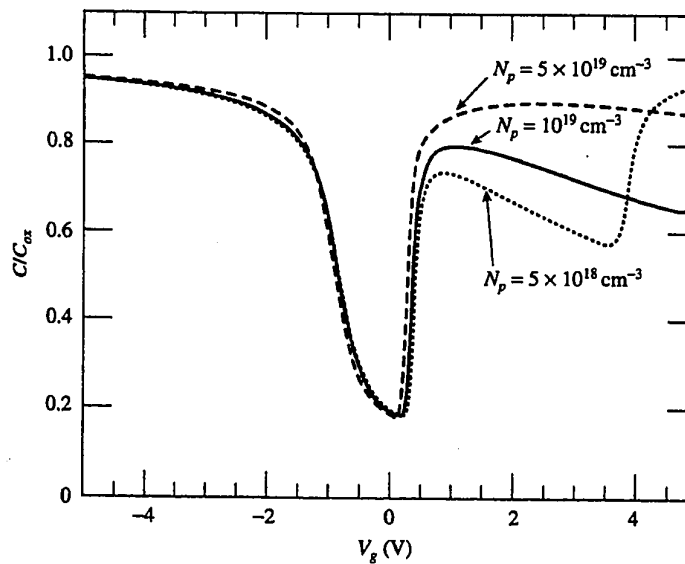


Figure 1.11 The polysilicon depletion effect on inversion capacitance of MOSFET with different polysilicon gate doping concentrations<sup>83</sup>.

Figure 1.10 shows the band diagram of an nMOSFET with  $n^+$  polysilicon gate. When the device is inverted, the  $n^+$  polysilicon gate is under depletion, resulting in an additional capacitance in series with the gate oxide capacitor, which reduces the total gate capacitance. The polysilicon depletion effect results in an additional 0.4 nm to the EOT of the gate dielectric and that due to the quantum confinement effect. Figure 1.11 shows the effect of the polysilicon depletion on the gate capacitance in inversion region, and it's clear that polysilicon depletion is much worse for polysilicon gate with less doping<sup>83</sup>. The extra EOT caused by polysilicon depletion effect is becoming intolerable for ultra-thin gate dielectrics, so using metal gate to replace polysilicon gate has been proposed to solve this problem<sup>92</sup>.

#### ***1.4.4 C-V Measurement in the Presence of High Leakage Current***

The Capacitance-Voltage (C-V) measurement is a convenient and accurate method to determine the gate capacitance or EOT. However, for an ultra-thin gate dielectric, the large leakage current and series resistance cause distortion of the measured C-Vs, especially in accumulation and inversion regions, due to the higher leakage currents.

For an ideal capacitor, the equivalent circuit can be described in Figure 1.12 (a): a capacitor is in series with the series resistance coming from the bulk and connecting resistances. However, for a capacitor with an ultra-thin gate dielectric, Figure 1.12(a) is no longer a valid description. The capacitor with an ultra-thin gate dielectric can be illustrated as a capacitor in parallel with a resistor. Therefore, even for the simplest equivalent circuit, there are three components, as illustrated in Figure 1.12(b). No matter whether the LCR meter is set to the parallel mode or series mode, the measured C-V can only provide one capacitance value and one conductance or resistance value at once. We have three unknowns, but only two independent measured data. Thus, it gives large uncertainty in the capacitance value. In order to solve this problem, we must design suitable test structures

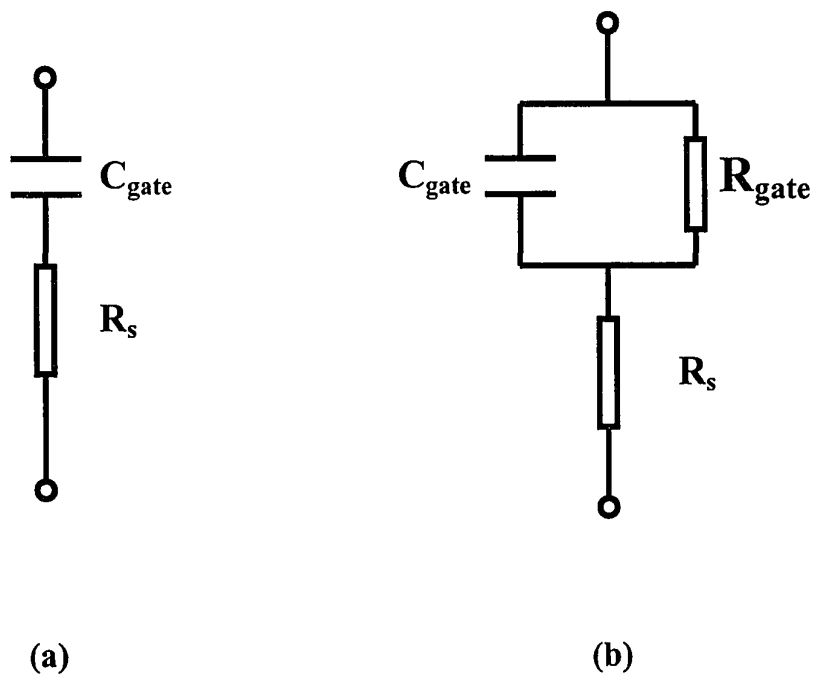


Figure 1.12 Equivalent circuit models. (a) represents model of gate capacitor without leakage current; (b) represents model of gate capacitor with leakage current.

and choose proper frequencies during the C-V measurement to reduce the influence of the gate leakage current and series resistance. Because the gate leakage current is much smaller in depletion region than that in accumulation or inversion region, one technique uses a least square fit of the portion of C-V between depletion and accumulation to a theoretical model to extract the gate oxide thickness<sup>84</sup>. Another method is to use two C-V measurements at different frequencies to extract the real C-V curve<sup>85</sup>. Because two C-V measurements provide us with 4 independently measured data points, two capacitance values and two conductance values, we will be able to obtain the real C-V.

### ***1.4.5 Other Emerging CMOS Technologies***

Besides new gate dielectric materials, many other new technologies, such as Silicon-On-Insulator (SOI)<sup>86,87</sup>, silicon germanium (SiGe) technology<sup>88,89</sup>, and metal gates<sup>90,91,92</sup>, or new device structures, such as Double-gate MOSFET<sup>93,94</sup> or FIN gate MOSFET<sup>95,96</sup>, are being developed to extend the scaling of Si CMOS. We choose two technologies that are closely related to gate dielectrics to discuss.

#### **Silicon Germanium Technology**

Recent work from IBM and other groups reveals that, using a SiGe layer to tensile strain the upper Si channel layer will significantly enhanced the electron mobility<sup>88</sup>. It has been known for a while that, because the six-fold degeneracy of Si conduction band is broken under the tensile strain, electrons tend to stay in the lower effective mass and lower energy sub-bands<sup>97,98</sup>. Therefore, it enhances the electron mobility. The tensile strain also breaks the heavy hole and light hole degeneracy. Thus, it raises the hole mobility as well. SiGe alloy has larger lattice constant and compatible with Si CMOS process, thus it is an ideal candidate to enhance channel carrier mobility. Since a typical MOSFET using a high-

k gate dielectric shows a lower mobility than that of MOSFET using silicon dioxide as the gate dielectric<sup>99</sup>, it seems that employing SiGe technology together with a high-k gate dielectric is a possible solution to compensate for the loss of mobility in MOSFET with high-k gate dielectrics.

### **Metal Gate**

As we discussed before, the polysilicon depletion can add about 0.4 nm to the EOT of the gate dielectric, which is significant when considering that the EOT of today's gate dielectrics is less than 2nm, and one day this 0.4 nm will be more than we can bear. In order to eliminate the polysilicon depletion, we have to abandon the almost exclusively used polysilicon gate technology, and find a suitable metal gate technology. From a device design point of view<sup>100</sup>, either a dual-gate metal technology or a single-gate metal technology is feasible for certain device structures. For bulk or partially depleted SOI technology, because of the need of heavy doping to control short channel effect and requirement of threshold voltage, it's desirable to use the dual-gate metal technology with the work function of one metal close to the Si conduction band and the work function of the other metal close to the Si valence band<sup>100</sup>. For double-gate MOSFET or fully depleted SOI device structure, single-gate metal close to the mid-gap of Si is suitable<sup>100</sup>. In addition to the right work function and low resistance, when considering the process integration issues, there are many more stringent requirements. First, a damage-free metal deposition technology, such as a CVD technology, must be found to deposit metals. Second, either finding metals which can sustain the high thermal budget during CMOS process or changing the process flow to low thermal budget to accommodate metals is necessary. Last, but not least, are the integration issues with high-k gate dielectrics. A combination of metal gate electrodes and high-k gate dielectrics is the ultimate gate stack for which we are

looking. However, when a metal contacts with a dielectric, because the dipole formed at the metal/dielectric interface can change the effective work function of the metal and dielectric, different metal/dielectric combinations can have different work functions, which complicates the metal work function requirement. Moreover, the possible chemical reaction between metal and dielectric can further complicate the situation. Because of the significant benefits brought by the metal/high-k gate stack, notable research activities are on going in this area.

## **1.5 The Requirements for High-k Gate Dielectrics**

Using high-k gate dielectrics to succeed silicon dioxide is a simple but brilliant idea. However, the real world is much more complicated. And, moreover, silicon dioxide is a tough act to follow. We have discussed the limits of silicon dioxide, but there are many superb qualities of silicon dioxide, and that's why silicon dioxide has been called a "God-sent" material. So, before we discuss the requirements for high-k gate dielectrics, we first review many premium qualities of silicon dioxide, which can be set as the benchmarks for high-k gate dielectrics.

### ***1.5.1 Merits of Silicon Dioxide***

Silicon dioxide is the natural oxide of silicon. Moreover, after decades of research and development, it has remarkably low interface and bulk trap densities and low fixed charge density. The mid-gap interface state density is  $\sim 10^{10} / \text{cm}^2 \text{eV}$ , and the bulk defect density is about  $10^{10} / \text{cm}^2$ . Therefore, it minimizes the trap-assisted leakage current and maintains high channel carrier mobility. The breakdown strength of silicon dioxide is about 10 to 15

MV/cm, which is remarkable. Few defects and high breakdown strength ensure the high reliability of silicon dioxide. In addition, silicon dioxide is thermally grown. The growth method is more economical and easier to control than deposition methods. Last, but not least are integration issues. Through the years, the industry has tailored a process to accommodate silicon dioxide. Since the industry has invested enormous resources to develop this process, it would like to continue to use it. So, it brings more challenges for implementing high-k dielectrics.

With these benchmarks in mind, we will discuss the more detailed requirements for the future gate dielectrics. Since metal oxides are the focus of this thesis, our discussion will focus on them.

### ***1.5.2 Dielectric Constant and Barrier Height***

First, the new gate dielectric should have high dielectric constant and high barrier height. The primary motivation to find a new gate dielectric to replace silicon dioxide is to reduce the leakage current significantly. As shown in Equations 1.2 and 1.3, either for direct tunneling or Fowler-Normheid tunneling, the current reduction is exponentially dependent on the dielectric thickness. A material with higher dielectric constant can achieve the same capacitance per unit area with a larger thickness, which results in a lower leakage current. Also, with a larger physical thickness, the material with a higher dielectric constant has potential of serving more CMOS technology generations than the material with a lower dielectric constant.  $\text{Al}_2\text{O}_3$ , because of its relatively low dielectric constant, only about 9, is less likely to be a serious contender to replace silicon dioxide. The tunneling current is also exponentially related to the barrier height. Moreover, considering that usually chips are working at elevated temperatures, it's important to employ a dielectric with high barrier height to block the thermionic current.  $\text{Ta}_2\text{O}_5$  and  $\text{SrTiO}_3$  both were

early contenders, but their low barrier heights over Si, less than 0.5 eV, cloud their future applications.

### ***1.5.3 High-k Gate Dielectrics/Si Interface***

Second, it is extremely important to have an excellent Si/dielectric interface, in terms of both electrical properties and thermal stability. Most high-k gate dielectrics show mid-gap interface-trap densities in the  $10^{11} - 10^{12} / \text{cm}^2 \text{eV}$  range<sup>101</sup>, which is much higher than that of silicon dioxide. We are not sure about the spatial distribution of fixed oxide charge, but if we assume most of it is located at the interface, the fixed charge density is about  $10^{12} / \text{cm}^2$ , which is also significantly higher than that of silicon dioxide. The traps and fixed charges may result in significant degradation of drive current or transconductance, serious flat band shift, instability during device operation, and reliability concerns. It is difficult to imagine that there is any material that will have a better interface with Si than silicon dioxide. Therefore, it's natural to try to solve the interface quality problem by inserting a thin layer of silicon dioxide. However, we need to pay a notable price for this solution. Because the two dielectrics are in series, the total capacitance will be reduced. The EOT of this gate stack structure is expressed in Equation 1.5:

$$EOT_{total} = T_{interface} + \frac{3.9}{K_{high-k}} T_{high-k} . \quad (1.5)$$

We are facing a dilemma here; a better interface or a smaller total EOT. Moreover, it is extremely difficult to control the interface of Si and metal oxides during the deposition and subsequent annealing process. From thermodynamic calculations, some materials, such as Ta<sub>2</sub>O<sub>5</sub> and TiO<sub>2</sub>, are unstable on Si, upon annealing; they either form silicon dioxide layer to increase the total EOT of the gate dielectrics, or form silicides to short out the source and drain. Even for materials that are supposed to be thermally stable on Si from

thermodynamic calculations, such as  $\text{ZrO}_2$  and  $\text{HfO}_2$ , to the best of our knowledge, no group has ever produced a high-k stack without the formation of an interfacial layer. For the conventional CMOS process flow, the gate dielectric typically experiences an annealing step at a temperature higher than 950 °C for the source and drain activation, which poses more challenges to control the interface between high-k materials and Si.

#### ***1.5.4 Bulk Properties of High-k Gate Dielectrics***

Third, the bulk properties of the gate dielectrics are critical too. The high density of defects or traps in the bulk of a high-k gate dielectric may have the following adverse effects: (1) It may cause trap-assisted current, thus undermines our effort to reduce leakage current through the use of high-k gate dielectrics; (2) The high densities of traps and charges may result in degraded drive current or transconductance; (3) The traps and charges in the dielectric may cause instability during device operation, such as unstable threshold voltage<sup>102</sup>; (4) The high density of defects in the gate dielectric leads to weak spots and possible breakdown paths, which may result in degraded breakdown field strength and gate dielectric lifetime<sup>103</sup>. Therefore, it is crucial to reduce the bulk oxide defects and charges. For the film morphology, it will be desirable to select a material with amorphous phase. A working chip requires good uniformity among numerous devices. However, because of the different grain orientations and grain boundaries, a polycrystalline gate dielectric fails to provide such uniformity across the whole chip, which may prove problematic for designers and manufacturers. To prevent the forming of silicon dioxide layer during the process flow, the high-k gate dielectric should be a good barrier for oxygen diffusion as well. The interface between gate electrode and gate dielectric also needs to be controlled. A polysilicon compatible material, such as  $\text{HfO}_2$ <sup>104</sup>, is crucial for a polysilicon gate process flow. Moreover, since metal gates could be used to replace polysilicon gate

eventually, new gate dielectric should have the right metal-dielectric work function, and compatibility among each other.

Now high-k gate dielectrics are far from satisfying these stringent requirements, and significant research efforts should be devoted to accelerate the progress.

## 1.6 Chapter Summary

The MOSFET has become the dominant device in the semiconductor industry since the early 70's. Nowadays the MOSFET is smaller, faster, and consumes less power than ever. Therefore, we are able to fabricate microchips, denser, faster, with more functions and less power dissipation. Yet after more than 30 years, the evolution is still going strong. However, the unprecedented scaling of MOSFET is not an easy walk. It took great efforts in research and development by the semiconductor industry and academia to push the scaling forward. Now with the gate length of Si MOSFET standing at 100 nm and below, the scaling of MOSFET is facing even more difficulties. Especially, for the first time, the usage of the most critical element of the MOSFET, silicon dioxide, is brought into question. The near-term solution, silicon oxynitride, is moving into production now. The long-term solutions and the focus of this thesis, high-k gate dielectrics, are rising from the horizon. Together with other new technologies, we have great confidence that high-k gate dielectrics will extend the extraordinary journey of CMOS scaling much further.

## **Chapter 2**

### **Zirconium Oxide ( $\text{ZrO}_2$ ) Made by Jet-Vapor-Deposition (JVD)**

As the gate length of Complementary Metal-Oxide-Semiconductor Field Effect Transistor (CMOSFET) is entering the sub-0.1 micron region, new gate dielectrics with higher dielectric constants--high-k gate dielectrics are under intensive research to succeed silicon dioxide. One major advantage of implementing high-k gate dielectrics is to reduce the gate tunneling leakage currents while maintaining the same or less Equivalent-Oxide-Thickness (EOT), which will increase the drive ability of MOSFET, and reduce its standby power consumption. However, employing high-k gate dielectrics presents tremendous challenges, because new high-k gate dielectrics must satisfy numerous stringent requirements as we discussed in Chapter 1. Among various candidates,  $\text{ZrO}_2$  and its

silicates<sup>68,69</sup> are among the promising to replace conventional thermal silicon dioxide as the gate dielectric.

In this chapter, we report on the electrical and physical properties of ultra-thin  $\text{ZrO}_2/\text{Zr}$  silicate films deposited by the Jet-Vapor-Deposition (JVD) process. Both MOS capacitors and MOSFETs were successfully fabricated. It is shown that JVD  $\text{ZrO}_2/\text{Zr}$  Silicate gate dielectrics can have equivalent oxide thicknesses (EOT) down to 1 nm, and possess high thermal stability, low leakage, high reliability, and other good electrical properties. Our analysis also shows that the compositions of JVD films vary with thickness. Thinner films are found to be Zr-silicate-like whereas thicker films are likely graded with a transition to stoichiometric  $\text{ZrO}_2$ . The presence of a thermally stable Zr silicate interfacial layer may prevent the formation of interfacial silicon oxide, despite the fact that *as-deposited* films are found to be oxygen rich. In contrast to other  $\text{ZrO}_2$  films reported in the literature, the EOTs of our films decrease after post-deposition annealing. From this study, JVD  $\text{ZrO}_2/\text{Zr}$  silicate was found to be able to survive an annealing temperature as high as 1000 °C, suggesting that JVD  $\text{ZrO}_2/\text{silicates}$  can be used in a conventional CMOS process, and no replacement-gate process is needed. In the last part of this chapter, using the examples of aluminum gate electrode and platinum gate electrode on top of  $\text{ZrO}_2$ , I will discuss the effects of different metal gate electrodes on the EOT and current transport properties. The results reveal the importance of choosing the proper gate electrodes for high-k gate dielectrics.

## 2.1 Jet-Vapor-Deposition (JVD) Process

The Jet-Vapor-Deposition (JVD) process, which was invented by Schmitt and Halpern<sup>105, 106</sup> is an innovative, versatile and potent technique for synthesizing high quality thin solid films. The major innovations of JVD are the “sonic jet in a low-vacuum fast flow” transporting condensable vapor to a substrate, and the “multiple jets, moving substrate” strategy<sup>107</sup> for depositing various solid films<sup>108</sup>.

### 2.1.1 Gas Flow

In JVD, a light inert gas, such as helium (He), forms a fast gas flow which is sustained by a low vacuum environment to carry out the vapor source generated in a nozzle to the substrate. Due to the pressure difference between the nozzle and the low-vacuum process chamber, as soon as the jet leaves the nozzle, it expands into a fast gas flow traveling at super-sonic speed, in which all atoms or molecular are moving in the same direction. When the pressure ratio of  $P_n/P_c$ , where  $P_n$  is the pressure in the nozzle pressure and  $P_c$  is the process chamber pressure, passes the Mach number, the species inside the jet move at super-sonic speed<sup>105</sup>. The Mach number,  $G$ , is given as,

$$G = \left(\frac{\gamma + 1}{2}\right)^{\gamma/(\gamma + 1)}, \quad (2.1)$$

where  $\gamma$  is the ratio between the two specific heats,  $C_p/C_v$ , which has a value of less than 2.1 for all gases<sup>109</sup>. The free super-sonic jet is created independent of the chamber boundary conditions and background pressure. As illustrated in Figure 2.1, the vapor source is carried out of the nozzle in a clear defined jet, and then it reaches the substrate and forms a laminar stream on the surface of the substrate. During the deposition, the jet is fast, highly

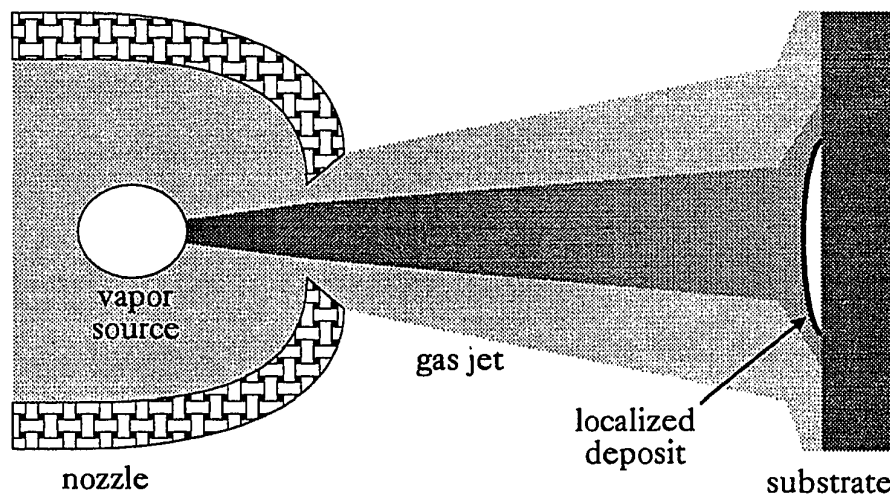


Figure 2.1 Schematic of a Jet Vapor Deposition (JVD) source with jet formation.

directional, and well defined. Thus, the deposition is localized and efficient. Because the sound velocities of commonly used carrier gases are quite large, (for example, the sound velocities of He and Ar are 1.02 km/sec and 0.322 km/sec respectively.) the kinetic energies of the atoms and molecules carried in the super-sonic jet can be as high as a fraction of 1 eV, which is equivalent to hundreds or thousands of degree Celsius in thermal energy. For example, the thermal energy of nitrogen atoms carrier by He is equivalent to 700 °C - 800 °C. Unlike many CVD processes, which require an elevated substrate temperature in order to provide enough thermal activation energy to sustain chemical reactions during film deposition, with such a high kinetic energy, JVD can complete many film depositions without heating the substrate. This unique feature is advantageous for ultra-thin film deposition. JVD possesses another unique feature of shielding effect. The difference of pressure inside the jet nozzle and pressure of the process chamber prevents diffusion of impurities into the jet. Moreover, because neither "information" nor mass can propagate upstream in a fast gas flow moving at a super-sonic speed, each jet maintains its own independence. This key feature guarantees that any two jets do not interfere with each other during processing, and this feature is very important for multi-jet deposition. As a result of the independence of jets and the short transport time of species from nozzle to the substrate, reactions only happen at the surface of the substrate.

### ***2.1.2 Vapor Source***

Another advantage of JVD is its high flexibility of selecting vapor sources. The vapor source could be a sputtered vapor source, a thermally evaporated vapor source, a microwave plasma vapor source, or even gas directly from a gas tank.

For metal oxide deposition, the metal vapor is generated by Direct Current (DC) sputtering in argon ambient of 1 Torr pressure, as shown in Figure 2.2. A tungsten

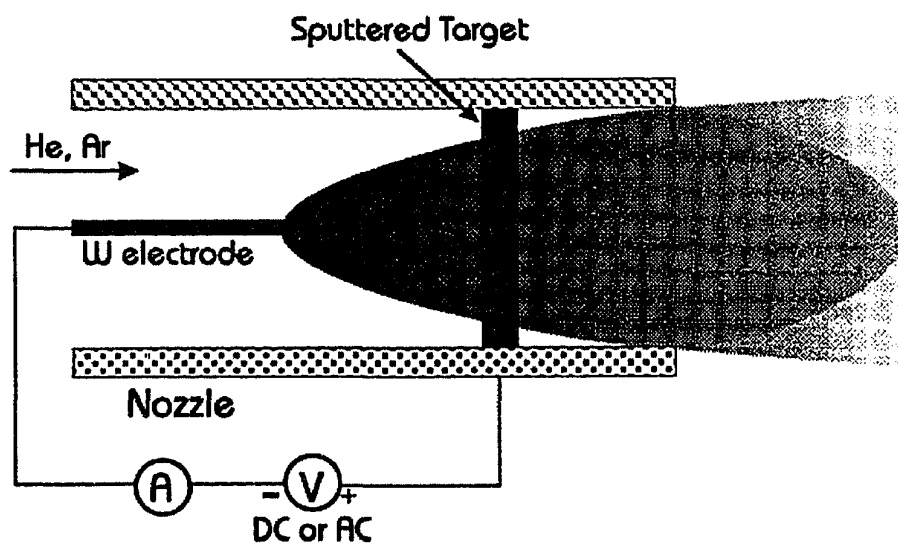


Figure 2.2 Schematic of a JVD sputtering vapor source using metal target.

electrode is connected to a negatively biased power supply, and a glow discharge is generated and upheld between the tungsten electrode and the metal target. The plasma and the sputtered metal vapor are carried out of the nozzle by He gas. The sputtering current providing the vital information of the sputtered species is closely monitored by an ammeter to sustain the optimal sputtering condition. In order to reach a strong jet formation condition, the downstream pressure is kept about 0.1 Torr to maintain a 10 to 1 upstream-to-downstream pressure ratio. Unlike CVD or Atomic Layer Deposition (ALD) which requires precursors for film deposition, the sputtering vapor source of JVD has vast flexibility. In principle, it can employ any pure metal as the target to form metal vapor, which constitutes a big advantage over CVD and ALD. Moreover, JVD enjoys advantages over conventional sputtering process as well. The pressure in the sputtering region of JVD can be as high as 1 Torr. At such a high pressure, the sputtered species tend to be thermalized with He carrier gas when they exit the sputtering region. As we discussed before, the kinetic energy of the species carried downstream by He is about a fraction of 1 eV, which does not cause damage to the substrate. Multiple metal vapor sources can be generated simultaneously, and carried out in separate jets to form multi-component metal alloys or metal oxides. In order to form metal oxide, another type of jet source is used to supply oxygen. Oxygen is delivered from a nozzle at super-sonic speed by helium to the surface of the substrate to oxidize the deposited metal to form metal oxide. A microwave cavity may be added to the oxygen gas nozzle to generate atomic oxygen for the oxidation of metal.

### ***2.1.3 Substrate Movement***

Because of the limit of the jet size, and to accommodate multiple vapor sources, a specially designed motion system of substrate was developed to achieve uniformity of the deposited film. The diameter of the jet is usually about 1-2 cm, but the diameter of the substrate is at least 2 inches. Therefore, in order to achieve the desired uniformity of deposited film, either the substrates or the vapor sources have to move during the deposition. Due to the complexity of the setup of the vapor sources, especially considering the possibility of employing multiple vapor sources simultaneously, a design with the movement of the substrates was implemented. As shown in Figure 2.3, a carousel sits at the center of a cylindrical chamber. Wafers are mounted on the sidewalls of the carousel, and the vapor sources facing the carousel are mounted on the sidewall of the chamber. The carousel spins at a constant speed and moves vertically with a linear translation oscillation simultaneously to realize the required thickness uniformity of the deposited film. During each cycle, all vapor sources will scan through the wafers once to ensure the uniformity of the component concentration of the deposited film. The combination of the motion system and the vapor sources makes it possible to achieve sub-monolayer deposition: less than one monolayer of metal or other materials may be deposited during one cycle, which enables uniform blending of several components at the sub-monolayer level. The substrate holder can be heated by a resistance heater during deposition. However, for the ultra-thin gate dielectrics studied in this dissertation, the deposition was done at room temperature.

Combining the unique super-sonic gas flow jet, the versatile vapor sources and the motion system, JVD is a very useful tool for thin film deposition, and excellent quality of dielectrics has been demonstrated in JVD nitride<sup>52</sup> and other films to be revealed in this dissertation.

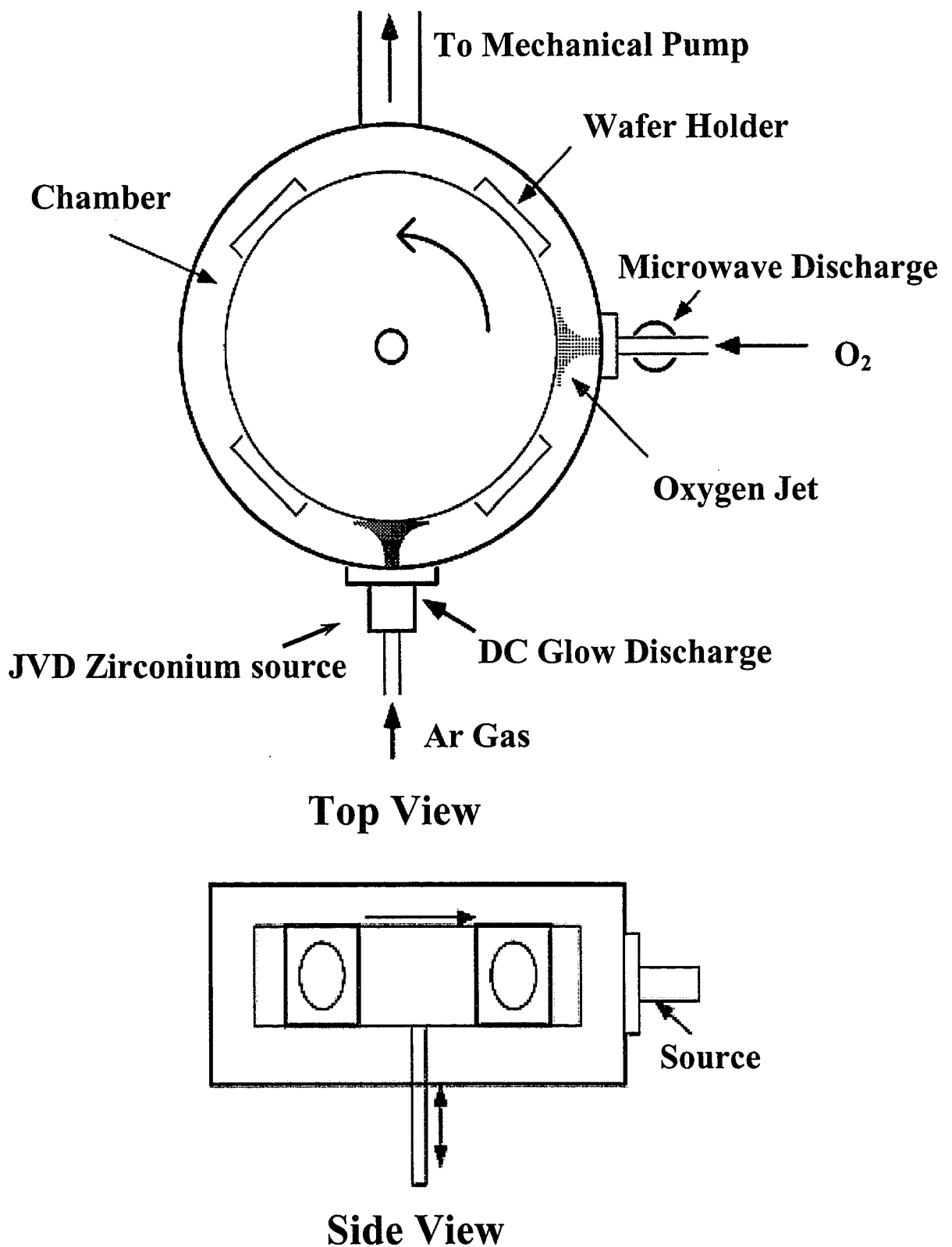


Figure 2.3 Schematic of the top view and the side view of the JVD system for  $\text{ZrO}_2$  deposition.

## 2.2 Device Fabrication

During the course of the dissertation study, MOS capacitors and MOSFETs were fabricated at Yale to study the properties of  $\text{ZrO}_2$  and other high-k materials. Figures 2.4 and 2.5 illustrate the process flows to fabricate MOS capacitors and MOSFETs with  $\text{ZrO}_2$  or other high-k materials as gate dielectrics. Most fabrication steps of the  $\text{ZrO}_2$  or other high-k MOS capacitors or MOSFETs follow the standard procedure for making MOS structures, except for the unique JVD gate dielectric deposition.

Unlike other methods, such as ALD, in which an ultra-thin silicon dioxide layer is required in order to grow high-quality  $\text{ZrO}_2$ <sup>110</sup>, high-quality JVD  $\text{ZrO}_2$  films are deposited by JVD process at room temperature on HF-last Si wafers directly. The omission of the ultra-thin silicon dioxide layer simplifies the process, and reduces the total EOT of the gate dielectric. The Post-Deposition-Anneal (PDA) is an important step to improve the quality of JVD  $\text{ZrO}_2$ , and usually the PDA of JVD  $\text{ZrO}_2$  is carried out at 550 °C or above. A sufficiently long PDA time at an elevated temperature is necessary to reduce the defects and improve the interface properties of JVD  $\text{ZrO}_2$  gate dielectrics. However, excessive annealing in an oxygen-rich environment may lead to the growth of the interfacial layer between  $\text{ZrO}_2$  and Si, which compromises the total EOT of JVD  $\text{ZrO}_2$ . In order to reduce the total EOT of JVD  $\text{ZrO}_2$ , normally the PDA is conducted in a dry ambient, such as nitrogen or forming gas. After the PDA, usually Aluminum (Al) or Platinum (Pt) is thermally evaporated on top of the  $\text{ZrO}_2$  films to form the top electrodes of MOS capacitors or MOSFETs. The Post-Metallization-Anneal (PMA) is another method to improve the quality of gate dielectrics. However, we found that the PMA usually leads to either degradation of JVD  $\text{ZrO}_2$  gate dielectrics in the presence of aluminum gate electrodes or

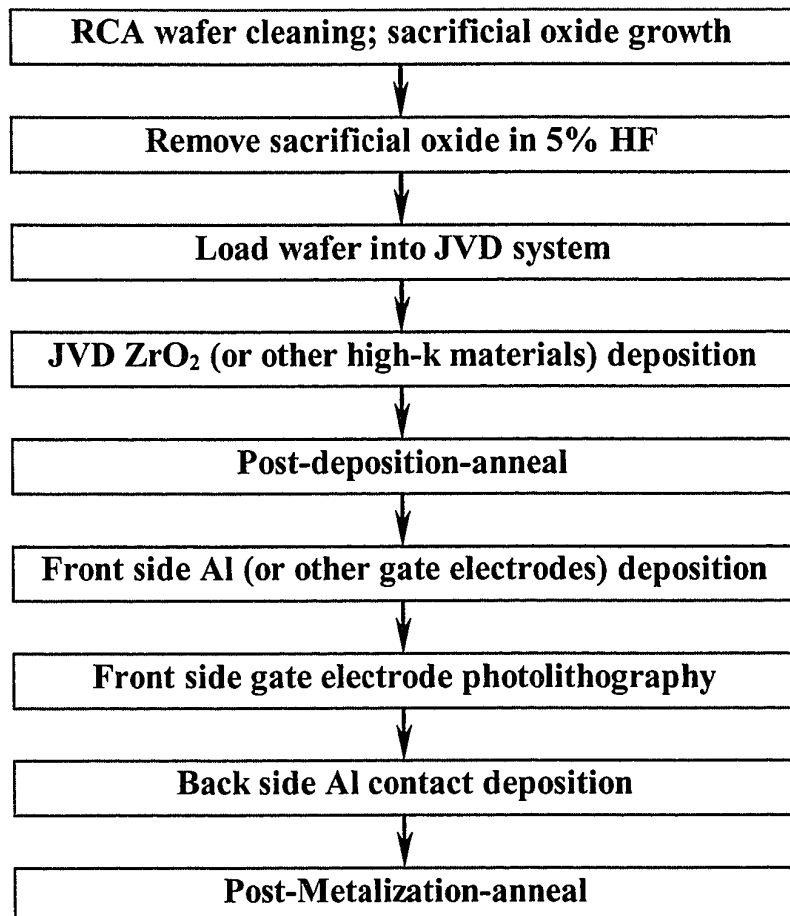


Figure 2.4 The process steps for JVD ZrO<sub>2</sub> (or other high-k materials) based MOS capacitor.

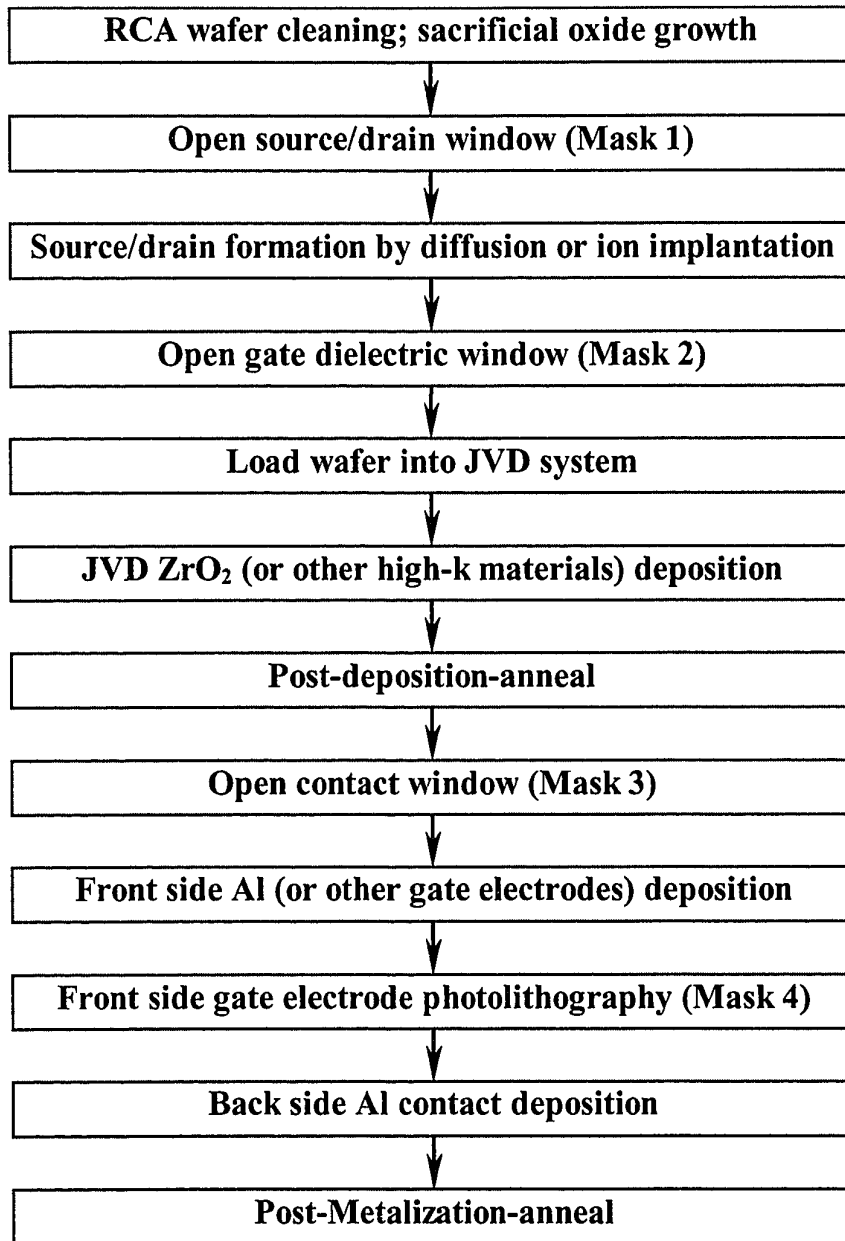


Figure 2.5 The process steps for JVD  $\text{ZrO}_2$  (or other high-k materials) based MOSFET.

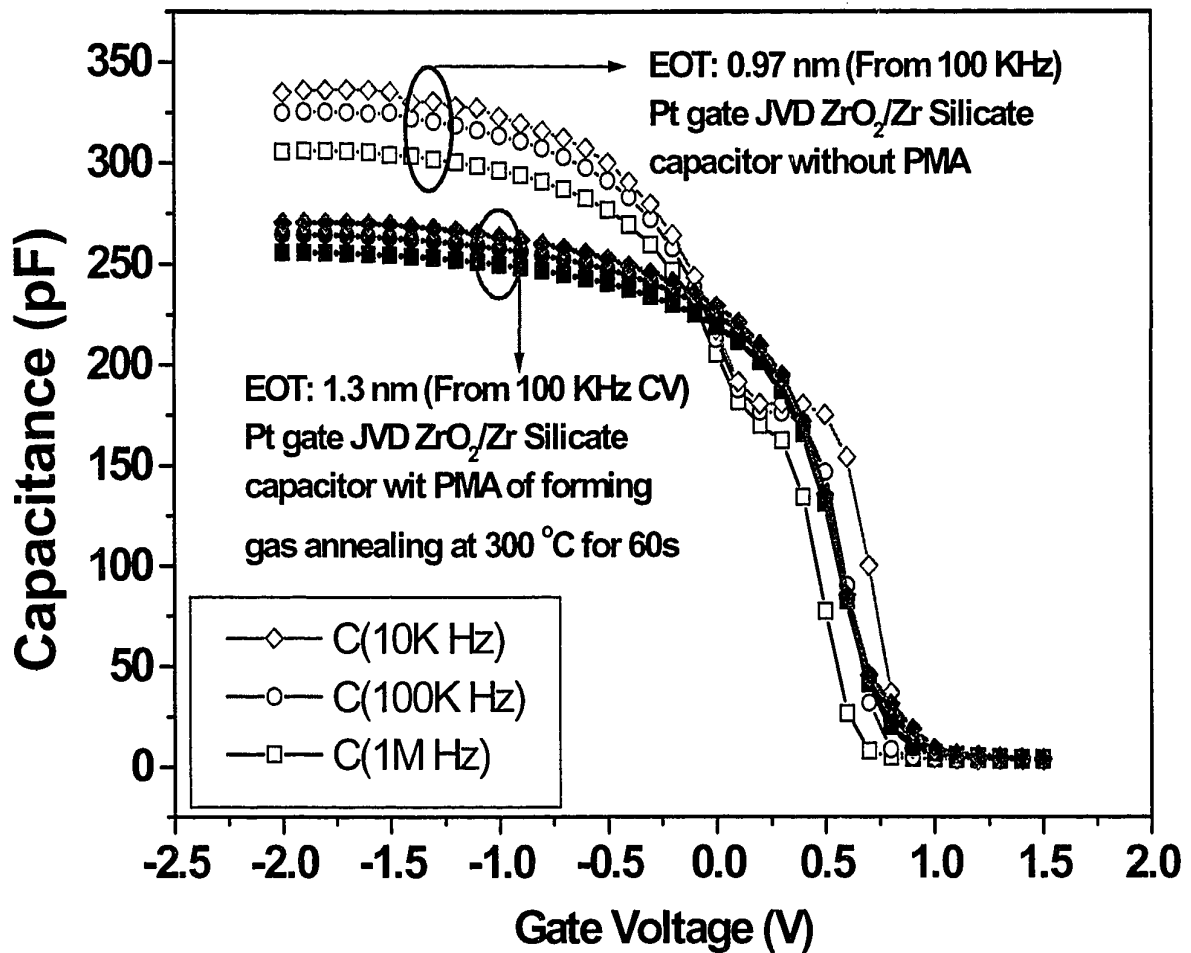


Figure 2.6 C-V Characteristics of Pt-gate JVD  $\text{ZrO}_2/\text{Zr}$  silicate gate dielectric reveal that, even with minimum annealing, the EOT increases from sub-1nm to 1.3 nm in the presence of the Pt gate.

significant growth of total EOT in the presence of Platinum gate electrodes. Possible reactions between  $\text{ZrO}_2$  and aluminum, or the diffusion of aluminum during PMA may result in the degradation of JVD  $\text{ZrO}_2$  quality. And platinum is known for serving as a catalyst to form the highly penetrating atomic oxygen, which may contribute to the significant growth of the total EOT after the PMA, as shown in Figure 2.6. The EOT of that JVD  $\text{ZrO}_2/\text{Zr}$  silicate gate dielectric increased from sub-1nm to 1.3 nm after only minimum PMA in forming gas. Therefore, usually no PMA was performed on devices using JVD  $\text{ZrO}_2$  as the gate dielectric.

## 2.3 Introduction to Zirconia ( $\text{ZrO}_2$ ) and Zircon ( $\text{ZrSiO}_4$ )

Zirconia ( $\text{ZrO}_2$ ), or Zirconium dioxide, is an important refractory oxide for both scientific and practical reasons. Before it drew the attention from the semiconductor industry for potential gate dielectric applications, because of its refractory nature, inertness to many hostile environments and availability, it had been used extensively in the high-temperature chemical industries. It also has been used extensively in solid-state electrochemical oxygen monitors due to its oxygen ion conduction property<sup>111</sup>. From the properties listed in Table 1.2,  $\text{ZrO}_2$  is a very promising candidate to replace silicon dioxide as the gate dielectric for Si CMOS. The dielectric constant of  $\text{ZrO}_2$  is about 23, and the bandgap of  $\text{ZrO}_2$  is more than 5 eV; moreover, it enjoys a relatively high barrier height, about 1.8 eV over the Si conduction band edge. The high dielectric constant, high bandgap, and high barrier height should reduce the tunneling leakage current significantly with good scalability. Furthermore, from thermodynamic calculations, when  $\text{ZrO}_2$  is in direct contact with Si at 1000 °K, it takes a positive free energy of 42.3 Kcal/mole to form silicon dioxide<sup>111</sup>. The difficulty of forming silicon dioxide with Si at elevated temperatures makes  $\text{ZrO}_2$  very

desirable for the conventional CMOS process flow, and provides a great potential for scalability. Though in reality the thermodynamic process is complicated by the presence of kinetic energy, when compared to the other high-k materials, such as  $\text{TiO}_2$  and  $\text{Ta}_2\text{O}_5$ ,  $\text{ZrO}_2$  still possesses better thermal stability. Moreover, JVD  $\text{ZrO}_2$  seems to possess a thermally stable interfacial layer on Si, which we will discuss more in this chapter.  $\text{ZrO}_2$  has three crystalline structures: monoclinic, tetragonal, and cubic. The monoclinic phase of  $\text{ZrO}_2$  is stable up to about 1100 °C. Above 1100 °C, the monoclinic phase transforms to the tetragonal phase, and the cubic phase has been observed at 2285 °C<sup>112</sup>.

Zircon ( $\text{ZrSiO}_4$ ), or zirconium silicate, is a mineral which has been used widely in the iron and steel industry. Zircon is chemically stable<sup>113</sup>. It is not attacked by inorganic and organic acids, except for hydrofluoric acid (HF). Zircon doesn't undergo dissociation until about 1500 °C to 2000 °C. In this temperature range, it disassociates into zirconia and silicon dioxide. Recently, with its acceptable dielectric constant, about 12-14, high barrier height of 2.1 eV, and high thermal stability on Si, it has become a serious contender in the race to replace silicon dioxide. During the JVD  $\text{ZrO}_2$  deposition, an interfacial layer of Zr silicate is unintentionally formed. This interfacial layer has demonstrated high thermal stability on Si, which will be discussed in more detail in Section 2.4.

## 2.4 General Properties of JVD $\text{ZrO}_2$ /Zr Silicate

High quality ultra-thin JVD  $\text{ZrO}_2$ /Zr silicate gate dielectrics were successfully synthesized. Both MOS capacitors and n-channel and p-channel MOSFETs were fabricated to evaluate the electrical properties. It is shown that films with equivalent oxide

thickness (EOT) of 1 nm still possess good properties. An interfacial layer whose composition resembles Zr silicate is formed during the JVD  $\text{ZrO}_2$  deposition. Therefore, we name our film JVD  $\text{ZrO}_2/\text{Zr}$  silicate.

#### ***2.4.1 C-V and I-V Characteristics of 1 nm (EOT) JVD $\text{ZrO}_2/\text{Zr}$ Silicate Films***

C-V measurement techniques are convenient and effective methods to evaluate the gate dielectric properties, such as the interface quality and the existence of mobile ions. For ultra-thin gate dielectrics, because of the existence of high leakage current, the quasi-static C-V measurement technique is no longer a valid tool. However, the multi-frequency C-V method is still effective to evaluate the gate dielectric quality. In Figure 2.7, some typical multi-frequency C-V characteristics of a JVD  $\text{ZrO}_2/\text{Zr}$  silicate film deposited on HF-last n-Si substrate are shown. The film went through a  $\text{N}_2$  Rapid Thermal Anneal (RTA) at 800 °C for 5 seconds, followed by a forming gas anneal at 550 °C. Aluminum was thermally evaporated to form the top electrode for this capacitor, and aluminum was also used as the back contact. To reduce the reaction with the electrode, no PMA was performed. After excluding the quantum confinement effect, the extracted EOT of this gate dielectric is 1.1 nm. The negligible frequency dependence and C-V hysteresis window indicate good interface and dielectric properties.

As we discussed before, the most important reason to implement high-k gate dielectrics to replace silicon dioxide for Si CMOS is to reduce the leakage current. JVD  $\text{ZrO}_2/\text{silicate}$  gate dielectrics satisfy this requirement by reducing leakage current significantly. In Figure 2.8, the Current-Voltage (I-V) characteristics of this 1.1nm film are compared to the calculated I-V of a 1.1nm thermal Silicon dioxide. In this case, the JVD  $\text{ZrO}_2/\text{silicate}$  capacitor is under substrate injection. Thus, electrons transport from the n-

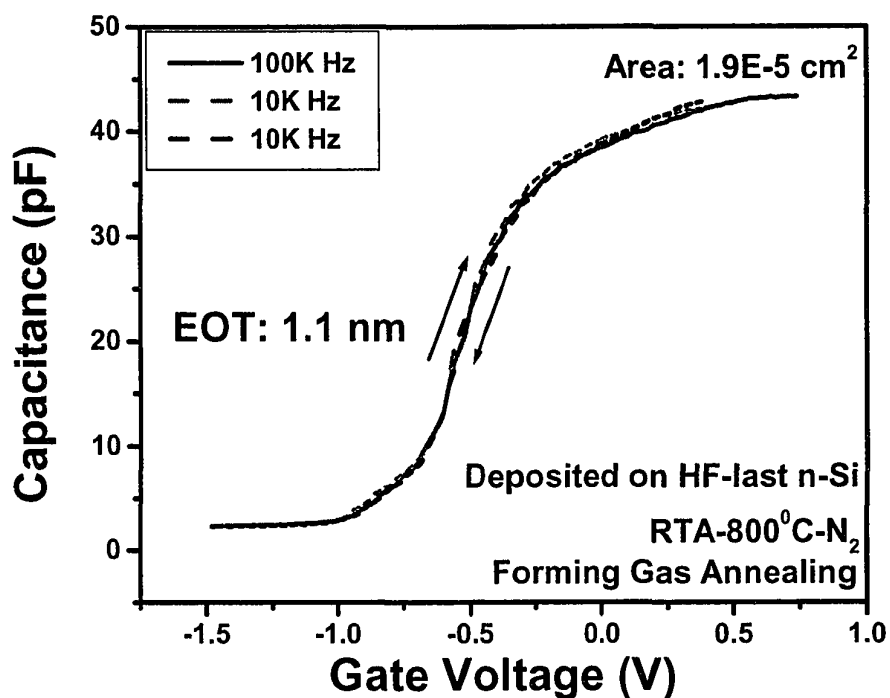


Figure 2.7 C-V Characteristics of a 1.1 nm JVD ZrO<sub>2</sub>/Zr silicate based MOS capacitor.

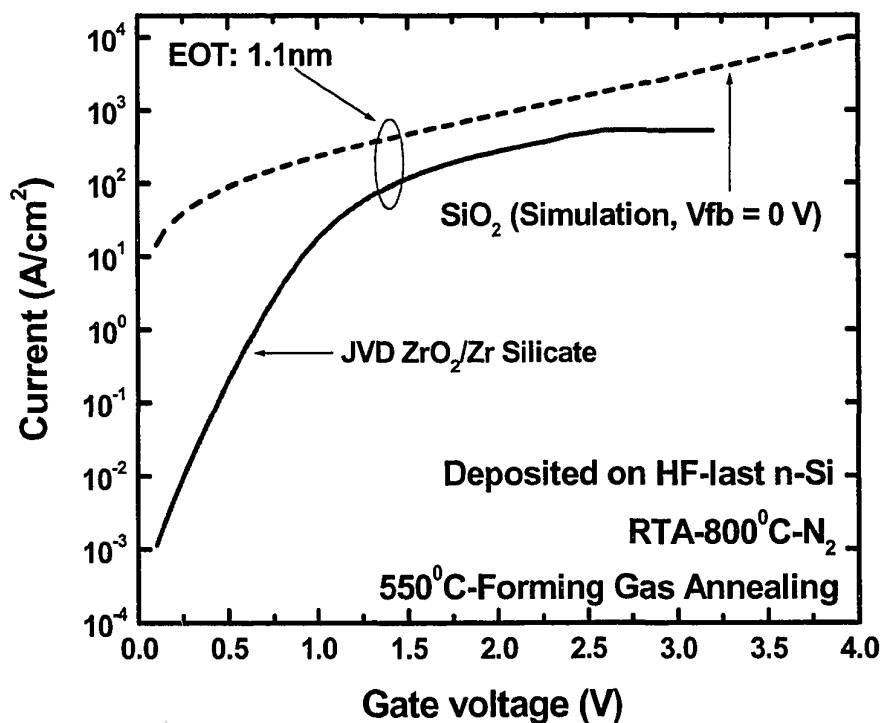


Figure 2.8 I-V Characteristics of a 1.1 nm JVD ZrO<sub>2</sub>/Zr silicate based MOS capacitor.

type silicon substrate to the gate. Because of the presence of the positive fixed charges, the flat-band voltage of this JVD  $\text{ZrO}_2/\text{Zr}$  silicate capacitor is shifted to the negative side, which means that for the same positive gate voltage it bears a larger electric field when compared to the thermal silicon dioxide without the flat-band voltage shift. However, even without correcting for the flat-band voltage difference, the current density of the JVD  $\text{ZrO}_2/\text{Zr}$  Silicate gate dielectric is at least 10x lower than that of thermal  $\text{SiO}_2$  for voltages below 1.2V, and the reduction is more significant at low electric fields. In Figure 2.9, the leakage current densities for JVD  $\text{ZrO}_2/\text{Zr}$  silicate gate dielectrics at various EOT values are compared to thermal silicon dioxide at a gate voltage of 1 V, showing reductions of at least one order of magnitude.

#### ***2.4.2 Properties of JVD $\text{ZrO}_2$ /Silicate Films after High Temperature Anneal***

How to reduce the EOT after high temperature annealing is a serious problem faced by high-k community. One interesting phenomenon that we have observed on JVD  $\text{ZrO}_2/\text{Zr}$  silicate gate dielectrics is that, in contrast to most other cases, the EOTs of our films are reduced significantly after annealing. C-V characteristics of a 1.5nm thick (EOT) JVD  $\text{ZrO}_2$ /silicate film before and after a  $\text{N}_2$  RTA at 1000  $^\circ\text{C}$  and a forming gas anneal at 550  $^\circ\text{C}$  are compared in Figure 2.10. The accumulation capacitance is inversely proportional to the EOT. The accumulation capacitance of this JVD  $\text{ZrO}_2$ /silicate film increases significantly after annealing, revealing a reduction of EOT. This change can be attributed to two factors: (1) the almost unchanged interfacial layer after high temperature annealing; (2) the elimination of excess oxygen or hydroxide group in the top layer of *as-deposited* films to make it more like stoichiometric  $\text{ZrO}_2$ . Moreover, the crystallization of

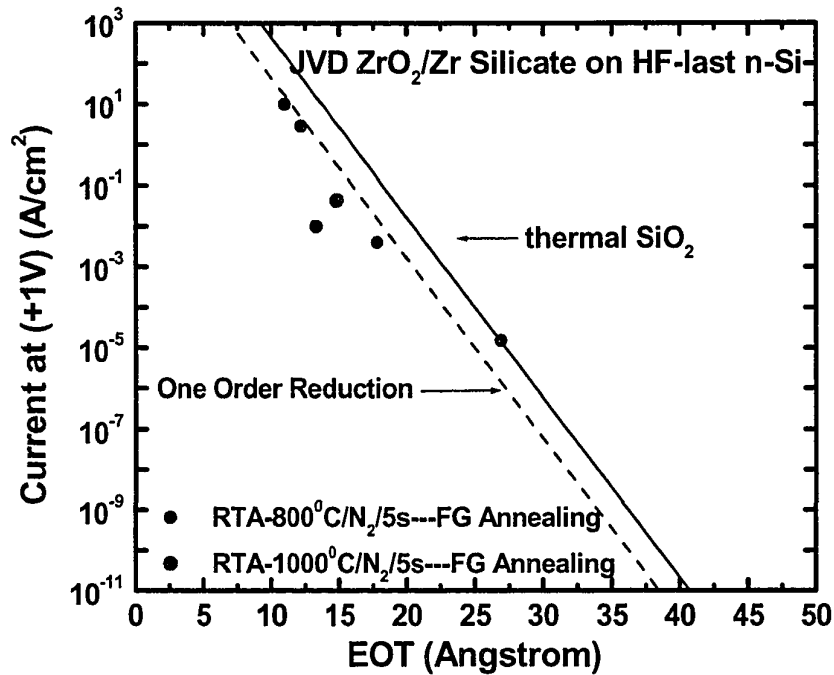


Figure 2.9 Leakage current comparison between JVDZrO<sub>2</sub>/Zr silicate and SiO<sub>2</sub> over a range of EOTs.

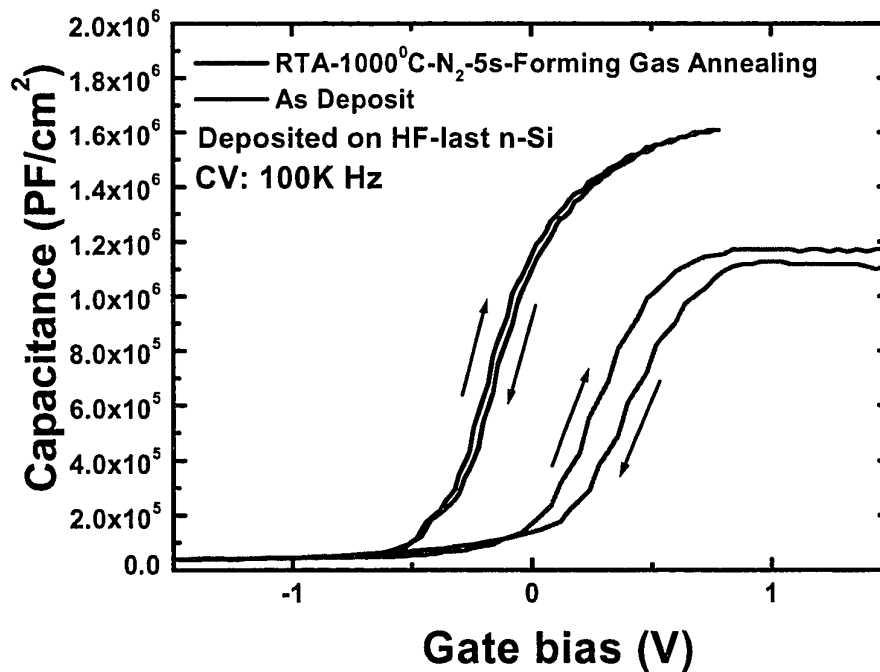


Figure 2.10 C-V curves of JVD ZrO<sub>2</sub>/Zr silicate based MOS capacitors reveal reduction of EOT after annealing.

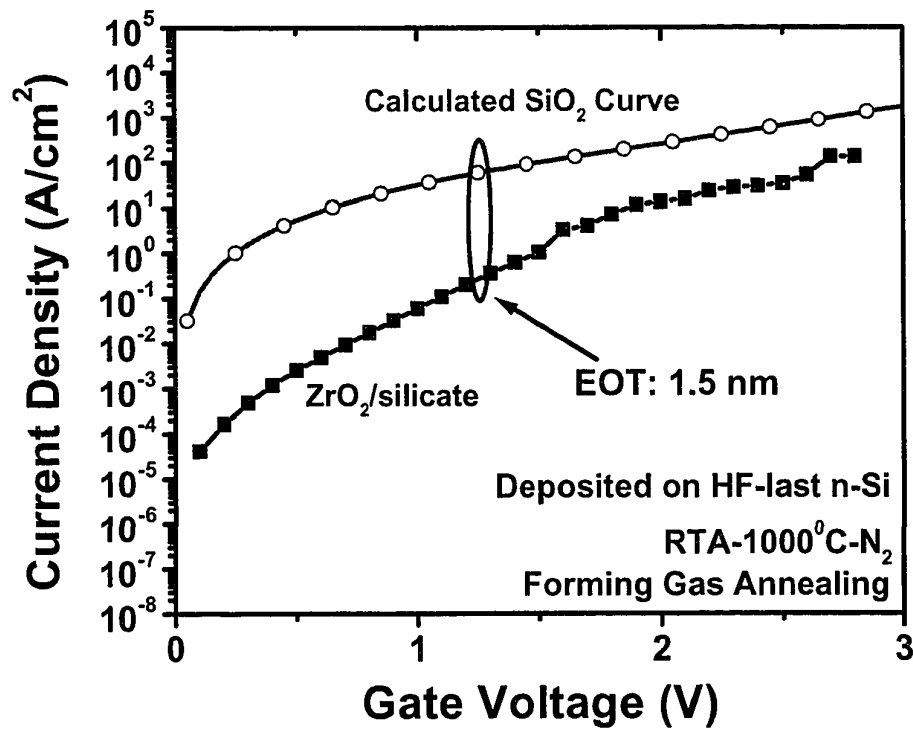


Figure 2.11 I-V characteristics of a JVD  $\text{ZrO}_2/\text{Zr}$  silicate based MOS capacitor after 1000 °C annealing compared to a calculated I-V curve of  $\text{SiO}_2$  with the same EOT.

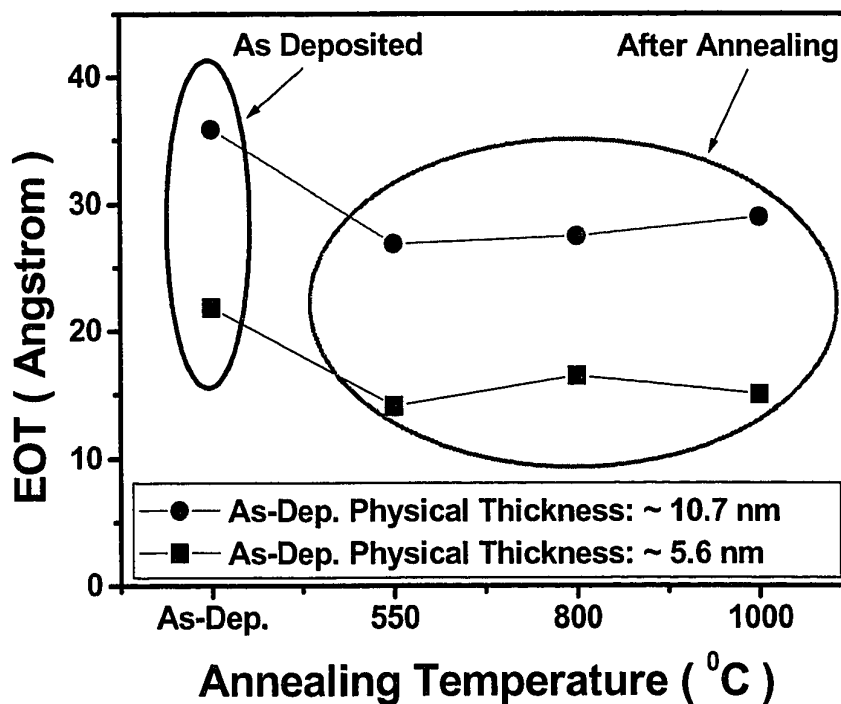


Figure 2.12 The EOTs of JVD  $\text{ZrO}_2/\text{Zr}$  silicate are reduced after annealing under various conditions.

the top layer after high temperature annealing may cause the dielectric constant to increase as well. The details of these changes will be explained in Section 2.3 in this chapter. Moreover, the good C-V curves also indicate the JVD ZrO<sub>2</sub>/silicate film possesses good dielectric properties after 1000 °C annealing. I-V characteristics also reveal a significant reduction of leakage current after 1000 °C annealing when compared to thermal silicon dioxide counterpart. The I-V curve measured under substrate injection of this 1.5 nm JVD ZrO<sub>2</sub>/silicate film after 1000 °C annealing is compared to a calculated I-V of a 1.5nm thermal silicon dioxide film in Figure 2.11. Just like the data in Figure 2.8, we have observed at least one order of magnitude reduction of leakage current for JVD ZrO<sub>2</sub>/silicate film when compared to silicon dioxide, and more reduction is observed at low electric fields. Both the C-V and I-V characteristics indicate that JVD ZrO<sub>2</sub>/silicate film possesses very promising electrical properties after high temperature annealing up to 1000 °C, which is very desirable for the conventional CMOS process.

The reduction of EOT is not only observed on the JVD ZrO<sub>2</sub>/silicate film after 1000 °C annealing, but also observed after annealing at other elevated temperatures. In Figure 2.12, the EOTs of two JVD ZrO<sub>2</sub>/silicate films before and after annealing at various temperatures: 550 °C, 800 °C, and 1000 °C are shown, and the reductions of EOT are observed for all annealed films.

### ***2.4.3 Reliability***

Constant-current stressing at high current and high electric field reveals the robustness and long-term reliability of a gate dielectric. Moreover, constant-current stressing is also useful to evaluate the bulk trapping properties of a gate dielectric. Bulk trapping is found responsible for the trap-assisted leakage current, shift of flat-band voltage, dielectric breakdown, and many other undesired properties. The results for some

JVD ZrO<sub>2</sub>/silicate films on both n-type and p-type silicon substrates under constant-current stressing at high currents and high electrical fields are shown in Figure 2.13. The JVD ZrO<sub>2</sub>/silicate film on p-type Si substrate is under gate injection, in which electrons transport from aluminum gate to the silicon substrate. For this 1.51 nm (EOT) thick JVD ZrO<sub>2</sub>/silicate film, the gate voltage shifted 26 mV after the constant-current stressing at 1A/cm<sup>2</sup> for 1,000 seconds. The 26 mV of the gate voltage shift corresponds to a trapped charge density of  $3.7 \times 10^{11} / \text{cm}^2$ . Correspondingly the 1.29nm (EOT) thick JVD ZrO<sub>2</sub>/silicate film on n-type Si substrate is under substrate injection. The voltage shift is 10 mV after 1000 seconds of the constant current stressing at 2 A/ cm<sup>2</sup>, corresponding to a trapped charge density of  $1.7 \times 10^{11} / \text{cm}^2$ . One thing needs to be pointed out is that, because for a ultra-thin gate dielectric, it is difficult to keep the carriers in the traps, the calculated trapped charge density from the C-V shift may underestimate the real trap density. However, the gate voltage shifts after long time high current stressing are sufficiently small, suggesting high dielectric strengths of JVD ZrO<sub>2</sub>/silicate films.

The breakdown statistics provides important information about the dielectric strength of a film, such as its intrinsic bonding strength, defect density, and process uniformity. A good breakdown statistics figure usually shows a tight distribution and high breakdown electric fields. Figure 2.14 presents the breakdown electric field distribution of a set of JVD ZrO<sub>2</sub>/silicate gate dielectrics. The device area is  $1.1 \times 10^{-4} \text{ cm}^2$  for every device used in this study. The EOTs of the n-type JVD ZrO<sub>2</sub>/silicate capacitors under gate injection and the p-type JVD ZrO<sub>2</sub>/silicate capacitors under substrate injection are 2.8 nm and 2.2 nm, respectively. For both polarities, the breakdown electric fields show tight distributions, suggesting high dielectric strength and good uniformity. Moreover, a 50% cumulative effective breakdown electric field is about 20 MV/cm for the 2.8 nm (EOT) JVD ZrO<sub>2</sub>/silicate film under gate injection, and about 17 MV/cm for the 2.2 nm (EOT) JVD

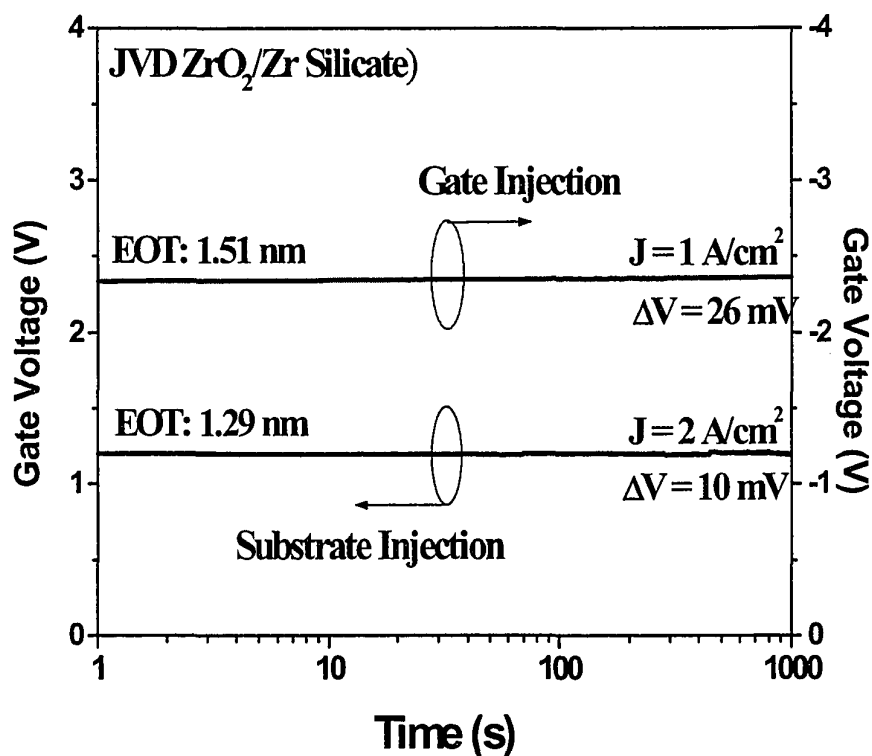


Figure 2.13 Constant-current stressing characteristics of JVD  $\text{ZrO}_2/\text{Zr}$  silicate based MOS capacitors.

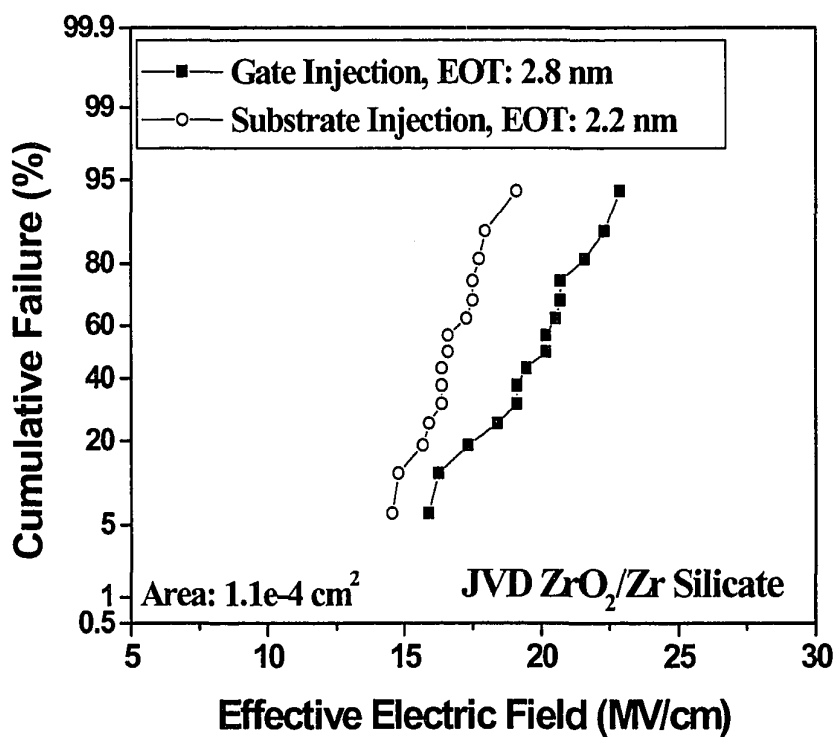


Figure 2.14 Breakdown field distributions of JVD  $\text{ZrO}_2/\text{Zr}$  silicate.

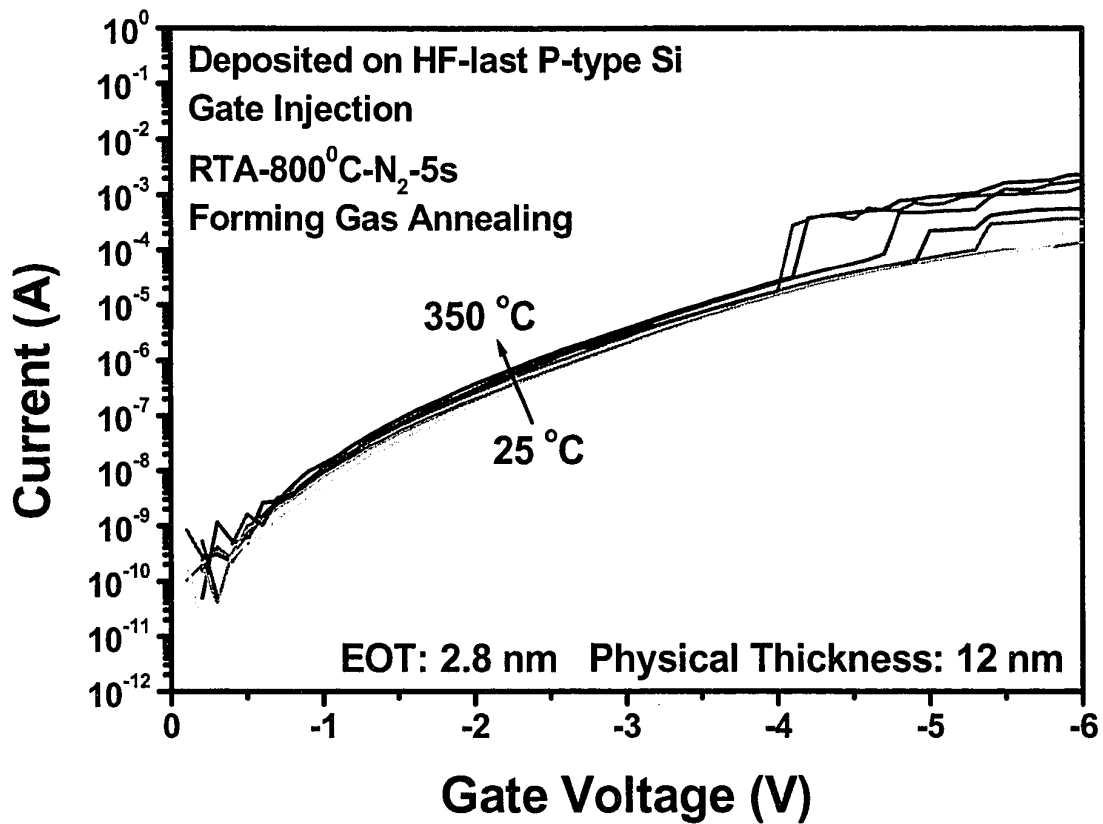


Figure 2.15 Temperature dependence of gate leakage currents for JVD ZrO<sub>2</sub>/Zr silicate based MOS capacitors.

**ZrO<sub>2</sub>/silicate film under substrate injection. The median effective breakdown electric fields are remarkable in both polarities.**

**The temperature dependence of I-V is another good indicator of dielectric properties. The tunneling current is independent of temperature or only weakly linked to temperature, but the trap-assisted leakage current is a strong function of temperature. Therefore, the weak temperature dependence of I-V suggests that tunneling is the dominant mechanism, and the trap-assisted mechanism only plays a minor role. Because electrons have more chances to encounter traps during transport through a thicker film, while the tunneling current is reduced due to the larger thickness, a thicker film is more suitable to evaluate the trap-assisted current. Thus, a relatively thick film, 12 nm of physical thickness, was used in this study. I-Vs of this JVD ZrO<sub>2</sub>/silicate gate dielectric under gate injection measured at various temperatures, from 25 °C to 350 °C, are shown in Figure 2.15. The weak temperature dependence indicates insignificant trap-assisted leakage currents, suggesting low bulk trap density of the JVD ZrO<sub>2</sub>/silicate gate dielectric. A high temperature environment is commonly used to accelerate the breakdown process of the gate dielectric. For the JVD ZrO<sub>2</sub>/silicate under gate injection, even at 350 °C, the breakdown electrical field is still above 10 MV/cm, again suggesting a robust gate dielectric.**

#### ***2.4.4 Film Morphology***

**In order to achieve high uniformity of device properties across the wafer, an amorphous phase or a single crystalline phase of a high-k gate dielectric is required. Because of the differences in grain orientations and grain boundaries across the wafer, the poly-crystalline phase causes serious concerns. X-ray Diffraction (XRD) is an economical and capable method to evaluate the morphology of a high-k film. In order to achieve sufficiently strong signal, a 100 nm thick JVD ZrO<sub>2</sub>/silicate film was employed in the XRD**

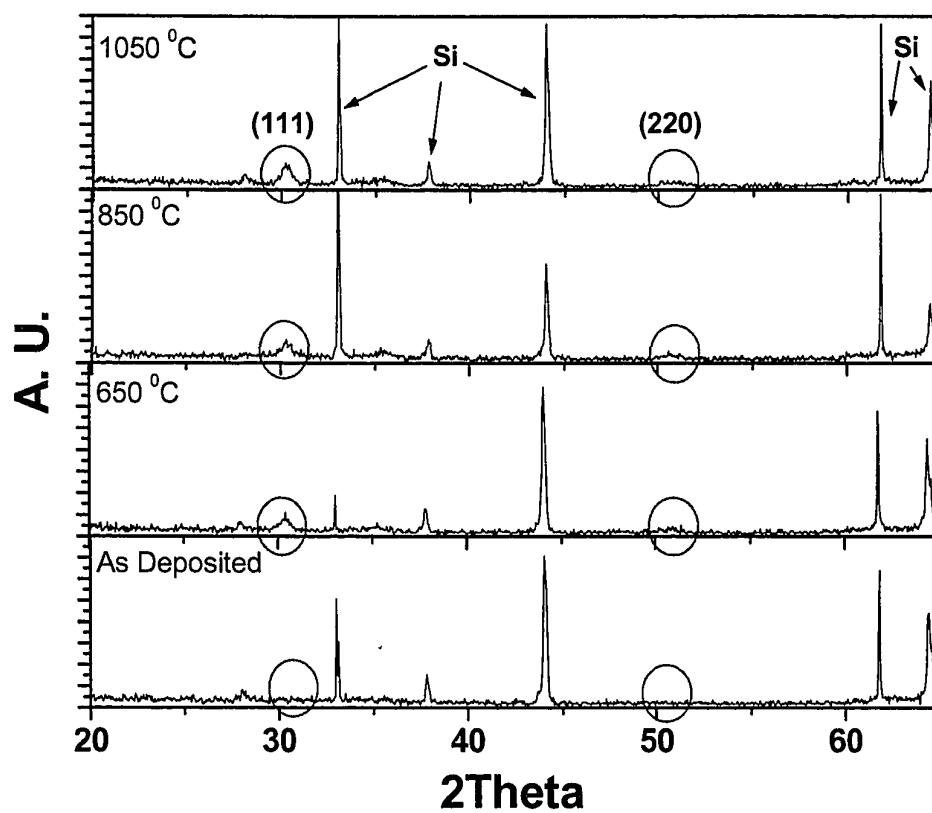


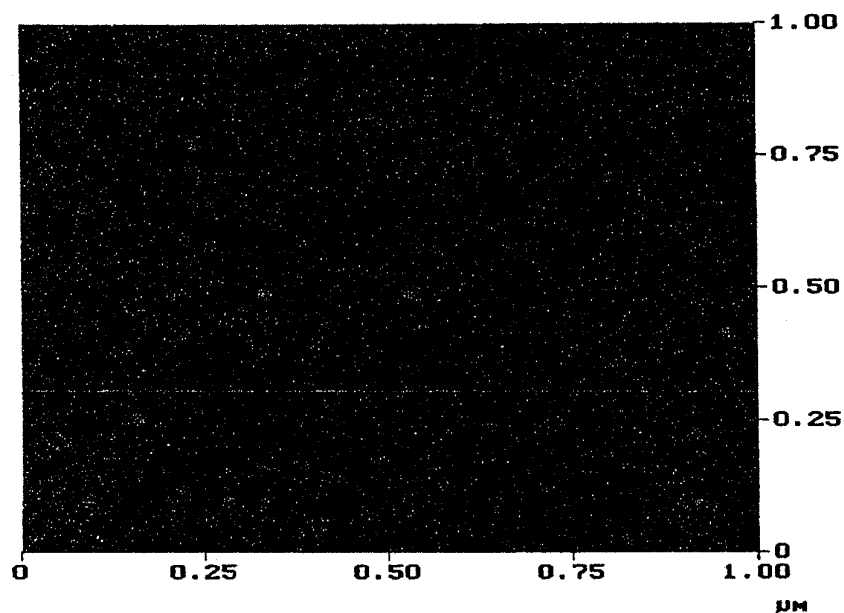
Figure 2.16 X-ray Diffraction (XRD) results show JVD  $\text{ZrO}_2/\text{Zr}$  silicate crystallized after annealing at 650 °C and above.

measurement. Unlike ALD or CVD deposited films, apparently the JVD  $\text{ZrO}_2/\text{silicate}$  is amorphous after the deposition, according to the XRD results presented in Figure 2.16, which is confirmed by Transmission Electron Microscope (TEM) image. However, after annealing at 650 °C and above, the (111) and (220) peaks of the tetragonal crystalline structure of  $\text{ZrO}_2$  appear on the XRD patterns, suggesting the JVD  $\text{ZrO}_2/\text{silicate}$  film is crystallized or partially crystallized. The formation of the polycrystalline phase may be a drawback of the JVD  $\text{ZrO}_2/\text{silicate}$  film.

Usually, as a consequence of the crystallization, the surface of a thin film becomes rough, which can cause serious uniformity problems. By measuring the forces at the atomic level between a sharp probing tip and a sample surface when the tip moves across the sample, Atomic Force Microscope (AFM) is able to take the images of surfaces of various materials in a non-contact mode. The bending of the cantilever holding the sharp probing tip in response to the force between the tip and the sample gives an accurate measure of the force. Very smooth surfaces were observed on the JVD  $\text{ZrO}_2/\text{silicate}$  films before and after 5 seconds of annealing in  $\text{N}_2$  at 1000 °C, as shown in Figure 2.17(a) and (b). The RMS roughness of this JVD  $\text{ZrO}_2/\text{silicate}$  film is 0.12 nm and 0.13 nm before and after annealing, respectively, suggesting the crystallization of the JVD  $\text{ZrO}_2/\text{silicate}$  film does not result in a degradation of surface uniformity.

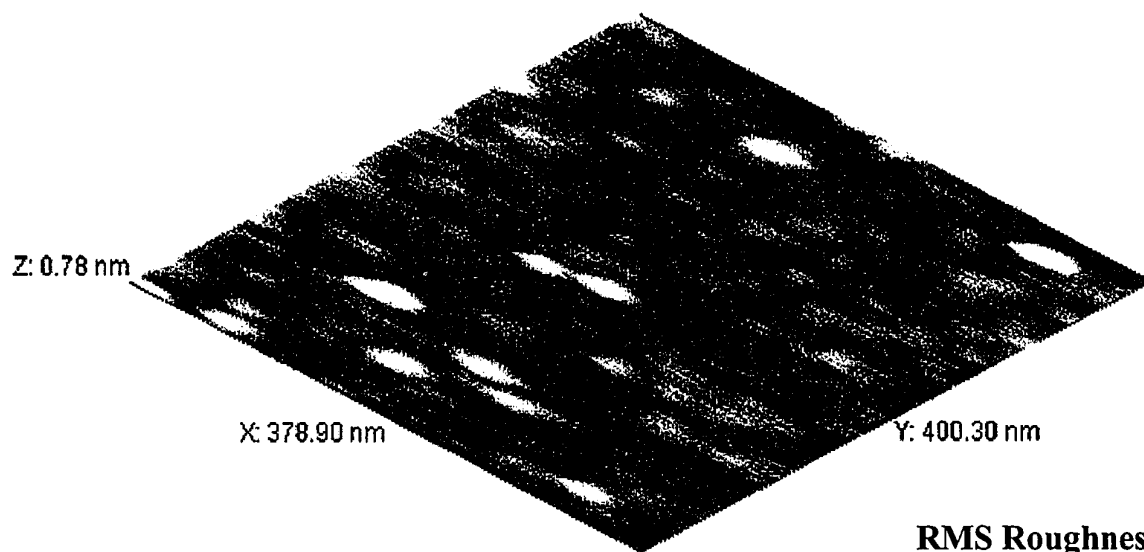
#### ***2.4.5 Dielectric Constant***

Figure 2.18 provides important information of the interfacial layers and dielectric constants of JVD  $\text{ZrO}_2/\text{Zr}$  silicates. From the slopes of the curves in these EOT vs physical thickness plots, we can get the dielectric constants of the films. Each EOT was extracted from C-V method after considering the quantum confinement effect, and each physical thickness was measured by ellipsometry. The JVD  $\text{ZrO}_2/\text{Zr}$  silicate appears to have graded



(a)

**RMS Roughness: 0.12 nm**



(b)

**RMS Roughness: 0.13 nm**

Figure 2.17 Very smooth surfaces of a 3 nm (physical thickness) JVD  $\text{ZrO}_2/\text{Zr}$  silicate film observed by AFM (a) before and (b) after a 1000 °C anneal.

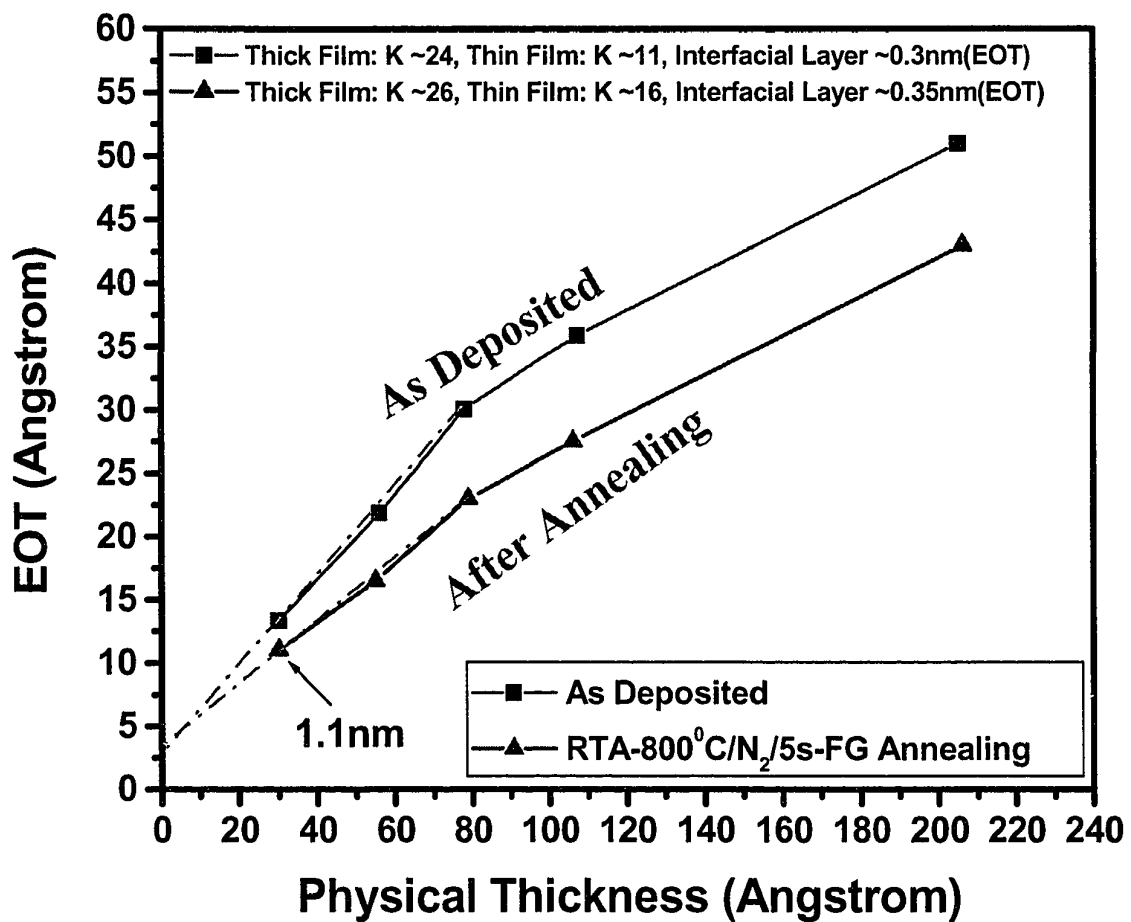


Figure 2.18 The EOT vs Physical Thickness plot for JVD ZrO<sub>2</sub>/Zr silicate provides information of dielectric constant and interfacial layer.

composition. For a relatively thin film, it is more Zr-silicate-like, with a dielectric constant about 11 for the as-deposited film, and a dielectric constant about 16 for the film annealed in N<sub>2</sub> at 800 °C for 5 seconds and in forming gas at 550 °C. And the top layers of a relatively thick film are more ZrO<sub>2</sub>-like with a dielectric constant about 24 for the as-deposited film, and a dielectric constant about 26 for the annealed film. If we assume that the interfacial layer is caused and self-limited by the dynamic reaction between ZrO<sub>2</sub> and Si during deposition, and unrelated to the total film thickness, then the intercepts of the linear fitting lines of the data on the EOT axis provide the interfacial layer thicknesses. The interfacial layer thickness appears very stable -- the extrapolated thickness is about 0.3nm and 0.35 nm in EOT before and after annealing, respectively. The results are consistent with XPS and High Resolution TEM (HRTEM). The very similar values of the extrapolated interfacial layer thickness before and after annealing indicate the high thermal stability of the interfacial layer, which we will discuss in detail in the next section.

## ***2.4.6 MOSFET Characteristics***

For any high-k gate dielectric, the transistor performance is the most important assessment. Because of the limitation of the process facilities at Yale University, only MOSFETs with channel lengths larger than 5 μm can be fabricated. Such a long channel MOSFET has a small drive current to gate leakage current ratio; thus, relatively thick JVD ZrO<sub>2</sub>/Zr silicate gate dielectrics were used in order to obtain working transistors. Both n-channel MOSFETs and p-channel MOSFETs using ultra-thin JVD ZrO<sub>2</sub>/Zr silicate as the gate dielectric were successfully fabricated, and demonstrated good transistor characteristics. Aluminum was thermally evaporated to form the electrodes and back contacts. The gate dielectrics of both n-channel and p-channel MOSFETs shown here received a 600°C/O<sub>2</sub>/5s post-deposition anneal.

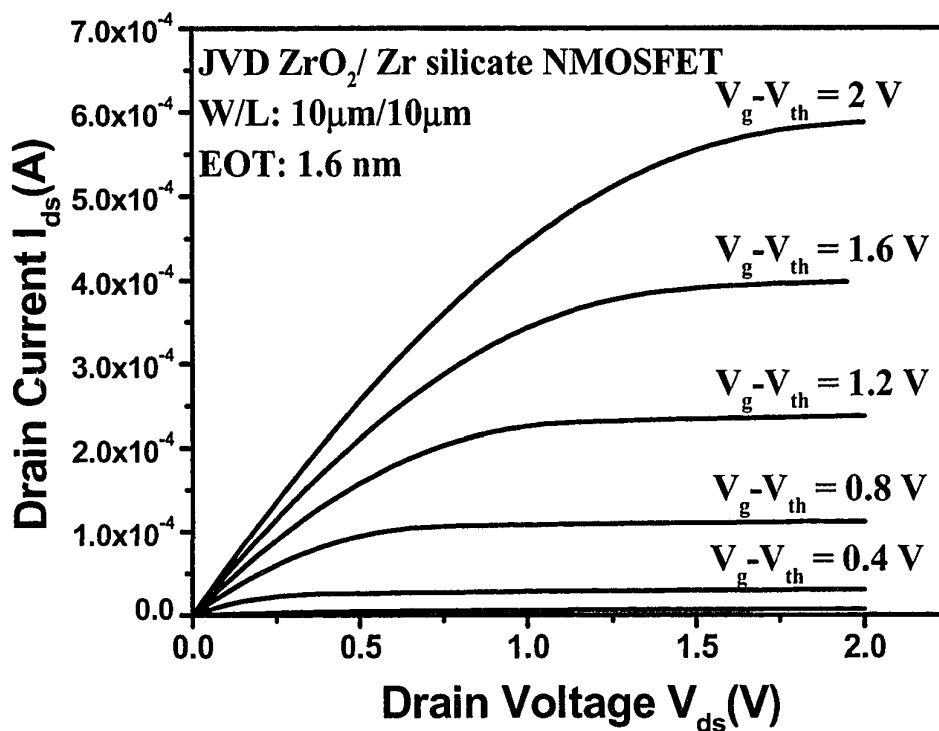


Figure 2.19 Output characteristics of an n-channel MOSFET with JVD  $\text{ZrO}_2/\text{Zr}$  silicate gate dielectric.

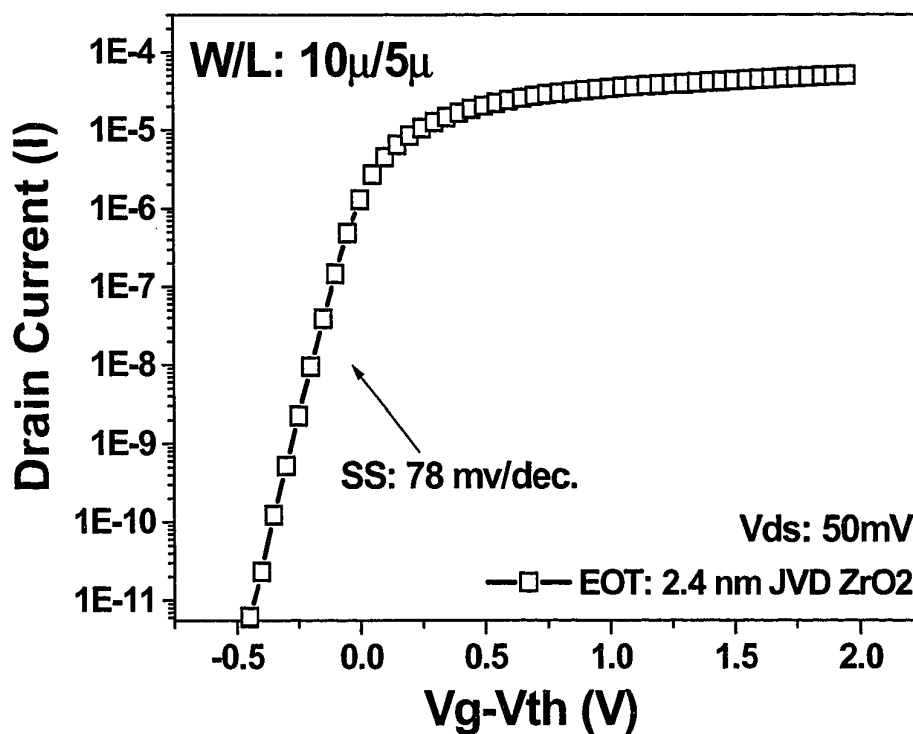


Figure 2.20 Subthreshold characteristic of an n-channel MOSFET with JVD  $\text{ZrO}_2/\text{Zr}$  silicate gate dielectric.

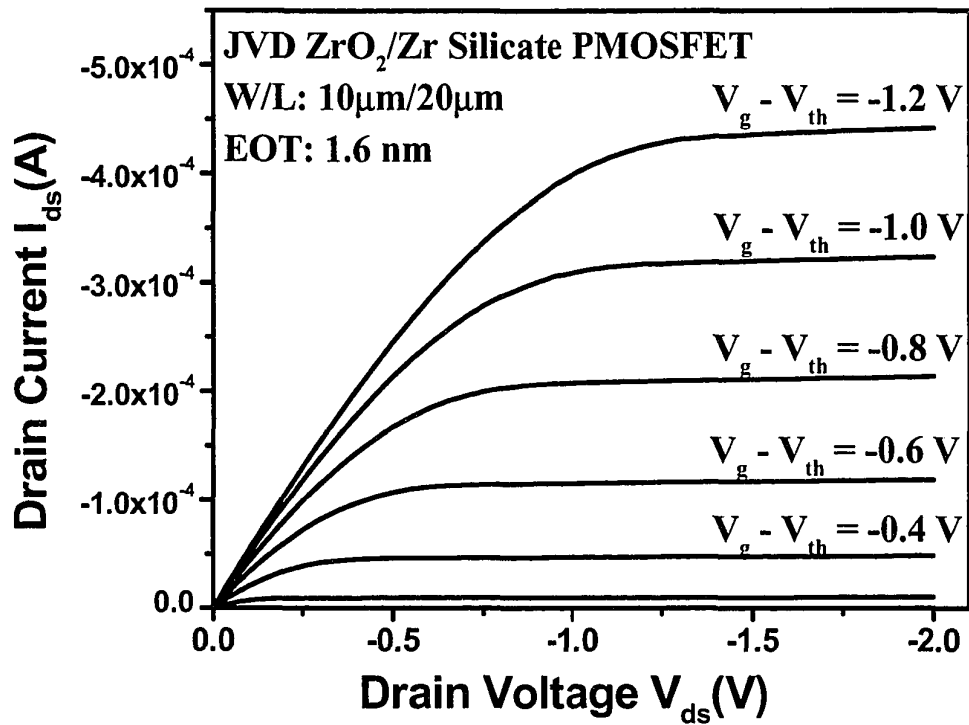


Figure 2.21 Output characteristics of a p-channel MOSFET with JVD  $\text{ZrO}_2/\text{Zr}$  silicate gat dielectric.

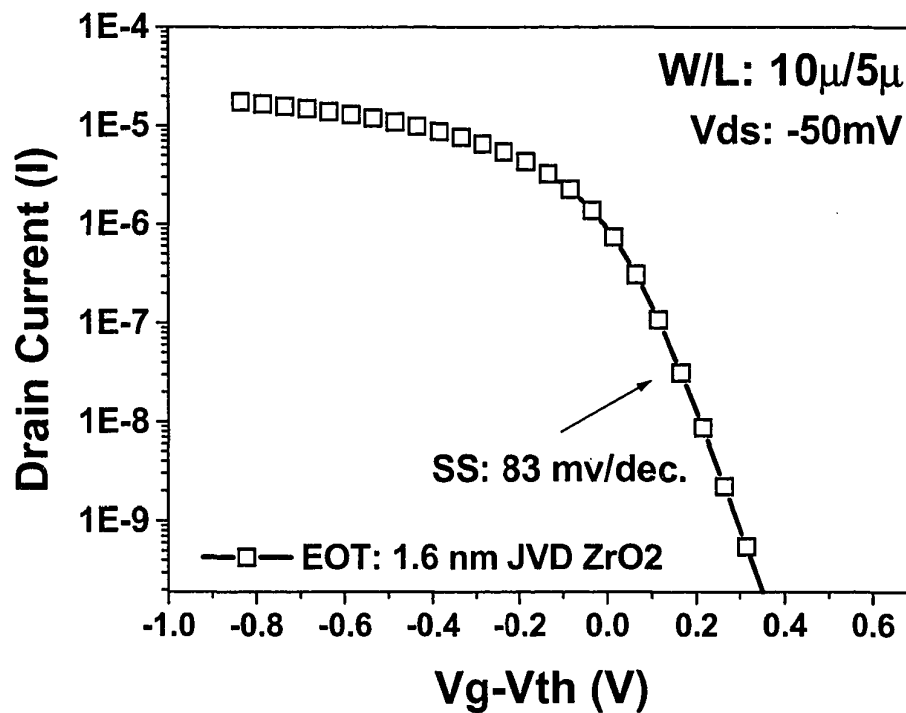


Figure 2.22 Subthreshold characteristic of a p-channel MOSFET with JVD  $\text{ZrO}_2/\text{Zr}$  silicate gate dielectric.

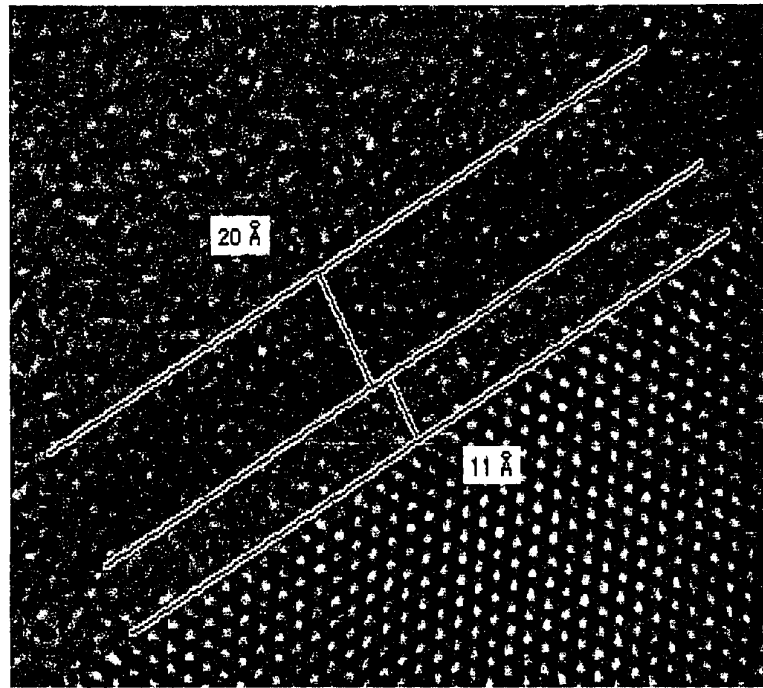
Figure 2.19 presents the  $I_d$ - $V_d$  characteristics for a JVD  $\text{ZrO}_2$ /silicate NMOSFET. The EOT of this JVD  $\text{ZrO}_2$ /silicate gate dielectric is about 1.6 nm. The transistor with 10  $\mu\text{m}$  long channel shows well-behaved output characteristics. Figure 2.20 shows the  $I_d$ - $V_g$  characteristics of a 2.4 nm (EOT) JVD  $\text{ZrO}_2$ /Silicate NMOSFET at a drain bias voltage of 50 mV. The channel length and width for this MOSFET are 5  $\mu\text{m}$  and 10  $\mu\text{m}$ , respectively. The deep subthreshold swing of 78 mV/dec indicates good switching characteristics with a high on/off current ratio. Figures 2.21 and 2.22 reveal the  $I_d$ - $V_d$  and  $I_d$ - $V_g$  characteristics of p-channel MOSFETs with 1.6 nm (EOT) JVD  $\text{ZrO}_2$ /silicate gate dielectrics. The devices show good output characteristics and good switching property with an 83 mV/dec subthreshold swing.

## 2.5 A Thermally Stable Interfacial Layer Between JVD $\text{ZrO}_2$ and Si

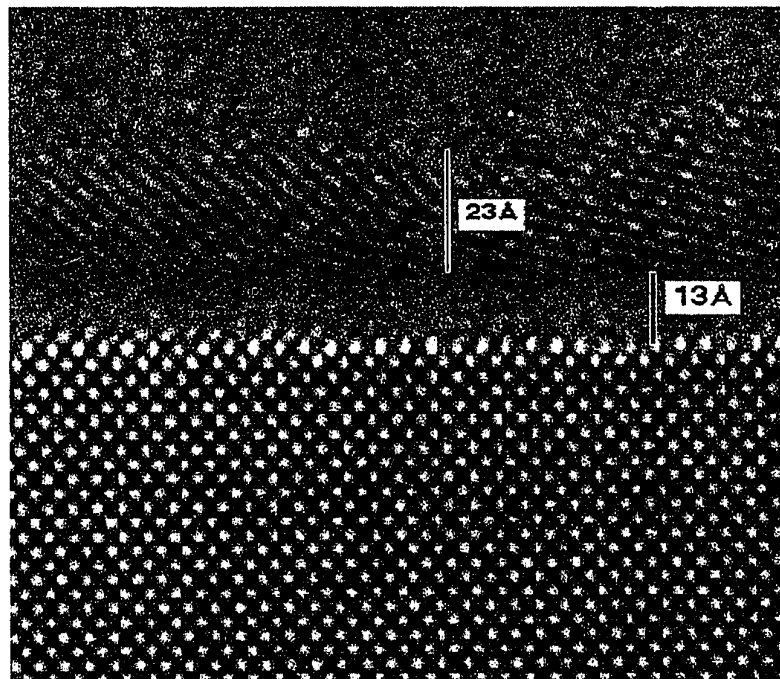
Other studies have shown that after high temperature annealing, the thickness of the interfacial layer between  $\text{ZrO}_2$  and Si increases dramatically<sup>2</sup>, the composition of the interfacial layer changes from Zr-silicate-like to  $\text{SiO}_2$ -like, and moreover, under certain process conditions, Zr silicide can be formed<sup>16</sup>. Furthermore, in ALD, a  $\text{SiO}_2$  layer at the interface is necessary to grow high quality  $\text{ZrO}_2$  smoothly. However, from our study, we found that  $\text{ZrO}_2$  deposited by the JVD process can grow smoothly directly on HF-last silicon, and it possesses remarkable thermal stability—withstanding anneals as high as 1000  $^\circ\text{C}$  without formation of silicide and silicon dioxide. The interfacial layer has been found to be Zr silicate like, and the presence of a thermally stable Zr silicate interfacial layer may prevent the formation of interfacial  $\text{SiO}_2$  despite the fact that *as-deposited* films have been found to be oxygen rich.

First, we shall examine the JVD  $\text{ZrO}_2$  before and after 1000 °C anneals through cross-sectional HRTEM. In Figure 2.23(a), the cross-sectional HRTEM image of one as-deposited JVD  $\text{ZrO}_2$  film shows that the dielectric possesses a two-layer amorphous structure with an interfacial layer about 1.1nm. From Figure 2.18, the extracted interfacial layer thickness is about 0.3nm in EOT, thus the bottom layer has a dielectric constant more than three times of that of silicon dioxide, suggesting that the bottom layer is not silicon dioxide, and likely to be Zr silicate. Both the interfacial layer and the top layer are very smooth. Another cross-sectional HRTEM image of the JVD  $\text{ZrO}_2$  after 1000 °C annealing is shown in Fig. 2.23(b). The top layer of the film is crystallized after such a high temperature anneal, and we have known from XRD measurements that crystallization can happen for annealing temperatures above 650 °C. But the interfacial layer was apparently unchanged after annealing: the interfacial layer stays amorphous and remains very smooth; there is no evidence of the formation of silicide; and apparently its thickness remains almost identical--only increases a couple of Angstroms, which is within the resolution limit of cross-sectional HRTEM.

Moreover, the thermally stable interfacial layer has been confirmed by other characterization tools. By detecting the energies of photoelectrons that are emitted from atoms when they are irradiated by soft X-ray photons in the 1 - 2 keV range, X-ray photoelectron spectroscopy (XPS) is a powerful analytical technique for solid thin films. Figure 2.24 presents the Si 2p spectrum of XPS before and after annealing. The bonding energy difference between the S-O bond and Si-Si bond in Si 2p spectrum is about 3.1 eV, which is about 1 eV smaller than the difference between the S-O bond and Si-Si bond in  $\text{SiO}_2$ , which again indicates the interfacial layer is Zr-silicate-like. Furthermore, the results from the angle-resolved XPS reveal that the Zr-O bonds are distributed through the whole film thickness, which further confirms the interfacial layer is Zr silicate. One striking feature of this Si 2p XPS spectrum is that the spectrum remains unchanged after 30 minutes

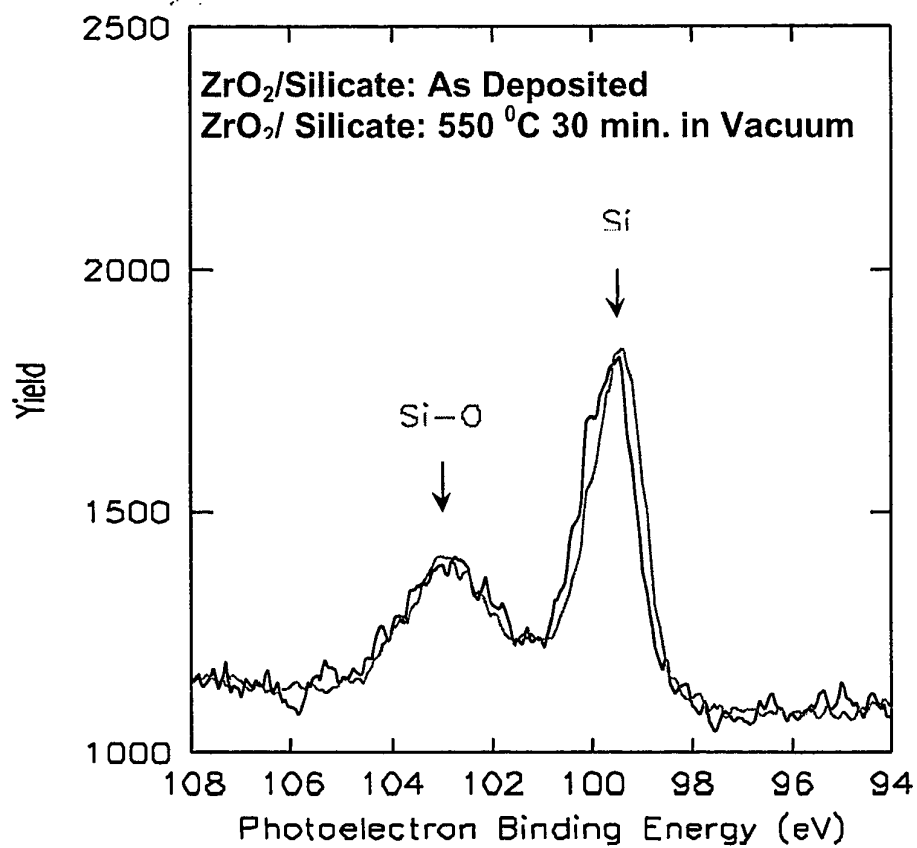


(a)



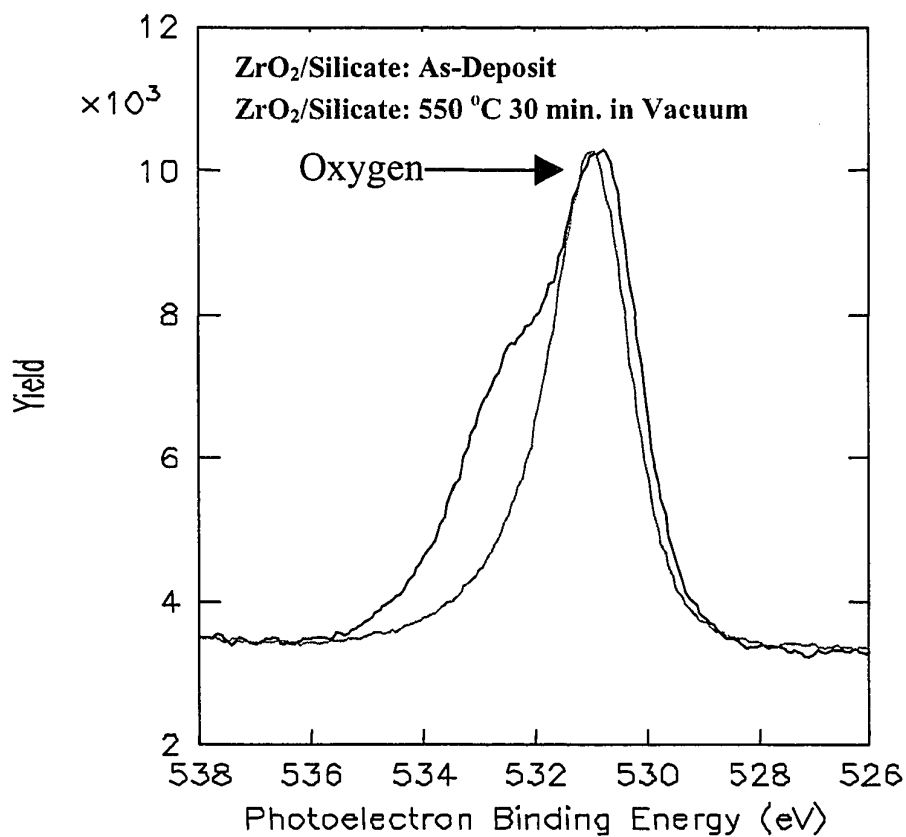
(b)

Figure 2.23 TEM Images of (a) as-deposited and (b) after 1000°C annealed JVD  $\text{ZrO}_2/\text{Zr}$  silicate Films.



## *Si 2p Spectrum*

Figure 2.24 Si 2p XPS Spectra of JVD ZrO<sub>2</sub>/Zr silicate are partially unchanged after long-time annealing in vacuum.



## *Oxygen 1s Spectrum*

Figure 2.25 Oxygen 1s XPS spectra of JVD ZrO<sub>2</sub>/Zr silicate changed dramatically after long-time annealing in vacuum.

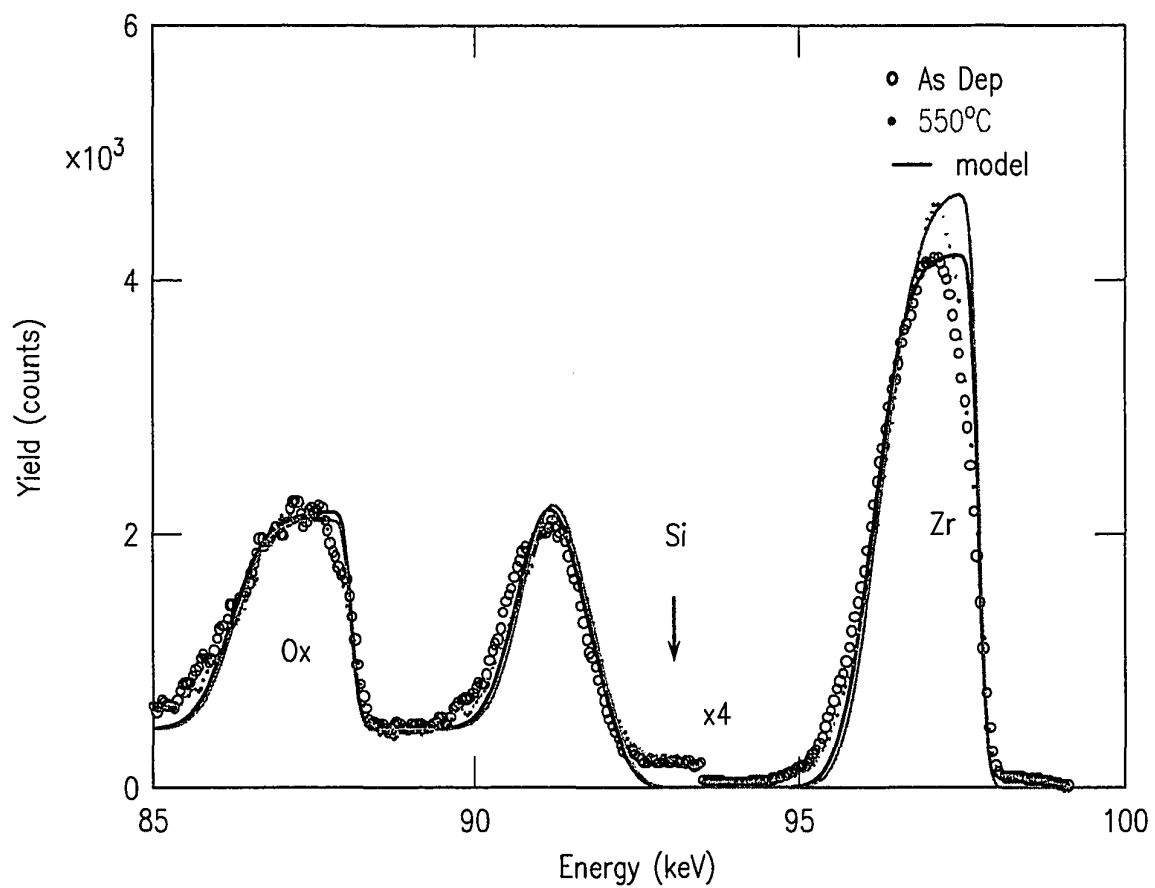


Figure 2.26 MEIS spectrum suggests reduced oxygen concentration upon annealing.

annealing at 550 °C, indicating that the interfacial layer between Si and ZrO<sub>2</sub> is stable during such an anneal as well. While the Si 2p spectrum remains the same, the O 1s spectrum changed dramatically during the anneal. Clearly there is a significant amount of oxygen loss in the film that occurs already at 550 °C, as can be seen by the O 1s spectrum in Fig. 2.25. The spectrum reveals two oxygen bonding states before annealing, where as a single bond energy is observed after annealing.

Medium Energy Ion Scattering (MEIS) based on the principle of Rutherford backscattering spectroscopy (RBS) is another powerful tool for thin film analysis. Because of the relatively low ion energy used in MEIS (typically 100 keV), and the usage of a high-resolution toroidal electrostatic ion energy analyzer<sup>114</sup>, almost-monolayer depth resolution can be obtained<sup>115,116</sup>. The data from MEIS, as shown in Figure 2.26, show JVD ZrO<sub>2</sub>/silicate is oxygen rich. And a reduction from Zr:O-ratio of 1:2.5 to 1:2.2 after annealing can be derived.

The formation of the thermally stable Zr Silicate layer and the oxygen rich feature of JVD ZrO<sub>2</sub>/Zr silicate may be attributed to a few unique characteristics of JVD. As we discussed at the beginning of this chapter, unlike the ALD, CVD, or sputtering, in JVD all Zr atoms and all oxygen molecules or atoms are moving in the same direction in their own jets, and basically collision free. The independence of the jets ensures that the oxidization of Zr metal only happens at the Si substrate surface, and no reaction happens during transportation. Moreover, under our deposition conditions, instead of clusters, only single Zr atoms are deposited. And most important, the sub-monolayer deposition feature of JVD enables the uniform reaction of Zr, oxygen, and the exposed silicon surface, thus it results in a uniform and dense interfacial layer. After the formation of the interfacial layer, the sub-monolayer deposition enables sufficient oxidation of Zr metal, which results in an oxygen rich film.

A  $\text{ZrO}_2$  film deposited by CVD or ALD shows the formation of Zr Silicide ( $\text{ZrSi}$ ) after annealing in oxygen-free environment<sup>117,118</sup>, and the oxygen vacancies and the lack of oxygen in the environment is believed to be the cause of the formation of  $\text{ZrSi}$ . In contrast, the oxygen rich nature of the JVD  $\text{ZrO}_2$ /silicate film prevents the formation of Zr silicide during long-time vacuum annealing. Moreover,  $\text{ZrSiO}_4$  is stable on Si, and positive Gibbs energy is necessary for  $\text{ZrSiO}_4$  to react with Si to form  $\text{SiO}_2$ ,  $\text{SiO}$ ,  $\text{ZrSi}$  or  $\text{ZrO}_2$  at elevated temperatures. Furthermore, the oxygen diffusion rate is much lower in  $\text{ZrSiO}_4$  than in  $\text{ZrO}_2$ <sup>113</sup>. Therefore, the presence of a high quality Zr silicate interfacial layer may prevent the diffusion of oxygen despite the fact that *as-deposited* films are found to be oxygen rich.

These results reveal that the presence of a high quality Zr silicate interfacial layer, which can be attributed to the unique JVD method, may prevent the formation of interfacial  $\text{SiO}_2$  up to 1000 °C, despite the fact that *as-deposited* films are found to be oxygen rich, which is very desirable in a conventional CMOS process.

## 2.6 $\text{ZrO}_2$ with Different Gate Electrodes

We have discussed the interface between  $\text{ZrO}_2$  and Si, and now let us discuss another important interface, the interface between  $\text{ZrO}_2$  and gate electrodes. Because of the additional 0.4 nm of EOT brought by the polysilicon depletion effect, metal gates have to be implemented together with high-k gate dielectrics as the final solution of the gate stack. As predicted in the ITRS 2002 update<sup>15</sup>, metal gates will be required by 2007 to eliminate the polysilicon depletion effect. In order to successfully implement high-k gate dielectrics and metal gates, two issues must be addressed. First, the combination of the high-k gate dielectric and its corresponding metal gate should have the right work function

value. Because of the dipole formed at the high-k gate dielectric and metal gate interface or the presence of a transition layer between high-k gate dielectric and metal gate, the effective work function of metal gate is different from the work function measured in vacuum, and it may be changed when it is subjected to the subsequent process conditions. Second, the formation of a transition layer between the high-k gate dielectric and metal gate during deposition and subsequent annealing may add unwanted EOT to the total EOT of the device, which compromises the effort of using metal gates to minimize the extra EOT caused by the polysilicon depletion.

Aluminum and platinum are two metals used often as the gate electrodes for high-k gate dielectrics during the course of this dissertation study, and indeed, they show different behaviors when deposited on top of  $\text{ZrO}_2$ . In order to focus the study on the effect of the interface between  $\text{ZrO}_2$  and aluminum, and  $\text{ZrO}_2$  and platinum, we should minimize the influence from another interface, the interface between Si and  $\text{ZrO}_2$ . Therefore, a high quality silicon oxynitride layer was used to ensure an excellent interface with the silicon substrate. An 8 nm (physical thickness) thick  $\text{ZrO}_2$  was deposited by CVD on top of a 1.5 nm (physical thickness) thick silicon oxynitride on n-type Si substrate. The aluminum gate was thermally evaporated, and the platinum gate was deposited by electron-beam deposition. No PMA was performed on these devices. As shown in Figure 2.27, the accumulation capacitance of the capacitor using platinum gate is higher than that of the capacitor using aluminum gate, despite the fact that both capacitors are supposed to have the identical gate dielectric. The EOT of the device using aluminum gate is about 0.6 nm thicker than that of the device using platinum gate, which is even more than the 0.4 nm extra EOT one would have gotten from the polysilicon depletion effect. This additional EOT may be caused by a transition layer between  $\text{ZrO}_2$  and aluminum, or a reduced effective dielectric constant of the gate dielectric caused by aluminum diffusion during

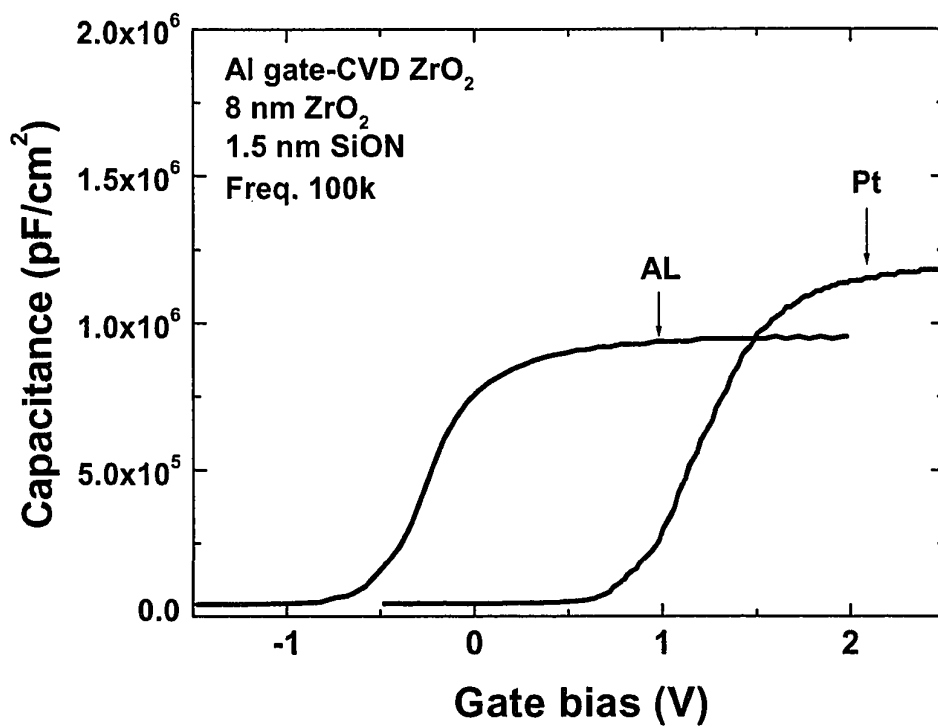


Figure 2.27 C-V characteristics of n-type  $\text{ZrO}_2$  MOS capacitors using Al and Pt as the gate electrodes.

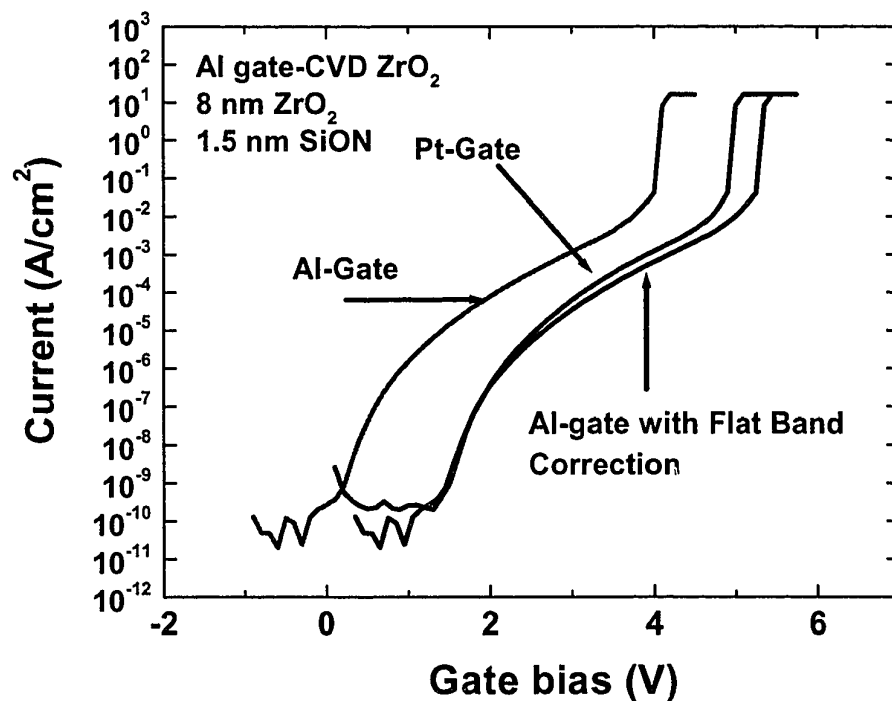


Figure 2.28 I-V characteristics of n-type  $\text{ZrO}_2$  MOS capacitors using Al and Pt as the gate electrodes.

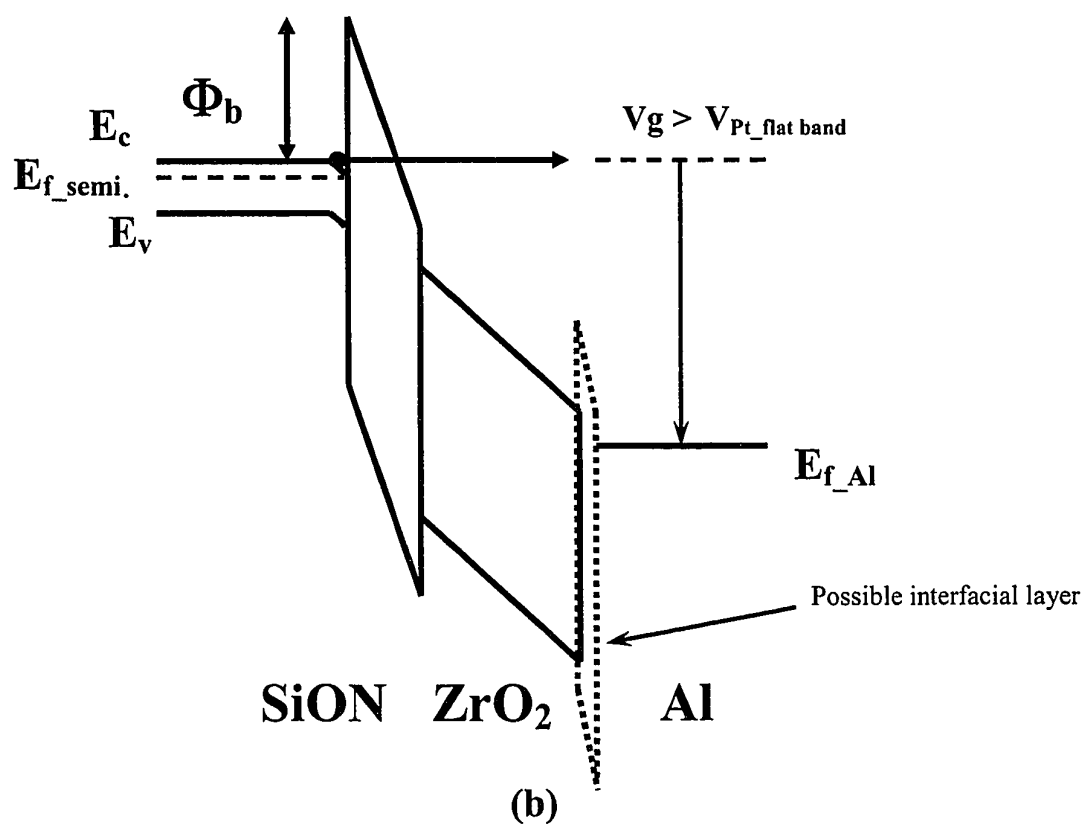
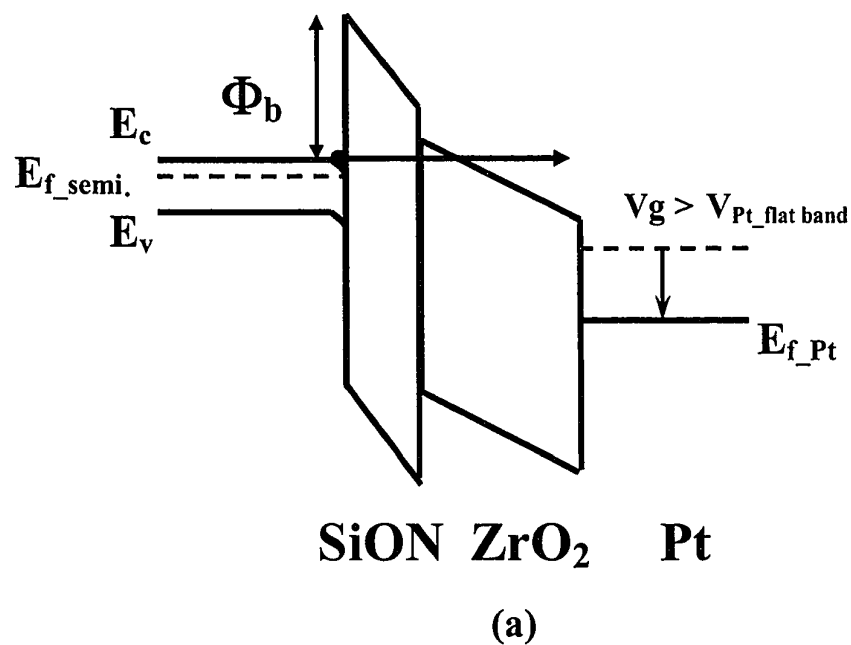


Figure 2.29 In substrate injection, electrons in MOS capacitors using either Pt gate or Al gate face same barrier height, though due to the work function difference between Pt and Al, the applied electric fields are different.

deposition. The result clearly shows that, if a metal gate is chosen improperly, it may add an even larger extra EOT than one would expect from polysilicon depletion. However, it seems the extra thickness of the capacitor using aluminum gate does not bring the benefit of reduced gate leakage current.

The work function difference between  $\text{ZrO}_2$ /aluminum and  $\text{ZrO}_2$ /platinum can be derived from the flat-band voltage shifts observed from C-V curves. After shifting the I-V curve of the  $\text{ZrO}_2$ /Aluminum capacitor by the derived work function difference from C-V, the I-V curve of the  $\text{ZrO}_2$ /Aluminum capacitor aligns almost perfectly with the I-V curve of the  $\text{ZrO}_2$ /platinum capacitor, especially in the low electric field region (Figure 2.28). This may be explained by the substrate injection mode for both capacitors. Because both n-type capacitors are under substrate injection, as illustrated in Figure 2.29, the incoming electrons face the same barrier height at the interface, and the same interfacial and bulk layers. In substrate injection mode, the possible transition layer between  $\text{ZrO}_2$  and aluminum has little influence on electron transport, as it only causes marginal reduction of the gate leakage current in the high electric field region.

The EOT derived from the p-type  $\text{ZrO}_2$ /aluminum capacitor reveals a larger EOT than that of the p-type  $\text{ZrO}_2$ /platinum capacitor as well, as shown in Figure 2.30. A 6 nm (physical thickness) thick  $\text{ZrO}_2$  was deposited by CVD on top of a 1.9 nm (physical thickness) thick silicon oxynitride on p-type Si substrate. The p-type capacitor is under gate injection. In gate injection, the incoming electrons are facing different barrier heights and different interface layers at the  $\text{ZrO}_2$ /aluminum or the  $\text{ZrO}_2$ /platinum interface, as presented in Figure 2.32. Therefore, they show drastically different current transport behavior (Figure 2.31). The applied electric field in the aluminum-gate capacitor is smaller than that in the platinum-gate capacitor at the same gate voltage under gate injection. However, the leakage current is larger in the aluminum-gate capacitor than that in the

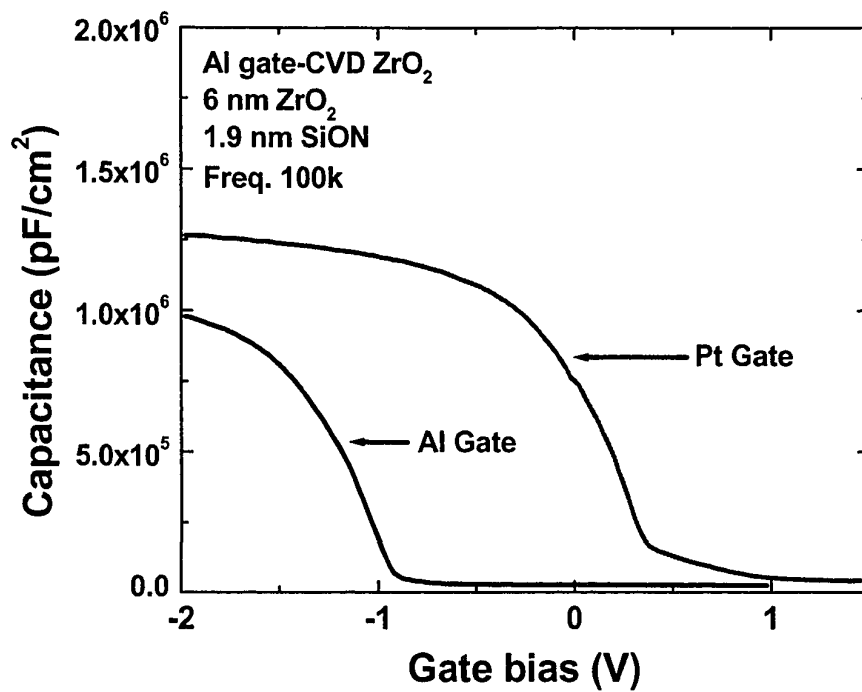


Figure 2.30 C-V characteristics of p-type  $\text{ZrO}_2$  MOS capacitors using Al and Pt as the gate electrodes.

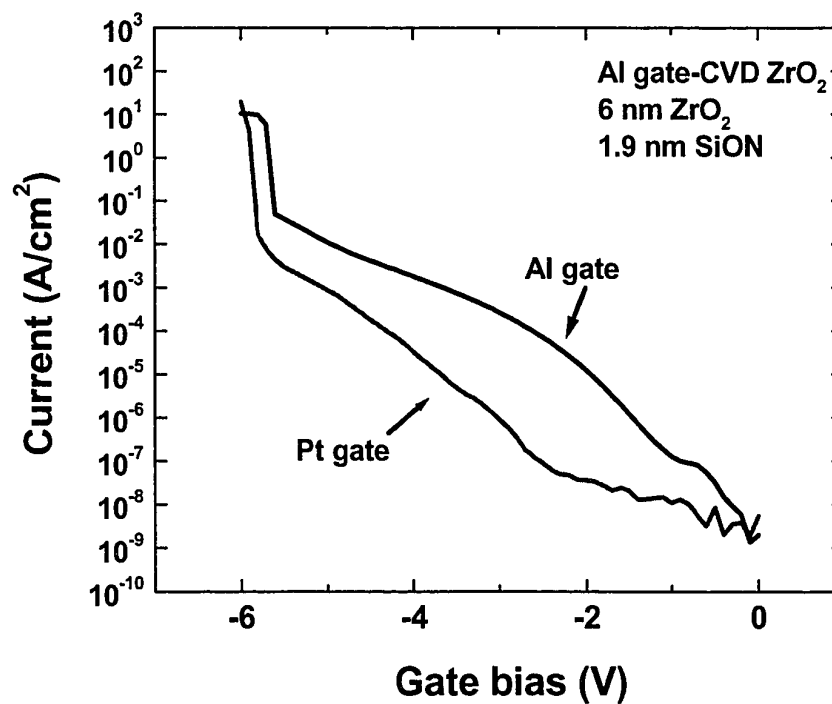
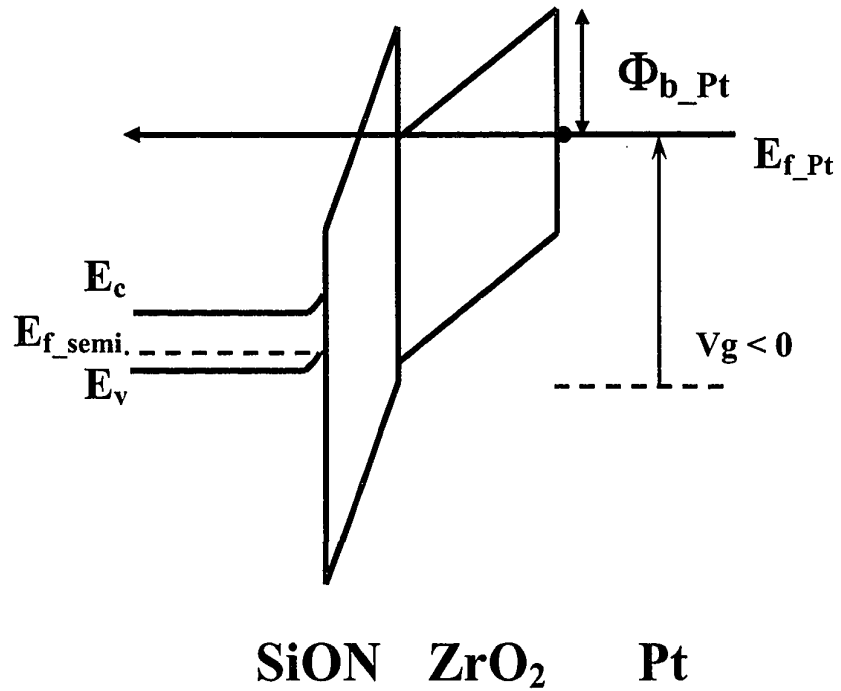
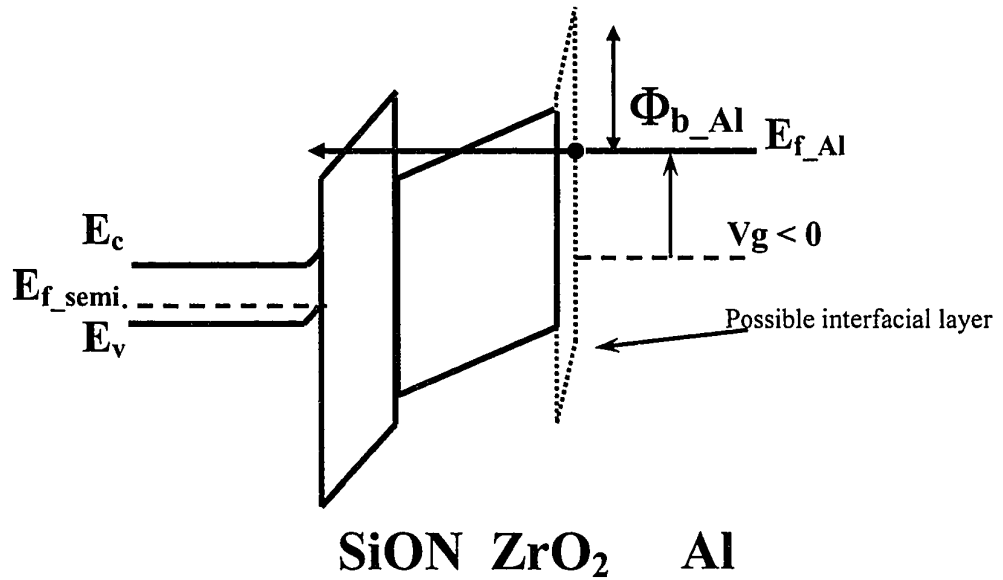


Figure 2.31 I-V characteristics of p-type  $\text{ZrO}_2$  MOS capacitors using Al and Pt as the gate electrodes.



(a)



(b)

Figure 2.32 In gate injection, electrons in MOS capacitors using Pt gate or Al gate face different barrier heights. The electric field applied on Al-gate device is smaller than that on Pt-gate device in this case.

platinum-gate capacitor under gate injection, because of the smaller tunnel barrier for the former, as illustrated in Figure 2.32.

It is clear that in order to choose a proper metal gate, possible formation of a transition layer between the metal gate and the high-gate dielectric, or possible diffusion from the metal gate into the high-k gate dielectric must be eliminated. And the transition layer near the metal gate and high-k dielectric interface influences the leakage current significantly under gate injection.

## 2.7 Chapter Summary

Our results have demonstrated that the  $\text{ZrO}_2/\text{Zr}$  silicate films synthesized by the unique JVD process can be scaled to at least 1nm with good dielectric properties, acceptable leakage current densities, and high reliability. Well-behaved n-channel and p-channel MOSFETs were successfully fabricated. Moreover, the JVD  $\text{ZrO}_2/\text{Zr}$  silicate gate dielectric possesses an interfacial layer with high thermal stability, which is desirable for conventional CMOS process flow. Also, the metal electrode has a significant influence on the properties of the MOS capacitor using  $\text{ZrO}_2$  as the gate dielectric, especially for the device under gate injection operation. The excellent results from JVD  $\text{ZrO}_2/\text{Zr}$  silicate gate dielectrics suggest the possibility of their use for fabricating high-quality CMOS devices with conventional CMOS processing procedures.

## Chapter 3

### Some Other High-k Gate Dielectrics: $\text{TiO}_2$ , $\text{Al}_2\text{O}_3$ , and $\text{Ta}_2\text{O}_5$ .

Numerous high-k materials have been under intensive research in industry and academia. However, none of the high-k materials studied satisfies all the stringent requirements for a gate dielectric to succeed silicon dioxide. Therefore, some innovative engineering approaches must be implemented to improve the quality of high-k gate dielectrics. In this chapter, we will present the results of the improved bulk properties and interface properties of several high-k gate dielectrics after using novel engineering approaches.

Except for its mediocre dielectric constant,  $\text{Al}_2\text{O}_3$  is an attractive candidate<sup>66,67</sup> to replace silicon dioxide for its high bandgap and barrier height, high thermal stability on silicon, and high crystallization temperature. On the other hand,  $\text{TiO}_2$ , another candidate, has exceptionally high dielectric constant, about 80, but its low bandgap, low thermal stability on silicon, and low crystallization temperature make it difficult to succeed silicon dioxide, though  $\text{TiO}_2$  gate dielectrics, including the JVD  $\text{TiO}_2$ , have demonstrated good interface properties and low leakage current<sup>55</sup>. The two materials mentioned above possess

opposite properties, and one's weaknesses are the other's strengths. Therefore, it is natural for us to combine these two materials to obtain a new material with improved properties. By combining  $\text{Al}_2\text{O}_3$  and  $\text{TiO}_2$ , we have demonstrated that the new titanium aluminates inherit the merits of both  $\text{Al}_2\text{O}_3$  and  $\text{TiO}_2$ , with better thermal stability and higher crystallization temperature than those of  $\text{TiO}_2$  and larger dielectric constant than that of  $\text{Al}_2\text{O}_3$ .

To obtain a good interface between a high-k material and Si is another big challenge for implementing high-k materials. Both  $\text{TiO}_2$  and  $\text{Ta}_2\text{O}_5$  are candidates to replace silicon dioxide. However, the low thermal stability on Si, such as the formation of silicon oxide or silicides upon processing, places them in disadvantage. In order to solve this problem, an ultra-thin JVD silicon nitride layer is inserted between a high-k material and Si. The high quality JVD silicon nitride ensures an extraordinary interface layer for the gate stack, and the oxygen-diffusion-blocking property of the JVD silicon nitride makes the EOT of the gate stack stable during subsequent high temperature anneals even in the presence of oxygen. Moreover, the relatively high dielectric constant of the JVD silicon nitride layer compared to that of  $\text{SiO}_2$  results in a modest reduction of the effective dielectric constant of the gate stack, while providing an excellent interface layer, which is a far better solution than a silicon dioxide interface layer. Furthermore, the JVD silicon nitride provides a larger barrier over Si conduction band edge than that of either  $\text{TiO}_2$  or  $\text{Ta}_2\text{O}_5$ , enabling it to block the thermionic currents at elevated temperatures.

For EOT of gate dielectric below 2nm, how to obtain the correct C-V curve to extract the EOT becomes a big problem. In Section 3.3, we will present a simple four-element equivalent circuit, together with a dual-frequency C-V measurement, to derive the correct C-V curve. This new method has many advantages over the conventional three-element method<sup>85</sup> and the widely used Hauser's method<sup>84</sup> for the EOT extraction.

## 3.1 Titanium Aluminates

In this section, we report the electrical and physical properties of ultra-thin titanium aluminates deposited by the JVD process. Both MOS Capacitors and MOSFETs were fabricated. It is shown that films with EOTs down to 1.2 nm possess good thermal stability and good electrical properties; for Al concentration of 30 atomic % or more, the film can survive an annealing temperature higher than 800 °C, which is attractive for the conventional CMOS process.

### *3.1.1 Fabrication of MOS Structures with Titanium Aluminates as Gate Dielectrics*

The Jet-Vapor-Deposition process used for the titanium aluminates deposition is very similar to the process for the zirconium oxide deposition. However, instead of using zirconium vapor source, two separate vapor sources, titanium and aluminum vapor sources, are employed. Using DC sputtering in argon ambient, the titanium vapor and the aluminum vapor are generated simultaneously by separate titanium and aluminum metal targets. One titanium vapor source, one aluminum vapor source, and one oxygen source are used to deposit titanium aluminates, as shown in Figure 3.1. The sputtering current, which is a function of voltage, electrode to target distance, and vapor pressure, controls the plasma density and the amount of the sputtered material. We are able to control the generation rates of the titanium source and the aluminum source by adjusting the corresponding sputtering currents. And by altering the generation rates of the titanium vapor and the aluminum vapor, we can modulate the titanium to aluminum ratio in titanium aluminates. The titanium vapor and aluminum vapor are carried down stream in helium gas. The downstream pressure is kept at about 0.1 Torr to maintain a 10 to 1

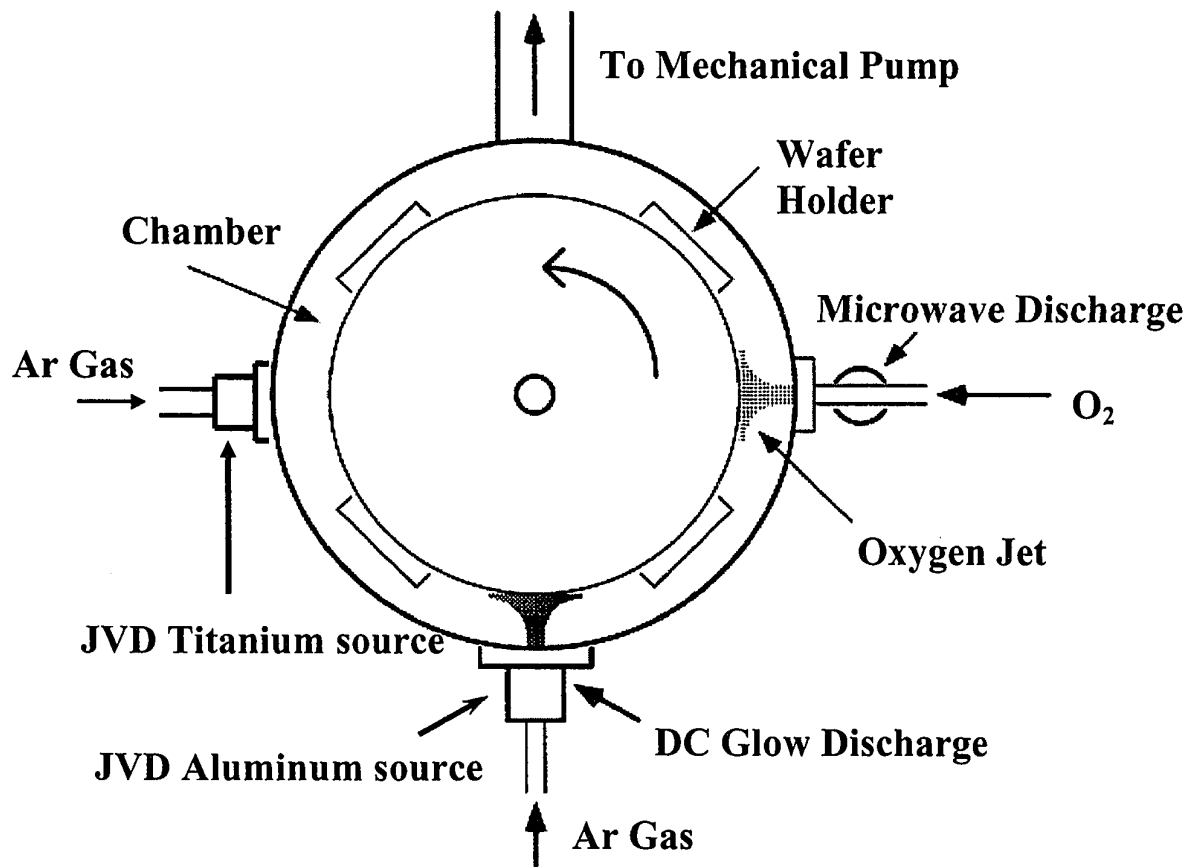


Figure 3.1 Schematic of the top view of the JVD system for titanium aluminates deposition.

upstream-to-downstream pressure ratio in order to generate the strong titanium and aluminum jets. When only the titanium vapor or the aluminum vapor is operating, the system can be used for titanium oxide or aluminum oxide deposition, respectively. The motion system for the titanium aluminates deposition is identical to the motion system for the zirconium oxide deposition. Wafers are mounted on the sidewalls of the carousel, which spins at a constant speed, and moves vertically with a linear translation oscillation simultaneously to achieve the required thickness uniformity of the deposited film. During each cycle, the titanium source, aluminum source, and oxygen source scan through the wafers one by one. The unique sub-monolayer deposition feature of the JVD process ensures uniform blending of titanium aluminates.

Normally ultra-thin titanium aluminates are deposited by the JVD process at room temperature on HF-last Si wafers. Various Post-Deposition-Anneal (PDA) conditions up to 1000 °C are used to tailor dielectric properties. The fabrication steps of the titanium aluminate MOS capacitors and MOSFETs are identical to those described in Figures 2.4 and 2.5. Aluminum is thermally evaporated to form the top electrodes and back contacts of MOS capacitors and MOSFETs. In order to reduce the reaction with the electrodes, no PMA is performed.

### ***3.1.2 TiO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub>***

Long before it was considered for the Si CMOS gate dielectric applications, because of its high refractive index, excellent chemical and abrasion resistance, and superb transmittance in the near-infrared and visible wavelengths, titanium oxide (TiO<sub>2</sub>) had found its applications in waveguide anti-reflection coatings<sup>19</sup>. Now owing to its exceptionally high dielectric constant, TiO<sub>2</sub> has caught the attention as a possible long-term solution to replace silicon dioxide. The dielectric constant of TiO<sub>2</sub> can be as high as 170 along the optical axis

in the single crystal tetragonal rutile phase<sup>120</sup>. Though normally the dielectric constant of TiO<sub>2</sub> thin film is lower than that of its single crystal phase, it still can reach 80<sup>121</sup>. The crystallization temperature of TiO<sub>2</sub> is quite low, which causes serious concerns for the uniformity requirement. The anatase crystal phase usually starts to crystallize at 300 °C and above, and the rutile phase normally requires a higher temperature, 800 °C or above, to crystallize<sup>122,123</sup>.

Due to its high melting point (2054 °C), hardness, and low electrical conductivity even at elevated temperatures, Aluminum oxide (Al<sub>2</sub>O<sub>3</sub>) is arguably the most widely used metal oxide. Now these excellent properties make it an attractive candidate to replace silicon dioxide as the gate dielectric for Si CMOS. The  $\alpha$  phase of Al<sub>2</sub>O<sub>3</sub> is the most well defined crystalline phase of Al<sub>2</sub>O<sub>3</sub>, and it is also the hardest known crystal and one of the most thermodynamically stable crystals<sup>111</sup>. However, the amorphous phase of Al<sub>2</sub>O<sub>3</sub> can exist up to 1100 °C<sup>111</sup>, which satisfies the process integration requirement of the conventional CMOS process. Moreover, its high bandgap and high barrier height make it a good insulator, though its low dielectric constant makes it less attractive for future CMOS applications.

### ***3.1.3 Titanium Oxide Made by JVD***

The results on the JVD TiO<sub>2</sub> are presented first, before we introduce the results on the JVD titanium aluminates. The JVD TiO<sub>2</sub> gate dielectrics deposited on Si substrates with EOTs down to 1.1 nm (EOT) possess good dielectric properties, as indicated by C-V and I-V measurements. And according to the best of our knowledge, they are the thinnest TiO<sub>2</sub> films ever made on Si substrate. The deposition of these ultra-thin JVD TiO<sub>2</sub> gate dielectrics was conducted at room temperature. The JVD TiO<sub>2</sub> gate dielectrics show promising properties after PDA at 600 °C. However, the JVD TiO<sub>2</sub> gate dielectrics

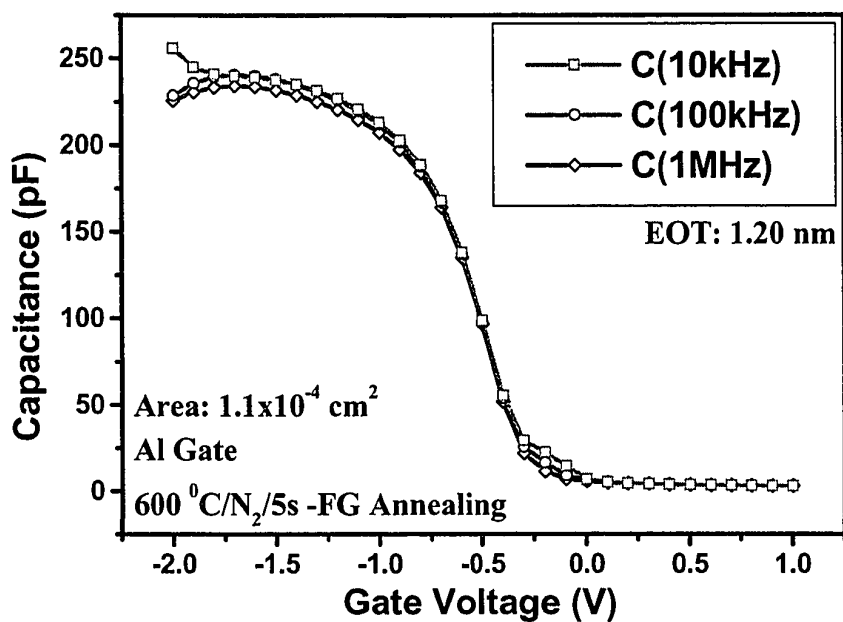
annealed at higher temperatures show significant degradation of film quality, which raises questions on its suitability in the conventional CMOS process flow.

The C-Vs of the JVD TiO<sub>2</sub> films deposited directly on HF-last p-type Si substrates and N<sub>2</sub>O plasma exposed p-type Si substrates are shown in Figures 3.2 and 3.3, respectively. The physical thicknesses of both films are about 3 nm, as measured by ellipsometry. Both JVD TiO<sub>2</sub> films were annealed at 600 °C in N<sub>2</sub> for 5s, and at 550 °C in forming gas for 30 minutes. The multi-frequency C-V and hysterises C-V results from both of the JVD TiO<sub>2</sub> films exhibit very small frequency dependence and negligible hysterises, which indicate excellent interface and bulk properties.

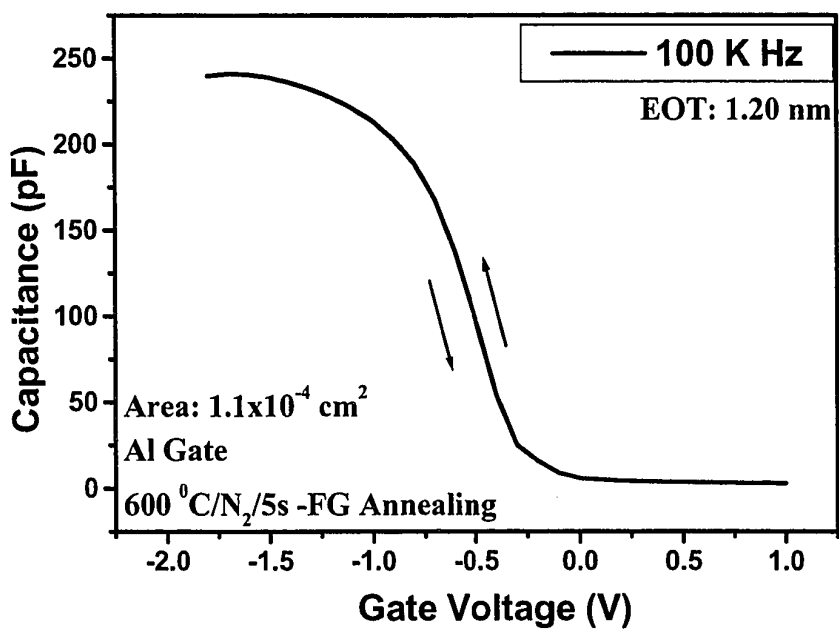
However, both of the JVD TiO<sub>2</sub> films deposited on the HF-last and N<sub>2</sub>O plasma exposed Si substrates collapse after the PDA at 800 °C in N<sub>2</sub> for 5s. As shown in Figure 3.4, the irregular shapes of C-V curves indicate very poor dielectric properties. Moreover, I-V measurements also reveal that the leakage currents of the JVD TiO<sub>2</sub> films annealed at 800 °C are significantly higher than those annealed at 600 °C, as shown in Figure 3.5.

It is clear that the JVD TiO<sub>2</sub> films can withstand the PDA at 600 °C, but they show signs of severe degradation after annealing at 800 °C. Therefore, the JVD TiO<sub>2</sub> films may be suitable for a replacement gate process flow, for which 600 °C is sufficient for anneals.

In order to improve the high-temperature properties of the JVD TiO<sub>2</sub>, we must implement some innovative methods. One solution is incorporating Al into TiO<sub>2</sub> to utilize the high thermal stability of Al. A thermally stable interface layer may also help to improve the properties of the JVD TiO<sub>2</sub> after high temperature anneals. Because there is no significant difference between the JVD TiO<sub>2</sub> films deposited on the HF-last Si surface or the N<sub>2</sub>O plasma treated Si surface, a more aggressive surface treatment, such as inserting an ultra-thin SiN layer between Si and TiO<sub>2</sub>, is necessary to achieve good dielectric properties after high temperature anneals.

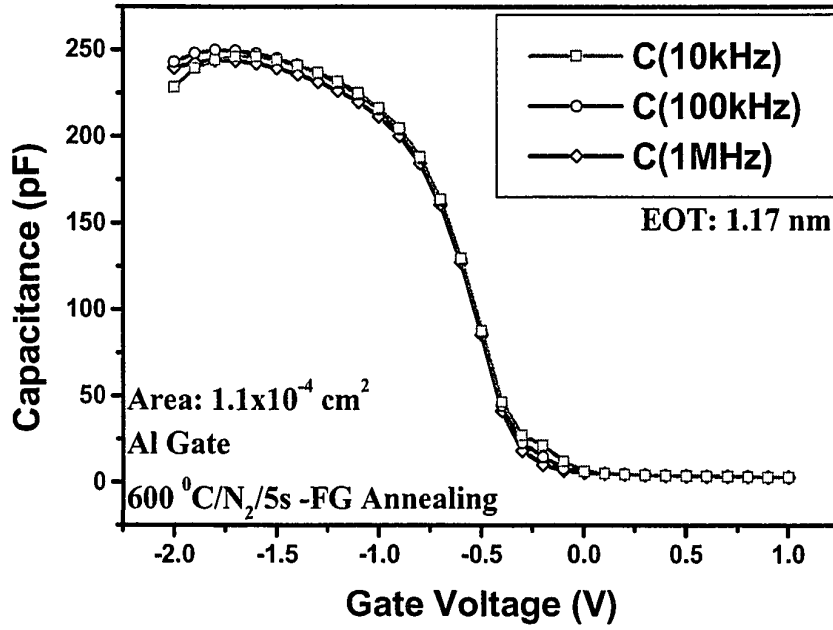


(a)

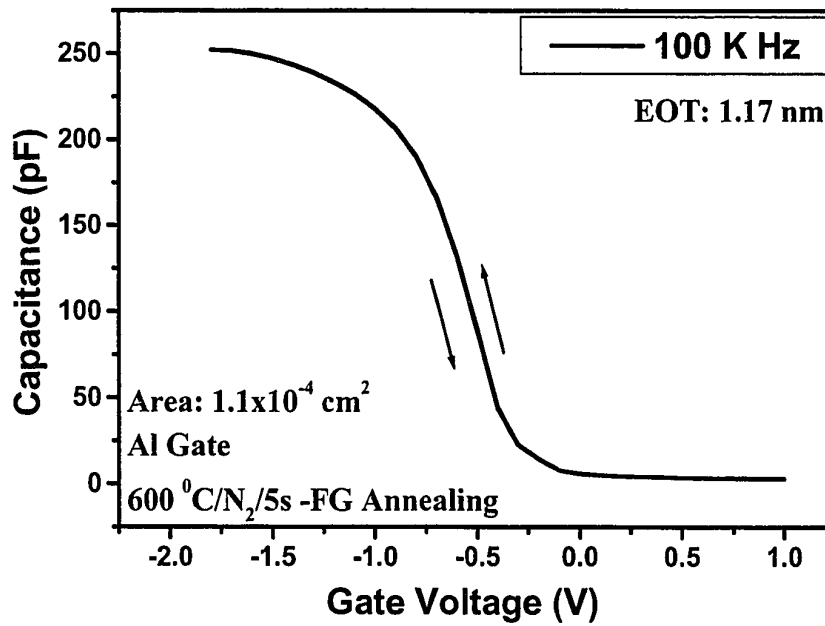


(b)

Figure 3.2 (a) Multi-frequency and (b) Hysteresis C-V characteristics of MOS capacitors with JVD  $\text{TiO}_2$  gate dielectrics deposited on HF-last Si surface.

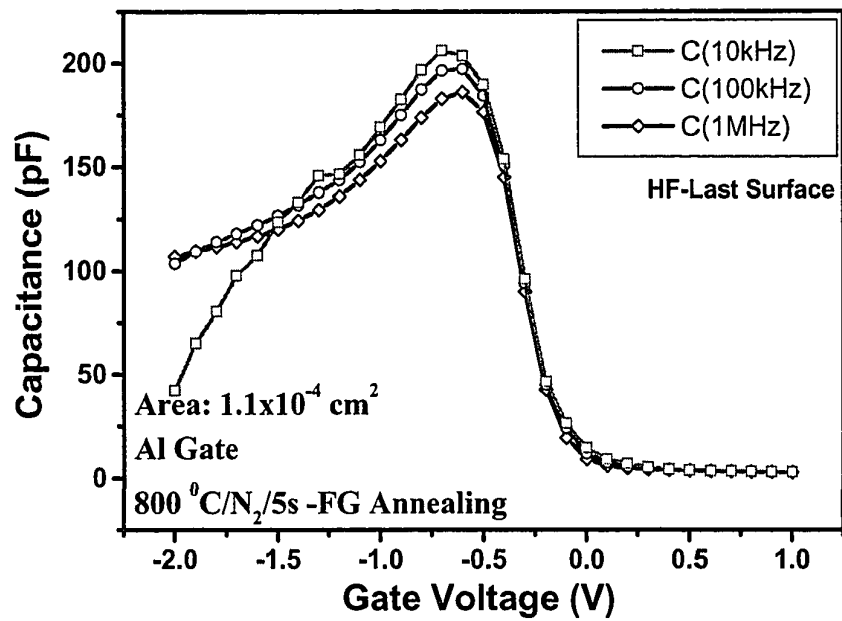


(a)

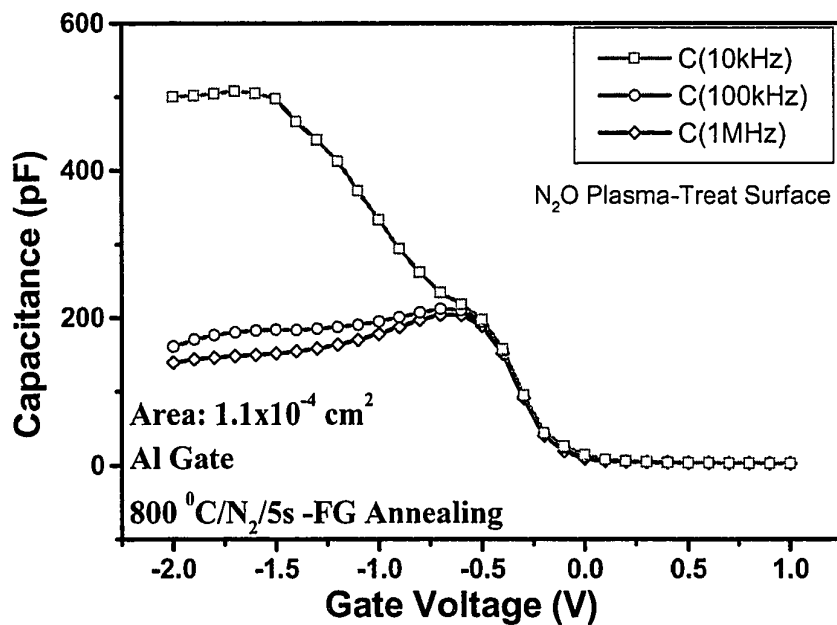


(b)

Figure 3.3 (a) Multi-frequency and (b) Hysteresis C-V characteristics of MOS capacitors with JVD  $\text{TiO}_2$  gate dielectrics deposited on  $\text{N}_2\text{O}$  plasma treated Si surface.



(a)



(b)

Figure 3.4 C-V Characteristics of MOS capacitors with JVD TiO<sub>2</sub> gate dielectrics (a) deposited on HF-last Si surface and (b) deposited on N<sub>2</sub>O plasma treated Si surface show poor dielectric properties after annealing at 800 °C.

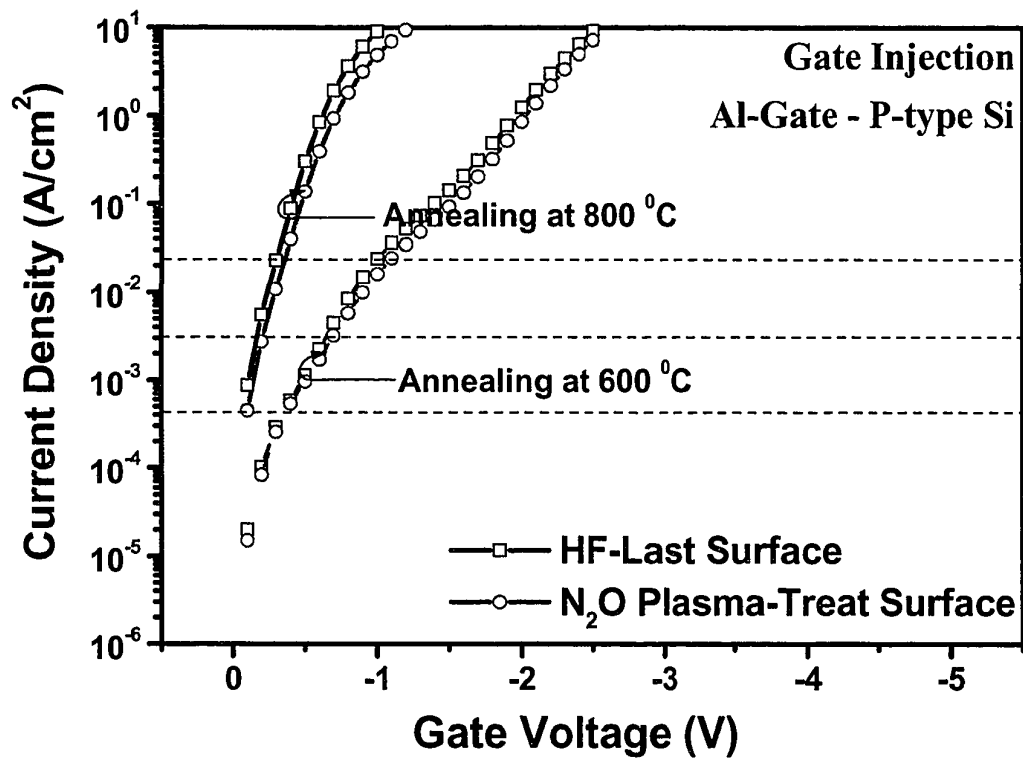


Figure 3.5 I-V Characteristics of JVD TiO<sub>2</sub> gate dielectrics deposited on N<sub>2</sub>O plasma treated Si surface and HF-last Si surface show the leakage currents increase dramatically after annealing at 800 °C when compared to the samples annealed at 600 °C.

### ***3.1.4 Properties of Titanium Aluminates***

#### **Crystallization Temperature**

One of the important purposes to incorporate Al into titanium oxide is to increase the crystallization temperature of titanium oxide. As shown in Figure 3.6, we observe that the crystallization temperature of titanium aluminate increases with the aluminum concentration. In order to increase the sensitivity of the XRD method, the angle between the incoming X-ray and the sample surface is set at  $5^\circ$ . At such a shallow angle, the X-ray beam travels a relatively long distance in a thin film, and it increases the X-ray's probing volume. Films as thick as 100 nm are used in this study. As shown in Figure 3.6(a),  $\text{TiO}_2$  is obviously crystallized after annealing at  $600^\circ\text{C}$ , which is confirmed by optical measurements as well. As indicated in Figure 3.7,  $\epsilon_1$  and  $\epsilon_2$  for the  $\text{TiO}_2$  annealed at  $600^\circ\text{C}$  reveal sharper peaks compared with those of the as-deposited amorphous  $\text{TiO}_2$ , which may be an indication of the onset of crystallization. By adding 15 atomic % aluminum, where the atomic concentration of aluminum is extracted from the deposition rates, this titanium aluminate film remains amorphous, as shown in Figure 3.6(b), which is confirmed by the TEM image. For the titanium aluminate film with 30 atomic % aluminum, we do not observe evidence of crystallization after PDA up to  $800^\circ\text{C}$  (Figure 3.6(c)). Moreover, with 80 atomic % aluminum in the film, the titanium aluminate film remains amorphous even after PDA at  $1000^\circ\text{C}$ . Optical measurements also indicate the rise of crystallization temperature with the increase of Al concentration, as suggested by the broadening of the small feature at  $\sim 3.5$  eV, as shown in Figure 3.8.

### **Dielectric Constant**

By adding titanium, we are able to increase the dielectric constant of  $\text{Al}_2\text{O}_3$ . We observe that the dielectric constant of titanium aluminate grows with titanium concentration, as shown in Figure 3.9. The dielectric constant was calculated as

$$\varepsilon = \frac{T_{\text{physical}}}{EOT} . \quad (3.1)$$

The physical thicknesses are measured by ellipsometry, and the EOTs are calculated from the capacitances in accumulation. To minimize the influence of the interface layer in the calculation of the dielectric constants of titanium aluminates, the dielectric constants are calculated from relatively thick films (~100 nm). The dielectric constant rises nonlinearly with the increase of the titanium concentration. For films with titanium concentrations less than 50 atomic %, the dielectric constant increases slowly. However, for films with titanium concentrations more than 50 atomic %, the dielectric constant increases rapidly. For the film with 20 atomic % titanium, the dielectric constant of the titanium aluminate is only about 10. However, for the film with 50 atomic % titanium, the dielectric constant increases to 25, which is comparable to that of  $\text{ZrO}_2$  or  $\text{HfO}_2$ . For the titanium aluminate film with 70 atomic % titanium, the dielectric constant is as high as 60. Moreover, the bandgap and barrier height also change with the titanium concentration, which we will discuss in detail in Chapter 4.

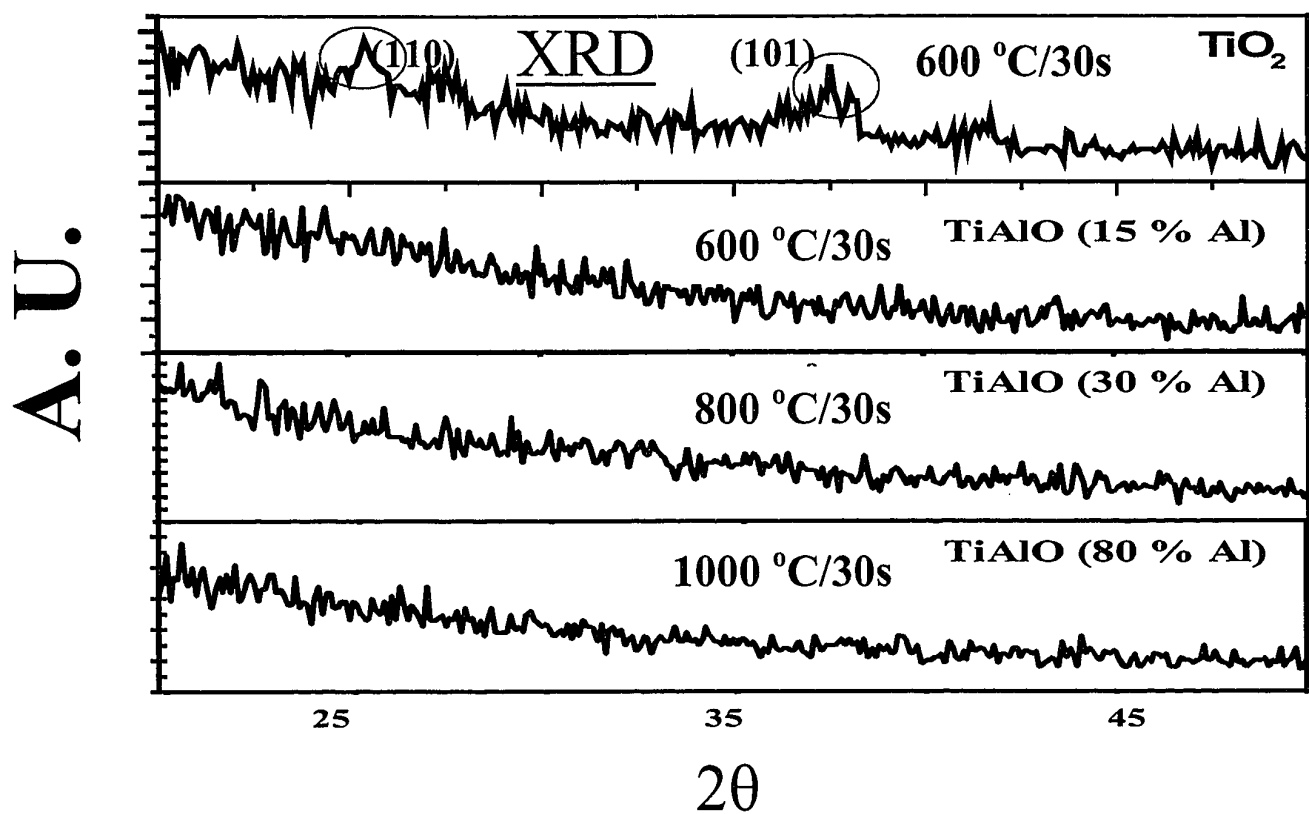


Figure 3.6 XRD reveals that the crystallization temperature for titanium aluminates increases with Al concentration.

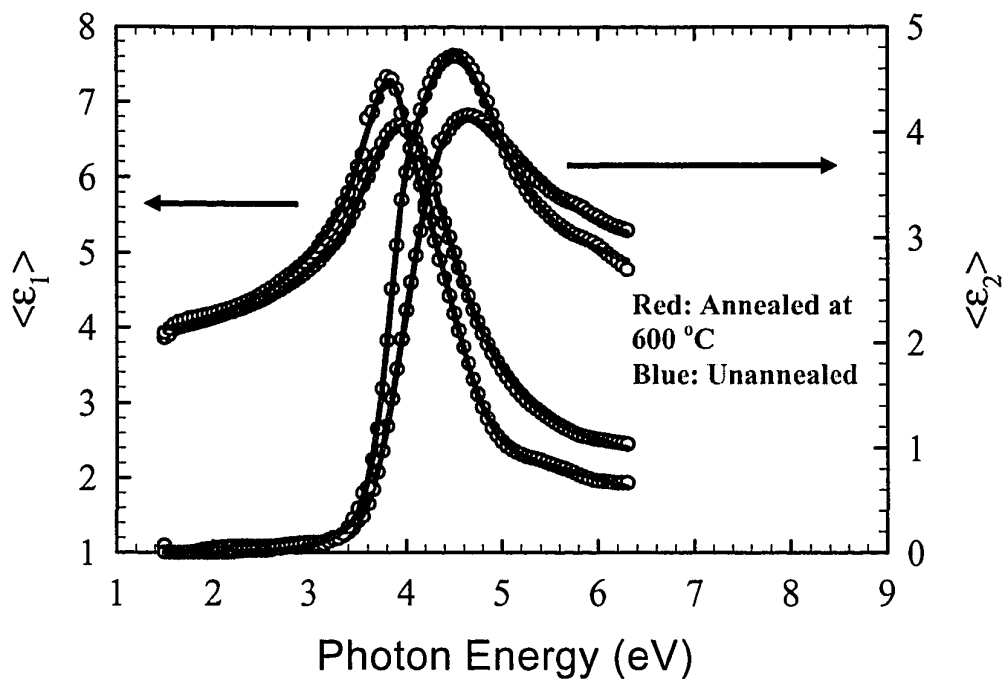


Figure 3.7  $\epsilon_1$  and  $\epsilon_2$  for the TiO<sub>2</sub> annealed at 600°C (red curves) show sharper peaks compared with those for the unannealed amorphous TiO<sub>2</sub> (blue curves), which indicate the onset of crystallization.

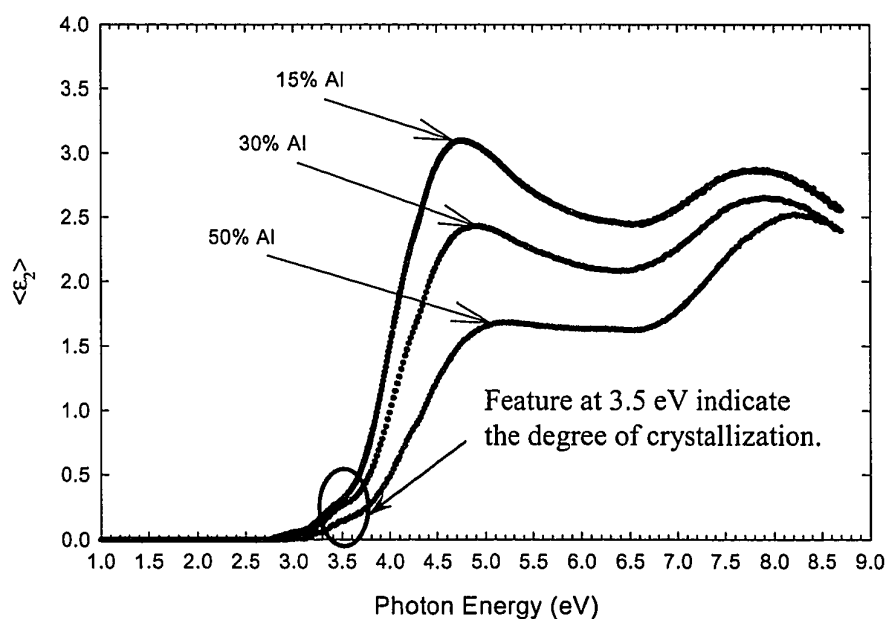


Figure 3.8 Optical measurements also confirm that the crystallization temperature for titanium aluminate increases with Al concentration.

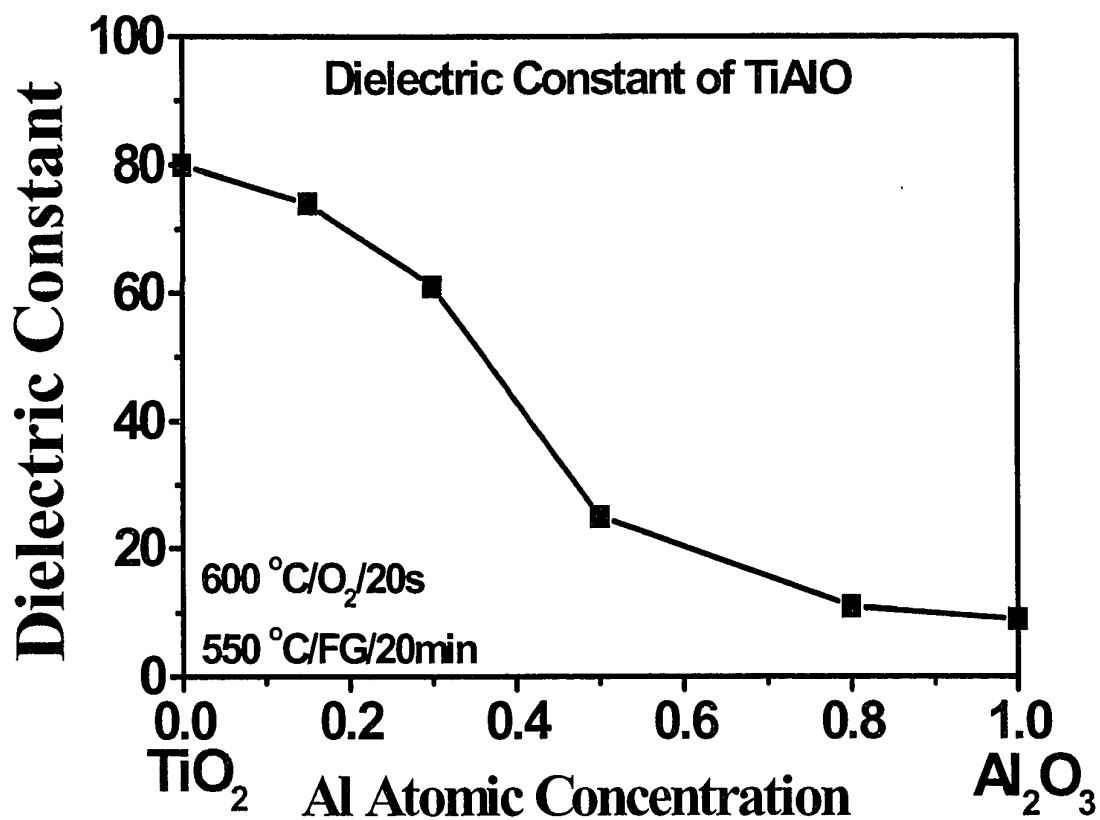


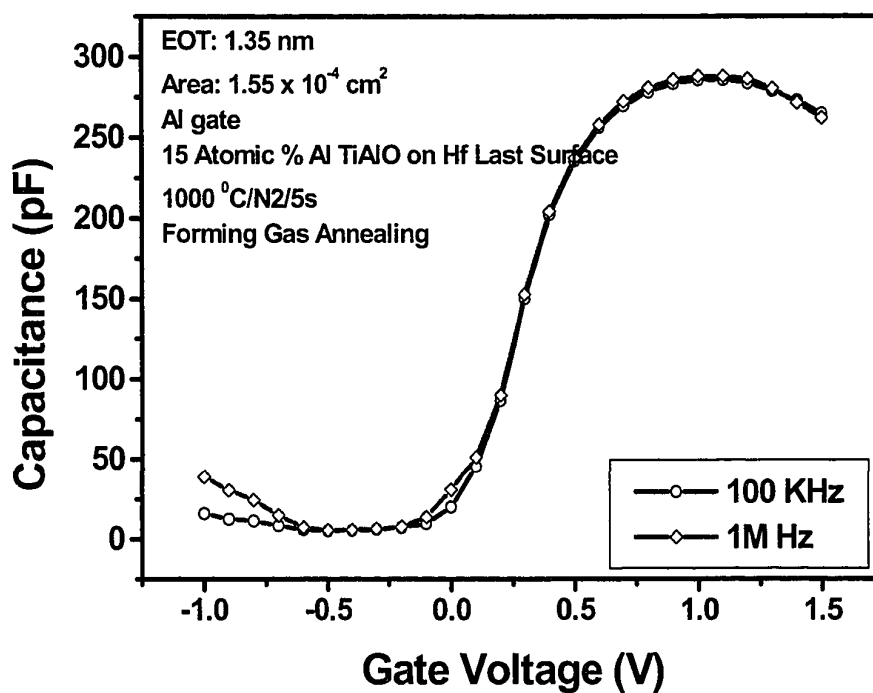
Figure 3.9 The dielectric constants for titanium aluminates.

### **Electrical Properties**

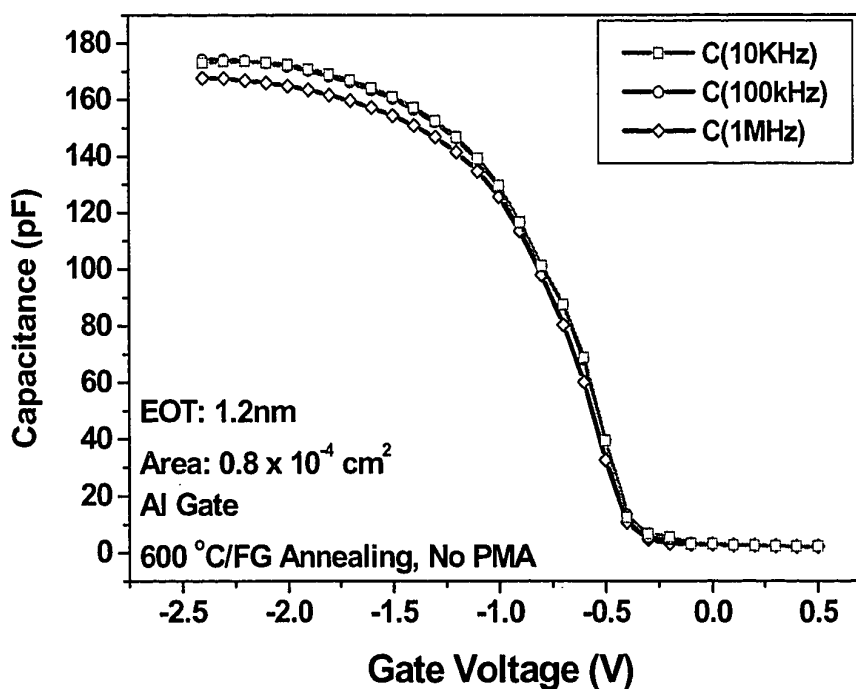
Electrical data reveal the improved dielectric properties of titanium aluminates over those of titanium oxide after high temperature anneals. Figure 3.10(a) presents the multi-frequency C-V of a titanium aluminate gate dielectric with 15 atomic % aluminum concentration on n-type substrate after PDA at 1000 °C. In contrast to the erratic shape and huge frequency dispersion in the accumulation region of the multi-frequency C-V of the JVD TiO<sub>2</sub> gate dielectric after a PDA at 800 °C, as shown in Figure 3.4, the negligible frequency dependence in the multi-frequency C-V of this titanium aluminate gate dielectric indicates good dielectric properties. C-V results demonstrate that adding aluminum into TiO<sub>2</sub> improves the high temperature stability of TiO<sub>2</sub>. The titanium aluminate gate dielectric with 15 atomic % aluminum concentration deposited on p-type silicon substrate also shows good multi-frequency C-V characteristics (Figure 3.10 (b)). After considering the quantum effect, an EOT of 1.2 nm is extracted for this film.

The I-V characteristics of this titanium aluminate gate dielectric also reveal a significant reduction of leakage current even after annealing at 1000 °C, when compared to that of thermal silicon dioxide with the same EOT, as presented in Figure 3.11. By considering the quantum confinement effect, an EOT of 1.35 nm is extracted from the C-V measurement for this titanium aluminate film. We observe at least one order of magnitude reduction of leakage current for this titanium aluminate film when compared to silicon dioxide, and more reduction is observed at low electric fields. Both the C-V and I-V characteristics suggest that the titanium aluminate gate dielectric with 15 atomic % aluminum concentration possesses good electrical properties after high temperature anneals up to 1000 °C.

Transistors using TiAlO as gate dielectrics were successfully fabricated. Figure 3.12 shows the Id-Vd characteristics of a NMOSFET with a titanium aluminate gate dielectric



(a)



(b)

Figure 3.10 C-V Characteristics of MOS capacitors based on the JVD titanium aluminate gate dielectrics with 15 atomic % Al concentration (a) on n-type Si substrate, and (b) on p-type Si substrate.

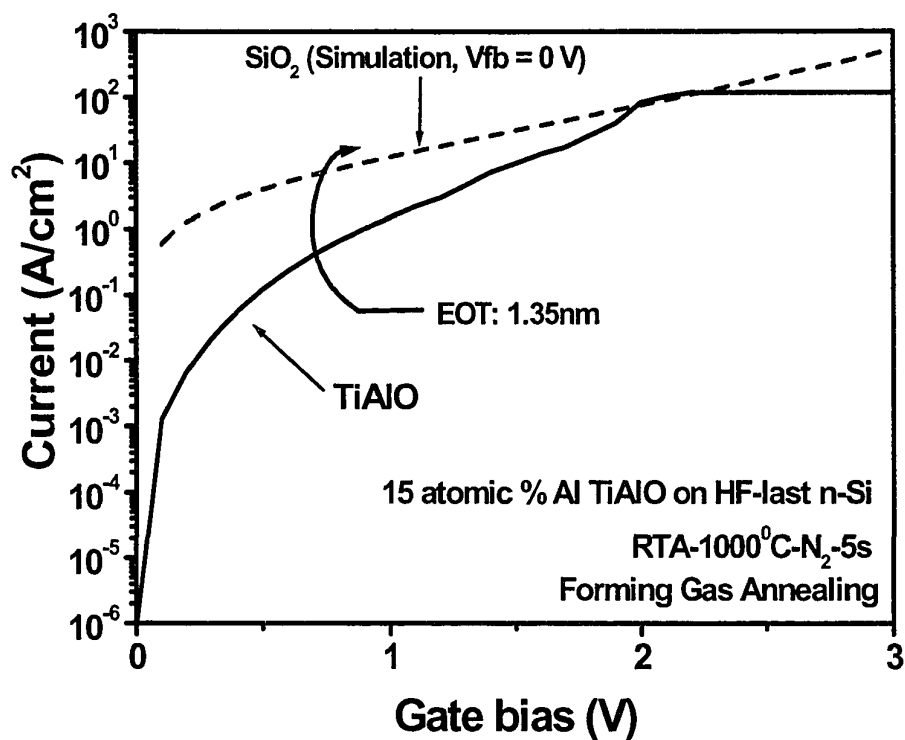


Figure 3.11 I-V Characteristic of a JVD titanium aluminate gate dielectric with 15 atomic % Al concentration compared with a calculated I-V of thermal silicon dioxide with the same EOT.

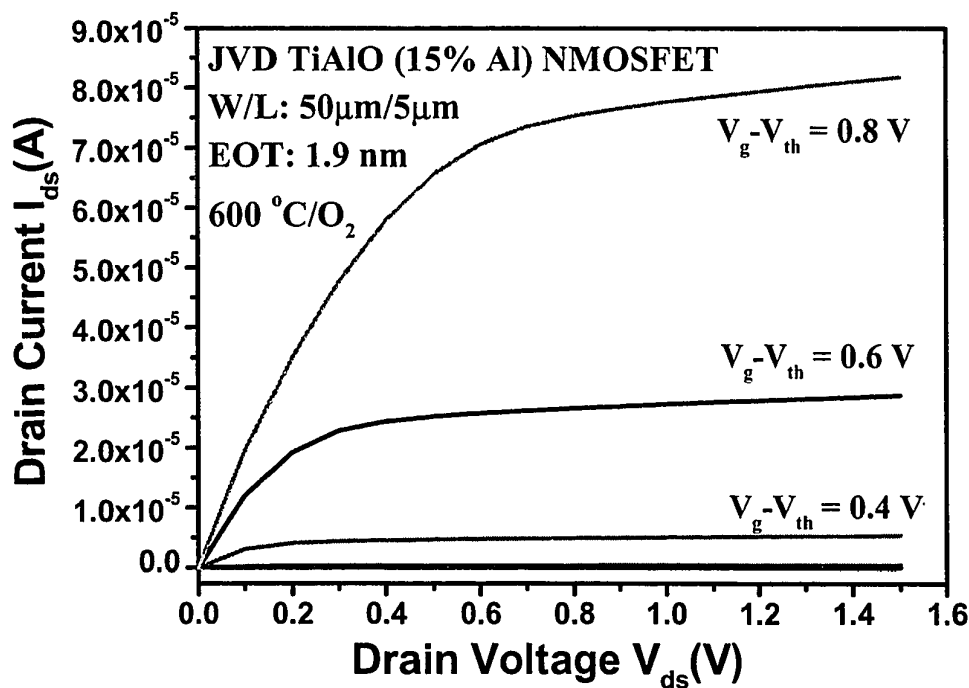


Fig. 3.12 Output characteristics of an n-channel MOSFET with a JVD titanium aluminate gate dielectric with 15 atomic % Al concentration.

having 15 atomic % aluminum concentration. The EOT of the gate dielectric of this 5 $\mu$  long and 50 $\mu$  wide NMOSFET is about 1.9 nm. The good output characteristics of this transistor also indicate good dielectric properties of the JVD titanium aluminate.

### ***3.1.5 Effects of Nano-Crystallization***

TEM images reveal that the titanium aluminate with 15 atomic % aluminum concentration is amorphous after annealing at 600 °C, as presented in Figure 3.13(a), which is verified by the XRD results as well. However, the titanium aluminate films with 15 atomic % aluminum concentration annealed at 800 °C and 1000 °C are partially crystallized, as shown in Figure 3.13(b) and 3.13(c), respectively. Most regions of the titanium aluminate films annealed at 800 °C and 1000 °C remain amorphous. However, there are nanometer-scale crystals embedded in the amorphous films, and the area occupied by the nanometer scale crystals is about 10 to 20 percent of the total area.

Such a morphology change of titanium aluminates has impacts on the electrical properties of devices using them as the gate dielectric. It seems such nano-crystallization has negligible influence on the leakage currents of a MOS capacitor with a considerable area. Typical I-V curves from the titanium aluminate films with 15 atomic % aluminum concentration after a 600 °C/10s anneal and a 800 °C/10s anneal are shown in Figure 3.14. The C-Vs of these two films indicate that they have identical flat band voltage. The EOTs are 1.27nm and 1.29 nm for the titanium aluminate films annealed at 600 °C and 800 °C, respectively. The perfect alignment of the two I-V curves measured on these two devices indicates that the leakage current is largely unaffected by the presence of the nanometer scale crystals. However, the areas of the devices that we measured are on the scale of 10<sup>-4</sup> cm<sup>2</sup> or more. The effects of the nano-crystalline on the leakage currents for devices with much smaller dimensions are not clear at this stage.

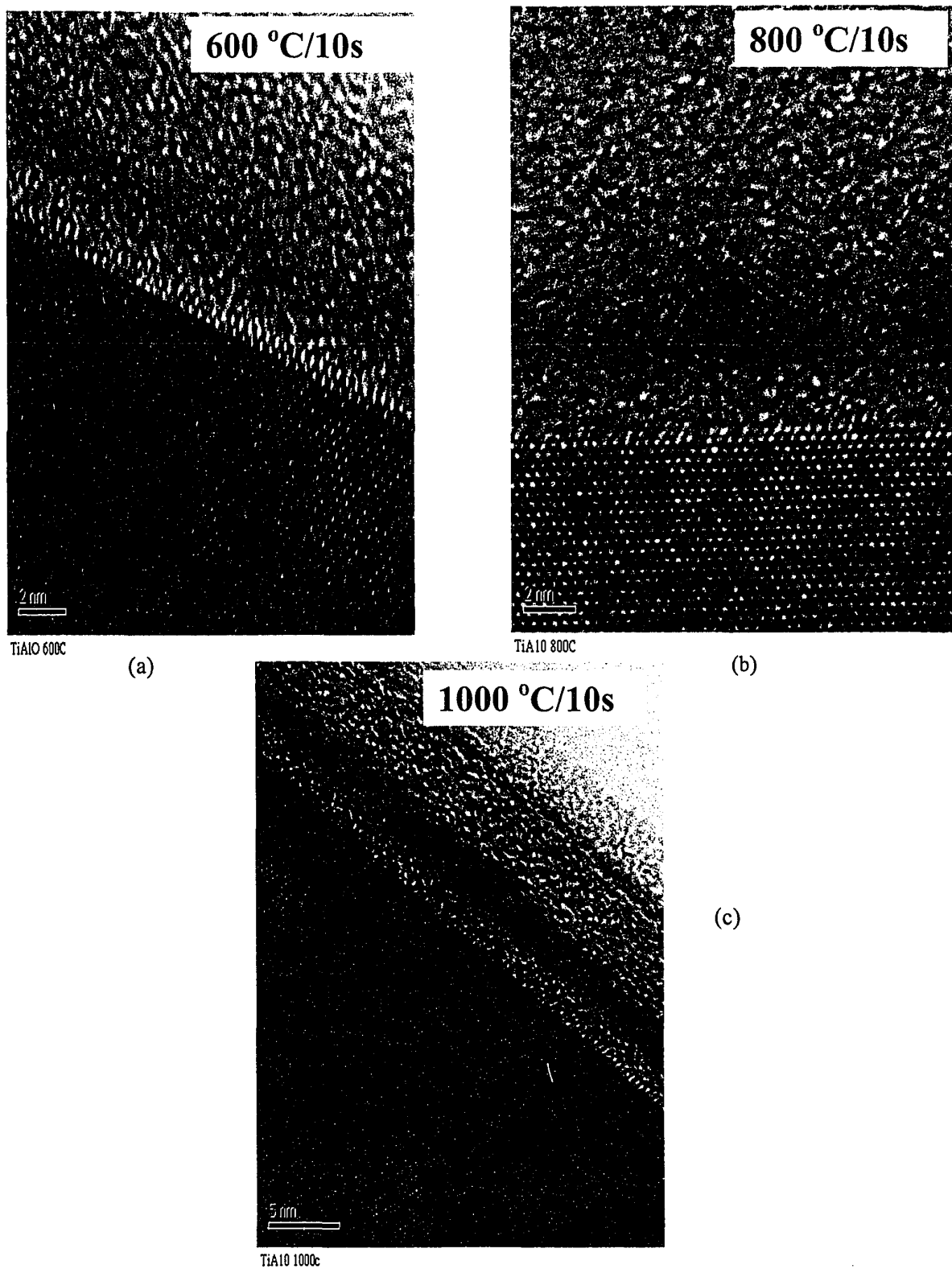


Figure 3.13 TEM images of JVD titanium aluminates with 15 atomic % Al concentration annealed at (a) 600 °C, (b) 800 °C and (c) 1000 °C reveal mixed phases after annealing at 800 °C or above.

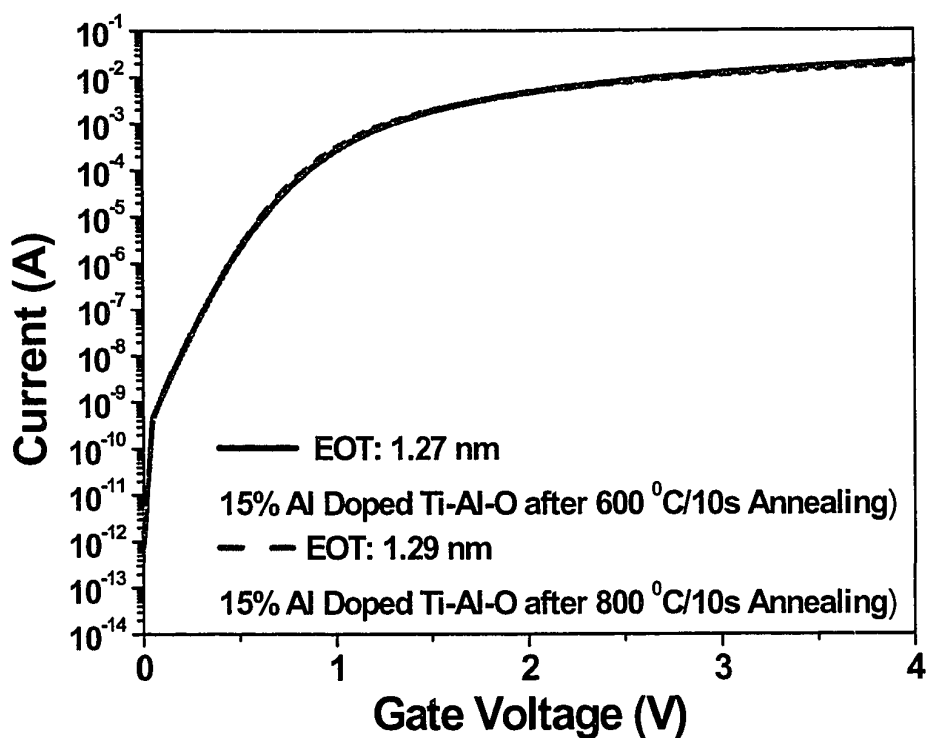


Figure 3.14 I-V characteristics of JVD titanium aluminates with 15 atomic % Al concentration unchanged after annealing at 600 °C and 800 °C.

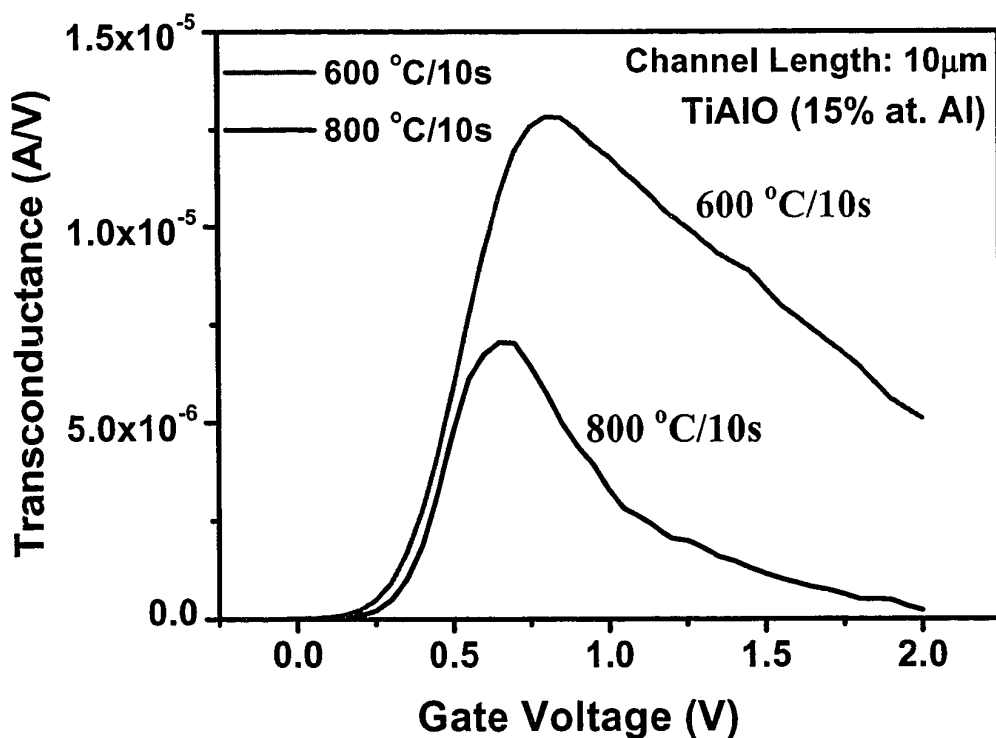


Figure 3.15 The transconductance of an NMOSFET having a JVD titanium aluminate gate dielectric with 15 atomic % Al concentration annealed at 800 °C degrades when compared with that after annealing at 600 °C.

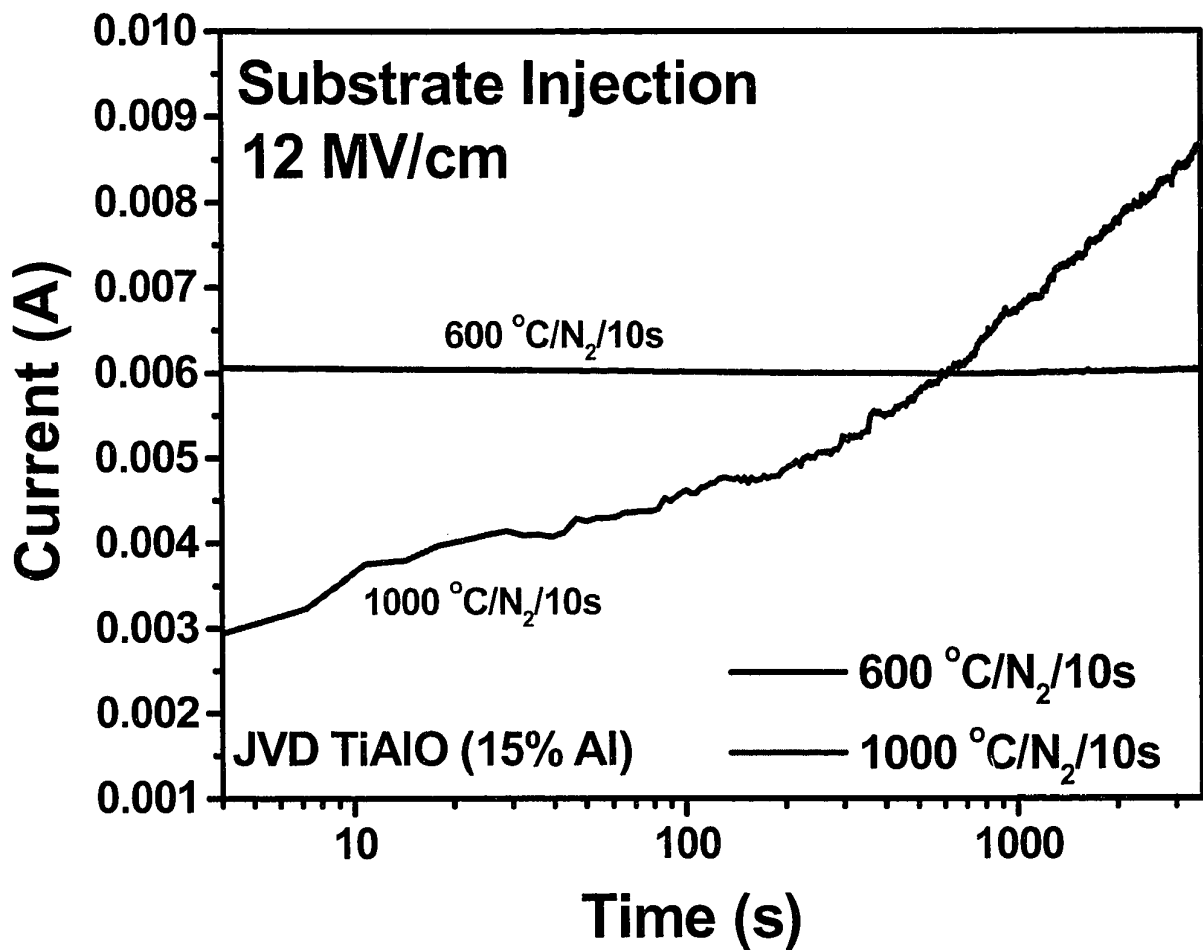


Figure 3.16 Constant-voltage stressing result reveals the degradation of reliability of a JVD titanium aluminate with 15 atomic % Al concentration after annealing at 1000 °C when compared to that after annealing at 600 °C.

Though the nano-crystallization has little influence on the leakage currents of devices with considerable sizes, it changes the transconductance of MOSFET dramatically. As shown in Figure 3.15, two transconductance curves are measured from two NMOSFETs using titanium aluminate gate dielectrics with 15 atomic % aluminum concentration after annealing at 600 °C and 800 °C, respectively. The results clearly show that the transconductance of the NMOSFET annealed at 600 °C, which is amorphous, is higher than that annealed at 800 °C, which is embedded with the nanometer-scale crystals. The results reveal that the mixed nano-crystalline-amorphous phase may cause transconductance degradation of MOSFET.

Not only does the transconductance suffer after the nano-crystallization of the titanium aluminate gate dielectric, but also its reliability degrades. As shown in Figure 3.16, during stressing at 12 MV/cm, the titanium aluminate film annealed at 600 °C, the amorphous film, shows a constant current, which suggests a robust film. However, in contrast, the current of the titanium aluminate film annealed at 1000 °C, the nano-crystallized film, increases gradually during the whole stressing process. The weak spots surrounding the nanometer scale crystals may result in much higher rates of trap generation during stressing. And the nano-crystallization of titanium aluminates does cause substantial degradation of transconductance and reliability of MOSFET.

By incorporating Al into TiO<sub>2</sub>, we have successfully increased the crystallization temperature of TiO<sub>2</sub>, and improved its electrical properties after high temperature anneals.

## 3.2 TiO<sub>2</sub>/SiN and Ta<sub>2</sub>O<sub>5</sub>/SiN Gate Stacks

Having an excellent interface between a high-k gate dielectric and Si is one of the most important and stringent requirements for any high-k gate dielectric. Besides the low trap and fix charge densities at the interface, it is critical that the interface between a high-k gate dielectric and Si remains stable during the CMOS process flow. However, even for the high-k materials that are thermally stable on Si from thermodynamic calculations, such as ZrO<sub>2</sub>, HfO<sub>2</sub>, And Al<sub>2</sub>O<sub>3</sub>, an unintended interfacial layer is unavoidable during deposition and subsequent anneals. Other less thermally stable high-k materials, such as TiO<sub>2</sub> and Ta<sub>2</sub>O<sub>5</sub>, cause more severe problems at the interface. TiO<sub>2</sub> and Ta<sub>2</sub>O<sub>5</sub> have the inclination to form a silicon oxide layer, which increases the total EOT of the gate dielectric, or form silicides, which short out the MOSFET. There is no better interface on Si than that of silicon dioxide. Therefore, some have inserted an ultra-thin layer of silicon dioxide between a high-k material and Si to improve the interface quality. However, this approach does come with a price. As we discussed in Chapter 1, such an approach limits the scalability of the gate dielectric. In order to improve the scalability of the gate stack, the interface layer is desired to have a high dielectric constant while possess good properties. The JVD silicon nitride has demonstrated interface quality comparable to thermal silicon dioxide and a dielectric constant about twice that of silicon dioxide. Thus, using the JVD silicon nitride as the buffer layer provides an excellent interface and improved scalability over silicon dioxide. Moreover, the JVD silicon nitride has strong diffusion resistance, which blocks oxygen diffusion and inter-diffusion between high-k materials and Si during thermal cycles in the process. Furthermore, the JVD silicon nitride also provides effective boron penetration resistance. And from our experimental results, the JVD TiO<sub>2</sub>/SiN and Ta<sub>2</sub>O<sub>5</sub>/SiN gate stacks have demonstrated good electrical properties.

### ***3.2.1 JVD Silicon Nitride***

As the JVD system for the metal oxide deposition, the JVD system for the silicon nitride deposition uses the same “sonic jet in a low-vacuum fast flow” principle and the “multiple jet, moving substrate” strategy<sup>107</sup> for film deposition. However, the vapor sources and substrate movement systems used for silicon nitride deposition are very different from those for the metal oxide deposition.

As shown in Figure 3.17, the vapor sources for the JVD silicon nitride deposition are provided directly by gas tanks. N<sub>2</sub> and diluted silane (0.2% SiH<sub>4</sub> in He) are used as the reaction gases for the silicon nitride deposition, and He is used as the carrier gas. The gases flow through a coaxial double quartz nozzle. N<sub>2</sub> and He flow in the outer nozzle, and diluted silane (0.2% SiH<sub>4</sub> in He) flows in the inner nozzle. A microwave cavity surrounding the outer nozzle is employed to generate nitrogen plasma in the outer nozzle. Due to the small diameter and high gas flow rate, the inner nozzle pressure remains at a sufficiently high level to prohibit plasma formation and associated silane dissociation. He carries out nitrogen plasma and silane in the form of supersonic jets. The high kinetic energy helps the reaction between silane and nitrogen radicals occurring at the Si surface to form silicon nitride. Usually before the silicon nitride deposition, N<sub>2</sub>O plasma, generated while flowing through the outer nozzle with He, is used for the pre-treatment of Si surface.

The schematic of the scanning motion system for JVD silicon nitride deposition is shown in Figure 3.18. The motion system is controlled by a computer program through a step motor controller to ensure thickness uniformity. One single wafer mounted on the sample holder is spinning while moving perpendicular to the super sonic jets in the horizontal direction.

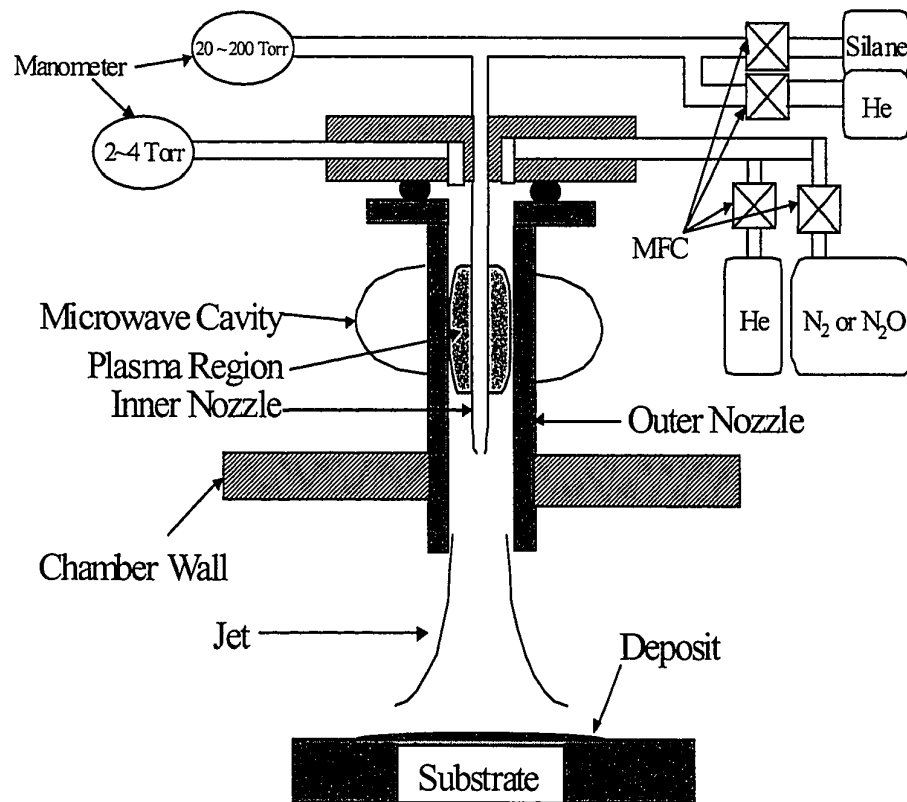


Figure 3.17 Schematic drawing of a concentric JVD source configuration for silicon nitride deposition.

Top View of JVD system

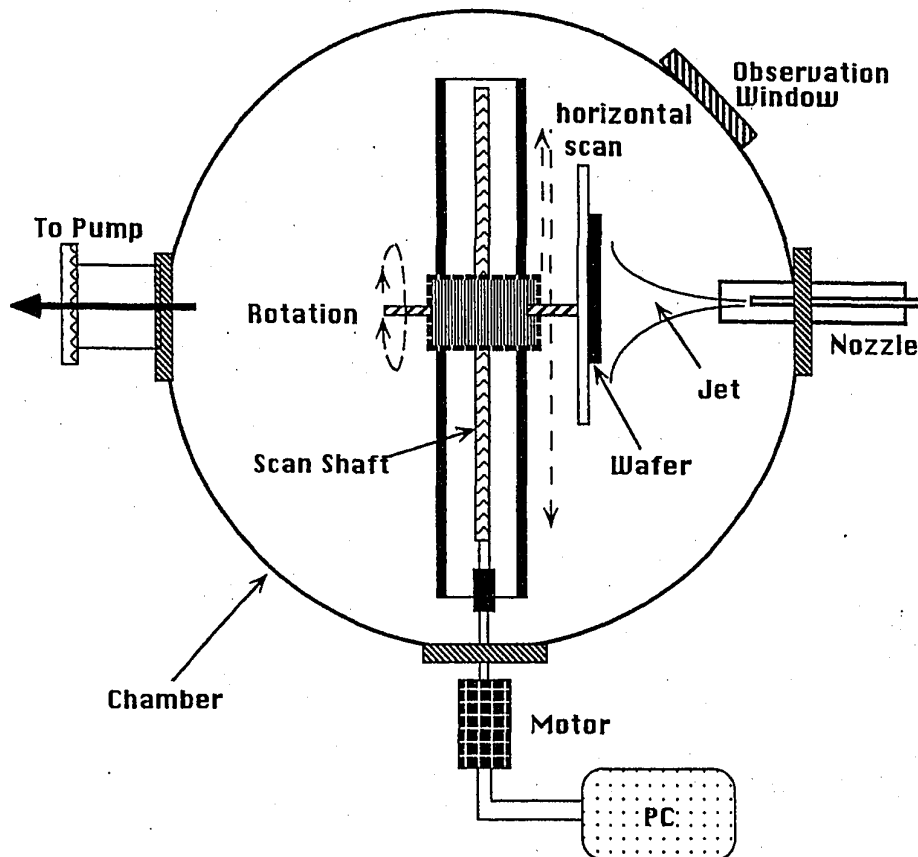


Figure 3.18 The top view of the JVD silicon nitride deposition system.

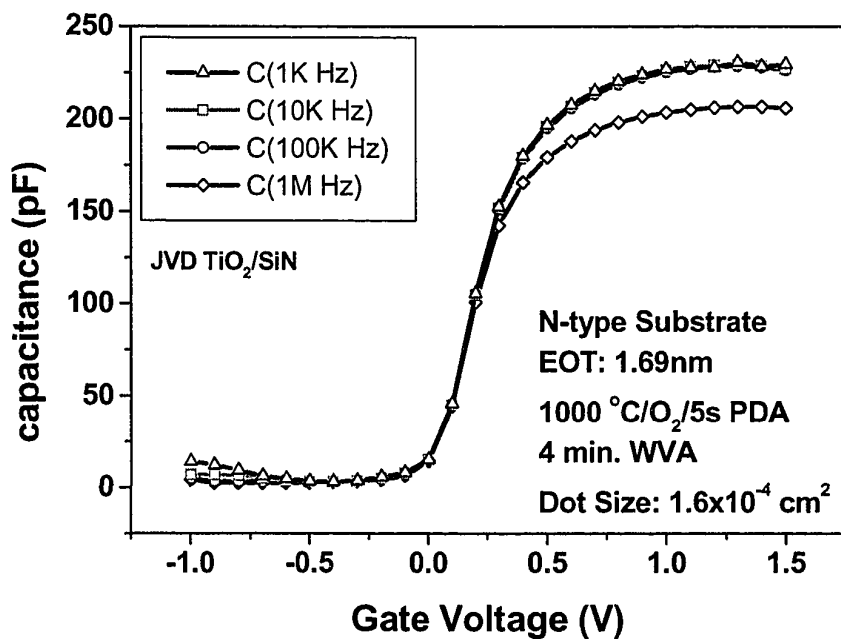
After the JVD silicon nitride deposition, the wafers are moved into another chamber for the metal oxide deposition.

The dielectric constant of the JVD silicon nitride is twice that of silicon dioxide. The bandgap of the JVD silicon nitride is about 5.19 eV, and it enjoys a barrier height of 2.15 eV over Si conduction band edge<sup>124</sup>. The JVD nitride has demonstrated excellent electrical properties, such as low leakage current, low interface trap density, low bulk trap density, low fixed charge density, high breakdown strength, negligible stress-induced leakage currents after stressing at high electric fields, and strong boron penetration resistance, on silicon and other semiconductors<sup>52,125</sup>. Both the n-channel MOSFETs and p-channel MOSFETs fabricated with the JVD silicon nitride as the gate dielectric exhibit comparable performance to the MOSFETs using thermal silicon dioxide as the gate dielectric. Moreover, the JVD silicon nitride is fully compatible with the current CMOS process flow. Therefore, the JVD silicon nitride is suitable for serving as a buffer layer for high-k materials.

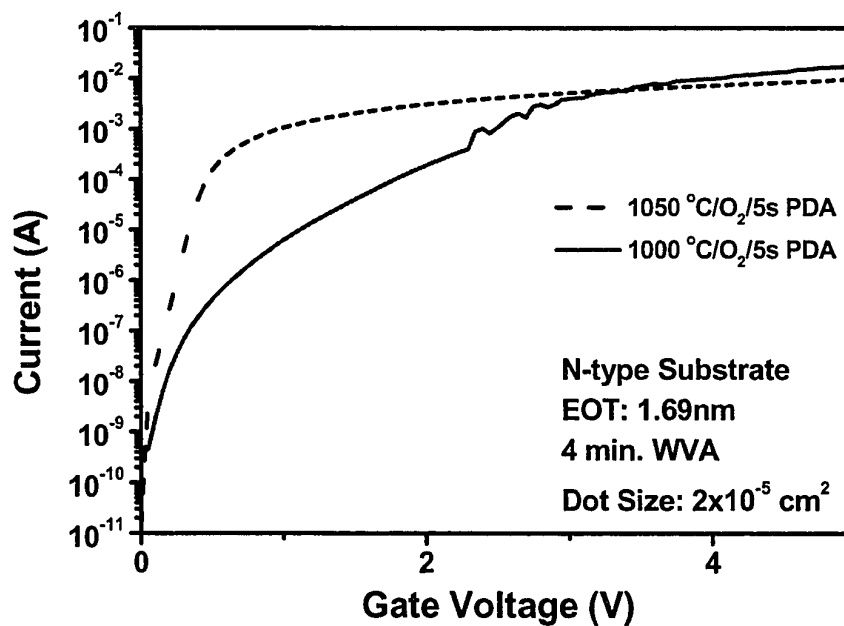
### ***3.2.2 JVD TiO<sub>2</sub>/SiN Gate Stack***

The JVD TiO<sub>2</sub>/SiN gate stack has demonstrated significantly lower gate leakage current than that of silicon dioxide, and comparable interface quality, reliability and electron mobility to those of silicon dioxide<sup>58</sup>. Moreover, the JVD TiO<sub>2</sub>/SiN gate stack also has demonstrated improved thermal stability over the JVD TiO<sub>2</sub> deposited on HF-last or N<sub>2</sub>O plasma treated Si substrates.

The JVD TiO<sub>2</sub> can not sustain an anneal at 800 °C or above, and such simple surface treatment as N<sub>2</sub>O plasma exposure before the JVD TiO<sub>2</sub> deposition is not sufficient to improve the thermal stability of the JVD TiO<sub>2</sub>. One way to improve the thermal stability of the JVD TiO<sub>2</sub> is incorporating Al into TiO<sub>2</sub>, as discussed in Section 3.1. Our study has also



(a)



(b)

Figure 3.19 (a) Multi-frequency C-V characteristics and (b) I-V characteristics of JVD TiO<sub>2</sub>/SiN gate dielectrics show good dielectric properties after annealing at 1000 °C. However, I-V results indicate that the gate stack shows the sign of breakdown after a 1050 °C anneal.

revealed that, by inserting an ultra-thin SiN layer, we are able to improve the electrical properties of the JVD TiO<sub>2</sub> after high temperature anneals. Unlike the JVD TiO<sub>2</sub> samples, the JVD TiO<sub>2</sub>/SiN gate stack exhibits good interface quality and low leakage current for RTA temperatures up to 1000 °C, as indicated in Figures 3.19(a) and 3.19(b). However, the film quality degrades significantly after a 1050 °C anneal. The sample that received a RTA at 1050 °C shows low-field breakdowns, as shown in Figure 3.19 (b), and no meaningful C-V characteristics can be obtained from the film after annealing at 1050 °C.

### ***3.2.3 JVD Ta<sub>2</sub>O<sub>5</sub>/SiN Gate Stack***

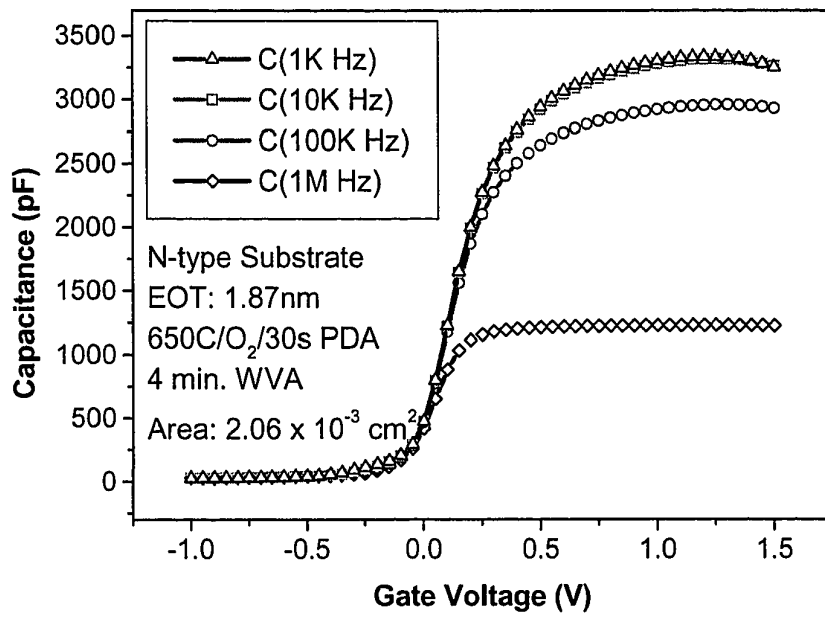
Tantalum Oxide (Ta<sub>2</sub>O<sub>5</sub>) has a long history of applications in the electronics industry, owing to its excellent electrical properties. Ta<sub>2</sub>O<sub>5</sub> serves as the insulating layer in some miniature capacitors used in hybrid circuits, and as an insulator in some DRAMs<sup>111</sup>. More recently, it has been explored to serve as the gate dielectric for Si CMOS<sup>126</sup>. However, its low thermal stability and low barrier height<sup>64</sup> could act as the show stopper. Inserting a high quality SiN layer between Ta<sub>2</sub>O<sub>5</sub> and Si can overcome these two major deficiencies of Ta<sub>2</sub>O<sub>5</sub>. Just like in the TiO<sub>2</sub> case, the JVD SiN provides an outstanding interface layer on Si, prevents possible reactions between Si and Ta<sub>2</sub>O<sub>5</sub> at elevated temperatures, and offers a sufficiently high barrier to block the thermionic currents at elevated temperatures.

The JVD Ta<sub>2</sub>O<sub>5</sub>/SiN gate stack has demonstrated excellent electrical properties, such as low interface trap density, low fixed trap density and high reliability after long time stressing at high electric fields. After process optimization, we have found that the JVD Ta<sub>2</sub>O<sub>5</sub>/SiN gate stacks demonstrate excellent electrical properties after PDA of 30s at 650 °C in oxygen and PMA in water vapor at 400 °C for 4 min.

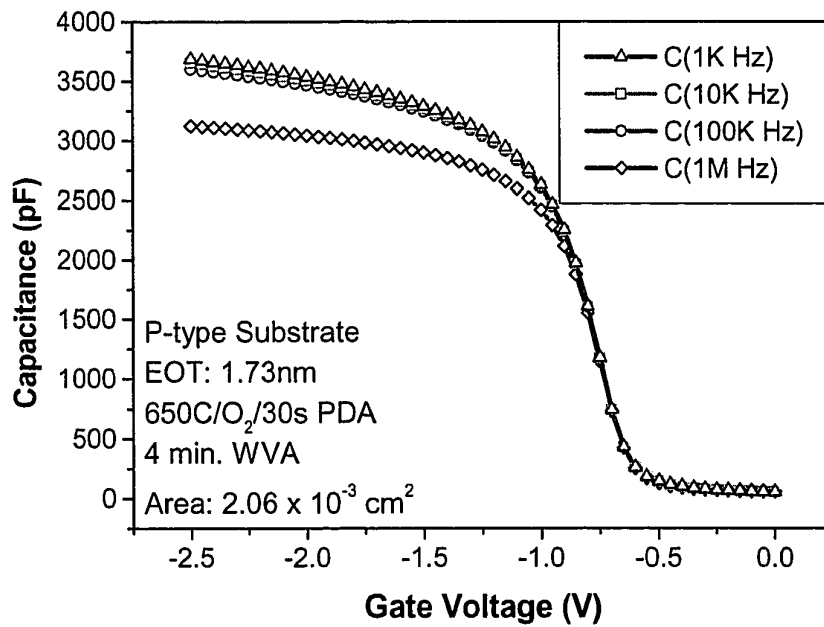
### **Electrical Properties of JVD Ta<sub>2</sub>O<sub>5</sub>/SiN Gate Stack**

For a gate dielectric with EOT smaller than 2 nm, multi-frequency C-V measurement is the primary method to evaluate its interface properties. In Figure 3.20, multi-frequency C-V characteristics of the JVD Ta<sub>2</sub>O<sub>5</sub>/SiN gate stacks deposited on both n-type and p-type Si substrates are shown. The films went through the optimized PDA and PMA for the Ta<sub>2</sub>O<sub>5</sub>/SiN gate stack. Aluminum was thermally evaporated to form the top electrodes and the back contacts of MOS capacitors. After excluding the quantum confinement effect, the extracted EOTs are 1.87 nm for the JVD Ta<sub>2</sub>O<sub>5</sub>/SiN film deposited on n-type Si substrate and 1.73 nm for the JVD Ta<sub>2</sub>O<sub>5</sub>/SiN film deposited on p-type Si substrate respectively. The almost perfect overlap of the C-V curves from inversion to accumulation for both the n-type and p-type MOS capacitors measured from 1K Hz to 100K Hz indicate excellent interface properties of the JVD Ta<sub>2</sub>O<sub>5</sub>/SiN gate stacks. The lower capacitance of the C-Vs measured at 1MHz in the accumulation region is due to series resistance. Moreover, the negligible flat-band voltage shifts for both the n-type and p-type JVD Ta<sub>2</sub>O<sub>5</sub>/SiN MOS capacitors suggest very low fixed charge densities.

As we discussed before, the most significant reason for implementing high-k gate dielectrics is to reduce the leakage current. The JVD Ta<sub>2</sub>O<sub>5</sub>/SiN gate dielectrics satisfy this requirement by reducing leakage currents significantly when compared to their silicon dioxide counterparts. Figures 3.21(a) and (b) show the very low leakage current densities of a 1.87 nm (EOT) JVD Ta<sub>2</sub>O<sub>5</sub>/SiN gate dielectric on n-type Si substrate under substrate injection, and another 1.73 nm (EOT) JVD Ta<sub>2</sub>O<sub>5</sub>/SiN gate dielectric on p-type Si under gate injection, respectively. The leakage current density of the 1.87 nm (EOT) JVD Ta<sub>2</sub>O<sub>5</sub>/SiN gate dielectric is less than 10<sup>-3</sup> A/cm<sup>2</sup> at 1 V, which is equivalent to the leakage current density of a 2.2 nm thermal silicon dioxide biased at 1V.

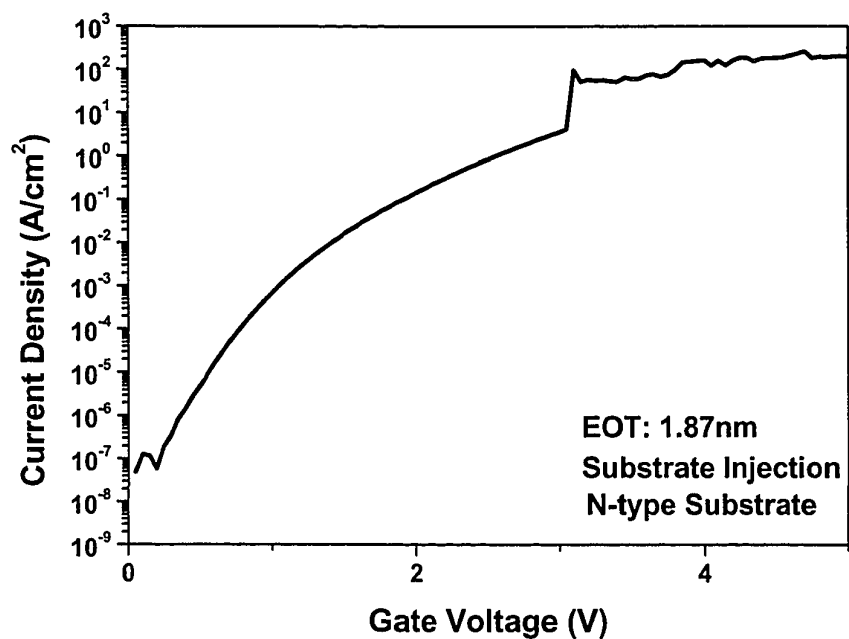


(a)

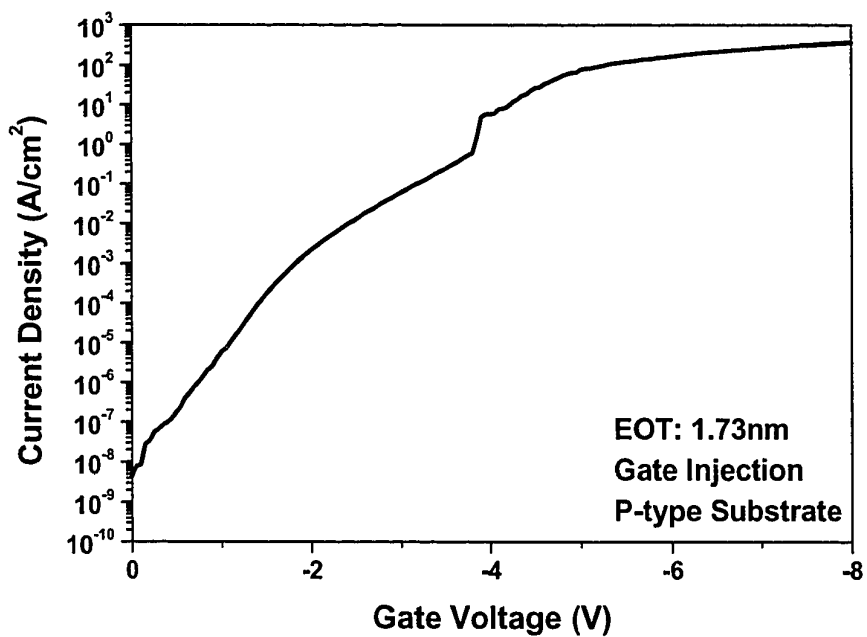


(b)

Figure 3.20 Excellent C-V Characteristics of MOS capacitors based on the JVD Ta<sub>2</sub>O<sub>5</sub>/SiN gate stacks (a) on n-type Si substrate and (b) on p-type Si substrate.



(a)



(b)

Figure 3.21 I-V Characteristics of JVD  $\text{Ta}_2\text{O}_5/\text{SiN}$  gate stacks (a) on n-type Si substrate under substrate injection and (b) on p-type Si substrate under gate injection.

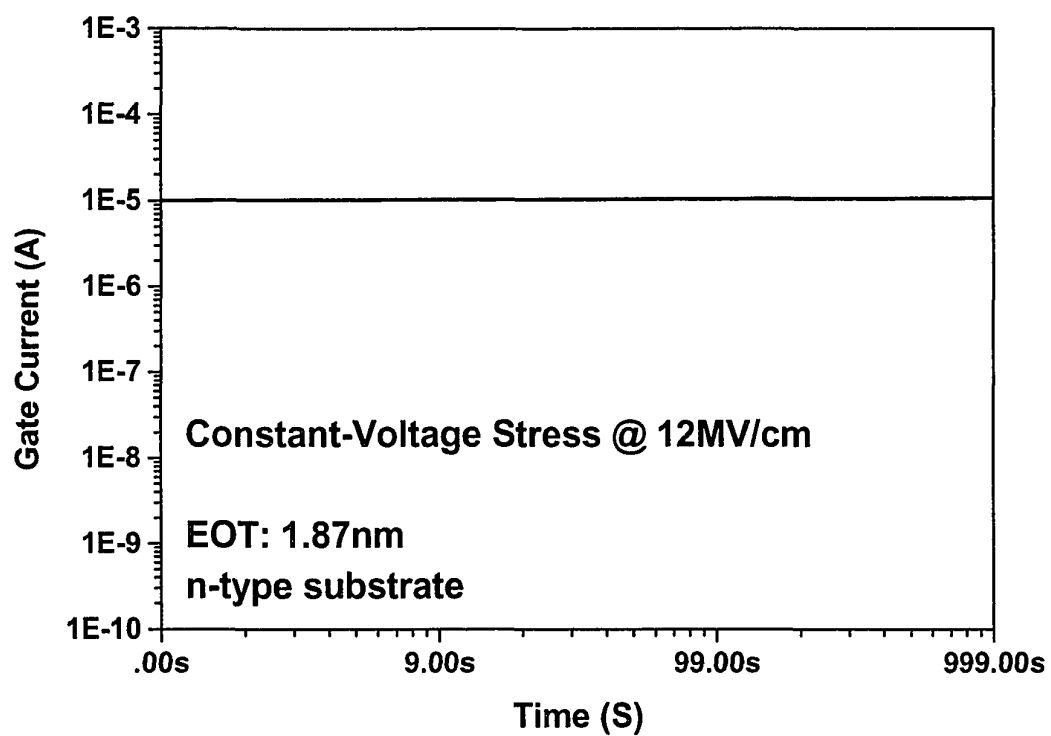


Figure 3.22 JVD Ta<sub>2</sub>O<sub>5</sub>/SiN gate stacks on n-type Si substrate under 12 MV/cm constant-voltage stressing.

The constant-voltage stressing result of the 1.87 nm (EOT) JVD Ta<sub>2</sub>O<sub>5</sub>/SiN gate dielectric on n-type Si substrate under substrate injection is shown in Figure 3.22. After stressing at the electric field of 12 MV/cm for 1,000 s, no soft breakdown or any other sign of degradation is observed. The leakage current only increases about 6% after such a long time of high electric field stressing, suggesting high dielectric strength of the JVD Ta<sub>2</sub>O<sub>5</sub>/SiN gate dielectric.

The results from both JVD TiO<sub>2</sub>/SiN and Ta<sub>2</sub>O<sub>5</sub>/SiN gate stacks have clearly demonstrated that, by employing the superb JVD SiN as the interface layer, one can produce gate stacks with outstanding interface quality, low leakage current, and other improved properties after high temperature anneals.

### 3.3 Correction for C-V Measurement

The gate dielectric thickness, or EOT, is one of the most important device parameters of an MOS capacitor or an MOSFET. And with the scaling down of gate dielectrics, the requirement for the accuracy of the EOT is becoming more stringent. The C-V method is a precise and most commonly used technique to determine the EOT. However, due to the high leakage current and serious resistance, C-V can no longer determine accurately the EOTs for ultra-thin gate dielectrics. Normally the EOT is determined from the accumulation capacitance or the inversion capacitance; however, the leakage currents are larger in accumulation and inversion than in other regions, which results in severe distortion of C-V characteristics in these two regions.

As we discussed in Chapter 1, for an ideal capacitor, the equivalent circuit can be described as two elements: a capacitor in series with a resistor, and the impedance of the two-element circuit can be presented as

$$Z = R_s + \frac{1}{j2\pi fC}, \quad (3.2)$$

where  $R_s$  is the series resistance,  $C$  is the capacitance, and  $f$  is the measurement frequency. Therefore, when the capacitor is measured by a LCR meter, the real part of the impedance is only influenced by the resistance of the series resistor, and the imaginary part of the impedance is only controlled by the capacitance of the gate capacitor.

However, it is no longer valid for a capacitor with an ultra-thin gate dielectric that has a large leakage current. The capacitor with an ultra-thin gate dielectric becomes a capacitor connected in parallel with a resistor in the equivalent circuit. Adding the series resistor, even in the simplest form, will require three components in the equivalent circuit, and the impedance of the three-element circuit can be described as

$$Z = \frac{R_c(1 - j2\pi fCR_c)}{1 + (2\pi fCR_c)^2} + R_s, \quad (3.3)$$

where  $R_s$  is the series resistance,  $R_c$  is the parallel resistance of the capacitor,  $C$  is the capacitance of the capacitor, and  $f$  is the measurement frequency. In this case, both the real part and the imaginary part of the impedance can be influenced by  $R_c$  and  $C$ . And neither the commonly used parallel mode nor the series mode in the C-V measurement represents the real capacitance of the ultra-thin gate dielectric anymore.

Usually the parallel circuit mode is the most commonly used equivalent circuit for C-V measurement. Therefore, the following discussion uses the parallel mode for C-V measurement. Figure 3.23 shows the typical multi-frequency C-V results measured from an ultra-thin JVD silicon nitride gate dielectric using the parallel mode. The C-V curves exhibit strong frequency dispersion, especially in the accumulation region. Furthermore, instead of the steady capacitance in accumulation, as presented by a normal MOS capacitor, the capacitance drops off when the capacitor is biased into deep accumulation, and this phenomenon is more severe at low frequencies.

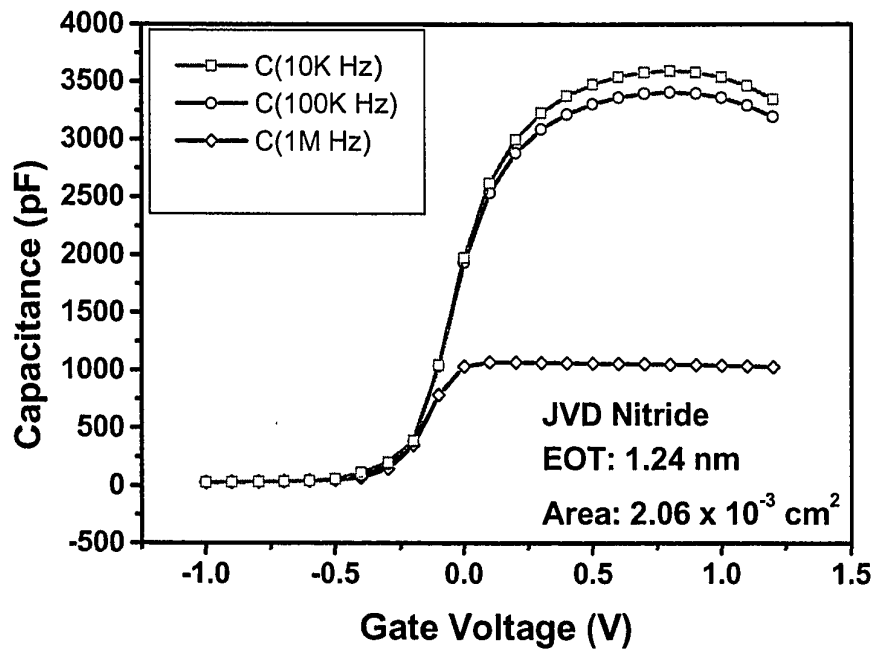


Figure 3.23 C-V characteristics of an ultra-thin JVD SiN gate dielectric display signs of the influence of the leakage current and series resistance.

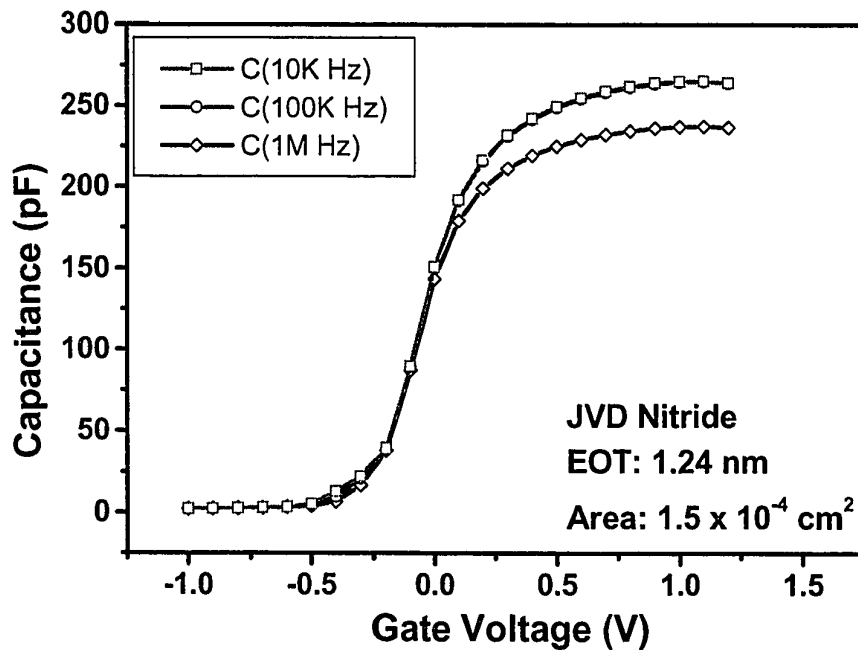


Figure 3.24 Compared to the data on Fig. 3.23, the adverse effects on C-V characteristics of an ultra-thin JVD SiN gate dielectric caused by leakage current and series resistance are minimized on a MOS capacitor with a smaller area.

The irregular C-Vs can be explained by the influence of the gate leakage current and series resistance. In accumulation, the tunneling leakage current increases exponentially with the gate voltage, which means that  $R_c$  decreases exponentially with the gate voltage. According to Equation 3.3, if  $C$  remains unchanged, the rapid decrease of  $R_c$  results in a drop off of the measured capacitance. Moreover, at high frequencies, the displacement current dominates. Therefore, the leakage current is less influential than that at low frequencies, causing the measured capacitance in accumulation not to drop off as rapidly as that at low frequencies. However, because the impedance of the gate capacitor becomes lower at higher frequencies, and the impedance of the series resistor does not change, when compared to those at low frequencies, the series resistance becomes more dominant, and a larger portion of the applied AC voltage drops across the series resistor. Therefore, the measured capacitance is smaller at high frequencies when compared to that at low frequencies.

Not only does the C-V curve of an ultra-thin gate dielectric display frequency dependence, it also exhibits area dependence. The capacitance of a capacitor can be expressed as

$$C = \frac{3.9S\epsilon_0}{d}, \quad (3.4)$$

where  $s$  is the area of the capacitor, and  $d$  is the EOT of the capacitor. The capacitance is proportional to the area of the capacitor, and inversely proportional to the thickness of the capacitor. Moreover, the resistance of a capacitor is inversely proportional to the area of the capacitor, and increases exponentially with EOT. Therefore, a capacitor with a small area and a small EOT resembles a capacitor with a large area and a big EOT in the equivalent circuit. The influence of the leakage current can be reduced by measuring a capacitor with a small area, and the observed abnormal behavior is minimized for a capacitor with a small area. Figure 3.24 shows the multi-frequency C-V curves for a

capacitor with an area less than one tenth of that of the capacitor shown in Figure 3.23. It is clear the C-V curves for the capacitor with the smaller area are more similar to the normal C-V curves. In principle, we can use a sufficiently small capacitor to obtain accurate results. However, it comes at a price as well. The small area increases the relative error in the area measurement, and reduces the signal to noise ratio. Thus, it reduces the level of precision in the measurement.

In order to accurately measure C-V, several methods have been developed to solve this critical problem. Because the gate leakage current is much smaller in depletion than that in accumulation or inversion, in order to reduce the influence of leakage current in C-V measurement, one technique uses a least square fit of the portion of C-V between depletion and accumulation to a theoretical model to extract the gate oxide thickness<sup>84</sup>. Another method uses two C-V measurements at two different frequencies, and a three-element equivalent circuit to extract the real C-V curve<sup>85</sup>. Two C-V measurements at two frequencies could provide us with 2 capacitance data and two conductance data at each voltage point. Therefore we have enough independent equations to derive C, R<sub>c</sub> and R<sub>s</sub>. Using the parallel measurement mode, where the measured capacitance and resistance are connected in parallel, we can derive the real gate capacitance from the commonly used three-element circuit model as:

$$C_{real\_gate} = \frac{f_1^2 C_{m1} [1 + (\frac{1}{2\pi f_1 R_{m1} C_{m1}})^2] + f_2^2 C_{m2} [1 + (\frac{1}{2\pi f_2 R_{m2} C_{m2}})^2]}{f_1^2 - f_2^2}, \quad (3.5)$$

where C<sub>m1</sub>, R<sub>m1</sub>, C<sub>m2</sub>, and R<sub>m2</sub> are measured capacitance and resistance at various frequencies; f<sub>1</sub> and f<sub>2</sub> are two frequencies used to do the measurement.

Both methods enjoy certain levels of success. However, both of them fail to solve the frequency dispersion in the C-V measurement in many cases. For Hauser's method<sup>84</sup>, if the part of C-V between depletion and accumulation is affected by leakage current as well, as

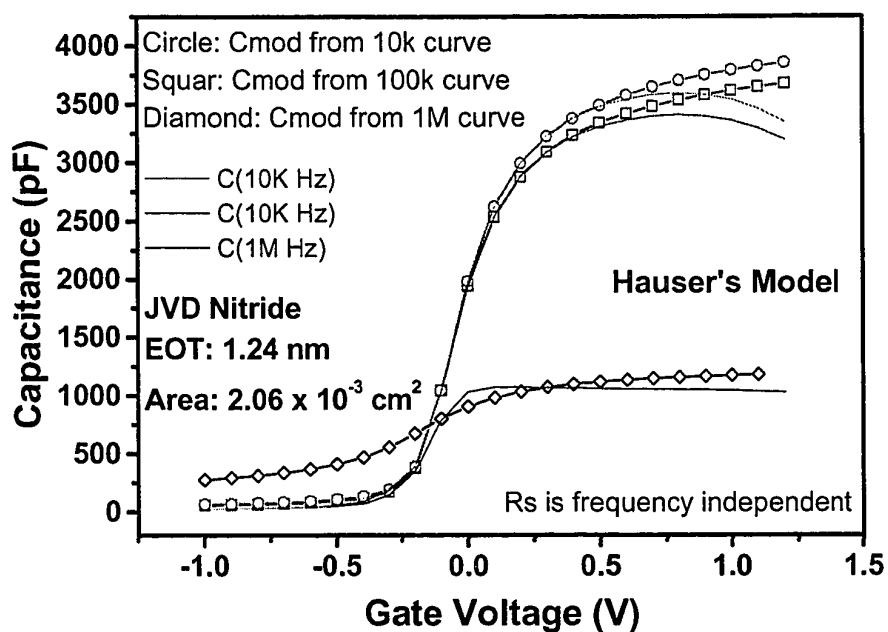


Figure 3.25 Hauser's model<sup>84</sup> fails to correct the adverse effects on C-V characteristics of an ultra-thin JVD SiN gate dielectric caused by leakage current and series resistance.

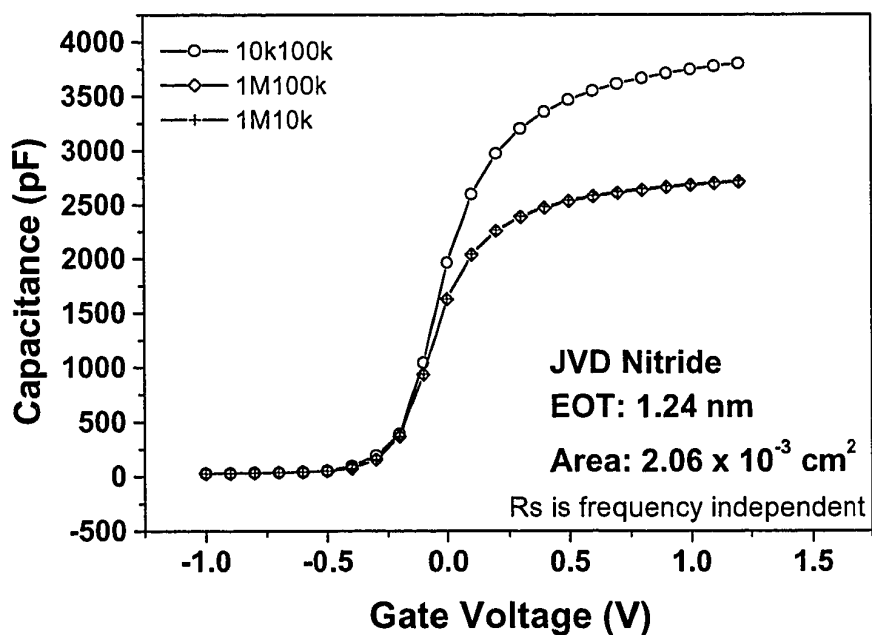


Figure 3.26 The three-element equivalent circuit fails to correct the adverse effects on C-V characteristics of an ultra-thin JVD SiN gate dielectric caused by leakage current and series resistance.

shown in Figure 3.25, this method loses its effectiveness. Therefore, different EOT values are extracted by using C-V curves measured at different frequencies. The dual-frequency C-V measurement using the three-element equivalent circuit becomes less useful for certain cases too, as shown in Figure 3.26. The extracted C-V from the C-V curves measured at 10K Hz and 100K Hz fails to align with the extracted C-V from the C-V curves measured at 10K Hz and 1M Hz, or 100k Hz and 1M Hz, for both the devices with the areas of  $2.06 \times 10^{-3} \text{ cm}^2$  and  $1.5 \times 10^{-4} \text{ cm}^2$ . In order to solve this problem, some employed a complicated grid structure<sup>127</sup>. It is more useful than the two methods mentioned above. However, it is a complicated and time-consuming method. Therefore, it is hard to implement.

A simple and effective 4-element circuit model was developed during the course of this thesis study, as shown in Figure 3.27, which significantly expands the usage of C-V measurement without adding significant amount of calculation. In the three-element model, we only acknowledge the existence of the series resistance. However, in reality, in an Alternative Current (AC) circuit, not only should we consider the series resistance, we should also include the capacitance component. An RC network is a much better description of the real circuit, especially in most cases in which the contact capacitance cannot be ignored<sup>128,129</sup>.

In the 4-element circuit, the impedance of the equivalent circuit can be described as the following,

$$Z = \frac{R_c(1 - j2\pi fCR_c)}{1 + (2\pi fCR_c)^2} + \frac{R_s(1 - j2\pi fC_sR_s)}{1 + (2\pi fC_sR_s)^2}, \quad (3.6)$$

where  $R_s$  is the series resistance,  $R_c$  is the resistance of the capacitor,  $C$  is the capacitance of the capacitor,  $C_s$  is the capacitor component in the contact circuit, and  $f$  is the measurement frequency. For the dual-frequency C-V measurement, we have 4 independent data points, including two capacitance data and two conductance data for each voltage point. Therefore, we have 4 independent equations for deriving four unknowns,  $C$ ,  $R_c$ ,  $C_s$ , and  $R_s$ .

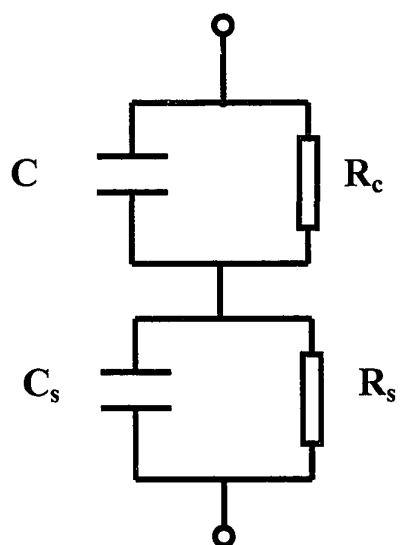
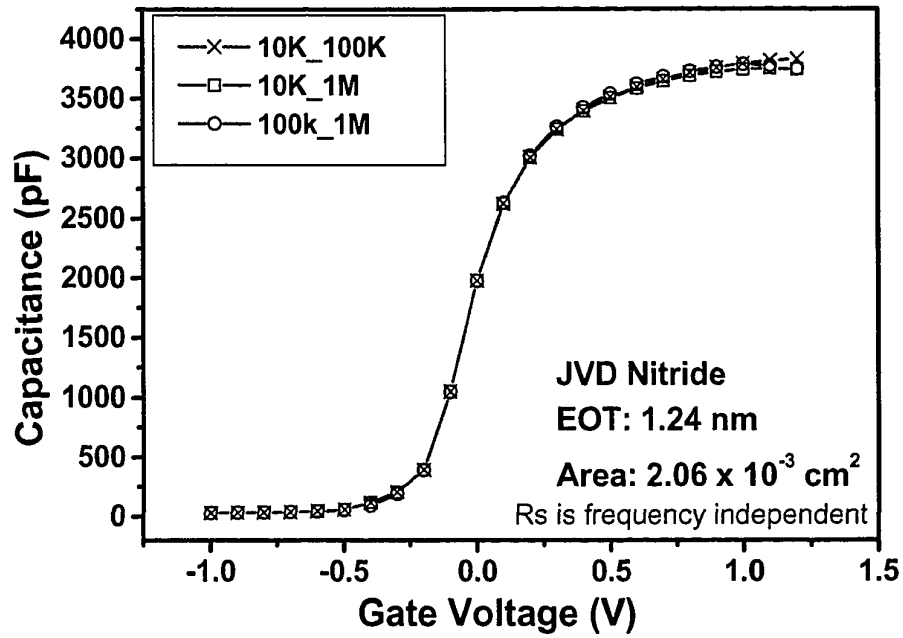
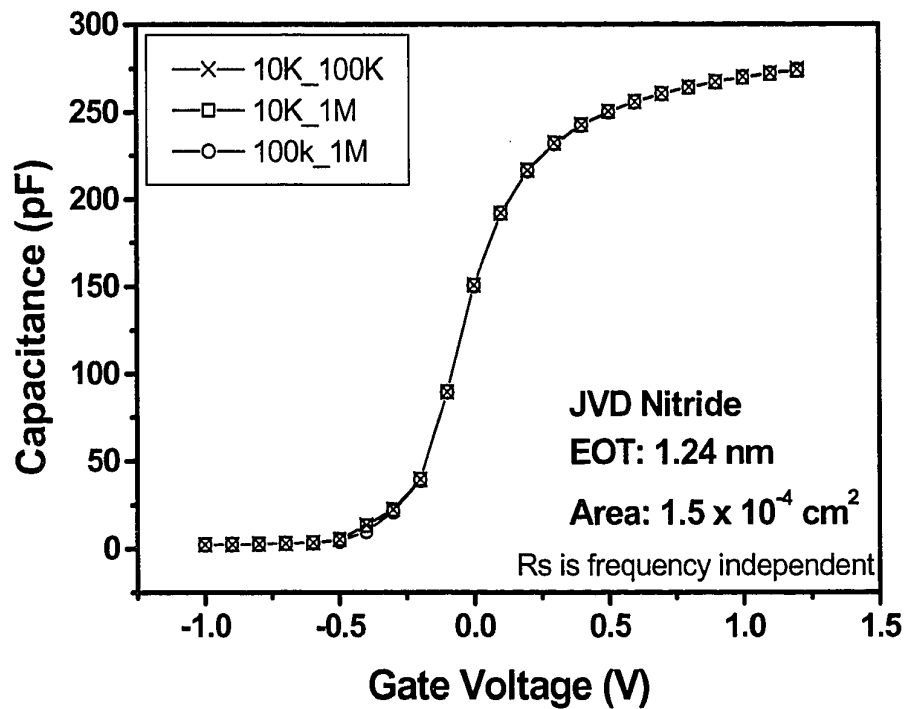


Fig. 3.27 Four-element equivalent circuit model



(a)



(b)

Figure 3.28 The four-element equivalent circuit successfully corrects the adverse effects on C-V characteristics of ultra-thin JVD SiN gate dielectrics caused by leakage current and series resistance on (a) an MOS capacitor with a relative large area and (b) an MOS capacitor with a relative small area.

The analytical form of  $C$  cannot be derived directly from these equations. However, the numerical solutions can be reached. A program coded in Mathematica<sup>®</sup> is used to solve these equations numerically.

Figure 3.28 (a) shows the corrected C-V curve extracted using the 4-element circuit from the multi-frequency C-V curve measured on a device with an area of  $2.06 \times 10^{-3} \text{ cm}^2$ . No matter whether one uses the combination of C-V curves measured at 10 k Hz and 100 KHz, or 10 KHz and 1MHz, or 10 KHz and 1M Hz, all the extracted C-Vs perfectly align with each other, demonstrating significant improvement over the Hauser's method or the three-element equivalent circuit method. Figure 3.28 (b) presents the corrected C-V curve extracted from a MOS capacitor with an area of  $1.5 \times 10^{-4} \text{ cm}^2$  using the four-element circuit. This result is consistent with that from the large area device. Obviously after using the dual-frequency and 4-element equivalent circuit, the frequency dispersion, area discrepancy, and drop of capacitance in the accumulation region could be corrected, and the C-V curve shows normal behavior.

The dual-frequency C-V method coupled with the four-element method clearly demonstrates its superiority over either Hauser's method or the three-element circuit model, as it solves the problems associated with the area dependence, frequency dependence, and capacitance drop in deep accumulation in the C-V measurement of ultra-thin gate dielectrics without adding significant amount of work.

### 3.4 Chapter Summary

The JVD  $\text{TiO}_2$  has some excellent electrical properties; however, its low thermal stability and low crystallization temperature raise serious concerns for its application as the gate dielectric for Si CMOS. We have demonstrated that (1) by incorporating aluminum into the JVD  $\text{TiO}_2$ , the crystallization temperature is increased and the electrical properties after high temperature anneals are improved without sacrificing the dielectric constant significantly; (2) inserting an ultra-thin JVD silicon nitride buffer layer between  $\text{TiO}_2$  and Si also improves the properties of the gate stack after high temperature anneals. Moreover, the JVD  $\text{Ta}_2\text{O}_5/\text{SiN}$  gate stack also demonstrates outstanding interface quality, low leakage current, and high dielectric strength. The effects of nano-crystallization on gate dielectric properties haven been investigated, and we have found that the nano-crystallization results in considerable degradation of transconductance and reliability. Finally, a new dual-frequency C-V measurement technique together with a four-element equivalent circuit is introduced, which extends the effectiveness of C-V measurement, and is better suited than Hauser's method and a three-element circuit model to deal with the problems of area dependence, frequency dependence, and capacitance drop in deep accumulation in the C-V measurement of ultra-thin gate dielectrics.

## Chapter 4

### Barrier Heights of High-k Dielectrics

The major motivation of employing high-k gate dielectrics to replace silicon dioxide is to reduce leakage currents in ultra-thin gate dielectrics without compromising the gate capacitance per unit area. If we assume that the tunneling current is the dominant conduction mechanism in high-k gate dielectrics, then under a given applied voltage, the tunneling current is decided by the thickness and barrier height of a gate dielectric. Usually gate leakage currents of different gate dielectrics are compared at the same EOT. Therefore, in order to model the tunneling current of a high-k gate dielectric, we must possess the knowledge of its dielectric constant and barrier height in addition to its thickness. Though determining the dielectric constant of an ultra-thin film is complicated by the presence of interfacial layers at the Si/high-k dielectric interface and the gate electrode/high-k gate dielectric interface, determining the barrier height of a high-k gate dielectric is a more difficult task.

In this chapter, the barrier heights of various high-k materials, such as Ta<sub>2</sub>O<sub>5</sub>, TiO<sub>2</sub>, ZrO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, and Tungsten metal gate are determined. The current transport mechanisms in Ta<sub>2</sub>O<sub>5</sub>/SiN and TiO<sub>2</sub>/SiN gate stacks over a wide temperature range are thoroughly investigated. We have found that a large bandgap does not guarantee a high barrier height, and the band alignment of a high-k gate dielectric to Si is vital.

## ***4.1 Current Conducting Mechanisms in Dielectrics***

In an ideal dielectric, there should be no current conduction. However, in reality, current conduction is not extinct even in thick dielectric films. Carriers always find various ways to travel through dielectric films. Moreover, the current normally grows rapidly with the decrease of dielectric thickness and the increase of applied electric field and temperature. The conduction mechanisms in dielectrics have been studied extensively, and many conduction mechanisms, such as tunneling, Schottky emission, and Frenkel-Poole conduction, have been identified and studied. We will discuss these conduction mechanisms in this section.

### ***4.1.1 Tunneling***

Tunneling, which we have introduced briefly in Chapter 1, is the most fundamental conduction mechanism, and it presents the lowest leakage current that can be achieved in a dielectric. As a fundamental quantum physics problem, electron tunneling through an energy barrier has been studied since the birth of quantum mechanics. Sommerfield and Bethe<sup>44</sup> conducted the first theoretical study on it. Since then, many more physicists, such as Holm<sup>130</sup> and Simmons<sup>43</sup>, have continued to work on this problem. Based on these works,

a generalized formula for tunneling current through an arbitrary barrier, as illustrated in Figure 4.1(a), can be derived as<sup>43</sup>,

$$J = J_0 \{ \bar{\phi} \exp(-A\bar{\phi}^{\frac{1}{2}}) - (\bar{\phi} + eV) \exp[-A(\bar{\phi} + eV)^{\frac{1}{2}}] \} \quad (4.1)$$

where,  $\bar{\phi} = \frac{1}{t} \int_0^t \phi(x) dx$ , is the average barrier height of an arbitrary-shape barrier  $\phi(x)$ ;

$t$  is the tunneling distance or the thickness of the barrier;

$$J_0 = q / 2\pi\hbar(\beta\hbar)^2 ;$$

$q$  is the electron charge;

$\hbar$  is the Plank's constant;

$\beta$  is a correction factor with a value close to 1;

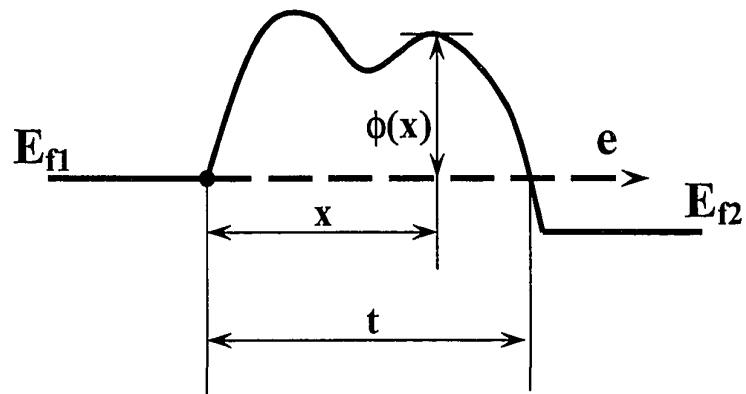
$$A = (4\pi\beta\hbar / \hbar)(2m^*)^{1/2} ;$$

$m^*$  is the effective electron mass in the insulator;

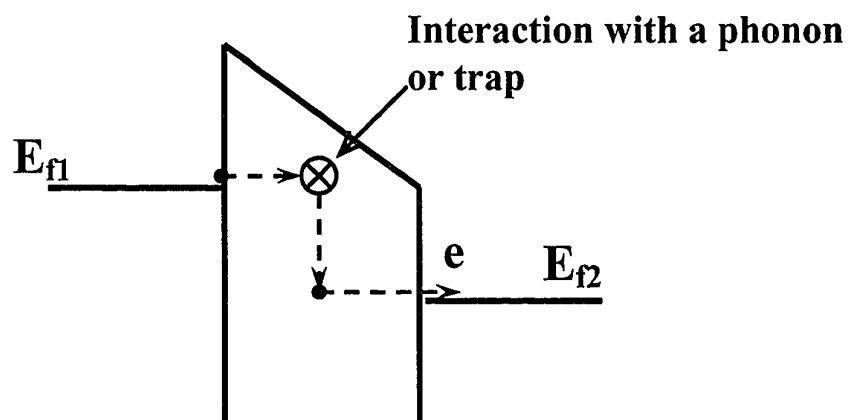
$V$  is the voltage drop across the dielectric layer; i.e. the dielectric voltage.

In order to derive Equation 4.1, the electron tunneling probability is calculated by using the Wentzel-Krammers-Brillouin (WKB) approximation<sup>43</sup> with a parabolic  $E$ - $k$  relationship in the oxide forbidden band.

As we discussed in Chapter 1, tunneling in oxide can be divided into two modes, direct tunneling and Fowler-Nordheim tunneling. Direct tunneling happens in the low electric fields region, where the oxide voltage is smaller than the barrier height, and electrons travel through a trapezoidal barrier to move into the other electrode directly, which is described by Equation 1.2. Fowler-Nordheim tunneling occurs in the high electric fields region, where the oxide voltage is larger than the barrier height, and electrons transport through a triangular barrier to tunnel into the oxide conduction band first, and then travel towards the other electrode, which is described by Equation 1.3. In contrast to



(a)



(b)

Figure 4.1 Schematic representations of (a) tunneling through an arbitrary barrier and (b) inelastic tunneling.

trap-assisted currents, in either mode, the tunneling current is a weak function of temperature.

The tunneling current is a good source to obtain important information of a barrier height. If the effective mass of electron in an oxide and its thickness are known, the barrier height can be extracted from the tunneling current.

Moreover, as shown in Figure 4.1(b), the tunneling process can be enhanced by interactions with traps and phonons. The trap- or phonon-assisted tunneling process is known as inelastic tunneling. The energy spectrum of the inelastic tunneling current, Inelastic Electron Tunneling Spectroscopy (IETS)<sup>131</sup>, is a very useful tool to study traps and phonons in ultra-thin dielectrics.

#### ***4.1.2 Other Conduction Mechanisms in Dielectrics***

For a perfect insulator at low temperature, tunneling should be the dominant conduction mechanism. However, at elevated temperatures, due to the limited size of barriers and defects in oxides, other, thermally excited, current transport mechanisms, such as Schottky emission or Frenkel-Poole emission, may emerge as the dominant conduction mechanisms. Normally microchips work at elevated temperatures. Moreover, high-k materials usually have a smaller barrier and a larger trap density than silicon dioxide. Therefore, it is extremely important to study the thermally excited conduction mechanisms in high-k dielectrics. (Tunneling and other conduction mechanisms are summarized in Table 4.1.)

##### **Schottky Emission**<sup>18</sup>

Schottky emission or thermionic emission is a carrier transport mode through dielectric, in which the thermally excited carriers overcome the barrier at the metal-

insulator interface or semiconductor-insulator interface and transport to the other side of the insulator, as described in Figure 4.2. If the carriers are electrons, the energy distribution of them is described by the Fermi-Dirac statistics. At an elevated temperature, the energy distribution of electrons tilts to the high-energy side. Therefore, at a sufficiently high temperature, a big portion of electrons in metal or semiconductor are excited to energy levels higher than the barrier height at the metal-insulator or semiconductor-insulator interface, and these high-energy electrons can escape over the barrier. In contrast to the tunneling mechanism, the Schottky emission current is a strong function of temperature. Moreover, as shown in Table 4.1, the Schottky emission current is a strong function of electric field too, which is due to the barrier lowering effect caused by the image force, as shown in Figure 4.3. The amount of Schottky barrier lowering or image force lowering,  $\Delta\phi$ , is written as

$$\Delta\phi = \sqrt{\frac{qE}{4\pi\epsilon_s}}. \quad (4.2)$$

where  $q$  is the electron charge,  $E$  is the electric field, and  $\epsilon_s$  is the high-frequency dielectric constant in the image force region.

Schottky emission may become the dominant conduction mechanism in gate dielectrics with low barrier heights at high temperatures. By analyzing the variation of Schottky emission current as a function of temperature and electric field, we are able to derive the barrier height at the metal-insulator or semiconductor insulator interface.

### **Frenkel-Poole Emission**<sup>18</sup>

Frenkel-Poole emission is another common current transport mechanism. The physics of Frenkel-Poole emission is very similar to that of Schottky emission. However, Frenkel-Poole emission is a trap-assisted current transport mechanism. In a trap-rich

insulator, the trapped electrons can be thermally excited into the conduction band and transport to the other side of the insulator in the presence of a large electric field, as shown in Figure 4.4(a). Just like that in Schottky emission, the energy distribution of the trapped electrons shifts to the high-energy end, and the depth of the trap potential well is also lowered by the image force at the enhanced electric field. Therefore, the Frenkel-Poole emission is also a strong function of both temperature and electric field. Except for substituting the barrier height at the interface by the depth of the trap potential well, the mathematical formula for Frenkel-Poole emission is almost identical to that of Schottky emission. For high-k gate dielectrics, with the presence of high-density traps, Frenkel-Poole emission becomes the major conduction mechanism in many cases.

At an extremely high temperature, the trapped carriers can be thermally excited out of traps even at low electrical fields and hopping from one trap to another trap, as shown in Figure 4.4(b). This process resembles the ohmic conduction characteristics. Therefore, it is named Ohmic conduction<sup>18</sup>.

Various conduction mechanisms exist in the current transport in a dielectric simultaneously. However, for a dielectric, different conduction mechanisms may dominate at different temperatures and electric fields. And these thermally excited conduction mechanisms may significantly affect CMOS circuits using high-k gate dielectrics operating at elevated temperatures.

| <i>Mechanism</i>              | <i>Mathematical Formula</i>                                                        | <i>Voltage and Temperature Dependence</i>  |
|-------------------------------|------------------------------------------------------------------------------------|--------------------------------------------|
| <i>FN Tunneling</i>           | $J \sim E^2 \exp \left[ -\frac{4\sqrt{2m^*} (q\phi_b)^{3/2}}{3q\hbar E} \right]$   | $\sim V^2 \exp(-b/V)$                      |
| <i>Schottky Emission</i>      | $J = A^* T^2 \exp \left[ \frac{-q(\phi_b - \sqrt{qE/4\pi\epsilon_i})}{kT} \right]$ | $\sim T^2 \exp(+a\sqrt{V}/T - q\phi_b/kT)$ |
| <i>Frenkel-Poole Emission</i> | $J \sim E \exp \left[ \frac{-q(\phi_b - \sqrt{qE/\pi\epsilon_i})}{kT} \right]$     | $\sim V \exp(+2a\sqrt{V}/T - q\phi_b/kT)$  |
| <i>Ohmic</i>                  | $J \sim E \exp(-\Delta E_{ac}/kT)$                                                 | $\sim V \exp(c/T)$                         |

\*  $J$  = current density,  $E$  = electric field,  $\epsilon_i$  = insulator dielectric constant,  $m^*$  = effective mass,  $d$  = insulator thickness,  $\Delta E_{ac}$  = activation energy,  $\phi_b$  = energy barrier height,  $k$  = Boltzman's constant, and  $V$  = insulator voltage.

Table 4.1 Basic Conduction Mechanisms in Insulators<sup>18</sup>

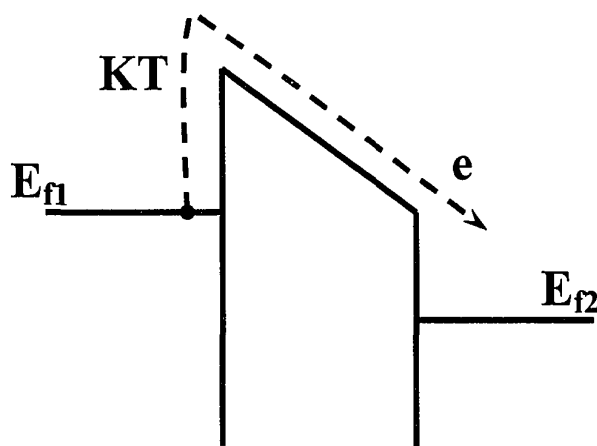


Figure 4.2 Schematic representation of Schottky emission.

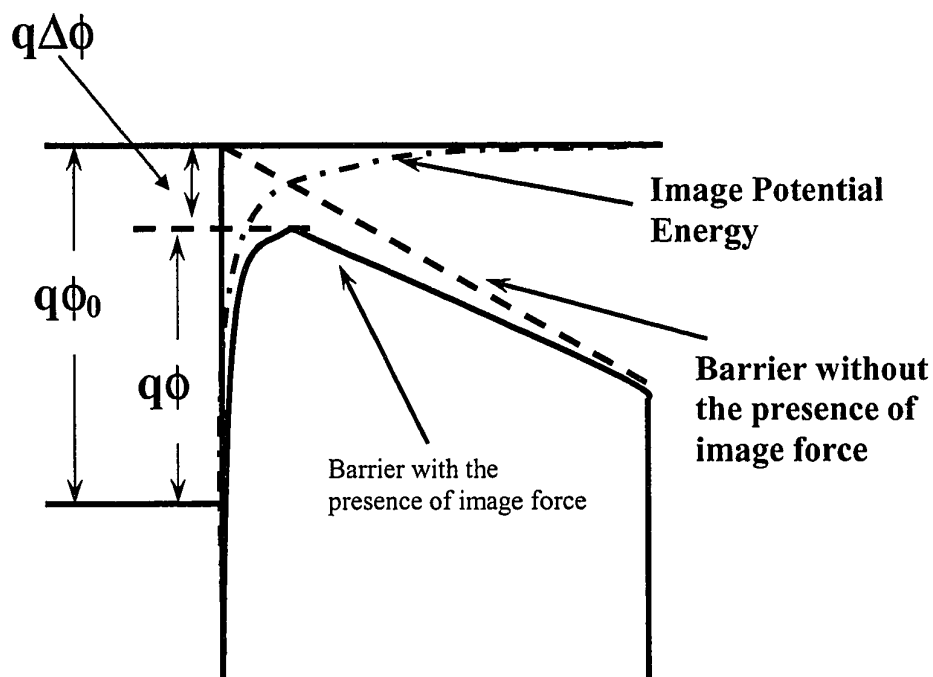
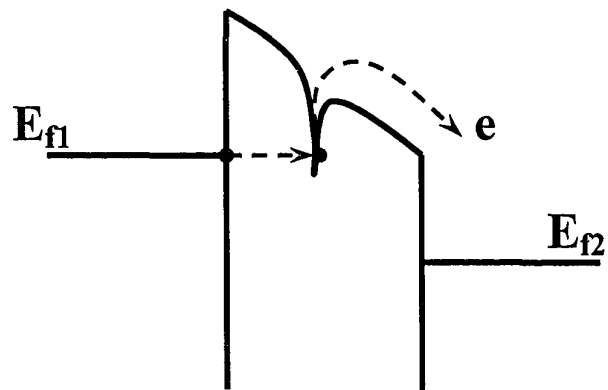
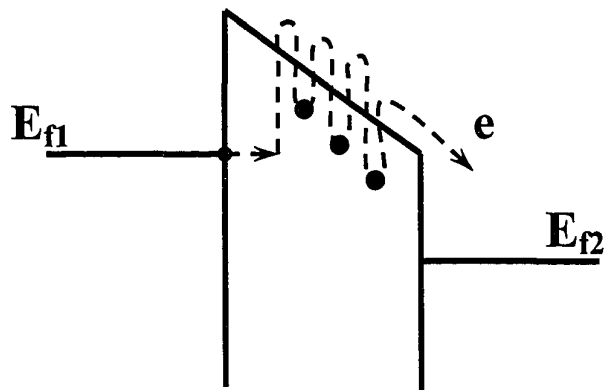


Figure 4.3 Schematic representation of the barrier lowering effect caused by the image force.



(a)



(b)

Figure 4.4 Schematic representations of (a) Frenkel-Poole emission and (b) Ohmic conduction.

## 4.2 Barrier Heights and Conduction Mechanisms in $\text{Ta}_2\text{O}_5$ and $\text{TiO}_2$

As presented in Chapter 2, both the  $\text{Ta}_2\text{O}_5/\text{SiN}$  stack and  $\text{TiO}_2$  or  $\text{TiO}_2/\text{SiN}$  stack deposited by the JVD process have demonstrated low densities of interface traps and dielectric charges, low leakage currents, and high reliability, and are seriously considered as candidates for advanced CMOS gate dielectric applications. Besides the concerns of thermal stability of these high-k materials, another major concern is the relatively low bandgaps of these metal oxides (4.65 eV and 3.25 eV, respectively, for  $\text{Ta}_2\text{O}_5$  and  $\text{TiO}_2$ ), which are significantly lower than those of  $\text{SiO}_2$  and  $\text{Si}_3\text{N}_4$ . Such low bandgaps may result in barrier heights that are too low to block the thermionic currents at elevated temperatures. Furthermore, adverse band alignments can make barrier heights even lower.

Therefore, it is meaningful to study the temperature dependence of gate currents in thin  $\text{Ta}_2\text{O}_5$  and  $\text{TiO}_2$  films. The study was conducted (1) to study the conduction mechanisms and band alignments of thin  $\text{Ta}_2\text{O}_5$  and  $\text{TiO}_2$  films, and (2) to determine whether the gate leakage current is tolerable at high temperatures for either of these high-k oxides. The I-V characteristics of these oxides were measured and analyzed over a wide temperature range, from 25 to 400  $^{\circ}\text{C}$ , in order to extract useful information of barrier height or conduction mechanism. The currents in  $\text{Ta}_2\text{O}_5$  samples exhibit stronger temperature dependence than those in  $\text{TiO}_2$  samples, especially at high fields, mainly due to a much smaller electron barrier height of  $\text{Ta}_2\text{O}_5$  over Si than that of  $\text{TiO}_2$  over Si.

$\text{Ta}_2\text{O}_5$  and  $\text{TiO}_2$  films were deposited by the JVD process on p-type (100) Si wafers that were covered by an ultra-thin layer of SiN as an interfacial buffer layer to prevent possible reactions between Si and  $\text{Ta}_2\text{O}_5$  or Si and  $\text{TiO}_2$ . The SiN buffer layers (~1.5 nm of physical thickness) were deposited by the JVD method at room temperature, and a post-

deposition anneal was performed at 600 °C in N<sub>2</sub> for 10s. The Ta<sub>2</sub>O<sub>5</sub> layer (~ 9 nm of physical thickness) was deposited at 300 °C, followed by a post-deposition anneal at 600 °C in O<sub>2</sub> for 20s. The TiO<sub>2</sub> layer (~ 12 nm of physical thickness) was deposited at 220 °C, followed by a post-deposition anneal at 600 °C in O<sub>2</sub> for 20s. Al was evaporated and patterned by photolithography to form the top electrode of MOS capacitors. The structures of both samples are shown in Figure 4.5. The excellent device-quality ultra-thin SiN buffer layer for both Ta<sub>2</sub>O<sub>5</sub> and TiO<sub>2</sub> films was processed the same way, and possess substantially the same quality. Moreover, because of the much smaller thickness of SiN buffer layer compared to that of either Ta<sub>2</sub>O<sub>5</sub> or TiO<sub>2</sub> layer, the leakage currents are limited by the metal oxide layers instead of the ultra-thin SiN buffer layer, and the differences between the two samples, to be discussed later, should be attributable to the metal oxides. Therefore, the I-V characteristics of either sample represent the current transport characteristics of metal oxide rather than that of SiN, while the SiN buffer layer provides an excellent interface with Si. The physical thicknesses of the gate dielectrics were determined by ellipsometry, and their EOT values were calculated from C-V curves by considering quantum corrections. The C-V data indicate low densities of interface traps and dielectric charges in both samples, and the extracted equivalent oxide thickness is ~2.5 nm for the Ta<sub>2</sub>O<sub>5</sub> sample and ~2.2 nm for the TiO<sub>2</sub> sample.

Figure 4.6 shows the I-V characteristics of a negatively biased Al/Ta<sub>2</sub>O<sub>5</sub>/SiN/Si capacitor from 27 °C to 400 °C, and Figure 4.7 shows those of a negatively biased Al/TiO<sub>2</sub>/SiN/Si capacitor measured from from 27 °C to 350 °C. In both cases, the Si substrates are p-type, so that they are biased in accumulation, and the electron currents originate from the Al electrode. While the room-temperature current levels are substantially the same for the two samples, they exhibit dramatically different temperature dependence. For negative gate voltages above 2 V, the TiO<sub>2</sub> sample exhibits very weak

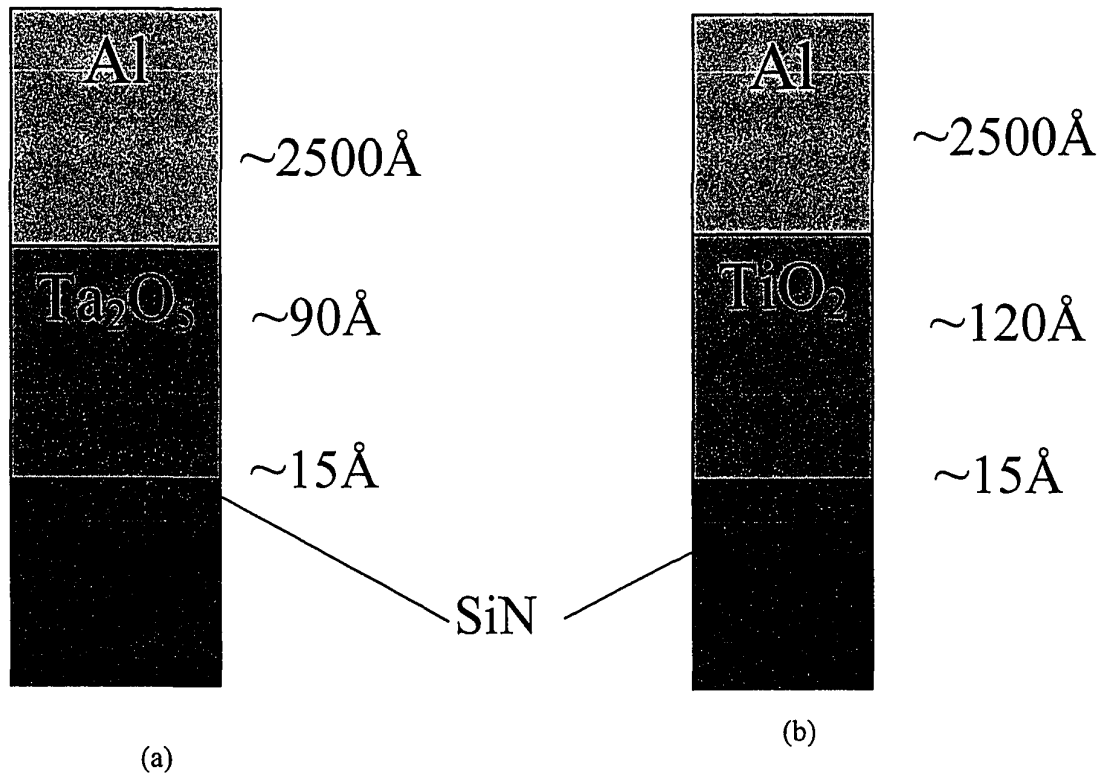


Figure 4.5 Schematic cross section views of (a) Al/Ta<sub>2</sub>O<sub>5</sub>/SiN/Si capacitor and (b) Al/TiO<sub>2</sub>/SiN/Si capacitor.

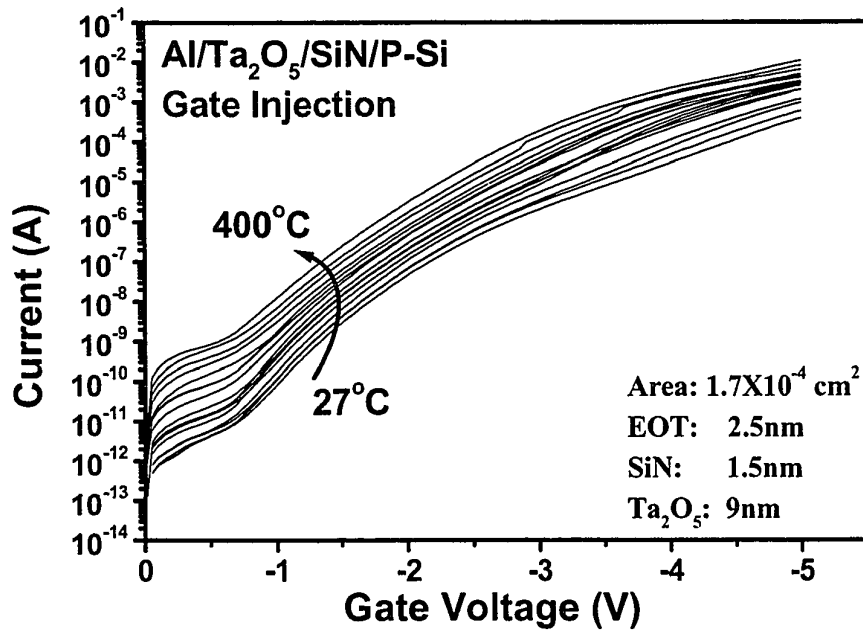


Figure 4.6 I-V characteristics of Al/Ta<sub>2</sub>O<sub>5</sub>/SiN/Si capacitor.

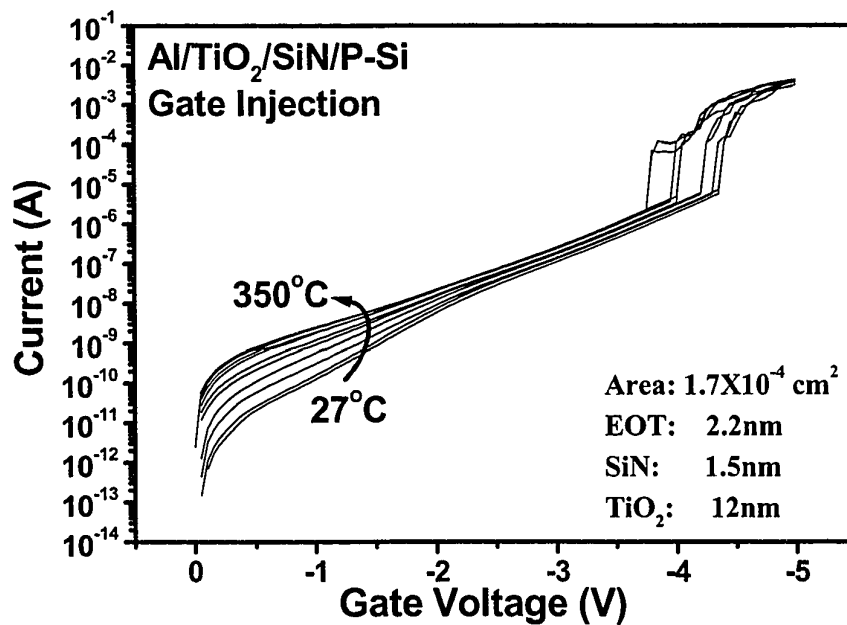


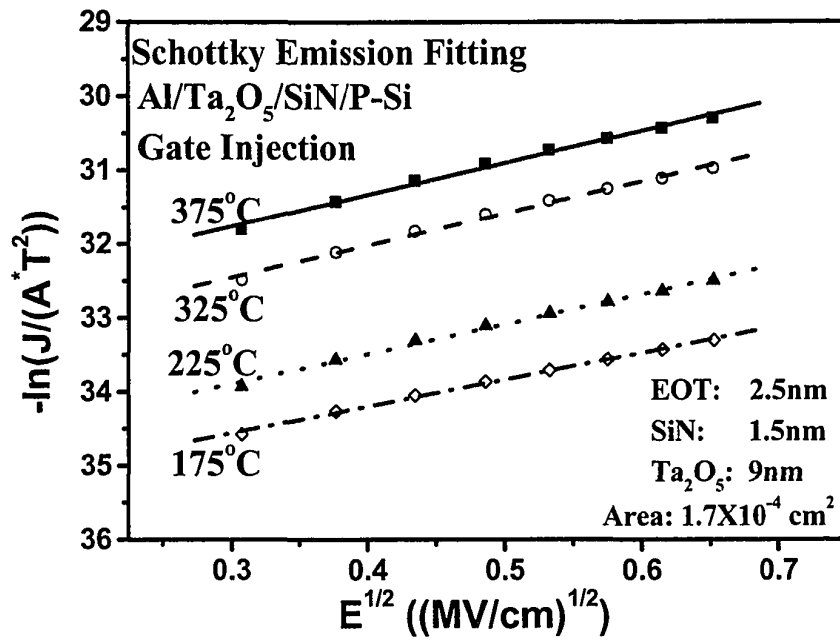
Figure 4.7 I-V characteristics of Al/TiO<sub>2</sub>/SiN/Si capacitor.

temperature dependence, suggesting tunneling as the dominant conduction mechanism, while the Ta<sub>2</sub>O<sub>5</sub> sample shows strong temperature dependence throughout the entire voltage range measured.

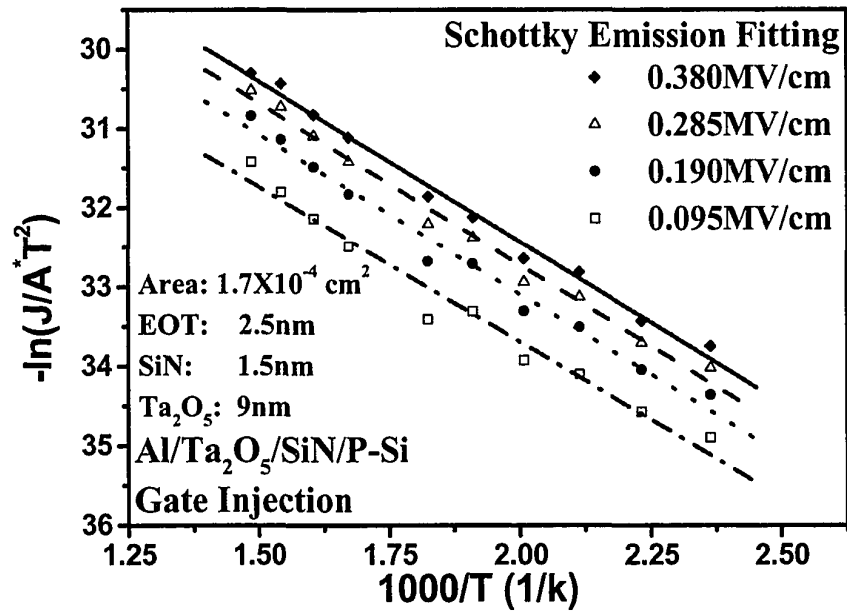
Two possible conduction mechanisms have been considered for the Ta<sub>2</sub>O<sub>5</sub> sample, of which the Frenkel-Poole mechanism was discarded because of the gross misfit between the theory and the data. The data, however, fit very well the Schottky-emission theory for temperatures above 175 °C, as shown in Figures 4.8(a) and (b). Schottky emission is a strong function of both temperature and electric field. Figure 4.8(a) presents the fitting as a function of electric field for four different temperatures, and Figure 4.8(b) displays the fitting as a function of temperatures above 175 °C, where Schottky emission becomes the dominant conduction mechanism. From these data, we extracted a Schottky barrier height of 0.35-0.38 eV between Al Fermi-level and Ta<sub>2</sub>O<sub>5</sub> conduction band edge, which is in good agreement with the barrier height reported for the Ta<sub>2</sub>O<sub>5</sub>/Si barrier of 0.28 eV measured by XPS<sup>132</sup> when the Al work function (4.15 eV) and the Si electron affinity (4.05 eV) are taken into account.

The weak temperature dependence exhibited in the high fields region of I-Vs of the TiO<sub>2</sub> sample suggests that tunneling may be the main conduction mechanism in this region. In deed, from the high-field I-V of the Al/TiO<sub>2</sub>/SiN/Si capacitor at room temperature, we fit the tunneling model very well, as shown in Figure 4.9, and extract a barrier height of ~1 eV between Al Fermi-level and TiO<sub>2</sub> conduction band edge by assuming an electron effective mass of 0.25 m<sub>0</sub>.

However, the strong temperature dependence of I-Vs in the low electric region suggests that thermally excited conduction mechanisms may be the dominant conduction mechanism. Data analysis indicates that Frenkel-Poole conduction is the dominant conduction mechanism for the TiO<sub>2</sub> sample in the low electric fields. Figures 4.10(a) and (b)



(a)



(b)

Figure 4.8 (a)  $-\ln(J/A \cdot T^2)$  vs  $1000/T$  fitting and (b)  $-\ln(J/A \cdot T^2)$  vs  $E^{1/2}$  fitting for Al/Ta<sub>2</sub>O<sub>5</sub>/SiN/Si capacitor.

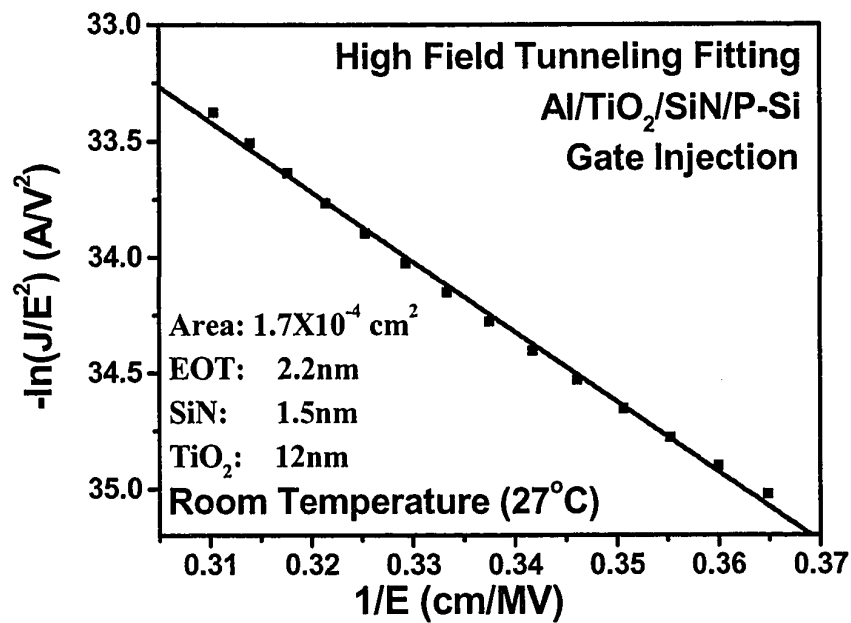
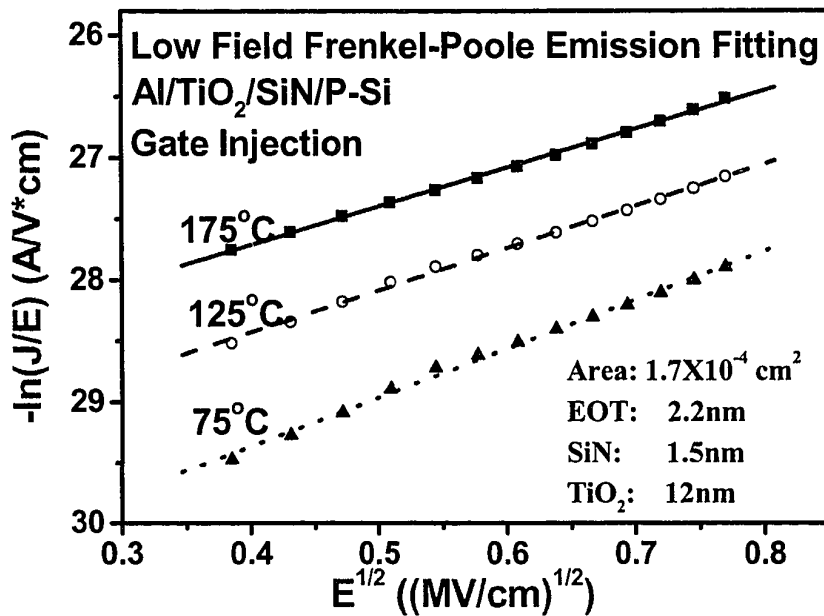
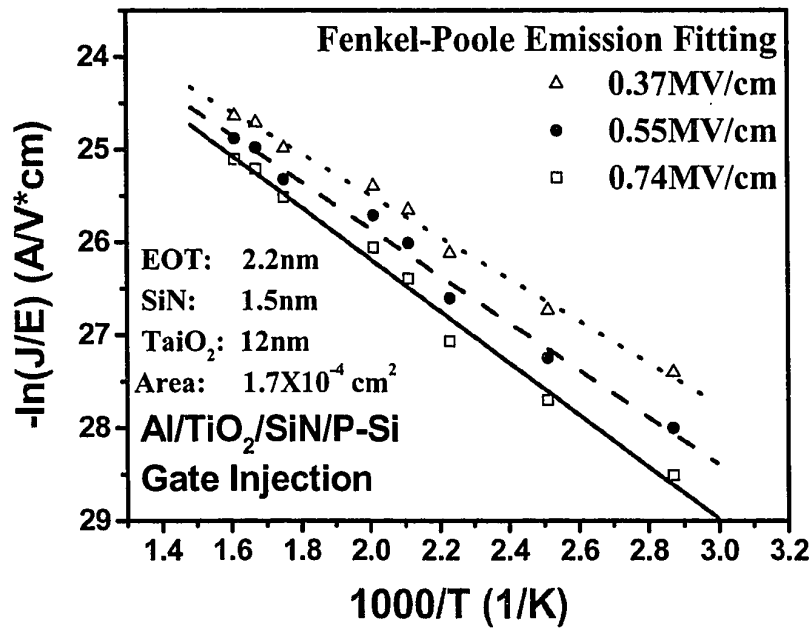


Figure 4.9 Tunneling fitting for Al/TiO<sub>2</sub>/SiN/Si capacitor at high electric fields.



(a)



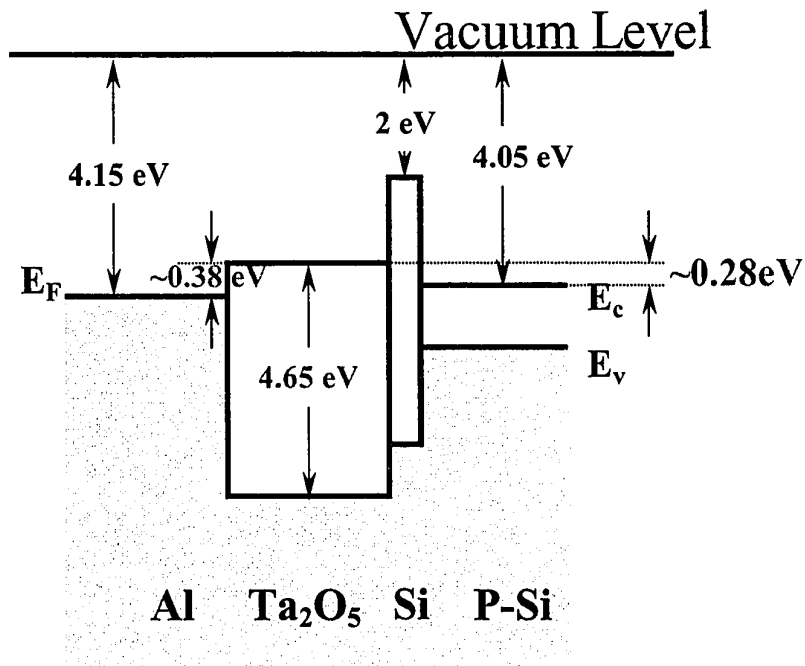
(b)

Figure 4.10 (a)  $-\ln(J/E)$  vs  $1000/T$  fitting and (b)  $-\ln(J/E)$  vs  $E^{1/2}$  fitting for Al/TiO<sub>2</sub>/SiN/Si capacitor at low electric fields.

show the Frenkel-Poole emission fitting for the Al/TiO<sub>2</sub>/SiN/Si capacitor. Just like Schottky emission, the I-V data of the TiO<sub>2</sub> sample were fitted to the Frenkel-Poole conduction model over the variations of temperature and electric field, respectively. In both cases, the low-field temperature dependence of the TiO<sub>2</sub> sample fits the Frenkel-Poole conduction model perfectly, with an extracted trap energy of 0.28-0.3 eV between the conduction bands of TiO<sub>2</sub> and Si.

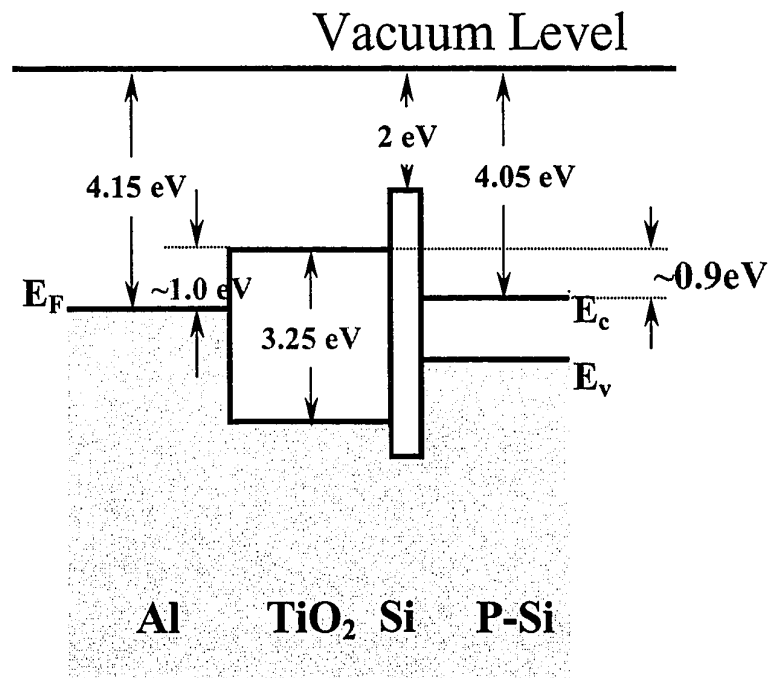
From the results of this study and existing knowledge, we have constructed the band diagrams for Al/Ta<sub>2</sub>O<sub>5</sub>/SiN/Si and Al/TiO<sub>2</sub>/SiN/Si systems, as shown in Figures 4.11(a) and (b) respectively. From our study, a Schottky barrier height about 0.38 eV is extracted between Al and Ta<sub>2</sub>O<sub>5</sub>. When we take the Al work function of 4.15 eV and the Si electron affinity of 4.05 eV into account, a barrier height of 0.28 eV can be extracted between Ta<sub>2</sub>O<sub>5</sub> and Si conduction band edges, which agrees with the barrier height measured by XPS<sup>6</sup>. Also, a barrier height of 0.9 eV between TiO<sub>2</sub> and Si conduction band edges can be extracted, when considering the Al work function and Si electron affinity as well. It is interesting to note that the bandgap of Ta<sub>2</sub>O<sub>5</sub> (~4.65 eV) is substantially larger than that of TiO<sub>2</sub> (~3.25 eV), but the electron barrier height for the former, 0.28 eV, is much lower than that for the latter, 0.9 eV, due to the different band alignments. This is the major reason for the much stronger temperature dependence of the I-V characteristics we have observed in the Ta<sub>2</sub>O<sub>5</sub> sample.

In summary, we have observed much stronger temperature dependence of I-V curves in Ta<sub>2</sub>O<sub>5</sub> than in TiO<sub>2</sub> samples. This is attributable to the much lower electron barrier height in the former, which leads to Schottky emission as the dominant conduction mechanism. In contrast, the TiO<sub>2</sub> sample exhibits tunneling as the dominant conduction mechanism in the high-field region, but Frenkel-Poole conduction in the low-field region. This study has revealed that the high bandgap of a high-k material does not guarantee a



**Al/Ta<sub>2</sub>O<sub>5</sub>/SiN/Si**

(a)



**Al/TiO<sub>2</sub>/SiN/Si**

(b)

Figure 4.11 Band diagrams of Al/Ta<sub>2</sub>O<sub>5</sub>/SiN/Si and Al/TiO<sub>2</sub>/SiN/Si.

high barrier height over Si conduction band edge, and in certain cases, such as Ta<sub>2</sub>O<sub>5</sub>, the band alignment plays a predominant role in the determination of barrier height.

### **4.3 Barrier Heights of Al<sub>2</sub>O<sub>3</sub>, ZrO<sub>2</sub>, and Fermi-level of Tungsten Measured by Photoemission**

The significance of either ZrO<sub>2</sub> or Al<sub>2</sub>O<sub>3</sub> in the race to replace silicon dioxide as the gate dielectric has been stated many times in the former chapters. And in Chapters 1 and 2, we have described the significance of employing the proper metal gates to reduce the polysilicon depletion effect. Moreover, a mid-gap metal gate electrode is necessary to achieve the most desirable threshold voltages for both NMOS and PMOS in Fully-Depleted Silicon-On-Insulator (FDSOI)<sup>133</sup> or Double-gate CMOS device structures<sup>134</sup>, if “intrinsic” channels<sup>135</sup> are used to reduce the threshold voltage variation and to improve the channel mobility. Tungsten is the most promising candidate as a mid-gap metal gate material, because of its good conductivity and near ideal mid gap work function. Moreover, Chemical-Vapor-Deposited (CVD) Tungsten<sup>136</sup> has shown compatibility with the existing CMOS process flow. Therefore, it is significant and necessary to measure the barrier heights of these important materials, which are the keys to obtain and model the threshold voltages and gate leakage currents of devices based on these materials. In our study, the barrier heights of CVD Tungsten and ALD Al<sub>2</sub>O<sub>3</sub> and ZrO<sub>2</sub> have been measured by the internal photoemission method directly on MOS structures.

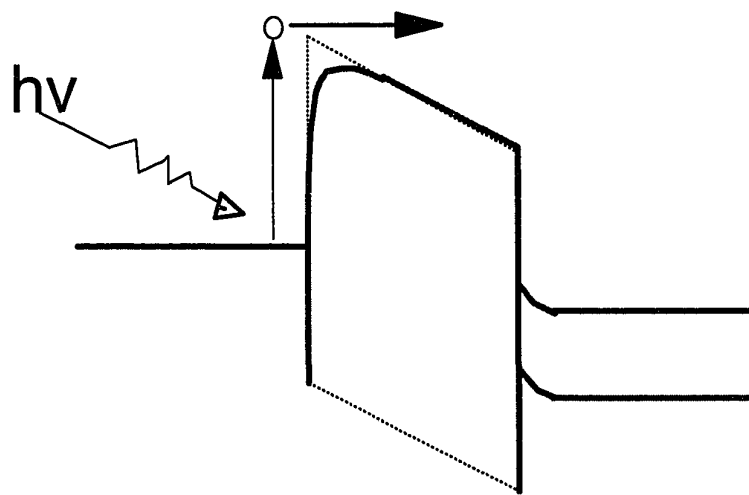
### 4.3.1 Internal Photoemission

Internal photoemission is an effective method to measure the barrier height directly on MOS structures<sup>137,138,139</sup>. The current transport process of internal photoemission in MOS structures is very similar to that of Schottky emission. However, instead of exciting carriers to high energy levels by elevating temperature, a different source, light, is employed to excite carriers. When shining light on a MOS structure, electrons in the metal or semiconductor absorb photons, and are excited to higher energy levels. If the photon energy of the illumination light is higher than the barrier height at the metal-insulator or semiconductor-insulator interface, the excited electrons will have enough energy to overcome the barrier, and transport to the other side, as shown in Figure 4.12. Therefore, instead of depending strongly on temperature as in Schottky emission, the current is a strong function of photon energy. In order to ensure sufficient carriers at the metal-insulator or semiconductor-insulator interface, a very thin metal layer is used as the top electrode to reduce the absorption of photons. Moreover, due to the image force lowering effect, the photocurrent is strongly dependent on voltage bias as well. Therefore, by studying the photocurrent as a function of two independent variables, photon energy and voltage, we can determine the interface barrier height of metal-insulator or semiconductor-insulator<sup>140,141</sup>.

Three basic processes, exciting electrons by photons, transporting to the metal-insulator or semiconductor-insulator interface, and moving over the interface barrier, determine the quantum yield of photoemission, which can be described as

$$Y(\hbar\omega, E_b) = \int_{E_b}^{\hbar\omega} Ni(\hbar\omega, E_b) \times P(E) dE, \quad (4.3)$$

*Photo Current  $\sim F(h\nu, V_g)$*



**Metal Insulator Si**

Figure 4.12 Schematic representation of internal photoemission.

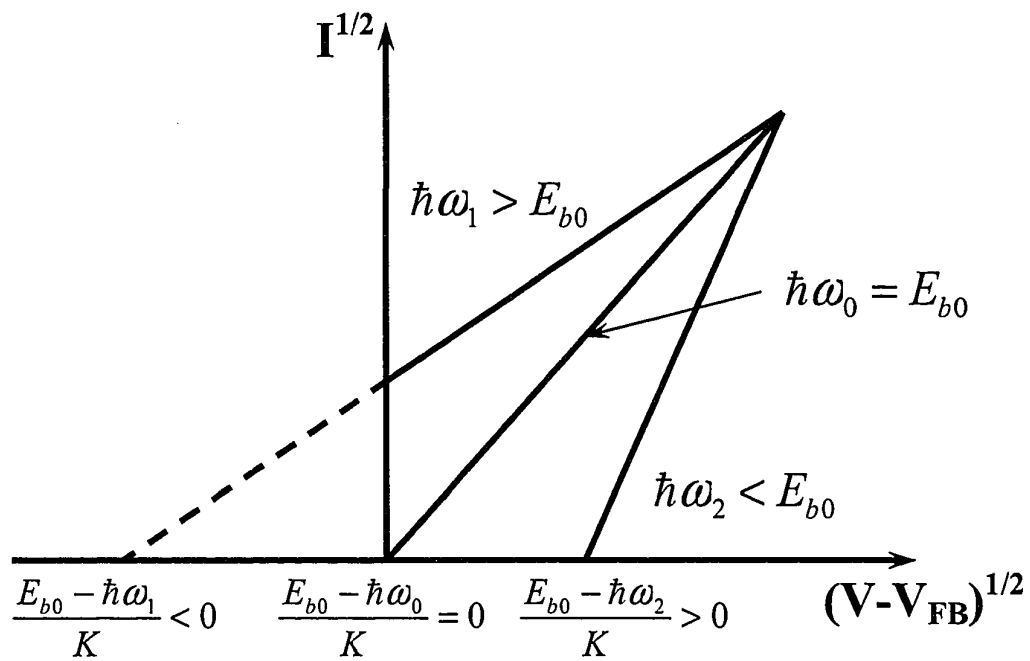


Figure 4.13 A family of normalized  $I^{1/2}$  vs.  $(V - V_{FB})^{1/2}$  curves illustrates the method of determining  $E_{b0}$ .

where  $E_b$  is the barrier height,  $\hbar\omega$  is the photon energy,  $Ni(\hbar\omega, E_b)$  is the energy distribution of electrons at the metal-insulator or semiconductor-insulator interface, and  $P(E)$  is the surface transmission probability.

If we assume that over a limited energy range, the density of unoccupied energy states, the transition probability between initial and final states, and the electron scattering factor are almost unchanged, and furthermore, use the non-direct optical transition approximation, the energy distribution of electrons at the interface becomes only a function<sup>137,138,139</sup> of  $(E - \hbar\omega)$ ,

$$Ni(\hbar\omega, E_b) = Ni(E - \hbar\omega). \quad (4.4)$$

Moreover, to a good approximation, we can assume the transmission probability as

$$P(E) = C(E - E_b), \quad (4.5)$$

where  $C$  is a constant.

Therefore, we can simplify the quantum yield as

$$Y(\hbar\omega, E_b) = C \int_{E_b}^{\hbar\omega} Ni(E - \hbar\omega) \times (E - E_b) dE. \quad (4.6)$$

The photocurrent can be expressed as

$$I = L \times Y / \hbar\omega, \quad (4.7)$$

where  $L$  is the total absorbed illuminating light energy in unit time. By substituting Equation 4.6 into Equation 4.7, the photocurrent can be written as

$$I = A(\hbar\omega) \int_0^{\hbar\omega - E_b} Ni(-E') \times (\hbar\omega - E_b - E') dE', \quad (4.8)$$

where  $A(\hbar\omega) = L \times C / \hbar\omega$ , and  $E' = \hbar\omega - E$ .

For the metal-insulator or degenerated Si-insulator interfacial barriers, the image force barrier lowering is the dominant factor for the field or voltage dependence at high electric fields ( $> 0.1$  MV/cm). Therefore, the barrier can be written as

$$E_b = E_{b0} - K(V - V_{FB})^{1/2}, \quad (4.9)$$

where  $V$  is the applied voltage, and  $V_{FB}$  is the flat band voltage of the measured device;  $K = (q/4\pi\epsilon_s)^{1/2}$ , in which  $q$  is the electron charge,  $t$  is the thickness of the dielectric, and  $\epsilon_s$  is the high-frequency dielectric constant in the image force region. Including the barrier lowering effect, the photocurrent becomes voltage dependent and is rewritten as

$$I = A(\hbar\omega) \int_0^{\hbar\omega - E_{b0} + K(V - V_{FB})^{1/2}} N_i(-E') \times (\hbar\omega - E_{b0} + K(V - V_{FB})^{1/2} - E') dE'. \quad (4.10)$$

For photoelectrons injected from the metal side, a step function is a good approximation for the energy distribution of electrons at the metal-insulator interface, and the photocurrent can be expressed as

$$I(\hbar\omega, V) = A(\hbar\omega) \times (\hbar\omega - E_{b0} + K(V - V_{FB})^{1/2})^2$$

or,

$$[I(\hbar\omega, V)]^{1/2} = [A(\hbar\omega)]^{1/2} \times (\hbar\omega - E_{b0} + K(V - V_{FB})^{1/2}). \quad (4.11)$$

A family of normalized  $I^{1/2}$  vs.  $(V - V_{FB})^{1/2}$  curves can be obtained, as shown in Figure 4.13. For  $\hbar\omega = E_{b0}$ , the line intercepts the  $(V - V_{FB})^{1/2}$  axis at zero. And, for  $\hbar\omega < E_{b0}$  or  $\hbar\omega > E_{b0}$ , the line intercepts the  $(V - V_{FB})^{1/2}$  axis at a positive or negative value, respectively. Thus, the barrier height can be simply and accurately determined regardless of the values of  $A(\hbar\omega)$ ,  $K$ , and the density of the illuminating light.

### 4.3.2 Barrier Heights of $Al_2O_3$ , $ZrO_2$ , and Fermi-level of Tungsten

Since photo current is small, in order to reduce leakage current, relatively thick dielectrics were used in our study.  $Al_2O_3$  was deposited on Si wafers by the ALD method, and the thicknesses of  $Al_2O_3$  are about 40nm and 45nm (physical thickness). The surfaces

of the n-type Si wafers were heavily implanted ( $10^{20} / \text{cm}^3$ ) to avoid possible band bending during substrate injection. Al was evaporated on top of the  $\text{Al}_2\text{O}_3$  to form the top electrodes by using shadow masks. The thickness of Al is less than 20nm, which allows enough light to pass through.  $\text{ZrO}_2$  films were deposited by CVD method. Tungsten films were deposited in high vacuum using  $\text{W}(\text{CO})_6$  method<sup>136</sup> directly on 20nm  $\text{SiO}_2$  that had been thermally grown on p-type Si substrate. The CVD Tungsten films were limited to about 20nm thick to allow enough photons through during the internal photoemission measurement. The test structures of the CVD Tungsten films, round shaped capacitors, were defined by photolithography, and the CVD Tungsten was etched out by hydrogen peroxide ( $\text{H}_2\text{O}_2$ ) solution. The light source used in this study was a mercury UV lamp, and a monochromator was employed to select the light with specific photon energies.

During the internal photoemission measurement, the polarity of the applied voltage on the gate electrode determines the direction of photocurrent generated by light illumination. For the  $\text{Al}/\text{Al}_2\text{O}_3/\text{p-Si}$  capacitor, when the Al gate electrode is negatively biased, photoelectrons are injected from the Al gate electrode into  $\text{Al}_2\text{O}_3$ . To use the method described in Section 4.3.1, a family of normalized  $I^{1/2}$  vs.  $(V-V_{FB})^{1/2}$  curves measured under different photon energies is shown in Figure 4.14. As described in Figure 4.13, if the photon energy of the incoming light is equal to the barrier height of  $\text{Al}-\text{Al}_2\text{O}_3$ , the line in the high fields region intercepts the  $(V-V_{FB})^{1/2}$  axis at zero. And for photon energies smaller or larger than the barrier height of  $\text{Al}-\text{Al}_2\text{O}_3$ , the extrapolated lines intercept the  $(V-V_{FB})^{1/2}$  axis at positive or negative values, respectively. Moreover, the values of these intercepts have a linear relationship with the photon energy. Therefore, we can plot the values of the intercepts vs. the photon energies, as shown in Figure 4.15. And the photon energy at the zero intercept is the interface barrier height between Al Fermi-level and  $\text{Al}_2\text{O}_3$  conduction band edge, which is  $3.1 \pm 0.1$  eV obtained from the measurement. To extract the interface barrier height between  $\text{Al}_2\text{O}_3$  conduction band edge and Si valence band edge, n-type MOS

capacitors with heavily doped surfaces are used. The gate electrode is positively biased, and the photocurrent flows from Si into  $\text{Al}_2\text{O}_3$  under illuminating. Using the method described above to extract the interfacial barrier height, a barrier height of  $4.1 \pm 0.1$  eV between the  $\text{Al}_2\text{O}_3$  conduction band edge and Si valence band edge was obtained, as shown in Figure 4.16. Considering the difference between the Al work function and Si valence band of 1 eV, the results are consistent with each other. Therefore, a band diagram of the Al-  $\text{Al}_2\text{O}_3$ -Si can be built, as shown in Figure 4.17.

Because Pt has a larger work function than that of Al, A Pt-gate MOS capacitor has a much smaller gate leakage current under gate injection than that of its Al-gate counterpart at the same electric field. Therefore, in order to minimize the influence of gate leakage current on photocurrent, Pt-gate MOS capacitors were used to measure the barrier height of  $\text{ZrO}_2$  in the photoemission measurement. A barrier height of 3.4 eV was obtained between Pt Fermi-level and  $\text{ZrO}_2$  conduction band edge.

The same method was applied to measure the work function of Tungsten as well. The barrier height between Si conduction band edge and  $\text{SiO}_2$  conduction band edge is well known, so by studying the barrier height between Tungsten and  $\text{SiO}_2$ , we can determine whether the Fermi-level of tungsten sits at the middle of Si bandgap. The tungsten gate electrode was negatively biased; therefore, electrons were injected from the tungsten gate into  $\text{SiO}_2$ . A barrier height of  $3.8 \pm 0.1$  eV was extracted between Tungsten Fermi-level and  $\text{SiO}_2$  conduction band edge, as shown in Figure 4.18. Moreover, the barrier height between Tungsten and  $\text{SiO}_2$  was obtained using the Fowler-Nordheim tunneling method. From the slope of the  $\ln(J/E^2)$  vs.  $1/E$  plot, we can calculate the barrier height between Tungsten Fermi-level and  $\text{SiO}_2$  conduction band edge, as shown in Figure 4.19. Considering the correction for the image force barrier lowering effect, a barrier height of 3.8 eV was

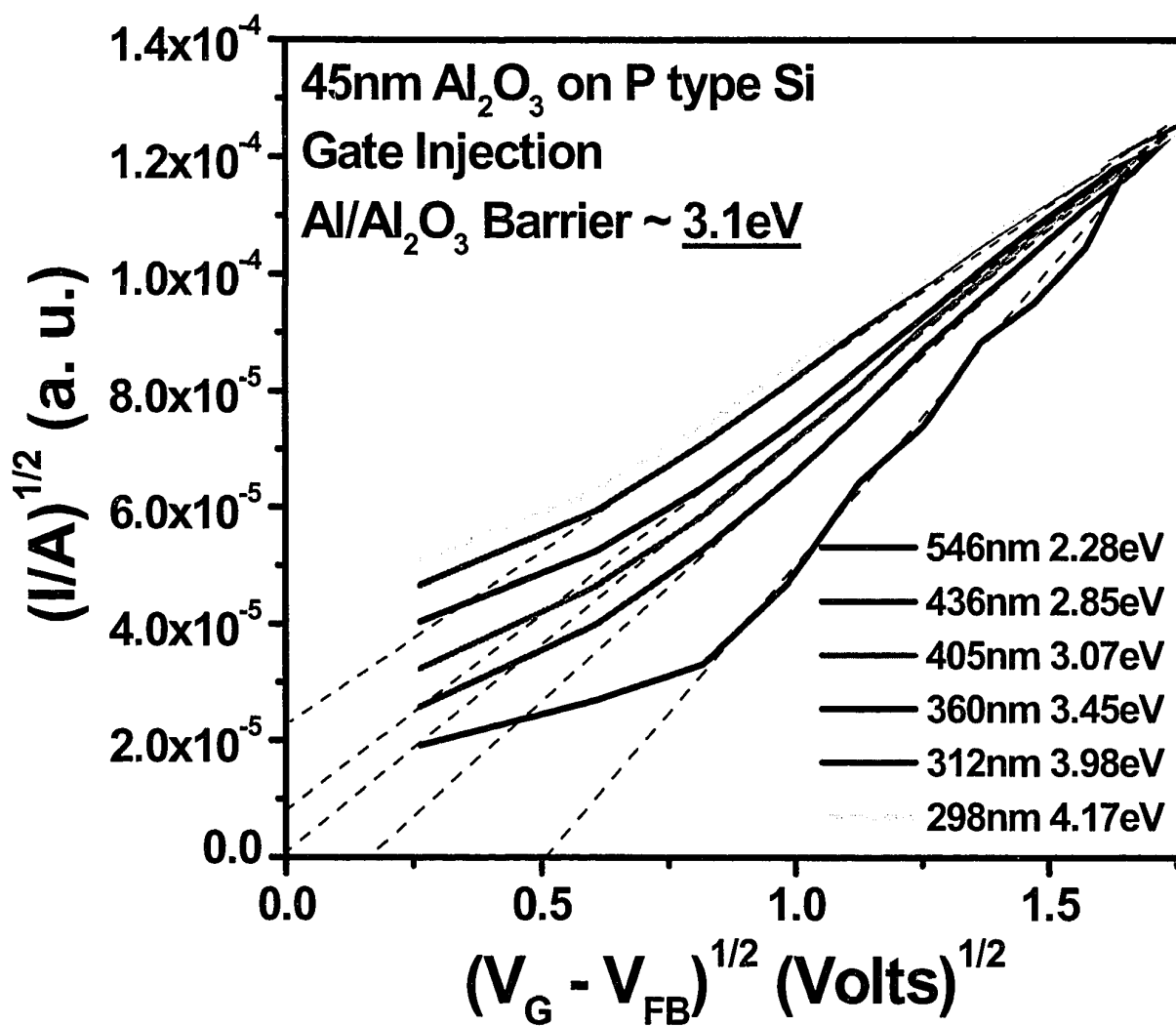


Figure 4.14 A family of  $I^{1/2}$  vs.  $(V - V_{fb})^{1/2}$  curves of Al/Al<sub>2</sub>O<sub>3</sub>/p-Si capacitor under gate photoinjection.

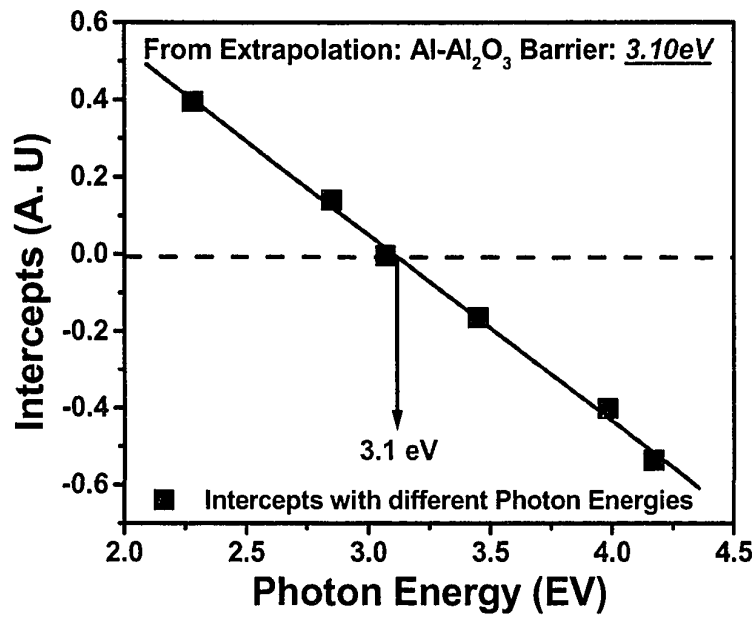


Figure 4.15 A barrier height of 3.1 eV between Al Fermi-level and Al<sub>2</sub>O<sub>3</sub> conduction band edge is determined by the photoemission method.

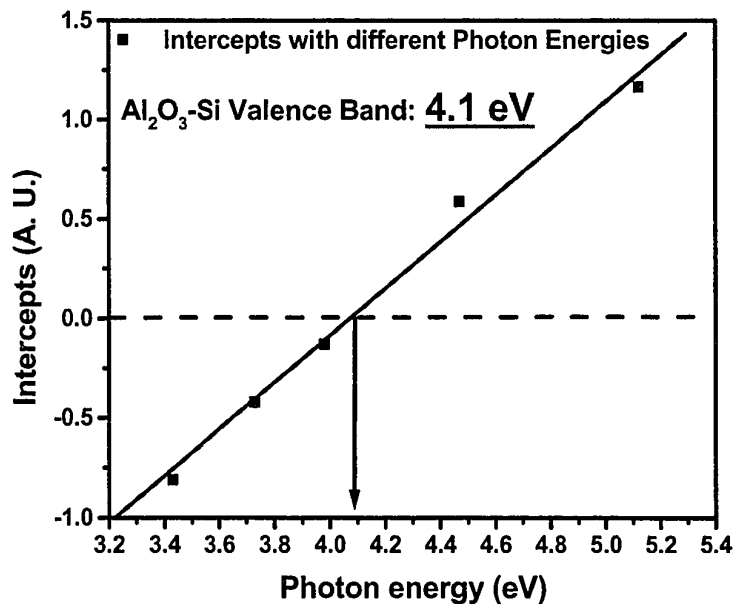
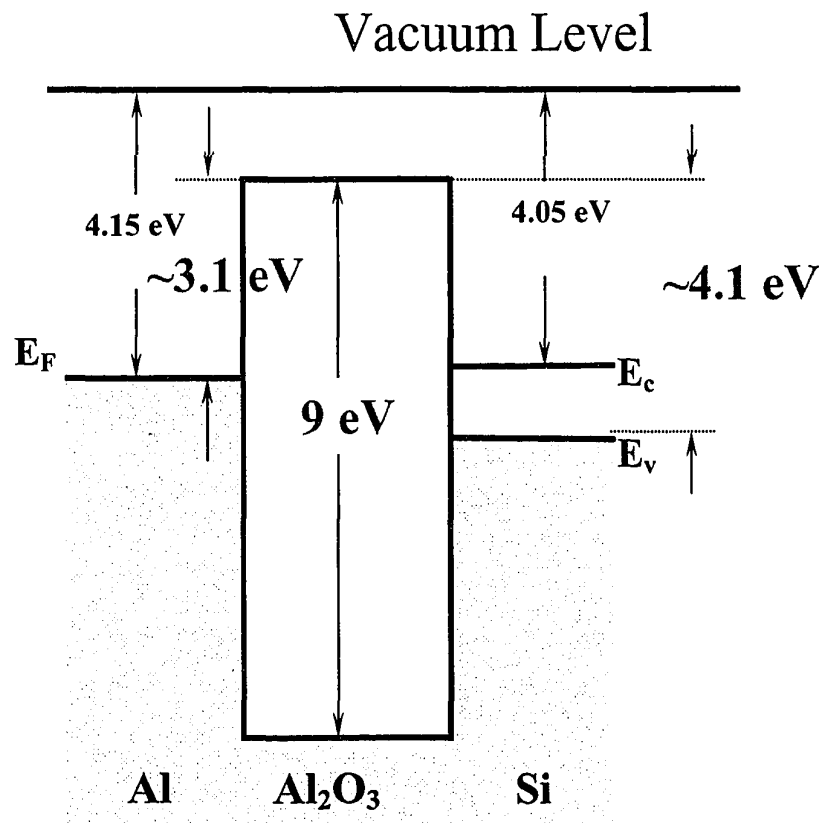


Figure 4.16 A barrier height of 4.1 eV between Al<sub>2</sub>O<sub>3</sub> conduction band edge and Si valence band is determined by the photoemission method.



### Al/Al<sub>2</sub>O<sub>3</sub>/Si

Figure 4.17 Band diagram of Al-Al<sub>2</sub>O<sub>3</sub>-Si.

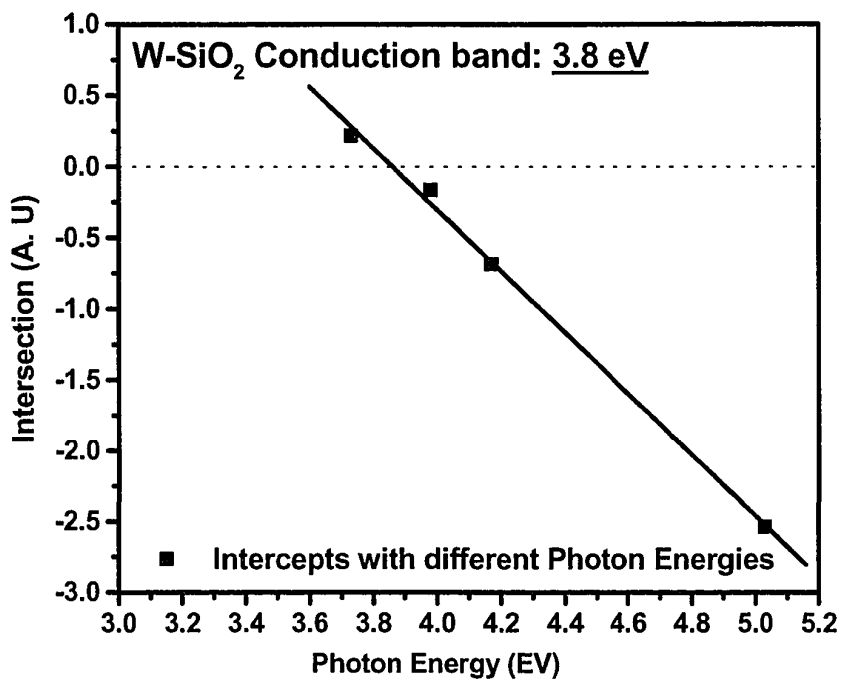


Figure 4.18 A barrier height of 3.8 eV between W Fermi-level and SiO<sub>2</sub> conduction band edge is determined by the photoemission method.

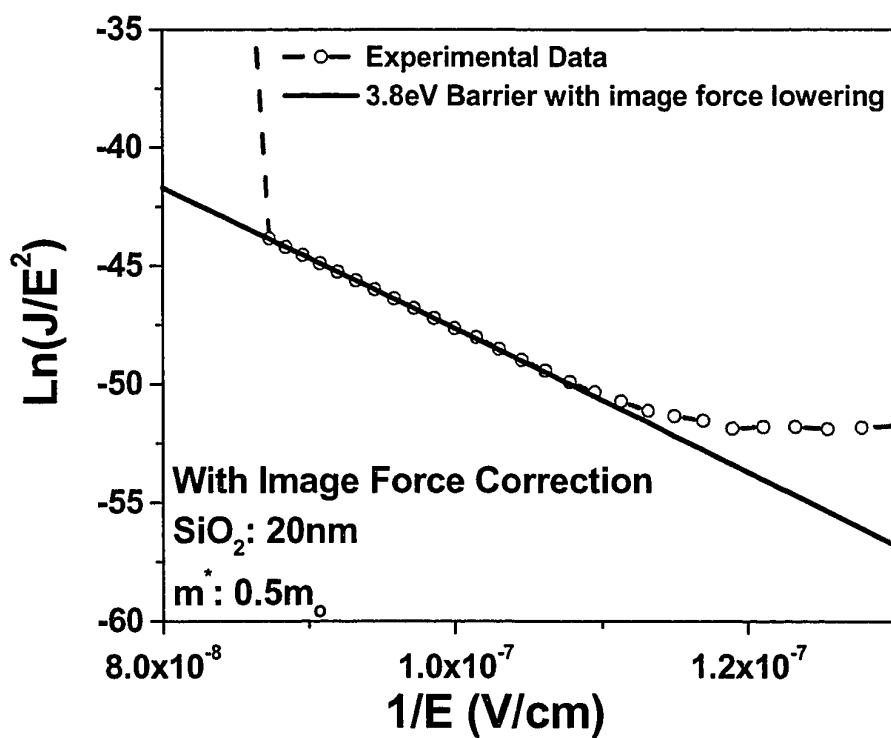


Figure 4.19 A barrier height of 3.8 eV between W Fermi-level and SiO<sub>2</sub> conduction band edge is determined by the tunneling method.

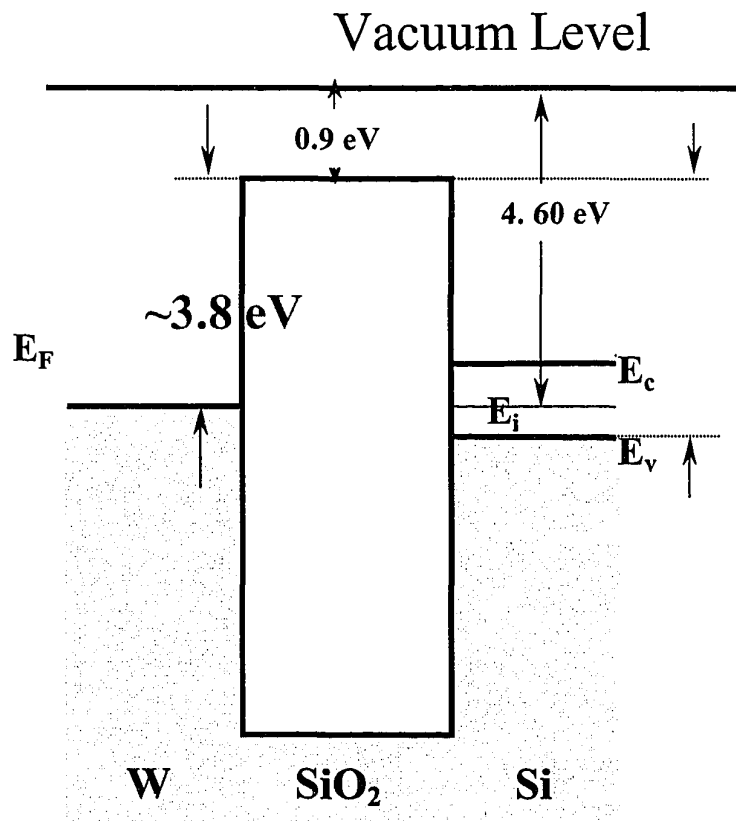


Figure 4.20 Band diagram of W- SiO<sub>2</sub>-Si.

obtained, which is consistent with the value measured by internal photoemission. The extracted work function of Tungsten satisfies the requirement of a mid-gap metal for FDSOI or Double-gate CMOS structures. In both cases, the well-acknowledged effective mass for SiO<sub>2</sub>, 0.5m<sub>0</sub>, was used for calculation. A band diagram is constructed for the W-SiO<sub>2</sub>-Si system, as show in Figure 4.20.

Al<sub>2</sub>O<sub>3</sub> enjoys a very high barrier, about 4.1 eV over the Si valence and about 3.0 eV over the Si conduction band edge. Such a high barrier makes it very attractive to be used as a gate insulator to reduce gate leakage currents, and it becomes more advantageous over other high-k materials at elevated temperatures. A barrier height of 3.4 eV is extracted between Pt Fermi-level and ZrO<sub>2</sub> conduction band edge. From the photoemission measurement on MOS structures, a barrier height of 3.8 eV was measured between Tungsten Fermi-level and SiO<sub>2</sub> conduction band edge, which satisfies the requirement for a mid gap metal.

## 4.4 Barrier Heights of ZrO<sub>2</sub> and Titanium Aluminates Measured by Low Temperature Tunneling

Fowler-Nordheim Tunneling is a simple and effective method to determine the barrier height from a MOS structure. However, because the barrier height and effective mass are coupled in the Fowler-Nordheim current, we have to know either the barrier height or the effective mass to derive the other parameter from Fowler-Nordheim measurement. In order to solve this problem, a dual gate electrodes method<sup>142</sup> is used. By using two different gate electrodes, such as Pt and Al, for the same insulator in MOS structures, we can obtain two independent equations, from the slopes of  $\ln(J/E^2)$  vs.  $1/E$  plots,

$$Slope_{Pt} = -\frac{8\pi(2qm^*)^{1/2}}{3h}\phi_{Pt}^{3/2}, \quad (4.11)$$

and

$$Slope_{Al} = -\frac{8\pi(2qm^*)^{1/2}}{3h}\phi_{Al}^{3/2}, \quad (4.12)$$

where  $m^*$  is the effective mass;  $\phi_{Pt}$  and  $\phi_{Al}$  are barrier heights for Pt and Al, respectively.

Moreover, the work function difference between these two different gate electrodes can be determined from C-V results. Therefore, we are able to obtain the values of barrier height and effective mass.

In high-k materials, because of the presence of high-density traps, usually Frenkel-Poole and other trap-assisted transports constitute a significant part of leakage current. However, because Frenkel-Poole and other trap-assisted transport mechanisms are thermally excited and exponentially dependent on temperature, the trap-assisted currents are drastically subdued at low temperatures. Therefore, the current transport becomes tunneling dominated. Combining the effectiveness of the dual-gate electrode method and low temperature measurement, we could get the tunneling parameters for high-k materials even in the presence of traps.

Gold-gate and Al-gate JVD ZrO<sub>2</sub> MOS capacitors were used for low temperature I-V measurement. The tunneling I-V plots for both the gold-gate MOS capacitor and Al-gate MOS capacitor are shown in Figures 4.21 and 4.22, respectively. From these plots, the derived barrier heights are 3.2 eV between gold Fermi-level and ZrO<sub>2</sub> conduction band edge, and 1.9 eV between aluminum Fermi-level and ZrO<sub>2</sub> conduction band edge, and the derived effective mass is 0.1  $m_0$ . A barrier height of 3.3 eV between Pt and ZrO<sub>2</sub> was measured by photoemission, as reported in Section 4.2. Considering the work function difference of 1.4 eV between Pt and Al measured from C-V curves, the barrier height derived from tunneling is consistent with the barrier height measured by photoemission. Moreover, as presented in Figure 4.23, from the tunneling fitting for n-type JVD ZrO<sub>2</sub> MOS

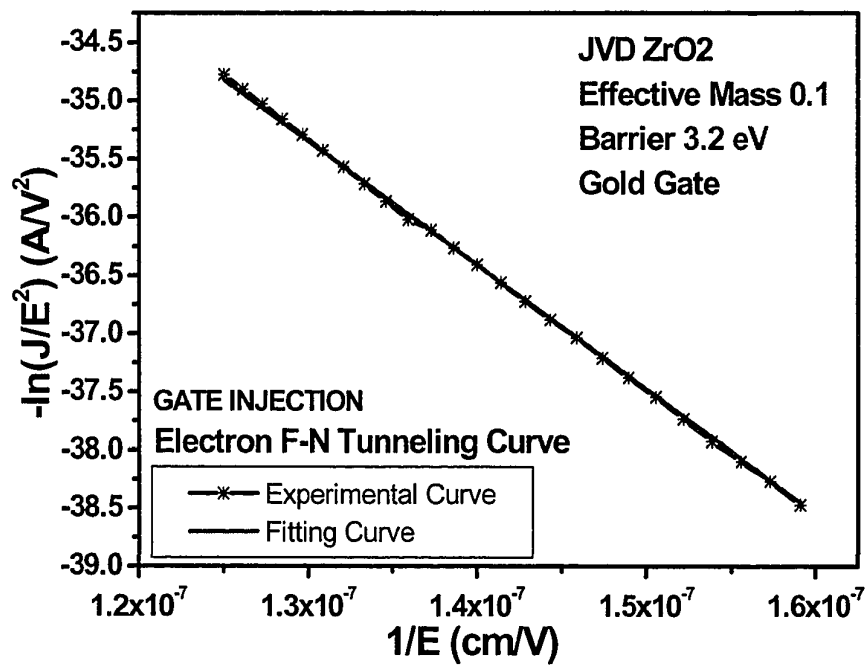


Figure 4.21 Tunneling fitting results from gold-gate JVD ZrO<sub>2</sub>/silicate capacitor under gate injection.

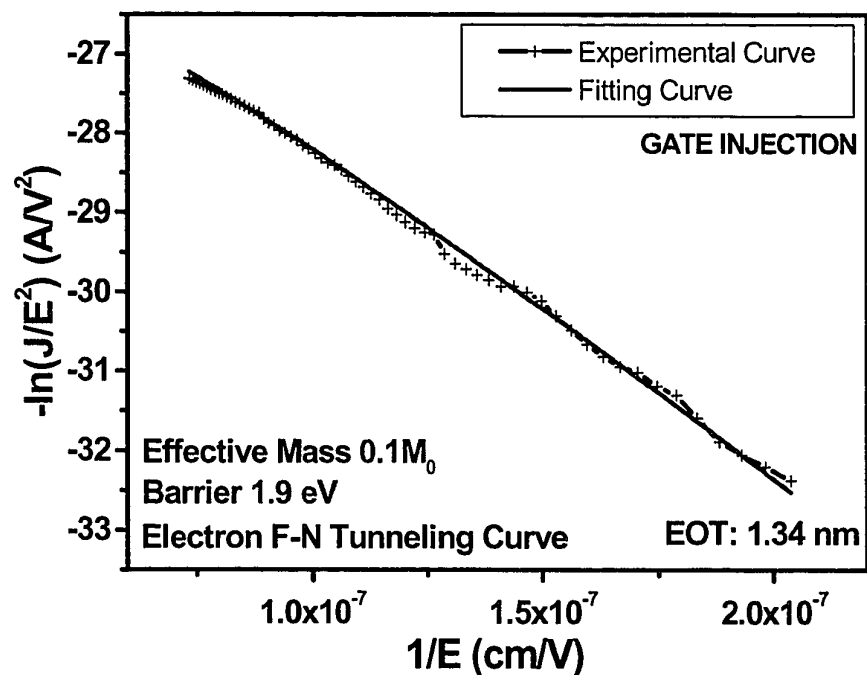


Figure 4.22 Tunneling fitting results from Al-gate JVD ZrO<sub>2</sub>/silicate capacitor under gate injection.

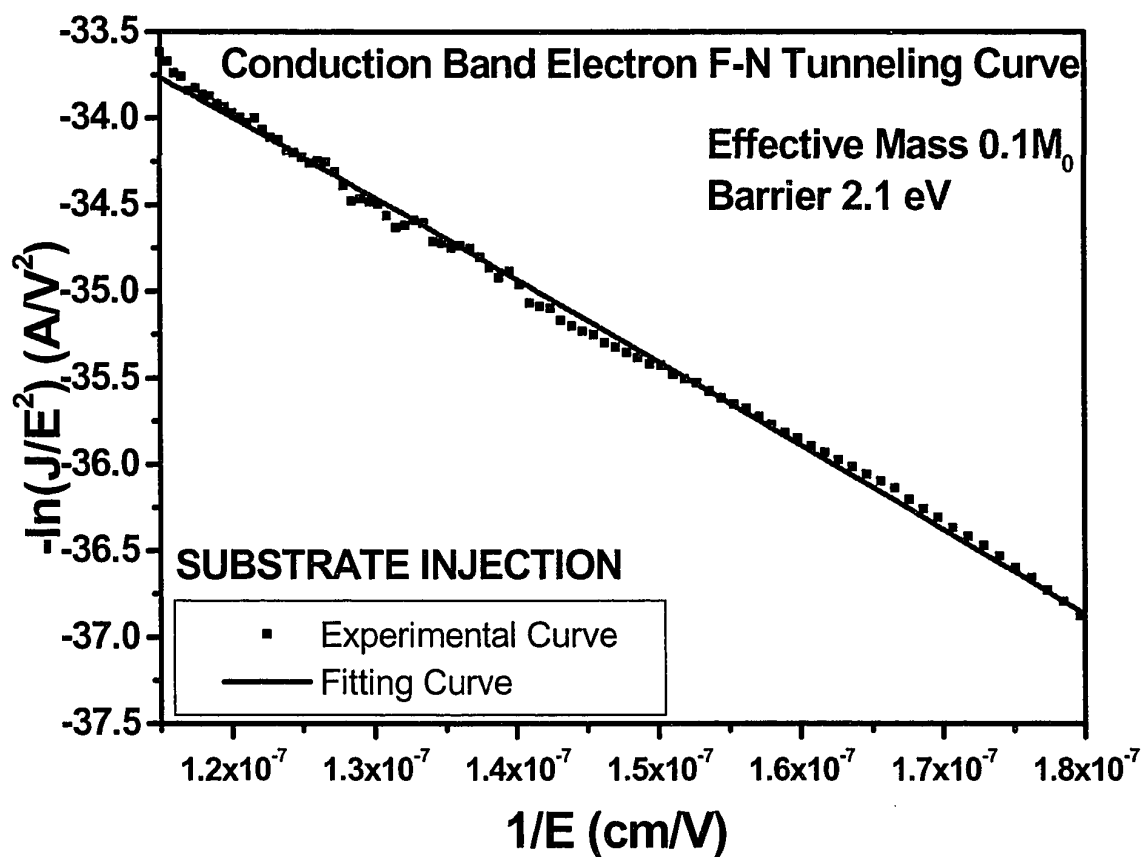
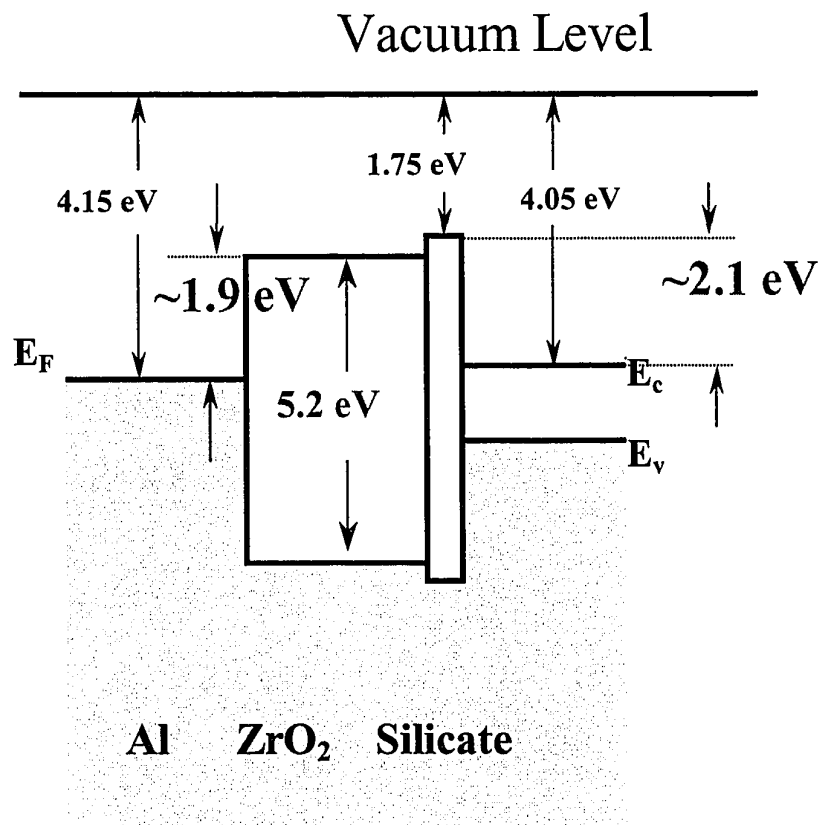


Figure 4.23 Tunneling fitting results from Al-gate JVD  $ZrO_2$ /silicate capacitor under substrate Injection.

capacitor under substrate injection, a barrier height of 2.1 eV between  $\text{ZrO}_2$  conduction band and Si conduction band was extracted by using the effective mass of 0.1  $m_0$ . We have shown in Chapter 2 that a thermally stable interfacial layer of Zr silicate is unintentionally formed between  $\text{ZrO}_2$  and Si during the deposition. And the difference in the barrier heights measured from gate injection and substrate injection, even after considering the difference in metal work function and silicon electron affinity may be attributed to the existence of the Zr silicate layer. Moreover, a band gap of 5.2 eV for the JVD  $\text{ZrO}_2$  has been measured by an N&K analyzer. Therefore, we can construct the band diagram for Al/ $\text{ZrO}_2$ /silicate/Si, as shown in Figure 4.24.

We used two different metal electrodes, Al and Pt, on titanium aluminate MOS capacitors to measure the barrier heights. The barrier heights of titanium aluminates with 15, 30, and 50 atomic percent aluminum concentrations have been studied. The work function difference between Pt and Al on titanium aluminates is 1.6 eV, which is about 0.2 eV higher than the work function difference between Pt and Al on  $\text{ZrO}_2$ . The effective work functions of various metal/dielectrics may be altered by the different dipoles formed at the metal/dielectric interfaces. The barrier height of titanium aluminate escalates with the aluminum concentration. From our study, the barrier heights of titanium aluminates with 15, 30, and 50 atomic % aluminum concentrations over Al Fermi-level are about 1 eV, 1.1 eV, and 1.5 eV, respectively, as shown in Figure 4.25. The barrier heights for titanium aluminates with 15 and 30 atomic % concentrations only increase slightly when compared to that of titanium oxide. However, for the titanium aluminate with 50 atomic % aluminum concentration, we observe an increase of barrier height of 0.4 eV when compared to that of titanium oxide.



## Al/ZrO<sub>2</sub>/Silicate/Si

Figure 4.24 Band diagrams of Al/ZrO<sub>2</sub>/Silicate/Si.

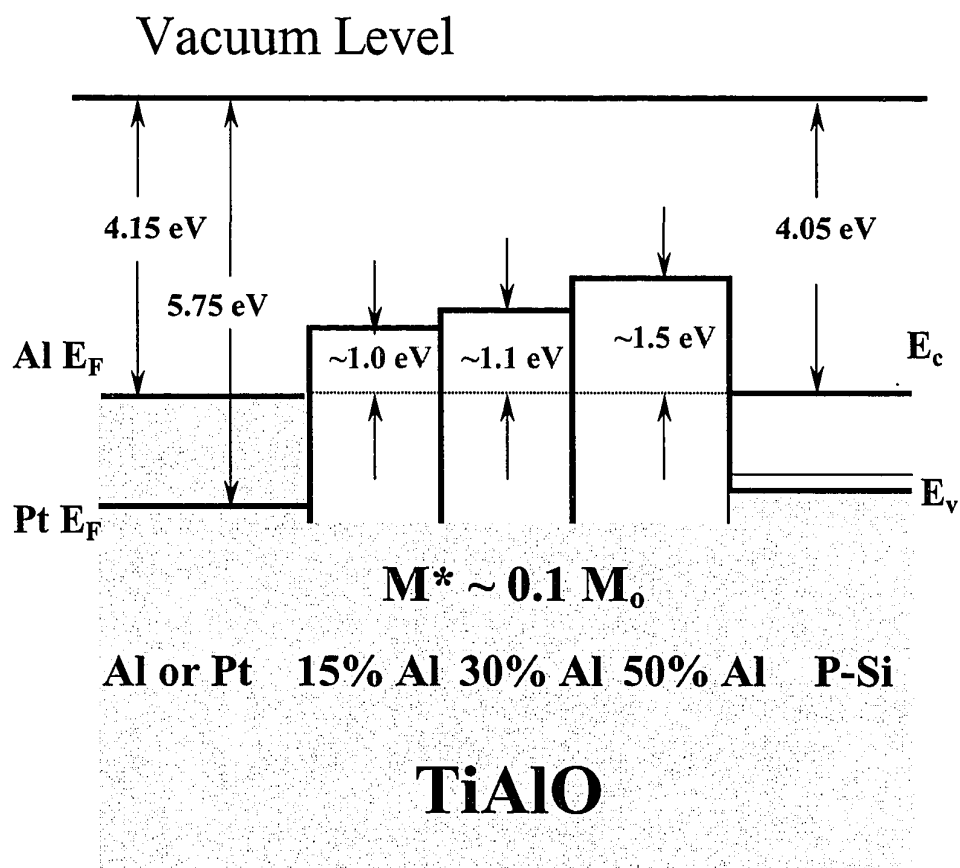


Figure 4.25 Band diagrams of titanium aluminates with 15, 30, and 50 atomic % aluminum concentrations.

## 4.5 Chapter Summary

The barrier heights and conduction mechanisms of several scientifically and technically important materials, such as  $\text{TiO}_2$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{Al}_2\text{O}_3$ , Tungsten,  $\text{ZrO}_2$ , and titanium aluminates have been studied by various methods.

We found that (1) though  $\text{Ta}_2\text{O}_5$  possess as a larger bandgap than that of  $\text{TiO}_2$ , due to its adverse band alignment to Si band,  $\text{Ta}_2\text{O}_5$  only has a barrier height of 0.28 eV over Si conduction band edge, which is much smaller than that of  $\text{TiO}_2$  and is too low to block the thermionic current. Because of the low barrier height, Schottky emission or thermionic emission becomes the dominant conduction mechanism in  $\text{Ta}_2\text{O}_5$ ; (2) Tungsten Fermi-level lies around the mid-gap of Si band, which makes it suitable as the single metal gate for FDSOI or Double-gate CMOS structures; (3) The high barrier height of 3.0 eV for ALD  $\text{Al}_2\text{O}_3$  over Si conduction band edge makes it attractive to reduce leakage current, especially at elevated temperatures; The barrier height of JVD  $\text{ZrO}_2$ /Silicate over Si conduction band edge is reasonably high, which is sufficient to block thermionic current at elevated temperatures; (4) Incorporating Al into  $\text{TiO}_2$  increases the barrier height of  $\text{TiO}_2$  over Si conduction band edge.

## **Chapter 5**

### **Traps and Transconductance Degradation in High-k Gated MOSFET**

As we discussed in Chapter 1, there are three main motivations for or consequences of the scaling of CMOS: a larger circuit density, a higher circuit speed, and smaller power dissipation per circuit. The whole purpose of employing high-k gate dielectrics to replace silicon dioxide can be summarized in one sentence, to reduce the power dissipation (mostly standby power dissipation) of a circuit while maintain the equivalent circuit density and circuit speed. As presented in the former chapters, several high-k gate dielectrics reduce leakage current notably when compared to silicon dioxide. Therefore, the goal of minimizing power dissipation can be achieved. However, besides the process integration

issues, the most difficult issue of implementing high-k gate dielectrics lies on preserving the high drive current or transconductance ( $G_m$ ), which relates to the high circuit speed. In reality, the drive current or transconductance of MOSFET with a high-k gate dielectric is considerably lower than that of MOSFET with silicon dioxide as the gate dielectric<sup>99</sup>. Therefore, instead of using a high-k gate dielectric, we could achieve the equivalent drive current or transconductance by using the silicon dioxide gate dielectric with a larger EOT, which also brings down leakage current. Because of this adverse effect, except for providing a better control of the short channel effect, the major benefits of implementing high-k gate dielectrics are lost.

The high trap density is another major deficiency of high-k gate dielectrics, which results in trap-assisted currents, causes shifts of threshold voltage, and raises serious concerns on reliability. Thus, the high trap density prevents any practical usage of high-k gate dielectrics.

In this chapter, the interface trap density and slow trap density are characterized by the charge pumping method at 77k and room temperature. Moreover, the channel mobile charge density in inversion is measured by the split-CV method. The transconductances of MOSFET's are measured at various temperatures, and their relations with trap densities are studied as well.

Through these studies, we have discovered that the high trap density is strongly correlated to the lowered transconductance, and the loss of carriers in the inversion channel. The degraded carrier mobility is not necessarily the main reason for the degraded channel conductance or transconductance of MOSFET's using high-k gate dielectrics.

## 5.1 Charge Pumping Measurement

The charge pumping technique, introduced by Bruglar and Jespers<sup>143</sup>, is a potent method for the characterization of trap density in a MOSFET. Because it performs directly on small geometry MOSFETs, it is powerful for the trap characterization for sub-micron transistors. Usually it is used to study the interface-trap density. However, not only can the traps located at the interface contribute to the charge pumping current, but also the traps located in the oxide within certain distances from the interface, the slow traps, can contribute to the charge pumping current by communicating with the Si substrate through tunneling<sup>144</sup>.

Using an n-channel MOSFET as an example (Figure 5.1), where a pulse string is applied to the gate of the n-channel MOSFET whose source, drain, and substrate are grounded. A current meter measures the current flowing through the source and drain, and the other current meter measures the current flowing through the substrate. Relevant information of trap density can be derived from either the source/drain current or the substrate current.

The basic physics of the charge pumping technique can be described as follows. During the charge pumping measurement, the base level of the applied gate pulse is set below the flat band voltage while the upper level of the pulse is placed above the threshold voltage of the device. Therefore, the Si channel surface of the measured MOSFET is swept from accumulation to inversion and then back to accumulation during one cycle of the pulse, as shown in Figure 5.2.

If there is no trap, either the total source and drain current or the total substrate current during one cycle of the pulse is zero. However, the presence of traps changes the whole picture. When the channel surface is in accumulation, all trapped electrons are

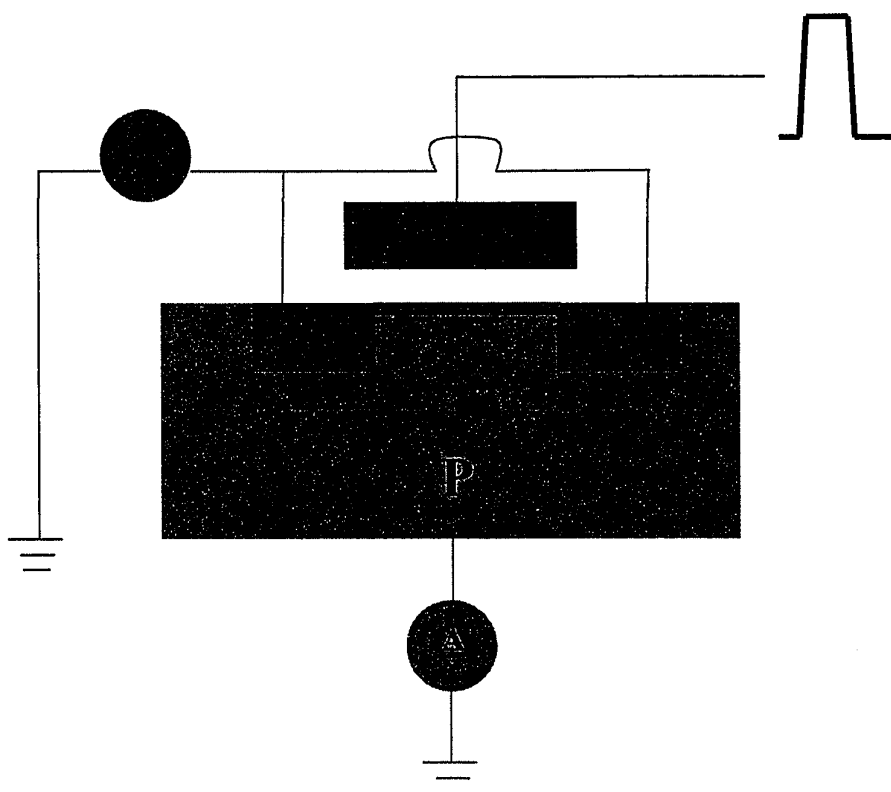
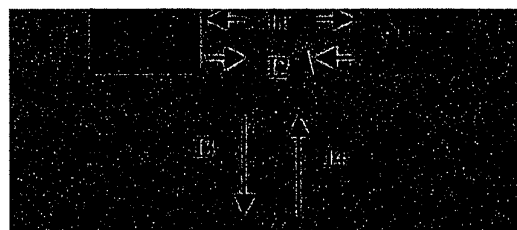
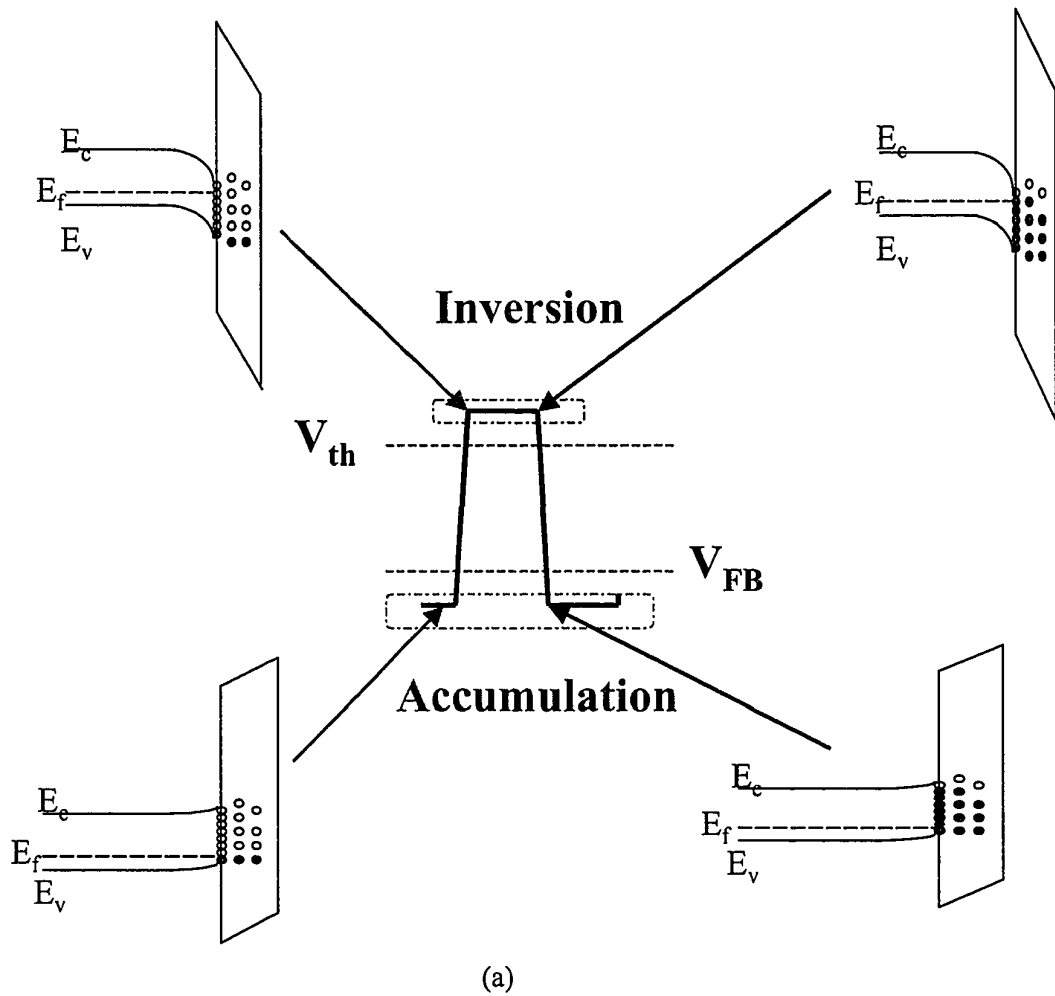


Figure 5.1 Schematic representation of the charge pumping measurement.



$$I_{cp} = I_2 - I_1 = I_4 - I_3$$

Figure 5.2 Origin of the charge pumping current.

located below the Fermi-level. Right after the channel surface is swept from accumulation into inversion, because of the short rising period of the pulse, most traps above the Fermi-level remain unfilled. However, as soon as the channel surface reaches inversion, holes are pushed out, and electrons are rushing into the channel from the source and drain. Therefore, the traps located up to the Fermi-level in inversion are filled in this period, which draws an extra source/drain current. When the channel surface is driven from inversion into accumulation, due to the short transition period, most trapped electrons do not have time to be emitted into the conduction band of Si, and they remain in the traps at the onset of accumulation. At this time, holes are moving from the substrate into the channel region, where they recombine with the trapped electrons, and this recombination process results in an additional substrate current. Therefore, either the source/drain current or the substrate current during one cycle provides the vital information of trap density.

The method used for extracting the interface-trap and slow-trap density is based on Bauza's model<sup>145,146,147</sup>. Using the Shockley-Read-Hall (SRH) statistics, the change of the occupancy factor  $F$  of an interface trap at an energy  $E$  can be described as

$$\frac{dF}{dT} = (1 - F)(c_n + e_p) - F(c_p + e_n), \quad (5.1)$$

where  $c$  is the capture rate,  $e$  is the emission rate, the subscript  $n$  stands for electrons, and  $p$  stands for holes.

If two assumptions, (1) the rise and fall times of the pulse are negligibly small; (2) the electron or hole density at the substrate surface is sufficiently large; are valid, carrier emissions can be neglected. Therefore, Equation 5.1 is reduced to

$$\frac{dF}{dT} = (1 - F)c_n, \quad (5.2)$$

at the upper level of the pulse, and to

$$\frac{dF}{dT} = -c_p F, \quad (5.3)$$

at the base level of the pulse.

During one complete cycle, the maximum occupancy factor occurs at the end of inversion, and the minimum occupancy factor happens at the end of accumulation. The variation of the occupancy factor during one cycle is

$$\Delta F = F_{\max} - F_{\min} = \frac{(1 - \exp(-c_n / 2f))(1 - \exp(-c_p / 2f))}{1 - \exp((-c_n / 2f) - (-c_p / 2f))}. \quad (5.4)$$

Therefore, the charge pumping current can be obtained as

$$\begin{aligned} I_{cp}(f) &= qAf \int_{E_{low}}^{E_{high}} D_{it}(E) \Delta F dE \\ &= qAf \int_{E_{low}}^{E_{high}} D_{it}(E) \frac{(1 - \exp(-c_n / 2f))(1 - \exp(-c_p / 2f))}{1 - \exp((-c_n / 2f) - (-c_p / 2f))} dE \end{aligned}, \quad (5.5)$$

where  $D_{it}(E)$  is the interface trap density,  $q$  is the electron charge,  $A$  is the area of the channel region of a MOSFET,  $E_{high}$  and  $E_{low}$  are the Fermi-levels corresponding to the upper and base levels of the pulse, respectively. Because normally

$$\Delta F = \frac{(1 - \exp(-c_n / 2f))(1 - \exp(-c_p / 2f))}{1 - \exp((-c_n / 2f) - (-c_p / 2f))} \approx 1, \quad (5.6)$$

Equation 5.5 can be simplified as

$$I_{cp} = q^2 Af N_{it}, \quad (5.7)$$

where  $N_{it} = \int_{E_{low}}^{E_{high}} D_{it}(E) dE$ . And the interface-trap density can be calculated as

$$N_{it} = \frac{I_{cp}}{q^2 Af}. \quad (5.8)$$

Moreover, the slow traps located in the oxide can communicate with Si substrate through tunneling, which contributes to an additional charge pumping current. Therefore,

we should accommodate the charge pumping current contributed by the slow traps in the model as well. Using the Heiman and Warfield model<sup>148</sup>, the capture cross sections of electrons and holes are written as

$$\sigma_e(x) = \sigma_e(0) \exp(-x / \lambda_e) , \quad (5.9)$$

and

$$\sigma_p(x) = \sigma_p(0) \exp(-x / \lambda_p) , \quad (5.10)$$

where  $\sigma_e(0)$  and  $\sigma_p(0)$  are the capture cross sections of traps located at the interface; and  $\lambda_e$  and  $\lambda_p$  are the attenuation coefficients for the capture process. Either the electron or the hole capture rate is proportional to its capture cross section. And both decay exponentially with the distance to the interface. Therefore, after considering the contribution from slow traps, the charge pumping current can be written as

$$\begin{aligned} I_{cp}(f) &= qAf \int_{E_{low}}^{E_{high}} \int_0^{D_{ox}} D_{ss} \Delta F dX dE \\ &= qAf \int_{E_{low}}^{E_{high}} \int_0^{D_{ox}} D_{ss} \frac{(1 - \exp(-c_n(x) / 2f))(1 - \exp(-c_p(x) / 2f))}{1 - \exp((-c_n(x) / 2f) - (-c_p(x) / 2f))} dX dE \end{aligned} \quad (5.11)$$

Moreover, because  $\Delta F$  can be approximated by a step function with an effective distance written as

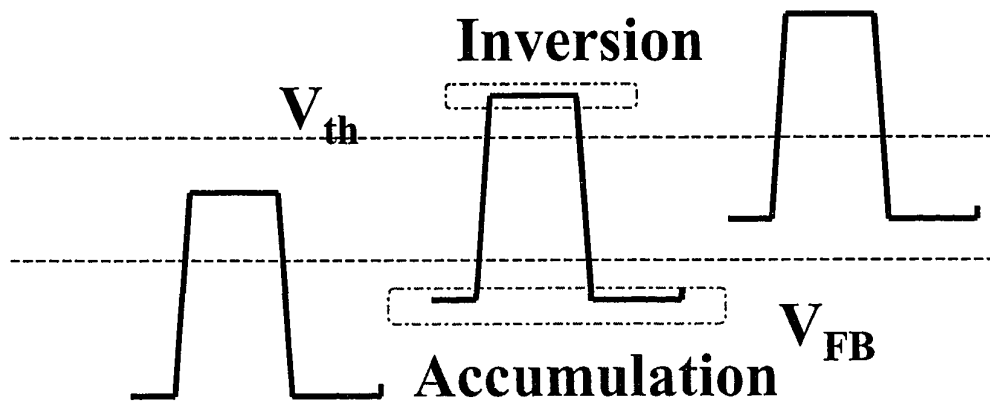
$$X_{eff} = \min[-\lambda_e \ln(c_n(0) / \ln(0.5)2f), -\lambda_p \ln(c_p(0) / \ln(0.5)2f)], \quad (5.12)$$

the total charge pumping current is simplified to

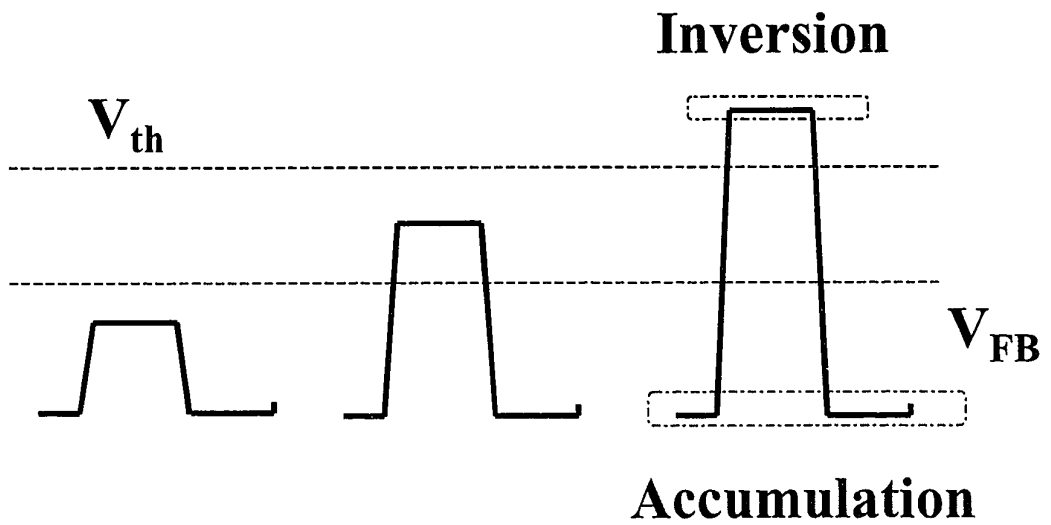
$$I_{cp}(f) = qAf \int_{E_{low}}^{E_{high}} \int_0^{X_{min}} D_{ss} dX dE , \quad (5.13)$$

and the density of slow traps can be obtained from the slope of the  $Q_{cp}$  vs  $\ln(f)$  plot

$$N_{ss} = -\frac{1}{A\lambda q^2} \frac{dQ_{cp}(f)}{d \ln f} , \quad (5.14)$$



(a)



(b)

Figure 5.3 Two patterns of pulse string applied in the charge pumping measurement.

where  $Q_{cp}(f)$  is the measured charge pumping charge, and  $N_{ss}$  is the interface trap density per unit area. In our study, the barrier heights and effective mass for SiO<sub>2</sub> were assumed to extract the effective slow trap densities for various high-k gate dielectrics, which provided a meaningful comparison of trapping properties among different gate dielectrics. Moreover, when the leakage current is high, a high-low frequency method was employed to exclude its influence<sup>149</sup>.

The string of gate pulses used in the charge pumping measurement can have two different patterns, as shown in Figure 5.3. In Pattern A, the amplitude of the pulse remains constant while the base level of the pulse varies from accumulation to inversion. In Pattern B, the base level of the pulse is fixed in accumulation, and the Si surface is driven into inversion with increasing amplitude. We selected Pattern A to perform the charge pumping measurement on MOSFETs with ultra-thin gate dielectrics, because it generates smaller gate leakage currents than that generated by Pattern B during the measurement.

## 5.2 The Effects of Trapping on Transconductance

The low conductance or transconductance in MOSFETs made of high-k films is a major obstacle for implementing high-k gate dielectrics. Without understanding and solving this problem properly, it is hard to imagine that we can place high-k gate dielectrics into any commercial product. The drive current or transconductance of a MOSFET is proportional to the product of carrier mobility and free carrier concentration. Many believe that the greatly degraded carrier mobility is the cause of the degraded drive current or transconductance observed on high-k gate dielectrics, and there has been suggestion that the mobility degradation is an intrinsic problem with high-k gate dielectrics caused by soft phonon scattering<sup>150</sup>. The results of our study reveal the loss of carriers in the inversion

channel playing a significant role in the degraded channel conductance or transconductance in the devices presented here.

### ***5.2.1 Results from MOSFET's with JVD ZrO<sub>2</sub>/silicate as Gate Dielectrics***

ZrO<sub>2</sub> gate dielectrics were deposited by the JVD process at room temperature on HF-last Si wafers. The gate dielectrics received a 600°C/O<sub>2</sub>/5s post-deposition anneal. Both n-channel MOSFETs and p-channel MOSFETs used aluminum as gate electrodes and metal contacts. In order to improve the source and drain contacts, a 3-minute forming gas post-metallization anneal was performed on these devices.

#### **N-channel MOSFET**

The loss of transconductance due to the trapping of free channel carriers by slow traps (border traps)<sup>151</sup> is evidenced by the hysteretic transconductance curve measured at 77K in Figure 5.4, where the “reverse sweep” direction renders the slow traps initially empty above the Fermi-level at a negative voltage, and these slow traps are gradually filled up by trapping electrons in the channel during the subsequent sweep to higher voltages, resulting in a lower transconductance. On the other hand, in the “forward sweep” case the border traps are initially filled up to the Fermi-level at 1.5 V, and the subsequent sweep to lower voltages will involve de-trapping of electrons (only slightly, due to the low temperature), and slightly increased transconductance.

The temperature dependence of the peak G<sub>m</sub> from 77K to 473K is shown in Figure 5.5, where the data from 303K to 473K vary as T<sup>-1</sup> and T<sup>-0.7</sup> for the 1.6 nm (EOT) and the 2.4 nm (EOT) JVD ZrO<sub>2</sub>/silicate samples, respectively, which are different from those of MOSFET with silicon dioxide gate dielectric<sup>7</sup>. Moreover, the relative amplitudes

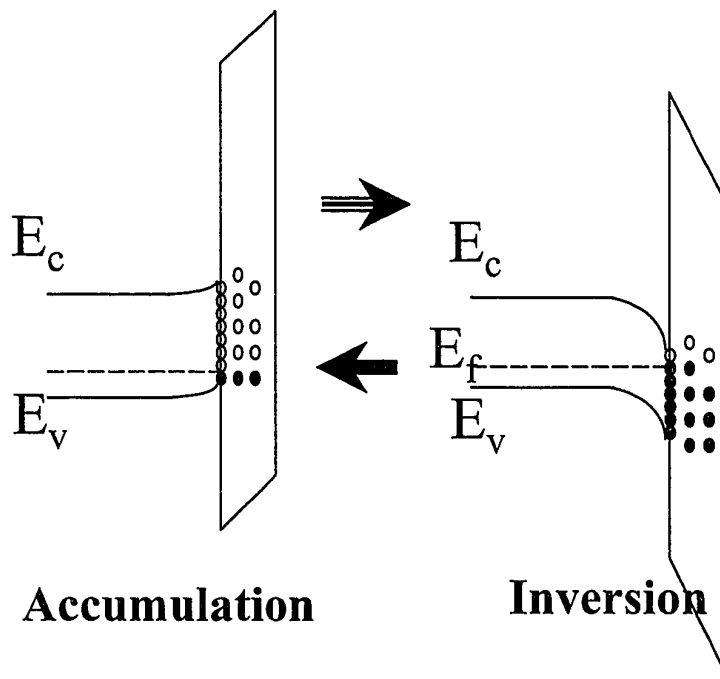
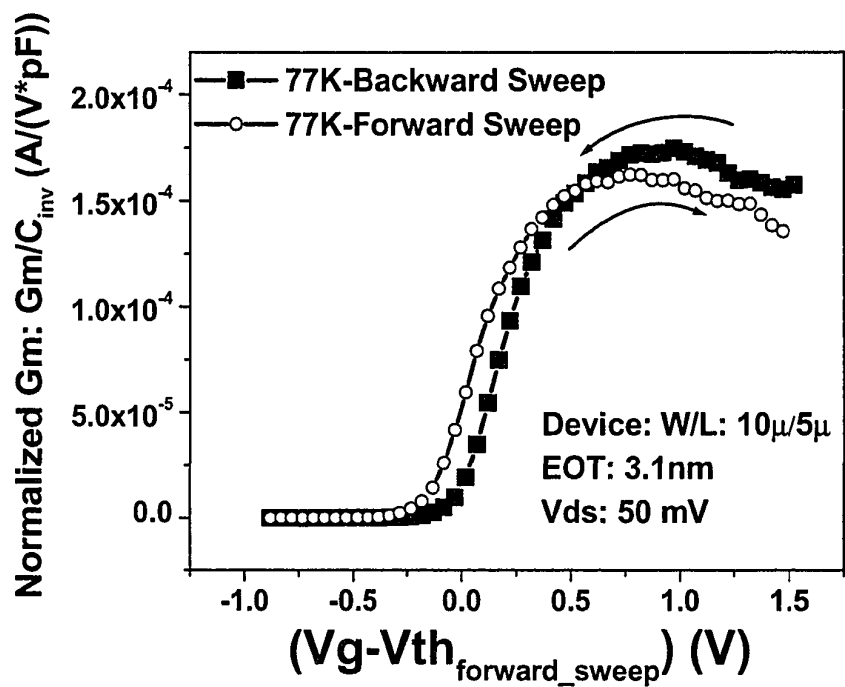


Figure 5.4 Hysteretic Gm curves at 77k resulting from trapping by border traps.

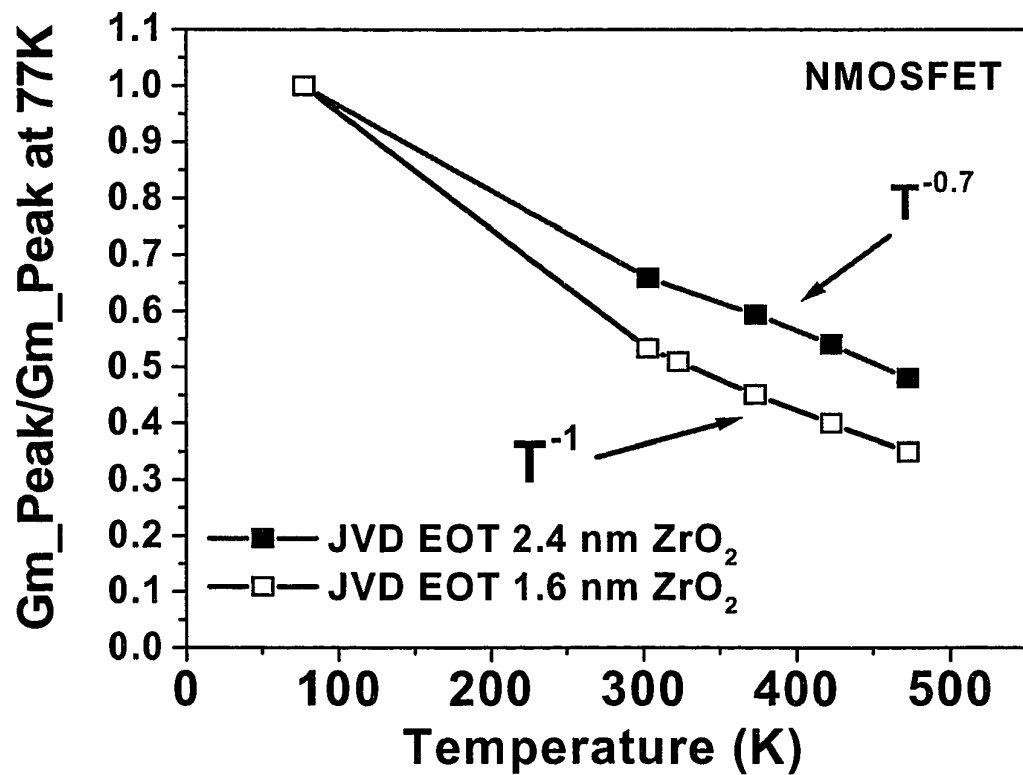


Figure 5.5 Temperature dependence of  $G_{m\_Peaks}$  of JVD  $ZrO_2$  NMOSFETs.

of the increase of transconductance from 303 K to 77 K of these JVD ZrO<sub>2</sub>/silicate devices are only about half of those normally observed on MOSFETs with silicon dioxide as the gate dielectric<sup>7</sup>. The weakened temperature dependence can be attributed to a few reasons, such as temperature-dependent trapping effect, or the weak temperature dependence of remote phonon scattering rate due to the smaller energy of optical phonon modes in ZrO<sub>2</sub> than those in silicon dioxide<sup>152</sup>.

The charge pumping technique was employed to characterize the interface-trap and slow-trap densities, and to study their correlations with transconductance. Figure 5.6 shows some charge pumping results on MOSFETs with JVD ZrO<sub>2</sub>/silicate gate dielectrics at 77k and room temperature. An interface-trap density of  $2\sim 3 \times 10^{11}/\text{cm}^2$  was determined from the maximum charge pumping current measured at 0.5 M Hz. At 77k, the Fermi-level of the p-type Si surface is closer to the valance band than that at room temperature. Therefore, when the Si surface is driven from accumulation to inversion, the Fermi-level sweeps through a larger portion of the Si band gap. Moreover, the thermal emission rate is reduced at 77k. Therefore, the charge pumping current is enhanced at 77k.

Figure 5.7 presents the typical frequency dependence of the charge pumping charges obtained on MOSFETs with JVD ZrO<sub>2</sub>/silicate gate dielectrics, where an average interface trap density of  $4 \times 10^{11}/\text{cm}^2$  was determined at high-frequency end, and a slow trap density of  $2.5 \times 10^{18}/\text{cm}^3$  was determined by applying Equation 5.14. Because of the presence of high-density slow traps, the charge pumping charge increased continuously with lowered frequency.

In order to study the relation between the trapping and transconductance of MOSFET's with JVD ZrO<sub>2</sub>/silicate gate dielectrics, we plot both the interface-trap density and slow-trap density vs. the normalized transconductance peak. And to our surprise, we found that the transconductance degrades almost linearly with both the interface-trap

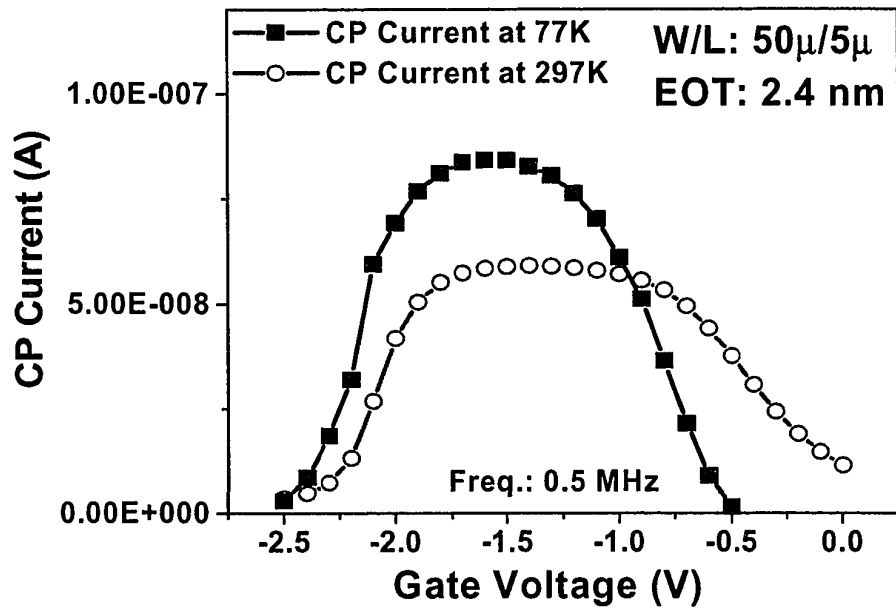


Figure 5.6 Charge pumping currents of JVD ZrO<sub>2</sub> NMOSFETs at room temperature and 77K.

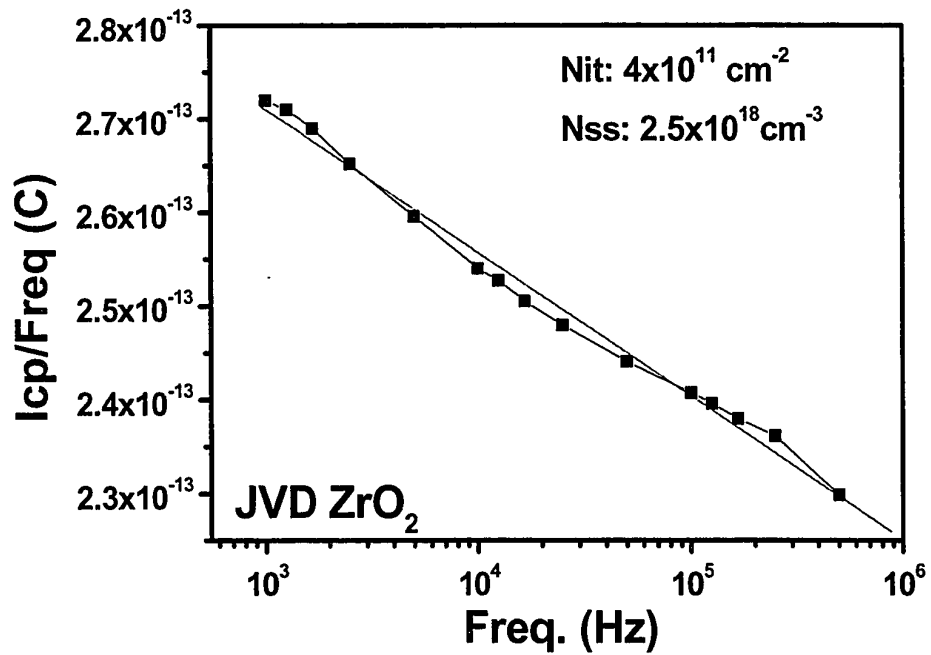


Figure 5.7 Frequency dependence of charge pumping currents of JVD ZrO<sub>2</sub> NMOSFETs at room temperature and 77K.

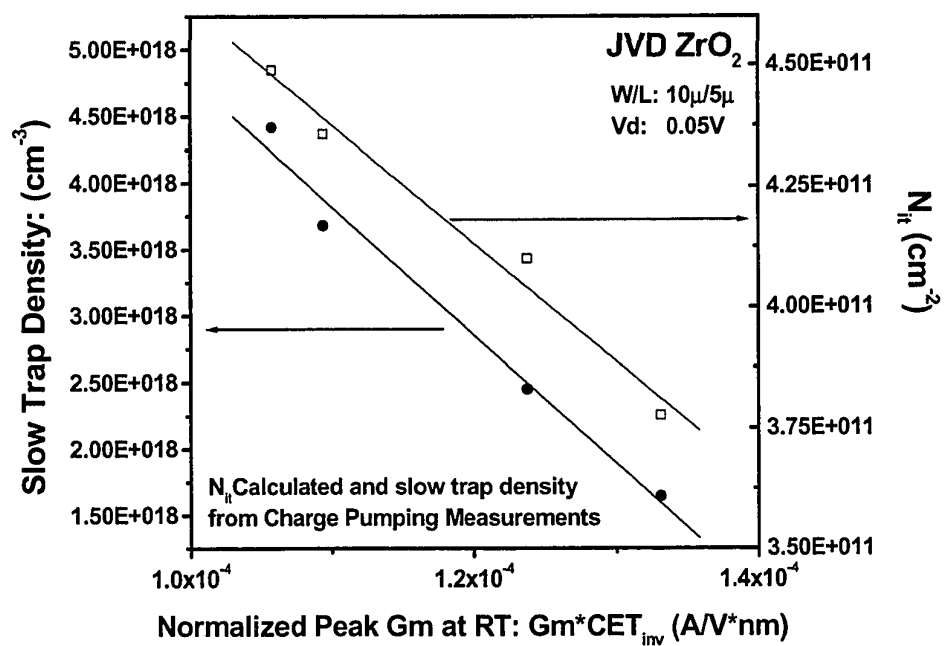


Figure 5.8 Normalized Gm peaks of JVD ZrO<sub>2</sub> NMOSFETs decrease linearly with the interface trap density and slow trap density.

density and the slow-trap density, as shown in Figure 5.8. The linear relationship existing between the normalized transconductance peak and the interface-trap density or the slow-trap density is another strong indication of the significant role that trapping plays in the transconductance degradation.

Moreover, we have employed the split-C-V method to accurately measure the channel carrier density. The split-C-V method is used to obtain the change in channel mobile charges with respect to gate voltage, and the change in bulk charge with respect to gate voltage, respectively<sup>153,154</sup>. Our interest is in using the split-C-V method to obtain the mobile charge density in the inversion channel of a MOSFET. A schematic representation of the split-C-V method is shown in Figure 5.9, where the electron displacement current flowing through the source and drain, and the hole displacement current flowing through the substrate, are measured separately. And the important information of mobile charges can be derived from the source and drain current,

$$I_{d+s} = \frac{dV_g}{dt} \frac{dQ_n}{dV_g}, \quad (5.15)$$

where  $t$  is the time,  $V_g$  is the gate voltage, and  $Q_n$  is the charge on the gate in inversion.

$\frac{dQ_n}{dV_g}$  can be measured as a capacitance. Ideally,  $Q_n$  equals the charge in the inversion channel, and by integrating the capacitance over  $V_g$ , we can obtain the mobile charge. However, when there is significant trapping,  $Q_n$  contains both the trapped charge and the inversion charge, and the approach mentioned above will result in an overestimation of the inversion charge. In order to minimize the effect of trapping<sup>155</sup>, an ideal gate capacitance vs. gate voltage curve can be obtained by first measuring the gate capacitance vs. gate voltage curve from depletion to accumulation, from which one can determine the EOT of gate dielectric as well as its ideal gate capacitance vs. gate voltage curve from depletion to inversion. Therefore, the mobile inversion charge can be obtained from the ideal curve

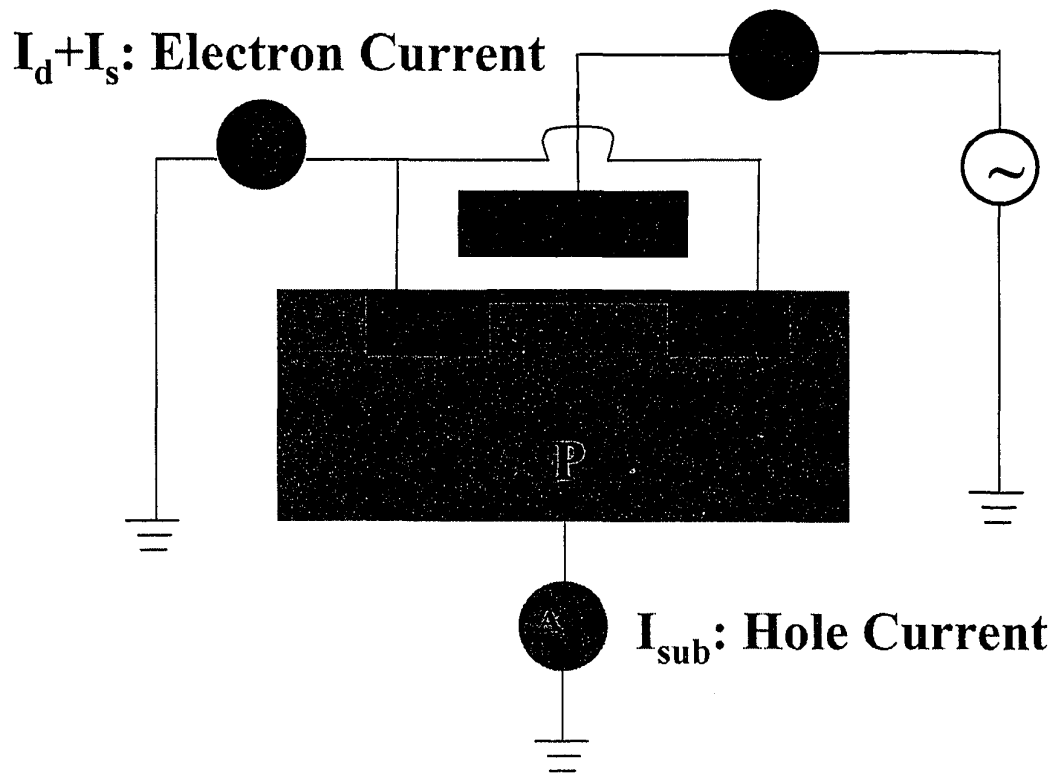


Figure 5.9 Schematic representation of the split-CV measurement.

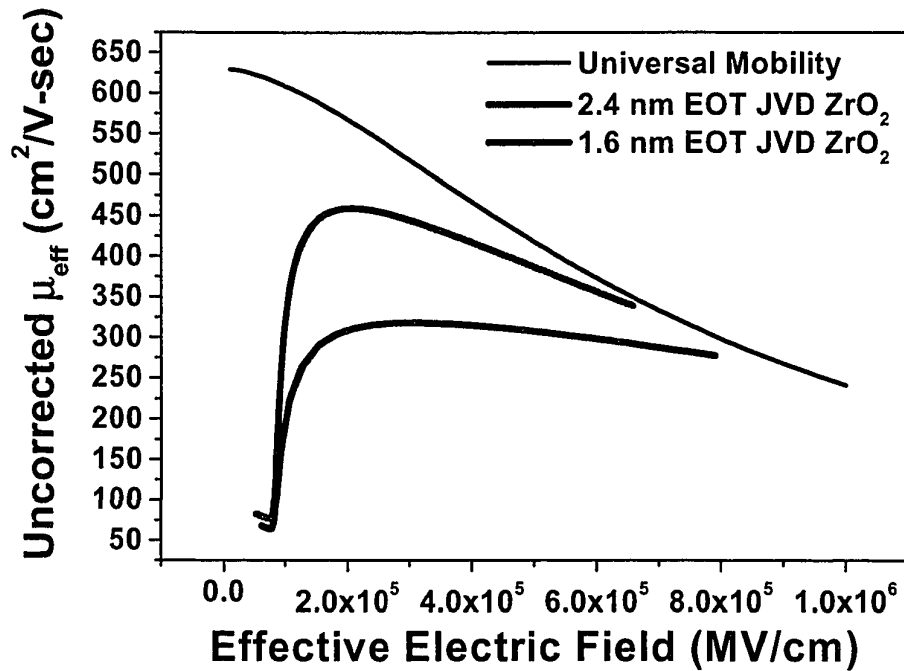


Figure 5.10 Extracted mobilities for NMOSFETs with 2.4 nm and 1.6 nm EOT of JVD ZrO<sub>2</sub>, where  $Q_I = (V_g - V_t)C_{ox}$  was used, which over-estimates the inversion charge.

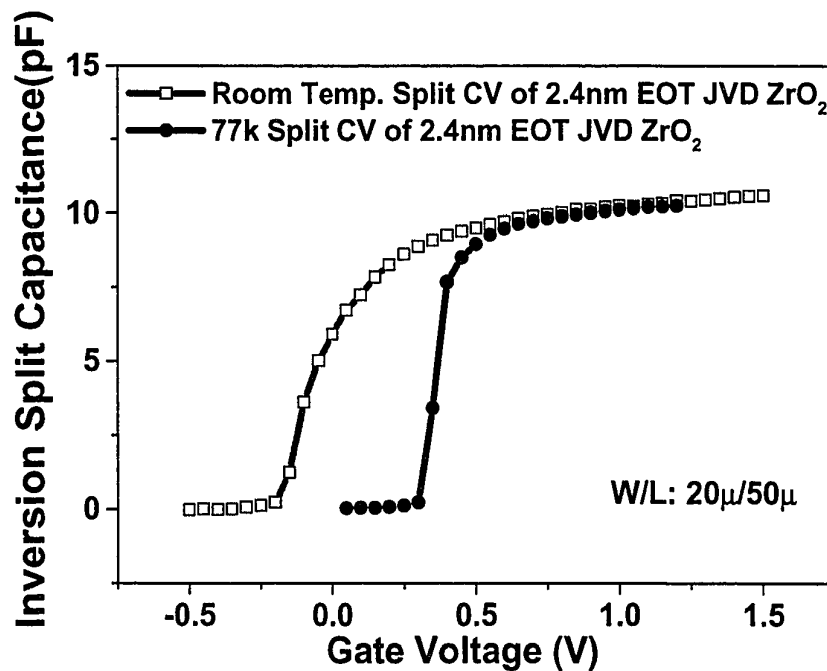


Figure 5.11 Split CVs of JVD ZrO<sub>2</sub> NMOSFET at room temperature and 77K.

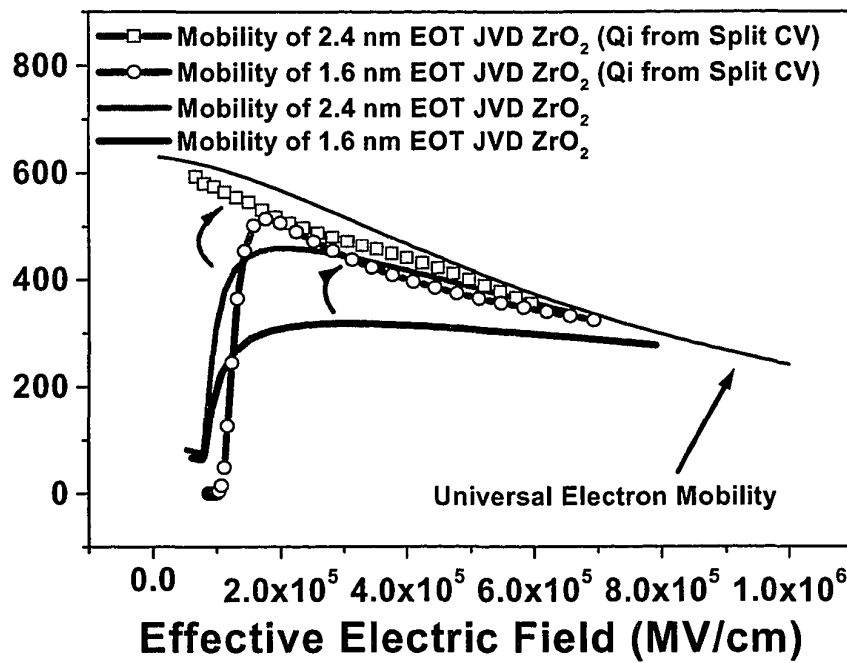


Figure 5.12 Mobilities recover after considering electron loss by trapping.

instead of the experimental curve, and in this way we may be able to eliminate the effect of trapping<sup>155</sup>.

Figure 5.10 shows the extracted apparent mobility for two n-channel MOSFET's with EOT of 1.6nm and 2.4 nm, respectively, where the inversion charge in each sample was calculated by using the equation,  $Q_I = (V_g - V_T) C_{ox}$ . The two JVD ZrO<sub>2</sub>/silicate gate dielectrics were processed the same way, except for the different physical thicknesses, 5 nm and 10nm, respectively. From the physical thickness and EOT, an interfacial layer about 6~7 Å in EOT was extracted, and its composition is Zr silicate-like as we discussed in Chapter 2. These two gate dielectrics have similar interface-trap densities as measured by the charge pumping technique. However, they show dramatically different apparent mobility values, with that of the 1.6 nm device about 30% lower than that of the 2.4 nm device, when one uses  $Q_I = (V_g - V_T) C_{ox}$  for the mobility calculation. However, by using the split-CV data (Figure 5.11) to obtain  $Q_I$  more accurately<sup>153,154</sup>, these two samples almost align with the universal mobility curve for effective fields above  $3 \times 10^5$  V/cm, as shown in Figure 5.12! This example strikingly reveals that the low apparent mobility in these samples is due to the over counting of channel electrons. Since the transconductance is proportional to the product of channel inversion charge and mobility, an over counting of the channel inversion charge would lead to an artificially depressed mobility. The results from these JVD ZrO<sub>2</sub>/silicate MOSFETs reveal that the loss of carriers in the inversion channel is a major reason for the degraded channel conductance or transconductance in the devices reported here.

### P-channel MOSFET

Figure 5.13 shows the hole mobilities at 77K, RT and 473K extracted from a JVD ZrO<sub>2</sub>/silicate p-channel MOSFET, where the room temperature data approach the

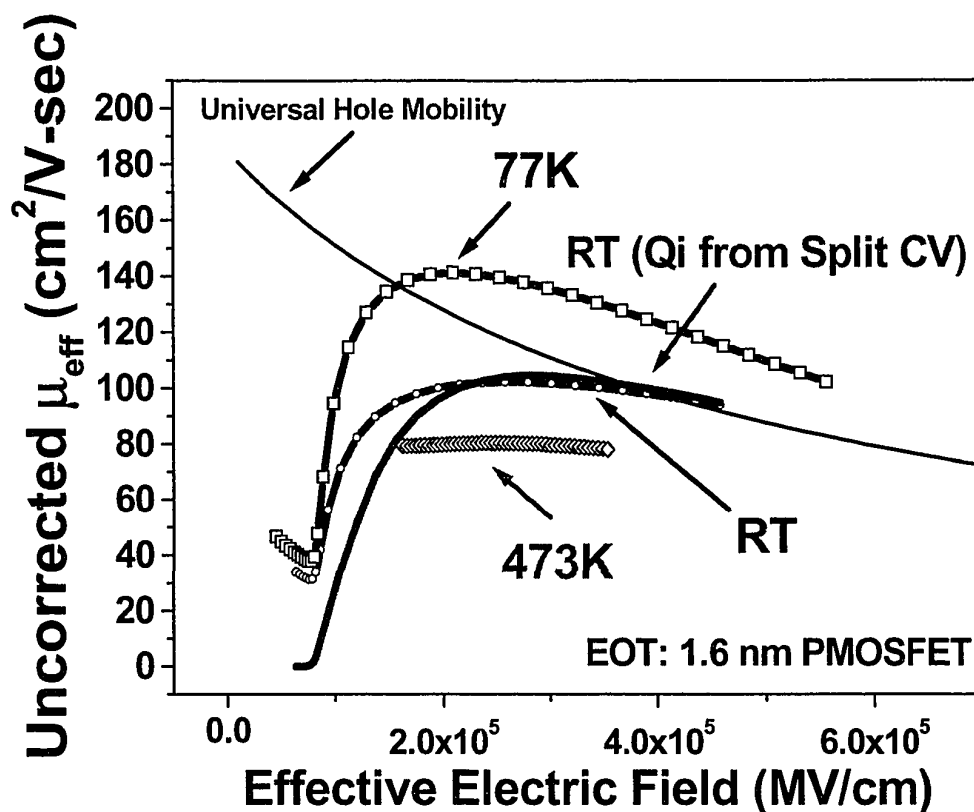


Figure 5.13 Hole mobility at 77k, room temperature, and 473k of PMOSFET with JVD  $\text{ZrO}_2$  gate dielectric.

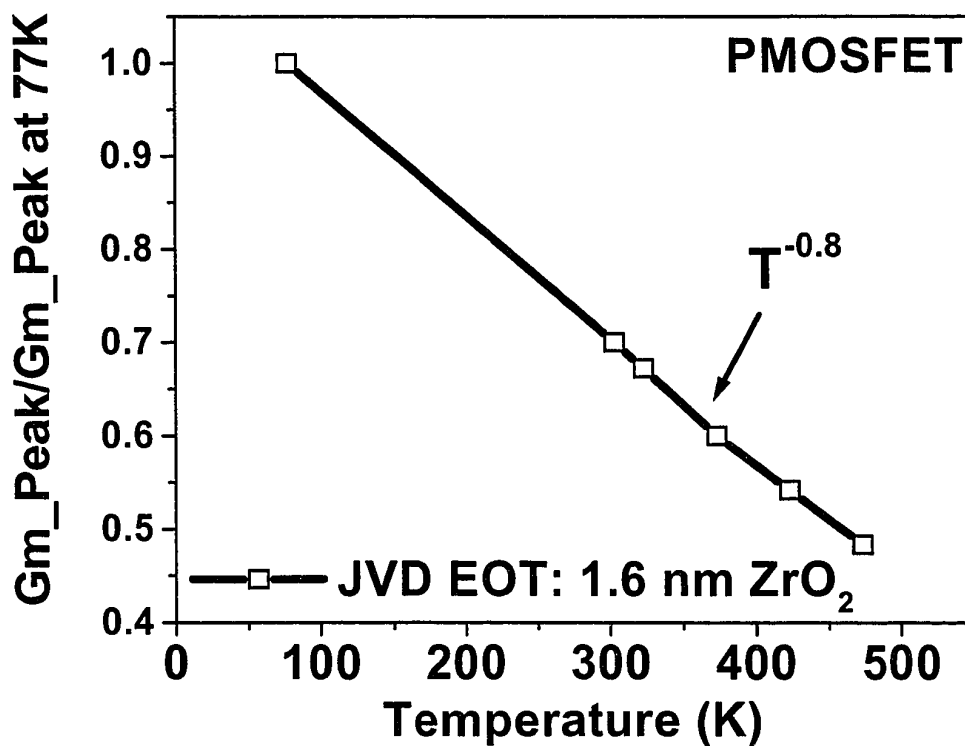


Figure 5.14 Temperature dependence of  $Gm\_Peak$  of JVD  $\text{ZrO}_2$  PMOSFET.

universal curve at high fields, but much lower at low fields even with the correction by using the split-CV data, which suggest different mechanisms for hole mobility.

The temperature dependence of peak  $G_m$  from 77K to 473K for this PMOSFET is shown in Figure 5.14, where the data vary as  $T^{-0.8}$  from 303K to 473K, which is also different from the temperature dependence observed on p-channel MOSFET's with silicon dioxide as the gate dielectric.

### ***5.2.2 Hf-based High-k Gate Dielectrics***

The results from other materials also demonstrate a similar trend. Among numerous high-k gate dielectrics,  $HfO_2$  and other Hf-based materials have emerged as popular candidates, and these Hf-based gate dielectrics have demonstrated many promising properties. But like all other high-k materials, severe trapping and low conductance or transconductance in MOSFETs made of these Hf-based high-k films pose daunting challenges. We have systematically investigated the transconductances at 77k and room temperature of MOSFETs with  $HfO_2$ , Hf silicate ( $HfSiO_x$ ), and Hf aluminate ( $HfAlO_x$ ) gate dielectrics. Moreover, the oxide charge density, interface-trap density and slow-trap density of these Hf-based gate dielectrics have been studied as well. We have found that the MOSFET with Hf silicate gate dielectric showed the highest transconductance at both 77k and room temperature, as well as the lowest trap densities among all the samples studied. On the other hand, the MOSFET with Hf aluminate gate dielectric shows the lowest transconductance and largest trap densities. The transconductance peaks of these three MOSFET's degrade linearly with both the interface-trap and slow-trap densities, which is similar to what we observed on MOSFET's with JVD  $ZrO_2$ /silicate gate dielectric, suggesting that traps may be responsible for the transconductance degradation in MOSFET's with Hf-base high-k gate dielectrics as well.

The fabrication of MOSFET's with these Hf-based high-k gate dielectrics followed a standard process flow until the gate dielectric deposition, and the fabrication of these MOSFET's were done at Motorola. The  $\text{HfO}_2$  and 65 atomic %  $\text{SiO}_2$  Hf silicate were deposited at around 500 °C using MOCVD. The 45 atomic %  $\text{Al}_2\text{O}_3$  Hf aluminate were deposited at 300 °C using the ALD method. Following a gate patterning step, the junctions were implanted and activated using a low temperature anneal. After a Co-silicidation process, a standard CMOS integration process was followed to fabricate the poly-Si/High-k gate stack MOSFET's on bulk Si. All devices used in this study were processed in the identical CMOS integration flow, except the step of gate dielectric deposition.

MOSFET's with 20 Å (EOTinv) Hf silicate, 21 Å (EOTinv)  $\text{HfO}_2$ , and 25 Å (EOTinv) Hf aluminate were used in this study, where the EOTinv refers to the EOT extracted from the inversion capacitance without considering the quantum effect and polysilicon depletion effect. Except for their different gate dielectrics, all MOSFETs used in this study are identical. Figure 5.15 shows the normalized transconductance curves measured at both 77K and room temperature for n-channel MOSFETs with  $\text{SiO}_2$  and the Hf-based high-k gate dielectrics. Obviously the MOSFET with the  $\text{SiO}_2$  gate dielectric has the highest transconductances at room temperature and 77K. At room temperature, The MOSFET's with Hf Silicate and  $\text{HfO}_2$  gate dielectrics have relatively low transconductances, whose peaks are at 80% and 70% of  $G_m$  Peak for the  $\text{SiO}_2$  sample, respectively; the  $G_m$  peak for the sample with the Hf aluminate gate dielectric is much lower, only about 30% of that for the sample with the  $\text{SiO}_2$  gate dielectric. As temperature going down from room temperature to 77K, the  $G_m$  peak for the sample with the  $\text{SiO}_2$  gate dielectric increases 4.4 times, due to the reduced phonon scattering. However, the  $G_m$  peaks for the samples with Hf Silicate,  $\text{HfO}_2$ , and Hf aluminate gate dielectrics only increase 2.7, 2.4 and 2.2 times, respectively, which results in much lower  $G_m$  peaks of MOSFET's with these Hf-based

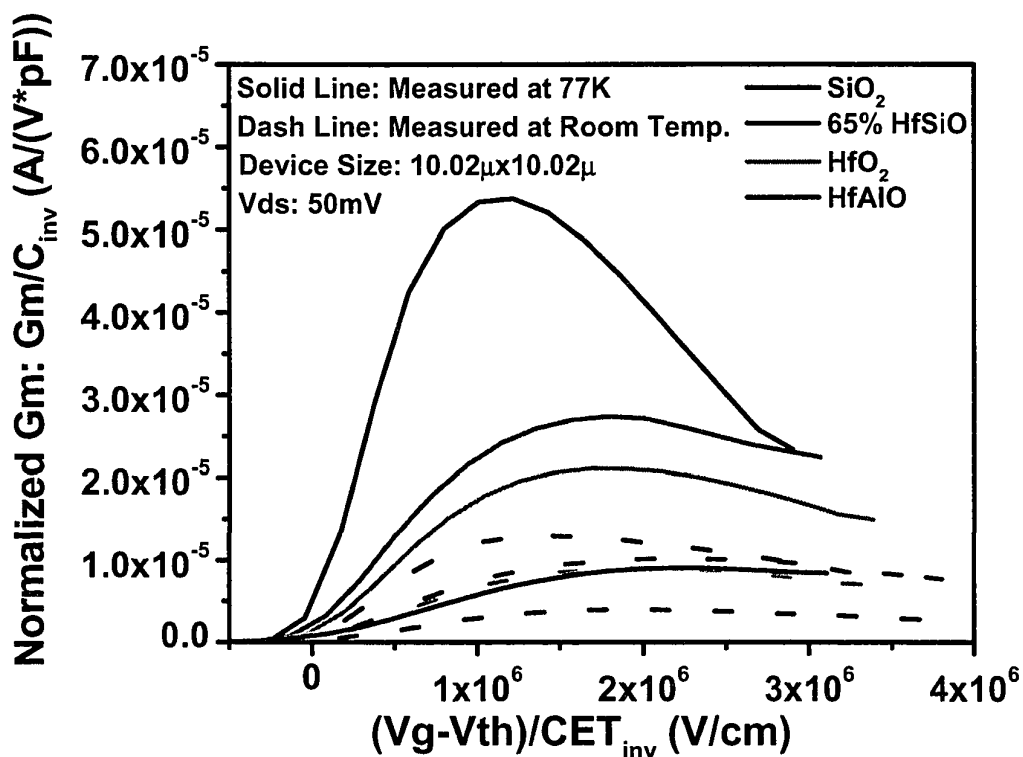


Figure 5.15 Normalized  $G_m$  peaks at 77k and room temperature of NMOSFETs with silicon dioxide and Hf-base gate dielectrics.

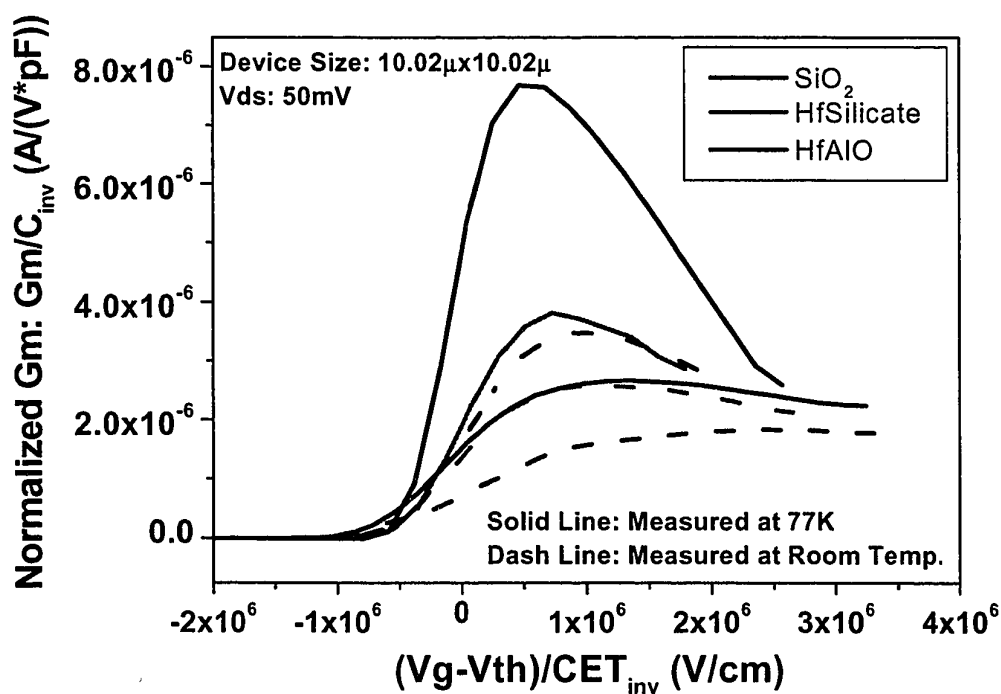


Figure 5.16 Normalized  $G_m$  peaks at 77k and room temperature of PMOSFETs with silicon dioxide and Hf-base gate dielectrics.

high-k gate dielectrics when compared to the  $G_m$  peak of MOSFET with  $\text{SiO}_2$  gate dielectric at 77K.

Similar results were observed on p-channel MOSFET's as well. Figure 5.16 shows the transconductance measured at both 77k and room temperature of MOSFETs with  $\text{SiO}_2$ , Hf silicate, and Hf aluminate gate dielectrics. The data show much stronger temperature dependence for the p-channel MOSFET with  $\text{SiO}_2$  gate dielectric. The  $I_d$ - $V_g$  characteristics of MOSFET's with  $\text{SiO}_2$ , Hf silicate,  $\text{HfO}_2$  and Hf aluminate gate dielectrics measured at both 77k and room temperature are shown in Figure 5.17. Due to the smaller thermal energy at 77K, the subthreshold swings of these MOSFETs measured at 77k are much smaller than those measured at room temperature. At the same temperature, for MOSFETs with similar geometries, the subthreshold swing is a good indicator of the interface-trap density. The subthreshold swing of the MOSFET with Hf aluminate gate dielectric is considerably larger than those of MOSFETs with other gate dielectrics at both 77k and room temperature, which suggests a higher trap density. However, for MOSFETs with  $\text{SiO}_2$ , Hf silicate and  $\text{HfO}_2$  gate dielectrics, their subthreshold swings virtually align with one another, and it is beyond the resolution of the subthreshold method to tell the differences. Therefore, a characterization method with higher precision is necessary to study the trapping properties.

As revealed in Section 5.2.1, trapping may contribute to the degraded transconductance in MOSFETs. Therefore, we employed the charge pumping measurement to study trapping in these Hf-based gate dielectrics and its correlation with transconductance.

In order to study the relationship between trap densities and transconductances in MOSFETs with Hf-based gate dielectrics, we plot their interface-trap densities and slow-trap densities vs. their normalized transconductance peaks, as shown in Figure 5.18. Consistent with the results from MOSFETs with JVD  $\text{ZrO}_2$ /silicate dielectrics, we found

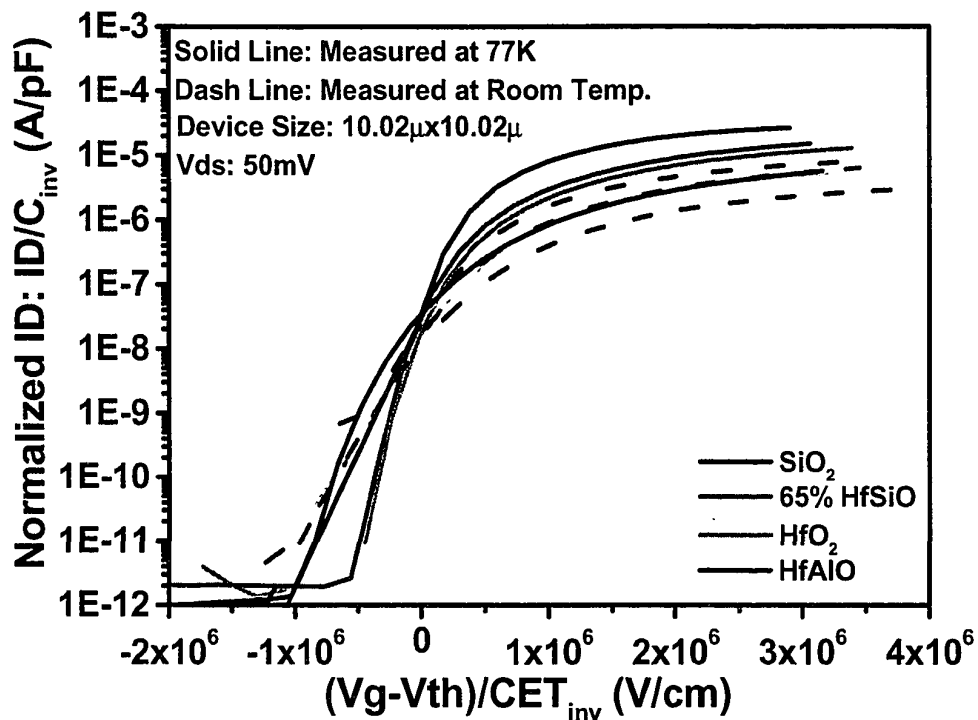


Figure 5.17 Normalized Id-Vg characteristics at 77k and room temperature of NMOSFETs with silicon dioxide and Hf-base gate dielectrics.

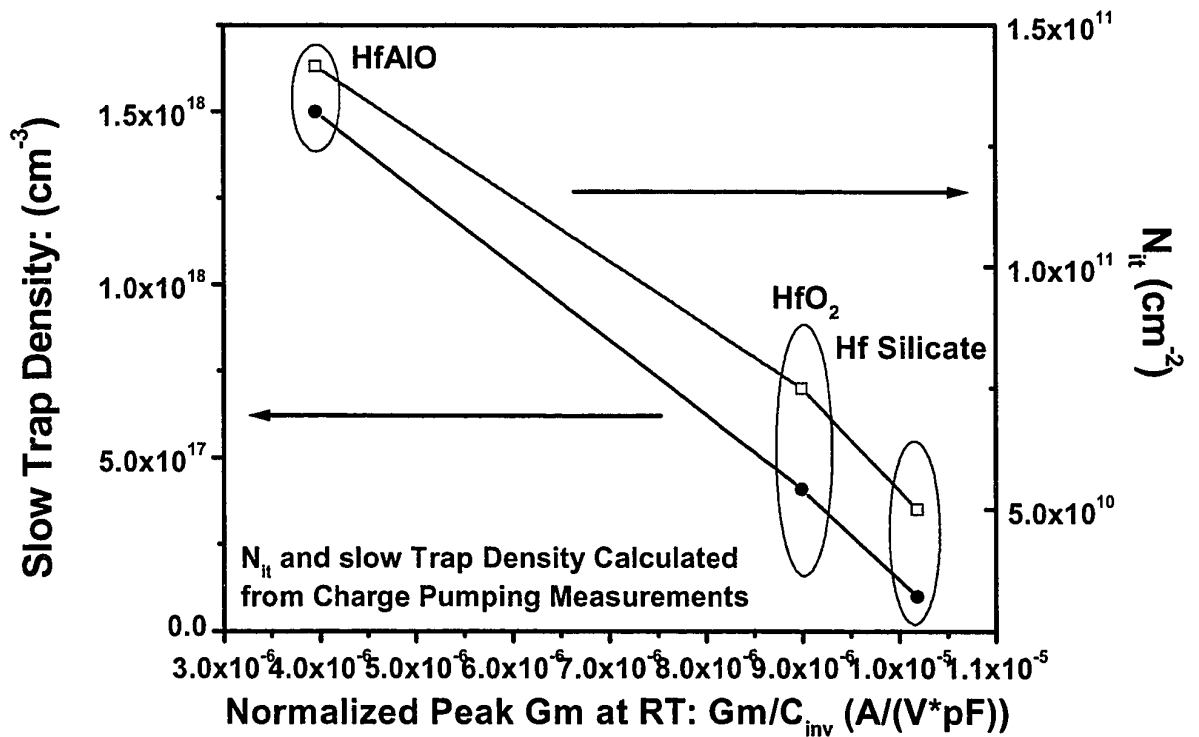


Figure 5.18 Normalized Gm peaks of NMOSFETs with Hf-base gate dielectrics decrease linearly with the interface-trap density and slow-trap density.

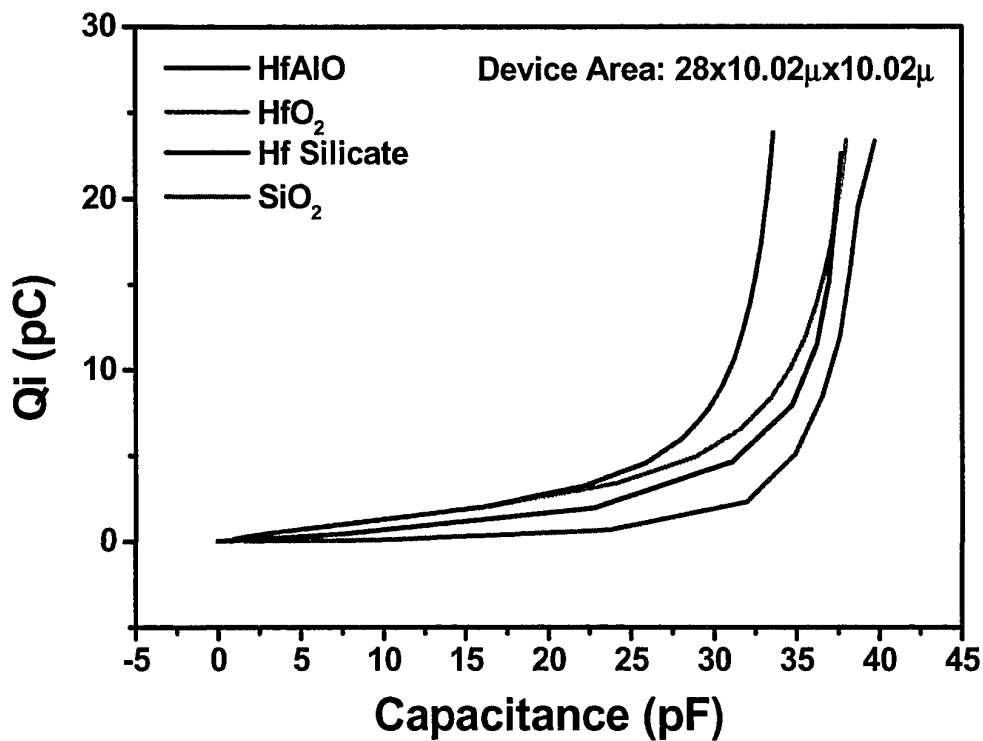


Figure 5.19 Inversion channel charges of NMOSFETs with Hf-based gate dielectrics.

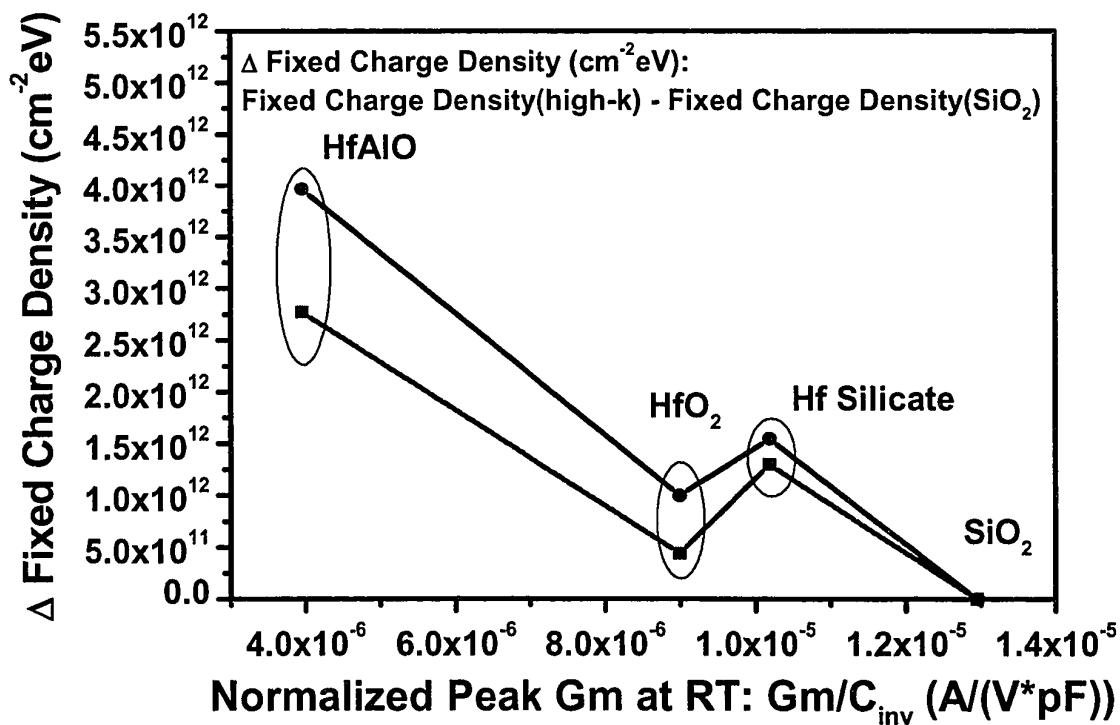


Figure 5.20 Normalized  $G_m$  peaks of NMOSFETs with Hf-base gate dielectrics do not correlate with the negative oxide charge density.

that normalized transconductance peak degraded linearly with both the interface-trap density and the slow-trap density. The linear relationships existing between the transconductance peak and trap densities reveal that traps may be responsible for the transconductance degradation of MOSFET's with these Hf-based gate dielectrics as well. Indeed, with the lowest interface-trap and slow-trap densities, MOSFET with the Hf silicate gate dielectric enjoys the superior transconductance over MOSFETs with HfO<sub>2</sub> and Hf aluminate gate dielectrics.

The inversion charge density vs. capacitance plots for MOSFETs with SiO<sub>2</sub> and Hf-based high-k gate dielectrics, obtained by the split-CV method are shown in Figure 5.19, where the modified split-CV method was used to correct for the trapping effect for the Hf aluminate sample<sup>155</sup>.

We also calculated the negative charge density in these Hf-based high-k gate dielectrics at room temperature and 77k. At 77K many more electrons are “frozen” in the traps than at room temperature, which causes a larger negative charge density. Hf aluminate has the largest increase of negative charge density from room temperature to 77k, followed by HfO<sub>2</sub> and Hf silicate, as shown in Figure 5.20, which again suggests the highest trap density in Hf aluminate, followed by HfO<sub>2</sub> and Hf silicate, as revealed by the charge pumping measurement. Moreover, we plot the negative charge densities vs. the normalized transconductance peaks to study their relationships. However, we found that the normalized transconductance peak is not correlated to the negative charge density. HfO<sub>2</sub> has the smallest negative charge densities at both room temperature and 77k, but its transconductance peaks are not the lowest. It indicates that transconductance is not directly related to the negative charge density.

## 5.3 Chapter Summary

The key findings of this study are (1) it is possible to make MOSFETs with high-k gate dielectrics with mobilities that fit closely to the universal mobility curve, (2) a major portion of the reduced transconductance or conductance can be attributed to trapping, (3) the temperature dependence of the transconductance in MOSFETs with high-k gate dielectrics is much weaker than that of MOSFET with silicon dioxide gate dielectric, (4) among Hf silicate,  $\text{HfO}_2$ , and Hf aluminate, the MOSFET with the Hf silicate gate dielectric shows the highest transconductance and lowest trap densities, (5) the normalized transconductance peaks of MOSFET's with these Hf-base gate dielectrics degrade linearly with both the interface trap-density and slow-trap density, but not correlated to the negative oxide charge density.

## **Chapter 6**

### **Summary and Future Work**

**With silicon dioxide approaching its limits as the gate dielectric for Si CMOS, making suitable ultra-thin high-k gate dielectrics is becoming necessary to develop faster and smaller transistors, creating microchips that work beyond today's barriers. This thesis study is devoted to research and development of ultra-thin high-k gate dielectrics, and the followings summarize the key results of this dissertation, and offers suggestions for future work.**

## 6.1 Summary

Scientifically, this dissertation research focuses on the understanding of many properties of high-k gate dielectrics, such as barrier heights, current conduction mechanisms, and degradation of drive current and transconductance; technically, this dissertation research focuses on developing ultra-thin high-k dielectrics which can extend the scaling limit beyond that provided by silicon dioxide.

Our results show that ultra-thin  $\text{ZrO}_2/\text{Zr}$  silicate films deposited by the JVD process can have EOTs down to 1 nm, and possess high thermal stability, low leakage current, high reliability, among other good electrical properties. Well-behaved n-channel and p-channel MOSFETs with JVD  $\text{ZrO}_2/\text{Zr}$  silicate gate dielectrics have been successfully fabricated. Our analysis also shows that the composition of a JVD film varies with its thickness. Thinner films are found to be Zr-silicate-like whereas thicker films are likely graded with a transition to stoichiometric  $\text{ZrO}_2$ . The presence of a thermally stable Zr silicate interfacial layer may prevent the formation of interfacial silicon oxide, despite the fact that *as-deposited* films are found to be oxygen rich. In contrast to other  $\text{ZrO}_2$  films reported in the literature, the EOTs of our films decrease after post-deposition annealing. From our study, JVD  $\text{ZrO}_2/\text{Zr}$  silicate was found to be able to survive an annealing temperature as high as 1000 °C, suggesting that JVD  $\text{ZrO}_2/\text{silicates}$  can be used in a conventional CMOS process, and no replacement-gate process is needed.

The JVD  $\text{TiO}_2$  gate dielectrics deposited on Si substrate with EOTs down to 1.1 nm (EOT) possess good dielectric properties, as indicated by CV and IV measurements. However, the JVD  $\text{TiO}_2$  gate dielectrics annealed at 800 °C or above show significant degradation of film quality, which raises concerns over its suitability in the conventional CMOS process flow. Moreover, the effects of nano-crystallization on properties of titanium aluminate gate dielectrics haven been investigated, and we have found that the nano-

crystallization results in considerable degradation of transconductance and reliability. Either incorporating Al into  $\text{TiO}_2$  to increase crystallization temperature, or using a high-quality ultra-thin JVD SiN layer to improve interface quality can improve the properties of the gate stack after high temperature annealing. CV and IV results reveal that JVD titanium aluminate gate dielectrics with 15 atomic % aluminum concentration and JVD  $\text{TiO}_2/\text{SiN}$  gate stack can withstand PDA up to 1000 °C.

The barrier height over Si conduction band edge is one of the most important parameters of a high-k dielectric to determine its ability to block leakage current, especially at elevated temperatures. The barrier heights over Si conduction band edge and conduction mechanisms of several scientifically and technically important materials, such as  $\text{TiO}_2$ ,  $\text{Ta}_2\text{O}_5$ ,  $\text{Al}_2\text{O}_3$ ,  $\text{ZrO}_2$ , and titanium aluminates have been studied by various methods, and the Fermi-level of Tungsten has been studied as well.

Our results reveal that (1)  $\text{Ta}_2\text{O}_5$  possesses a larger bandgap than that of  $\text{TiO}_2$ . However, due to its adverse band alignment to Si band,  $\text{Ta}_2\text{O}_5$  only has a barrier height of 0.28 eV over Si conduction band edge, which is much smaller than that of  $\text{TiO}_2$  and is too low to block the thermionic current. Because of the low barrier height, Schottky emission or thermionic emission becomes the dominant conduction mechanism in over the  $\text{Ta}_2\text{O}_5$  barrier; (2) The high barrier height of 3.0 eV for ALD  $\text{Al}_2\text{O}_3$  over Si conduction band edge makes it attractive to reduce leakage current, especially at elevated temperatures; The barrier height of 2.1 eV for JVD  $\text{ZrO}_2/\text{Silicate}$  over the Si conduction band edge is reasonably high, which is sufficient to block thermionic current at elevated temperatures; (3) Incorporating Al into  $\text{TiO}_2$  increases the barrier height of  $\text{TiO}_2$  over the Si conduction band edge; (4) The work function of 4.7 eV for Tungsten makes its Fermi-level to sit around the mid-gap of Si band. Therefore, it is suitable as the single metal gate for FDSOI or Double-gate CMOS structures.

Drive current or transconductance degradation in MOSFETs with high-k gate dielectrics is one of the biggest obstacles for implementing high-k gate dielectrics. Through the course of this dissertation study, we have found that (1) it is possible to make MOSFETs with high-k gate dielectrics with mobilities that fit closely to the universal mobility curve, (2) a major portion of the reduced transconductance or conductance can be attributed to trapping, (3) the temperature dependence of the transconductance in MOSFETs with high-k gate dielectrics is much weaker than that of MOSFET with silicon dioxide gate dielectric, (4) Among MOSFET's with Hf silicate,  $\text{HfO}_2$ , and Hf aluminate, the device with Hf silicate shows the highest transconductance and lowest trap densities, (5) The normalized transconductance peaks of these Hf-base gate dielectrics degrade linearly with both the interface trap density and slow trap density, but not correlated to the negative charge density.

## 6.2 Future Work

It is a daunting job for any high-k gate dielectric to satisfy all the requirements to succeed silicon dioxide. Therefore, there is a long way to go before we can place any high-k gate dielectric into any commercial product. There are many important and interesting issues waiting to be solved, such as process integration issues, reliability issues, etc. Among all the unsolved problems, I would like to highlight three important problems associated with high-k gate dielectrics further, and they are the trapping problem, the mobility degradation problem, and the scalability problem.

## **Trapping**

In my opinion, trapping is the most critical problem for implementing high-k gate dielectrics. It is a do or die problem. The high-density traps in high-k gate dielectrics cause extra trap-assisted currents, especially at elevated temperatures, degradation of the drive current or transconductance in MOSFET, threshold voltage shift, and other reliability issues. All these undesirable consequences of trapping significantly compromise the suitability of high-k gate dielectrics, and only by solving the trapping problem in high-k gate dielectrics, we can have any chance of implementing high-k gate dielectrics in CMOS technology.

Understanding the origin of trapping in high-k gate dielectrics will lay the foundation to solve it successfully. The traps can be divided into interface traps and bulk traps. Interface traps relate to the bonding between Si and high-k gate dielectrics, and bulk traps relate to the bonding in high-k dielectrics. In silicon dioxide or silicon nitride, the bonds are covalence bonds<sup>156</sup>. However, the bonds in metal oxides are ionic bonds. Could this difference contribute to the more severe trapping in high-k dielectrics? Many physical and chemical characterizations accompanied by electrical measurements must be performed to understand the origin of trapping.

With or without understanding the causes of the severe trapping in high-k gate dielectrics, we need to develop engineering solutions, and due to the time constrain, we may have to solve this problem, even before understanding the causes thoroughly. The simplest way to minimize the interface trap density is to insert a layer of silicon dioxide or high-quality SiN between Si and high-k gate dielectrics, though it increases the total EOT. Proper surface treatments and anneals could be effective to reduce both interface trap and bulk trap densities. Developing new materials which do not exist naturally but have good

interface with Si is another way to solve this problem. Finally, we may need to develop innovative device designs and circuit designs to tolerate trapping to certain levels.

### **Mobility Degradation**

Whether or not phonon scattering is more severe in MOSFETs with high-k gate dielectrics than in conventional MOSFET remains debatable. With the presence of high-density traps and charges, the phonon scattering mechanism may be overshadowed by the coulomb scattering mechanism. Therefore, in order to understand the phonon scattering problem in high-k gated MOSFET, besides developing novel mobility characterization methods, we should reduce significantly traps and charges in high-k gate dielectrics. Moreover, from theoretical calculations<sup>150</sup>, phonon scattering is less severe in silicate dioxide gated MOSFETs than in metal oxide-gated MOSFETs. Therefore, for high-performance applications, silicates may be more advantageous than metal oxides.

### **Scalability**

With the EOT of silicon oxynitride gate dielectric approaching 1 nm in the state-of-the-art MOSFET, the EOT of high-k gate dielectrics must be in the same range to be competitive. How to minimize both the interface layer between silicon and high-k gate dielectric, and the interface layer between gate electrodes and high-k gate dielectric is critical for reducing the total EOT. Moreover, in the long term, the dielectric constant of the popular choices, HfO<sub>2</sub> and ZrO<sub>2</sub>, may still be too low. Therefore, we must investigate dielectrics with higher dielectric constants to improve the scalability.

There is a long way to go before finally implementing any high-k gate dielectric in volume production, but because of its importance, enormous resources have been and will

be committed to solve this problem. And I believe that many innovative solutions will be developed to address these difficulties. Hundreds of years ago, glass was a luxury commodity, and only technicians in Venice, Italy could make beautiful bubble-free glassware. Even after massive efforts, technicians in other places still failed to solve the bubble problem. Therefore, some people decided to buy the recipe from Venice. After paying an extremely high price, they got the recipe, but there was only one word on the recipe: Stirring. Just like glass making, maybe after a few simple but innovative solutions, we will be able to use high-k gate dielectrics in commercial products.

## **Appendix**

### **A.1 Constant-Electric Field Scaling Rules**

**Dennard proposed the first set of rules aiming to chart the design of the scaled down MOSFET to control these adverse effects<sup>13</sup>. The constant electric field scaling rules shed the first light on the complicated design issues of CMOS scaling, and opened doors for the more sophisticated scaling rules. The idea behind it is quite simple, but brilliant. For the device operation, ultimately, neither the device dimensions nor the applied voltages, but rather the electric fields define the characteristics of the device. In order for a scaled device to work in a similar manner to its larger version, we must maintain the electric field values and patterns unchanged in the scaled device. To achieve this object, we should scale down both**

the lateral and vertical dimensions of MOSFET. If  $k$  is used as the scaling factor, the gate oxide thickness, channel length and width, and junction depth should be scaled down by a factor of  $k$ . Moreover, in order to reduce the depletion region width by a factor of  $k$  as well, the substrate doping density and source and drain doping density should be scaled up by a factor of  $k$ , and the source to drain voltage and gate voltage should be scaled down by a factor of  $k$ . Therefore, the drive current is scaled down by a factor of  $k$ ; the area/per circuit is scaled down by a factor of  $k^2$ ; the delay time per circuit,  $VC/I$ , is scaled down by a factor of  $k$ ; and power dissipation  $VI$  is scaled down by a factor of  $k^2$ . Table A.1 and Figure A.1 reveal the details of the constant electric field scaling. It's obvious that, following the constant electric field scaling rules to scale down MOSFET, we can achieve a denser and faster circuit with less power consumption.

## A.2 Beyond the Constant-Electric Field Scaling

Though the constant electric field scaling rules provide the basic directions for the MOSFET scaling, in the real world the scaling is more complicated, and it is getting more and more complicated with the fast shrinking dimensions of MOSFET. Several reasons have contributed to the complicated MOSFET scaling. First, rather than changing the voltage to keep the electric fields unchanged, the circuit designers would like to maintain the voltage supply constant between different generations of CMOS technology, which increases the electric fields for each generation. Second, there are a few physical parameters, that are unscalable, such as the bandgap of Si and the thermal voltage,  $kT/q$ . Third, for the recent and future technology generations, it is more difficult to scale down certain elements than others, which further complicates the MOSFET scaling. Therefore, the more generalized scaling rules, such as Baccarani's constant voltage scaling rules<sup>14</sup>,

were proposed. The generalized scaling rules focus on preserving the electric field patterns, rather than the electric field values. By doing so, it enables the gate of the scaled down device to maintain a very similar control over the channel region as that in the larger device, thus reduces the adverse effects coming from the scaled down devices. Table A.2 shows the details of the generalized scaling rules. With the increase of complexity of MOSFET scaling, the worldwide semiconductor industry jointly published the “International Technology Roadmap for Semiconductor (ITRS)” to predict and guide the evolution of the future CMOS technology generations. Table A.3 lists the prediction of CMOS technology up to 2016 from the 2002 update of the ITRS<sup>15</sup>.

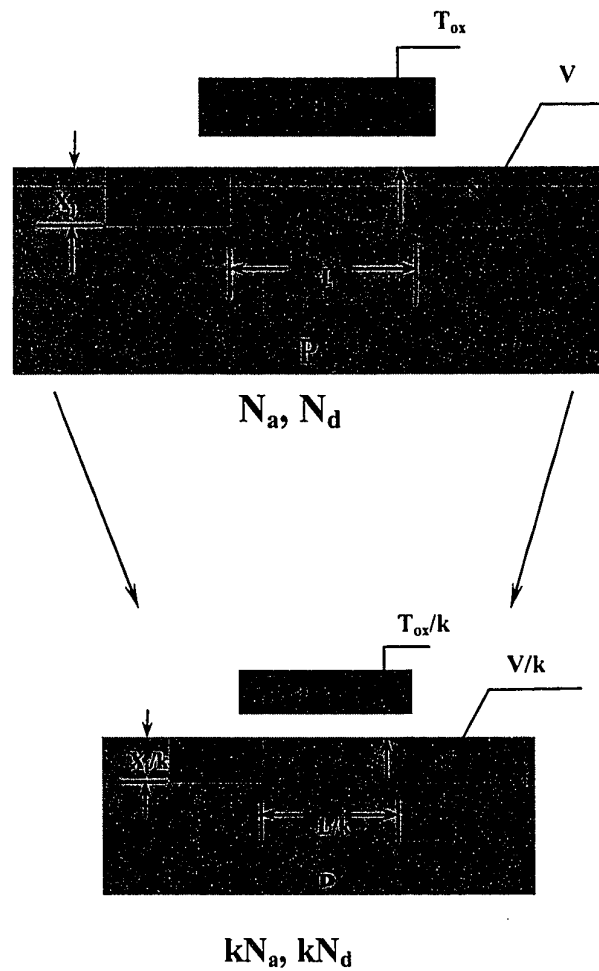


Figure A.1 MOSFETs under constant-electric field scaling rule<sup>13</sup>.

| <i>CMOS Device and Circuit Parameters</i>    |                                                    | <i>Multiplicative Factor (<math>\kappa &gt; 1</math>)</i> |
|----------------------------------------------|----------------------------------------------------|-----------------------------------------------------------|
| <b>Scaling Parameters</b>                    | Device Dimensions ( $T_{ox}$ , $L$ , $W$ , $x_j$ ) | $1/\kappa$                                                |
|                                              | Doping Concentration ( $N_a$ , $N_d$ )             | $\kappa$                                                  |
|                                              | Voltage ( $V$ )                                    | $1/\kappa$                                                |
| <b>Device Characteristics after Scaling</b>  | Electrical Field ( $E$ )                           | 1                                                         |
|                                              | Depletion-Layer Width ( $W_D$ )                    | $1/\kappa$                                                |
|                                              | Capacitance ( $C = \epsilon A / T_{ox}$ )          | $1/\kappa$                                                |
|                                              | Inversion Charge Density ( $Q_i$ )                 | 1                                                         |
|                                              | Dive Current ( $I$ )                               | $1/\kappa$                                                |
| <b>Circuit Characteristics after Scaling</b> | Circuit Delay Time ( $\tau \sim CV/I$ )            | $1/\kappa$                                                |
|                                              | Power Dissipation Per Circuit ( $P \sim VI$ )      | $1/\kappa^2$                                              |
|                                              | Circuit Area                                       | $1/\kappa^2$                                              |

Table A.1 Constant-field Scaling of MOSFET device and circuit parameters<sup>13</sup>

| <i>CMOS Device and Circuit Parameters</i>    |                                                    | <i>Multiplicative Factor (<math>\kappa &gt; 1</math>)</i> |
|----------------------------------------------|----------------------------------------------------|-----------------------------------------------------------|
| <b>Scaling Parameters</b>                    | Device Dimensions ( $T_{ox}$ , $L$ , $W$ , $x_j$ ) | $1/\kappa$                                                |
|                                              | Doping Concentration ( $N_a$ , $N_d$ )             | $\kappa^2$                                                |
|                                              | Voltage ( $V$ )                                    | 1                                                         |
| <b>Device Characteristics after Scaling</b>  | Electrical Field ( $E$ )                           | $\kappa$                                                  |
|                                              | Depletion-Layer Width ( $W_D$ )                    | $1/\kappa$                                                |
|                                              | Capacitance ( $C = \epsilon A / T_{ox}$ )          | $1/\kappa$                                                |
|                                              | Inversion Charge Density ( $Q_i$ )                 | $\kappa$                                                  |
|                                              | Dive Current ( $I$ )                               | $\kappa$                                                  |
| <b>Circuit Characteristics after Scaling</b> | Circuit Delay Time ( $\tau \sim CV/I$ )            | $1/\kappa^2$                                              |
|                                              | Power Dissipation Per Circuit ( $P \sim VI$ )      | $\kappa$                                                  |
|                                              | Circuit Area                                       | $1/\kappa^2$                                              |

Table A.2 Constant-voltage scaling of MOSFET device and circuit parameters<sup>14</sup>.

|                                           | 2004    | 2007    | 2010    | 2013    | 2016    |
|-------------------------------------------|---------|---------|---------|---------|---------|
| <b>Technology generation (nm)</b>         | 90      | 65      | 45      | 32      | 22      |
| <b>High Performance Logic Technology</b>  |         |         |         |         |         |
| <b>Gate length (nm)</b>                   | 37      | 25      | 18      | 13      | 9       |
| <b>EOT(physical) (nm)<sup>(a)</sup></b>   | 0.9-1.4 | 0.6-1.1 | 0.5-0.8 | 0.4-0.6 | 0.4-0.5 |
| <b>EOT(electrical) (nm)<sup>(b)</sup></b> | 2       | 1.4     | 1.2     | 1       | 0.9     |
| <b>Supply Voltage (V)</b>                 | 1       | 0.7     | 0.6     | 0.5     | 0.4     |
| <b>Low Standby Power Technology</b>       |         |         |         |         |         |
| <b>Gate length (nm)</b>                   | 53      | 32      | 22      | 16      | 11      |
| <b>EOT(physical) (nm)<sup>(a)</sup></b>   | 1.4-1.8 | 1.0-1.4 | 0.8-1.2 | 0.7-1.1 | 0.6-1.0 |
| <b>EOT(electrical) (nm)<sup>(b)</sup></b> | 2.4     | 1.7     | 1.5     | 1.4     | 1.3     |
| <b>Supply Voltage (V)</b>                 | 1.1     | 0.9     | 0.8     | 0.7     | 0.6     |

(a) EOT(physical) only accounts for the EOT value of the gate dielectric.

(b) EOT(electrical) accounts for the EOT values of the gate electrode depletion, inversion layer quantum effect and gate dielectric.

Table A.3 The future CMOS technology generations from 2002 update of the ITRS<sup>15</sup>.

## Bibliography

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<sup>1</sup> J.E. Lilienfeld, U.S. Patent 1,745,175, 1930

<sup>2</sup> O. Heil, British Patent 439,457, 1935

<sup>3</sup> D. Kahng and M. M. Atalla, "Silicon-Silicon Dioxide Field Induced Surface Devices," presented at the IRE-AIEE Solid-State Device Research Conference, Carnegie Institute of Technology, 1960.

<sup>4</sup> F. M. Wanlass and C. T. Sah, "Nanowatt Logic Using Field-Effect Metal-Oxide Semiconductor Triodes," IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 32-33, 1963.

<sup>5</sup> J. C. Sarace, R. E. Kerwin, D. L. Klein, and R. Edwards, "Metal-Nitride-Oxide-Silicon Field Effect Transistors with Self-Aligned Gate," J. Solid-State Electron. 11 pp. 653-660, 1968.

<sup>6</sup> G. E. Moore, "Cramming more components onto integrated circuits," Electronics, Vol. 38, N. 8, Apr., 1965.

<sup>7</sup> Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*: Cambridge University Press, 1998.

<sup>8</sup> SIA, *The national technology roadmap for semiconductors technology needs*: Semiconductor Industry Associations (SIA), 1994.

<sup>9</sup> SIA, *The national technology roadmap for semiconductors technology needs*: Semiconductor Industry Associations (SIA), 1997.

<sup>10</sup> S. Yang, S. Ahmed, B. Arcot, R. Arghavani, P. Bai, S. Chambers, P. Charvat, P. Cotner, R. Gasser, T. Ghani, M. Hussein, C. Jan, C. Kardas, J. Maiz, P. McGregor, B. McIntyre, P. Nguyen, P. Packan, I. Post, S. Sivakumar, J. Steigerwald, "A high performance 180 nm generation logic technology," *IEDM Tech. Digest*, pp. 197-200, 1998.

<sup>11</sup> T. Ghani, S. Ahmed, P. Aminzadeh, J. Bielefeld, P. Charvat, C. Chu, M. Harper, P. Jacob, C. Jan, J. Kavalieros, C. Kenyon, R. Nagisetty, P. Packan, J. Sebastian, M. Taylor, J. Tsai, S. Tyagi, S. Yang, M. Bohr, "100 nm gate length high performance/low power CMOS transistor structure," *IEDM Tech. Digest*, pp. 415-418, 1999.

<sup>12</sup> S. Tyagi, M. Alavi, R. Bigwood, T. Bramblett, J. Brandenburg, W. Chen, B. Crew, M. Hussein, P. Jacob, C. Kenyon, C. Lo, B. McIntyre, Z. Ma, P. Moon, P. Nguyen, L. Rumaner, R. Schweinfurth, S. Sivakumar, M. Stettler, S. Thompson, B. Tufts, J. Xu, S. Yang and M. Bohr, "A 130 nm generation logic technology

featuring 70 nm transistors, dual Vt transistors and 6 layers of Cu interconnects," *IEDM Tech. Digest*, pp. 567-570, 2000.

<sup>13</sup> R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 256-268, 1974.

<sup>14</sup> G. Baccarani, M. R. Wordeman, and R. H. Dennard, "Generalized scaling theory and its application to a ¼ micronmeter MOSFET design," *IEEE Transaction on Electron Devices*, vol. 31, pp. 452, 1984.

<sup>15</sup> International Technology Roadmap for Semiconductors (ITRS), 2002 update, Semiconductor Industry Associations, 2002

<sup>16</sup> R. Chau, J. Kavalieros, B. Roberds, R. Schenker, D. Lionberger, D. Barlage, B. Doyle, R. Arghavani, A. Murthy, and G. Dewey, "30 nm Physical Gate Length CMOS Transistors with 1.0 ps n-MOS and 1.7 ps p-MOS Gate Delays," *IEDM Tech. Digest*, pp. 45-48, 2000.

<sup>17</sup> E. Merzbacher, *Quantum Mechanics*: John Wiley & Sons, 1970.

<sup>18</sup> S. M. Sze, *Physics of Semiconductor Devices*: John Wiley & Sons, 1981.

<sup>19</sup> S.-H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultra-thin-oxide nMOSFET's," *IEEE Electron Device Lett.*, vol. 18, pp. 209-211, 1997.

<sup>20</sup> C. Y. Wang, "Doping of n+ and p+ polysilicon in dual-gate CMOS process," *1988 IEDM, Technical Digest*, pp. 238, 1988.

<sup>21</sup> Z. Zhou and D. K. Shroder, "Boron penetration in dual gate process technology," *Semiconductor International*, pp. 98, 1998.

<sup>22</sup> J. R. Pfister, F. K. Bake, T. C. Mele, H. H. Tseng, P. J. Tobin, J. D. Hayden, J. W. Miller, C. D. Gunderson, and L. C. Parrillo, "The effects of Boron penetration on p+ polysilicon gates MOS devices," *IEEE Trans. Electron Devices*, vol. 37, pp. 1842, 1990.

<sup>23</sup> B. Y. Kim, I. M. Liu, H. F. Luan, M. Gardner, J. Fulford, and D. L. Kwong, "Impact of boron penetration on gate oxide reliability and device lifetime in p+ polysilicon p-MOSFETs," *IEDM Tech. Digest*, pp. 463-466, 1997.

<sup>24</sup> C. R. Barrett and R. C. Smith, "Failure modes and reliability of dynamic RAMs," presented at IEEE International Electron Devices Meeting (IEDM '76), 1976.

<sup>25</sup> I. C. Chen, S. E. Hollan, and C. Hu, "Electrical breakdown in thin gate and tunneling oxides," *IEEE Trans. Electron Devices*, vol. 32, pp. 273, 1985.

<sup>26</sup> D. J. DiMaria and J. Stasiak, "Trap creation in silicon dioxide produced by hot electrons," *J. Appl. Phys.*, vol. 65, pp. 2342, 1989.

<sup>27</sup> K. F. Scheugraf and C. Hu, "Hole injection SiO<sub>2</sub> breakdown model for very low voltage lifetime extrapolation," *IEEE Trans. Electron Devices*, vol. 41, pp. 761, 1994.

<sup>28</sup> J. H. Stathis, "Reliability limits for the gate insulator in CMOS Technology," *IBM Journal of Research and Development*, vol. 46, No. 2/3, pp. 265-286, March/May, 2002.

<sup>29</sup> J. Sune, E. Wu, "Statistics of successive breakdown events for ultra-thin gate oxides," *IEDM Tech. Digest*, pp. 147-150, 2002.

<sup>30</sup> I. C. Chen, S. E. Hollan, K. K. Young, C. Chang, and C. Hu, "Substrate Hole Current and Oxide Breakdown," *Appl. Phys. Lett.* 49, pp. 669-671, 1986.

<sup>31</sup> J. C. Lee, I. C. Chen, and C. Hu, "Modeling and Characterization of Gate Oxide Reliability," *IEEE Trans. Electron Devices* 35, pp. 2268-2278, 1988.

<sup>32</sup> J. W. McPherson and H. C. Mogul, "Underlying Physics of the Thermochemical E Model in Describing Low-Field Time-dependent Breakdown in SiO<sub>2</sub> Thin Films," *J. Appl. Phys.* 84, pp. 1513-1523, 1988.

<sup>33</sup> J. W. McPherson and R. B. Khamankar, "Molecular Model for Intrinsic Time-Dependent Dielectric Breakdown in SiO<sub>2</sub> Dielectrics and the Reliability Implications for Hyper-Thin Gate Oxide," *Semicond. Sci. Technol.* 15, pp. 462-470, 2000.

<sup>34</sup> J. H. Stathis, "Percolation Models for Gate Oxide Breakdown," *J. Appl. Phys.* 86, pp. 5757-5766, 1999.

<sup>35</sup> M. A. Alam, J. D. Bude, B. Weir, P. Silverman, A. Ghetti, D. Monroe, K. P. Cheung, and S. Moccio, "An Anode Hole Injection Percolation Model for Oxide Breakdown – the 'Doom's Day Scenario Revisited,'" *IEDM Tech. Digest*, pp. 715-718, 1999.

<sup>36</sup> M. A. Alam, B. E. Weir, P. J. Silverman, J. D. Bude, A. Ghetti, Y. Ma, M. M. Brown, D. Hwang, and A. Hamad, "Physics and Prospects of Sub-2nm Oxides," *The Physics and Chemistry of SiO<sub>2</sub> and the Si-SiO<sub>2</sub>*

- Interface – 4, Vol. 2000-2, H. Z. Massoud, I. J. R. Baumvol, M. Hirose, and E. H. Poindexter, Eds., The Electrochemical Society, Pennington, NJ, pp. 365-376, 2000.
- <sup>37</sup> M. L. Green, E. P. Gusev, R. Degraeve, and E. L. Garfunkel, "Ultrathin (< 4nm) SiO<sub>2</sub> and Si-O-N Gate Dielectric layers for Silicon Microelectronics: Understanding the Processing, Structure, and Physical and Electrical Limits," *J. Appl. Phys.* 90, pp. 2057-2121, 2001.
- <sup>38</sup> B. E. Weir, M. A. Alam, J. D. Bude, P. J. Silverman, A. Ghetti, F. Baumann, P. Diodato, D. Monroe, T. Sorsch, G. L. Timp, Y. Ma, M. M. Brown, A. Hamad, D. Hwang, and P. Mason, "Gate Oxide Reliability Projection to the Sub-2nm Regime," *Semicond. Sci. Technol.* 15, pp. 455-461, 2000.
- <sup>39</sup> P. D. Agnello, "Process Requirements for continued scaling of CMOS – the need and prospects for atomic-level manipulation," *IBM Journal of Research and Development*, vol. 46, No. 2/3, pp. 317-338, March/May, 2002.
- <sup>40</sup> M. M. Heyns, T. Bearda, I. Cornelissen, S. D. Gendt, R. Degraeve, G. Groeseneken, C. Kenens, D. M. Knotter, and L. M. Loewensein, "Cost-effective cleaning and high quality thin gate oxides," *IBM J. Res. Develop.*, vol. 43, pp. 339, 1999.
- <sup>41</sup> C. T. Liu, F. H. Baumann, A. Ghetti, H. H. Vuong, C. P. Chang, K. P. Cheung, J. I. Colonell, W. Y. C. Lai, E. J. Lloyd, J. F. Miner, C. S. Pai, H. Vaidya, R. Liu, and J. T. Clemens, "Sever thickness variation of sub-3 nm gate oxide due to Si surface faceting, poly-Si intrusion, and corner stress," presented at Symposium on VLSI Technology, Kyoto, Japan, 1999.
- <sup>42</sup> C. B. Duke, "Tunneling in Solids," Academic Press: New York and London, 1969.
- <sup>43</sup> J. G. Simmons, "Generalized formula for the electrical tunneling effect between similar electrodes separated by a thin insulating film," *J. Appl. Phys.*, vol. 34, no. 6, pp. 1793, 1963.
- <sup>44</sup> A. Sommerfeld and H. Bethe, "Handbuch der physik von geiger scheel," vol. 24/2, pp. 450, Julius Spring-Verlag, Berlin, 1933.
- <sup>45</sup> R. H. Fowler and L. Nordheim, *Proc. Roy. Soc.(London)*, A119, pp. 173, 1928.
- <sup>46</sup> H. S. Momose, T. Morimoto, Y. Ozawa, K. Yamabe, and H. Iwai, "Electrical characteristics of rapid thermal nitrided-oxide gate n- and p-MOSFET's with less than 1 atom% nitrogen concentration," presented at IEEE International Electron Devices Meeting (IEDM '96), San Francisco, 1995
- <sup>47</sup> H. C. Lu, E. P. Gusev, T. Gustafson, M. L. Green, D. Brasen, and E. Garfunkel, "Compositional and mechanistic aspects of ultra thin oxynitride film growth on Si(100)," *Microelectron. Eng.*, vol. 36, pp. 29, 1997.
- <sup>48</sup> A. B. Joshi, J. Ahn, and D. L. Kwong, "Oxynitride gate dielectrics for p+ polysilicon gate MOS devices," *IEEE Electron Device Letters*, vol. 14, pp. 560, 1993.
- <sup>49</sup> T. Matsuoka, "Hot carrier induced degradation of N<sub>2</sub>O-oxynitride gate oxide NMOSFET's," *IEEE Trans. Electron Devices*, vol. 43, pp. 1364, 1996.
- <sup>50</sup> E. Cartier, D. A. Buchanan, and G. J. Dunn, "Atomic Hydrogen-induced interface degradation of reoxidized nitrided silicon dioxide on silicon," *Appl. Phys. Lett.*, vol. 64, pp. 901, 1994.
- <sup>51</sup> K. A. Ellis and R. A. Buhrman, "Nitrous oxide (N<sub>2</sub>O) processing for silicon oxynitride gate dielectrics," *IBM J. Res. Develop.*, vol. 43, pp. 287, 1999.
- <sup>52</sup> T. P. Ma, "Making silicon nitride film a viable gate dielectric," *IEEE Transactions on Electron Devices*, vol. 45, pp. 680, 1998.
- <sup>53</sup> Y. Wu and G. Lucovsky, "Ultrathin nitride/oxide (N/O) gate dielectrics for p+-polysilicon gated pMOSFET's prepared by a combined remote plasma enhanced CVD/thermal oxidation process," *IEEE Electron Device Letters*, vol. 19, pp. 367, 1998.
- <sup>54</sup> Y. Abe and T. Fukuda, "TiO<sub>2</sub> thin films formed by electron cyclotron resonance plasma oxidation at high temperature and their application to capacitor dielectrics," *Jpn. J. Appl. Phys.*, vol. 33, pt. 2, pp. L1248, 1994.
- <sup>55</sup> S. Campbell, D. C. Gilmer, X. Wang, M. Hsieh, H. Kim, W. Gladfelter, and J. Yan, "MOSFET transistors fabricated with high permittivity TiO<sub>2</sub> Dielectrics," *IEEE Transactions on Electron Devices*, vol. 44, pp. 104, 1997.
- <sup>56</sup> C. Hobbs, R. Hegde, B. Maiti, H. Tseng, D. Gilmer, P. Tobin, O. Adetutu, F. Huang, D. Weddington, R. Nagabushnam, D. O'Meara, K. Reid, L. La, L. Grove, and M. Rossow, "Sub-quarter micron CMOS process for TiN-gate MOSFET's with TiO<sub>2</sub> gate dielectric formed by titanium oxidation," *1999 Symposium on VLSI Technology, Digest of Technical Papers*, pp. 133, 1999.
- <sup>57</sup> X. Guo and T. P. Ma, "High quality ultra-thin TiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> Gate Dielectric for Giga Scale MOS Technology," *IEDM Tech. Digest*, pp. 377-340, 1998

- <sup>58</sup> X. Guo, X. Wang, Z. Luo, T. P. Ma, T. Tamagawa, "High Quality Ultrathin(1.5nm) TiO(2)/Si(3)N(4) Gate Dielectric for Deep submicron Devices", *IEDM Tech. Digest*, pp.137-40, 1999.
- <sup>59</sup> J.-L. Autran, R. Devine, C. Chaneliere, and B. Balland, "Fabrication and Characterization of Si MOSFETs with PECVD Amorphous Ta<sub>2</sub>O<sub>5</sub> Gate Insulator," *IEEE Electron Device Lett.* 18, pp. 447, 1997.
- <sup>60</sup> Y. Momiyama, H. Minakata, and T. Sugii, "Ultra-Thin Ta<sub>2</sub>O<sub>5</sub>/SiO<sub>2</sub> Gate Insulator with TiN Gate Technology for 0.1  $\mu$ m MOSFETs," *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 135, 1997.
- <sup>61</sup> D. Park, Y.-C. King, Q. Lu, T.-J. King, C. Hu, A. Kalnitsky, S.-P. Tay, and C.-C. Cheng, "Transistor Characteristics with Ta<sub>2</sub>O<sub>5</sub> Gate Dielectrics," *IEEE Electron Device Lett.* 19, pp. 441, 1998.
- <sup>62</sup> G. B. Alers, D. J. Werder, Y. Chabal, H. C. Lu, E. P. Gusev, E. Garfunkel, T. Gustafsson, and R. S. Urdahl, "Intermixing at the tantalum oxide/silicon interface in gate dielectric structures," *Appl. Phys. Lett.*, 73, pp. 1517-19, 1998.
- <sup>63</sup> C. J. Taylor, D. C. Gilmer, D. Colombo, G. D. Wilk, S. A. Campbell, J. Roberts, and W. L. Gladfelter, *J. Am. Chem. Soc.* 121, pp. 5220, 1999.
- <sup>64</sup> Z. Luo, X. Guo, T. P. Ma, T. Tamagawa, "Temperature Dependence of Gate Currents in Thin Ta(2)O(5) and TiO(2) Films", *Applied Physics Letters*, Volume 79, Issue 17 pp. 2803-2804, Oct. 22, 2001.
- <sup>65</sup> A. Chin, C. C. Liao, C. H. Lu, W. J. Chen, and C. Tsai, "Device and reliability of high-K Al<sub>2</sub>O<sub>3</sub> gate dielectric with good mobility and low Dit," *Symposium on VLSI Technology, Digest of Technical Papers*, pp.135-136, 1999.
- <sup>66</sup> L. Manchanda, W. H. Lee, J. E. Bower, F. H. Baumann, W. L. Brown, C. J. Case, R. C. Keller, Y. O. Kim, and E. J. Laskowski, "Gate quality doped high k films for CMOS beyond 100 nm 3-10 nm Al<sub>2</sub>O<sub>3</sub> with low leakage and low interface states," *IEDM Tech. Digest*, pp.605-608, 1998..
- <sup>67</sup> D. Buchanan, E. Gusev, E. Cartier, H. Okorn-Schmidt, K. Rim, M. Gribelyuk, A. Mocuta, A. Ajmera, M. Copel, S. Guha, N. Bojarczuk, A. Callegari, C. D'Emic, P. Kozlowski, K. Chan, R. J. Fleming, P. Jamison, J. Brown, and R. Arndt, "80 nm Poly-Silicon Gated n-FETs with Ultra-Thin Al<sub>2</sub>O<sub>3</sub> Gate Dielectric for ULSI Applications," *IEDM Tech. Digest*, pp. 223-226, 2000.
- <sup>68</sup> Yanjun Ma, Yoshi Ono, Lisa Stecker, David R. Evans, and S. T. Hsu, "Zirconium Oxide Based Gate Dielectrics with EOT of Less Than 1.0 nm and Performance of Submicron MOSFET using a Nitride Gate Replacement Process," *IEDM Tech. Digest*, pp. 149, 1999.
- <sup>69</sup> W.-J. Qi, R. Nieh, B. H. Lee, L. Kang, Y. Jeon, K. Onishi, T. Nagi, S. Banerjee, and J. C. Lee, "MOSCAP and MOSFET Characteristics Using ZrO<sub>2</sub> Gate Dielectric Deposited Directly on Si," *IEDM Tech. Digest*, pp. 145-148, 1999.
- <sup>70</sup> Z. Luo, T.P. Ma, E. Cartier, M. Copel, T. Tamagawa and B. Halpern, "Ultra-thin ZrO(2) (or Silicate) with high thermal stability for CMOS Gate Application," *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 135 - 136, June, 2001.
- <sup>71</sup> B. H. Lee, L. Kang, W.-J. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. C. Lee, "Ultra Thin Hafnium Oxide with Low Leakage and Excellent Reliability for Alternative Gate Dielectric Application," *IEDM Tech. Digest*, pp. 133-136, 1999.
- <sup>72</sup> S. J. Lee, H. F. Luan, C. H. Lee, T. S. Jeon, W. P. Bai, Y. Senaki, D. Roberts, and D. L. Kwong, "High Quality Ultra Thin CVD HfO<sub>2</sub> Gate Stack with Poly-Si Gate Electrode," *IEDM Tech. Digest*, pp. 31-34, 2000.
- <sup>73</sup> L. K. Kang, Y. Jeon, K. Onishi, B. H. Lee, W.-J. Qi, R. Nieh, S. Gopalan, and J. C. Lee, "Single-Layer Thin HfO<sub>2</sub> Gate Dielectric with n+ Polysilicon Gate," *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 44, 2000.
- <sup>74</sup> G. D. Wilk, R. M. Wallace, and J. M. Anthony, "Hafnium and Zirconium Silicates for Advanced Gate Dielectrics," *J. Appl. Phys. Vol.* 87, pp. 484-492, 2000.
- <sup>75</sup> Y. H. Wu, M. Y. Yang, and C. M. Kwei, "Electrical Characteristics of High Quality La<sub>2</sub>O<sub>3</sub> Gate Dielectric with EOT of 5Å," *IEEE Electron Device Lett.* 21, 7, 2000.
- <sup>76</sup> S. Guha, E. Cartier, M. A. Gribelyuk, N. A. Bojarczuk, and M. C. Copel, "Atomic Beam Deposition of Lanthanum and Yttrium Based Oxide Thin Films for Gate Dielectrics," *Appl. Phys. Lett.* 77, pp. 2710, 2000.
- <sup>77</sup> J. Kwo, M. Hong, A. R. Kortan, K. L. Queeney, Y. J. Chabal, R. L. Opila, Jr., D. A. Muller, S. N. G. Chu, B. J. Sapjeta, T. S. Lay, J. P. Mannaerts, T. Boone, H. W. Krautter, J. J. Krajewski, A. M. Sergnt, and J. M. Rosamilia, "Properties of high  $k$  gate dielectrics Gd<sub>2</sub>O<sub>3</sub> and Y<sub>2</sub>O<sub>3</sub> for Si," *J. Appl. Phys.* 89, pp.3920-3927, 2001.

- <sup>78</sup> S. Y. Lee, D. J. Jung, Y. J. Song, B. J. Koo, S. O. Park, H. J. Cho, S. J. Oh, D. S. Hwang, S. I. Lee, J. K. Lee, Y. S. Park, and I. S. Jung, "A FRAM technology using 1T1C and triple metal layers for high performance and high density FRAMs," *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 141-142, 1999.
- <sup>79</sup> T. Eshita, K. Nakamura, M. Mushiga, A. Itho, S. Miyagaki, H. Yamawaki, M. Aoki, S. Kishii, and Y. Arimoto, "Fully functional 0.5  $\mu\text{m}$  64-kbit embedded SBT FeRAM using a new low temperature SBT deposition technique," *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 139-140, 1999.
- <sup>80</sup> F. Stern, "Quantum properties of surface space-charge layers," *CRC Crit. Rev. Solid-state Sci.* Vol. 4, pp. 499, 1974.
- <sup>81</sup> F. Stern and W. E. Howard, "Properties of semiconductor surface inversion layers in the electric quantum limit," *Phys. Rev.* 163, pp.816, 1967.
- <sup>82</sup> F. Stern, "Self-consistent results for n-type Si inversion layers," *Phys. Rev. B* 5, pp. 4891, 1972.
- <sup>83</sup> R. Rios and N. D. Arora, "Determination of ultra-thin gate oxide thickness for CMOS structures using quantum effects," *IEDM Tech. Digest*, pp. 18-21, 1994.
- <sup>84</sup> P. J. Hauser, "Estimating oxide thickness of tunnel oxides down to 1.5 nm using conventional capacitance-voltage measurement on MOS capacitors," NC State University, 1998.
- <sup>85</sup> J. F. Lonnum and J. S. Johannessen, "Dual-frequency modified CV technique," *Electron Lett.*, vol. 22, no.9, pp. 456-457, Apr. 1986.
- <sup>86</sup> G. G. Shahidi, C. A. Anderson, B. A. Chappell, T. I. Chappell, J. H. Comfort, B. Davari, R. H. Dennard, R. L. Franch, P. A. McFarland, J. S. Neely, T. H. Ning, M. R. Polcari, and J. D. Warnock, "A Room Temperature 0.1  $\mu\text{m}$  CMOS on SOI," *IEEE Trans. Electron Devices* 41, pp. 2405, 1994.
- <sup>87</sup> A. Ajmera, J. W. Sleight, F. Assaderaghi, R. Bolam, A. Bryant, M. Coffey, H. Hovel, J. Lasky, E. Leobandung, W. Rausch, D. Sadana, D. Schepis, L. F. Wagner, K. Wu, B. Davari, and G. Shahidi, "A 0.22  $\mu\text{m}$  CMOS-SOI Technology with a Cu BEOL," *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 15-16, 1999.
- <sup>88</sup> K. Rim, S. Koester, M. Hargrove, J. Chu, P. M. Mooney, J. Ott, T. Kanarsky, P. Ronsheim, M. Jeong, A. Grill, and H.-S. P. Wong, "Strained Si NMOSFETs for High Performance CMOS Technology," *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 59-60, 2001.
- <sup>89</sup> Z.-Y. Cheng, M. Currie, C. Leitz, G. Taraschi, E. Fitzgerald, J. Hoyt, and D. Antoniadis, "Electron Mobility Enhancement in Strained-Si n-MOSFETs Fabricated on SiGe-on-Insulator (SGOI) Substrates," *IEEE Electron Device Lett.* 22, pp. 321-323, 2001.
- <sup>90</sup> D.-G. Park, K.-Y. Lim, H.-J. Cho, T.-H. Cha, J.-J. Kim, J.-K. Ko, I.-S. Yeo, and J.-W. Park, "Novel Damage-Free Direct Metal Gate Process Using Atomic Layer Deposition," *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 65-66, 2001.
- <sup>91</sup> V. Misra, H. Zhong and H. Lazar, "Electrical Properties of Ru-Based Alloy Gate Electrodes for Dual Metal Gate Si-CMOS", *IEEE Electron Device Letters*, Vol. 23, 6, pp. 354-356, June, 2002.
- <sup>92</sup> Q. Lu, R. Lin, P. Ranade, Y. C. Yeo, X. F. Meng, H. Takeuchi, T.-J. King, C. Hu, H. Luan, S. Lee, W. Bai, C.-H. Lee; D.-L. Kwong, X. Guo, X. W. Wang, T. P. Ma, "Molybdenum metal gate MOS technology for post-SiO<sub>2</sub> gate dielectrics," *IEDM Tech. Digest*, pp. 641 -644, 2000.
- <sup>93</sup> M. Jeong, E. Jones, T. Kanarsky, Z. Ren, O. Dokumaci, R. Roy, L. Shi, T. Furukawa, Y. Taur, R. Miller, and H.-S. P. Wong, "Experimental Evaluation of Carrier Transport and Device Design for Planar Symmetric/Asymmetric Double-Gate/Ground-Plane CMOSFETs," *IEDM Tech. Digest*, pp. 441-444, 2001.
- <sup>94</sup> H.-S. Wong, D. Frank, Y. Taur, and J. Stork, "Design and Performance Considerations for Sub-0.1  $\mu\text{m}$  Double-Gate SOI MOSFET's," *IEDM Tech. Digest*, p. 747-750, 1994.
- <sup>95</sup> X. Huang, W.-C. Lee, C. Ku, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," *IEDM Tech. Digest*, pp. 67-70, 1999.
- <sup>96</sup> J. Kedzierski, D. M. Fried, E. J. Nowak, T. Kanarsky, J. H. Rankin, H. Hanafi, W. Natzle, D. Boyd, Y. Zhang, R. A. Roy, J. Newbury, C. Yu, Q. Yang, P. Saunders, C. P. Willets, A. Johnson, S. P. Cole, H. E. Young, N. Carpenter, D. Rakowski, B. A. Rainey, P. E. Cottrell, M. Jeong, and H.-S. P. Wong, "High-Performance Symmetric-Gate and CMOS-Compatible  $V_t$  Asymmetric-Gate FinFET Devices," *IEDM Tech. Digest*, pp. 437-440, 2001.
- <sup>97</sup> T. Vogelsang and H. R. Hofmann, "Electron Transport in Strained Silicon Layers on Si<sub>1-x</sub>Ge<sub>x</sub> Substrates," *Appl. Phys. Lett.* 63, pp. 186, 1993.

- <sup>98</sup> M. Fischetti and S. Laux, "Band Structure, Deformation Potentials, and Carrier Mobility in Strained Si, Ge, and SiGe Alloys," *J. Appl. Phys.* 80, pp. 2234, 1996.
- <sup>99</sup> E. Gusev, D. Buchanan, E. Cartier, A. Kumar, D. DiMaria, S. Guha, A. Callegari, S. Zafar, P. Jamison, D. Neumayer, M. Copel, M. Gribelyuk, H. Okorn-Schmidt, C. D'Emic, P. Kozlowski, K. Chan, N. Bojarczuk, L.-A. Rannarsson, P. Ronsheim, K. Rim, R. Fleming, A. Mocuta, and A. Ajmera, "Ultrathin High-*k* Gate Stacks for Advanced CMOS Devices," *IEDM Tech. Digest*, pp. 451–454, 2001.
- <sup>100</sup> H.-S. P. Wong, "Beyond the conventional transistor," *IBM Journal of Research and Development*, vol. 46, No. 2/3, pp. 133-168, March/May, 2002.
- <sup>101</sup> R. M. Wallace and G. Wilk, "High-*k* Gate Dielectrics Materials," *MRS Bulletin*, pp. 192, March, 2002.
- <sup>102</sup> S. Zafar, A. Callegari, E. P. Gusev, M. V. Fischetti, "Charge trapping in high *k* gate dielectric stacks," *IEDM Tech. Digest*, pp. 517–520, 2002.
- <sup>103</sup> T. Kauerauf, R. Degraeve, E. Cartier, B. Govoreany, P. Blomme, B. Kaczer, L. Pantisan, A. Kerber, G. Groeseneken, "Towards understanding degradation and breakdown of SiO<sub>2</sub>/sub 2/high-*k* stacks," *IEDM Tech. Digest*, pp. 521-524, 2002.
- <sup>104</sup> C. Hobbs, H. Tseng, K. Reid, B. Taylor, L. Dip, L. Hebert, R. Garcia, R. Hegde, J. Grant, D. Gilmer, A. Franke, V. Dhandapani, M. Azrak, L. Prabhu, R. Rai, S. Bagchi, J. Conner, S. Backer, F. Dumbuya, B. Nguyen, P. Tobin, "80 nm poly-Si gate CMOS with HfO<sub>2</sub> gate dielectric," *IEDM Tech. Digest*, pp. 651-654, 2001.
- <sup>105</sup> J. J. Schmitt and B. L. Halpern, "Method and apparatus for the deposition of solid films of material from a jet stream entraining the gaseous phase of said material," *U.S. Patent 4 788 082*, 1988.
- <sup>106</sup> J. J. Schmitt and B. L. Halpern, "Method from microwave plasma assisted supersonic gas jet deposition of thin films," *U.S. Patent 5 356 672*, 1994.
- <sup>107</sup> J. J. Schmitt and B. L. Halpern, *U.S. Patent 5 256 205*, 1993.
- <sup>108</sup> B. L. Halpern and J. J. Schmitt, "Multiple jets and moving substrates: Jet Vapor Deposition of multicomponent thin films," *J. Vac. Sci. Technol. A* 12(4), 1994.
- <sup>109</sup> C. L. Hwang, "High dielectric constant materials for ULSI applications, Ph. D. Thesis," in *Department of Electrical Engineering*. New Haven, CT: Yale University, 1994.
- <sup>110</sup> M. Copel, M. Gribelyuk, and E. Gusev, "Structure and Stability of Ultrathin Zirconium Oxide Layers on Si(001)," *Appl. Phys. Lett.* 76, pp. 436, 2000.
- <sup>111</sup> M. B. Bever, *Encyclopedia of Materials Science and Engineering*: Pergamon press and the MIT press, first edition, 1986.
- <sup>112</sup> D. K. Smith and C. F. Cline, *J. AM. Ceram. Soc.* 45, 249, 1962.
- <sup>113</sup> A. M. Alper, "High Temperature Oxides, Part II Oxides of Rare Earths, Titanium, Zirconium, Hafnium, Niobium and Tantalum": Academic Press, 1970.
- <sup>114</sup> R. M. Tromp, M. Copel, M. C. Reuter, M. Horn von Hoegen, J. Speidell, and R. Koudijs, "A New 2-D Particle Detector for a Toroidal Electrostatic Analyser," *Rev. Sci. Instrum.* 62, pp. 2679, 1991.
- <sup>115</sup> H. C. Lu, E. P. Gusev, E. Garfunkel, and T. Gustafsson, "An Ion Scattering Study of the Interaction of Oxygen with Si(111): Surface Roughening and Oxide Growth," *Surf. Sci.* 341, pp. 111, 1996.
- <sup>116</sup> J. Vrijmoeth, P. M. Zagwijn, J. W. M. Frenken, and J. F. van der Veen, "Monolayer Resolution in Medium-Energy Ion-Scattering Experiments on the NiSi<sub>2</sub>(111) Surface," *Phys. Rev. Lett.* 67, pp. 1134, 1991.
- <sup>117</sup> T. S. Jeon, J. M. White, and D. L. Kwong, "Thermal stability of ultrathin ZrO<sub>2</sub> films prepared by chemical vapor deposition on Si(100)," *Appl. Phys. Lett.* Vol. 78, No. 3, pp. 368-370, 2001.
- <sup>118</sup> C. M. Perkins, B. B. Triplett, P. C. McIntyre, K. C. Saraswat, E. Shero, "Thermal stability of polycrystalline silicon electrodes on ZrO<sub>2</sub> gate dielectrics," *Appl. Phys. Lett.* Vol. 81, No. 8, pp. 1417-1419, 2002.
- <sup>119</sup> S. C. Sun and T. F. Chen, "Effects of electrode materials and annealing ambients on the electrical properties of TiO<sub>2</sub> thin films by metalorganic chemical vapor deposition," *Jpn. J. Appl. Phys.*, vol. 36, Pt. 1, pp. 1346, 1997.
- <sup>120</sup> P. Alexandrov, J. Koprinarova, and D. Todornov, "Physical properties of TiO<sub>2</sub> thin films," *Solid-State electron.*, vol. 47, pp. 1333, 1996.
- <sup>121</sup> B. H. Lee, Y. Jeon, K. zawadzki, W. Qi, and J. Lee, "Effects of interfacial layer growth on the electrical characteristics of thin titanium oxide films on silicon," *Applied Physics Letters*, vol. 74, pp. 3143, 1999.
- <sup>122</sup> C. Deckert, "Wet Etching of Insulators and Dielectrics," in *Thin Film Processing*, 1995.

- <sup>123</sup> S. A. Campbell, H. S. Kim, D. C. Gilmer, B. He, T. Ma, and W. L. Gladfelter, "Titanium dioxide (TiO<sub>2</sub>) based gate insulators," *IBM J. Res. Develop.*, vol. 43, pp. 383, 1999.
- <sup>124</sup> X. Guo, "Advanced High-k Gate Dielectrics for Scaled MOS Device Applications," Ph. D. Thesis, Yale University, 1999.
- <sup>125</sup> X. Wang, Z. J. Luo, T. P. Ma, "High-Temperature Characteristics of High-Quality SiC MIS Capacitors with O/N/O Gate Dielectric," *IEEE Trans. on Electron Devices*, Vol. 47, No. 2, Feb. 2000.
- <sup>126</sup> D. Park, Q. Lu, T. King, and C. Hu, "SiON/Ta<sub>2</sub>O<sub>5</sub>/TiN gate-stack transistor with 1.8 nm equivalent SiO<sub>2</sub> thickness," *IEDM Tech. Digest*, pp. 381, 1998.
- <sup>127</sup> C. Choi, J. Goo, T. Oh, Z. Yu, R. W. Dutton, and C. H. Diaz, "MOS C-V characterization of ultrathin gate oxide thickness (1.3 -1.8 nm)," *IEEE Electron Device Letters*, vol. 20, pp. 292, 1999.
- <sup>128</sup> Jeng-Jye-Shiau; Fahrenbruch, A.-L.; Bube, R.-H., Influence of AC contact impedance on high-frequency, low-temperature, or fast-transient junction measurements in semiconductors, *Journal-of-Applied-Physics.*, 61(4), pp. 1556-61, 15 Feb. 1987.
- <sup>129</sup> Venkatesan, V.; Das, K.; von-Windheim, J.-A.; Geis, M.-W., Effect of back contact impedance on frequency dependence of capacitance-voltage measurements on metal/diamond diodes, *Applied-Physics-Letters.*, 63(8), pp. 1065-1067, 23 Aug. 1993.
- <sup>130</sup> R. Holm, *J. Appl. Phys.*, vol. 22, pp. 569, 1951.
- <sup>131</sup> Whye-Kei Lye, "Inelastic Electron Tunneling Spectroscopy of the Silicon Metal-Oxide-Semiconductor System," Thesis, Yale University, 1998.
- <sup>132</sup> H. Itokawa, T. Maruyama, S. Miyazaki, and M. Hirose, *Proc. SSDM*, pp. 158, Japan Society of Applied Physics, 1999.
- <sup>133</sup> L. T. Su, J. B. Jacobs, J. E. Chung, and D. A. Antoniadis, "Short-channel effects in deep-submicrometer SOI MOSFETS," *Proceeding of the 1993 IEEE International SOI Conference*, Palm Springs, CA, 1993, pp. 112-113.
- <sup>134</sup> D. J. Frank, S. E. Lauz, and M. V. Fischetti, *IEDM Tech. Digest*, pp. 553-556, 1992.
- <sup>135</sup> H. S. Wong and Y. Taur, *IEDM Tech. Digest*, pp. 705-708, 1993.
- <sup>136</sup> D. A. Buchanan, F. R. Mafeely, and J. J. Yurkus, "Fabrication of midgap metal gates compatible with ultrathin dielectrics," *Appl. Phys. Lett.*, Vol. 73, pp. 1676-1678, 1998.
- <sup>137</sup> R. J. Powell, "Interface Barrier Energy Determination from Voltage Dependence of Photoinjected Currents," *J. Appl. Phys.*, Vol. 41, No. 6, pp. 2424-2432, 1970.
- <sup>138</sup> R. J. Powell, "Photoinjection into SiO<sub>2</sub>: Use of Optical Interference to Determine Electron and Hole Contributions," *J. Appl. Phys.*, Vol. 40, No. 13, pp. 5093-5101, 1969.
- <sup>139</sup> E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*: John Wiley & Sons, 1982.
- <sup>140</sup> R. Williams, "Photoemission of Electrons from Silicon into Silicon Dioxide," *Physical Review*, Vol. 140, No. 2A, pp. A569-A575, 1965.
- <sup>141</sup> C. A. Mead, E. H. Snow, and B. E. Deal, "Barrier Lowering and Field Penetration at Metal-Dielectric Interfaces," *Appl. Phys. Lett.*, Vol. 9, No. 1, pp. 53-55, 1966.
- <sup>142</sup> Ying Shi, "CMOS Gate Dielectric Scaling: Limitations and Opportunities," Thesis, Yale University, 1998.
- <sup>143</sup> J. S. Brugler and P. G. A. Jespers, "Charge Pumping in MOS Devices," *IEEE Trans. On Electron Devices*, Vol. 16, pp. 297, 1969.
- <sup>144</sup> R. E. Paulsen and M. H. White, "Theory and Application of Charge Pumping for the Characterization of Si-SiO<sub>2</sub> Interface and Near Interface Oxide Traps," *IEEE Trans. On Electron Devices*, Vol. 41, No. 7, pp. 1213-1216, 1994.
- <sup>145</sup> D. Bauza and G. Ghibaudo, "Analytical study of the Contribution of Fast and Slow Oxide Traps to the Charge pumping Current in MOS Structures," *Solid-state Electronics*, Vol. 39, No. 4, pp 563-570, 1996
- <sup>146</sup> D. Bauza and Y. Maneglia, "In-depth Exploration of Si-SiO<sub>2</sub> Interface Traps in MOS Transistors Using the Charge Pumping Technique," *IEEE Trans. on Electron Devices*, Vol. 44, No. 12, pp 2262-2266, 1997.
- <sup>147</sup> C. E. Weintraub, E. Vogel, J. R. Hauser, Yang Nian, V. Misra, J. J. Wortman, J. Ganem, P. Masson, "Study of low-frequency charge pumping on thin stacked dielectrics," *IEEE Trans. On Electron Devices*, Vol. 48, pp. 2754-2762, 2001.
- <sup>148</sup> F. P. Heiman and G. Warfield, "The effect of oxide traps on the MOS capacitance," *IEEE Trans. On Electron Devices*, Vol. 12, pp. 167, 1965.

- 
- <sup>149</sup> P. Masson, J.-L. Autran, J. Brini, "On the tunneling component of charge pumping current in ultrathin gate oxide MOSFETs," IEEE Electron Device Letters, Vol. 20, pp. 92-94, 1999.
- <sup>150</sup> M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, "Effective electron mobility in Si inversion layers in metal-oxide-semiconductor systems with a high- $\kappa$  insulator: The role of remote phonon scattering," J. Appl. Phys., Vol. 90, pp. 4587-4608, 2001
- <sup>151</sup> M. Khare, X. W. Wang, T. P. Ma, "Transconductance in nitride-gate or oxynitride-gate transistors," IEEE Electron Device Letters, Volume: 20 Issue: 1, Jan. 1999, pp: 57 -59
- <sup>152</sup> Private conversation between T. P. Ma and M. V. Fischetti, June, 2003.
- <sup>153</sup> J. Koomen, "Investigation of The Most Channel Conductance in Weak Inversion," Solid-State Electronics, Vol. 16, No. 7, pp. 801, 1973.
- <sup>154</sup> C. G. Sodini, T.W. Ektedt, and J. L. Moll, "Charge Accumulation and Mobility in Thin Dielectric MOS Transistors," Solid State Electronics, Vol.25, No.9, pp.833, 1982.
- <sup>155</sup> W.J. Zhu, "Hafnium Oxide and Hafnium Aluminum Oxide for CMOS Applications," Ph. D. Thesis, Yale Univeristy, 2003.
- <sup>156</sup> A.V. Rzhzanov, Silicon nitride in electronics: Elsevier Science Publishers, 1988.