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Utility Patent Application Transmittal

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Attorney Docket No: 115-34USCIP/12667/100126
First Inventor: James H. Derbyshire
Title: Module Integration Integrated Circuits

Application Elements:

1. ☒ Fee Calculation (see Box 14)
2. ☒ Applicant claims small entity status.
3. ☒ Specification Total Pages - 25
 - Description
 - Claims
 - Abstract of the Disclosure
4. ☒ Drawing(s) - (6 Figures) Total Sheets - 6
5. ☒ Oath or Declaration Total Pages - 3
 - a. ☒ Newly executed (original or copy)
 - b. ☐ Unexecuted
 - c. ☐ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 12 completed)
 - i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in
the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

Accompanying Application Parts:

6. ☒ Assignment Papers (cover sheet & document(s))
7. ☐ Information Disclosure Statement (IDS)/PTO-1449 Copies of IDS Citations ☐
8. ☐ Preliminary Amendment
9. ☒ Return Receipt Postcard *(Should be specifically itemized)*
10. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
11. ☐ Other:

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12. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

☐ Continuation of prior Application No. ☐ Divisional filed ☐ Continuation-in-part (CIP)

Prior application information: Examiner: Group Art Unit:

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5c, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon which a portion has been inadvertently omitted from the submitted application parts.

13. CORRESPONDENCE ADDRESS: 23838

Gary Morris, Reg. No. 40,735
Kenyon & Kenyon
1500 K Street, N.W., Suite 700
Washington, DC 20005-1257
PHONE: (202) 220-4200
FAX: (202) 220-4201

Agent: Gary Morris, Reg. No. 40,735

14. FEE CALCULATION:

☒ Applicant Claims Small Entity Status						AMOUNT		
1. BASIC FILING FEE								
Large Entity			Small Entity					
Fee Code	Fee (\$)	Fee Code	Fee (\$)					
1001	770.00	2001	385.00					
						\$385.00		
2. EXTRA CLAIM FEES								
				Extra Claims	Fee From Below			
Total Claims	35	-	20	=	15		x \$9.00	=
Independent Claims	3	-	3	=	0		x \$43.00	=
Multiple Dependent					\$**		=	
Large Entity			Small Entity					
Fee Code	Fee (\$)	Fee Code	Fee (\$)					
1202	18.00	2202	9.00					
1201	86.00	2201	43.00					
						\$135.00		
3. OTHER								
Fee Code - 8021	Fee (\$)	Recording Patent Assignment						
	40.00							
TOTAL						\$560.00		

15. ☒ The Commissioner is hereby authorized to charge all fees in Box 14 above to Deposit Account 50-1142.
16. ☒ The Commissioner is hereby authorized to charge any additional fees required or credit any overpayment to Deposit Account No. 50-1142.

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Submitted By:



Gary Morris, Reg. No. 40,735
Telephone: (202) 220-4200

Module Integration Integrated Circuits

[0001] This application is a continuation in part of United States Patent Application No: 10/680,208, filed on: October 08, 2003.

Field of the Invention

[0002] The invention relates to the field of RF front-end circuits and more specifically to the field of multi-standard RF front-end circuits implemented in a small module size.

Background of the Invention

[0003] Typically, manufacturers in the area of wireless products wish to implement radio media interface circuits into radio terminals, such as PCMCIA cards or dongles, which typically must operate within the context of two or more radio standards but in accordance with one standard at any one time. These radio standards are for example collectively referred to as the IEEE 802 standard, which is well known to those of skill in the art. This standard is typically divisible into a number of individual radio standards including one standard at 5.8GHz, known as 802.11a, and another two standards at 2.45GHz, known as 802.11b and 802.11g.

[0004] In terms of these radio standards, manufacturers are often interested in building radio terminals that will be able to operate at 802.11a, b, and g standards, with only one particular standard being active at any one time. As a result, the manufacturers are interested in acquiring a front-end module that incorporates receive and transmission elements such as the low noise amplifiers (LNA), power amplifiers (PA), impedance matching components, and RF switches for all the standards that the terminal or card must deal with. Thus providing them with flexibility in their radio terminal designs.

[0005] Unfortunately, PAs and other components such as the LNA, are highly specialized components that have specifications that generally do not overlap with other radio frequency bands. Thus, a 5.8 GHz PA is generally not suitable for use 2.4GHz PA. As a result, distinct components such as the LNAs and PAs are incorporated into the module in order to accommodate different radio standards. Moreover, many of the high

performance RF components such as PAs and LNAs have a relatively low level of ancillary circuit integration. For example, voltage regulation circuits, temperature regulation circuits, control circuits and other circuits that are used for control and optimization of the operation of the PA are often not integrated into a same die with the PA but rather disposed as discrete components, on separate semiconductor substrates, within the module surrounding the PA die. It is well understood by most module designers that adding more components to the module increases cost, reduces yield and durability while resulting in an increase in module size. This effect is compounded when additional circuitry is used for each active RF component such as an RF switch, LNA, and PA.

[0006] Recent advances in SiGe BiCMOS technology have allowed for progressively higher levels of integration of high-performance RF components. For example, a high-performance 2.45GHz PA for the 802.11b/g standard implemented in SiGe BICMOS technology can incorporate voltage and temperature regulation circuitry along with various power optimization and control schemes manifested in control circuitry. The benefit of such high levels of integration are well understood by the IC design community and include reduced module sizes, reduced cost, reduced assembly time, and increased yield and module longevity. Moreover, for PAs in particular, the robustness of the PA in tolerating of mismatch conditions to the antenna can be improved with voltage standing wave ratio (VSWR) sensing circuitry and PA output power sensing circuitry integrated into the PA chip. In this particular example, a determination of high VSWR might lead to the generation of a control signal to reduce power output and thereby protect one or more PA gain stages from over voltage conditions. Clearly, integration of this type of ancillary circuitry into the PA has the potential to increase PA performance and robustness with a minimum increase in the module size. In respect of LNAs, the integration of bias point control circuitry is important.

[0007] However, the usage of SiGe BiCMOS technology in the industry is currently limited. For example, for 5.8GHz PAs, only a small number of manufacturers are utilizing SiGe for whereas several end users are utilizing GaAs or group III-V based technologies. The GaAs based technologies however offer more gain per stage and lower

losses in the RF signal path at 5.8GHz. GaAs based technology, however, is often unsuitable for the integration of ancillary circuits for use with the GaAs based RF component. Voltage regulation, for example, may not be integrated into the GaAs based PA due to the lack of suitable elementary devices within the GaAs based technology. Therefore, in the context of a module, the module designer is compelled to add those additional circuits, or dies, for supporting of the GaAs based components. As mentioned previously, the addition of more components causes a detriment to the module size and cost.

[0008] A need therefore exists to for providing a compact RF module that supports a number of RF standards. It is therefore an object of the invention to provide a compact RF module that overcomes the limitations of the prior art by facilitating integration of multiple circuit components into a same module in order to support a number of RF standards.

Summary of the Invention

[0009] In accordance with the invention there is provided an electronic apparatus comprising: a first integrated circuit semiconductor die comprising; a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path; a second integrated circuit semiconductor die comprising: a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first portion of a first signal conditioning circuit for a signal propagating along the first signal path; and, a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.

[0010] In accordance with the invention there is provided a method of manufacturing a module comprising: providing a first signal conditioning circuit comprising a first portion and a second portion; implementing the first portion of the first signal conditioning circuit within a first semiconductor die; implementing the second portion of the first signal conditioning circuit within a second semiconductor die; bonding the first

and second dies to a common substrate; and, forming electrical connections between the two dies to complete the first signal conditioning circuit from the first portion of the first signal conditioning circuit and the second portion of the first signal conditioning circuit.

[0011] In accordance with the invention there is provided an electronic apparatus comprising: a first integrated circuit semiconductor die comprising: a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path; a third portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along the first signal path; a second integrated circuit semiconductor die comprising: a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first and third portions of the first signal conditioning circuit for a signal propagating along the first signal path; and, a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.

Brief Description of the Drawings

[0012] Exemplary embodiments of the invention will now be described in conjunction with the following drawings, in which:

[0013] FIG. 1 illustrates a prior art integration of components into a module;

[0014] FIG. 2 illustrates a first embodiment of the invention, a module 200 having two semiconductor substrates integrated within the module, as opposed to three, as shown in FIG. 1;

[0015] FIG. 3 illustrates a second embodiment of the invention, which illustrates a more specific implementation of the first embodiment of the invention;

[0016] FIG. 4 illustrates the method of manufacturing a circuit in accordance in accordance with an embodiment of the present invention; and,

[0017] FIG. 5 illustrates a third embodiment of the invention, a module 500 having two semiconductor substrates integrated within the module.

[0018] FIG. 6 illustrates a fourth embodiment of the invention, a module 600 having first and second integrated circuit semiconductor dies, 611 and 612, integrated within the module 600.

Detailed Description of Embodiments of the Invention

[0019] FIG. 1 illustrates a prior art integration of components into a module 100. Disposed within the module 100 is a first signal conditioning circuit 101, a second signal conditioning circuit 102 and a voltage regulator circuit 103. The first signal conditioning circuit is disposed between a first RF signal input port 100a and a first RF signal output port 100b. The second signal conditioning circuit is disposed between a second RF signal input port 100c and a second RF signal output port 100d. A regulated supply voltage is provided to both the first and second signal conditioning circuits from the regulator circuit 103, which is disposed on a different semiconductor substrate than the first and second signal conditioning circuits, 101 and 102. A supply voltage is provided to the regulator circuit 103 from a battery (not shown) through a positive supply voltage input port 100e and through a ground port 100f. The first and second signal conditioning circuits are also connected to the ground port 100f.

[0020] The voltage regulator circuit 103 is disposed as the third component of this module 100. Typically, the voltage regulation properties of the regulator circuit 103 are not optimized for operating with either the first or the second signal conditioning circuits in order to save on module cost 100. But, a trade-off in the module 100 specifications allows for the use of a single regulator circuit 103 for regulating the supply voltage to both signal conditioning circuits. Providing a separate voltage regulator for each signal conditioning circuit would unfortunately add another semiconductor substrate to the module 100 and result in an increased module cost.

[0021] For example, the module 100 shown in FIG. 1 is for use in cellular telephones, where two cellular band power amplifier circuits (PAs) are incorporated into the module

as the first and second signal conditioning circuits, 101 and 102. In such a module, the voltage regulation circuit is typically silicon-based and disposed with power amplifier modules of two different types, such as GaAs based PAs. It is not uncommon to find that the module size is determined by the area required for the ancillary circuits, such as the voltage regulation circuit 103, rather than by the area required by core RF components, such as the PAs.

[0022] Referring to the prior art module illustrated in FIG. 1, all circuits included into the module are disposed as discrete components. Unfortunately, this leads to progressively larger and more expensive modules as functionality and performance are increased. A further disadvantage of the old technology lies in the additional assembly cost and additional assembly time associated with placing and wiring these numerous circuits and components within the module 100. It is well understood that in designing and manufacturing of the module, the area requirements grow in proportionality to the number of circuits and components used. Furthermore, the probability of manufacturing errors and defects increases in proportion to the number of circuits and components required in the design.

[0023] FIG. 2 illustrates a first embodiment of the invention, a module 200 having two semiconductor substrates integrated within the module, as opposed to three, as shown in FIG. 1. A first signal conditioning circuit 201 is formed on a first semiconductor substrate 211 and a second signal conditioning circuit 202 is formed on a second semiconductor substrate 212. The first signal conditioning circuit 201 is disposed between a first RF signal input port 200a and a first RF signal output port 200b. The second signal conditioning circuit 202 is disposed between a second RF signal input port 200c and a second RF signal output port 200d.

[0024] In addition, a first ancillary circuit 203 and a second ancillary circuit 204 are disposed on the first semiconductor substrate 211. The first ancillary circuit 203, in the form of a first voltage regulator circuit, is for providing a first regulated supply voltage to the first signal conditioning circuit 201. The second ancillary circuit 203, in the form of a second voltage regulator circuit, is for providing a second regulated supply voltage

to the second signal conditioning circuit 202. An unregulated supply voltage from a source (not shown) is provided to the first and second regulator circuits through a positive supply voltage terminal 200e and a ground terminal 200f. In this embodiment, the first and second voltage regulator circuits, 203 and 204, are integrated into the first semiconductor substrate 211, along with the first signal conditioning circuit 201. A first interface port 211a disposed on the first semiconductor die 211 and connected to the second ancillary circuit 204 connects the second ancillary circuit 204 to the second semiconductor die using a second interface port 212a. The second interface port 212a is connected to the second signal conditioning circuit 202. For example, the first signal conditioning circuit comprises an amplifying circuit, such as a PA circuit or a low noise amplifier (LNA) circuit.

[0025] The integration of circuit components into the module 200 provides for a first integrated circuit formed in a first semiconductor substrate 211 and manufactured using a first semiconductor process. Disposed within the first integrated circuit is the first signal conditioning circuit 201 for performing a first signal conditioning function and the first ancillary circuit 203 electrically coupled to the first signal conditioning circuit 201 only for use by the first signal conditioning circuit 201 during operation thereof. The second ancillary circuit 204 is for other than being used by the first signal conditioning circuit 201 during operation thereof. The second integrated circuit 202 is electrically coupled to the second ancillary circuit 204 and formed in the second semiconductor substrate 212 and co-packaged with the first integrated circuit 211 within the module 200. The second integrated circuit 202 operates in conjunction with the second ancillary circuit 204, via the connection between the first and second interface ports, 211a and 212a, for performing the second signal conditioning function. Optionally, the second signal conditioning function is a similar function to the function performed by the first signal conditioning circuit 201.

[0026] Advantageously, the integration of circuit functionality into one or more of the semiconductor substrates offers immediate benefit. Integration of these ancillary circuits into the same die area already occupied by one of the other core components is efficient in respect of die area usage. The integration into a module 200, as shown in FIG. 2,

allows for integration of different signal conditioning circuits that do not have overlap in their RF bands. The first signal conditioning circuit 201 is for example integrated within the first semiconductor substrate 211 using SiGe BiCMOS technology, along with the first and second voltage regulator circuits, 203 and 204. The second signal conditioning circuit 202 is, for example, integrated into the semiconductor substrate 212 using a GaAs process. As a result of this integration, the completed module 200 accommodates different radio standards in a single package. For example, for a 5.8GHz PA, the second signal conditioning circuit 202 is used and for a 2.45GHz PA the first signal conditioning circuit is used 201.

[0027] FIG. 3 illustrates a second embodiment of the invention, which illustrates a more specific implementation of the first embodiment of the invention. Referring to FIG. 3, a module 300 having two semiconductor substrates, 311 and 312, integrated therein, is shown. A first signal conditioning circuit 301 is formed on a first semiconductor substrate 311 and a second signal conditioning circuit 302 is formed on a second semiconductor substrate 312. The first signal conditioning circuit 301 is disposed between a first RF signal input port 300a and a first RF signal output port 300b along a first signal path. The second signal conditioning circuit 302 is disposed between a second RF signal input port 300c and a second RF signal output port 300d along a second signal path.

[0028] A first plurality of ancillary circuitry 303a through 303n, in the form of a first plurality of control circuitry, is disposed within the first semiconductor substrate 311. At least one of the plurality 303n of ancillary circuitry, 303a through 303n, is unrelated to the operation of the first signal conditioning circuit 301 and used for accommodating the requirements of the second signal conditioning circuit 302 formed on the second semiconductor substrate 312. A plurality of electrical connections, 306a through 306n, - in the form of wire bonds, for example, is used for electrically coupling the at least one of the plurality 303n of ancillary circuitry to the second semiconductor substrate 312 for use by the second signal conditioning circuit 302. The plurality of electrical connections are disposed between a first plurality of interface ports disposed on the first semiconductor die and connected to the a least one of the plurality 303n of ancillary

circuitry, 303a through 303n, and a second plurality of interface ports. The second plurality of interface ports are connected to the second signal conditioning circuit 302. The second signal conditioning circuit 302 is for performing a second signal conditioning function in conjunction with the a least one of the plurality 303n of ancillary circuitry, 303a through 303n, connected thereto. The first signal conditioning circuit 301 is for performing a first signal conditioning function independent of the second signal conditioning circuit 302. As a result, RF signals propagating along the first signal path and the second signal path do not interfere with each other because the signal paths are separated on separate semiconductor dies.

[0029] Referring to the embodiment shown in FIG. 3, the first signal conditioning circuit comprises a first impedance transforming circuit 301a, in series with three amplification stages, 301b through 301d, and in series with a second impedance transforming circuit 301e. Disposed within the second signal conditioning circuit are a third impedance transforming circuit 302a, in series with three amplification stages, 302b through 302d, and in series with a second impedance transforming circuit 302e. Although the signal conditioning circuits are disposed on different semiconductor substrates, they perform similar functions. In this case, both signal conditioning circuits comprise PAs since they are used in RF amplification applications and as a result provide similar functions.

[0030] In addition, a plurality of power detector circuits 304a through 304n are also preferably integrated within the first semiconductor substrate 311. These power detector circuits are preferably used for detecting of RF output signal power being propagated from the first RF signal output port 300b and the second RF signal output port 300d. Other circuit blocks, such as circuit block 305, are also integrated within the first semiconductor substrate. Because the first semiconductor substrate is preferably manufactured using a process that supports a plurality of suitable elementary devices, such as SiGe BiCMOS, the integration of the first and second ancillary circuits is facilitated and serves to reduce space in the module without the addition of additional circuit components manufactured on additional semiconductor substrates, which causes a detriment to the module size and cost. Preferably, the semiconductor process that

supports a larger scale of integration is utilized for integrating of a larger plurality of integrated circuit components therein.

[0031] Integration of a majority of ancillary circuit functionality into one or more of the semiconductor dies offers immediate benefit. Integration of these ancillary circuits into the same die area used by one of the core components is very efficient in respect of area usage within the module. The integration into a module, as shown in FIG. 2 and FIG. 3, allows for integration of different signal conditioning circuits into a same module that do not have overlap in their RF bands.

[0032] Optionally, a carrier platform, element 205 shown in FIG. 2, is used for supporting the various semiconductor dies, 211 and 212, and optionally other electrical components. The carrier platform 205 is for example a multi-layer laminate or even a silicon-based platform. The function of the carrier platform 205 is to support the semiconductor dies and to provide a means of interconnecting the electrical signals and power supply rails for each semiconductor die, 211 and 212. The embodiments of the invention are applicable for use in modules and other types of sub-assemblies where more than one component is co-located. Co-location referring to the disposition of the module components in close enough proximity such that PCB traces, wirebonds or other technologies are used to interconnect the components to each other. Often the components are in close enough proximity that wirebonding from one semiconductor die to another is sufficient. Thus, these semiconductor dies, 211 and 212, are placed onto the carrier platform 205 and wirebonded or flip-chipped to establish an electrical connection to interconnect traces forming part of the carrier platform 205. Typically, after placement of semiconductor dies and upon completion of wiring therebetween a mold compound is applied to finish the module.

[0033] Advantageously, only one of the semiconductor substrates within the module are designed to incorporate all the additional regulation and optimization circuitry required by the other signal conditioning circuits in the form of active RF components. In this manner, die area within the module is minimized, and thereby cost, and the number of components that require circuit connections therebetween is minimized. Furthermore,

selection of active RF components on the basis of RF performance is greatly facilitated without placing additional regulation and additional optimization circuits for the greater performing RF components.

[0034] Disposing the first and second signal conditioning circuits on separate substrates advantageously eliminates crosstalk issues therebetween. Thus, output signal noise is minimized. Prior to designing of a module, a module designer of skill in the art determines which signal conditioning circuits will pose problems when integrated on a same semiconductor die and as such those circuits are integrated on separate dies.

[0035] FIG. 4 illustrates a method steps for manufacturing a circuit for reducing crosstalk therein. A first signal conditioning circuit is implemented within a first semiconductor die, in step 401. A first portion of a second signal conditioning circuit is implemented in the first semiconductor die, in step 402. Referring to step 403, a second portion of the second signal conditioning circuit is implemented in a second semiconductor die. Thereafter, in step 404, the first and second dies are bonded to a common substrate, and in step 405, wire bonding between the two dies is performed to complete the second signal conditioning circuit.

[0036] FIG. 5 illustrates a third embodiment of the invention, a module 500 having two semiconductor substrates, 511 and 512, integrated within the module. A first portion of a first signal conditioning circuit 501 and first and second ancillary circuits, 503 and 504, are integrated on a first semiconductor substrate 511 and a second portion of the first signal conditioning circuit 505 as well as first and second portions of the second signal conditioning circuit, 502 and 506, are integrated on a second semiconductor substrate 512. The first portion of the first signal conditioning circuit 501 is disposed between a first RF signal input port 500a and a first semiconductor substrate output port 511b, where the second portion of the first signal conditioning circuit 505 is coupled between the first semiconductor substrate output port 511b and a first RF signal output port 500b. The first portion of the second signal conditioning circuit 502 and the second portion of the second signal conditioning circuit 506 are disposed in series between a second RF signal input port 500c and a second RF signal output port 500d.

[0037] The first ancillary circuit 503, in the form of a first voltage regulator circuit, is for providing a first regulated supply voltage to the first portion of the first signal conditioning circuit 501. The second ancillary circuit 504, in the form of a second voltage regulator circuit, is for providing a second regulated supply voltage to the second portion of the first signal conditioning circuit 505 and to the first and second portions of the second signal conditioning circuit, 502 and 506. An unregulated supply voltage from a source (not shown) is provided to the first and second regulator circuits through a positive supply voltage terminal 500e and a ground terminal 500f.

[0038] The integration of circuit components into the module 500 provides for a first integrated circuit formed in a first semiconductor substrate 511 and manufactured using a first semiconductor process. Disposed within the first integrated circuit is the first portion of the first signal conditioning circuit 501 for performing a first signal conditioning function in conjunction with the second portion of the first signal conditioning circuit 505 and the first and second ancillary circuits 503 and 504 electrically coupled to the first and second portions of the first signal conditioning circuit, 501 and 505, respectively. The second ancillary circuit 504 is for other than being used by the first portion of the first signal conditioning circuit 501 during operation thereof. The second integrated circuit 502 includes the first portion of the second signal conditioning circuit 502 and the second portions of the first and second signal conditioning circuits, 505 and 506, where these portions operate using the electrically coupled second ancillary circuit 504 formed in the first semiconductor substrate 511 and co-packaged with the first integrated circuit 511 within the module 500.

[0039] The second integrated circuit 502 operates in conjunction with the second ancillary circuit 504, via a connection between the first and second interface ports, 511a and 512a. Optionally, the second signal conditioning function is a similar function to the function performed by the first signal conditioning circuit 501.

[0040] For example, the first semiconductor substrate 511 is a SiGe semiconductor substrate and the first signal conditioning circuit 501 and 505 is a PA circuit, which is

known to have high loss, or low quality factor, when integrated on the silicon wafer. It is well known to those of skill in the art that inductors disposed on the silicon substrate suffer performance degradation due to absorption of RF energy within the substrate and other factors, as compared to inductors that are integrated on a semi-insulating GaAs substrate. Thus, for example, the second semiconductor substrate 512 is a GaAs substrate, where low-loss passive devices are integrated therein for use by the second portion of the first signal conditioning circuit 501. For example, the second portion of the first signal conditioning circuit 505 is an impedance matching circuit, for use with the first portion of the first signal conditioning circuit 501 in the form of a 2.4GHz SiGe-based PA. The first portion of the second signal conditioning circuit is for example in the form of a 5GHz PA.

[0041] Advantageously, this integration scheme provides a module designer with the best attributes of both semiconductor substrates, which in this case are silicon and GaAs, in order to achieve a high level of performance, and integration, with a low number of module components. Of course, other components, such as transmission lines, capacitors, and inductors for use by the SiGe-based die, are integrated within the second semiconductor substrate in order to provide increased operating efficiency.

[0042] Advantageously, the integration of circuit functionality into one or more of the semiconductor substrates offers immediate benefit. Integration of these ancillary circuits into the same die area already occupied by one of the other core components is efficient in respect of die area usage. The integration into a module 200, 500, as shown in FIGs. 2 and 5, allows for integration of different signal conditioning circuits that do not have overlap in their RF bands. The first signal conditioning circuit 201 and, 501 and 505, is for example integrated within the first semiconductor substrate 211, 511 using SiGe BiCMOS technology, along with the first and second voltage regulator circuits, 203 and 204, and 503 and 504. The second signal conditioning circuit 202, 502 and 506, for example, is integrated into the semiconductor substrate 212, 512 using a GaAs process. As a result of this integration, the completed module 200, 500 accommodates different radio standards in a single package. For example, for a 5.8GHz PA, the second signal

conditioning circuit 202, 502 and 506 is used for the 5.8GHz PA and for a 2.45GHz PA the first signal conditioning circuit 201, 501 and 505 is used.

[0043] FIG. 6 illustrates a fourth embodiment of the invention, a module 600 having first and second integrated circuit semiconductor dies, 611 and 612, integrated within the module 600. A first portion of a first signal conditioning circuit 601a, a third portion of the first signal conditioning circuit 601b and first and second ancillary circuits, 603 and 604, are integrated within the first integrated circuit semiconductor die 611. A second portion of the first signal conditioning circuit 605 as well as first and second portions of the second signal conditioning circuit, 602 and 606, are integrated on the second integrated circuit semiconductor die 612.

[0044] The first portion of the first signal conditioning circuit 601a is disposed between a first RF signal input port 600a and an electrical connection 620b that connects an output port of the first portion of the first signal conditioning circuit 601a to a second portion of the first signal conditioning circuit 605 disposed in the second integrated circuit semiconductor die 612. An input port of the third portion of the first signal conditioning circuit 601b is coupled to an output port of the second portion of the first signal conditioning circuit 605 using an electrical connection 602c, where an output port of the third portion of the first signal conditioning circuit 601b forms an RF signal output port 600b. Thus, a first signal path is formed from the first RF signal input port 600a through to the first RF signal output port 600b.

[0045] A first portion of a second signal conditioning circuit 602 and the second portion of the second signal conditioning circuit 606 are disposed in series between a second RF signal input port 600c and a second RF signal output port 600d. A first ancillary circuit 603, in the form of a first voltage regulator circuit, is for providing a first regulated supply voltage to the first portion and third portions of the first signal conditioning circuit, 601a and 601b. The second ancillary circuit 604, in the form of a second voltage regulator circuit, is for providing a second regulated supply voltage to the second portion of the first signal conditioning circuit 605 and to the first and second portions of the second signal conditioning circuit, 602 and 606, through an electrical connection 620a.

An unregulated supply voltage from a source (not shown) is provided to the first and second regulator circuits through a positive supply voltage terminal 600e and a ground terminal 600f.

[0046] The function of the first signal conditioning circuit, 601a, 605 and 601b, is to provide a first signal conditioning function utilizing the portions thereof disposed in the first and second integrated circuit semiconductor dies, 611 and 612. Preferably, the second portion of the first signal conditioning circuit 605 is an interstage matching circuit for performing an impedance match between the first and third portions, 601a and 601b, which are preferably in the form of power amplifier circuits. Thus, for example, if the first integrated circuit semiconductor die 611 includes silicon and the second integrated circuit semiconductor die 612 includes GaAs, then a signal propagating from the first portion 601a leaves the first semiconductor substrate 611, using electrical connection 620b, for interstage matching using the second portion 605. Thereafter, once the signal has been interstage matched, the signal leaves the second integrated circuit semiconductor die 612 and is propagated along using electrical connection 620c to the first integrated circuit semiconductor die 611, where it is received by an input port of the third portion 601b.

[0047] Optionally, the second portion of the first signal conditioning circuit 605 is coupled to the RF input port 600a for receiving of the RF input signal directly and serves to provide an impedance match between the input port and the third portion of the first signal conditioning circuit 601b.

[0048] Advantageously, the integration of the second portion of the first signal conditioning circuit 605 within the second integrated circuit semiconductor die 612 allows for signal conditioning operations that are more easily, or more cost effectively, facilitated by devices manufactured within the second integrated circuit semiconductor die 612 to be performed by circuitry integrated within the second integrated circuit semiconductor die for a signal propagating along the first signal path. Furthermore, those devices that allow for signal conditioning operations that are more easily, or more cost effectively, facilitated by devices manufactured within the first integrated circuit

semiconductor die 611 to be performed by circuitry disposed within the first integrated circuit semiconductor die 611 for the signal propagating along the first signal path.

[0049] When the module design is performed, the signal conditioning circuit and ancillary circuits are integrated on the semiconductor dies in such a manner that the area of the die is minimized and other issues, such as noise and crosstalk, are also reduced. In the prior art, different signal conditioning and ancillary circuits are often disposed within the modules without foresight given to a reduction in module area and minimization of individual semiconductor die usage. Typically many different semiconductor dies are disposed within the module on the substrate, which unfortunately increases the manufacturing costs and does not result in a compact module size. Additionally, using some semiconductor manufacturing technologies is more costly for implementing of certain ancillary circuitry. For example, GaN and InP technologies have much larger costs associated with die area usage than silicon-based technologies. As a result, implementing an ancillary circuit in InP or GaN becomes significantly more expensive than implementing the functionally similar ancillary circuit in a silicon based technology.

[0050] Though the embodiments of the invention refer to two or more signal conditioning circuits such as power amplifiers, it is well understood and appreciated in the art that the efficient provision of ancillary circuits necessary or beneficial to the operation of other types of circuits is enabled using this invention. For example, other signal conditioning circuits, such as memory buffers are envisioned for use exclusively by a separate PLL-type circuit and die. In the context of a module, this invention is very useful because it obviates the placement of some additional dies within. It does, however, require that the IC designer and module designer work with an overall view of the module objectives and the requirements of the various functional circuits in the module. With this invention and the realization that some ancillary circuits will be integrated into the same semiconductor die area as the signal conditioning circuits unrelated to those ancillary circuits, the partitioning of signal conditioning circuits and the ancillary circuits becomes an optimization task.

[0051] Though the above embodiments refer to a SiGe BiCMOS manufacturing technology, other suitable manufacturing technologies for integration of the ancillary circuitry is also supported according to the invention.

[0052] The embodiments of the invention further advantageously allow for integration of silicon-based technologies with other technologies such as GaAs, InP, and GaN that do not support a similar level of component integration.

[0053] Numerous other embodiments may be envisaged without departing from the spirit or scope of the invention.

Claims

What is claimed is:

1. An electronic apparatus comprising:
a first integrated circuit semiconductor die comprising:
a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path; and
a second integrated circuit semiconductor die comprising:
a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first portion of a first signal conditioning circuit for a signal propagating along the first signal path; and,
a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.
2. An electronic apparatus according to claim 1, comprising a second signal conditioning circuit comprising a first portion of the second signal conditioning circuit and a second portion of the second signal conditioning circuit integrated within the second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path.
3. An electronic apparatus according to claim 2, wherein the first signal conditioning function and the second signal conditioning function provide similar signal conditioning functions.
4. An electronic apparatus according to claim 1, wherein the first integrated circuit die is manufactured using a first semiconductor process and utilizes a silicon based technology.

5. An electronic apparatus according to claim 4, wherein the second integrated circuit die is manufactured using a second semiconductor process and utilizes other than a silicon based technology.
6. An electronic apparatus according to claim 1, wherein the first portion of the first signal conditioning circuit comprises at least a power amplifier circuit and where the function of the first portion of the first signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit.
7. An electronic apparatus according to claim 6, wherein the second portion of the first signal conditioning circuit comprises an impedance matching circuit.
8. An electronic apparatus according to claim 2, wherein the second signal conditioning circuit comprises at least a power amplifier circuit and where the function of the first portion of the second signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit.
9. An electronic apparatus according to claim 8, wherein the second portion of the second signal conditioning circuit comprises an impedance matching circuit and where the function of the first portion of the second signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit.
10. An electronic apparatus according to claim 2, wherein the first semiconductor process does not facilitate manufacturing and integration of at least one of the second portion of the first signal conditioning circuit and the second portion of the second signal conditioning circuit.
11. An electronic apparatus according to claim 1, wherein the second integrated circuit die is manufactured using a second semiconductor process that is different from that used to manufacture the first integrated circuit die.

12. An electronic apparatus according to claim 1, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.

13. An electronic apparatus according to claim 12, wherein the second integrated circuit die is derived from a second semiconductor wafer that is comprised of other one of Si, SiGe, GaAs, InP, and GaN.

14. An electronic apparatus according to claim 1, wherein the first integrated circuit die is manufactured using a BiCMOS process.

15. An electronic apparatus according to claim 1, wherein the second portion of the first signal conditioning circuit comprises at least one of a capacitor and an inductors and a signal transmission line.

16. An electronic apparatus according to claim 2, comprising:
a first ancillary circuit integrated within the first integrated circuit die and electrically coupled to the first portion of the first signal conditioning circuit for use during operation thereof.

17. An electronic apparatus according to claim 16, comprising a second ancillary circuit integrated within the first integrated circuit semiconductor die and electrically coupled to the second portion of the first signal conditioning circuit and to the first and second portions of the second signal conditioning circuit for other than performing the first or the second signal conditioning function and for use by the second portion of the first signal conditioning circuit and the first and second portions of the second signal conditioning circuit during operation thereof.

18. A method of manufacturing a module comprising:

providing a first signal conditioning circuit comprising a first portion and a second portion;
implementing the first portion of the first signal conditioning circuit within a first semiconductor die;
implementing the second portion of the first signal conditioning circuit within a second semiconductor die;
bonding the first and second dies to a common substrate; and,
forming electrical connections between the two dies to complete the first signal conditioning circuit from the first portion of the first signal conditioning circuit and the second portion of the first signal conditioning circuit.

19. A method according to claim 18, comprising:

providing a second signal conditioning circuit comprising a first portion and a second portion; and,
implementing the first and second portions of the second signal conditioning circuit in the second semiconductor die.

20. A method according to claim 18, wherein the first semiconductor die comprises a first portion of a first signal path and the second semiconductor die comprises a second portion of the first signal path, the first signal path disposed between a first input port and a first output port.

21. A method according to claim 20, wherein the second semiconductor die comprises a second signal path that is other than the second portion of the first signal path and in approximate RF isolation therefrom.

22. A method according to claim 18, wherein the second semiconductor die is manufactured using a more expensive semiconductor process than that used for manufacturing of the first semiconductor die.

23. A method according to claim 18, wherein the first portion of the first signal conditioning circuit is more cost effectively implemented in the first semiconductor die.
24. A method according to claim 18, wherein the first semiconductor die does not facilitate implementation of the second portion of the first signal conditioning circuit therein.
25. A method according to claim 18, wherein implementing of the second portion of the first signal conditioning circuit within the second semiconductor die provides increased performance in signal conditioning as compared to implementing of the second portion of the first signal conditioning circuit within the first semiconductor die.
26. A method according to claim 18, wherein prior to implementing the first signal conditioning circuit comprises partitioning of the first signal conditioning circuit into the first portion and the second portion.
27. An electronic apparatus comprising:
a first integrated circuit semiconductor die comprising:
a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path;
a third portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along the first signal path; and
a second integrated circuit semiconductor die comprising:
a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first and third portions of the first signal conditioning circuit for a signal propagating along the first signal path; and,
a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.

28. An electronic apparatus according to claim 27, comprising:
- a first RF signal input port coupled with an input port of the first portion of the first signal conditioning circuit for receiving of a first RF input signal; and
 - a first RF signal output port coupled with an output port of the third portion of the first signal conditioning circuit for providing of a first RF output signal,
- wherein the first signal path is disposed between the first RF signal input port and the first RF signal output port,
- wherein the coupling circuit comprises;
- a first electrical connection disposed between an output port the first portion of the first signal conditioning circuit and an input port of the second signal conditioning portion of the first signal conditioning circuit; and,
 - a second electrical connection disposed between an output port the second portion of the first signal conditioning circuit and an input port of the third signal conditioning portion of the first signal conditioning circuit.
29. An electronic apparatus according to claim 27, comprising:
- a first RF signal input port coupled with an input port of the second portion of the first signal conditioning circuit for receiving of a first RF input signal; and
 - a first RF signal output port coupled with an output port of the third portion of the first signal conditioning circuit for providing of a first RF output signal,
- wherein the first signal path is disposed between the first RF signal input port and the first RF signal output port,
- wherein the coupling circuit comprises;
- a second electrical connection disposed between an output port the second portion of the first signal conditioning circuit and an input port of the third signal conditioning portion of the first signal conditioning circuit.
30. An electronic apparatus according to claim 27, comprising a second signal conditioning circuit comprising a first portion of the second signal conditioning circuit and a second portion of the second signal conditioning circuit integrated within the

second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path;

31. An electronic apparatus according to claim 27, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.

32. An electronic apparatus according to claim 31, wherein the second integrated circuit die is derived from a second semiconductor wafer that is comprised of the other one of Si, SiGe, GaAs, InP, and GaN.

33. An electronic apparatus according to claim 27, wherein the second portion of the first signal conditioning circuit comprises an interstage matching circuit.

34. An electronic apparatus according to claim 27, comprising a first ancillary circuit integrated within the first integrated circuit die and electrically coupled to the first portion and the third portion of the first signal conditioning circuit for use during operation thereof.

35. An electronic apparatus according to claim 34, comprising a second ancillary circuit integrated within the first integrated circuit semiconductor die and electrically coupled to the second portion of the first signal conditioning circuit for use during operation thereof.

Abstract

A first signal conditioning circuit is formed from a first portion, a second portion and a third portion. Signal conditioning functions of each of these portions are facilitated by a predetermined type of integrated semiconductor die within which they are formed. Two different semiconductor dies are thus provided for facilitating integration of the first through third signal conditioning portions therein. Wire bonds are provided between the two different semiconductor dies in order to form circuit paths between the different first through third portions. The signal routing using between the two different semiconductor dies provides for completing of the first signal conditioning circuit having a first signal conditioning function. For example, circuits such as interstage matching circuits are disposed on a different semiconductor die than power amplifier circuits.

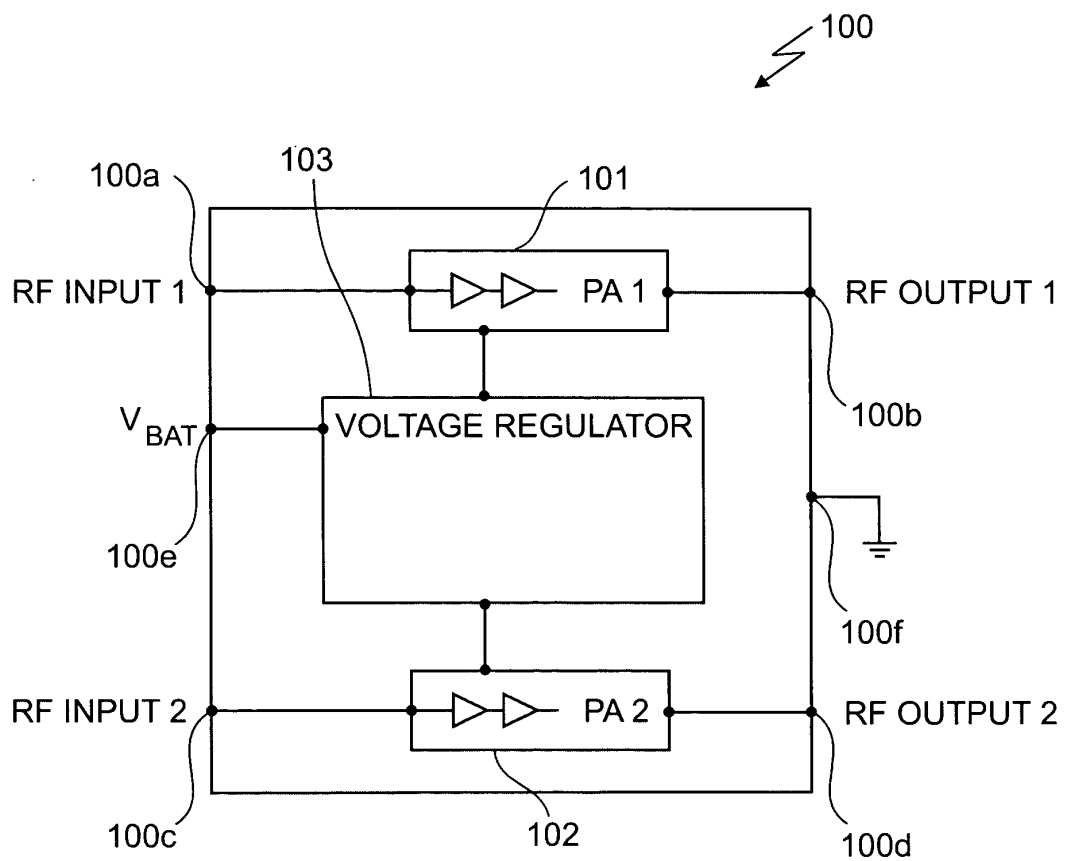


Figure 1
(PRIOR ART)

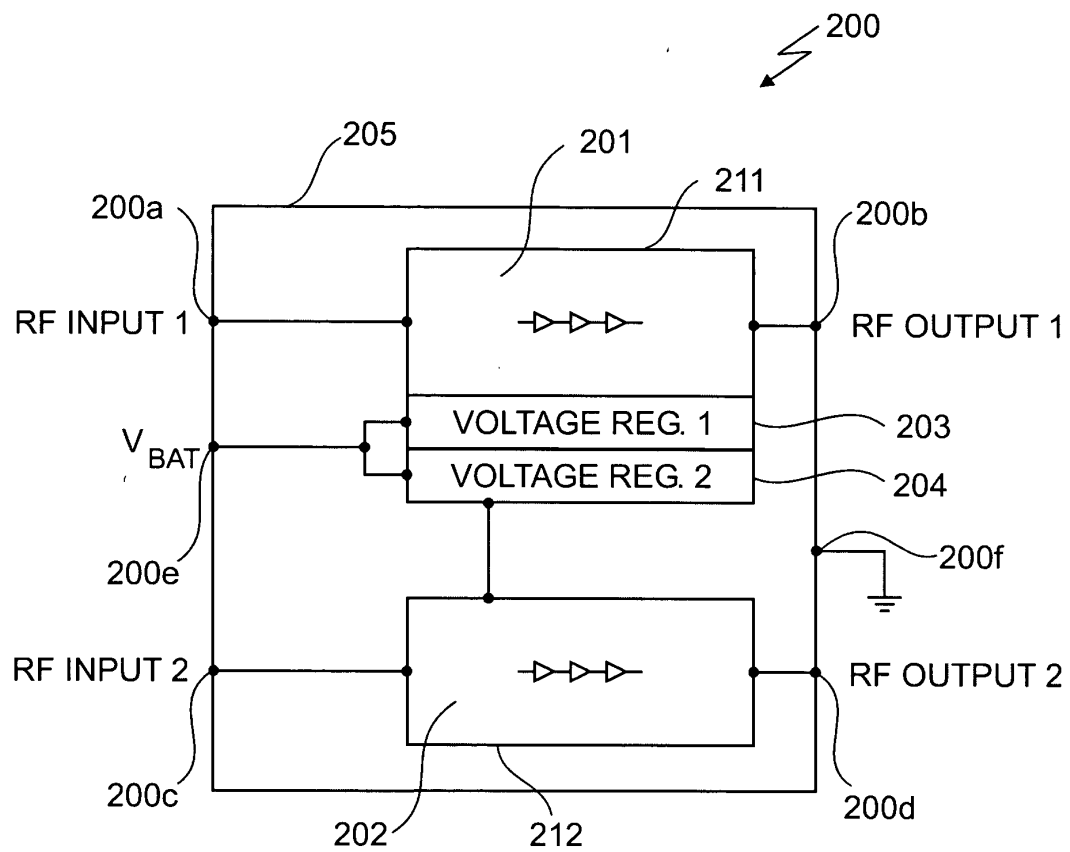


Figure 2

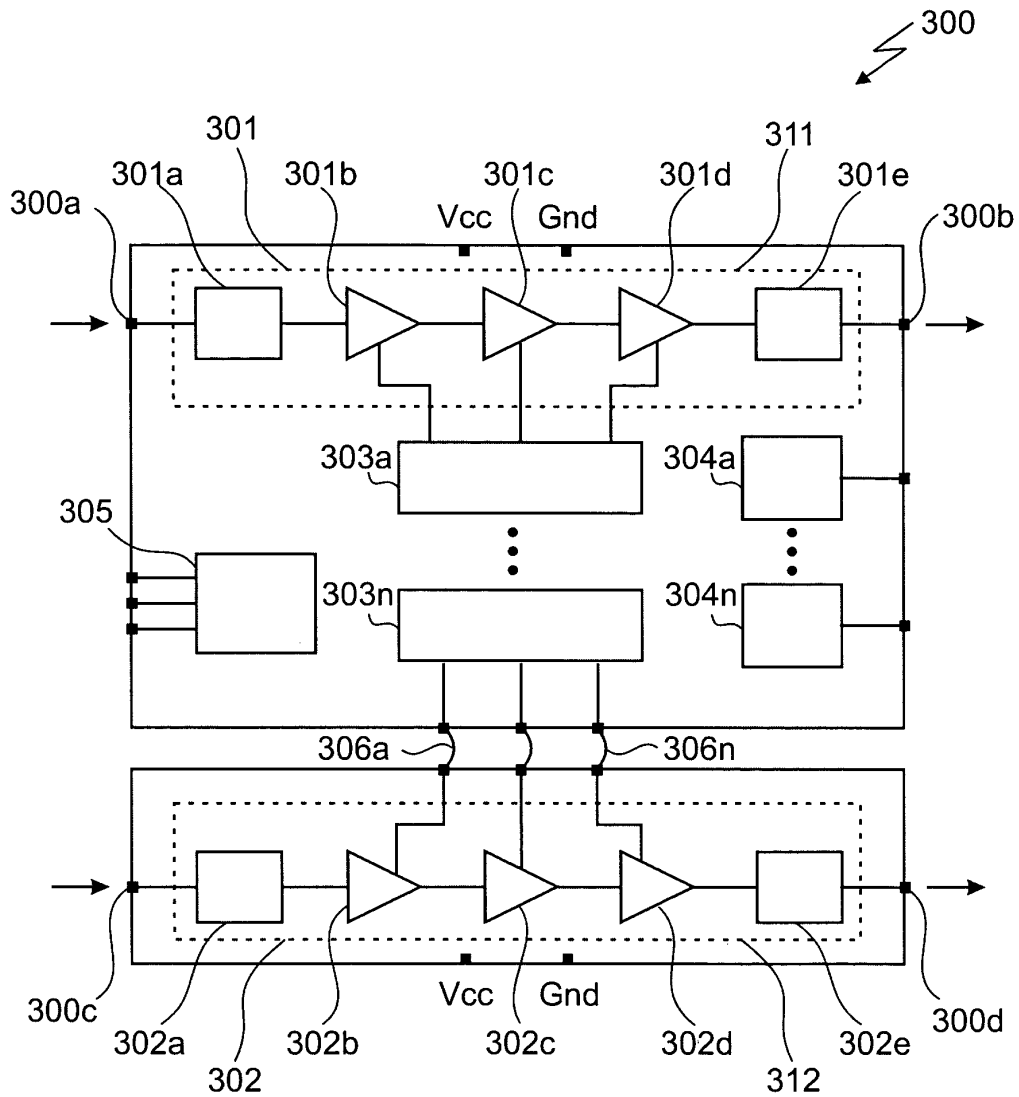


Figure 3

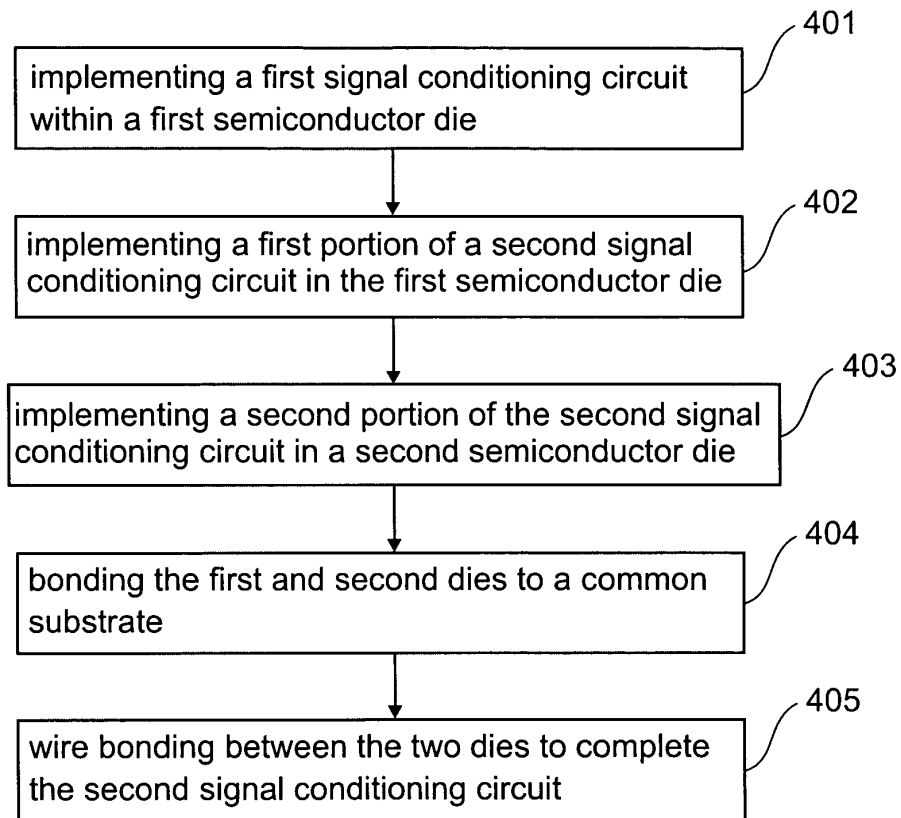


Figure 4

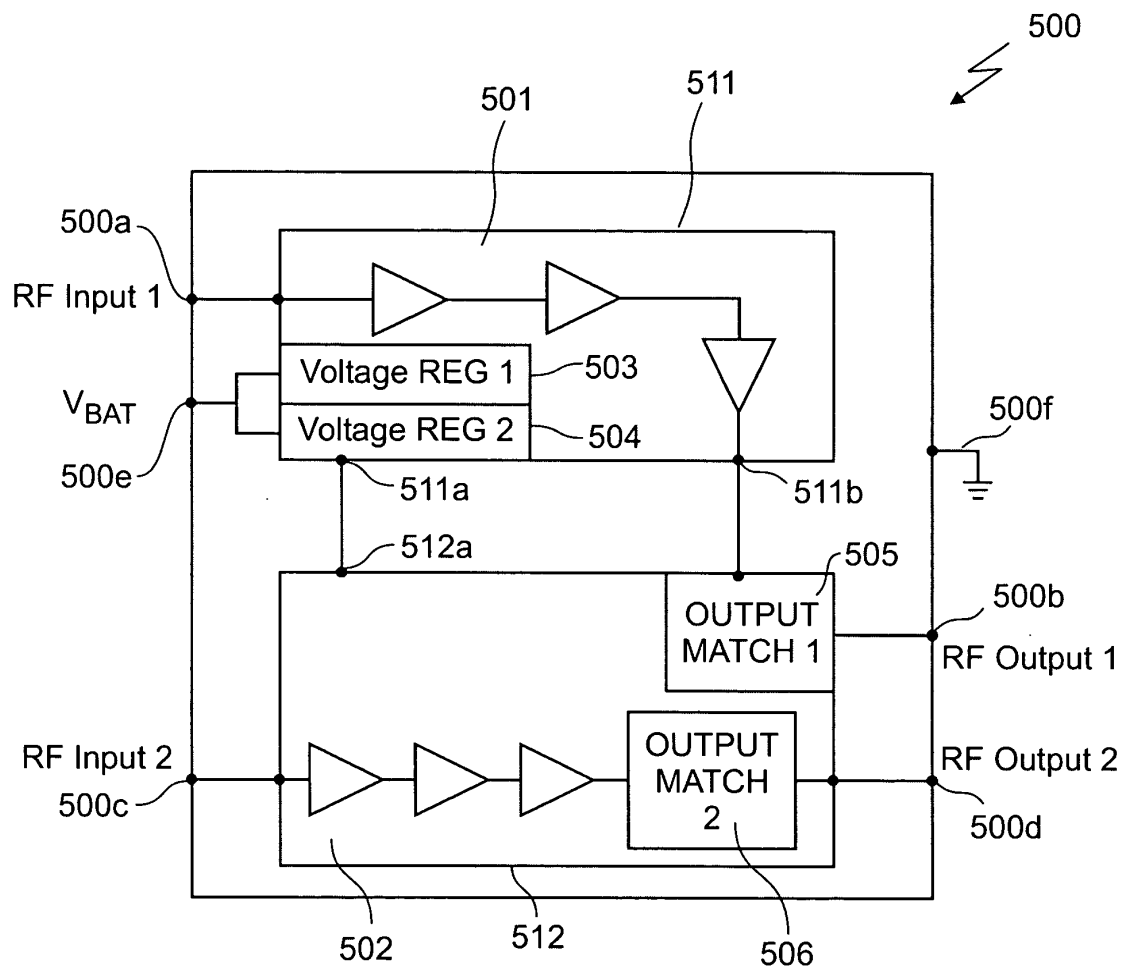


Figure 5

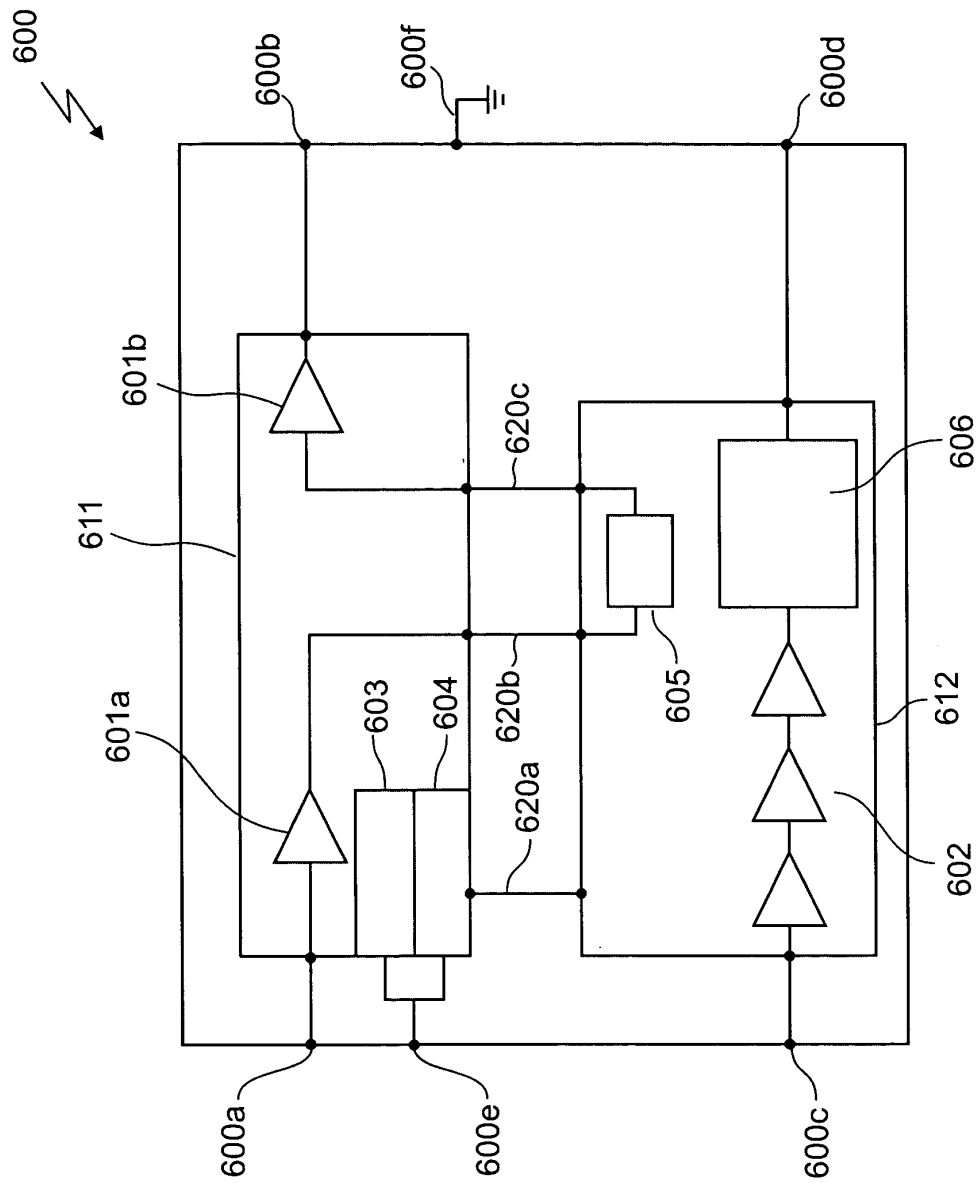


Figure 6

COMBINED DECLARATION & POWER OF ATTORNEY FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63) ☒ Declaration Submitted With Initial Filing OR ☐ Declaration Submitted After Initial Filing (37 CFR 1.16(e) Required)	Attorney Docket Number	115-34USCIP/12667/100126
	First Named Inventor	James H. Derbyshire
	COMPLETE IF KNOWN	
	Application Number	New Filing
	Filing Date	
	Group Art Unit	
	Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Module Integration Integrated Circuits

the specification of which

☒ is attached hereto OR

☐ as filed on (MM/DD/YYYY) _____ as United States Application Number _____ or PCT International Application Number _____ and was amended on (MM/DD/YYYY)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365 (b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?	
				Yes	No

☐ Additional foreign application numbers are listed on a supplementary priority data sheet (PTO/SB/02B) attached hereto:

COMBINED DECLARATION & POWER OF ATTORNEY- Utility or Design Patent Application		Attorney Docket No. 115-34USCIP/12667/100126	
I hereby appoint Practitioners at Customer Number 23838			
as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith.			
Direct all correspondence to: Gary Morris, Reg. No. 40,735 Kenyon & Kenyon 1500 K Street, N.W., Suite 700 Washington, DC 20005-1257 PHONE: (202) 220-4200 FAX: (202) 220-4201			
I hereby declare that all statements made herein of my own knowledge are true and that all statements were made on information and belief are believed to be true; and further that these statements were made with the knowledge that wilful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardize the validity of the application or any patent issued thereon.			
NAME OF SOLE OR FIRST INVENTOR:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle [if any]) James H.		Family Name or Surname Derbyshire	
Inventor's Signature <i>James Derbyshire</i>		Date <i>28 May 2004</i>	
Residence: City Ottawa	State Ontario	Country Canada	Citizenship Canadian
Mailing Address 470 Manor Avenue			
City Ottawa	State Ontario	ZIP K1M 0H9	Country Canada
NAME OF SECOND INVENTOR:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle [if any]) Alan J.A.		Family Name or Surname Trainor	
Inventor's Signature		Date	
Residence: City Harlow	State Essex	Country United Kingdom	Citizenship British
Mailing Address 1 Jocelyns			
City Harlow	State Essex	ZIP CM17 0BT	Country United Kingdom
NAME OF THIRD INVENTOR:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle [if any])		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	ZIP	Country
☐ Additional Inventors are being named on the supplemental Additional Inventors sheet PTO/SB/02A attached hereto.			

COMBINED DECLARATION & POWER OF ATTORNEY- Utility or Design Patent Application		Attorney Docket No. 115-34USCIP/12667/100126	
I hereby appoint Practitioners at Customer Number 23838 as my/our attorney(s) or agent(s) to prosecute the application identified above, and to transact all business in the United States Patent and Trademark Office connected therewith. Direct all correspondence to: Gary Morris, Reg. No. 40,735 Kenyon & Kenyon 1500 K Street, N.W., Suite 700 Washington, DC 20005-1257 PHONE: (202) 220-4200 FAX: (202) 220-4201 I hereby declare that all statements made herein of my own knowledge are true and that all statements were made on information and belief are believed to be true; and further that these statements were made with the knowledge that wilful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardize the validity of the application or any patent issued thereon.			
NAME OF SOLE OR FIRST INVENTOR:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle [if any]) James H.		Family Name or Surname Derbyshire	
Inventor's Signature		Date	
Residence: City Ottawa	State Ontario	Country Canada	Citizenship Canadian
Mailing Address 470 Manor Avenue			
City Ottawa	State Ontario	ZIP K1M 0H9	Country Canada
NAME OF SECOND INVENTOR:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle [if any]) Alan J.A.		Family Name or Surname Trainor	
Inventor's Signature <i>Alan J.A. Trainor</i>		Date <i>27 May 2004</i>	
Residence: City Harlow	State Essex	Country United Kingdom	Citizenship British
Mailing Address 1 Jocelyns			
City Harlow	State Essex	ZIP CM17 0BT	Country United Kingdom
NAME OF THIRD INVENTOR:		☐ A petition has been filed for this unsigned inventor	
Given Name (first and middle [if any])		Family Name or Surname	
Inventor's Signature		Date	
Residence: City	State	Country	Citizenship
Mailing Address			
City	State	ZIP	Country
☐ Additional Inventors are being named on the supplemental Additional Inventors sheet PTO/SB/02A attached hereto.			

PATENT APPLICATION SERIAL NO. _____

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET

06/04/2004 HMARZI1 00000065 501142 10857938

01 FC:2001	385.00 DA
02 FC:2202	135.00 DA

PTO-1556
(5/87)

*U.S. Government Printing Office: 2002 — 489-267/86033

PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2003

Application or Docket Number

10857938

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	35	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	35 minus 20 =	15
INDEPENDENT CLAIMS	3 minus 3 =	
MULTIPLE DEPENDENT CLAIM PRESENT ☐		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**
Independent	*	Minus	***
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**
Independent	*	Minus	***
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**
Independent	*	Minus	***
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM ☐			

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SMALL ENTITY TYPE ☐

OR OTHER THAN SMALL ENTITY

RATE	FEE
BASIC FEE	385.00
X\$ 9=	135
X43=	
+145=	
TOTAL	520

RATE	FEE
BASIC FEE	770.00
X\$18=	
X86=	
+290=	
TOTAL	

SMALL ENTITY OR

OTHER THAN SMALL ENTITY

RATE	ADDITIONAL FEE
X\$ 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$ 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$18=	
X86=	
+290=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$ 9=	
X43=	
+145=	
TOTAL ADDIT. FEE	

RATE	ADDITIONAL FEE
X\$18=	
X86=	
+290=	
TOTAL ADDIT. FEE	



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450



Utility Patent Application Transmittal

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No: 115-34USCIP/12667/100126
First Inventor: James H. Derbyshire
Title: Module Integration Integrated Circuits

Application Elements:

1. ☒ Fee Calculation (see Box 14)
2. ☒ Applicant claims small entity status.
3. ☒ Specification Total Pages - 25
 - Description
 - Claims
 - Abstract of the Disclosure
4. ☒ Drawing(s) - (6 Figures) Total Sheets - 6
5. ☒ Oath or Declaration Total Pages - 3
 - a. ☒ Newly executed (original or copy)
 - b. ☐ Unexecuted
 - c. ☐ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 12 completed)
 - i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in
the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

Accompanying Application Parts:

6. ☒ Assignment Papers (cover sheet & document(s))
7. ☐ Information Disclosure Statement (IDS)/PTO-1449 Copies of IDS Citations ☐
8. ☐ Preliminary Amendment
9. ☒ Return Receipt Postcard *(Should be specifically itemized)*
10. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
11. ☐ Other:

Attorney Docket No: 115-34USCIP/12667/100126
First Inventor: James H. Derbyshire

Page 2

12. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

☐ Continuation of prior Application No. ☐ Divisional filed ☐ Continuation-in-part (CIP)

Prior application information: Examiner: Group Art Unit:

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5c, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon which a portion has been inadvertently omitted from the submitted application parts.

13. CORRESPONDENCE ADDRESS: 23838

Gary Morris, Reg. No. 40,735
Kenyon & Kenyon
1500 K Street, N.W., Suite 700
Washington, DC 20005-1257
PHONE: (202) 220-4200
FAX: (202) 220-4201

Agent: Gary Morris, Reg. No. 40,735

14. FEE CALCULATION:

☒ Applicant Claims Small Entity Status						AMOUNT
1. BASIC FILING FEE						
Large Entity			Small Entity			
Fee Code	Fee (\$)		Fee Code	Fee (\$)		
1001	770.00		2001	385.00		
						\$385.00
2. EXTRA CLAIM FEES						
				Extra Claims	Fee From Below	
Total Claims	35	-	20 =	15	x \$9.00 =	
Independent Claims	3	-	3 =	0	x \$43.00 =	
Multiple Dependent				\$** =		
Large Entity			Small Entity			
Fee Code	Fee (\$)		Fee Code	Fee (\$)		
1202	18.00		2202	9.00		
1201	86.00		2201	43.00		
3. OTHER						
Fee Code - 8021	Fee (\$) - 40.00		Recording Patent Assignment			
						\$40.00
TOTAL						\$560.00

15. ☒ The Commissioner is hereby authorized to charge all fees in Box 14 above to Deposit Account 50-1142.
16. ☒ The Commissioner is hereby authorized to charge any additional fees required or credit any overpayment to Deposit Account No. 50-1142.

Date: June 2, 2004

Submitted By:



Gary Morris, Reg. No. 40,735
Telephone: (202) 220-4200



HW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application Of: Derbyshire et al. Our File No: 115-34 US CIP/12667/100126
Application No: 10/857,938 Art Unit: 2681
Filed: June 2, 2004 Examiner: Unknown
Title: Module Integration Integrated Circuits

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450 U.S.A.

**Information Disclosure Statement
- Under 37 CFR 1.97(e)(1)**

Sir:

Applicant submits herewith an Information Disclosure Statement (Form PTO-1449)
and copies of references listed therein.

The documents listed in the IDS were cited in a Search Report mailed
February 28, 2005 from the Canadian Patent Office in the corresponding PCT application
not more than three months prior to the filing of this statement.

Respectfully submitted,

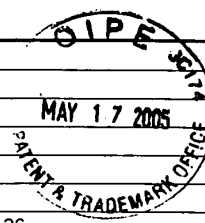
For *David J. Zibelli*
Gary Morris, Reg. No. 40,735
David J. Zibelli, 36,394
Kenyon & Kenyon
1500 K Street, N.W., Suite 700
Washington, DC 20005-1257

May 17, 2005
Date

Tel: (202) 220-4200
Fax: (202) 220-4201

/ml

Substitute form for form 1449A & 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application No.	10/857,938
		Filing Date	June 2, 2004
		First Named Inventor	Derbyshire et al.
		Group Art Unit	2681
		Examiner Name	Unknown
Sheet 1 of 1	Attorney Docket No.	115-34 US CIP/12667/100126	



U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
		5,258,325		Spitzer et al.	11-02-1993	
		5,731,945		Bertin et al.	03-24-1998	

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in capital letters), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
		Guckenberger et al., "Integrated DC-DC Converter Design for Improved WCDMA Power Amplifier Efficiency in SiGe BiCMOS Technology", Proceedings of the 2003 International Symposium on Low Power Electronics and Design ISLPED '03, Aug. 25-27, 2003, pp. 449-454	
		Diels et al., "Single Package Integration of RF Blocks for a 5 Ghz WLAN Application", IEEE Transactions on Advanced Packaging, vol. 24, no. 3, August 2001, pp. 384-391	

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

1 Unique citation designation number. 2 See attached Kinds of U.S. Patent Documents. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

IPW



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Application No: 10/857,938

Art Unit: 2681

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Title: Module Integration Integrated Circuits

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**Information Disclosure Statement
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Sir:

Applicant submits herewith an Information Disclosure Statement (Form PTO-1449)
and copies of references listed therein.

The documents listed in the IDS were cited in a Search Report mailed
September 29, 2005 from the ISA/CA in the second corresponding PCT application not
more than three months prior to the filing of this statement.

Respectfully submitted,

A handwritten signature in black ink, appearing to be "G. Morris".

Gary Morris, Reg. No. 40,735

Kenyon & Kenyon
1500 K Street, N.W., Suite 700
Washington, DC 20005-1257

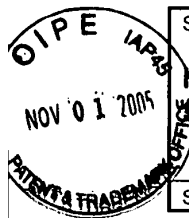
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Date

Tel: (202) 220-4200

Fax: (202) 220-4201



Substitute form for form 1449A & 1449B/PTO		Complete if Known	
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		Filing Date	June 2, 2004
		First Named Inventor	Derbyshire et al.
		Group Art Unit	2681
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Sheet 1 of 1	Attorney Docket No.	115-34 US CIP/12667/100126	

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
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		Office ³	Number ⁴	Kind Code ⁵ (if known)				
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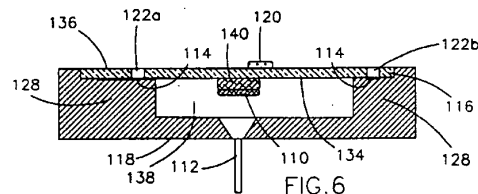
(71) Applicant: **DELCO ELECTRONICS CORPORATION**
700 East Firmin Street
Kokomo Indiana 46902(US)

(72) Inventor: **Matly, John Michael**
4208 Brooke Road
Kokomo, IN 46902(US)
Inventor: **Dawson, Janet Soong**
3408 Melody Lane
East Kokomo, IN 46902(US)

(74) Representative: **Haines, Arthur Donald et al**
Patent Section 1st Floor Gideon House 28
Chapel Street
Luton, Bedfordshire LU1 2SE (GB)

(54) **Pressure sensor and method of assembly thereof.**

(57) A pressure sensor assembly is provided containing a substrate (116) having signal conditioning circuitry (110,126,130) disposed on both surfaces (134,136) of the substrate (116), with the critical pressure sensing element (140) disposed on one surface (134) of the substrate (116) and the laser trimmable resistors (120) disposed on the other surface (136) of the substrate (116). A ported housing (118) seals the one side (134) of the substrate (116) containing the pressure sensing element (140), thereby forming a pressurizable chamber while having the signal conditioning circuitry (126,130) and resistors (120) on the other surface (136) exposed for calibration by laser trimming of the resistors (120). This eliminates the requirement for a separate housing for the critical pressure sensing element (140). In addition, when the ported housing (118) is mounted to the pressure sensing side (134) of the substrate (116) for formation of the sealed pressure chamber, the through-holes (122) which electrically interconnect the signal processing circuitry (110,126,130) on both sides (134,136) of the substrate (116) are also concurrently sealed.



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This invention relates to a pressure sensor and to a method of producing a pressure sensor. More particularly, an embodiment of this invention relates to the packaging and assembly of a pressure sensor, wherein the sensor employs a double sided substrate having thick film circuitry on both surfaces, as well as an enclosed pressure sensitive integrated circuit on one of those surfaces, yet exposed signal conditioning circuitry on the other surface allowing for calibration of that signal conditioning circuitry by laser trimming means.

Pressure sensors are used in automotive vehicles for a variety of purposes, such as for sensing the vacuum pressure at the intake manifold of a vehicle's engine, as well as for other applications. Generally, such pressure sensors contain a pressure sensitive element. A common type of pressure sensitive element includes a piezo-resistive silicon element which is integrated with appropriate adjusting circuitry in a monolithic silicon integrated circuit. The piezo-resistive silicon element typically contains a diaphragm and piezo-resistive strain sensors disposed on the diaphragm, which are connected to the adjusting circuitry for measuring the deflection of the diaphragm due to pressure changes.

Often, the pressure sensor requires calibration to compensate for the variations that tend to occur during manufacturing between individual pressure sensing elements and signal conditioning circuitry. To provide for this compensation, it is advantageous to include either separately or as part of the integrated circuit, a conditioning network that permits customized adjustment of the output parameters for the individual pressure sensor. This conditioning network typically is a network of resistors, of which some may be selectively modified or removed from the integrated circuit by laser trimming the area of the resistors or alternatively by opening fusible links in the network. However, in order to calibrate these pressure sensors, the critical pressure sensing element must first be enclosed within a pressurizable chamber.

In the past, many different types of pressure sensor assemblies have been disclosed. Often, the pressure sensing element has been disposed within a separate container for pressurization by means of a port, such as disclosed in US-A-4,295,117. The separate container allows the pressure sensing element to be appropriately pressurized while the signal conditioning circuitry remains exposed, thereby facilitating the laser trimming of the exposed circuitry during calibration. An illustrative example of this type of prior art pressure sensor assembly is illustrated in cross-section in Figure 1. (The size of the components shown in Figures 1 to 3 are enlarged for the purposes of this description.) The container 10

housing the pressure sensing integrated circuit is located adjacent to, but separate from, the substrate 16 having the associated signal conditioning circuitry. The container 10 is required so that the pressure sensing element can be pressurized. Both the container 10 and substrate 16 are glued to a backplate 14, therefore leaving only one side of the substrate 16 available for the signal conditioning circuitry. This is an inefficient use of substrate space and unduly increases the size of the assembly. During calibration of this type of sensor, pressure is applied to the pressure sensing element within the container 10 through a port 12. A laser is then able to access, from above, and trim the resistor 20 within the signal conditioning circuitry, before a cover 18 is attached.

This prior art approach of Figure 1 has generally been satisfactory, although has shortcomings. The separate container 10 housing the sensing element undesirably increases the number of components within the assembly. The use of a separate container 10 also requires that additional interface joints be formed within the assembly, which increases the number of processing steps, thereby possibly decreasing product reliability. Also, as stated above, by utilizing only a single side of the substrate 16 for the signal conditioning circuitry, the available area of the substrate is not efficiently maximized.

An alternative prior art approach is shown in cross-section in Figure 2. In this configuration, the critical pressure sensing element 10a is attached to a substrate 16 having the associated signal conditioning circuitry also disposed thereon. The substrate 16 is attached to a backplate 14. The pressure sensing element 10a is not contained within a separate container. Rather, pressurization of only the rear of the pressure sensing element 10a is achieved by means of the port 12. In this embodiment, thus, the sensing of pressure changes at the rear of the sensing element is needed for calibration of a resistor 20 within the signal processing circuitry. After laser trimming, a cover 18 is attached to seal and protect the components.

This second approach is problematic in that, again, only a single side of the substrate 16 can support signal conditioning circuitry, since the second side is necessarily sealed by the backplate 14 for pressurization during calibration of the pressure sensing element 10a through the port 12. Therefore, the second side cannot be exposed to the laser trimming operations, leaving only the topside available for the signal conditioning circuitry. In addition, rear sensing technology is required.

Another illustrative prior art approach is shown in cross-section in Figure 3. Here, the substrate 16 is suspended within a housing 18, therefore

permitting both sides of the substrate 16 to support signal conditioning circuitry. However, in order to calibrate the resistors 20a and 20b of the signal conditioning circuitry, the resistors 20a and 20b must be exposed. This, therefore, requires that the pressure sensing integrated circuit be enclosed within its own container 10 and pressurized by means of the port 12, since the sealing cover 18 is not attached until after the laser trimming operations carried out during calibration. Although this approach allows both sides of the substrate 16 to support signal conditioning circuitry, the design is still less than ideal since the pressure sensing element requires a separate pressurizable container 10. In addition, a design such as this would most probably include electrically conductive through-holes for electrical interconnection of the two sides of signal conditioning circuitry. For calibration, these through-holes would also require sealing, unless the pressure sensing integrated circuit was sealed in its own container, as shown.

US-A-4,756,193 and US-A-4,859,227 have offered an alternative approach to housing the pressure sensing element within a separate container. Both these patents leave the pressure sensing chip in an open chamber and then enclose it by means of a flange on the pressure application nozzle. Therefore, when the chamber requires pressurization, such as for the calibration operation, the pressure sensing element is sealed by the flange of the pressure application nozzle. This has been a satisfactory approach; however, this design utilizes only a single side of the device for supporting the signal conditioning circuitry.

The present invention seeks to provide an improved pressure sensor and method of producing such a pressure sensor.

According to an aspect of the present invention, there is provided a pressure sensor as specified in claim 1.

This invention can provide a pressure sensor assembly which maximizes the efficiency of the design by employing a double sided substrate for population by signal conditioning circuitry, and by eliminating the requirement for separately containing the pressure sensitive element. In addition, such a pressure sensor could facilitate the calibration of the signal conditioning circuitry of the pressure sensing element by laser trimming operations. Furthermore, such a pressure sensor can be amenable for manufacturing by automotive production techniques for use in automotive applications.

The invention can also provide a pressure sensor wherein the pressure sensing element is attached to one surface of a substrate, that surface being appropriately sealed and pressurized, yet wherein signal conditioning circuitry including

trimmable resistors, remains accessible for laser trimming during calibration, prior to final sealing of the pressure sensor.

Through-holes may be provided from one surface of the substrate to another at a perimeter of the substrate, allowing adhesive at the perimeter of the substrate to seal the through-holes.

According to another aspect of the present invention, there is provided a method of producing a pressure sensor as specified in claim 5.

Preferably, the method concurrently mounts the substrate to a housing and seals through-holes which provide electrical interconnection between the two sides of the substrate having disposed thereon signal conditioning circuitry.

In a practical embodiment, a pressure sensor assembly is provided which provides a substrate having signal conditioning circuitry disposed on opposite surfaces of a supporting substrate, with the pressure sensing element disposed on one of these surfaces and laser trimmable resistors disposed on the other surface of the substrate. A separate housing for the pressure sensing element is not required, since the preferred housing seals the side of the substrate containing the pressure sensing element thereby forming a pressurizable chamber, yet with the preferred housing, the resistors disposed on the opposite side of the substrate remain exposed for laser trimming during calibration.

Preferably, the housing includes a circumferential ledge, on which the supporting substrate rests. This ledge spaces the substrate up from the bottom surface of the housing, thereby forming an air-tight chamber below the substrate for the pressure sensing element. A port may be provided into the chamber within a wall of the housing for pressurization of the chamber. In addition, when the substrate is attached to the circumferential ledge of the housing for sealing the pressure sensing element, through-holes which electrically interconnect the signal processing circuitry on both of the substrates are also concurrently sealed, since the through-holes are preferentially disposed along the perimeter of the substrate so as to contact the circumferential ledge within the housing.

When the substrate is mounted to the circumferential ledge within the housing, the through-holes are preferably sealed and a pressure chamber is concurrently formed. After final calibration and laser trimming of the resistors provided on the opposite surface of the substrate, a cover may be attached to seal the exposed signal conditioning circuitry.

A significant advantage of this embodiment is that the signal-processing circuitry remains accessible until the final passivation treatment is ap-

plied to the assembly. Where thick film circuitry is utilized, such an advantage allows for final trimming of the resistors in the circuit for the purpose of correcting any signal output errors resulting from processing tolerances of the circuit and the pressure sensing element. In addition, the design of this assembly can efficiently provide for opposite surfaces of the supporting substrate to be populated by signal conditioning circuitry, therefore reducing the size of the substrate required and accordingly the size of the entire device. Also, a separate housing for the critical pressure sensing element may not be required since the pressure sensing side of the substrate can be sealed airtight while the other side of the substrate remains exposed for calibration, thereby minimizing the number of components and joints within the assembly. In addition, extra processing steps may not be required for sealing the electrical interconnection through-holes electrically connecting the circuitry disposed on both surfaces of the substrate.

The design of this embodiment can provide a small compact assembly amenable to automotive production techniques.

An embodiment of the present invention is described below, by way of illustration only, with reference to the accompanying drawings, in which:

Figures 1 to 3 are cross-sectional side views of the construction and arrangement of prior art pressure sensor assemblies;

Figure 4 is a cross-sectional bottom plan view of an embodiment of pressure sensor assembly showing a pressure sensing element and associated signal processing circuitry;

Figure 5 is a cross-sectional plan view of the pressure sensor assembly of Figure 4;

Figure 6 is a cross-sectional side view of the pressure sensor assembly taken along line 6-6 of Figure 4 showing a pressure chamber and sealed substrate; and

Figure 7 is a cross-sectional side view of the finished pressure sensor assembly of Figure 6.

As shown in Figures 4 to 7 (which are enlarged views), a pressure sensor assembly is provided which contains a substrate 116 having signal conditioning circuitry disposed on opposite surfaces 134 and 136 of the substrate 116, with the critical pressure sensing integrated circuit 110 disposed on the lower surface 134 of the substrate 116 and signal conditioning circuitry containing at least one resistor 120 disposed on the top surface 136 of the substrate 116 which can be laser trimmed during calibration. The housing 118 seals the bottom side 134 of the substrate 116 containing the pressure sensing chip 110, thereby forming a pressurizable chamber 138, while keeping the resistor 120 on the top surface 136 exposed for subsequent laser

trimming. In addition, when the lower surface 134 of the substrate 116 is secured to a circumferential ledge 128 of the housing 118 for formation of the pressure chamber 138, the through-holes 122 which electrically interconnect the circuitry provided on the two surfaces 134 and 136 are sealed at the same time.

With specific reference to Figure 4, a pressure sensing chip 110 is disposed on the lower surface 134 of an alumina substrate 116. The pressure sensing chip 110 preferably consists of a piezo-resistive silicon element which is integrated with adjusting circuitry in a monolithic silicon integrated circuit. The piezo-resistive silicon element typically contains a diaphragm and piezo-resistive strain sensors disposed on the diaphragm and connected to the adjusting circuitry for measuring the deflection of the diaphragm arising from pressure differentials across the diaphragm. Any other suitable means for sensing pressure changes could be employed instead of this type of pressure sensing integrated circuit 110.

The pressure sensing circuit 110 is bonded to the top of a rectangle (or other shape corresponding to the lower surface of pressure sensing circuit 110) of PyrexTM glass or suitable material. A layer of a suitable bonding agent is deposited evenly onto the bottom surface 134 of the substrate 116 at that region where the sensing element 110 is to be attached. The bonding agent ensures uniform adhesion between the components. A preferred bonding agent might be a silicone adhesive, such as Dow Corning 6611 silicone compound. This compound is a high purity silicone having an additional advantage of avoiding ionic contamination of the sensitive electronic circuitry.

The base of the glass layer is attached to the lower surface 134 of the substrate 116 by means of a suitable bonding agent, such as silicone adhesive. The glass layer provides an even transition between coefficients of thermal expansion for the various materials, while the silicone adhesive serves to absorb any undesirable stresses produced during use which could be transmitted directly to the sensing chip 110 if it were mounted directly to the substrate 116.

Additional associated thick film signal processing circuitry, represented by electrically conductive runners 126, is deposited on the lower surface 134 of substrate 116 and electrically connected to pressure sensing integrated circuit 110. The pattern of the runners 126 is merely an example, the actual pattern depending on the specific application for the pressure sensor.

The thick film signal conditioning circuitry represented by runners 126 on the lower surface 134 are in electrical communication with the thick film signal conditioning circuitry provided on the top

surface 136 of the substrate 116 by means of through-holes 122, represented by electrically conductive runners 130 in Figure 5. The electrically conductive runners 126 and 130 allow the input power and output signal to be transmitted to and from the pressure sensor chip 110 for signal conditioning and processing. The conditioned output signal is thereafter transmitted from the thick film circuitry 126 and 130 to the associated vehicle control system by means of external electrical connections (not shown), which are known in the art.

The thick film circuitry 126 and 130 is deposited onto the respective surfaces 134 and 136 of the alumina substrate 116 using conventional means such as silk screening techniques, although other techniques could also be used. The thick film circuitry 126 and 130 can be of any electrically conductive material, such as copper, nickel, palladium or silver or an electrically conductive alloy of these materials. A preferred composition for the thick film circuitry 126 and 130 is a conventional palladium-silver alloy due to its good conductivity and the expertise already available in the field of depositing such a material.

As stated above, electrically conductive through-holes 122a and 122b (shown in Figures 4 and 5) provide connection paths between the two surfaces 134 and 136 of the substrate 116 for electrically connecting the thick film circuitry 126 and 130 on both surfaces 134 and 136 of the substrate 116. The interior, cylindrical surface of the electrically conductive through-holes 122 is coated with an electrically conductive material, such as a conventional palladium-silver alloy, but may include any of those materials listed above for formation of the thick film circuitry. The actual number of through-holes 122 may vary depending on the specific application. Two through-holes 122a and 122b are shown in the embodiment, although it is reasonable to expect that there could be a large number of through-holes in a particular application.

The through-holes 122a and 122b contact respective bond pads 124a and 124b on the lower surface 134 of the substrate 116 (Figure 4) and respective bond pads 124c and 124d on the top surface 136 (Figure 5). The bond pads 124 are formed from the same electrically conductive material as the thick film circuitry 126, so as to ensure intimate and continuous contact between a bond pad 124 and a through-hole 122. Although the bond pads 124 do not need to be formed of the same electrically conductive material used for the thick film circuitry 126 and 130, it is practical and efficient to use the same material on a single surface of the substrate 116 so as to minimize processing steps. The uniform and continuous

contact between the through-holes 122 and bond pads 124 ensures continuous electrical connection between the thick film signal conditioning circuits 126 and 130 provided on both surfaces 134 and 136 of the substrate 116.

An advantage of this embodiment is that both surfaces 134 and 136 of the substrate 116 are designed to support signal conditioning thick film circuitry 126 and 130. This preferred design minimizes the space required for the signal conditioning circuitry 126 and 130, thereby providing an efficient and compact pressure sensor package.

As shown most clearly in Figures 4 and 5, the through-holes 122 are purposely positioned along the perimeter of the substrate 116. This readily enables the subsequent sealing and packaging of the pressure sensing integrated circuit 110, as described more fully below. In the preferred embodiment, regardless of the number of through-holes 122 employed, the through-holes 122 are all positioned along the perimeter of the substrate 116. In addition, it is to be noted that the through-holes 122 may be useful for electromagnetic interference purposes as well as for electrically interconnecting the signal conditioning circuitry 126 and 130. For electromagnetic protection, some or all of the through-holes 122 would contact an electrical ground instead of contacting the bond pads 124 associated with the signal conditioning circuitry 126 and 130.

Figure 5 illustrates the top surface 136 of the substrate 116. A single resistor 120 is shown as part of the signal conditioning circuitry 130, although in practice, a plurality of resistors may be provided within the signal conditioning circuitry 130. In addition, although not shown in Figure 4, resistors may be provided on the opposite, lower surface 124 of the substrate 130 as well. However, these resistors would not be accessible by laser trimming methods during calibration. In addition, as stated above with reference to Figure 4, the exact pattern delineated by the thick film circuitry 130 is dependent on the particular application, as will be apparent to the person skilled in the art. The resistor 120 is preferably of a ruthenium thick film material deposited onto the surface 136 using conventional means such as silk screening.

As shown in Figure 6, the lower surface 134, which forms a pressure sensing side of substrate 116, is enclosed within a ported housing 118. The ported housing 118 is preferably formed from a rigid light-weight material, such as Celanex 3300D, a 30% glass filled polyester commonly referred to throughout the industry as "PBT", although other suitable materials could also be employed.

The ported housing 118 contains an integral circumferential ledge 128 disposed around its cir-

cumference for concurrently sealing the through-holes 122 on formation of the pressure chamber 138. The pressure sensing integrated circuit 110 must be in a sealed pressure chamber 138 in order to calibrate the sensor and to operate properly. The perimeter of the lower surface 134 of the substrate 116 is secured to the circumferential ledge 128 of the housing 118 by suitable means, such as Dow Corning 6611 silicone adhesive, although other suitable materials could also be used. This adhesive region is represented by region 114 on the lower surface 134 of the substrate 116 (also shown in Figure 4).

The through-holes 122, which electrically interconnect the signal processing circuitry 126 and 130 on both surfaces 134 and 136 around the perimeter of the substrate 116, also contact the circumferential ledge 128 of the ported housing 118 so as to be sealed concurrently on formation of the pressure chamber 138. This concurrent sealing of the through-holes 122 ensures an air-tight pressure chamber 138 for the pressure sensing chip 110 and intimate adhesion between the ported housing 118 and the substrate 116.

A port 112 is provided within the ported housing 118 for pressurizing the pressure sensing chamber 138. The pressure sensing chamber 138, which encloses the pressure sensing integrated circuit 110, is found by the walls of the ported 118 and the bottom surface 134 of the substrate 116. The port 112 is preferably formed from a rigid molded plastics material, although can be formed from any suitable material that can withstand pressurization. In addition, it may be desirable to provide a plurality of ports 112 within the ported housing 118, depending on the application.

It is to be noted that the pressure sensing integrated circuit 110 can be located anywhere on the lower surface 134 of the substrate 116. It is advantageous that the pressure sensing chip 110 be placed near the centre of the substrate 116 for minimization of stress due to the movement of the diaphragm. However, at this location the chip 110 is the most exposed to the effects of pressurization from the port 112, which can cause other types of stresses. Therefore, in some circumstances it may be preferable to position the pressure sensing chip 110 near but not at the centre of the substrate 116.

During testing and calibration of the assembly, test pressures are applied through port 112 into the pressure sensing chamber 138 over a variety of temperatures. The signal conditioning circuitry 126 and 130 and resistor 120 on the top surface 136 of the substrate 116 are accordingly tested. If modification of the resistor 120 is required, a laser is used to trim the necessary area from the resistor 120, therefore adjusting its resistivity and its signal output. The use of laser trimming is known in the

microelectronics art and so will not be described in further detail herein.

It is to be recognized that this embodiment permits testing and adjusting to be carried out without requiring that the entire package, probes or test equipment be enclosed in any special low pressure atmosphere. Moreover, testing and adjusting does not require sensing of the rear surface of the substrate 116 or optical access to the surface of the pressure sensing chip 110.

After testing and calibration, a high temperature vulcanizing silicone passivation gel (not shown), such as Dow Corning Q3-6635, is fed into the chamber to protect the substrate 116 and overlaying circuitry 130 and components 120. Such a protective gel is very compliant for purposes of minimizing stresses due to thermal expansion and contraction of the gel in relation to the internal components of the pressure sensor assembly.

As shown in Figure 7, a top cover 132 is attached to the perimeter of the ported housing 118 to seal the exposed top surface 136 of the substrate 116 having the signal conditioning circuitry 130 and laser trimmed resistor 120. The top cover 132 is preferably formed from a rigid molded plastics material, such as the glass filled polyester employed to form the ported housing 118, or any suitable material. The top cover 132 is attached to the ported housing 118 by any suitable means, such as by the use of an adhesive like Dow Corning 6611 silicone compound.

An air gap of approximately 1.5 mm (1/16 inches) is left between the cover and the silicone passivation gel to provide for thermal expansion.

A significant advantage of this embodiment is that both the pressure sensing integrated circuit 110 and the hybrid thick film circuitry 126 and 130 are enclosed within a package in a manner which minimizes the weight and space requirements of the package. This is accomplished by efficiently utilizing both sides of the substrate 116 for supporting the circuitry. Furthermore, the pressure sensing integrated circuit 110 does not require a separate housing since the pressure sensing side of the substrate 116 is sealed air-tight by the ported housing 118.

An additional advantage is that the through-holes 122 are sealed concurrently as the substrate 116 is mounted to the housing 118, therefore eliminating additional processing steps. This is accomplished with the use of the preferred ported housing 118 which has a circumferential ledge 128 on which the supporting substrate 116 is mounted, which also seals the through-holes 122. This ledge 128 spaces the substrate 116 above the lower surface of the housing 116, thereby forming an air-tight pressure chamber 138 below the substrate 116 for the pressure sensing chip 110.

A further advantage is that the hybrid thick film circuitry remains accessible after being deposited onto the substrate 116 until the final passivation treatment is applied. This allows for final trimming of the resistors 120 in the circuitry 130 for the purpose of correcting any signal output errors resulting from processing of the individual elements of both the circuitry 130 and the pressure sensing integrated circuit 110 due to tolerances and thermally or mechanically induced stresses.

This design provides a small compact assembly which is amenable to automotive production techniques.

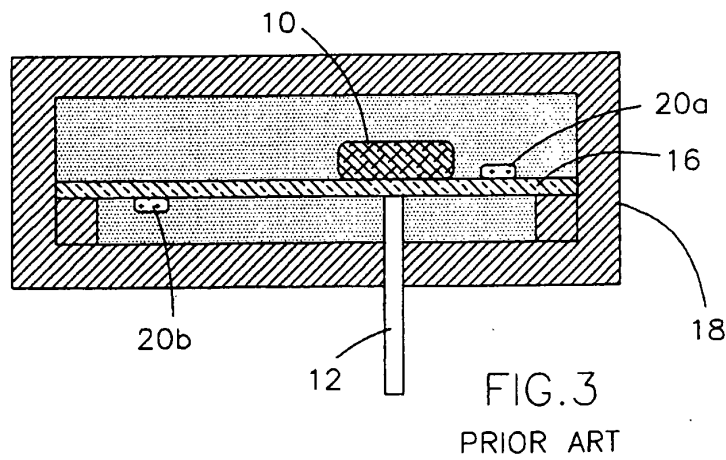
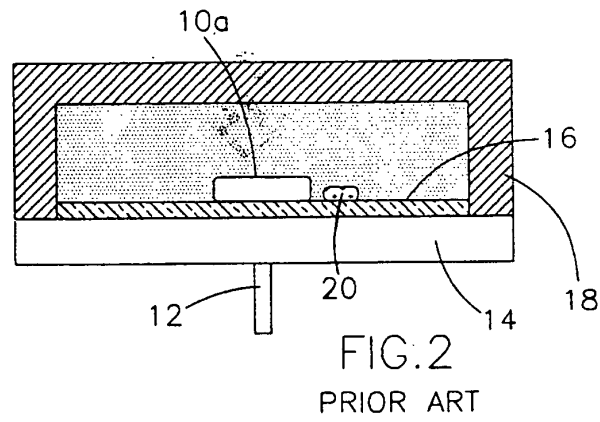
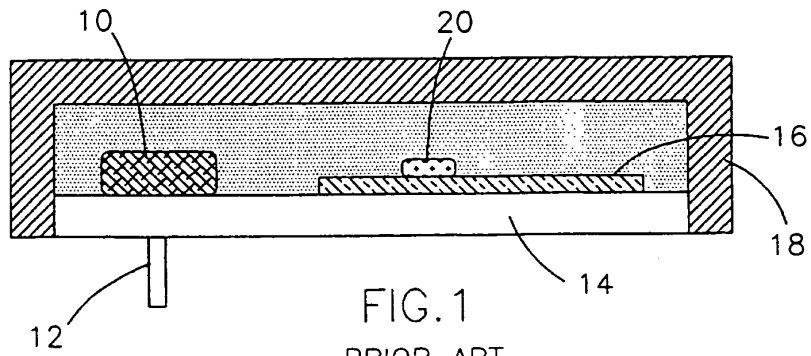
The ported housing could also be designed in such a manner as to form a pressure chamber at the same time as sealing the through-holes, even when the through-holes are not located along the perimeter of the substrate.

Claims

1. A pressure sensor comprising a substrate (116) including substantially oppositely disposed first and second surfaces (134,136); thick film signal conditioning circuitry (126,130) disposed on the first surface (134) and including at least one resistor (120) having a resistance adjustable in response to a signal output by the signal conditioning circuitry; a pressure sensing integrated circuit (110) disposed on the second surface and including a pressure sensitive element (140) and associated circuitry (110) for producing a pressure sensitive output signal; at least one electrically conductive passage (122a,122b) in the substrate coupled to the thick film signal conditioning circuitry and to the associated circuitry; and a ported housing (118) including a ledge (128), the substrate being mounted on the ledge and the or each passage being sealed so as to form a pressurized chamber enclosing the pressure sensing integrated circuit.
2. A pressure sensor according to claim 1, wherein the or each electrically conductive passage is located adjacent a perimeter of the substrate; the ledge of the ported housing extending along the perimeter of the substrate.
3. A pressure sensor according to claim 1 or 2, comprising a cover (32) for enclosing the first surface (136) of the substrate after adjustment of the resistance of the or each resistor disposed on the first surface of the substrate.
4. A pressure sensor according to any one of claims 1 to 3, wherein the substrate is of

alumina and the pressure sensing integrated circuit is of silicon.

5. A method of producing a pressure sensor comprising the steps of providing a substrate (116) including first and second surfaces (134,136); providing on the first surface (136) a thick film signal conditioning circuit (126,130) including at least one resistor (120) having an adjustable resistance; providing on the second surface (134) a pressure sensing integrated circuit (110) including a pressure sensitive element (140) and associated circuitry (110) for producing a pressure sensitive output signal; providing on the substrate at least one electrically conductive passage (122a,122b) for electrically interconnecting the thick film signal conditioning circuit and the associated circuitry; and enclosing the second surface (134) of the substrate by means of a ported housing (128) and substantially simultaneously sealing the or each electrically conductive passage so as to form a pressurisable chamber.
6. A method according to claim 5, wherein the or each electrically conductive passage is located adjacent a perimeter of the substrate.
7. A method according to claim 5 or 6, comprising the steps of pressurizing the chamber so as to cause the pressure sensitive integrated circuit and the signal conditioning circuit to produce an output signal; and adjusting the resistance of the or each resistor (120) disposed on the first surface in response to the output signal.
8. A method according to claim 7, comprising the step of enclosing the first surface of the substrate after adjustment of the or each resistor.
9. A method according to claim 8, wherein the substrate is enclosed in a manner as to make the pressure sensor air-tight.
10. A method according to claim 8 or 9, comprising the step of passivating the first surface of the substrate after adjustment of the or each resistor and before enclosing the first surface of the substrate.



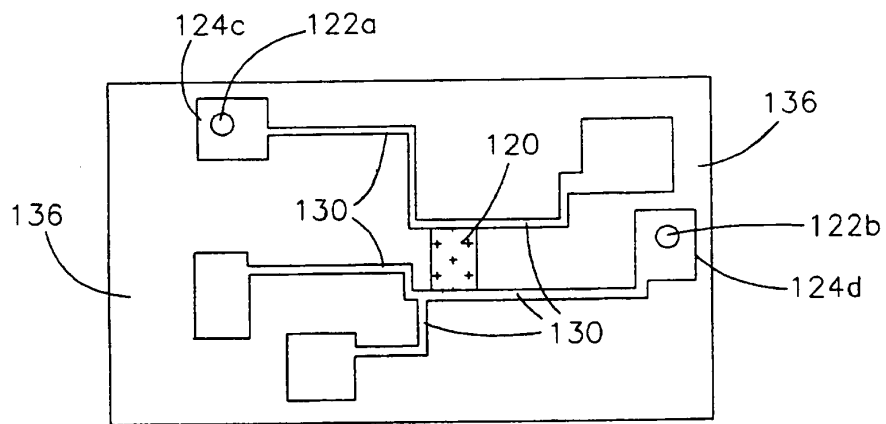
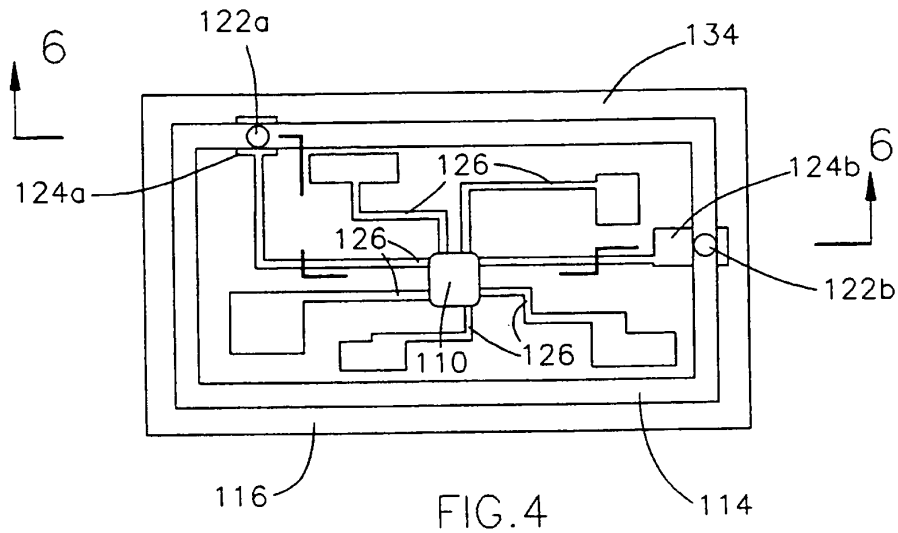


FIG.5

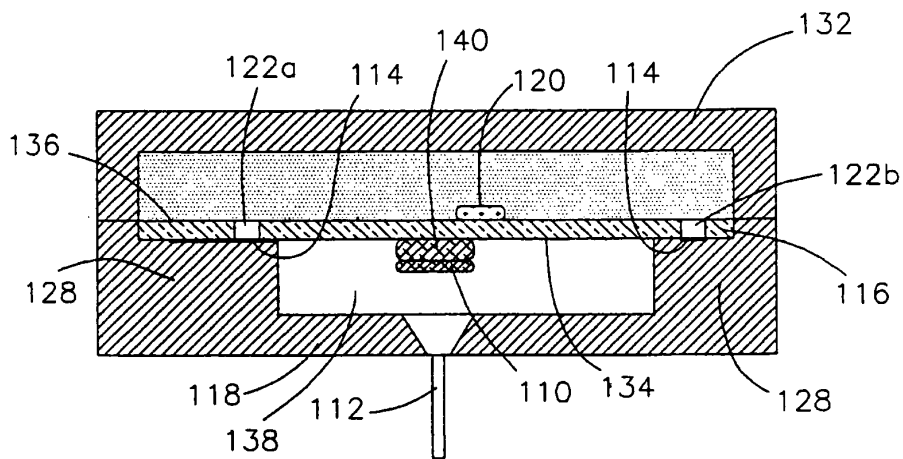
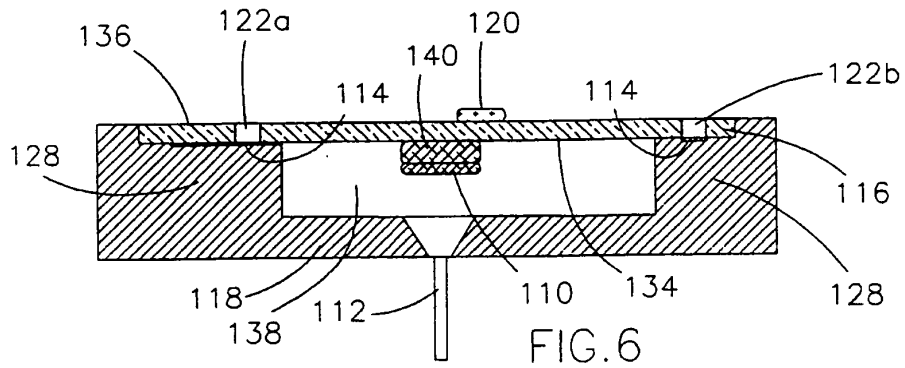


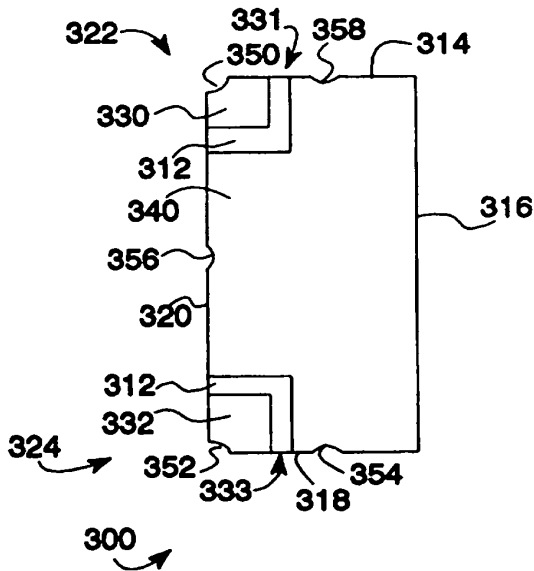
FIG. 7

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(21) International Application Number: PCT/US95/10769 (22) International Filing Date: 25 August 1995 (25.08.95) (30) Priority Data: 08/329,222 26 October 1994 (26.10.94) US (71) Applicant: BAIER & BAIER, INC. doing business as LARK ENGINEERING [US/US]; 27282 Calle Arroyo, San Juan Capistrano, CA 92675 (US). (72) Inventors: BREE, Daniel, R.; 4234 Serena Avenue, Oceanside, CA 92056 (US). LEM, Rafael; Prolongacion Aguas Calientes, 204 Col. Cacho, Tijuana, Baja California 22150 (MX). (74) Agent: KLEINKE, Bernard, L.; Suite 1580, 101 West Broadway, San Diego, CA 92101 (US).		(81) Designated States: AM, AT, AU, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, EE, ES, FI, GB, GE, HU, JP, KE, KG, KP, KR, KZ, LK, LR, LT, LU, LV, MD, MG, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SI, SK, TJ, TT, UA, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG), ARIPO patent (KE, MW, SD, SZ, UG). Published <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>
(54) Title: METHOD OF SURFACE MOUNTING RADIO FREQUENCY COMPONENTS AND THE COMPONENTS		
(57) Abstract The method of surface mounting radio frequency components includes using at least one radio frequency component (300, 810, 850) having a pair of input/output contact points (330, 332, 830, 832, 870, 872) or areas at corners on the underside of the component, wherein each of the input/output contact points or areas abuts the adjoining edges of the corners. The component is positioned relative to a pair of traces (846, 856, 858, 860) on a circuit for enabling an electrical connection thereto in a range of angular dispositions. By using a single non-customized component, adjacent components can be configured with a signal flow path of a range between about 0 degree (a chain configuration) and about 180 degrees (a "U" turn). 		

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Description**METHOD OF SURFACE MOUNTING RADIO FREQUENCY
COMPONENTS AND THE COMPONENTS****Technical Field**

5 The present invention relates in general to an improved method for surface mounting radio frequency components, and a radio frequency component for mounting in accordance with the improved mounting method. The invention more particularly relates to a method of
10 surface mounting radio frequency components in a manner which facilitates the placement of the components in close proximity to one another, and which can be accomplished with an improved radio frequency component.

Background Art

15 There have been many methods for the surface mounting of radio frequency components, in particular those components which interact with signals having frequencies between approximately one kilohertz and approximately twenty six gigahertz. An example of such a
20 prior art surface mounting method for radio frequency components required the use of a circuit board having a number of traces thereon in cooperation with components having electronic devices on a carrier. A pair of
25 input/output launch pads, or contact areas, located on the underside surface of the carrier member connected to the electronic devices provide an external connection point to the component.

 The prior known method requires the components to be positioned on the circuit board according to a
30 predetermined design. Once positioned, the contact points of the components have been connected to the traces by soldering. The components have been oriented on the circuit board to position the edges of the components preferably at right angles to the traces to

avoid unwanted perisitic effects where at least a portion of the high frequency signal can otherwise be lost.

While the prior known surface mounting technique for radio frequency components has served its purpose
5 generally in facilitating the assembly procedure, it has not provided a designer of radio frequency circuits with much flexibility. The lack of flexibility relates to the requirement for customization in the development process. The design of radio frequency circuits is an application
10 specific undertaking. The designer must not only specify the types of electronic devices contained within the component, but also specify the configuration of the board layout for the components for each radio frequency application. The configuration of each one of the
15 components is important, since it is desirable to have a high density clustering of the components on the board to reduce its overall size. As a result, the designer must not only design the layout of the traces on the circuit board, but also design the configuration of the
20 components to be used with the custom designed circuit board.

Efficiency can be increased by the designer by creatively arranging the positions of the components in the layout of the board. However, the customization of
25 each one of the components and the board layout required greatly increases the cost of producing radio frequency devices. Therefore, it would also be highly desirable to have a new and improved method of surface mounting radio frequency components which does not
30 require, or at least greatly reduces, required customization of the radio frequency components and the associated board layout, and which permits the manufacturing of radio frequency devices in a relatively inexpensive manner.

Another drawback of the conventional surface mounting technique for radio frequency components relates to the layout of the traces used to connect components. Due to the inherent characteristics of radio frequency signals, the traces are positioned on the circuit board in such a manner to eliminate right angle bends therein. Thus, instead of using a simple right angle bend to redirect the course of a trace, designers have resorted to the use of mitered corners and interconnecting trace segments at less severe angles, to achieve a desired circuit within the constraints imposed by the size of the circuit board.

Using mitered bends and other such design restrictions for the traces, the amount of circuit board is undesirably large to accommodate all of the required traces. The result has been an overly large board with a less than desirable density of components.

This inefficient use of the circuit board is even more apparent when bends and turns to the trace are required. For example, a 180° "U"-turn in a trace connecting two parallel chains of radio frequency components, such as filters, requires the dedication of a large area of the circuit board to accommodate a segmented U-shaped trace. Thus, valuable space on the board to accommodate the large U-shaped segmented trace is lost. Also, the U-shaped trace can cause an unwanted and undesirable loss of the radio frequency signal.

Therefore, it would also be highly desirable to have a new and improved method of surface mounting radio frequency components in a more effective manner.

Disclosure of Invention

Therefore, the principal object of the present invention is to provide a new and improved method of surface mounting radio frequency components, and a radio frequency component for use in such a method, to reduce

greatly the need for customizing the radio frequency components, to increase component density, and to simplify the board layout design requirements.

5 Briefly, the above and further objects of the present invention are realized by providing a new and improved method of surface mounting radio frequency components, and a radio frequency component for use therein, to facilitate greatly circuit board layout and to reduce or eliminate entirely the requirement for
10 customized radio frequency components. Such a new and novel method of surface mounting radio frequency components utilizes the circuit board in an efficient manner to enhance the highly desirable high density clustering of components.

15 The method of surface mounting radio frequency components includes using at least one radio frequency component having a pair of input/output contact points or areas at corners on the underside of the component, wherein each of the input/output contact points or areas
20 abuts the adjoining edges of the corners. The component is positioned relative to a pair of traces on a circuit board for enabling an electrical connection thereto in a range of angular dispositions. By using a single non-customized component, adjacent components can be
25 configured with a signal flow path of a range between about 0° (a chain configuration) and about 180° (a "U"-turn).

Brief Description of Drawings

30 The above mentioned and other objects and features of this invention and the manner of attaining them will become apparent, and the invention itself will be best understood by reference to the following description of the embodiment of the invention in conjunction with the accompanying drawings, wherein:

FIG. 1 is a partial diagrammatical view of a portion of a prior art radio frequency circuit, illustrating conventional surface mounting methods;

5 FIG. 2 is a partial diagrammatical view of a portion of another prior art radio frequency circuit, illustrating conventional surface mounting methods;

FIG. 3 is a partially diagrammatic, broken away elevational view of a radio frequency component, which is constructed according to the present invention;

10 FIG. 4 is an enlarged bottom view of the radio frequency component of FIG. 3;

FIG. 5 is a partial diagrammatical view of a radio frequency circuit, including a radio frequency component, which is surface mounted according to the method of the present invention to provide a signal flow path having a 180° turn;

20 FIG. 6 is a partial diagrammatical view of another radio frequency circuit utilizing the radio frequency component of FIG. 5, which is also surface mounted according to the method of the present invention to provide a signal flow path having a 90° turn;

25 FIG. 7 is a partial diagrammatical view of yet another radio frequency circuit, also utilizing the radio frequency component of FIG. 5, which is also surface mounted according to the method of the present invention to provide a signal flow path having a 0° turn (linear or chain configuration);

30 FIG. 8 is a partial diagrammatical view of a further radio frequency circuit, which is also surface mounted according to the method of the present invention to provide a 180° signal flow path turn;

35 FIG. 9 is a partial diagrammatical view of another radio frequency circuit, and another radio frequency component, which is also surface mounted according to the present invention; and

FIG. 10 is a partial diagrammatical view of another radio frequency circuit, which is also surface mounted according to the method of the present invention;

FIG. 11 is a partial diagrammatical view of yet
5 another radio frequency circuit, and yet another radio frequency component for use therein, which is also surface mounted according to the method of the present invention.
Best Mode for Carrying Out the Invention

Referring now to FIG. 1, there is shown a bottom
10 view of a portion of a prior art radio frequency circuit generally indicated at 10, which employs conventional surface mounting techniques according to a prior art method. The circuit 10 includes a conventional radio frequency component 11 having a generally rectangular
15 underside 12 and edges 14, 16, 18 and 20. Edges 14 and 20 intersect at a corner area generally indicated at 22 of the underside 12, and edges 16 and 18 intersect to form a corner area generally indicated at 24 of underside 12.

20 A pair of input/output contact members 30 and 32 are disposed at the opposite respective side edges 20 and 16 spaced from the respective corner areas 22 and 24 to enable the radio frequency component 11 to be connected electrically to the circuit board.

25 According to the prior art method of surface mounting the component 11, the radio frequency component 11 is positioned over the circuit board to align the input/output connection members 30 and 32 with a pair of traces 40 and 50, respectively. In order to reduce
30 interference introduced by the traces 40 and 50, the traces 40 and 50 include connection portion 42 and 52, respectively, which are connected to the input/output connection members 30 and 32 by conventional soldering techniques and which are substantially perpendicular to
35 the adjacent edges 20 and 16, respectively.

It is well known in the art that an improper arrangement of the traces carrying radio frequency signals can cause a loss of the signals. In this regard, traces having sharp turns, such as right angle turns without any mitering or other design considerations, are to be avoided since the adjoining traces can create unwanted perisitic effects in the form of electrical interference. The result of such interference is a signal loss.

To reduce signal losses caused by abrupt turns in the traces, all right angle turns in the course of the segmented trace 50 on a circuit board (not shown) have been eliminated by using angled trace members, such as trace members 54, 56, 58 and 60. In this regard, trace members 52 and 60 are spaced apart from one another, and are substantially parallel, but the intermediate portion of the trace 50 employs an irregular shape due to the segments 54, 56 and 58.

In order to connect trace members 52 and 60 without using a 90° bend, trace member 56 is positioned perpendicular to both trace members 52 and 60. Rather than intersecting trace members 52 and 60 at right angles, trace member 56 is connected to trace members 52 and 60 by angled trace members 54 and 58. In this regard, the angled trace members 54 and 58 form about 45° angles with the trace members 52 and 56, as well as trace members 56 and 60.

The angled trace members 54 and 58 form mitered corners 53 and 57 in the trace 50, thereby eliminating detrimental effects due to sharp turns in the trace. However, the resulting segmented trace 50 extending to an adjacent component (not shown) occupies an undesirably large amount of space on the circuit board (not shown) and thus the resulting component spacing is not very

dense. Also, the large segmented traces can produce an undesired loss in signal.

Referring now to FIG. 2, there is shown another prior art radio frequency circuit 200 which is surface mounted to a circuit board 201 according to a prior art method. The conventional surface mounting method uses a pair of conventional radio frequency components 210 and 280 for mounting on the circuit board 201. As both radio frequency components 210 and 280 are substantially similar to one another, only radio frequency component 210 will now be considered hereinafter in greater detail.

The radio frequency component 210 includes a generally rectangularly shaped underside surface 212 having edges 214, 216, 218 and 220. A pair of input/output connection members 230 and 232 are disposed at opposite edges 214 and 218. The input/output connection members 230 and 232 abut edges 214 and 218, respectively, and are located at about a midpoint thereof. The component 210 is similar to the prior art component 11 (FIG. 1) except that the input/output connection members 230 and 232 have been positioned directly opposite of one another at the end edges of the component. This U-shaped configuration enables components, such as components 210 and 280, to connect a pair of parallel linear chains of components in a 180° signal flow path configuration. In this regard, for example, depending on the polarity, a signal can enter the component 280 at trace 272, flow through the component 280, a segmented U-shaped trace 250, the component 220, and out the trace 242 to complete the 180° flow path turn.

The radio frequency component 210 is positioned relative to traces 240 and 250 to align the input/output connection members 232 and 230 therewith. The component 210 is then mounted to the traces 240 and 250 to connect

electrically the input/output connection members 232 and 230 thereto, wherein the traces 240 and 250 form a 90° angle relative to the opposite edges 218 and 214, respectively.

5 Similarly, the component 280 is positioned relative to the trace 250 and another trace 270 to position the input/output connection members 282 and 284 therewith. The component 280 is then mounted to the circuit board to connect electrically the traces 250 and 270 to the
10 input/output connection members 282 and 284. The traces 250 and 270 form a 90° angle with the opposite edges 286 and 288, respectively. As a result, the components 210 and 280 are mounted to the circuit board in a parallel manner, and are connected to one another by the trace
15 250.

As discussed previously, all right angles with special mitering or other design considerations in radio frequency traces are to be avoided to eliminate signal losses associated with the sharp turns. Thus, the prior
20 art method of surface mounting components 210 and 280 in parallel was accomplished by eliminating all right angled bends in the trace 250.

In order to eliminate all unwanted right angled bends, the segmented trace 250 was divided into trace
25 numbers 252, 254, 256, 258 and 260. Trace members 252 and 260 are attached to the input/output connection members 230 and 282, respectively, and are substantially parallel to one another. The trace member 256 is
30 positioned perpendicular to the trace members 252 and 260, and is connected thereto by trace members 254 and 258. By angling the trace members 254 and 258 at about a 45° angle from trace members 252, 256 and 260 to form mitered corners, the trace 250 is substantially U-shaped and permits the connection of the components 210 and 280
35 to one another without the use of a right angled turn.

While the use of mitered corners eliminated right angled bends and rounded turns in connecting the components 210 and 280 to one another with the trace 250, signal losses were still prevalent. The signal losses
5 resulted from the relatively long length of the segmented trace 250 and the per unit length resistance associated with the trace 250. Thus, by increasing the length of the trace 250 by using mitered turns to eliminate interference losses, losses due to resistance have
10 increased.

Furthermore, requiring mitered turns in the segmented trace 250 causes the components 210 and 280 to be spaced further apart from one another in an undesirable manner. This is necessitated by the need to
15 include the angled trace members 254 and 258 which extend in both the x and y coordinates of the plane defined by the circuit board 201. As a result of the components 210 and 280 being spaced further apart, the component density on the circuit board 201 is reduced, thereby reducing the
20 efficient use of available circuit board surface area.

From the foregoing, it is apparent that the prior art components 11, 210 and 280, and the methods of surface mounting them, are restrictive and inefficient. In this regard, all traces connected to the respective
25 input/output connection members must be normal to edges adjacent to the input/output connection members. To deviate from this introduces interference caused by a trace forming an acute angle with the adjacent edge. In addition, the lengths of traces connecting parallel
30 components are increased, thereby increasing the signal losses. Furthermore, the spacing between components is increased. Increasing the space between components requires more surface area of the circuit board to surface mount the components, reducing the efficient
35 utilization of available circuit board surface area.

Referring now to the drawings, and more particularly to FIGS. 3 and 4 thereof, there is shown a radio frequency component 300 which is constructed according to the present invention, and which is surface mounted according to a method of the present invention. The component 300 includes a rectangular carrier portion 310 having an upper surface 311 and an electrically non-conductive underside surface 312. A housing 313 is attached to the upper surface 311 and encloses an electronic device 370 within. It will be understood by one skilled in the art that the radio frequency device 370 could contain a filter, an amplifier, or an oscillator, or any other radio frequency device.

Considering now the carrier member 310 in greater detail with respect to FIG. 4, the carrier member is defined by the edges 314, 316, 318 and 320. Adjoining edges 314 and 320 form a corner portion 322, while adjoining edges 318 and 320 form a corner portion 324. Input/output connection members 330 and 332 are disposed in the corners 322 and 324, respectively, to facilitate the electrical connection of the radio frequency device 370. In this regard, the radio frequency device 370 is connected between the input/output connection members 330 and 332 by a means not shown to permit the device 370 to be activated.

Input/output connection member 330 abuts the edges 314 and 320 and the input/output connection member 332 abuts the edges 318 and 320, wherein the edge 320 is common to both of the input/output connecting members 330 and 332. Also disposed on the underside surface 312, and spaced apart from the input/output connection members 330 and 332 by a pair of gaps 331 and 333, is a base portion 340. The input/output connection members 330 and 332 and the base member 340 are electrically conductive to enable the component 300 to function in a radio frequency

circuit (not shown). However, the input/output connection members 330 and 332 are electrically isolated from the base portion 340 on the underside surface 312 due to gaps 331 and 333.

5 The edges 314, 318 and 320 include semi-circular notches 354, 356 and 358, as well as quarter-radius notches 350 and 352. All of the notches 350, 352, 354, 356 and 358 are half-plated to facilitate post assembly inspection.

10 Referring now to FIGS. 5-8, a number of methods of surface mounting radio frequency components, such as the radio frequency component 300 illustrated in FIGS. 3 and 4, are illustrated.

15 Referring now to FIG. 8, there is shown a radio frequency circuit 800 which is surface mounted according to the present invention. The circuit 800 utilizes three substantially similar components 300, 810 and 850, in connection with a circuit board 801 having traces 846, 856, 858 and 860 thereon.

20 Using the component 300 of FIGS. 3 and 4, the component 300 is positioned relative to the traces 856 and 858. The input/output connection members 330 and 332 are mounted to the traces 856 and 858, respectively, to complete the electrical connection therebetween. A
25 reference line 804 is indicative of the central axis of the component 300.

30 Another component 810, having a reference line 802 indicative of the central axis of the component 810, is rotated about an angle G relative to the reference line 804 to orient the component 810 perpendicular to the component 300, wherein the angle G is about 90°. The input/output connection members 830 and 832 are aligned with traces 846 and 856, respectively. The component 810 is mounted to the traces 846 and 856 to electrically
35 connect the input/output connection members 830 and 832

thereto. In this mounted position, the traces 558 and 556 are rotated from a common edge 816, which abuts both the input/output connection members 830 and 832, by the angles K and H, wherein the angles K and H are about 90°.

5 Similarly, the component 850 includes input/output connection members 870 and 872 and a common edge 856 which abuts both of the input/output connection members 870 and 872. The component 850 is positioned relative to traces 858 and 860, wherein the component 850 is
10 substantially parallel to the component 810. The input/output connection members 870 and 872 are electrically connected to the traces 860 and 858, thereby completing a "U"-turn consisting of the three similar components 300, 810 and 850.

15 It will be understood by one skilled in the art that the components 300, 810 and 850 occupy approximately the same amount of circuit board space on circuit board 801 that was occupied by the prior art components 210 and 280, connected by the trace 250 on circuit board 201 of
20 FIG. 2. Thus, circuit 800 enables three components to be used in the amount of space where previously only two components could be used.

 By surface mounting the three components 300, 810 and 850 in the same amount of space previously used by
25 only two components, the efficient use of the circuit board 801 is significantly increased. Furthermore, by replacing the trace 250 (FIG. 2) with a component, component 300, the losses resulting from the resistance of the trace 250 are eliminated. Therefore, the method
30 of surface mounting according to the present invention permits the mounting of a larger number of components on a fixed amount of surface area, thereby enabling a larger component density on a circuit board, while reducing the signal losses due to trace resistance characteristics.

As described previously, the input/output connection members 330 and 333 (FIGS. 3-8) are disposed at corner surfaces 332 and 334. As a result of the input/output connection members 330 and 332 being located on the corner surfaces 332 and 324, a trace can be connected to the input/output connection members 330 and 332 at a number of angles not possible with the prior art component configuration. For example, the trace may be connected to the input/output connection member 330 at an angle of between about 90° and 180° from the common edge 320 without the trace forming an acute angle with either edge 320 or edge 314.

Considering now the method of surface mounting the radio frequency circuit 500 (FIG. 5), the circuit 500 is surface mounted to a circuit board (not shown) utilizing the radio frequency component 300. The circuit board includes a pair of traces 540 and 550 for connecting electrically the component 300 to other components (not shown).

In operation, the component 300 is positioned relative to the traces 540 and 550 to enable the input/output connection members 330 and 332 to be aligned with the traces 540 and 550. Once aligned, the component 300 is mounted to the circuit board to connect the input/output connection members 330 and 332 to the traces 540 and 550, respectively. The traces 540 and 550 are connected to the input/output connection members 330 and 332 at angles A and B, relative to the common edge 320, wherein the angles A and B are about 90°.

By connecting the traces 540 and 550 at 90° angles to the common edge 320, the component 300 facilitates a 180° change in direction of the flow of a radio frequency signal. For example, the traces 540 and 550 could be connected to a pair of parallel chains of radio frequency components (not shown). The signal transmitted through

one of the chains enters the component 300 through one of the traces 540 or 550. The signal passes through the component 300 and is redirected 180° before being transmitted to the other chain of components through the other trace 550 or 540.

Considering now the method of surface mounting the radio frequency circuit 600 (FIG. 6), the circuit 600 utilizes the component 300 in a variation of the circuit 500. In this regard, the method of surface mounting the component 300 requires the component 300 to be positioned relative to traces 640 and 650 of a circuit board (not shown), wherein the input/output connection members 330 and 332 are aligned therewith. The input/output connection members 330 and 332 are mounted to the circuit board to connect electrically the input/output connection members 330 and 332 to the traces 640 and 650, respectively. The traces 650 and 640 are connected to the input/output connection members 330 and 332 at angles C and D relative to the common edge 320, respectively, wherein the angles C and D are about 135°.

The connection of traces 650 and 640 at 135° angles to the common edge 320 enables a pair of chains of components (not shown) to be connected to one another in a manner similar to the circuit 500 of FIG. 1. However, in circuit 600, the component 300 facilitates a 90° change in direction of the flow of the radio frequency signal. Thus, the signal transmitted through one of the traces 650 or 640 to the component 300 flows therethrough, and the signal is redirected 90° before being transmitted to the other chain of components through the other trace 640 or 650.

Considering now the method of surface mounting the circuit 700 (FIG. 7), the circuit 700 is produced using the component 300 in conjunction with a circuit board (not shown) having the traces 750 and 740 thereon. The

component 300 is positioned relative to the traces 740 and 750 to align the input/output connection members 330 and 332 therewith. Once positioned, the input/output connection members 330 and 332 are connected to the
5 traces 740 and 750, respectively, to complete the mounting of the component 300. The traces 750 and 740 are connected to the input/output connection members 330 and 332 at angles E and F relative to the common edge 320, respectively, wherein the angles E and F are about
10 180°.

The connection of traces 750 and 740 at 180° angles to the common edge 320 enables a pair of chains of radio frequency components (not shown) to be connected to one another wherein the flow of the radio frequency signal is
15 not redirected. Instead, the chains of components are co-linear with the component 300. The signal flows from one chain to the component 300, and on to the other chain without changing direction. Thus, the component 300 facilitates a 0° change in direction of signal flow.

20 It will be understood by one skilled in the art that the angles C and D are only representative of an infinite number of possible angles which can be used, and which are in the range bounded by the angles A and B at one end and the angles E and F at the other end. Because of the
25 wide variety of angles permissible, the radio frequency components of the present invention can be utilized in a large variety of radio frequency circuits where the angles between the common edge and the traces vary. Due to the flexibility provided by the method of the present
30 invention, and the inventive radio frequency component used therein, the component 300 facilitates the connection of adjacent components (not shown) in arrangements wherein the angle between the adjacent components can be configured to vary between about 0°
35 (FIG. 7) and about 180° (FIG. 5). Thus, the

configuration of a component, such as component 300, may be utilized in a large number of circuits. In this way, a designer can rely on a single component's configuration to satisfy a large number of circuit design requirements.

5 The flexibility available is increased by using components, such as component 300, in chains to form the desired circuit. In this way, the flexibility provided by each one of the components provides the designer with an unlimited amount of design options to optimize the use
10 of available circuit board surface area.

Furthermore, the use of a common component configuration for completing a circuit reduces the cost of surface mounting the components. When using the common component, the component can be specified as an
15 off-the-shelf item, reducing the cost of the method of the present invention.

The previously described components 300, 810 and 850, which are all constructed according to the present invention, provide a designer with the flexibility to
20 create a large number of radio frequency circuits. In order to provide additional flexibility, a component 910 (FIG. 9) is contemplated. The component 910 is substantially similar to the components 300, 810 and 850, except that the input/output connection members 930 and
25 934 are positioned in opposite corner locations 922 and 926. The corner surfaces 922 and 926 are formed by the adjoining edges 914 and 915, and 912 and 918, respectively. In this regard, the edges 914 and 918 are about parallel to one another.

30 Considering now the method of surface mounting circuit 900, the component 910 is positioned relative to a pair of traces 950 and 960. The component 910 then is mounted to the traces 950 and 960. In this mounted position, the input/output connection members 930 and 934
35 are electrically connected to the traces 950 and 960 and

the traces 950 and 960 are rotated from the opposite edges 914 and 918 by angles R and P, respectively, wherein R and P are about 90°.

The angles R and P can be adjusted to be between
5 about 90° and about 180°. In this way, the traces always form an acute angle with any of the edges 912, 914, 916 or 918. Thus, the losses associated with a trace making an acute angle with an edge are eliminated.

Referring now to FIG. 10, there is shown another
10 radio frequency circuit 1000. The circuit 1000 includes an antenna device 1010 which is connected simultaneously to the radio frequency components 300 and 850 in a diplexing or multiplexing configuration.

The component 300 is positioned relative to a pair
15 of traces 1050 and 1060. Similarly, the component 850 is positioned relative to a pair of traces 1070 and 1080. The component 850 is rotated about 180° from the orientation of the component 300, wherein the input/output connection members 870 and 872 are spaced
20 apart from the input/output connection members 332 and 330, respectively.

The components 300 and 850 are mounted to the traces 1050, 1060, 1070 and 1080, connecting the input output connection members 330, 332, 870 and 872 thereto. The
25 traces 1060 and 1070 are rotated from the common edges 320 and 856 by angles M and N. The angles M and N are about 135°. It will be understood by one skilled in the art that the angles M and N may vary between about 90° and about 150°. The traces 1060 and 1070 terminate at a
30 trace 1020, which is in turn connected to the antenna device 1010 to transmit a radio frequency signal received by the antenna device 1010 to the components 300 and 850.

Referring now to FIG. 11, there is shown another embodiment of a radio frequency circuit 1100, which is
35 also surface mounted according to the present invention.

The circuit 1100 includes a radio frequency component 1110 which includes three input/output connection members 1130, 1132 and 1134, located on three corner surfaces 1122, 1124 and 1126 on the undersurface 1112. The
5 input/output connection members 1130 and 1132 abut in edge 1116 while the input/output connection members 1132 and 1134 abut an edge 1118.

The component 1110 is positioned relative to three traces 1150, 1160, and 1170. The input/output connection
10 members 1130, 1132 and 1134 are connected to the traces 1150, 1160 and 1170. An antenna device 1180 is connected to a trace 1182 and the trace 1182 is electrically connected to the trace 1150 to provide a radio frequency signal to the component 1110.

15 From the foregoing, one skilled in the art will understand that a large variety of radio frequency circuits can be constructed using a number of similarly configured radio frequency components. Other radio frequency components having slightly different
20 configurations can be used to accommodate a particular need, such as the input of a remote signal. In this way, the basic building blocks available to a designer of radio frequency circuits are substantially similar, thereby reducing the design time of each radio frequency
25 circuit. Furthermore, the variety of radio frequency components for any number of possible circuit design is substantially reduced enabling the components to be more readily available.

While particular embodiments of the present
30 invention have been disclosed, it is to be understood that various different modifications are possible and are contemplated within the true spirit and scope of the appended claims. There is no intention, therefore, of limitations to the exact abstract or disclosure herein
35 presented.

What is claimed is:

1. A method of surface mounting radio frequency components to a circuit board, comprising:

using at least one rectangular surface mounting
5 component having a pair of input/output connection members disposed at a pair of adjacent corner surfaces on the underside of said component, each of said input/output connection members abuts adjoining edges of said corner surfaces, wherein said input/output
10 connection members abut a common edge;

using a circuit board having a plurality of traces disposed thereon;

positioning said component relative to a first trace and a second trace to align said input/output
15 connection members with said first trace and said second trace; and

mounting said component to said circuit board, wherein said input/output connection members are connected electrically to said first trace and said
20 second trace, each one of said traces intersects said common edge at an angle between about 90° and about 180°.

2. A method according to claim 1, further comprising:

using another of said surface mounting
25 components;

rotating said another surface mounting component about 90° from the orientation of said surface mounting component;

positioning said another surface mounting
30 component relative to said second trace and a third trace, wherein said second trace is substantially straight; and

mounting said another surface mounting component to said circuit board, wherein said
35 input/output connection members of said another surface

mounting component are connected electrically to said second trace and said third trace, said second trace and said third trace intersecting said common edge of said another surface mounting component at an angle between
5 about 90° and about 180°.

3. A method according to claim 1, further comprising:

using a second surface mounting component;
rotating said second surface mounting component
10 between about 0° and about 180° from the orientation of said surface mounting component;
positioning said second surface mounting component relative to a third trace and a fourth trace to align said input/output connection members of said second
15 surface mounting component with said third trace and said fourth trace;

mounting said second surface mounting component to said circuit board, wherein said input/output connection members of said second surface mounting
20 component are connected electrically to said third trace and said fourth trace, said third trace and said fourth trace each intersecting said common edge of said second surface mounting component at an angle of between about 90° and about 180°; and

25 connecting electrically said second trace and said third trace without using mitered turns.

4. A method according to claim 3, further comprising:

using a third surface mounting component;
30 rotating said third surface mounting component about 90° from the orientation of said surface mounting component;

positioning said third surface mounting component relative to said second trace and said third

trace, wherein said second trace and said third trace are substantially straight; and

mounting said third surface mounting component to said circuit board, wherein said input/output
5 connection members of said third surface mounting component are connected electrically to said second trace and said third trace, said second trace and said third trace each intersecting said common edge of said third surface mounting component at an angle of between about
10 90° and about 180°.

5. A method of surface mounting radio frequency components to a circuit board, comprising:

using at least one rectangular surface mounting component having a first input/output connection member,
15 a second input/output connection member and a third input/output connection member disposed at three corner surfaces on the underside of said component, each of said input/output connection members abuts adjoining edges of said corner surfaces, wherein said first and said second
20 input/output connection members abut a common edge, and said second and said third input/output connection members abut another common edge;

using a circuit board having a first, a second and a third trace disposed thereon;

25 positioning said component relative to said first, said second and said third trace, wherein said first input/output connection member is aligned with said first trace, said second input/output connection member is aligned with said second trace and said third
30 input/output connection member is aligned with said third trace; and

mounting said component to said circuit board, wherein said first, said second and said third input/output connection members are connected
35 electrically to said first, said second and said third

traces, respectively, said first trace and said second trace each intersecting said common edge at an angle of between about 90° and about 180°.

6. A method according to claim 5, further comprising:

using an antenna means;

connecting electrically said antenna means to said third trace to provide a signal to said component.

7. A method according to claim 3, further comprising:

rotating said second surface mounting component about 180° from the orientation of said surface mounting component;

positioning said second surface mounting component relative to a third trace and a fourth trace to align said input/output connection members of said second surface mounting component with said third trace and said fourth trace;

mounting said second surface mounting component to said circuit board, wherein said input/output connection members of said second surface mounting component are connected electrically to said third trace and said fourth trace, said third trace and said fourth trace each intersecting said common edge of said second surface mounting component at an angle of between about 90° and about 180°;

connecting electrically said second trace to said third trace, wherein said second and said third trace are substantially straight; and

connecting an antenna means at about the intersection of said second trace and said third trace to provide a signal to said component and said second component.

8. A radio frequency component for facilitating the mounting thereof on a circuit board, comprising:

at least two traces disposed on said circuit board;

a rectangular carrier member including an underside having a pair of input/output connection members disposed at adjacent corner surfaces of said underside for enabling the electrical connection of said carrier member to said traces, each of said input/output connection members abuts adjoining edges of said corner surfaces, wherein said input/output connection members abut a common edge; and

wherein each one of said traces intersects said common edge at an angle of between about 90° and about 180°.

9. A radio frequency component according to claim 8, wherein each of said traces intersects said common edge at an angle of between about 105° and about 165°.

10. A radio frequency component according to claim 8, wherein each of said traces intersects said common edge at an angle of between about 120° and about 150°.

11. A radio frequency component according to claim 8, wherein each of said traces intersects said common edge at an angle of about 135°.

12. A radio frequency component according to claim 8, further comprising:

another input/output connection member disposed on another corner surface for enabling said carrier member to be connected electrically to a third trace, wherein said another input/output connection member abuts adjoining edges of said another corner surface.

13. A radio frequency component for facilitating the mounting thereof on to a system board, comprising:

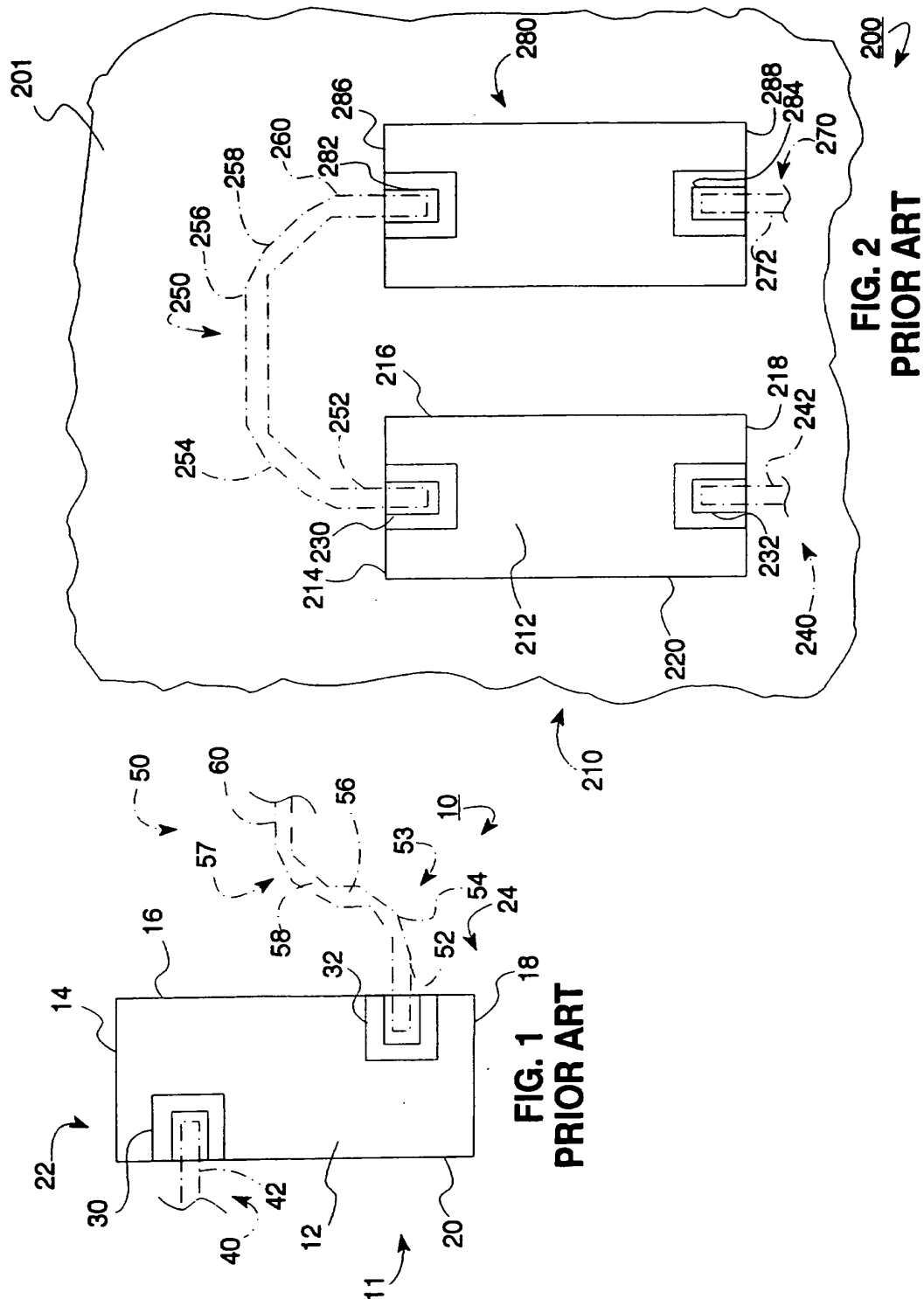
at least two traces disposed on said circuit board;

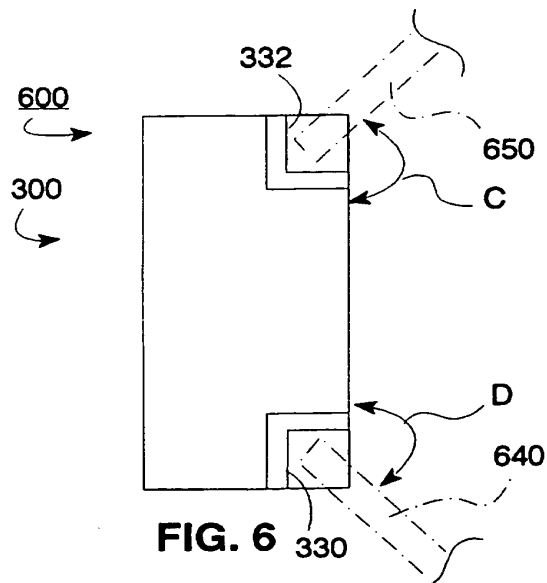
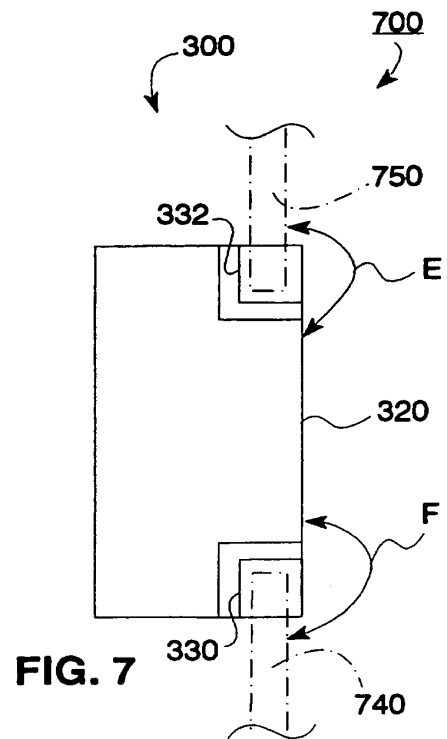
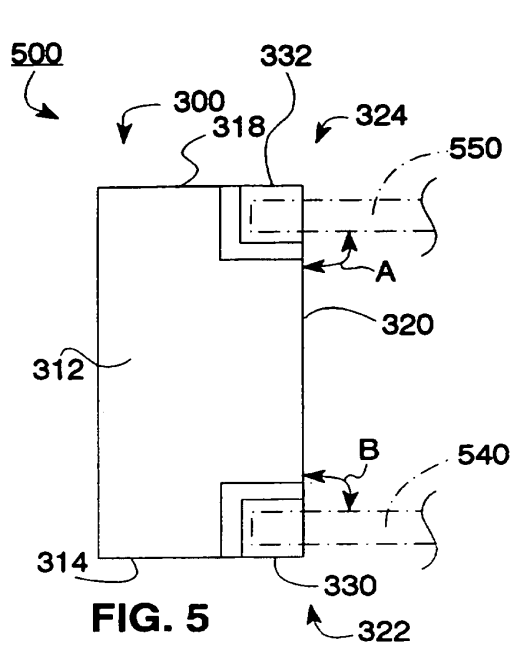
a rectangular carrier member including an underside having a pair of input/output connection

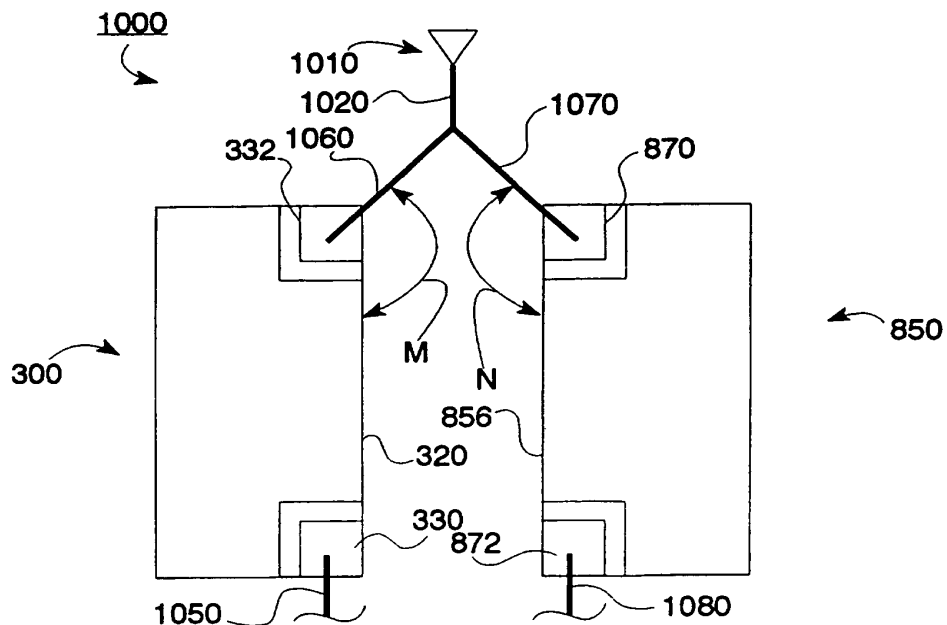
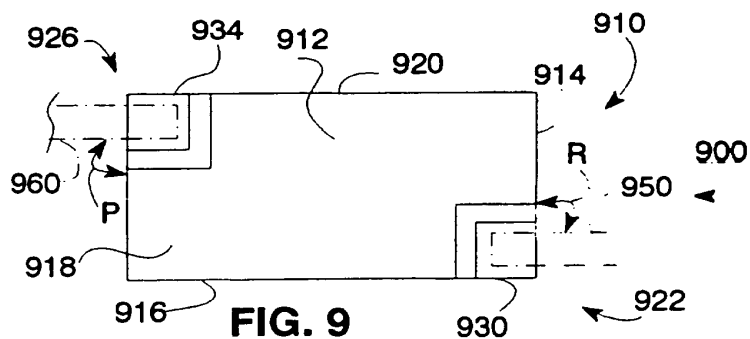
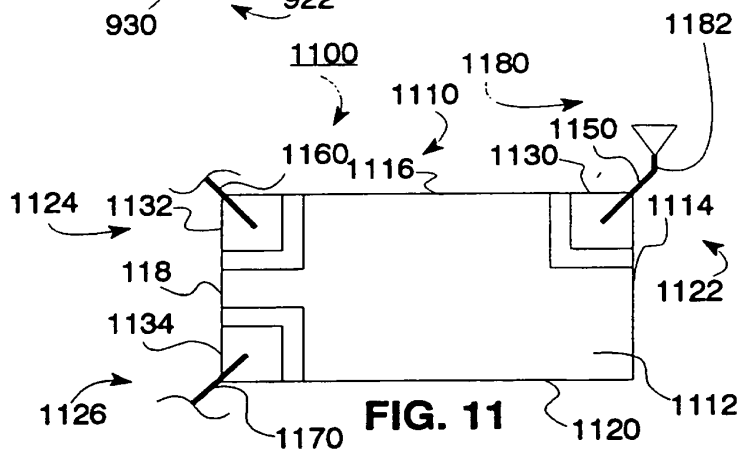
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members disposed at opposite corner surfaces of said underside for enabling the electrical connection of said carrier member to said traces, each of said input/output connection members abuts adjoining edges of said corner
5 surfaces, wherein said input/output connection members abut oppositely disposed edges; and

wherein each one of said traces intersects said opposite edges at an angle of between about 90° and about 180°.





**FIG. 10****FIG. 9****FIG. 11**

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/10769

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) H05K 1/00

US CL :174/260

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 174/260,250,261; 361/760; 428/901

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 3,964,087 (MALLON) 15 JUNE 1976 SEE FIGURE 1	1-13
A	US, A, 4,796,079 (HETTIGER) 03 JANUARY 1989 SEE FIGURE 2	1-13
A	US, A, 5,418,329 (KATOH ET AL.) 23 MAY 1995 SEE FIGURE 4	1-13

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:

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O document referring to an oral disclosure, use, exhibition or other means

P document published prior to the international filing date but later than the priority date claimed

T

later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X

document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

A

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Date of the actual completion of the international search

04 JANUARY 1996

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Facsimile No. (703) 305-3230

Authorized officer

LAURA THOMAS *Laura Thomas*

Telephone No. (703) 308-2258

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(71) Applicant: **International Business Machines Corporation**
Old Orchard Road
Armonk, N.Y. 10504(US)

(72) Inventor: **Jackson, Kennethh Paul**
67 Garfield Avenue
Danbury, Connecticut 06810(US)
Inventor: **Raver, Norman**
2281 Sultana Drive
Yorktown Heights, New York 10598(US)

(74) Representative: **Klocke, Peter, Dipl.-Ing.**
IBM Deutschland GmbH Patentwesen und
Urheberrecht Schönalcher Strasse 220
W-7030 Böblingen(DE)

(54) **Wire bond connection system.**

(57) Electrical circuit including a first array (22) and a second array (16) of electrical components mounted on a circuit board having an electrically conductive cladding (20), comprising a system for interconnecting the components of the first array to the components of the second array with parallel signal channels. In each of the channels, there is one electrically conductive strip (48) formed within the cladding (20) and providing for a path of current from a component of the second array to a component of the first array. A second conductive path is provided for conducting current from the first array to the

second array. The conductive strip forms therewith a portion of a loop which generates a magnetic field in the presence of currents flowing through the two paths. There is magnetic coupling between the paths of one channel to the paths of the other channel, the magnetic coupling provided by the wire loops having a positive coefficient of mutual inductance while the coupling from loops lying in a plane parallel to the padding is characterized by a mutual inductance of negative coupling coefficient. The positive and the negative mutual inductances tend to cancel for reduction of crosstalk among the channels.

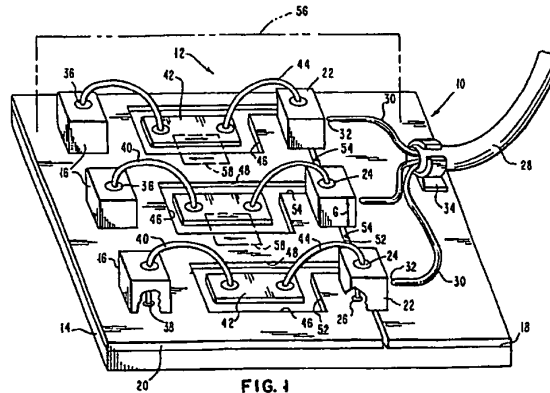


FIG. 1

Xerox Copy Centre

EP 0 436 074 A1

WIRE BOND CONNECTION SYSTEM

This invention relates to the use of wire bond connections among a set of electrical components mounted on a metal clad circuit board and, more particularly, to a system to reduce mutual coupling between adjacent wire connections for substantial elimination of crosstalk between parallel electric circuits.

Various forms of construction are employed in building electrical circuits. The form of construction varies in accordance with the types of components which are to be interconnected. By way of example, one common form of construction employs the interconnection of numerous circuit modules upon a circuit board which serves to support the circuit modules. Frequently, the circuit board is clad, at least on a top surface thereof facing the modules, with an electrically-conductive sheet, such as a metal sheet. Portions of the sheet may be cut away to form constructive strips which interconnect various terminals of the circuit modules. In the case of certain modules, manufacture of the circuit is facilitated by the use of relatively short wire segments which are spaced apart from the circuit board, and make direct connection among various terminals of the circuit modules.

A situation of particular interest employing the foregoing construction with the external wire segments is found in optical communications wherein solid-state lasers are employed as transmitting elements for generating short-duration light pulses which are radiated from individual ones of the lasers into corresponding optical fibers of a set of optical fibers constituting an optical transmission line. By way of example, a solid-state laser may be constructed in the form of a diode of gallium-aluminum-arsenide which generates a pulse of light upon excitation of the diode with a suitable pulse of current.

An electro-optical transmitter employing a set of laser diodes may be constructed by use of a circuit board which supports laser driver circuits and the laser diodes, the latter being excited by the driver circuits. The driver circuits are formed as individual modules. Also, each of the laser diodes is formed as an individual module including terminals for receipt of the electrical current, and also having a light-output port through which light is directed to an end of an optical fiber. Due to the physical shapes of the modules, it is the present manufacturing practice to connect some of the terminals of the modules by the metallic sheet or cladding on a circuit board, while other ones of the terminals are interconnected by segments of electrically-conductive wires.

In a typical arrangement of the electro-optical

transmitter, the modules are arranged in a set of parallel channels wherein each channel has a driver module, the laser diode, and an optical fiber. The wire segments which interconnect the components of the respective channels are disposed parallel to each other in an array of wire segments.

A problem arises in that the wire segments are sufficiently close to each other to introduce a significant amount of mutual magnetic coupling of electric signals conducted by the wire segments in the respective signal channels. This results in crosstalk or coupling of signals between the channels. The reliability of the electro-optical communication is reduced because the crosstalk acts as a source of noise which may introduce error in the communication. It is noted that in the typical electro-optical communication system, pulse modulation of an optical carrier is employed. Pulse modulation rates as high as one GHz (gigahertz) are available at the present time. At such high pulse frequencies, wire segments having lengths of approximately one millimeter or less can have strong magnetic coupling for crosstalk between the wire segments.

By way of example in the construction of electric circuits with printed circuit boards, Yamazaki et al, U. S. Pat. 4,758,805 discloses in Figs. 7 and 19 connections in the form of partial loops from pins to conductive strips on a circuit board. Similar construction is shown in Figs. 2 and 8 of Saburi et al, U. S. Pat. 4,782,310.

The aforementioned problem is overcome and other advantages are provided by a system for interconnecting components on a circuit board as claimed wherein connections are made both by conductive strips on a surface of the board and by wire segments spaced apart from the circuit board. In accordance with the invention, the system provides for a modification of connections by wire segments by serially connecting each wire segment with a configuration of strip conductors which provides for a mutual magnetic coupling among adjacent signal channels which is of the opposite sense to a mutual coupling among the wire segments. By the introduction of both positive and negative coefficients of mutual inductance, there is significant cancellation of the crosstalk. While it is possible, theoretically, to completely cancel the net mutual coupling and the crosstalk, as a practical matter in the construction of the circuit of the plural channels of an electro-optical transmitter, it is anticipated that there will be some variation in the configuration of the various partial wire segments such that the opposed mutual coupling formed within the configuration of conductive strips cannot completely balance and compensate for the mutual

coupling among the wire segments. Thus, the inter-connection system of the invention can accomplish significant cancellation of the mutual coupling and the crosstalk.

The methodology involved in constructing the compensating mutual coupling can be explained as follows. An array of wire segments arranged parallel to each other, with each wire segment being part of an electro-optical signal transmission channel, can be viewed as an array of loops or partial loops disposed in planes parallel to each other. The planes are perpendicular to the metal-clad surface of the circuit board. This arrangement of the loops is similar to the coaxial arrangement of the loops of wire in a solenoid wherein a magnetic field has lines of flux which pass through and link equally the respective loops of wire in the solenoid. As is well known, in such a configuration of loops, the coefficients of inductance and mutual coupling are both positive. However, there is an alternative configuration which can be viewed by considering the case of two loops of the foregoing solenoid. By displacing one of the loops relative to the other loop so that the two loops are arranged side by side in a common plane, and wherein the directions of positive current flow (clockwise or counterclockwise) are retained the same in both loops, it is apparent that a magnetic field induced in a first of the loops must curve around in a circular path to intercept the second loop. Thus, the magnetic field passes through the second loop in the reverse direction from the previous case. This results in a negative mutual inductance.

The development of the desired compensating mutual inductance is accomplished in a preferred embodiment of the invention by etching electrically conductive paths in the metallic sheet which serves as a cladding of the circuit board. The etching provides a border circumscribing each pad and insulating the pad from the rest of the cladding. In the array of parallel signal channels, the pads are arranged side-by-side, each pad surrounded by its border, and the borders of the successive pads are spaced apart by electrically conductive strips. Each electrically conductive strip serves as a path for the transmission of current between circuit modules of the respective signal channels.

Each wire segment, instead of extending the full distance from one circuit module to the next circuit module in the signal channel, extends only as far as an end of the conductive pad in the signal channel. Thereupon, the current in the wire segment travels along the pad for a predetermined distance after which the current is fed from the pad to the next component. The connection from the pad to the next component may be accomplished by either a further loop or partial loop of wire segment, or may be accomplished by a strip con-

ductor extending from the pad to the next circuit module. Current flowing through a wire loop in a signal channel flows about the loop in a plane perpendicular to the cladded surface of the circuit board. However, current, flowing forward to the next component by way of the pad, flows within the plane of the cladding. Current, returning from the foregoing component by way of the conductive strip between adjacent borders, also flows within the plane of the cladding. The forward and returning currents are coplanar in the vicinity of the pad, and produce effectively a loop of current disposed parallel to the cladded surface of the circuit board.

The foregoing construction of the two loops in each signal channel provides for one loop which is perpendicular to the cladded surface and a second loop which is parallel to the cladded surface of the circuit board. In view of the fact that the channels are arranged parallel to each other, the loops which are disposed perpendicularly to the cladded surface can be described electrically in terms of positive mutual magnetic coupling, while the loops of the successive channels which lie parallel to the cladded surface can be characterized electrically as having a negative mutual magnetic coupling. The loops lying parallel to the cladded surface may be elongated and may be broadened to provide a geometric configuration having a desired amount of mutual coupling for canceling the mutual coupling of the wire-segment groups.

In particular, the mutual coupling increases with increasing length of a segment of the border lying between the conductive strip and the pad at each channel, and also increases with increasing width of the border segment. This is in accordance with the general theory of mutual coupling wherein the coupling is proportional to the amount of magnetic flux linking each loop. Thereby, by using a predetermined length for each of the wire segments in constructing the wire loops perpendicular to the cladded surface, the dimensions of the pads, the dimensions of the insulating borders surrounding the respective pads, and the dimensions of the conductive strips separating the adjacent borders of the respective pads can be selected to provide the requisite amount of mutual coupling for negating the mutual coupling among the wire loops. Thereby, the invention accomplishes its goal of essentially canceling the unwanted mutual coupling and the crosstalk associated therewith between the adjacent signal channels.

The aforementioned aspects and other features of the invention are explained in the following description of preferred embodiments, taken in connection with the accompanying drawing wherein:

Fig. 1

is a simplified perspective view, partially stylized, of an electro-optical communication sys-

tem with electronic component modules supported on a circuit board, and wherein electrical connections are made both by wire loops and strip conductors in accordance with the invention;

Fig. 2

is a plan view of an enlarged fragmentary portion of Fig. 1 with important dimensions of the pad structure being identified therein;

Figs. 3A and 3B

together demonstrate magnetic coupling with positive and negative mutual inductance among a pair of electrically conductive wire loops disposed in different configurations of position relative to each other; and

Fig. 4

shows in plan view, partially stylized, an alternative embodiment to the structure of Fig. 2.

With reference to Figs. 1-2, there is shown circuitry 10 in the transmitting portion of an electro-optical communication system 12, the circuitry being built upon a circuit board 14, and including circuit modules 16 supported on a top surface 18 of the board 14. The term "top" is used by way of convenience in describing the circuit board 14 as shown in Fig. 1, it being understood that, in practice, the board 14 may be oriented horizontally, vertically, or in some other orientation. The board 14 is formed of electrically-insulating, dielectric material, such as fibrous glass embedded in epoxy by way of example, or as a silicon substrate, by way of further example, and includes an electrically conductive cladding 20 covering at least a portion of the top surface 18. Typically, the cladding 20 is formed of a thin metal sheet such as a copper sheet.

Also included within the circuitry 10 is a set of solid-state lasers 22, each laser 22 being formed typically, of a diode of gallium-aluminum-arsenide. Each of the lasers 22 is constructed in modular form, and may be supported by the board 14 or a separate support (not shown) coplanar with the board 14. Each laser 22 has two terminals, namely, a first terminal 24 located at a top portion of the laser 22 and a second terminal 26 located at a bottom portion of the laser 22. Electric current is to be applied via the terminals 24 and 26 to the laser 22 for activating the laser to emit radiation, which may be referred to as light, even though such radiation may be in the infrared region of the electromagnetic spectrum a typical wavelength being 840 nanometers.

The communication system 12 includes an optical cable 28 having individual fibers 30 which are optically coupled to respective ones of the lasers 22. Each of the lasers 22 has an output port (not shown in the figures) though the light is emitted to impinge upon an end surface 32 of a respective

optical fiber 30 located in front of the laser output port. The fibers 30 and the cable 28 are held in position by a suitable support 34 which may stand upon the board 14 or upon some other structure (not shown) adjacent to the board 14.

Each of the circuit modules 16 may be provided with a set (not shown) of numerous contacts for making electrical connection with other circuit elements including power supplies and signal generators which have been deleted in the drawing to facilitate presentation of the inventive features of the circuitry 10. Electrical connection with such contacts may be made by electrical strip conductors formed within the cladding 20 in accordance with manufacturing procedures well known in the construction of printed-circuit boards. Of particular interest in the practice of the invention is the fact that each circuit module 16 has a pair of output terminals, namely, a first terminal 36 located on a top of the module 16 and a second terminal 38 located on a bottom of the module 16, for outputting electric drive current to activate the laser 22.

In accordance with the invention, each of the circuit modules 16 applies current to a single one of the lasers 22. Connection of the terminals 36 and 38 of a module 16 with the terminals 24 and 26, respectively, of the corresponding laser 22 is made as follows to provide a path of current flow between the module 16 and the laser 22. Current flows along this path from the first terminal 36 of the module 16 to the first terminal 24 of the laser 22, and returns to the module 16 from the second terminal 26 of the laser 22 to the second terminal 38 of the module 16. Connection of the first terminal 36 to the first terminal 24 is made by a serial connection of an output lead 40, an electrically conducting pad 42, and an input lead 44.

The pad 42 is formed from material of the cladding 20 and is constructed as an island surrounded by an electrically-insulating border 46 which separates the pad 42 from the remainder of the cladding 20. The border 46 is formed by etching away the metallic material of the cladding 20, and may be left as an empty trough (as portrayed in the drawing), or may be filled with electrically-insulating potting material such as epoxy. Connection between each of the modules 16 and its corresponding laser 22 is made in the same fashion, there being a pad 42 disposed between each of the modules 16 and its corresponding laser 22.

Thus, it is shown in Figs. 1-2, the pads 42 are arranged side-by-side in an array, with each pad 42 being surrounded by its border 46. The border 46 of one of the pads 42 is separated by an electrically conductive strip 48 from the border 46 of the next pad 42. The conductive strip 48 which serves as a return path for electrical current and connects between the second terminal 26 of a

laser 22 to the second terminal 38 of the corresponding module 16. The return current path provided by a strip 48 is located to the right side of the pad 42 so as to provide the identical configuration of interconnection structure between each of the modules 16 and their respective lasers 22. Each module 16 with its laser 22 and the interconnecting structure may be regarded as a signal channel 50. If desired, the return current paths provided by the strips 48 could be placed to the left side of each of the pads 42 (not shown); however, it is important in the practice of the invention that the return current path provided by the strip 48 be on the same side of the pad 42 in each of the signal channels 50.

As shown in Fig. 1, a portion of the module 16 has been cut away to show connection of the second terminal 38 with the cladding 20 and the strip 48 formed from the cladding 20. The output lead 40 of the module 16 extends from the first terminal 36 of the module 16 to a first end portion, to be referred to as the front, of the pad 42. The input lead 44 extends from a second end portion, to be referred to as the back, of the pad 42 to the first terminal 24 of the laser 22. A portion of the laser 22 is cut away to show the second terminal 26 and its connection to an enlarged distal end 52 of the strip 48. The distal end 52 has been enlarged to facilitate locating the second terminal 26 upon the strip 48. It is noted that the distal end 52 is separated from the rest of the cladding 20 by an electrically-insulating boundary 54 which extends from the border 46 of a pad 42 in one signal channel 50 to the border 46 of the pad 42 in the next signal channel 50. Preferably, the boundary 54 is formed by etching away material of the cladding 20 to form a trough. The boundary 54 may be left in the form of an open trough, or may be filled with electrically-insulating potting material such as epoxy.

By way of alternative embodiments in the construction of the invention, it is noted that in an experimental model of the invention, the boundaries 54 were not constructed, and the distal ends 52 of the strips 48 were in electrical contact with the rest of the cladding 20. As a result, returning electric current from a laser 22 would flow primarily via the strip 48 nearest the second terminal 26 and the second terminal 38 of the signal channel 50 due to resistivity in the metal cladding 20. However, return current would also flow through other ones of the strips 48. Nevertheless, this experimental model of the invention did produce beneficial cancellation of mutual inductance between the signal channels because a major part of the current flows through one of the strips 48. However, in order to have a more precise control over the cancellation of mutual inductance, it is preferable to

have well defined paths of current flow. Such well defined paths are attained by construction of the boundary 54, as depicted in Figs. 1 and 2, to ensure that all of the return current from a laser 22 flows within the strip 48 of the signal channel 50, rather than being dispersed among other ones of the strips 48. Accordingly, the boundary 54 is provided in each of the signal channels 50 in the preferred embodiment of the invention.

Each of the output leads 40 and each of the input leads 44, in the embodiment is constructed of a partial loop of electrically conducting material, such as copper wire, and is oriented in a plane, such as the plane 56, which is perpendicular to the top surface 18 of the board 14. The wire loops of the output leads 40 are arranged side-by-side in an array. Similarly, the wire loops of the input leads 44 are arranged side-by-side in an array. The arrangement of the wire loops of the output leads 40 allows for the generation of magnetic fields produced by currents flowing in the output leads 40, the magnetic fields having flux which links the loops to provide for a positive coefficient of mutual coupling. Similarly, currents flowing in the input leads 44 generate magnetic flux which so links the loops to provide for a positive coefficient at mutual coupling.

In each of the signal channels 50, there is a partial loop 58 in the plane of the cladding 20, depicted in Fig. 1 by a dashed line, wherein current flows towards a laser 22 along one side of a border 46 and returns from the laser 22 along the opposite side of the border 46. The directions of current flow are indicated by arrows in the loop 58. To facilitate the description, the partial loop will be referred to simply as a loop, it being understood that the loop consists of only two parallel current paths disposed parallel to each other on opposite sides of a segment of a border 46. In each of the signal channels 50, current flows in the clockwise direction in each of the loops 58.

The flow of currents in the loops 58 generates magnetic flux which passes through the loops in a direction normal to the plane of the cladding 20 and circulates around, in a flux path plane perpendicular to the cladding plane, to intercept a neighboring loop 58 to provide a coefficient of mutual coupling which is negative. Therefore, contiguous signal channels 50 are linked magnetically by both positive and negative components of mutual inductance. By adjusting the length and width of the segment of the border 46 in each loop 58, the negative and the positive components of the mutual inductance can be made equal so as to cancel. The cancellation of the mutual inductance is a major feature of the invention which significantly reduces crosstalk among the various signal channels 50.

The cancellation of the mutual inductance is demonstrated with reference to Figs. 3A and 3B. In Fig. 3A, two loops 60 and 62 of wire are arranged coaxially to each other about an axis 64, and are disposed adjacent to each other, one above the other. Currents flow in the positive sense in each of the loops 60 and 62 counterclockwise as indicated by arrows on each of the loops. In Fig. 3B, loop 62 has been translated to the left and set alongside of and coplanar with the loop 60. The positive sense of current flow remains counterclockwise in each of the loops 60 and 62 as indicated by the arrows of the loops. In Fig. 3A, magnetic flux produced by current in either of the loops is directed downward along the axis 64 and links both of the loops 60 and 62. In Fig. 3B, flux produced by current in the loop 60 is directed downward through the loop 60 and travels along a curved path to pass through the loop 62 in the upward direction. This is the reverse of the situation depicted in Fig. 3A wherein flux produced by current in the loop 60 is directed downward through the loop 62. As a result, mutual inductance in the situation of Fig. 3A has a sense which is opposite the sense of the mutual inductance in the situation of Fig. 3B.

In Fig. 3A, in response to a positive change in magnitude of current flow in the loop 60, there is induced a back electromotive force producing a voltage drop in the positive direction of current flow in the loop 60, this being represented by a positive value of inductance. There is also produced a positive voltage drop in the direction of current in the loop 62, this being represented by a positive coefficient of mutual inductance. In contrast, in the situation of Figs. 3B, a positive increase of current flow in the loop 60 produces a voltage drop in the loop 62 which is directed opposite the direction of positive current flow, this being represented by a negative coefficient of mutual inductance. Upon comparing the two situations depicted in Figs. 3A and 3B with the arrangement of the electrical conductors of Fig. 1, it is seen that the arrangements of the partial loops of the output leads 40 and of the input leads 44 correspond to the arrangement of the loops 60 and 62 of Fig. 3A.

The arrangement of the loops 58 disposed in the common plane of the cladding 20 corresponds to the arrangement of the loop 60 and 62 of Fig. 3B. Therefore, the various signal channels 50 experience a magnetic coupling via positive mutual inductance of the output leads 40 and of the input leads 44 while experiencing magnetic coupling via negative mutual inductance in the loops 58. As noted above, in accordance with the invention, the dimensions of the current conducting elements in the loops 58 are adjusted to provide for a magnitude of negative mutual coupling which cancels the positive mutual coupling to produce a signifi-

cant reduction in a crosstalk among the signal channels.

Fig. 5 shows an alternative embodiment of the invention wherein the circuit modules 16 have been reconfigured to locate the first terminal at the bottom of the module 16, the first terminal being identified as 36A in its location at the bottom of the module 16. With this configuration of the modules 16, the output leads 40 of Fig. 2 are eliminated. Connection of the first terminal 36A in each of the modules 16 is provided by a strip conductor 66 which is formed from the material of the cladding 20. The strip conductor 66 extends from the terminal 36A to the front of the corresponding pad 42. In view of the removal of the output lead 40, there is less coupling of the magnetic field among the signal channels 50 by mutual inductance with the positive coefficient. Accordingly, the configuration of each of the loops 58 is to be altered to reduce the magnitude of coupling with a negative coefficient of mutual inductance.

As shown in Fig. 5, the configuration of the border, identified as the border 46A in Fig. 5, has been changed from that of the border 46 of Figs. 1 and 2 to accommodate the new connection between the first terminal 36A and the pad 42. Therein, the length of the pad 42 between front and back portions of the pad is reduced to provide for reduced coupling between the loops 58. With either the configuration of the embodiments of Figs. 1 and 5, the invention provides for substantial cancellation of the magnetic coupling for reduction in crosstalk so as to provide for improved digital communication with reduced error rate.

It is noted that any number of the signal channels 50 may be employed. To facilitate the drawing, only three of the channels 50 are portrayed in Fig. 2. However, in the aforementioned experimental model, four of the channels 50 were constructed. Many more channels may be constructed on a single circuit board, for example, there may be thirty two channels. In the construction of the foregoing experimental model, the following dimensions were employed. The dimensions are identified in Fig. 3. The spacing, A, on centerlines between contiguous channels is equal to 200 microns. The length, B, of a wire segment employed for either a lead 40 or 42 is equal to 500 microns, the cross section of the wire being square and measuring 25 microns on a side. The length, C, of a pad 42 is equal to 500 microns. The width, D, of a pad 42 is equal to 125 microns. The width, E, of a segment of the border 46 surrounding a pad 42 is equal to 25 microns. The width, F, of the conductive strip 48 between the borders 46 of successive pads 42 is equal to 25 microns. The height, G, (Fig. 1) of a laser 22 is equal to 150 microns, this being approximately equal to the

height of a circuit module 16.

Claims

1. An interconnection system for an electrical circuit, the electrical circuit including a first array (16) and a second array (22) of electrical components mounted on a circuit board (14) having an electrically conductive cladding (20), the system interconnecting the components of the first array to the components of the second array in parallel signal channels with prevention of crosstalk among the channels, comprising:
 - a plurality of wire segments arranged side by side and spaced apart in an array, each of said wire segments having a first end and a second end, the first ends of the wire segments being connected to a first terminal in each of respective components of said first array;
 - a plurality of electrically conductive pads (42) arranged side by side and spaced apart in an array facing said array of wire segments, each of said pads being surrounded by an insulating border (46) insulating the pad from the cladding, each of said pads having a first end portion and a second end portion opposite the first end portion, the second end portions of said pads being connected to a first terminal in each of respective components of said second array;
 - an array of conductive strips (48) formed in said cladding and located between successive ones of said pads, said borders being separated from each other by said conductive strips, said conductive strips extending from said first array of components to said second array of components to provide electrical connection between a second terminal in each component of said first array and a second terminal in each corresponding component of said second array; and
 - wherein the second ends of said wire segments are connected to the first end portions in respective ones of said pads for communicating signals in respective ones of said signal channels, each of said wire segments forming a first partial loop disposed in a plane perpendicular to a plane of said cladding, the first loops providing magnetic coupling with a first mutual inductance among successive ones of said wire segments, there being segments of said borders contiguous said strips, each of said border segments defining a second partial loop parallel to said cladding plane in respective ones of said signal channels, the second loops providing magnetic coupling with a second mutual inductance among successive

ones of said pads, the second mutual inductance tending to cancel the first mutual inductance for prevention of crosstalk among said signal channels.

2. A system according to claim 1 wherein said pads have a rectangular shape.
3. A system according to claim 2 further comprising a second plurality of wire segments arranged side-by-side and spaced apart in an array, each of the wire segments of said second plurality of electrically conductive pads being arranged side-by-side and spaced apart, the wire segments of said second plurality of wire segments each having a first end and a second end of which the first ends of the wire segments are connected to the first terminal in each of respective components of said second array, the second end portions of said pads being connected respectively to the second ends of said second plurality of wire segments.
4. An electro-optical transmitter for the generation and transmission of optical signals via optical fibers, the system including an array of solid-state lasers (22) positioned for applying light to the optical fibers, an array of laser driver modules (16) electrically connected to said lasers for exciting the lasers to generate light signals, the lasers and the drivers constituting an electrical circuit; and
 - wherein in said electrical circuit, said drivers and said lasers are mounted on a circuit board having an electrically conductive cladding, the electrical circuit including a system for interconnecting the drivers to the lasers via parallel signal channels with prevention of crosstalk among the channels;
 - said interconnection system comprises a plurality of wire segments arranged side-by-side and spaced apart in an array, each of said wire segments having a first end and a second end, the first ends of the wire segments being connected to a first terminal in each of respective ones of said lasers;
 - a plurality of electrically conductive pads arranged side-by-side and spaced apart in an array facing said array of wire segments, each of said pads being surrounded by an insulating border insulating the pad from the cladding, each of said pads having a first end portion and a second end portion opposite the first end portion, the second end portions of said pads being connected to a first terminal in each of said drivers;
 - an array of conductive strips formed in said cladding and located between successive ones

of said pads, said borders being separated from each other by said conductive strips, said conductive strips extending from said lasers to said drivers to provide electrical connection between a second terminal in each of said lasers and a second terminal in a corresponding one of each of said drivers; and wherein the second ends of said wire segments are connected to the first end portions in respective ones of said pads for communicating signals in respective ones of said signal channels, each of said wire segments forming a first partial loop disposed in a plane perpendicular to a plane of said cladding, the first loops providing magnetic coupling with a first mutual inductance among successive ones of said wire segments, there being segments of said borders contiguous said strips, each of said border segments defining a second partial loop parallel to said cladding plane in respective ones of said signal channels, the second loops providing magnetic coupling with a second mutual inductance among successive ones of said pads, the second mutual inductance tending to cancel the first mutual inductance for prevention of crosstalk among said signal channels.

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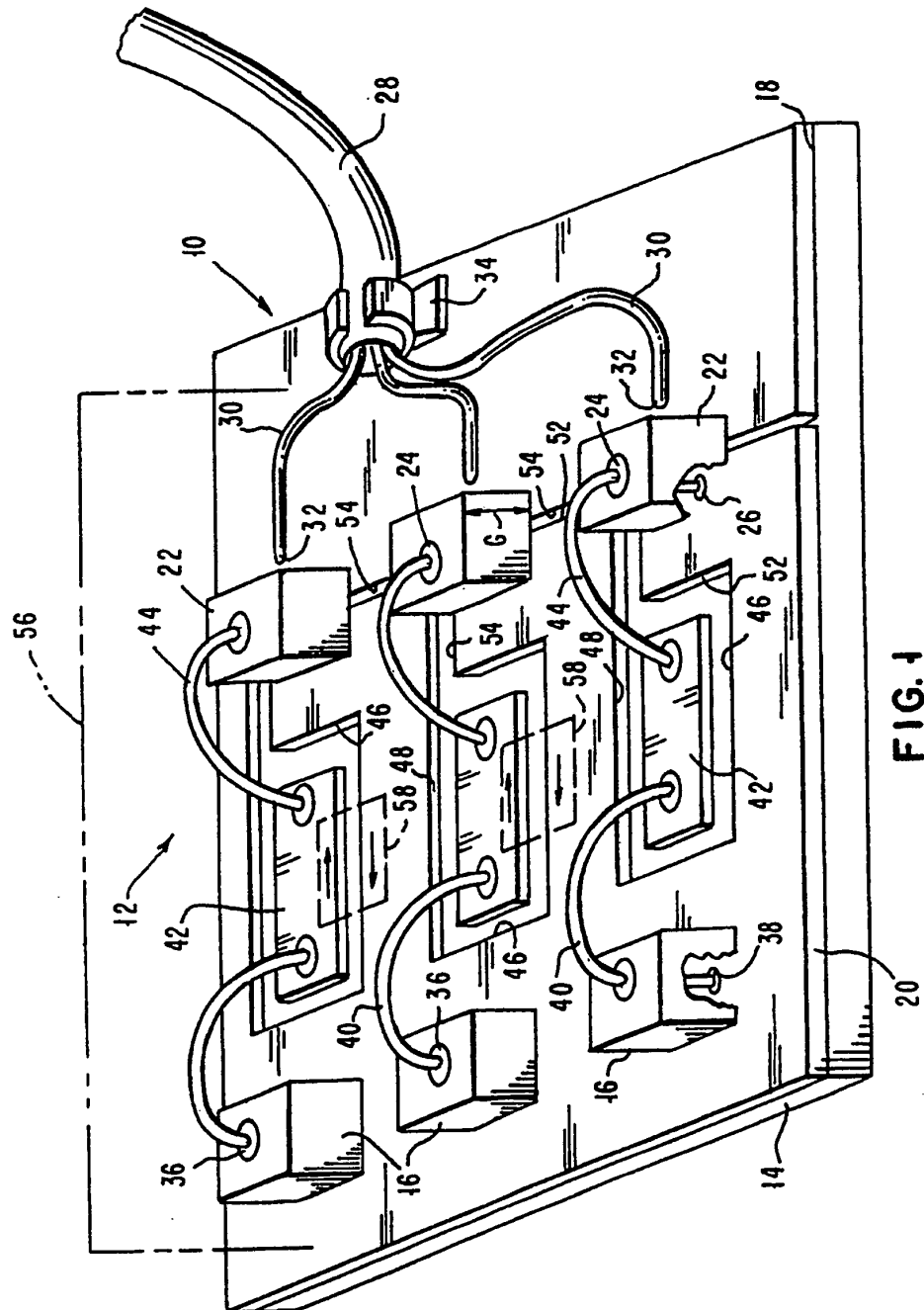


FIG. 1

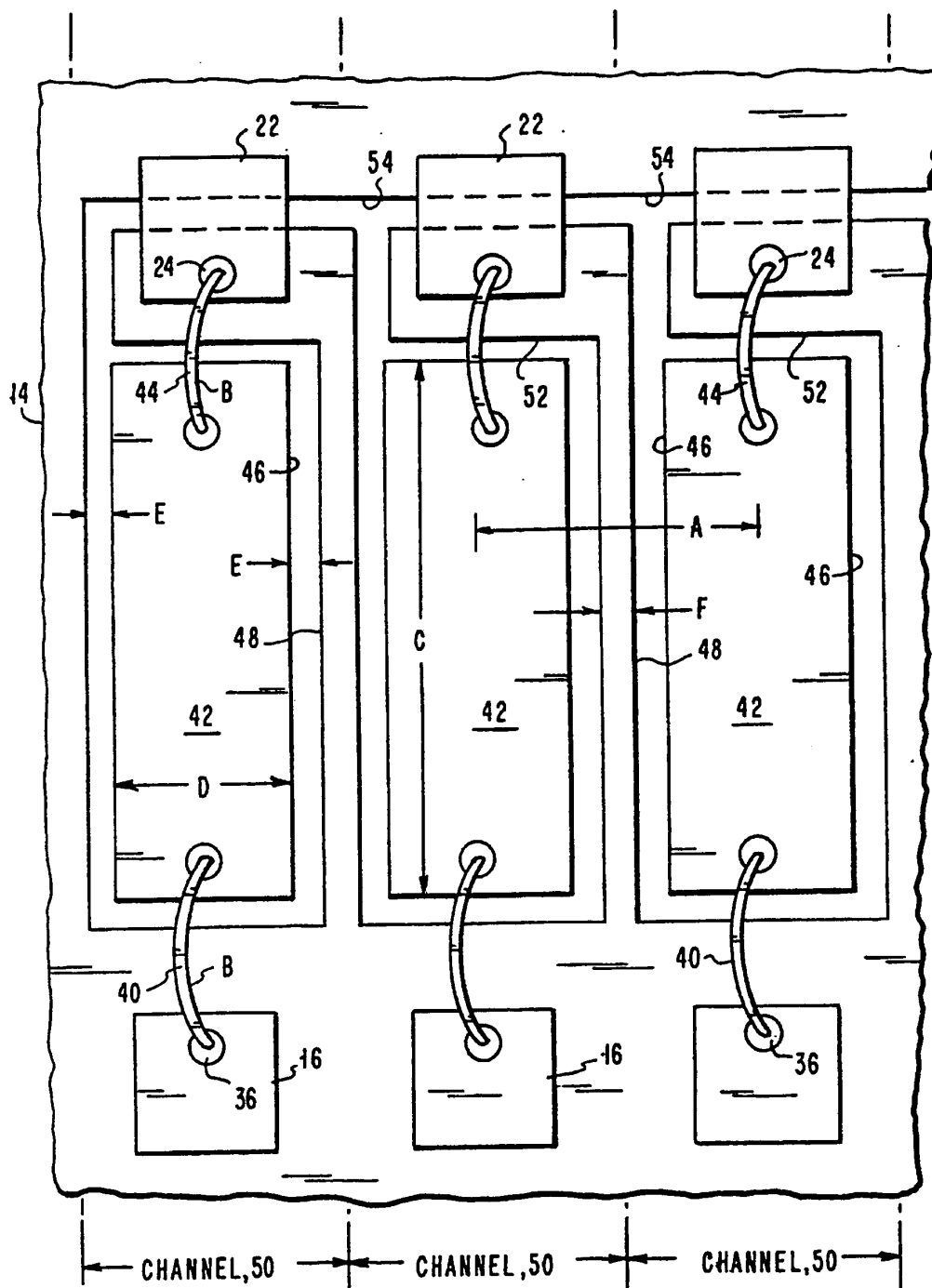


FIG. 2

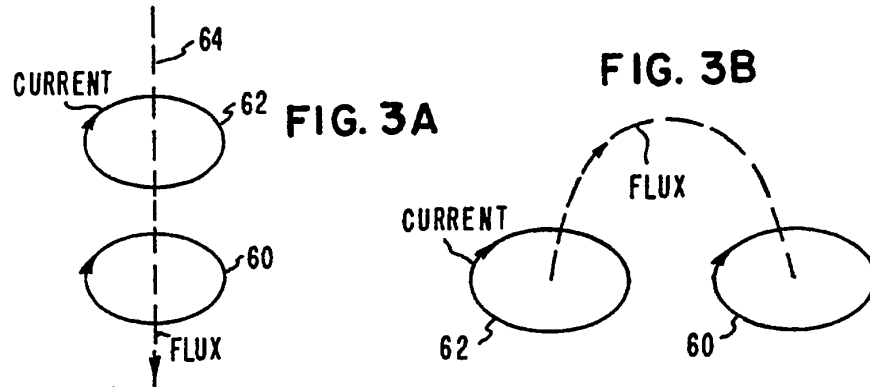
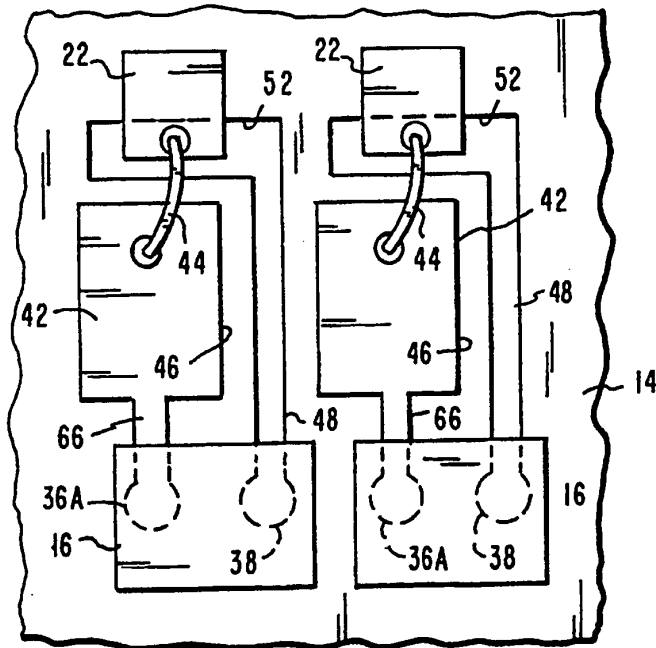


FIG. 4





European
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EUROPEAN SEARCH REPORT

Application Number

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DOCUMENTS CONSIDERED TO BE RELEVANT					
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)		
Y	WO-A-8 304 157 (COMPAGNIE D'INFORMATIQUE MILITAIRE SPATIALE ET AERONAUTIQUE) * page 7, lines 11 - 33; figure 6 * - - - -	1,4	G 02 B 6/42		
Y	US-A-3 963 920 (PALMER) * column 3, lines 22 - 59; figure 3 * - - - -	1,4			
A,D	US-A-4 758 805 (YAMAZAKI) * column 3, lines 5 - 19 * - - - -	1			
A,D	EP-A-0 216 389 (NIPPONDENSO) * column 4, line 45 - page 5, line 11 * - - - - -	1			
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)		
			G 02 B H 05 K H 02 H H 03 H		
The present search report has been drawn up for all claims					
Place of search The Hague		Date of completion of search 23 April 91	Examiner TOUSSAINT F.M.A.		
<table border="0"><tr><td>CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention</td><td>E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</td></tr></table>				CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention	E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document
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(71) Applicant: **Broadcom Corporation**
Irvine, California 92618-7013 (US)

(72) Inventors:
• **Tonietto, Davide**
92677 Laguna Niguel (US)
• **Ghiasi, Ali**
95014 Cupertino, California (US)

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(74) Representative: **Jehle, Volker Armin, Dipl.-Ing.**
Patentanwälte
Bosch, Graf von Stosch, Jehle,
Flüggensstrasse 13
80639 München (DE)

(54) **Signal conditioning circuit with input equalization and output pre-emphasis**

(57) A high-speed bit stream interface module interfaces a high-speed communication media to a communication Application Specific Integrated Circuit (ASIC) via a Printed Circuit Board (PCB). The high-speed bit stream interface module includes a line side interface, a board side interface, and a signal conditioning circuit. The line side interface includes a media coupler that receives the line side media, either copper media or optical media. The board side interface couples the high-

speed serial bit stream interface module to the PCB. A signal conditioning circuit communicatively couples to the line side interface and to the board side interface. The signal conditioning circuit receives an RX signal (X) from the line side interface, conditions the RX signal (306), and provides the RX signal to the board side interface (A'). The signal conditioning circuit receives a TX signal (D') from the board side interface, conditions the TX signal (312), and provides the TX signal to the Line side interface (Y).

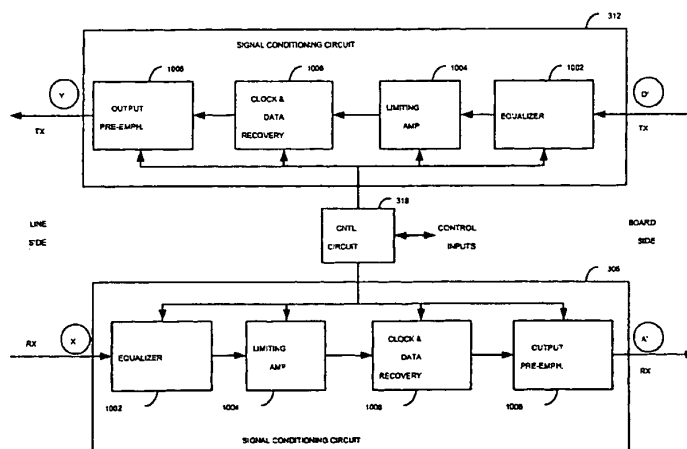


FIG. 10

Description**BACKGROUND OF THE INVENTION**5 **1. TECHNICAL FIELD OF THE INVENTION**

[0001] The present invention relates generally to communication systems; and more particularly to high-speed serial bit stream communications.

10 **2. DESCRIPTION OF RELATED ART**

[0002] The structure and operation of communication systems is generally well known. Communication systems support the transfer of information from one location to another location. Early examples of communication systems included the telegraph and the public switch telephone network (PSTN). When initially constructed, the PSTN was a circuit switched network that supported only analog voice communications. As the PSTN advanced in its structure and operation, it supported digital communications. The Internet is a more recently developed communication system that supports digital communications. As contrasted to the PSTN, the Internet is a packet switch network.

[0003] The Internet consists of a plurality of switch hubs and digital communication lines that interconnect the switch hubs. Many of the digital communication lines of the Internet are serviced via fiber optic cables (media). Fiber optic media supports high-speed communications and provides substantial bandwidth, as compared to copper media. At the switch hubs, switching equipment is used to switch data communications between digital communication lines. WANs, Internet service providers (ISPs), and various other networks access the Internet at these switch hubs.

[0004] In a particular example of a packet switched network, a switch that services the digital communication requirements of a number of users located within a building in a large city couples via fiber media to switches mounted in other buildings within the city, to switches located in other cities/states/countries, and to switch hubs servicing the Internet. This structure is not unique to the Internet. Portions of the PSTN, wireless cellular network infrastructure, Wide Area Networks (WANs), and other communication systems employ the same or similar structures.

[0005] Switches route incoming traffic and outgoing traffic. A typical switch (or switch hub) includes a housing having a plurality of slots that are designed to receive Printed Circuit Boards (PCBs) upon which integrated circuits and various media connectors are mounted. The PCBs removably mount within the racks of the housing and typically communicate with one another via a back plane of the housing. Each PCB typically includes at least two media connectors that couple the PCB to a pair of optical cables and/or copper media. The optical and/or copper media serves to couple the PCB to other PCBs of other switches located in the same geographic area or to other PCBs of other switches located at another geographic area.

[0006] Typically, Application Specific Integrated Circuits (ASICs) mount upon the PCBs of the housing and perform switching operations for the data that is received on the coupled media and data that is transmitted on the coupled media. The coupled media typically terminates in a receptacle mounted on the PCB. Transceiving circuitry coupled to the receptacle and mounted upon the PCB performs signal conversion operations from the signal format of the coupled media and a bit stream format of the ASIC. In most installations, the media, e.g., optical media, operates in a simplex fashion. In such case, one optical media will carries incoming data (RX data) to the PCB while another optical media carries outgoing data (TX data) from the PCB. Thus, the transceiving circuitry typically includes incoming circuitry and outgoing circuitry, each of which couples to a media connector on a first side and communicatively couples to the ASIC on a second side. The ASIC may also couple to a back plane interface that allows the ASIC to communicate with other ASICs located in the enclosure via a back plane connection. The ASIC is designed and implemented to provide desired switching operations. The operation of such enclosures and the PCBs mounted therein is generally known.

[0007] The conversion of information on the optical media or copper media to a signal that may be received by the ASIC and vice versa requires satisfaction of a number of requirements. First, the coupled physical media has particular RX signal requirements and TX signal requirements. These requirements must be met at the boundary of the connector to the physical media. Further, the ASIC has its own unique RX and TX signal requirements. These requirements must be met at the ASIC interface. Thus, the transceiving circuit that resides between the physical media and the ASIC must satisfy all of these requirements.

[0008] Various standardized interfaces have been employed to couple the transceiving circuit to the ASIC. These standardized interfaces include the XAUI interface, the Xenpak interface, the GBIC interface, the XGMII interface, and the 300 Pin MSA interface. Each of these particular standardized interfaces has unique requirements and related shortcomings. Generally, each of these interfaces requires substantial PCB board space and some of these interfaces supports a lesser throughput than is required by many current systems.

[0009] Thus, there is a need in the art for low cost universal interface that interfaces an ASIC to a high-speed serial media on a printed circuit board.

BRIEF SUMMARY OF THE INVENTION

[0010] Thus, in order to overcome the shortcomings of the prior interfaces, among other shortcomings, a high-speed bit stream interface module constructed according to the present invention communicatively interfaces a high-speed communication media to a communication Application Specific Integrated Circuit (ASIC). The high-speed bit stream interface module includes a line interface that couples to a pair of high speed interface lines and a communication ASIC interface that communicatively couples to the communication ASIC.

[0011] The high-speed bit stream interface module is removably mountable on a Printed Circuit Board (PCB) that services the communication ASIC. Depending upon the particular embodiment of the high-speed bit stream interface module, the line interface supports optical media or copper based media. In various embodiments described herein, the media includes a TX media upon which data is transmitted and RX media upon which data is received. In one embodiment, therefore, the high-speed bit stream interface module includes receptacles for at least one pair of fiber optic media. In another embodiment, the high-speed bit stream interface module includes receptacles for at least one pair of copper media. The high-speed bit stream interface module may be received by the PCB in a socket that supports both communication with the communication ASIC and that supports the control and powering of the high-speed bit stream interface module. Such mounting allows the high-speed bit stream interface module to be removed while the remaining components mounted on the PCB continue to function.

[0012] The interface between the high-speed bit stream interface module and the communication ASIC is referred to as the board interface. The board interface includes a TX path and an RX path. The TX path of the board interface carries data from the communication ASIC to the high-speed bit stream interface module. Such data is received by the high-speed bit stream interface module and conditioned into a format suitable for delivery to a coupled TX media. Likewise, the high-speed bit stream interface module receives RX data from a coupled RX media and conditions it. After conditioning, the high-speed bit stream interface module provides the conditioned RX data to the communication ASIC via the RX path of the board interface.

[0013] According to the present invention, the high-speed bit stream interface module includes line connectors, a board interface connector, and a signal conditioning circuit that is controlled by control circuitry also contained in the high-speed bit stream interface module. The signal conditioning circuit includes an input equalizer, a limiting amplifier, clock and data recovery circuitry, and output pre-emphasis circuitry. The input equalizer receives an input bit stream and equalizes the input bit stream to remove deterministic jitter from the input bit stream. The limiting amp receives the output of the equalizer and amplifies the bit stream to predefined amplitude. The clock and data recovery circuitry receives the output of the limiting amplifier and recovers the clock and the data from the signal. The output pre-emphasis circuitry receives the output of the clock and data recovery circuitry and pre-emphasizes the bit stream prior to its transmission.

[0014] According to the present invention, identical signal conditioning circuits are used for the RX path serviced by the high-speed bit stream interface module and for the TX path serviced by the high-speed bit stream interface module. In such case, the various components of the signal conditioning circuit are controllable by a coupled control circuit to cause them to perform the unique operations of each serviced path. By using identically constructed signal conditioning circuits for both the RX path and the TX path and simply programming the signal conditioning circuits for their own unique operations, substantial design efficiencies, manufacturing efficiencies, and construction efficiencies are obtained.

[0015] By being able to program the operation of the components of the signal conditioning circuit, the unique characteristics of the TX path and the RX path are substantially/fully addressed. These programmable characteristics address both the input side of the signal conditioning circuit and the output side of the signal conditioning circuit. In the RX path, the signal conditioning circuit receives data at the line side. Further, in the TX path, the signal conditioning circuit receives data at the board side. The input characteristics in the TX path vary with the type of media providing the receive bit stream on the line side. For example, when optical fiber is employed as the line side media, the input bit stream will have different characteristics than will the input bit stream when serviced by a copper media. Moreover the input characteristics on the board side TX path vary significantly from the input characteristics on the line side RX path. Further, the output characteristics on the line side of the signal conditioning circuit in the TX path differ greatly from the output characteristics required of the signal conditioning circuit on the board side in the RX path. The output characteristics are separately addressed by the programmable characteristics of the signal conditioning circuit of the present invention.

[0016] According to an aspect of the invention, a high-speed serial bit stream conditioning circuit is provided comprising:

an adaptive equalizer that receives a high-speed serial bit stream and that spectrally shapes the high-speed serial bit stream to produce an equalized high-speed serial bit stream; and
a clock and data recovery circuit operably coupled to the output of the adaptive equalizer that recovers the equalized

high-speed bit stream to produce an output high-speed serial bit stream.

[0017] Advantageously, the adaptive equalizer automatically determines spectral shaping control settings; and
the adaptive equalizer uses the spectral shaping control settings to spectrally shape the high-speed serial bit stream such that the spectral characteristics of the equalized high-speed serial bit stream substantially correspond to reference spectral characteristics.

[0018] Advantageously, the spectral shaping control settings comprise at least one filter setting and at least one gain setting.

[0019] Advantageously, the signal conditioning circuit determines the spectral shaping control settings based upon a ratio of a first spectral component of the high-speed serial bit stream to a second spectral component of the high-speed serial bit stream.

[0020] Advantageously, the equalizer spectrally shapes the high-speed serial bit stream to remove deterministic jitter from the high-speed serial bit stream.

[0021] Advantageously, the signal conditioning circuit spectrally shapes the high-speed serial bit stream to remove inter symbol interference from the high-speed serial bit stream.

[0022] Advantageously, the equalizer comprises:

an automatic gain control loop that receives the high-speed serial bit stream and that performs gain control operations on the high-speed serial bit stream;

an adaptive equalizer operably coupled to receive the output of the automatic gain control loop, wherein the adaptive equalizer equalizes the high-speed serial bit stream based upon spectral shaping control settings to produce the equalized high-speed serial bit stream; and

an adaptive equalizer feedback operably coupled to the output of the automatic gain control loop, wherein the adaptive equalizer determines the spectral shaping control settings and provides the spectral shaping control settings to the adaptive equalizer.

[0023] Advantageously, the adaptive equalizer comprises:

a constant gain low pass filter;

a plurality of cascaded tuned amplifiers; and

a summing node,

wherein the constant gain low pass amplifier and the plurality of cascaded tuned amplifiers receive the output of the automatic gain control loop, wherein the summing node receives the output of the constant gain low pass amplifier and the output of the plurality of cascaded tuned amplifiers, and wherein the summing node sums the output of the constant gain low pass amplifier and the output of the plurality of cascaded tuned amplifiers based upon the spectral shaping control settings.

[0024] Advantageously, the adaptive equalizer feedback comprises:

a first feedback path that determines a first spectral component of the equalized high-speed serial bit stream;

a second feedback path that determines a first spectral component of the equalized high-speed serial bit stream; and

an integrator operably coupled to receive and compare the first feedback path and the second feedback path, wherein the integrator produces the spectral shaping control settings.

[0025] Advantageously, the first feedback path comprises a first tuned amplifier, a gain stage, and a rectifier;

the second feedback path comprises a second tuned amplifier, a gain stage, and a rectifier; and

wherein the first tuned amplifier passes a first spectral component of the equalized high-speed serial bit stream; and

wherein the second tuned amplifier passes a second spectral component of the equalized high-speed serial bit stream.

[0026] Advantageously, the high-speed serial bit stream conditioning circuit further comprises output pre-emphasis circuit that controllably modifies the spectrum of the equalized high-speed bit stream to pre-compensate for the spectral characteristics of a signal path upon which the equalized high-speed bit stream will be output.

[0027] Advantageously, the high-speed serial bit stream conditioning circuit further comprises a limiting amplifier that receives high-speed serial bit stream and that controllably amplifies high-speed serial bit stream to produce high-speed serial bit stream in a desired output range.

[0028] Advantageously, the clock and data recovery circuit has an adjustable Phase Locked Loop (PLL) bandwidth

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that is controlled based upon the bandwidth of the high-speed serial bit stream.

[0029] According to another aspect of the invention, a method for equalizing a high-speed serial bit stream is provided comprising:

- 5 receiving the high-speed serial bit stream;
spectrally shaping the high-speed serial bit stream based upon spectral shaping control settings; and
adjusting the spectral shaping control settings so that the spectral characteristics of the high-speed serial bit stream substantially correspond to reference spectral characteristics.
- 10 [0030] Advantageously, the spectral shaping control settings comprise at least one filter setting and at least one gain setting.
[0031] Advantageously, the spectral shaping control settings are determined by:
- 15 determining a first spectral component of the high-speed serial bit stream;
determining a second spectral component of the high-speed serial bit stream; and
determining the spectral shaping control settings based upon a ratio of the first spectral component and the second spectral component.
- [0032] Advantageously, the spectrally shaping the high-speed serial bit stream removes deterministic jitter from the high-speed serial bit stream.
- 20 [0033] Advantageously, the spectrally shaping the high-speed serial bit stream removes inter symbol interference from the high-speed serial bit stream.
- [0034] Advantageously, the method further comprises modifying the spectrum of the output high-speed serial bit stream to pre-compensate for the spectral characteristics of a signal path upon which the output high-speed serial bit stream is coupled.
- 25 [0035] Advantageously, the method further comprises amplifying the high-speed serial bit stream using a gain setting corresponding to a dynamic range of the high-speed serial bit stream as received.
- [0036] Advantageously, the method further comprises recovering the high-speed bit stream to produce an output high-speed serial bit stream, wherein recovering the high-speed serial bit stream is performed using a Phase Locked Loop (PLL) having a controllable PLL bandwidth that is set to correspond to a jitter bandwidth of the high-speed serial bit stream.
- 30 [0037] Other features and advantages of the present invention will become apparent from the following detailed description of the invention made with reference to the accompanying drawings.

35 BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0038] These and other features, aspects and advantages of the present invention will be more fully understood when considered with respect to the following detailed description, appended claims and accompanying drawings wherein:

- 40 FIG. 1 is a block diagram illustrating a printed circuit board upon which high-speed bit stream interface modules constructed according to the present invention are mounted;
FIG. 2 is a block diagram illustrating the interconnection of a high-speed bit stream interface module constructed according to the present invention with a communication ASIC;
- 45 FIG. 3 is a block diagram illustrating a first embodiment of a high-speed bit stream interface module of the present invention that services optical fiber media;
FIG. 4 is a block diagram illustrating a second embodiment of a high-speed bit stream interface module of the present invention that services copper media;
FIG. 5A is a block diagram illustrating generally the structure of a portion of structure of the communication ASIC of FIG. 1;
- 50 FIG. 5B is a block diagram illustrating a pin out of the interface between the high-speed bit stream interface module of the present invention and a communication ASIC;
FIG. 5C is a transmitter electrical specification of the interface between the high-speed bit stream interface module of the present invention and a communication ASIC and also a diagram illustrating the described return loss characteristics;
- 55 FIG. 5D is a transmitter jitter specification of the interface between the high-speed bit stream interface module of the present invention and a communication ASIC and also a diagram illustrating how the components of the jitter specification are defined;

FIG. 5E is a receiver electrical specification of the interface between the high-speed bit stream interface module of the present invention and a communication ASIC and also a diagram illustrating the described return loss characteristics;

FIG. 5F is a receiver jitter specification of the interface between the high-speed bit stream interface module of the present invention and a communication ASIC and also a diagram illustrating how the components of the jitter specification are defined;

FIG. 5G is a graph illustrating the frequency response of a connector of the high-speed bit stream interface module in combination with a 4" FR4 trace of the PCB coupling the connector to the communication ASIC;

FIGS. 6A and 6B are diagrams illustrating a bit stream that has no little or no jitter;

FIGS. 7A and 7B illustrate a bit stream having some jitter and the manner in which jitter effects the eyes of the data;

FIGS. 7A and 7B illustrate a bit stream having some jitter and amplitude variations and the manner in which the jitter and amplitude variations affect the ability of a receiver to extract data there from;

FIGS. 8A and 8B illustrate a bit stream having significant jitter and significant amplitude variations and the manner in which the jitter and amplitude variations affect the ability of a receiver to extract data there from;

FIGS. 9A and 9B illustrate a bit stream having significant jitter and significant amplitude variations and the manner in which the jitter and amplitude variations preclude a receiver from extracting all carried data from the bit stream;

FIG. 10 is a block diagram illustrating signal conditioning circuits constructed according to the present invention that service both a TX path and a RX path for a high-speed bit stream interface module constructed according to the present invention;

FIG. 11 is a block diagram illustrating a clock and data recovery circuit constructed according to the present invention;

FIG. 12 is a logic diagram illustrating operations according to the present invention in setting the PLL bandwidth of the clock and data recovery circuits of the TX path and RX path signal conditioning circuits;

FIG. 13 is a logic diagram illustrating operation according to the present invention in programming an equalizer to compensate for deterministic jitter;

FIG. 14 is a block diagram illustrating one embodiment of an equalizer and a limiting amp of a signal conditioning circuit constructed according to the present invention;

FIG. 15 is a schematic diagram illustrating the structure of one of the cascaded tuned amplifiers of the equalizer of FIG. 14;

FIG. 16 is a graph illustrating the theoretical power spectrum of a Pseudo Random Bit Stream signal (PRBS) and the power spectral density of a PRBS signal with high frequency attenuation;

FIG. 17 is a graph illustrating various signal path attenuation properties and equalizer frequency responses corresponding to the signal path attenuation properties;

FIG. 18 is a logic diagram illustrating operation according to the present invention in determining pre-emphasis circuit settings for a particular signal path and connector combination;

FIG. 19 is a graph illustrating various frequency responses of the connection between the high-speed bit stream interface module and the communication ASIC of the PCB;

FIG. 20 is a logic diagram illustrating operation according to the present invention in programming the dynamic range of a limiting amplifier of the signal conditioning circuit of the present invention;

FIG. 21 is a block diagram illustrating a limiting amp 1004 constructed according to the present invention; and

FIG. 22 is a schematic diagram illustrating a common mode logic stage of the limiting amplifier of the signal conditioning circuit of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0039] FIG. 1 is a block diagram illustrating a Printed Circuit Board (PCB) 100 upon which high-speed bit stream interface modules 102A, 102B, and 102C constructed according to the present invention are mounted. The PCB 100 illustrated in FIG. 1 may be installed in a housing that services all or a portion of the communication requirements of a particular switch. The PCB 100 includes three high-speed bit stream interface modules 102A, 102B, and 102C. Each of these high-speed bit stream interface modules 102A, 102B, and 102C couples both to a pair of lines on a line interface side and also couples to conductive traces via connectors on the board interface side. Each of the high-speed bit stream interface modules 102A, 102B, and 102C when mounted on the PCB 100 communicates services respective communications for Application Specific Integrated Circuits (ASICs) 104A, 104B, and 104C, respectively. During normal operations, the high-speed bit stream interface module 102A, 102B, and 102C interface to respective communication lines and to respective communication ASICs 104A, 104B, and 104C, respectively.

[0040] As will be described further with reference to FIGS. 3 and 4, the lines coupling to the high-speed bit stream interface modules 102A, 102B, and 102C may be optical, copper or another media type. When the high-speed bit stream interface modules 102A, 102B, and 102C service optical media, communications may be according to SONET,

10GIGE, 10GFC, or another operating standard. The housing and the PCBs located therein may serve as an Internet switch, an Internet hub, an Intranet switch, a telephone network hub, a data center, a Wide Area Network (WAN), or service communication system device.

5 [0041] With the embodiment of FIG. 1, the high-speed bit stream interface modules 102A, 102B, and 102C support a minimum of 8" of FR4 trace on the PCB 100. The high-speed bit stream interface modules 102A, 102B, and 102C are data and protocol agnostic such that they can service a large number of differing bit stream interface standards. In such case, the high-speed bit stream interface modules 102A, 102B, and 102C support any various communication protocol and data rate. It is anticipated that the high-speed bit stream interface modules 102A, 102B, and 102C will support data rates in the 10 GBPS range. However, other data rates may also be supported.

10 [0042] Each of the communication ASICs 104A, 104B, and 104C communicates with other ASICs via a back plane 108 and respective back plane interfaces 106A, 106B, and 106C. The structure and operation of back plane communications is generally known and will not be described further herein except as it relates to the present invention.

[0043] The teachings of the present invention may be applied to a standardized module format. In particular, many of the teachings of the present invention have been incorporated into the XFP (10 Gigabit Form factor Pluggable Module) specification. However, the teachings of the present invention may be practiced without practicing a standardized specification to achieve the great benefits of the present invention.

15 [0044] FIG. 2 is a block diagram illustrating the interconnection of a high-speed bit stream interface module constructed according to the present invention with a communication ASIC. As is illustrated in FIG. 2, the high-speed bit stream interface module 102A couples on the line interface side (line side) to a TX media and an RX media. Further, on the board interface side (board side), the high-speed bit stream interface module 102A couples to receive TX data from communication ASIC 104A and couples to produce RX data to communication ASIC 104A. In the embodiments illustrated herein, the high-speed bit stream interface module 102A supports high-speed bit stream communications. The bit stream communications may be either in a non-return-to-zero (NRZ) bit stream data format or in a return-to-zero bit stream data format. These bit stream data formats are protocol agnostic and thus the high-speed bit stream interface module 102A supports various operating standards and operates upon the high-speed bit stream in a fashion that is consistent with a number of bit stream communication protocols.

20 [0045] The high-speed bit stream interface module 102A operates to condition signals received at points labeled as X and D. Further, the high-speed bit stream interface module operates to produce data at points A and Y. All data is received in a high-speed bit stream format and is produced in a high-speed bit stream format. From point D to point Y the high-speed bit stream interface module 102A receives a board side bit stream and conditions the bit stream to remove the deterministic jitter and to prepare the bit stream for transmission in a format that meets the line interface transmission standard at point Y. Likewise, the high-speed bit stream interface module 102A receives a line side bit stream at point X and conditions the line side bit stream prior to producing the bit stream at point A on the board side interface in a desired format. The term "bit stream" is used interchangeably herein with the term "data."

25 [0046] The communication ASIC 104A as is further illustrated in FIG. 5 produces data at point C and receives data at point B. The communication ASIC 104A will have requirements for the condition of the received data at point B and will have transmit specifications for the data it produces at point C. Further, from point C to point D, the PCB 100 trace will degrade the quality of the data between point C and point D. As is known, PCB traces attenuate high frequency signals due to skin effect of the traces. Further, dielectric loss of the PCB 100 will also affect the properties of data traveling along the trace. The PCB 100 also degrades/distorts the quality of the bit stream traveling from point A to point B as it does the bit stream traveling from point C to point D.

30 [0047] The high-speed bit stream interface module 102A must produce a signal at point A that upon receipt at point B by the communication ASIC 104A meets the received signal requirements of the communication ASIC 104A. Further, the high-speed bit stream interface module 102A must produce a signal at point Y that meets the transmission requirements of the line side interface. Moreover, the high-speed bit stream interface module 102A must receive TX data at point D and condition the signal sufficiently so that it meets the transfer requirements at point Y. Also, the high-speed bit stream interface module must receive RX data at point X and condition the signal sufficiently so that it meets the transfer requirements at point A. The manner in which the high-speed bit stream interface module 102A performs these tasks is further described herein in detail with reference to FIGS. 3-22.

35 [0048] FIG. 3 is a block diagram illustrating a first embodiment of a high-speed bit stream interface module of the present invention that services optical fiber media. As shown in FIG. 3, when the high-speed bit stream interface module 102A, 102B, or 102C services an optical fiber media, the high-speed bit stream interface module 102A includes components required for servicing to the optical fiber. In particular, in the RX path the optical fiber couples to the high-speed bit stream interface module 102A at a photo diode receptacle 302 that includes a pre-amplification circuit. The photo diode and pre-amplification circuit 302 receives an optical signal from the RX path fiber media and converts the optical signal to an electrical signal. The output of the photo diode pre-amplification circuit 302 is provided to trans-impedance amplifier 304, which amplifies the signal. The output of the trans-impedance amplifier 304 is received by signal conditioning circuit 306. The signal conditioning circuit 306 receives the signal at point X and conditions the circuit to produce

an output at point A'. The output signal at point A' is then coupled via connector 310 to point A on the board side of the high-speed bit stream interface module 102A (or 102B or 102C).

[0049] In the TX path, the high-speed bit stream interface module 102A receives TX data from the communication ASIC at point D on the board side. Connector 310 couples the transmit signal to the signal conditioning circuits at point D'. The signal conditioning circuit 312 receives the signal at point D', conditions the signal, and produces a conditioned signal to laser diode amplifier 314 at point Y. The laser diode amplifier 314 amplifies the signal received from signal conditioning circuit 312 at point Y and provides the electrical signal to laser 316. Laser 316 couples to transmit optical media and produces the transmit signal at that location.

[0050] FIG. 4 is a block diagram illustrating a second embodiment of a high-speed bit stream interface module of the present invention that services copper media. As is shown in FIG. 4, the embodiment of the high-speed bit stream interface module that services a copper media does not include those components respective to the optical media. However, the high-speed bit stream interface module 102A, 102B, or 102C includes the connector 310, signal-conditioning circuit 312, signal conditioning circuit 306, and the control circuitry 318. However in the embodiment of FIG. 4, in the TX path the output signal conditioning circuit 312 couples the TX data directly to TX media connector 402 that couples the TX data to TX copper media. Likewise, in the RX path an RX media connector 404 couples to RX copper media to receive the RX data and to couple the RX data to signal conditioning circuit 306.

[0051] As will be described further, the signal conditioning circuits 306 and 312 have an identical structure but are controllable to meet the specific requirements of their respective signal paths. The flexibility provided by the programmability of these circuits is significant. Because of this flexibility, the high-speed bit stream interface module 102A, 102B, or 102C may be installed in any PCB and be employed to service any of a large number of bit stream interface standards. By programming the operation of the signal conditioning circuits 306 and 312, the high-speed bit stream interface module 102A, 102B, or 102C is able to compensate for the unique construction of the PCB which it services, the requirements of the coupled ASIC, and also the requirements of the serviced media/protocol.

[0052] FIG. 5A is a block diagram illustrating generally a portion of the structure of the communication ASIC (104A, 104B, or 104C) of FIG. 1. As shown in FIG. 5A, the communication ASIC 104A (104B or 104C) includes a signal processing integrated circuit 502, a multiplexer 504, and a demultiplexer 506. On the RX side the demultiplexer 506 receives the RX data at point B and demultiplexes the data to provide the de-multiplexed data to the signal processing integrated circuit 502. On the transmit side, the signal processing integrated circuit 502 produces TX data to the multiplexer 504 which multiplexes the data to produce the transmit data at point C. As was previously described, the multiplexer 504 produces data at point C according to transmit specifications for the communication ASIC 104A-104C. Likewise, the demultiplexer 506 is required to recover a signal at point B that meets its receive signal characteristics.

[0053] As was previously illustrated with respect to FIG. 1, communication ASIC couples to the back plane 108 via a back plane interface. Thus, the signal processing integrated circuit includes an interface to the back plane interface. Of course, the communication ASIC 104A (104B or 104C) will typically include components in addition to those illustrated in FIG. 5A.

[0054] FIG. 5B is a block diagram illustrating a pin out of the interface between the high-speed bit stream interface module of the present invention and a communication ASIC. In addition to the two wire serial interface the module has a number of low speed hard wired pins for control and status of the high-speed bit stream interface module. The interface between the high-speed bit stream interface module and the communication ASIC includes differential RX data signal lines RD+ and RD-. The interface further includes differential TX data signal lines TX+ and TX-. Further, the interface includes differential clock lines RefCLK+ and RefCLK-. The interface further includes various status lines, power lines, ground lines, and other lines as indicated in Table 1 - below.

TABLE 1 -

Module Interface to Communication ASIC			
Pin	Logic	Symbol	Name/Description
1		Gnd	Module Ground
2		VEE5	Optional -5.2V Power Supply
3	LVTTL-I	Mod_Desel	Module De-select; When held low allows the module to respond to 2-wire serial interface commands
4	LVTTL-O	Interrupt	Interrupt; Indicates presence of an important condition which can be read over the serial 2-wire interface
5	LVTTL-I	TX_DIS	Transmitter Disable; Transmitter Laser Source Turned Off
6		VCC5	+5V Power Supply

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TABLE 1 - (continued)

Module Interface to Communication ASIC			
Pin	Logic	Symbol	Name/Description
7		Gnd	Module Ground
8		VCC3	+3.3V Power Supply
9		VCC3	+3.3V Power Supply
10	LVTTL-I	SCA	Two Wire Interface Clock
11	LVTTL-I/O	SDA	Two Wire Interface Data Line
12	LVTTL-O	Mod_Abs	Indicates Module is not present. Grounded in the Module
13	LVTTL-O	Mod_NR	Module Not Ready; Indicating Module Operational Fault
14	LVTTL-O	RX LOS	Receiver Loss of Signal Indicator
15		Gnd	Module Ground
16		Gnd	Module Ground
17	CML-O	RD-	Receiver Inverted Data Output
18	CML-O	RD+	Receiver Non-Inverted Data Output
19		Gnd	Module Ground
20		VCC2	+1.8V Power Supply
21	LVTTL-I	P_Down	Power down; When high, places the module in the low power standby mode and on the falling edge of P Down initiates a module reset.
22		VCC2	+1.8V Power Supply
23		Gnd	Module Ground
24	PECL-I	RefCLK+	Reference Clock Non-Inverted Input, AC coupled on the host board
25	PECL-I	RefCLK-	Reference Clock Inverted Input, AC coupled on the host board
26		Gnd	Module Ground
27		Gnd	Module Ground
28	CML-I	TD-	Transmitter Inverted Data Input
29	CML-I	TD+	Transmitter Non-Inverted Data Input
30		Gnd	Module Ground

[0055] The Mod_NR is an output pin when High, indicates any condition which transmitter or receiver data is not valid. The Mod_NR output pin is an open collector and must be pulled to VCC3 on the host board. A module not implementing Mod_NR shall hold the signal low in the module. The Mod_DeSel is an input pin when held Low by the host, the module respond to 2-wire serial communication commands. The Mod_DeSel allow the use of multiple modules on a single 2-wire interface bus. When the Mod_DeSel pin is high, the module shall not respond to or acknowledge any 2-wire interface communication from the host. Mod_DeSel pin is an open collector and must be pulled to VCC3 in the module. A module not implementing Mod_DeSel shall hold the signal low in the module. Interrupt is an output pin when High indicates possible module operational fault or a status change critical to the host system. The Interrupt pin is an open collector output and must be pulled to VCC3 on the host board. Modules not implementing Interrupt shall hold the pin low in the module.

[0056] When TX_DIS is asserted, "High" turns off the module transmitter output. The TX_DIS pin and must be pulled up to VCC3 on the module board. Mod_ABS is pulled up to VCC3 on the host board and grounded in the module. Mod_ABS is then asserted "High" when the module is physically absent from a host slot. The RX_LOS when held High indicates insufficient optical power for reliable signal reception. The RX_LOS pin is an open collector and must be pulled up to VCC3 on the host board. The P_Down pin, when held High by the host, places the module in the standby mode with a maximum power dissipation of 1.5W. On the negative edge of the P_Down transition a module is reset. The P_Down pin must be pulled up to VCC3 in the module.

[0057] FIG. 5C is a transmitter electrical specification of the interface between the high-speed bit stream interface module of the present invention and a communication ASIC. As is shown in FIG. 5C, the transmitter specifications for the interface between the high-speed bit stream interface module 102A and the communication ASIC 104A are set forth. The PCB 100 upon which the high-speed bit stream interface module 102A and the communication ASIC 104A are mounted is preferably constructed of an FR4 material. However, in some embodiments, the FR4 material is enhanced to provide better performance. The transmitter electrical specification has typically 50 Ohm single-ended output impedance and a 100-Ohm differential output impedance. Output impedance matching is required to be within 10%. The common mode logic output amplitude of the differential output is max 600 microvolts and typically 500 microvolts. Further, the output rise and fall time from 20% to 80% is typically 28 picoseconds with a minimum of 24 picoseconds and a max of 40 picoseconds. The differential output return loss up is maximum -10 dB up to a frequency of 7.5 gigahertz. The single-ended output return loss is maximum -5 dB up to a frequency of 15 gigahertz. The diagram of FIG. 5C is a graph illustrating return loss of the transmitter interface as a function of frequency.

[0058] FIG. 5D is a transmitter jitter specification of the interface between the high-speed bit stream interface module of the present invention and a communication ASIC and also a diagram illustrating how the components of the jitter specification are defined. In particular, FIG. 5D addresses the jitter specification for the high-speed bit stream interface module transmitter operations on its board side. As illustrated in FIG. 5D, the transmitter has a nominal bit rate between 9.95 gigahertz and 10.75 gigahertz. The deterministic jitter produced by the transmitter has typically .12 UI units of maximum .15 UI units. The random jitter produced by the transmitter has typically .13 UI units and maximum .15 UI units. The eye mask for the transmitter is shown in the graph of FIG. 5D and the manner in which the eye mask relates to the specification of the table of FIG. 5D. The SONET jitter (RMS) for the board side interface at up to 80 megahertz is a maximum of 10 milli-units.

[0059] FIG. 5E is a receiver electrical specification of the interface between the high-speed bit stream interface module of the present invention and a communication ASIC and also a diagram illustrating the described return loss characteristics (as a function of frequency). As was the case for the transmitter specs, the single-ended input impedance is 50 Ohms typical and the differential input impedance is 100 Ohms typical. Further, the input impedance match is 10%, the common mode logic input differential amplitude peak-to-peak is minimum 125 mV and the maximum 1000 mV. The differential input return loss as is plotted in the graph of FIG. 5E is -10dB up to 7.5 gigahertz. Further, the single-ended input return loss is -5dB up to 15 gigahertz.

[0060] FIG. 5F is a receiver jitter specification of the interface between the high-speed bit stream interface module of the present invention and a communication ASIC and also a diagram illustrating how the components of the jitter specification are defined. The table and graph of FIG. 5F defines the receiver interface of the high-speed bit stream interface module 102A with regard to the receipt of the bit stream from communication ASIC 104A across the traces of the PCB 100.

[0061] As was the case of the transmitter of the module, the nominal bit rate has a minimum of 9.95 gigahertz and a maximum of 10.75 gigahertz. The deterministic jitter of the receiver is .35 UIs typically and .55 UIs max. The random jitter supported by the receiver is typically .18 UI and maximum .2 UI. The eye mask as is further defined in the graph of FIG. 5F shows the tolerance of the receiver to jitter in the received bit stream from the communication ASIC 104A. Further, the SONET jitter up to 80 megahertz is 30 micro units.

[0062] FIG. 5G is a graph illustrating the frequency response of a connector of the high-speed bit stream interface module in combination with a 4" FR4 trace of the PCB 100 coupling the connector to the communication ASIC. The frequency response as illustrated exhibits attenuation that increases with frequency. This behavior is addressed by the signal conditioning circuit 312 and 306 of the high-speed bit stream interface module 102A. Such signal conditioning is both performed on received signals to open the eye of the receive signals and is also employed on the transmit side of the high-speed bit stream interface module 102A to precondition output signals that are transmitted across the PCB 100 to the communication ASIC 104A. The manner in which signals may be degraded upon receipt is described further with reference to FIGS. 6-9. The signal conditioning circuit that operates upon such RX signals and that operates upon the RX signals to produce compliant TX signals is described further with reference to FIGS. 10-22.

[0063] Jitter is a term that describes the variation in phase of bits of a bit stream signal. Jitter can be divided into main categories: deterministic jitter and non-deterministic jitter. Non-deterministic Jitter (or random jitter, RJ) arises from noise or other transmission related phenomena that can be described only on a statistical basis. In this category fall Gaussian noise related jitter and 1/f noise related jitter, among others. Random jitter cannot be compensated for in any way. The communication ASIC and the TX media have a certain maximum amount of non-deterministic jitter that they can tolerate. Deterministic jitter (DJ), on the other hand, is predictable in nature and some forms of deterministic jitter are such that once the phenomenon that generates this jitter is known it can be compensated. An example of DJ is ISI (inter symbol interference) related jitter. If the bandwidth of a transmission media, e.g., PCB 100 trace, is below the Nyquist rate, ISI will arise and create a certain amount of DJ in the bit stream carried by the PCB 100 trace.

[0064] Two phenomena contribute to limit the bandwidth of board traces and cables. The first is skin effect and the second is dielectric loss. Skin effect dominates the high frequency attenuation in cables. Dielectric loss is the main

cause of bandwidth limitation for board traces. Each of these phenomena alone, or in combination, attenuate high frequency components of the bit stream and introduce group delay variations that cause ISI which degrades the received bit stream adding DJ to the RJ.

[0065] The envelope of the power spectrum of a Pseudo Random Bit Stream (PRBS) signal is described as:

$$PRBS(\omega) \equiv \frac{[\text{Sin}(\frac{\pi f}{\text{Bitrate}})]^2}{[\frac{\pi f}{\text{Bitrate}}]^2} \quad \text{Equation (1)}$$

[0066] When the PRBS signal is sent through a band limited transmission line, such as a trace formed on the PCB 100, the PRBS spectrum is altered resulting into ISI. As will be described further with reference to FIGs. 10-22, the high-speed bit stream interface module 102A, 102B, or 102C of the present invention operates in an attempt to fully restore the power spectrum of the PRBS signal therefore eliminating most, if not all of the ISI. The equalized PRBS signal may then be recovered so that even a large ISI residual will be removed and a maximum jitter tolerance may be met.

[0067] FIGs. 6A through 9B illustrate received bit streams with differing levels of jitter/ISI. FIGs. 6A and 6B are diagrams illustrating a bit stream that has little or no jitter. A bit stream 602 is received at point D or point X by the high-speed bit stream interface module 102A. The bit stream 602 includes both a positive and a negative component since it is received as a differential signal. FIG. 6A illustrates the positive component of the bit stream 602, which is a clean bit stream with no jitter. FIG. 6B illustrates the superimposition of the positive and negative components of the differential bit stream. When the positive and negative components are brought together, eyes are formed, each of which corresponds to a bit of data carried by the bit stream. Eyes 652, 654 and 656 correspond to bits carried during respective bit times. As illustrated, eyes 652, 654 and 656 are evenly distributed and have a substantially equal duration and magnitude. Such is the case because the bit stream 602 has little or no jitter. With such an even distribution, the extraction of data from bit stream 602 is relatively easy.

[0068] FIGs. 7A and 7B illustrate a bit stream having some jitter and amplitude variations and the manner in which the jitter and amplitude variations affect the ability of a receiver to extract data there from. The bit stream 702 of FIG. 7A as compared to the bit stream 602 of FIG. 6A has substantial jitter and some amplitude variation. The bit stream 702 is an NRZ bit stream. Thus, the amplitude will typically vary with time. As shown in FIG. 7B, the positive and negative components of the bit stream 702 are combined to produce eyes 752, 754, and 756 corresponding to respective bit times. Because of the jitter and amplitude variation in the bit stream 702, eyes 752, 754, and 756 have differing durations and/or heights. Extraction of data from the bit stream 702 may therefore be difficult, certainly more difficult than that required for extracting data from the bit stream of FIGs. 6A and 6B.

[0069] FIGs. 8A and 8B illustrate a bit stream having significant jitter and significant amplitude variations and the manner in which the jitter and amplitude variations affect the ability of a receiver to extract data there from. As shown in FIG. 8A, the bit stream 802 has significant jitter and also has variations in its magnitude. When this bit stream is operated upon to create eyes 852, 854, and 856, the eyes are of different duration and are of differing magnitude. In particular, eye 854 is very small in amplitude and short in duration. Thus, extraction of data from the bit stream 802 will be difficult.

[0070] FIGs. 9A and 9B illustrate a bit stream 902 having significant jitter and significant amplitude variations and the manner in which the jitter and amplitude variations preclude a receiver from extracting all carried data from the bit stream 902. As is shown, bit stream 902 includes significant jitter and variations in its magnitude. When the bit stream is operated upon in an attempt to produce eyes in the data, as shown in FIG. 9B, the jitter and magnitude variations are significant enough such that no eye is produced at 954. Thus, this bit stream 902 is of such poor quality that a data bit at position 954 is non-recoverable. The high-speed bit stream interface module 102A (102B or 102C) of the present invention operates to remove deterministic jitter from the bit stream 902 so that data can be extracted from the bit stream.

[0071] FIG. 10 is a block diagram illustrating signal conditioning circuits constructed according to the present invention that service both a TX path and a RX path for a high-speed bit stream interface module constructed according to the present invention. As is shown in FIG. 10, signal conditioning circuit 312 servicing a TX path and signal conditioning circuit 306 servicing a RX path are identical circuits. In such case, each of signal conditioning circuit 312 and signal conditioning circuit 306 includes an input equalizer 1002, a limiting amplifier 1004, a clock and data recovery circuit (CDR) 1006, and an output pre-emphasis circuit 1008. Each of these circuits is controlled by a control circuit 318 that may be programmed by pin settings, a digital interface, e.g., I2C interface, or by another type of interface. Based upon these control inputs, the signal conditioning circuits 312 and 306 will perform signal conditioning commensurate with the respective signal paths they service.

[0072] As is shown, the signal conditioning circuit 312 receives the TX data at point D' on the board side of the high-speed bit stream interface module. As will be described further herein, the programming of the input equalizer 1002,

the limiting amp 1004, the clock and data recovery circuit 1006, and output pre-emphasis circuit 1008 of the signal conditioning circuit 312 depends upon the fact that it resides in the TX path. Alternately, the signal conditioning circuit 306 receives the TX data at point X on the line side of the high-speed bit stream interface module. Thus, the programming of the input equalizer 1002, the limiting amp 1004, the clock and data recovery circuit 1006, and output pre-emphasis circuit 1008 of the signal conditioning circuit 306 depends upon the fact that it resides in the RX path.

[0073] As was illustrated in FIG. 2, ISI jitter is generated from point A to point B and from point C to point D due to band limitations of the copper traces of the PCB 100. Also if the line side media is a copper cable and not an optical fiber, ISI will be present at the receiver input at point X. Thus, according to the present invention, the signal conditioning circuit 312 removes ISI due to bandwidth limitations of the PCB 100 in the TX path. Further, according to the present invention, the signal conditioning circuit 306 removes ISI caused by copper media on the RX path. Because both signal conditioning circuits 306 and 312 use the same integrated circuit, the input equalizer 1002, the limiting amp 1004, and the clock and data recovery circuit 1006 can each be controlled independently depending on the input conditions and application to remove ISI jitter.

[0074] The advantages of such approach are that (1) it allows longer traces on the PCB 100 between C and D and/or cheaper dielectric material for the board construction; (2) it reduces the amount of unfiltered DJ transferred from point C to the transmit point Y; (3) integration of the equalizer 10002, in the same device with the limiting amplifier 1004 and CDR 1006 allows a considerable area saving which is critical in small form factor modules; and (4) the possibility of disabling the operation of the equalizer 1002 and limiting amplifier 1004 independently from the CDR 1006 allows power saving in case they are not needed.

[0075] According to another aspect of the present invention, the output pre-emphasis circuit 1008 is employed to precondition the output bit stream at point A'. Referring to both FIGs. 2-4 and 10, the signal path on the PCB 100 from point A to point B is also subject to the bandwidth limitations of the board traces. Further, because the signal conditioning circuit 306 produces the RX bit stream right before the connector between the module and the PCB 100, the RX bit stream is prone to reflections due to the connector itself at point A'. Reflection of high frequency components of the bit stream, due to the degradation at high frequency of the S11 parameters of the connector itself, generates another form of deterministic jitter that can reduce the system performance. Given a certain connector, with a certain S11 characteristics the higher the frequency content of the data the higher the jitter generated. Hence, depending on the characteristic of connectors and traces a different shaping of the transmitted spectrum is needed.

[0076] Also, the swing requirement is different at point A than it is at point Y. At point A, in the case of short PCB 100 traces, small amplitude can suffice to drive the signal across to the communication ASIC 104C. However, smaller amplitude is actually beneficial because it decreases EMI (electro-magnetic interference). At point Y, larger amplitude is needed to drive the laser or directly the line in case a copper cable is used. Because the Common Mode Logic (CML) drivers of the output of the module 102A drive 50-ohm terminations, halving the driver swing will also half the power dissipation of the driver itself.

[0077] Thus, according to the present invention, the output pre-emphasis circuit 1008 can be programmed with different transmitted signal spectrum shaping settings. Such programming allows the programmability of the output swing of the signal conditioning circuits 306 and 312. Further, the output pre-emphasis conditioning circuit 1008, in the case of poor high frequency reflection response of the connectors at point D', can be programmed in order to reduce the bandwidth of the bit stream. Therefore reflection due to the connector is decreased until the amount of ISI generated by the circuit itself plus the ISI generated by the PCB 100 traces is equal to the ISI generated by reflection in the connector. In the case of good high frequency response of the connector, the output pre-emphasis circuit will be programmed to increase the high frequency content of the transmitted bits stream in order to compensate for high frequency loss along the traces of the PCB 100, thus increasing the maximum supportable trace length.

[0078] If EMI (electro-magnetic interference) due to sharp signal edges is a concern, the output pre-emphasis conditioning circuit 1008 will be used to reduce high frequency content of bit stream traveling on the PCB 100 to the communication ASIC 104A. The output pre-emphasis conditioning circuit 1008 can be disabled and turned off if not needed in order to save power and to reduce head production. This approach is superior to simple pre-emphasis because it considers also the case when it is beneficial to filter to reduce the high frequency content of the transmitted signal.

[0079] Referring FIGs. 2, 3, 4, and 10, the sensitivity requirements for the signal conditioning circuits 306 and 312 at points X and D' are different. If interfacing with optical fiber (as shown in FIG. 3) very small amplitude signal must be detected properly at point X. At point D (and D') instead the bit stream travels from the ASIC across the PCB 100 traces and high sensitivity is not required. The sensitivity of the signal conditioning circuits (306 and 312) is determined by the gain of the limiting amplifier 1004 at the input to the CDR 1006. Generally higher limiting amplifier 1004 gain comes at the cost of higher power consumption. A limiting amplifier 1004 with a sensitivity of few mV accounts for 50% of the power consumption of a signal conditioning circuit (312 or 306). With the same signal conditioning circuit used as either 306 or 312, therefore, power in the limiting amplifier 1004 of signal conditioning circuit 312 is wasted because its required sensitivity is small as compared to the required sensitivity of the limiting amplifier 1004 of signal conditioning

circuit 306.

[0080] According to the present invention, the input sensitivity of the limiting amplifier 1004 is programmable. Therefore, the sensitivity (and power consumption) of the limiting amplifier 1004 may be controlled to find the best use of the signal conditioning circuit 312 or 306 in which the limiting amplifier resides. As will be described further with reference to FIGs. 14, 21, and 22, varying the bias current of the limiting amplifier to change its gain is performed. For example, we will take a limiting amplifier composed of a number of CML buffers as is shown in FIGs. 21 and 22. Each CML buffer provides a small signal gain, which will be proportional to $\sqrt{I_{bias}}$. Therefore decreasing the bias current of each CML stage by half will decrease the overall limiting amplifier sensitivity roughly by 30%.

[0081] Referring again to FIGs. 2-4 and 10, jitter tolerance and jitter transfer requirements are different for the TX path and the RX path. In a Phase Locked Loop (PLL) based single loop CDR 1006, jitter tolerance and jitter generation are related. A certain amount of jitter on the input data will be tracked (or tolerated) up to the PLL bandwidth. Also, up to the PLL bandwidth, all of the jitter that appears at the input will be transmitted to the output. Smaller tracking bandwidth results in a smaller amount of jitter being transferred to the output. However, the tracking bandwidth cannot be so small so that the CDR 1006 is intolerant to jitter within an acceptable jitter range, i.e., will easily lose lock on the receive bit stream.

[0082] Referring particularly to FIG. 2, point X resides at the line side interface. Thus, at point X, jitter tolerance has to be compliant with a supported operating standard, e.g., SONET, Gigabit Ethernet, etc. Thus, for point X, the PLL bandwidth of the CDR 1006 of the signal conditioning circuit 306 is determined by the appropriate operating specification. On the other hand, at point D (D'), data is received from the transmitter of the communication ASIC. In this case a typical communication ASIC system will employ an architecture like the one illustrated in FIG. 5A, in which the ASIC multiplexes and retimes the bit stream using a clean clock. This clean clock produced by the ASIC is obtained by filtering a clock generated in the receiver portion of the communication ASIC transceiver by a very narrow bandwidth PLL. This ASIC clock generation process operates so that the bit stream transmitted by the communication ASIC at point C has a relatively small jitter bandwidth, typically in the order of few KHz. Therefore jitter tracking bandwidth of the TX path signal conditioning circuit 312 is typically considerably smaller than the jitter tracking bandwidth of the RX path signal conditioning circuit 306 for the bit stream received at point X.

[0083] Thus, according to the present invention, the CDR 1006 includes a PLL that has a programmable PLL bandwidth. In such case, the bandwidth of the CDR 1006 PLL in the TX path may be reduced with respect to the CDR 1006 PLL of the RX path until noise generated by the PLL VCO is the dominant noise source. By being able to program the bandwidth of the PLL of the CDR 1006, a reduced amount of ISI jitter picked up from point C to point D via the PCB 100 trace will be transferred to point Y. Further, a reduced amount of noise generated by the VCO in the ASIC transmitter will be transmitted at point Y.

[0084] FIG. 11 is a block diagram illustrating a clock and data recovery circuit constructed according to the present invention. The CDR 1006 receives data in and produces data out. The CDR 1006 includes a PLL 1110 having a phase detector 1102, a charge pump 1104, and a voltage-controlled oscillator (VCO) 1106. The phase detector 1102 receives as its input the data in bit stream and the output of the VCO 1106. The output of the VCO 1106 is also used as a clock input to flip-flop 1108 to synchronize the data out with the output of the VCO 1106.

[0085] According to the present invention, the control circuit 318 controls the bandwidth of the PLL 1110 by controlling the phase detector 1102 gain, the charge pump 1104 current, and the VCO 1106 gain. Referring to FIG. 2, and as previously described above, when separate instances of the CDR 1006 service the TX and the RX path, the TX and RX paths have different requirements with regard to the feed through of jitter from point D to point Y and from point X to point A. Thus, the bandwidth of the PLL 1110 of the CDR 1006 of the signal conditioning circuit 312 is set differently than the bandwidth of the PLL 1110 of the CDR 1006 of the signal conditioning circuit 306. With these settings differing, the manner in which the signal conditioning circuit 312 and the signal conditioning circuit 306 track jitter in their respective bit stream inputs differs as well.

[0086] FIG. 12 is a logic diagram illustrating operations according to the present invention in setting the PLL 1110 bandwidth of the CDRs 1006 of the TX path and RX path signal conditioning circuits 306 and 312. As is generally known, the bandwidth of a PLL 1110 determines the ability of the PLL 1110 to track the phase of an input bit stream. Various operating standards describe the jitter bandwidth of a bit stream that is produced according to the operating standards. Further, devices such as the communication ASIC must also produce bit streams with particular jitter bandwidths. As an example of such characteristics, when the high-speed bit stream interface module supports a SONET line side standard, the phase bandwidth of the stream is approximately 8 megahertz. Further, the communication ASIC includes a multiplexer 504 (shown in FIG. 5) that produces output data having a particular phase bandwidth. An example of such a phase bandwidth is 5-10 kilohertz. In order to operate consistently with a coupled device it is desirable to tune the CDR 1006 of the signal conditioning circuits 312 and 306 of the high-speed bit stream interface module to correspond to the bandwidths of the corresponding data streams. In particular the jitter bandwidth of the operating standard must be met at point X, e.g., 8 MHz. On the other, with the jitter bandwidth of the communication ASIC 1004A multiplexer 504 known, it is desirable not to pass RJ introduced by the PCB 100 trace from point C to point D through

to point Y.

[0087] Thus, according to FIG. 12, operation includes first determining the jitter bandwidth (phase bandwidth of the bit stream) of the line side data (step 1202). Such jitter bandwidth of line side data for example, would be according to the SONET specification approximately 8 megahertz. With this jitter bandwidth determined, operation includes setting the bandwidth of the PLL 1006 of the RX path signal conditioning circuit 306 of FIG. 10. With further reference to FIG. 11, the gain of the PLL 1110 is set by setting the phase detector 1102 gain, the charge pump 1104 current, and the VCO 1106 gain. As is generally known, the bandwidth of the PLL 1110 is a function of the phase detector gain, the charge pump current, and the VCO gain. According to one particular structure of a PLL, the bandwidth of the PLL 1110 is a linear function of each of these inputs. Thus, in the step 1204, the PLL of the clock and data recovery circuit 1006 of the signal conditioning circuit RX path 306 has these parameters set accordingly.

[0088] Next, the method of FIG. 12 includes determining the jitter bandwidth of communication ASIC data received at point D' by signal conditioning circuit 312 of FIG. 10. The multiplexer 504 of the communication ASIC 104A of FIG. 5 determines the jitter bandwidth of the communication ASIC data. Referring again to FIG. 12, once the jitter bandwidth of the communication ASIC data is determined, the bandwidth of the PLL of the clock and data recovery circuit 1006 of the TX signal conditioning circuit 312 is set to substantially match the jitter bandwidth of the communication ASIC multiplexer 504. Setting a PLL within the clock and data recovery circuit 1006 of the TX signal conditioning circuit 312 of FIG. 10 is performed in a similar manner to setting such jitter bandwidth of the PLL of the clock and data recovery circuit 1006 of the RX signal conditioning circuit 306.

[0089] FIG. 13 is a logic diagram illustrating operation according to the present invention in programming an equalizer to compensate for deterministic jitter. As was previously described with reference to FIG. 5A through FIG. 9B, signal paths that carry bit streams will introduce random jitter and deterministic jitter into the bit stream. Random jitter in general cannot be compensated for via an equalization technique. However, deterministic jitter if characterized can be partially overcome via the equalization of the input bit stream by an equalizer 1002 of signal conditioning circuit 312 or 306 for example. Operation according to the present invention commences when the deterministic jitter in a received bit stream is estimated (step 1302). The estimation of deterministic jitter introduced by a given bit stream may be done theoretically or empirically.

[0090] For example, when the communication ASIC 104A and the high-speed bit stream interface module 102A mount upon PCB 100, the link between the high-speed bit stream interface module 102A and communication ASIC 104A will be characterized. Formed on the PCB 100 are an RX trace and a TX trace, each of which has a trace width, a trace depth, a trace distance, a trace path and a trace separation between the other of the TX trace or the RX trace. Further, the PCB 100 has additional board characteristics that will typically affect the propagation characteristics of the RX trace and the TX trace. With a standardized board format such as the FR4 standardized format, the signal propagation characteristics of the traces carrying the RX and TX data may be at least partially characterized. Typically, this characterization will be in the form of a frequency response of the respective trace and/or the manner in which the trace causes inter symbol interference, e.g., channel response, impulse response, etc. In a particular embodiment described herein with reference to FIG. 16, characterization of the signal path of the received bit stream is characterized in the frequency domain. In such case, equalization is also characterized in the frequency domain.

[0091] Operation continues wherein the frequency response of an equalizer that removes some or all of the deterministic jitter in the receive bit stream is determined (step 1304). As will be evident from the FIG. 17, the equalizer settings (that correspond to a linear filter) are determined to invert the deterministic jitter introduced by the signal path over which the bit stream is received. Then, the equalizer is programmed to operate upon the received bit stream to remove some or all of the deterministic jitter (step 1306). For example, equalizer 1002 of signal conditioning circuit 312 servicing the TX path will receive a bit stream from the communication ASIC. The trace carrying the TX data from the multiplexer of the communication ASIC to the equalizer 1002 of the signal conditioning circuit 312 will introduce deterministic jitter. The equalizer 1002 of the signal conditioning circuit 312 of FIG. 10 is therefore programmed at step 1306 to operate upon the received bit stream to remove some or all of the deterministic jitter.

[0092] Likewise, equalizer 1002 of signal conditioning circuit 306 is programmed to remove some or all of the deterministic jitter in the RX bit stream from the line side interface. The line side interface may also be characterized similarly to the manner in which the communication ASIC side of the interface is characterized to determine the deterministic jitter.

[0093] FIG. 14 is a block diagram illustrating one embodiment of an equalizer and a limiting amp of a signal conditioning circuit constructed according to the present invention. As is shown, the equalizer 1002 includes an Automatic Gain Control (AGC) loop 1402, an adaptive equalizer 1404, and an adaptive equalizer feedback 1406. The AGC loop 1402 includes a plurality of variable gain amplifiers 1418 that adjust the amplitude of a received bit stream and a feedback control loop that includes a rectifier 1414 and an integrator 1416. The feedback control loop receives as its input the output of the adaptive equalizer 1404 and controls the gain of the plurality of cascaded variable gain amplifiers 1418.

[0094] Adaptive equalizer 1404 includes a constant gain low pass filter 1410 and a plurality of cascaded tuned am-

plifiers 1408. The structure of the cascaded tuned amplifiers 1408 will be described further with reference to FIG. 15. The adaptive equalizer feedback 1406 includes an integrator 1420 that receives its inputs from separate signal paths, each of which receive as its input the output of the adaptive equalizer 1404. The first signal path includes tuned amplifier 1422, gain stage 1424, and rectifier 1426 and couples to the positive input of the integrator. The second signal path includes tuned amplifier 1428, gain stage 1430, and rectifier 1432 and couples to the negative input of the integrator. The output of the adaptive equalizer 1404 also serves as the input to the limiting amplifier 1004 that includes a plurality of gain stages that will be described further with reference to FIGs. 21 and 22.

[0095] The equalizer 1002 of FIG. 14 operates according to the following principles: (1) The input signal is amplified and its amplitude is held constant by the AGC loop 1402; (2) The output of the AGC loop 1402 is fed to two amplifying paths. A first amplifying path includes a low pass filter 1404 that has a flat band response with a -3dB BW > Nyquist and a second amplifying path that includes either band pass or high pass characteristics.

[0096] As described with reference to FIG. 14, the second path includes the cascaded tuned amplifiers 1408; (3) The two outputs of the two signal paths of the adaptive equalizer 1404 are summed by a variable gain summing circuit 1434 that is controlled by the adaptive feedback equalizer circuit 1406; (4) The power of the signal by the adaptive equalizer 1404 is measured at two frequency points f_1 , f_2 with $f_2 > f_1$ by the adaptive equalizer feedback 1406 (due to tuning of tuned amplifiers 1422 and 1428) and the ratio of the two power $P(f_1)/P(f_2)$ measurements is compared after being separately gained by gain stages 1424 and 1430, respectively. The manner in which this is done is illustrated in FIG. 16 and shows that for a 10 GHz bit stream, these frequencies may be selected as 2 GHz and 5 GHz. The points f_1 and f_2 are referred to as points A and B in FIG. 16. This ratio will indicate the high frequency attenuation in the bit stream. In such example, the tuned amplifier 1422 and 1428 center frequencies are chosen accordingly.

[0097] In the case of an ideal PRBS signal, the ratio will be equal to the reference and the adaptive equalizer 1404 would provide not frequency adjustment. Higher, if the signal is degraded by the low pass effects (high frequency attenuation) of the transmission path, e.g., point C to D, than the ratio will be higher than the reference. The comparison result causes the integrator 1420 to provide a feed back signal that adjusts the variable gain summing circuit 1434. If the PRBS signal high frequency components are degraded, the gain of the high pass path 1408 is increased until the ratio becomes equal to the reference and the high frequency content of the PRBS signal is restored, thus eliminating most of the ISI. In such case, the shape of the spectrum output by the equalizer will match as closely as possible the spectrum of the ideal PRBS signal.

[0098] The equalizer 1002 is a linear equalizer. That means that the processing on the signal is linear. In order for the above system to function properly, the signal must be maintain reasonably linear along the path. Clamping the signal at a rail would distort the signal spectrum and lead to errors in the amount of equalization applied. Therefore the AGC loop 1402 is necessary. The feedback path of the AGC loop 1402 (the rectifier 1414 and the integrator 1416) monitors the signal amplitude at the output of the AGC 1402 and provides feedback to the VGA 1418 via the integrator 1416. The VGA 1418 thus maintains the output amplitude constant based upon the feedback.

[0099] An ideal amplitude detector would be a peak detector capable of detecting the max amplitude and storing it indefinitely. At very high speed any peak detector, due to circuit speed limitations, behaves in reality as a signal energy detector. Considering two PRBS input signals with the same amplitude, with the first transmitted with full Nyquist bandwidth and the second being low-pass filtered, the second signal will result in a lower value, as detected by the amplitude detector. Therefore for this application, signals with the same amplitude but with different loss at high frequency would force the AGC loop 1402 to settle at different amplitude levels for the signals.

[0100] Strongly attenuated signals will actually tend to saturate the AGC loop 1402 and therefore be clamped. This is unacceptable if linear operation of the adaptive equalizer 1404 must be maintained. Thus, according to the present invention, the sensing point of the amplitude detector is moved from the output of the AGC loop 1402 (shown as dotted path A) to the output of the adaptive equalizer 1404 (shown as path B). In doing so, the amplitude detector senses a signal already equalized and the above-described result is precluded.

[0101] The configuration described above consists in two feedback loops sensing at one point X and controlling in two different points, control point Y (at the VGA 1418) and control point Z (at variable gain summing circuit 1434). If both feedback loops have gain in the same frequency range the stability of the whole system would be compromised. Such is not the case with the present invention because the adaptive equalizer 1404 is composed of a first path for the signal which is a flat response buffer (low pass) 1410 with a bandwidth > Nyquist, and a second path which is realized with a cascade of tuned amplifiers 1408. The tuned amplifiers are realized with Common Mode Logic (CML) buffers with inductive loads. The tuned amplifiers have excellent DC rejection and therefore the DC gain of the adaptive equalizer 1404 does not change with the amount of equalization applied. Thus, the adaptive equalizer 1404 doesn't interfere with the AGC loop 1402. The structure of each of these tuned amplifiers is illustrated in FIG. 15.

[0102] FIG. 15 is a schematic diagram illustrating the structure of one of the cascaded tuned amplifiers 1408 of the adaptive equalizer 1404 of FIG. 14. The cascaded tuned amplifier includes a tuned amplifier stage 1502 and a flat band/boost selector stage 1504. Based on a bias input to the tuned amplifier 1502, the tuned amplifier provides a gain of the cascaded tuned amplifier. The flat band/boost selector 1504 receives V_{eqP} and V_{eqN} as the inputs and receives

the output of the tuned amplifier 1502. The flat band/boost selector introduces a boost into the signal path. The characteristics of the tuned amplifier stage 1502 and the flat band/boost selector stage 1504 of the cascaded tuned amplifier 1408 illustrated (as well as of the characteristics of the constant gain low pass filter 1410) are determined based upon the bit rate of the serviced bit stream and also the expected manner in which the serviced bit stream is affected by the PCB on the board side and/or the media on the line side. The manner in which this is performed is straightforward.

[0103] FIG. 16 is a graph illustrating the theoretical power spectrum of a Pseudo Random Bit Stream signal (PRBS) and the power spectral density of a PRBS signal with high frequency attenuation. Referring back to FIG. 13, at step 1302, it was required that the deterministic jitter in a receive bit stream is estimated. One technique for doing such estimation is to compare the power spectrum of a received pseudo random bit stream with the theoretical power spectrum of a pseudo random bit stream. Such determination may be done by looking at magnitudes of the power spectrum at particular frequencies, e.g., at points A and B of the theoretical power spectrum of the PRBS. Then, the actual magnitudes of the attenuated PRBS power spectrum at points A' and B' on the frequency spectrum are also determined. Based upon the relationship of A' and B' to A and B, the high frequency attenuation of the pseudo random bit stream is determined. This high frequency attenuation corresponds significantly to the deterministic jitter in the receive bit stream. As was previously described with reference to FIG. 14, the adaptive equalizer feedback 1406 uses this relationship as feedback to the adaptive equalizer 1404. The adaptive equalizer 1404 uses this feedback to adjust its frequency response.

[0104] FIG. 17 is a graph illustrating various signal path attenuation properties and equalizer frequency responses corresponding to the signal path attenuation properties. As illustrated in FIG. 17, one signal path attenuation characteristic is addressed via equalizer setting 1. Further, another signal path attenuation setting is addressed by equalizer setting 2. Finally, a third signal path attenuation setting is addressed by equalizer setting 3. As is evident, appropriate equalizer settings will partially/fully invert the frequency response to produce a desired frequency response for any high frequency attenuation caused by the signal path. Such a desired frequency response is shown.

[0105] FIG. 18 is a logic diagram illustrating operation according to the present invention in determining pre-emphasis circuit settings for a particular signal path and connector combination. Operation commences wherein the frequency response of a combined connector and signal path are determined (step 1802). For example, one combination of signal path and connector relate to the RX path serviced by the high-speed bit stream interface module 102A. Such connector and signal path couple the high-speed bit stream interface module 102A to the PCB 100 for further coupling the signals to the communication ASIC 104A. The connector in the PCB 100 board trace have there own unique signal propagation characteristics. Thus, at step 1802, the combined characteristics of this signal path are determined.

[0106] Likewise, at step 1802, the frequency response of a connector and a signal path may also be determined for the line interface of the high-speed bit stream interface module 102A. Once the frequency response of the connector and signal paths are determined, operation proceeds to step 1804 in which pre-emphasis circuit settings that will be employed by the pre-emphasis circuit are determined. As was the case of the equalizer 1002, the output pre-emphasis circuit 1008 settings are intended to pre-emphasize the signal to compensate for signal path characteristics. Once these output pre-emphasis circuit settings are determined, the output pre-emphasis circuit 1008 is programmed to pre-emphasize the signal to pre-compensate for the frequency response of the connector and signal path. Referring back to FIG. 10, output pre-emphasis circuit 1008 of signal conditioning circuit 312 is programmed to compensate for at least the line side connector. Likewise, output pre-emphasis circuit 1008 of signal conditioning circuit 306 is programmed to compensate for the characteristics of the connector and trace that couple the signal conditioning circuit 306 to the communication ASIC. The output pre-emphasis circuit 1008 may be constructed as a linear filter having a frequency response whose settings are selected by the control circuit 318 based upon the particular installation.

[0107] FIG. 19 is a graph illustrating various frequency responses of the connection between the high-speed bit stream interface module 102A and the communication ASIC 104A of the PCB 100. The combination of the interconnection between the high-speed bit stream interface module 102A and the communication ASIC 104A includes the connector for the module 102A and the PCB 100 trace between the connector and the communication ASIC 104A. Three separate frequency response curves are shown in FIG. 19. A first frequency response curve illustrates a poor connector and a good trace. A second frequency response curve illustrates frequency response for an average connector and an average trace. Finally, a third frequency response curve illustrates the frequency response for a good connector in a poor trace. Based upon the frequency response of the signal path that will be addressed, the output pre-emphasis circuit 1008 of the signal conditioning circuit 306 will be programmed to precondition the signal in an inverted manner. By preconditioning the signal in a manner inverted to the frequency response of the signal path, theoretically, the signal will be received to have a spectrum corresponding to the PRBS spectrum.

[0108] Likewise, the output pre-emphasis circuit 1008 of the signal conditioning circuit 312 may be programmed to pre-compensate for the connector to the line side media and/or for to pre-compensate for the line side media itself. In this fashion, the preconditioned signal, after having been transmitted across the connector and/or the media will have a spectrum more similar to the PRBS spectrum than it would otherwise have. As the reader should appreciate, when a copper media is used on the line side, more preconditioning would typically be required than when an optical media

is used.

[0109] Also shown in FIG. 19 is a desired frequency response for a received bit stream at the far end of connector/media or connector/trace being serviced. The frequency axis of FIG. 19 is not labeled. Such is the case because each particular connector/media or connector/trace will typically have a different frequency response. Further, this frequency response will typically be more complex than that as shown in FIG. 19. Thus, the graph of FIG. 19 is illustrative only. However, the teachings of the present invention provided partially by FIG. 19 will cause the design of an integrated circuit incorporating such teachings to be straightforward to one of skill in the art.

[0110] FIG. 20 is a logic diagram illustrating operation according to the present invention in programming the dynamic range of a limiting amplifier of the signal conditioning circuit of the present invention. Because the signal conditioning circuit of the present invention is employed both in the TX path and the RX path of the high-speed bit stream interface module 102A of FIG. 1, it must operate upon input bit streams having significantly different dynamic ranges. For example, when the signal conditioning circuit is employed to service the RX signal path of the high-speed bit stream interface module 102A such as a signal conditioning circuit 306 of FIG. 10 illustrates, the input signal will be of a relatively low dynamic range. Further, when the signal conditioning circuit 312 of FIG. 10 is employed to service the TX path of the high-speed bit stream interface module 102A, the input signal has a relatively larger dynamic range. However, because the structure of the signal conditioning circuit is the same for both implementations, the limiting amp 1004 of the signal conditioning circuit must be capable of accepting varying different dynamic ranges.

[0111] Thus, according to the operation of FIG. 20, the limiting amp is programmed for its intended purpose. As a first operation, the dynamic range of the input signal is first determined (step 2002). Then, based upon the dynamic range of the input signal as expected, the input gain required for the input signals is determined (step 2004). Finally, the limiting amplifier is programmed to provide an input gain corresponding to the expected dynamic range on the input signal (step 2006).

[0112] FIG. 21 is a block diagram illustrating a limiting amp 1004 constructed according to the present invention. As is shown, the limiting amp 1004 includes a plurality of CML stages 2102A-2102F. Each of these CML stages 2102A-2102F receives a respective gain select signal. This gain select signal is employed to determine the gain for the respective stage. In the embodiment of FIG. 21, the control circuit 318 provides the gain select signal, with such control signal potentially differing for the signal conditioning circuit 306 as compared to the control signal provided to signal conditioning circuit 312.

[0113] FIG. 22 is a schematic diagram illustrating a common mode logic stage of the limiting amplifier 1004 of the signal conditioning circuit 312 or 306. The CML stage 2102A-2102F of FIG. 22 is cascaded with other CML stages as is illustrated in FIG. 21. The control signal for the CML stage illustrated in FIG. 22 is employed to set the I_{bias} current for the stage. As is generally known, the gain of such a CML stage is proportioned to the square root of the I_{bias} for the stage. Thus, the gain select signal as provided by the control circuit illustrated in FIG. 10 will determine the particular gain for the CML stage.

[0114] The invention disclosed herein is susceptible to various modifications and alternative forms. Specific embodiments therefore have been shown by way of example in the drawings and detailed description. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the invention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the claims.

Claims

1. A high-speed serial bit stream interface that communicatively couples a line side media to a communication Application Specific Integrate Circuit (ASIC), the high-speed serial bit stream interface comprising:

a line side interface that communicatively couples to the line side media, that receives an RX signal therefrom, and that transmits a TX signal thereto;
 a board side interface that communicatively couples to the communication ASIC, that receives the TX signal therefrom, and that transmits the RX signal thereto;
 a signal conditioning circuit communicatively coupled between the line side interface and the board side interface;

wherein the signal conditioning circuit receives the RX signal from the line side interface, conditions the RX signal, and provides the RX signal to the board side interface, wherein the signal conditioning circuit is controllable to spectrally shape the RX signal; and

wherein the signal conditioning circuit receives the TX signal from the board side interface, conditions the TX signal, and provides the TX signal to the line side interface,

wherein the signal conditioning circuit is controllable to spectrally shape the TX signal.

2. The high-speed serial bit stream interface of claim 1, wherein the RX signal and the TX signal each comprise a single high-speed serial bit stream.

3. The high-speed serial bit stream interface of claim 1, wherein:

the signal conditioning circuit spectrally shapes the RX signal using first spectral shaping control settings; and
the signal conditioning circuit spectrally shapes the TX signal using second spectral shaping control settings.

4. The high-speed serial bit stream interface of claim 3, wherein:

the first spectral shaping control settings are determined based upon the spectral shape of the RX signal prior to conditioning relative to reference spectral characteristics; and
the second spectral shaping control settings are determined based upon the spectral shape of the TX signal prior to conditioning relative to reference spectral characteristics.

5. The high-speed serial bit stream interface of claim 4, wherein:

the signal conditioning circuit determines the second spectral shaping control settings based upon a ratio of a first spectral component of the RX signal to a second spectral component of the RX signal; and
the signal conditioning circuit determines the second spectral shaping control settings based upon a ratio of a first spectral component of the TX signal to a second spectral component of the TX signal.

6. The high-speed serial bit stream interface of claim 3, wherein:

the signal conditioning circuit automatically determines the first spectral shaping control settings; and
the signal conditioning circuit automatically determines the second spectral shaping control settings.

7. The high-speed serial bit stream interface of claim 1, wherein the signal conditioning circuit spectrally shapes the TX signal to remove deterministic jitter from the TX signal.

8. The high-speed serial bit stream interface of claim 1, wherein the signal conditioning circuit spectrally shapes the TX signal to remove inter symbol interference from the TX signal.

9. The high-speed serial bit stream interface of claim 1, wherein:

the signal conditioning circuit spectrally shapes the TX signal to remove deterministic jitter from the TX signal;
and
the signal conditioning circuit spectrally shapes the RX signal to remove deterministic jitter from the RX signal.

10. The high-speed serial bit stream interface of claim 1, wherein the signal conditioning circuit comprises:

an RX signal path that operates upon the RX signal; and
a TX signal path that operates upon the TX signal.

11. The high-speed serial bit stream interface of claim 1, wherein the signal conditioning circuit further comprises:

output pre-emphasis circuit that controllably modifies the spectrum of its serviced signal to pre-compensate for the spectral characteristics of a signal path upon which the serviced signal will be output; and

wherein the output pre-emphasis circuitry servicing the RX signal and the output pre-emphasis circuitry servicing the TX signal are separately controlled to produce differing pre-compensation operations of the RX signal and for the TX signal.

12. The high-speed serial bit stream interface of claim 1, wherein the signal conditioning circuit further comprises:

a limiting amplifier that receives the respective serviced signal and that controllably amplifies the respective

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served signal to produce the respective serviced signal in a desired output range; and

wherein the limiting amplifier servicing the RX signal and the limiting amplifier servicing the TX signal are separately controlled to produce respective serviced signals in the desired output range.

5

13. The high-speed serial bit stream interface of claim 1, wherein the signal conditioning circuit further comprises:

10

a clock and data recovery circuit having an adjustable Phase Locked Loop (PLL) bandwidth that communicatively couples to the output of the limiting amplifier and receives, recovers, and reclocks the respective serviced signal; and

15

wherein the PLL bandwidth of the clock and data recovery circuit servicing the RX signal and the PLL bandwidth of the clock and data recovery circuit servicing the TX signal are separately controlled based upon respective serviced signal characteristics.

14. A high-speed serial bit stream conditioning circuit comprising:

20

an adaptive equalizer that receives a high-speed serial bit stream and that spectrally shapes the high-speed serial bit stream to produce an equalized high-speed serial bit stream; and
a clock and data recovery circuit operably coupled to the output of the adaptive equalizer that recovers the equalized high-speed bit stream to produce an output high-speed serial bit stream.

15. The high-speed serial bit stream conditioning circuit of claim 14, wherein:

25

the adaptive equalizer automatically determines spectral shaping control settings; and
the adaptive equalizer uses the spectral shaping control settings to spectrally shape the high-speed serial bit stream such that the spectral characteristics of the equalized high-speed serial bit stream substantially correspond to reference spectral characteristics.

30

16. The high-speed serial bit stream conditioning circuit of claim 15, wherein the spectral shaping control settings comprise at least one filter setting and at least one gain setting.

17. A method for equalizing a high-speed serial bit stream comprising:

35

receiving the high-speed serial bit stream;
spectrally shaping the high-speed serial bit stream based upon spectral shaping control settings; and
adjusting the spectral shaping control settings so that the spectral characteristics of the high-speed serial bit stream substantially correspond to reference spectral characteristics.

40

18. The method of claim 17, wherein the spectral shaping control settings comprise at least one filter setting and at least one gain setting.

19. The method of claim 17, wherein the spectral shaping control settings are determined by:

45

determining a first spectral component of the high-speed serial bit stream;
determining a second spectral component of the high-speed serial bit stream; and
determining the spectral shaping control settings based upon a ratio of the first spectral component and the second spectral component.

50

20. The method of claim 17, wherein the spectrally shaping the high-speed serial bit stream removes deterministic jitter from the high-speed serial bit stream.

55

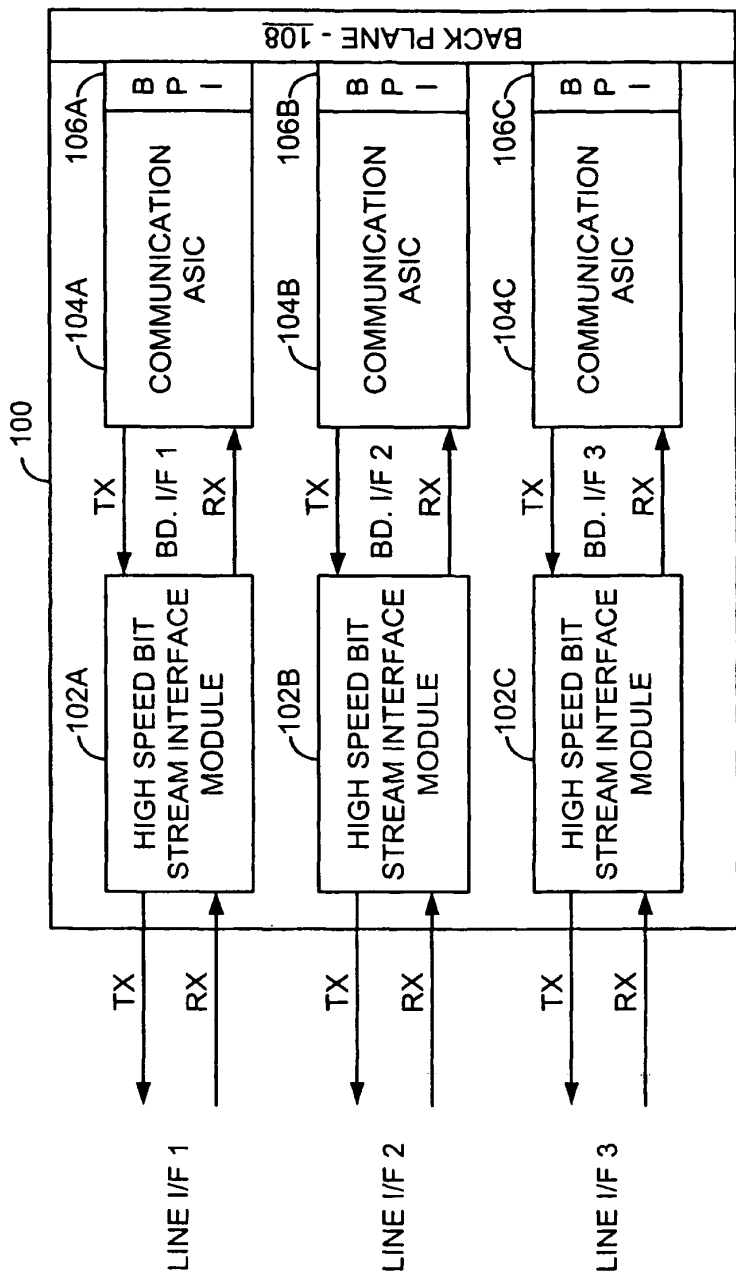


FIG. 1

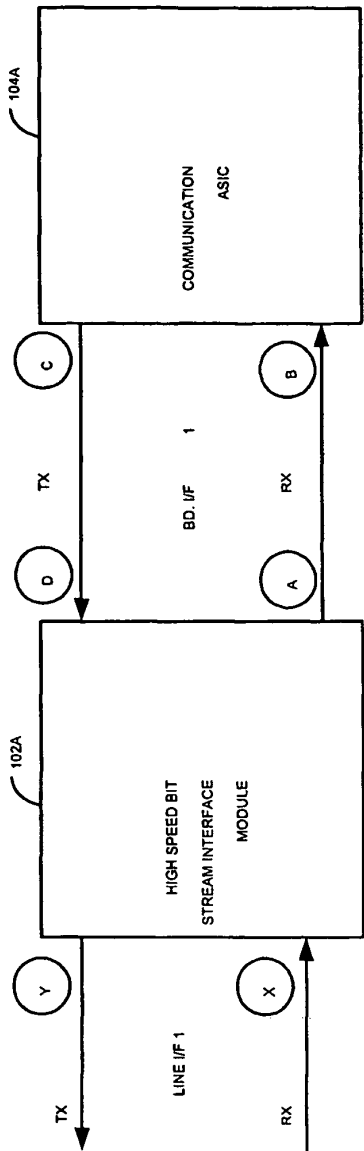


FIG. 2

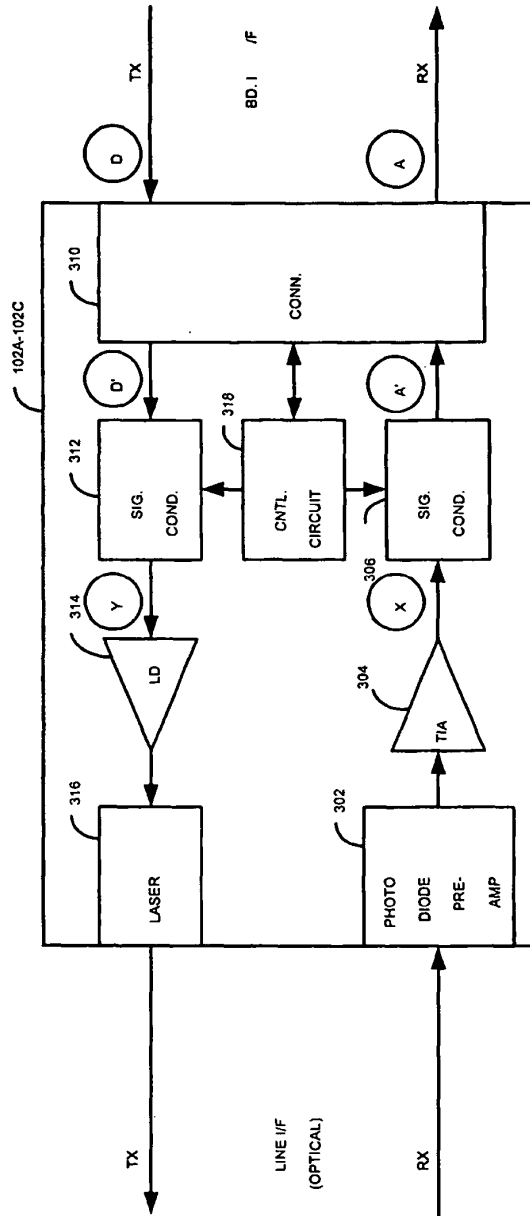


FIG. 3

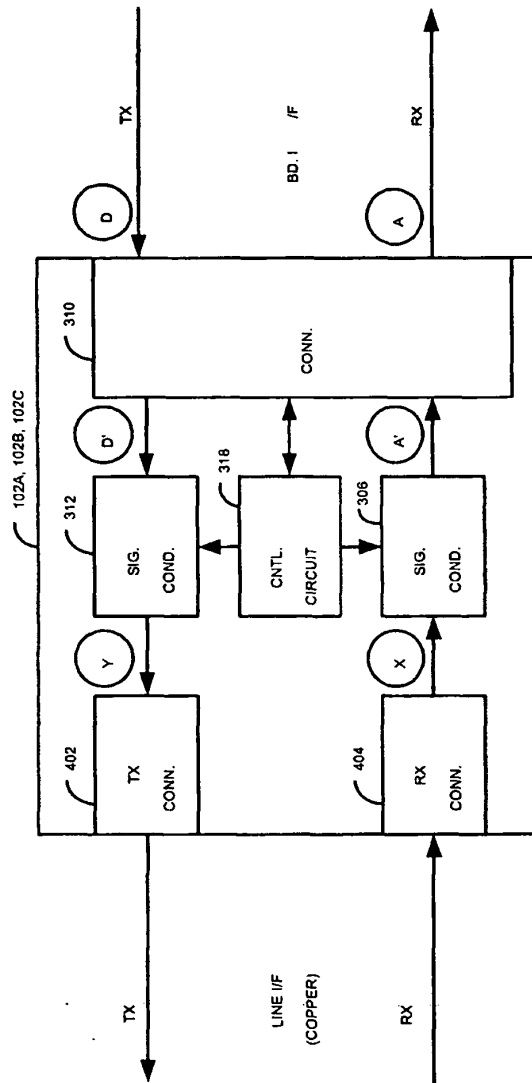


FIG. 4

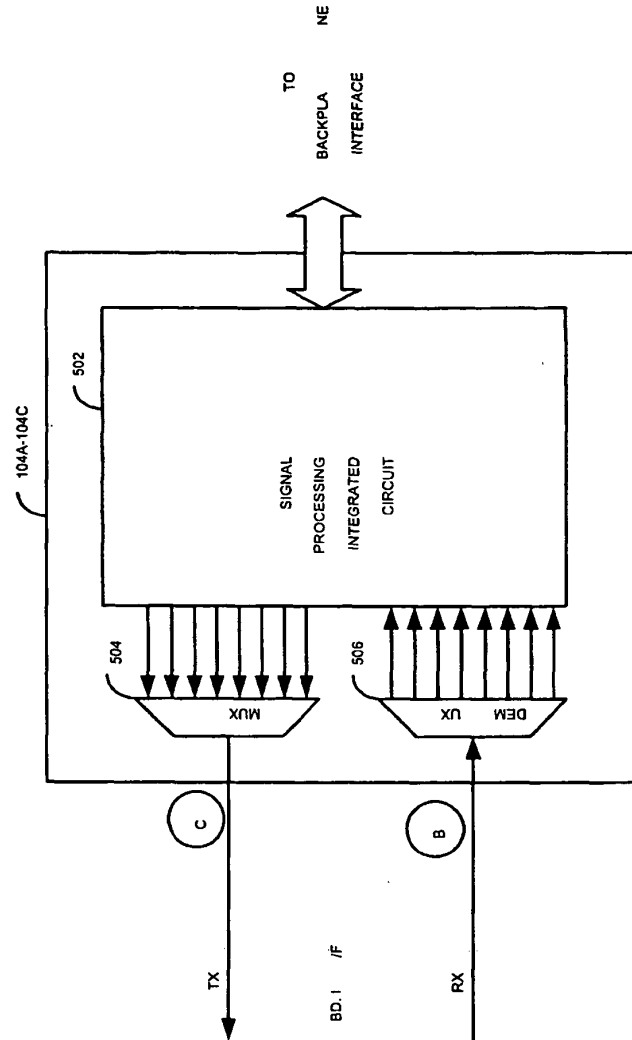


FIG. 5A

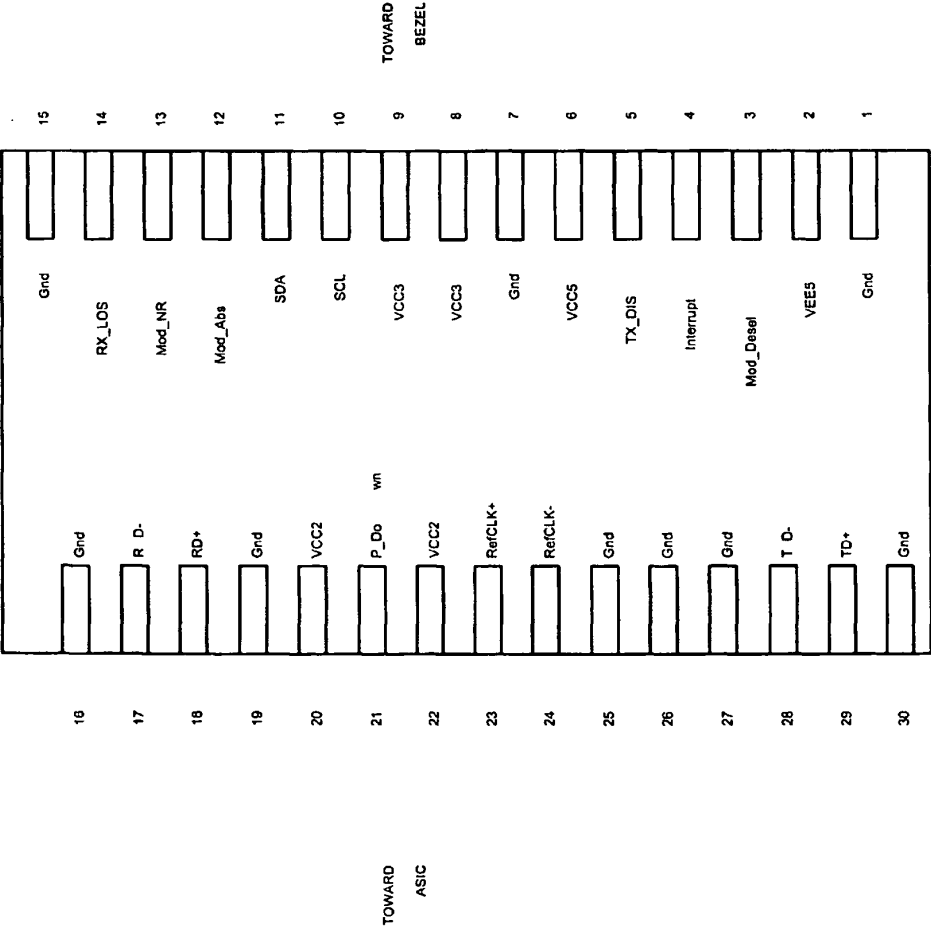


FIG. 5B

Parameter (Transmitter)	Symbol	Conditions	Min	Typ	Max	Units
Single Ended Output Impedance	Z_{in}		40	50	60	Ω
Differential Output Impedance	Z_o		80	100	120	Ω
Output Impedance Match	Z_{in}				10	%
CML output Amplitude, Diff., P-P	ΔV_{QDO}			500	600	mV
Output Rise and Fall time (20% to 80%)	t_{RH}, t_{FH}					ps
			24	28	40	
Differential output return loss up	S11	Up to 7.5 GHz			-10	dB
		7.5-15 GHz			*	dB
Single Ended output return loss	S11	Up to 15 GHz			-6	dB

* $RL = -10 + 16.6 \text{ Log}(f/7.5)$

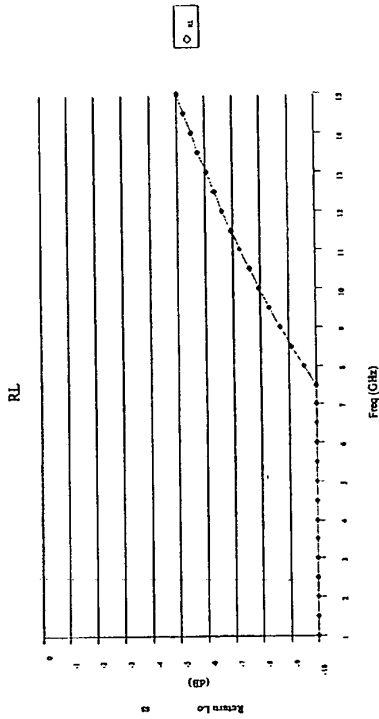


FIG. 5C

Parameter (Transmitter)	Symbol	Conditions	Min	Typ	Max	Units
Nominal Bit Rate	f		9.95		10.75	GHz
Deterministic Jitter	DJ	MIS/802.3ae		0.12	0.15	UI
Random Jitter	RJ	MIS/802.3ae		0.13	0.15	UI
Eye Ma sk	X1				0.15	UI
Eye Ma sk	X2				0.4	UI
Eye Ma sk	Y1				200	mV
Eye Ma sk	Y2				300	mV
SOENT Jitter (RMS)		Up to 80 MHz			10	mU

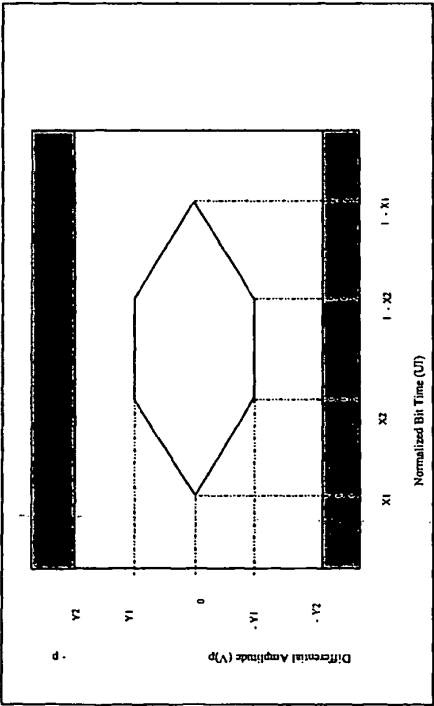


FIG. 5D

Parameter (Receiver)	Symbol	Conditions	Min	Typ	Max	Units
Single Ended Input Impedance	Z_{in}		40	50	60	Ω
Differential Input Impedance	Z_{in}		80	100	120	Ω
Input Impedance Match	Z_{in}				10	%
CML Input Differential Ampl., p-p	ΔV_{QDO}		125		1000	mV
Differential Input Return Loss	S22	Up to 7.5 GHz			-10	dB
		7.5-15 GHz			-1	dB
Single Ended Input Return Loss	S22	Up to 15 GHz			-5	dB

1. $RL = (0 - 16.6 \text{ Log}(f/7.5))$
2. Single ended return loss is necessary for EML.

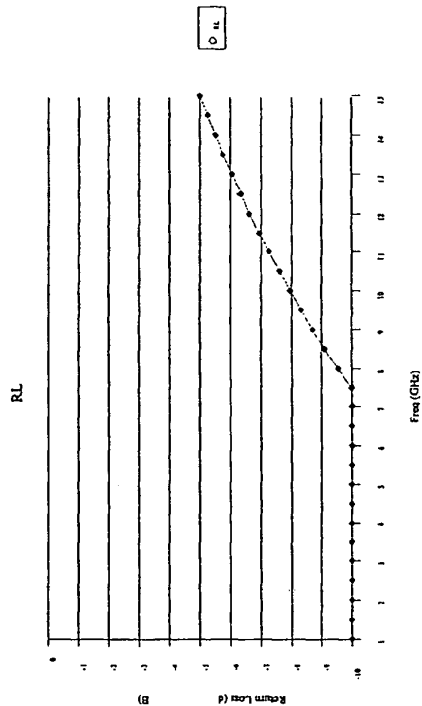


FIG. 5E

Parameter (Receiver)	Symbol	Conditions	Min	Typ	Max	Units
Nominal Bit Rate	f		9.95		10.75	GHz
Deterministic Jitter *	DJ	MIS/802.3ae		0.35	0.55	UI
Random Jitter	RJ	MIS/802.3ae		0.18	0.2	UI
Eye Ma sk	X1				0.35	UI
Eye Ma sk	Y1				62.5	mV
Eye Ma sk	Y2				500	mV
SOENT Jitter		Up to 80 MHz			30	mU

* 0.25 UI of DJ is allocated to ISI from 8" of FR4 PCB trace.

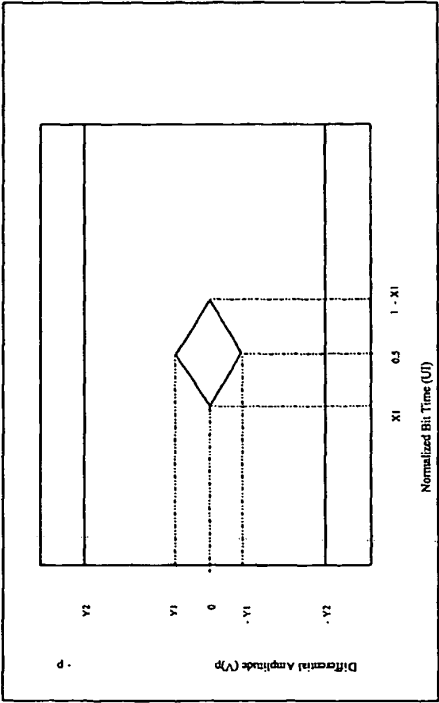


FIG. 5F

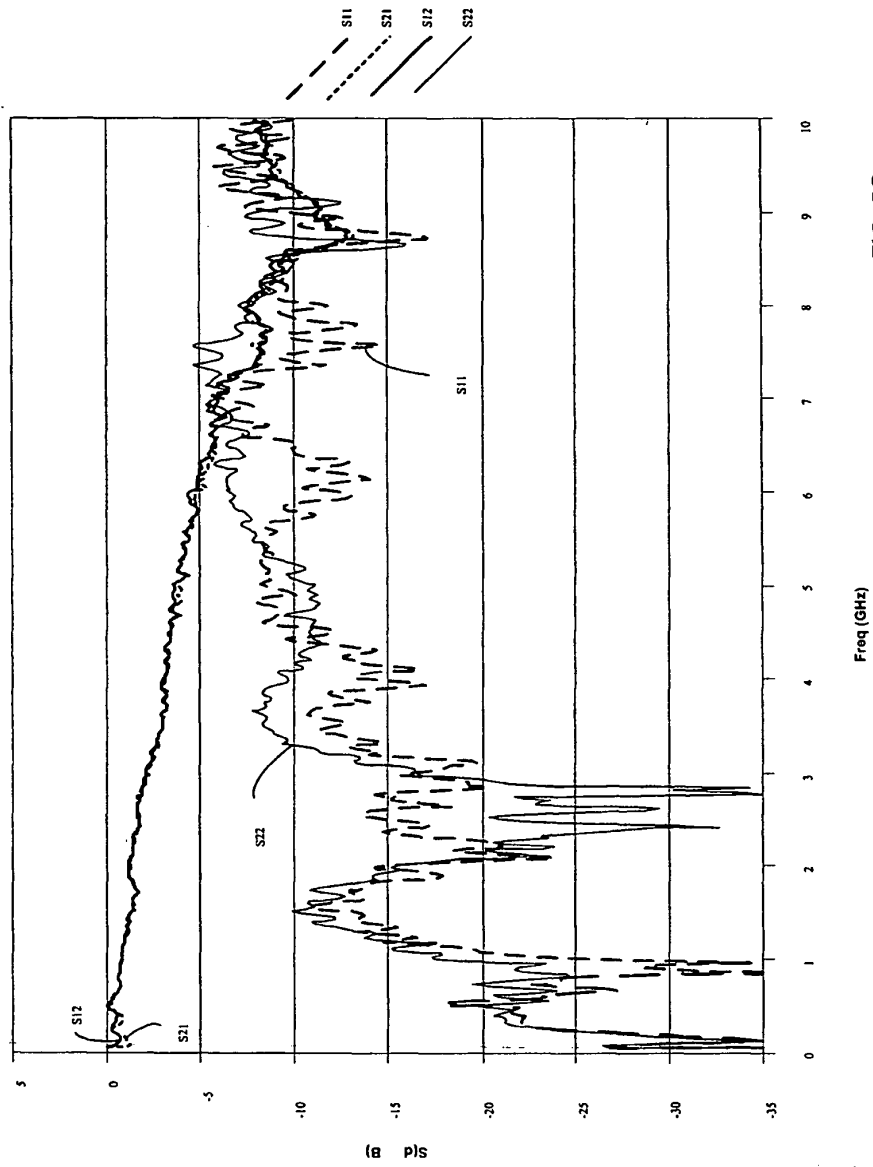


FIG. 5G

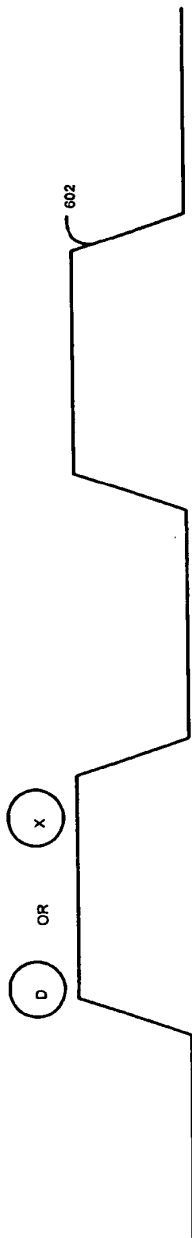


FIG. 6A

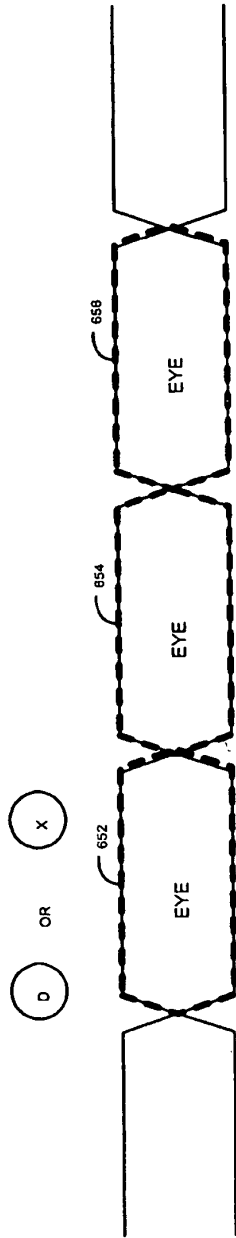


FIG. 6B

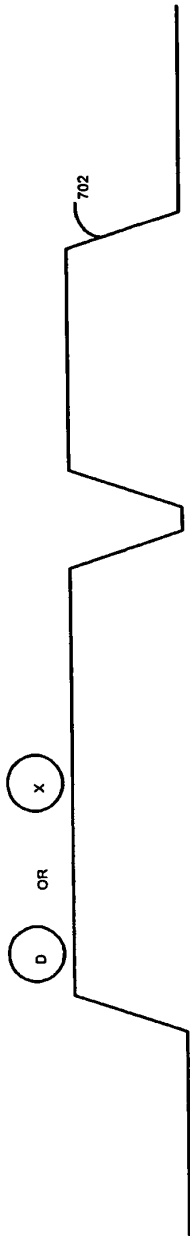


FIG. 7A

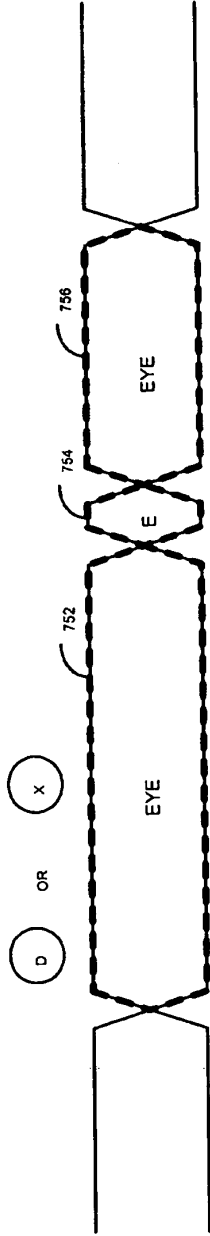


FIG. 7B

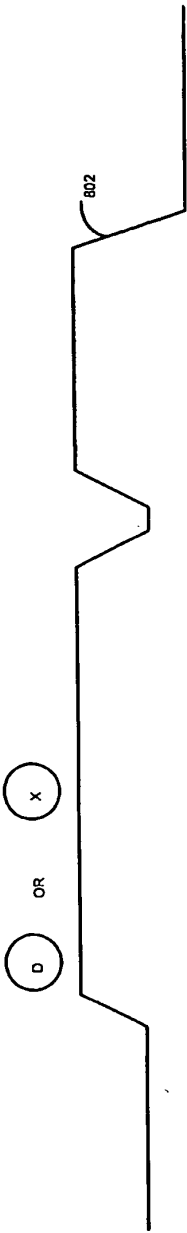


FIG. 8A

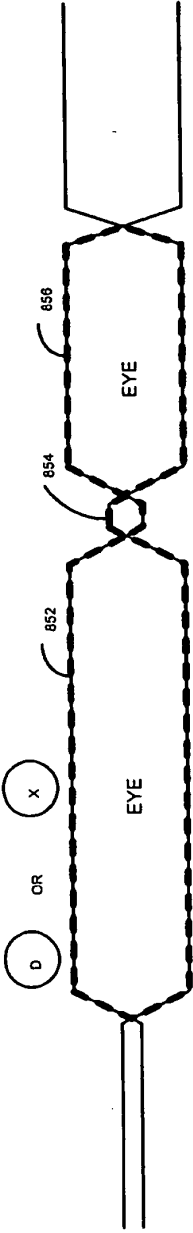


FIG. 8B

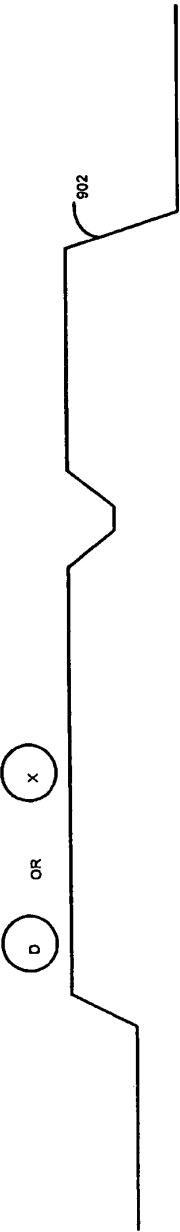


FIG. 9A

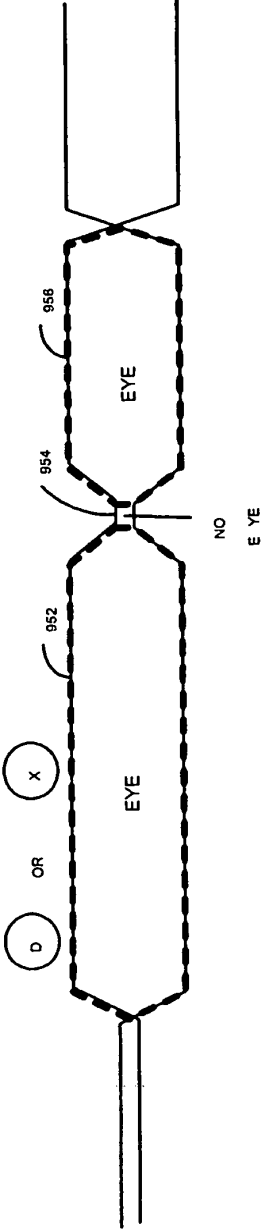


FIG. 9B

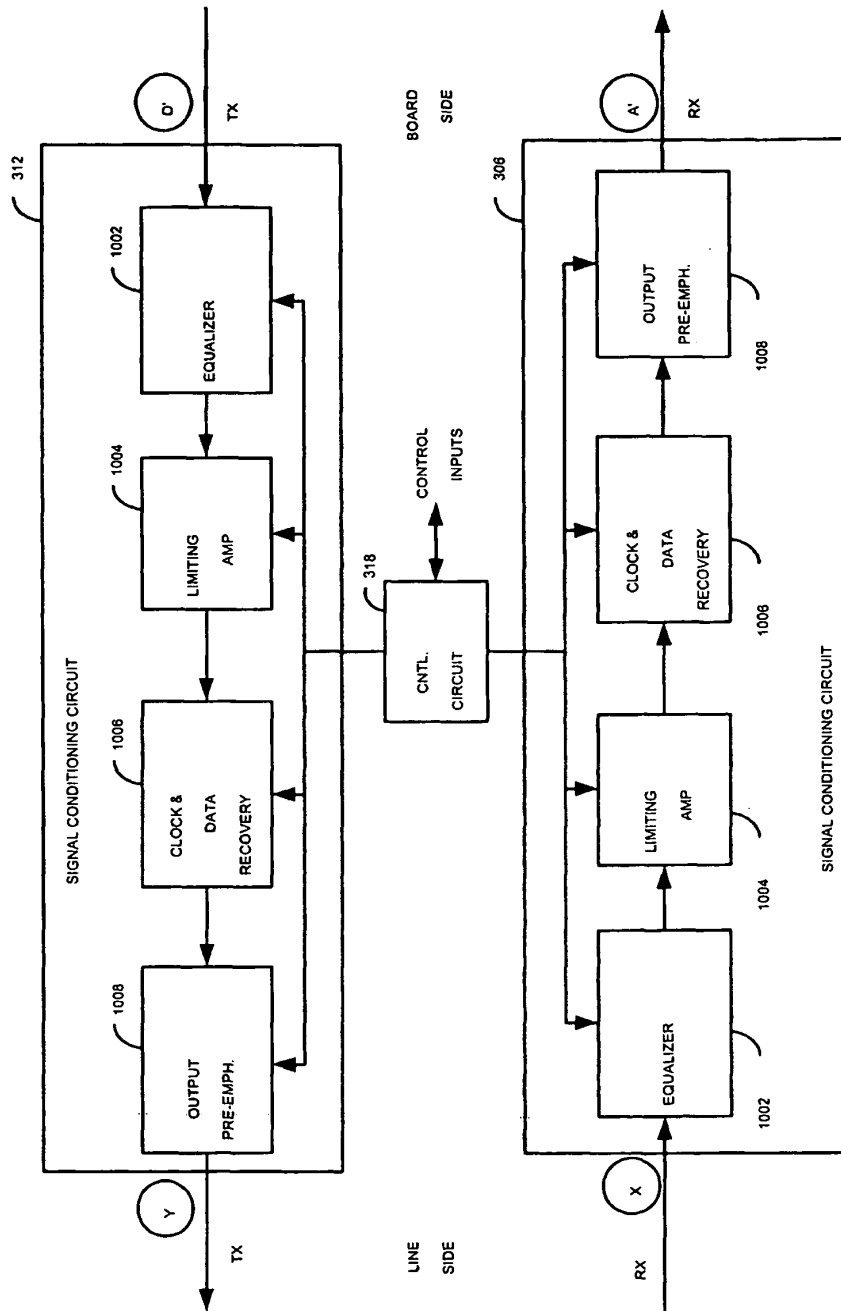


FIG. 10

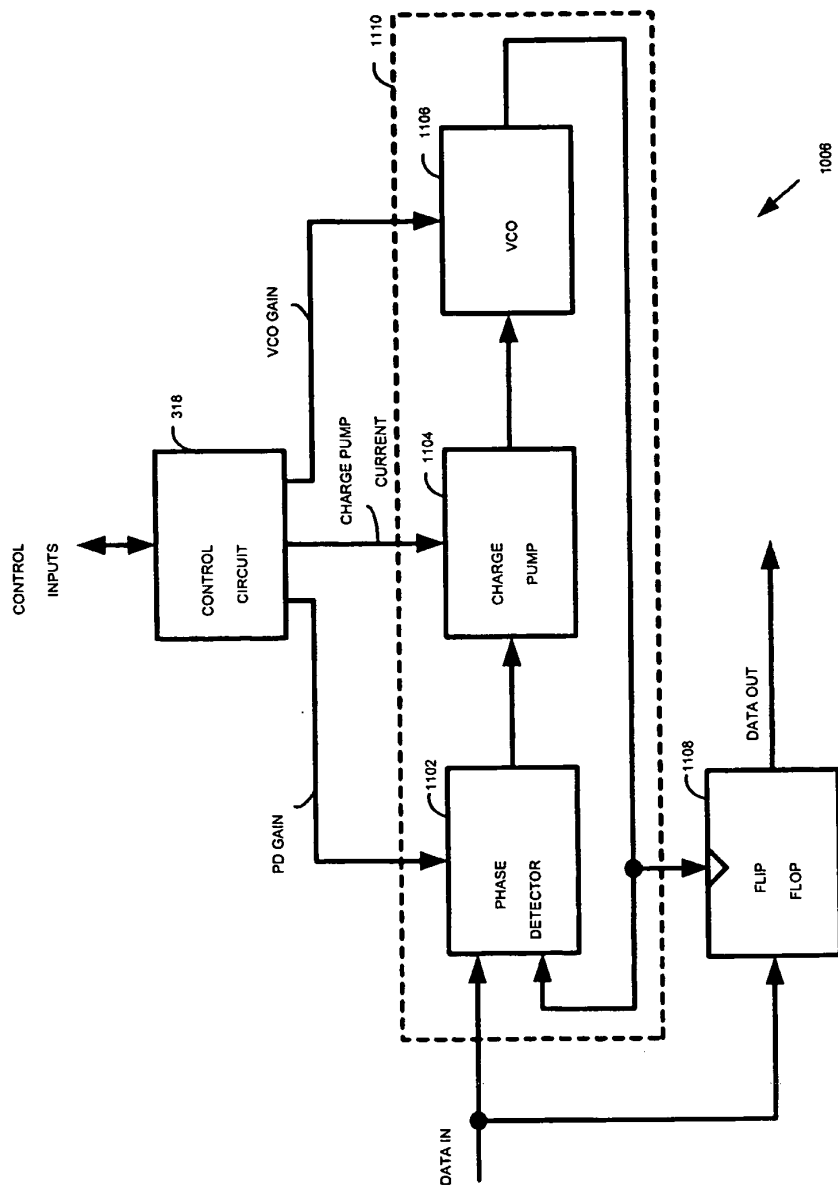


FIG. 11

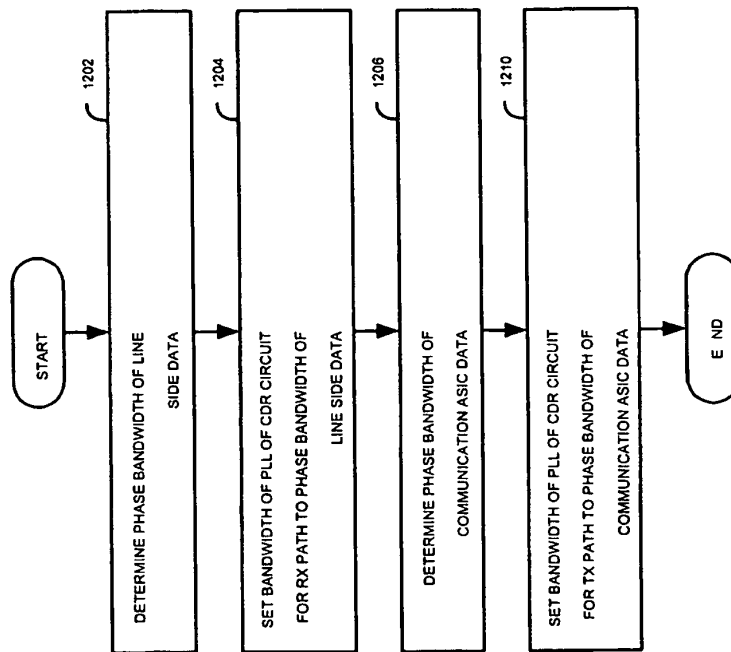


FIG. 12

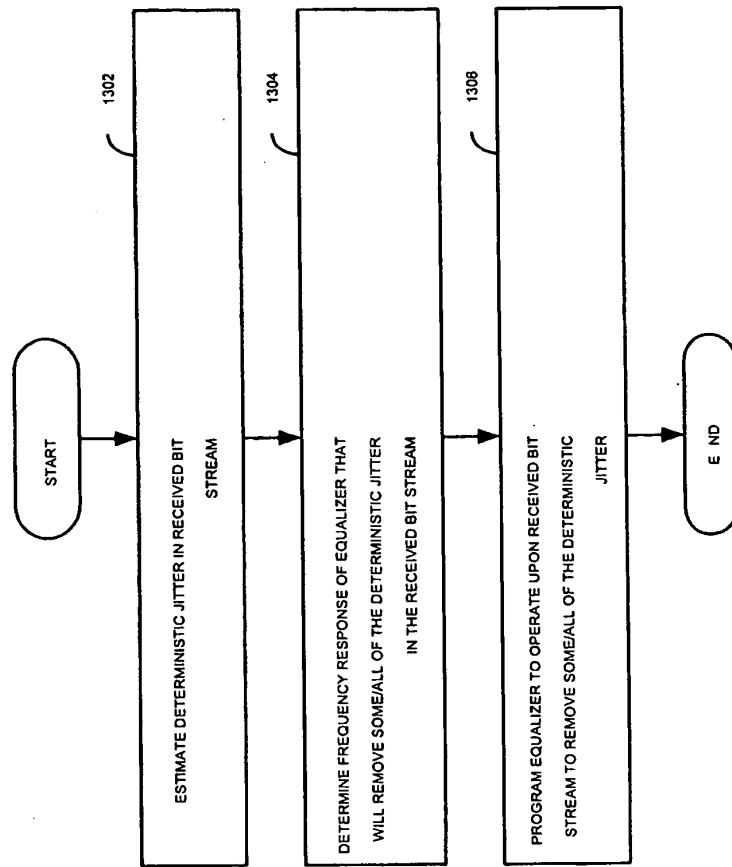


FIG. 13

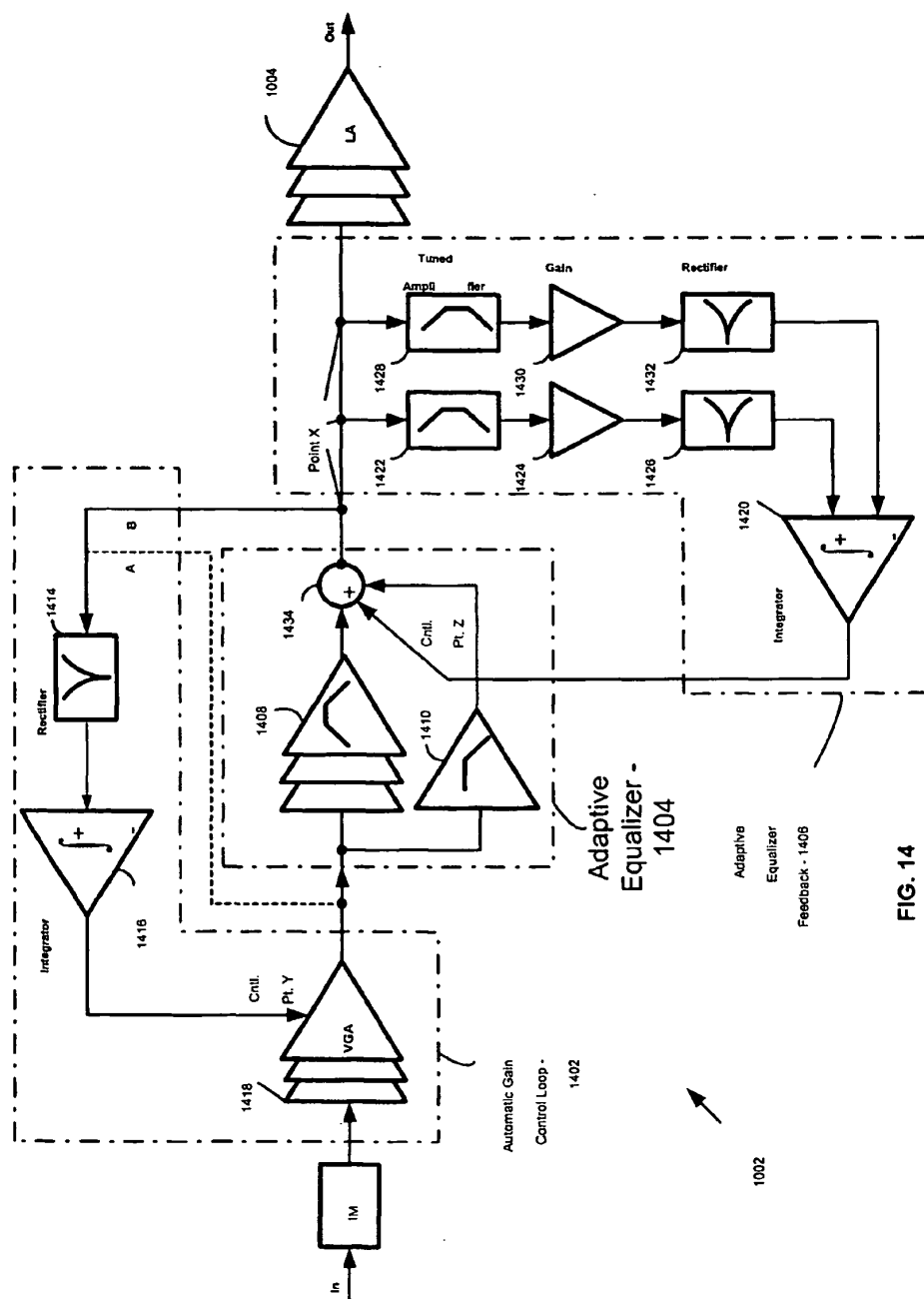


FIG. 14

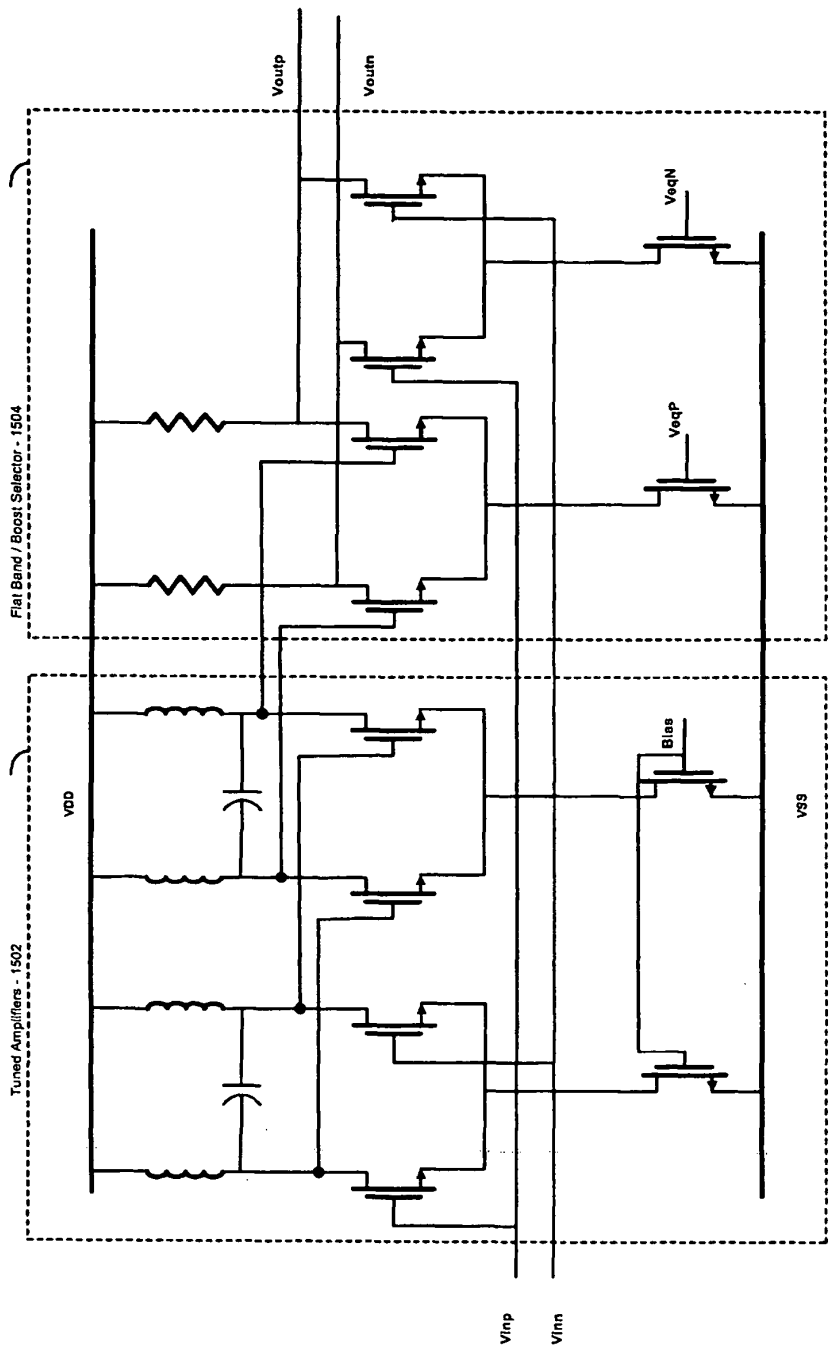


FIG. 15

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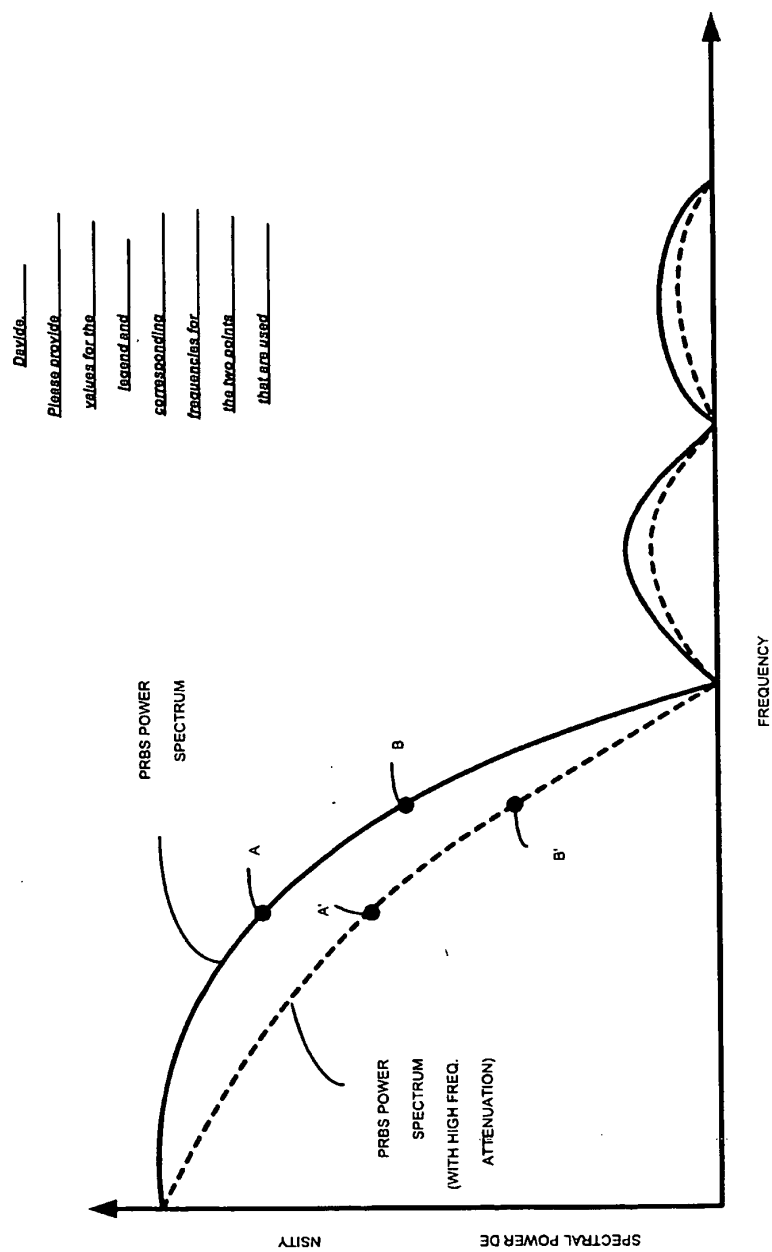


FIG. 16

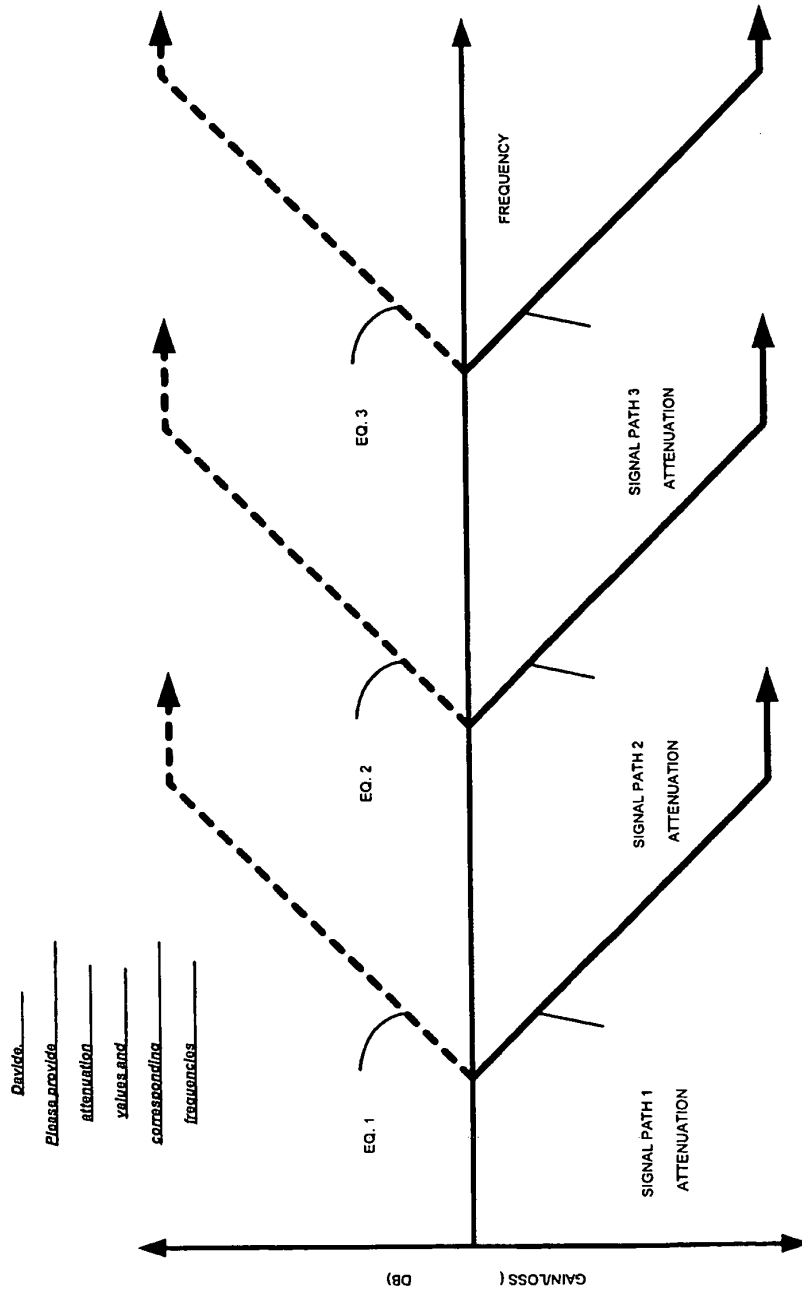


FIG. 17

Provide
 Please provide
 attenuation
 values and
 corresponding
 frequencies

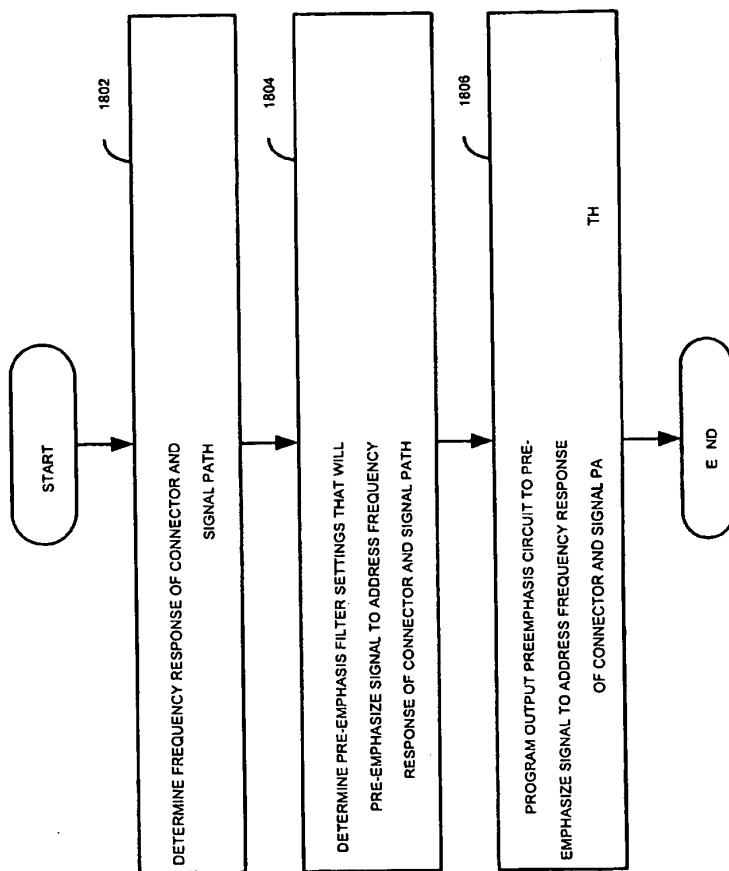


FIG. 18

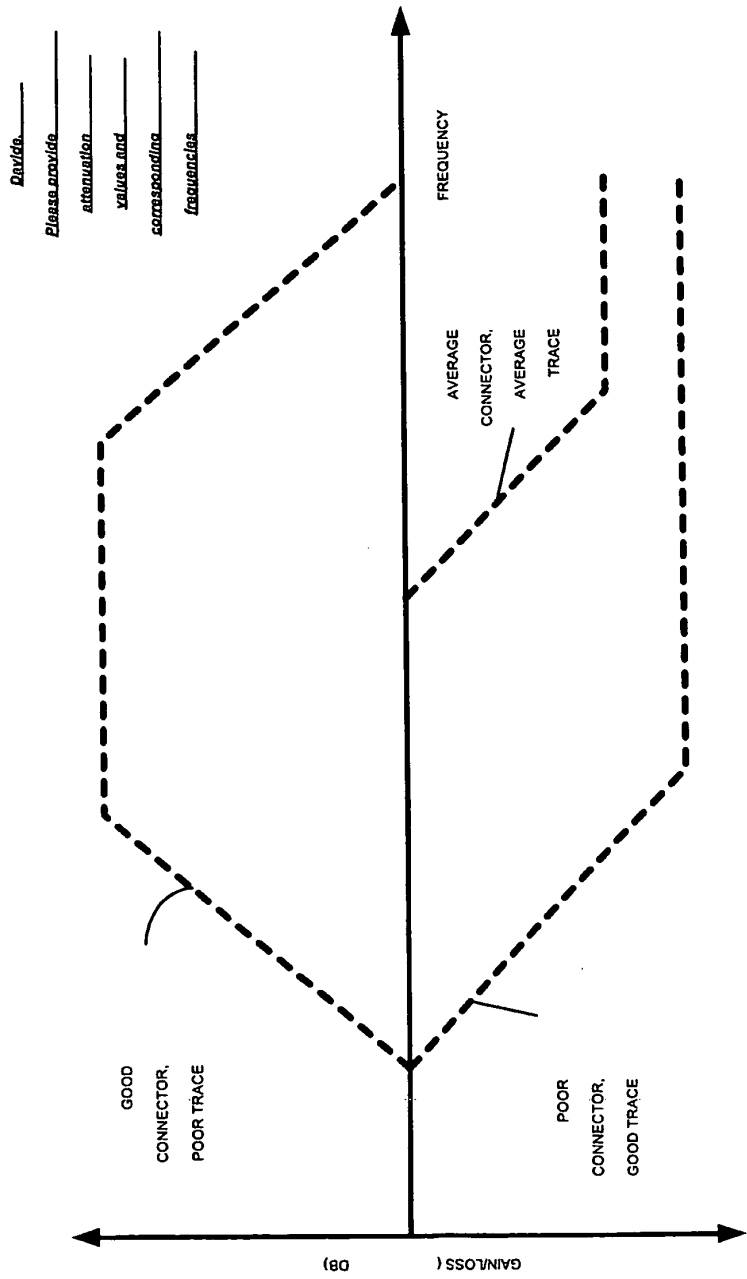


FIG. 19

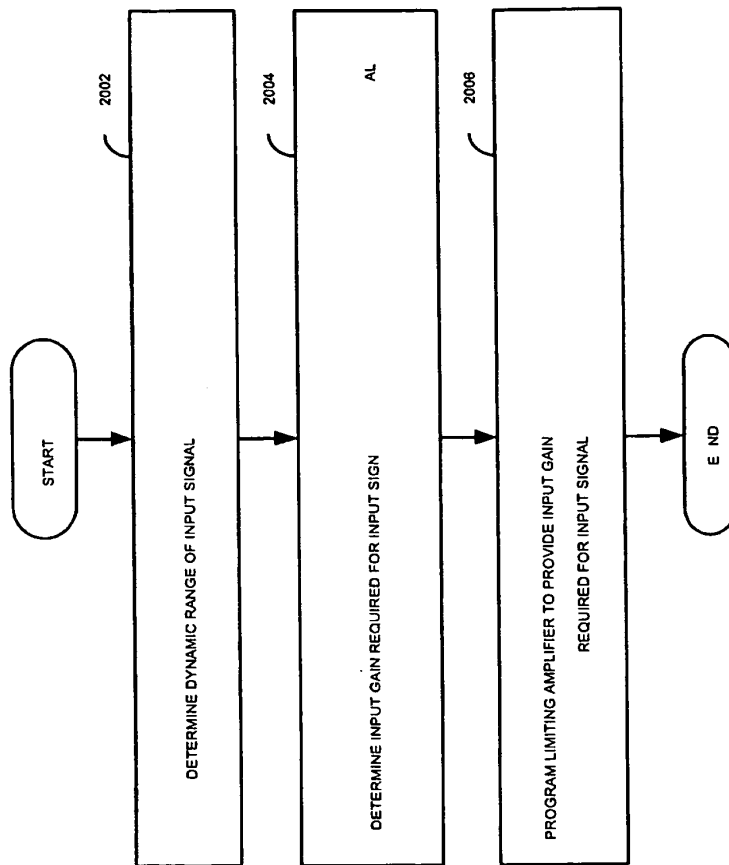


FIG. 20

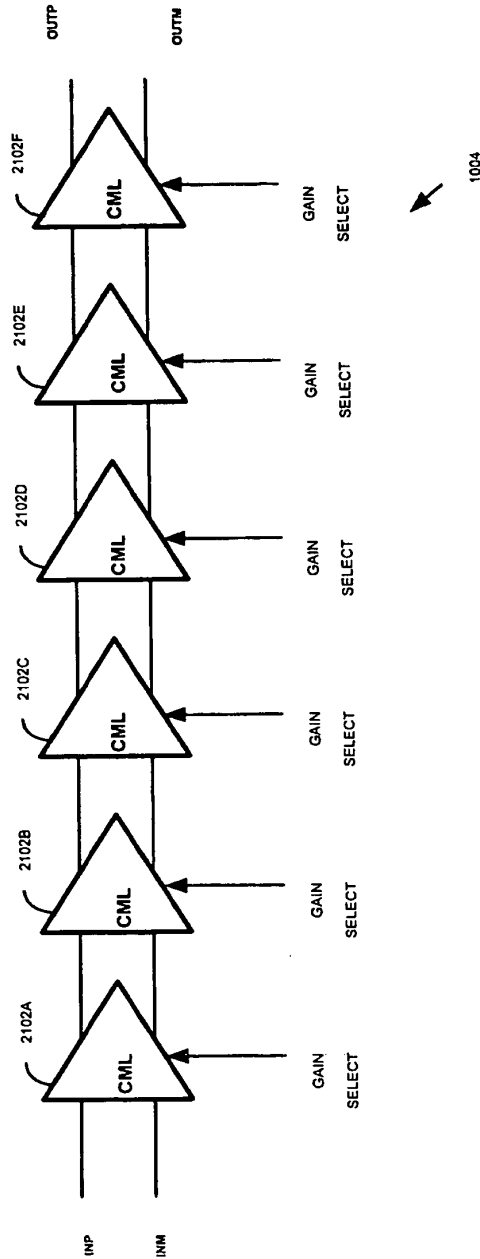


FIG. 21

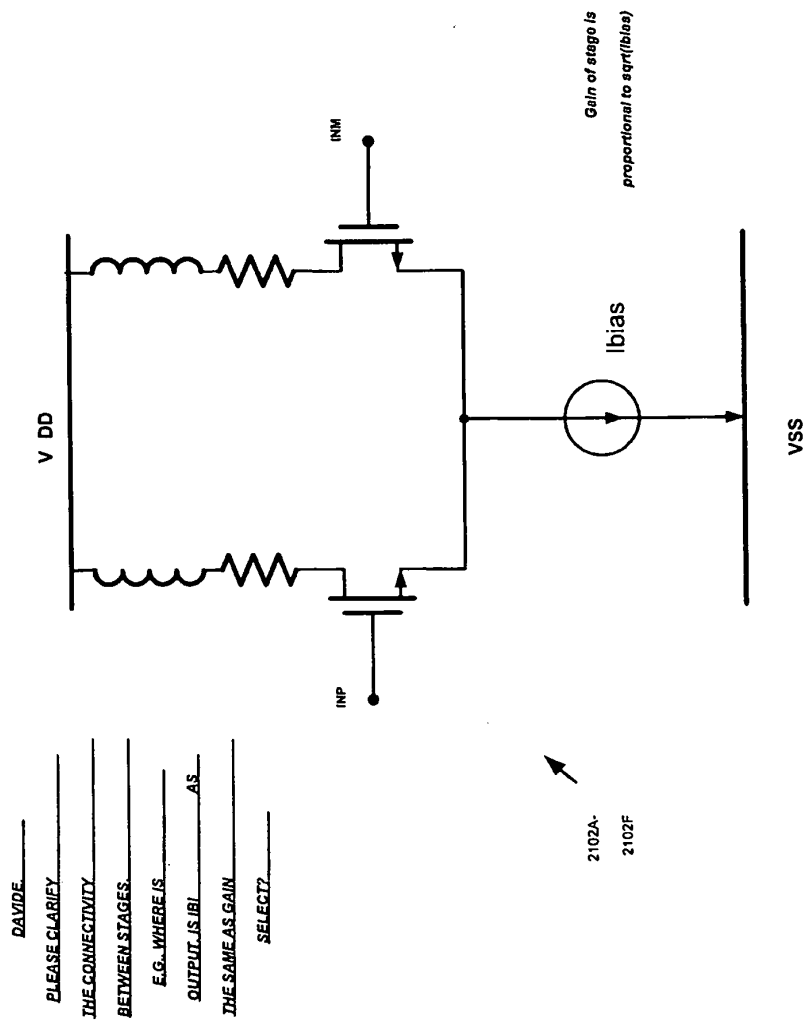


FIG. 22



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 03 01 6706

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	CHEN W Y: "A DIRECT EQUALIZATION METHOD" 1997 IEEE INTERNATIONAL CONFERENCE ON ACOUSTICS, SPEECH, AND SIGNAL PROCESSING. SPEECH PROCESSING, DIGITAL SIGNAL PROCESSING. MUNICH, vol. 3, 21 - 24 April 1997, pages 2505-2508, XP000735068 IEEE, NEW YORK, NY, USA ISBN: 0-8186-7920-4 * abstract * * page 2507, left-hand column, line 18 - right-hand column, line 21 * * figures 6,7,10 * ---	1-20	H04L25/02 H04L25/03 H04L25/20
X	EP 0 928 088 A (CIT ALCATEL) 7 July 1999 (1999-07-07) * paragraph [0009] - paragraph [0013] * * figure 1 * ---	1-20	
X	WO 02 32005 A (MANTILLO KARI ;NOKIA CORP (FI)) 18 April 2002 (2002-04-18) * paragraph [0005] - paragraph [0006] * * paragraph [0017] * * figures 4-6 * ---	1-10, 12-20 11	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H04L
A			
X	US 2001/033614 A1 (HUDSON JOHN E) 25 October 2001 (2001-10-25) * paragraph [0052] - paragraph [0055] * * paragraph [0060] - paragraph [0063] * * figure 2 * ---	14-20 1-13	
A			
A	US 6 377 076 B1 (GAUTHIER CLAUDE R) 23 April 2002 (2002-04-23) * column 1, line 11 - line 19 * * column 3, line 37 - line 58 * * figure 5 * -----	1,11,14, 17	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 21 October 2003	Examiner Marselli, M
CATEGORY OF CITED DOCUMENTS X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons &: member of the same patent family, corresponding document			

EPO FORM 1500 (03.02) (P4C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 03 01 6706

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
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21-10-2003

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			CN 1220530 A	23-06-1999
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			EP 1119146 A2	25-07-2001
US 6377076	B1	23-04-2002	NONE	

EPO FORM P0489

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

WIRING SUBSTRATE FOR HIGH FREQUENCY

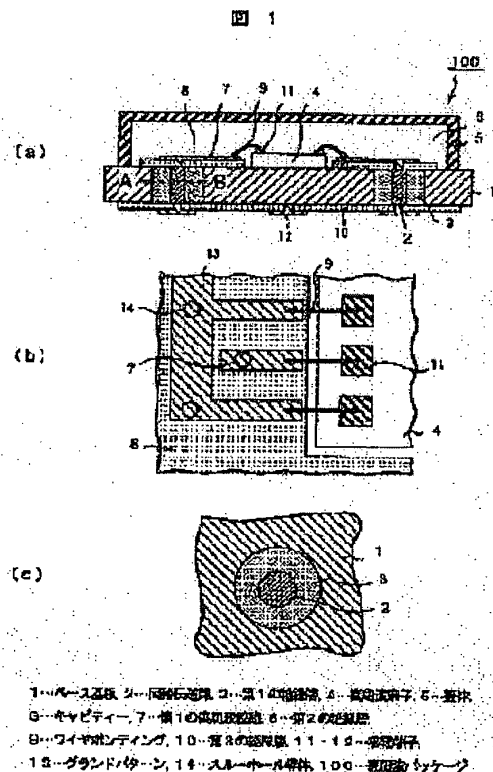
Patent number: JP2001298123
Publication date: 2001-10-26
Inventor: MATSUZAKI EIJI; SHIGI HIDETAKA; MATSUSHIMA NAOKI; HASEBE TAKEHIKO; FUJITA TAKESHI; MATSUMOTO KUNIO
Applicant: HITACHI LTD
Classification:
- international: H01L23/12; H01L21/60; H01L23/02; H01P5/08; H05K1/05
- european:
Application number: JP20000121061 20000417
Priority number(s):

Report a data error here

Abstract of JP2001298123

PROBLEM TO BE SOLVED: To provide a compact and highly reliable wiring substrate for high frequency of a simplified structure by sealing a substrate hermetically whereon a high frequency element is mounted and reducing transmission loss of a high frequency signal.

SOLUTION: A coaxial transmission path which is subjected to hermetic seal is formed in a base substrate formed of metal, and a high frequency circuit block including a high frequency element is sealed hermetically by means of a base substrate and a lid body. Input/output of a high frequency signal to a high frequency element and an electrical connection to other circuit block are carried out via the coaxial transmission path.



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(19) 日本国特許庁 (J P)

(12) 公開特許公報 (A)

(11) 特許出願公開番号

特開2001-298123

(P2001-298123A)

(43) 公開日 平成13年10月26日 (2001. 10. 26)

(51) Int.Cl. ⁷	識別記号	F I	テ-マ-ト*(参考)
H 0 1 L 23/12	3 0 1	H 0 1 L 23/12	3 0 1 C 5 E 3 1 5
		21/60	3 0 1 A 5 F 0 4 4
21/60	3 0 1		3 1 1 S
	3 1 1	23/02	H
23/02		H 0 1 P 5/08	M
審査請求 未請求 請求項の数11 O L (全 9 頁) 最終頁に続く			

(21) 出願番号 特願2000-121061(P2000-121061)

(22) 出願日 平成12年4月17日 (2000. 4. 17)

(71) 出願人 000005108

株式会社日立製作所

東京都千代田区神田駿河台四丁目6番地

(72) 発明者 松崎 永二

神奈川県横浜市戸塚区吉田町292番地 株

式会社日立製作所生産技術研究所内

(72) 発明者 志饒 英孝

神奈川県横浜市戸塚区吉田町292番地 株

式会社日立製作所生産技術研究所内

(74) 代理人 100075096

弁理士 作田 康夫

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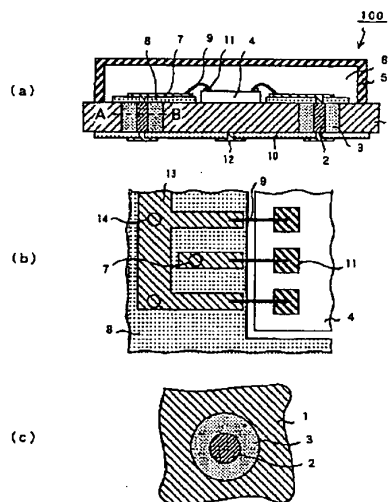
(54) 【発明の名称】 高周波用配線基板

(57) 【要約】

【課題】高周波素子を搭載する基板を気密に封止するとともに高周波信号の伝送損失を低減し、簡略化した構造からなる小形で高信頼性の高周波用配線基板を提供する。

【解決手段】金属からなるベース基板にハーメチックシールされた同軸伝送路を形成し、ベース基板と蓋体により高周波素子を含む高周波回路ブロックを気密封止する。高周波素子への高周波信号の入出力と他の回路ブロックとの電気的接続を上記同軸伝送路を介して行う。

図 1



1…ベース基板、2…同軸伝送路、3…第1の絶縁層、4…高周波素子、5…溶剤、
6…キャビティ、7…第1の高周波伝導層、8…第2の絶縁層、
9…ワイヤボンディング、10…第3の絶縁層、11・12…接続端子、
13…グランドパターンの、14…スルーホール部、15…高周波用パッケージ

【特許請求の範囲】

【請求項1】 金属部材からなるベース基板と、該ベース基板内部に第1の絶縁部材を介して設けられた該ベース基板の2つの主表面を接続する同軸伝送路と、上記ベース基板の少なくとも一方の主表面上に搭載された高周波素子と、該高周波素子を含む高周波回路ブロックを覆うように設けられた蓋体とからなる高周波用配線基板であって、上記ベース基板と上記同軸伝送路と上記第1の絶縁部材によりハーメチックシールを行うことにより、上記ベース基板と上記蓋体により構成されるキャビティー内に上記高周波回路ブロックを気密封止することを特徴とする高周波用配線基板。

【請求項2】 金属部材からなるベース基板と、該ベース基板内部に第1の絶縁部材を介して設けられた該ベース基板の2つの主表面を接続する同軸伝送路と、上記ベース基板の少なくとも一方の主表面上に設けられた少なくとも2つ以上の複数の回路ブロックとからなる高周波用配線基板であって、上記回路ブロックの少なくとも1つは、上記ベース基板と上記同軸伝送路と上記第1の絶縁部材によりハーメチックシールされ、上記ベース基板と蓋体によって構成されるキャビティー内に気密封止された高周波素子を含む高周波回路ブロックであり、該高周波素子を含む高周波回路ブロックと他の回路ブロックとの電気的接続を、上記ベース基板内部に設けられた上記同軸伝送路と、上記回路ブロックが設けられていない上記ベース基板の反対側の配線によって行うことを特徴とする高周波用配線基板。

【請求項3】 請求項1又は2に記載の高周波用配線基板において、上記高周波素子と上記高周波用線路あるいは上記同軸伝送路との接続を、ワイヤボンディング、リボン、金属層付テープのいずれかによって行うことを特徴とする高周波用配線基板。

【請求項4】 請求項1又は2に記載の高周波用配線基板において、上記高周波素子と上記高周波用線路あるいは上記同軸伝送路との接続を、導電性接着剤を用いてフリップチップ実装により行うことを特徴とする高周波用配線基板。

【請求項5】 請求項1乃至4のいずれかに記載の高周波用配線基板において、上記高周波回路ブロック内に抵抗、キャパシタ、コイル等の受動回路素子を設けることを特徴とする高周波用配線基板。

【請求項6】 請求項1乃至4のいずれかに記載の高周波用配線基板において、上記高周波回路ブロック内に上記ベース基板を一方の電極の一部とするキャパシタを設けることを特徴とする高周波用配線基板。

【請求項7】 請求項1乃至6のいずれかに記載の高周波用配線基板において、上記ベース基板内部に設けられる上記同軸伝送路を上記ベース基板と同一部材で構成することを特徴とする高周波用配線基板。

【請求項8】 請求項1乃至6のいずれかに記載の高周

波用配線基板において、上記ベース基板内部に設けられる上記同軸伝送路を、径方向において、少なくとも2つ以上の部材により構成することを特徴とする高周波用配線基板。

【請求項9】 請求項8に記載の高周波用配線基板において、上記同軸伝送路の中心部分を、上記ベース基板と同一部材により構成することを特徴とする高周波用配線基板。

【請求項10】 請求項8に記載の高周波用配線基板において、上記同軸伝送路の最外周部分を、上記ベース基板と同一部材により構成することを特徴とする高周波用配線基板。

【請求項11】 請求項1乃至10のいずれかに記載の高周波用配線基板において、上記ベース基板を構成する部材を、少なくともニッケル(Ni)、クロム(Cr)、マンガン(Mn)のいずれかを含む鉄(Fe)系合金、該鉄合金に銅(Cu)クラッドを施した鉄系複合材、銅(Cu)、モリブデン(Mo)、タングステン(W)、のいずれかより選択することを特徴とする高周波用配線基板。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は半導体素子を収納するためのパッケージ等に用いられる配線基板に係わり、特に、マイクロ波やミリ波領域の周波数の高い信号を処理するための配線基板に関する。

【0002】

【従来の技術】近年、高速な情報網システムが急速に展開され、通信衛星システムや追突防止用レーダ等の高周波帯で動作する半導体装置の需要が増大している。

【0003】マイクロ波やミリ波を取り扱う高周波素子を搭載した高周波パッケージでは、誘電体基板と、誘電体基板の表面に接続された壁体や蓋体によって形成されるキャビティー内に気密封止された高周波素子が収納されている。そして、高周波素子と電気的に接続された信号伝送回路と外部回路基板に形成された信号伝送回路を電気的に接続することにより高周波信号の入出力を行っている。このような高周波パッケージの例を図7に示す。これらの高周波パッケージについては、特開平7-263887号や特開平11-345910号、特開2000-22043号等の公開特許公報で述べられている。図7(a)に示した高周波パッケージ701では、誘電体基板31と蓋体32で形成されたキャビティー33内に気密封止された高周波素子34が搭載されている。誘電体基板31の表面にはストリップ線路やマイクロストリップ線路等の高周波用伝送線路36が形成され、ワイヤボンディングやリボン等により高周波素子34に接続されている。この高周波用伝送線路36を蓋体32を通してキャビティー33の外部に引き出し、さらに、誘電体基板31の側面を経由して裏面に引き回し、誘電体基板31の裏面側に高周波用伝送線路36を延ばしている。そして、外部回路基板41の高周波用伝送線路42と高

周波用伝送線路36を半田等の導電性接着剤37により接続し、高周波用伝送線路42を介して、高周波信号の入出力と他の高周波パッケージ701'との接続を行っている。

図7(b)に示した高周波パッケージ702では、キャビティ53内の誘電体基板51の表面に一端が高周波素子54と接続された高周波用伝送線路56が形成され、誘電体基板51の裏面には高周波用伝送線路58が形成されている。

【0004】そして、高周波用伝送線路56と高周波用伝送線路58をスルーホール導体57により接続している。この高周波パッケージ702の場合にも、高周波パッケージ701と同様に、誘電体基板51の裏面側の高周波用伝送線路58と外部回路基板61の高周波用伝送線路62とを半田等の導電性接着剤59を用いて接続し、高周波用伝送線路62を介して、高周波信号の入出力や他の高周波パッケージ702'との接続を行っている。図7(c)に示した高周波パッケージでは、導電性の蓋体により、複数の高周波素子がそれぞれ別個に気密封止され、誘電体基板71の表面から金属板78、85を貫通するスルーホールが各高周波素子の入出力端に形成されている。該スルーホールの内部には、スルーホール導体77、83が形成され、スルーホール導体77とスルーホール導体83は伝送線路接続部80によって接続されている。金属板78、85の内部では、スルーホール導体83はテフロンスリーブ79、84を挟んで金属板78、85により囲まれており、同軸伝送線路となっている。この例の場合、誘電体基板81の表面に形成された高周波用伝送線路82とスルーホール導体77、83を介して、高周波信号の入出力と各高周波素子間の接続が行われている。

【0005】

【発明が解決しようとする課題】図7(a)の場合、高周波用伝送線路36が蓋体32を通過する場合、通過部で線路がマイクロストリップ線路からストリップ線路に変換されるため、信号線幅を狭くする必要がある。その結果、高周波用伝送線路36の蓋体32通過部で反射損、放射損が発生し易く、高速信号の特性劣化が生じやすいという問題があった。またミリ波帯で用いた場合、高周波用伝送線路36が誘電体基板31の側面で大きく曲げられていることから、高周波信号の反射が大きくなり、高周波信号を伝送することが困難になることがあった。それに対し、図7(b)の場合、誘電体基板41のキャビティ43側の高周波用伝送線路56とその反対側の高周波用伝送線路58をスルーホール導体57により接続しているため、図7(a)のような蓋体32通過部での反射損や放射損は軽減される。しかし、マイクロ波からミリ波帯領域の高周波信号の場合、高周波伝送線路56、59とスルーホール導体57の接続部が曲折していることなどから、スルーホール導体57部での透過損失が大きくなり、特性劣化なく高周波信号を伝送することが困難であった。また、図7(c)の場合、スルーホール導体83が同軸伝送線路であることから、高周波信号の伝送損失を小さくできる。しかし、テ

フロン（登録商標）スリーブ79内においてスルーホール導体83が偏芯しやすいなど、スルーホール内への同軸伝送線路の形成が困難であり、また、スルーホール導体77とスルーホール導体83の接続部の信頼性が劣るなどの問題があった。

【0006】本発明では、高周波素子を搭載する基板を気密に封止するとともに高周波信号の伝送損失を低減し、簡略化した構造からなる小形で高信頼性の高周波用配線基板を提供することを目的としている。

【0007】

【課題を解決するための手段】上記目的は、金属部材からなるベース基板と、該ベース基板内部に第1の絶縁部材を介して設けられた該ベース基板の2つの主表面を接続する同軸伝送路と、上記ベース基板の少なくとも一方の主表面上に搭載された高周波素子と、該高周波素子を含む高周波回路ブロックを覆うように設けられた蓋体と、からなる高周波用配線基板であって、上記ベース基板と上記同軸伝送路と上記第1の絶縁部材によりハーメチックシールを行うことにより、上記高周波回路ブロックを上記ベース基板と上記蓋体により構成されるキャビティ内に気密封止することを特徴とする請求項1に記載の高周波用配線基板によって達成される。すなわち、ハーメチックシールされた同軸伝送路が設けられた金属部材からなるベース基板と蓋体で構成されるキャビティ内に高周波素子を含む高周波回路ブロックを気密封止し、高周波素子への信号の入出力や他の回路ブロックとの接続を金属部材からなるベース基板中に設けられた同軸伝送路を介して行うことにより、達成される。かかる構成によれば、高周波信号は同軸線路によって伝送され、外部回路との距離も短縮できるからである。

【0008】請求項2に記載の高周波用配線基板は、金属部材からなるベース基板と、該ベース基板内部に第1の絶縁部材を介して設けられた該ベース基板の2つの主表面を接続する同軸伝送路と、上記ベース基板の少なくとも一方の主表面上に設けられた少なくとも2つ以上の複数の回路ブロックと、からなる高周波用配線基板であって、上記回路ブロックの少なくとも1つは、上記ベース基板と上記同軸伝送路と上記第1の絶縁部材によりハーメチックシールされ、上記ベース基板と蓋体によって構成されるキャビティ内に気密封止された高周波素子を含む高周波回路ブロックであり、該高周波素子を含む高周波回路ブロックと他の回路ブロックとの電気的接続を、上記ベース基板内部に設けられた上記同軸伝送路と、上記回路ブロックが設けられていない上記ベース基板の反対側の配線によって行うことを特徴とするものである。

【0009】請求項3に記載の高周波用配線基板は、請求項1又は2に記載の高周波用配線基板において、上記高周波素子と高周波用線路あるいは上記同軸伝送路との接続を、ワイヤボンディング、リボン、金属層付テープ

のいずれかによって行うことを特徴とするものである。

【0010】請求項4に記載の高周波用配線基板は、請求項1又は2に記載の高周波用配線基板において、上記高周波素子と上記高周波用線路あるいは上記同軸伝送路との接続を、導電性接着剤を用いてフリップチップ実装により行うことを特徴とするものである。かかる構成によれば、高周波素子と高周波用線路あるいは同軸伝送路との接続部でリード線によるインダクタンス成分の影響を低減できる。

【0011】請求項5に記載の高周波用配線基板は、請求項1乃至4のいずれかに記載の高周波用配線基板において、上記高周波回路ブロック内に抵抗、キャパシタ、コイル等の受動回路素子を設けること、を特徴とするものである。かかる構成によれば、終端抵抗やデカップリングキャパシタを高周波素子の近傍に配設できることになり、ノイズ発生を低減できるようになる。

【0012】請求項6に記載の高周波用配線基板は、請求項1乃至4のいずれかに記載の高周波用配線基板において、上記高周波回路ブロック内に上記ベース基板を一方の電極の一部とするキャパシタを設けることを特徴とするものである。すなわち、ベース基板が導電性の金属部材により構成されていることを利用して、ベース基板を電極としたキャパシタを高周波回路ブロック内に形成したものである。かかる構成によれば、デカップリングキャパシタを高周波素子の直下に配設できることから実装面積を小さくでき、デカップリングキャパシタを設けた高周波パッケージを小さくできる。

【0013】請求項7に記載の高周波用配線基板は、請求項1乃至6のいずれかに記載の高周波用配線基板において、上記ベース基板内部に設けられる上記同軸伝送路を上記ベース基板と同一部材で構成することを特徴とするものである。かかる構成によれば、同一工程により同軸伝送路の導体部分とそれを取り囲む絶縁層を埋め込むスルーホール部分を同時に形成できることから、製造工程が簡略化され、上記同軸伝送路の断面形状品質を上げることができる。

【0014】請求項8に記載の高周波用配線基板は、請求項1乃至6のいずれかに記載の高周波用配線基板において、上記ベース基板内部に設けられる上記同軸伝送路を、径方向において、少なくとも2つ以上の部材により構成すること、を特徴とするものである。

【0015】請求項9に記載の高周波用配線基板は、請求項8に記載の高周波用配線基板において、上記同軸伝送路の中心部分を、上記ベース基板と同一部材により構成することを特徴とするものである。かかる構成によれば、ベース基板と同じ部材からなる同軸伝送路の外周部分に低抵抗材料からなる層を設けることができ、請求項8に記載の高周波用配線基板に設けられた同軸伝送路の抵抗を下げるができる。

【0016】請求項10に記載の高周波用配線基板は、

請求項8に記載の高周波用配線基板において、上記同軸伝送路の最外周部分を、上記ベース基板と同一部材により構成することを特徴とするものである。かかる構成によれば、同軸伝送路の中心部を抵抗率の低い部材で構成し、外周をハーメチックシールに適した部材で構成できるようになり、ハーメチックシールの品質を上げながら、同軸伝送路の抵抗を低くできる。

【0017】請求項11に記載の高周波用配線基板は、請求項1乃至10のいずれかに記載の高周波用配線基板において、上記ベース基板を構成する部材を、少なくともニッケル(Ni)、クロム(Cr)、マンガン(Mn)のいずれかを含む鉄(Fe)系合金、該鉄合金に銅(Cu)クラッドを施した鉄系複合材、銅(Cu)、モリブデン(Mo)、タングステン(W)、のいずれかより選択することを特徴とするものである。すなわち、ガラス封着の可能な金属部材をベース基板として用いることにより、ハーメチックシールの可能な同軸伝送路の形成を可能にしている。

【0018】

【発明の実施の形態】〈第1の実施の形態〉本発明の第1の実施の形態を図1に示す。図1(a)は第1の実施の形態を要部断面図で示したものであり、図1(b)は第1の実施の形態における高周波素子とグランド付きコプレーナ線路からなる高周波用伝送線路との接続状況を示す要部平面図であり、図1(c)はベース基板内に設けた同軸伝送路の断面(図1(a)のA-B断面)を示したものである。図において、100は本発明による高周波用配線基板を利用した高周波パッケージを、1は金属部材からなるベース基板を、2は該ベース基板1内に設けられた同軸伝送路を、3は該同軸伝送路2を囲むように設けられた第1の絶縁層を、4は高周波素子を、5は蓋体を、6はベース基板1と蓋体5により形成されるキャビティを、7は第1の高周波用伝送線路を、8はベース基板1上に設けられた第2の絶縁層を、9はワイヤボンディングを、10はベース基板1の裏面側に設けられた第3の絶縁層を、11は高周波素子4の接続端子を、12はベース基板1の裏面側に設けられた接続端子を、13は第2の絶縁層8上に形成されたグランドパターンを、14はベース基板1とグランドパターン13を接続するスルーホール導体を、示す。同軸伝送路2は第1の絶縁層3により金属部材からなるベース基板1から電気的に分離され、高周波素子4と第1の高周波用伝送線路7は第2の誘電体層により、接続端子12は第3の絶縁層により、金属部材からなるベース基板1と電気的に分離されている。かかる構成において、本実施の形態では、ベース基板1をグランドプレーンとして用いる。

【0019】本実施の形態では、高周波回路ブロックへの信号の入出力をベース基板1内に設けた同軸伝送路2によって行っているため、高周波信号の伝送損失を小さくできる。また、同軸伝送路2はベース基板1をまっすぐに貫通して背面側の接続端子12に達しているため、構

造は単純なものになり、キャビティー6の外部への引き出し線の長さを短いものとしている。

【0020】本実施の形態の特徴は、同軸伝送路2の部分をハーメチックシールとし、ベース基板1と蓋体5により形成されるキャビティー6の中に高周波素子4と高周波用伝送線路7からなる高周波回路ブロックを気密に封止している点にある。従って、ベース基板1と同軸伝送路2としてはハーメチックシールの可能な材料を選択することが必要である。そのような材料として、少なくともニッケル(Ni)、クロム(Cr)、マンガン(Mn)のいずれかを含む鉄(Fe)系合金、該鉄合金に銅(Cu)クラッドを施した鉄系複合材、銅(Cu)、モリブデン(Mo)、タングステン(W)の中から選択することが好ましい。第1の絶縁層3としては、ベース基板1と同軸伝送路2の材料に合わせて選択すればよい。例えば、CuやMoに対してはアルミノケイ酸ガラス、コパール(29%のNiと17%のCoを含む鉄合金)やWに対してはホウケイ酸ガラス、42アロイ(42%のNiを含む鉄合金)に対してはソーダライムガラス、ジュメット(42アロイに対してCuクラッドを施したもの)に対してはアルカリ鉛ガラスなどである。また、本実施の形態においては、高周波素子4と第1の高周波用伝送線路の接続をワイヤボンディングにより行っているが、リボンや金属層付きテープを用いても差し支えない。

【0021】蓋体5としては、キャビティー6から外部に電磁波が漏洩することを防止できる材料から構成することが望ましい。例えば、金属、導電性セラミック、セラミック金属複合材料、絶縁基板表面に導電性材料利用を塗布したもの等から選択すればよい。第1の高周波用伝送線路7としてグランド付きコプレーナ線路を用いているが、これに限定されるものではなく、マイクロストリップ線路やストリップ線路であっても差し支えない。また、高周波用伝送線路7としては、CuやAu、Ag、W等の低抵抗材料を用いることが好ましい。

【0022】なお、本実施例の場合、同軸伝送路2の中に接続部が存在しないため、図7(c)で懸念される接続部の信頼性が劣るという問題は発生しない。

【0023】〈第2の実施の形態〉第2の実施の形態を図2と図3により説明する。図2は本発明による高周波用配線基板を利用した高周波パッケージ210、220、230の要部断面図を示しており、図3は該高周波パッケージ210、220、230のベース基板1の中に形成される同軸伝送路2の断面構造を示したものである。すなわち、図3(a)は図2(a)のA-B断面を、図3(b)は図2(b)のA-B断面を、図3(c)は図2(c)のA-B断面を示している。

【0024】この実施の形態の基本構造は第1の実施の形態と同じであり、第1の実施の形態と異なる点は次の通りである。高周波パッケージ210では、ベース基板1内に形成される同軸伝送路2がベース基板1と同じ材料

から構成されている。高周波パッケージ220では、ベース基板1内に形成される同軸伝送路2が径方向に対して2層になっており、その中心部201がベース基板1と同一部材により構成され、外周部202がベース基板1とは異なる部材により構成されている。高周波パッケージ230の場合にも、ベース基板1内に形成される同軸伝送路2が径方向に対して2層になっており、その外周部202がベース基板1と同一部材により構成され、中心部201がベース基板1とは異なる部材により構成されている。これらの違いにより本発明の効果を失わないので、本実施の形態の場合にも第1の実施の形態と同じ効果を得ることができる。

【0025】本実施の形態における高周波パッケージ210の場合、ベース基板1内に形成する同軸伝送路2は、同軸伝送路2の周囲の第1の絶縁層3を充填するためのスルーホールを従来のフォトリソ法を用いて形成することにより実現できる。このため、同軸伝送路2の形成工程が簡略化され、また、スルーホール導体の位置精度を高くできる。これにより、同軸伝送路2の特性インピーダンスの制御が容易になる。高周波パッケージ220では、ベース基板1と同一部材からなる同軸伝送路2の外周をCuのような低抵抗材料により被覆し、高周波パッケージ210における同軸伝送路2の抵抗を低くしている。また、高周波パッケージ220の場合には、ベース基板1と同一部材からなる同軸伝送路2の内部にCuのような低抵抗材料を充填し、高周波パッケージ210における同軸伝送路2の抵抗を低くしている。すなわち、同軸伝送路2をのを高周波パッケージ220または高周波パッケージ230で示した構造とすることにより、ベース基板1と同一部材からなる同軸伝送路の抵抗を低くできる。

【0026】〈第3の実施の形態〉第3の実施の形態を図4により説明する。図4は本発明による高周波用配線基板を利用した高周波パッケージ410、420、430を要部断面図で示したものである。図において、23は半田を、15はAu-Sn等からなる導電性の接着剤を示す。本実施の形態では、高周波素子4が第1の高周波用伝送線路7に対してフリップチップボンディングされている。この点が本実施の形態は第1の実施の形態と異なっている。それ以外の構造や製造方法は、第1の実施の形態と同じである。ここで述べた相違によって本発明の効果が失われないことは明白であり、本実施の形態の場合にも第1の実施の形態と同じ効果を得ることができる。また本実施の形態の場合、高周波素子4と第1の高周波用伝送線路7の接続にワイヤボンディングのような細いリード線を用いていないので、リード線の寄生インダクタンスに起因した高周波信号の特性劣化を抑制できる。

【0027】図4(b)に示した高周波パッケージ420の場合、第1の高周波用伝送線路7は接続端子の役割しかもたず、高周波素子4への高周波信号の入出力は同軸伝送路2からほとんどダイレクトに行われる。これにより、

高周波信号の伝送損失をさらに小さくでき、また、高周波パッケージの小型化が可能になる。なお、図4(c)の高周波パッケージ430では、導電性の蓋体5を介して高周波素子4の背面側電極と、ベース基板1からなるグランドプレーンとを接続している例として示したものである。

【0028】〈第4の実施の形態〉図5により、第4の実施の形態を説明する。図において、16はチップ部品を、17はキャパシタを、18は抵抗素子を、170はキャパシタ17の誘電体層を、171はキャパシタ17の下部電極を、172はキャパシタ17の上部電極を、173は下部電極17の一部を構成する導体層を示し、510と520、530は高周波パッケージを示す。その他の符号は図1～図4の場合と同じである。

【0029】図5(a)に示した高周波パッケージ510では、第1の高周波用伝送線路7に抵抗やキャパシタ、コイル等のチップ部品16が取り付けられ、図5(b)に示した高周波パッケージ520ではベース基板1を下部電極171の一部として用いたキャパシタ17がベース基板1上に設けられており、図5(c)に示した高周波パッケージ530では、抵抗素子18が第1の高周波用伝送線路7に接続されるように設けられている。これらのパッケージでは、キャパシタや抵抗等の受動素子をキャビティ6内に収納することによって高周波素子4の近傍に配置させ、これらの受動素子をデカップリングキャパシタや終端抵抗として用いることにより、ノイズの発生や電源電圧の変動を抑制している。

【0030】なお、本実施の形態においても、ハーメチックシールした同軸伝送路2がベース基板1内に形成されており、第1の実施の形態と同じ効果を得ることができる。

【0031】〈第5の実施の形態〉第5の実施の形態を図6に示す。図において、19はベース基板1の背面側に設けられた第2の高周波用伝送線路を、20は個別部品を、21は気密封止されていない場所に形成された第3の高周波用伝送線路を、22は第3の高周波用伝送線路21と個別部品20を接続するリード線を示し、610と620、630は気密封止された高周波パッケージを表している。その他の符号は、図1～図5の場合と同じである。図6(a)に示した高周波用配線基板では、ハーメチックシールされた同軸伝送路2を有するベース基板1上に気密封止された回路ブロックと、個別部品20が搭載された回路ブロックが設けられており、これらの回路ブロックを同軸伝送路2とベース基板1の背面側に設けられた第2の高周波用伝送線路19によって接続している。また、図6(b)に示した高周波用配線基板では、ハーメチックシールされた同軸伝送路2を有するベース基板1上に気密封止された回路ブロックが2つ設けられており、これらの回路ブロックを同軸伝送路2とベース基板1の背面側に設けられた第2の高周波用伝送線路19によって接続してい

る。これらの回路ブロック間の信号のやりとりを、ベース基板1内に設けられた同軸伝送路2と背面側に形成された第2の高周波用伝送線路19によって行われるため、伝送損失を小さく抑えることができる。高周波用伝送線路としては、マイクロストリップ線路やストリップ線路、グランド付きコプレーナ線路を用いればよい。なお、本実施の形態では、ベース基板1上に2つの回路ブロックを形成しているが、2つに限定されないことはいうまでもない。

【0032】

【発明の効果】以上のように、本発明によれば、高周波素子を含む高周波回路ブロックを、ハーメチックシールされた同軸伝送路を金属からなるベース基板と蓋体により気密封止し、高周波素子への入出力や他の回路ブロックとの電氣的接続を上記同軸伝送路を介して行うので、高周波信号の伝送損失を低減し、簡略化した構造からなる小形で高信頼性の高周波用配線基板を提供できる。

【図面の簡単な説明】

【図1】(a)は第1の実施の形態を要部断面図で示したものであり、(b)は第1の実施の形態における高周波素子とグランド付きコプレーナ線路からなる高周波用伝送線路との接続状況を示す要部平面図であり、(c)はベース基板内に設けた同軸伝送路の断面を示したものである。

【図2】本発明による高周波用配線基板を利用した第2の実施の形態を示す高周波パッケージの要部断面図である。

【図3】本発明の第2の実施の形態でベース基板内に形成される同軸伝送路の断面構造を示したものである。

【図4】本発明による高周波用配線基板を利用した第3の実施の形態を示す高周波パッケージの要部断面図である。

【図5】本発明による高周波用配線基板を利用した第4の実施の形態を示す高周波パッケージの要部断面図である。

【図6】本発明による高周波用配線基板を利用した第5の実施の形態を示す高周波パッケージの要部断面図である。

【図7】従来の高周波パッケージを示す要部断面図である。

【符号の説明】

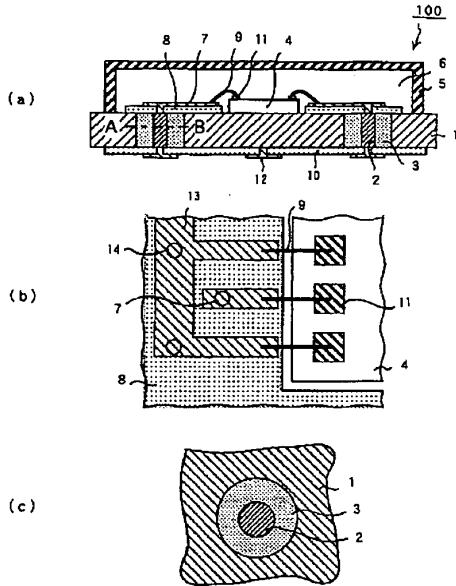
1…ベース基板、2…同軸伝送路、3, 8, 10…絶縁層、4, 34, 54, 74…高周波素子、5, 32, 52, 72…蓋体、6, 33, 43, 73…キャビティ、7, 19, 21, 36, 42, 56, 58, 62, 76…高周波用伝送線路、9, 35, 55, 75…ワイヤボンディング、11, 12…接続端子、13…グランドパターン、14, 57, 77, 83…スルーホール導体、15, 37, 59…導電性接着剤、16…チップ部品、17…キャパシタ、18…抵抗素子、20…個別部品、22…リード線、23…半田、170…キャパシタの誘電体層、171…キャパシタの下部電極、172…キャパシ

タの上部電極、31,51,71,81…誘電体基板、41,61…外部回路基板、80…伝送線路接続部、78,85…金属板、79,84…テフロンスリーブ、173…キャパシタの下部電極を構

成する導体層、201…同軸伝送路の中心部、202…同軸伝送路の外周部、100,210,220,230,410,420,430,510,520,530,610,620,630,701,702,703…高周波パッケージ。

【図1】

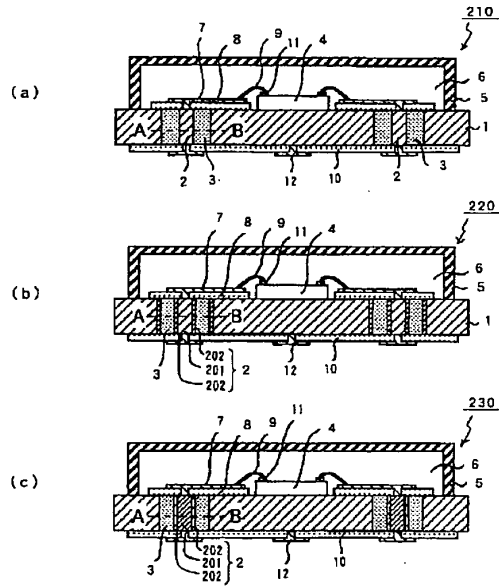
図 1



1…ベース基板、2…同軸伝送路、3…第1の絶縁層、4…高周波素子、5…蓋体、6…キャピティ、7…第1の高周波線路、8…第2の絶縁層、9…ワイヤボンディング、10…第3の絶縁層、11・12…接続端子、13…グラウンドパターン、14…スルーホール導体、100…高周波パッケージ

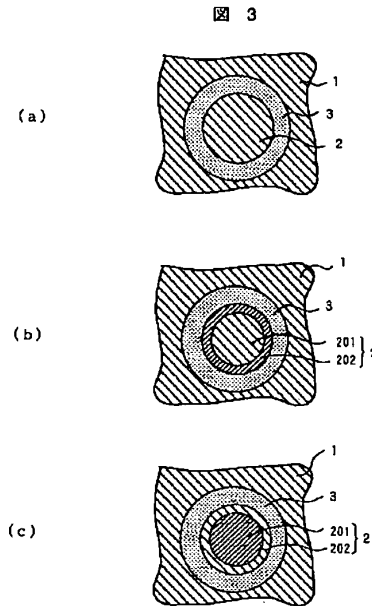
【図2】

図 2

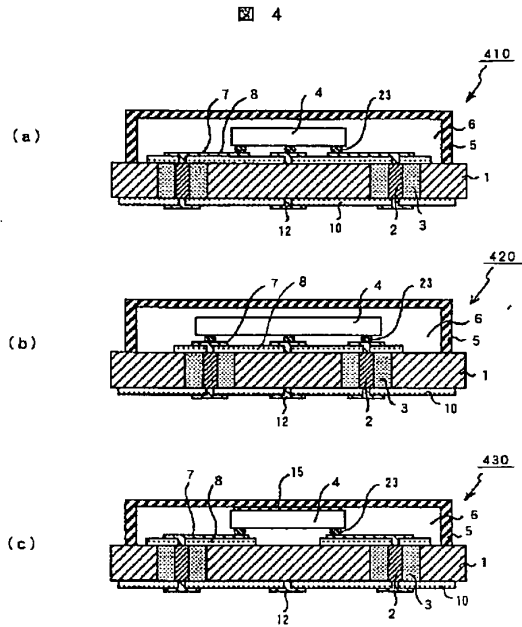


201…同軸伝送路の内側の部分、202…同軸伝送路の外側の部分、201・220・230…高周波パッケージ

【図3】

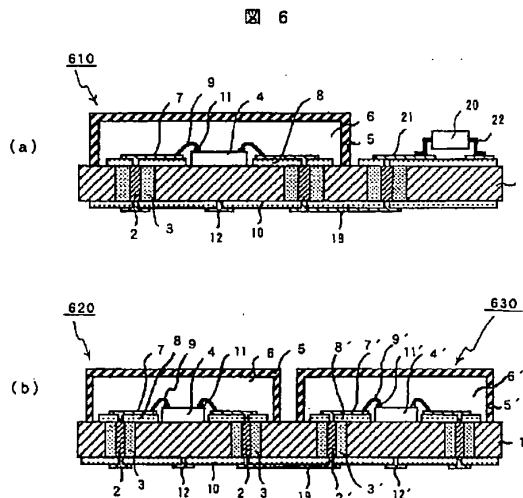


【図4】



15...導電性接着剤 23...はんだ、
410・420・430...高周波パッケージ

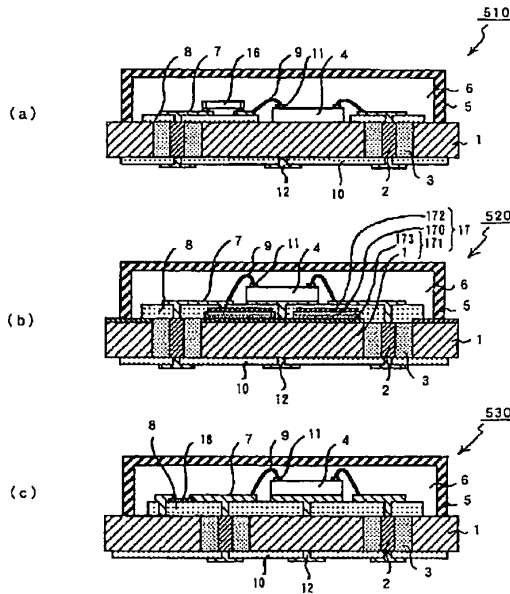
【図6】



19...第2の高周波伝送線路、20...個別部品、21...第3の高周波線路、
22...リード線、610・620・630...高周波パッケージ

【図5】

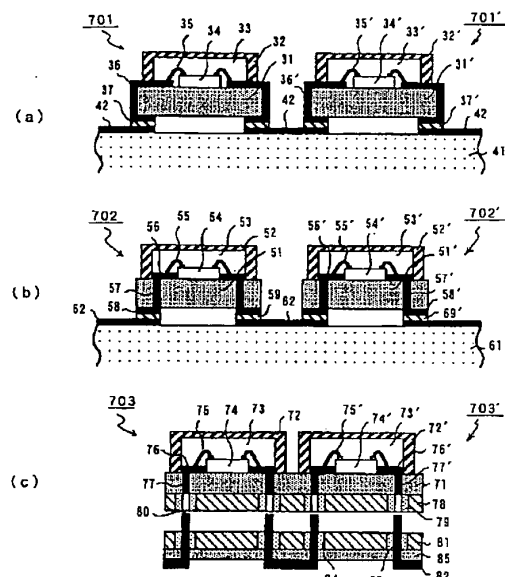
図 5



16…チップ部品 17…キャパシタ、18…抵抗素子、170…溶着体層
171…下部電極 172…上部電極 173…導電性層
510・520・530…高周波パッケージ

【図7】

図 7



31, 51, 71, 81…高周波基板、32, 52, 72…素子、33, 43, 73…キャパシタ、
34, 54, 74…高周波素子、35, 55, 75…ワイヤ、37, 57, 83…導電性接着剤、
36, 42, 56, 58, 62, 76…高周波用伝送回路、57, 77, 83…スルーホール導体、
41, 61…外部回路基板、80…伝送回路接続部、78, 85…金属板、
79, 84…テフロンスリブ、701, 702, 703…高周波用パッケージ

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(72) 発明者 松嶋 直樹		(72) 発明者 松本 邦夫	
神奈川県横浜市戸塚区吉田町292番地 株		神奈川県横浜市戸塚区吉田町292番地 株	
式会社日立製作所生産技術研究所内		式会社日立製作所生産技術研究所内	
(72) 発明者 長谷部 健彦		F ターム (参考) 5E315 AA02 AA05 AA11 BB02 BB04	
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式会社日立製作所生産技術研究所内		DD27 GG22	
(72) 発明者 藤田 毅		5F044 AA02 AA07 KK04 KK10 KK11	
神奈川県横浜市戸塚区吉田町292番地 株		LL01	
式会社日立製作所生産技術研究所内			

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- (71) Applicant: **BERKANA WIRELESS INC.** [US/US];
2005 Hamilton Avenue, Suite 200, San Jose, CA 95125 (US).
- (72) Inventors: **KIM, Beomsup**; 811 Candlewood Drive, Cupertino, CA 95125 (US). **CONROY, Cormac, S.**; 655 S. Fair Oaks Avenue #J-208, Sunnyvale, CA 94086 (US).
- (74) Agent: **VAN PELT, Lee**; Van Pelt & Yi LLP, 4906 El Camino Real, Suite 205, Los Altos, CA 94022 (US).
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(54) Title: CONFIGURABLE WIRELESS INTERFACE

(57) Abstract: A multistandard RF transceiver is disclosed that may optionally include selectable mixers; selectable amplifiers; a configurable analog filter; and a configurable analog to digital converter. The multistandard RF transceiver may also include a data interface for sending data to a host controller and a control interface for receiving configuration commands from the host controller. The configuration commands identify a wireless standard that is to be implemented by the RF receiver. An RF processor processes an RF signal wherein the processed RF signal is output to the host controller on the data interface.

CONFIGURABLE WIRELESS INTERFACE

FIELD OF THE INVENTION

The present invention relates generally to wireless communication. More specifically, a configurable wireless interface is disclosed.

BACKGROUND OF THE INVENTION

5 With the increasing popularity of portable computing devices and wireless connectivity, there has been a proliferation of wireless communication standards and protocols. For example, a Personal Digital Assistant (PDA) may communicate with several other portable or non portable devices wirelessly and run wireless
10 applications. Such a PDA may at different times (and in some cases, concurrently) implement WLAN, Bluetooth, GPS, Cellular, Cordless or other RF applications. Currently, each such application requires its own software and hardware and as a result each application that is enabled contributes individually to the cost of the portable device. In addition, each application is generally configured in the device
15 before the device is sold, or in some cases purchased as a hardware add on.

It would be very useful if a device could be developed that could be configured and reconfigured to implement different wireless applications and protocols as desired. Furthermore, if such a device could use common hardware or reconfigurable software resources to implement different protocols or applications,
20 then the cost of potentially including a large selection of applications in a device could be reduced. What is needed, therefore, is a configurable wireless interface that

could be included in a device to allow that device to be configured to run multiple wireless applications.

SUMMARY OF THE INVENTION

It should be appreciated that the present invention can be implemented in numerous ways, including as a process, an apparatus, a system, a device, a method, or a computer readable medium such as a computer readable storage medium or a computer network wherein program instructions are sent over optical or electronic communication links. Several inventive embodiments of the present invention are described below.

10 A configurable wireless interface is disclosed. In one embodiment, a multistandard RF receiver includes a plurality of selectable mixers; a plurality of selectable amplifiers; a configurable analog filter; and a configurable analog to digital converter.

In one embodiment, a multistandard RF transmitter includes a plurality of selectable mixers; a plurality of selectable amplifiers; a configurable analog filter; and a configurable analog to digital converter.

In one embodiment, a multistandard RF receiver includes a data interface for sending data to a host controller and a control interface for receiving configuration commands from the host controller. The configuration commands identify a wireless standard that is to be implemented by the RF receiver. An RF processor processes an RF signal wherein the processed RF signal is output to the host controller on the data interface.

In one embodiment, a multistandard RF transmitter includes a data interface for receiving data from a host controller and a control interface for receiving configuration commands from the host controller. The configuration commands identify a wireless standard that is to be implemented by the RF transmitter. An RF processor processes an RF signal. The processed RF signal is transmitted in accordance with the wireless standard.

These and other features and advantages of the present invention will be presented in more detail in the following detailed description and the accompanying figures which illustrate by way of example the principles of the invention.

10

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and in which:

15 Figure 1 is a block diagram illustrating how a modular RF interface interacts with a host.

Figure 2A is a diagram illustrating an architecture used in one embodiment of a modular wireless interface that includes an RF/IF system with both a transmitter and a receiver.

20 Figure 2B is a diagram illustrating in detail a configurable signal path between the amplifiers, mixers, and digital filter shown in Figure 2A on the receive side.

Figure 2C is a diagram illustrating in detail a configurable signal path between the amplifiers, mixers, and digital filter shown in Figure 2A on the transmit side.

Figure 3 is a diagram illustrating a feature register included in the modular RF interface.

5 Figure 4A is a diagram illustrating an application table for the transmit side included in a control database as shown in Figure 1.

Figure 4B is a diagram illustrating an application table for the transmit side included in a control database as shown in Figure 1.

10 Figure 5 is a flow chart illustrating a process for programming the modular RF interface to include a new application by adding a new application table.

Figure 6 is a flow chart illustrating a process for configuring the modular RF interface to implement a selected application.

Figure 7 is a flow chart illustrating a process for the modular RF interface reporting to a host the features that are available.

15 Figure 8 is a flow chart illustrating a process for the programming of the control interface.

DETAILED DESCRIPTION

A detailed description of a preferred embodiment of the invention is provided below. While the invention is described in conjunction with that preferred
20 embodiment, it should be understood that the invention is not limited to any one

embodiment. On the contrary, the scope of the invention is limited only by the appended claims and the invention encompasses numerous alternatives, modifications and equivalents. For the purpose of example, numerous specific details are set forth in the following description in order to provide a thorough understanding of the present invention. The present invention may be practiced according to the claims without some or all of these specific details. For the purpose of clarity, technical material that is known in the technical fields related to the invention has not been described in detail so that the present invention is not unnecessarily obscured.

Figure 1 is a block diagram illustrating how a modular RF interface 100 interacts with a host 102. Host 102 includes a data interface 104 and a control interface 106. Host processor 108 uses control interface 106 to first determine the features that are enabled for modular RF interface 100 and then to select a feature. Host processor 108 then uses data interface 104 to send data to the modular RF interface for transmission and to receive data from the modular RF interface.

Modular RF interface 100 likewise includes a data interface 114 and a control interface 116. Modular RF interface 100 also includes a feature register 118 that communicates with control interface 116 and is described further in Figure 3. Feature register 118 stores a code that indicates features that have been programmed into the modular RF interface. Control interface 116 also communicates with control database 120 to select a feature when a feature selection is made by the host processor. Control database 120 includes a table for each application that may be selected that includes various parameters used to program the modular RF interface to support the selected application.

In some embodiments, programming interface 122 is provided to write new application tables to control database 120 or to edit existing application tables. By loading new parameters for an application, the modular RF interface can be configured to support a new application or an updated existing application without a hardware change. The RF interface is engineered or re-engineered by software input to the programming interface. This flexible design allows new applications to be installed in the modular RF interface and made available to the host by simply downloading the required parameters.

It should be noted that programming interface 122 may logically and/or physically be a separate interface as shown in Figure 1 or may alternatively be implemented as part of control interface 116. A special code or sequence may be used to indicate a programming mode where the control database is being updated instead of an operating mode where an application table is being selected to obtain parameters for loading into the modular RF interface. It should also be noted that in some embodiments, the control database is not programmable and is contained in ROM that is configured before the chip is sold and is not writeable. However, the ability to program new applications and modify old applications on the modular RF interface and therefore potentially add new functionality to the modular RF interface and the host is an important feature in many embodiments.

When an application table is selected, the data from the table is used to configure various devices included in RF processor 124. RF processor 124, once configured, receives data from the host via data interface 114 for transmission and/or receives a signal from an antenna for processing and returns the processed signal to

the host. Data interface 114 may be any suitable interface capable of exchanging data between the host and the modular RF interface. In one embodiment, data interface 114 is a serial interface. In embodiments that plug the modular RF interface into a legacy application, data interface 114 may include a remodulator that recreates a
5 signal that is processed by a conventional baseband processor on the host.

Figure 2A is a diagram illustrating an architecture used in one embodiment of a modular wireless interface that includes an RF/IF system with both a transmitter and a receiver. Preferably, this system is contained on a single chip 200. In one embodiment, the system is implemented on separate chips with a high speed interface
10 provided between the chips. It should be noted that in some embodiments, a transmitter only or a receiver only may be implemented.

On the transmit side, in the embodiment shown, three possible antenna inputs 202 are shown. The signal paths from each of the antennas are shown separately through amplifiers 204 which are preferably low noise amplifiers and mixers 206
15 which are driven by local oscillator 205 controlled by a digital synthesizer 207. In some embodiments, a common amplifier may be used by the different antennas by implementing a series of switches to select the desired antenna. Likewise, in some embodiments, a common antenna may be shared by different amplifiers by implementing a series of switches or other appropriate arrangement.

20 It should be noted that in other embodiments, different numbers of signal paths may be included. Also, in some embodiments, a signal path may be used for more than one application. For example, one signal path may be used for GSM, GPRS, and EDGE. In general, the low noise amplifier and the mixer are determined

by the frequency band of the application or wireless protocol that is being implemented. Applications that may be implemented in a signal path include WCDMA, or GSM, GPRS, and EDGE or TDMA, CDMA and CDMA 2000-xx or wireless LANs, Bluetooth, cordless phones and GPS or DCS1800 and PCS or PCS
5 1900. Other applications may be included as well.

Filter 208 receives a signal from the selected signal path that includes a selected amplifier and mixer. Filter 208 is programmed according to a selected application to appropriately provide anti aliasing and/or image rejection. In one embodiment, filter 208 is a low pass filter and the frequency cutoff is programmed
10 according to the selected application. Filter 208 may also be a bandpass filter. In one embodiment, filter 208 is an active or passive RC filter and a switchable array of capacitors or resistors or both is programmed to select the required components for a given response. The output of filter 208 is input to an analog to digital converter (ADC) 210. The digital output of ADC 210 is processed by a digital signal processor
15 (DSP) 212. DSP 212 is reconfigurable and is programmed to process the signal in a manner that varies with the selected application. In general, DSP 212 processes both I and Q channel signals received from ADC 210. DSP 212 may also be configured to process a signal that is being transmitted.

In some embodiments, the signal is not converted all the way down to
20 baseband in the analog domain and DSP 212 includes a numerical oscillator that down converts the signal in the digital domain the remainder of the way to baseband from the intermediate frequency achieved by the selected mixer and digitally controlled local oscillator.

In one embodiment, DSP 212 is configured to perform all baseband processing of the signal. However, in different embodiments, various signal processing functions may be performed off chip by a host processor. For example, voice processing, coding/decoding, and error correction may be performed on the host processor while
5 modulation and demodulation, equalization and filtering are performed by the on chip transceiver using DSP 212. A host controller function may be implemented partly on chip and partly on the host. In certain embodiments, for the purpose of communicating with a legacy system that includes a baseband processor configured to receive an analog IF signal input, DAC 214 is provided to remodulate the signal to
10 communicate with baseband processor 216. The baseband processor preferably is implemented on the host. In some embodiments, a dedicated baseband processor chip may be used.

In a similar manner, the transmit side includes programmable components that are configured to work with different applications such as the ones listed above as
15 well as separate components included in alternative signal paths. An analog signal may be received from baseband processor 216 if a legacy device is being used. ADC 234 converts an analog input to a digital signal to be processed by DSP 212. Alternatively, a digital signal may be input to the chip using a suitable digital interface. DSP 212 encodes and/or modulates the signal according to the selected
20 application and provides an output to DAC 230. The output of DAC 230 is filtered by a programmable analog filter 228. The output of filter 228 is selectably routed to a signal path that includes a mixer 226 and an amplifier 224. The output of amplifier 224 is sent to a transmit antenna or transmitting system. In some embodiments, the separate signal paths may be combined.

In some embodiments, the transmitter may additionally be reconfigured to include digital up conversion. Also, the transmitter mode may be switched to a translational loop architecture for constant envelope modulation schemes such as GSM.

5 Figure 2B is a diagram illustrating in detail a configurable signal path between the amplifiers, mixers, and digital filter shown in Figure 2A on the receive side. Switch 250 selects an amplifier and switches 252 and 254 select a mixer. Other signal paths are used in other embodiments. For example, the mixer and amplifier may be selected as a pair.

10 Figure 2C is a diagram illustrating in detail a configurable signal path between the amplifiers, mixers, and digital filter shown in Figure 2A on the transmit side. Switch 260 selects an amplifier and switches 262 and 264 select a mixer. Other signal paths are used in other embodiments. For example, the mixer and amplifier may be selected as a pair.

15 The transceiver architecture shown shows a configurable signal path using switches as well as individually configurable components that are reprogrammed and reused in different modes. In other embodiments, the signal path is configured in other manners and different configurable components may be selected. However, the benefit of reusing certain components is still enjoyed. In particular, the common DSP
20 greatly reduces the amount of area required to implement the different protocols.

Figure 3 is a diagram illustrating a feature register included in the modular RF interface. For the purpose of illustration, a 16 bit register is shown wherein each bit corresponds to an application that may be implemented by the modular RF interface.

In other embodiments, applications may be represented by more complex codes for the purpose of security. In the example shown, bits are labeled that correspond to a GPS, a wireless LAN, and a CDMA feature.

Figure 4A is a diagram illustrating an application table for the transmit side included in control database 120 as shown in Figure 1. The application table includes various parameters that are used to either select a signal path by switching between amplifiers and mixers or to configure components such as a filter, an ADC or a DAC. Application table 400 includes an application ID 402 that is used to match an application ID specified by the host for the purpose of selecting the application table. A low noise amplifier identifier 404 selects a low noise amplifier and a mixer identifier 406 selects a mixer. A local oscillator/IF identifier specifies an IF and selects or programs a local oscillator. Identifiers 402, 404, and 406 select or configure the signal path that leads to the programmable analog filter as shown in Figure 4A.

The programmable analog filter is programmed according to filter parameters 410 which define the analog filter response. It should be noted that each of the parameters shown may be an array of parameters or a pointer to a data structure that contains the parameter or set of parameters.

The ADC is configured according to the ADC parameters 416 and 418. Parameter 416 specifies the ADC sample rate and Parameter 418 specifies the ADC precision. Other ADC parameters are specified in other embodiments. By specifying the filter parameters and the ADC parameters, the filter and ADC are configured to

operate for different applications. The reuse of the ADC and filter components for different applications greatly reduces the cost of the modular RF interface.

If a digital down conversion is performed, then parameter 420 may be used to specify a numerical oscillator or digital IF. Digital filter parameters may also be specified. For example, parameter 422 specifies digital filter coefficients; and parameter 424 specifies digital filter taps.

If a DAC is used after the DSP to generate an analog signal for a legacy interface to communicate with the baseband processor, then analog interface identifier 426 may be included to indicate the type of analog waveform that is to be generated.

In general, different analog waveforms may be generated for different types of baseband processors. In one embodiment, either a digital or an analog PLL is used to generate a timing signal for the legacy or digital interface. A digital or analog PLL may be used with the DAC or digital interface for the baseband or host processor and support various types of timing and data formatting. The PLL can generate different phase or frequency through programming. Parameter 428 is used to program various kinds of timing and data formatting.

Figure 4B is a diagram illustrating an application table for the transmit side included in control database 120 as shown in Figure 1. The application table includes various parameters that are used to either select a signal path by switching between amplifiers and mixers or to configure components such as a filter, an ADC or a DAC. Application table 450 includes an application ID 452 that is used to match an application ID specified by the host for the purpose of selecting the application table. A power amplifier driver identifier 454 selects a low noise amplifier and a mixer

identifier 456 selects a mixer. A local oscillator/IF identifier specifies an IF and selects or programs a local oscillator. Identifiers 452, 454, and 456 select or configure the signal path that leads to the programmable analog filter as shown in Figure 4A.

- 5 The programmable analog filter is programmed according to filter parameters 460 which define the analog filter response. It should be noted that each of the parameters shown may be an array of parameters or a pointer to a data structure that contains the parameter or set of parameters.

The DAC is configured according to the DAC parameters 416 and 418.

- 10 Parameter 416 specifies the DAC sample rate and Parameter 418 specifies the DAC precision. Other DAC parameters are specified in other embodiments. By specifying the filter parameters and the DAC parameters, the filter and DAC are configured to operate for different applications. The reuse of the DAC and filter components for different applications greatly reduces the cost of the modular RF interface.

- 15 If a digital up conversion to a digital IF is performed, then parameter 420 may be used to specify a numerical oscillator or digital IF. Digital filter parameters may also be specified. For example, parameter 422 specifies digital filter coefficients; and parameter 424 specifies digital filter taps. If an ADC is used before the DSP in the transmit path to receive an analog signal from the baseband processor, then analog
- 20 interface identifier 476 may be included to indicate the type of analog waveform is to be received. In general, different analog waveforms may be generated by different types of baseband processors. In one embodiment, either a digital or an analog PLL is used to generate a timing signal for the legacy or digital interface. A digital or analog

PLL may be used with the ADC or digital interface to receive the data from the baseband or host processor and provide various type of timing and identify the data formatting. The PLL can generate different phase or frequency through programming. Parameter 4478 is used to program various kind of timing and data formatting.

5 It should be noted that in other embodiments, different data structures are used to configure or select components for the modular RF interface. The disclosed table format is one of many structures that may be used as is deemed appropriate for a specific system.

 In a similar manner, identifiers and parameters are also specified on the
10 transmit side so that the transmit signal path is selected and the transmit DAC and analog filter are configured.

 Figure 5 is a flow chart illustrating a process for programming the modular RF interface to include a new application by adding a new application table. The process starts at 500. In step 502, the new application table is received. Next, in step 504, the
15 application table is confirmed or checked for errors. Any standard technique for doing this may be implemented including hashing the table and checking the hash value. In step 506, the application register (as shown in Figure 3) is updated to indicate that the new application is available on the modular RF interface.

 Figure 6 is a flow chart illustrating a process for configuring the modular RF
20 interface to implement a selected application. The process starts at 600. In step 602, an application identifier is received. In step 604, application parameters are retrieved from the application table that corresponds to the application identifier. In step 606,

the application parameters are loaded to configure devices. Finally, in step 608, devices are selected according to the application parameters. The process ends at 610.

Figure 7 is a flow chart illustrating a process for the modular RF interface reporting to a host the features that are available. The process starts at 700. In step 702, an inquiry for the feature registry is received. In step 704, the feature registry is retrieved. In step 706, the feature registry is transmitted. The process ends at 708. It should be noted that in some embodiments, the feature registry may be directly accessed by the host.

In some embodiments, depending on the host or baseband processor, it may be desirable to program the control/data interface, protocol or signaling. The programming interface supports this programming. Figure 8 is a flow chart illustrating a process for the programming of the control interface. The process starts at 800. In a step 802, a control/data path format table is received. In step 804, the table is checked for errors. If errors are found, then the system waits until a correct format table is received. In some embodiments, the system requests that the format table be resent. The system also may fail to acknowledge the table and then wait for the format table to be resent. Once the table is confirmed, the control/data path registers are updated in step 806. The process ends at 808.

A modular RF interface has been described. The modular RF interface is configurable to support different applications by selecting a set of stored parameters that select a signal path and configure components. The modular RF interface may be programmed to support additional applications by loading in configuration data for such applications.

Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. It should be noted that there are many alternative ways of implementing both the process and
5 apparatus of the present invention. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.

WHAT IS CLAIMED IS:

CLAIMS

1. A multistandard RF receiver comprising:
a plurality of selectable mixers;
a plurality of selectable amplifiers;
5 a configurable analog filter; and
a configurable analog to digital converter.
2. A multistandard RF transmitter comprising:
a plurality of selectable mixers;
10 a plurality of selectable amplifiers;
a configurable analog filter; and
a configurable digital to analog converter.
3. A multistandard RF receiver comprising:
15 a data interface for sending data to a host controller;
a control interface for receiving configuration commands from the host
controller wherein the configuration commands identify a wireless standard that is to
be implemented by the RF receiver; and
an RF processor for processing an RF signal wherein the processed RF signal
20 is output to the host controller on the data interface.
4. A multistandard RF receiver as recited in claim 3 further including a feature
register for storing information about wireless standards supported by the device.
- 25 5. A multistandard RF receiver as recited in claim 3 further including a control
database for storing parameters for implementing the wireless standard.
6. A multistandard RF receiver as recited in claim 3 wherein the RF receiver
includes a configurable signal path.
- 30 7. A multistandard RF receiver as recited in claim 3 wherein the RF receiver
includes configurable components.

8. A multistandard RF receiver as recited in claim 3 wherein the RF receiver includes a configurable analog filter.
- 5 9. A multistandard RF receiver as recited in claim 3 wherein the RF receiver includes configurable analog to digital converter.
10. A multistandard RF receiver as recited in claim 3 wherein the RF receiver includes plurality of selectable mixers.
- 10 11. A multistandard RF receiver as recited in claim 3 wherein the RF receiver includes plurality of selectable amplifiers.
12. A multistandard RF transmitter comprising:
- 15 a data interface for receiving data from a host controller;
a control interface for receiving configuration commands from the host controller wherein the configuration commands identify a wireless standard that is to be implemented by the RF transmitter; and
an RF processor for processing an RF signal wherein the processed RF signal
20 is transmitted in accordance with the wireless standard.
13. A multistandard RF transmitter as recited in claim 12 further including a feature register for storing information about wireless standards supported by the device.
- 25 14. A multistandard RF transmitter as recited in claim 12 further including a control database for storing parameters for implementing the wireless standard.
15. A multistandard RF transmitter as recited in claim 12 wherein the RF
30 transmitter includes a configurable signal path.
16. A multistandard RF transmitter as recited in claim 12 wherein the RF transmitter includes configurable components.

17. A multistandard RF transmitter as recited in claim 12 wherein the RF transmitter includes a configurable analog filter.
18. A multistandard RF transmitter as recited in claim 12 wherein the RF transmitter includes configurable digital to analog converter.
19. A multistandard RF transmitter as recited in claim 12 wherein the RF transmitter includes plurality of selectable mixers.
20. A multistandard RF transmitter as recited in claim 12 wherein the RF transmitter includes plurality of selectable amplifiers.
21. A multistandard RF transceiver comprising:
a plurality of selectable mixers;
a plurality of selectable amplifiers; and
a configurable digital signal processor that is configured to process a received signal or a signal that is being transmitted.
22. A method of processing an RF signal including:
receiving configuration information from a host processor;
configuring a signal path in accordance with the configuration information;
and
configuring components in accordance with the configuration information.
23. A host processor for interacting with a multistandard RF transceiver comprising:
a data interface for transmitting data to and receiving data from the multistandard RF transceiver; and
a control interface for sending configuration information to the multistandard RF transceiver.
24. A host processor for interacting with a multistandard RF transceiver as recited in claim 23 wherein the host processor receives information from the multistandard

RF transceiver indicating the standards that are supported by the multistandard RF transceiver for interacting with a host processor.

25. A multistandard RF receiver comprising:
5 an RF processor for processing an RF signal;
a digital to analog converter for converting the processed RF signal to a digital signal;
a digital signal processor for manipulating the digital signal; and
a programmable interface for outputting the processed signal.
10
26. A multistandard RF receiver as recited in claim 25 wherein the programmable interface includes a digital to analog converter for generating an analog signal.
27. A multistandard RF receiver as recited in claim 25 wherein the programmable
15 interface includes a programmable PLL.
28. A multistandard RF transmitter comprising:
a programmable interface for receiving a signal to be transmitted;
a digital signal processor for outputting a processed signal from the
20 programmable interface for transmitting;
an analog to digital converter for converting the processed signal to an analog signal; and
an RF processor for processing the analog signal.
- 25 29. A multistandard RF transmitter as recited in claim 28 wherein the programmable interface includes an analog to digital converter for converting the signal to be transmitted to a digital signal.
30. A multistandard RF transmitter as recited in claim 28 wherein the
30 programmable interface includes a programmable PLL.
31. A multistandard RF transceiver comprising:
a modular RF interface;
a control database having parameters for programming the RF interface;

a programming interface configured to receive updates for the control database.

32. A multistandard RF transceiver as recited in claim 31 wherein the
5 programming interface is activated by a code that indicates that the control database is
to be updated.

33. A multistandard RF transceiver as recited in claim 31 wherein the
programming interface is separate from an interface used to select a set of values in
10 the control database for programming the RF interface.

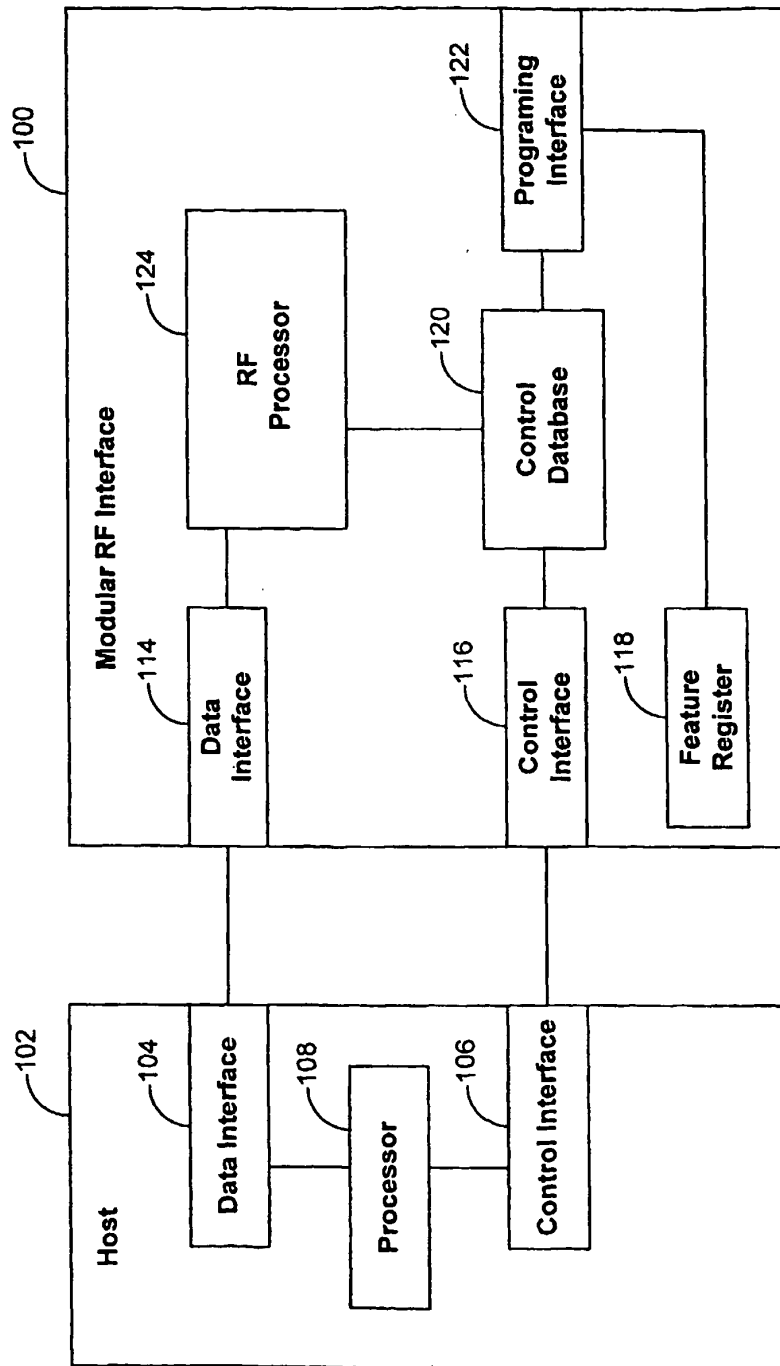


Figure 1

SUBSTITUTE SHEET (RULE 26)

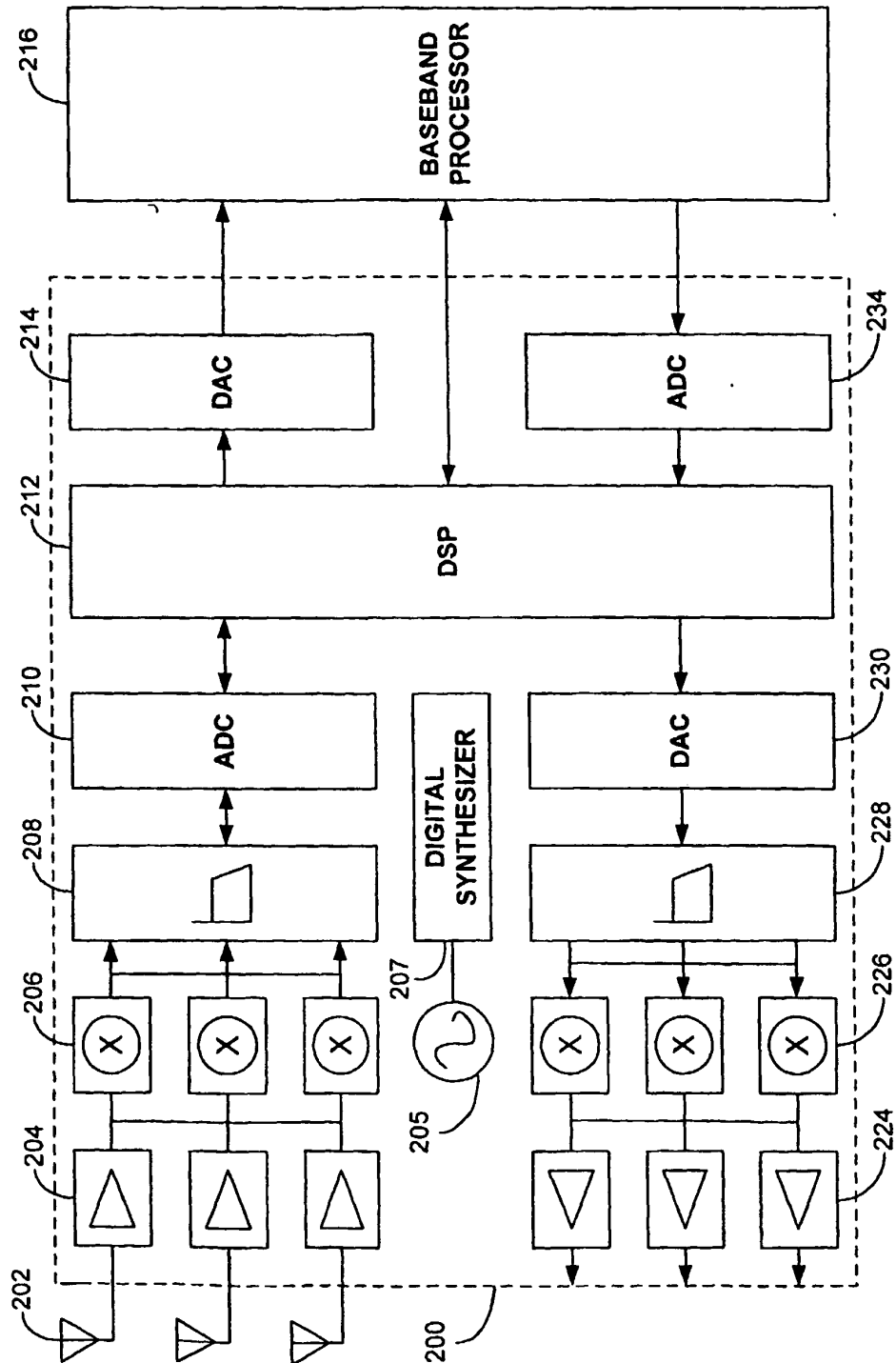


Figure 2A

SUBSTITUTE SHEET (RULE 26)

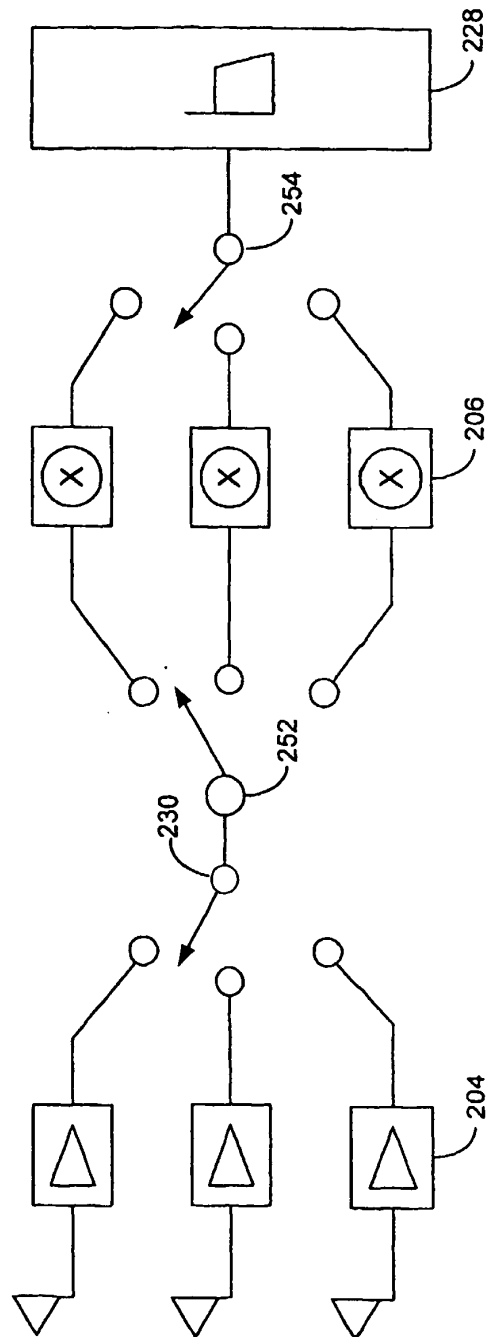


Figure 2B

SUBSTITUTE SHEET (RULE 26)

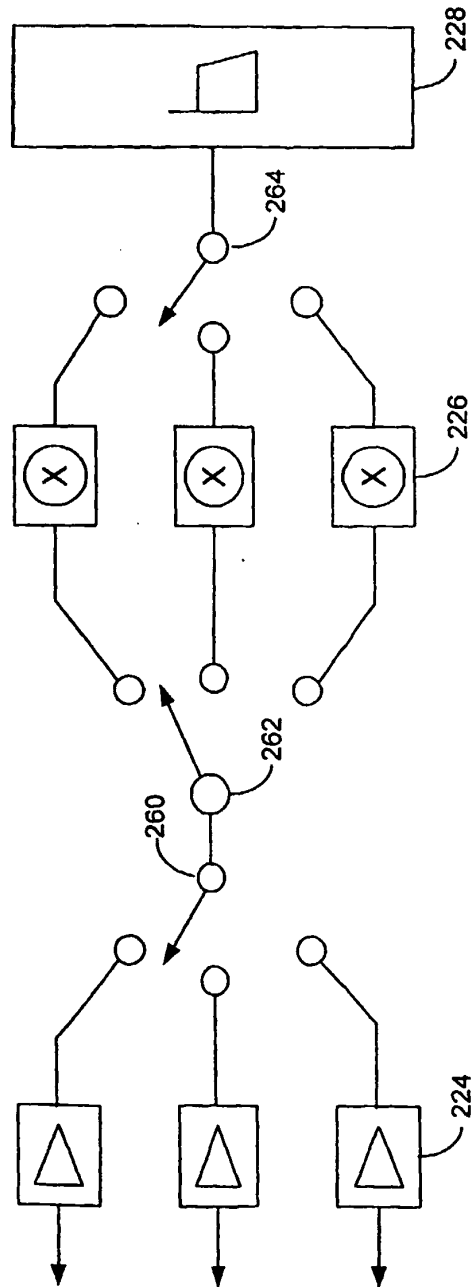
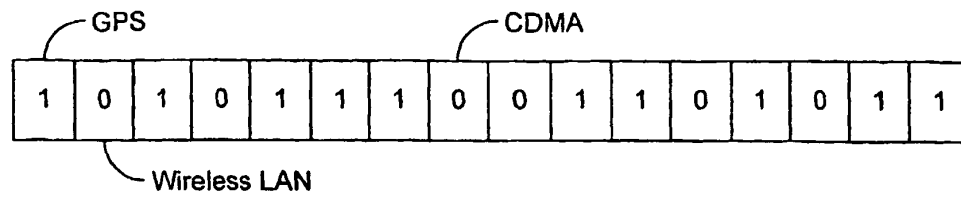


Figure 2C

SUBSTITUTE SHEET (RULE 26)

**Figure 3**

SUBSTITUTE SHEET (RULE 26)

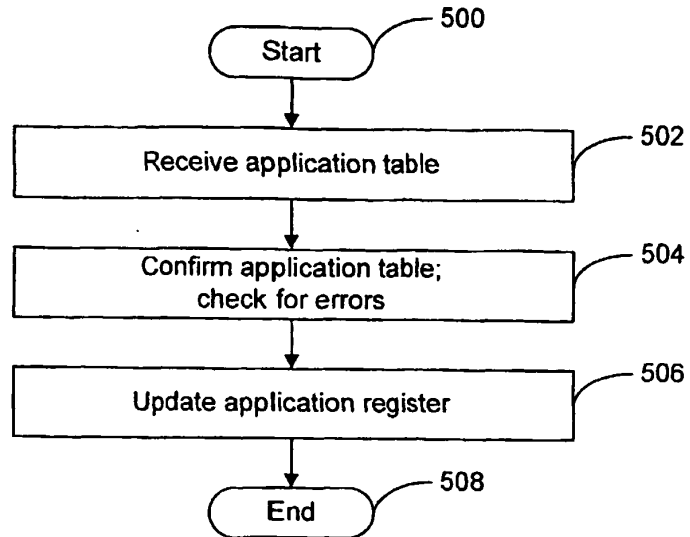
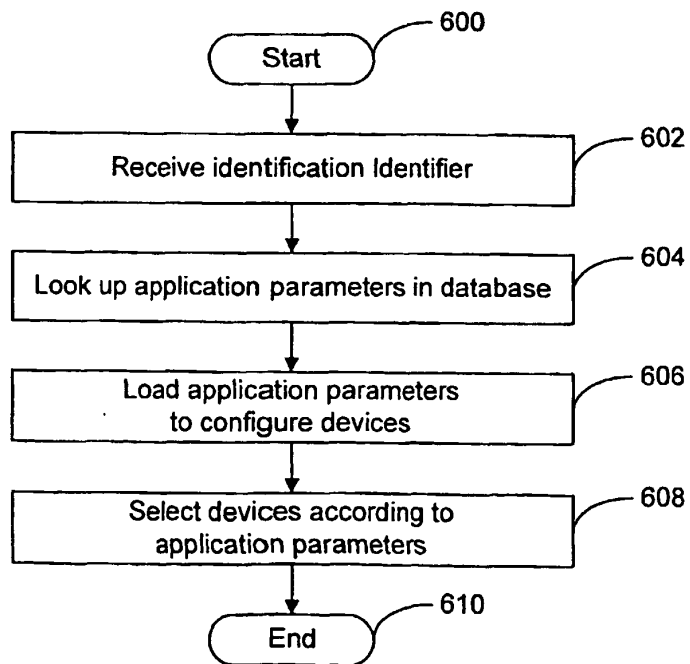
Application ID	452
Power Amplifier Driver	454
Mixer	456
Local Oscillator/IF	458
Analog Filter Parameters	460
DAC Sample Rate	466
DAC Precision	468
Numerical Oscillator/Digital IF	470
Digital Filter Coefficients	472
Digital Filter Taps	474
Analog Interface	476

Figure 4B

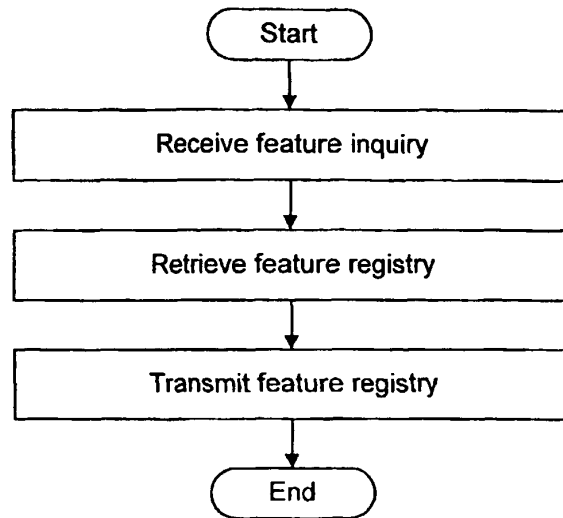
Application ID	402
Low Noise Amplifier	404
Mixer	406
Local Oscillator/IF	408
Analog Filter Parameters	410
ADC Sample Rate	416
ADC Precision	415
Numerical Oscillator/Digital IF	420
Digital Filter Coefficients	422
Digital Filter Taps	424
Analog Interface	426
Timing and Formatting	428

Figure 4A

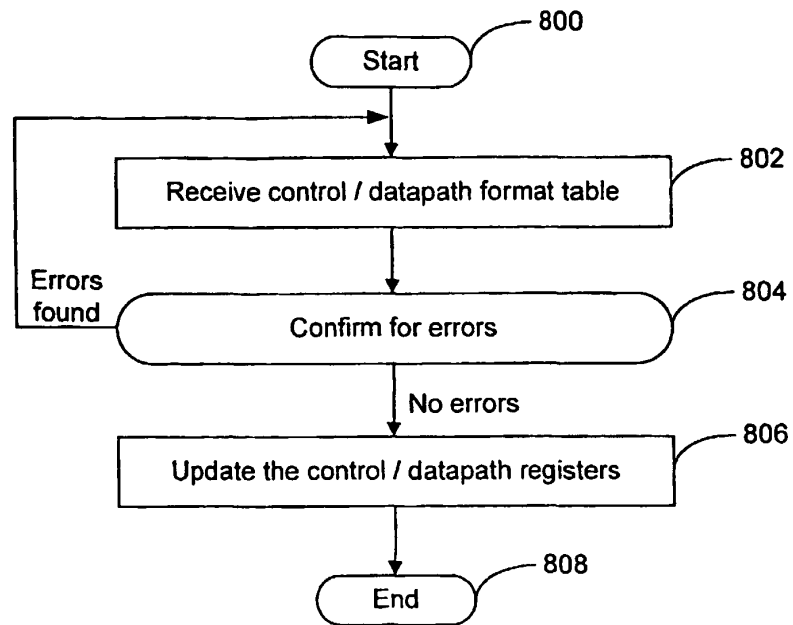
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**Figure 5****Figure 6**

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**Figure 7**

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**Figure 8**

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	97001	second\$4 with (die chip pcb integrated near3 circuit IC semiconductor) with substrat\$4	US-PGPUB; USPAT	OR	ON	2008/01/15 09:40
S2	192	S1 and "455"/\$.ccls. and (@riad<="20031008" @ad<="20030108")	US-PGPUB; USPAT	OR	ON	2008/01/15 09:28



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/857,938	06/02/2004	James H. Derbyshire	115-34USCIP/12667/100126	5643
23838 7590 01/25/2008 KENYON & KENYON LLP 1500 K STREET N.W. SUITE 700 WASHINGTON, DC 20005			EXAMINER LE, NHAN T	
			ART UNIT 2618	PAPER NUMBER
			MAIL DATE 01/25/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/857,938	DERBYSHIRE ET AL.	
	Examiner	Art Unit	
	Nhan T. Le	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 June 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-17 and 27-32 is/are allowed.
- 6) ☒ Claim(s) 18, 20, 22-24, 26 is/are rejected.
- 7) ☒ Claim(s) 19, 21 and 25 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413) |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) ☒ Information Disclosure Statement(s) (PTO/SB/08) | 5) ☐ Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>11/01/05, 05/17/05</u> | 6) ☐ Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35

U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 18, 20, 22-24, 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Kimura (US 6,734,553).

As to claim 18, Kimura teaches a method of manufacturing a module comprising: providing a first signal conditioning circuit comprising a first portion and a second portion (see fig. 1, numbers 11, 21, col. 4, lines 40-51); implementing the first portion of the first signal conditioning circuit within a first semiconductor die (see fig. 1, numbers 11, 21, col. 4, lines 40-51); implementing the second portion of the first signal conditioning circuit within a second semiconductor die (see fig. 1, numbers 13, 23, col. 4, lines 40-51); bonding the first and second dies to a common substrate (see col. 4, lines 52-67, col. 5, lines 1-5); and, forming electrical connections between the two dies to complete the first signal conditioning circuit from the first portion of the first signal conditioning circuit and the second portion of the first signal conditioning circuit (see col. 4, lines 52-67, col. 5, lines 1-5).

As to claim 20, Kimura teaches wherein the first semiconductor die

comprises a first portion of a first signal path (see col. 4, lines 52-67, col. 5, lines 1-5) and the second semiconductor die comprises a second portion of the first signal path (see col. 4, lines 52-67, col. 5, lines 1-5), the first signal path disposed between a first input port and a first output port (see col. 5, lines 11-39).

As to claim 22, Kimura teaches wherein the second semiconductor die is manufactured using a more expensive semiconductor process than that used for manufacturing of the first semiconductor die (see col. 6, lines 10-39).

As to claim 23, Kimura teaches wherein the first portion of the first signal conditioning circuit is more cost effectively implemented in the first semiconductor die (see col. 6, lines 10-39).

As to claim 24, Kimura teaches wherein the first semiconductor die does not facilitate implementation of the second portion of the first signal conditioning circuit therein (see col. 5, lines 11-39).

As to claim 26, Kimura teaches wherein prior to implementing the first signal conditioning circuit comprises partitioning of the first signal conditioning circuit into the first portion and the second portion (see col. 5, lines 11-39).

Allowable Subject Matter

2. Claims 19, 21, 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to claim 19, the applied reference fails to teach providing a second signal conditioning circuit comprising a first portion and a second portion; and,

implementing the first and second portions of the second signal conditioning circuit in the second semiconductor die as cited in the claim.

As to claim 21, the applied reference fails to teach wherein the second semiconductor die comprises a second signal path that is other than the second portion of the first signal path and in approximate RF isolation therefrom as cited in the claim.

As to claim 25, the applied reference fails to teach wherein implementing of the second portion of the first signal conditioning circuit within the second semiconductor die provides increased performance in signal conditioning as compared to implementing of the second portion of the first signal conditioning circuit within the first semiconductor die as cited in the claim.

3. Claims 1-17, 27-32 are allowed over the prior art.

As to claim 1, Kimura (US 6,734,553) teaches semiconductor device; Oida et al (US 7,245,884) teaches RF schedule; Tamaki et al (US 7,164,905) teaches high frequency module; Ishida et al (US 6,054,900) teaches power amplifier MMIC and mobile communication terminal; Mohwinkel et al (US 5,983,089) teaches slotline mounted flip chip. The teaching of these prior arts either combine or alone fails to teach a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first portion of a first signal conditioning circuit for a signal propagating along the first signal path.

Dependent claims 2-17 are allowable for the same reason.

As to claim 27, Kimura (US 6,734,553) teaches semiconductor device; Oida et al (US 7,245,884) teaches RF schedule; Tamaki et al (US 7,164,905) teaches high frequency module; Ishida et al (US 6,054,900) teaches power amplifier MMIC and mobile communication terminal; Mohwinkel et al (US 5,983,089) teaches slotline mounted flip chip. The teaching of these prior arts either combine or alone fails to teach a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first and third portions of the first signal conditioning circuit for a signal propagating along the first signal path.

Dependent claims 28-32 are allowable for the same reason.

Conclusion

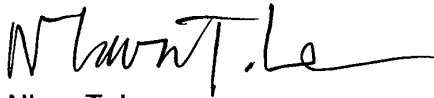
4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Le whose telephone number is 571-272-7892. The examiner can normally be reached on 08:00-05:00 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on 571-272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number:
10/857,938
Art Unit: 2618

Page 6

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

A handwritten signature in black ink, appearing to read 'Nhan T. Le', with a long horizontal flourish extending to the right.

Nhan T. Le

Notice of References Cited	Application/Control No. 10/857,938	Applicant(s)/Patent Under Reexamination DERBYSHIRE ET AL.	
	Examiner Nhan T. Le	Art Unit 2618	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,734,553	05-2004	Kimura, Naoto	257/723
*	B	US-7,245,884	07-2007	Oida et al.	455/90.3
*	C	US-7,164,905	01-2007	Tamaki et al.	455/403
*	D	US-6,054,900	04-2000	Ishida et al.	330/286
*	E	US-5,983,089	11-1999	Mohwinkel et al.	455/323
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
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	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



Substitute form for form 1449A & 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application No.	10/857,938
		Filing Date	June 2, 2004
		First Named Inventor	Derbyshire et al.
		Group Art Unit	2681 2618
		Examiner Name	Unknown N. L.
Sheet 1 of 1	Attorney Docket No.	115-34 US CIP/12667/100126	

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
N.L.		5,258,325		Spitzer et al.	11-02-1993	—
		5,731,945		Bertin et al.	03-24-1998	—

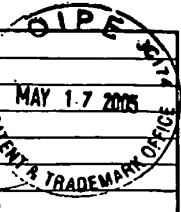
FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
N.L.		EPO	0 543 430	A2	Delco Electronics Corporation	05-26-2003	—	
			WO 96/13965		Baier & Baier, Inc.	05-09-1996	—	
		EPO	0 436 074	A1	International Business Machines Corporation	07-10-1991	—	
		EPO	1 385 305	A1	Broadcom Corporation	01-28-2004	—	
			WO 03/061174	A2	Berkana Wireless Inc.	07-24-2003	—	
		JP	2001298123		Hitachi Ltd.	10-26-2001	—	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in capital letters), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶	

Examiner Signature	N. L.	Date Considered	01/15/08
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1 Unique citation designation number. 2 See attached Kinds of U.S. Patent Documents. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

Substitute form for form 1449A & 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application No.	10/857,938
		Filing Date	June 2, 2004
		First Named Inventor	Derbyshire et al.
		Group Art Unit	2881 2678
		Examiner Name	Unknown N. Le
Sheet 1 of 1	Attorney Docket No.	115-34 US CIP/12667/100126	



U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
Nle		5,258,325		Spitzer et al.	11-02-1993	—
e		5,731,945		Bertin et al.	03-24-1998	—

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. 1	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in capital letters), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T ⁶
Nle		Guckenberger et al., "Integrated DC-DC Converter Design for Improved WCDMA Power Amplifier Efficiency in SiGe BiCMOS Technology", Proceedings of the 2003 International Symposium on Low Power Electronics and Design ISLPED '03, Aug. 25-27, 2003, pp. 449-454		—
Nle		Diels et al., "Single Package Integration of RF Blocks for a 5 Ghz WLAN Application", IEEE Transactions on Advanced Packaging, vol. 24, no. 3, August 2001, pp. 384-391		←

Examiner Signature	N. Le	Date Considered	01/15/08
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1 Unique citation designation number. 2 See attached Kinds of U.S. Patent Documents. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

Index of Claims



Application/Control No.

10/857,938

Examiner

Nhan T. Le

Applicant(s)/Patent under Reexamination

DERBYSHIRE ET AL.

Art Unit

2618

✓	Rejected
=	Allowed

—	(Through numeral) Cancelled
+	Restricted

N	Non-Elected
I	Interference

A	Appeal
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Claim	Date
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BIB DATA SHEET

CONFIRMATION NO. 5643

SERIAL NUMBER 10/857,938	FILING or 371(c) DATE 06/02/2004 RULE	CLASS 455	GROUP ART UNIT 2618 115-34USCIP/12667/100126	ATTORNEY DOCKET NO.	
APPLICANTS James H. Derbyshire, Ottawa, CANADA; Alan J.A. Trainor, Harlow, UNITED KINGDOM; ** CONTINUING DATA ***** This application is a CIP of 10/680,208 10/08/2003 <i>Yes Nile</i> ** FOREIGN APPLICATIONS ***** <i>No Nile</i> ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** ** SMALL ENTITY ** 07/23/2004					
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <i>N. Trainor</i> Examiner's Signature <i>Le</i> Initials		STATE OR COUNTRY CANADA	SHEETS DRAWINGS 6	TOTAL CLAIMS 35	INDEPENDENT CLAIMS 3
ADDRESS KENYON & KENYON LLP 1500 K STREET N.W. SUITE 700 WASHINGTON, DC 20005 UNITED STATES					
TITLE Module integration integrated circuits					
FILING FEE RECEIVED 520	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Search Notes (continued)



Application/Control No.

10/857,938

Examiner

Nhan T. Le

Applicant(s)/Patent under
Reexamination

DERBYSHIRE ET AL.

Art Unit

2618

SEARCHED

Class	Subclass	Date	Examiner
257	723 724 784	06/15/08	N/le
455	2621		
	329,333	✓	✓

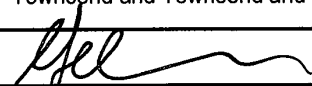
INTERFERENCE SEARCHED

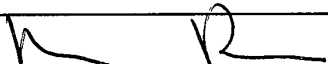
Class	Subclass	Date	Examiner

**SEARCH NOTES
(INCLUDING SEARCH STRATEGY)**

	DATE	EXMR
First search	01/15/08	

TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10857938 (Confirm. No. 5643)	
	Filing Date	June 2, 2004	
	First Named Inventor	James Derbyshire	
	Art Unit	2618	
	Examiner Name	Le, Nhan T	
Total Number of Pages in This Submission	3	Attorney Docket Number	027066-001510US

ENCLOSURES (Check all that apply)			
☐ Fee Transmittal Form ☐ Fee Attached ☐ Amendment/Reply ☐ After Final ☐ Affidavits/declaration(s) ☐ Extension of Time Request ☐ Express Abandonment Request ☐ Information Disclosure Statement ☐ Certified Copy of Priority Document(s) ☐ Reply to Missing Parts/ Incomplete Application ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53	☐ Drawing(s) ☐ Licensing-related Papers ☐ Petition ☐ Petition to Convert to a Provisional Application ☒ Power of Attorney, Revocation Change of Correspondence Address ☐ Terminal Disclaimer ☐ Request for Refund ☐ CD, Number of CD(s) _____ ☐ Landscape Table on CD	☐ After Allowance Communication to TC ☐ Appeal Communication to Board of Appeals and Interferences ☐ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) ☐ Proprietary Information ☐ Status Letter ☒ Other Enclosure(s) (please identify below): Statement Under 37 CFR 3.73(b)	Remarks The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.
SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm Name	Townsend and Townsend and Crew LLP		
Signature			
Printed name	Gary S. Morris		
Date	19 March 2008	Reg. No.	40,735

CERTIFICATE OF TRANSMISSION/MAILING			
I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent and Trademark Office on the date shown below.			
Signature			
Typed or printed name	melissa Possess	Date	3/21/08

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: James H. Derbyshire, et al.

Application No./Patent No.: 10857938 Filed/Issue Date: June 2, 2004

Entitled: MODULE INTEGRATION INTEGRATED CIRCUITS

SiGe Semiconductor Inc., a Corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest; or
2. ☐ an assignee of less than the entire right, title and interest
(The extent (by percentage) of its ownership interest is _____ %)

in the patent application/patent identified above by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 015432, Frame 0084, or for which a copy thereof is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

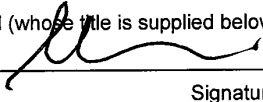
1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
2. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
3. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.



Signature

Gary S. Morris

Printed or Typed Name

Authorized Practitioner
Title

19 March 2008

Date

202-481-9988

Telephone Number

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☒ Practitioners associated with the Customer Number:

20350

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☒ The address associated with Customer Number:

20350

OR

☐ Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone			Email

Assignee Name and Address:

SiGe Semiconductor Inc.
1050 Morrison Drive
Suite 100
Ottawa, Ontario Canada K2H 8K7

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	<i>Steve Kovacic</i>	Date	December 31, 2007
Name	Stephen Kovacic	Telephone	613 820 9244
Title	Director Legal & IP Management		

60094602 v1

Electronic Acknowledgement Receipt

EFS ID:	3036282
Application Number:	10857938
International Application Number:	
Confirmation Number:	5643
Title of Invention:	Module integration integrated circuits
First Named Inventor/Applicant Name:	James H. Derbyshire
Customer Number:	23838
Filer:	Gary S. Morris/Melissa Pessagno
Filer Authorized By:	Gary S. Morris
Attorney Docket Number:	115-34USCIP/12667/100126
Receipt Date:	21-MAR-2008
Filing Date:	02-JUN-2004
Time Stamp:	15:51:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		027066_001510USPOA.PD F	174595 96d3410535c48684d20d2889f29c50f7 5997ff3a	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Miscellaneous Incoming Letter	1	1
	Power of Attorney	2	3
Warnings:			
Information:			
Total Files Size (in bytes):		174595	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of: DERBYSHIRE et al.

Our File: 115-34 USCIP/12667/100126

Application No: 10/857,938

Filed: June 2, 2004

Group Art Unit: 2618

Examiner: Nhan T. LE

Title: Module Integration Integrated Circuits

April 3, 2008

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
U.S.A.

**Supplemental Information Disclosure Statement
- Under 37 CFR 1.97(e)(1)**

Sir:

Applicant submits herewith a Supplemental Information Disclosure Statement (Form PTO-1449) and copies of non-patent documents for Examiner's review.

The documents listed in the IDS were cited in a Supplementary Search Report mailed **February 1, 2008** from the European Patent Office from the corresponding EP application for parent patent application number US 10/680,208 and applicant submits copies of two restriction requirements from the USPTO and their respective responses and a recent Office Action mailed December 26, 2007.

Respectfully submitted,



Gary Morris, Reg. No. 40,735
Townsend and Townsend and Crew LLP
601 Pennsylvania Avenue, N.W.
South Building, Suite 900
Washington, DC 20004-2601
U.S.A.

Tel: (202) 434-8195
Fax: (202) 434-8171

Enclosures: Copy of Form PTO 1449
Copies of non-patent documents

/ds

Substitute form for form 1449A & 1449B/PTO		<i>Complete if Known</i>	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application No.	10/857,938
		Filing Date	June 2, 2004
		First Named Inventor	DERBYSHIRE et al.
		Group Art Unit	2618
		Examiner Name	Nhan T. LE
Sheet 1 of 1	Attorney Docket No.	115-34USCIP/12667/100126	

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
		US 2001/011926	A1	Adar Aharon	08-09-2001	
		US 6,075,995	A	Jensen Niels J.	06-13-2000	
		US 2003/165052	A1	Negishi Mikio et al.	09-04-2003	
		US 5,844,853		Kitsukawa et al.	12-01-1998	

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. 1	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in capital letters), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
		FURST R: "With GaAs Mmics Towards Dual Band Front End Applications In Wireless Communication" EUROPEAN MICROWAVE CONFERENCE. CONFERENCE PROCEEDINGS, vol. 2, 8 September 1997 (1997-09-08), pages 1289-1294, XP010253196	
		USPTO, for US patent application no. 10/680,208, 1 st Restriction Requirement mailed 09/13/2006	
		US patent application no. 10/680,208, response to 1 st Restriction Requirement filed 10/12/2006	
		USPTO, for US patent application no. 10/680,208, 2 nd Restriction Requirement mailed 04/05/2007	
		US patent application no. 10/680,208, response to 2 nd Restriction Requirement filed 05/03/2007	
		USPTO, for US patent application no. 10/680,208, 1 st Office Action mailed 12/26/2007	

Examiner Signature		Date Considered	
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1 Unique citation designation number. 2 See attached Kinds of U.S. Patent Documents. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

Electronic Acknowledgement Receipt

EFS ID:	3098804
Application Number:	10857938
International Application Number:	
Confirmation Number:	5643
Title of Invention:	Module integration integrated circuits
First Named Inventor/Applicant Name:	James H. Derbyshire
Customer Number:	23838
Filer:	Gary S. Morris/Melissa Pessagno
Filer Authorized By:	Gary S. Morris
Attorney Docket Number:	115-34USCIP/12667/100126
Receipt Date:	03-APR-2008
Filing Date:	02-JUN-2004
Time Stamp:	14:41:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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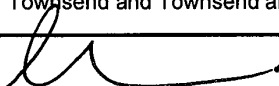
File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		027066_001510US_Response_InformationDisclosureStatement.pdf	1801655 40739322acd70eec07fad5b096cb8d8e1d407799	yes	45

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Miscellaneous Incoming Letter	1	1
	Amendment Copy Claims/Response to Suggested Claims	2	11
	Information Disclosure Statement (IDS) Filed	12	13
	NPL Documents	14	19
	NPL Documents	20	24
	NPL Documents	25	31
	NPL Documents	32	36
	NPL Documents	37	44
	NPL Documents	45	45
Warnings:			
Information:			
Total Files Size (in bytes):		1801655	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

TRANSMITTAL FORM <i>(to be used for all correspondence after initial filing)</i>	Application Number	10/857,938	
	Filing Date	June 2, 2004	
	First Named Inventor	James H. DERBYSHIRE	
	Art Unit	2618	
	Examiner Name	Le, Nhan T.	
Total Number of Pages in This Submission	44	Attorney Docket Number	027066-001510US

ENCLOSURES <i>(Check all that apply)</i>		
☐ Fee Transmittal Form ☐ Fee Attached ☒ Amendment/Reply ☐ After Final ☐ Affidavits/declaration(s) ☐ Extension of Time Request ☐ Express Abandonment Request ☒ Information Disclosure Statement ☐ Certified Copy of Priority Document(s) ☐ Reply to Missing Parts/ Incomplete Application ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53	☐ Drawing(s) ☐ Licensing-related Papers ☐ Petition ☐ Petition to Convert to a Provisional Application ☐ Power of Attorney, Revocation Change of Correspondence Address ☐ Terminal Disclaimer ☐ Request for Refund ☐ CD, Number of CD(s) _____ ☐ Landscape Table on CD	☐ After Allowance Communication to TC ☐ Appeal Communication to Board of Appeals and Interferences ☐ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) ☐ Proprietary Information ☐ Status Letter ☐ Other Enclosure(s) (please identify below):
☐ Remarks The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm Name	Townsend and Townsend and Crew LLP		
Signature			
Printed name	Gary S. Morris		
Date	April 3, 2008	Reg. No.	40,735

CERTIFICATE OF TRANSMISSION/MAILING			
I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent and Trademark Office on the date shown below.			
Signature			
Typed or printed name		Date	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No: 10/857,938 Confirmation No.: 5643
Inventor: James H. Derbyshire
Filed: 06/02/2004
TC/A.U.: 2618
Examiner: Le, Nhan T
Docket No.: 115-34USCIP/12667/100126
Title: Module Integration Integrated Circuits
Customer No.: 25319

April 3, 2008

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450, U.S.A.

Amendment

Sir,

This is in response to the Office action mailed on 01/25/2008. Please amend the application, as follows:

Listing of the Claims begins on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

Listing of Claims:

The listing of claims will replace all prior versions, and listings of claims in the application:

Claim 1 (original) An electronic apparatus comprising:

a first integrated circuit semiconductor die comprising:

a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path; and

a second integrated circuit semiconductor die comprising;

a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first portion of a first signal conditioning circuit for a signal propagating along the first signal path; and,

a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.

Claim 2 (original) An electronic apparatus according to claim 1, comprising a second signal conditioning circuit comprising a first portion of the second signal conditioning circuit and a second portion of the second signal conditioning circuit integrated within the second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path.

Claim 3 (original) An electronic apparatus according to claim 2, wherein the first signal conditioning function and the second signal conditioning function provide similar signal conditioning functions.

Claim 4 (original) An electronic apparatus according to claim 1, wherein the first integrated circuit die is manufactured using a first semiconductor process and utilizes a silicon based technology.

Claim 5 (original) An electronic apparatus according to claim 4, wherein the second integrated circuit die is manufactured using a second semiconductor process and utilizes other than a silicon based technology.

Claim 6 (original) An electronic apparatus according to claim 1, wherein the first portion of the first signal conditioning circuit comprises at least a power amplifier circuit and where the function of the first portion of the first signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit.

Claim 7 (original) An electronic apparatus according to claim 6, wherein the second portion of the first signal conditioning circuit comprises an impedance matching circuit.

Claim 8 (original) An electronic apparatus according to claim 2, wherein the second signal conditioning circuit comprises at least a power amplifier circuit and where the function of the first portion of the second signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit.

Claim 9 (original) An electronic apparatus according to claim 8, wherein the second portion of the second signal conditioning circuit comprises an impedance matching circuit and where the function of the first portion of the second signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit.

Claim 10 (original) An electronic apparatus according to claim 2, wherein the first semiconductor process does not facilitate manufacturing and integration of at least one of the second portion of the first signal conditioning circuit and the second portion of the second signal conditioning circuit.

Claim 11 (original) An electronic apparatus according to claim 1, wherein the second integrated circuit die is manufactured using a second semiconductor process that is different from that used to manufacture the first integrated circuit die.

Claim 12 (original) An electronic apparatus according to claim 1, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.

Claim 13 (original) An electronic apparatus according to claim 12, wherein the second integrated circuit die is derived from a second semiconductor wafer that is comprised of other one of Si, SiGe, GaAs, InP, and GaN.

Claim 14 (original) An electronic apparatus according to claim 1, wherein the first integrated circuit die is manufactured using a BiCMOS process.

Claim 15 (original) An electronic apparatus according to claim 1, wherein the second portion of the first signal conditioning circuit comprises at least one of a capacitor and an inductors and a signal transmission line.

Claim 16 (original) An electronic apparatus according to claim 2, comprising:
a first ancillary circuit integrated within the first integrated circuit die and electrically coupled to the first portion of the first signal conditioning circuit for use during operation thereof.

Claim 17 (original) An electronic apparatus according to claim 16, comprising a second ancillary circuit integrated within the first integrated circuit semiconductor die and electrically coupled to the second portion of the first signal conditioning circuit and to the first and second portions of the second signal conditioning circuit for other than performing the first or the second signal conditioning function and for use by the second portion of the first signal conditioning circuit and the first and second portions of the second signal conditioning circuit during operation thereof.

Claim 18 (currently amended) A method of manufacturing a module comprising:
providing a first signal conditioning circuit comprising a first portion and a second portion;

providing a second signal conditioning circuit comprising a first portion and a second portion;

implementing the first portion of the first signal conditioning circuit within a first semiconductor die;

implementing the second portion of the first signal conditioning circuit within a second semiconductor die;

implementing the first and second portions of the second signal conditioning circuit in the second semiconductor die;

bonding the first and second dies to a common substrate; and,

forming electrical connections between the two dies to complete the first signal conditioning circuit from the first portion of the first signal conditioning circuit and the second portion of the first signal conditioning circuit.

Claim 19 (cancelled) ~~A method according to claim 18, comprising:~~

~~—— providing a second signal conditioning circuit comprising a first portion and a second portion; and,~~

~~—— implementing the first and second portions of the second signal conditioning circuit in the second semiconductor die.~~

Claim 20 (original) A method according to claim 18, wherein the first semiconductor die comprises a first portion of a first signal path and the second semiconductor die comprises a second portion of the first signal path, the first signal path disposed between a first input port and a first output port.

Claim 21 (original) A method according to claim 20, wherein the second semiconductor die comprises a second signal path that is other than the second portion of the first signal path and in approximate RF isolation therefrom.

Claim 22 (original) A method according to claim 18, wherein the second semiconductor die is manufactured using a more expensive semiconductor process than that used for manufacturing of the first semiconductor die.

Claim 23 (original) A method according to claim 18, wherein the first portion of the first signal conditioning circuit is more cost effectively implemented in the first semiconductor die.

Claim 24 (original) A method according to claim 18, wherein the first semiconductor die does not facilitate implementation of the second portion of the first signal conditioning circuit therein.

Claim 25 (original) A method according to claim 18, wherein implementing of the second portion of the first signal conditioning circuit within the second semiconductor die provides increased performance in signal conditioning as compared to implementing of the second portion of the first signal conditioning circuit within the first semiconductor die.

Claim 26 (original) A method according to claim 18, wherein prior to implementing the first signal conditioning circuit comprises partitioning of the first signal conditioning circuit into the first portion and the second portion.

Claim 27 (original) An electronic apparatus comprising:

- a first integrated circuit semiconductor die comprising:
 - a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path;
 - a third portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along the first signal path; and
- a second integrated circuit semiconductor die comprising:
 - a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first and third portions of the first signal conditioning circuit for a signal propagating along the first signal path; and,
 - a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.

Claim 28 (original) An electronic apparatus according to claim 27, comprising:

- a first RF signal input port coupled with an input port of the first portion of the first signal conditioning circuit for receiving of a first RF input signal; and

- a first RF signal output port coupled with an output port of the third portion of the first signal conditioning circuit for providing of a first RF output signal,

- wherein the first signal path is disposed between the first RF signal input port and the first RF signal output port,

- wherein the coupling circuit comprises;

- a first electrical connection disposed between an output port the first portion of the first signal conditioning circuit and an input port of the second signal conditioning portion of the first signal conditioning circuit; and,

- a second electrical connection disposed between an output port the second portion of the first signal conditioning circuit and an input port of the third signal conditioning portion of the first signal conditioning circuit.

Claim 29 (original) An electronic apparatus according to claim 27, comprising:

- a first RF signal input port coupled with an input port of the second portion of the first signal conditioning circuit for receiving of a first RF input signal; and

- a first RF signal output port coupled with an output port of the third portion of the first signal conditioning circuit for providing of a first RF output signal,

- wherein the first signal path is disposed between the first RF signal input port and the first RF signal output port,

- wherein the coupling circuit comprises;

- a second electrical connection disposed between an output port the second portion of the first signal conditioning circuit and an input port of the third signal conditioning portion of the first signal conditioning circuit.

Claim 30 (original) An electronic apparatus according to claim 27, comprising a second signal conditioning circuit comprising a first portion of the second signal conditioning circuit and a second portion of the second signal conditioning circuit integrated within the second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path;

Claim 31 (original) An electronic apparatus according to claim 27, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.

Claim 32 (original) An electronic apparatus according to claim 31, wherein the second integrated circuit die is derived from a second semiconductor wafer that is comprised of the other one of Si, SiGe, GaAs, InP, and GaN.

Claim 33 (original) An electronic apparatus according to claim 27, wherein the second portion of the first signal conditioning circuit comprises an interstage matching circuit.

Claim 34 (original) An electronic apparatus according to claim 27, comprising a first ancillary circuit integrated within the first integrated circuit die and electrically coupled to the first portion and the third portion of the first signal conditioning circuit for use during operation thereof.

Claim 35 (original) An electronic apparatus according to claim 34, comprising a second ancillary circuit integrated within the first integrated circuit semiconductor die and electrically coupled to the second portion of the first signal conditioning circuit for use during operation thereof.

Remarks/Arguments

Applicant notes that regarding the disposition of the claims, the Office Action mailed on 01/25/2008 erroneously indicates that claims 1-32 are pending in the application. In fact, claims 1-35 currently are pending in the application. Claims 33-35 depend either directly or indirectly from allowed claim 27.

Claim 18 is currently amended. Claim 19 has been cancelled.

Information Disclosure Statement

Applicant has submitted under separate cover an Information Disclosure Statement including those references that have been cited in a European Search report, in respect of a European application corresponding to United States application 10/680,208, of which the instant application is a Continuation-In-Part.

Claim Rejections – 35 USC § 102

Claims 18, 20, 22-24 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Kimura (US 6,734,553).

Applicant has amended claim 18 to include all of the features recited in claim 19, which is objected to as being dependent upon a rejected base claim. Accordingly, Applicant respectfully submits that amended claim 18 now defines allowable subject matter. Favorable consideration is kindly requested.

Claims 20, 22-24 and 26 all depend either directly or indirectly from believed allowable amended claim 18. Accordingly, claims 20, 22-24 and 26 are also believed to be in proper condition for allowance. Favorable consideration is kindly requested.

Allowable Subject Matter

Applicant wishes to thank the Examiner for the indication of the allowability of claims 1-17 and 27-32. In addition, Applicant has adopted the Examiner's suggestion and has amended claim 18 to include the subject matter of objected to claim 19.

Appl. No. 10/857,938
Reply to Office action mailed on 01/25/2008

As mentioned supra, claims 1-35 are currently pending in the application. Since claims 33-35 depend from allowable claim 27, Applicant has assumed that these claims are also considered to be allowable. Applicant respectfully requests an acknowledgment as to the allowability of claims 33-35.

Applicant looks forward to receiving favourable consideration of the instant application.

Respectfully submitted,

A handwritten signature in black ink, appearing to be 'GM' followed by a stylized flourish.

Gary Morris, Reg. No. 40,735

Townsend and Townsend and Crew LLP
601 Pennsylvania Avenue, N.W.
South Building, Suite 900
Washington, DC 20004-2601
U.S.A.

Tel: (202) 434-8195
Fax: (202) 434-8171

MW/ds

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 10/857,938		Filing Date 06/02/2004		☐ To be Mailed			
APPLICATION AS FILED – PART I												
(Column 1)			(Column 2)			SMALL ENTITY ☒ OR		OTHER THAN SMALL ENTITY				
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)	FEE (\$)		RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A	N/A		N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*		X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*		X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).										
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))												
* If the difference in column 1 is less than zero, enter "0" in column 2.												
APPLICATION AS AMENDED – PART II												
(Column 1)			(Column 2)			(Column 3)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY	
AMENDMENT	04/03/2008		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		* 34	Minus	** 35	= 0	X \$25 =	0	OR	X \$ =		
	Independent (37 CFR 1.16(h))		* 3	Minus	*** 3	= 0	X \$105 =	0	OR	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))											
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
							TOTAL ADD'L FEE	0	OR	TOTAL ADD'L FEE		
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))		*	Minus	**	=	X \$ =		OR	X \$ =		
	Independent (37 CFR 1.16(h))		*	Minus	***	=	X \$ =		OR	X \$ =		
	☐ Application Size Fee (37 CFR 1.16(s))											
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
							TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.												

Legal Instrument Examiner:

//Katischa R. Wanzer//

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/857,938	06/02/2004	James H. Derbyshire	115-34USCIP/12667/100126

CONFIRMATION NO. 5643

POA ACCEPTANCE LETTER

20350
TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834



Date Mailed: 04/21/2008

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/21/2008.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/krwanzer/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/857,938	06/02/2004	James H. Derbyshire	115-34USCIP/12667/100126

CONFIRMATION NO. 5643

23838
KENYON & KENYON LLP
1500 K STREET N.W.
SUITE 700
WASHINGTON, DC 20005

POWER OF ATTORNEY NOTICE



Date Mailed: 04/21/2008

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/21/2008.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/krwanzer/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

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NOTICE OF ALLOWANCE AND FEE(S) DUE

20350 7590 06/02/2008

TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER

LE, NHAN T

ART UNIT

PAPER NUMBER

2618

DATE MAILED: 06/02/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/857,938	06/02/2004	James H. Derbyshire	115-34USCIP/12667/100126	5643

TITLE OF INVENTION: MODULE INTEGRATION INTEGRATED CIRCUITS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$720	\$300	\$0	\$1020	09/02/2008

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20350 7590 06/02/2008

**TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834**

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/857,938	06/02/2004	James H. Derbyshire	115-34USCIP/12667/100126	5643

TITLE OF INVENTION: MODULE INTEGRATION INTEGRATED CIRCUITS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	\$720	\$300	\$0	\$1020	09/02/2008

EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, NHAN T	2618	455-333000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
 (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
 (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/857,938	06/02/2004	James H. Derbyshire	115-34USCIP/12667/100126	5643
20350	7590	06/02/2008	EXAMINER	
TOWNSEND AND TOWNSEND AND CREW, LLP TWO EMBARCADERO CENTER EIGHTH FLOOR SAN FRANCISCO, CA 94111-3834			LE, NHAN T	
			ART UNIT	PAPER NUMBER
			2618	
DATE MAILED: 06/02/2008				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 906 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 906 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/857,938	DERBYSHIRE ET AL.	
	Examiner	Art Unit	
	NHAN T. LE	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 04/03/2008.
2. ☒ The allowed claim(s) is/are 1-18 and 20-35.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|---|--|
| <ol style="list-style-type: none"> 1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☒ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date <u>04/03/08</u> 4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | <ol style="list-style-type: none"> 5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413),
Paper No./Mail Date ____. 7. ☐ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other ____. |
|---|--|

DETAILED ACTION

Allowable Subject Matter

1. The following is an examiner's statement of reasons for allowance:

Claims 1-18, 20-35 are allowed for the reason as stated in the applicant's remarks under Allowable Subject Matter section, on page 9, lines 1-3, filed 04/03/2008

2. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Le whose telephone number is 571-272-7892. The examiner can normally be reached on 08:00-05:00 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on 571-272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business

Application/Control Number: 10/857,938

Page 3

Art Unit: 2618

Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nhan T Le/
Art Unit 2618
Nhan Le

/Edward Urban/
Supervisory Patent Examiner, Art Unit 2618

Substitute form for form 1449A & 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application No.	10/857,938
		Filing Date	June 2, 2004
		First Named Inventor	DERBYSHIRE et al.
		Group Art Unit	2618
		Examiner Name	Nhan T. LE
Sheet 1 of 1	Attorney Docket No.	115-34USCIP/12667/100126	

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
/NL/		US 2001/011926	A1	Adar Aharon	08-09-2001	
↓		US 6,075,995	A	Jensen Niels J.	06-13-2000	
		US 2003/165052	A1	Negishi Mikio et al.	09-04-2003	
		US 5,844,853		Kitsukawa et al.	12-01-1998	

FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
		Office ³	Number ⁴	Kind Code ⁵ (if known)			
							T ⁶

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in capital letters), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
/NL/		FURST R: "With GaAs Mmics Towards Dual Band Front End Applications In Wireless Communication" EUROPEAN MICROWAVE CONFERENCE. CONFERENCE PROCEEDINGS, vol. 2, 8 September 1997 (1997-09-08), pages 1289-1294, XP010253196	
↓		USPTO, for US patent application no. 10/680,208, 1 st Restriction Requirement mailed 09/13/2006	
		US patent application no. 10/680,208, response to 1 st Restriction Requirement filed 10/12/2006	
		USPTO, for US patent application no. 10/680,208, 2 nd Restriction Requirement mailed 04/05/2007	
		US patent application no. 10/680,208, response to 2 nd Restriction Requirement filed 05/03/2007	
		USPTO, for US patent application no. 10/680,208, 1 st Office Action mailed 12/26/2007	

Examiner Signature	/Nhan Le/	Date Considered	05/21/2008
-----------------------	-----------	--------------------	------------

1 Unique citation designation number. 2 See attached Kinds of U.S. Patent Documents. 3 Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4 For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5 Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. 6 Applicant is to place a check mark here if English language Translation is attached.

<i>Index of Claims</i> 	Application/Control No. 10857938	Applicant(s)/Patent Under Reexamination DERBYSHIRE ET AL.
	Examiner NHAN T LE	Art Unit 2618

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47			
CLAIM			DATE									
Final	Original		05/22/2008									
1	1	=										
2	2	=										
3	3	=										
4	4	=										
5	5	=										
6	6	=										
7	7	=										
8	8	=										
9	9	=										
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31	32	=										
32	33	=										
33	34	=										
34	35	=										

Search Notes 	Application/Control No. 10857938	Applicant(s)/Patent Under Reexamination DERBYSHIRE ET AL.
	Examiner NHAN T LE	Art Unit 2618

SEARCHED			
Class	Subclass	Date	Examiner
455	323, 333, 334, 338, 339, 340, 341	05/22/08	Nle
333	166, 185, 246, 260	05/22/08	Nle
257	723, 724, 784	05/22/08	Nle

SEARCH NOTES		
Search Notes	Date	Examiner
Update Search	05/22/08	Nle
Double Patenting Search	05/22/08	Nle

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
Interference Search, see East Search history		05/22/08	Nle

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S3	81	((first second\$4) near3 (portion\$3 part \$1)) same (die chip pcb integrated near3 circuit IC semiconductor) same signal\$3 same (electric\$3 near3 connect\$3) same substrat\$4	US-PGPUB; USPAT	OR	ON	2008/05/22 08:45
S4	141	apparatus and (first second) near3 portion and integrated and semiconduct\$3 and condition\$3 and signal \$3 and path and substrate and (electrical near4 connect\$3) and die\$1. clm.	US-PGPUB; USPAT	OR	ON	2008/05/22 09:27

5/ 22/ 08 9:37:28 AM

C:\Documents and Settings\NLe1\My Documents\EAST\Workspaces\10857938.wsp

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
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Alexandria, Virginia 22313-1450
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20350 7590 06/02/2008

TOWNSEND AND TOWNSEND AND CREW LLP
Two Embarcadero Center
Eighth Floor
San Francisco, CA 94111-3834
U.S.A.

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/857,938	06/02/2004	James H. Derbyshire	115-34USCIP/12667/100126	5643

TITLE OF INVENTION:

MODULE INTEGRATION INTEGRATED CIRCUITS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
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EXAMINER	ART UNIT	CLASS-SUBCLASS
LE, NHAN T	2618	455-333000

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☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

- 1 Townsend and Townsend and Crew LLP
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

SiGe Semiconductor Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Ottawa, Ontario, CANADA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

- ☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☒ Advance Order - # of Copies 3

4b. Payment of Fee(s):

- ☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 201430 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above. NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature

Typed or printed name Gary S. Morris

Date June 26, 2008

Registration No. 40,735

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		10857938		
Filing Date:		02-Jun-2004		
Title of Invention:		MODULE INTEGRATION INTEGRATED CIRCUITS		
First Named Inventor/Applicant Name:		James H. Derbyshire		
Filer:		Gary S. Morris/Melissa Pessagno		
Attorney Docket Number:		115-34USCIP/12667/100126		
Filed as Small Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	2501	1	720	720
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	3	3	9
Total in USD (\$)				1029

Electronic Acknowledgement Receipt

EFS ID:	3521860
Application Number:	10857938
International Application Number:	
Confirmation Number:	5643
Title of Invention:	MODULE INTEGRATION INTEGRATED CIRCUITS
First Named Inventor/Applicant Name:	James H. Derbyshire
Customer Number:	20350
Filer:	Gary S. Morris/Melissa Pessagno
Filer Authorized By:	Gary S. Morris
Attorney Docket Number:	115-34USCIP/12667/100126
Receipt Date:	26-JUN-2008
Filing Date:	02-JUN-2004
Time Stamp:	11:29:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1029
RAM confirmation Number	10817
Deposit Account	201430
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	027066_001500_IssueFee.pdf	101184 81c583dfa159beb842e803bb1dda60084d44032	no	1
Warnings:					
Information:					
2	Fee Worksheet (PTO-06)	fee-info.pdf	8452 3316290f0028db9462025dda51e331a71a45cf06	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			109636		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/857,938	08/05/2008	7409200	115-34USCIP/12667/100126	5643

20350 7590 07/16/2008
TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 906 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

James H. Derbyshire, Ottawa, CANADA;
Alan J.A. Trainor, Harlow, UNITED KINGDOM;

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:



Practitioners associated with the Customer Number:

12075

OR



Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:



The address associated with Customer Number:

12075

OR

☐ Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone			Email

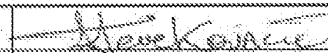
Assigned Name and Address:

SiGe Semiconductor Inc.
1050 Morrison Drive, Suite 100
Ottawa, Ontario Canada K2H 8K7

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee.

Signature		Date	May 19, 2011
Name	Stephen J. Kovacic	Telephone	978 289 2934
Title	Director, Legal		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. This information is required to obtain or retain a benefit by the person which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 2 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2905. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 322(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	11702790
Application Number:	10857938
International Application Number:	
Confirmation Number:	5643
Title of Invention:	MODULE INTEGRATION INTEGRATED CIRCUITS
First Named Inventor/Applicant Name:	James H. Derbyshire
Customer Number:	20350
Filer:	Aaron Spencer Kamlay
Filer Authorized By:	
Attorney Docket Number:	027066-001510US
Receipt Date:	23-DEC-2011
Filing Date:	02-JUN-2004
Time Stamp:	18:05:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assignee showing of ownership per 37 CFR 3.73(b).	027066-001510US_POA.pdf	74670 bdb81864be97daa26923f8892d9ba7a3fc5ddc7a	no	1

Warnings:

Information:

2	Power of Attorney	SIGE_POA.pdf	255961 49d0d83bc62d1f89aad30b226ebc2b54cfd b1ca4	no	2
Warnings:					
Information:					
Total Files Size (in bytes):				330631	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

STATEMENT UNDER 37 CFR 3.73(b)

PTO/SB/96 (07-09)

Attorney Docket No. 027066-001510US

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: James H. Derbyshire

Application No./Patent No.: 10/857,938 Filed/Issue Date: 06-02-2004

Titled: MODULE INTEGRATION INTEGRATED CIRCUITS

SIGE SEMICONDUCTOR INC., a corporation
(Name of Assignee) (Type of Assignee: corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;
2. ☐ an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or
3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 015432, Frame 0084, or for which a copy thereof is attached.

OR

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet (s).

- ☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/ASKamlay/
Signature

December 23, 2011
Date

Aaron S Kamlay, Reg. No. 58,813
Printed or Typed Name

Attorney for Assignee
Title



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/857,938	06/02/2004	James H. Derbyshire	027066-001510US

CONFIRMATION NO. 5643

POWER OF ATTORNEY NOTICE

20350
KILPATRICK TOWNSEND & STOCKTON LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834



Date Mailed: 01/04/2012

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/23/2011.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/sibrahim/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
10/857,938	06/02/2004	James H. Derbyshire	027066-001510US

CONFIRMATION NO. 5643

POA ACCEPTANCE LETTER



12075
Morris & Kamlay LLP
1629 K ST NW
Suite 300
Washington, DC 20006

Date Mailed: 01/04/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/23/2011.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/sibrahim/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No: 10/857,938 Confirmation No.: 5643
Filed: June 2, 2004
Patent No.: 7,409,200
Issued on: August 5, 2008
Docket No.: 115-34 US/CIP
Title: MODULE INTEGRATION INTEGRATED CIRCUITS
Customer No.: 25319

April 20, 2012

By Fax only: 2 pages

Mail Stop M Correspondence
Director of the USPTO
United States Patent & Trade-marks Office
P.O. Box 1450
Alexandria, VA 22313-1450
U.S.A.

1-571-273-6500

Dear Sir:

**Change of Entity Status to Large Entity and Payment of
Annuity Fee Deficiency Owed Under 37 C.F.R. § 1.28(c)**

▪ Applicant has recently discovered that through unintentional error, the Office was not notified of a loss of entitlement to Small entity status as required by § 1.27 (g)(2) at the time the first (3.5 years) maintenance fee was paid (February 6, 2012). This error occurred in good faith, without deceptive intent, and was not directed to any fraudulent deception before the United States Patent and Trademark Office.

- Itemization of the deficiency payment is as follows:

04/24/2012 MBANGURA 00000011 501142 7409200
01 FC:1599 565.00 DA

Type of fee erroneously paid as Small entity and current fee for Large entity	Small Entity fee actually paid and date when paid	Deficiency owed (USD)
Maintenance Fee \$1130.00	\$565.00 Paid on February 6, 2012	\$565.00

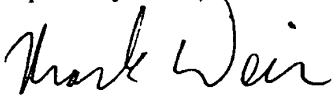
TOTAL DEFICIENCY PAYMENT OWED:**USD \$565.00**

Please charge the amount of \$565.00 for payment of the deficiency owed to Deposit Account 50-1142.

Please also charge any additional fees required or credit any overpayment to Deposit Account No.: 50-1142.

Applicant looks forward to receipt of confirmation in change of entity status from Small to Large.

Respectfully submitted,



Mark Robert Weir *Regn. No. 57949*

MW/jm

Freedman & Associates
Suite 230, 55 Murray Street
Ottawa, Ontario
K1N 5M3 Canada

Tel: 613-274-7272
Fax: 613-274-7414



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Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
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MAILED

JUN 04 2012

OFFICE OF PETITIONS

**MORRIS & KAMLAY LLP
1150 18TH STREET, N.W.
SUITE 575
WASHINGTON DC 20036**

In re Patent No. 7,409,200 :
Issue Date: August 5, 2008 :
Application No. 10/857,938 :
Filed: June 2, 2004 :
Attorney Docket No. 027066-001510US :

NOTICE

This is a notice regarding your request for acceptance of a fee deficiency submission under 37 CFR 1.28 submitted on April 20, 2012.

The Office no longer investigates or rejects original or reissue patent under 37 CFR 1.56. **1098 Off. Gaz. Pat. Office 502 (January 3, 1989)**. Therefore, nothing in this Notice is intended to imply that an investigation was done.

Your fee deficiency submission under 37 CFR 1.28 is hereby **ACCEPTED**.

This patent is no longer entitled to small entity status. Accordingly, all future fees paid in this patent must be paid at the large entity rate.

There is no indication that the person signing the request was ever given a power of attorney to prosecute the application. If the person signing the request desires to receive future correspondence regarding this patent, the appropriate power of attorney documents must be submitted. While a courtesy copy of this decision is being mailed to the person signing the request, all future correspondence will be directed to the address currently of record until appropriate instructions are received.

Inquiries related to this communication should be directed to the undersigned at (571) 272-3208.

/KOC/
Karen Creasy
Petitions Examiner
Office of Petitions

Cc:

**FREEDMAN & ASSOCIATES
SUITE 230, 55 MURRAY STREET
OTTAWA, ONTARIO
KIN 5M3 CANADA**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No: 10/857,938 Confirmation No.: 5643
Filed: June 2, 2004
Patent No.: 7,409,200
Issued on: August 5, 2008
Docket No.: 115-34 US/CIP
Title: MODULE INTEGRATION INTEGRATED CIRCUITS
Customer No.: 25319

April 20, 2012

By Fax only: 2 pages

Mail Stop M Correspondence
Director of the USPTO
United States Patent & Trade-marks Office
P.O. Box 1450
Alexandria, VA 22313-1450
U.S.A.

1-571-273-6500

Dear Sir:

**Change of Entity Status to Large Entity and Payment of
Annuity Fee Deficiency Owed Under 37 C.F.R. § 1.28(c)**

▪ Applicant has recently discovered that through unintentional error, the Office was not notified of a loss of entitlement to Small entity status as required by § 1.27 (g)(2) at the time the first (3.5 years) maintenance fee was paid (February 6, 2012). This error occurred in good faith, without deceptive intent, and was not directed to any fraudulent deception before the United States Patent and Trademark Office.

- Itemization of the deficiency payment is as follows:

04/24/2012 MBANGURA 00000011 501142 7409200
01 FC:1599 565.00 DA
04/24/2012 MBANGURA 00000011 501142 7409200
01 FC:1599 565.00 CR
06/04/2012 CKHLOK 00000005 501142 7409200
01 FC:1559 565.00 DA

Type of fee erroneously paid as Small entity and current fee for Large entity	Small Entity fee actually paid and date when paid	Deficiency owed (USD)
Maintenance Fee \$1130.00	\$565.00 Paid on February 6, 2012	\$565.00

TOTAL DEFICIENCY PAYMENT OWED:**USD \$565.00**

Please charge the amount of \$565.00 for payment of the deficiency owed to Deposit Account 50-1142.

Please also charge any additional fees required or credit any overpayment to Deposit Account No.: 50-1142.

Applicant looks forward to receipt of confirmation in change of entity status from Small to Large.

Respectfully submitted,



Mark Robert Weir Regn. No. 57949

MW/jm

Freedman & Associates
Suite 230, 55 Murray Street
Ottawa, Ontario
K1N 5M3 Canada

Tel: 613-274-7272
Fax: 613-274-7414