

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KANGXI COMMUNICATION TECHNOLOGIES
Petitioner,

v.

SKYWORKS SOLUTIONS, INC.,
Patent Owner.

U.S. Patent No. 7,409,200
Issue Date: AUGUST 5, 2008

Title: MODULE INTEGRATION INTEGRATED CIRCUITS

Inter Partes Review No.: IPR2025-00912

**DECLARATION OF AYMAN ADEL FAYED IN SUPPORT OF PETITION
FOR INTER PARTES REVIEW OF U.S. PATENT NO. 7,409,200**

TABLE OF CONTENTS

	Page
I. INTRODUCTION.....	1
II. MY BACKGROUND AND QUALIFICATIONS.....	3
III. RELEVANT LEGAL STANDARDS.....	7
IV. OVERVIEW.....	10
V. BACKGROUND.....	17
A. Summary of the '200 Patent.....	17
B. Claim Construction.....	21
C. Priority Date of the Challenged Claims.....	21
D. Person of Ordinary Skill in the Art.....	21
E. State of the Art.....	22
1. Techniques for Implementing Modules With Multiple Semiconductor Dies Were Well-Known.....	22
2. Partitioning Circuits Within a Multi-Die Module to Take Advantage of Diverse Semiconductor Technologies Was a Routine Practice	25
3. It Was Well-Understood that Different Semiconductor Technologies had Different Benefits for RF Circuit Design.....	27
4. Implementing Power Amplifier Circuits on Different Types of Semiconductor Dies Was Well-Known	30
VI. CHALLENGES.....	32
A. Identification of Challenges	32
B. Prior Art.....	32
VII. IDENTIFICATION OF HOW THE CLAIMS ARE INPATENTABLE.....	33
A. Challenge 1: Claims 1-2, 4, 10-13, 15, 18-20, 23-26, and 29-31 and obvious under 35 U.S.C. §103(a) over Garlepp.....	33
1. Garlepp.....	33
2. Detailed Application of Garlepp to the Challenged Claims	35

B. Challenge 2: Claims 1-2, 6, 10-15, 18-20, 23-26, and 29-31 are obvious under 35 U.S.C. §103(a) over Magoon in View of Ngompe.....	56
1. Magoon	56
2. Ngompe	59
3. Motivation to Combine	61
4. Detailed Application of Magoon in View of Ngompe to the Challenged Claims.....	63

I. INTRODUCTION

1. I, Ayman Adel Fayed, declare as follows:

2. I am over the age of eighteen (18) and otherwise competent to make this declaration.

3. I have been retained by Kangxi Communication Technologies (Petitioner) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office. Although I am being compensated at my rate of \$700 per hour for the time I spend on this matter, no part of my compensation depends on the outcome of this proceeding, and I have no other interest in this proceeding. To the best of my knowledge, I have no financial interest in Client.

4. This Petition for inter partes review involves U.S. Patent No. 7,409,200 (“the ’200 Patent”) (EX-1001), titled “MODULE INTEGRATION INTEGRATED CIRCUITS” and lists James H. Derbyshire as the inventor.

5. For the purposes of this inter partes review as discussed later, I have been instructed to assume that the effective filing date of the Claims of the ’200 Patent challenged by the Petitioner in this inter partes review is no earlier than October 8, 2003, the filing date of Application 10/680,208 from which the ’200 Patent claims priority as a Continuation in Part.

6. I understand that according to USPTO records, the '200 Patent is currently assigned to SIGe Semiconductor Inc.

7. The '200 Patent is directed to RF front-end circuits and more specifically to the field of multi-standard RF front-end circuits implemented in a small module size. The RF circuits are signal conditioning circuits that are partitioned and integrated in two semiconductor dies within the module.

8. In preparing this Declaration, I have reviewed the '200 Patent (EX-1001), the file history of the '200 Patent (EX-1002), and each of the documents cited herein, and I have considered these documents in light of the general knowledge in the art as of October 8, 2003.

9. In formulating my opinions, I have relied upon my experience in the relevant art. I have also considered the viewpoint of a person of ordinary skill in the art ("POSITA") in the relevant field, as of October 8, 2003, who I describe below (§V.D.). For convenience, the materials I considered in forming my opinion are listed in Appendix A.

10. I have been asked to provide my technical expertise, analysis, insights, and opinions regarding the '200 Patent and relevant references that form the basis of the arguments set forth in the accompanying Petition for inter partes review of the '200 Patent. As described in detail below, I offer the following opinions in this Declaration:

- A POSITA would have found Claims 1-2, 4, 10-13, 15, 18-20, 23-26, and 29-31 of the '200 Patent obvious over Garlepp.
- A POSITA would have found Claims 1-2, 6, 10-15, 18-20, 23-26, and 29-31 are obvious over Magoon in view of Ngompe.

II. MY BACKGROUND AND QUALIFICATIONS

11. I have over 26 years of experience in the fields of electrical, computer, and electrical communications engineering. My industry and research experience and expertise specifically relevant to the '200 Patent includes the design of power management, data converters, and analog and mixed-signal integrated circuits for wireless System-on-Chip ("SoC") with multiple integrated Radio-Frequency ("RF") transceivers for various wireless standards, such as GSM, WCDMA, WIMAX, WLAN, and Bluetooth. This encompasses a variety of low-noise low-EMI power regulators and modulators and delta-sigma data converters for wireless RF CODECs.

12. I earned my M.Sc. and Ph.D. in Electrical and Computer Engineering from The Ohio State University in 2000 and 2004, respectively. I earned a B.Sc. in Electronics and Electrical Communications Engineering from Cairo University in Egypt in 1998. I am currently a Professor in the Department of Electrical and Computer Engineering at The Ohio State University.

13. A selected summary of my specific experience relevant to the '200 Patent includes my 2005-2008 role as a member of the technical staff and as an analog, mixed-signal, and power management integrated circuit designer for the Wireless Terminal Business Unit at Texas Instruments. In that role, I led the system and circuit design of embedded power management/electronics solutions for integrated wireless, RF, and baseband applications in 65nm/45nm digital CMOS technologies. My responsibilities included power system architecture, supply domain definition and specifications, noise and power budgeting, RF-friendly dc-dc power converter techniques, ripple suppression and cancellation techniques, and low-leakage circuit techniques for linear and switching power regulators for RF and mixed-signal modules.

14. I also led the clear spectrum task force at Texas Instruments, where I was responsible for the development of design & verification methodology for power management/electronics modules in large mixed-signal System-on-Chip with multi noise-sensitive RF cores, including Cellular, Bluetooth, and Wireless LAN RF transceivers. This encompassed circuit design, power distribution networks, package and board parasitics modeling, communication across supply domains, and power supply isolation. My experience also includes the design of various classes of delta-sigma data converters including switched-C, continuous-time, and single-amplifier based architectures for wireless RF CODEC

applications in 45nm/65nm CMOS processes for GSM/WCDMA (2G/3G) wireless standards.

15. My relevant experience also includes my role as an assistant professor (2009-2014) then associate professor (2014-2015) at Iowa State University, then as an associate professor (2015-2020) then full professor (2020-present) at The Ohio State University, where I supervised the research of 14 Ph.D. students, over 11 M.Sc. students, who, for example, designed various classes of integrated linear and switching power regulators, low-noise low-EMI power converters for RF circuits, high-frequency switching converters with on-chip outputs, and continuous- and discrete-time signal filters, all in 350nm/65nm/45nm/28nm CMOS technologies.

16. The focus of my professional and research work has been on analog, mixed-signal, and power management integrated circuits, including for RF applications. I have authored or co-authored over 71 technical papers in international journals and conferences and have been an inventor or co-inventor on 8 US and international patents. Much of my published work, including my Master's and Ph.D. research, covers the area of analog, mixed-signal, and power management/electronics integrated circuits.

17. My expertise in and contributions to the field of analog, mixed-signal, and power management/electronics integrated circuits have been

recognized in many ways. For example, from 2016 to 2023, I have been serving on the editorial board (as an associate editor) of the IEEE Transactions on Circuits and Systems I, which is the leading journal of the IEEE Circuits and Systems Society. I have also been serving as a member of the Technical Program Committee of many leading IEEE international conferences, such as RF Integrated Circuits Symposium (2011-2021), Applied Power Electronics Conference (2018-present), and International Symposium of Circuits and Systems (2012-present). I am also currently serving as the chair of the Analog Signal Processing Technical Committee of the IEEE Circuits and Systems Society. I have also received the Best Associate Editor Award from IEEE Transactions on Circuits and Systems–I in 2020, 2021 and 2022, and the 2022 IEEE Circuits and Systems Society Outstanding Technical Committee Award. I have also received the 2021 IEEE Transactions on Power Electronics Second Place Prize Paper Award from the IEEE Power Electronics Society, the 2015 Darlington Best Transactions Paper Award from the IEEE Circuits and System Society, the National Science Foundation CAREER Award in 2013, and the Northrop Grumman Chair Professorship from Iowa State University in 2013 and 2014.

18. My curriculum vitae, which includes a more detailed summary of my background and experience, is attached as EX-1004.

III. RELEVANT LEGAL STANDARDS

19. I am not a lawyer and do not provide any legal opinions in this Declaration. Although I am not a lawyer, I have been informed and understand that certain legal standards are to be applied by technical experts in forming opinions regarding the meaning and validity of patent claims. I have been asked to provide my opinions regarding whether the claims of the '200 Patent would have been obvious to a person having ordinary skill in the art at the time of the alleged invention, in light of the prior art.

20. I have been informed and understand that a patent claim is not patentable under 35 U.S.C. § 103 if the differences between the patent claim and the prior art are such that the claimed subject matter as a whole would have been obvious at the time the claimed invention was made to a person having ordinary skill in the relevant art. Obviousness, as I have been informed and understand, is based on the scope and content of the prior art, the differences between the prior art and the claim, the level of ordinary skill in the art, and, to the extent that they exist, certain objective indicia of nonobviousness.

21. I understand that objective indicia can be important evidence regarding whether a patent is obvious or nonobvious, if it has an appropriate nexus to the claimed invention, i.e., is a result of the merits of a claimed invention (rather than the result of design needs or market-pressure advertising

or similar activities). Such indicia include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention as compared to the closest prior art; praise of the invention by the infringer or others in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art.

22. I have been informed that whether there are any relevant differences between the prior art and the claimed invention is to be analyzed from the view of a person of ordinary skill in the relevant art at the time of the invention. As such, my opinions below as to a person of ordinary skill in the art are as of the time of the invention, even if not expressly stated as such; for example, even if stated in the present tense.

23. In analyzing the relevance of the differences between the claimed invention and the prior art, I have been informed that I must consider the impact, if any, of such differences on the obviousness or nonobviousness of the invention as a whole, not merely some portion of it. The person of ordinary skill faced with a problem is able to apply his or her experience and ability to solve the problem and also look to any available prior art to help solve the problem.

24. I have been informed that a precise teaching in the prior art directed to the subject matter of the claimed invention is not needed. I have been informed that one may take into account the inferences and creative steps that a person of ordinary skill in the art would have employed in reviewing the prior art at the time of the invention. For example, if the claimed invention combined elements known in the prior art and the combination yielded results that were predictable to a person of ordinary skill in the art at the time of the invention, then this evidence would make it more likely that the claim was obvious. On the other hand, if the combination of known elements yielded unexpected or unpredictable results, or if the prior art teaches away from combining the known elements, then this evidence would make it more likely that the claim that successfully combined those elements was not obvious.

25. I have been informed and understand that there are recognized, exemplary, rationales for combining or modifying references to show obviousness of claimed subject matter. Some of the rationales include the following: combining prior art elements according to known methods to yield predictable results; simple substitution of one known element for another to yield predictable results; use of a known technique to improve a similar device (method or product) in the same way; applying a known technique to a known device (method or product) ready for improvement to yield predictable results;

choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; known work in one field of endeavor may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations are predictable to one of ordinary skill in the art; and some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art teachings to arrive at the claimed invention.

IV. OVERVIEW

26. The '200 Patent is directed to the problem of providing a high-performance, compact electronic module that incorporates electronic circuits for radio frequency (RF) front-end applications.

27. In general, an RF front-end module is a collection of components that interfaces with the antenna and provides the initial processing of incoming radio signals (reception) and/or the final amplification of outgoing radio signals (transmission). A front-end module that handles both reception and transmission is referred to as a “transceiver.” The module’s components include signal conditioning circuits with specialized components, such as low noise amplifiers (LNAs) in the receive signal path and power amplifiers in the transmit signal path. The components also include ancillary circuits (e.g., voltage

regulators) for use by the signal conditioning circuits. RF front-end modules can include circuitry to support multiple different RF standards or frequency bands.

28. According to the '200 Patent, one problem associated with a multi-standard RF module is that separate circuitry is needed for each standard, thus increasing the component count. This, in turn, increases cost, reduces yield and durability, and increases module size. EX-1001 1:36-55. The '200 Patent describes another problem: the semiconductor technology best suited for integrating some components of the circuitry often is not suited for integrating other components. Thus, RF module designers invariably included multiple different semiconductor dies in their modules. EX-1001 2:12-27; 4:3-13.

29. The '200 Patent purports to address these problems by providing a technique for partitioning the circuitry into functional portions along a signal path, and then integrating the different portions within discrete semiconductor dies.¹ The dies are mounted on a common substrate within the module and

¹ The '200 Patent uses the terms “**die**” and “**semiconductor** substrate” as synonyms. *See* EX-1001, 4:40-41, 54; 6:49-50, 64 (referring to component 511 as both a “semiconductor substrate” and “semiconductor die”). This usage should not be confused with the “substrate” recited in the claims, which references a substrate in the context of a package substrate that supports dies. *See* '200 Patent, Claim 1

electrically interconnected to complete the signal path. An example embodiment is an RF front-end module in which the partitioned circuitry is the PA circuitry for amplifying RF signals, which the '200 Patent generally refers to as a “signal conditioning circuit.”

30. An embodiment of a module 500 implementing the '200 Patent's circuit partitioning and integration scheme is illustrated in FIG. 5:

(claiming: “a **substrate** for supporting the first and second **integrated circuit semiconductor dies**”), Fig. 4 (step 404: “bonding the first and second **dies** to a **common substrate**”).

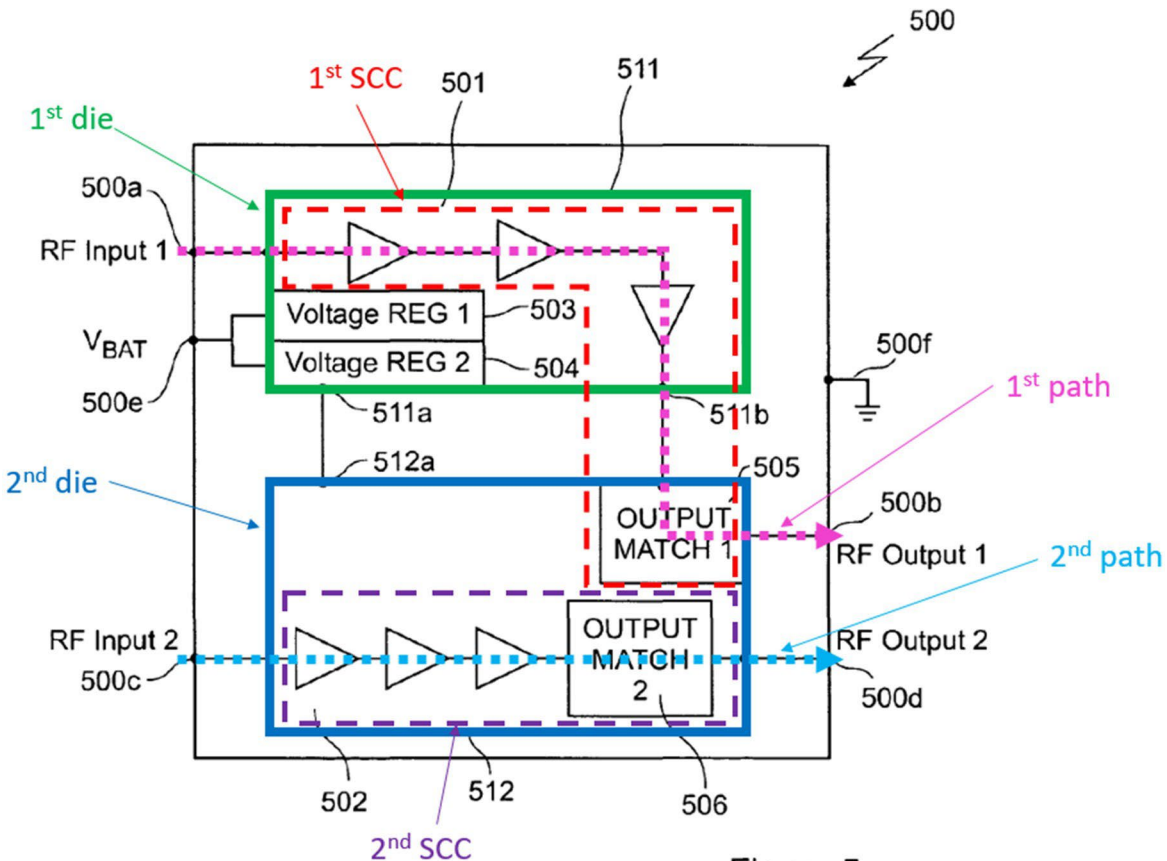


Figure 5

EX-1001, FIG. 5 (annotated).

31. Module 500 includes two signal conditioning circuits (“SCCs”): a first SCC 501, 505 disposed along a first signal path; and a second SCC 502, 506 disposed along a second signal path. Each SCC is implemented as a PA circuit and is partitioned into two series-connected portions—a PA portion 501/502 and an impedance matching portion 505/506.

32. Module 500 also includes a first semiconductor die 511 made of silicon germanium (SiGe) and a second semiconductor die 512 made of gallium

arsenide (GaAs). With respect to the **first SCC**, PA portion 501 is formed in the **first die 511** using SiGe BiCMOS technology, while the impedance matching portion 505 is formed in the **second die 512 using GaAs technology**. EX-1001 7:32-8:66. For the **second SCC**, portions 502 and 506 both are integrated in the **second die 512**.

33. According to the '200 Patent, partitioning the first SCC across different dies is implemented so that the “[s]ignal conditioning functions of each of [its] portions are facilitated by a predetermined type of semiconductor die within which they are formed.” EX-1001, Abstract. The '200 Patent states that this design scheme is “efficient in respect of die area usage,” “provides the module designer with the best attributes of both semiconductor [dies] . . . in order to achieve a high level of performance, and integration, with a low number of module components,” and results in a compact module size. EX-1001, 2:28-33; 8:43-47; 8:52-56. In other words, the '200 Patent is directed to a RF module with multiple semiconductor dies that is implemented by partitioning signal conditioning circuits along their respective signal paths and integrating the resulting partitions into the die best suited for each portion’s functionality.

34. But well before the '200 Patent, implementing modules in this manner was a well-known and conventional practice. For example, as illustrated below, *Garlepp* discloses the same multiple-die architecture for RF modules

where elements in common with the '200 Patent are color coded in the same color.

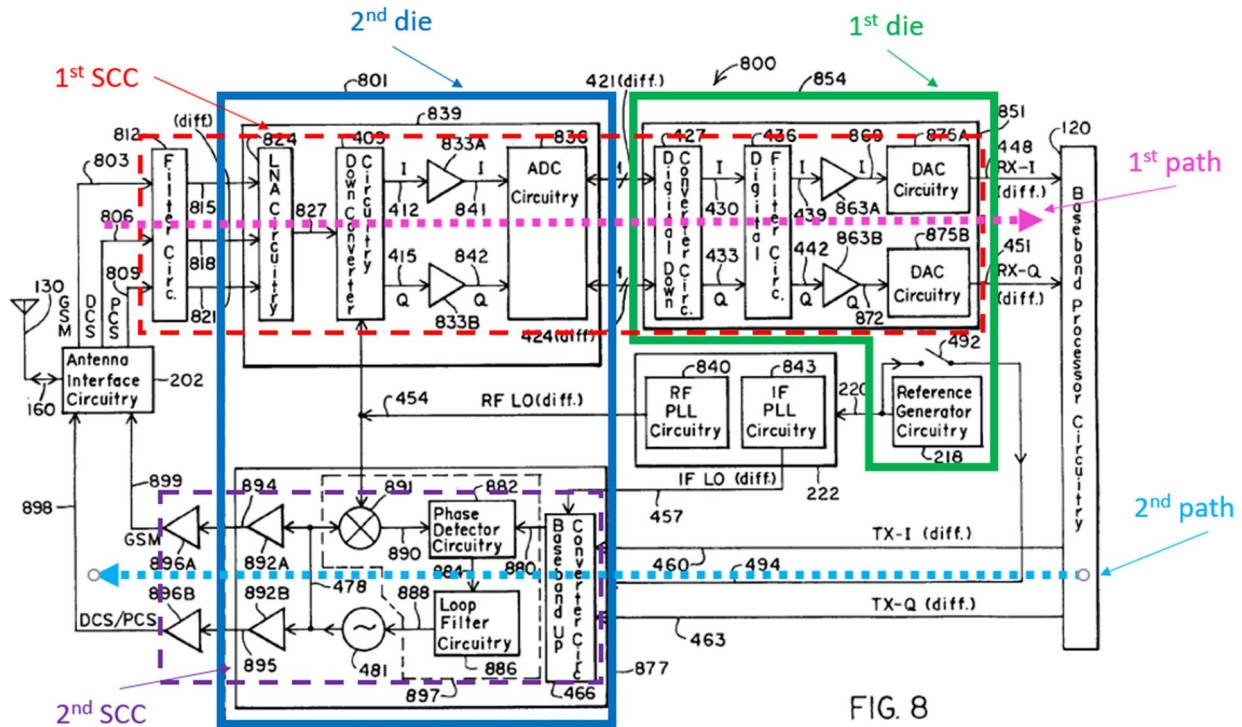


FIG. 8

EX-1005, FIG. 8 (annotated), ¶¶5, 46

35. As in the '200 Patent, *Garlepp*'s module includes two signal conditioning circuits and two interconnected semiconductor dies fabricated using different semiconductor processes. Like the '200 Patent, the **first SCC** (i.e., "receive path circuitry") is partitioned along a **first signal path** so that portion 851 is formed in **first die 854** and portion 839 is formed in **second die 801**. Also like the '200 Patent, the entirety of the **second SCC** (i.e., transmitter

signal conditioning circuits and integration across semiconductor dies required by the Challenged Claims.

V. BACKGROUND

A. Summary of the '200 Patent

38. The '200 Patent is directed to “RF front-end circuits and more specifically to the field of multi-standard RF front-end circuits implemented in a small module size.” EX-1001, 1:9-11. The RF circuits are signal conditioning circuits that are partitioned and integrated in two semiconductor dies within the module.

39. The '200 Patent acknowledges that modules incorporating signal conditioning circuits integrated in multiple dies was well-known. An example of a prior art RF module is shown in FIG. 1.

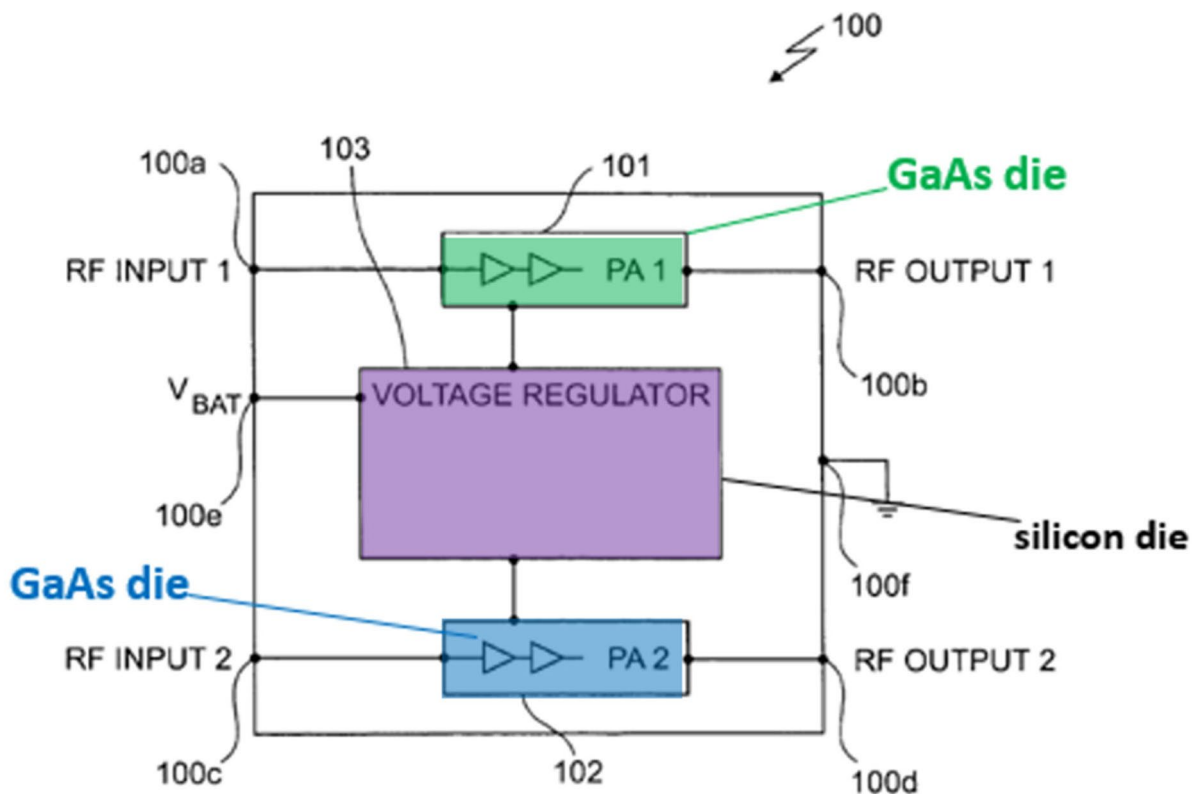


Figure 1
(PRIOR ART)

EX-1001, FIG. 1 (annotated).

40. Module 100 includes three semiconductor dies: two gallium arsenide (GaAs) (green/blue) dies and one silicon die (purple). Two signal conditioning circuits implemented as power amplifier (PA) circuit 101 and PA circuit 102 are integrated on each of the separate GaAs dies, while ancillary circuitry is integrated on the silicon die.

41. The '200 Patent discloses examples of two-die modules that purport to improve on the three-die prior art module of FIG. 1, such as the module 500 in annotated FIG. 5:

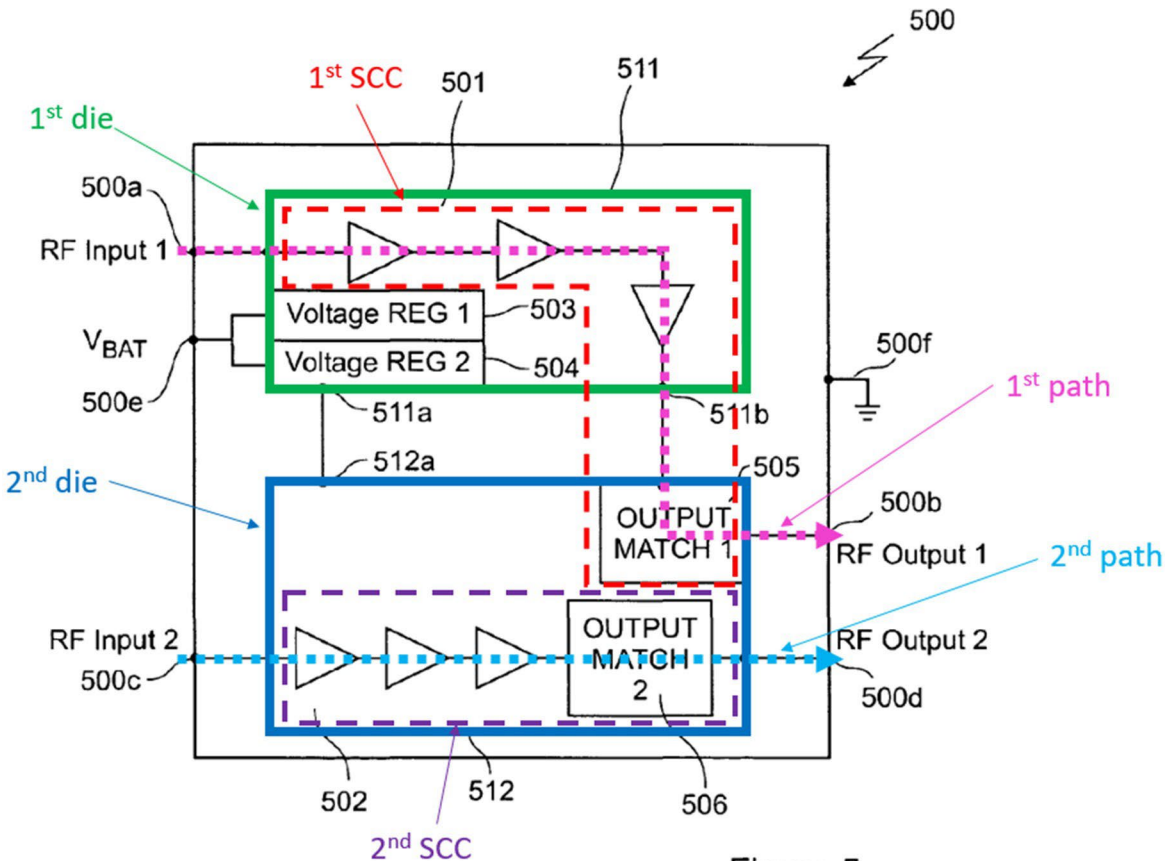


Figure 5

EX-1001, FIG. 5 (annotated).

42. Module 500 includes a first SCC 501, 505 and a second SCC 502, 506 implemented as PA circuits, each having a series-connected PA portion and an output impedance matching portion disposed along a signal path. The number of dies is reduced relative to prior art FIG. 1 by integrating ancillary circuits (i.e., voltage regulators) 503, 504 together with PA portion 501 of the

first SCC within the first die 511. EX-1001, 1:56-66. Another difference is that the first SCC is partitioned between the first die 511 and the second die 512. Thus, a first signal path extends between the RF input port 500a on the first die to the RF output port 500b on the second die. The second signal path resides entirely within the second die, extending from the RF input port 500c to the RF output port 500d. EX-1001, 8:27-39.

43. In FIG. 5, first die 511 is manufactured using SiGe BiCMOS technology, which the '200 Patent acknowledges was known to be suitable both for integration of PAs and for ancillary circuits. EX-1001, 1:56-2:11. Second die 512 is manufactured using GaAs technology, which the '200 Patent acknowledges routinely was used for integration of PAs and was known to be suited for integration of passive components (e.g., inductors in matching circuit), but unsuitable for the integration of ancillary circuits. EX-1001, 2:12-23, 8:28-36. Thus, as shown in FIG. 5, the first SCC is partitioned so that its PA portion 501 is formed in the SiGe die 511, and the matching portion 505 is formed in the GaAs die 512. According to the '200 Patent: "Advantageously, this integration scheme provides a module designer with the best attributes of both semiconductor substrates, which in this case are silicon and GaAs, in order to achieve a high level of performance, and integration, with a low number of module components." EX-1001, 8:43-47.

44. All of the Challenged Claims are directed to the partitioning and multi-die integration scheme shown in FIG. 5 of the '200 Patent or a variation in the partitioning, as shown in FIG. 6.

B. Claim Construction

45. I have been informed and understand that in order to properly evaluate the '200 Patent, the terms of the claims must first be interpreted. I understand that Petitioner proposes that each claim term be given its plain and ordinary meaning in this proceeding. The prior art herein meets each claim limitation under any reasonable construction.

C. Priority Date of the Challenged Claims

46. For the purpose of this inter partes review, I have been instructed to assume that the effective filing date of each of the Challenged Claims is the filing date of the '200 Patent, October 8, 2003.

D. Person of Ordinary Skill in the Art

47. I have been informed and understand that a Person of Ordinary Skill in the Art ("POSITA") is a hypothetical person who is presumed to be aware of all pertinent prior art, thinks along conventional wisdom in the art, and is a person of ordinary creativity.

48. A POSITA in October 8, 2003, would have been someone knowledgeable and familiar with the signal conditioning circuits and semiconductor chip design and packaging that are pertinent to the '200 Patent.

49. A POSITA would have had a bachelor's degree in electrical or electronics engineering, or an equivalent degree or equivalent training, and approximately three years of experience working with RF circuit design and packaging and/or similar technology. Less professional experience can be remedied by additional education, and vice versa.

E. State of the Art

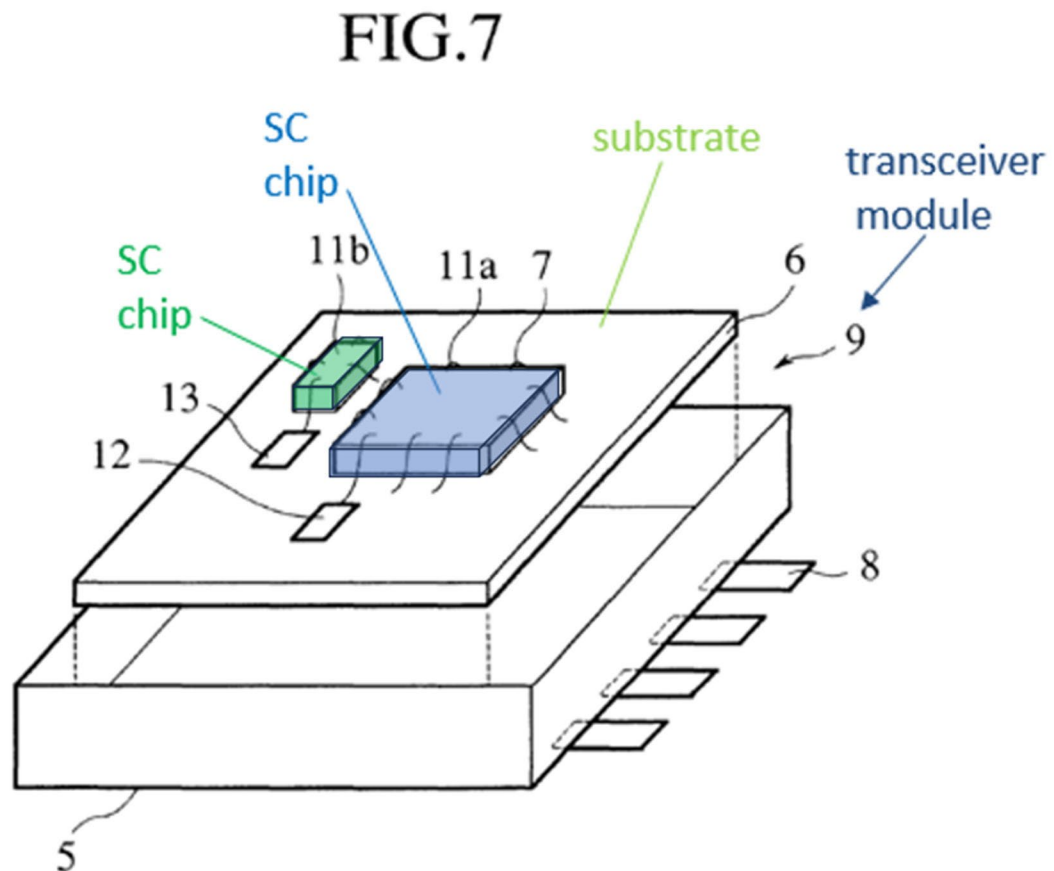
50. The following section describes the relevant state of the art for multiple die modules as of the priority date with citation to exemplary corroborating references. The references, and this discussion of what was known to POSITAs, provide factual support for the general description of the state of the art at the time of the invention, and provide additional motivation to modify or combine teachings in the references.

1. Techniques for Implementing Modules With Multiple Semiconductor Dies Were Well-Known

51. By October 2003, techniques for manufacturing module structures for packaging and interconnecting multiple semiconductor dies were well-known. For example, *Pedder* (EX-1014) discloses that “[t]he multichip module (MCM) approach to interconnection and packaging employs unpackaged naked dies mounted on a high interconnection density substrate structure, with the resulting assembly then packaged to form a module.” EX-1014, 1:1-5. As exemplified by *Pedder*, known interconnection techniques included wire-

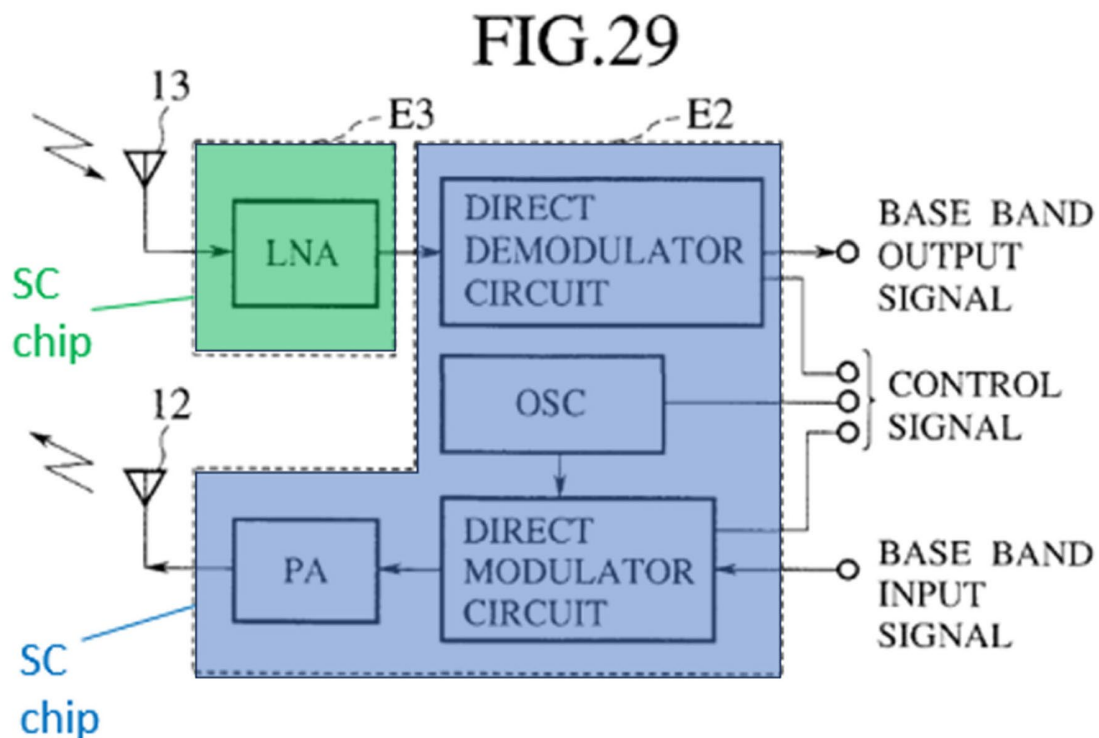
bonding and flip chip soldering, and recognized benefits of MCMs were increased performance, as well as reduction in size and weight and improved reliability. EX-1014, 1:5-28.

52. Given the known benefits achievable with multiple die modules, the RF industry had long been exploring the use of such design strategy in RF transceivers used for devices, such as cellular phones. For example, *Yoshihara* (EX-1013) describes numerous embodiments of RF transceiver packages, including a module with “semiconductor chips” that are “mounted on a single substrate”:



EX-1013, FIG. 7, 7:4-22 (“chips ... 11a, 11b connected by bonding wires 7 to a transmitter antenna 12 and a receiver antenna 13”).

53. In FIG. 29, *Yoshihara* discloses a corresponding two-die (i.e., two semiconductor chips) circuit arrangement for the RF module, in which “the circuit arrangement E3 of one of the two semiconductor chips includes an LNA [low noise amplifier] and that E2 of the other includes a direct demodulator circuit, an OSC and a PA.” EX-1013, 16:61-17:2.



EX-1013, FIG. 29; *see also* EX-1009 (Abstract) (disclosing “a single-package solution that contains different components that are interconnected with a multi-chip module (MCM) interconnect technology” for RF transceivers).

2. Partitioning Circuits Within a Multi-Die Module to Take Advantage of Diverse Semiconductor Technologies Was a Routine Practice

54. By October 2003, implementing multi-die modules using dies manufactured in different semiconductor technologies was a well-known practice. Indeed, although a desire existed for integration of systems on a unitary semiconductor device (referred to as “system-on-chip”), the industry recognized that partitioning circuits into functional blocks, each fabricated in a different semiconductor die, had benefits, including performance and manufacturing advantages. For example, *Chan* (EX-1008) discloses that “[t]raditional multi-chip modules (MCM’s) are a conventional approach to providing a semiconductor solution” for integrated circuit designs that can be partitioned into discrete functional blocks. EX-1008, ¶5. In these traditional MCMs, multiple “semiconductor devices that are mounted on a common base substrate provide the functionality associated with two or more function blocks.” EX-1008, ¶¶31, 35, 36. By using multiple interconnected semiconductor devices, each circuit block “can be matched with a particular semiconductor

substrate technologies [sic] and/or semiconductor fabrication processes for enhancing performance, reducing unit cost, etc.” EX-1008, ¶¶5, 25.

55. The art includes other examples of the MCM “conventional approach” for RF front-end systems. For example, *Wambacq* (EX-1009) discloses a “single-package solution” for RF transceivers in which “GaAs MMICs [and] silicon chips” are mounted on a common substrate. EX-1009, Figs. 4, 5, Sections 3, 4. Like *Chan*, *Wambacq* explains that an advantage of a single package solution relative to a “single-chip system” is that “partitioning of the system into its subsystems, each realized in the most suitable technology, will lead to lower cost, increase of manufacturing yield and optimal performance.” EX-1009 (Section 3). *See also Ryckaert* (EX-1011, p.1037) (disclosing a single-package RF module “using elements realized in different technologies” to meet the “performances expected from high-end applications . . . while keeping the cost and the size of the system as low as possible”).

56. *Wambacq* was not alone in implementing partitioning in RF modules. For example, in the same time frame as *Wambacq*, *Larson* (EX-1010) disclosed a chip-set for a then-commercially available personal handyphone system (PHS) transceiver that included multiple dies made from different semiconductor technologies, as shown in Fig. 2 below:

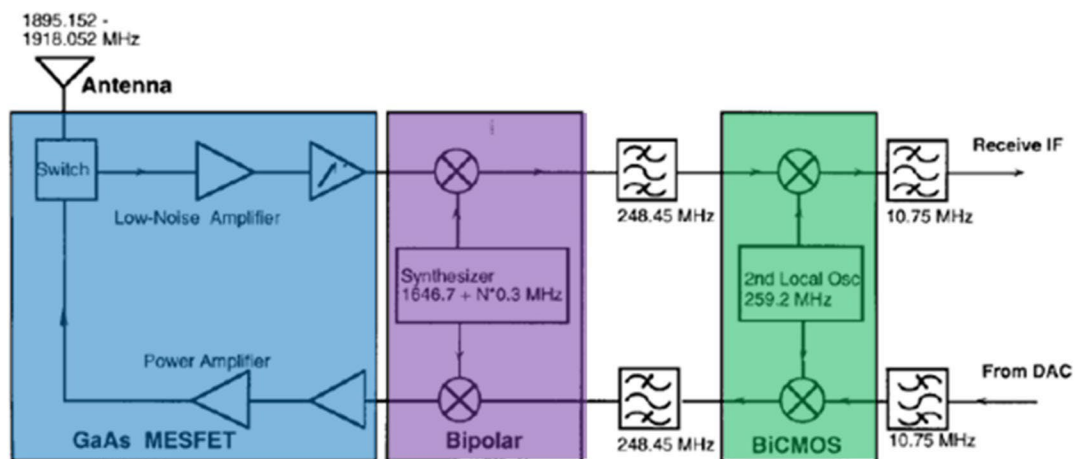


Fig. 2. Simplified block diagram of PHS transceiver [5].

EX-1010, Fig. 2 (annotated). *Larson* states:

The partitioning of the differing technologies in this system is fairly representative of current technologies, where **GaAs MESFET** technology is employed for the high-performance areas near the antenna (switch, low-noise, and power amplifiers), **silicon bipolar** technology is employed for the frequency synthesizer portion because of its low phase noise capabilities, and **BiCMOS** is used for higher levels of integration in a mixed-signal environment.

EX-1010, p.389.

3. It Was Well Understood that Different Semiconductor Technologies had Different Benefits for RF Circuit Design

57. By October 2003, RF circuit and module designers were well-versed regarding the attributes of different semiconductor technologies and their suitability for different electrical components and functionality. As the '200 Patent acknowledges, it was well known that GaAs technology can “offer more

gain per stage and lower losses” for RF components (e.g. PAs), but could be “unsuitable for the integration of ancillary circuits for use with the GaAs based RF component.” EX-1001, 2:16-20. The ’200 Patent also acknowledges that the benefits of SiGe BiCMOS technology were well-known, including its use for achieving “higher levels of integration of high-performance RF components,” such as some PAs and LNAs. EX-1001, 1:56-63. And, with respect to the suitability of certain semiconductor technologies for implementing PAs and passive components, the ’200 Patent states:

- a PA circuit is “**known** to have high loss, or low quality factor, when integrated on the silicon wafer” (EX-1001, 8:23-27); and
- “It is **well known** to those of skill in the art that inductors disposed on the silicon substrate suffer performance degradation due to absorption of RF energy within the substrate and other factors, as compared to inductors that are integrated on a semi-insulating GaAs substrate.” (EX-1001, 8:27-31).

58. The ’200 Patent’s statements regarding the known characteristics and suitability of various semiconductor technologies for RF integrated circuit designs are corroborated by the art. For example, in 1999, *Wambacq* disclosed that “in the majority of today’s RF front-end implementations most active components are realized in GaAs (e.g., LNA, power amplifier, mixer, antenna

switch) or silicon bipolar technologies (e.g. frequency synthesizer, mixer,...).” EX-1009 (Section 2). In the same time frame as *Wambacq, Larson* reported on the “advantages and disadvantage of each of the competing technologies—Si CMOS and bipolar junction transistors (BJT’s), Si/SiGe HBT’s and GaAs MESFET’s, PHEMTS and HBT’s”² in light of the various performance requirements for RF transceivers. EX-1010, p.387.

59. *Shi* (EX-1012), which also is directed to “low power, reduced size, reduced cost, and robust performance” multi-chip RF transceivers, provides other examples of the in-depth knowledge of the RF industry and the tradeoffs designers routinely faced. For instance:

Costs of manufacturing a radio frequency integrated circuit (IC) may be reduced by switching from one integrated circuit manufacturing process to another. For example, a CMOS process may be used instead of a GaAs, silicon bipolar or bi-CMOS process since it is a more cost affective [sic] method of IC manufacture and is typically the technology choice for digital ICs. Such a CMOS process, however, increases

² “HBT” refers to a heterojunction bipolar transistor. “MESFET” refers to a metal-semiconductor field effect transistor. “PHEMT” refers to pseudomorphic high electron mobility transistor.

temperature and process related variations. As such, noise, gain variation, mismatches and other factors that negatively impact an RF IC performance are increased for a CMOS process. Thus, **in many RF IC applications, a designer chooses between cost savings and performance.**

EX-1012, ¶¶7, 8.

4. Implementing Power Amplifier Circuits on Different Types of Semiconductor Dies Was Well-Known

60. By October 2003, it was well-known to implement PA circuits in semiconductor dies of various types. As an example, *Yamamoto* (EX-1015) discloses dual-band power amplifier circuitry 1A, including multiple power amplifier stages and impedance matching circuits, implemented in two semiconductor dies.

31

VI. CHALLENGES

A. Identification of Challenges

61. Based on my understanding of the law of obviousness discussed above, Claims 1-2, 4, 10-13, 15, 18-20, 23-26, and 29-31 of the '200 Patent are unpatentable as being obvious over Garlepp, alone, and Claims 1-2, 6, 10-15, 18-20, 23-26, and 29-31 are unpatentable as being obvious over Magoon in view of Ngompe.

Ground	Claims	Basis	Reference(s)
1	1-2, 4, 10-13, 15, 18-20, 23-26, and 29-31	§103	<i>Garlepp</i> (EX-1004)
2	1-2, 6, 10-15, 18-20, 23-26, and 29-31	§103	<i>Magoon</i> (EX-1005) in view of <i>Ngompe</i> (EX-1006)

B. Prior Art

62. 1. I have been informed that *Garlepp* (EX-1005) qualifies as prior art at least under (pre-AIA) 35 U.S.C. §102(a).

63. I have been informed *Magoon* (EX-1006) qualifies as prior art at least under (pre-AIA) 35 U.S.C. §102(a).

64. I have been informed *Ngompe* (EX-1007) qualifies as prior art at least under (pre-AIA) 35 U.S.C. §102(a).

VII. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE

A. Challenge 1: Claims 1-2, 4, 10-13, 15, 18-20, 23-26, and 29-31 and obvious under 35 U.S.C. §103(a) over *Garlepp*.

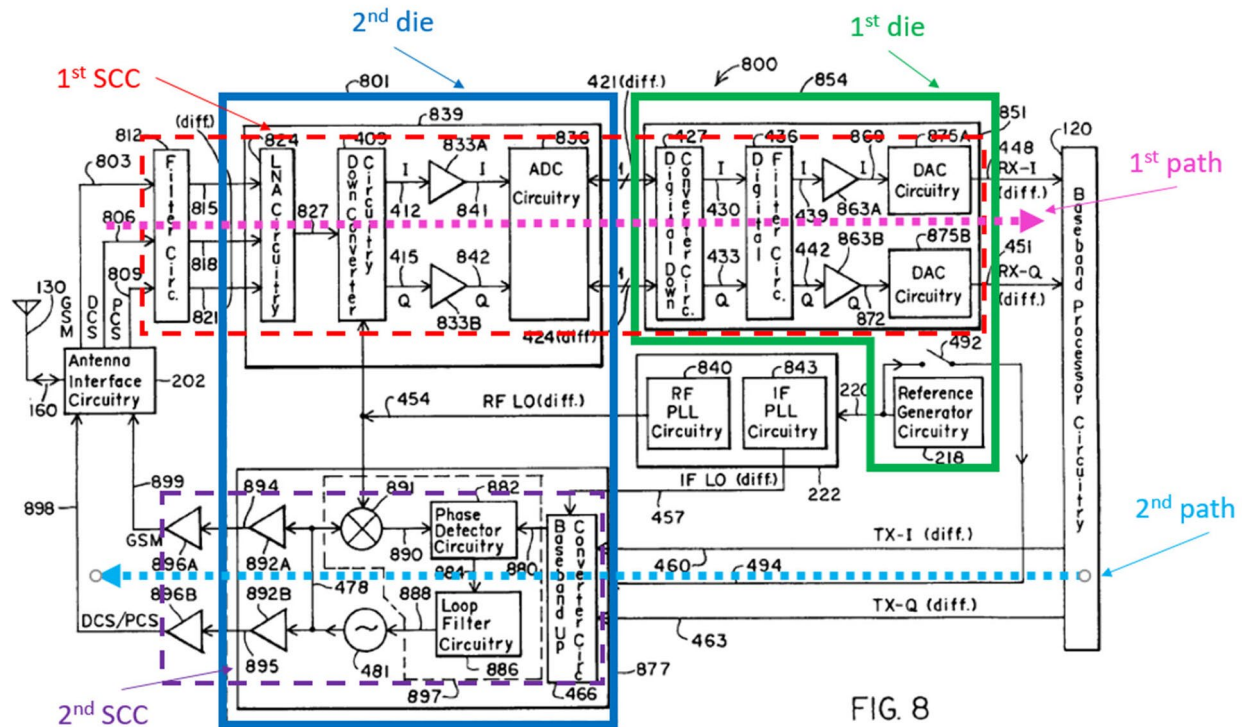
1. *Garlepp*

65. *Garlepp* is directed to the same problem as the '200 Patent:

“provid[ing] highly integrated, high-performance, low-cost, and low form-factor RF solutions,” for RF transceivers used in applications, such as cellular handsets. Although then-recent industry efforts had focused on “providing an RF transceiver within a single integrated circuit (IC),” *Garlepp* recognized the same solution proposed by the '200 Patent, e.g., that partitioning the RF circuitry into circuit blocks integrated within different semiconductor dies could improve performance, while at the same time resulting in a low-cost and low form-factor solution. EX-1005, ¶5, 46.

66. *Garlepp*'s partitioned transceiver 800 is shown in annotated FIG. 8 (Annotated FIG. 8)³:

³ Annotated FIG. 8 is from corresponding U.S. Patent No. 7,035,611, representing the formal drawing corresponding to the handwritten FIG. 8 from EX-1005.



EX-1005, FIG. 8 (annotated).

67. Garlepp's RF transceiver includes two signal conditioning circuits disposed along separate signal paths: **receive path** circuitry 839, 851 and **transmit path** circuitry 877. EX-1005, ¶86. Garlepp's **first SCC** is partitioned into portions 839, 851 that are integrated within a respective **first die** 854 and a **second die** 801 that are manufactured from separate semiconductor processes. EX-1005, ¶¶103, 141. The entirety of the **second SCC** (877) is integrated within the **second die** 801. Thus, a **first signal path** is formed from an RF signal input port through the portion 839 of the **first SCC** within the **second die** 801, through the portion 854 of the **first SCC** within the **first die** 854 to a baseband signal output port. The **second signal path** is formed from a baseband signal input port

through the **second SCC** within the **second die** 512 and to an RF signal output port.

68. Thus, *Garlepp* discloses the same circuit partitioning and integration arrangement as the '200 Patent claims, in which a signal conditioning circuit is partitioned along a signal path and integrated within different semiconductor dies in a manner best suited to enhance performance, while also reducing cost and size.

2. Detailed Application of *Garlepp* to the Challenged Claims

Claim 1

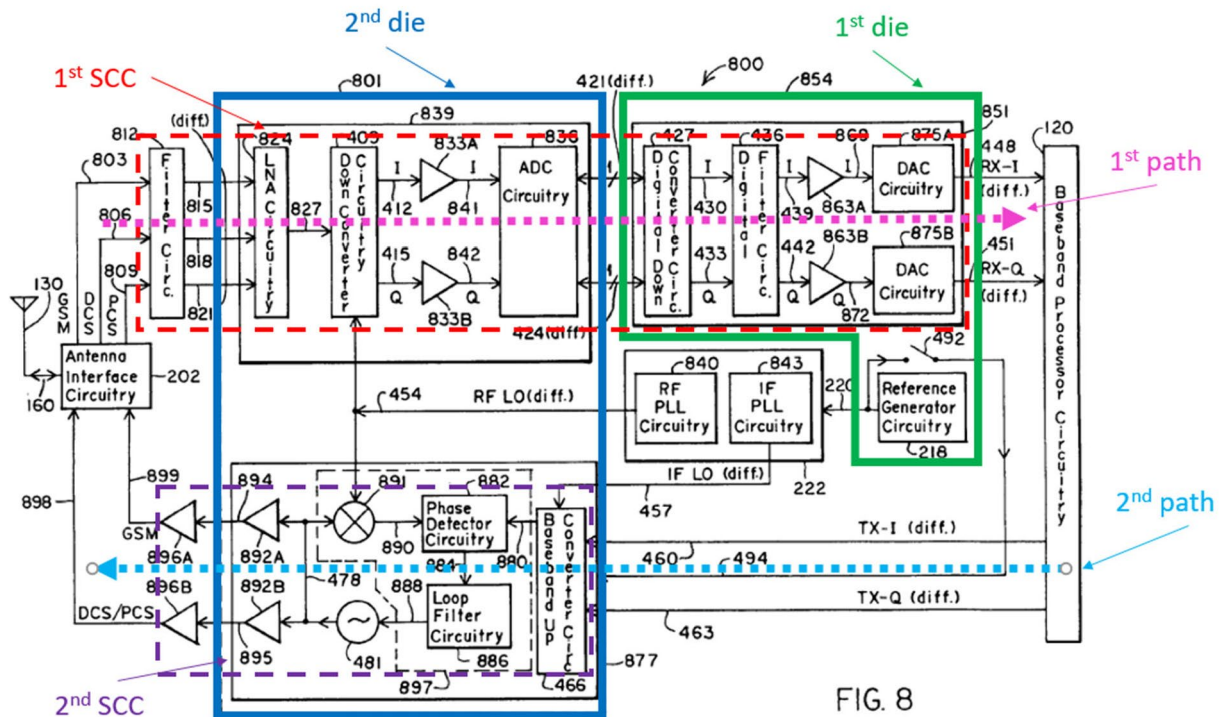
[1.0] An electronic apparatus comprising:

69. To the extent the preamble is limiting, *Garlepp* discloses “partitioning RF apparatus [*electronic apparatus*] so as to provide highly integrated, high-performance, low-cost, and low form-factor RF solutions.” EX-1005, ¶46.

[1.1] a first integrated circuit semiconductor die comprising:

70. *Garlepp* discloses “**integrated circuit devices**” made from “**semiconductor** fabrication processes” for use in an “RF apparatus, such as a cellular telephone handset **chipset** implemented in complementary metal oxide **semiconductor**” (*integrated circuit semiconductor dies*). EX-1005, ¶¶6, 141.

71. *Garlepp* discloses that its RF transceiver includes “circuit partitions, or circuit blocks.” EX-1005, ¶103. In FIG. 8, **partition 854** (*first integrated circuit die*) includes the receiver digital circuitry 851. EX-1005, ¶103:



EX-1005, Annotated FIG. 8.

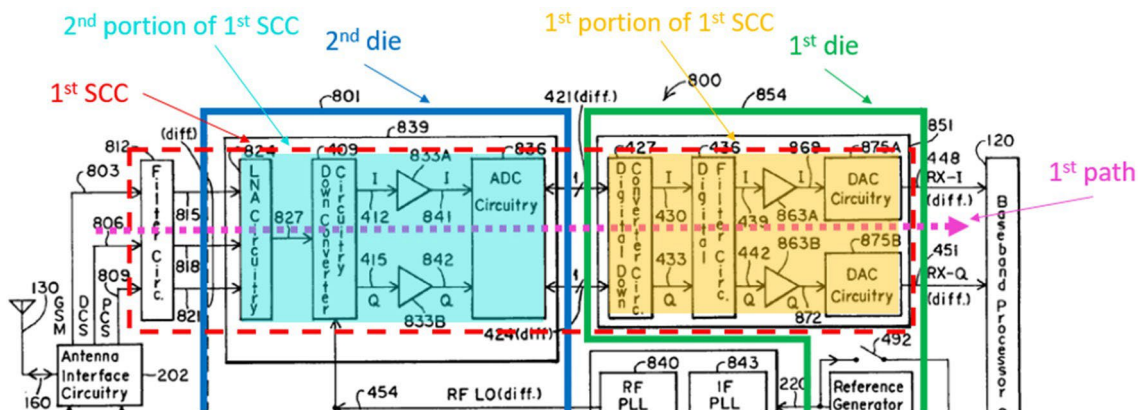
72. *Garlepp* also discloses that each circuit **partition** “resides within an **integrated circuit device**” (*integrated circuit die*). EX-1005, ¶103. *Garlepp* further discloses “a **silicon die that houses** the receiver circuitry.” EX-1005, ¶230. *Garlepp* further discloses that the circuit architecture of the RF transceiver “allows **on-chip integration** of the digital filter circuitry,” which is part of the “circuit partition” that includes the receiver digital circuitry 851. EX-

1005, ¶230. *Garlepp* uses the terms “integrated circuit device,” “die,” and “chip” interchangeably, thus corroborating that a circuit partition “residing within an integrated circuit device” is circuitry integrated within an *integrated circuit semiconductor die*.

[1.2] a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path; and

73. *Garlepp* discloses “**receive path circuitry**” (first signal conditioning circuit) arranged on a **first signal path** between the antenna interface circuitry 202 and baseband processor 120 (*disposed along a first signal path*), as shown in Annotated FIG. 8 above. EX-1005, ¶¶XX; EX-1005, FIG. 8 (annotated).

74. The **receive path circuitry** includes receiver digital circuitry 851 (first portion) within **partition 854** (first integrated circuit die) as shown in the portion of Annotated FIG. 8 below. EX-1005, ¶¶86, 103.



EX-1005, FIG. 8 (annotated).

75. As described below with respect to limitation [1.4], the **first SCC** also includes a **second portion** arranged along the **first signal path** on the **partition** 801 (*second integrated circuit die*). EX-1005, ¶¶86, 103. The **second portion** includes analog receive circuitry 839 (which includes low noise amplifier (LNA) circuitry 824, down-converter circuitry 409, programmable gain amplifiers (PGAs) 833A,B, and ADC 836) that accepts filtered RF signals from filter circuitry 812 and generates in-phase and quadrature receive signals 421, 424 at its output. The **first portion** includes digital receive circuitry 851 (which includes digital down-converter circuitry 427, digital filter circuit 436, PGAs 863A,B and DAC 875A,B) that accepts signals 421, 424 and generates analog receive signals 448, 451 at its output, which are provided to baseband circuitry 120. In other words, *Garlepp* teaches that the “**receive path circuitry**” accepts “filtered RF signals” at an input and operates on the signals along the “receive path” to provide “analog receive signals” at an output. EX-1005 ¶¶91-94, 96-97.

76. A POSITA understood that the functions performed by the **receive path circuitry** (i.e., amplify 824, down-convert 409, amplify 833, up-convert 427, filter 436, amplify 863) condition the receive signal as it propagates along the receive signal path. These functions are “signal conditioning” because the signals are amplified, frequency-translated, and filtered by the various stages of

the receive path circuitry to prepare the signals for the next stage in the receive path. (EX-1016 (“**signal conditioning**” is “processing of a signal to improve its intelligibility, signal-to-noise ratio, or the like”; “processing or conversion of a signal, so as to make it compatible with a given channel, device, or system”)).

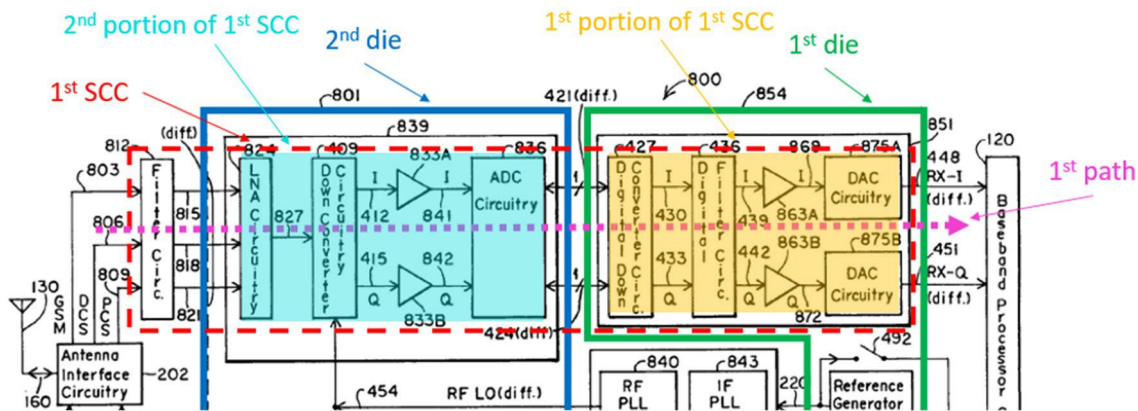
77. Garlepp therefore discloses that the **receive path circuitry** is a *first signal conditioning circuit* (“SCC”) disposed along *a first signal path*, and the **digital receiver circuitry 851** is a *first portion* of the *first SCC*.

[1.3] a second integrated circuit semiconductor die comprising;

78. Garlepp discloses a **partition 801** that resides within a different semiconductor integrated circuit device (*second integrated circuit semiconductor die*). As explained above for element [1.1], partition 801 is formed as an integrated circuit on *a semiconductor die*. EX-1005 ¶¶103, 141.

[1.4] a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first portion of a first signal conditioning circuit for a signal propagating along the first signal path; and,

79. Garlepp discloses “**receive path circuitry**” (*first SCC*) includes **receiver analog circuitry 839** (*second portion*) integrated within **partition 801** (*second die*) and **receiver digital circuitry 851** (*first portion*) integrated within **partition 854** (*first die*), as shown in the portion of Annotated FIG. 8 below:



EX-1005, ¶¶91-97, FIG. 8 (annotated).

80. As explained above for element [1.2], the amplifying and down-converting functions performed by the receiver analog circuitry 839 (*second portion*) and the down-converting, filtering, amplifying functions performed by receiver digital circuitry 851 (*first portion*) that are described in *Garlepp* are *signal conditioning functions on a signal propagating along the first signal path*.

[1.5] a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.

81. Element [1.5] merely adds a substrate to support the first and second dies and provide interconnections between them. As discussed in the State of the Art above (Section V.F), a POSITA understood that the first and second dies of *Garlepp*'s chipset would be interconnected (e.g., by wire bonding or flip-chip assembly) and supported on a common structure (*a substrate*) because that was the well-known and conventional way of connecting and

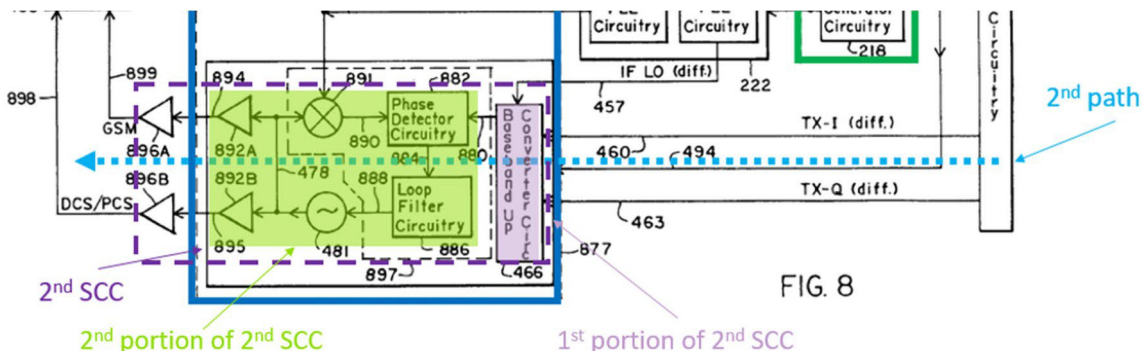
supporting semiconductor chipsets. EX-1008, ¶5; EX-1009, (Section 3); EX-1013, FIG. 7, 7:4-22; EX-1014, 1:1-28. Further, *Garlepp* discusses that any conventional packaging method, including modules, can be used to provide a low-cost and low form-factor RF solution. EX-1005, ¶¶46, 164 (“circuit partitions may alternatively reside within other substrates, carriers, or packaging arrangements. By way of illustration, other partitioning arrangements may use **modules**, thin-film modules, thick-film modules, isolated partitions on a single substrate, circuit-board partitions, and the like”), 272-273 (disclosing that antenna interface circuitry 202 can be coupled “to an integrated circuit or **module** that includes the rest of the RF receive path circuitry,” such as the “circuitry shown in FIG. 8”).

Claim 2

[2.0] An electronic apparatus according to claim 1, comprising a second signal conditioning circuit comprising a first portion of the second signal conditioning circuit and a second portion of the second signal conditioning circuit integrated within the second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path.

82. *Garlepp* discloses RF transceiver 800 includes transmitter circuitry 877 that provides transmit signals 894, 895 to power amplifiers 896A, 896B (second signal conditioning circuit). *Garlepp* discloses transmitter circuitry 877

is integrated within **partition 801** (*second integrated circuit die*); accepts “transmit input signals” 460, 463 from baseband circuitry 120; and provides “buffered transmit signals” 894, 895 to **power amplifiers 896A, 896B**, which provide “amplified RF signals” 899, 898. EX-1005, ¶¶100-101. *Garlepp* therefore discloses that the **transmitter circuitry 877** and **power amplifiers 896A, 896B** (collectively, *second SCC*) are disposed along a *second signal path* because circuitry 877 accepts transmit input signals at its input and power amplifiers 896 generate amplified transmit signals at the output. As shown in the portion of annotated FIG. 8 below, the **transmit signal path** (*second path*) is different than the **receive signal path** (*first path*).



EX-1005, FIG. 8 (annotated).

83. *Garlepp* further discloses that **transmitter circuitry 877** (*second conditioning circuit*) includes **offset phase lock loop (PLL) circuitry 897**, **transmit voltage controlled oscillator (VCO) circuitry 481** and **output buffers**

892A,B (second portion); and baseband up-converter circuitry 466 (first portion). EX-1005, FIG 8 (annotated), ¶¶100-102.

84. *Garlepp* discloses that the baseband up-converter circuitry 466 accepts the analog transmit input signals 460, 463, mixes those signals with the IF local oscillator signal 457, and provides a transmit IF signal 880 to the offset PLL circuitry 897. The offset mixer circuitry 891 in circuitry 897 mixes the transmit VCO output signal 478 with the RF local oscillator signal 454, and provides a mixed signal 890 to the phase detector circuitry 882. The phase detector circuitry 882 compares the mixed signal 890 to the transmit IF signal 880 and provides an offset PLL error signal 884 to the loop filter circuitry 886. The loop circuitry 886 provides a filtered offset PLL signal 888 to the transmit VCO circuitry 481. Transmitter output buffers 892A and 892B receive the transmit VCO output signal 478 and provide buffered transmit signals 894 and 895 to a pair of power amplifiers 896A and 896B. EX-1005, ¶¶100-102.

85. A POSITA understood that the functions performed by the first and second portions of the transmitter circuitry 877 (i.e., up-convert, mix, buffer) condition the transmit signal as it propagates along the transmit signal path. These functions are “signal conditioning” because they are operations performed to prepare the signals for use by the next stage in the transmit path. *Garlepp* therefore discloses that the transmitter circuitry 877 is a *second signal*

conditioning circuit disposed along a second signal path, which includes first and second portions that perform a signal conditioning function on a signal propagating along a second signal path.

Claim 4

[4.0] An electronic apparatus according to claim 1, wherein the first integrated circuit die is manufactured using a first semiconductor process and utilizes a silicon-based technology.

86. As discussed above, receiver digital circuitry 851 resides within first die 854 (*first integrated circuit die*). EX-1005, ¶103.

87. *Garlepp* discloses that its RF transceiver can be “a cellular telephone handset chipset implemented in complementary metal oxide semiconductor (CMOS).” EX-1005, ¶6. Further, with reference to FIG. 15, *Garlepp* discloses “CMOS implementation of the receiver circuitry 1520,” which “may constitute . . . the receiver circuitr[y] shown in the preceding figures [including FIG. 8].” EX-1005, ¶¶181, 202. A POSITA understood that CMOS is a *semiconductor process that utilizes a silicon-based technology*, as corroborated by *Garlepp*’s disclosure of “a **silicon die** that houses the receiver circuitry.” EX-1005, ¶230. Further, as discussed in the State of the Art, *supra*, the use of “a CMOS process . . . is typically the technology choice for digital ICs” and, thus, would have been an obvious design choice for implementing

receiver digital circuitry 851 in the first die that would achieve known and predictable results. EX-1012, ¶7.

Claim 10

[10.0] An electronic apparatus according to claim 2, wherein the first semiconductor process does not facilitate manufacturing and integration of at least one of the second portion of the first signal conditioning circuit and the second portion of the second signal conditioning circuit.

88. As discussed with respect to claims 1 and 2, the *second portion of the first signal conditioning circuit and the second portion of the second signal conditioning circuit* are on the *second die*. *Garlepp* discloses that the *first and second dies* “typically result from separate semiconductor fabrication processes and manufacturing lines.” EX-1005, ¶141.

89. By disclosing “separate” semiconductor fabrication processes and manufacturing lines, *Garlepp* is disclosing that the second die is fabricated using a semiconductor process that is different than the first semiconductor process used for the first die. Because *Garlepp* uses different semiconductor processes for the two dies—one of which houses the analog circuitry and the other of which houses the digital circuitry—a POSITA understood that the semiconductor process for the first die does not facilitate manufacturing and integration of at least one of the second portion of the first signal conditioning circuit and the second portion of the second signal conditioning circuit, which

are on the second die. *Garlepp*'s disclosure that the analog LNA circuitry (which is integrated on the *second die*) can be a "CMOS bipolar implementation" corroborates that different semiconductor processes are used for the digital circuitry on the first die and the analog circuitry on the second die. EX-1005, ¶¶181, 203.

90. Moreover, as discussed in the State of the Art, *supra*, the use of different semiconductor technologies and processes within a single module or on a common supporting substrate, where the circuit partitions are "matched with a particular semiconductor substrate technologies and/or semiconductor fabrication processes for enhancing performance, reducing unit cost, etc.," was a well-known, conventional design practice. EX-1008, ¶¶5, 25; EX-1009, Figs. 4, 5, Sections 3, 4; EX-1010, p.389; EX-1011, p.1037.

Claim 11

[11.0] An electronic apparatus according to claim 1, wherein the second integrated circuit die is manufactured using a second semiconductor process that is different from that used to manufacture the first integrated circuit die.

91. *Garlepp* discloses this limitation for the same reason as discussed with respect to Claim 10.

Claim 12

[12.0] An electronic apparatus according to claim 1, wherein the first integrated circuit die is derived

from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.

92. For the reasons discussed above for Claim 4, *Garlepp* discloses this limitation.

Claim 13

[13.0] An electronic apparatus according to claim 12, wherein the second integrated circuit die is derived from a second semiconductor wafer comprised of other one of Si, SiGe, GaAs, InP, and GaN.

93. *Garlepp* discloses that the first and second dies are made from different semiconductor fabrication processes. EX-1005, ¶141. *Garlepp* further discloses that the LNA circuitry, which is integrated on the *second die*, can be a “CMOS bipolar implementation.” EX-1005, ¶¶181, 203. A POSITA understood that a SiGe process technology (“*wafer comprised of other one of Si*”) is an obvious design choice for implementing CMOS bipolar (i.e., BiCMOS) circuitry in a die that would achieve known and predictable results.

94. Further, as explained in the State of the Art, *supra*, the use of wafers made of semiconductor materials other than native Si, such as SiGe, for high-performance RF circuits (e.g., analog receiver circuitry 839 and transmitter circuitry 877) was well-known and routine. *E.g.*, EX-1001, 1:56-63 (the use of SiGe BiCMOS technology can achieve “higher levels of integration of high-performance RF components,” such as PAs and LNAs). A POSITA would have

been motivated to use a known non-native Si wafer, such as a SiGe wafer, to integrate *Garlepp*'s receiver analog circuitry 839 and transmit circuitry 877 in partition 801 to enhance performance, increase the level of integration and reduce size in a known and predictable manner.

Claim 15

[15.0] An electronic apparatus according to claim 1, wherein the second portion of the first signal conditioning circuit comprises at least one of a capacitor and an inductors and a signal transmission line.

95. In addition to the receiver path circuitry (*first SCC*) discussed above for claim 1, *Garlepp* discloses a “matching network 1515” that provides impedance matching between filter circuitry 812 and the input stage (i.e., LNA circuitry 834) of receiver analog circuitry 839 (*second portion of first SCC*). EX-1005, ¶¶180-181. *Garlepp* further discloses that “one may use distributed **transmission lines** to perform impedance transformation” in “a differential distributed matching network” and that “one may fully or partially implement any of the differential **transmission lines** described above using ... the substrate of a silicon die (such as a **silicon die that houses the receiver circuitry**).” EX-1005, ¶¶221, 228, 230. By disclosing that the transmission lines (1) provide for impedance matching between the filter circuitry 812 and the input stage of receiver analog circuitry 839 and (2) can be implemented in the die that houses

the receiver circuitry, *Garlepp* is disclosing that the receive circuitry 839 (second portion of first SCC) comprises a signal transmission line.

Claim 18

[18.0]. A method of manufacturing a module comprising:

96. To the extent the preamble is limiting, *Garlepp* teaches this limitation for the same reasons as discussed with respect to limitation [1.0].

[18.1] providing a first signal conditioning circuit comprising a first portion and a second portion;

97. *Garlepp* teaches this limitation for the same reasons as discussed with respect to limitations [1.2] and [1.4].

[18.2] providing a second signal conditioning circuit comprising a first portion and a second portion;

98. *Garlepp* teaches this limitation for the same reasons as discussed with respect to Claim 2.

[18.3] implementing the first portion of the first signal conditioning circuit within a first semiconductor die;

99. *Garlepp* teaches this limitation for the same reasons as discussed with respect to limitations [1.1] and [1.2].

[18.4] implementing the second portion of the first signal conditioning circuit within a second semiconductor die;

100. *Garlepp* teaches this limitation for the same reasons as discussed with respect to limitations [1.3] and [1.4].

[18.5] implementing the first and second portions of the second signal conditioning circuit in the second semiconductor die;

101. *Garlepp* teaches this limitation for the same reasons as discussed with respect to Claim 2.

[18.6] bonding the first and second dies to a common substrate; and,

102. *Garlepp* teaches this limitation for the same reasons as discussed with respect to limitation [1.5]. Further, as discussed in the State of the Art, *supra*, manufacturing a multiple-die module by bonding dies to a common substrate was a well-known, conventional practice. EX-1008, ¶5; EX-1014, 1:1-28; EX-1013, FIG. 7, 7:4-22.

[18.7] forming electrical connections between the two dies to complete the first signal conditioning circuit from the first portion of the first signal conditioning circuit and the second portion of the first signal conditioning circuit.

103. *Garlepp* teaches this limitation for the same reasons as discussed with respect to limitation [1.5].

Claim 19

[19.0] A method according to claim 18, wherein the first semiconductor die comprises a first portion of a first signal path and the second semiconductor die comprises a second portion of the first signal

path, the first signal path disposed between a first input port and a first output port.

104. *Garlepp* discloses this limitation for the same reasons as discussed with respect to Claim 1.

Claim 20

[20.0] A method according to claim 19, wherein the second semiconductor die comprises a second signal path that is other than the second portion of the first signal path and in approximate RF isolation therefrom.

105. *Garlepp* discloses this limitation for the same reason as discussed with respect to Claims 1 and 2. Further, *Garlepp* also discloses that the “timing of the transmit mode and receive mode in the GSM specifications help to mitigate potential interference between the transceiver’s receive-path circuitry and its transmit-path circuitry” (*in approximate RF isolation therefrom*). EX-1005, ¶62.

Claim 23

[23.0] A method according to claim 18, wherein the first semiconductor die does not facilitate implementation of the second portion of the first signal conditioning circuit therein.

106. *Garlepp* discloses this limitation for the same reason as discussed with respect to Claim 10.

Claim 24

[24.0] A method according to claim 18, wherein implementing of the second portion of the first signal conditioning circuit within the second semiconductor die provides increased performance in signal conditioning as compared to implementing of the second portion of the first signal conditioning circuit within the first semiconductor die.

107. *Garlepp* discloses: “The receiver analog circuitry [*second portion of first SCC within second die*] and the receiver digital circuitry [*first portion of first SCC within first die*] are partitioned so that interference effects between the receiver analog circuitry and the receiver digital circuitry tend to be reduced.” EX-1005, Abstract. By stating that *Garlepp*’s partitioning reduces interference, *Garlepp* is disclosing that implementing the receiver analog circuitry (*second portion of first SCC*) in the *second die* as opposed to in the *first die* provides for *increased performance in signal conditioning*.

Claim 25

[25.0] A method according to claim 18, wherein prior to implementing the first signal conditioning circuit comprises partitioning of the first signal conditioning circuit into the first portion and the second portion.

108. *Garlepp* discloses this limitation for the same reason as discussed with respect to Claim 1. Further, as discussed in the State of the Art,

partitioning a circuit prior to implementing it was a routine and conventional design practice. EX-1008, ¶¶2, 5.

Claim 26

[26.0] An electronic apparatus comprising:

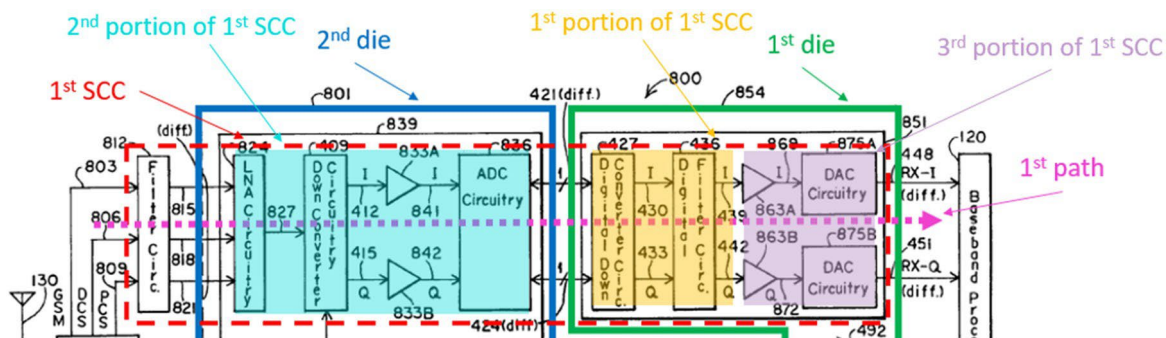
109. *Garlepp* discloses this limitation for the reasons discussed with respect to limitation [1.0].

[26.1] a first integrated circuit semiconductor die comprising:

110. *Garlepp* discloses this limitation for the reasons discussed with respect to limitation [1.1].

[26.2] a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path;

111. As explained above for Claim 1, *Garlepp* discloses that the **receive path circuitry** (*first SCC*) includes receiver digital circuitry 851 integrated within **partition 854** (*first die*) that conditions signals propagating on the **receive path** (*first signal path*). EX-1005, ¶103. *Garlepp* further discloses circuitry 851 includes **digital down-converter circuitry 427 and digital filter circuitry 436** (*first portion*) and **digital PGAs 863A,B and DAC 875A,B** (*third portion*). EX-1005, ¶¶96-97.



EX-1005, FIG. 8 (annotated).

[26.3] a third portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along the first signal path; and

112. *Garlepp* discloses this limitation for the reasons discussed with respect to limitation [26.2].

[26.4] a second integrated circuit semiconductor die comprising;

113. *Garlepp* discloses this limitation for the reasons discussed with respect to limitation [1.3].

[26.5] a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first and third portions of the first signal conditioning circuit for a signal propagating along the first signal path; and,

114. *Garlepp* discloses this limitation for the reasons discussed with respect to limitations [1.4] and [26.2].

[26.6] a substrate for supporting the first and second integrated circuit semiconductor dies and for

providing electrical connection to and from the first and second integrated circuit semiconductor dies.

115. *Garlepp* discloses this limitation for the reasons discussed with respect to limitation [1.5].

Claim 29

[29.0] An electronic apparatus according to claim 26, comprising a second signal conditioning circuit comprising a first portion of the second signal conditioning circuit and a second portion of the second signal conditioning circuit integrated within the second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path.

116. *Garlepp* discloses this limitation for the reasons discussed with respect to Claim 2.

Claim 30

[30.0] An electronic apparatus according to claim 26, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.

117. *Garlepp* discloses this limitation for the reasons discussed with respect to Claim 12.

Claim 31

[31.0] An electronic apparatus according to claim 30, wherein the second integrated circuit die is derived from a second semiconductor wafer

comprised of other one of Si, SiGe, GaAs, InP, and GaN.

118. *Garlepp* discloses this limitation for the reasons discussed with respect to Claim 13.

B. Challenge 2: Claims 1-2, 6, 10-15, 18-20, 23-26, and 29-31 are obvious under 35 U.S.C. §103(a) over Magoon in View of Ngompe.

1. Magoon

119. *Magoon* discloses a quadband RF transceiver BiCMOS chip for GSM/GPRS 850/900/1800/1900 applications “that integrates all of the functions necessary to implement a multiband homodyne global system for mobile telecommunication radio except for the power amplifier (PA) and radio frequency (RF) passives”. EX-1006, p.1710 (Abstract). *Magoon* is directed to the same goal as the '200 Patent, *e.g.*, increasing the level of circuit integration, while reducing costs and size. According to Magoon:

As modern cellphones become ubiquitous, the critical factors in their manufacture become cost, size, and time to market. The high integration of radio ICs reduces board area and complexity while cutting component cost and system design time.

120. EX-1006, p.1710 (Section I). *Magoon* discloses the same solution as the '200 Patent: partitioning signal conditioning circuits along their signal paths and integrating the partitions within different semiconductor dies. The

receive circuitry is integrated within a silicon-based BiCMOS transceiver chip, while the transmit circuitry is partitioned into a transmit section on the same BiCMOS chip and an off-chip PA circuitry. EX-1006, p.1710 (Abstract), p.1718-19 (Section VII), Fig. 20. While *Magoon* does not provide details about the off-chip PA circuitry, as discussed in more detail below, a POSITA understood that the circuitry was formed in a semiconductor die.

121. Annotated Fig. 1 illustrates the architecture of *Magoon's* transceiver, including the transceiver chip and the off-chip PA circuitry:

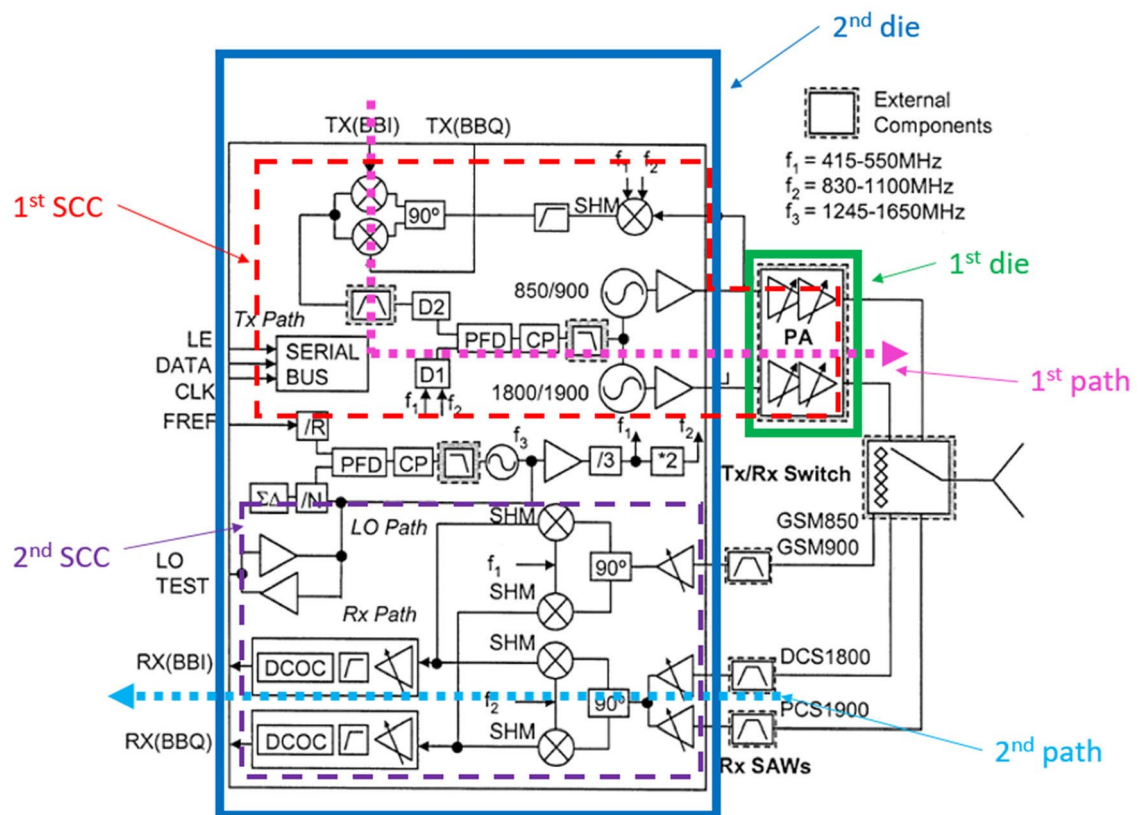


Fig. 1. Top-level schematic of transceiver, with external RF components.

EX-1006, Annotated Fig. 1.

122. The transceiver chip includes a receive (Rx) path (*second signal path*) and a transmit (Tx) path (*first signal path*). Receive signal conditioning circuitry along the receive path receives RF signals on pins or bond-wires at the inputs of the low-noise amplifiers (LNAs) and provides baseband receive signals (RX(BBI), RX(BBQ)) at output pins or bond-wires. EX-1006, p.1710 (Section II), Fig. 1.

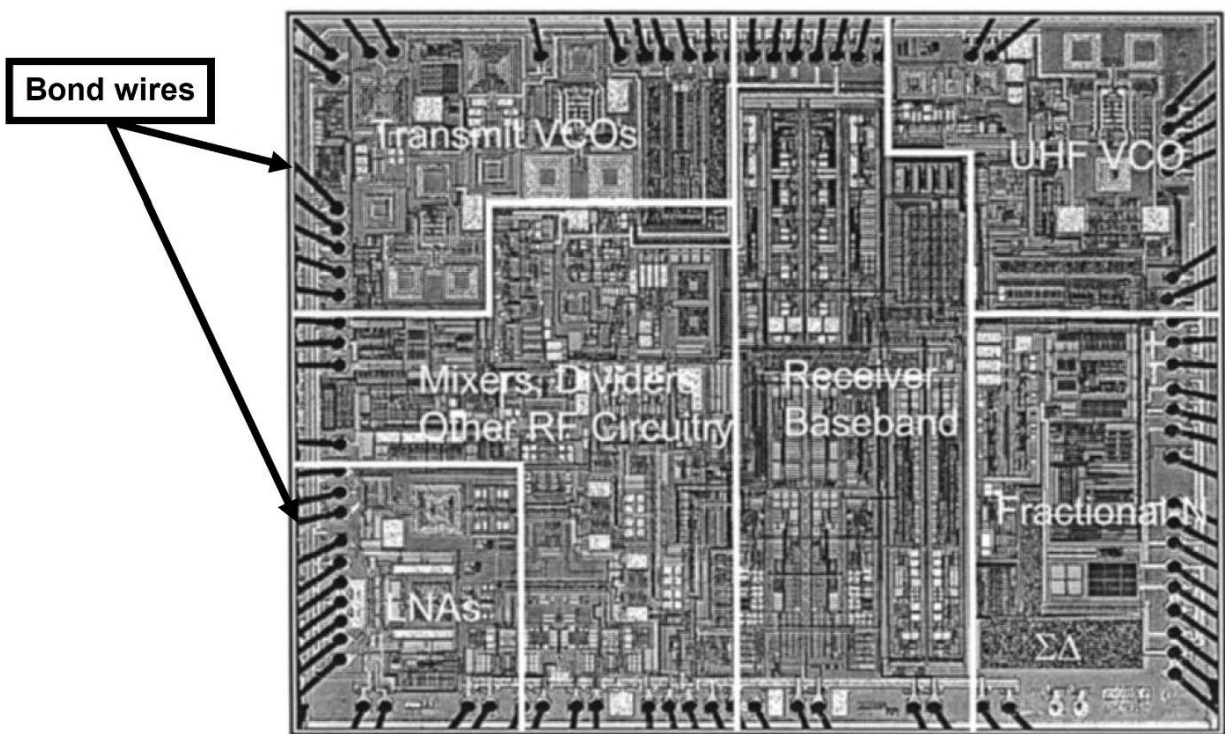


Fig. 20. Microphotograph of transceiver.

EX-1006, Fig. 20 (annotated).

123. The portion of the transmit signal conditioning circuitry along the **transmit path** on the transceiver chip receives baseband transmit signals at the input and provides RF signals at output pins or bond-wires to the off-chip PA

circuitry. EX-1006, p.1710 (Section II). The off-chip PA circuitry (which is another portion of the transmit signal conditioning circuitry) provides amplified RF signals for transmission via an antenna.

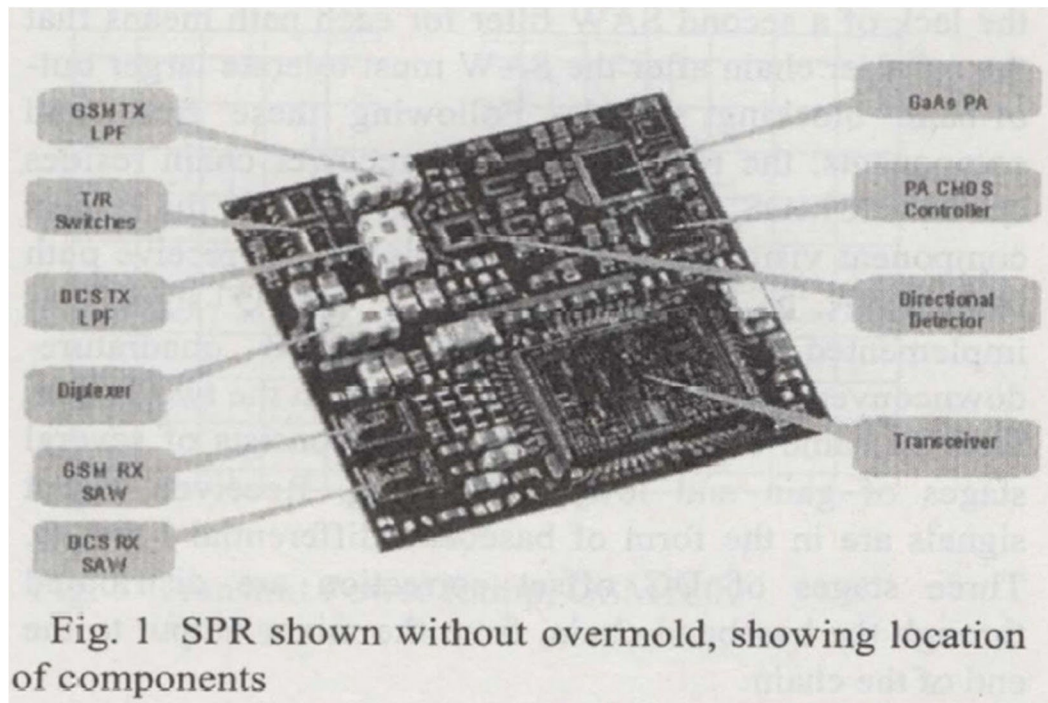
124. Thus, just like the '200 Patent, *Magoon* discloses two interconnected semiconductor devices and two signal conditioning circuits along two signal paths. One signal conditioning circuit (the receiver circuitry) resides entirely within one die, while the other signal conditioning circuit (the transmitter circuitry) is partitioned between both dies for the same purpose as described in the '200 Patent, e.g., to take advantage of the beneficial attributes of both semiconductor substrates, including the well-known attribute of using silicon-based BiCMOS for higher levels of integration of high performance RF components (such as LNAs) and a different semiconductor technology best suited for PAs.

2. Ngompe

125. *Ngompe* discloses a single-package radio (SPR) module for a cellular handset that “realizes all the RF functions required for the dual-band GSM [900/1800] application.” EX-1007, p.387 (Abstract). Like the '200 Patent's module and *Magoon*, the SPR module is implemented on a substrate that supports and interconnects multiple components where “[d]iverse die

technologies are utilized to apply the optimum process for each function.” *Id.*

The SPR module is shown in Fig. 1:



EX-1007, Fig. 1 (annotated).

126. *Ngompe* discloses: “The assembly consists of a combination of chip-on-board with wire bonding, and reflow-soldered SMT components.” EX-1007, p.387. Among other components, the SPR module includes a BiCMOS transceiver die and a GaAs HBT PA. EX-1007, p.387 (Abstract), Fig. 1.

127. *Ngompe*’s BiCMOS transceiver die includes substantially the same receive and transmit circuitry as *Magoon*’s BiCMOS transceiver die, with the exception that *Ngompe*’s dualband transceiver covers 900 MHz and 1800 MHz applications while *Magoon*’s quadband transceiver further covers 850 MHz and

1900 MHz. Specifically, the receive circuitry in both transceiver dies follows a direct-conversion architecture, and the transmit circuitry includes an up conversion phase locked loop (PLL) chain with on-chip voltage controlled oscillators (VCOs) to drive the off-chip PAs. *Compare* EX-1006, Abstract & Fig. 1 *with* EX-1007, Abstract & Fig. 2.

3. Motivation to Combine

128. The authors of both *Magoon* and *Ngompe* were with Skyworks Solutions, Inc., the Patent Owner. EX-1006, p.1710; EX-1007, p.387. *Magoon* teaches a quadband RF transceiver that includes a silicon-based BiCMOS transceiver chip and off-chip PA circuitry, but does not provide the details of the off-chip PA. *Ngompe* teaches a “single package radio” (SPR) module implemented as a dualband RF transceiver that includes a BiCMOS transceiver chip and off-chip GaAs PA chip mounted on and interconnected by a common substrate. *Ngompe* discloses “[d]iverse die technologies are utilized to apply the optimum process for each function.” EX-1007, p.387 (Abstract).

129. First, it would have been obvious to combine *Magoon* with *Ngompe*’s teachings to achieve a “single package radio” with *Magoon*’s BiCMOS chip and PA circuitry mounted on and interconnected by a common substrate. *Ngompe* discloses that its SPR solution is “implemented on a low cost 4-layer laminate substrate” and “makes use of multiple semiconductor and

packaging technologies to condense” the size of the complete radio. P.387 (Abstract); P.390 (Conclusion). *Magoon* teaches that as “cell phones become ubiquitous, the critical factors in their manufacture become cost, size, and time to market.” P.1710 (Introduction). A POSITA would have been motivated to apply the express semiconductor die and packaging teachings of *Ngompe* to *Magoon*’s known RF transceiver to achieve a high-performance, low cost, condensed size SPR solution with a fast time to market, particularly given that *Ngompe* and *Magoon* utilize the same type of transceiver design for the same types of RF applications (with the exception that *Ngompe*’s transceiver includes circuitry for only two of the RF bands covered by *Magoon*’s transceiver).

130. Second, as discussed in the State of the Art, *supra*, doing so would have been nothing more than applying known multi-chip packaging techniques to a known RF transceiver to achieve a predictable result. EX-1008, ¶5 (packaging of multiple diverse semiconductor dies on a common laminate substrate was “conventional”); EX-1009 (Section 3) (disclosing “single-package solution” for a RF transceiver having GaAs and silicon chips mounted on a common substrate); EX-1013, FIG. 7, 7:4-22; EX-1014, 1:1-28.

131. Moreover, a POSITA would have had a reasonable expectation of success in combining *Ngompe*’s packaging solution with *Magoon*’s RF transceiver. Doing so would involve no more than routine skill to achieve

predictable results, as demonstrated in the State of the Art, *supra*. EX-1008, ¶5; EX-1009 (Section 3); EX-1013, FIG. 7, 7:4-22.

4. Detailed Application of Magoon in View of Ngompe to the Challenged Claims

Claim 1

[1.0] An electronic apparatus comprising:

132. To the extent the preamble is limiting, *Magoon* discloses an “RF transceiver” (*an electronic apparatus*). EX-1006, p.1710; Fig. 1.

[1.1] a first integrated circuit semiconductor die comprising:

133. *Magoon* in view of *Ngompe* discloses this limitation.

134. *Magoon* discloses a quadband radio transceiver that includes power amplifier circuitry and a BiCMOS chip. EX-1006, p.1710 (Abstract).

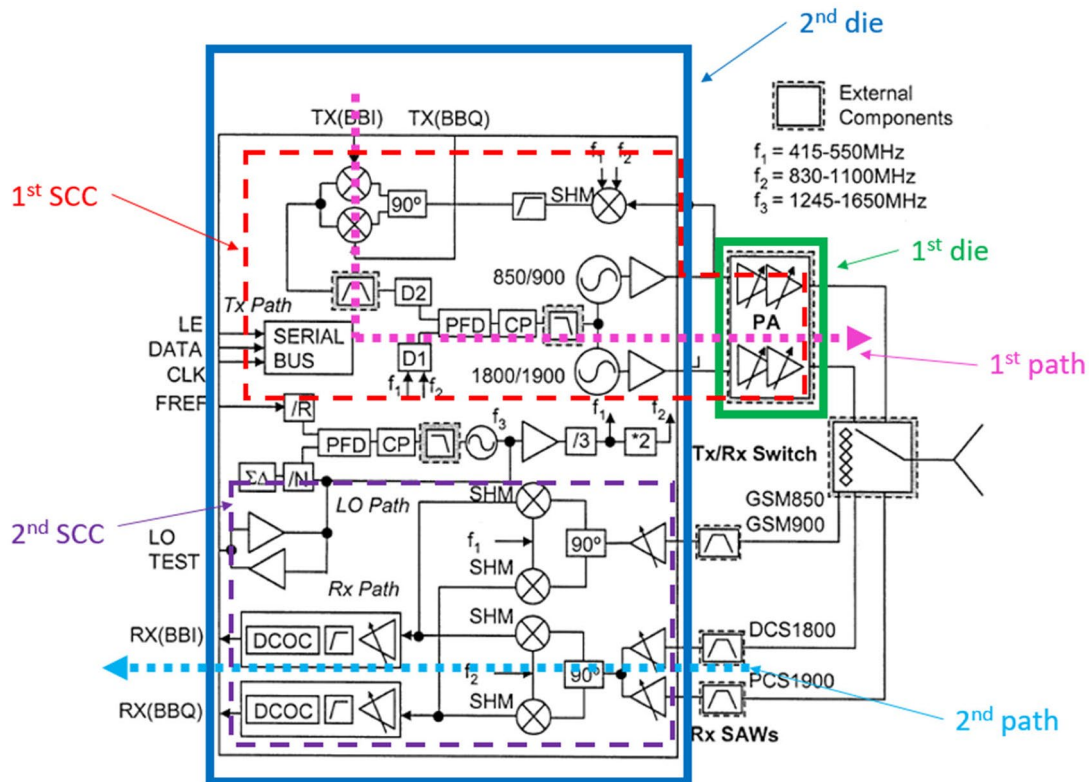


Fig. 1. Top-level schematic of transceiver, with external RF components.

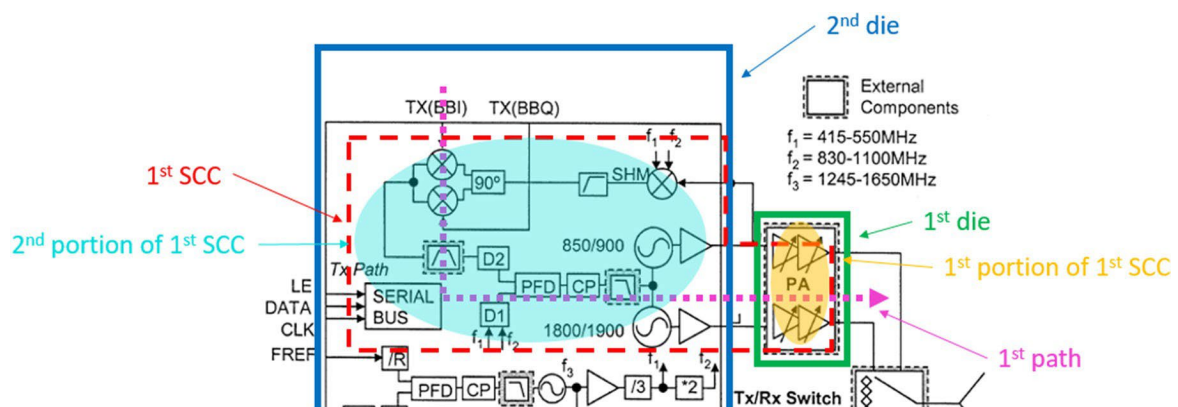
EX-1006, Fig. 1 (annotated). *Magoon* does not expressly disclose that the PA circuitry in Fig. 1 includes at least one *integrated circuit semiconductor die*.

135. *Ngompe* discloses an SPR module having a BiCMOS transceiver die that includes a transmitter section “to drive the GaAs HBT PA” (*an integrated circuit semiconductor die*). EX-1007, p.388 (Section III), p.387 (Fig. 1). A POSITA would be motivated to implement *Magoon*’s PA circuitry on a semiconductor die, as taught by *Ngompe*, to reduce module size, increase performance, and reduce time to market. Doing so would be nothing more than applying conventional processes in widely known manners. Moreover, as discussed in the State of the Art, *supra*, a POSITA understood that it was

common to implement PA circuitry on a GaAs semiconductor die to partition the system into its subsystems, each realized in the most suitable technology, to provide the known benefit of optimal performance, lower cost, and increased manufacturing yield. EX-1008, ¶¶5, 25; EX-1009, Figs. 4, 5, Sections 3, 4; EX-1011, p.1037.

[1.2] a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path; and

136. Magoon discloses a **Tx Path** (first signal path) made up of an “up-conversion transmit phase-locked loop (PLL) including on chip transmit voltage-controlled oscillators (VCOs)” (second portion of first SCC) to provide signals to **power amplifier (PA) circuitry** (first portion of first SCC). EX-1006, p.1710, Fig. 1.



EX-1006, Fig. 1 (annotated). A POSITA understood that the functions performed by the transmit PLLs/VCOs (frequency conversion) and PA circuitry (amplification) condition the transmit signal as it propagates along the Tx path.

These functions are “signal conditioning” because the signals are processed / altered (i.e., frequency converted and amplified) by the various stages of the transmit path circuitry to prepare the signals for the next stage in the transmit path. *Magoon* therefore discloses that the transmit PLLs/VCOs and PA circuitry together form a *first signal conditioning circuit* (“SCC”) disposed along a *first signal path*, and the PA circuitry is a *first portion of the first SCC*.

[1.3] a second integrated circuit semiconductor die comprising;

137. *Magoon* discloses a “**BiCMOS chip**” (*second integrated circuit semiconductor die*). EX-1006, p.1710 (Abstract).

[1.4] a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first portion of a first signal conditioning circuit for a signal propagating along the first signal path; and,

138. *Magoon* discloses **transmit PLLs/VCOs** (*second portion*) disposed along a **TX path** (*first signal path*) on the **BiCMOS chip** (*second die*). EX-1006, pp.1710, 1717 (Section V), Fig. 1. For the reasons explained above for [1.2], a POSITA understood the transmit PLLs/VCOs to perform signal conditioning functions along with the PA circuitry (*first portion*) on signals propagating along the TX path (*first signal path*).

[1.5] a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.

139. *Magoon* in view of *Ngompe* discloses this limitation.

140. *Magoon* discloses that a benefit of its complete LO integration is “that the only RF signals present on pins or bond wires are the received inputs at the LNAs and the transmitted outputs to the PA.” EX-1006, p.1710 (Section II). The inputs to the LNAs and the outputs to the PA described by *Magoon* are *for providing electrical connection to and from the BiCMOS transceiver die (second integrated circuit semiconductor die) and the PA circuitry (first integrated circuit semiconductor die)*. EX-1006, Fig. 20 (showing bond wires on transceiver chip). *Ngompe* discloses an SPR module including a “BiCMOS transceiver die” (*second integrated circuit die*) and a “GaAs HBT power amplifier” (*first integrated circuit die*) that are supported on a “lamineate substrate.” The “assembly consists of a combination of chip-on-board with wire bonding” to provide for electrical interconnection between the transceiver die and the PA die. EX-1007, p.387 (Abstract, Section II, Fig. 1), p.388 (Section II). As explained above, a POSITA would be motivated to combine *Ngompe*’s express packaging teachings with *Magoon*. See §VII.B.3, *supra*. Doing so would have been nothing more than the application of a known solution to

achieve a known and predictable result with a reasonable expectation of success.
EX-1008 ¶¶5, 35, 36; EX-1009 (Section 3); EX-1013, FIG. 7, 7:4-22; EX-1014,
1:1-28.

Claim 2

***[2.0] An electronic apparatus according to claim 1,
comprising a second signal conditioning circuit
comprising a first portion of the second signal
conditioning circuit and a second portion of the
second signal conditioning circuit integrated
within the second integrated circuit die for
performing a second signal conditioning function
on a signal propagating along a second signal
path that is different than the first signal path.***

141. Magoon discloses that the BiCMOS chip (second die) includes a
“receive path” / “Rx Path” (second signal path) that:

consists of three single-ended low-noise amplifiers (LNAs) that drive
two sets of quadrature subharmonic mixers (SHMs) whose outputs are
combined in a common I/Q analog baseband chain. The baseband
chains include low-pass channel select filtering, programmable gain,
and dc offset correction.

EX-1006, p.1710 (Section II); Fig. 1.

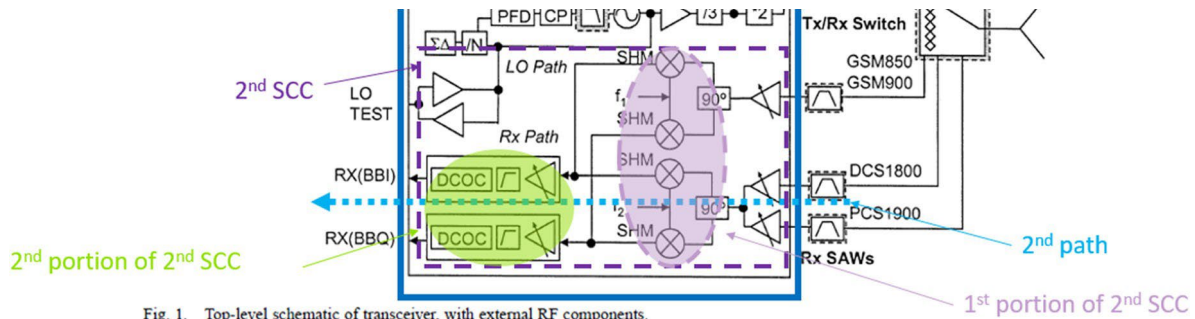


Fig. 1. Top-level schematic of transceiver, with external RF components.

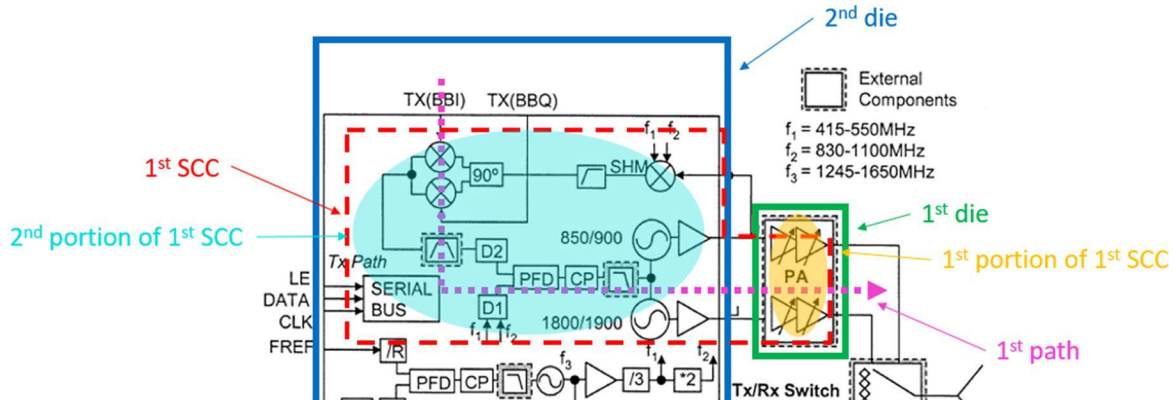
142. EX-1006, Fig. 1(annotated). A POSITA understood that functions performed by the circuitry along the Rx Path are “signal conditioning” because the signals are processed / altered (i.e., amplified, mixed, filtered, and corrected) by the various stages of the receive path circuitry to prepare the signals for the next stage in the receive path. *Magoon* therefore discloses that the receive path circuitry is a *second signal conditioning circuit* disposed along a *second signal path*, and the LNAs and SHMs are a *first portion* of the *second signal conditioning circuit*.

Claim 6

[6.0] An electronic apparatus according to claim 1, wherein the first portion of the first signal conditioning circuit comprises at least a power amplifier circuit and where the function of the first portion of the first signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit.

143. *Magoon* discloses that the **transmitter path circuitry** (*first SCC*) includes **PA circuitry** (*first portion*) having multi-stage PA circuitry (*power*

amplifier circuit) for amplifying the signals received from the on-chip transmit section (second portion). EX-1006, pp.1710-1711 (Section II).



EX-1006, Fig. 1(annotated). *Magoon's* disclosure of multi-stage PA circuitry in Fig. 1 is a disclosure of a power amplifier circuit that performs the function of *amplifying an input signal*.

Claim 10

[10.0] *An electronic apparatus according to claim 2, wherein the first semiconductor process does not facilitate manufacturing and integration of at least one of the second portion of the first signal conditioning circuit and the second portion of the second signal conditioning circuit.*

144. *Magoon* in view of *Ngompe* discloses this limitation.

145. *Magoon* discloses that the transceiver chip (*second die*), which includes a transmit section (*second portion of first SCC*) and the baseband chains of the receive path circuitry (*second portion of second SCC*), is made using a silicon-based BiCMOS process. EX-1006, Sections II, VII. However, *Magoon*

does not expressly disclose a particular semiconductor process for manufacturing the PA circuitry.

146. *Ngompe* discloses a BiCMOS transceiver chip and a GaAs HBT PA. EX-1007, p.387 (Fig. 1), p. 388 (Section III). *Ngompe* discloses: “Diverse die technologies are utilized to apply the optimum process for each function.” EX-1007, p.387 (Abstract, Fig. 1). A POSITA would have been motivated to use different semiconductor process technologies for *Magoon*’s transceiver chip and PA circuitry, respectively, as taught by *Ngompe* to optimize the manufacturing of each of the transceiver circuitry and PA circuitry and to enhance performance in a known and predictable manner. This teaching is consistent with the disclosure in the ’200 Patent that using the most suitable semiconductor technology is “an optimization task” to achieve known and predictable benefits. EX-1001, Abstract, 10:52-57.

Claim 11

[11.0] An electronic apparatus according to claim 1, wherein the second integrated circuit die is manufactured using a second semiconductor process that is different from that used to manufacture the first integrated circuit die.

147. *Magoon* view of *Ngompe* discloses this limitation for reasons discussed with respect to Claim 10.

Claim 12

[12.0] An electronic apparatus according to claim 1, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.

148. *Magoon* in view of *Ngompe* discloses this limitation for reasons discussed with respect to Claim 10. Specifically, *Ngompe* discloses a GaAs HBT PA. EX-1007, p.387 (Fig. 1), p. 388 (Section III).

Claim 13

[13.0] An electronic apparatus according to claim 12, wherein the second integrated circuit die is derived from a second semiconductor wafer comprised of other one of Si, SiGe, GaAs, InP, and GaN.

149. *Magoon* in view of *Ngompe* discloses this limitation for reasons discussed with respect to Claim 10.

Claim 14

[14.0] An electronic apparatus according to claim 1, wherein the first integrated circuit die is manufactured using a BiCMOS process.

150. *Magoon* does not expressly disclose a semiconductor process for manufacturing the PAs (*first die*).

151. As discussed in the State of the Art, *supra*, the use of a BiCMOS process to manufacture PAs was known in the RF industry. For example, the '200 Patent discloses that "[r]ecent advances in SiGe BiCMOS technology have

allowed for progressively higher levels of integration of high-performance RF components,” including PAs. EX-1001, 1:56-63. A POSITA would be motivated to manufacture *Magoon’s* PA circuitry using the semiconductor process best suited for the functionality of the PA, and BiCMOS would have been a known design choice to achieve a predictable result. Further, a POSITA understood that separating the components between first and second dies made using a BiCMOS process avoids interference that could occur if the components were on a single BiCMOS die.

Claim 15

[15.0] An electronic apparatus according to claim 1, wherein the second portion of the first signal conditioning circuit comprises at least one of a capacitor and an inductors and a signal transmission line.

152. Magoon discloses transmit section (*second portion of first SCC*) on the BiCMOS chip includes PLLs and VCOs. Capacitors and inductors are basic elements of PLL and VCO circuits and, conventionally, are integrated in the die with the other components of the PLL and VCO circuits. EX-1006, p.1719 (Section VII) (“The inductors were implemented in a 3-um-thick third metal layer. MIM capacitors between the second and third metal layers...”).

Claim 18

[18.0]. A method of manufacturing a module comprising:

153. To the extent the preamble is limiting, *Magoon* discloses this limitation for the reasons discussed with respect to Claim 1.

[18.1] providing a first signal conditioning circuit comprising a first portion and a second portion;

154. *Magoon* discloses this limitation for reasons discussed with respect to limitations [1.2] and [1.4].

[18.2] providing a second signal conditioning circuit comprising a first portion and a second portion;

155. *Magoon* discloses this limitation for reasons discussed with respect to Claim 2.

[18.3] implementing the first portion of the first signal conditioning circuit within a first semiconductor die;

156. *Magoon* discloses this limitation for reasons discussed with respect to limitations [1.1] and [1.2].

[18.4] implementing the second portion of the first signal conditioning circuit within a second semiconductor die;

157. *Magoon* discloses this limitation for reasons discussed with respect to limitations [1.3] and [1.4].

[18.5] implementing the first and second portions of the second signal conditioning circuit in the second semiconductor die;

158. *Magoon* discloses this limitation for reasons discussed with respect to Claim 2.

[18.6] bonding the first and second dies to a common substrate; and,

159. *Magoon* in view of *Ngompe* discloses this limitation for reasons discussed with respect to limitation [1.5]. Further, as discussed in the State of the Art, *supra*, manufacturing a multiple-die module by bonding dies to a common substrate was a well-known, conventional practice. EX-1008, ¶5; EX-1014, 1:1-28; EX-1013, FIG. 7, 7:4-22.

[18.7] forming electrical connections between the two dies to complete the first signal conditioning circuit from the first portion of the first signal conditioning circuit and the second portion of the first signal conditioning circuit.

160. *Magoon* discloses this limitation for reasons discussed with respect to limitation [1.5].

Claim 19

[19.0] A method according to claim 18, wherein the first semiconductor die comprises a first portion of a first signal path and the second semiconductor die comprises a second portion of the first signal path, the first signal path disposed between a first input port and a first output port.

161. *Magoon* discloses this limitation for reasons discussed with respect to Claim 1.

Claim 20

[20.0] A method according to claim 19, wherein the second semiconductor die comprises a second signal path that is other than the second portion

of the first signal path and in approximate RF isolation therefrom.

162. *Magoon* discloses that the BiCMOS chip (*second die*) is laid out to reduce “the risk of unwanted coupling of signals between circuits.” EX-1006, p.1718 (Section VI.B). *Magoon* explains that the transmit VCOs on the Tx path (*second portion of first path*) and the LNAs on the Rx path (*second path*) are situated in the extreme corners of the die, as shown in the microphotograph below:

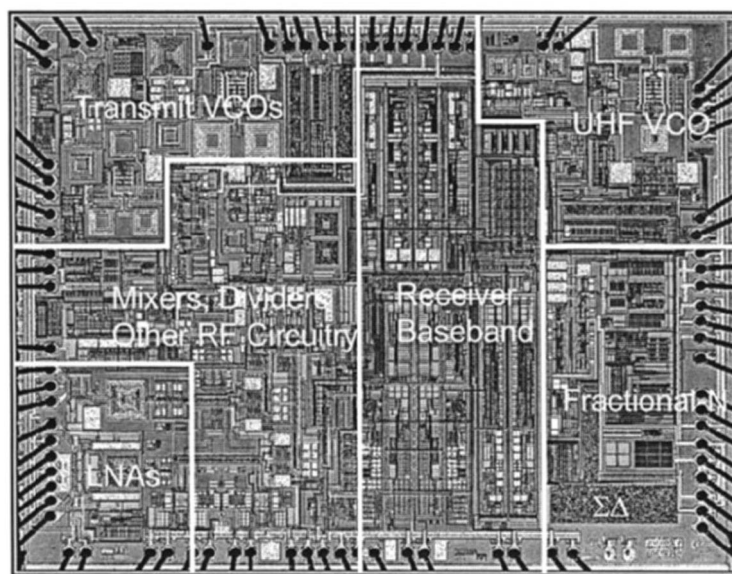


Fig. 20. Microphotograph of transceiver.

EX-1006, Fig. 20.

163. By stating that the chip layout reduces unwanted coupling between the Tx path and the Rx path, *Magoon* is disclosing that the paths are in *approximate RF isolation therefrom*.

Claim 23

[23.0] A method according to claim 18, wherein the first semiconductor die does not facilitate implementation of the second portion of the first signal conditioning circuit therein.

164. *Magoon* in view *Ngompe* discloses this limitation for the reasons discussed with respect to Claim 10.

Claim 24

[24.0] A method according to claim 18, wherein implementing of the second portion of the first signal conditioning circuit within the second semiconductor die provides increased performance in signal conditioning as compared to implementing of the second portion of the first signal conditioning circuit within the first semiconductor die.

165. *Magoon* in view *Ngompe* discloses this limitation.

166. *Ngompe* discloses an SPR module having a BiCMOS chip (*second die*) and a GaAs PA (*first die*) where “[d]iverse die technologies are utilized to apply the optimum process for each function.” EX-1007, p.387 (Abstract). A POSITA would be motivated to apply *Ngompe*’s express teachings to *Magoon*’s RF transceiver to increase performance in signal conditioning. Doing so would amount to applying known processes to a known apparatus to achieve a predictable result.

Claim 25

[25.0] A method according to claim 18, wherein prior to implementing the first signal conditioning circuit comprises partitioning of the first signal conditioning circuit into the first portion and the second portion.

167. *Magoon* in view of *Ngompe* discloses this limitation for the same reason as discussed with respect to Claim 1.

Claim 26

[26.0] An electronic apparatus comprising:

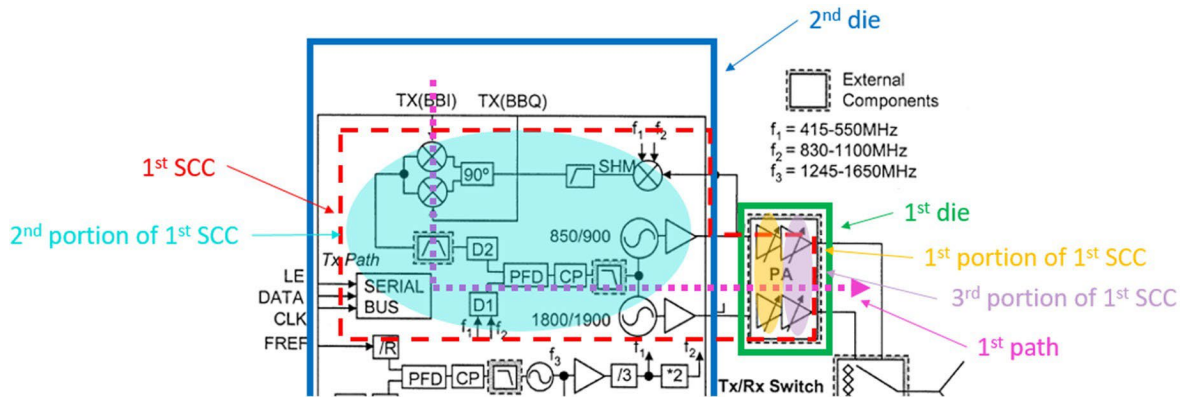
168. *Magoon* discloses this limitation for reasons discussed with respect to limitation [1.0].

[26.1] a first integrated circuit semiconductor die comprising:

169. *Magoon* in view of *Ngompe* discloses this limitation for reasons discussed with respect to limitation [1.1].

[26.2] a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path;

170. *Magoon* in view of *Ngompe* discloses a quadband PA module that includes a 850/900 MHz PA branch and a 1800/1900 PA branch:



EX-1006, Fig. 1 (annotated). A POSITA reading *Magoon* understood that each branch includes multistage power amplifiers (as shown schematically in Fig. 1) and, thus, that each branch includes a **first portion** and a **third portion** of the **first SCC**. See also disclosures for [1.2] above.

[26.3] a third portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along the first signal path; and

171. *Magoon* in view of *Ngompe* discloses this limitation for reasons discussed with respect to limitation [26.2].

[26.4] a second integrated circuit semiconductor die comprising;

172. *Magoon* discloses this limitation for reasons discussed with respect to limitation [1.3].

[26.5] a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first and third portions of

the first signal conditioning circuit for a signal propagating along the first signal path; and,

173. *Magoon* in view of *Ngompe* discloses this limitation for reasons discussed with respect to limitations [1.4] and [26.3].

[26.6] a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.

174. *Magoon* in view of *Ngompe* discloses this limitation for reasons discussed with respect to limitation [1.5] above.

Claim 29

[29.0] An electronic apparatus according to claim 26, comprising a second signal conditioning circuit comprising a first portion of the second signal conditioning circuit and a second portion of the second signal conditioning circuit integrated within the second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path.

175. *Magoon* discloses this limitation for reasons discussed with respect to Claim 2.

Claim 30

[30.0] An electronic apparatus according to claim 26, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.

176. *Magoon* in view of *Ngompe* discloses this limitation for reasons discussed with respect to Claim 12.

Claim 31

[31.0] An electronic apparatus according to claim 30, wherein the second integrated circuit die is derived from a second semiconductor wafer comprised of other one of Si, SiGe, GaAs, InP, and GaN.

177. *Magoon* discloses this limitation for reasons discussed with respect to Claim 13.

CONCLUSION AND DECLARATION

The findings and opinions set forth in this declaration are based on my research and analysis to date. I may continue my examinations in view of additional documents or other factual evidence over the course of this proceeding that may necessitate supplementing and/or refining my opinions. I reserve the right to add to, alter, or delete my opinions and my Declaration upon discovery of additional information. I reserve the right to make such changes as necessary. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination. I declare that all statements made herein on my own knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

[SIGNATURE ON FOLLOWING PAGE]

Dated: 04/19/2025

By: 
Ayman Fayed, PhD

APPENDIX A – MATERIALS RELIED UPON

EX-1001	U.S. Patent No. 7,409,200 to Derbyshire et al. (“200 Patent”), Filing Date of June 2, 2004
EX-1002	Prosecution History of U.S. Patent No. 7,409,200
EX-1003	Intentionally Left Blank
EX-1004	<i>Curriculum Vitae</i> of Dr. Ayman Fayed
EX-1005	U.S. Patent Publication No. 2003/0017809 A1 to Garlepp et al. (“ <i>Garlepp</i> ”), Filing Date of February 19, 2002 and Publication Date of January 23, 2003
EX-1006	R. Magoon et al., “A Single-Chip Quad-Band (850/900/1800/1900 MHz Direct Conversion GSM/GPRS RF Transceiver with Integrated VCOs and Fractional-N Synthesizer,” published in IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 37, No. 12, pp. 1710-1720, December 2002 (“ <i>Magoon</i> ”)
EX-1007	E. Ngompe et al., “Architecture and Performance Overview of a Highly Integrated 13x13mm Single-Package Radio (SPR) Module for Dualband EGSM900 / GSM1800 Applications,” published in 2003 IEEE Radio Frequency Integrated Circuits Symposium, pp. 387-390 (“ <i>Ngompe</i> ”)
EX-1008	U.S. Patent Publication No. 2003/0089998 A1 to Chan et al. (“ <i>Chan</i> ”), Filing Date of November 9, 2001, Publication Date of May 15, 2003
EX-1009	P. Wambacq et al., “A single-package solution for wireless transceivers,” published in Design, Automation and Test in Europe Conference and Exhibition, 1999 (“ <i>Wambacq</i> ”)
EX-1010	L.E. Larson, “Integrated Circuit Technology Options for RFIC’s—Present Status and Future Directions,” published in IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 33, No. 3, pp. 387-399, March 1998 (“ <i>Larson</i> ”)
EX-1011	J. Ryckaert et al., “Single-package 5GHz WLAN RF module with embedded patch antenna and 20dBm power amplifier,” published in 2003 MTT-S Digest, pp. 1037-1040 (“ <i>Ryckaert</i> ”)

EX-1012	U.S. Patent Publication No. 2003/0139147 A1 to Shi (“ <i>Shi</i> ”), Filing Date of March 21, 2002, and Publication Date of July 24, 2003.
EX-1013	U.S. Patent No. 5,898,909 to Yoshihara et al (“ <i>Yoshihara</i> ”), Filing Date of September 27, 1996, Issue Date of April 27, 1999
EX-1014	European Patent Application Publication No. EP 0 632 497 A2 to Pedder (“ <i>Pedder</i> ”), Filing Date of June 16, 1994, Publication Date of January 4, 1995
EX-1015	U.S. Patent No. 6,297,694 to Yamamoto (“ <i>Yamamoto</i> ”), Filing Date of November 24, 1999, Issue Date of October 2, 2001
EX-1016	WILEY ELECTRICAL AND ELECTRONICS ENGINEERING DICTIONARY (2004), p. 707 (signal conditioning)
EX-1017	Declaration of Ingrid Hsieh-Yee, Ph.D.