

A Single-Chip Quad-Band (850/900/1800/1900 MHz) Direct Conversion GSM/GPRS RF Transceiver with Integrated VCOs and Fractional- N Synthesizer

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Abstract—Recent trends in the integration of entire systems on-chip have spurred the development of homodyne radios as alternatives to the more mature yet harder to integrate super-heterodyne architectures. This paper presents a monolithic device that integrates all of the functions necessary to implement a multi-band homodyne global system for mobile telecommunications radio except for the power amplifier (PA) and radio frequency (RF) passives. The single BiCMOS chip includes a quad-band direct conversion receiver that down converts RF to quadrature analog baseband. The front-end circuitry is followed by a low-dc-offset, high-dynamic-range, analog I/Q baseband chain. The transmit section is comprised of a quad-band up-conversion transmit phase-locked loop (PLL) including on chip transmit voltage-controlled oscillators (VCOs). The stringent GSM receive band phase noise specifications are met without the use of surface acoustic wave filters. A single $\Sigma\Delta$ fractional- N synthesizer locking a fully integrated ultrahigh frequency VCO generates the system local oscillator signal.

Index Terms—BiCMOS, calibration, direct conversion, frequency dividers, $g_m C$ filters, GPRS, GSM, land mobile radio cellular systems, microwave circuits, modulation, noise, phase-locked loops, power amplifiers, quad band, receivers, system on chip (SOC), transceivers, transmitters, UHF, voltage-controlled oscillators.

I. INTRODUCTION

AS MODERN cell phones become ubiquitous, the critical factors in their manufacture become cost, size, and time to market. The high integration of radio ICs reduces board area and complexity while cutting component cost and system design time. Low-cost manufacturers desire freedom to choose the cheapest and most reliable IC for each main handset function. In this context, the interface between the transceiver and the various baseband ICs available on the market becomes important. Radio receiver outputs need to be able to interface to low-dynamic-range analog-to-digital converters (ADCs) through a simple I/Q interface and require little or no digital post processing. Direct conversion and low intermediate frequency (IF) receivers permit increased integration, lower cost, and reduce radio complexity by removing the need for external IF surface

acoustic wave (SAW) filters and multiple local oscillator (LO) signals. However, many direct conversion receiver (DCR) implementations [1] and all low IF receivers still require wide dynamic range ADCs.

This work presents a DCR that avoids the traditional problems by means of frequency planning, floor planning, and calibration techniques. The receiver includes a low-dc-offset, high-input-dynamic-range analog I/Q baseband chain capable of interfacing to 9-b ADCs. The transmitter architecture is based on the commonly used translational loop. A single integrated LO provides the channel selection for both the transmitter and the receiver. All VCOs and phase-locked loops (PLLs) are on chip [2].

II. DEVICE OVERVIEW

A block diagram of the transceiver, including the necessary external RF components, is shown in Fig. 1. The only required external components, excluding impedance matching and loop filter components, are receive band select SAW filters, a switch-plexer, and a power amplifier (PA). Standard differential analog I/Q interfaces are used for the transmitter inputs and for the receiver outputs.

The receive path consists of three single-ended low-noise amplifiers (LNAs) that drive two sets of quadrature subharmonic mixers (SHMs) whose outputs are combined in a common I/Q analog baseband chain. The baseband chains include low-pass channel select filtering, programmable gain, and dc offset correction. A fully integrated translational loop transmitter locks two wide-band on-chip oscillators (one for 1800/1900 MHz, and the other for 850/900 MHz). The loop also includes a down-conversion feedback mixer and a quadrature modulator, along with a phase frequency detector and charge pump. Frequency synthesis is completely integrated including a UHF oscillator and fractional- N PLL. Several stages of LO processing are required to ease the design of the UHF oscillator and to provide quad-band functionality. One of the benefits of complete LO integration is that the only RF signals present on pins or bond wires are the received inputs at the LNAs and the transmitted outputs to the PA.

The transceiver incorporates a three-wire serial interface programming bus providing frequency control, gain control, and broad testability of integrated blocks. A test port is provided for

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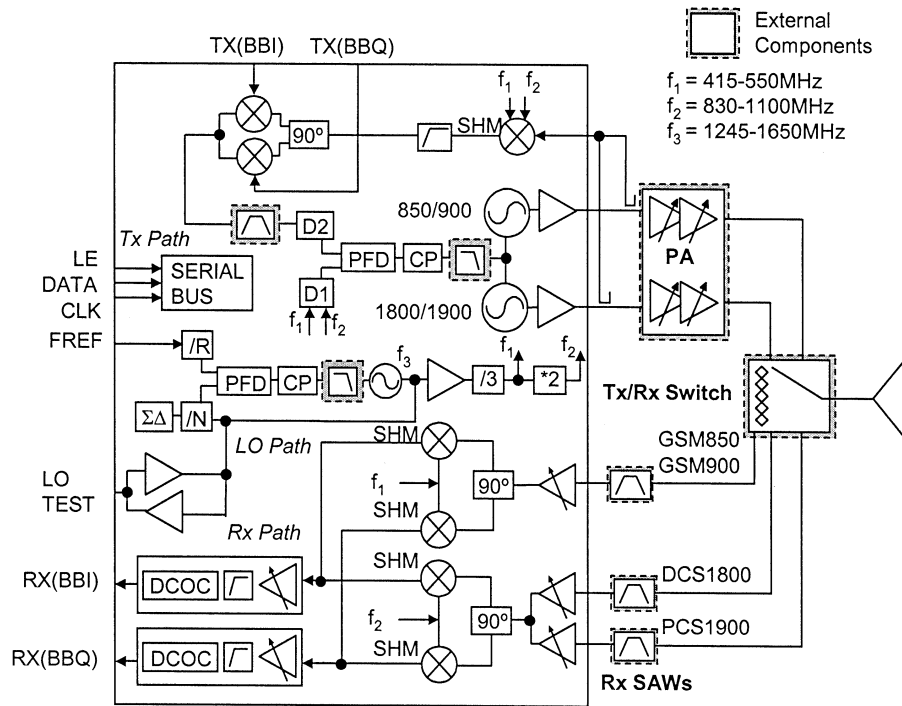


Fig. 1. Top-level schematic of transceiver, with external RF components.

monitoring the LO during testing and is disabled during normal operation. Separate transmit, receive, and synthesizer control input pins permit enabling from the digital baseband.

III. DCR

The direct conversion approach presents several unique design challenges. All of these have to do with the generation of excessive or time-varying dc offsets at the outputs of the receiver. Aside from simple process and layout related mismatches, the two primary sources of dc are LO leakage to the RF inputs and even-order nonlinearities in the receive path. While constant dc offsets can be calibrated out, mechanisms that result in unpredictable time-varying dc offsets must be suppressed by a careful choice of architecture and circuit design.

1) *DC Offsets*: DC offsets can corrupt data in systems such as global system for mobile telecommunications (GSM), where information is present down to dc. It is possible to subtract offsets in the DSP, provided they are constant over a given receive slot. Large dc offsets may overload the ADC or some portion of the analog baseband, causing the received signal to clip, corrupting information before correction in the DSP is possible. Signal independent dc can be generated in several ways. One way is through mismatches in the mixer and baseband. Offsets from mismatches can pose a problem since most of the receiver's gain appears after the mixer, and so even small offsets, once gained up, can overwhelm the receiver. Fortunately, fixed dc offsets may be corrected by activating the mixer and baseband early and performing a closed-loop calibration.

A second source of dc offsets comes from the LO signal coupling onto the receive chain at some point before the mixer. This signal, once present, is down converted to dc. As shown

in Fig. 2(a), the LO signal may couple to the output and or the input of the LNA or reradiate and reflect off an external surface and be picked up by the antenna. In the first case, simple dc offset calibration may be used. In the second case, calibration is also possible but may be inaccurate if interfering signals are present on the antenna. The third case, however, represents an unpredictable situation leading to a time-varying dc signal. LO re radiation must thus be minimized by design.

2) *IIP2*: Another way that dc can be generated is through second-order nonlinearity in the signal path. These nonlinearities cause strong out of band signals to be converted to dc, as in

$$F(x) = a_1 \cdot x + a_2 \cdot x^2$$

$$F(A \cdot \cos(\omega t)) = a_1 \cdot A \cdot \cos(\omega t) + \frac{1}{2} \cdot a_2 \cdot A^2 [1 + \cos(2 \cdot \omega t)] \quad (1)$$

and are collectively characterized by the second-order intercept point, IIP2 of the receiver. See Fig. 3. IIP2 effects can be caused by two distinct mechanisms. One mechanism involves simple even-order nonlinearities in the mixer or baseband. This phenomenon is characteristic of single-ended circuits and is even possible in differential circuits if asymmetries are present. The other mechanism involves large RF blocking signals coupling onto the LO chain and phase modulating the LO signal. See Figs. 2(b) and 4. Since one of the resulting side bands corresponds to the original RF signal, the RF is down converted to dc as shown in

$$LO' = LO + k \cdot RF_{\text{blocker}}$$

$$= \cos(\omega_{LO} \cdot t) + k \cdot \cos(\omega_{RF} \cdot t)$$

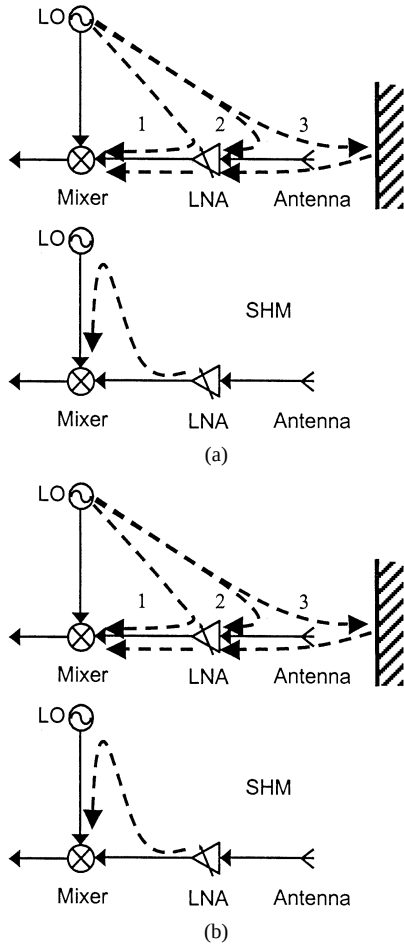


Fig. 2. Coupling paths that can cause dc offsets. (a) LO to RF coupling. (b) RF to LO coupling.

$$RF \cdot LO' = \frac{1}{2} [A \cdot \cos((\omega_{RF} \pm \omega_{LO}) \cdot t)] + k \cdot A^2 [1 + \cos(2 \cdot \omega_{RF} t)]. \quad (2)$$

IIP2 performance is especially important in cases where blocker strength varies unpredictably in the middle of a receive slot. In these cases, dc offset calibration is impossible and DSP algorithms are less effective. It is this situation, specified for GSM by the AM suppression test [3], which sets the lower bound on IIP2 in a GSM DCR. For example, in the EGSM band, the radio must be able to reliably continue receiving a signal at -99 dBm when a -31 -dBm signal at 6-MHz offset unexpectedly turns on mid slot. The required IIP2 can be calculated as

$$\begin{aligned} IIP2_{req}(\text{dBm}) &= 2 \cdot P_{blocker}(\text{dBm}) \\ &\quad - (P_{signal} - SNR_{req} + 3 \text{ dB}) \\ IIP2_{req} &= 2 \cdot (-31 \text{ dBm}) \\ &\quad - (-99 \text{ dBm} - 9 \text{ dB} + 3 \text{ dB}) \\ &= +43 \text{ dBm (at the antenna)} \\ IIP2_{req} &= +40 \text{ dBm (at the LNA input, assuming} \\ &\quad 3 \text{ dB front end loss).} \end{aligned} \quad (3)$$

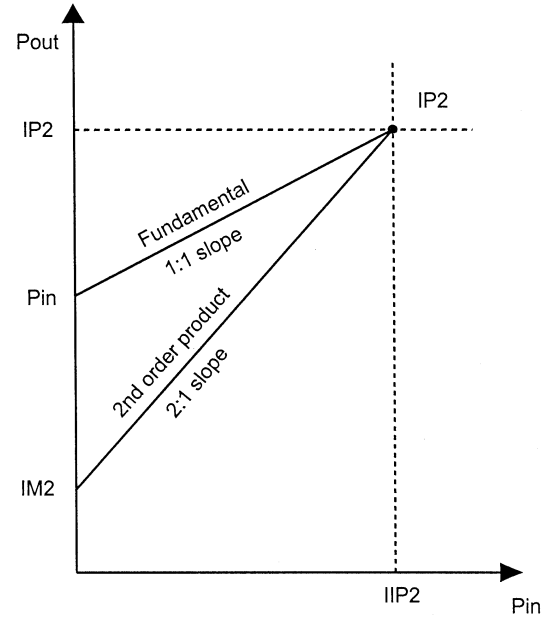


Fig. 3. Second-order intercept diagram. Both axes are in dBm.

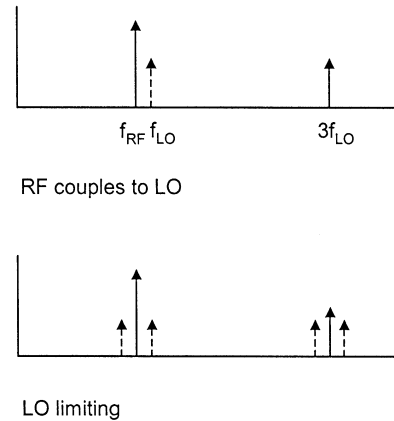


Fig. 4. Modulation of LO by RF.

A. Ratioed LO Frequency Plan

LO and RF self mixing can both be reduced using offset frequency architectures [4]. One method for generating offset LO signals is through a combination of frequency dividers and multipliers. In such a system, subharmonic LO signals should be of even order relative to the received signal. This requirement arises from the common use of differential hard switched circuits in dividers, LO buffers, and mixers. Hard switched differential circuits tend to generate odd harmonics of the switching frequency and also respond to interfering signals close to their odd harmonics, as if they were sidebands of the fundamental.

In the LO chain presented here and shown in Fig. 1, a single LO provides a signal in the range from 1250 to 1650 MHz. This signal is fed to a frequency divide-by-three circuit, which generates a subharmonic LO signal in the range 415 to 550 MHz. This signal is then passed directly to a 1/2 LO SHM to down convert received signals in the 850-MHz US cellular and 900-MHz EGSM bands. Alternately, for high band operation, the signal is passed to a frequency doubler generating an LO signal from 830

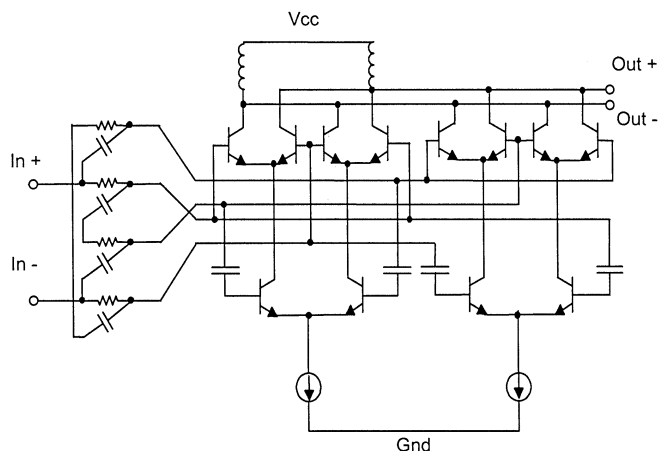


Fig. 5. Low-output harmonic doubler.

MHz to 1.1 GHz. This LO signal is then fed to a 1/2 LO SHM to down convert signals in the 1800-MHz DCS and 1900-MHz PCS bands.

1) *Frequency Doubling and 1/2 LO Mixers*: The use of a subharmonic LO signal clearly reduces LO reradiation and self mixing. Since the reradiated LO signal will be present at 1/2 or 1/4 the received frequency, it will not be down converted to baseband. In addition, RF coupling onto a subharmonic LO will not modulate the LO signal in a fashion that can degrade IIP2.

The implementation of the frequency doubling function is critical. Typically, frequency doubling in both SHM [9] and frequency doublers is implemented by multiplying two signals of the same frequency that are phase split by 90 degrees, as represented by

$$\sin(\omega t) \cdot \cos(\omega t) = \frac{1}{2} \cdot \sin(2\omega t). \quad (4)$$

An efficient doubling circuit makes use of hard switched phase split signals instead of sinusoidal signals. The circuit shown in Fig. 5 accomplishes frequency doubling as follows. An RC polyphase filter provides the quadrature phase split. The resulting signal then drives a pair of hard switched Gilbert multipliers [6]. The use of two such multipliers, whose outputs are summed and whose inputs are cross coupled, provides higher order symmetry [7]. This symmetry guarantees low-output even-order harmonics (provided that the phase split is accurate).

Since (4) essentially represents the up conversion of one signal by the other, it should be clear that the sidebands of either signal will be up converted with their frequency offsets intact, as shown in Fig. 6. In other words, RF signals coupling onto a subharmonic LO will generate sidebands at offsets equal to the frequency difference between the subharmonic LO signal and RF signal. Even after the fundamental frequency is doubled in the frequency doubler or SHM, this offset is maintained resulting in sidebands at, for example, $F_{RF} \pm F_{LO}$, where $F_{LO} \sim 1/2 F_{RF}$. Such sidebands will not align with the original received signal, and will not result in IIP2 degradation.

2) *Divide by Three*: Although subharmonics do not reradiate at the RF frequency, they can generate harmonics that do. The VCO generating the LO signal includes relatively large structures in its resonant tank and operates at relatively high

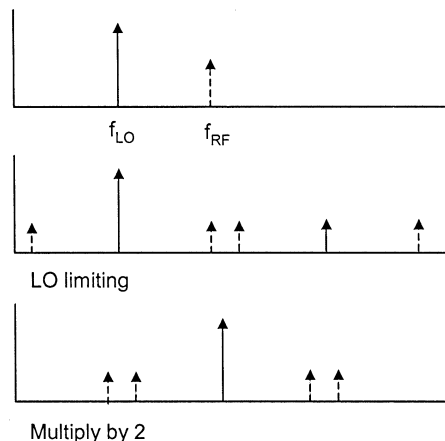


Fig. 6. Modulation of 1/2 LO by RF.

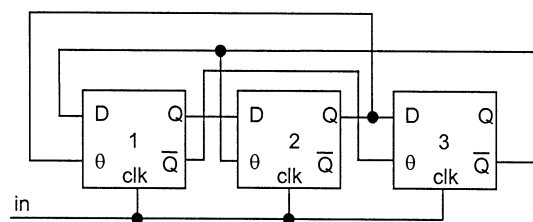


Fig. 7. Architecture of frequency divide-by-three with 50% duty cycle.

power. To avoid problems with VCO-generated harmonics, the oscillator runs at three times the subharmonic frequency and is followed by a lower power divide-by-three circuit. The analysis of the interaction between even-order subharmonic signals and received signals also applies to odd multiples of even-order subharmonics. LO signals at 3/2 and 3/4 the receive frequency are as insensitive to coupling as those at 1/2 and 1/4. As an additional benefit, VCOs can more easily be integrated in the 1.5-GHz range than in the 0.5-GHz range as discussed later in this paper.

Two problems arise from the implementation of a frequency divide-by-three. The first results from the fact that most odd-order frequency dividers generate outputs with non 50% duty cycles. This results in generation of strong even-order harmonics, obviating the use of an even-order subharmonic LO. The second problem is more subtle. As mentioned before, doubling of frequencies typically involves quadrature split inputs. If polyphase filters are used to generate quadrature, the input signals are required to be sinusoidal. Therefore, the reduction of higher harmonics at the output of the frequency divide-by-three is very important [8].

A true 50% duty cycle frequency divide-by-three was implemented using three phase-switchable level-sensitive latches connected in a loop. Each latch, in addition to its data and clock inputs, has a third input which is denoted by θ . This input toggles the latch between triggering on the positive and negative levels of the clock. Proper interconnection of Q , D , and θ between latches (shown in Fig. 7) results in a signal of 1/3 the clock frequency propagating through the loop by one latch each 1/2 clock cycle. The resulting waveforms are shown in Fig. 8(a). Implementation of such latches in differential emitter coupled logic (ECL) permits the necessary signal inversions without asymmetry.

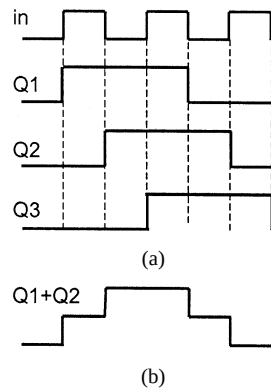


Fig. 8. (a) Internal states of divide-by-three. (b) Output generated by summing two internal states.

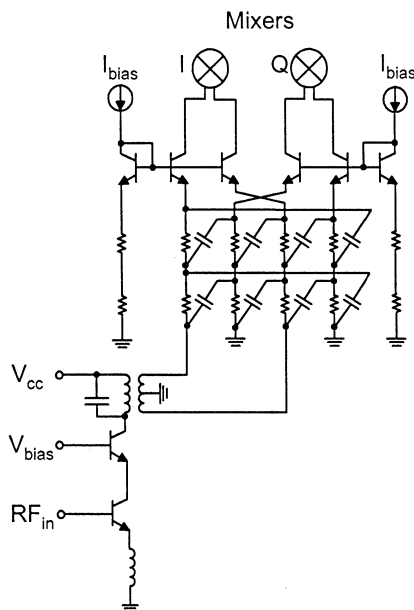


Fig. 9. LNA, RF path phase split, and mixer RF port.

In order to suppress the strong third harmonic present in the square wave outputs of this divider, one additional step is needed. Each of the three latches has as its output a signal 60° delayed from the previous stage. Summation of two such signals results in an output with a fundamental 30° shifted from the first, with slightly less than twice the amplitude. The third harmonics of the summed signals, however, are 180° split and as a result they completely cancel. The resulting much more sinusoidal signal is shown in Fig. 8(b).

3) *RF Path Quadrature Generation*: Simple 90° phase splitting of the subharmonic LO is insufficient to generate I/Q receiver outputs because upon frequency doubling; the phase also doubles to 180° . The use of 45° splits has also been explored [9]; however, most schemes are either very lossy or lose accuracy over process variations. As an alternative, quadrature may be generated in the RF path. An RF path phase splitter is shown in Fig. 9. A two-stage polyphase filter guarantees amplitude matching across band and process. By incorporating this structure as degeneration for the replica biasing of the common base

TABLE I
RECEIVER PERFORMANCE. SENSITIVITY NUMBERS INCLUDE LOSSES FROM FRONT-END FILTERS AND SWITCHPLEXER

Receiver	850/900MHz	1800MHz	1900MHz
NF	3.1dB	3.6dB	4.1dB
LO re-radiation	-110dBm	-105dBm	-103dBm
IQ phase match	1°	1°	1°
IQ amplitude match	0.5dB	0.5dB	0.5dB
Gain range	10-105dB	10-100dB	10-100dB
Typical sensitivity	-109dBm	-107dBm	-107dBm
Required sensitivity [3]	-102dBm	-100dBm	-102dBm
IIP2 over channels (cal.)	> 50dBm	> 50dBm	> 50dBm
3dB baseband BW	98kHz	98kHz	98kHz
Group delay to 100kHz	< 0.3 μ s	< 0.3 μ s	< 0.3 μ s
Rejection at 3MHz	> 120dB	> 120dB	> 120dB
Sensitivity with blocker	-105.5dBm	-104dBm	-104dBm
Req'd sens. with blocker [3]	-99dBm	-97dBm	-97dBm
Bias current (incl. Synth.)	75mA	80mA	80mA
Operating voltage	2.7-3.6V	2.7-3.6V	2.7-3.6V

RF port of the mixer, one can implement the phase split without any extra voltage headroom. The use of a common base RF port provides significant isolation between the mixer core and LNA, attenuating any LO signal that might couple back to the LNA and potentially self mix.

4) *Results*: Reradiation of on-frequency LO signal measured at the LNA input is -110 dBm in GSM, -105 dBm in DCS, and -103 dBm in PCS. In addition, the subharmonic LO chain exhibits good phase noise as evidenced by the fact that the worst case blockers desensitize the receiver by less than 4 dB. The RF path phase split is effective in generating quadrature accurate to 1° and 0.5 dB measured at the baseband outputs. The NF measured for the whole receiver is 3.1 dB in GSM, 3.6 dB in DCS, and 4.1 dB in PCS. See Table I. As compared to traditional superheterodyne receivers, power is saved by replacing the IF strip with baseband amplifiers and filters and by removing one local oscillator. Unfortunately, these power benefits tend to be balanced out by the greater complexity and integration of the LO chain. The receiver (including PLL and oscillator) consumes 75 and 80 mA from 2.7 V in GSM and DCS modes, respectively.

B. IIP2 Cancellation

Although the frequency plan described above is effective in suppressing RF self mixing, simple second-order nonlinearity still limits IIP2. IIP2 in a purely differential structure (such as a double balanced mixer) is theoretically infinite. All IIP2 effects must therefore be a consequence of asymmetry. Although most asymmetries can be reduced by careful layout and design, imperfections will always be present due to device mismatch. In order to compensate for this problem, an IIP2 cancellation scheme was developed. This scheme essentially introduces an intentional (digitally programmable) asymmetry into the mixer in order to null blocker induced dc offsets, thereby canceling IIP2. This calibration provides a 15-dB improvement in receiver IIP2 across the band, raising it from better than 35 dBm to better than 50 dBm for all bands. Fig. 10 shows the effect on dc of a blocker at a 6-MHz offset ramping from -30 to -24 dBm in the presence of a -99 -dBm wanted signal.

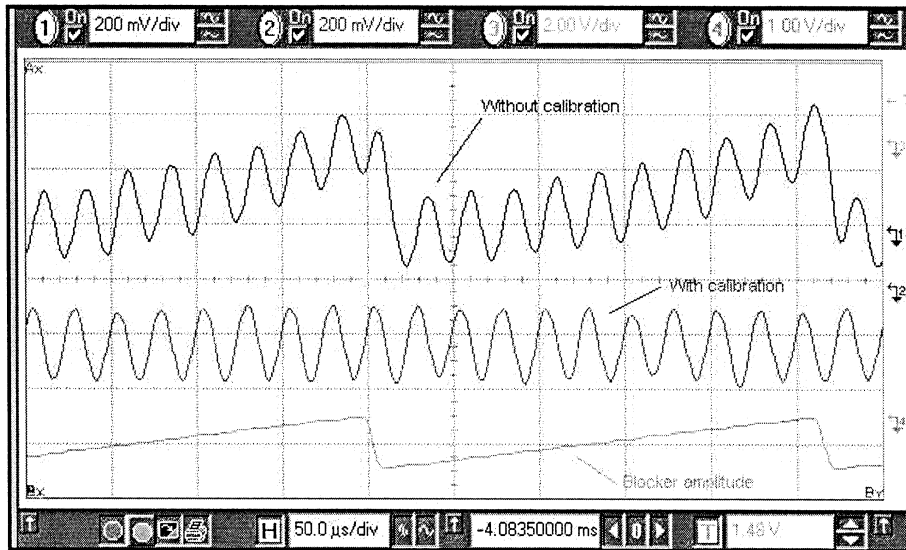


Fig. 10. Effects of AM modulated blocker (bottom curve) on received signal with and without IIP2 calibration.

C. Baseband Circuitry

One of the benefits of the DCR is the migration of all the functions usually present in the IF strip to baseband. In principle, any function performed at an IF of several hundred megahertz is easier to implement at several hundred kilohertz with less power consumption and higher integration. However, the standard challenges associated with high dynamic range are then complicated by a new set of problems including dc offsets, flicker noise, and even-order nonlinearities [10].

Without the benefit of a high Q channel select filter and wide range IF PGA, the baseband is forced to deal with the full range of blocker and signal strengths present at the mixer output. In addition, the baseband must be able to handle the entire possible range of signal and blocker strengths without significantly degrading the noise performance of the receiver or compressing the wanted signal. A GSM receiver with an NF of 3 dB and a 1-dB compression point of -22 dBm requires a dynamic range of approximately 95 dB. To avoid undesired degradation, this translates to a dynamic range of more than 105 dB in the baseband.

In this design, the distribution of gain and filtering is designed to attenuate far out blockers early in the chain to ease headroom requirements for later stages (see Figs. 11 and 12). The current mode output of the mixer is directly coupled to a folded cascode stage implementing two real poles set by resistor and capacitor combinations with 40 dB of effective gain. This stage is followed by a Sallen Key filter, which implements two complex conjugate poles and 10 dB of gain. Such RC-based filters and amplifiers have very high dynamic range, but must be wide band enough to avoid inband interference from process variations. Once the far out blockers (1.6 MHz, 3 MHz, and beyond) are attenuated, the dynamic range requirements of the following stages are relaxed. Lower dynamic range permits the use of low power and tightly controlled $g_m C$ filters to remove the closer blockers (200 kHz, 400 kHz, and 600 kHz). A continuous time filter [11] was used instead of a switched capacitor filter [12] due to concerns that the reference clock would couple to the on

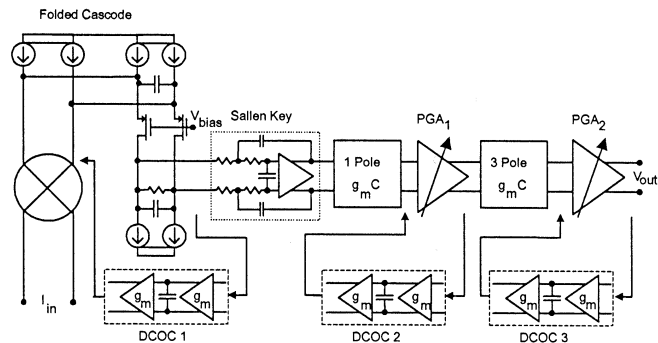


Fig. 11. Mixer output and baseband chain.

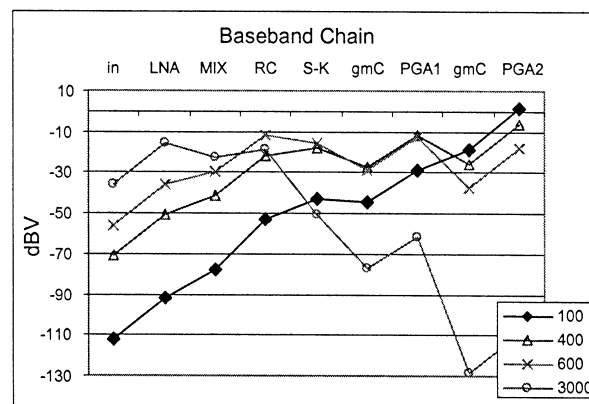


Fig. 12. Baseband chain level diagram.

chip LNA and VCOs. Gain stages are interleaved with the filters to increase wanted signal strength and to ease noise restrictions. In order to avoid compression at higher desired signal levels, the gain is made programmable. See Fig. 13.

Since dc offsets caused by mismatch can completely compress the output of the baseband at high gain, the stages were designed with low input referred dc offset. Every high gain stage

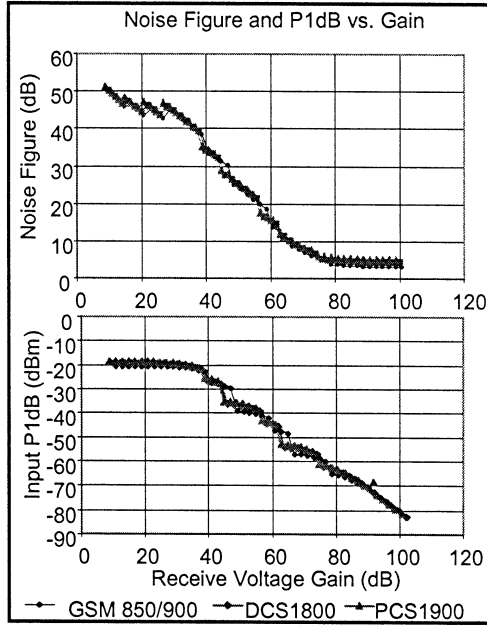


Fig. 13. In-band compression point and noise figure over gain.

is accompanied by a dc offset loop set to calibrate out its residual dc.

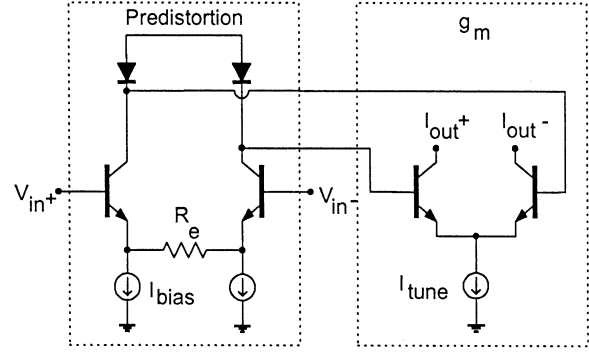
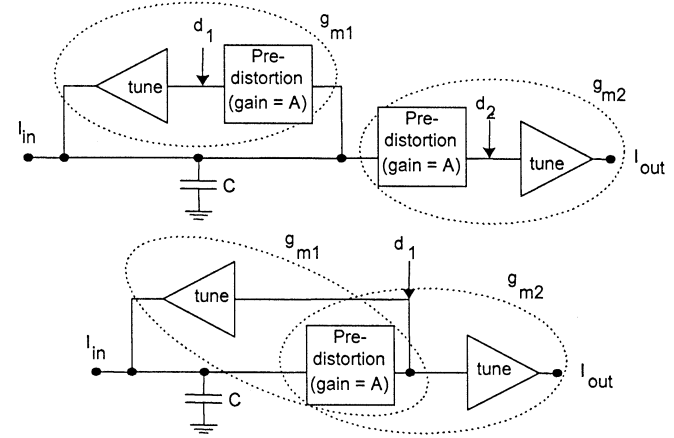
1) *Folded Cascode Mixer Output*: To ease headroom requirements at the output of the mixer core, a PFET folded cascode carries the signal in current mode to a transimpedance output. To reduce the magnitude of the far out blocking signals, a capacitor is connected across the output of the mixer core. This capacitor interacts with the input impedance of the folded cascode to form a real pole.

Removal of the dominant blockers means that the bias through the cascode can be much less than that through the mixer. Large voltage swings are kept absent from the output of the mixer core by the low impedance of the cascode. The current mode signal from the folded cascode is driven into a shunt RC, where the signal is converted into a voltage and simultaneously filtered a second time. After two poles of filtering, the dynamic range requirements are reduced from 105 to 85 dB. Any in-band gain or delay variation resulting from these real poles is compensated by the Sallen Key stage that follows them.

2) *Low-Offset, Low-Noise $g_m C$ Filter*: The $g_m C$ filters make use of feedback to minimize noise and dc offset generation. The unit $g_m C$ cell is shown in Fig. 14. A standard two quadrant Gilbert multiplier is used [6]. A degenerated transconductance connects to a pair of diodes providing predistortion before driving an undegenerated differential pair. The resulting circuit produces a linear stage with transconductance given by

$$G_m = \frac{I_{out, diff}}{V_{in, diff}} = \frac{I_{tune}}{R_e \cdot I_{bias}}. \quad (5)$$

Generally, $g_m C$ filters make use of separate transconductors for each feedforward and feedback path. In this design, area and power savings are realized by using only one predistortion

Fig. 14. Tunable g_m stage.Fig. 15. Two implementations of a single pole $g_m C$ filter.

stage for each capacitor. Multiple transconductances are implemented by connecting multiple tunable differential pairs to each predistortion stage. Each transconductance can be represented by a predistortion stage with small-signal voltage gain A and a tunable stage which, together with A , yields g_m . Separate and shared predistortion implementations of a single pole design are shown in Fig. 15. The transfer function for both designs is given by

$$\frac{I_{out}}{I_{in}} = \frac{G_{m2}}{sC + G_{m1}}. \quad (6)$$

The effects of noise or dc offsets introduced by the predistortion stages are very different in these two implementations. These effects can be modeled by perturbations d_1 and d_2 after each predistortion stage. The responses to these perturbations for the separate case and the combined case are given by

$$I_{out} = \frac{G_{m2}}{A} \left[d_2 + d_1 \cdot \left(\frac{G_{m1}}{G_{m1} + sC} \right) \right] \quad (7)$$

$$I_{out} = \frac{G_{m2}}{A} \cdot \left(d_1 \cdot \frac{sC}{G_{m1} + sC} \right). \quad (8)$$

The combined case yields two advantages. First, d_2 is no longer present. Second, d_1 is suppressed in band by the presence of the sC term in the numerator. Indeed, at dc, the perturbation is completely eliminated, reducing flicker noise and dc offsets in

TABLE II
SYNTHESIZER SUMMARY

Synthesizer	
Tuning range	1250MHz -1650MHz
Resolution	3Hz
Settling time (to 100ppm)	175 μ s
Req'd settling time (to 100ppm) [3]	287 μ s
PN @ 100kHz	-106dBc/Hz
PN @ 400kHz	-124dBc/Hz
PN @ 3MHz	-141dBc/Hz
Bias current	28mA

this stage. This suppression means matching and flicker noise are of little concern in the design of predistortion stages, and therefore the designs can be optimized for very small size and low power. In a similar fashion, the predistortion reuse can be extended to n th-order $g_m C$ filters containing real and or complex poles.

IV. LO AND FREQUENCY SYNTHESIS

In order to accommodate a quad-band transceiver capable of GPRS operation, a wide-tuning, fast-locking PLL is necessary. A fractional- N architecture [14] is chosen with a nominal loop bandwidth of 25 kHz achieving lock times of less than 175 μ s. Due to stringent noise specifications and process limitations, a standard varactor-based VCO system is unacceptable. A hybrid technique is used where the UHF is centered digitally before the analog PLL is engaged. The digital calibration adjusts a switched capacitor array to bring the VCO's frequency within a few megahertz of the desired frequency. Once the calibration is complete, the analog loop provides the fine-tuning. See Table II.

A. UHF VCO

The UHF VCO is based on a standard negative g_m topology coupled to an LC tank [15]. The negative g_m is created by a cross-coupled PFET pair. A PMOS core was used instead of an NMOS core not only because the buried channel PMOS device inherently has lower $1/f$ noise, but also to isolate the devices from the substrate.

The differential LC tank consists of a pair of on-chip spiral inductors oriented to reject common mode magnetic pickup, a varactor, and a binary weighted capacitor array [16]. The switched capacitor array is designed to provide the highest Q possible and still provide the necessary C_{on}/C_{off} ratio needed to achieve the required tuning range. The inductor size is optimized for a quality factor (Q) of about 9 and self-resonant frequency (SRF) of about 9 GHz to help noise performance and tuning range.

B. Fractional- N PLL

The fractional- N PLL [14] is used to offer fast channel switching and arbitrarily fine frequency resolution and to alleviate design constraints for phase noise and reference spurious, as shown in Fig. 16. The fine frequency resolution is accomplished by interpolating a fractional division using an oversampled $\Delta\Sigma$ modulator with coarse integer divider.

The fractional- N synthesizer consists of a P/FD and charge pump that have four different settings for phase detector gain as

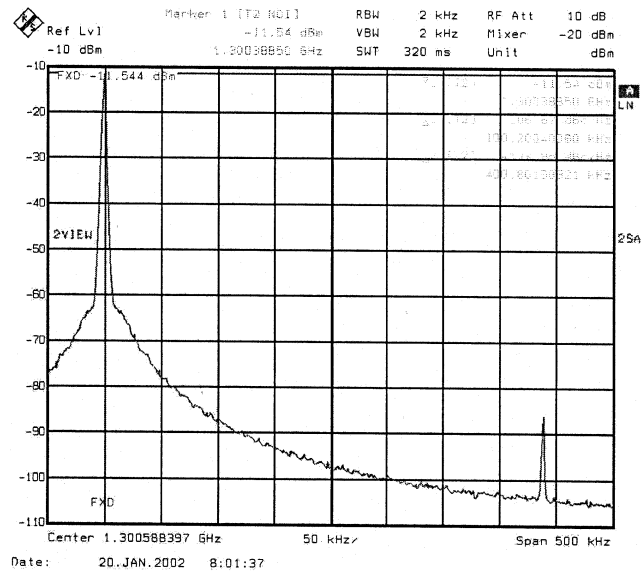


Fig. 16. LO spectrum.

well as a polarity bit. The 8/9 prescaler consists of a dual modulus 4/5 divider and a toggle flip-flop. A third-order $\Delta\Sigma$ modulator is used. It has two additional out-of-band poles to filter out the quantization noise at high frequencies. The 3-b output of the $\Delta\Sigma$ modulator is fed to a control block that provides randomized data to the counters.

V. TRANSLATION LOOP TRANSMITTER

The transmitter consists of a frequency translation up-conversion loop [17] with in-loop vector modulation. One LO signal provides both the down-converted and reference IF signals. Because it is generated by dividing down the LO, the channel-dependent IF prevents pulling between the VCOs and LO to IF crossover spurs. The use of selectable frequency dividers and programmable charge pump gain and polarity adds flexibility for frequency planning. The transmit PLL meets the required GSM spectral mask with margin, as shown in Fig. 17. Many of the LO blocks are shared with the receiver, reducing area.

The I/Q vector modulators in the feedback path of the transmitter PLL use a harmonic cancellation technique to reduce IM3 spurs. The modulator performs third-harmonic cancellation by generating two phase-split IF signals that are 60° phase shifted from each other. Using these signals to drive the switching core of the modulator results in third-harmonic terms 180° apart. When the outputs are summed, this technique provides over 20 dB of third-harmonic suppression and allows the external IF filter to be a simple LC shunt filter.

Completely differential, integrated VCOs in the transmitter as well as the LO avoid unwanted interaction through bond wires. The transmit VCOs cover all four bands and meet the stringent out-of-band noise specifications of the GSM standard [3]. See Table III. The same digital frequency centering technique is used for the transmitter that is used for the UHF PLL. Since both PLLs are on the same chip and the transmit and UHF frequencies are related through known band select and divide ratio information, the transmit channel request for the digital centering

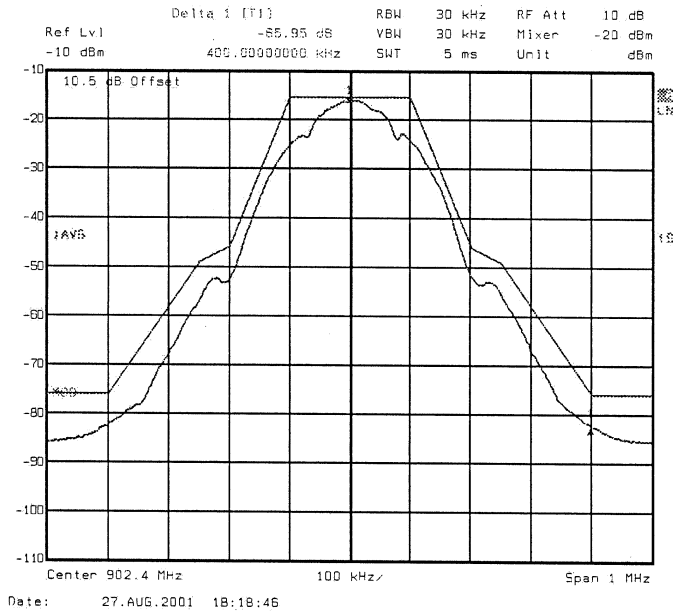


Fig. 17. GSM output spectrum.

TABLE III
TRANSMITTER SUMMARY

Transmitter	850/900MHz	1800/1900MHz
Phase error	1.5°	1.6°
Req'd phase error (RMS) [3]	<5°	<5°
200kHz noise	-36dBc/30kHz	-36dBc/30kHz
Req'd 200kHz noise [3]	-30dBc/30kHz	-30dBc/30kHz
400kHz noise	-64dBc/30kHz	-65dBc/30kHz
Req'd 400kHz noise [3]	-60dBc/30kHz	-60dBc/30kHz
20MHz noise	-164dBc/Hz	-158dBc/Hz
Req'd 20MHz noise [3]	-161dBc/Hz	-155dBc/Hz
Bias current (incl. Synth.)	130mA	120mA
Operating voltage	2.7-3.6V	2.7-3.6V

is calculated through a decoder block each time the device is programmed for a new LO channel.

VI. INTEGRATION ISSUES

A. Observability and Controllability

The device is made programmable via a serial bus to facilitate testing, debugging, and optimization. The simplest way to use digital control in an RF SOC is by turning off and bypassing blocks. An example is in a completely integrated LO chain. A bidirectional LO port buffer allows observation of the UHF VCO or the use of an external LO (Fig. 18). Normally, the buffer takes the UHF VCO as an input and drives the LO chain. If the VCO is to be monitored, an extra buffer is activated, driving external inductive loads through the LO port. Alternately, a separate buffer may be biased, using the LO pads as inputs. Such a capability makes it possible to distinguish between problems in the oscillator, the PLL, and the LO buffers or mixers and characterize them separately.

A second way digital control can be used is in the modification of circuit properties. For example, individually modu-

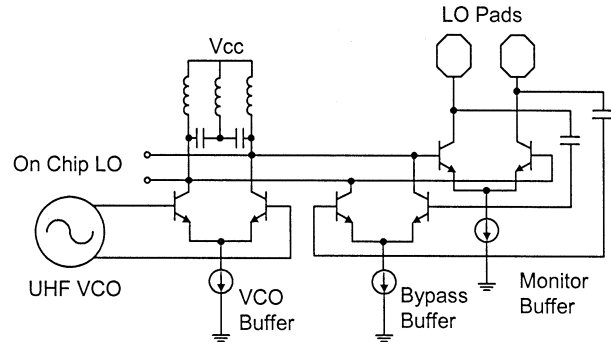


Fig. 18. LO test buffer.

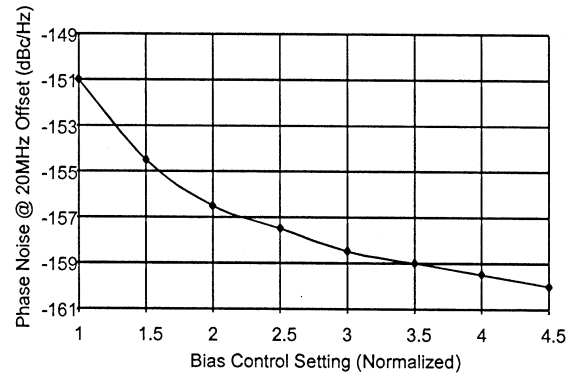


Fig. 19. Programmable bias in DCS/PCS transmitter VCO.

lating the bias currents of RF blocks and observing the effects can often reveal sources of excessive noise or nonlinearity in an RF chain. In addition, such controllability allows for software optimization of circuits, permitting system designers to tradeoff performance and power consumption in the different sections of a receive or transmit chain. See Fig. 19.

B. Layout

This level of radio integration [18] raises the risk of unwanted coupling of signals between circuits. Careful top-level layout reduces such risks. Specifically, as shown in Fig. 20, the sigma-delta UHF VCO transmit VCOs and LNAs have been situated in the extreme four corners of the chip. To prevent switching noise in the fractional- N synthesizer from interfering with the LNAs, the two circuits are separated by the low-noise baseband analog circuitry. n- and p-type substrate contacts under the baseband supply and ground shunt synthesizer switching noise in the substrate. The degradation of receiver NF due to the synthesizer is less than 0.2 dB.

VII. PROCESS SELECTION

The transceiver was designed in a 0.35- μm BiCMOS process [19] with NPN $f_t = 35$ GHz. The RF and analog signal paths made extensive use of the high-performance NPN devices, benefiting from their higher speed, better matching, and lower flicker noise. The availability of bipolar junction transistors (BJTs) did not preclude the use of CMOS in those RF applications where CMOS is superior (e.g., in VCOs). Since BJTs provide higher, more predictable g_m and f_t , they were used in the receivers LNAs. Although BJTs are often maligned for their nonlinearity, when combined with high speed, strongly non-

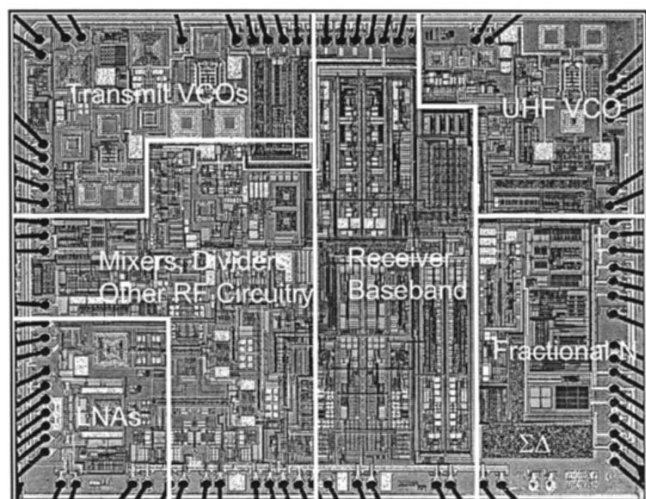


Fig. 20. Microphotograph of transceiver.

linear circuits are ideal for implementing mixers. In addition, since BJTs rely on the behavior of junctions in bulk silicon, rather than surface oxide interfaces, both matching and flicker noise are better in high-speed BJTs than comparable speed MOSFETs. Both mismatch and flicker noise have important consequences for the signal quality at the baseband output of the mixers in a DCR, implying that such mixers are best implemented in BJTs.

CMOS logic was used extensively in the frequency synthesizer as well as an effective means for digital controllability. CMOS was also used in the design of compact, low-power analog circuits. FET current mirrors are generally smaller than standard degenerated BJT mirrors (especially when lateral PNPs are being used). The fact that MOSFET gates draw no real current found use in the implementation of track and hold circuits for dc offset correction in the receiver.

Two properties of CMOS were exploited in the design of RF blocks. The gate of a CMOS transistor looks predominantly capacitive and generates no gate shot noise. In addition, CMOS transistors can be driven deep into the triode region and recover at speeds comparable to their turn-on times without generating excessive noise. In BJTs, deep saturation leads to degradation in β , f_t and all relevant capacitances and noise mechanisms. These properties of CMOS can be used for circuits where very strong signals are needed in combination with low wide-band noise [20].

The inductors were implemented in a 3- μm -thick third metal layer, permitting construction of high Q resonant tanks on chip. MIM capacitors between the second and third metal layers provided very high Q capacitance with a minimum of backside parasitic.

VIII. CONCLUSION

We have presented a quad-band GSM transceiver that integrates all of the active components of the radio except for the PA. The chip includes a direct conversion receiver, frequency synthesizer, transmitter, and all the VCOs. The IC meets the required specifications for GPRS class 12 with margin [3].

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