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Yamamoto

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(54) **HIGH FREQUENCY POWER AMPLIFIER**

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(52) **U.S. Cl.** **330/51**; 330/295; 330/298; 330/134

(58) **Field of Search** 330/51, 126, 295, 330/296, 298, 133, 134, 285

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(57) **ABSTRACT**

A dual band system high frequency power amplifier has biasing circuits and a bias switching circuit, each circuit having heterojunction bipolar transistors (HBTs) so that the high frequency power amplifier can be integrated with an MMIC of HBTs. A bias switching circuit for switching a first biasing circuit and a second biasing circuit, each made with HBTs, is built with common AlGaAs or GaAs HBTs, having three or more such HBTs connected in series so that the total of each base-emitter voltage, Vbe, does not exceed 3 V.

18 Claims, 9 Drawing Sheets

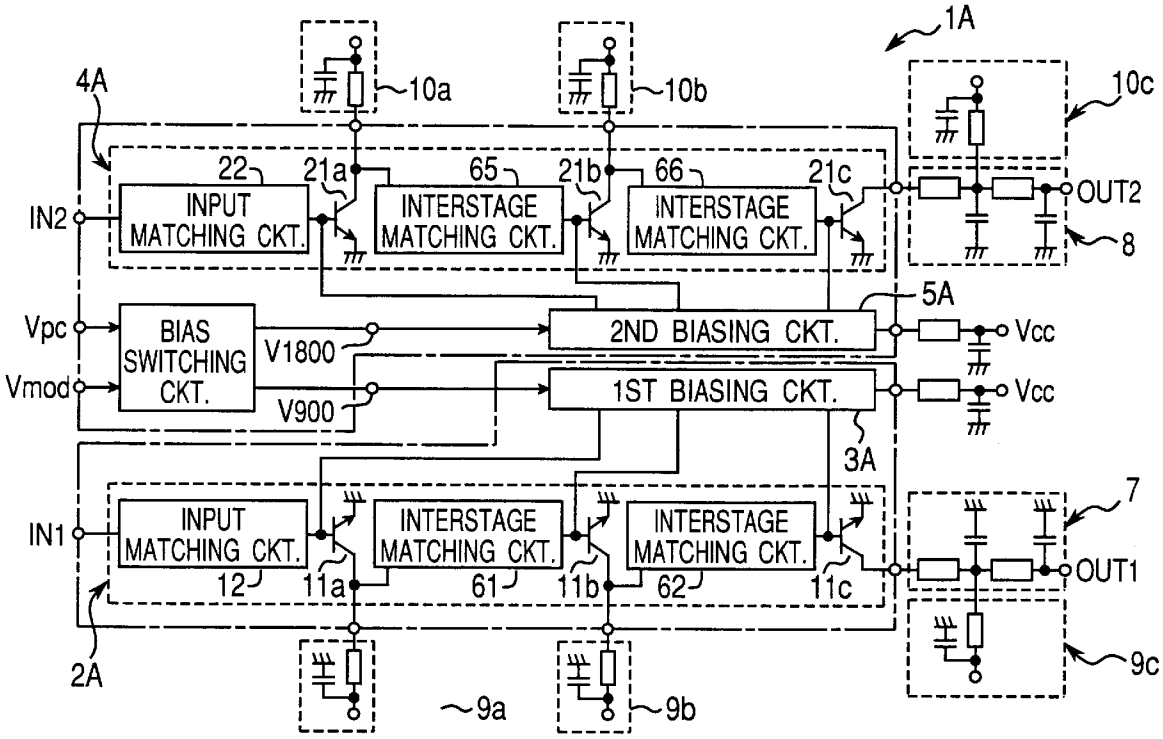


Fig.1

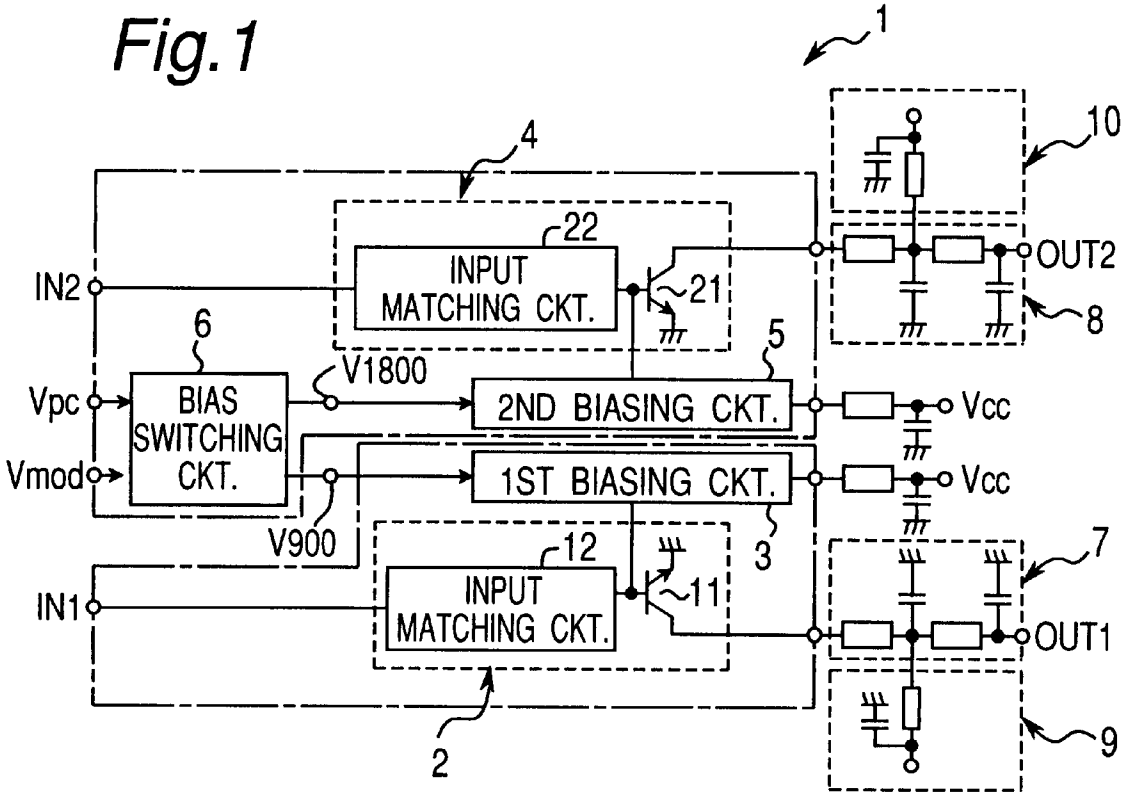

1
4
10
22
INPUT MATCHING CKT.
21
OUT2
IN2
8
6
5
V1800
Vpc
BIAS SWITCHING CKT.
2ND BIASING CKT.
Vcc
Vmod
1ST BIASING CKT.
Vcc
V900
12
3
7
IN1
INPUT MATCHING CKT.
11
OUT1
2
9

Fig.2

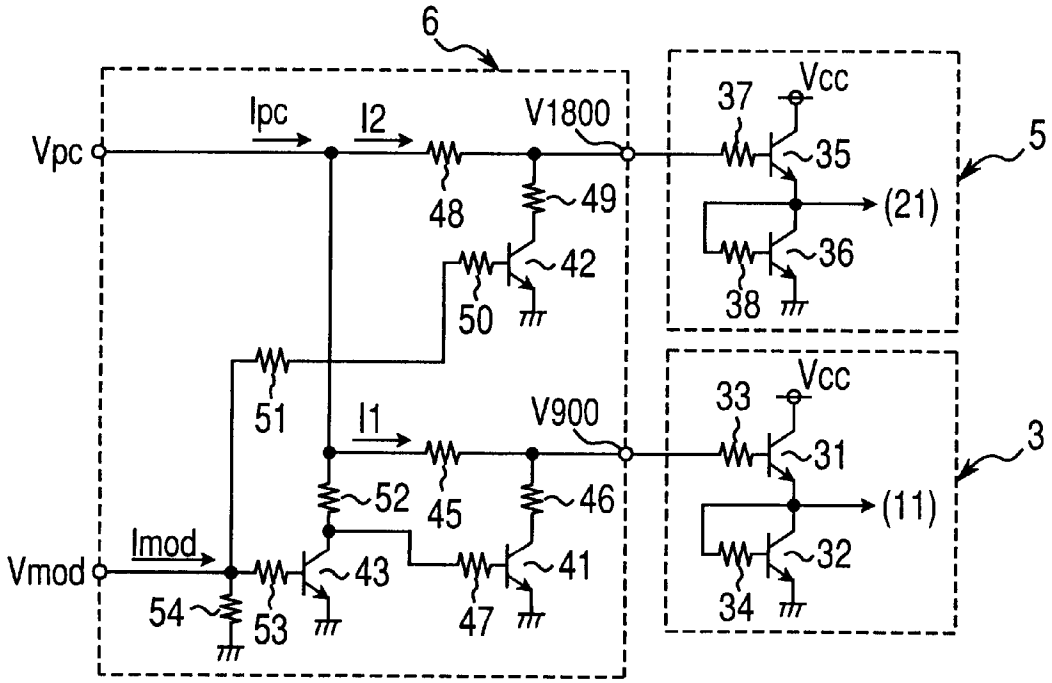

6
Vcc
37
Ipc
I2
V1800
Vpc
35
5
48
49
(21)
36
42
38
50
51
Vcc
33
I1
V900
31
3
52
45
46
(11)
Imod
32
Vmod
43
41
54
53
47
34

Fig.3A

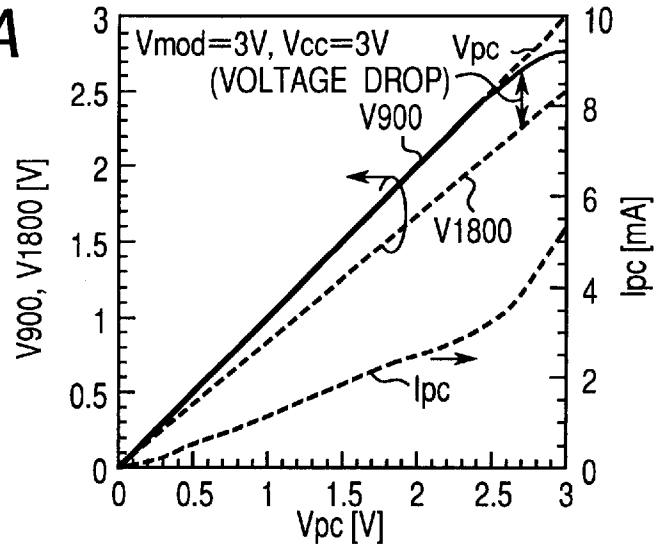


Fig.3B

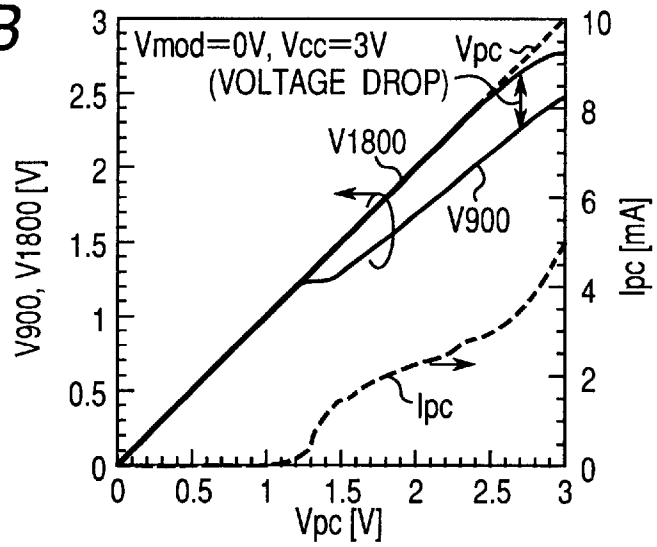
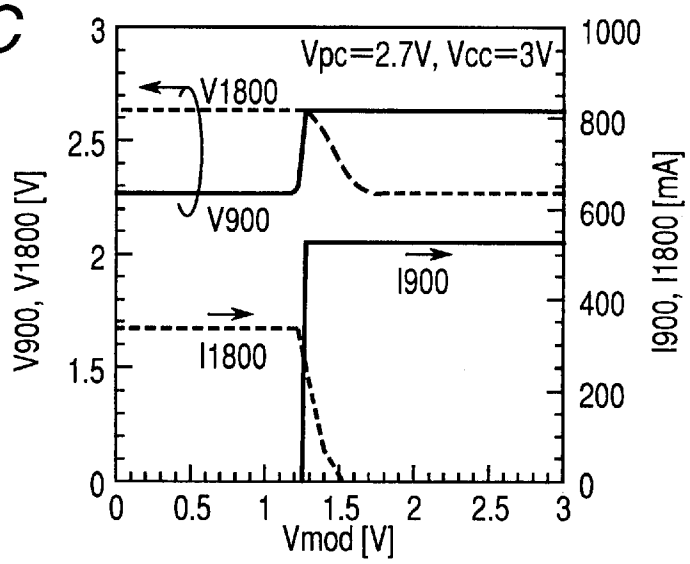


Fig.3C



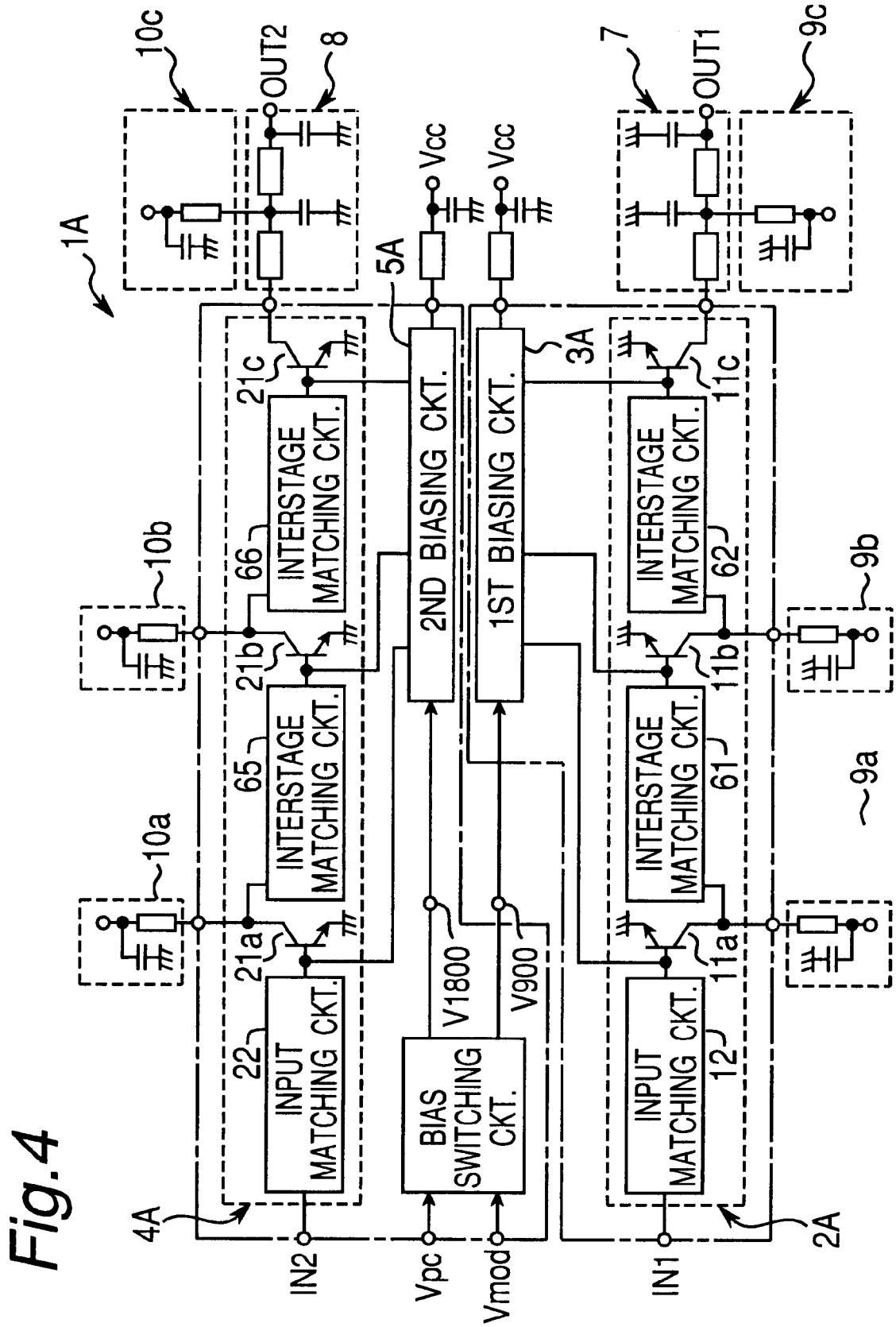

1A
10c
OUT2
8
Vcc
Vcc
7
OUT1
9c
5A
3A
21c
INTERSTAGE MATCHING CKT.
66
2ND BIASING CKT.
1ST BIASING CKT.
11c
INTERSTAGE MATCHING CKT.
62
10b
21b
11b
9b
65
INTERSTAGE MATCHING CKT.
61
INTERSTAGE MATCHING CKT.
9a
10a
21a
11a
22
INPUT MATCHING CKT.
V1800
V900
BIAS SWITCHING CKT.
12
INPUT MATCHING CKT.
4A
2A
IN2
Vpc
Vmod
IN1

Fig.4

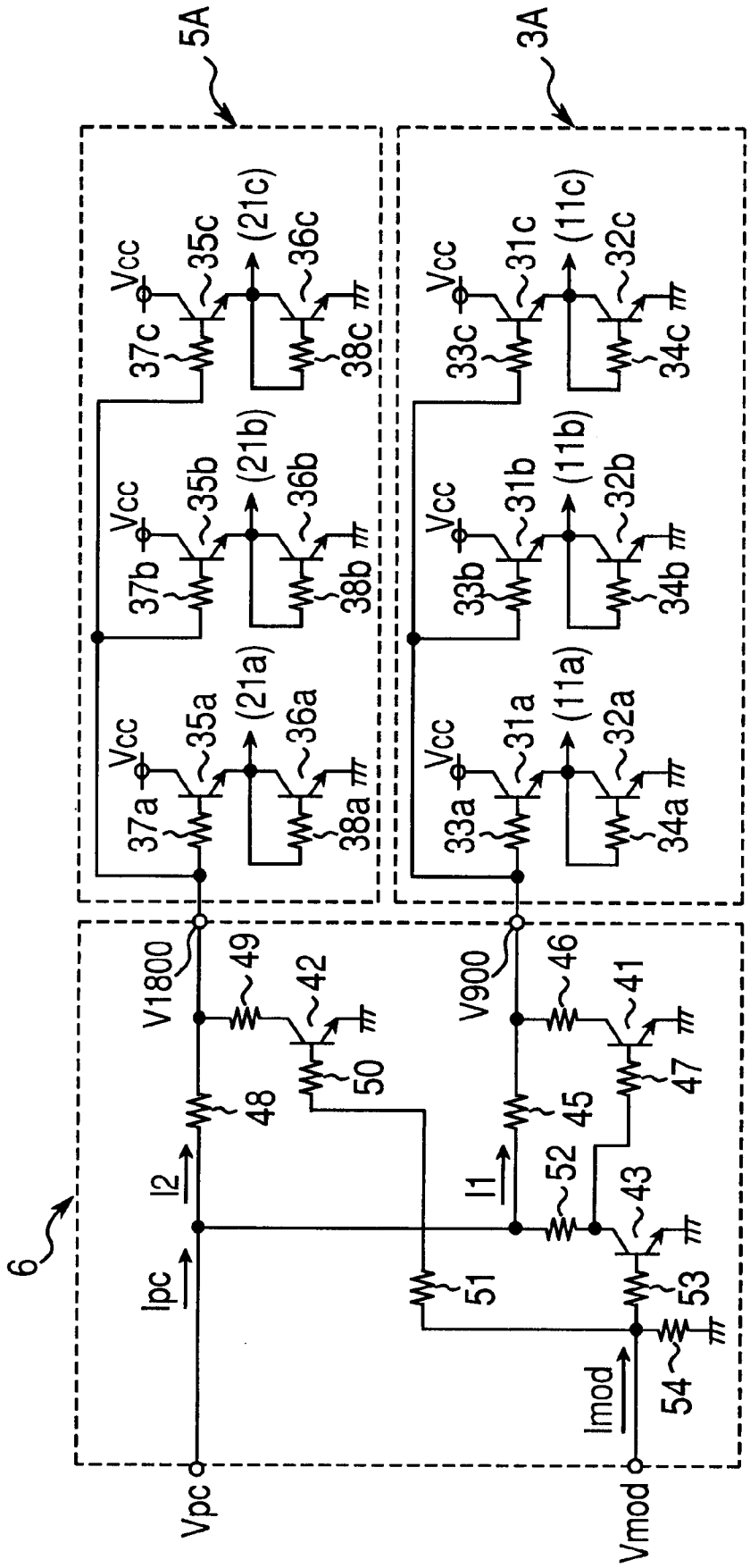

5A
3A
Vcc
37a
35a
(21a)
36a
38a
37b
35b
(21b)
36b
38b
37c
35c
(21c)
36c
38c
33a
31a
(11a)
32a
34a
33b
31b
(11b)
32b
34b
33c
31c
(11c)
32c
34c
V1800
V900
49
42
50
48
46
41
47
45
52
43
51
53
54
6
I2
Ipc
I1
Imod
Vpc
Vmod

Fig.5

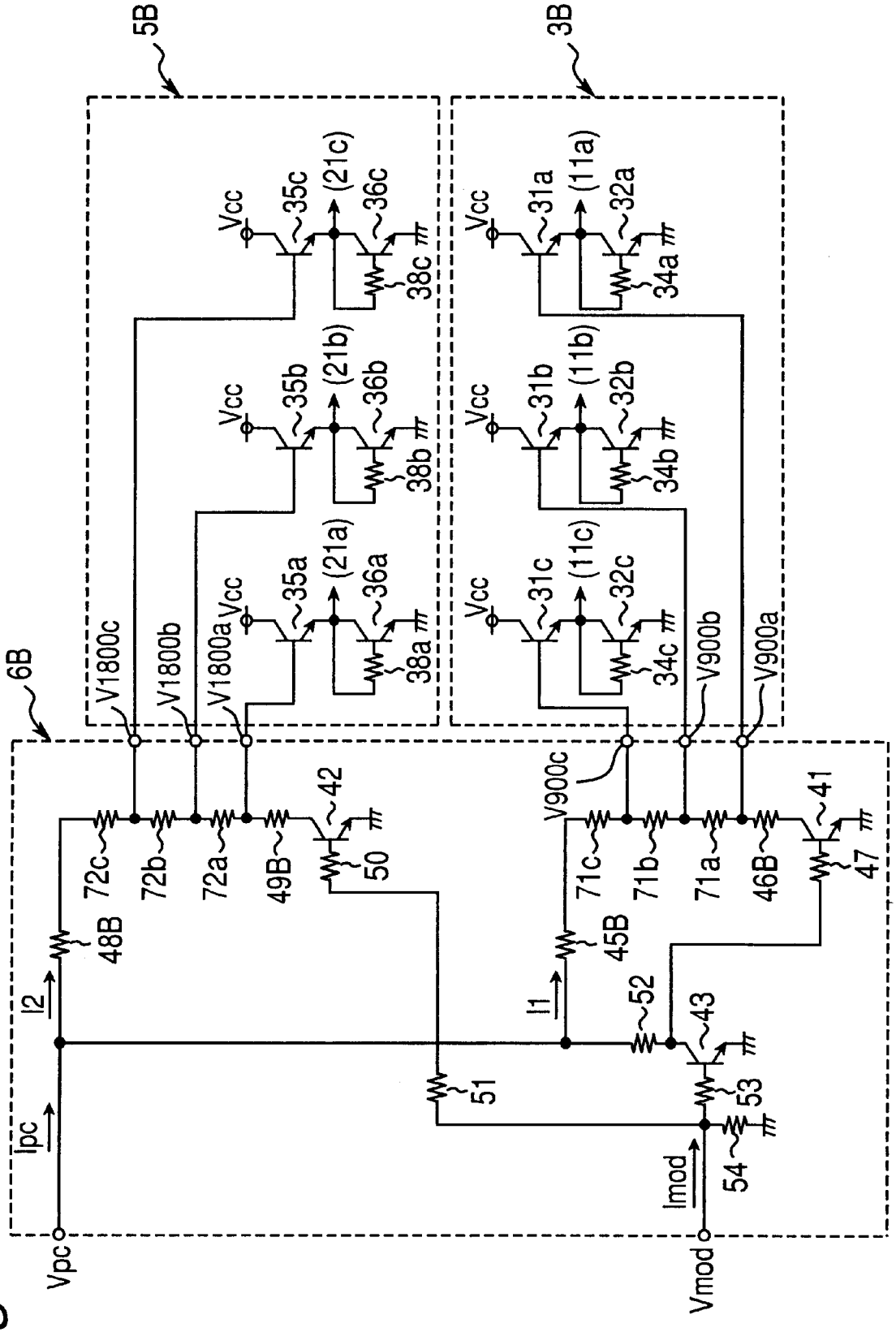

5B
3B
6B
Vcc
35c
(21c)
36c
38c
35b
(21b)
36b
38b
35a
(21a)
36a
38a
31a
(11a)
32a
34a
31b
(11b)
32b
34b
31c
(11c)
32c
34c
V1800c
V1800b
V1800a
V900c
V900b
V900a
72c
72b
72a
49B
42
50
48B
I2
Ipc
Vpc
51
71c
71b
71a
46B
41
47
45B
I1
52
43
53
54
Imod
Vmod

Fig.6

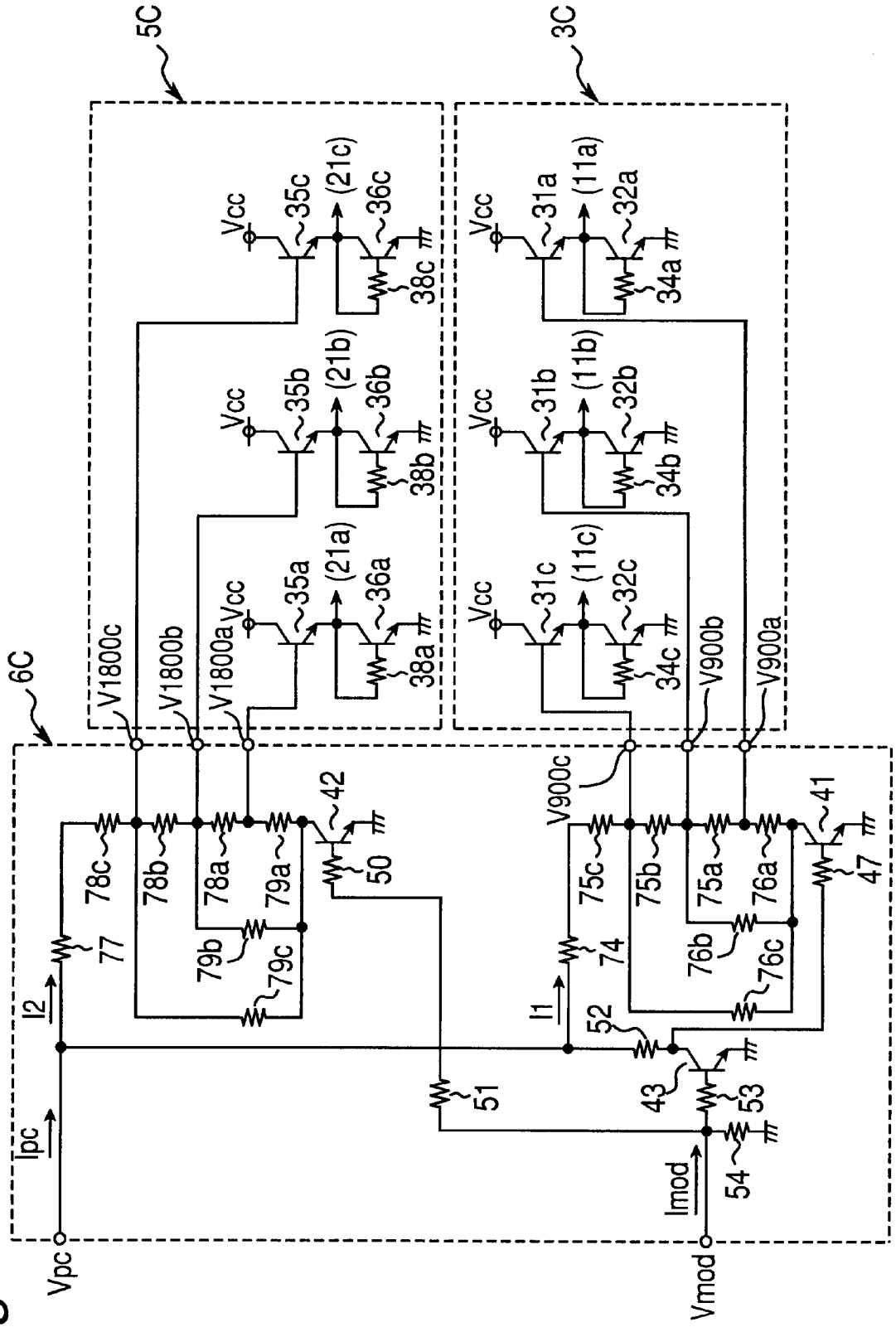

5C
3C
6C
Vcc
35c
(21c)
36c
38c
35b
(21b)
36b
38b
35a
(21a)
36a
38a
31a
(11a)
32a
34a
31b
(11b)
32b
34b
31c
(11c)
32c
34c
V1800c
V1800b
V1800a
V900c
V900b
V900a
78c
78b
78a
79a
79b
79c
77
42
50
51
75c
75b
75a
76a
76b
76c
74
41
47
52
43
53
54
I2
Ipc
I1
Imod
Vpc
Vmod

Fig.7

Fig.8

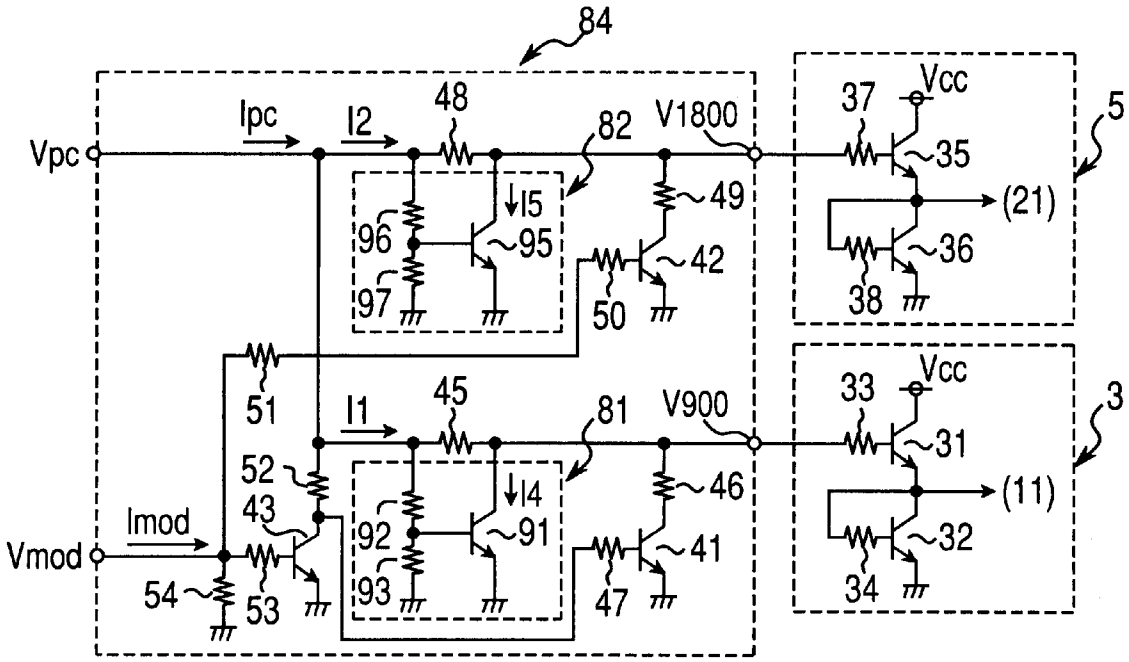
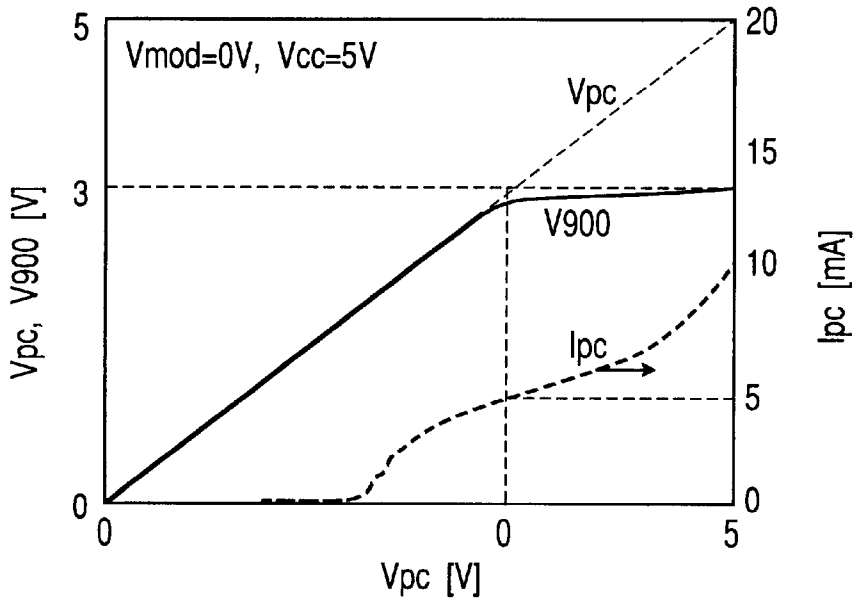

84
Vpc
Ipc
I2
48
82
V1800
37
Vcc
5
35
(21)
36
38
I5
96
95
97
49
42
50
51
I1
45
81
V900
33
Vcc
3
31
(11)
32
34
52
43
Imod
Vmod
54
53
I4
92
91
93
46
41
47

Fig.9


Vmod=0V, Vcc=5V
Vpc
V900
Ipc
Vpc, V900 [V]
Ipc [mA]
Vpc [V]
0
3
5
0
5
10
15
20
0
0
5

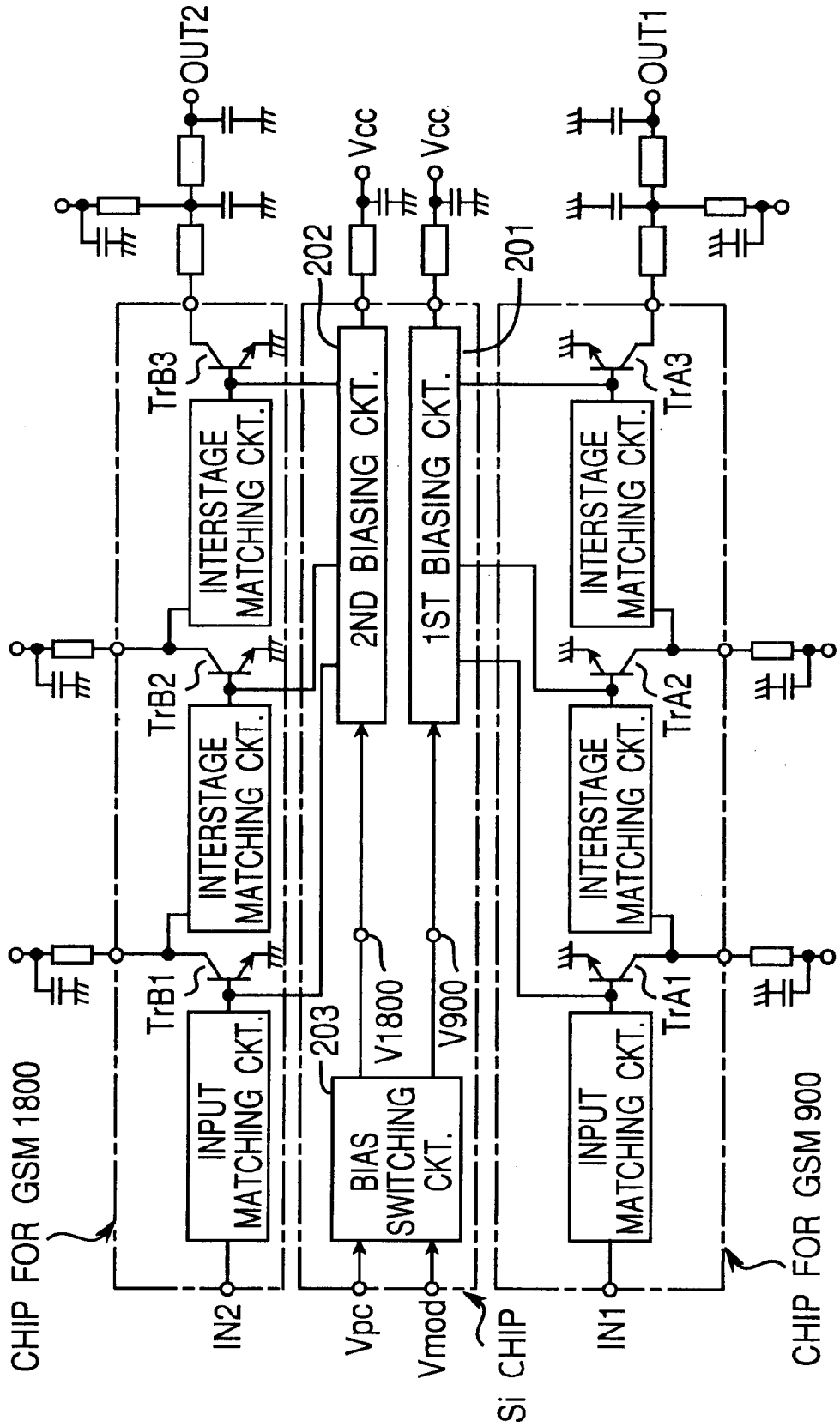


Fig.10 PRIOR ART

Fig.11 PRIOR ART

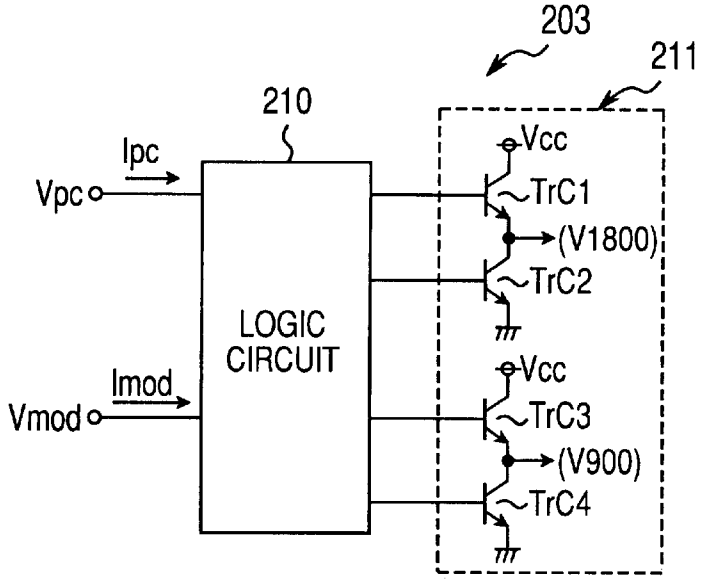


Fig.12A PRIOR ART

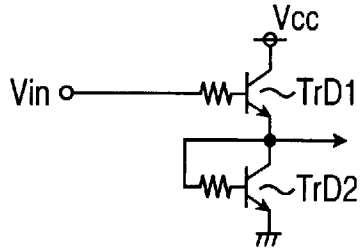
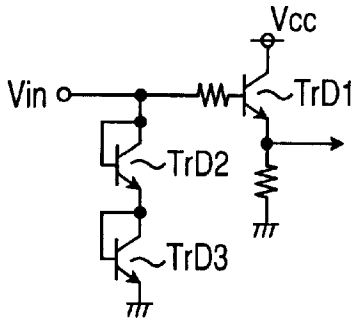


Fig.12B PRIOR ART



HIGH FREQUENCY POWER AMPLIFIER

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a high frequency power amplifier for dual band systems used, for example, in mobile telephones, and relates more particularly to a high frequency power amplifier of heterojunction bipolar transistors (HBT) having a bias switching circuit for switching a bias circuit to select a power amplifier.

2. Description of the Prior Art

Monolithic microwave integrated circuits (MMICs) and modules (hybrid ICs and multichip modules) using GaAs metal-semiconductor field effect transistors (MESFETs), GaAs high electron mobility transistors (HEMTs), or GaAs-based HBTs are widely used in power amplifiers for mobile communications devices. Compared with a conventional FET, a GaAs-based HBT does not require a negative gate bias voltage, enabling a single power supply operation, and can effect an on/off operation similarly to a Si-MOSFET but without an analog switch on the drain side. A further advantage is that GaAs-based HBTs can be used to achieve a smaller power amplifier generating a rated output power with a higher output power density than is possible with a conventional FET power amplifier. GaAs-based HBTs are therefore considered promising as power elements in future mobile communication devices.

With recent sharp increases in demand for mobile phones, telephones and services enabling access to two systems using a single handset have been introduced. In Europe, for example, there are two mobile telephone services: GSM 900 (Global System for Mobile Communications), a 900 MHz system that is the most widely used mobile telephone service in Europe, and DCS 1800, a competing system that operates in the 1800 MHz band. Japan also has two systems: Personal Digital Cellular (PDC), a 900 MHz mobile telephone system, and PHS (Personal Handyphone System), a 1900 MHz digital cordless telephone system. So-called dual band mobile phones that can switch between two different telephone services are already available.

FIG. **10** is an exemplary circuit block diagram of a high frequency power amplifier for use in a conventional dual band mobile phone.

Referring to FIG. **10**, GSM 900 transistors TrA**1** to TrA**3**, that is, HBTs for amplification in the 900 MHz band, are biased by a first biasing circuit **201**. GSM 1800 TrB**1** to TrB**3**, that is, HBTs for amplification in the 1800 MHz band, are biased by a second biasing circuit **202**.

Bias switching circuit **203** exclusively selects and operates either the first biasing circuit **201** or second biasing circuit **202** based on the signal level of a two-valued input signal Vmod applied to the Vmod terminal. The bias switching circuit **203** also passes an output control signal based on the signal level of the input signal Vpc applied to the Vpc terminal to the first biasing circuit **201** or second biasing circuit **202** to adjust the level of the output signal passed from output terminals OUT**1** and OUT**2**. When input signal Vpc is 0 V, the bias switching circuit **203** stops the operation of both the GSM 900 power amplifier and the GSM 1800 power amplifier regardless of input signal Vmod.

FIG. **11** is a typical circuit diagram of the bias switching circuit **203** used in the conventional high frequency power amplifier shown in FIG. **10**. As shown in FIG. **11**, this bias switching circuit **203** comprises a logic circuit **210** of CMOS or other silicon circuit elements, and an output buffer **211**.

The output buffer **211** comprises a plurality of npn transistors TrC**1** to TrC**4** made in silicon. The logic circuit **210** converts the input signal Vpc supplied from a DA converter (not shown in the figure) according to the signal level of input signal Vmod, and outputs either signal V**900** or V**1800** through output buffer **211**. The bias switching circuit **203** thus outputs signal V**900** or V**1800** to select a particular power amplifier and controls the signal level of the output signal from the selected power amplifier based on input signal Vpc, and stops operation of the other (unselected) power amplifier regardless of input signal Vpc.

It is to be noted that while the first biasing circuit **201** and second biasing circuit **202** shown in FIG. **10** are made with silicon elements, those shown in FIG. **12**A and FIG. **12**B are made using HBT as known from the literature. The biasing circuit shown in FIG. **12**A can compensate for a change in the base-emitter voltage Vbe according to the temperature coefficient of the power amplification HBT in FIG. **10** by means of transistor TrD**2**, as can the biasing circuit shown in FIG. **12**B using transistors TrD**2** and TrD**3**.

It is to be noted that all transistors TrD**1** to TrD**3** in FIGS. **12**A and **12**B are HBTS, and either signal V**900** or V**1800** in FIG. **11** can be applied to either biasing circuit through the biasing circuit input terminal Vin.

Unlike an FET, however, an HBT operates by amplifying the base current, and requires a base current supply between several 10 to 100 mA to achieve the high 2 W to 4 W output of a GSM phone. It is, however, also difficult to directly obtain such a high base current from a standard Si-CMOS IC because the output current used to assure a specific output voltage from a standard CMOS device is a maximum of several milliamperes.

Furthermore, two power amplifiers can be easily controlled using input signals Vpc and Vmod due to the general utility of the logic circuit design when silicon elements are used in the bias switching circuit, but a separate control circuit using silicon elements is required for controlling devices other than the HBT power amplifier.

When silicon elements are used in the bias switching circuit and biasing circuits, or just the bias switching circuit, these circuits cannot be integrated to an MMIC comprising HBTs. A separate silicon chip is therefore needed, and this reduces yield during mass production.

SUMMARY OF THE INVENTION

With consideration for the aforementioned problems, an object of the present invention is to provide a dual band system high frequency power amplifier that can be integrated with an MMIC comprising HBTs by using HBTs to form the biasing circuits and bias switching circuit of each dual band system high frequency power amplifier comprising HBTs.

To achieve this object, a high frequency power amplifier according to the present invention has two power amplifiers each having at least one power amplifying heterojunction bipolar transistor (HBT), two biasing circuits each disposed for each power amplifier and including a HBT, and a bias switching circuit for exclusively switching operation between the biasing circuits in accordance with first and second signals input to the bias switching circuit. The bias switching circuit of the high frequency power amplifier has a first switching circuit including an HBT for controlling output of the first signal for controlling biasing circuit operation to one of the biasing circuits; a second switching circuit including an HBT for controlling output of the first signal to an other biasing circuit; and a third switching

circuit including an HBT for controlling operation of the second switching circuit according to the second signal for controlling operation of the first switching circuit to exclusively select and operate the first and second switching circuits.

The bias switching circuit for switching operation of biasing circuits constructed with HBTs thus has a first switching means for controlling output to one biasing circuit, a second switching circuit for controlling output to another biasing circuit, and a third switching circuit for exclusively selecting the first or second switching circuit to operate. The first to third switching means of the bias switching circuit are made using common AlGaAs or GaAs HBTs, three or more of which are connected in series so that the total combined base-emitter voltage Vbe does not exceed 3 V. The bias switching circuit can therefore operate reliably even in low 3-V power supply systems, and can thus be integrated with an HBT MMIC to simply the manufacturing process.

The first and second switching means each preferably has a resistance series circuit having a plurality of resistors connected in series for voltage dividing the signal Vpc voltage, wherein the HBT in each of the first and second switching means is a ground connecting HBT for controlling connection of the resistance series circuit to ground, and output a control signal to a corresponding biasing circuit from a node between specific resistors in this resistance series circuit.

The bias switching circuit can thus be achieved using few HBT and resistors, and the increase in MMIC chip size resulting from bias switching circuit integration can be minimized.

Yet further preferably, each power amplifier is a multi-stage power amplifier for power amplifying by means of a plurality of power amplifying HBTs, each corresponding biasing circuit has a circuit for supplying bias to each power amplifying HBT, and the first and second switching circuits output control signals to the corresponding biasing circuit so that the first signal current gradually increases from a bias supplied to the first stage power amplifying HBT to a bias supplied to the last stage power amplifying HBT.

It is therefore possible to minimize the voltage drop in signal Vpc to the circuit supplying bias to the last-stage power amplifying HBT in each biasing circuit, that is, the HBT from which the most current flows for a signal Vpc.

Yet further preferably, the first and second switching circuit each further has a signal level adjusting resistor for adjusting the level of the control signal applied to the corresponding biasing circuit, the signal level adjusting resistor being parallel connected to a node between specific resistors in the resistance series circuit and a node between the resistance series circuit and ground connecting HBT.

Yet further preferably, an HBT in the third switching circuit controls bias supply to the base of the HBT in the second switching circuit according to the second signal. A bias switching circuit of HBTs that can operate in a 3-V system can thus be achieved, and the bias switching circuit can be integrated with a HBT MMIC.

When it is additionally desirable to prevent thermal runaway and heat damage to the power amplifier resulting from an externally applied overvoltage, the first and second switching circuits each further preferably includes a protection circuit for protecting each biasing circuit from an overvoltage applied to a terminal which receives the first signal. In this case, each protection circuit is preferably a Vbe multiplier comprising an HBT. As a result, thermal runaway and heat damage to the power amplifier resulting from an externally applied overvoltage can be prevented with a simple circuit design.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be readily understood from the following description of preferred embodiments thereof made with reference to the accompanying drawings, in which like parts are designated by like reference numeral and in which:

FIG. **1** is a typical circuit diagram of a high frequency power amplifier for a dual band system according to a first embodiment of the present invention;

FIG. **2** shows the first biasing circuit, second biasing circuit, and bias switching circuit shown in FIG. **1**;

FIG. **3**A, FIG. **3**B and FIG. **3**C are graphs showing an operating characteristic of the bias switching circuit shown in FIG. **2**;

FIG. **4** is a typical circuit diagram showing an alternative version of the high frequency power amplifier for a dual band system shown in FIG. **1**;

FIG. **5** shows the first biasing circuit, second biasing circuit, and bias switching circuit shown in FIG. **4**;

FIG. **6** is a typical circuit diagram showing an alternative version of the first biasing circuit, second biasing circuit, and bias switching circuit;

FIG. **7** is a typical circuit diagram showing a further alternative version of the first biasing circuit, second biasing circuit, and bias switching circuit;

FIG. **8** is a typical circuit diagram of a high frequency power amplifier according to a second embodiment of the present invention;

FIG. **9** is a graph of a typical operating characteristic of the bias switching circuit in the power amplifier shown in FIG. **8**;

FIG. **10** is a typical circuit block diagram of a dual band system high frequency power amplifier according to the related art;

FIG. **11** is a typical circuit diagram of the bias switching circuit shown in FIG. **10**; and

FIG. **12**A and FIG. **12**B are typical circuit diagrams of the biasing circuits shown in FIG. **10** comprising HBTs.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of the present invention are described below with reference to the accompanying figures.

Embodiment 1

FIG. **1** is a typical circuit diagram of a high frequency power amplifier for a dual band system according to a first embodiment of the present invention. It is to be noted that the dual band system high frequency power amplifier shown in FIG. **1** comprises two single-stage power amplifiers, one each for GMS 900 and GMS 1800 systems.

As shown in FIG. **1**, high frequency power amplifier **1** comprises a first power amplifier **2**, a GSM 900 power amplifier; a first biasing circuit **3** for biasing the first power amplifier **2**; a second power amplifier **4**, a GSM 1800 power amplifier; a second biasing circuit **5** for biasing the second power amplifier **4**; a bias switching circuit **6** for exclusively selecting and operating either first biasing circuit **3** or second biasing circuit **5**; output matching circuits **7** and **8**; and collector biasing circuits **9** and **10**.

The first power amplifier **2** comprises power amplifying HBT **11** and input matching circuit **12**. HBT **11** power amplifies a high frequency signal input from input terminal **IN1** through input matching circuit **12**, and outputs the amplified high frequency signal from output terminal **OUT1** through output matching circuit **7**. Bias is supplied from collector biasing circuit **9** to the collector of HBT **11**, and another bias is supplied from the first biasing circuit **3** to the base of HBT **11**, for this operation.

The second power amplifier **4** similarly comprises power amplifying HBT **21** and input matching circuit **22**. The HBT **21** power amplifies a high frequency signal input from input terminal **IN2** through input matching circuit **22**, and outputs the amplified high frequency signal from output terminal **OUT2** through output matching circuit **8**. Bias is supplied from collector biasing circuit **10** to the collector of HBT **21**, and another bias is supplied from the second biasing circuit **5** to the base of HBT **21**, for this operation.

Operation of the first biasing circuit **3** and second biasing circuit **5** is controlled by bias switching circuit **6**. More specifically, the bias switching circuit **6** outputs a signal **V900**, which is a control signal for the first biasing circuit **3**, or a signal **V1800**, which is a control signal for the second biasing circuit **5**, to exclusively select and operate first biasing circuit **3** or second biasing circuit **5** based on the signal level of a two-value input signal Vmod (which is high at 3 V or low at 0 V, for example) applied from an external source to the Vmod terminal.

Based on the signal level of an input signal Vpc applied to the Vpc terminal from an external source, the bias switching circuit **6** also outputs signal **V900** or signal **V1800** to adjust the output level of the signal passed from output terminals **OUT1** and **OUT2**. By varying the level of input signal Vpc between 0 to 3 V, for example, the signal level of the output signal from output terminal **OUT1** or **OUT2** can be varied from a minus several ten dBm to +34 dBm. In addition, when input signal Vpc is 0 V, bias switching circuit **6** stops bias supply to both first biasing circuit **3** and second biasing circuit **5** to stop operation of both first power amplifier **2** and second power amplifier **4**.

FIG. **2** is a detailed circuit diagram of first biasing circuit **3**, second biasing circuit **5**, and bias switching circuit **6** shown in FIG. **1**. As shown in FIG. **2**, the first biasing circuit **3** comprises HBT **31** and **32**, and resistors **33** and **34**. Resistor **33** is the base resistance of HBT **31**, and resistor **34** is the base resistance of HBT **32**.

The collector of HBT **31** is connected to power supply terminal Vcc to which a specific dc supply voltage is applied; the emitter is connected to the collector of HBT **32**; and the node between the HBT **31** emitter and HBT **32** collector is connected to the base of HBT **11** in the first power amplifier **2** and is thus used as the output of the first biasing circuit **3**. The base of HBT **31** is connected through resistor **33** to the **V900** output terminal of bias switching circuit **6**. Control signal **V900** is thus applied from bias switching circuit **6** to the base of HBT **31**.

The base of HBT **32** is connected through resistor **34** to the collector, and the emitter is to ground. HBT **32** can thus compensate for a change in the base-emitter voltage Vbe according to the temperature coefficient of HBT **11** in first power amplifier **2**.

The second biasing circuit **5** similarly comprises HBTs **35** and **36**, and resistors **37** and **38**. Resistor **37** is the base resistance of HBT **35**, and resistor **38** is the base resistance of HBT **36**. The collector of HBT **35** is connected to power supply terminal Vcc, the emitter to the collector of HBT **36**, and this emitter-collector node is connected to the base of HBT **21** in the second power amplifier **4** and is thus used as the output of the second biasing circuit **5**. The base of HBT **35** is connected through resistor **37** to the **V1800** output terminal of bias switching circuit **6**. Control signal **V1800** is thus applied from bias switching circuit **6** to the base of HBT **35**.

The base of HBT **36** is connected through resistor **38** to the collector, and the emitter is to ground. HBT **36** can thus compensate for a change in the base-emitter voltage Vbe according to the temperature coefficient of HBT **21** in second power amplifier **4**.

The bias switching circuit **6** comprises HBTs **41** to **43**, and resistors **45** to **54**. Terminal Vpc is connected through a series circuit of resistors **45** and **46** to the collector of HBT **41**. The node between resistors **45** and **46** is connected to terminal **V900** of bias switching circuit **6**, and through resistor **33** of first biasing circuit **3** to the base of HBT **31**. The base of HBT **41** is connected through resistor **47** to the collector of HBT **43**, and the emitter is to ground.

Terminal Vpc is likewise connected through a series circuit of resistors **48** and **49** to the collector of HBT **42**. The node between resistors **48** and **49** is connected to terminal **V1800** of bias switching circuit **6**, and through resistor **37** of second biasing circuit **5** to the base of HBT **35**. The base of HBT **42** is connected through a series circuit of resistors **50** and **51** to terminal Vmod, and the emitter is to ground. Terminal Vmod is connected to the base of HBT **43** through resistor **53**, and to ground through resistor **54**. The collector of HBT **43** is connected to terminal Vpc through resistor **52**, and the emitter is to ground.

When 2.7 V is applied to terminal Vpc in a bias switching circuit **6** thus comprised, 3 V is applied to terminal Vmod and Vmod thus goes high, HBT **43** switches on. HBT **41** therefore switches off and HBT **42** switches on. When HBT **42** is on, voltage Vpc of terminal Vpc is voltage divided by resistors **48** and **49**. If the resistance of resistor **48** is R**48** and the resistance of resistor **49** is R**49**, the voltage at terminal **V1800** drops to {Vpc×R**49**/(R**48**+R**49**)}. As a result, HBTs **35** and **36** in the second biasing circuit **5** turn off.

Current also flows through resistor **45** and resistor **33** to the base of HBT **31** in first biasing circuit **3** because HBT **41** is off. As a result, bias dependent on voltage Vpc is supplied from the output of first biasing circuit **3** to the base of HBT **11** in first power amplifier **2**, and output power dependent on the voltage Vpc can be obtained from the output terminal **OUT1** of first power amplifier **2**.

If, for example, 2.7 V is then applied to terminal Vpc, and 0 V is applied to terminal Vmod so that terminal Vmod goes low, HBT **43** switches off; HBT **41** therefore switches on, and HBT **42** switches off. When HBT **41** is on, voltage Vpc at terminal Vpc is voltage divided by resistors **45** and **46**. If the resistance of resistor **45** is R**45** and the resistance of resistor **46** is R**46**, the voltage at terminal **V900** drops to {Vpc×R**46**/(R**45**+R**46**)}. As a result, HBTs **31** and **32** in the first biasing circuit **3** turn off.

Current also flows through resistor **48** and resistor **37** to the base of HBT **35** in second biasing circuit because HBT **41** is on. As a result, bias dependent on voltage Vpc is supplied from the output of second biasing circuit **5** to the base of HBT **21** in second power amplifier **4**, and output power dependent on the voltage Vpc can be obtained from the output terminal **OUT2** of second power amplifier **4**.

When voltage Vpc goes to 0 V, HBT **31** in first biasing circuit **3** and HBT **35** in second biasing circuit **5** turn off irrespective of the voltage at terminal Vmod, that is, regard-

less of the operating state of HBT **41** and HBT **42**. As a result, both first power amplifier **2** and second power amplifier **4** stop operating.

By thus using a bias switching circuit **6** of HBTs, a dual band system high frequency power amplifier **1** can be achieved using two chips, a GSM 900 chip comprising first power amplifier **2** and first biasing circuit **3**, and a GSM 1800 chip comprising second power amplifier **4** and second biasing circuit **5**, and the bias switching circuit **6** can be formed on either of these two chips.

The circuit current required for switching the bias switching circuit **6** is supplied from terminal Vpc, and the current supplied from terminal Vpc increases compared with a conventional bias switching circuit comprising silicon elements. The increase can be controlled by optimizing the values (Ra+Rb) and Ra where R**45**=R**48**=Ra, and R**46**=R**49**=Rb. For example, when first biasing circuit **3** is operating and second biasing circuit **5** is stopped, the voltage drop at resistor **45** will be (I1×Ra) where I1 is the current flowing to resistor **45**, and the voltage drop at resistor **48** will be {Vpc×Ra/(Ra+Rb)}. It is therefore possible by optimizing the values of Ra and Rb to minimize the current supplied from terminal Vpc within the range where no problems will occur for practical purposes.

FIG. **3**A to FIG. **3**C are graphs showing an operating characteristic of the bias switching circuit shown in FIG. **2** under various conditions. FIG. **3**A shows the relationship between current Ipc supplied from terminal Vpc, and voltages V**900** and V**1800** at terminal V**900** and terminal V**1800** in response to a voltage Vpc, when Vmod is 3 V. FIG. **3**B shows the same when Vmod is 0 V. FIG. **3**C shows the relationship between current I**900** output from terminal V**900**, current I**1800** output from terminal V**1800**, and voltages V**900** and V**1800** at terminal V**900** and terminal V**1800** in response to a voltage Vmod, when Vpc is 2.7 V

It will be known from FIGS. **3**A to **3**C that when Vpc is 2.7 V, the current supply can be switched between first power amplifier **2** and second power amplifier **4** with a current Ipc of approximately 3.5 mA.

It is to be noted that while the present invention has been described above with reference to a single-stage power amplifier in FIG. **1** and FIG. **2**, the present invention shall not be so limited and can obviously be applied to a multi-stage power amplifier. FIG. **4** is a typical circuit diagram showing an alternative version of the high frequency power amplifier for a dual band system shown in FIG. **1**. It is to be noted that a high frequency power amplifier for a dual band system having a three-stage power amplifier is shown in FIG. **4**, and that like parts are indicated by the same reference numerals. Further description of such like parts is omitted below where only the differences between the high frequency power amplifier shown in FIG. **1** and that in FIG. **4** are described.

The high frequency power amplifier shown in FIG. **4** differs from that in FIG. **1** in that the first power amplifier **2** and second power amplifier **4** are each a three-stage power amplifier. The circuit design of the first biasing circuit **3** and second biasing circuit **5** in FIG. **1** is thus also changed. The first power amplifier **2** in FIG. **1** is thus shown in FIG. **4** and referred to below as first power amplifier **2**A, the first biasing circuit **3** as first biasing circuit **3**A, the second power amplifier **4** as second power amplifier **4**A, the second biasing circuit **5** as second biasing circuit **5**A, and the high frequency power amplifier **1** as high frequency power amplifier **1**A.

As shown in FIG. **4**, first power amplifier **2**A comprises HBTs **11***a* to **11***c* for power amplifying; input matching circuit **12**; and interstage matching circuits **61** and **62**.

HBT **11***a* power amplifies a high frequency signal input from input terminal IN**1** through input matching circuit **12**, and HBT **11***b* power amplifies the high frequency signal amplified by HBT **11***a* and input thereto through interstage matching circuit **61**. HBT **11***c* power amplifies the high frequency signal amplified by HBT **11***b* and input thereto through interstage matching circuit **62**. The amplified high frequency signal is then output through output matching circuit **7** from output terminal OUT**1**.

Bias is supplied to the collector of HBTs **11***a* to **11***c* from corresponding collector biasing circuits **9***a* to **9***c*. Bias is also supplied to the base of HBTs **11***a* to **11***c* from first biasing circuit **3**A.

Second power amplifier **4**A likewise comprises HBTs **21***a* to **21***c* for power amplifying; input matching circuit **22**; and interstage matching circuits **65** and **66**.

HBT **21***a* power amplifies a high frequency signal input from input terminal IN**1** through input matching circuit **22**, and HBT **21***b* power amplifies the high frequency signal amplified by HBT **21***a* and input thereto through interstage matching circuit **65**. HBT **21***c* power amplifies the high frequency signal amplified by HBT **21***b* and input thereto through interstage matching circuit **66**. The amplified high frequency signal is then output through output matching circuit **8** from output terminal OUT**2**.

Bias is supplied to the collector of HBTs **21***a* to **21***c* from corresponding collector biasing circuits **10***a* to **10***c*. Bias is also supplied to the base of HBTs **21***a* to **21***c* from second biasing circuit **5**A.

As with the high frequency power amplifier **1** shown in FIG. **1** and FIG. **2**, bias switching circuit **6** controls operation of the first biasing circuit **3**A and second biasing circuit **5**A. More specifically, bias switching circuit **6** outputs a signal V**900**, which is a control signal for the first biasing circuit **3**A, or a signal V**1800**, which is a control signal for the second biasing circuit **5**A, to exclusively select and operate first biasing circuit **3**A or second biasing circuit **5**A based on the signal level of a two-value input signal Vmod. Based on the signal level of an input signal Vpc applied to the Vpc terminal from an external source, bias switching circuit **6** also outputs signal V**900** or signal V**1800** to adjust the output level of the signal passed from output terminals OUT**1** and OUT**2**.

FIG. **5** is a typical circuit diagram of first biasing circuit **3**A, second biasing circuit **5**A, and bias switching circuit **6** shown in FIG. **4**. It is to be noted that like parts in FIG. **5** and FIG. **2** are indicated by the same reference numerals. Further description of such like parts is omitted below where only the differences between FIG. **5** and FIG. **2** are described.

FIG. **5** differs from FIG. **2** in that a biasing circuit identical to the first biasing circuit **3** shown in FIG. **2** is disposed for each of the HBTs **11***a* to **11***c* in the first power amplifier **2**A, and a biasing circuit identical to second biasing circuit **5** in FIG. **2** is disposed for each of the HBTs **21***a* to **21***c* in the second power amplifier **4**A.

As shown in FIG. **5**, first biasing circuit **3**A comprises HBTs **31***a* to **31***c* and **32***a* to **32***c*, and resistors **33***a* to **33***c* and **34***a* to **34***c*. Resistors **33***a* to **33***c* are the base resistance of the corresponding HBT **31***a* to **31***c*, and resistors **34***a* to **34***c* are the base resistance of the corresponding HBT **32***a* to **32***c*. It is to be noted that HBTs **31***a* to **31***c* correspond to HBT **31** in FIG. **2**, HBTs **32***a* to **32***c* to HBT **32** in FIG. **2**, resistors **33***a* to **33***c* to resistor **33** in FIG. **2**, and resistors **34***a* to **34***c* to resistor **34** in FIG. **2**. Connections thereto are also the same as shown in the first biasing circuit **3** in FIG. **2**, and further description thereof is thus omitted below.

The node between the emitter of HBT **31***a* and the collector of HBT **32***a* is connected to the base of HBT **11***a* in first power amplifier **2**A. The node between the emitter of HBT **31***b* and the collector of HBT **32***b* is connected to the base of HBT **11***b* in first power amplifier **2**A. The node between the emitter of HBT **31***c* and the collector of HBT **32***c* is likewise connected to the base of HBT **11***c* in the first power amplifier **2**A.

The second biasing circuit **5**A likewise comprises HBTs **35***a* to **35***c* and **36***a* to **36***c*, and resistors **37***a* to **37***c* and **38***a* to **38***c*. Resistors **37***a* to **37***c* are the base resistance of the corresponding HBT **35***a* to **35***c*, and resistors **38***a* to **38***c* are the base resistance of the corresponding HBT **36***a* to **36***c*. It is to be noted that HBTs **35***a* to **35***c* correspond to HBT **35** in FIG. **2**, HBTs **36***a* to **36***c* to HBT **36** in FIG. **2**, resistors **37***a* to **37***c* to resistor **37** in FIG. **2**, and resistors **38***a* to **38***c* to resistor **38** in FIG. **2**. Connections thereto are also the same as shown in the second biasing circuit **5** in FIG. **2**, and further description thereof is thus omitted below.

The node between the emitter of HBT **35***a* and the collector of HBT **36***a* is connected to the base of HBT **21***a* in second power amplifier **4**A. The node between the emitter of HBT **35***b* and the collector of HBT **36***b* is connected to the base of HBT **21***b* in second power amplifier **4**A. The node between the emitter of HBT **35***c* and the collector of HBT **36***c* is likewise connected to the base of HBT **21***c* in the second power amplifier **4**A.

The bases of HBT **31***a* to **31***c* are connected through corresponding resistors **33***a* to **33***c* to the **V900** terminal of bias switching circuit **6**. The bases of HBT **35***a* to **35***c* are connected through corresponding resistors **37***a* to **37***c* to the **V1800** terminal of bias switching circuit **6**.

Operation of this first biasing circuit **3**A is identical to the operation of the first biasing circuit **3** shown in FIG. **2**, operation of second biasing circuit **5**A is identical to second biasing circuit **5** in FIG. **2**, and operation of the bias switching circuit **6** with respect to first biasing circuit **3**A and second biasing circuit **5**A is also the same as described above with reference to FIG. **2**. Further description thereof is thus omitted below.

By thus using a bias switching circuit **6** of HBTs, a dual band system high frequency power amplifier **1**A can be achieved using two chips, a GSM 900 chip comprising first power amplifier **2**A and first biasing circuit **3**A, and a GSM 1800 chip comprising second power amplifier **4**A and second biasing circuit **5**A, and the bias switching circuit **6** can be formed on either of these two chips.

FIG. **6** is a circuit diagram of a further alternative embodiment of the first biasing circuit **3**A, second biasing circuit **5**A, and bias switching circuit **6** shown in FIG. **4**. It is to be noted that like parts in FIG. and FIG. **6** are indicated by the same reference numerals. Further description of such like parts is omitted below where only the differences between FIG. **5** and FIG. **6** are described.

The circuits shown in FIG. **6** differ from those in FIG. **5** in that base resistors **33***a* to **33***c* of the first biasing circuit **3**A in FIG. **5**, and base resistors **37***a* to **37***c* in the second biasing circuit **5**A in FIG. **5**, are omitted; and a series circuit of resistors **71***a* to **71***c* is inserted between resistors **45** and **46**, and a series circuit of resistors **72***a* to **72***c* is inserted between resistors **48** and **49**, in the bias switching circuit **6** in FIG. **5**. Resistors **45**, **46**, **48**, and **49** in FIG. **5** are therefore shown in FIG. **6** and referred to below as resistors **45**B, **46**B, **48**B, and **49**B; first biasing circuit **3**A as first biasing circuit **3**B; second biasing circuit **5**A as second biasing circuit **5**B; and bias switching circuit **6** as bias switching circuit **6**B.

As noted above and shown in FIG. **6**, a series circuit of resistors **71***a* to **71***c* is inserted between resistors **45**B and **46**B of the bias switching circuit **6**B, and the node between resistor **46**B and resistor **71***a* is connected to the base of HBT **31***a* through intervening output terminal **V900***a* of bias switching circuit **6**B. The node between resistor **71***a* and resistor **71***b* is connected to the base of HBT **31***b* through output terminal **V900***b* of bias switching circuit **6**B. The node between resistor **71***b* and resistor **71***c* is connected to the base of HBT **31***c* through output terminal **V900***c* of bias switching circuit **6**B.

A series circuit of resistors **72***a* to **72***c* is likewise inserted between resistors **48**B and **49**B of bias switching circuit **6**B. The node between **49**B and resistor **72***a* is connected to the base of HBT **35***a* through output terminal **V1800***a* of bias switching circuit **6**B; the node between resistor **72***a* and resistor **72***b* is connected to the base of HBT **35***b* through output terminal **V1800***b*; and the node between resistor **72***b* and resistor **72***c* is connected to the base of HBT **35***c* through output terminal **V1800***c*.

Voltage drop in the base bias voltage from terminal Vpc due to HBT **31***c* through which the highest base current flows when first biasing circuit **3**B operates, or HBT **35***c* through which the highest base current flows when second biasing circuit **5**B operates can therefore be minimized. This is effective when all of the circuits of the dual band system high frequency power amplifier are integrated into a single chip.

FIG. **7** is a circuit diagram of a further alternative embodiment of the first biasing circuit **3**A, second biasing circuit **5**A, and bias switching circuit **6** shown in FIG. **4**. It is to be noted that like parts in FIG. **5**, FIG. **6** and FIG. **7** are indicated by the same reference numerals. Further description of such like parts is omitted below where only the differences between FIG. **7** and FIG. **6** are described.

The bias switching circuit **6**C shown in FIG. **7** differs from the bias switching circuit **6**B in FIG. **6** in that resistors **74**, **75***a* to **75***c*, and **76***a* to **76***c* are provided in place of resistors **45**B, **46**B, and **71***a* to **71***c*; and resistors **77**, **78***a* to **78***c*, and **79***a* to **79***c* are provided in place of resistors **48**B, **49**B, and **72***a* to **72***c*.

As shown in FIG. **7**, a series circuit of resistors **74**, **75***a* to **75***c*, and **76***a* is connected between terminal Vpc of bias switching circuit **6**C and the collector of HBT **41**. The node between resistors **75***a* and **76***a* is connected to the base of HBT **31***a* through output terminal **V900***a* of bias switching circuit **6**C; the node between resistors **75***a* and **75***b* is connected to the base of HBT **31***b* through output terminal **V900***b* of bias switching circuit **6**C; and the node between resistors **75***b* and **75***c* is connected to the base of HBT **31***c* through output terminal **V900***c*. Note, further, that resistor **76***b* is connected between terminal **V900***b* and the collector of HBT **41**, and resistor **76***c* is connected between terminal **V900***c* and the collector of HBT **41**.

A series circuit of resistors **77**, **78***a* to **78***c*, and **79***a* is similarly connected between terminal Vpc of bias switching circuit **6**C and the collector of HBT **42**. The node between resistors **78***a* and **79***a* is connected to the base of HBT **35***a* through output terminal **V1800***a* of bias switching circuit **6**C; the node between resistors **78***a* and **78***b* is connected to the base of HBT **35***b* through output terminal **V1800***b* of bias switching circuit **6**C; and the node between resistors **78***b* and **78***c* is connected to the base of HBT **35***c* through output terminal **V1800***c*. Note, further, that resistor **79***b* is connected between terminal **V1800***b* and the collector of HBT **42**, and resistor **79***c* is connected between terminal **V1800***c* and the collector of HBT **42**.

Voltage drop in the base bias voltage from terminal Vpc due to HBT **31***c* through which the highest base current flows when first biasing circuit **3**C operates, or HBT **35***c* through which the highest base current flows when second biasing circuit **5**C operates can therefore be minimized. This is effective when all of the circuits of the dual band system high frequency power amplifier are integrated into a single chip. It is also possible to optimize the current supplied to the base of HBTs **31***a* to **31***c* and **35***a* to **35***c* by controlling the resistance ratio of the resistors, and it is thereby possible to optimize current Ipc.

The bias switching circuit for switching operation between a first biasing circuit and a second biasing circuit, each made with HBTs, is thus made with readily available AlGaAs or GaAs HBTs in a high frequency power amplifier according to this first preferred embodiment of the present invention, and three or more HBTs are connected in series to assure that the total of each base-emitter voltage Vbe does not exceed 3 V. It is therefore possible to construct a dual band system high frequency power amplifier using HBTs of which the on voltage of the base-emitter voltage Vbe is high (1.35 V, for example). As a result, this high frequency power amplifier can be integrated into an MMIC that can operate reliably even at a 3-V low supply voltage, and the manufacturing process can therefore be simplified.

Embodiment 2

If an overvoltage is applied to input terminal Vpc of the bias switching circuits in the various versions of the first embodiment described above, this overvoltage is also applied to the first and second biasing circuit. It is alternatively possible, however, to dispose an overvoltage protection circuit to the bias switching circuit so that an overvoltage applied to the input terminal Vpc is not applied to the first and second biasing circuits. A dual band system high frequency power amplifier so comprised is described below as the second preferred embodiment of the present invention.

FIG. **8** is a typical circuit diagram showing the first biasing circuit, second biasing circuit, and bias switching circuit in a dual band system high frequency power amplifier according to this second preferred embodiment of the present invention. It is to be noted that a typical circuit diagram of a high frequency power amplifier according to this second embodiment of the invention is the same as that shown in FIG. **1** except for changing the reference numeral for the bias switching circuit, and further description is therefore omitted below.

In addition, like parts in FIG. **8** and FIG. **2** are indicated by the same reference numerals. Further description of such like parts is omitted below where only the differences between FIG. **8** and FIG. **2** are described.

The bias switching circuit **84** shown in FIG. **8** differs from the bias switching circuit **6** in FIG. **2** in the addition of protection circuits **81** and **82**.

As shown in FIG. **8**, this bias switching circuit **84** comprises HBT **41** to **43**, resistors **45** to **54**, and protection circuits **81** and **82**.

Protection circuit **81** comprises HBT **91** and resistors **92** and **93**, and forms a Vbe multiplier. Resistors **92** and **93** are connected in series between terminal Vpc and ground. The collector of HBT **91** is connected to a node between resistor **45** and resistor **46**, that is, to terminal V**900**; the base is connected to a node between resistor **92** and resistor **93**; and the emitter is to ground.

Protection circuit **82** likewise comprises HBT **95** and resistors **96** and **97**, and forms a Vbe multiplier. Resistors **96** and **97** are connected in series between terminal Vpc and ground. The collector of HBT **95** is connected to a node between resistor **48** and resistor **49**, that is, to terminal V**1800**; the base is connected to a node between **96** and resistor **97**; and the emitter is to ground.

In a bias switching circuit **84** thus comprised, the on voltage of HBT **91** in protection circuit **81** is multiplied {(R**92**+R**93**)/R**93**} where the resistance of resistor **92** is R**92** and the resistance of resistor **93** is R**93**. For example, if the on voltage of HBT **91** is approximately 1.3 V, and resistances R**92** and R**93** are set so that {(R**92**+R**93**)/R**93**}=2.3, HBT **91** will turn on when voltage Vpc goes to 3 V, and collector current I**4** will flow to HBT **91**. A voltage drop thus occurs at resistor **45**, controlling the voltage at terminal V**900** to 3 V or less so that when an overvoltage is applied to terminal Vpc, the overvoltage is prevented from being directly applied to first biasing circuit **3**, and is thus prevented from being applied to the first power amplifier **2**.

The on voltage of HBT **95** in protection circuit **82** is likewise multiplied {(R**96**+R**97**)/R**97**} where the resistance of resistor **96** is R**96** and the resistance of resistor **97** is R**97**. For example, if the on voltage of HBT **95** is approximately 1.3 V, and resistances R**96** and R**97** are set so that {(R**96**+R**97**)/R**97**}=2.3, HBT **95** will turn on when voltage Vpc goes to 3 V, and collector current I**5** will flow to HBT **95**. A voltage drop thus occurs at resistor **48**, controlling the voltage at terminal V**1800** to 3 V or less so that when an overvoltage is applied to terminal Vpc, the overvoltage is prevented from being directly applied to second biasing circuit **5**, and is thus prevented from being applied to the second power amplifier **4**.

FIG. **9** is a graph of the operating characteristics of the bias switching circuit **84** shown in FIG. **8**. As will be known from FIG. **9**, the voltage at terminal V**900** increases proportionally to voltage Vpc when voltage Vpc<3 V, and is controlled to 3 V or less when voltage Vpc≧3 V.

It is to be noted that this preferred embodiment as shown in FIG. **8** adds protection circuits **81** and **82** to the bias switching circuit **6** shown in FIG. **2**, but the present invention shall not be so limited. More specifically, protection circuits **81** and **82** can be alternatively added to any of the bias switching circuits shown in FIG. **5**, FIG. **6**, and FIG. **7**. The bias switching circuit will be the same as shown in FIG. **8** when the protection circuits **81** and **82** are added to the bias switching circuit in FIG. **5**. However, when added to bias switching circuit **6**B in FIG. **6**, the collector of HBT **91** in protection circuit **81** is connected to a node between resistors **45**B and **71***c*, and the collector of HBT **95** in protection circuit **82** is connected to a node between resistors **48**B and **72***c*. When these protection circuits are added to the bias switching circuit **6**C in FIG. **7**, the collector of HBT **91** in protection circuit **81** is connected to a node between resistors **74** and **75***c*, and the collector of HBT **95** in protection circuit **82** is connected to a node between resistors **77** and **78***c*.

As described above, a high frequency power amplifier according to this second preferred embodiment of the present invention has protection circuits **81** and **82** forming Vbe multipliers in the bias switching circuit **84** so that when an overvoltage is applied to terminal Vpc, the overvoltage is not passed and applied to terminal V**900** or V**1800**.

Therefore, when a high frequency power amplifier according to this preferred embodiment is used in a system such as a GSM mobile phone in which the power source of the power amplifier is connected directly to a battery power source, it is possible to protect the first power amplifier **2** and second power amplifier **4** from thermal runaway when, for

example, terminal Vpc accidentally directly contacts the battery for some reason. Heat damage to the high frequency power amplifier or a mobile phone in which this high frequency power amplifier is used can thus also be prevented, and these protective and safety benefits can be achieved in addition to the benefits obtained by a high frequency power amplifier according to the first embodiment of the invention.

Although the present invention has been described in connection with the preferred embodiments thereof with reference to the accompanying drawings, it is to be noted that various changes and modifications will be apparent to those skilled in the art. Such changes and modifications are to be understood as included within the scope of the present invention as defined by the appended claims, unless they depart therefrom.

What is claimed is:

1. A high frequency power amplifier for a dual band system, comprising:

first and second power amplifiers, each power amplifier comprising at least one power amplifying heterojunction bipolar transistor (HBT);

first and second biasing circuits providing a bias for the first and second power amplifiers, respectively, each biasing circuit comprising an HBT; and

a bias switching circuit for exclusive switching between the first and second biasing circuits in accordance with first and second signals input to the bias switching circuit, the bias switching circuit comprising:

a first switching circuit comprising a first HBT for controlling output of the first signal to the second biasing circuit;

a second switching circuit comprising a second HBT for controlling output of the first signal to the first biasing circuit; and

a third switching circuit comprising a third HBT for controlling operation of the second switching circuit according to the second signal for controlling operation of the first switching circuit, for exclusive selection and operation of the first and second switching circuits wherein the first power amplifier and the first biasing circuit are integrated circuits integrated in a first semiconductor substrate, the second power amplifier and the second biasing circuit are integrated circuits integrated in a second semiconductor substrate, and the biasing circuit is an integrated circuit integrated with other circuits on one of the first and second semiconductor substrates.

2. The high frequency power amplifier according to claim **1**, wherein

each of the first and second switching circuits comprises a series resistance circuit having a plurality of resistors connected in series for voltage dividing a signal voltage, and;

the first and second HBTs are ground-connecting HBTs for controlling connection of the series resistance circuit to ground, and for outputting a control signal to the second and first biasing circuits, respectively, from a node between resistors in the series resistance circuit.

3. The high frequency power amplifier according to claim **2**, wherein:

each of the first and second power amplifiers is a multistage power amplifier including a plurality of power amplifying HBTs,

each of the first and second biasing circuits has a circuit for supplying a bias to each of the power amplifying HBTs of a corresponding one of the first and second power amplifiers, and

the first and second switching circuits output control signals to the second and first biasing circuits, respectively, so that a bias current gradually increases from a bias supplied to a first stage power amplifying HBT to a bias supplied to a last stage power amplifying HBT.

4. The high frequency power amplifier according to claim **2**, wherein each of the first and second switching circuits comprises a signal level adjusting resistor for adjusting the control signal applied to the corresponding one of the first and second biasing circuits, the signal level adjusting resistor being connected to a node between resistors in the series resistance circuit and to a node between the series resistance circuit and the ground-connecting HBTs.

5. The high frequency power amplifier according to claim **2**, wherein the first, second, and third HBTs have respective bases and the third HBT of the third switching circuit controls a bias supplied to the base of the second HBT of the second switching circuit according to the second signal.

6. The high frequency power amplifier according to claim **1**, wherein each of the first and second switching circuits comprise protection circuits for protecting the first and second biasing circuits, respectively, from an overvoltage applied to a terminal for receiving the first signal.

7. The high frequency power amplifier according to claim **6**, wherein each protection circuit is a Vbe multiplier comprising an HBT.

8. The high frequency power amplifier according to claim **1**, wherein each of the first, second, and third HBTs includes a respective base and collector, the second signal is supplied to respective bases of the first and third HBTs of the first and third switching circuits, and the signal produced at the collector of the third HBT of the third switching circuit is supplied to the base of the second HBT of the second switching circuit.

9. A high frequency power amplifier for a dual band system, comprising:

first and second power amplifiers, each power amplifier comprising at least one power amplifying heterojunction bipolar transistor (HBT);

first and second biasing circuits providing a bias for the first and second power amplifiers, respectively, each biasing circuit comprising an HBT; and

a bias switching circuit for exclusive switching between the first and second biasing circuits in accordance with first and second signals input to the bias switching circuit, the bias switching circuit comprising:

a first switching circuit comprising a first HBT for controlling output of the first signal which controls operation of the second biasing circuit;

a second switching circuit comprising a second HBT for controlling output of the first signal to the first biasing circuit, wherein each of the first and second switching circuits comprises a series resistance circuit having a plurality of resistors connected in series for voltage dividing a signal voltage, and the first and second HBTs are ground-connecting HBTs for controlling connection of the series resistance circuit to ground, and for outputting a control signal to the second and first biasing circuits, respectively, from a node between resistors in the series resistance circuit; and

a third switching circuit comprising a third HBT for controlling operation of the second switching circuit according to the second signal for controlling opera-

tion of the first switching circuit, for exclusive selection and operation of the first and second switching circuits.

10. The high frequency power amplifier according to claim **9**, wherein:

each of the first and second power amplifiers is a multistage power amplifier including a plurality of power amplifying HBTs,

each of the first and second biasing circuits has a circuit for supplying a bias to each of the power amplifying HBTs of a corresponding one of the first and second power amplifiers, and

the first and second switching circuits output control signals to the second and first biasing circuits, respectively, so that a bias current gradually increases from a bias supplied to a first stage power amplifying HBT to a bias supplied to a last stage power amplifying HBT.

11. The high frequency power amplifier according to claim **9**, wherein each of the first and second switching circuits comprises a signal level adjusting resistor for adjusting the control signal applied to the corresponding one of the first and second biasing circuits, the signal level adjusting resistor being connected to a node between resistors in the series resistance circuit and to a node between the series resistance circuit and the ground-connecting HBTs.

12. The high frequency power amplifier according to claim **9**, wherein the first, second, and third HBTs have respective bases and the third HBT of the third switching circuit controls a bias supplied to the base of the second HBT of the second switching circuit according to the second signal.

13. The high frequency power amplifier according to claim **9**, wherein the first and second switching circuits comprise protection circuits for protecting the first and second biasing circuits, respectively, from an overvoltage applied to a terminal for receiving the first signal.

14. The frequency power amplifier according to claim **13**, wherein each protection circuit is a Vbe multiplier comprising an HBT.

15. The high frequency power amplifier according to claim **9**, wherein each of the first, second, and third HBTs includes a respective base and collector, the second signal is supplied to respective bases of the first and third HBTs of the first and third switching circuits, and the signal produced at the collector of the third HBT of the third switching circuit is supplied to the base of the second HBT of the second switching circuit.

16. A high frequency power amplifier for a dual band system, comprising:

first and second power amplifiers, each power amplifier comprising at least one power amplifying heterojunction bipolar transistor (HBT);

first and second biasing circuits providing a bias for the first and second power amplifiers, respectively, each biasing circuit comprising an HBT; and

a bias switching circuit for exclusive switching between the biasing circuits in accordance with first and second signals input to the bias switching circuit, the bias switching circuit comprising:

a first switching circuit comprising an HBT for controlling output of the first signal to the first biasing circuit;

a second switching circuit comprising an HBT for controlling output of the first signal to the second biasing circuit; and

a third switching circuit comprising an HBT for controlling operation of the second switching circuit according to the second signal for controlling operation of the first switching circuit for exclusive selection and operation of the first and second switching circuits, wherein each of the first and second switching circuits comprises a protection circuit for protecting a corresponding one of the first and second biasing circuits from an overvoltage applied to a terminal for receiving the first signal.

17. The frequency power amplifier according to claim **16**, wherein each protection circuit is a Vbe multiplier comprising an HBT.

18. A high frequency power amplifier for a dual band system, comprising:

first and second power amplifiers, each power amplifier comprising at least one power amplifying heterojunction bipolar transistor (HBT);

first and second biasing circuits providing a bias for the first and second power amplifiers, respectively, each biasing circuit comprising an HBT; and

a bias switching circuit for exclusive switching between the biasing circuits in accordance with first and second signals input to the bias switching circuit, the bias switching circuit comprising:

a first switching circuit comprising an HBT for controlling output of the first signal to the first biasing circuit;

a second switching circuit comprising an HBT for controlling output of the first signal to the second biasing circuit; and

a third switching circuit comprising an HBT for controlling operation of the second switching circuit according to the second signal for controlling operation of the first switching circuit for exclusive selection and operation of the first and second switching circuits, wherein each of the HBTs includes a respective base and collector, the second signal is supplied to respective bases of the HBTs of the first and third switching circuits, and the signal produced at the collector of the HBT of the third switching circuit is supplied to the base of the HBT of the first switching circuit.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,297,694 B1
APPLICATION NO. : 09/448519
DATED : October 2, 2001
INVENTOR(S) : Kazuya Yamamoto

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 13, line 46, change “biasing” to --bias switching--.

Signed and Sealed this
Sixteenth Day of August, 2011

David J. Kappos

David J. Kappos
Director of the United States Patent and Trademark Office