

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KANGXI COMMUNICATION TECHNOLOGIES
Petitioner,

v.

SKYWORKS SOLUTIONS, INC.,
Patent Owner.

U.S. Patent No. 7,409,200
Issue Date: AUGUST 5, 2008

Title: MODULE INTEGRATION INTEGRATED CIRCUITS

Inter Partes Review No.: IPR2025-00912

**PETITION FOR *INTER PARTES* REVIEW OF PATENT NO. 7,409,200
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. §§ 42.1-.80, 42.100-.107**

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PETITIONER'S EXHIBIT LIST

EX-1001	U.S. Patent No. 7,409,200 to Derbyshire et al. ("200 Patent"), Filing Date of June 2, 2004
EX-1002	Prosecution History of U.S. Patent No. 7,409,200
EX-1003	Declaration of Dr. Ayman Fayed
EX-1004	<i>Curriculum Vitae</i> of Dr. Ayman Fayed
EX-1005	U.S. Patent Publication No. 2003/0017809 A1 to Garlepp et al. ("Garlepp"), Filing Date of February 19, 2002 and Publication Date of January 23, 2003
EX-1006	R. Magoon et al., "A Single-Chip Quad-Band (850/900/1800/1900 MHz Direct Conversion GSM/GPRS RF Transceiver with Integrated VCOs and Fractional-N Synthesizer," published in IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 37, No. 12, pp. 1710-1720, December 2002 (" <i>Magoon</i> ")
EX-1007	E. Ngompe et al., "Architecture and Performance Overview of a Highly Integrated 13x13mm Single-Package Radio (SPR) Module for Dualband EGSM900 / GSM1800 Applications," published in 2003 IEEE Radio Frequency Integrated Circuits Symposium, pp. 387-390 (" <i>Ngompe</i> ")
EX-1008	U.S. Patent Publication No. 2003/0089998 A1 to Chan et al. (" <i>Chan</i> "), Filing Date of November 9, 2001, Publication Date of May 15, 2003
EX-1009	P. Wambacq et al., "A single-package solution for wireless transceivers," published in Design, Automation and Test in Europe Conference and Exhibition, 1999 (" <i>Wambacq</i> ")
EX-1010	L.E. Larson, "Integrated Circuit Technology Options for RFIC's—Present Status and Future Directions," published in IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 33, No. 3, pp. 387-399, March 1998 (" <i>Larson</i> ")
EX-1011	J. Ryckaert et al., "Single-package 5GHz WLAN RF module with embedded patch antenna and 20dBm power amplifier," published in 2003 MTT-S Digest, pp. 1037-1040 (" <i>Ryckaert</i> ")

EX-1012	U.S. Patent Publication No. 2003/0139147 A1 to Shi (“ <i>Shi</i> ”), Filing Date of March 21, 2002, and Publication Date of July 24, 2003.
EX-1013	U.S. Patent No. 5,898,909 to Yoshihara et al (“ <i>Yoshihara</i> ”), Filing Date of September 27, 1996, Issue Date of April 27, 1999
EX-1014	European Patent Application Publication No. EP 0 632 497 A2 to Pedder (“ <i>Pedder</i> ”), Filing Date of June 16, 1994, Publication Date of January 4, 1995
EX-1015	U.S. Patent No. 6,297,694 to Yamamoto (“ <i>Yamamoto</i> ”), Filing Date of November 24, 1999, Issue Date of October 2, 2001
EX-1016	WILEY ELECTRICAL AND ELECTRONICS ENGINEERING DICTIONARY (2004), p. 707 (signal conditioning)
EX-1017	Declaration of Ingrid Hsieh-Yee, Ph.D.

I. INTRODUCTION

Pursuant to 35 U.S.C. §§311 *et seq.* and 37 C.F.R. §42.1 *et seq.*, Kangxi Communications Technologies (“Petitioner”) petitions for *inter partes* review of Patent No. 7,409,200 (the “’200 Patent”) (EX-1001). Petitioner submits that claims 1-2, 4, 6, 10-15, 18-20, 23-26, and 29-31 (the “Challenged Claims”) of the ’200 Patent are unpatentable under (pre-AIA) 35 U.S.C. §103(a) in view of the prior art discussed herein. This Petition demonstrates by a preponderance of the evidence that there is a reasonable likelihood that Petitioner will prevail with respect to at least one of the Challenged Claims. Accordingly, Petitioner requests that the Board institute an IPR of the ’200 Patent pursuant to 37 C.F.R. §42.108.

II. OVERVIEW

The ’200 Patent is directed to the problem of providing a high-performance, compact electronic module that incorporates electronic circuits for radio frequency (RF) front-end applications.

In general, an RF front-end module is a collection of components that interfaces with the antenna and provides the initial processing of incoming radio signals (reception) and/or the final amplification of outgoing radio signals (transmission). A front-end module that handles both reception and transmission is referred to as a “transceiver.” The module’s components include signal conditioning circuits with specialized components, such as low noise amplifiers

(LNAs) in the receive signal path and power amplifiers in the transmit signal path.

The components also include ancillary circuits (e.g., voltage regulators) for use by the signal conditioning circuits. RF front-end modules can include circuitry to support multiple different RF standards or frequency bands. EX-1003, ¶27.

According to the '200 Patent, one problem associated with a multi-standard RF module is that separate circuitry is needed for each standard, thus increasing the component count. This, in turn, increases cost, reduces yield and durability, and increases module size. EX-1001 1:36-55. The '200 Patent describes another problem: the semiconductor technology best suited for integrating some components of the circuitry often is not suited for integrating other components. Thus, RF module designers invariably included multiple different semiconductor dies in their modules. EX-1001 2:12-27; 4:3-13; EX-1003, ¶28.

The '200 Patent purports to address these problems by providing a technique for partitioning the circuitry into functional portions along a signal path, and then integrating the different portions within discrete semiconductor dies.¹ The dies are

¹ The '200 Patent uses the terms “**die**” and “**semiconductor** substrate” as synonyms. *See* EX-1001, 4:40-41, 54; 6:49-50, 64 (referring to component 511 as both a “semiconductor substrate” and “semiconductor die”). This usage should not be confused with the “substrate” recited in the claims, which references a substrate

mounted on a common substrate within the module and electrically interconnected to complete the signal path. An example embodiment is an RF front-end module in which the partitioned circuitry is the PA circuitry for amplifying RF signals, which the '200 Patent generally refers to as a “signal conditioning circuit.” EX-1003, ¶29.

An embodiment of a module 500 implementing the '200 Patent's circuit partitioning and integration scheme is illustrated in FIG. 5:

in the context of a package substrate that supports dies. *See* '200 Patent, Claim 1 (claiming: “a **substrate** for supporting the first and second **integrated circuit semiconductor** dies”), Fig. 4 (step 404: “bonding the first and second **dies** to a **common substrate**”).

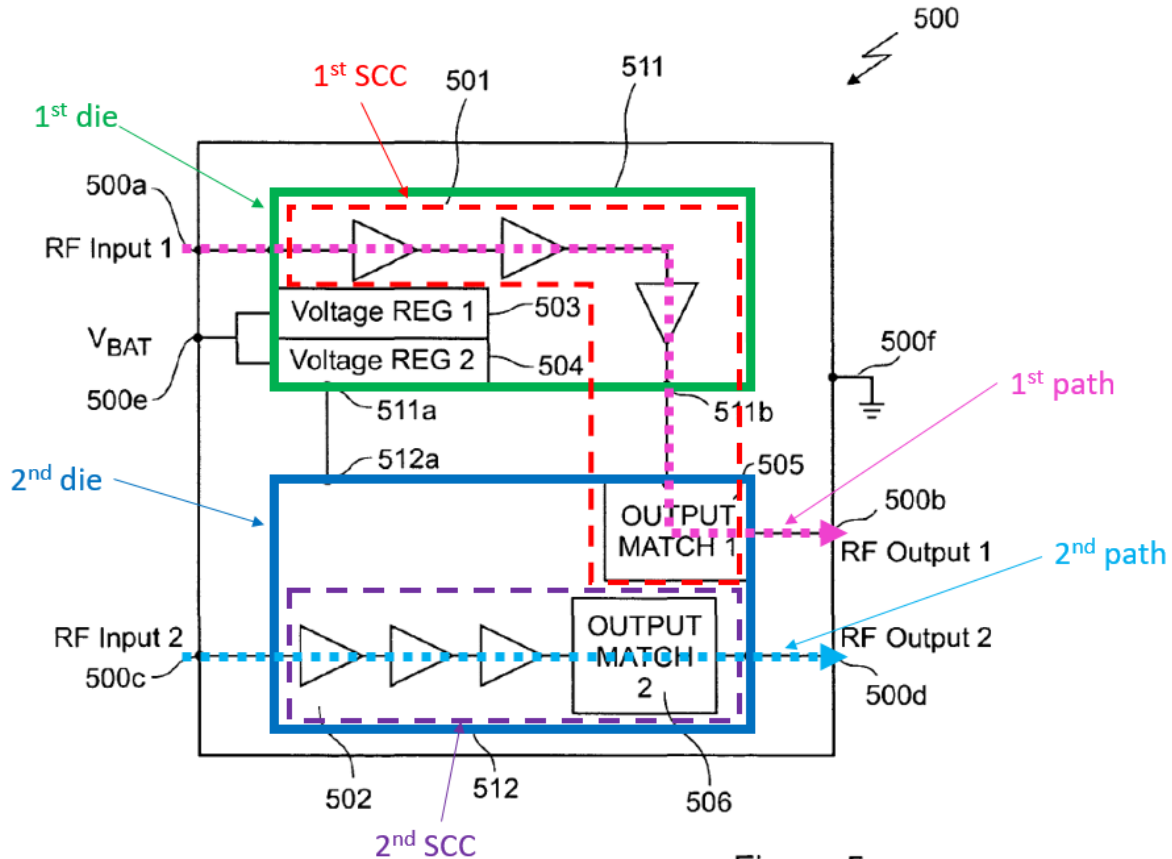


Figure 5

EX-1001, FIG. 5 (annotated); EX-1003, ¶30.

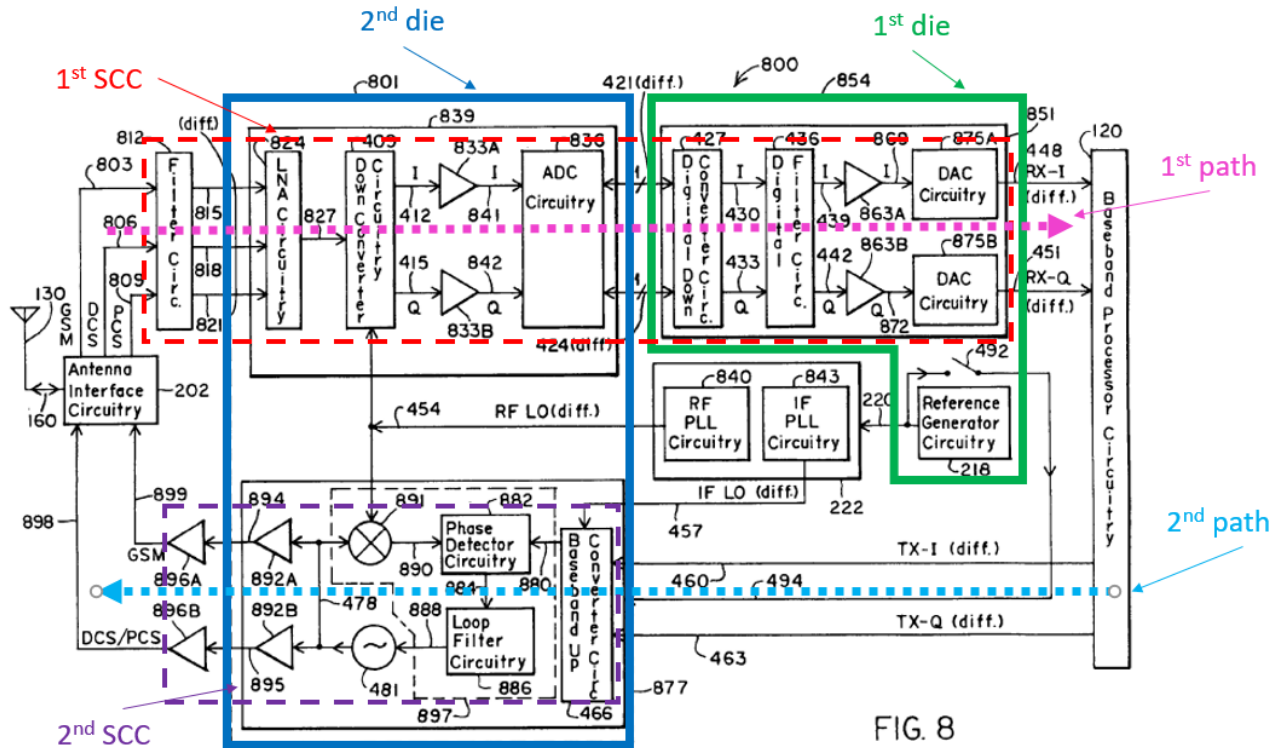
Module 500 includes two signal conditioning circuits (“SCCs”): a first SCC 501, 505 disposed along a first signal path; and a second SCC 502, 506 disposed along a second signal path. Each SCC is implemented as a PA circuit and is partitioned into two series-connected portions—a PA portion 501/502 and an impedance matching portion 505/506. EX-1003, ¶31.

Module 500 also includes a first semiconductor die 511 made of silicon germanium (SiGe) and a second semiconductor die 512 made of gallium arsenide (GaAs). With respect to the first SCC, PA portion 501 is formed in the first die

511 using SiGe BiCMOS technology, while the impedance matching portion 505 is formed in the second die 512 using GaAs technology. EX-1001 7:32-8:66; EX-1003, ¶32. For the second SCC, portions 502 and 506 both are integrated in the second die 512.

According to the '200 Patent, partitioning the first SCC across different dies is implemented so that the “[s]ignal conditioning functions of each of [its] portions are facilitated by a predetermined type of semiconductor die within which they are formed.” EX-1001, Abstract. The '200 Patent states that this design scheme is “efficient in respect of die area usage,” “provides the module designer with the best attributes of both semiconductor [dies] . . . in order to achieve a high level of performance, and integration, with a low number of module components,” and results in a compact module size. EX-1001, 2:28-33; 8:43-47; 8:52-56; EX-1003, ¶33. In other words, the '200 Patent is directed to a RF module with multiple semiconductor dies that is implemented by partitioning signal conditioning circuits along their respective signal paths and integrating the resulting partitions into the die best suited for each portion’s functionality. EX-1003, ¶33.

But well before the '200 Patent, implementing modules in this manner was a well-known and conventional practice. For example, as illustrated below, *Garlepp* discloses the same multiple-die architecture for RF modules where elements in common with the '200 Patent are color coded in the same color.



EX-1005, FIG. 8 (annotated), ¶¶5, 46; EX-1003, ¶34.

As in the '200 Patent, *Garlepp*'s module includes two signal conditioning circuits and two interconnected semiconductor dies fabricated using different semiconductor processes. Like the '200 Patent, the **first SCC** (i.e., "receive path circuitry") is partitioned along a **first signal path** so that portion 851 is formed in **first die 854** and portion 839 is formed in **second die 801**. Also like the '200 Patent, the entirety of the **second SCC** (i.e., transmitter circuitry 877), which is disposed along a **second signal path**, is formed in **second die 801**. EX-1005, ¶¶86, 91-103, 164; EX-1003, ¶35.

Likewise, *Magoon* as modified by *Ngompe* illustrates a multiple-die module

implemented by partitioning circuits into functional portions and then integrating each portion using a semiconductor technology most suited to the portion's functionality, as illustrated below:

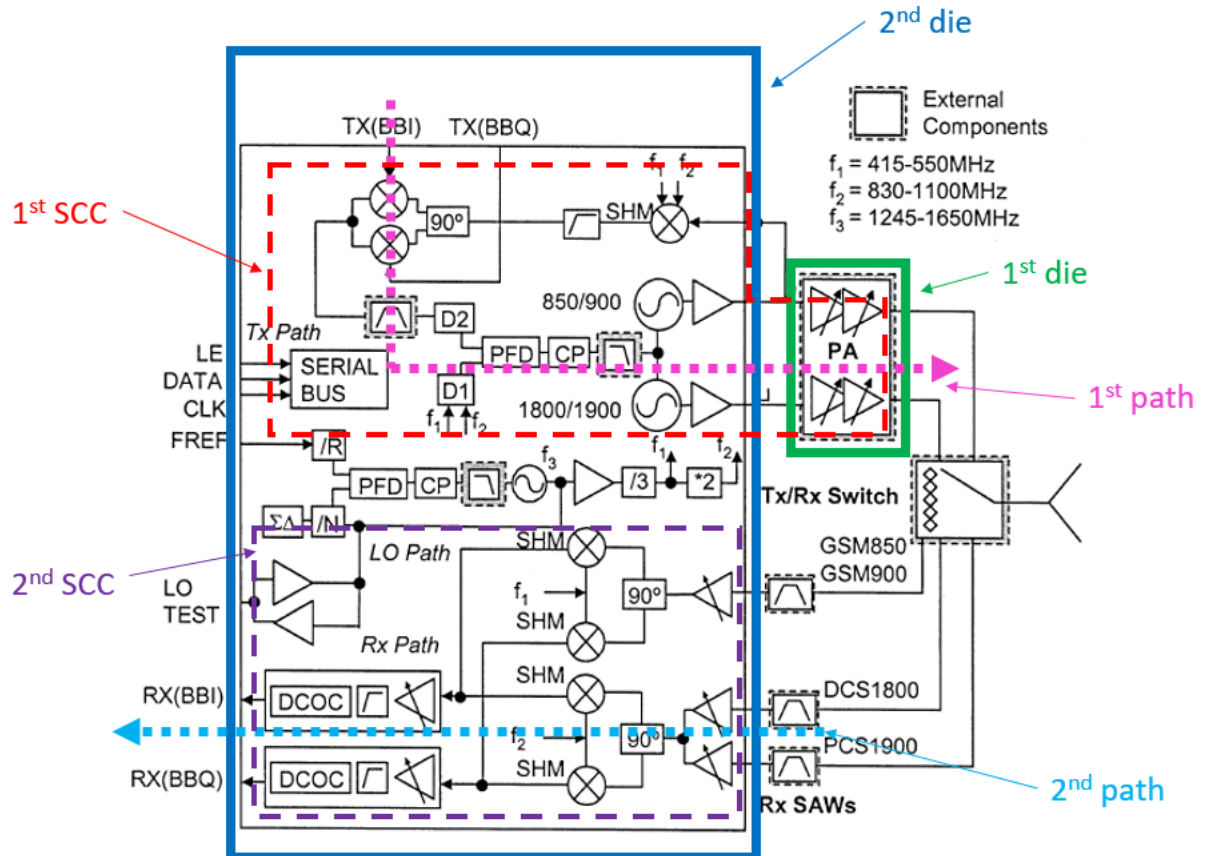


Fig. 1. Top-level schematic of transceiver, with external RF components.

EX-1006 FIG. 1 (annotated); EX-1003, ¶36.

As demonstrated below, *Garlepp* alone, and *Magoon* in view of *Ngompe* each disclose multiple-die RF modules with the same partitioning of signal conditioning circuits and integration across semiconductor dies required by the Challenged Claims.

III. GROUNDS FOR STANDING (37 C.F.R. §42.104(A))

Petitioner certifies that the '200 Patent is eligible for IPR and that Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the presented grounds. 37 C.F.R. §42.104(a). This Petition is filed pursuant to 37 C.F.R. §42.106(a).

IV. RELIEF REQUESTED (37 C.F.R. §42.22(A))

Petitioner respectfully requests institution of an IPR pursuant to 37 C.F.R. §42.108 and cancellation of the Challenged Claims.

V. REASONS FOR THE RELIEF REQUESTED

As explained in §§II and V-VIII of this Petition and in the Declaration of Petitioner's Expert, Dr. Ayman Fayed (EX-1003), the apparatus and methods recited in the Challenged Claims are obvious over the prior art.²

VI. BACKGROUND

A. Summary of the '200 Patent

The '200 Patent is directed to "RF front-end circuits and more specifically to the field of multi-standard RF front-end circuits implemented in a small module size." EX-1001, 1:9-11. The RF circuits are signal conditioning circuits that are partitioned and integrated in two semiconductor dies within the module. EX-1003, ¶38.

² The Petition cites to the exhibits' original page numbers. All emphasis in quoted materials and annotations to the figures have been added by Petitioner.

The '200 Patent acknowledges that modules incorporating signal conditioning circuits integrated in multiple dies was well-known. An example of a prior art RF module is shown in FIG. 1.

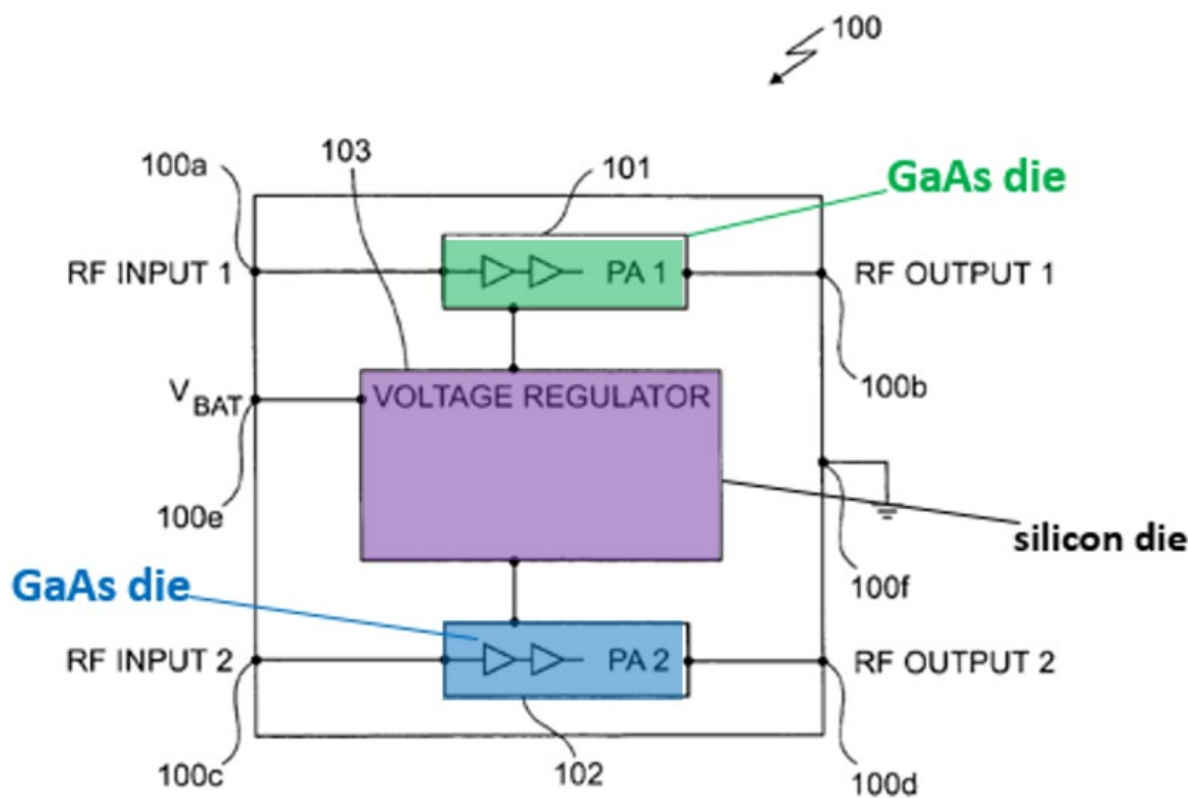


Figure 1
(PRIOR ART)

EX-1001, FIG. 1 (annotated); EX-1003, ¶39.

Module 100 includes three semiconductor dies: two gallium arsenide (GaAs) (green/blue) dies and one silicon die (purple). Two signal conditioning circuits implemented as power amplifier (PA) circuit 101 and PA circuit 102 are

dies is reduced relative to prior art FIG. 1 by integrating ancillary circuits (i.e., voltage regulators) 503, 504 together with PA portion 501 of the **first SCC** within the **first die 511**. EX-1001, 1:56-66. Another difference is that the **first SCC** is partitioned between the **first die 511** and the **second die 512**. Thus, a **first signal path** extends between the RF input port 500a on the **first die** to the RF output port 500b on the **second die**. The **second signal path** resides entirely within the **second die**, extending from the RF input port 500c to the RF output port 500d. EX-1001, 8:27-39. EX-1003, ¶42.

In FIG. 5, **first die 511** is manufactured using SiGe BiCMOS technology, which the '200 Patent acknowledges was known to be suitable both for integration of PAs and for ancillary circuits. EX-1001, 1:56-2:11. **Second die 512** is manufactured using GaAs technology, which the '200 Patent acknowledges routinely was used for integration of PAs and was known to be suited for integration of passive components (e.g., inductors in matching circuit), but unsuitable for the integration of ancillary circuits. EX-1001, 2:12-23, 8:28-36. Thus, as shown in FIG. 5, the **first SCC** is partitioned so that its PA portion 501 is formed in the SiGe **die 511**, and the matching portion 505 is formed in the GaAs **die 512**. According to the '200 Patent: “Advantageously, this integration scheme provides a module designer with the best attributes of both semiconductor substrates, which in this case are silicon and GaAs, in order to achieve a high level

of performance, and integration, with a low number of module components.” EX-1001, 8:43-47; EX-1003, ¶43.

All of the Challenged Claims are directed to the partitioning and multi-die integration scheme shown in FIG. 5 of the ’200 Patent or a variation in the partitioning, as shown in FIG. 6.

B. Summary of the Prosecution History

The ’200 Patent was filed June 2, 2004, and claims benefit as a continuation-in-part to U.S. Application No. 10/680,208 filed October 8, 2003 (’208 Application).

Claims 1-17 and 27-35 (issued as independent claims 1 and 26, and dependent claims 2-17 and 25-34) were allowed in the first Office action. EX-1002 pp.53-59. Original independent claim 18 (a method claim) was rejected, although its dependent claim 19 was deemed allowable. EX-1002 pp.190-196. In response, the Applicant amended independent claim 18 to include the limitations of original claim 19. EX-1002 pp.213-222. A Notice of Allowance then issued, with no specific reason provided for allowance. EX-1002 pp.226-231.

All independent claims broadly recite the partitioning and integration scheme shown in FIG. 5 and FIG. 6. Specifically, each independent claim requires two “semiconductor dies,” and a “signal conditioning circuit” partitioned into “portions,” with one portion integrated within one die and another portion

integrated within the other die.

C. Priority Date of the Challenged Claims

The Patent Owner bears the burden of establishing that it is entitled to the priority date of the '208 Application. For purposes of this Petition, because each of the cited prior art references is prior art to the Challenged Claims of the '200 Patent regardless of whether the Challenged Claims are entitled to the filing date of the '208 Application, this Petition assumes a priority date of October 8, 2003. EX-1001 (63).

D. Claim Construction

Petitioner proposes that each claim term be given its plain and ordinary meaning in this proceeding. The prior art herein meets each claim limitation under any reasonable construction. EX-1003, ¶45.

E. Person of Ordinary Skill in the Art

A POSITA in October 2003 would have been someone knowledgeable and familiar with the signal conditioning circuits and semiconductor chip design and packaging that are pertinent to the '200 Patent. A POSITA would have had a bachelor's degree in electrical or electronics engineering, or an equivalent degree or equivalent training, and approximately three years of experience working with RF circuit design and packaging and/or similar technology. Less professional experience can be remedied by additional education, and vice versa. EX-1003,

¶49.

F. State of the Art

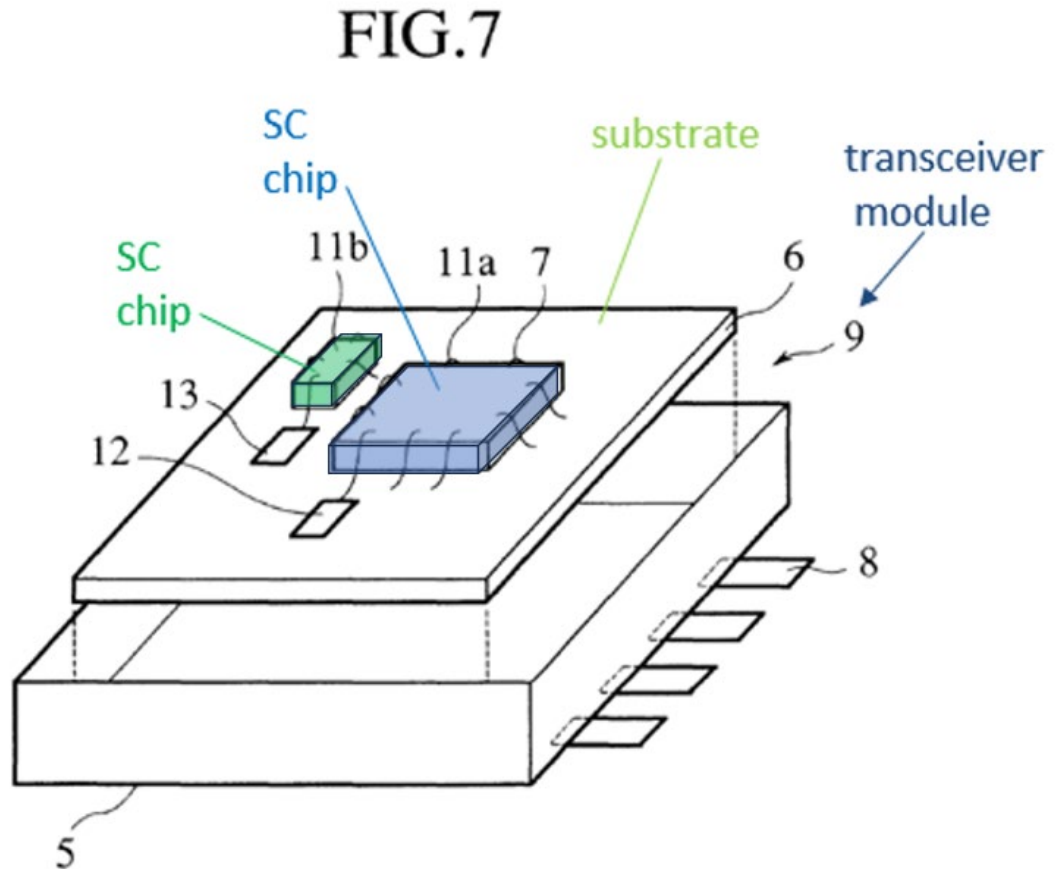
The following section describes the relevant state of the art for multiple die modules as of the priority date, as explained by Dr. Fayed, with citation to exemplary corroborating references. EX-1003, ¶50. The references, and this discussion of what was known to POSITA, provide factual support for the general description of the state of the art at the time of the invention, and provide additional motivation to modify or combine teachings in the references.

1. Techniques for Implementing Modules With Multiple Semiconductor Dies Were Well-Known

By October 2003, techniques for manufacturing module structures for packaging and interconnecting multiple semiconductor dies were well-known. For example, *Pedder* (EX-1014) discloses that “[t]he multichip module (MCM) approach to interconnection and packaging employs unpackaged naked dies mounted on a high interconnection density substrate structure, with the resulting assembly then packaged to form a module.” EX-1014, 1:1-5. As exemplified by *Pedder*, known interconnection techniques included wire-bonding and flip chip soldering, and recognized benefits of MCMs were increased performance, as well as reduction in size and weight and improved reliability. EX-1014, 1:5-28. EX-1003, ¶51.

Given the known benefits achievable with multiple die modules, the RF industry

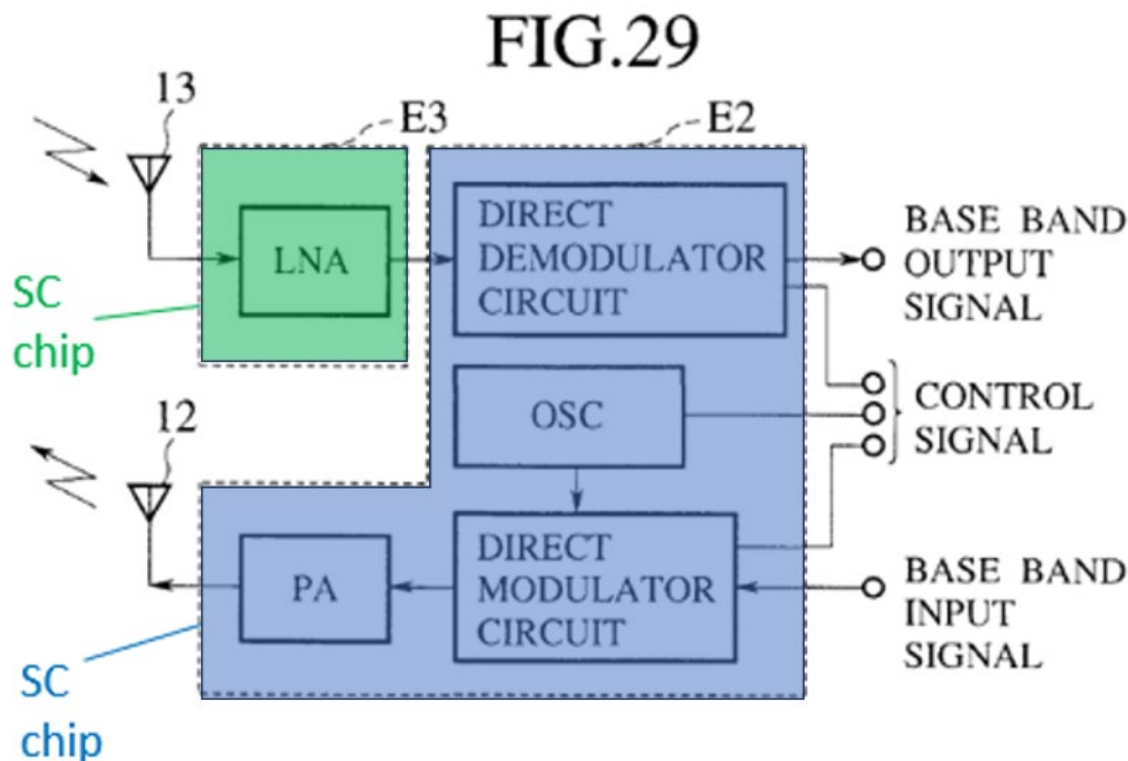
had long been exploring the use of such design strategy in RF transceivers used for devices, such as cellular phones. For example, *Yoshihara* (EX-1013) describes numerous embodiments of RF transceiver packages, including a module with “semiconductor chips” that are “mounted on a single substrate”:



EX-1013, FIG. 7, 7:4-22 (“chips ... 11a, 11b connected by bonding wires 7 to a transmitter antenna 12 and a receiver antenna 13”); EX-1003, ¶52.

In FIG. 29, *Yoshihara* discloses a corresponding two-die (i.e., two semiconductor chips) circuit arrangement for the RF module, in which “the circuit arrangement E3 of one of the two semiconductor chips includes an LNA [low

noise amplifier] and that E2 of the other includes a direct demodulator circuit, an OSC and a PA.” EX-1013, 16:61-17:2. EX-1003, ¶52.



EX-1013, FIG. 29; EX-1009 (Abstract) (disclosing “a single-package solution that contains different components that are interconnected with a multi-chip module (MCM) interconnect technology” for RF transceivers). EX-1003, ¶53.

2. Partitioning Circuits Within a Multi-Die Module to Take Advantage of Diverse Semiconductor Technologies Was a Routine Practice

By October 2003, implementing multi-die modules using dies manufactured in different semiconductor technologies was a well-known practice. Indeed, although a desire existed for integration of systems on a unitary semiconductor

device (referred to as “system-on-chip”), the industry recognized that partitioning circuits into functional blocks, each fabricated in a different semiconductor die, had benefits, including performance and manufacturing advantages. For example, *Chan* (EX-1008) discloses that “[t]raditional multi-chip modules (MCM’s) are a conventional approach to providing a semiconductor solution” for integrated circuit designs that can be partitioned into discrete functional blocks. EX-1008, ¶5. In these traditional MCMs, multiple “semiconductor devices that are mounted on a common base substrate provide the functionality associated with two or more function blocks.” EX-1008, ¶¶31, 35, 36. By using multiple interconnected semiconductor devices, each circuit block “can be matched with a particular semiconductor substrate technologies [sic] and/or semiconductor fabrication processes for enhancing performance, reducing unit cost, etc.” EX-1008, ¶¶5, 25. EX-1003, ¶54.

The art includes other examples of the MCM “conventional approach” for RF front-end systems. For example, *Wambacq* (EX-1009) discloses a “single-package solution” for RF transceivers in which “GaAs MMICs [and] silicon chips” are mounted on a common substrate. EX-1009, Figs. 4, 5, Sections 3, 4. Like *Chan*, *Wambacq* explains that an advantage of a single package solution relative to a “single-chip system” is that “partitioning of the system into its subsystems, each realized in the most suitable technology, will lead to lower cost, increase of

manufacturing yield and optimal performance.” EX-1009 (Section 3). *See also* Ryckaert (EX-1011, p.1037) (disclosing a single-package RF module “using elements realized in different technologies” to meet the “performances expected from high-end applications . . . while keeping the cost and the size of the system as low as possible”). EX-1003, ¶55.

Wambacq was not alone in implementing partitioning in RF modules. For example, in the same time frame as *Wambacq*, *Larson* (EX-1010) disclosed a chip-set for a then-commercially available personal handyphone system (PHS) transceiver that included multiple dies made from different semiconductor technologies, as shown in Fig. 2 below:

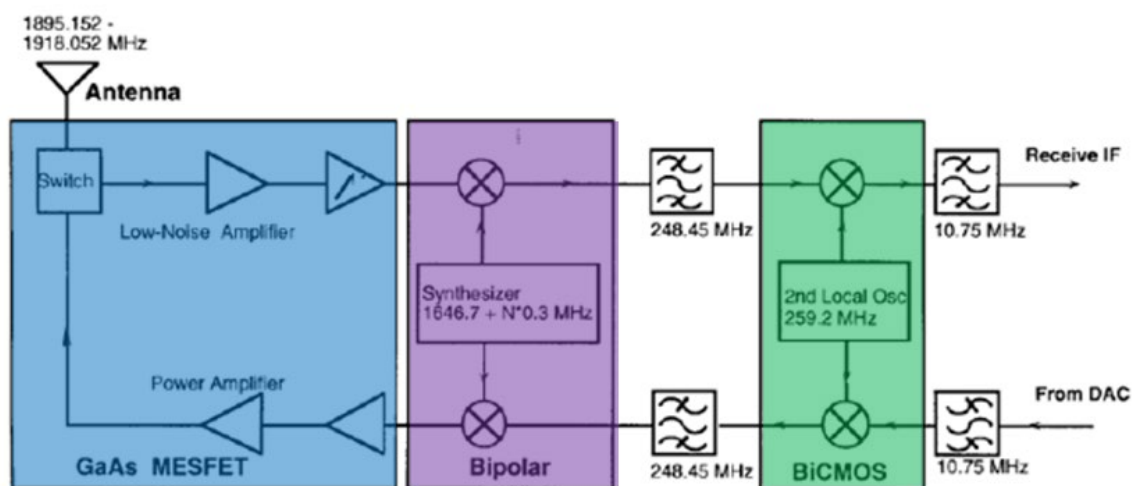


Fig. 2. Simplified block diagram of PHS transceiver [5].

EX-1010, Fig. 2 (annotated); EX-1003, ¶56.

Larson states:

The partitioning of the differing technologies in this system is fairly representative of current technologies, where **GaAs MESFET** technology is employed for the high-performance areas near the antenna (switch, low-noise, and power amplifiers), **silicon bipolar** technology is employed for the frequency synthesizer portion because of its low phase noise capabilities, and **BiCMOS** is used for higher levels of integration in a mixed-signal environment.

EX-1010, p.389. EX-1003, ¶56.

3. It Was Well-Understood that Different Semiconductor Technologies had Different Benefits for RF Circuit Design

By October 2003, RF circuit and module designers were well-versed regarding the attributes of different semiconductor technologies and their suitability for different electrical components and functionality. EX-1003, ¶57. As the '200 Patent acknowledges, it was well known that GaAs technology can “offer more gain per stage and lower losses” for RF components (e.g. PAs), but could be “unsuitable for the integration of ancillary circuits for use with the GaAs based RF component.” EX-1001, 2:16-20. The '200 Patent also acknowledges that the benefits of SiGe BiCMOS technology were well-known, including its use for achieving “higher levels of integration of high-performance RF components,” such as some PAs and LNAs. EX-1001, 1:56-63. EX-1003, ¶57. And, with respect to the suitability of certain semiconductor technologies for implementing PAs and passive components, the '200 Patent states:

- a PA circuit is “**known** to have high loss, or low quality factor, when integrated on the silicon wafer” (EX-1001, 8:23-27); and
- “It is **well known** to those of skill in the art that inductors disposed on the silicon substrate suffer performance degradation due to absorption of RF energy within the substrate and other factors, as compared to inductors that are integrated on a semi-insulating GaAs substrate.” (EX-1001, 8:27-31); EX-1003, ¶57.

The '200 Patent's statements regarding the known characteristics and suitability of various semiconductor technologies for RF integrated circuit designs are corroborated by the art. For example, in 1999, *Wambacq* disclosed that “in the majority of today's RF front-end implementations most active components are realized in GaAs (e.g., LNA, power amplifier, mixer, antenna switch) or silicon bipolar technologies (e.g. frequency synthesizer, mixer,...).” EX-1009 (Section 2). EX-1003, ¶58. In the same time frame as *Wambacq*, *Larson* reported on the “advantages and disadvantage of each of the competing technologies—Si CMOS and bipolar junction transistors (BJT's), Si/SiGe HBT's and GaAs MESFET's, PHEMTs and HBT's”³ in light of the various performance requirements for RF

³ “HBT” refers to a heterojunction bipolar transistor. “MESFET” refers to a metal-semiconductor field effect transistor. “PHEMT” refers to pseudomorphic high

transceivers. EX-1010, p.387. EX-1003, ¶58.

Shi (EX-1012), which also is directed to “low power, reduced size, reduced cost, and robust performance” multi-chip RF transceivers, provides other examples of the in-depth knowledge of the RF industry and the tradeoffs designers routinely faced. For instance:

Costs of manufacturing a radio frequency integrated circuit (IC) may be reduced by switching from one integrated circuit manufacturing process to another. For example, a CMOS process may be used instead of a GaAs, silicon bipolar or bi-CMOS process since it is a more cost affective [sic] method of IC manufacture and is typically the technology choice for digital ICs. Such a CMOS process, however, increases temperature and process related variations. As such, noise, gain variation, mismatches and other factors that negatively impact an RF IC performance are increased for a CMOS process. Thus, **in many RF IC applications, a designer chooses between cost savings and performance.**

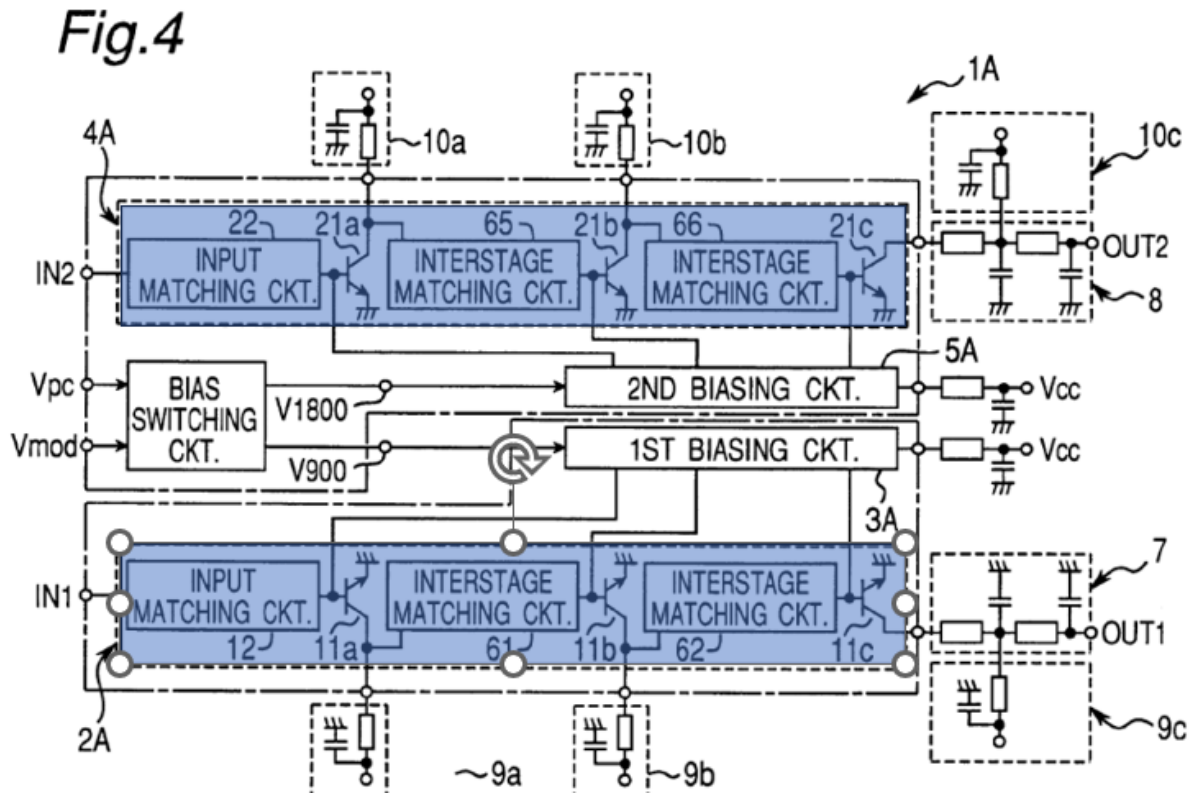
EX-1012, ¶¶7, 8. EX-1003, ¶59.

4. Implementing Power Amplifier Circuits on Different Types of Semiconductor Dies Was Well-Known

By October 2003, it was well-known to implement PA circuits in semiconductor dies of various types. As an example, *Yamamoto* (EX-1015)

electron mobility transistor. EX-1003, ¶58.

discloses dual-band power amplifier circuitry 1A, including multiple power amplifier stages and impedance matching circuits, implemented in two semiconductor dies.



EX-1015, FIG. 4; 1:13-18; 7:65-67; 9:41-48; EX-1003, ¶60.

Although *Yamamoto*'s PAs are implemented as GaAs HBTs, the selection of other semiconductor materials and processes was a routine engineering design choice with known and predictable results. For example, *Larson* discloses that the "final power output stage is typically implemented in silicon MOS, GaAs MESFET, or HBT technology". EX-1010, p.288. The '200 Patent's disclosure of known PA circuits implemented in both SiGe BiCMOS and GaAs confirms the

routine nature of choosing semiconductor materials and processes. EX-1001, 1:56-63; 2:12-16; 4:6-9. EX-1003, ¶60.

VII. IDENTIFICATION OF CHALLENGES

A. Challenged Claims

Claims 1-2, 4, 6, 10-15, 18-20, 23-26, and 29-31 of the '200 Patent are challenged in this Petition.

B. Statutory Grounds for Challenges

The Challenges are set forth in detail below and summarized as follows:

Ground	Claims	Basis	Reference(s)
1	1-2, 4, 10-13, 15, 18-20, 23-26, and 29-31	§103	<i>Garlepp</i> (EX-1005)
2	1-2, 6, 10-15, 18-20, 23-26, and 29-31	§103	<i>Magoon</i> (EX-1006) in view of <i>Ngompe</i> (EX-1007)

Garlepp (EX-1005) is U.S. Patent Publication No. 2003/0017809 titled “Apparatus and Method for Front-End Circuitry in Radio-Frequency Apparatus” filed February 19, 2002 and published January 23, 2003. EX-1005, 1. *Garlepp* qualifies as prior art at least under (pre-AIA) 35 U.S.C. §102(a). *Garlepp* was not cited or applied by the examiner during the '200 Patent prosecution.

Magoon (EX-1006) is a paper titled “*A Single-Chip Quad-Band*

(850/900/1800/1900 MHz Direct Conversion GSM/GPRS RF Transceiver with Integrated VCOs and Fractional-N Synthesizer,” published in IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 37, No. 12, December 2002, and was publicly available before the earliest priority date of the ’200 Patent. EX-1017 (Hsieh-Yeh Declaration) ¶¶26-54. *Magoon* qualifies as prior art at least under (pre-AIA) 35 U.S.C. §102(a). *Magoon* was not cited or applied by the examiner during the ’200 Patent prosecution.

Ngompe (EX-1007) is a paper titled “*Architecture and Performance Overview of a Highly Integrated 13x13 mm Single-Package Radio (SPR) Module for Dualband EGSM900/GSM1800 Applications,*” published in 2003 IEEE RADIO FREQUENCY INTEGRATED CIRCUITS SYMPOSIUM, June 8, 2003, and was publicly available before the earliest priority date for the ’200 Patent. EX-1017 ¶¶55-81. *Ngompe* qualifies as prior art at least under (pre-AIA) 35 U.S.C. §102(a). *Ngompe* was not cited or applied by the examiner during the ’200 Patent prosecution.

VIII. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE

A. Ground 1: Claims 1-2, 4, 10-13, 15, 18-20, 23-26, and 29-31 are obvious under 35 U.S.C. §103(a) over *Garlepp*.

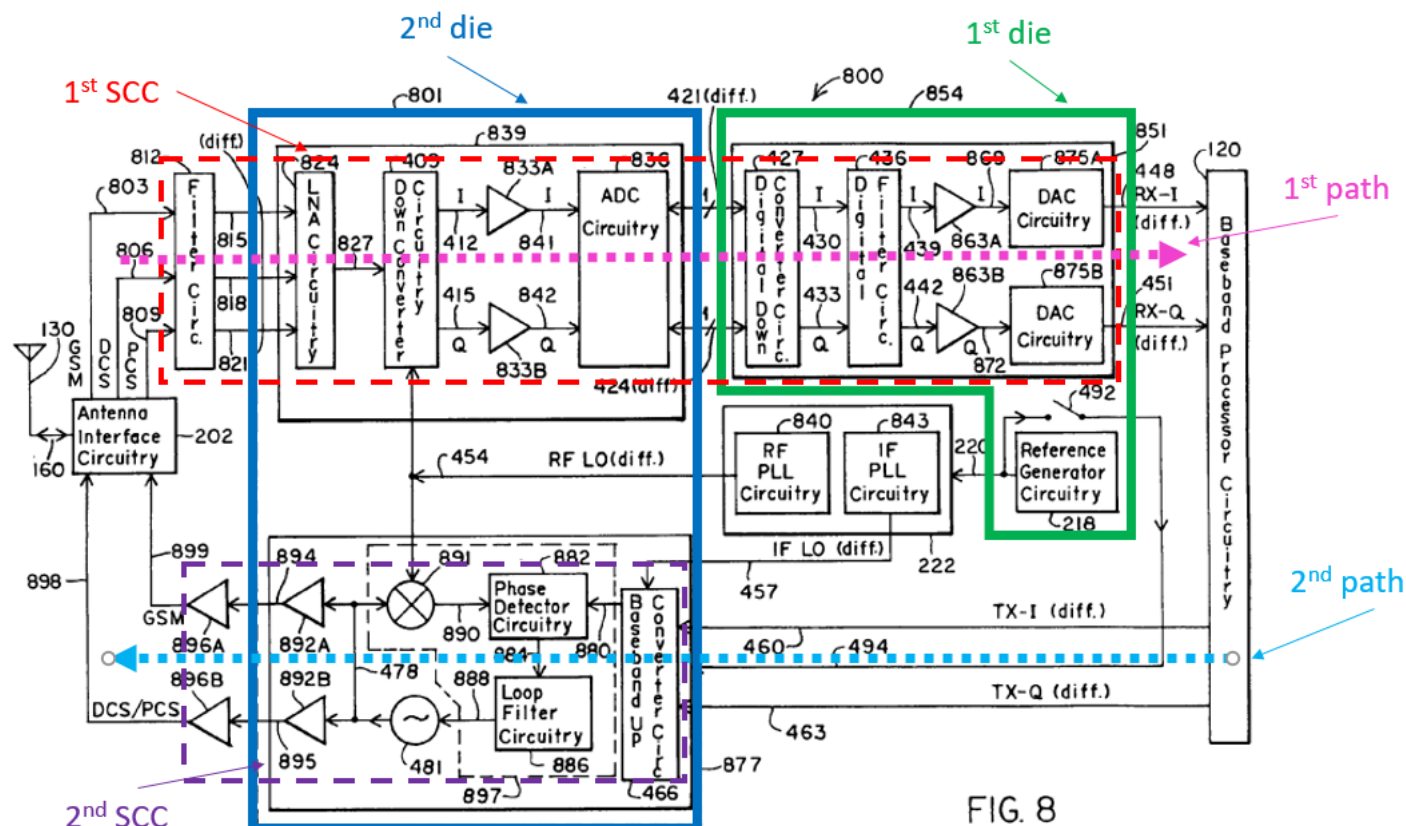
1. *Garlepp*

Garlepp is directed to the same problem as the ’200 Patent: “provid[ing] highly integrated, high-performance, low-cost, and low form-factor RF solutions,” for RF transceivers used in applications, such as cellular handsets. Although then-

recent industry efforts had focused on “providing an RF transceiver within a single integrated circuit (IC),” *Garlepp* recognized the same solution proposed by the ’200 Patent, e.g., that partitioning the RF circuitry into circuit blocks integrated within different semiconductor dies could improve performance, while at the same time resulting in a low-cost and low form-factor solution. EX-1005, ¶5, 46. EX-1003, ¶65.

Garlepp’s partitioned transceiver 800 is shown in annotated FIG. 8 (Annotated FIG. 8)⁴:

⁴ Annotated FIG. 8 is from corresponding U.S. Patent No. 7,035,611, representing the formal drawing corresponding to the handwritten FIG. 8 from EX-1005.



EX-1005, FIG. 8 (annotated). EX-1003, ¶166.

Garlepp's RF transceiver includes two signal conditioning circuits disposed along separate signal paths: **receive path** circuitry 839, 851 and **transmit path** circuitry 877. EX-1005, ¶86. Garlepp's **first SCC** is partitioned into portions 839, 851 that are integrated within a respective **first die** 854 and a **second die** 801 that are manufactured from separate semiconductor processes. EX-1005, ¶¶103, 141. The entirety of the **second SCC** (877) is integrated within the **second die** 801. Thus, a **first signal path** is formed from an RF signal input port through the portion 839 of the **first SCC** within the **second die** 801, through the portion 854 of the **first**

SCC within the first die 854 to a baseband signal output port. The second signal path is formed from a baseband signal input port through the second SCC within the second die 512 and to an RF signal output port. EX-1003, ¶67.

Thus, *Garlepp* discloses the same circuit partitioning and integration arrangement as the '200 Patent claims, in which a signal conditioning circuit is partitioned along a signal path and integrated within different semiconductor dies in a manner best suited to enhance performance, while also reducing cost and size. EX-1003, ¶68.

2. Detailed Application of *Garlepp* to the Challenged Claims

a. Claim 1

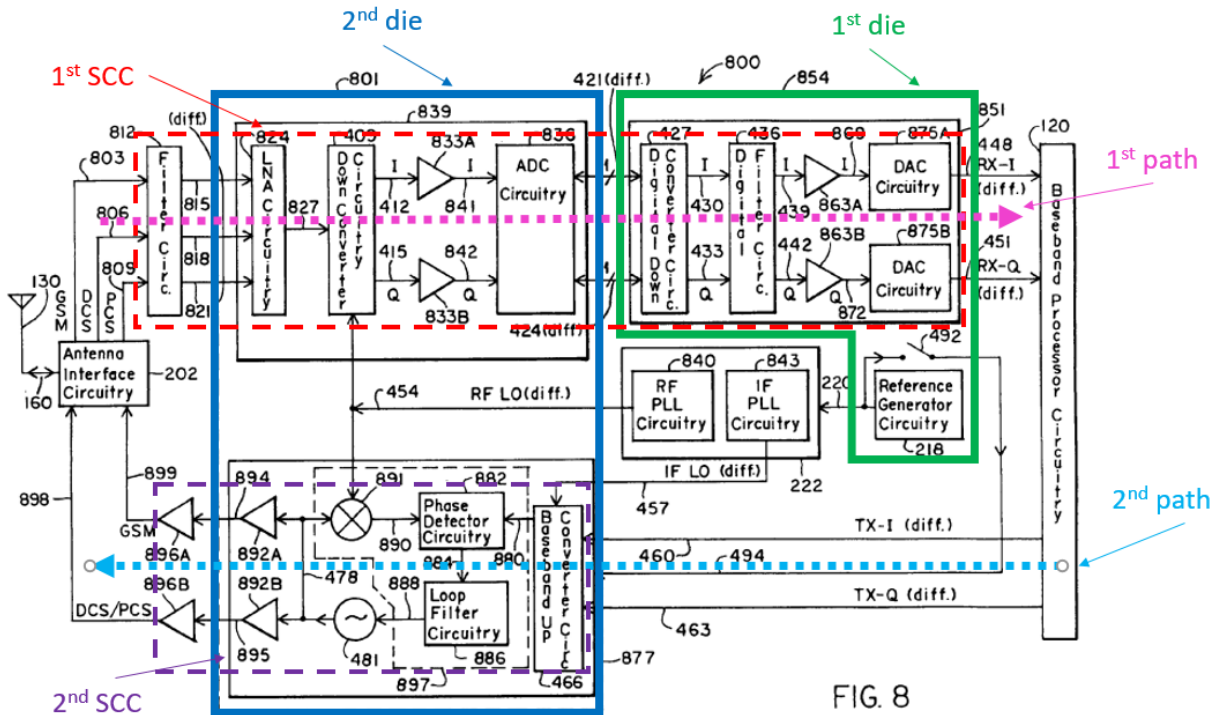
i. [1.0] *An electronic apparatus comprising:*

To the extent the preamble is limiting, *Garlepp* discloses “partitioning RF apparatus [*electronic apparatus*] so as to provide highly integrated, high-performance, low-cost, and low form-factor RF solutions.” EX-1005, ¶46. EX-1003, ¶69.

ii. [1.1] *a first integrated circuit semiconductor die comprising:*

Garlepp discloses “**integrated circuit devices**” made from “**semiconductor fabrication processes**” for use in an “RF apparatus, such as a cellular telephone handset **chipset** implemented in complementary metal oxide **semiconductor**” (*integrated circuit semiconductor dies*). EX-1005, ¶¶6, 141; EX-1003, ¶70.

Garlepp discloses that its RF transceiver includes “circuit partitions, or circuit blocks.” EX-1005, ¶103. In FIG. 8, **partition 854** (*first integrated circuit die*) includes the receiver digital circuitry 851. EX-1005, ¶103:



EX-1005, Annotated FIG. 8. EX-1003, ¶71.

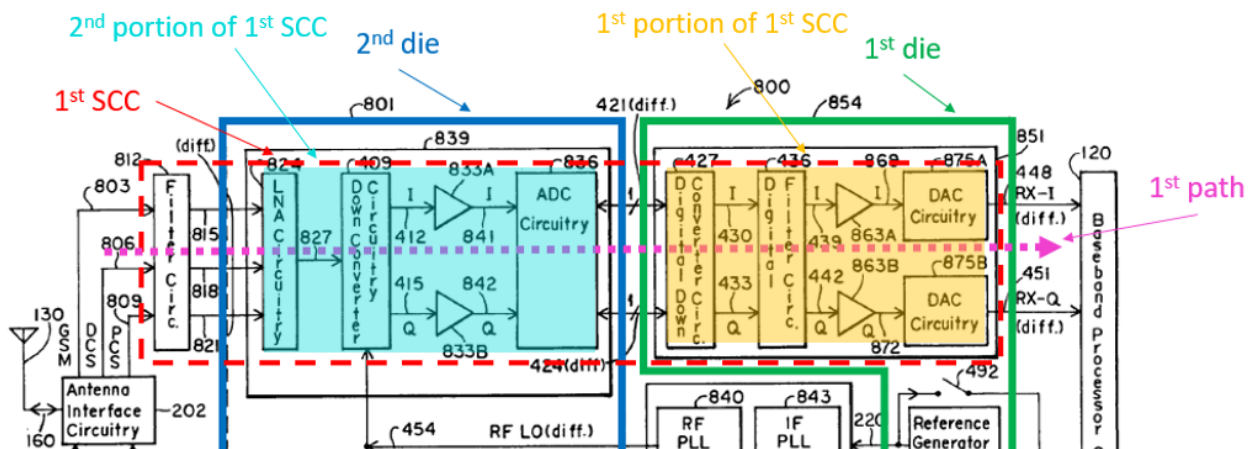
Garlepp also discloses that each circuit **partition** “resides within an **integrated circuit device**” (*integrated circuit die*). EX-1005, ¶103. *Garlepp* further discloses “a **silicon die that houses** the receiver circuitry.” EX-1005, ¶230. *Garlepp* further discloses that the circuit architecture of the RF transceiver “allows **on-chip integration** of the digital filter circuitry,” which is part of the “circuit partition” that includes the receiver digital circuitry 851. EX-1005, ¶230. *Garlepp* uses the terms “integrated circuit device,” “die,” and “chip” interchangeably, thus

corroborating that a circuit partition “residing within an integrated circuit device” is circuitry integrated within an *integrated circuit semiconductor die*. EX-1003, ¶72.

- iii. [1.2] a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path; and

Garlepp discloses “receive path circuitry” (first signal conditioning circuit) arranged on a first signal path between the antenna interface circuitry 202 and baseband processor 120 (disposed along a first signal path), as shown in Annotated FIG. 8 above. EX-1005, ¶¶XX; EX-1005, FIG. 8 (annotated). EX-1003, ¶73.

The receive path circuitry includes receiver digital circuitry 851 (first portion) within partition 854 (first integrated circuit die) as shown in the portion of Annotated FIG. 8 below. EX-1005, ¶¶86, 103.



EX-1005, FIG. 8 (annotated). EX-1003, ¶74.

As described below with respect to limitation [1.4], the **first SCC** also includes a **second portion** arranged along the **first signal path** on the **partition** 801 (*second integrated circuit die*). EX-1005, ¶¶86, 103. The **second portion** includes analog receive circuitry 839 (which includes low noise amplifier (LNA) circuitry 824, down-converter circuitry 409, programmable gain amplifiers (PGAs) 833A,B, and ADC 836) that accepts filtered RF signals from filter circuitry 812 and generates in-phase and quadrature receive signals 421, 424 at its output. The **first portion** includes digital receive circuitry 851 (which includes digital down-converter circuitry 427, digital filter circuit 436, PGAs 863A,B and DAC 875A,B) that accepts signals 421, 424 and generates analog receive signals 448, 451 at its output, which are provided to baseband circuitry 120. In other words, *Garlepp* teaches that the “**receive path circuitry**” accepts “filtered RF signals” at an input and operates on the signals along the “receive path” to provide “analog receive signals” at an output. EX-1005 ¶¶91-94, 96-97. EX-1003, ¶75.

A POSITA understood that the functions performed by the **receive path circuitry** (i.e., amplify 824, down-convert 409, amplify 833, up-convert 427, filter 436, amplify 863) condition the receive signal as it propagates along the receive signal path. These functions are “signal conditioning” because the signals are amplified, frequency-translated, and filtered by the various stages of the receive path circuitry to prepare the signals for the next stage in the receive path. EX-

1003, ¶76 (EX-1016 (“**signal conditioning**” is “processing of a signal to improve its intelligibility, signal-to-noise ratio, or the like”; “processing or conversion of a signal, so as to make it compatible with a given channel, device, or system”))).

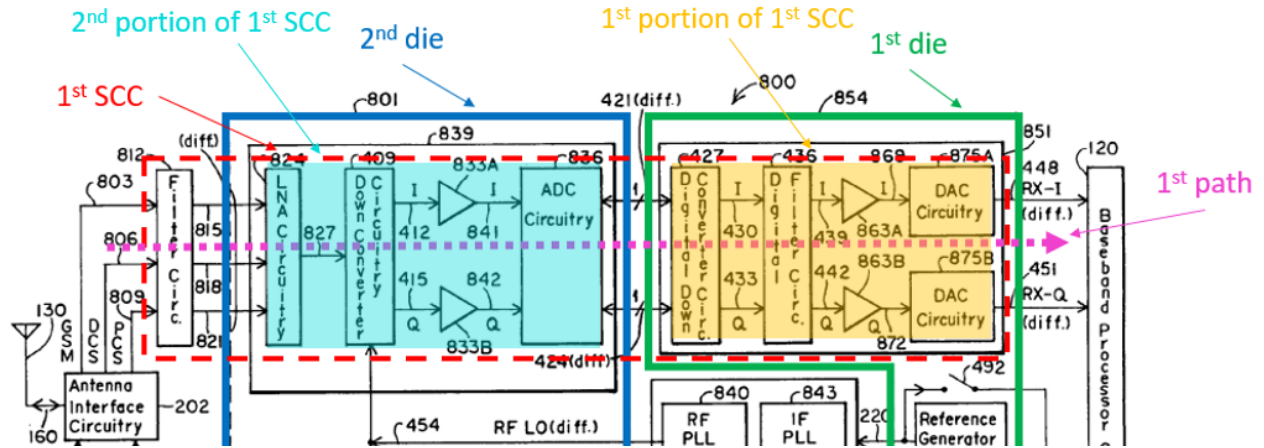
Garlepp therefore discloses that the **receive path circuitry** is a *first signal conditioning circuit* (“SCC”) disposed along a *first signal path*, and the **digital receiver circuitry 851** is a *first portion* of the *first SCC*. EX-1003, ¶77.

iv. [1.3] a second integrated circuit semiconductor die comprising;

Garlepp discloses a **partition 801** that resides within a different semiconductor integrated circuit device (*second integrated circuit semiconductor die*). As explained above for element [1.1], partition 801 is formed as an integrated circuit on a *semiconductor die*. EX-1005 ¶¶103, 141; EX-1003, ¶78.

v. [1.4] a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first portion of a first signal conditioning circuit for a signal propagating along the first signal path; and,

Garlepp discloses “**receive path circuitry**” (*first SCC*) includes **receiver analog circuitry 839** (*second portion*) integrated within **partition 801** (*second die*) and **receiver digital circuitry 851** (*first portion*) integrated within **partition 854** (*first die*), as shown in the portion of Annotated FIG. 8 below:



EX-1005, ¶¶91-97, FIG. 8 (annotated). EX-1003, ¶79.

As explained above for element [1.2], the amplifying and down-converting functions performed by the receiver analog circuitry 839 (*second portion*) and the down-converting, filtering, amplifying functions performed by receiver digital circuitry 851 (*first portion*) that are described in *Garlepp* are *signal conditioning functions* on a *signal propagating along the first signal path*. EX-1003, ¶80.

- vi. ***[1.5] a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.***

Element [1.5] merely adds a substrate to support the first and second dies and provide interconnections between them. As discussed in the State of the Art above (Section V.F), a POSITA understood that the first and second dies of *Garlepp*'s chipset would be interconnected (e.g., by wire bonding or flip-chip assembly) and supported on a common structure (*a substrate*) because that was the

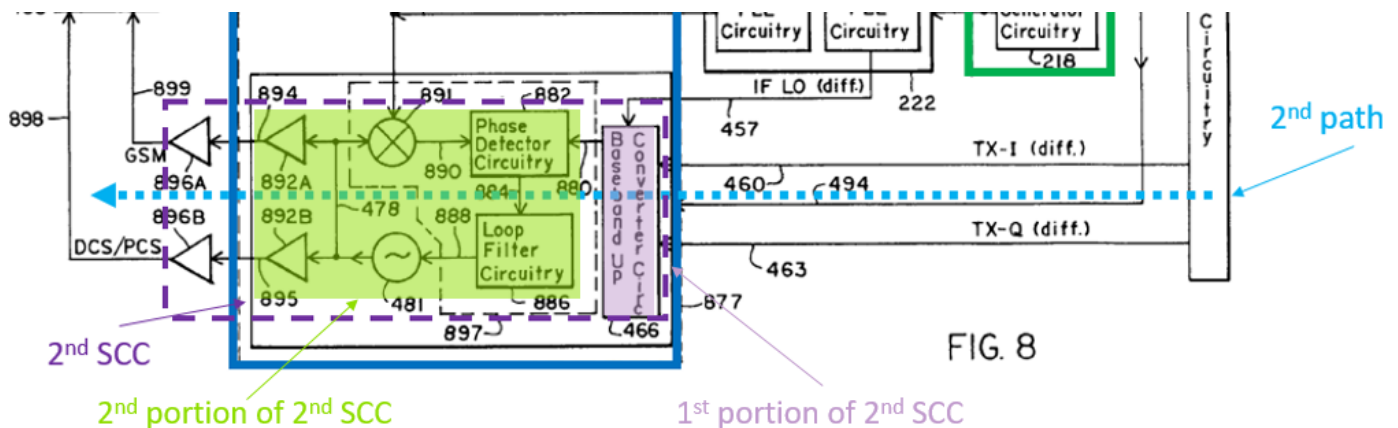
well-known and conventional way of connecting and supporting semiconductor chipsets. EX-1008, ¶5; EX-1009, (Section 3); EX-1013, FIG. 7, 7:4-22; EX-1014, 1:1-28. EX-1003, ¶81. Further, *Garlepp* discusses that any conventional packaging method, including modules, can be used to provide a low-cost and low form-factor RF solution. EX-1005, ¶¶46, 164 (“circuit partitions may alternatively reside within other substrates, carriers, or packaging arrangements. By way of illustration, other partitioning arrangements may use **modules**, thin-film modules, thick-film modules, isolated partitions on a single substrate, circuit-board partitions, and the like”), 272-273 (disclosing that antenna interface circuitry 202 can be coupled “to an integrated circuit or **module** that includes the rest of the RF receive path circuitry,” such as the “circuitry shown in FIG. 8”). EX-1003, ¶81.

b. Claim 2

- i. [2.0] An electronic apparatus according to claim 1, comprising a second signal conditioning circuit comprising a first portion of the second signal conditioning circuit and a second portion of the second signal conditioning circuit integrated within the second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path.*

Garlepp discloses RF transceiver 800 includes transmitter circuitry 877 that provides transmit signals 894, 895 to power amplifiers 896A, 896B (second signal conditioning circuit). *Garlepp* discloses transmitter circuitry 877 is integrated

within **partition 801** (*second integrated circuit die*); accepts “transmit input signals” 460, 463 from baseband circuitry 120; and provides “buffered transmit signals” 894, 895 to **power amplifiers 896A, 896B**, which provide “amplified RF signals” 899, 898. EX-1005, ¶¶100-101. *Garlepp* therefore discloses that the **transmitter circuitry 877** and **power amplifiers 896A, 896B** (collectively, *second SCC*) are disposed along a *second signal path* because circuitry 877 accepts transmit input signals at its input and power amplifiers 896 generate amplified transmit signals at the output. As shown in the portion of annotated FIG. 8 below, the **transmit signal path** (*second path*) is different than the **receive signal path** (*first path*).



EX-1005, FIG. 8 (annotated). EX-1003, ¶82.

Garlepp further discloses that **transmitter circuitry 877** (*second conditioning circuit*) includes **offset phase lock loop (PLL) circuitry 897**, **transmit voltage controlled oscillator (VCO) circuitry 481** and **output buffers 892A,B** (*second*

portion); and **baseband up-converter circuitry 466** (*first portion*). EX-1005, FIG 8 (annotated), ¶¶100-102. EX-1003, ¶83.

Garlepp discloses that the baseband up-converter circuitry 466 accepts the analog transmit input signals 460, 463, mixes those signals with the IF local oscillator signal 457, and provides a transmit IF signal 880 to the offset PLL circuitry 897. The offset mixer circuitry 891 in circuitry 897 mixes the transmit VCO output signal 478 with the RF local oscillator signal 454, and provides a mixed signal 890 to the phase detector circuitry 882. The phase detector circuitry 882 compares the mixed signal 890 to the transmit IF signal 880 and provides an offset PLL error signal 884 to the loop filter circuitry 886. The loop circuitry 886 provides a filtered offset PLL signal 888 to the transmit VCO circuitry 481. Transmitter output buffers 892A and 892B receive the transmit VCO output signal 478 and provide buffered transmit signals 894 and 895 to a pair of power amplifiers 896A and 896B. EX-1005, ¶¶100-102; EX-1003, ¶84.

A POSITA understood that the functions performed by the first and second portions of the transmitter circuitry 877 (i.e., up-convert, mix, buffer) condition the transmit signal as it propagates along the transmit signal path. These functions are “signal conditioning” because they are operations performed to prepare the signals for use by the next stage in the transmit path. EX-1003, ¶85 (citing EX-1016).

Garlepp therefore discloses that the transmitter circuitry 877 is a *second signal*

conditioning circuit disposed along a second signal path, which includes first and second portions that perform a signal conditioning function on a signal propagating along a second signal path. EX-1003, ¶85.

c. Claim 4

- i. [4.0] *An electronic apparatus according to claim 1, wherein the first integrated circuit die is manufactured using a first semiconductor process and utilizes a silicon based technology.***

As discussed above, receiver digital circuitry 851 resides within first die 854 (*first integrated circuit die*). EX-1005, ¶103.

Garlepp discloses that its RF transceiver can be “a cellular telephone handset chipset implemented in complementary metal oxide semiconductor (CMOS).” EX-1005, ¶6. Further, with reference to FIG. 15, *Garlepp* discloses “CMOS implementation of the receiver circuitry 1520,” which “may constitute . . . the receiver circuitr[y] shown in the preceding figures [including FIG. 8].” EX-1005, ¶¶181, 202. A POSITA understood that CMOS is a *semiconductor process that utilizes a silicon based technology*, as corroborated by *Garlepp*’s disclosure of “a **silicon die** that houses the receiver circuitry.” EX-1005, ¶230. Further, as discussed in the State of the Art, *supra*, the use of “a CMOS process . . . is typically the technology choice for digital ICs” and, thus, would have been an obvious design choice for implementing receiver digital circuitry 851 in the first die that would achieve known and predictable results. EX-1012, ¶7. EX-1003,

¶87.

d. **Claim 10**

- i. ***[10.0] An electronic apparatus according to claim 2, wherein the first semiconductor process does not facilitate manufacturing and integration of at least one of the second portion of the first signal conditioning circuit and the second portion of the second signal conditioning circuit.***

As discussed with respect to claims 1 and 2, the *second portion of the first signal conditioning circuit* and the *second portion of the second signal conditioning circuit* are on the *second die*. *Garlepp* discloses that the *first and second dies* “typically result from separate semiconductor fabrication processes and manufacturing lines.” EX-1005, ¶141; EX-1003, ¶88; [2.0].

By disclosing “separate” semiconductor fabrication processes and manufacturing lines, *Garlepp* is disclosing that the second die is fabricated using a semiconductor process that is different than the first semiconductor process used for the first die. Because *Garlepp* uses different semiconductor processes for the two dies—one of which houses the analog circuitry and the other of which houses the digital circuitry—a POSITA understood that the semiconductor process for the first die does not facilitate manufacturing and integration of at least one of the second portion of the first signal conditioning circuit and the second portion of the second signal conditioning circuit, which are on the second die. *Garlepp*’s disclosure that the analog LNA circuitry (which is integrated on the *second die*)

can be a “CMOS bipolar implementation” corroborates that different semiconductor processes are used for the digital circuitry on the first die and the analog circuitry on the second die. EX-1005, ¶¶181, 203. EX-1003, ¶89.

Moreover, as discussed in the State of the Art, *supra*, the use of different semiconductor technologies and processes within a single module or on a common supporting substrate, where the circuit partitions are “matched with a particular semiconductor substrate technologies and/or semiconductor fabrication processes for enhancing performance, reducing unit cost, etc.,” was a well-known, conventional design practice. EX-1008, ¶¶5, 25; EX-1009, Figs. 4, 5, Sections 3, 4; EX-1010, p.389; EX-1011, p.1037. EX-1003, ¶90.

e. Claim 11

- i. [11.0] An electronic apparatus according to claim 1, wherein the second integrated circuit die is manufactured using a second semiconductor process that is different from that used to manufacture the first integrated circuit die.*

Garlepp discloses this limitation for the same reason as discussed with respect to Claim 10. EX-1003, ¶91.

f. Claim 12

- i. [12.0] An electronic apparatus according to claim 1, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.*

For the reasons discussed above for Claim 4, *Garlepp* discloses this limitation. EX-1003, ¶92.

g. Claim 13

- i. [13.0] An electronic apparatus according to claim 12, wherein the second integrated circuit die is derived from a second semiconductor wafer comprised of other one of Si, SiGe, GaAs, InP, and GaN.*

Garlepp discloses that the first and second dies are made from different semiconductor fabrication processes. EX-1005, ¶141. *Garlepp* further discloses that the LNA circuitry, which is integrated on the *second die*, can be a “CMOS bipolar implementation.” EX-1005, ¶¶181, 203. A POSITA understood that a SiGe process technology (*wafer comprised of other one of Si*) is an obvious design choice for implementing CMOS bipolar (i.e., BiCMOS) circuitry in a die that would achieve known and predictable results. EX-1003, ¶93.

Further, as explained in the State of the Art, *supra*, the use of wafers made of semiconductor materials other than native Si, such as SiGe, for high-performance RF circuits (e.g., analog receiver circuitry 839 and transmitter circuitry 877) was well-known and routine. *E.g.*, EX-1001, 1:56-63 (the use of SiGe BiCMOS technology can achieve “higher levels of integration of high-performance RF components,” such as PAs and LNAs). A POSITA would have been motivated to use a known non-native Si wafer, such as a SiGe wafer, to

integrate *Garlepp*'s receiver analog circuitry 839 and transmit circuitry 877 in partition 801 to enhance performance, increase the level of integration and reduce size in a known and predictable manner. EX-1003, ¶94.

h. Claim 15

- i. [15.0] An electronic apparatus according to claim 1, wherein the second portion of the first signal conditioning circuit comprises at least one of a capacitor and an inductors and a signal transmission line.*

In addition to the receiver path circuitry (*first SCC*) discussed above for claim 1, *Garlepp* discloses a “matching network 1515” that provides impedance matching between filter circuitry 812 and the input stage (i.e., LNA circuitry 834) of receiver analog circuitry 839 (*second portion of first SCC*). EX-1005, ¶¶180-181. *Garlepp* further discloses that “one may use distributed **transmission lines** to perform impedance transformation” in “a differential distributed matching network” and that “one may fully or partially implement any of the differential **transmission lines** described above using ... the substrate of a silicon die (such as a **silicon die that houses the receiver circuitry**).” EX-1005, ¶¶221, 228, 230. By disclosing that the transmission lines (1) provide for impedance matching between the filter circuitry 812 and the input stage of receiver analog circuitry 839 and (2) can be implemented in the die that houses the receiver circuitry, *Garlepp* is disclosing that the receive circuitry 839 (*second portion of first SCC*) comprises a

signal transmission line. EX-1003, ¶95.

i. Claim 18

i. *[18.0]. A method of manufacturing a module comprising:*

To the extent the preamble is limiting, *Garlepp* teaches this limitation for the same reasons as discussed with respect to limitation [1.0]. EX-1003, ¶96.

ii. *[18.1] providing a first signal conditioning circuit comprising a first portion and a second portion;*

Garlepp teaches this limitation for the same reasons as discussed with respect to limitations [1.2] and [1.4]. EX-1003, ¶97.

iii. *[18.2] providing a second signal conditioning circuit comprising a first portion and a second portion;*

Garlepp teaches this limitation for the same reasons as discussed with respect to Claim 2. EX-1003, ¶98.

iv. *[18.3] implementing the first portion of the first signal conditioning circuit within a first semiconductor die;*

Garlepp teaches this limitation for the same reasons as discussed with respect to limitations [1.1] and [1.2]. EX-1003, ¶99.

v. *[18.4] implementing the second portion of the first signal conditioning circuit within a second semiconductor die;*

Garlepp teaches this limitation for the same reasons as discussed with

respect to limitations [1.3] and [1.4]. EX-1003, ¶100.

- vi. ***[18.5] implementing the first and second portions of the second signal conditioning circuit in the second semiconductor die;***

Garlepp teaches this limitation for the same reasons as discussed with respect to Claim 2. EX-1003, ¶101.

- vii. ***[18.6] bonding the first and second dies to a common substrate; and,***

Garlepp teaches this limitation for the same reasons as discussed with respect to limitation [1.5]. Further, as discussed in the State of the Art, *supra*, manufacturing a multiple-die module by bonding dies to a common substrate was a well-known, conventional practice. EX-1008, ¶5; EX-1014, 1:1-28; EX-1013, FIG. 7, 7:4-22. EX-1003, ¶102.

- viii. ***[18.7] forming electrical connections between the two dies to complete the first signal conditioning circuit from the first portion of the first signal conditioning circuit and the second portion of the first signal conditioning circuit.***

Garlepp teaches this limitation for the same reasons as discussed with respect to limitation [1.5]. EX-1003, ¶103.

j. **Claim 19**

- i. ***[19.0] A method according to claim 18, wherein the first semiconductor die comprises a first portion of a first signal path and the second semiconductor die comprises a second portion of***

the first signal path, the first signal path disposed between a first input port and a first output port.

Garlepp discloses this limitation for the same reasons as discussed with respect to Claim 1. EX-1003, ¶104.

k. Claim 20

- i. [20.0] A method according to claim 19, wherein the second semiconductor die comprises a second signal path that is other than the second portion of the first signal path and in approximate RF isolation therefrom.*

Garlepp discloses this limitation for the same reason as discussed with respect to Claims 1 and 2. Further, *Garlepp* also discloses that the “timing of the transmit mode and receive mode in the GSM specifications help to mitigate potential interference between the transceiver’s receive-path circuitry and its transmit-path circuitry” (*in approximate RF isolation therefrom*). EX-1005, ¶62. EX-1003, ¶105.

l. Claim 23

- i. [23.0] A method according to claim 18, wherein the first semiconductor die does not facilitate implementation of the second portion of the first signal conditioning circuit therein.*

Garlepp discloses this limitation for the same reason as discussed with respect to Claim 10. EX-1003, ¶106.

m. Claim 24

- i. [24.0] A method according to claim 18, wherein implementing of the second portion of the first signal conditioning circuit within the second semiconductor die provides increased performance in signal conditioning as compared to implementing of the second portion of the first signal conditioning circuit within the first semiconductor die.*

Garlepp discloses: “The receiver analog circuitry [*second portion of first SCC within second die*] and the receiver digital circuitry [*first portion of first SCC within first die*] are partitioned so that interference effects between the receiver analog circuitry and the receiver digital circuitry tend to be reduced.” EX-1005, Abstract; EX-1003, ¶107. By stating that *Garlepp*’s partitioning reduces interference, *Garlepp* is disclosing that implementing the receiver analog circuitry (*second portion of first SCC*) in the *second die* as opposed to in the *first die* provides for *increased performance in signal conditioning*. EX-1003, ¶107.

n. Claim 25

- i. [25.0] A method according to claim 18, wherein prior to implementing the first signal conditioning circuit comprises partitioning of the first signal conditioning circuit into the first portion and the second portion.*

Garlepp discloses this limitation for the same reason as discussed with respect to Claim 1. Further, as discussed in the State of the Art, partitioning a circuit prior to implementing it was a routine and conventional design practice. EX-1008, ¶¶2, 5. EX-1003, ¶108.

o. **Claim 26**

i. ***[26.0] An electronic apparatus comprising:***

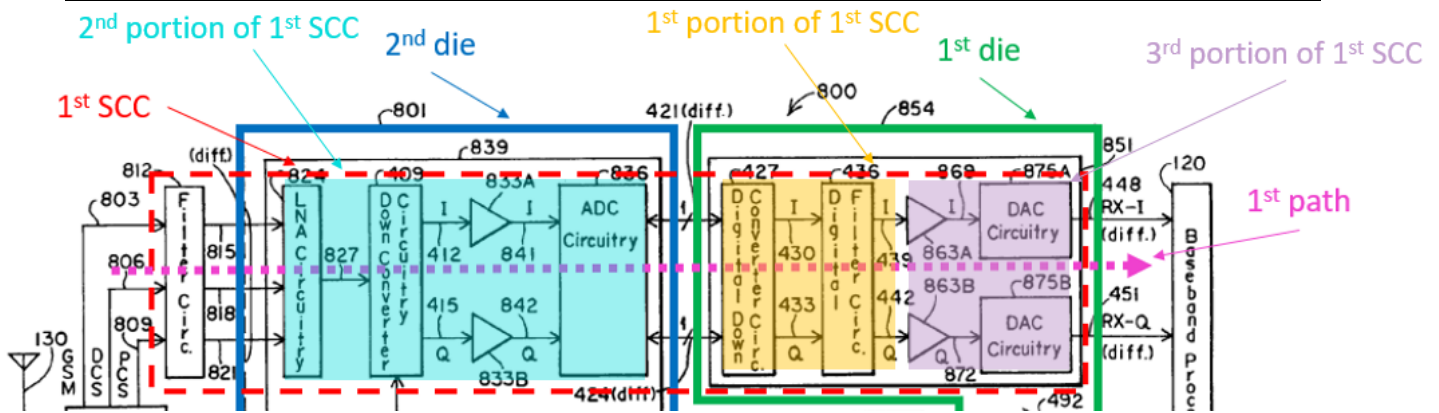
Garlepp discloses this limitation for the reasons discussed with respect to limitation [1.0]. EX-1003, ¶109.

ii. ***[26.1] a first integrated circuit semiconductor die comprising:***

Garlepp discloses this limitation for the reasons discussed with respect to limitation [1.1]. EX-1003, ¶110.

iii. ***[26.2] a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path;***

As explained above for Claim 1, *Garlepp* discloses that the **receive path circuitry** (*first SCC*) includes receiver digital circuitry 851 integrated within **partition 854** (*first die*) that conditions signals propagating on the **receive path** (*first signal path*). EX-1005, ¶103; EX-1003, ¶111. *Garlepp* further discloses circuitry 851 **includes digital down-converter circuitry 427 and digital filter circuitry 436** (*first portion*) and **digital PGAs 863A,B and DAC 875A,B** (*third portion*). EX-1005, ¶¶96-97. EX-1003, ¶111.



EX-1005, FIG. 8 (annotated). EX-1003, ¶111.

- iv. *[26.3] a third portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along the first signal path; and*

Garlepp discloses this limitation for the reasons discussed with respect to limitation [26.2]. EX-1003, ¶112.

- v. *[26.4] a second integrated circuit semiconductor die comprising;*

Garlepp discloses this limitation for the reasons discussed with respect to limitation [1.3]. EX-1003, ¶113.

- vi. *[26.5] a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first and third portions of the first signal conditioning circuit for a signal propagating along the first signal path; and,*

Garlepp discloses this limitation for the reasons discussed with respect to limitations [1.4] and [26.2]. EX-1003, ¶114.

- vii. *[26.6] a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.*

Garlepp discloses this limitation for the reasons discussed with respect to limitation [1.5]. EX-1003, ¶115.

p. **Claim 29**

- i. *[29.0] An electronic apparatus according to claim 26, comprising a second signal conditioning circuit comprising a first portion of the second signal conditioning circuit and a second portion of the second signal conditioning circuit integrated within the second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path.*

Garlepp discloses this limitation for the reasons discussed with respect to Claim 2. EX-1003, ¶116.

q. **Claim 30**

- i. *[30.0] An electronic apparatus according to claim 26, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.*

Garlepp discloses this limitation for the reasons discussed with respect to Claim 12. EX-1003, ¶117.

r. **Claim 31**

- i. [31.0] An electronic apparatus according to claim 30, wherein the second integrated circuit die is derived from a second semiconductor wafer comprised of other one of Si, SiGe, GaAs, InP, and GaN.*

Garlepp discloses this limitation for the reasons discussed with respect to Claim 13. EX-1003, ¶118.

B. Ground 2: Claims 1-2, 6, 10-15, 18-20, 23-26, and 29-31 are obvious under 35 U.S.C. §103(a) over Magoon in View of Ngompe.

1. Magoon

Magoon discloses a quadband RF transceiver BiCMOS chip for GSM/GPRS 850/900/1800/1900 applications “that integrates all of the functions necessary to implement a multiband homodyne global system for mobile telecommunication radio except for the power amplifier (PA) and radio frequency (RF) passives”. EX-1006, p.1710 (Abstract). *Magoon* is directed to the same goal as the ’200 Patent, *e.g.*, increasing the level of circuit integration, while reducing costs and size. EX-1003, ¶119. According to *Magoon*:

As modern cellphones become ubiquitous, the critical factors in their manufacture become cost, size, and time to market. The high integration of radio ICs reduces board area and complexity while cutting component cost and system design time.

EX-1006, p.1710 (Section I); EX-1003, ¶120.

Magoon discloses the same solution as the '200 Patent: partitioning signal conditioning circuits along their signal paths and integrating the partitions within different semiconductor dies. The receive circuitry is integrated within a silicon-based BiCMOS transceiver chip, while the transmit circuitry is partitioned into a transmit section on the same BiCMOS chip and an off-chip PA circuitry. EX-1006, p.1710 (Abstract), p.1718-19 (Section VII), Fig. 20. While *Magoon* does not provide details about the off-chip PA circuitry, as discussed in more detail below, a POSITA understood that the circuitry was formed in a semiconductor die. EX-1003, ¶120.

Annotated Fig. 1 illustrates the architecture of *Magoon*'s transceiver, including the transceiver chip and the off-chip PA circuitry:

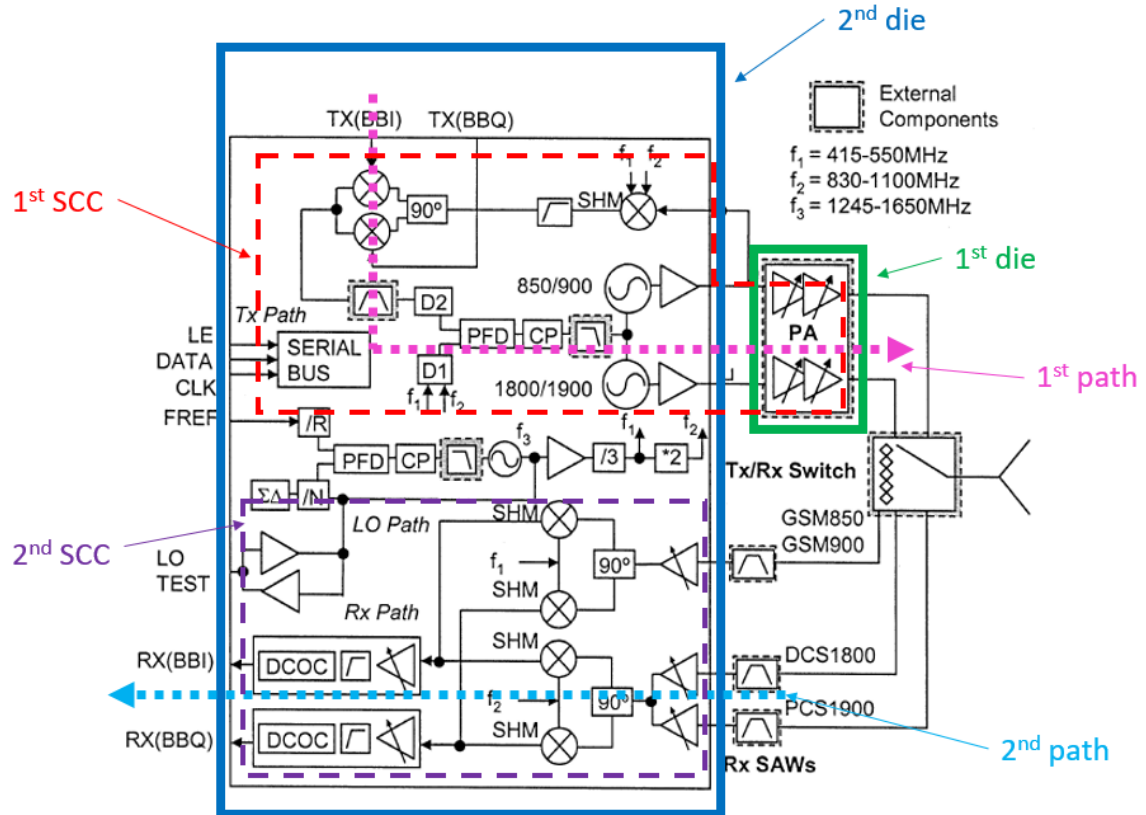


Fig. 1. Top-level schematic of transceiver, with external RF components.

EX-1006, Annotated Fig. 1; EX-1003, ¶121.

The transceiver chip includes a receive (Rx) path (*second signal path*) and a transmit (Tx) path (*first signal path*). Receive signal conditioning circuitry along the receive path receives RF signals on pins or bond-wires at the inputs of the low-noise amplifiers (LNAs) and provides baseband receive signals (RX(BBI), RX(BBQ)) at output pins or bond-wires. EX-1006, p.1710 (Section II), Fig. 1.

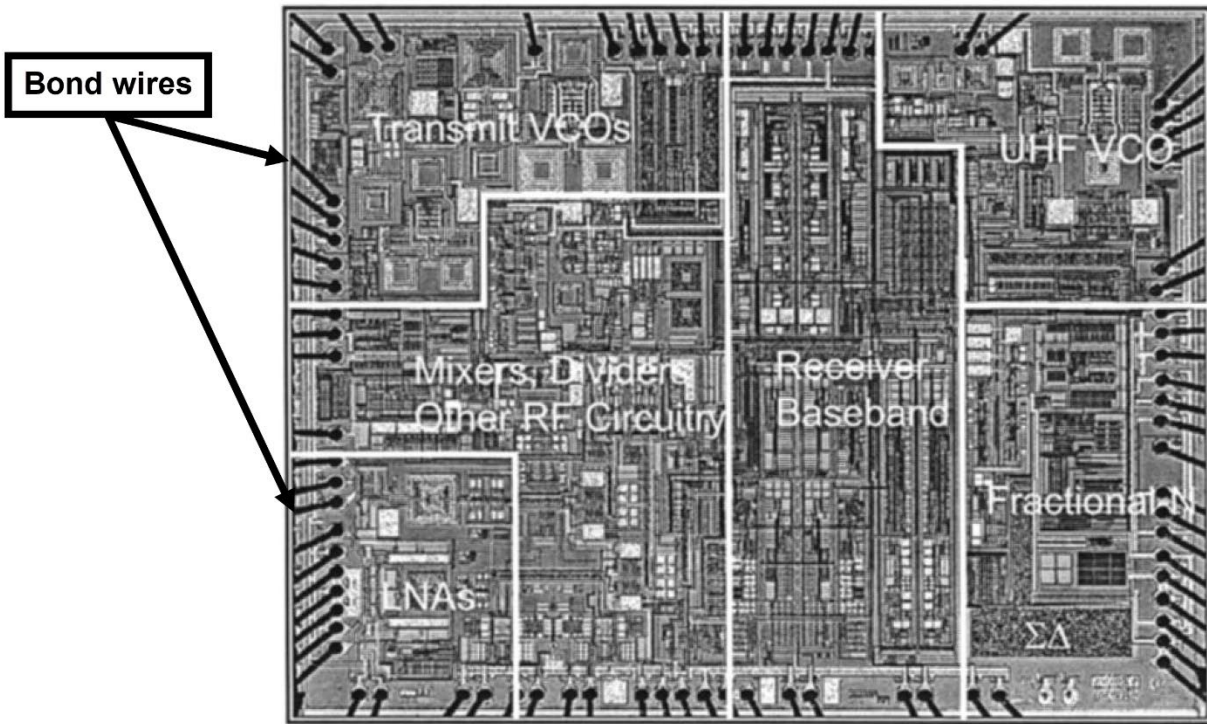


Fig. 20. Microphotograph of transceiver.

EX-1006, Fig. 20 (annotated); EX-1003, ¶122.

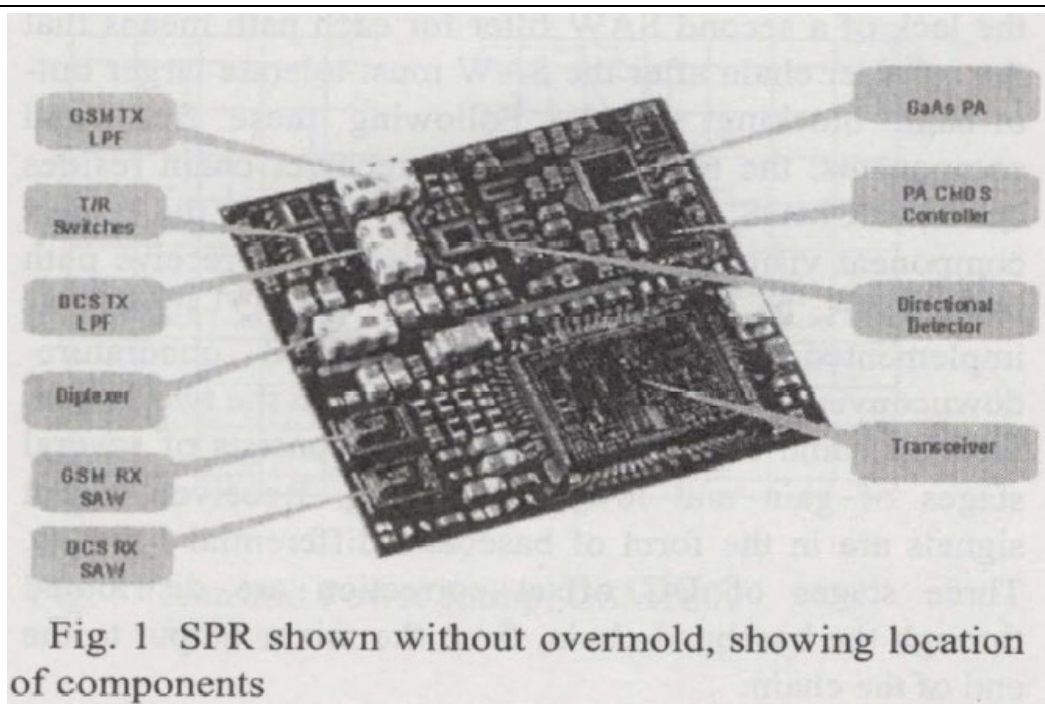
The portion of the transmit signal conditioning circuitry along the **transmit path** on the transceiver chip receives baseband transmit signals at the input and provides RF signals at output pins or bond-wires to the off-chip PA circuitry. EX-1006, p.1710 (Section II). The off-chip PA circuitry (which is another portion of the transmit signal conditioning circuitry) provides amplified RF signals for transmission via an antenna. EX-1003, ¶123.

Thus, just like the '200 Patent, *Magoon* discloses two interconnected semiconductor devices and two signal conditioning circuits along two signal paths. One signal conditioning circuit (the receiver circuitry) resides entirely within one

die, while the other signal conditioning circuit (the transmitter circuitry) is partitioned between both dies for the same purpose as described in the '200 Patent, e.g., to take advantage of the beneficial attributes of both semiconductor substrates, including the well-known attribute of using silicon-based BiCMOS for higher levels of integration of high performance RF components (such as LNAs) and a different semiconductor technology best suited for PAs. EX-1003, ¶124.

2. Ngompe

Ngompe discloses a single-package radio (SPR) module for a cellular handset that “realizes all the RF functions required for the dual-band GSM [900/1800] application.” EX-1007, p.387 (Abstract). Like the '200 Patent's module and *Magoon*, the SPR module is implemented on a substrate that supports and interconnects multiple components where “[d]iverse die technologies are utilized to apply the optimum process for each function.” *Id.* The SPR module is shown in Fig. 1:



EX-1007, Fig. 1 (annotated); EX-1003, ¶125.

Ngompe discloses: “The assembly consists of a combination of chip-on-board with wire bonding, and reflow-soldered SMT components.” EX-1007, p.387. Among other components, the SPR module includes a BiCMOS transceiver die and a GaAs HBT PA. EX-1007, p.387 (Abstract), Fig. 1. EX-1003, ¶126.

Ngompe’s BiCMOS transceiver die includes substantially the same receive and transmit circuitry as *Magoon*’s BiCMOS transceiver die, with the exception that *Ngompe*’s dualband transceiver covers 900 MHz and 1800 MHz applications while *Magoon*’s quadband transceiver further covers 850 MHz and 1900 MHz. Specifically, the receive circuitry in both transceiver dies follows a direct-conversion architecture, and the transmit circuitry includes an up conversion phase

locked loop (PLL) chain with on-chip voltage controlled oscillators (VCOs) to drive the off-chip PAs. *Compare* EX-1006, Abstract & Fig. 1 *with* EX-1007, Abstract & Fig. 2. EX-1003, ¶127.

3. Motivation to Combine

The authors of both *Magoon* and *Ngompe* were with Skyworks Solutions, Inc., the Patent Owner. EX-1006, p.1710; EX-1007, p.387; EX-1003, ¶128. *Magoon* teaches a quadband RF transceiver that includes a silicon-based BiCMOS transceiver chip and off-chip PA circuitry, but does not provide the details of the off-chip PA. *Ngompe* teaches a “single package radio” (SPR) module implemented as a dualband RF transceiver that includes a BiCMOS transceiver chip and off-chip GaAs PA chip mounted on and interconnected by a common substrate. *Ngompe* discloses “[d]iverse die technologies are utilized to apply the optimum process for each function.” EX-1007, p.387 (Abstract). EX-1003, ¶128.

First, it would have been obvious to combine *Magoon* with *Ngompe*’s teachings to achieve a “single package radio” with *Magoon*’s BiCMOS chip and PA circuitry mounted on and interconnected by a common substrate. *Ngompe* discloses that its SPR solution is “implemented on a low cost 4-layer laminate substrate” and “makes use of multiple semiconductor and packaging technologies to condense” the size of the complete radio. P.387 (Abstract); P.390 (Conclusion). *Magoon* teaches that as “cell phones become ubiquitous, the critical factors in their

manufacture become cost, size, and time to market.” P.1710 (Introduction). A POSITA would have been motivated to apply the express semiconductor die and packaging teachings of *Ngompe* to *Magoon*’s known RF transceiver to achieve a high-performance, low cost, condensed size SPR solution with a fast time to market, particularly given that *Ngompe* and *Magoon* utilize the same type of transceiver design for the same types of RF applications (with the exception that *Ngompe*’s transceiver includes circuitry for only two of the RF bands covered by *Magoon*’s transceiver). EX-1003, ¶129.

Second, as discussed in the State of the Art, *supra*, doing so would have been nothing more than applying known multi-chip packaging techniques to a known RF transceiver to achieve a predictable result. EX-1008, ¶5 (packaging of multiple diverse semiconductor dies on a common laminate substrate was “conventional”); EX-1009 (Section 3) (disclosing “single-package solution” for a RF transceiver having GaAs and silicon chips mounted on a common substrate); EX-1013, FIG. 7, 7:4-22; EX-1014, 1:1-28. EX-1003, ¶130.

Moreover, a POSITA would have had a reasonable expectation of success in combining *Ngompe*’s packaging solution with *Magoon*’s RF transceiver. Doing so would involve no more than routine skill to achieve predictable results, as demonstrated in the State of the Art, *supra*. EX-1008, ¶5; EX-1009 (Section 3); EX-1013, FIG. 7, 7:4-22. EX-1003, ¶131.

4. Detailed Application of *Magoon* in View of *Ngompe* to the Challenged Claims

a. Claim 1

i. [1.0] An electronic apparatus comprising:

To the extent the preamble is limiting, *Magoon* discloses an “RF transceiver” (*an electronic apparatus*). EX-1006, p.1710; Fig. 1.

ii. **[1.1] a first integrated circuit semiconductor die comprising:**

Magoon in view of *Ngompe* discloses this limitation. EX-1003, ¶133.

Magoon discloses a quadband radio transceiver that includes **power amplifier circuitry** and a **BiCMOS chip**. EX-1006, p.1710 (Abstract).

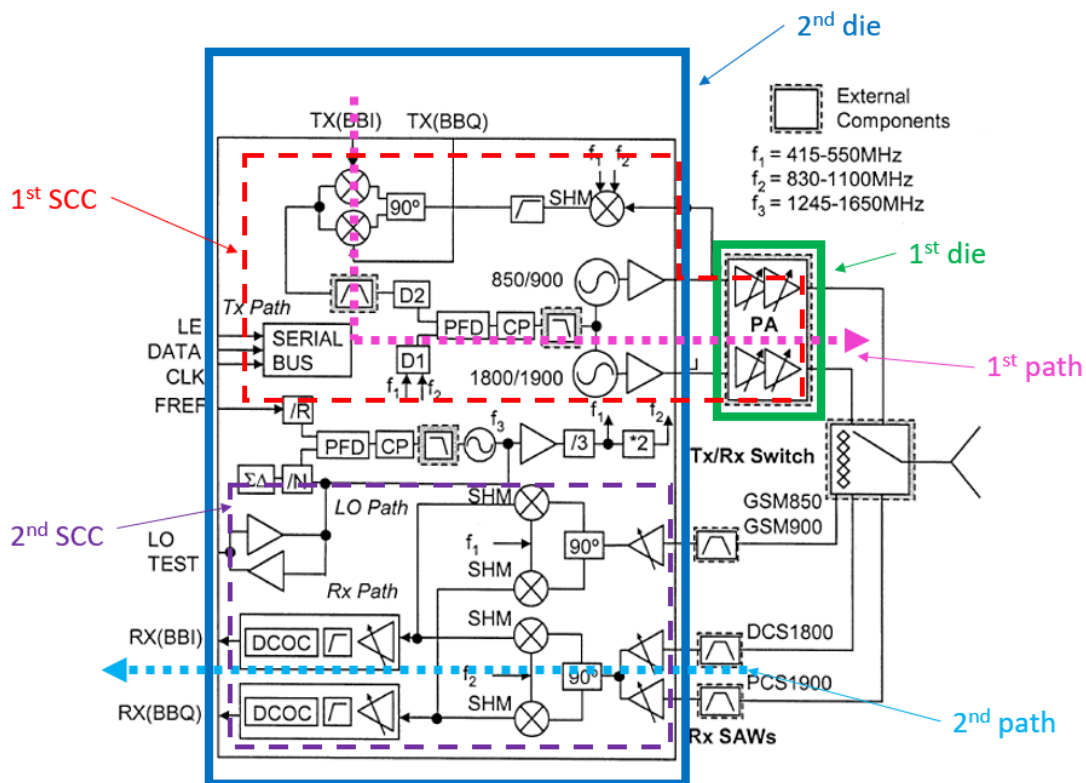


Fig. 1. Top-level schematic of transceiver, with external RF components.

EX-1006, Fig. 1 (annotated); EX-1003, ¶134.

Magoon does not expressly disclose that the PA circuitry in Fig. 1 includes at least one *integrated circuit semiconductor die*. EX-1003, ¶134.

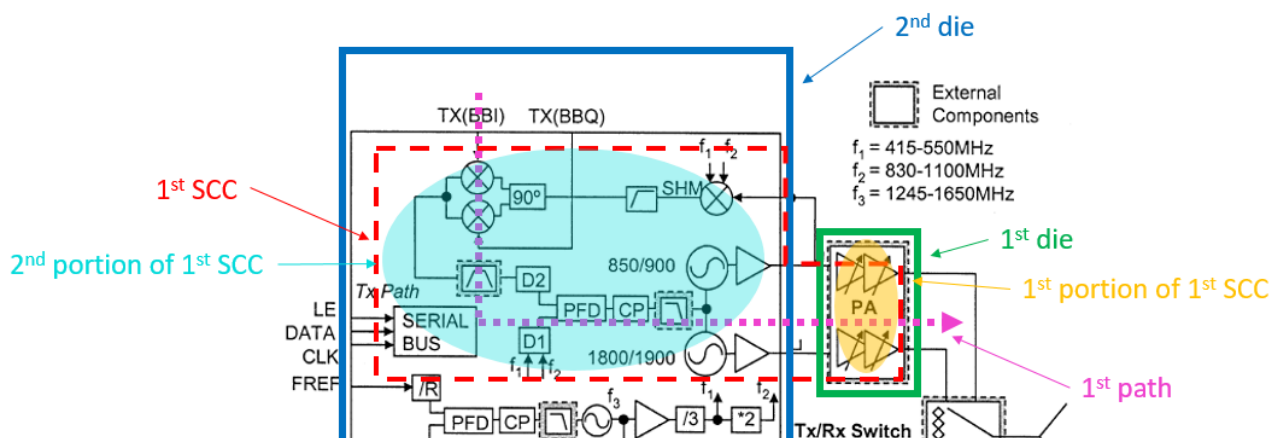
Ngompe discloses an SPR module having a BiCMOS transceiver die that includes a transmitter section “to drive the GaAs HBT PA” (*an integrated circuit semiconductor die*). EX-1007, p.388 (Section III), p.387 (Fig. 1). A POSITA would be motivated to implement *Magoon*’s PA circuitry on a semiconductor die, as taught by *Ngompe*, to reduce module size, increase performance, and reduce time to market. Doing so would be nothing more than applying conventional processes in widely known manners. EX-1003, ¶135. Moreover, as discussed in the State of the Art, *supra*, a POSITA understood that it was common to implement PA circuitry on a GaAs semiconductor die to partition the system into its subsystems, each realized in the most suitable technology, to provide the known benefit of optimal performance, lower cost, and increased manufacturing yield. EX-1008, ¶¶5, 25; EX-1009, Figs. 4, 5, Sections 3, 4; EX-1011, p.1037. EX-1003, ¶135.

- iii. ***[1.2] a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path; and***

Magoon discloses a **Tx Path** (*first signal path*) made up of an “**up-conversion transmit phase-locked loop (PLL) including on chip transmit voltage-controlled oscillators (VCOs)**” (*second portion of first SCC*) to provide signals to

power amplifier (PA) circuitry (*first portion of first SCC*). EX-1006, p.1710, Fig.

1. EX-1003, ¶136.



EX-1006, Fig. 1 (annotated); EX-1003, ¶136.

A POSITA understood that the functions performed by the transmit PLLs/VCOs (frequency conversion) and PA circuitry (amplification) condition the transmit signal as it propagates along the Tx path. These functions are “signal conditioning” because the signals are processed / altered (i.e., frequency converted and amplified) by the various stages of the transmit path circuitry to prepare the signals for the next stage in the transmit path. EX-1003, ¶136 (citing EX-1016). *Magoon* therefore discloses that the transmit PLLs/VCOs and PA circuitry together form a *first signal conditioning circuit* (“SCC”) disposed along a *first signal path*, and the PA circuitry is a *first portion of the first SCC*. EX-1003, ¶136.

iv. **[1.3] a second integrated circuit semiconductor die comprising;**

Magoon discloses a “BiCMOS chip” (*second integrated circuit semiconductor die*). EX-1006, p.1710 (Abstract). EX-1003, ¶137.

- v. ***[1.4] a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first portion of a first signal conditioning circuit for a signal propagating along the first signal path; and,***

Magoon discloses transmit PLLs/VCOs (*second portion*) disposed along a TX path (*first signal path*) on the BiCMOS chip (*second die*). EX-1006, pp.1710, 1717 (Section V), Fig. 1. EX-1003, ¶138. For the reasons explained above for [1.2], a POSITA understood the transmit PLLs/VCOs to perform signal conditioning functions along with the PA circuitry (*first portion*) on signals propagating along the TX path (*first signal path*). EX-1003, ¶138.

- vi. ***[1.5] a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.***

Magoon in view of Ngompe discloses this limitation. EX-1003, ¶139.

Magoon discloses that a benefit of its complete LO integration is “that the only RF signals present on pins or bond wires are the received inputs at the LNAs and the transmitted outputs to the PA.” EX-1006, p.1710 (Section II). The inputs to the LNAs and the outputs to the PA described by Magoon are for providing

electrical connection to and from the BiCMOS transceiver die (second integrated circuit semiconductor die) and the PA circuitry (first integrated circuit semiconductor die). EX-1006, Fig. 20 (showing bond wires on transceiver chip). Ngompe discloses an SPR module including a “BiCMOS transceiver die” (*second integrated circuit die*) and a “GaAs HBT power amplifier” (*first integrated circuit die*) that are supported on a “lamineate *substrate*.” The “assembly consists of a combination of chip-on-board with wire bonding” to provide for electrical interconnection between the transceiver die and the PA die. EX-1007, p.387 (Abstract, Section II, Fig. 1), p.388 (Section II). As explained above, a POSITA would be motivated to combine Ngompe’s express packaging teachings with Magoon. See §VII.B.3, *supra*. Doing so would have been nothing more than the application of a known solution to achieve a known and predictable result with a reasonable expectation of success. EX-1008 ¶¶5, 35, 36; EX-1009 (Section 3); EX-1013, FIG. 7, 7:4-22; EX-1014, 1:1-28. EX-1003, ¶140.

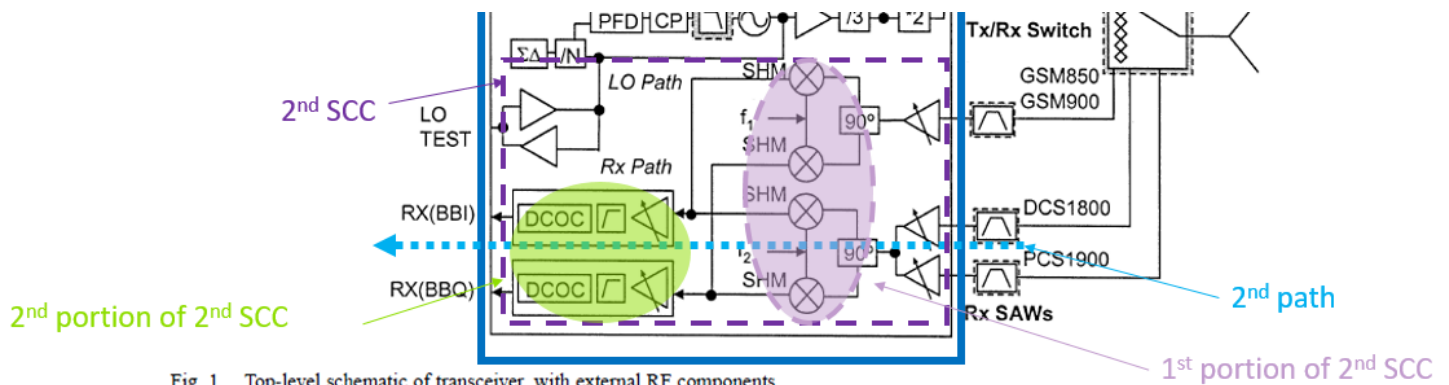
b. Claim 2

- i. [2.0] An electronic apparatus according to claim 1, comprising a second signal conditioning circuit comprising a first portion of the second signal conditioning circuit and a second portion of the second signal conditioning circuit integrated within the second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path.*

Magoon discloses that the BiCMOS chip (second die) includes a “receive path” / “Rx Path” (second signal path) that:

consists of three single-ended low-noise amplifiers (LNAs) that drive two sets of quadrature subharmonic mixers (SHMs) whose outputs are combined in a common I/Q analog baseband chain. The baseband chains include low-pass channel select filtering, programmable gain, and dc offset correction.

EX-1006, p.1710 (Section II); Fig. 1. EX-1003, ¶141.



EX-1006, Fig. 1(annotated). EX-1003, ¶142.

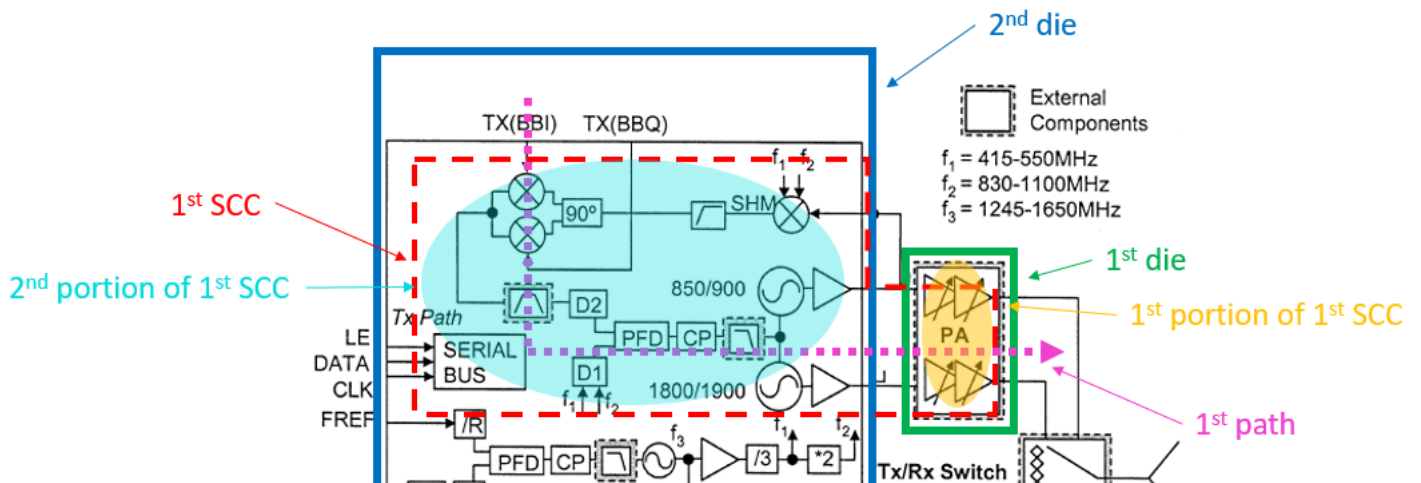
A POSITA understood that functions performed by the circuitry along the Rx Path are “signal conditioning” because the signals are processed / altered (i.e., amplified, mixed, filtered, and corrected) by the various stages of the receive path circuitry to prepare the signals for the next stage in the receive path. EX-1003, ¶142 (citing EX-1016). Magoon therefore discloses that the receive path circuitry is a *second signal conditioning circuit* disposed along a *second signal path*, and the

LNAs and SHMs are a *first portion* of the *second signal conditioning circuit*. EX-1003, ¶142.

c. **Claim 6**

- i. ***[6.0] An electronic apparatus according to claim 1, wherein the first portion of the first signal conditioning circuit comprises at least a power amplifier circuit and where the function of the first portion of the first signal conditioning circuit is for amplifying of an input signal using the at least a power amplifier circuit.***

Magoon discloses that the **transmitter path circuitry** (*first SCC*) includes **PA circuitry** (*first portion*) having multi-stage PA circuitry (*power amplifier circuit*) for amplifying the signals received from the **on-chip transmit section** (*second portion*). EX-1006, pp.1710-1711 (Section II); EX-1003, ¶143.



EX-1006, Fig. 1(annotated); EX-1003, ¶143.

Magoon's disclosure of multi-stage PA circuitry in Fig. 1 is a disclosure of a power amplifier circuit that performs the function of *amplifying an input signal*.

EX-1003, ¶143.

d. Claim 10

- i. [10.0] An electronic apparatus according to claim 2, wherein the first semiconductor process does not facilitate manufacturing and integration of at least one of the second portion of the first signal conditioning circuit and the second portion of the second signal conditioning circuit.*

Magoon in view of *Ngompe* discloses this limitation. EX-1003, ¶144.

Magoon discloses that the transceiver chip (*second die*), which includes a transmit section (*second portion of first SCC*) and the baseband chains of the receive path circuitry (*second portion of second SCC*), is made using a silicon-based BiCMOS process. EX-1006, Sections II, VII. However, *Magoon* does not expressly disclose a particular semiconductor process for manufacturing the PA circuitry. EX-1003, ¶145.

Ngompe discloses a BiCMOS transceiver chip and a GaAs HBT PA. EX-1007, p.387 (Fig. 1), p. 388 (Section III). *Ngompe* discloses: “Diverse die technologies are utilized to apply the optimum process for each function.” EX-1007, p.387 (Abstract, Fig. 1). A POSITA would have been motivated to use different semiconductor process technologies for *Magoon's* transceiver chip and PA circuitry, respectively, as taught by *Ngompe* to optimize the manufacturing of

each of the transceiver circuitry and PA circuitry and to enhance performance in a known and predictable manner. This teaching is consistent with the disclosure in the '200 Patent that using the most suitable semiconductor technology is “an optimization task” to achieve known and predictable benefits. EX-1001, Abstract, 10:52-57. EX-1003, ¶146.

e. **Claim 11**

- i. ***[11.0] An electronic apparatus according to claim 1, wherein the second integrated circuit die is manufactured using a second semiconductor process that is different from that used to manufacture the first integrated circuit die.***

Magoon view of *Ngompe* discloses this limitation for reasons discussed with respect to Claim 10. EX-1003, ¶147.

f. **Claim 12**

- i. ***[12.0] An electronic apparatus according to claim 1, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.***

Magoon in view of *Ngompe* discloses this limitation for reasons discussed with respect to Claim 10. Specifically, *Ngompe* discloses a GaAs HBT PA. EX-1007, p.387 (Fig. 1), p. 388 (Section III). EX-1003, ¶148.

g. **Claim 13**

- i. ***[13.0] An electronic apparatus according to claim 12, wherein the second integrated circuit die is derived from a second semiconductor wafer***

comprised of other one of Si, SiGe, GaAs, InP, and GaN.

Magoon in view of *Ngompe* discloses this limitation for reasons discussed with respect to Claim 10. EX-1003, ¶149.

h. Claim 14

i. An electronic apparatus according to claim 1, wherein the first integrated circuit die is manufactured using a BiCMOS process.

Magoon does not expressly disclose a semiconductor process for manufacturing the PAs (*first die*). EX-1003, ¶150.

As discussed in the State of the Art, *supra*, the use of a BiCMOS process to manufacture PAs was known in the RF industry. For example, the '200 Patent discloses that “[r]ecent advances in SiGe BiCMOS technology have allowed for progressively higher levels of integration of high-performance RF components,” including PAs. EX-1001, 1:56-63. A POSITA would be motivated to manufacture *Magoon*’s PA circuitry using the semiconductor process best suited for the functionality of the PA, and BiCMOS would have been a known design choice to achieve a predictable result. Further, a POSITA understood that separating the components between first and second dies made using a BiCMOS process avoids interference that could occur if the components were on a single BiCMOS die. EX-1003, ¶151.

i. Claim 15

- i. [15.0] An electronic apparatus according to claim 1, wherein the second portion of the first signal conditioning circuit comprises at least one of a capacitor and an inductors and a signal transmission line.*

Magoon discloses transmit section (*second portion of first SCC*) on the BiCMOS chip includes PLLs and VCOs. Capacitors and inductors are basic elements of PLL and VCO circuits and, conventionally, are integrated in the die with the other components of the PLL and VCO circuits. EX-1006, p.1719 (Section VII) (“The inductors were implemented in a 3-um-thick third metal layer. . . . MIM capacitors between the second and third metal layers...”). EX-1003, ¶152.

j. Claim 18

- i. [18.0]. A method of manufacturing a module comprising:*

To the extent the preamble is limiting, *Magoon* discloses this limitation for the reasons discussed with respect to Claim 1. EX-1003, ¶153.

- ii. [18.1] providing a first signal conditioning circuit comprising a first portion and a second portion;*

Magoon discloses this limitation for reasons discussed with respect to limitations [1.2] and [1.4]. EX-1003, ¶154.

- iii. [18.2] providing a second signal conditioning circuit comprising a first portion and a second portion;*

Magoon discloses this limitation for reasons discussed with respect to Claim 2. EX-1003, ¶155.

- iv. [18.3] implementing the first portion of the first signal conditioning circuit within a first semiconductor die;**

Magoon discloses this limitation for reasons discussed with respect to limitations [1.1] and [1.2]. EX-1003, ¶156.

- v. [18.4] implementing the second portion of the first signal conditioning circuit within a second semiconductor die;**

Magoon discloses this limitation for reasons discussed with respect to limitations [1.3] and [1.4]. EX-1003, ¶157.

- vi. [18.5] implementing the first and second portions of the second signal conditioning circuit in the second semiconductor die;**

Magoon discloses this limitation for reasons discussed with respect to Claim 2. EX-1003, ¶158.

- vii. [18.6] bonding the first and second dies to a common substrate; and,**

Magoon in view of *Ngompe* discloses this limitation for reasons discussed with respect to limitation [1.5]. Further, as discussed in the State of the Art, *supra*, manufacturing a multiple-die module by bonding dies to a common substrate was a well-known, conventional practice. EX-1008, ¶5; EX-1014, 1:1-28; EX-1013, FIG. 7, 7:4-22. EX-1003, ¶159.

- viii. *[18.7] forming electrical connections between the two dies to complete the first signal conditioning circuit from the first portion of the first signal conditioning circuit and the second portion of the first signal conditioning circuit.*

Magoon discloses this limitation for reasons discussed with respect to limitation [1.5]. EX-1003, ¶160.

k. **Claim 19**

- i. *A method according to claim 18, wherein the first semiconductor die comprises a first portion of a first signal path and the second semiconductor die comprises a second portion of the first signal path, the first signal path disposed between a first input port and a first output port.*

Magoon discloses this limitation for reasons discussed with respect to Claim 1. EX-1003, ¶161.

l. **Claim 20**

- i. *A method according to claim 19, wherein the second semiconductor die comprises a second signal path that is other than the second portion of the first signal path and in approximate RF isolation therefrom.*

Magoon discloses that the BiCMOS chip (*second die*) is laid out to reduce “the risk of unwanted coupling of signals between circuits.” EX-1006, p.1718 (Section VI.B). *Magoon* explains that the transmit VCOs on the Tx path (*second portion of first path*) and the LNAs on the Rx path (*second path*) are situated in the extreme corners of the die, as shown in the microphotograph below:

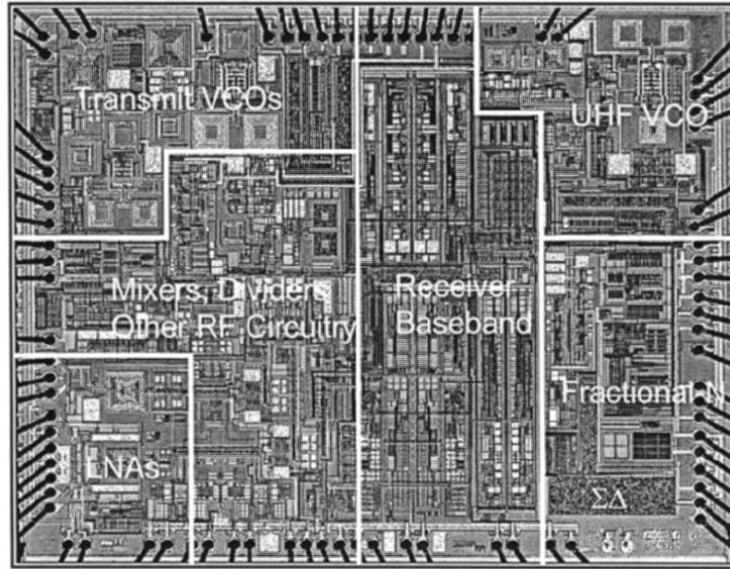


Fig. 20. Microphotograph of transceiver.

EX-1006, Fig. 20. EX-1003, ¶162.

By stating that the chip layout reduces unwanted coupling between the Tx path and the Rx path, *Magoon* is disclosing that the paths are in *approximate RF isolation therefrom*. EX-1003, ¶163.

m. Claim 23

- i. A method according to claim 18, wherein the first semiconductor die does not facilitate implementation of the second portion of the first signal conditioning circuit therein.*

Magoon in view *Ngompe* discloses this limitation for the reasons discussed with respect to Claim 10. EX-1003, ¶164.

n. Claim 24

- i. A method according to claim 18, wherein implementing of the second portion of the first signal conditioning circuit within the second*

semiconductor die provides increased performance in signal conditioning as compared to implementing of the second portion of the first signal conditioning circuit within the first semiconductor die.

Magoon in view of *Ngompe* discloses this limitation. EX-1003, ¶165.

Ngompe discloses an SPR module having a BiCMOS chip (*second die*) and a GaAs PA (*first die*) where “[d]iverse die technologies are utilized to apply the optimum process for each function.” EX-1007, p.387 (Abstract). A POSITA would be motivated to apply *Ngompe*’s express teachings to *Magoon*’s RF transceiver to increase performance in signal conditioning. Doing so would amount to applying known processes to a known apparatus to achieve a predictable result. EX-1003, ¶166.

o. Claim 25

- i. A method according to claim 18, wherein prior to implementing the first signal conditioning circuit comprises partitioning of the first signal conditioning circuit into the first portion and the second portion.***

Magoon in view of *Ngompe* discloses this limitation for the same reason as discussed with respect to Claim 1. EX-1003, ¶167.

p. Claim 26

- i. [26.0] An electronic apparatus comprising:***

Magoon discloses this limitation for reasons discussed with respect to

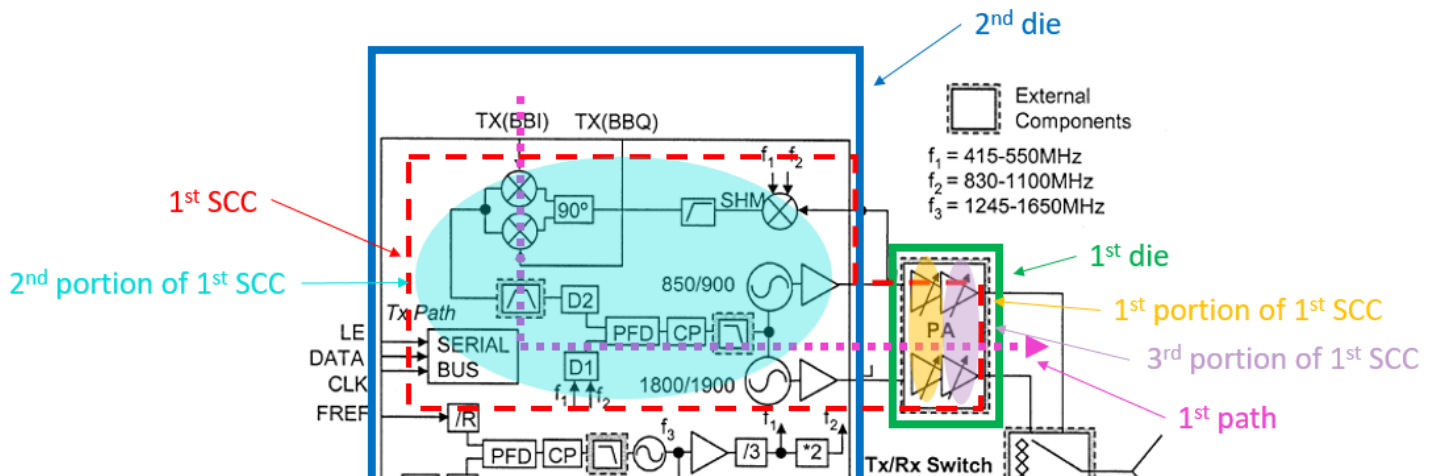
limitation [1.0]. EX-1003, ¶168.

ii. **[26.1] a first integrated circuit semiconductor die comprising:**

Magoon in view of *Ngompe* discloses this limitation for reasons discussed with respect to limitation [1.1]. EX-1003, ¶169.

iii. **[26.2] a first portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along a first signal path;**

Magoon in view of *Ngompe* discloses a quadband PA module that includes a 850/900 MHz PA branch and a 1800/1900 PA branch:



EX-1006, Fig. 1 (annotated); EX-1003, ¶170.

A POSITA reading *Magoon* understood that each branch includes multistage power amplifiers (as shown schematically in Fig. 1) and, thus, that each branch includes a first portion and a third portion of the first SCC. EX-1003, ¶170. See also disclosures for [1.2] above.

- iv. ***[26.3] a third portion of a first signal conditioning circuit integrated within the first integrated circuit die and disposed along the first signal path; and***

Magoon in view of *Ngompe* discloses this limitation for reasons discussed with respect to limitation [26.2]. EX-1003, ¶171.

- v. ***[26.4] a second integrated circuit semiconductor die comprising;***

Magoon discloses this limitation for reasons discussed with respect to limitation [1.3]. EX-1003, ¶172.

- vi. ***[26.5] a second portion of the first signal conditioning circuit integrated within the second integrated circuit die and disposed along the first signal path for performing a first signal conditioning function along with the first and third portions of the first signal conditioning circuit for a signal propagating along the first signal path; and,***

Magoon in view of *Ngompe* discloses this limitation for reasons discussed with respect to limitations [1.4] and [26.3]. EX-1003, ¶173.

- vii. ***[26.6] a substrate for supporting the first and second integrated circuit semiconductor dies and for providing electrical connection to and from the first and second integrated circuit semiconductor dies.***

Magoon in view of *Ngompe* discloses this limitation for reasons discussed with respect to limitation [1.5] above. EX-1003, ¶174.

q. **Claim 29**

- i. [29.0] An electronic apparatus according to claim 26, comprising a second signal conditioning circuit comprising a first portion of the second signal conditioning circuit and a second portion of the second signal conditioning circuit integrated within the second integrated circuit die for performing a second signal conditioning function on a signal propagating along a second signal path that is different than the first signal path.*

Magoon discloses this limitation for reasons discussed with respect to Claim

2. EX-1003, ¶175.

r. Claim 30

- i. [30.0] An electronic apparatus according to claim 26, wherein the first integrated circuit die is derived from a first semiconductor wafer comprised of one of Si, SiGe, GaAs, InP, and GaN.*

Magoon in view of *Ngompe* discloses this limitation for reasons discussed with respect to Claim 12. EX-1003, ¶176.

s. Claim 31

- i. [31.0] An electronic apparatus according to claim 30, wherein the second integrated circuit die is derived from a second semiconductor wafer comprised of other one of Si, SiGe, GaAs, InP, and GaN.*

Magoon discloses this limitation for reasons discussed with respect to Claim 13. EX-1003, ¶177.

IX. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Party-in-Interest (37 C.F.R. § 42.8(b)(1))

Petitioner certifies that the real party-in-interest in this Petition is Kangxi Communications Technologies.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

1. Judicial Matters

As of the filing date of this Petition and to the best knowledge of Petitioner, the '200 Patent is involved in the following litigation and investigation:

Case Heading	Number	Court	Date
<i>Skyworks Solutions, Inc. v. Kangxi Communication Technologies Shanghai Co., Ltd et al.</i>	CDCA-8-24-cv-00976	CDCA	May 6, 2024
<i>Wireless Front-End Modules, Devices Containing the Same, and Components Thereof</i>	Inv. No. 337-TA-3762	ITC	July 17, 2024

2. Administrative Matters

As of this Petition's filing date and to the best knowledge of Petitioner, the '200 Patent has not been subject to any *inter partes* reviews, reissues, or reexaminations.

3. Related Patents

To the best knowledge of Petitioner, the U.S. patent applications and U.S. patents related to the '200 Patent include U.S. Patent No. 7,754,539.

C. Lead/Back-up Counsel (37 C.F.R. § 42.8(b)(3)):

Petitioner provides the following designation of counsel:

Lead Counsel:

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In a concurrently filed Power of Attorney, Petitioner has granted Power of Attorney to Practitioners at Duane Morris LLP.

D. Notice of Service Information (37 C.F.R. § 42.8(b)(4)):

Please direct all correspondence to lead and back-up counsel at the above addresses. Petitioner consents to electronic service at the email addresses above.

X. CONCLUSION

Petitioner requests the Board institute IPR and cancel the Challenged Claims.

Respectfully submitted,

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ATTORNEY FOR PETITIONER

Dated: April 22, 2025.

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. §42.24 *et seq.*, the undersigned certifies that this document complies with the type-volume limitations. This document contains 12,362 words as calculated by the “Word Count” feature of Microsoft 365, the word processing program used to create it. Pursuant to 37 C.F.R. § 42.24(d), this word count excludes the table of contents, table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing.

Dated: April 22, 2025

/Diana M. Sangalli/

Diana M. Sangalli
Lead Counsel for Petitioner
Registration No. 40,798

CERTIFICATION OF SERVICE ON PATENT OWNER

Pursuant to 37 C.F.R. §§42.6(e), 42.8(b)(4) and 42.105, the undersigned certifies that on the April 22, 2025 a complete and entire copy of this Petition for *Inter Partes* Review of U.S. Patent 7,409,200 and all supporting exhibits were served via Federal Express, postage prepaid, to the correspondence address of record for the '200 Patent:

Date of service April 22, 2025

Manner of service FEDERAL EXPRESS

Documents served Petition for *Inter Partes* Review Under 35 U.S.C. § 312 and 37 C.F.R. § 42.104 of U.S. 8,446,823; Petitioner's Exhibit List; All Exhibits; Petitioner's Power of Attorney.

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