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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
17/374,789	07/13/2021	Zvi Tannenbaum	ZTANN.002P1C7	189449

Acknowledgement of Loss of Entitlement to Entity Status Discount

The entity status change request below filed through Private PAIR on 05/19/2023 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

X Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be notification of loss of entitlement to small or micro entity status, as applicable.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/Jordan M. Cox/
Name:	Jordan M. Cox
Registration Number:	70875

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/374,789	01/31/2023	11570034	ZTANN.002P1C7	1893

20995 7590 01/11/2023

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site http://pair.uspto.gov for additional inventors):

Zvi Tannenbaum, Palo Alto, CA;
Dean E. Dauger, Huntington Beach, CA;

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Advanced Cluster Systems, Inc., Newport Beach, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	17/374789
	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2447
(Multiple sheets used when necessary)	Examiner	Unassigned
SHEET 1 OF 12	Attorney Docket No.	ZTANN.002P1C7

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number *Number - Kind Code (if known)* Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	7,533,168	05-12-2009	Pabla et al.	
	2	2020/0153677 (Attorney Docket No. ZTANN.002P1C5) U.S. Application No. 16/449,084 and its entire prosecution history**	05-14-2020	Tannenbaum et al.	
	3	5,423,046	06-06-1995	Nunnelley et al.	
	4	5,881,315	03-09-1999	Cohen	
	5	5,930,768	07-27-1999	Hooban	
Change(s) applied to document, /C.S./ 12/13/2021	**6**	6,006,259 12/1999	~~11-28-1999~~	Adelman et al.	
	7	6,067,609	05-23-2000	Meeker et al.	
	8	6,074,427	06-13-2000	Fought et al.	
	9	6,108,699	08-22-2000	Moiin	
	10	6,195,680	02-27-2001	Goldszmidt et al.	
	11	6,202,080	03-13-2001	Lu et al.	
	12	6,546,403	04-08-2003	Carlson, Jr. et al.	
	13	6,578,068	06-10-2003	Bowman-Amuah	
	14	6,604,134	08-05-2003	Haury	
	15	6,691,216	02-10-2004	Kelly et al.	
	16	6,751,698	06-15-2004	Deneroff et al.	
	17	6,782,537	08-24-2004	Blackmore et al.	
	18	6,968,335	11-22-2005	Bayliss et al.	
	19	6,968,359	11-22-2005	Miller	
	20	7,031,944	04-18-2006	Tanioka	
	21	7,093,004	08-15-2006	Bernardin et al.	
	22	7,136,924	11-14-2006	Dauger	
	23	7,139,882	11-21-2006	Suzuoki et al.	
	24	7,174,381	02-06-2007	Gulko et al.	

Examiner Signature /HERMON ASRES/	Date Considered 11/20/2021

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.A./

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

First Inventor: Tannenbaum, Zvi	**Conf. No.:** 1893
App. No.: 17/374789	**Filed:** July 13, 2021
Examiner: Asres, Hermon	**Art Unit:** 2449
Title: CLUSTER COMPUTING	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

In response to the Notice of Allowance dated August 31, 2022, Applicant respectfully submits the following item:

Comments on Statement of Reasons for Allowance begin on page 2.

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

In response to the Examiner's Statement of Reasons for Allowance in the Notice of Allowance mailed on August 31, 2022 ("Reasons"), Applicant respectfully submits the following comments.

Applicant thanks the Examiner for the diligent examination of each of the pending claims and acknowledging the patentability thereof. Applicant wishes to point out that each claim is separately patentable based on the combination of features recited therein and not on any particular feature or group of features. Accordingly, to the extent that the Reasons omit claim elements, add claim elements, group claims together, or identify purportedly similar features or distinguishing features of a claim or a group of claims, Applicant respectfully disagrees with the Reasons. Additionally, to the extent that the Reason's paraphrasing of the subject matter of the claims deviates from the actual language recited in each individual claim, Applicant respectfully disagrees with the Reasons. Applicant respectfully disagrees with the Reasons to the extent there is any implication that the patentability of the dependent claims is dependent on, or these claims have the same scope as, the independent claim from which each depends. As noted above, patentability of each claim rests on each claim taken as a whole on its own merits. For dependent claims, their additional limitations may also provide additional reasons for patentability.

The Reasons (as well as other Office communications) characterize cited references. Applicant respectfully disagrees with the Reasons to the extent that such characterizations differ from the actual teachings of each of such references. Applicant also respectfully reserves the right to traverse the characterizations of what any particular reference shows or teaches, of what any combination of references shows or teaches, or the appropriateness of combining references in the future.

Applicant reserves the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the application's disclosure. Accordingly, reviewers of this or any child or related prosecution history shall not reasonably infer that Applicant has made any disclaimers or disavowals of any subject matter.

Applicant attaches herewith payment of the issue fee and requests that the application proceed to issuance. Should the Examiner have any concerns, the Examiner is invited to contact the undersigned at the telephone number below.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: November 29, 2022

By: /Jordan M. Cox/
Jordan M. Cox
Registration No. 70,875
Registered Practitioner
(949) 760-0404

56230795

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20995 7590 08/31/2022
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/374,789	07/13/2021	Zvi Tannenbaum	ZTANN.002P1C7	1893

TITLE OF INVENTION: CLUSTER COMPUTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	11/30/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
ASRES, HERMON	2449	709-223000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Knobbe, Martens,
2 Olson & Bear, LLP
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Advanced Cluster Systems, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Newport Beach, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ☑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ☑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

☑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 11-1410

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Jordan M. Cox/ Date 11/28/2022

Typed or printed name Jordan M. Cox Registration No. 70,875

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/374,789	**11/29/2022 06:34:40 PM ET**	**ZTANN.002P1C7**

Title of Invention

CLUSTER COMPUTING

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	1893	FILED BY	Eiko Fukuda
PATENT CENTER #	61230645	FILING DATE	07/13/2021
CUSTOMER #	20995	FIRST NAMED INVENTOR	Zvi Tannenbaum
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Jordan Cox

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
2022-09-01 Comments on Reason of Allowance - ZTANN.002P1C7.pdf	3	Post Allowance Communication - Incoming	81 KB
2022-09-01 Issue Fee - ZTANN.002P1C7.pdf	1	Issue Fee Payment (PTO-85B)	182 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
2022-09-01 Comments on	8113396D374A33105DFB177A54E957BE8E1BBB394A23E0B6E

Reason of Allowance - ZTANN.002P1C7.pdf	693527C4FF233397115A0389FB1BBB669DB77775233CD735502A5CDFA584CC3C91D6B16A02005A0
2022-09-01 Issue Fee - ZTANN.002P1C7.pdf	6BE2823325017CB22BAA9D34722C31BE4DDC0F3C31D5F535097FED4ADC18CB6357656425EE562C1069BF517E149CF51AA2FA285F4F6E04A99D348CA515EA9485

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/374,789	11/29/2022 06:34:40 PM ET	ZTANN.002P1C7

Title of Invention

CLUSTER COMPUTING

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	1893	FILED BY	Eiko Fukuda
PATENT CENTER #	61230645	AUTHORIZED BY	Jordan Cox
CUSTOMER #	20995	FILING DATE	07/13/2021
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Zvi Tannenbaum

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 2564	E2022ASI36062242	Evelyn Salcido

PRE-AUTHORIZED ACCOUNT	PRE-AUTHORIZED CATEGORY
111410	37 CFR 1.16 (National application filing, search, and examination fees); 37 CFR 1.17 (Patent application and reexamination processing fees)

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2501	UTILITY ISSUE FEE	600.00	1	600.00
			TOTAL AMOUNT:	$600.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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New International Application Filed with the USPTO as a Receiving Office

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/374,789	07/13/2021	Zvi Tannenbaum	ZTANN.002P1C7	1893

20995 7590 11/21/2022

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
ASRES, HERMON	

ART UNIT	PAPER NUMBER
2449	

NOTIFICATION DATE	DELIVERY MODE
11/21/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

efiling@knobbe.com
jayna.cartee@knobbe.com

Notice of Allowability	Application No. 17/374,789	Applicant(s) Tannenbaum et al.	
	Examiner HERMON ASRES	Art Unit 2449	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 11/07/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 2-31 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HERMON ASRES/
Primary Examiner, Art Unit 2449

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	17/374789
	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
(Multiple sheets used when necessary)	Examiner	Asres, Hermon
SHEET 1 OF 1	Attorney Docket No.	ZTANN.002P1C7

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number *Number - Kind Code (if known)* Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	2002/0013832	01-31-2002	Hubbard	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document *Country Code-Number-Kind Code* Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T[1]
	2	EP 1 501 013	01-26-2005	Toshiba KK		

56557504

Examiner Signature /HERMON ASRES/	Date Considered 11/17/2022

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.A./

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/374,789	11/07/2022 08:14:08 PM ET	ZTANN.002P1C7

Title of Invention

CLUSTER COMPUTING

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	1893	FILED BY	Eiko Fukuda
PATENT CENTER #	61153171	AUTHORIZED BY	Jordan Cox
CUSTOMER #	20995	FILING DATE	07/13/2021
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Zvi Tannenbaum

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 1990	E2022A7K15201126	Eiko Fukuda

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2806	SUBMISSION OF AN INFORMATION DISCLOSURE STATEMENT	130.00	1	130.00
			TOTAL AMOUNT:	$130.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
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Title of Invention

CLUSTER COMPUTING

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	1893	FILED BY	Eiko Fukuda
PATENT CENTER #	61153171	FILING DATE	07/13/2021
CUSTOMER #	20995	FIRST NAMED INVENTOR	Zvi Tannenbaum
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Jordan Cox

Documents

TOTAL DOCUMENTS: 0

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)

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New Applications Under 35 U.S.C. 111

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U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number *Number - Kind Code (if known)* Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	2002/0013832	01-31-2002	Hubbard	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document *Country Code-Number-Kind Code* Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	**T[1]**
	2	EP 1 501 013	01-26-2005	Toshiba KK		

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Examiner Signature	Date Considered
***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

T[1] - Place a check mark in this area when an English language Translation is attached.

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CUSTOMER #	20995	FIRST NAMED INVENTOR	Zvi Tannenbaum
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Jordan Cox

Documents

TOTAL DOCUMENTS: 3

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
2022-11-01 IDS List Form - ZTANN.002P1C7.pdf	1	Information Disclosure Statement (IDS) Form (SB08)	110 KB
Warning: This is not a USPTO supplied IDS fillable form. Data in the form cannot be automatically loaded to other USPTO systems.			
2022-11-04 IDS Transmittal - ZTANN.002P1C7.pdf	2	Transmittal Letter	79 KB
FOR_EP_1501013.pdf	55	Foreign Reference	7008 KB

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DOCUMENT	MESSAGE DIGEST(SHA-512)
2022-11-01 IDS List Form - ZTANN.002P1C7.pdf	636CDC461142464008FFC96A687B803CC20FDB0C838CF0CA63A7D26C79B26334AD9B0B7F14ED0759C67DB6CB6350C12D5B4DD2CAC0BCC06E76B4A4F0E1275120
2022-11-04 IDS Transmittal - ZTANN.002P1C7.pdf	86336380867DE71D5AABC95AE924718E95E1B4B575DA6FA354176D8AE9EB0A990A711AADCAFF060F3B1918A6D8652BAFF28EBC3BDA6EBE515EC46F39F7639AD0
FOR_EP_1501013.pdf	70AD3DAEA247E72C4F8A3E2136740F76CB8F3C363F522A19C018BCAED57EA81A513CA7829405745F499421DA5A6E0A7E302B2E6A4D5EF2AF63EAB3B3F07A51A0

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(54) Method and system for scheduling real-time periodic tasks

(57) An information processing system periodically performs a real-time operation including a plurality of chained tasks. The system includes a plurality of processors (12), a unit for dividing the chained tasks into a first task group and a second task group based on a relationship in order of execution among the tasks, the second task group being executed after the first task group, and a unit for performing a scheduling operation of periodically assigning each of the first task group and the second task group to at least one of the processors (12) to periodically execute the first task group at regular time intervals and periodically execute the second task group at the regular time intervals with a one-period delay relative to the first task group.

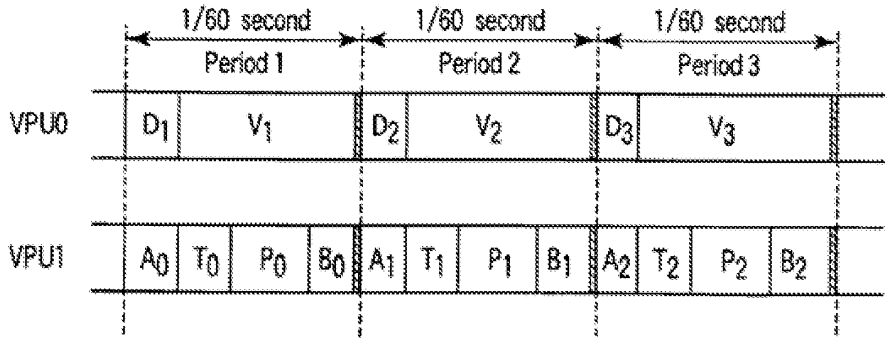


FIG. 11

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Description

[0001] The present invention relates to a scheduling method and an information processing system for periodically performing a real-time operation including a combination of a plurality of chained tasks.

[0002] Conventionally, computer systems such as server computers have utilized system architecture such as a multiprocessor and a parallel processor in order to improve in throughput. Both of the processors achieve a parallel computing operation using a plurality of processing units.

[0003] Jpn. Pat. Appln. KOKAI Publication No. 10-143380 discloses a system having a plurality of processing units. This system includes a single high-speed CPU, a plurality of low-speed CPUs and a shared memory. Processes are assigned to the high-speed and low-speed CPUs in consideration of parallelism and execution time of each process.

[0004] Jpn. Pat. Appln. KOKAI Publication No. 9-180025 discloses a scheduling technique of scheduling threads such that the same processor executes threads belonging to the same process.

[0005] Not only the computer system but also an embedded device that needs to process a large amount of data such as AV (audio video) data in real time has recently required that system architecture such as a multiprocessor and a parallel processor be introduced to improve in throughput.

[0006] Under the present circumstances, however, a real-time processing system that is predicated on the above system architecture is hardly reported.

[0007] In the real-time processing system, each operation needs completing within the limit of allowed time. In order to perform a real-time operation including a combination of a plurality of chained tasks periodically at regular time intervals, all the chained tasks need completing within the time interval of each period. However, they cannot be completed if the chained tasks of the real-time operation are long.

[0008] An object of the present invention is to provide a method and an information processing system capable of performing a real-time operation including a combination of a plurality of chained tasks with efficiency using a plurality of processors.

[0009] According to an embodiment of the present invention, there is provided a method of periodically performing a real-time operation including a plurality of chained tasks using a plurality of processors, the method comprising: dividing the chained tasks into a first task group and a second task group based on a relationship in order of execution among the tasks, the second task group being executed after the first task group; and performing a scheduling operation of periodically assigning each of the first task group and the second task group to at least one of the processors to periodically execute the first task group at regular time intervals and periodically execute the second task group at the regular time intervals with a one-period delay relative to the first task group.

[0010] This summary of the invention does not necessarily describe all necessary features so that the invention may also be a sub-combination of these described features.

[0011] The invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a block diagram showing an example of a computer system that configures a real-time processing system according to an embodiment of the present invention.

FIG. 2 is a block diagram of an MPU (master processing unit) and VPUs (versatile processing units) provided in the real-time processing system according to the embodiment of the present invention.

FIG. 3 is a diagram showing an example of a virtual address translation mechanism used in the real-time processing system according to the embodiment of the present invention.

FIG. 4 is a diagram showing an example of data mapped in real address space in the real-time processing system according to the embodiment of the present invention.

FIG. 5 is an illustration of effective address space, virtual address space and real address space in the real-time processing system according to the embodiment of the present invention.

FIG. 6 is a block diagram of a receiver for digital TV broadcast.

FIG. 7 is a diagram showing an example of a program module executed by the real-time processing system according to the embodiment of the present invention.

FIG. 8 is a table showing an example of a structural description included in the program module shown in FIG. 7.

FIG. 9 is a chart showing a flow of data among programs corresponding to the program module shown in FIG. 7.

FIG. 10 is a chart showing a parallel operation of the program module shown in FIG. 7, which is performed by two VPUs.

FIG. 11 is a chart showing a pipeline operation of the program module shown in FIG. 7, which is performed by two VPUs.

FIG. 12 is a diagram showing an example of an operating system in the real-time processing system according to the embodiment of the present invention.

FIG. 13 is a diagram showing another example of the operating system in the real-time processing system according to the embodiment of the present invention.

FIG. 14 is a diagram showing a relationship be-

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tween a virtual machine OS and a guest OS in the real-time processing system according to the embodiment of the present invention.

FIG. 15 is a chart showing resources that are time-divisionally assigned to a plurality of guest OSes in the real-time processing system according to the embodiment of the present invention.

FIG. 16 is a chart showing specific resources that are occupied by a specific guest OS in the real-time processing system according to the embodiment of the present invention.

FIG. 17 is a diagram of VPU runtime environment used as a scheduler in the real-time processing system according to the embodiment of the present invention.

FIG. 18 is a diagram showing an example of VPU runtime environment that is implemented in the virtual machine OS used in the real-time processing system according to the embodiment of the present invention.

FIG. 19 is a diagram showing an example of VPU runtime environment that is implemented as a guest OS used in the real-time processing system according to the embodiment of the present invention.

FIG. 20 is a diagram showing an example of VPU runtime environment that is implemented in each of the guest OSes used in the real-time processing system according to the embodiment of the present invention.

FIG. 21 is a diagram showing an example of VPU runtime environment that is implemented in one guest OS used in the real-time processing system according to the embodiment of the present invention.

FIG. 22 is an illustration of MPU-side VPU runtime environment and VPU-side VPU runtime environment used in the real-time processing system according to the embodiment of the present invention.

FIG. 23 is a flowchart showing a procedure performed by the VPU-side VPU runtime environment used in the real-time processing system according to the embodiment of the present invention.

FIG. 24 is a flowchart showing a procedure performed by the MPU-side VPU runtime environment used in the real-time processing system according to the embodiment of the present invention.

FIG. 25 is an illustration of threads belonging to a tightly coupled thread group and executed by different processors in the real-time processing system according to the embodiment of the present invention.

FIG. 26 is an illustration of interaction between tightly coupled threads in the real-time processing system according to the embodiment of the present invention.

FIG. 27 is an illustration of mapping of local storages of VPUs executing partner threads in effective address spaces of the tightly coupled threads in the real-time processing system according to the embodiment of the present invention.

FIG. 28 is an illustration of allocation of processors to threads belonging to a loosely coupled thread group in the real-time processing system according to the embodiment of the present invention.

FIG. 29 is an illustration of interaction between loosely coupled threads in the real-time processing system according to the embodiment of the present invention.

FIG. 30 is an illustration of a relationship between processes and threads in the real-time processing system according to the embodiment of the present invention.

FIG. 31 is a flowchart showing a procedure for performing a scheduling operation in the real-time processing system according to the embodiment of the present invention.

FIG. 32 is a diagram showing a state transition of threads in the real-time processing system according to the embodiment of the present invention.

FIG. 33 is a chart illustrating a relationship between a thread and its execution terms in the real-time processing system according to the embodiment of the present invention.

FIG. 34 is a chart of tightly coupled threads running at once in an execution term in the real-time processing system according to the embodiment of the present invention.

FIG. 35 is a chart showing a periodic execution model in the real-time processing system according to the embodiment of the present invention.

FIG. 36 is a chart showing an aperiodic execution model in the real-time processing system according to the embodiment of the present invention.

FIG. 37 is an illustration of a task graph.

FIG. 38 is an illustration of the principle of a reservation graph used in the real-time processing system according to the embodiment of the present invention.

FIG. 39 is an illustration of an example of a reservation graph used in the real-time processing system according to the embodiment of the present invention.

FIG. 40 is a diagram illustrating a hierarchical scheduler used in the real-time processing system according to the embodiment of the present invention.

FIG. 41 is a chart illustrating examples of parameters used for scheduling in the hard real-time class by the real-time processing system according to the embodiment of the present invention.

FIG. 42 is an illustration of absolute timing constraint used in the real-time processing system according to the embodiment of the present invention.

FIG. 43 is an illustration of relative timing constraint used in the real-time processing system according to the embodiment of the present invention.

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FIG. 44 is an illustration of mutual exclusive constraint used in the real-time processing system according to the embodiment of the present invention.

FIG. 45 is a table illustrating synchronization mechanisms in the real-time processing system according to the embodiment of the present invention.

FIG. 46 is a flowchart showing a procedure for selectively using the synchronization mechanisms in the real-time processing system according to the embodiment of the present invention.

FIG. 47 is a diagram showing an example of a reservation graph used in the real-time processing system according to the embodiment of the present invention.

FIG. 48 is a diagram showing an example of a reservation request created in the real-time processing system according to the embodiment of the present invention.

FIG. 49 is a chart showing an example of scheduling performed by the real-time processing system according to the embodiment of the present invention on the basis of the reservation request shown in FIG. 48.

FIG. 50 is a chart illustrating a first example of scheduling of software pipeline type performed by the real-time processing system according to the embodiment of the present invention.

FIG. 51 is a chart illustrating a second example of scheduling of software pipeline type performed by the real-time processing system according to the embodiment of the present invention.

FIG. 52 is a flowchart of procedures for the scheduling of software pipeline type performed by the real-time processing system according to the embodiment of the present invention.

FIG. 53 is a chart illustrating a third example of scheduling of software pipeline type performed by the real-time processing system according to the embodiment of the present invention.

FIG. 54 is a chart illustrating a first example of scheduling performed in consideration of the number of buffers by the real-time processing system according to the embodiment of the present invention.

FIG. 55 is a chart illustrating a second example of scheduling performed in consideration of the number of buffers by the real-time processing system according to the embodiment of the present invention.

FIG. 56 is a chart illustrating a third example of scheduling performed in consideration of the number of buffers by the real-time processing system according to the embodiment of the present invention.

FIG. 57 is a flowchart of procedures for the scheduling performed in consideration of the number of buffers by the real-time processing system according to the embodiment of the present invention.

FIG. 58 is a chart illustrating a fourth example of scheduling performed in consideration of the number of buffers by the real-time processing system according to the embodiment of the present invention.

FIG. 59 is a diagram showing an example of a reservation graph having a hierarchical structure used in the real-time processing system according to the embodiment of the present invention.

FIG. 60 is a diagram showing an example of a reservation request which is created by the real-time processing system according to the embodiment of the present invention and which takes into consideration of the tightly coupled thread group.

FIG. 61 is a chart showing an example of scheduling performed by the real-time processing system according to the embodiment of the present invention on the basis of the reservation request shown in FIG. 60.

FIG. 62 is a diagram showing an example of a reservation list used in the real-time processing system according to the embodiment of the present invention.

FIG. 63 is a flowchart showing a procedure for reserving an execution term in the real-time processing system according to the embodiment of the present invention.

[0012] An embodiment of the present invention will now be described with reference to the accompanying drawings.

[0013] FIG. 1 shows an example of a configuration of a computer system for achieving a real-time processing system according to an embodiment of the present invention. The computer system is an information processing system that performs various operations, which need to be done in real time, under timing constraint. The computer system can be used as not only a general-purpose computer but also an embedded system for various electronic devices to perform operations that need to be done in real time. Referring to FIG. 1, the computer system comprises an MPU (master processing unit) 11, a plurality of VPUs (versatile processing units) 12, a connecting device 13, a main memory 14 and an I/O (input/output) controller 15. The MPU 11, VPUs 12, main memory 14 and IO controller 15 are connected to each other by the connecting device 13. The connecting device 13 is formed of a bus or an inter-connection network such as a crossbar switch. If a bus is used for the connecting device 13, it can be shaped like a ring. The MPU 11 is a main processor that controls an operation of the computer system. The MPU 11 mainly executes an OS (operating system). The VPUs 12 and IO controller 15 can execute some functions of the OS. Each of the VPUs 12 is a processor for performing various operations under the control of the MPU 11. The MPU 11 distributes the operations (tasks) to the VPUs 12 in order to perform these operations

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(tasks) in parallel. The operations can thus be performed at high speed and with high efficiency. The main memory 14 is a storage device (shared memory) that is shared by the MPU 11, VPUs 12 and I/O controller 15. The main memory 14 stores the OS and application programs. The I/O controller 15 is connected to one or more I/O devices 16. The controller 15 is also referred to as a bridge device.

[0014] The connecting device 13 has a QoS (quality of service) function that guarantees a data transfer rate. The QoS function is fulfilled by transferring data through the connecting device 13 at a reserved bandwidth (transfer rate). The QoS function is used when write data is transmitted to the memory 14 from one VPU 12 at 5 Mbps or when it is done between one VPU 12 and another VPU 12 at 100 Mbps. Each of the VPUs 12 designates (reserves) a bandwidth (transfer rate) for the connecting device 13. The connecting device 13 assigns the designated bandwidth to the VPU 12 by priority. If a bandwidth is reserved for data transfer of a VPU 12, it is secured even though another VPU 12, MPU 11 or IO controller 15 transfers a large amount of data during the data transfer of the former VPU 12. The QoS function is particularly important to computers that perform real-time operations.

[0015] The computer system shown in FIG. 1 comprises one MPU 11, four VPUs 12, one memory 14 and one IO controller 15. The number of VPUs 12 is not limited. The system need not comprise any MPU and, in this case, one VPU 12 performs the operation of the MPU 11. In other words, one VPU 12 serves as a virtual MPU 11.

[0016] FIG. 2 shows an MPU 11 and VPUs 12. The MPU 11 includes a processing unit 21 and a memory management unit 22. The processing unit 21 accesses the memory 14 through the memory management unit 22. The memory management unit 22 performs a virtual memory management function and manages a cache memory in the memory management unit 22. Each of the VPUs 12 includes a processing unit 31, a local storage (local memory) 32 and a memory controller 33. The processing unit 31 can gain direct access to the local storage 32 in the same VPU 12. The memory controller 33 serves as a DMA (direct memory access) controller that transfers data between the local storage 32 and memory 14. The memory controller 33 utilizes the QoS function of the connecting device 13 and has a function of designating a bandwidth and that of inputting/outputting data at the designated bandwidth. The memory controller 33 also has the same virtual memory management function as that of the memory management unit 22 of the MPU 11. The processing unit 31 uses the local storage 32 as a main memory. The processing unit 31 does not gain direct access to the memory 14 but instructs the memory controller 33 to transfer the contents of the memory 14 to the local storage 32. The processing unit 31 accesses the local storage 32 to read/write data. Moreover, the processing unit 31 instructs the memory controller 33 to write the contents of the local storage 32 to the memory 14.

[0017] The memory management unit 22 of the MPU 11 and the memory controllers 33 of the VPUs 12 perform virtual memory management as shown in FIG. 3. The address viewed from the processing unit 21 of the MPU 11 or the memory controllers 33 of the VPUs 12 is a 64-bit address as indicated in the upper part of FIG. 3. In the 64-bit address, an upper 36-bit portion indicates a segment number, a middle 16-bit portion indicates a page number, and a lower 12-bit portion indicates a page offset. The memory management unit 22 and memory controllers 33 each include a segment table 50 and a page table 60. The segment table 50 and page table 60 convert the 64-bit address into the real address space that is actually accessed through the connecting device 13.

[0018] For example, the following data items are mapped in the real address (RA) space viewed from the MPU 11 and each VPU 12, as shown in FIG. 4.

1. Memory 14 (main storage device)
2. Control registers of MPU 11
3. Control registers of VPUs 12
4. Local storages of VPUs 12
5. Control registers of I/O devices (including control registers of I/O controller 15)

[0019] The MPU 11 and VPUs 12 can access any address in the real address space to read/write data items 1 to 5. It is particularly important to be able to access the real address space and thus access the local storage 32 of any VPU 12 from the MPU 11 and VPUs 12 and even from the I/O controller 15. Furthermore, the segment table 50 or page table 60 can prevent the contents of the local storage 32 of each VPU 12 from being read or written freely.

[0020] FIG. 5 shows memory address spaces managed by the virtual memory management function shown in FIG. 3. It is the EA (effective address) space that is viewed directly from the programs executed on the MPU 11 or VPUs 12. An effective address is mapped in the VA (virtual address) space by the segment table 50. A virtual address is mapped in the RA (real address) space by the page table 60. The RA space has a structure as shown in FIG. 4.

[0021] The MPU 11 can manage the VPUs 12 using a hardware mechanism such as a control register. For example, the MPU 11 can read/write data from/to the register of each VPU 12 and start/stop each VPU 12 to execute programs. Communication and synchronization between the MPU 11 and each of the VPUs 12 can be performed by means of a hardware mechanism such as a mailbox and an event flag, as can be communication and synchronization between the VPUs 12.

[0022] The computer system according to the present embodiment allows software to perform such an operation of an electric device that makes a stringent demand

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on real-time operations as conventionally implemented. For example, one VPU 12 carries out a computation corresponding to some hardware components that compose the electric device and concurrently another VPU 12 carries out a computation corresponding to other hardware components that compose the electric device.

[0023] FIG. 6 simply shows a hardware structure of a receiver for digital TV broadcast. In this receiver, a DEMUX (demultiplexer) circuit 101 divides a received broadcast signal into compressing-encoded data streams corresponding to audio data, video data and subtitle data. An A-DEC (audio decoder) circuit 102 decodes the compressing-encoded audio data stream. A V-DEC (video decoder) circuit 103 decodes the compressing-encoded video data stream. The decoded video data stream is sent to a PROG (progressive conversion) circuit 105 and converted into a progressive video signal. The progressive video signal is sent to a BLEND (image blending) circuit 106. A TEXT (subtitle data processing) circuit 104 converts the compressing-encoded subtitle data stream into a subtitle video signal and sends it to the BLEND circuit 106. The BLEND circuit 106 blends the video signal sent from the PROG circuit 105 and the subtitle video signal sent from the TEXT circuit 104 and outputs the blended signal as a video stream. A series of operations as described above is repeated at a video frame rate (e.g., 30, 32 or 60 frames per second).

[0024] In order to perform operations of the hardware shown in FIG. 6 by software, the present embodiment provides a program module 100 as shown in FIG. 7. The program module 100 is an application program for causing the computer system to perform the operations of the DEMUX circuit 101, A-DEC circuit 102, V-DEC circuit 103, TEXT circuit 104, PROG circuit 105 and BLEND circuit 106 shown in FIG. 6. The application program is described by multi-thread programming, and is structured as a group of threads for executing a real-time operation. The real-time operation includes a combination of a plurality of tasks. The program module 100 contains a plurality of programs (a plurality of routines) each executed as a thread. Specifically, the program module 100 contains a DEMUX program 111, an A-DEC program 112, a V-DEC program 113, a TEXT program 114, a PROG program 115 and a BLEND program 116. These programs 111 to 116 are programs describing procedures of tasks corresponding to operations (DMUX operation, A-DEC operation, V-DEC operation, TEXT operation, PROG operation, BLEND operation) of the circuits 101 to 106. More specifically, when the program module 100 runs, a thread corresponding to each of the programs 111 to 116 is generated, and dispatched to one or more VPUs 12 and executed thereon. A program corresponding to the thread dispatched to the VPU 12 is loaded to the local storage 32 of the VPU 12, and the thread executes the program on the local storage 32. The program module 100 is obtained by packaging the programs 111 to 116, which correspond to hardware modules for configuring a receiver for digital TV broadcast, with data called a structural description 117.

[0025] The structural description 117 is information indicative of how the programs (threads) in the program module 100 are combined and executed. The structural description 117 includes information indicative of a relationship in input/output (in chain) between chained programs 111 to 116 and costs (time) necessary for executing each of the programs 111 to 116. FIG. 8 shows an example of the structural description 117.

[0026] The structural description 117 shows modules (programs in the program module 100) each executed as a thread and their corresponding inputs, outputs, execution costs, and buffer sizes necessary for the outputs. For example, the V-DEC program of No. (3) receives the output of the DEMUX program of No. (1) as an input and transmits its output to the PROG program of No. (5). The buffer necessary for the output of the V-DEC program is 1 MB and the cost for executing the V-DEC program in itself is 50. The cost can be described in units of time (time period) necessary for executing the program, or step number of the program. It also can be described in units of time required for executing the program by a virtual processor having some virtual specifications. Since the VPU specifications and performance may vary from computer to computer, it is desirable to describe the cost in such virtual units. If the programs are executed according to the structural description 117 shown in FIG. 8, data flows among the programs as illustrated in FIG. 9.

[0027] The structural description 117 also shows coupling attribute information which indicates a coupling attribute between threads corresponding to the programs 111 to 116 as thread parameters. The coupling attribute includes two different attributes of a tightly coupled attribute and a loosely coupled attribute. A plurality of threads having the tightly coupled attribute are executed in cooperation with each other and referred to as a tightly coupled thread group. The computer system of the present embodiment schedules the threads belonging to each tightly coupled thread group such that the threads belonging to the same tightly coupled thread group can simultaneously be executed by different VPUs. A plurality of threads having the loosely coupled attribute is referred to as a loosely coupled thread group. A programmer can designate a coupling attribute between threads corresponding to the programs 11 to 16 using thread parameters. The tightly and loosely coupled thread groups will be described in detail with reference to FIG. 25 et seq. The thread parameters including the coupling attribute information can be described directly as codes in the programs 111 to 116, not as the structural description 117.

[0028] Referring to FIGS. 10 and 11, there now follows descriptions as to how the computer system of the present embodiment executes the programs 111 to 116. Assume here that the computer system includes two

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VPUs of VPU0 and VPU1. FIG. 10 shows time for assigning the programs to each of the VPUs when video data of 30 frames is displayed per second. Audio and video data for one frame is output within a time interval corresponding to one period. First, the VPU0 executes the DEMUX program to perform the DEMUX operation and writes its resultant audio, video and subtitle data to the buffers. After that, the VPU1 executes the A-DEC program and TEXT program to perform the A-DEC operation and the TEXT operation in sequence and writes their results to the buffers. Then, the VPU0 executes the V-DEC program to perform the V-DEC operation and writes its result to the buffer. The VPU0 executes the PROG program to perform the PROG operation and writes its result to the buffer. Since the VPU1 has already completed the TEXT program at this time, the VPU0 executes the last BLEND program to perform the BLEND operation, in order to create final video data. The above processing is repeated for every period.

[0029] An operation to determine which program is executed by each of the VPUs and when it is done to perform a desired operation without delay is called scheduling. A module to carry out the scheduling is called a scheduler. In the present embodiment, the scheduling is carried out based on the above structural description 117 contained in the program module 100. In the scheduling operation, both execution start timing and execution term of each of threads that execute the programs 111 to 116 are determined based on the structural description 117, thereby to assign each of the threads to one or more VPUs 12. The following operations are performed when the program module 100 is to be executed.

1. The operating system receives the program module 100 from an external storage or the memory 13, and reads a plurality of programs 111 to 116 and the structural description 117 from the program module 100.
2. Based on the structural description 117, the scheduler in the operating system determines both execution start timing and execution term of each of threads (DEMUX, V-DEC, A-DEC, TEXT, PROG and BLEND) for executing the programs 111 to 116 in the program module 100 to assign the threads (DEMUX, V-DEC, A-DEC, TEXT, PROG and BLEND) to one or more VPUs.

[0030] As described above, in the real-time processing system, the execution start timing and execution term of each of threads (DEMUX, V-DEC, A-DEC, TEXT, PROG and BLEND) that executes the chained programs 111 to 116 in the program module 100 are determined based on the structural description 117. Thus, the threads for performing a real-time operation can efficiently be scheduled without describing timing constraint conditions of each operation in codes of a program.

[0031] FIG. 11 shows the programs executed when video data of 60 frames is displayed per second. FIG. 11 differs from FIG. 10 as follows. In FIG. 11, data of 60 frames needs to be processed per second, whereas in FIG. 10, data of 30 frames is processed per second and thus data processing for one frame can be completed in one period (1/30 second). In other words, one-frame data processing cannot be completed in one period (1/60 second) and thus a software pipeline operation that spans a plurality of (two) periods is performed in FIG. 11. For example, in period 1, the VPU0 executes the DEMUX program and V-DEC program for the input signal. After that, in period 2, the VPU1 executes the A-DEC, TEXT, PROG and BLEND programs and outputs final video data. In period 2, the VPU0 executes the DEMUX and V-DEC programs in the next frame. The DEMUX and V-DEC programs of the VPU0 and the A-DEC, TEXT, PROG and BLEND programs of the VPU1 are executed over two periods in pipeline mode.

[0032] In order to carry out the above pipeline operation, the following operations are performed when the program module 100 is executed:

1. The operating system receives the program module 100 from the external storage or memory 13 and reads the structural description 117 from the program module 100.
2. The scheduler in the operating system determines the order in which a plurality of tasks DEMUX, V-DEC, A-DEC, TEXT, PROG and BLEND are executed by the programs 111 to 116 in the program module 100 based on the structural description 117. The scheduler then divides the tasks into a first task group and a second task group. The second task group follows the first task group. For example, the tasks DEMUX and V-DEC belong to the first task group and the tasks A-DEC, TEXT, PROG and BLEND belong to the second task group.
3. The scheduler uses at least two processors VPU0 and VPU1 and periodically allocates at least one of the processors to each of the first and second task groups to periodically execute the first task group (DEMUX and V-DEC) and the second task group (A-DEC, TEXT, PROG and BLEND) in pipeline mode. If the scheduler performs a pipeline operation using two processors VPU0 and VPU1, it periodically assigns the first task group (DEMUX and V-DEC) to the VPU0 such that the VPU0 executes the first task group periodically at time intervals of 1/60 second. The scheduler periodically assigns the second task group (A-DEC, TEXT, PROG and BLEND) to the VPU1 such that the VPU1 executes the second task group periodically at time intervals of 1/60 second with a one-period delay relative to the first task group.

[0033] The two processors VPU1 and VPU2 can execute the second task group in parallel. For example,

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while the VPU1 executes the tasks A-DEC and TEXT of the second task group, the VPU2 executes the tasks PROG and BLEND of the second task group.

[0034] In the program module 100 shown in FIG. 7, a plurality of tasks DEMUX, V-DEC, A-DEC, TEXT, PROG and BLEND are executed by different threads. The above task groups can thus be referred to as thread groups.

[0035] The program module 100 shown in FIG. 7 can be prerecorded in a flash ROM and a hard disk in a device incorporating the computer system of the present embodiment, or circulated through a network. In this case, the contents of operations to be performed by the computer system vary according to the type of a program module downloaded through the network. Thus, the device incorporating the computer system can perform the real-time operation corresponding to each of various pieces of dedicated hardware. If new player software, decoder software and encryption software necessary for reproducing new contents are distributed together with the contents as program modules executable by the computer system, any device incorporating the computer system can reproduce the contents within acceptable limits of ability.

Operating System

[0036] When only one OS (operating system) 201 is loaded into the computer system of the present embodiment, it manages all real resources (MPU 11, VPUs 12, memory 14, I/O controller 15, I/O device 16, etc.), as shown in FIG. 12.

[0037] On the other hand, a virtual machine system can perform a plurality of OSes at once. In this case, as shown in FIG. 13, a virtual machine OS 301 is loaded into the computer system to manage all real resources (MPU 11, VPUs 12, memory 14, I/O controller 15, I/O device 16, etc.). The virtual machine OS 301 is also referred to as a host OS. One or more OSes 302 and 303 that are also referred to as guest OSes are loaded on the virtual machine OS 301. Referring to FIG. 14, the guest OSes 302 and 303 each run on a computer including virtual machine resources given by the virtual machine OS 301 and provide various services to application programs managed by the guest OSes 302 and 303. In the example of FIG. 14, the guest OS 302 appears as if it operated on a computer including one MPU 11, two VPUs 12 and one memory 14, and the guest OS 303 appears as if it operated on a computer including one MPU 11, four VPUs 12 and one memory 14. The virtual machine OS 301 manages which one of VPUs 12 of the real resources actually corresponds to a VPU 12 viewed from the guest OS 302 and a VPU 12 viewed from the guest OS 303. The guest OSes 302 and 303 need not be aware of the correspondence.

[0038] The virtual machine OS 301 schedules the guest OSes 302 and 303 to allocate all the resources in the computer system to the guest OSes 302 and 303 on a time-division basis. Assume that the guest OS 302 carries out a real-time operation. To perform the operation thirty times per second at an exact pace, the guest OS 302 sets its parameters to the virtual machine OS 301. The virtual machine OS 301 schedules the guest OS 302 to reliably assign necessary operation time to the guest OS 302 once per 1/30 second. The operation time is assigned to a guest OS that does not require a real-time operation by priority lower than a guest OS that requires a real-time operation. FIG. 15 shows that the guest OSes 302 and 303 run alternately, representing time by the horizontal axis. While the guest OS 302 (OS1) is running, the MPU 11 and all the VPUs 12 are used as resources of the guest OS 302 (OS1). While the guest OS 303 (OS2) is running, the MPU 11 and all the VPUs 12 are used as resources of the guest OS 303 (OS2).

[0039] FIG. 16 shows an operation mode different from that in FIG. 15. There is a case where it is to be wished that a VPU 12 be used continuously according to target applications. This case corresponds to, for example, an application that necessitates continuing to monitor data and events all the time. The scheduler of the virtual machine OS 301 manages the schedule of a specific guest OS such that the guest OS occupies a specific VPU 12. In FIG. 16, a VPU 3 is designated as a resource exclusively for a guest OS 302 (OS1). Even though the virtual machine OS 301 switches the guest OS 302 (OS1) and guest OS 303 (OS2) to each other, the VPU 3 always continues to operate under the control of the guest OS 302 (OS1).

[0040] In order to execute programs using a plurality of VPUs 12 in the present embodiment, a software module called a VPU runtime environment is used. The software module includes a scheduler for scheduling threads to be assigned to the VPUs 12. When only one OS 201 is implemented on the computer system of the present embodiment, a VPU runtime environment 401 is implemented on the OS 201 as illustrated in FIG. 17. The VPU runtime environment 401 can be implemented in the kernel of the OS 201 or in a user program. It can also be divided into two for the kernel and user program to run in cooperation with each other. When one or more guest OSes run on the virtual machine OS 301, the following modes are provided to implement the VPU runtime environment 401:

1. Mode of implementing the VPU runtime environment 401 in the virtual machine OS 301 (FIG. 18).
2. Mode of implementing the VPU runtime environment 401 as one OS managed by the virtual machine OS 301 (FIG. 19). In FIG. 19, the guest OS 304 running on the virtual machine OS 301 is the VPU runtime environment 401.
3. Mode of implementing a dedicated VPU runtime environment in each of the guest OSes managed by the virtual machine OS 301 (FIG. 20). In FIG. 20, the VPU runtime environments 401 and 402 are im-

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plemented in their respective guest OSes 302 and 303. The VPU runtime environments 401 and 402 run in association with each other, if necessary, using a function of communication between the guest OSes provided by the virtual machine OS 301.

4. Mode of implementing the VPU runtime environment 401 in one of the guest OSes managed by the virtual machine OS 301 (FIG. 21). A guest OS 303 having no VPU runtime environment utilizes the VPU runtime environment 401 of a guest OS 302 using a function of communication between the guest OSes provided by the virtual machine OS 301.

[0041] The above modes have the following merits:

Merits of Mode 1

[0042] The scheduling of a guest OS managed by the virtual machine OS 301 and that of the VPUs can be combined into one. Thus, the scheduling can be done efficiently and finely and the resources can be used effectively; and

[0043] Since the VPU runtime environment can be shared among a plurality of guest OSes, a new VPU runtime environment need not be created when a new guest OS is introduced.

Merits of Mode 2

[0044] Since a scheduler for the VPUs can be shared among guest OSes on the virtual machine OS, the scheduling can be performed efficiently and finely and the resources can be used effectively;

[0045] Since the VPU runtime environment can be shared among a plurality of guest OSes, a new VPU runtime environment need not be created when a new guest OS is introduced; and

[0046] Since the VPU runtime environment can be created without depending upon the virtual machine OS or a specific guest OS, it can be standardized easily and replaced with another. If a VPU runtime environment suitable for a specific embedded device is created to perform scheduling utilizing the characteristics of the device, the scheduling can be done with efficiency.

Merit of Mode 3

[0047] Since the VPU runtime environment can optimally be implemented in each guest OS, the scheduling can be performed efficiently and finely and the resources can be used effectively.

Merit of Mode 4

[0048] Since the VPU runtime environment need not be implemented in all the guest OSes, a new guest OS is easy to add.

[0049] As is evident from the above, all the modes 1 to 4 can be used to implement the VPU runtime environment. Any other modes can be used when the need arises.

Service Provider

[0050] In the computer system according to the present embodiment, the VPU runtime environment 401 provides various services (a communication function using a network, a function of inputting/outputting files, calling a library function such as a codec, interfacing with a user, an input/output operation using an I/O device, reading of date and time, etc.) as well as functions of managing and scheduling various resources (operation time of each VPU, a memory, bandwidth of a connection device, etc.) associated with the VPUs 12. These services are called from application programs running on the VPUs 12. If a simple service is called, it is processed by service programs on the VPUs 12. A service that cannot be processed only by the VPUs 12, such as communication processing and file processing, is processed by service programs on the MPU 11. The programs that provide such services are referred to as a service provider (SP).

[0051] FIG. 22 shows one example of the VPU runtime environment. The principal part of the VPU runtime environment is present on the MPU 11 and corresponds to an MPU-side VPU runtime environment 501. A VPU-side VPU runtime environment 502 is present on each of the VPUs 12 and has only the minimum function of carrying out a service that can be processed in the VPU 12. The function of the MPU-side VPU runtime environment 501 is roughly divided into a VPU controller 511 and a service broker 512. The VPU controller 511 chiefly provides a management mechanism, a synchronization mechanism, a security management mechanism and a scheduling mechanism for various resources (operation time of each VPU, a memory, a virtual space, bandwidth of a connection device, etc.) associated with the VPUs 12. It is the VPU controller 511 that dispatches programs to the VPUs 12 based on the results of scheduling. Upon receiving a service request called by the application program on each VPU 12, the service broker 512 calls an appropriate service program (service provider) and provides the service.

[0052] Upon receiving a service request called by the application program on each VPU 12, the VPU-side VPU runtime environment 502 processes only services that are processable in the VPU 12 and requests the service broker 512 to process services that are not processable therein.

[0053] FIG. 23 shows a procedure for processing a service request by the VPU-side VPU runtime environment 502. Upon receiving a service call from an application program (step S101), the VPU-side VPU runtime environment 502 determines whether the service can be processed therein (step S102). If the service can be

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processed, the VPU runtime environment 502 executes the service and returns its result to the calling part (steps S103 and S107). If not, the VPU runtime environment 502 determines whether a service program that can execute the service is registered as one executable on each VPU 12 (step S104). If the service program is registered, the VPU runtime environment 502 executes the service program and returns its result to the calling part (steps S105 and S107). If not, the VPU runtime environment 502 requests the service broker 512 to execute the service program and returns a result of the service from the service broker 512 to the calling part (steps S106 and S107).

[0054] FIG. 24 shows a procedure for processing a service that is requested by the VPU-side VPU runtime environment 502 by the service broker 512 of the MPU-side VPU runtime environment 501. Upon receiving a service call from the VPU-side VPU runtime environment 502 (step S111), the service broker 512 determines whether the VPU runtime environment 501 can process the service (step S112). If the service can be processed, the service broker 512 executes the service and returns its result to the VPU-side VPU runtime environment 502 of the calling part (steps S113 and S114). If not, the service broker 512 determines whether a service program that can execute the service is registered as one executable on the MPU 11 (step S114). If the service program is registered, the service broker 512 executes the service program and returns its result to the VPU-side VPU runtime environment 502 of the calling part (steps S116 and S114). If not, the service broker 512 returns an error to the VPU-side VPU runtime environment 502 of the calling part (step S117).

[0055] Results reply to some service requests issued from the program to be executed by each VPU 12, and no results reply to other service requests. The destination of the reply is usually a thread that issues a service request; however, another thread, a thread group or a process can be designated as the destination of the reply. It is thus favorable that the destination be included in a message to request a service. The service broker 512 can be realized using a widely used object request broker.

Real-time Operation

[0056] The computer system according to the present embodiment serves as a real-time processing system. The operations to be performed by the real-time processing system are roughly divided into the following three types:

1. Hard real-time operation
2. Soft real-time operation
3. Best effort operation (non-real-time operation)

The hard and soft real-time operations are a so-called real-time operation. The real-time processing system of the present embodiment has concepts of both thread and process like a number of existing OSes. First, the thread and process in the real-time processing system will be described.

[0057] The thread has the following three classes:

1. Hard real-time class

[0058] Timing requirements are very important. This thread class is used for such an important application as to cause a grave condition when the requirements are not met.

2. Soft real-time class

[0059] This thread class is used for an application whose quality simply lowers even if the timing requirements are not met.

3. Best effort class

[0060] This thread class is used for an application including no timing requirements.

[0061] In the present embodiment, the thread is a unit of execution for the real-time operation. The threads have their related programs that are to be executed by the threads. Each of the threads holds its inherent information that is called a thread context. The thread context contains, for example, information of a stack and values stored in the register of the processor.

[0062] In the real-time processing system, there are two different threads of MPU and VPU threads. These two threads are classified by processors (MPU 11 and VPU 12) that execute the threads and their models are identical with each other. The thread context of the VPU thread includes the contents of the local storage 32 of the VPU 12 and the conditions of a DMA controller of the memory controller 33.

[0063] A group of threads is called a thread group. The thread group has the advantage of efficiently and easily performing, e.g., an operation of giving the same attribute to the threads of the group. The thread group in the hard or soft real-time class is roughly divided into a tightly coupled thread group and a loosely coupled thread group. The tightly coupled thread group and loosely coupled thread group are discriminated from each other by attribute information (coupling attribute information) added to the thread groups. The coupling attribute of the thread groups can explicitly be designated by the codes in the application programs or the above-described structural description.

[0064] The tightly coupled thread group is a thread group that is made up of threads running in cooperation with each other. In other words, the threads belonging to the tightly coupled thread group tightly collaborate with each other. The tightly collaboration implies an interaction such as frequent communication and synchronization between threads or an interaction that decreas-

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es in latency. The threads belonging to the same tightly coupled thread group are always executed simultaneously. On the other hand, the loosely coupled thread group is a thread group that obviates a tightly collaboration between threads belonging to the group. The threads belonging to the loosely coupled thread group carry out communications for transferring data through the buffer on the memory 14.

Tightly Coupled Thread Group

[0065] As shown in FIG. 25, different VPUs are allocated to the threads of the tightly coupled thread group and the threads are executed at the same time. These threads are called tightly coupled threads. The execution terms of the tightly coupled threads are reserved in their respective VPUs, and the tightly coupled threads are executed at the same time. In FIG. 25, a tightly coupled thread group includes two tightly coupled threads A and B, and the threads A and B are executed at once by the VPU0 and VPU1, respectively. The real-time processing system of the present embodiment ensures that the threads A and B are executed at once by different VPUs. One of the threads can directly communicate with the other thread through a local storage or control register of the VPU that executes the other thread.

[0066] FIG. 26 illustrates communication between threads A and B, which is performed through the local storages of VPU0 and VPU1 that execute the threads A and B, respectively. In the VPU0 that executes the thread A, an RA space corresponding to the local storage 32 of the VPU1 that executes the thread B is mapped in part of an EA space of the thread A. For this mapping, an address translation unit 331 provided in the memory controller 33 of the VPU0 performs address translation using a segment table and page table. The address translation unit 331 converts (translates) a part of the EA space of the thread A to the RA space corresponding to the local storage 32 of the VPU1, thereby to map the RA space corresponding to the local storage 32 of the VPU1 in part of the EA space of the thread A.

[0067] In the VPU1 that executes the thread B, an RA space corresponding to the local storage 32 of the VPU0 that executes the thread A is mapped in part of an EA space of the thread B. For this mapping, an address translation unit 331 provided in the memory controller 33 of the VPU1 performs address translation using the segment table and page table. The address translation unit 331 converts a part of the EA space of the thread B to the RA space corresponding to the local storage 32 of the VPU0, thereby to map the RA space corresponding to the local storage 32 of the VPU0 in part of the EA space of the thread B.

[0068] FIG. 27 shows mapping of local storage (LS1) 32 of the VPU1 executing the thread B in the EA space of the thread A executed by the VPU0 and mapping of local storage (LS0) 32 of the VPU0 executing the thread A in the EA space of the thread B executed by the VPU1. For example, when data to be transferred to the thread B is prepared on the local storage LS0, the thread A sets a flag indicative of this preparation in the local storage LS0 of the VPU0 or the local storage LS1 of the VPU1 that executes the thread B. In response to the setting of the flag, the thread B reads the data from the local storage LS0.

[0069] According to the present embodiment described above, tightly coupled threads can be specified by the coupling attribute information, and the tightly coupled threads A and B are sure to be executed at once by different VPUs, respectively. Thus, an interaction of communication and synchronization between the threads A and B can be performed more lightly without delay.

Loosely Coupled Thread Group

[0070] The execution term of each of threads belonging to the loosely coupled thread group depends upon the relationship in input/output between the threads. Even though the threads are subject to no constraints of execution order, it is not ensured that they are executed at the same time. The threads belonging to the loosely coupled thread group are called loosely coupled threads. FIG. 28 shows a loosely coupled thread group including two threads C and D as loosely coupled threads, which are executed by their respective VPU0 and VPU1. The threads C and D differ in execution term as is apparent from FIG. 28. Communication between the threads C and D is carried out by the buffer prepared on the main memory 14 as shown in FIG. 29. The thread C executed by the VPU0 writes data, which is prepared in the local storage LS0, to the buffer prepared on the main memory 14 by DMA transfer. The thread D executed by the VPU1 reads data from the buffer on the main memory 14 and writes it to the local storage LS1 by DMA transfer when the thread D starts to run.

Process and Thread

[0071] As shown in FIG. 30, a process includes one address space and one or more threads. The threads can be included in the process regardless of their number and type. For example, only VPU threads can be included in the process and so can be a mixture of VPU and MPU threads. As a thread holds a thread context as its inherent information, a process holds a process context as its inherent information. The process context contains both an address space inherent in the process and thread contexts of all threads included in the process. The address space can be shared among all the threads of the process. One process can include a plurality of thread groups, but one thread group cannot belong to a plurality of processes. Thus, a thread group belonging to a process is inherent in the process.

[0072] In the real-time processing system of the present embodiment, there are two models of a thread

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first model and an address space first model as method for creating a new thread. The address space first model is the same as that adopted in the existing OS and thus can be applied to both the MPU and VPU threads. On the other hand, the thread first model can be applied only to the VPU threads and is peculiar to the real-time processing system of the present embodiment. In the thread first model, the existing thread (which is one for creating a new thread, i.e., a parent thread of the new thread) first designates a program to be executed by a new thread and causes the new thread to start to execute the program. The program is then stored in the local storage of the VPU and starts to run from a given address. Since no address space is related to the new thread at this time, the new thread can gain access to the local storage of the VPU and not to the memory 14. After that, when the need arises, the new thread in itself calls a service of VPU runtime environment and creates an address space. The address space is related to the new thread, and the new thread can gain access to the memory 14. In the address space first model, the existing thread creates a new address space or designates the existing address space, and arranges program, which is to execute by the new thread, in the address space. Then, the new thread starts to run the programs. The merit of the thread first model is that a thread can be executed only by the local storage to reduce overhead costs required for generating, dispatching and exiting the thread.

Scheduling of Threads

[0073] A scheduling operation performed by the VPU runtime environment 401 will now be described with reference to the flowchart shown in FIG. 31. The scheduler in the VPU runtime environment 401 checks a coupling attribute between threads based on coupling attribute information added to each group of threads to be scheduled (step S121). The scheduler determines whether each thread group is a tightly coupled thread group or a loosely coupled thread group (step S122). The coupling attribute is checked referring to the descriptions of threads in program codes or thread parameters in the above structural description 117. If the tightly and loosely coupled thread groups are each specified, the threads to be scheduled are separated into the tightly and loosely coupled thread groups.

[0074] The scheduling of threads belonging to the tightly coupled thread group is performed as follows. In order to execute threads of a tightly coupled thread group, which are selected from the threads to be scheduled, by their respective VPUs at once, the scheduler in the VPU runtime environment 401 reserves an execution term of each of the VPUs, whose number is equal to that of the threads, and dispatches the threads to the VPUs at once (step S123). The scheduler maps an RA space in part of an EA space of a thread using the address translation unit 331 in a VPU that executes the thread (step S124), the RA space corresponding to the local storage of a VPU that executes a partner thread interacting with the former thread. As for the threads belonging to the loosely coupled thread group which are selected from the threads to be scheduled, the scheduler dispatches the threads in sequence to one or more VPUs based on the relationship in input/output between the threads (step S125).

[0075] If a tightly coupled thread group, which is a set of threads running in cooperation with each other, is selected based on the coupling attribute information, it can be ensured that the threads belonging to the tightly coupled thread group are executed at once by different processors. Consequently, communication between threads can be achieved by a lightweight mechanism of gaining direct access to, e.g., the registers of processors that execute their partner threads each other. The communication can thus be performed lightly and quickly.

State Transition of Threads

[0076] A thread generally makes a state transition from when it is created until it is deleted. As shown in FIG. 32, a thread makes the following seven state transitions.

1. Not-existent state: This state is logical and does not exist in an effective thread.
2. DORMANT state: A thread is created and does not start running yet.
3. READY state: The thread is ready to start running.
4. WAITING state: The thread waits for conditions to meet to start (resume) running.
5. RUNNING state: The thread is actually running on the VPU or MPU.
6. SUSPENDED state: The thread is forcibly suspended by the VPU runtime environment and other threads.
7. WAITING-SUSPENDED state: The waiting and suspended states overlap each other.

[0077] The conditions of transition between the above seven states and the thread contexts involved in the transition are as follows.

[Transition from NOT EXISTENT state to DORMANT state]

[0078] This transition is made by creating a thread.

[0079] A thread context is created but its contents are in the initial state.

[Transition from DORMANT state to NOT EXISTENT state]

[0080] This transition is made by deleting a thread.

[0081] If the thread is set to store its thread context,

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the stored thread context is discarded by the transition.

[Transition from DORMANT state to WAITING state]

[0082] This transition is made when the thread requests the runtime environment to schedule the thread.

[Transition from WAITING state to READY state]

[0083] This transition is made when an event (e.g., synchronization, communication, timer interruption) for which the thread waits is generated.

[Transition from READY state to RUNNING state]

[0084] This transition is made when the thread is dispatched to MPU or VPU by the runtime environment.

[0085] The thread context is loaded. When the thread context is saved, it is restored.

[Transition from RUNNING state to READY state]

[0086] This transition is made when the running of the thread is preempted.

[Transition from RUNNING state to WAITING state]

[0087] This transition is made when the thread suspends its own running to wait for an event using a synchronization mechanism, a communication mechanism and the like.

[0088] The thread in every class can be set to store its thread context. When a thread is set to store its thread context, the thread context is saved by the runtime environment when the thread transits from RUNNING state to WAITING state. The saved thread context is maintained unless the thread transits to DORMANT state and restored when the thread transits to the RUNNING state.

[Transition from RUNNING state to SUSPENDED state]

[0089] This transition is made when the running of the thread is forcibly suspended in response to an instruction from the runtime environment or other threads.

[0090] The thread in every class can be set to store its thread context. When a thread is set to store its thread context, the thread context is saved by the runtime environment when the thread transits from RUNNING state to SUSPENDED state. The saved thread context is maintained unless the thread transits to DORMANT state and restored when the thread transits to the RUNNING state.

[Transition from RUNNING state to DORMANT state]

[0091] This transition is made when the thread in itself exits its own running.

[0092] When the thread is set to store its thread context, the contents of the thread context are discarded by the transition.

[Transition from WAITING state to WAITING-SUSPENDED state]

[0093] This transition is made when the thread is forced to stop by instruction from outside while it is waiting for an event to generate in the WAITING state.

[Transition from WAITING-SUSPENDED state to WAITING state]

[0094] This transition is made when the thread resumes running by instruction from outside while it is in the WAITING-SUSPENDED state.

[Transition from WAITING-SUSPENDED state to SUSPENDED state]

[0095] This transition is made when the event for which the thread waits in the WAITING state is generated.

[Transition from SUSPENDED state to READY state]

[0096] This transition is made when the thread resumes running by instruction from outside.

[Transition from READY state SUSPENDED state]

[0097] This transition is made when the thread stops running by external environment.

Execution Term of Thread

[0098] The term of the running state of a thread to which a VPU is allocated is called an execution term. In general, a term from creation to deletion of a thread includes a plurality of execution terms of the thread. FIG. 33 shows an example of thread states varied from creation to deletion. This example includes two execution terms during the presence of the thread. The thread context can be saved and restored using various methods. Most normal threads run so as to save a context at the end of an execution term and restore the context at the beginning of the next execution term. In a certain periodic operation, the thread run so as to create a new context at the beginning of an execution term, use the context during the execution term, and discard the context at the end of the execution term in every period.

Execution Term of Threads belonging to Tightly Coupled Thread Group

[0099] FIG. 34 shows execution terms of threads belonging to the same tightly coupled thread group. All the

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threads belonging to a certain tightly coupled thread group are scheduled by the VPU runtime environment 401 such that they can run at once in one execution term. This tightly coupled thread group is used chiefly for hard real-time threads. In order to achieve the operation, therefore, the VPU runtime environment 401 designates processors used at once and their number when an execution term is reserved for the hard real-time class. Moreover, the VPU runtime environment 401 makes contexts of threads running at once correspondent to the processors, respectively.

[0100] The threads, which belonged to the tightly coupled thread group in a certain execution term, can run separately from each other in other execution term by canceling their tightly coupled relationship. Each of the threads has to sense whether it runs as a tightly coupled thread or separately from another thread and perform an operation of communication and synchronization with its partner thread. Each of the threads is provided with an attribute that indicates preemptive or non-preemptive. The preemptive attribute permits a thread to be preempted during its execution term and, in other words, permits the thread to stop running. The non-preemptive attribute ensures that a thread cannot be preempted during its execution term. The non-preemptive attribute varies in meaning from thread class to thread class. In the hard real-time class, when a thread starts to run, nothing but the thread in itself can stop the running until its execution term ends. In the soft real-time class, preemptiveness is essential and thus the non-preemptive attribute is not supported. In the best effort class, a thread can be protected against being preempted from another best effort class, but it can be preempted from a higher-level class such as the hard real-time class and soft real-time class.

Execution Models of Threads

[0101] The execution models of threads can roughly be classified into two models: a periodic execution model as shown in FIG. 35 and an aperiodic execution model as shown in FIG. 36. In the periodic execution model, a thread is executed periodically. In the aperiodic running model, a thread is executed based on an event. The periodic execution model can be implemented using a software interrupt or an event object such as synchronization primitives. In the hard real-time class, the periodic execution model is implemented using a software interrupt. In other words, the VPU runtime environment 401 jumps to an entry point of a thread determined by a given method with timing to start a periodic operation or calls a callback function registered in advance by a given procedure. In the soft real-time class, the periodic execution model is implemented using an event object. In other words, since the VPU runtime environment 401 notifies a generation of a previously-registered event object in each period, a soft real-time thread waits an event object in each period, and perform a given operation upon generation of the event, thereby realizing a periodic execution model. In the best effort class, the periodic execution model can be implemented using either one of a software interrupt or an event object. The actual execution does not always start at the beginning of each period, but may be delayed within constraints.

[0102] Using an event model, the aperiodic execution model can be realized as the periodic execution model. In the soft real-time class and best effort class, the aperiodic execution model differs from the periodic execution model only in the timing with which an event is notified and these models are the same in the implementing method. In the hard real-time class, the minimum inter-arrival time and the dead line, which are necessary for securing time requirements, strongly constrain the operation of the system; accordingly, the aperiodic execution is restricted.

Context Switching

[0103] In the real-time processing system according to the present embodiment, one of methods for switching a context at the end of the execution term of a VPU thread can be selected. Since the costs for switching the context are very high, the selection of one method improves the efficiency of switching. The selected method is used at the end of the reserved execution term of a thread. When a context is switched during the execution term or at the time of preemption, all contexts of the current thread need to be saved in whatever case and restored when the thread resumes running next. For example, there are following methods of switching a VPU context.

1. Discard of Contexts

[0104] No contexts are saved.

2. Complete Saving of Contexts

[0105] All contexts of a VPU, including the states of the register and local storage of the VPU and those of the DMA controller in the memory controller, are saved.

3. Graceful Saving of Contexts

[0106] The context switching is delayed until all operations of the DMA controller in the memory controller in a VPU are completed. After that, the contents of the register and local storage in the VPU are saved. In this method, all the contexts of the VPU as well as the complete saving are saved.

[0107] One scheduler can be implemented to schedule both MPU and VPU threads and different schedulers can be done to schedule their respective MPU and VPU threads. Since the MPU and VPU threads differ in costs for switching a context, the implementation of different schedulers becomes more efficient.

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Scheduling in Hard Real-Time Class

[0108] The scheduling of threads in the hard real-time class is performed using a reservation graph of an extended task graph. FIG. 37 shows an example of the task graph. The task graph represents a relationship between tasks. In FIG. 37, the arrows between tasks indicate the dependence of the tasks (relationship in input/output between the tasks). According to the example of FIG. 37, tasks 1 and 2 can freely start to run, a task 3 can start to run after both the tasks 1 and 2 stop running, and tasks 4 and 5 can start to run after the task 3 stops running. The task graph has no concepts of contexts. For example, when the tasks 1 and 4 should be processed using the same context, it cannot be described in the task graph. The following reservation graph of the extended task graph is therefore used in the real-time processing system of the present embodiment.

[0109] First, consider the task graph to be a relationship between not tasks but execution terms. By relating a context to each of the execution terms, a thread corresponding to the context runs in the execution term. If the same context is related to a plurality of execution terms, its corresponding thread runs in each of the execution terms. In the example shown in FIG. 38, the context of thread 1 is related to execution terms 1 and 2, and the thread 1 runs in each of the execution terms 1 and 2. An attribute indicative of constraints of hard real-time ensured by the runtime environment is added to each of arrows between the execution terms in FIG. 52. Using a reservation graph so created, operation models and constraints such as time requirements of a real-time application can be described without making any modifications to the model of the real-time application. FIG. 39 shows an example of the reservation graph created based on the graph shown in FIG. 38. Contexts 1, 2 and 3 in FIG. 39 correspond to those of threads 1, 2 and 3 in FIG. 38, respectively.

Scheduling in Soft Real-Time Class

[0110] The scheduling of threads in the soft real-time class is performed using a fixed priority scheduling method in order to allow the running patterns of threads to be predicted. Two different scheduling algorithms are prepared for the scheduling method: one is fixed priority FIFO scheduling and the other is fixed priority round robin scheduling. In order to execute a higher-priority thread by priority, even while a lower-priority thread is running, the lower-priority thread is preempted and immediately the higher-priority thread starts to run. In order to avoid a priority inversion problem that occurs in a critical section, it is desirable to perform a synchronization mechanism such as a priority inheritance protocol and a priority ceiling protocol.

Scheduling in Best Effort Class

[0111] The scheduling of threads in the best effort class is performed using dynamic priority scheduling and the like.

Hierarchical Scheduler

[0112] The scheduling function in the VPU runtime environment 401 can be fulfilled as a hierarchical scheduler as shown in FIG. 40. In other words, thread-level scheduling has two hierarchies of thread inter-class scheduling and thread intra-class scheduling. Thus, the scheduler in the VPU runtime environment 401 has a thread intra-class scheduling section 601 and a thread inter-class scheduling section 602. The thread inter-class scheduling section 602 schedules threads spreading over thread classes. The thread intra-class scheduling section 601 schedules threads belonging to each of thread classes. The section 601 includes a hard real-time (hard RT) class scheduling section 611, a soft real-time (soft RT) class scheduling section 612 and a best effort class scheduling section 613.

[0113] The thread inter-class scheduling and thread intra-class scheduling have a hierarchical structure. First, the thread inter-class scheduling operates to determine which thread class is executed and then which thread in the thread class is executed. The thread inter-class scheduling employs preemptive fixed priority scheduling. The hard real-time class has the highest priority, with the soft real-time class and the best effort class following in that order. When a thread in a higher-priority class is ready to run, a lowest-priority thread is preempted. Synchronization between thread classes is achieved by a synchronous primitive provided by the VPU runtime environment 401. In particular, only the primitive can be used in a hard real-time thread to prevent a block from occurring in the hard real-time thread. When a best effort thread blocks a soft real-time thread, it is processed as a soft real-time thread to prevent priority from being inverted between thread classes. Furthermore, the use of, e.g., the priority inheritance protocol prevents another soft real-time thread from blocking the best effort thread.

Thread Parameters

[0114] In the real-time processing system according to the present embodiment, threads are scheduled using various parameters. The parameters common to the threads in each class are as follows:

Class of threads (hard real-time, soft real-time, best effort);
Resources for use (number of MPUs or VPUs, bandwidth, physical memory size, I/O device);
Priority; and
Preemptive or non-preemptive.

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[0115] The following are parameters for the threads in the hard real-time class:

Execution term;
Dead line;
Period or minimum inter-arrival time; and
VPU context switching method.

[0116] FIG. 41 shows examples of fundamental parameters for the hard real-time class. In example 1 to designate an execution term shown in the uppermost part of FIG. 41, one MPU and two VPUs are reserved at once in the designated execution term, and the context of each of the VPUs is completely saved. In this case, the threads run at the same time on the three processors and, after the execution term, the contexts of VPU threads as well as that of an MPU thread are completely saved. In the upper right of FIG. 55, example 2 shows a method of designating a deadline to ensure that an operation represented by the number of VPUs and their execution term is performed before the deadline. The deadline is designated by relative time starting at the request time when a reservation request is made. In the lowermost part of FIG. 41, example 3 shows a method of designating a periodic execution. In this example, an execution term that designates two VPUs 12 is periodically repeated, and the contexts of VPU threads are discarded after the execution term for each period, with the result that all operations are performed by new contexts. Moreover, the deadline is designated by relative time starting at the beginning of the period.

[0117] For example, there are following constraints as other parameters used in the hard real-time class:

Timing constraints (absolute timing constraint and relative timing constraint);
Precedence constraint; and
Mutual exclusive constraint.

[0118] The timing constraints provide a unit which delays execution timing. The absolute timing constraint is a condition for designating delay time with reference to static timing, such as the start time of a period, as shown in FIG. 42. The relative timing constraint is a condition for designating permissible delay time with reference to dynamic timing and an event, such as the start time and end time of a certain, as shown in FIG. 43. Since the precedence constraint can be achieved by designating delay time as 0 or longer with reference to the end time of a certain execution term using the relative timing constraint, it can be considered to be a special one for the relative timing constraint.

[0119] The mutual exclusive constraint is a condition for ensuring that execution terms do not overlap each other, as shown in FIG. 44. The mutual exclusive constraint makes it possible to lessen the prediction impossibility of the execution term, which is caused by a lock. In other words, all threads common to some resources are prevented from running at once to obviate a lock regarding the resources.

Synchronization mechanisms for Threads

[0120] In the real-time processing system according to the present embodiment, the following synchronous primitives are used as synchronization mechanisms for threads:

Semaphore;
Message queue;
Message buffer;
Event flag;
Barrier; and
Mutex.

[0121] The other synchronous primitives can be used. The real-time processing system of the present embodiment provides the following three methods to achieve the above synchronization mechanisms:

[0122] The synchronization mechanisms are implemented on the memory (main storage) 14 or the local storage 32 of a VPU using an instruction such as a TEST & SET;

[0123] The synchronization mechanisms are implemented by hardware mechanisms such as a mail box and a signal register; and

[0124] The synchronization mechanisms are implemented using a mechanism provided as a service by the VPU runtime environment.

[0125] Since the synchronization mechanisms have advantages and disadvantages, it is desirable to selectively use them according to the attributes of threads as shown in FIG. 45. In other words, a synchronization mechanism implemented using the memory (main storage MS) 14 that is shared and accessed by the MPU and VPUs can be used for threads in all classes. In contrast, a synchronization mechanism implemented on the local storage LS of a VPU 12 can be used only for threads belonging to the tightly coupled thread group. This is because only the threads belonging to the tightly coupled thread group ensure that their partner threads for synchronization run at the same. For example, if a thread belonging to the tightly coupled thread group is used for a synchronization mechanism implemented on the local storage of a VPU that executes the partner thread, the execution of the partner thread is ensured when the synchronization mechanism is used. Thus, the local storage of the VPU that executes the partner thread always stores information for the synchronization mechanism.

[0126] A synchronization mechanism using a unit other than the memory (main storage MS) and local storage LS can be implemented by a hardware mechanism or a service of the VPU runtime environment 401. Since the threads belonging to the tightly coupled thread or those in the hard real-time class require a high-speed synchro-

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nization mechanism, the synchronization mechanism implemented by the hardware mechanism is desirable to use in the threads. In contrast, the synchronization mechanism provided by the runtime environment is desirable to use in the threads belonging to the loosely coupled thread group or those belonging to the soft real-time class and best effort class.

Automatic Selection of Synchronization Mechanism

[0127] In the real-time processing system according to the present embodiment, the above synchronization mechanisms can automatically be selected or switched in accordance with the attribute and status of threads. This operation is performed by a procedure as shown in FIG. 46. While threads for synchronization belong to the tightly coupled thread group (YES in step S201), a high-speed synchronization mechanism that is implemented by the memory 14, the local storage 32 of each VPU 12 or the hardware mechanism is used (steps S202, S203, S204, S205). When the threads change in status to cancel their tightly coupled relationship (NO in step S201), the high-speed synchronization mechanism is switched to a synchronization mechanism that is implemented as a synchronization mechanism on the memory 14 or a service of the VPU runtime environment 401 (steps S206, S207, S208).

[0128] The above switching can be provided for programs running on the VPUs 12 in the form of a library or as a service of the VPU runtime environment 502 in each of the VPUs 12. A plurality of synchronization mechanisms can be switched as follows. The synchronization mechanisms can be secured in advance and used selectively or new synchronization mechanisms can be secured when the switching is performed.

[0129] For a synchronization mechanism using local storages of VPUs 12, threads needs to be executed at once by the VPUs like threads belonging to the tightly coupled thread group. This constraint is eased as follows. While a thread is not running, the contents of the local storage are stored in the memory 14 when the thread runs last, and mapping is so controlled that the stored contents are indicated by the entries of the page table or segment table indicating the local storage. According to this method, while the partner thread is not running, the thread can continue running as if there is a local storage related to the partner thread. When the thread starts to run by allocating a VPU 12 thereto, the contents stored in the memory 14 are restored to the local storage of the VPU 12 to change the mapping of a corresponding page table or segment table. Using a backup copy of the local storages of the VPUs 12, the synchronization mechanism using the local storages of VPUs 12 can be used even for threads that do not belong to the tightly coupled thread group.

Reservation Graph

[0130] FIG. 47 shows a reservation graph corresponding to the data flow shown in FIG. 9. In FIG. 47, six boxes represent execution terms. The upper left number on each of the boxes indicates the ID of an execution term to be reserved. The symbol in each box indicates the identifier of a thread context related to the execution term. The lower right number on each box indicates the length (cost) of the execution term. The arrows connecting the boxes all denote precedence constraints. In other words, an arrow extending from one box to another box indicates that an operation in the execution term of the latter box starts after an operation in that of the former box is completed. A chain of execution terms can thus be represented. The number with each arrow denotes an ID of a buffer used for data transfer between execution terms connected by the arrow, and the value with each number denotes the size of a buffer. The following are procedures 1 to 7 for performing operations in accordance with the reservation graph shown in FIG. 47.

1. Create a thread context that executes the DEMUX program 111 and call its identifier DEMUX.
2. Create a thread context that executes the A-DEC program 112 and call its identifier A-DEC.
3. Create a thread context that executes the V-DEC program 113 and call its identifier V-DEC.
4. Create a thread context that executes the TEXT program 114 and call its identifier TEXT.
5. Create a thread context that executes the PROG program 115 and call its identifier PROG.
6. Create a thread context that executes the BLEND program 116 and call its identifier BLEND.
7. Create a reservation request having a data structure as shown in FIG. 48 and sends it to the VPU runtime environment 401 to make a reservation.

[0131] According to each of the above procedures 1 to 6, if a program is designated to run as a thread, the VPU runtime environment 401 assigns necessary resources to the program to create a thread context. The handle of the thread context is returned and thus referred to as an identifier.

[0132] FIG. 48 shows a reservation request containing buffer data written as BUFFER and execution term data written as TASK. The buffer data is used to declare a buffer on the memory 14 for data transfer between execution terms. In the buffer data, "Id" indicates buffer number, "Size" indicates buffer size, "SrcTask" shows execution term number that writes data and "DstTask" shows execution term number that reads data. In the execution term data, "Id" represents execution term number, "Class" indicates thread class (VPU shows VPU thread and HRT shows hard real-time class. In addition to these, there are MPU showing MPU thread, SRT showing soft real-time class, BST showing best ef-

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fort class and so on). "ThreadContext" denotes thread context corresponding to the execution term, "Cost" indicates length or cost of the execution term, "Constraint" represents various constraints based on the execution term, "InputBuffer" shows a list of identifiers of buffers read in the execution term and "OutputBuffer" indicates a list of identifiers of buffers written in the execution term. The "Constraint" also can include "Precedence" showing precedence constraint, "Absolute Timing" showing absolute timing constraint, "Relative Timing" showing relative timing constraint and "Exclusive" showing mutual exclusive constraint. The "Constraint" has a list of numbers of execution terms of partner threads for constraints.

[0133] The buffer area reserved by the reservation request shown in FIG. 48 is allocated to the main memory 14 and released therefrom by the VPU runtime environment 401. The allocation of the buffer area is performed when a thread that writes data to the buffer area starts to run. The release of the buffer area is performed when a thread that reads data from the buffer area exits. The thread can be notified of the address of the allocated buffer using an address, a variable or a register that is predetermined when the thread starts to run. In the real-time processing system of the present embodiment, when the program module 100 shown in FIG. 7 is provided, the structural description 117 shown in FIG. 8 is read out of the program module 100 and, based on the structural description 117, a thread context is created by the above procedures and a reservation request as shown in FIG. 48 is created and issued, thereby providing a function of executing the program module 100. This function allows the operation of dedicated hardware described by the program module 100 as shown in FIG. 7 to be performed by processing software by a plurality of processors. A program module having a structure as shown in FIG. 7 is created for each hardware to be implemented and then executed by an apparatus having a function conforming to the real-time processing system of the present embodiment, with the result that the apparatus can be operated as desired hardware.

[0134] Providing the reservation request shown in FIG. 48, the VPU runtime environment 401 determines which VPU 12 executes each task with which timing in a period. This is scheduling. Actually, a plurality of reservation requests can be provided at once; therefore, operation timing is determined to prevent them from contradicting each other (prevent given constraints from not being satisfied). Assuming that only the reservation request shown in FIG. 48 is made when there are two VPUs 12 as shown in FIG. 49, the scheduling is performed such that the VPU 0 sequentially performs DEMUX, V-DEC, PROG and BLEND operations which cannot be done in parallel and after the DEMUX operation, the VPU1 performs the A-DEC and TEXT operations that can be done in parallel.

Software Pipeline

[0135] If there is no time enough to perform the DEMUX, V-DEC, PROG and BLEND operations in sequence within one period, software pipeline processing is carried out over a plurality of periods. For example, as shown in FIG. 50, the VPU 0 performs the DEMUX and V-DEC operations in the first period and the VPU 1 performs the A-DEC, TEXT, PROG and BLEND operations in the second period. In the second period, the VPU 0 performs DEMUX and V-DEC operations in the next frame in parallel with the A-DEC, TEXT, PROG and BLEND operations. In other words, as shown in FIG. 51, the pipeline processing is performed in which the VPU 1 performs the A-DEC, TEXT, PROG and BLEND operations upon receipt of outputs from the DEMUX and V-DEC operations in the preceding period while the VPU 0 is performing the DEMUX and V-DEC operations.

[0136] FIG. 52 is a flowchart of procedures for scheduling to achieve a software pipeline operation.

[0137] The VPU runtime environment 401 determines whether all of the threads DEMUX, V-DEC, PROG and BLEND, which need to be executed in sequence, can be done within one period (step S401). The length of one period is preset to the VPU runtime environment 401 as an execution condition of the program module 100. The length can be described explicitly in the structural description 117. In step S401, the total execution term of the threads DEMUX, V-DEC, PROG and BLEND is predicted based on the costs of these threads. The predicted total execution term is compared with the length of one period.

[0138] If the VPU runtime environment 401 determines that the threads DEMUX, V-DEC, PROG and BLEND cannot be executed within one period (NO in step S401), it divides all the threads DEMUX, V-DEC, A-DEC, TEXT, PROG and BLEND for executing the program module 100 into two groups (referred to as first and second thread groups hereinafter) that can be executed in sequence, based on the order of execution of the threads DEMUX, V-DEC, A-DEC, TEXT, PROG and BLEND (step S402). The first thread group is a set of one or more threads executed before the second thread group, and the second thread group is a set of one or more threads executed after the first thread group. In the present embodiment, the threads DEMUX and V-DEC belong to the first thread group and the threads A-DEC, TEXT, PROG and BLEND belong to the second thread group to satisfy the precedence constraints between the threads and make the total execution term of each of the groups not longer than the time interval corresponding to one period.

[0139] The VPU runtime environment 401 performs the scheduling operation to periodically assigns the execution term of each of the threads belonging to the first thread group (DEMUX and V-DEC) to the VPU0 such that the VPU0 executes the first thread group periodi-

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cally at time intervals of 1/60 second (step S403). In step S403, periodic execution of each of the threads DEMUX and V-DEC is reserved for the VPU0. Then, the VPU runtime environment 401 performs the scheduling operation to periodically assigns each of the threads belonging to the second thread group (A-DEC, TEXT, PROG and BLEND) to the VPU1 such that the VPU1 executes the second thread group periodically at time intervals of 1/60 second with a one-period delay relative to the first thread group (step S404). In step S404, periodic execution of each of the threads A-DEC, TEXT, PROG and BLEND is reserved for the VPU1.

[0140] Two processors VPU0 and VPU1 execute the first thread group (DEMUX and V-DEC) and the second thread group (A-DEC, TEXT, PROG and BLEND) in pipeline mode. Consequently, the first thread group and the second thread group are executed in parallel while the second thread group is delayed one period relative to the first thread group, thus outputting frame data processing results for each period of 1/60 second.

[0141] In the above example, the VPU0 always executes the first thread group (DEMUX and V-DEC) and the VPU1 always executes the second thread group (A-DEC, TEXT, PROG and BLEND). As shown in FIG. 53, however, scheduling can be carried out to periodically replace a processor to which the first thread group is assigned and a processor to which the second thread group is assigned.

Scheduling in Consideration of the Number of Buffers

[0142] When a buffer is used to transfer data between a thread running in an execution term and a thread running in another execution term, the buffer is occupied from the beginning of the execution term on the data write side to the end of the execution term on the data read side. For example, as shown in FIG. 54, when a buffer on the memory 14 (main storage) is used to transfer data between execution terms A and B, it is occupied from the beginning of execution term A to the end of execution term B. Therefore, when a buffer is used to transfer data from execution term A to execution term B and the execution terms A and B belong to their respective periods adjacent to each other in software pipeline processing, the number of buffers required varies according to the execution timing in the execution terms A and B. For example, as shown in FIG. 55, when threads are scheduled such that they run in the execution term A earlier than in the execution term B in each period, data is transferred from execution term An (An indicates execution term A in period n) to execution term Bn in the next period, and data is transferred from execution term An+1 to execution term Bn+1 in the next period. Since the execution term An+1 is interposed between An and Bn, the buffer for transferring data from An to Bn cannot be used for transferring data from An+1 to Bn+1 but a new buffer has to be used. In other words, two buffers are required. On the other hand, as shown in FIG. 56, when threads are scheduled such that they start to run in execution term A after the end of execution term B in one period, data that is written to a buffer in execution term An is read out of the buffer in execution term Bn. Then, data is written to the same buffer in execution term An+1 and read therefrom in execution term Bn+1. That is, a single buffer has only to be used.

[0143] In the real-time processing system according to the present embodiment, the scheduler in the VPU runtime environment 401 schedules execution terms to be reserved such that the amount of use of buffer memory areas becomes as small as possible. More specifically, in order to execute software pipeline processing of two VPUs 0 and 1, the scheduler in the VPU runtime environment 401 divides an operation into two partial operations (one to be performed first by the VPU 0 and the other to be performed next by the VPU 1) as shown in the flowchart in FIG. 57 (step S211). Then, the scheduler extracts threads (thread A in the partial operation to be performed first and thread B in the partial operation to be performed next) which inputs/outputs data through a buffer between the two VPUs (step S212). The threads A and B are scheduled such that the thread A starts to run after the end of the execution term for the thread B in each period (step S213).

[0144] The execution term of the thread B can thus be interposed between the two execution terms of the thread A corresponding to consecutive two periods.

[0145] FIG. 58 shows a specific example of scheduling performed in consideration of the number of buffers. As described above, the thread DEMUX in the first thread group is a thread for writing to a buffer data to be transferred to the A-DEC in the second thread group. In order to transfer data between the threads DEMUX and A-DEC by a single buffer, in the example of FIG. 58, the execution start timing of each of the threads A-DEC and DEMUX is controlled such that the thread DEMUX starts to run after the thread A-DEC completes running in each period. The VPU runtime environment 401 reserves a buffer area 1 on the memory 14 when the thread DEMUX starts to run in period 1 and releases it when the thread A-DEC completes running in the next period 2. Then, the VPU runtime environment 401 reserves the buffer area 1 on the memory 14 when the thread DEMUX starts to run in period 2 and releases it when the thread A-DEC completes running in the next period 3.

Reservation Graph having a Hierarchical Structure

[0146] Though the reservation graph shown in FIG. 47 has no hierarchical structure, a reservation graph having a hierarchical structure can be used as shown in FIG. 59. In FIG. 59, the execution term A precedes the execution term B and the execution term B precedes the execution term C. In the execution term B, the execution term D precedes execution terms E and F. Resolving the hierarchy, the execution term A precedes the execution term D and the execution terms E and F precede

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the execution term C.

Reservation Request made in Consideration of Tightly Coupled Thread Group

[0147] In the reservation graph shown in FIG. 47, when a thread executing the V-DEC and a thread executing the PROG belong to the tightly coupled thread group, a reservation request indicative of the coupled attribute is created as shown in FIG. 60. In this reservation request, "TightlyCoupled" indicates an ID of the execution term corresponding to the partner thread. The above threads are therefore scheduled as shown in FIG. 61 such that they can be executed at once by different VPUs. In this case, the threads can communicate with each other via a local storage and thus no buffers need to be provided on the memory 14.

Scheduling Algorithm based on Structural Description

[0148] There now follows descriptions as to a procedure for reserving an execution term of each thread based on the structural description incorporated into the program module.

[0149] FIG. 8 shows an example of the structural description 117 incorporated in the program module 100 shown in FIG. 7. With the structural description 117, the VPU runtime environment 401 performs the following steps.

1. The programs that are written in the module field of the structural description 117 are loaded to generate threads that execute the programs.

In the present embodiment, one thread is generated for each of entries of the structural description 117. If the structural description 117 includes entries having the same module name, a plurality of threads that execute the same module are generated so as to correspond to their respective entries. In the example of FIG. 8, all threads are generated to belong to one process; however, the threads can belong to different processes or thread groups can belong to different processes.

2. A reservation request having a data structure as shown in FIG. 48 is created based on the information of the structural description 117.

3. The reservation request is sent to the VPU runtime environment to schedule the threads and start to run the threads.

[0150] The above step 2 of creating the reservation request is performed as follows.

[0151] First, BUFFER records are created to correspond to the output fields of the structural description 117 in a one-to-one basis and added to the reservation request. For instance, in the example of FIG. 8, the second output data of the DEMUX module is supplied to the V-DEC through the 1-MB buffer, so that a BUFFER record whose Id is 2 as shown in FIG. 48 is created. In this BUFFER record, the buffer size is described as 1MB in Size field, reference to TASK record whose Id is 1 and which corresponds to a DEMUX module that writes data to the buffer is described in SrcTask field, and reference to TASK record whose Id is 3 and which corresponds to a V-DEC module that reads data from the buffer is described in DstTask field.

[0152] Then, TASK records are created to correspond to the module fields of the structural description 117 on a one-to-one basis and added to the reservation request. For instance, in the example of FIG. 8, a TASK record whose Id is 3 as shown in FIG. 48 is created as one corresponding to the V-DEC module. This TASK record has the following information.

[0153] Class field: Flag to indicate what attribute is used to execute a thread designated in the TASK record.

[0154] In this field, "VPU" represents a thread that runs on the VPU and "HRT" shows a thread in the hard-real time class. These information items are set based on the information described in the thread parameters of the structural description 117 shown in FIG. 8.

[0155] ThreadContext field: Flag to designate a thread context of a thread whose running is to be reserved in the TASK record. More specifically, a program module designated in the module field of the structural description 117 is loaded, a thread that executes the program module is generated by the VPU runtime environment 401, and an identifier (a pointer or the like) of the thread context of the thread is recorded in the "ThreadContext" field.

[0156] Constraint field: Flag to record constraints of the TASK record. When the constraint is precedence constraint, a required number of Ids of another TASK record preceded by the TASK record is designated after the "Precede" field. For example, a TASK record whose Id is 3 precedes a TASK record corresponding to the PROG module whose Id is 5.

[0157] InputBuffer field: Flag to designate a required number of Ids of the Buffer record of a buffer from which data is read by the thread designated by the TASK record.

[0158] OutputBuffer field: Flag to designate a required number of Ids of the Buffer record of a buffer to which data is written by the thread designated by the TASK record.

[0159] If the structural description is provided as discussed above, its corresponding reservation request is created.

[0160] When the reservation request is sent to the scheduler in the VPU runtime environment 401, the scheduler creates a schedule necessary for performing the reservation request. This schedule represents which VPU is allocated to which thread with which timing and how long the VPU is allocated in a period as shown in FIG. 49. Actually, the schedule can be represented by a reservation list as shown in FIG. 62.

[0161] The reservation list shown in FIG. 62 includes

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reservation entries related to the respective VPUs. Each of the reservation entries includes a start time field indicating when a thread is executed by VPU in each period (execution start timing of the thread), an execution term field indicating how long the VPU is allocated to the thread (execution term of the thread), and a running thread field indicating an identifier of the thread. The reservation entries are sorted in order of start time according to the VPUs and linked to the reservation list.

[0162] The procedure for creating a reservation list as shown in FIG. 62 from the reservation request shown in FIG. 48 or FIG. 60 can be carried out by the flowchart shown in FIG. 63.

[0163] Basically, the TASK records in the reservation request have only to be sequenced in consideration of the relationship in input/output using BUFFER and the running time of VPUs has only to be assigned to each of the TASK records in the order of data flow. It is then necessary to simultaneously allocate the VPUs to the Tasks belonging to the tightly coupled thread group.

[0164] The procedure is shown in FIG. 63. Upon receiving a reservation request, the VPU runtime environment 401 schedules all the tasks designated by TASK records in the reservation request by the following steps (in other words, the VPU runtime environment 401 creates a reservation list for reserving a VPU to which each task is assigned and the execution start timing and execution term of the task).

[0165] Step S301: The VPU runtime environment 401 selects a task whose all of preceding tasks (input tasks) have been already scheduled, and which have no tightly coupled attributes, from among tasks that are not scheduled. If a task is preceded by no input tasks, it is determined as one whose input tasks have been already scheduled.

[0166] If there is a task whose input tasks have been already scheduled, and which have no tightly coupled attributes, the VPU runtime environment 401 selects it and moves to step S302. If not, it moves to step S304.

[0167] Step S302: If there is a VPU that can assign the execution start timing and execution term of the selected task under satisfactory constraints, the VPU runtime environment 401 moves to step S303. If not, the VPU runtime environment 401 fails in the scheduling and makes a notification of the fail.

[0168] Step S303: The VPU runtime environment 401 creates reservation entries of the selected task and links them to the reservation list.

[0169] Step S304: The VPU runtime environment 401 selects tasks whose all input tasks have been already scheduled, and that belong to a tightly coupled group, from among tasks that are not scheduled. If tasks are preceded by no input tasks, they are determined as ones whose input tasks have been already scheduled.

[0170] If there are tasks whose input tasks have been already scheduled, and which belong to the tightly coupled group, the VPU runtime environment 401 selects them and moves to step S305. If not, it ends scheduling.

Step S305: If there are VPUs that can reserve all tasks included in the selected tasks at once (to have the same execution start timing and the same execution term), the VPU runtime environment 401 moves to step S306. If not, the VPU runtime environment 401 fails in the scheduling and makes a notification of the fail.

[0171] Step S306: Reservation entries of all tasks of the selected set of tasks are created and linked to the reservation list.

[0172] The steps of scheduling for one reservation request has been described. Actually, a plurality of reservation requests are usually present at once in one system. In this case, the reservation requests can be scheduled through the above steps and, more favorably, they can be done simultaneously through the above steps.

[0173] The present embodiment has been described taking the program module describing the operations of a digital TV broadcast receiver as an example. If, however, a program module describing the operations of various types of hardware is prepared, the operations of hardware can be performed by software.

[0174] The MPU 11 and VPUs 12 provided in the computer system shown in FIG. 1 can be implemented as parallel processor mixed on one chip. In this case, too, the VPU running environment executed by the MPU 11 or the VPU running environment executed by a specific VPU or the like can control scheduling for the VPUs 12.

[0175] The software pipeline operation can be performed by three VPUs. A plurality of chained tasks for performing a real-time operation are divided into first to three task groups to be processed in sequence. Each of the task groups is periodically assigned to at least one of the VPUs such that the three VPUs periodically execute the three task groups in pipeline mode. If VPU1, VPU2 and VPU3 are used, the VPU0 periodically executes the first task group, the VPU1 periodically executes the second task group with a one-period delay relative to the first task group, and the VPU2 periodically executes the third task group with a one-period delay relative to the second task group.

[0176] A plurality of VPUs can execute the tasks of a task group in parallel. If a task group includes a plurality of tasks that can run in parallel, a plurality of VPUs can execute the tasks of the task group in parallel.

[0177] If the programs running as the VPU running environment or the programs of the operating system including the VPU running environment are stored in a computer readable storage medium and then introduced and executed in a computer including a plurality of processors each having a local memory, the same advantages as those of the foregoing embodiment of the present invention can be obtained.

Claims

1. A method of periodically performs a real-time operation including a plurality of chained tasks using a

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plurality of processors (12), the method **characterized by** comprising the steps of:

dividing the chained tasks into a first task group and a second task group based on a relationship in order of execution among the tasks, the second task group being executed after the first task group; and
performing a scheduling operation of periodically assigning each of the first task group and the second task group to at least one of the processors (12) to periodically execute the first task group at regular time intervals and periodically execute the second task group at the regular time intervals with a one-period delay relative to the first task group.

2. The method according to claim 1, **characterized in that** the first task group includes a first task of the chained tasks which writes, to a buffer, data to be transferred to a second task of the chained tasks included in the second task group, and the method further comprises the steps of:

reserving the buffer on a memory (14) shared by the processors when the first task starts to run; and
releasing the buffer when the second task completes running.

3. The method according to claim 1, **characterized in that** the first task group includes a first task of the chained tasks which writes, to a buffer, data to be transferred to a second task of the chained tasks included in the second task group, and the method further comprises a step of controlling execution start timing of each of the first task and the second task to start the execution of the first task in each period corresponding to each of the regular time intervals after the execution of the second task is completed in said each period.

4. The method according to claim 1, **characterized in that** the dividing step includes dividing the chained tasks into the first task group, the second task group and a third task group based on a relationship in order of execution among the tasks, the third task group being executed after the second task group; and the performing step includes performing a scheduling operation of periodically assigning each of the first task group, the second task group and the third task group to at least one of the processors (12) to periodically execute the first task group at the regular time intervals, periodically execute the second task group at the regular time intervals with a one-period delay relative to the first task group, and periodically execute the third task group at the regular time intervals with a one-period delay relative to the second task group.

5. An information processing system which periodically performs a real-time operation including a plurality of chained tasks, the system **characterized by** comprising:

a plurality of processors (12);
means for dividing the chained tasks into a first task group and a second task group based on a relationship in order of execution among the tasks, the second task group being executed after the first task group; and
means for performing a scheduling operation of periodically assigning each of the first task group and the second task group to at least one of the processors (12) to periodically execute the first task group at regular time intervals and periodically execute the second task group at the regular time intervals with a one-period delay relative to the first task group.

6. The information processing system according to claim 5, **characterized in that** the first task group includes a first task of the chained tasks which writes, to a buffer, data to be transferred to a second task of the chained tasks included in the second task group, and the system further comprises:

a memory (14) shared by the processors (12);
means for reserving the buffer on the memory (14) when the first task starts to run; and
means for releasing the buffer when the second task completes running.

7. The information processing system according to claim 5, **characterized in that** the first task group includes a first task of the chained tasks which writes, to a buffer, data to be transferred to a second task of the chained tasks included in the second task group, and the system further comprises means for controlling execution start timing of each of the first task and the second task to start the execution of the first task in each period corresponding to each of the regular time intervals after the execution of the second task is completed in said each period.

8. The information processing system according to claim 5, **characterized in that** the means for dividing includes means for dividing the chained tasks into the first task group, the second task group and a third task group based on a relationship in order of execution among the tasks, the third task group being executed after the second task group, and the means for performing the scheduling operation includes means for performing a scheduling operation of periodically assigning each of the first task

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group, the second task group and the third task group to at least one of the processors (12) to periodically execute the first task group at the regular time intervals, periodically execute the second task group at the regular time intervals with a one-period delay relative to the first task group, and periodically execute the third task group at the regular time intervals with a one-period delay relative to the second task group.

9. A program which is stored in a computer-readable media and causes a computer including a plurality of processors (12) to periodically perform a real-time operation including a plurality of chained tasks, the program **characterized by** comprising:

causing the computer to divide the chained tasks into a first task group and a second task group based on a relationship in order of execution among the tasks, the second task group being executed after the first task group; and
causing the computer to perform a scheduling operation of periodically assigning each of the first task group and the second task group to at least one of the processors (12) to periodically execute the first task group at regular time intervals and periodically execute the second task group at the regular time intervals with a one-period delay relative to the first task group.

10. The program according to claim 9, **characterized in that** the first task group includes a first task of the chained tasks which writes, to a buffer, data to be transferred to a second task of the chained tasks included in the second task group, and the program further comprises:

causing the computer to reserve the buffer on a memory (14) shared by the processors when the first task starts to run; and
causing the computer to release the buffer when the second task completes running.

11. The program according to claim 9, **characterized in that** the first task group includes a first task of the chained tasks which writes, to a buffer, data to be transferred to a second task of the chained tasks included in the second task group, and the program further comprises causing the computer to control execution start timing of each of the first task and the second task to start the execution of the first task in each period corresponding to each of the regular time intervals after the execution of the second task is completed in said each period.

12. The program according to claim 9, **characterized in that** causing the computer to divide the chained tasks includes causing the computer to divide the chained tasks into the first task group, the second task group and a third task group based on a relationship in order of execution among the tasks, the third task group being executed after the second task group; and causing the computer to perform the scheduling operation includes causing the computer to perform the scheduling operation of periodically assigning each of the first task group, the second task group and the third task group to at least one of the processors (12) to periodically execute the first task group at the regular time intervals, periodically execute the second task group at the regular time intervals with a one-period delay relative to the first task group, and periodically execute the third task group at the regular time intervals with a one-period delay relative to the second task group.

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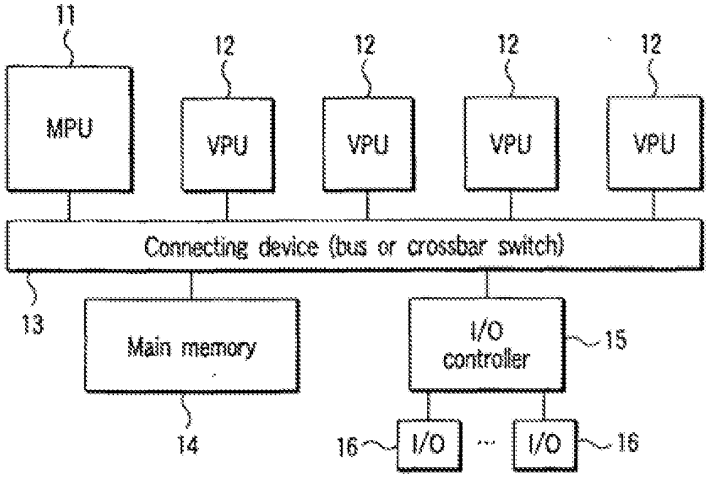

11
12
12
12
12
MPU
VPU
VPU
VPU
VPU
Connecting device (bus or crossbar switch)
13
Main memory
I/O controller
15
14
16
I/O
I/O
16

FIG. 1

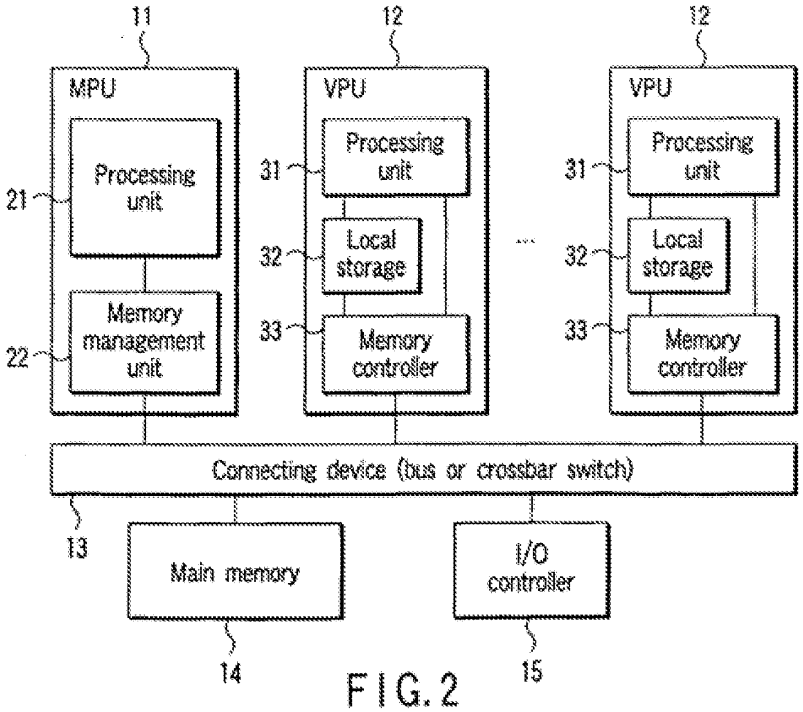

11
12
12
MPU
VPU
VPU
Processing unit
21
Memory management unit
22
31
Processing unit
32
Local storage
33
Memory controller
31
Processing unit
32
Local storage
33
Memory controller
Connecting device (bus or crossbar switch)
13
Main memory
I/O controller
14
15

FIG. 2

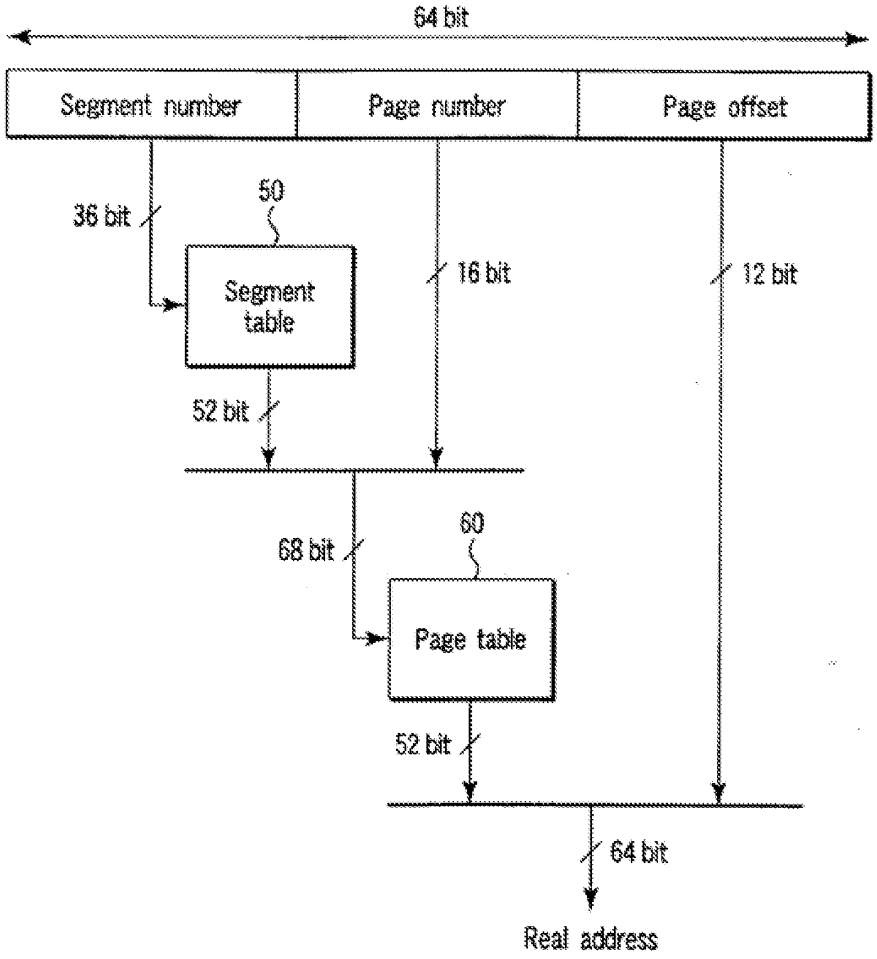

64 bit
Segment number
Page number
Page offset
36 bit
50
Segment table
16 bit
12 bit
52 bit
68 bit
60
Page table
52 bit
64 bit
Real address

FIG. 3

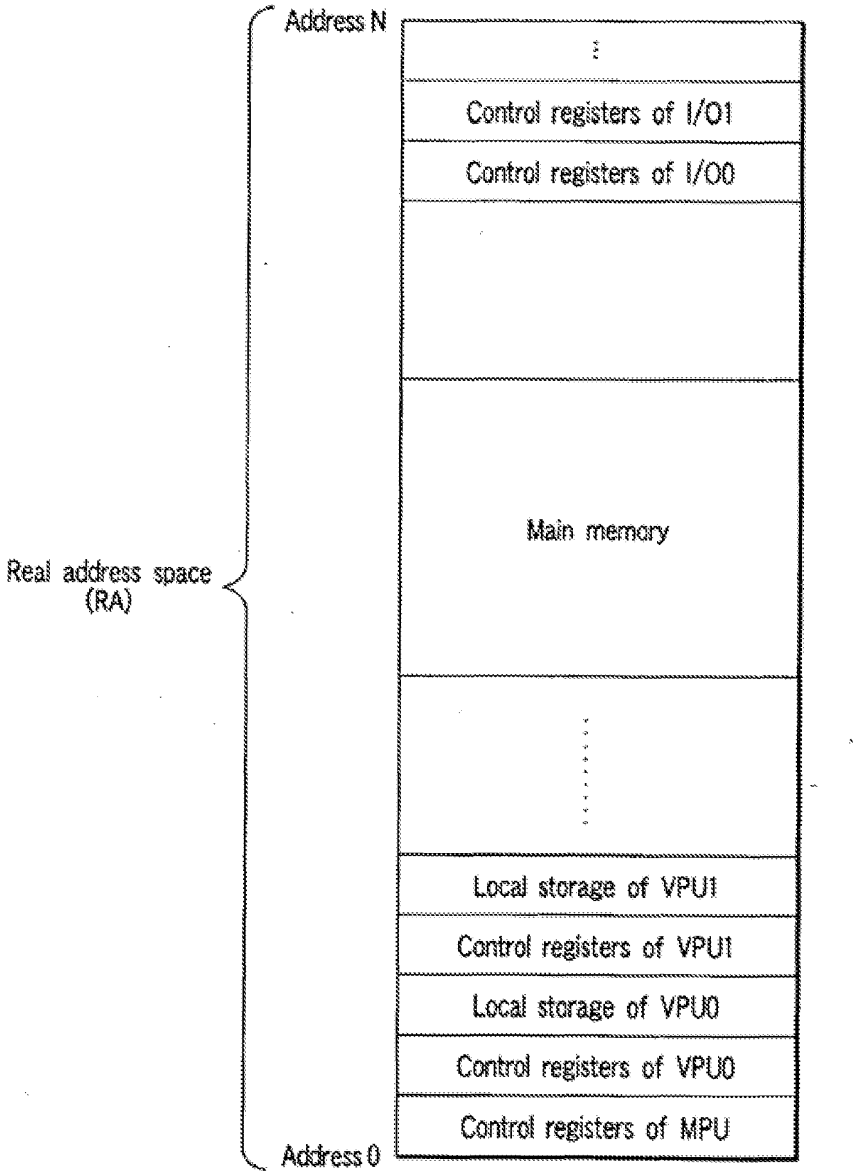

Address N
Control registers of I/O1
Control registers of I/O0
Main memory
Real address space
(RA)
Local storage of VPU1
Control registers of VPU1
Local storage of VPU0
Control registers of VPU0
Control registers of MPU
Address 0

FIG. 4

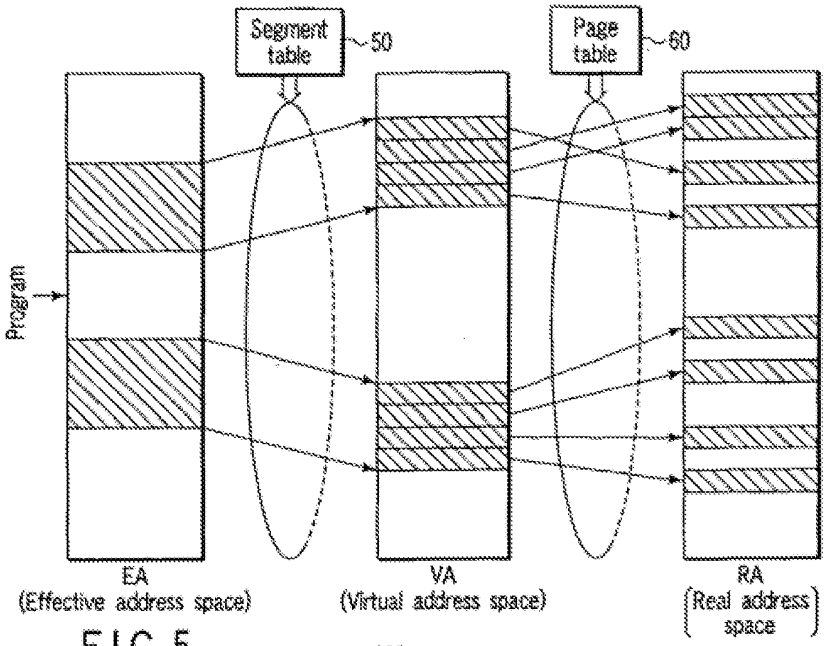


FIG. 5

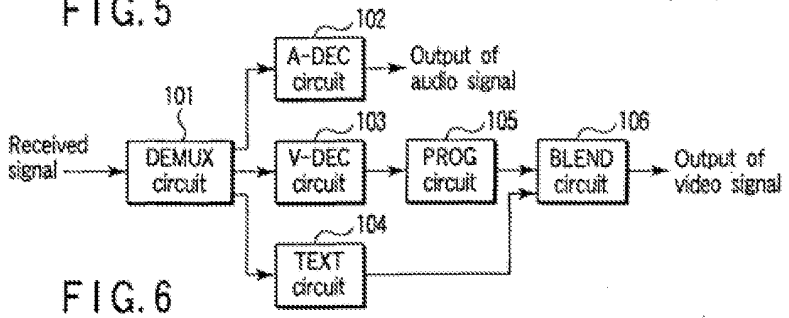


FIG. 6

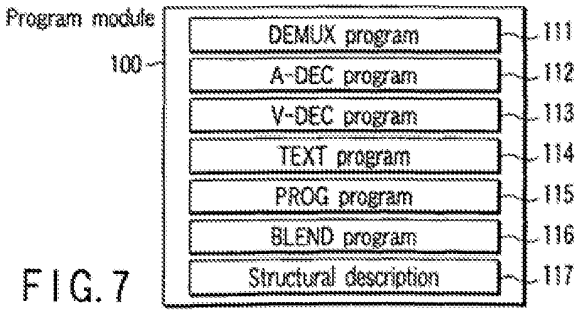


FIG. 7

Structural description 117

Number	Program	Input	Output	Cost	Buffer
(1)	DEMUX	Received signal	(2) (3) (4)	5	100KB 1MB 10KB
(2)	A-DEC	(1)	Audio output	10	———
(3)	V-DEC	(1)	(5)	50	1MB
(4)	TEXT	(1)	(6)	5	10KB
(5)	PROG	(3)	(6)	20	1MB
(6)	BLEND	(4) (5)	Video output	10	———
Thread parameters { · Tightly coupled thread group : · Loosely coupled thread group : }					
Others					

FIG. 8

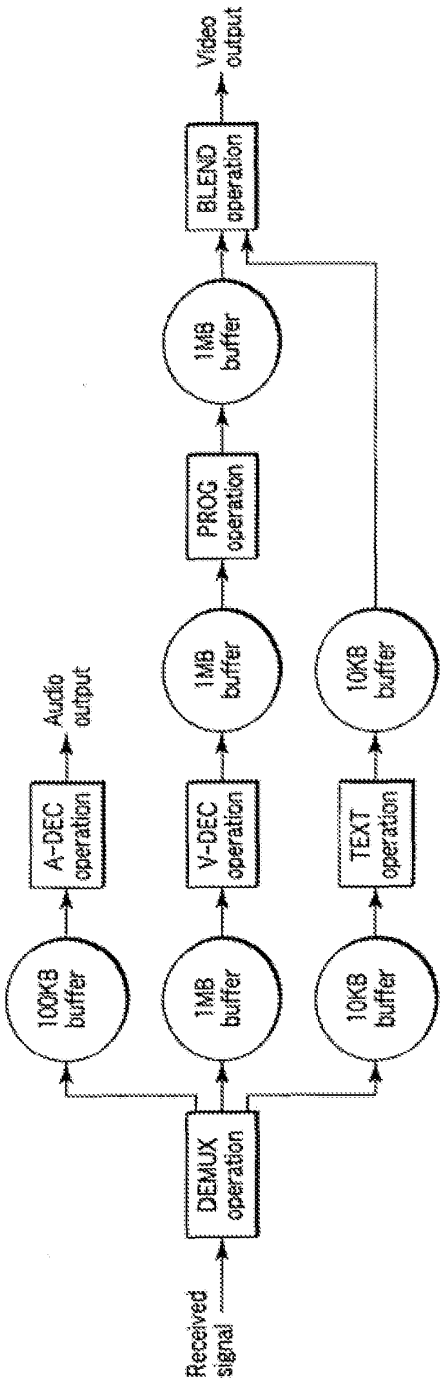

Received signal
DEMUX operation
100KB buffer
1MB buffer
10KB buffer
A-DEC operation
V-DEC operation
TEXT operation
Audio output
1MB buffer
10KB buffer
PROG operation
1MB buffer
BLEND operation
Video output

FIG. 9

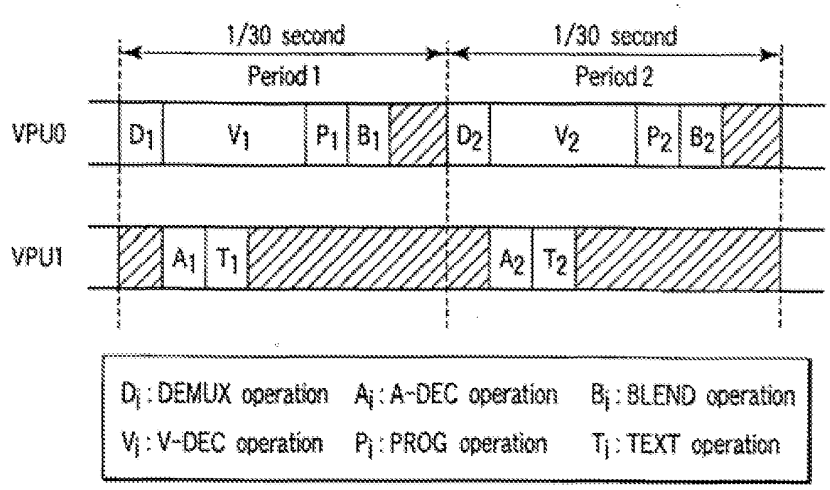

1/30 second
Period 1
1/30 second
Period 2
VPU0
D1
V1
P1
B1
D2
V2
P2
B2
VPU1
A1
T1
A2
T2
Di : DEMUX operation
Ai : A-DEC operation
Bi : BLEND operation
Vi : V-DEC operation
Pi : PROG operation
Ti : TEXT operation

FIG. 10

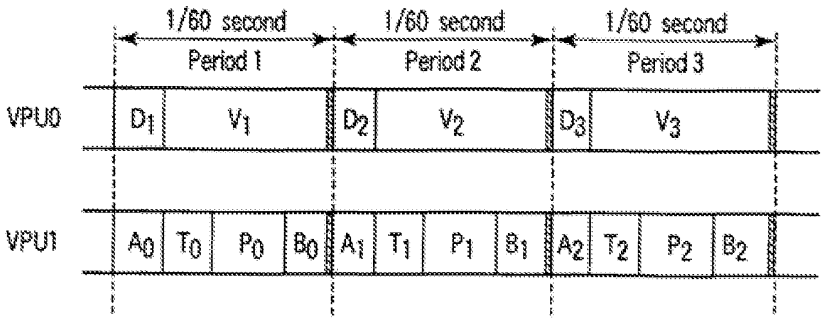

1/60 second
Period 1
1/60 second
Period 2
1/60 second
Period 3
VPU0
D1
V1
D2
V2
D3
V3
VPU1
A0
T0
P0
B0
A1
T1
P1
B1
A2
T2
P2
B2

FIG. 11

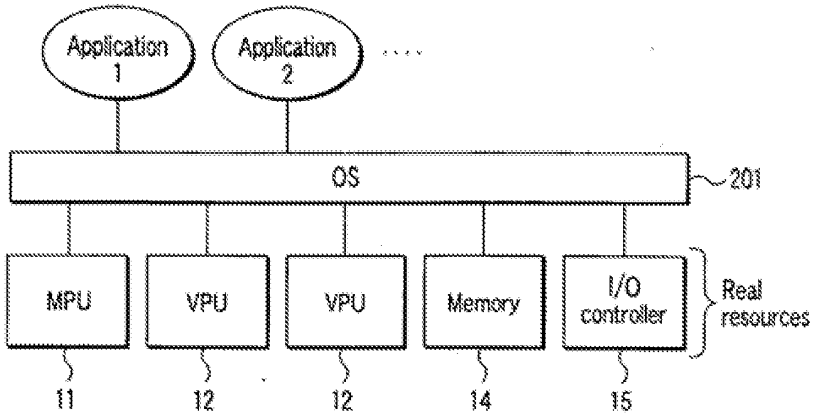

Application 1
Application 2
OS
201
MPU
VPU
VPU
Memory
I/O controller
Real resources
11
12
12
14
15

FIG. 12

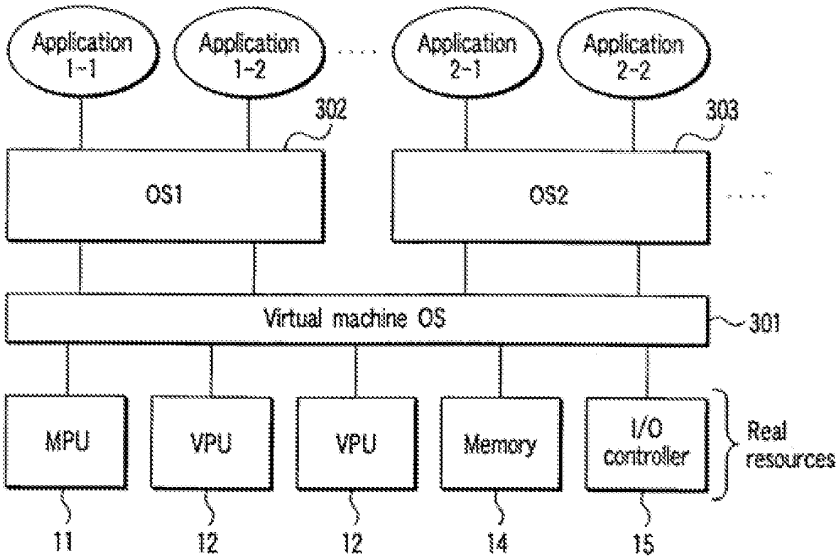

Application 1-1
Application 1-2
Application 2-1
Application 2-2
302
303
OS1
OS2
Virtual machine OS
301
MPU
VPU
VPU
Memory
I/O controller
Real resources
11
12
12
14
15

FIG. 13

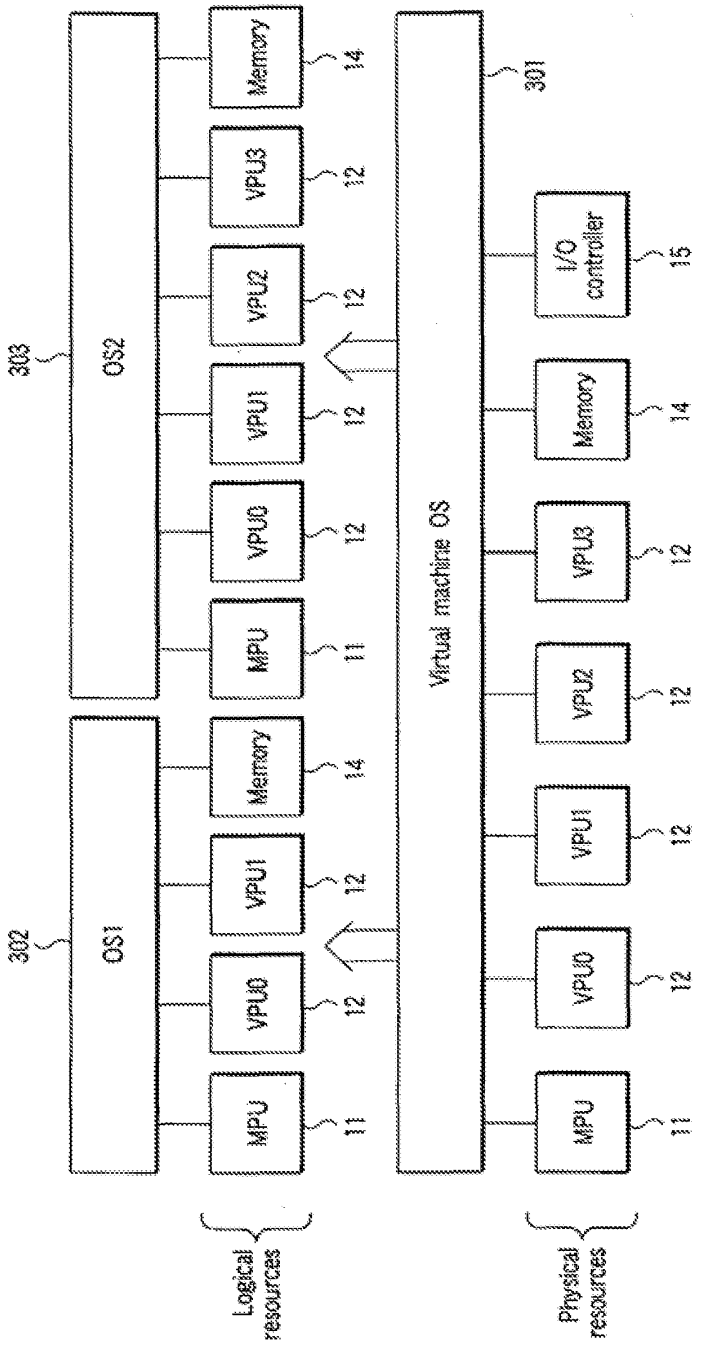

303
OS2
302
OS1
MPU
11
VPU0
12
VPU1
12
Memory
14
VPU2
12
VPU3
12
Virtual machine OS
301
I/O controller
15
Logical resources
Physical resources

FIG. 14

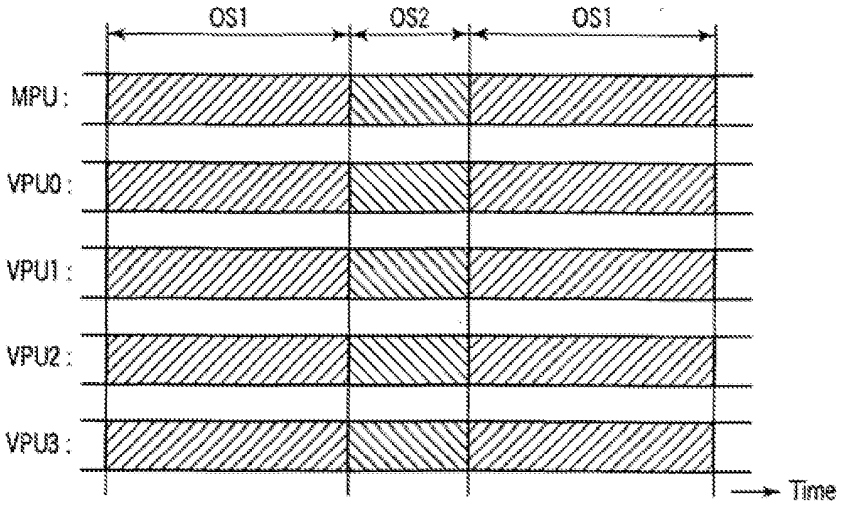

OS1
OS2
OS1
MPU :
VPU0 :
VPU1 :
VPU2 :
VPU3 :
Time

FIG. 15

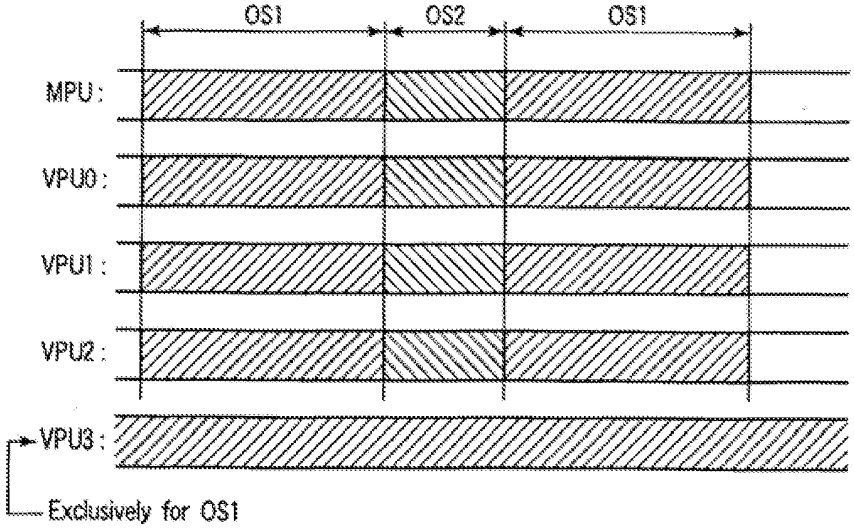

OS1
OS2
OS1
MPU :
VPU0 :
VPU1 :
VPU2 :
VPU3 :
Exclusively for OS1

FIG. 16

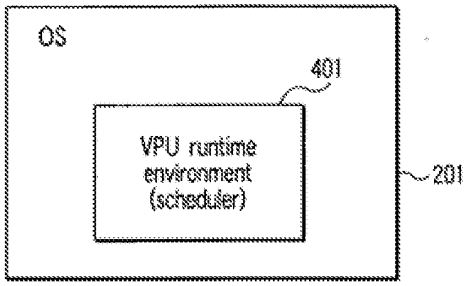


FIG. 17

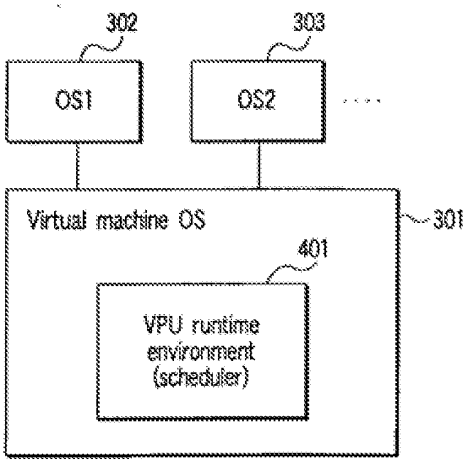


FIG. 18

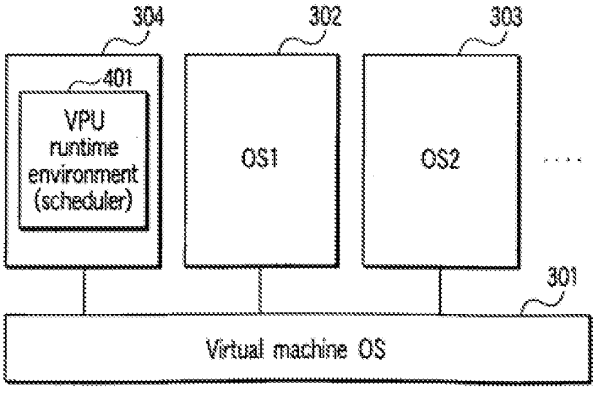


FIG. 19

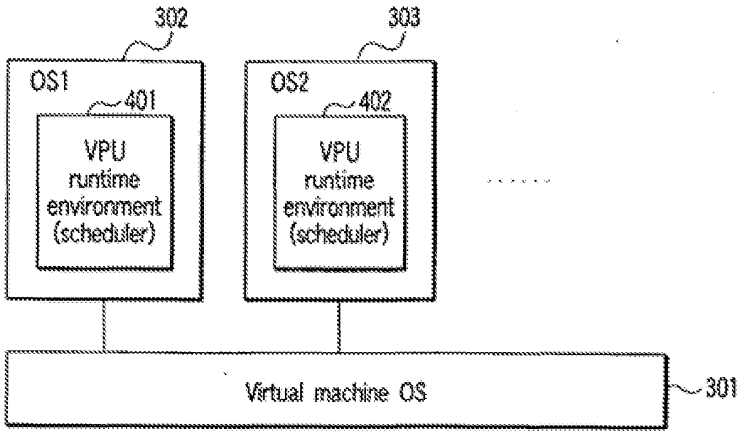

302
303
OS1
401
VPU runtime environment (scheduler)
OS2
402
VPU runtime environment (scheduler)
Virtual machine OS
301

FIG. 20

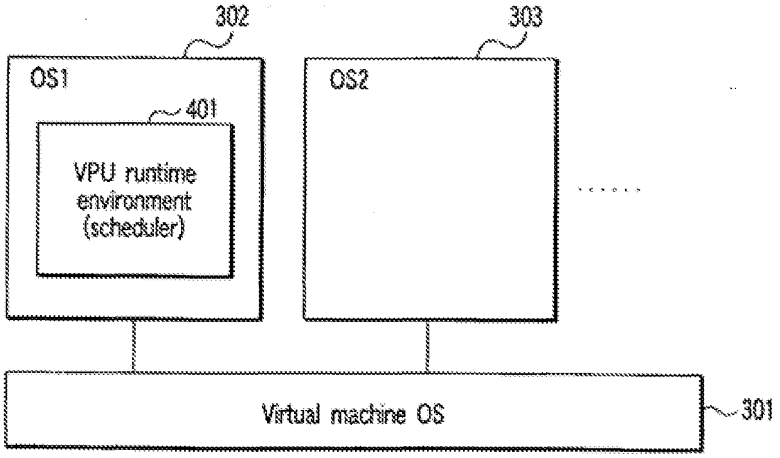

302
303
OS1
401
VPU runtime environment (scheduler)
OS2
Virtual machine OS
301

FIG. 21

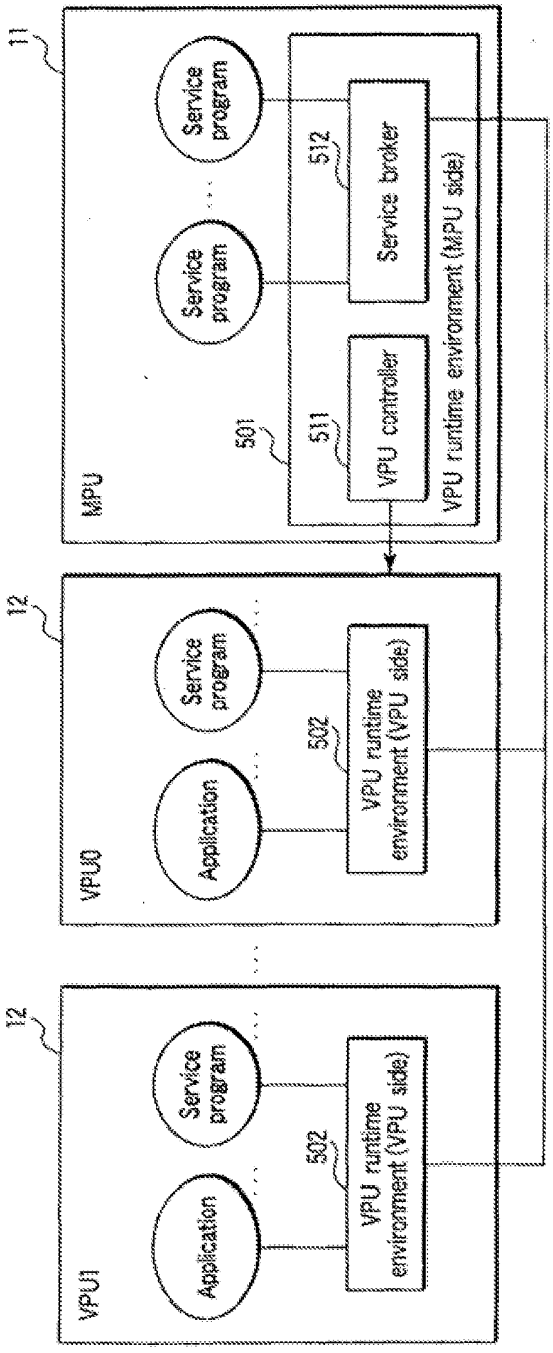

11
MPU
Service program
Service program
501
511
VPU controller
512
Service broker
VPU runtime environment (MPU side)
12
VPU0
Service program
Application
502
VPU runtime environment (VPU side)
12
VPU1
Service program
Application
502
VPU runtime environment (VPU side)

FIG. 22

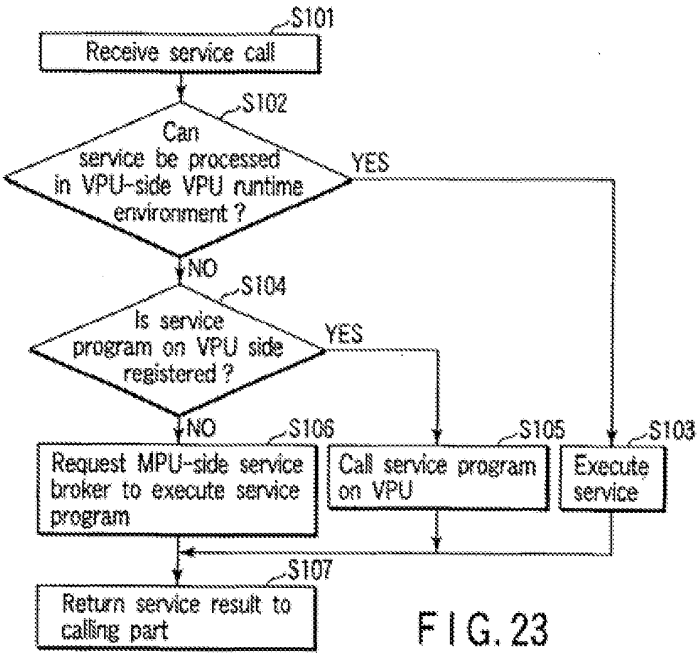

S101
Receive service call
S102
Can service be processed in VPU-side VPU runtime environment ?
YES
NO
S104
Is service program on VPU side registered ?
YES
NO
S106
Request MPU-side service broker to execute service program
S105
Call service program on VPU
S103
Execute service
S107
Return service result to calling part

FIG. 23

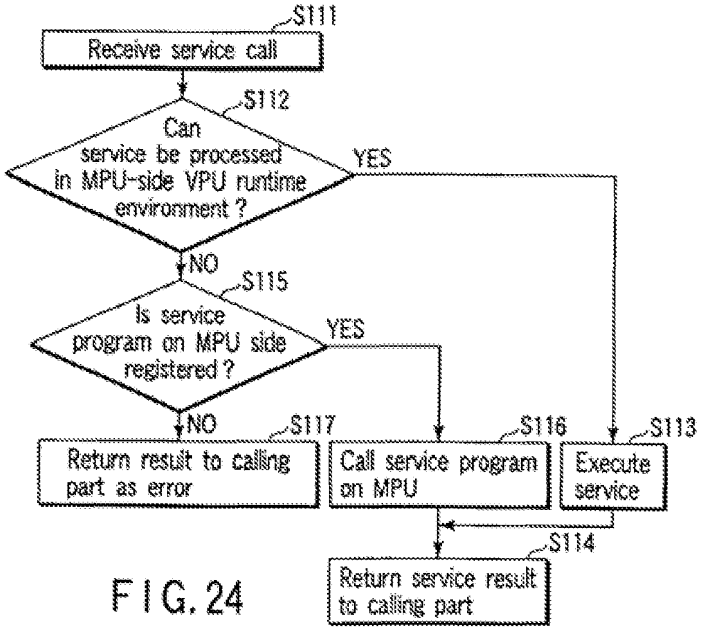

S111
Receive service call
S112
Can service be processed in MPU-side VPU runtime environment ?
YES
NO
S115
Is service program on MPU side registered ?
YES
NO
S117
Return result to calling part as error
S116
Call service program on MPU
S113
Execute service
S114
Return service result to calling part

FIG. 24

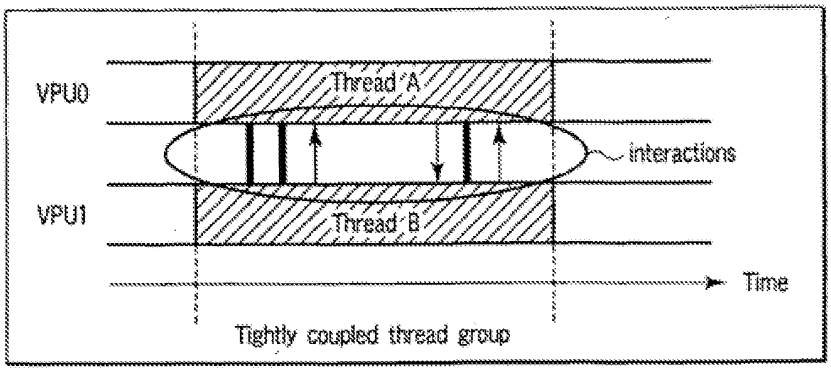

VPU0
Thread A
interactions
VPU1
Thread B
Time
Tightly coupled thread group

FIG. 25

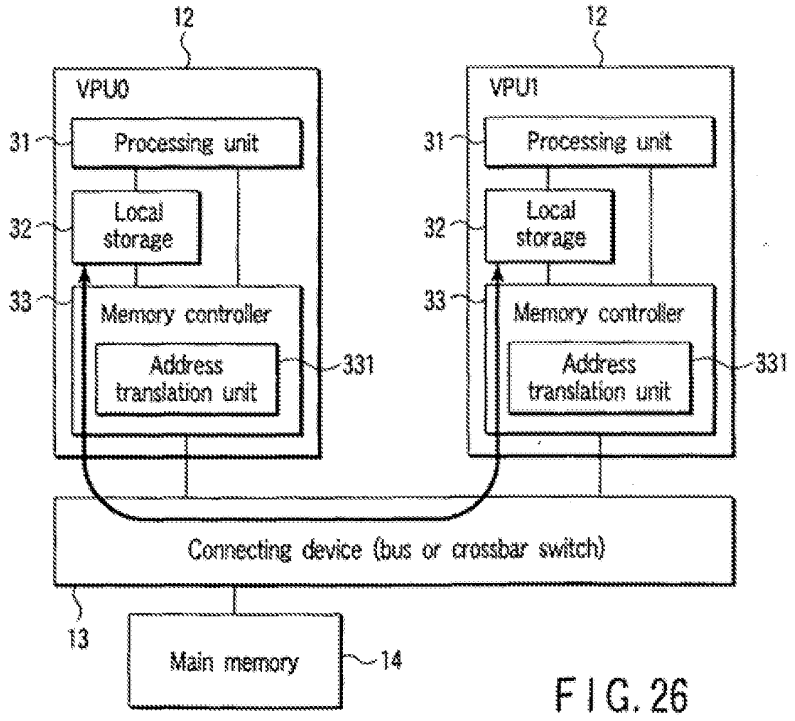

12
12
VPU0
VPU1
31
Processing unit
31
Processing unit
32
Local storage
32
Local storage
33
Memory controller
33
Memory controller
Address translation unit
331
Address translation unit
331
Connecting device (bus or crossbar switch)
13
Main memory
14

FIG. 26

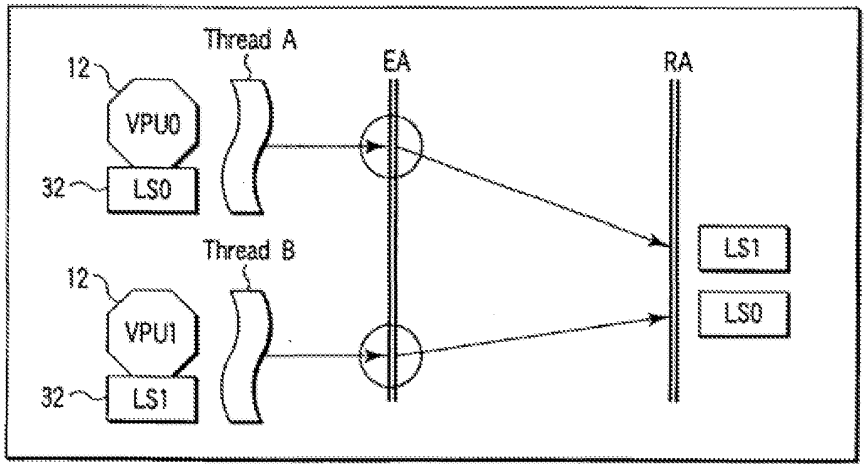

Thread A
12
VPU0
32
LS0
EA
RA
LS1
LS0
Thread B
12
VPU1
32
LS1

FIG. 27

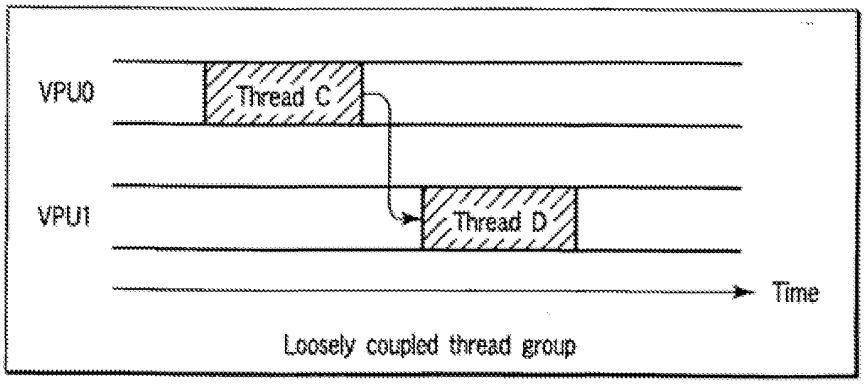

VPU0
Thread C
VPU1
Thread D
Time
Loosely coupled thread group

FIG. 28

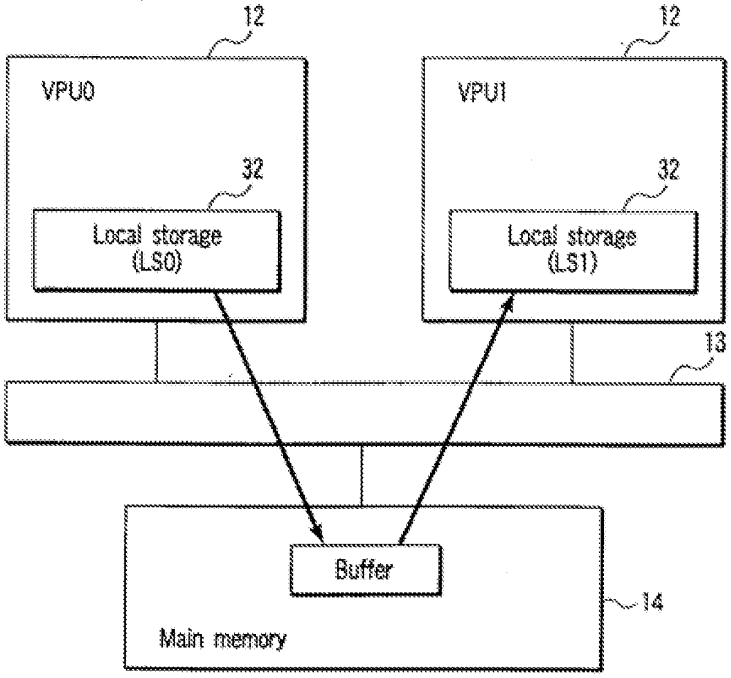

12
12
VPU0
VPU1
32
32
Local storage (LS0)
Local storage (LS1)
13
Buffer
14
Main memory

FIG. 29

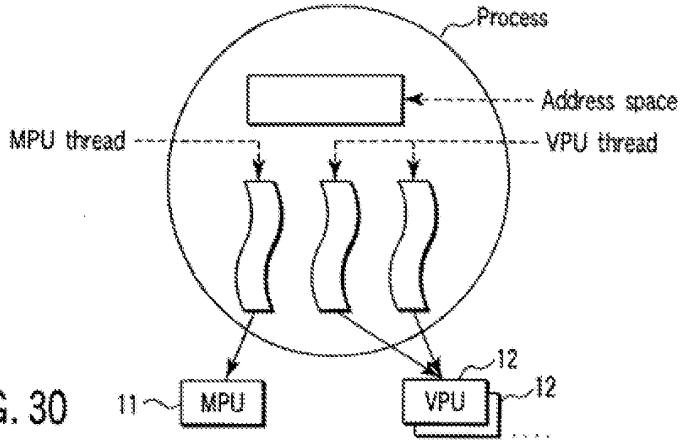

Process
Address space
MPU thread
VPU thread
12
12
11
MPU
VPU

FIG. 30

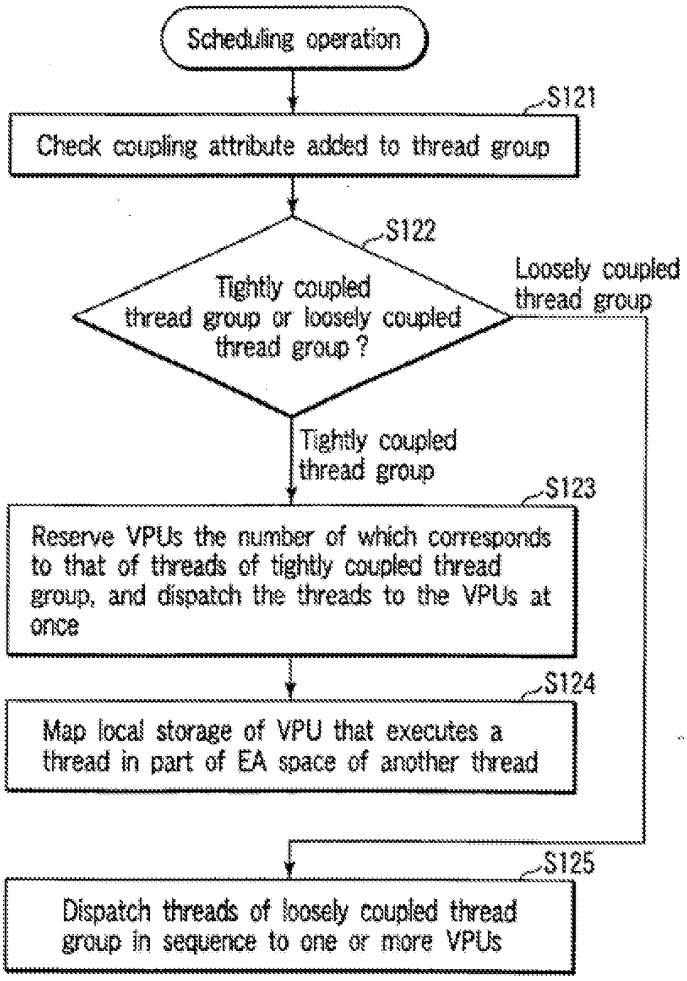

Scheduling operation
S121
Check coupling attribute added to thread group
S122
Tightly coupled thread group or loosely coupled thread group ?
Loosely coupled thread group
Tightly coupled thread group
S123
Reserve VPUs the number of which corresponds to that of threads of tightly coupled thread group, and dispatch the threads to the VPUs at once
S124
Map local storage of VPU that executes a thread in part of EA space of another thread
S125
Dispatch threads of loosely coupled thread group in sequence to one or more VPUs

FIG. 31

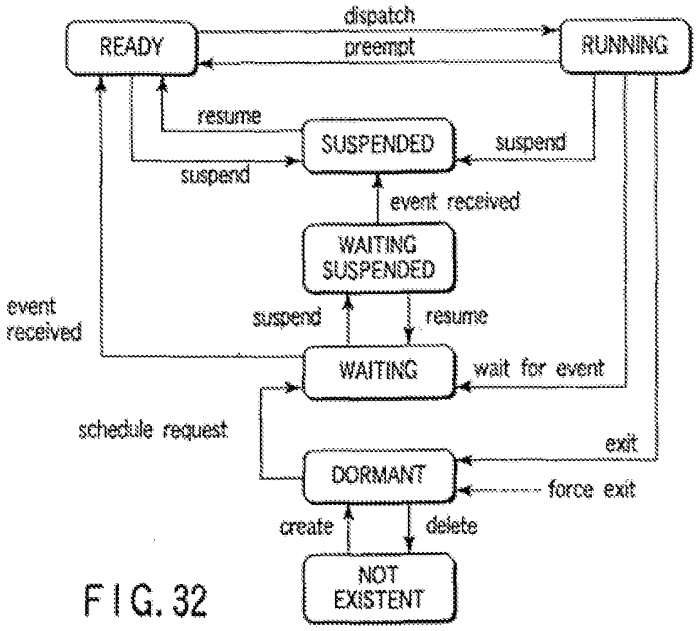


FIG. 32

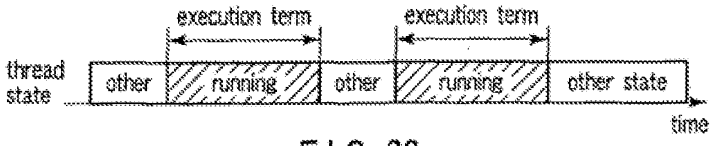


FIG. 33

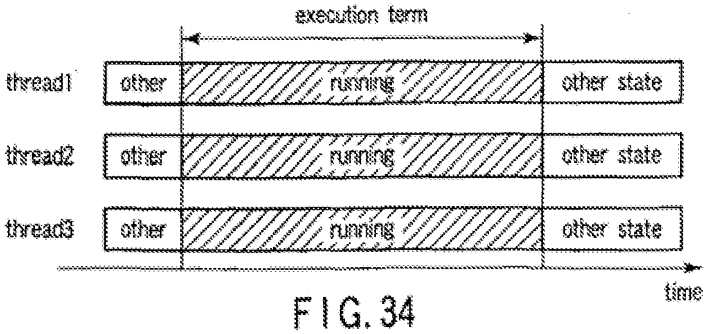


FIG. 34

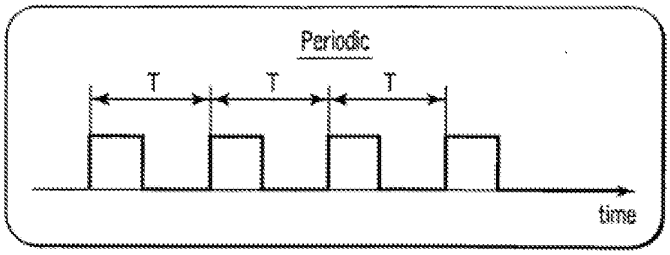


FIG. 35

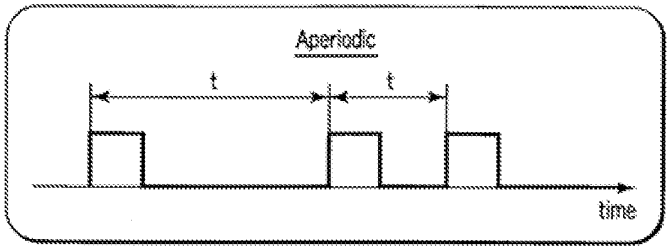


FIG. 36

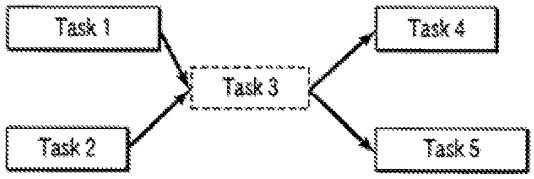


FIG. 37

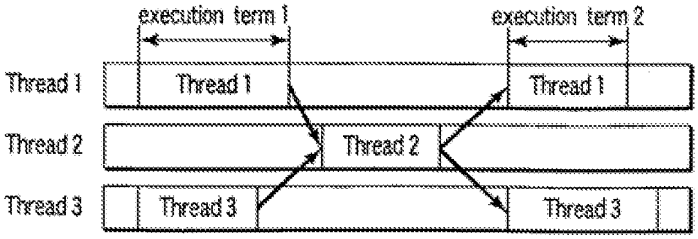


FIG. 38

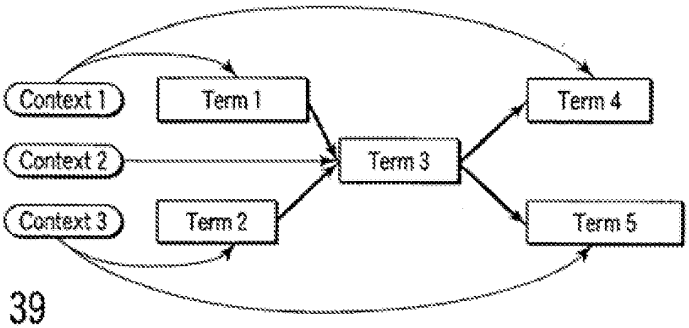


FIG. 39

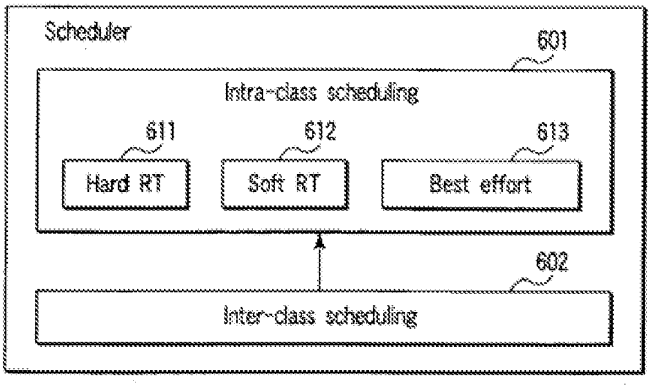


FIG. 40

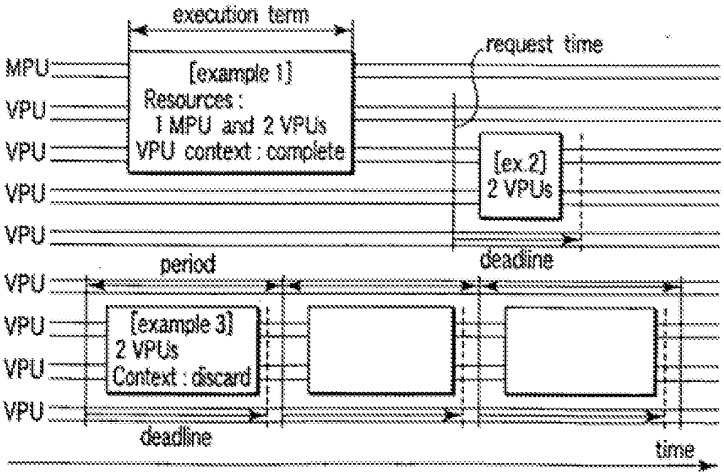


FIG. 41

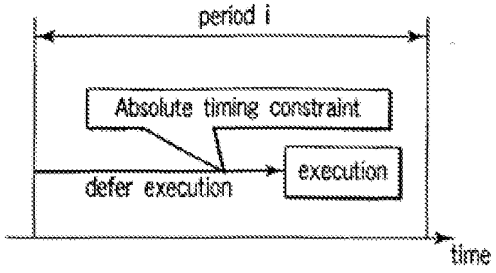


FIG. 42

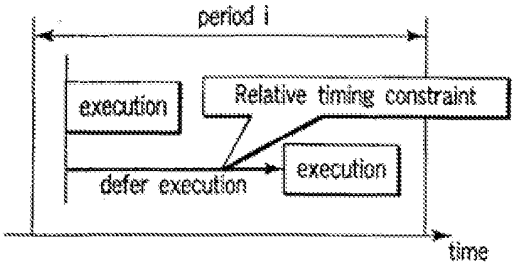


FIG. 43

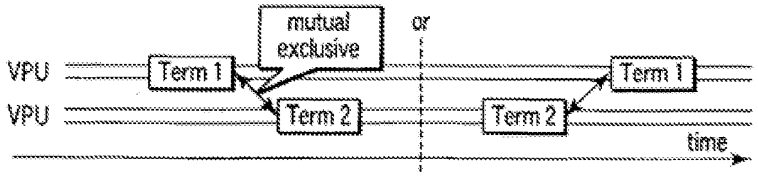


FIG. 44

		Tightly coupled thread group	Loosely coupled thread group
On memory	LS	Can use	Cannot use
	MS	Can use	
Other		Should use hardware primitives	Should use mechanisms provided by VPU Runtime Environment

FIG. 45

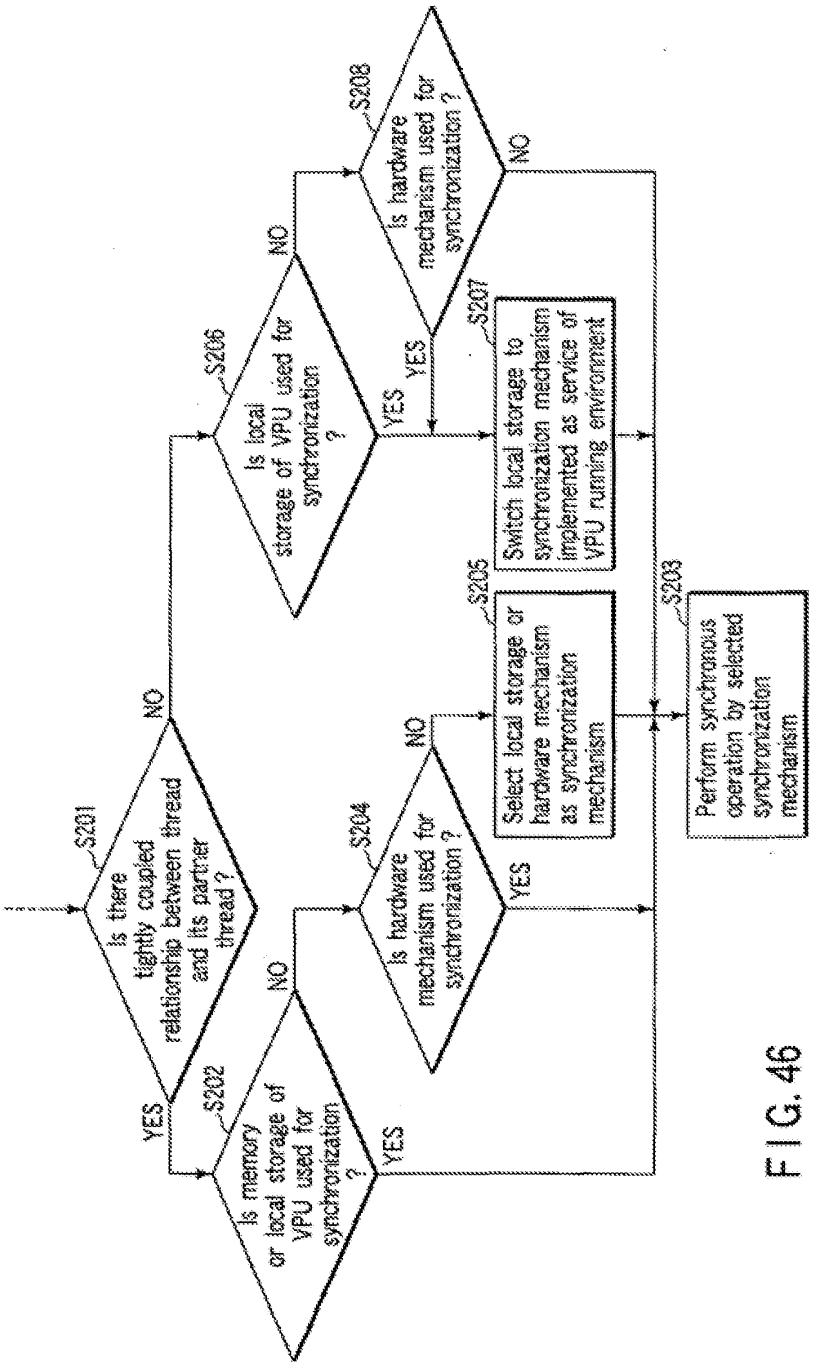

S201
Is there tightly coupled relationship between thread and its partner thread ?
YES
NO
S202
Is memory or local storage of VPU used for synchronization ?
YES
NO
S204
Is hardware mechanism used for synchronization ?
YES
NO
S205
Select local storage or hardware mechanism as synchronization mechanism
S206
Is local storage of VPU used for synchronization ?
YES
NO
S207
Switch local storage to synchronization mechanism implemented as service of VPU running environment
S208
Is hardware mechanism used for synchronization ?
YES
NO
S203
Perform synchronous operation by selected synchronization mechanism

FIG. 46

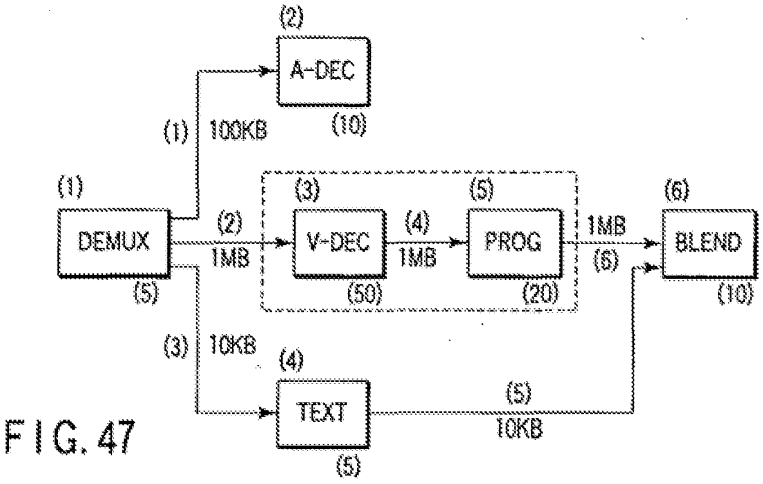


FIG. 47

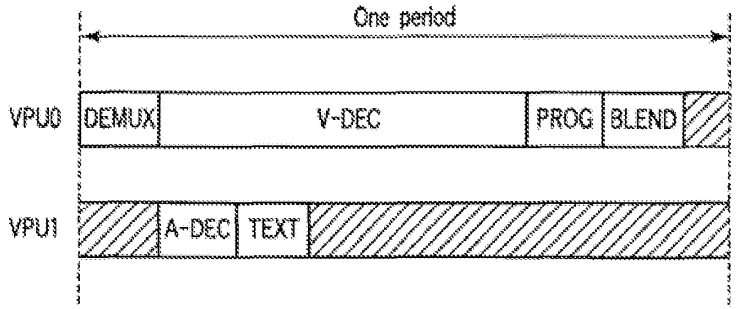


FIG. 49

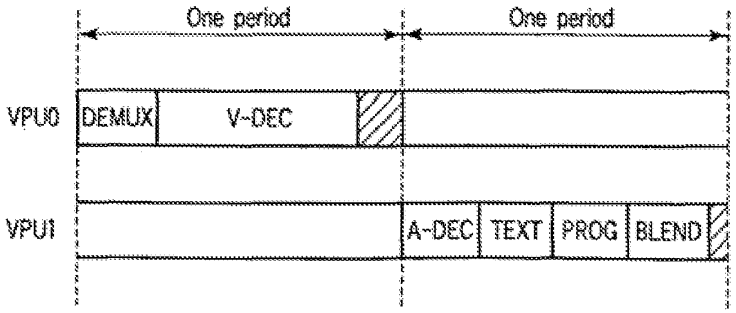


FIG. 50

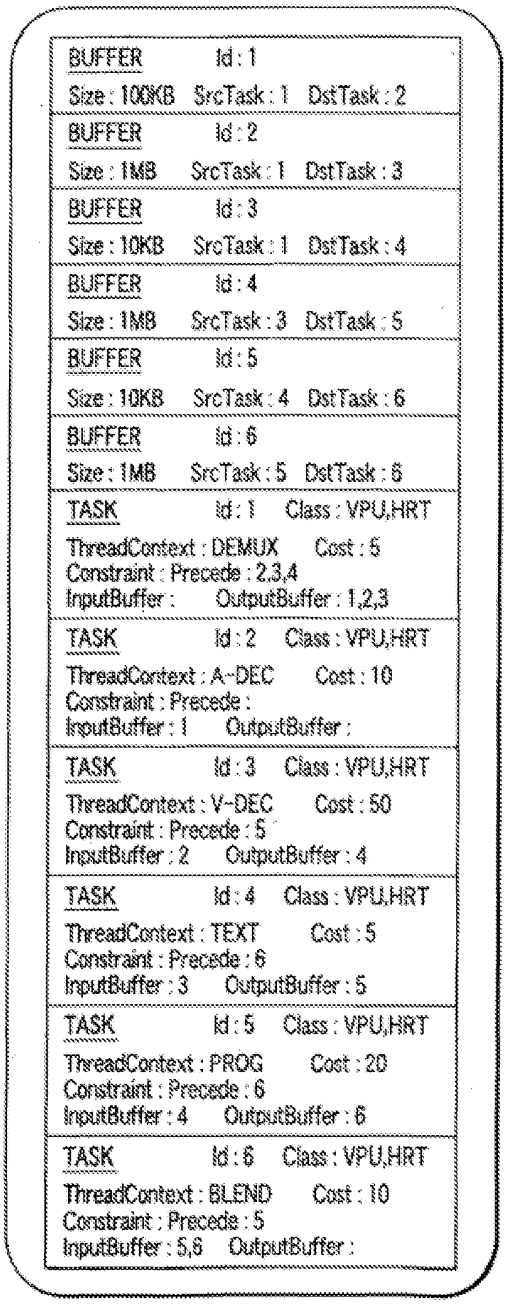

BUFFER Id : 1
Size : 100KB SrcTask : 1 DstTask : 2
BUFFER Id : 2
Size : 1MB SrcTask : 1 DstTask : 3
BUFFER Id : 3
Size : 10KB SrcTask : 1 DstTask : 4
BUFFER Id : 4
Size : 1MB SrcTask : 3 DstTask : 5
BUFFER Id : 5
Size : 10KB SrcTask : 4 DstTask : 6
BUFFER Id : 6
Size : 1MB SrcTask : 5 DstTask : 6
TASK Id : 1 Class : VPU,HRT
ThreadContext : DEMUX Cost : 5
Constraint : Precede : 2,3,4
InputBuffer : OutputBuffer : 1,2,3
TASK Id : 2 Class : VPU,HRT
ThreadContext : A-DEC Cost : 10
Constraint : Precede :
InputBuffer : 1 OutputBuffer :
TASK Id : 3 Class : VPU,HRT
ThreadContext : V-DEC Cost : 50
Constraint : Precede : 5
InputBuffer : 2 OutputBuffer : 4
TASK Id : 4 Class : VPU,HRT
ThreadContext : TEXT Cost : 5
Constraint : Precede : 6
InputBuffer : 3 OutputBuffer : 5
TASK Id : 5 Class : VPU,HRT
ThreadContext : PROG Cost : 20
Constraint : Precede : 6
InputBuffer : 4 OutputBuffer : 6
TASK Id : 6 Class : VPU,HRT
ThreadContext : BLEND Cost : 10
Constraint : Precede : 5
InputBuffer : 5,6 OutputBuffer :

FIG. 48

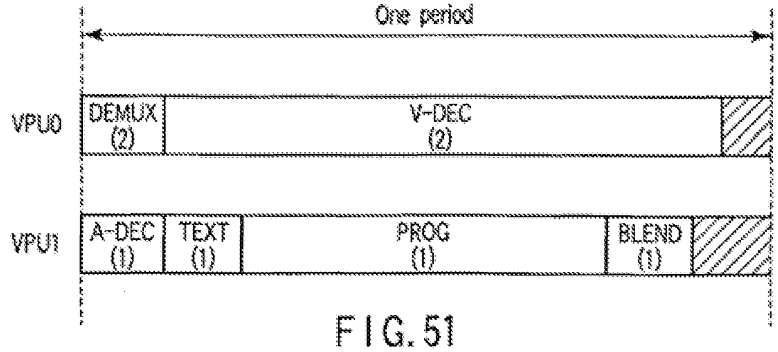


FIG. 51

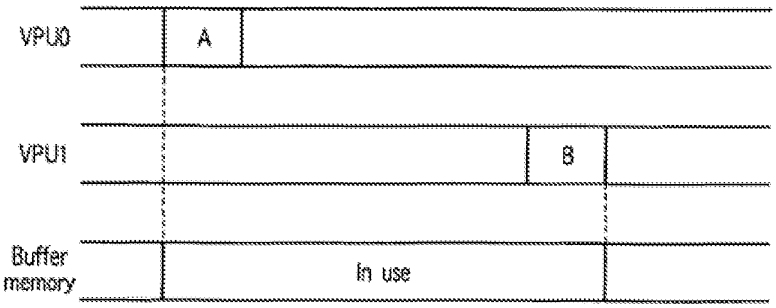


FIG. 54

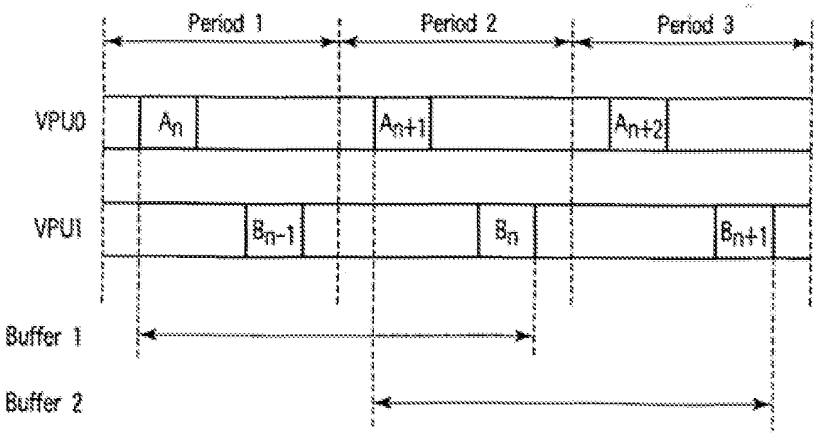


FIG. 55

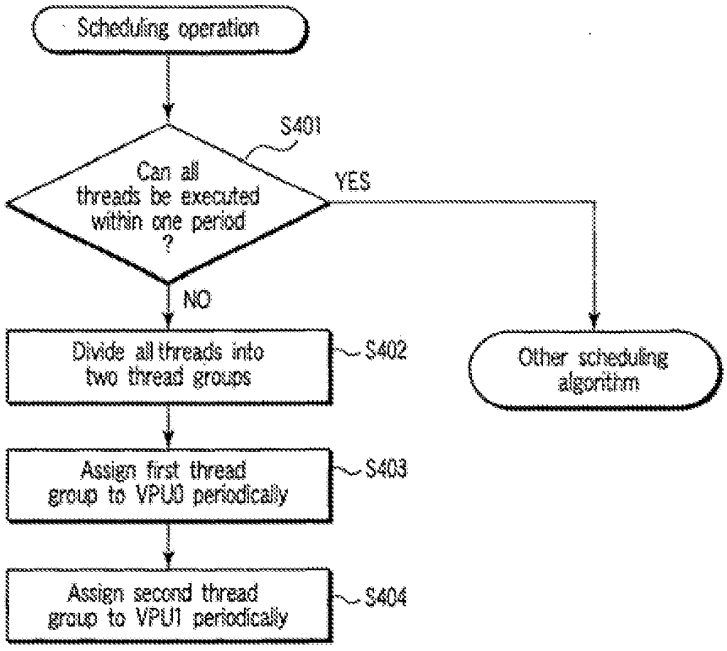

Scheduling operation
S401
Can all threads be executed within one period ?
YES
NO
Divide all threads into two thread groups
S402
Other scheduling algorithm
Assign first thread group to VPU0 periodically
S403
Assign second thread group to VPU1 periodically
S404

FIG. 52

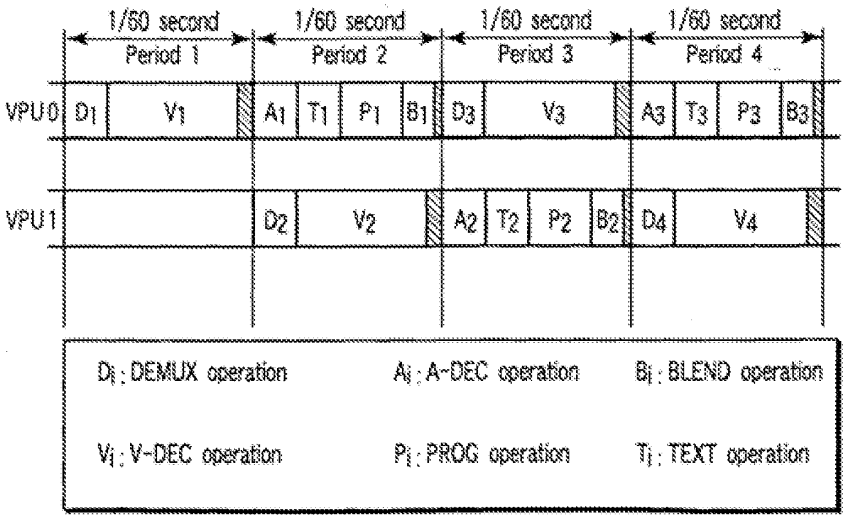

1/60 second
Period 1
1/60 second
Period 2
1/60 second
Period 3
1/60 second
Period 4
VPU 0
D1 V1 A1 T1 P1 B1 D3 V3 A3 T3 P3 B3
VPU 1
D2 V2 A2 T2 P2 B2 D4 V4
Di : DEMUX operation
Ai : A-DEC operation
Bi : BLEND operation
Vi : V-DEC operation
Pi : PROG operation
Ti : TEXT operation

FIG. 53

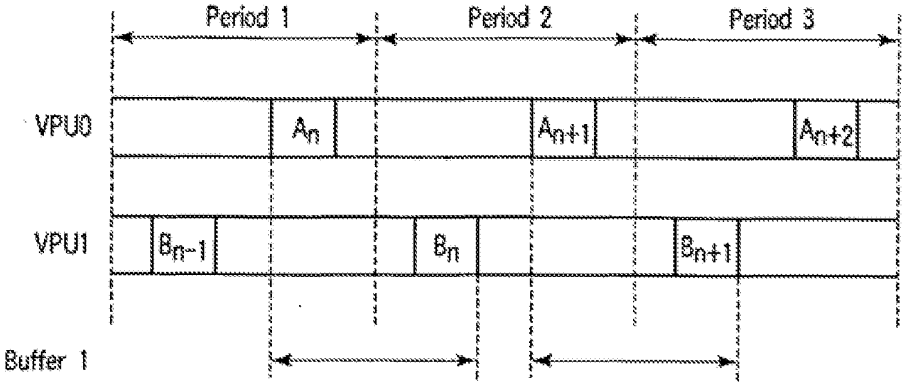

Period 1
Period 2
Period 3
VPU0
An
An+1
An+2
VPU1
Bn-1
Bn
Bn+1
Buffer 1

FIG. 56

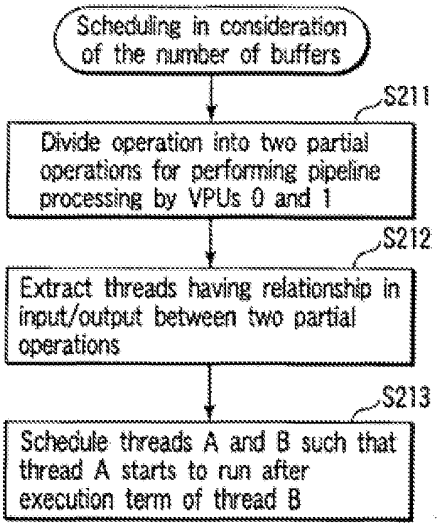

Scheduling in consideration of the number of buffers
S211
Divide operation into two partial operations for performing pipeline processing by VPUs 0 and 1
S212
Extract threads having relationship in input/output between two partial operations
S213
Schedule threads A and B such that thread A starts to run after execution term of thread B

FIG. 57

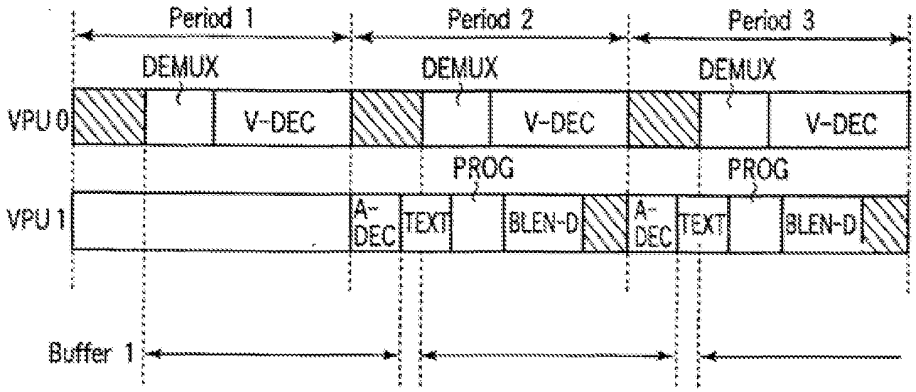

Period 1
Period 2
Period 3
DEMUX
DEMUX
DEMUX
VPU 0
V-DEC
V-DEC
V-DEC
PROG
PROG
VPU 1
A-DEC
TEXT
BLEN-D
A-DEC
TEXT
BLEN-D
Buffer 1

FIG. 58

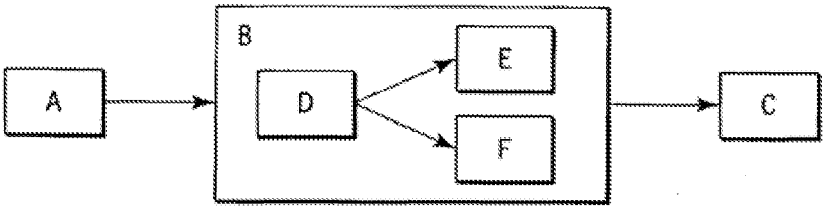

A
B
D
E
F
C

FIG. 59

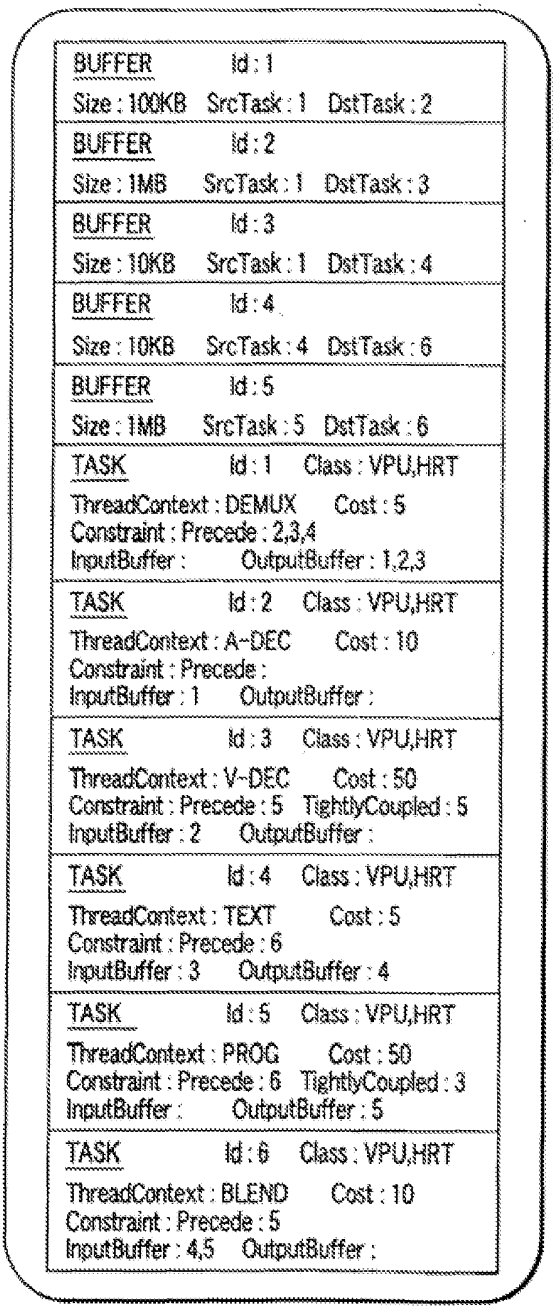

BUFFER Id : 1
Size : 100KB SrcTask : 1 DstTask : 2
BUFFER Id : 2
Size : 1MB SrcTask : 1 DstTask : 3
BUFFER Id : 3
Size : 10KB SrcTask : 1 DstTask : 4
BUFFER Id : 4
Size : 10KB SrcTask : 4 DstTask : 6
BUFFER Id : 5
Size : 1MB SrcTask : 5 DstTask : 6
TASK Id : 1 Class : VPU,HRT
ThreadContext : DEMUX Cost : 5
Constraint : Precede : 2,3,4
InputBuffer : OutputBuffer : 1,2,3
TASK Id : 2 Class : VPU,HRT
ThreadContext : A-DEC Cost : 10
Constraint : Precede :
InputBuffer : 1 OutputBuffer :
TASK Id : 3 Class : VPU,HRT
ThreadContext : V-DEC Cost : 50
Constraint : Precede : 5 TightlyCoupled : 5
InputBuffer : 2 OutputBuffer :
TASK Id : 4 Class : VPU,HRT
ThreadContext : TEXT Cost : 5
Constraint : Precede : 6
InputBuffer : 3 OutputBuffer : 4
TASK Id : 5 Class : VPU,HRT
ThreadContext : PROG Cost : 50
Constraint : Precede : 6 TightlyCoupled : 3
InputBuffer : OutputBuffer : 5
TASK Id : 6 Class : VPU,HRT
ThreadContext : BLEND Cost : 10
Constraint : Precede : 5
InputBuffer : 4,5 OutputBuffer :

FIG. 60

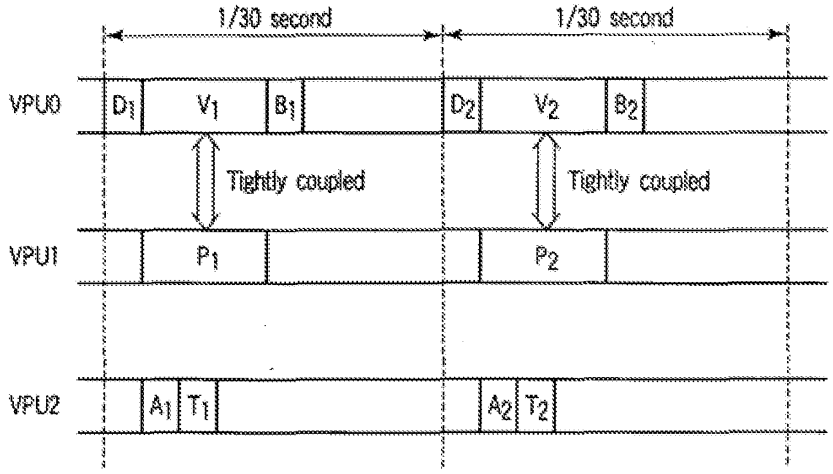

1/30 second
1/30 second
VPU0
D1
V1
B1
D2
V2
B2
Tightly coupled
Tightly coupled
VPU1
P1
P2
VPU2
A1
T1
A2
T2

FIG. 61

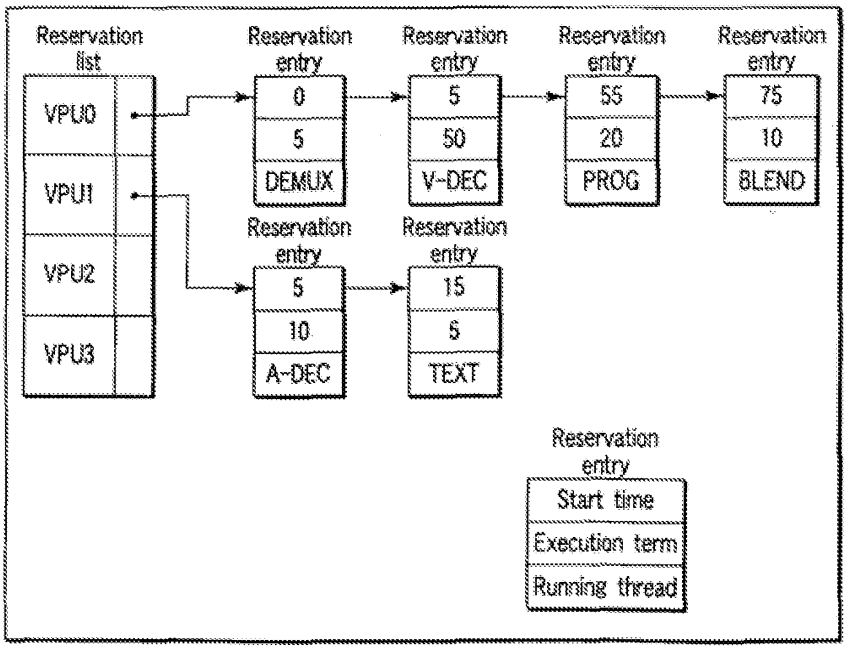

Reservation list
VPU0
VPU1
VPU2
VPU3
Reservation entry
0
5
DEMUX
Reservation entry
5
50
V-DEC
Reservation entry
55
20
PROG
Reservation entry
75
10
BLEND
Reservation entry
5
10
A-DEC
Reservation entry
15
5
TEXT
Reservation entry
Start time
Execution term
Running thread

FIG. 62

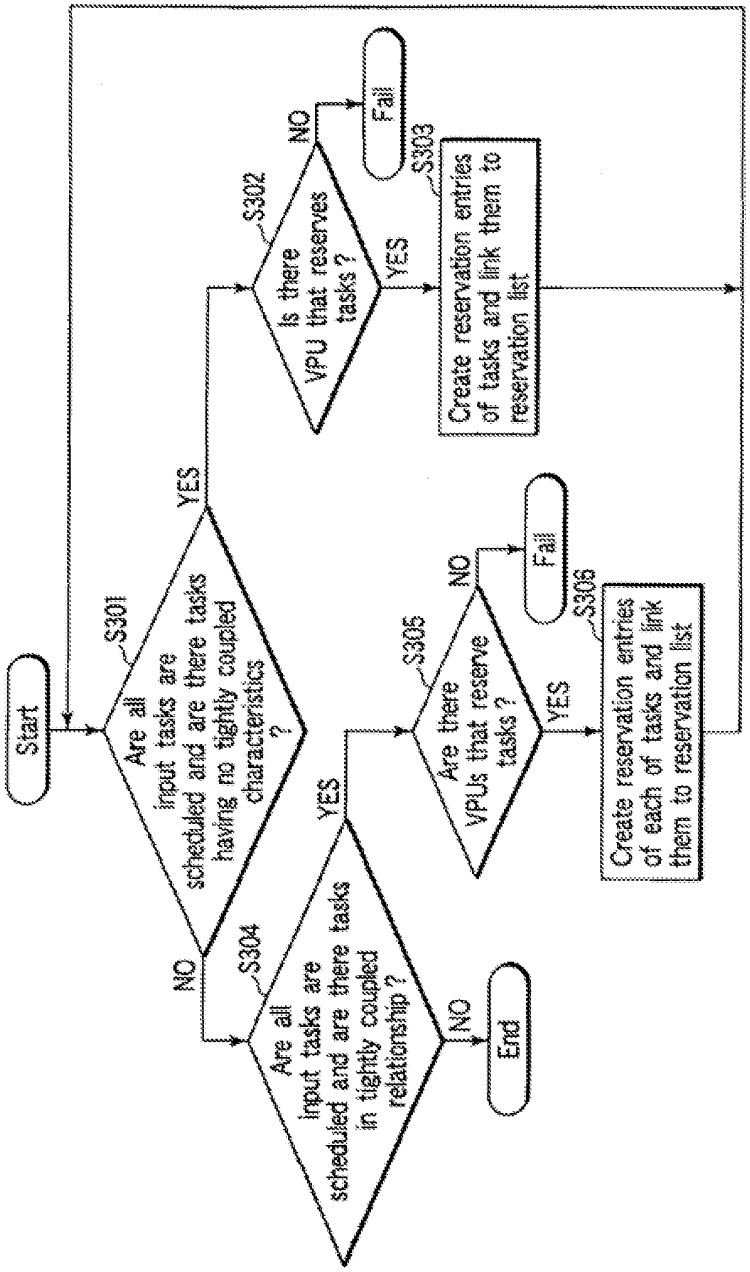

Start
S301
Are all input tasks are scheduled and are there tasks having no tightly coupled characteristics ?
YES
NO
S302
Is there VPU that reserves tasks ?
NO
Fail
YES
S303
Create reservation entries of tasks and link them to reservation list
S304
Are all input tasks are scheduled and are there tasks in tightly coupled relationship ?
YES
NO
End
S305
Are there VPUs that reserve tasks ?
NO
Fail
YES
S306
Create reservation entries of each of tasks and link them to reservation list

FIG. 63

INFORMATION DISCLOSURE STATEMENT

First Inventor: Tannenbaum, Zvi	**Conf. No.:** 1893
App. No.: 17/374789	**Filed:** July 13, 2021
Examiner: Asres, Hermon	**Art Unit:** 2449
Title: CLUSTER COMPUTING	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

References and Listing

Pursuant to 37 CFR 1.56, an Information Disclosure Statement listing references is provided herewith.

Pursuant to 37 C.F.R § 1.97(g) and (h), Applicant makes no representation that the information is considered to be material to patentability. Additionally, inclusion on this list is not an admission that any of the cited documents are prior art in this application. Further, Applicant makes no representation that better art does not exist.

No Disclaimers

To the extent that anything in the Information Disclosure Statement or the listed references could be construed as a disclaimer of any subject matter supported by the present application, Applicant hereby rescinds and retracts such disclaimer.

Timing of Disclosure

This Information Disclosure Statement is being filed after the mailing date of a final action, Notice of Allowance, or other action that closes prosecution.

CERTIFICATION UNDER 37 CFR 1.97(e)(1)

I hereby certify that each item of information contained in this Statement was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three (3) months prior to the filing of this Information Disclosure Statement.

This Statement is accompanied by the fee set forth in 37 CFR 1.17(p). The Commissioner is authorized to charge any additional fees which may be required or to credit any overpayment to Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: November 7, 2022

By: /Jordan M. Cox/
Jordan M. Cox
Registration No. 70,875
Registered Practitioner
(949) 760-0404

56583324

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/374,789	07/13/2021	Zvi Tannenbaum	ZTANN.002P1C7	1893

20995 7590 09/16/2022

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
ASRES, HERMON	

ART UNIT	PAPER NUMBER
2449	

NOTIFICATION DATE	DELIVERY MODE
09/16/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

efiling@knobbe.com
jayna.cartee@knobbe.com

Response to Rule 312 Communication	Application No.	Applicant(s)	
	17/374,789	Tannenbaum et al.	
	Examiner	Art Unit	AIA (FITF) Status
	HERMON ASRES	2449	No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ The amendment filed on 06 September 2022 under 37 CFR 1.312 has been considered, and has been:
   - a) ☑ entered.
   - b) ☐ entered as directed to matters of form not affecting the scope of the invention.
   - c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
     Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.
   - d) ☐ disapproved. See explanation below.
   - e) ☐ entered in part. See explanation below.
   - f) ☐ not entered because the supplemental or corrected Application Data sheet (ADS)
     - ☐ was not accompanied by a petition to accept an unintentionally delayed claim under 37 CFR 1.55 or 27 CFR 1.78;
     - ☐ did not identify the information being changed in accordance with 37 CFR 1.76(c)(2);
     - ☐ was not properly signed in accordance with 37 CFR 1.76(e) (or 37 CFR 1.33(b) for applications filed prior to September 16, 2012).

/HERMON ASRES/
Primary Examiner, Art Unit 2449

OK TO ENTER: /H.A./

ZTANN.002P1C7 PATENT

AMENDMENT AFTER ALLOWANCE UNDER 37 C.F.R. § 1.312

First Inventor: Tannenbaum, Zvi	**Conf. No.:** 1893
App. No.: 17/374789	**Filed:** July 13, 2021
Examiner: Asres, Hermon	**Art Unit:** 2449
Title: CLUSTER COMPUTING	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

Applicant submits the following Amendment after the mailing of the Notice of Allowance dated August 31, 2022 in connection with the above-identified application.

Amendments to the Claims begin on page 2.

Remarks begin on page 11.

AMENDMENT AFTER ALLOWANCE UNDER 37 C.F.R. § 1.312

First Inventor: Tannenbaum, Zvi	**Conf. No.:** 1893
App. No.: 17/374789	**Filed:** July 13, 2021
Examiner: Asres, Hermon	**Art Unit:** 2449
Title: CLUSTER COMPUTING	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

Applicant submits the following Amendment after the mailing of the Notice of Allowance dated August 31, 2022 in connection with the above-identified application.

Amendments to the Claims begin on page 2.

Remarks begin on page 11.

AMENDMENTS TO THE CLAIMS

1. (Canceled)

2. (Previously Presented) A computer cluster comprising:

a plurality of nodes, wherein each of the plurality of nodes comprises a hardware processor, wherein one or more of the nodes are configured to receive a command to start a cluster initialization process for the computer cluster, and wherein each of the nodes is configured to access a non-transitory computer-readable medium comprising program code for a single-node kernel that, when executed, is capable of causing the hardware processor to evaluate mathematical expressions; and

a communications network interface for the nodes to communicate results of mathematical expression evaluation with each other using a peer-to-peer architecture;

wherein the plurality of nodes comprises:

a first node comprising a first hardware processor configured to access a first memory comprising program code for a user interface and program code for a first single-node kernel, the first single-node kernel configured to interpret user instructions and distribute calls to at least one of a plurality of other nodes for execution; and

a second node comprising a second hardware processor with a plurality of processing cores, wherein the second node is configured to receive calls from the first node, execute at least a first mathematical expression evaluation, and communicate a result of the first mathematical expression evaluation to a third node;

wherein the third node comprises a third hardware processor with a plurality of processing cores, wherein the third node is configured to receive the result of the first mathematical expression evaluation from the second node, execute at least a second mathematical expression evaluation using the received result, and communicate the result of the second mathematical expression evaluation to the first node;

wherein the first node is configured to return the result of the second mathematical expression evaluation to the user interface;

wherein one or more of the nodes are configured to:

accept user instructions;

after accepting user instructions, communicate at least some of the user instructions using the communications network interface for the nodes to communicate with each other; and

after communicating at least some of the user instructions using the communications network interface, communicate at least some of the user instructions to one or more single-node kernels.

3. (Previously Presented) The computer cluster of claim 2, wherein the communications network interface comprises at least one of: a local bus, a local area network (LAN), a wide area network (WAN), a storage area network (SAN), a TCP/IP interface over Ethernet, or a wireless network interface.

4. (Previously Presented) The computer cluster of claim 2, wherein each of the nodes comprises one or more cluster node modules.

5. (Previously Presented) The computer cluster of claim 2, wherein each single-node kernel is stored in a non-transitory computer-readable medium and configured to accept and execute a request.

6. (Previously Presented) The computer cluster of claim 5, wherein each of the nodes comprises one or more cluster node modules, wherein each of the cluster node modules comprises instructions stored in a non-transitory computer-readable medium, and wherein the instructions, when executed by the hardware processor, cause the cluster node module to communicate with the single-node kernel and with one or more other cluster node modules.

7. (Currently Amended) The computer cluster of claim 6, wherein the one or more ~~plurality of~~ cluster node modules act as a cluster.

8. (Currently Amended) The computer cluster of claim 6, wherein the one or more ~~plurality of~~ cluster node modules communicate with one another to act as a cluster.

9. (Previously Presented) The computer cluster of claim 2, wherein the computer cluster includes the user interface.

10. (Previously Presented) The computer cluster of claim 6, wherein each cluster node module accepts instructions from the user interface and interprets one or more of the instructions.

11. (Previously Presented) The computer cluster of claim 2, wherein the cluster initialization process comprises establishing communication among two or more of the nodes.

12. (Previously Presented) The computer cluster of claim 2, wherein the cluster initialization process comprises configuring access by one or more of the nodes to a computer-readable medium comprising program code for the single-node kernel.

13. (Previously Presented) The computer cluster of claim 12, wherein the cluster initialization process comprises establishing message-passing support among the nodes in the cluster.

14. (Previously Presented) The computer cluster of claim 12, wherein the cluster initialization process comprises launching cluster node modules by the cluster.

15. (Previously Presented) The computer cluster of claim 14, wherein the cluster initialization process comprises assigning a processor identification number to each of the cluster node modules.

16. (Previously Presented) The computer cluster of claim 2, wherein the cluster initialization process comprises:

launching cluster node modules by the cluster; and

after launching the cluster node modules, configuring access by one or more of the nodes to a non-transitory computer-readable medium comprising program code for the single-node kernel.

17. (Previously Presented) The computer cluster of claim 2, wherein the cluster initialization process comprises:

launching cluster node modules by the cluster;

after launching the cluster node modules, establishing communication among two or more of the nodes; and

after establishing communication among two or more of the nodes, assigning a processor identification number to each of the cluster node modules.

18. (Previously Presented) The computer cluster of claim 2, wherein one or more of the nodes are configured to communicate at least some of the user instructions.

19. (Previously Presented) The computer cluster of claim 18, wherein one or more of the nodes are configured to communicate at least some of the user instructions to one or more single-node kernels.

20. (Previously Presented) The computer cluster of claim 2, wherein one or more of the nodes are configured to accept user instructions via one or more of the nodes.

21. (Previously Presented) The computer cluster of claim 20, wherein one or more of the nodes are configured to communicate at least some of the user instructions using the communications network interface for the nodes to communicate with each other.

22. (Previously Presented) The computer cluster of claim 2, wherein one or more of the nodes are configured to transmit at least some of the user instructions that originate from a user interface.

23. (Previously Presented) The computer cluster of claim 2, wherein one or more of the nodes are configured to parallelize at least some of the user instructions before communicating at least some of the user instructions to one or more single-node kernels.

24. (Previously Presented) The computer cluster of claim 2, wherein one or more of the nodes are configured to:

accept user instructions;

after accepting user instructions, communicate at least some of the user instructions using the communications network interface for the nodes to communicate with each other; and

after communicating at least some of the user instructions using the communications network interface, communicate at least some of the user instructions to one or more single-node kernels.

25. (Previously Presented) The computer cluster of claim 2, wherein the plurality of nodes are configured to communicate with one another to interpret and translate commands for execution by a plurality of single-node kernels.

26. (Currently Amended) A computer cluster comprising:

a plurality of nodes, wherein one or more of the nodes are configured to receive:

a command to start a cluster initialization process for the computer cluster, wherein the cluster initialization process comprises establishing communication among two or more of the nodes; and

an instruction from a user interface or a script;

and

a communications network interface for the nodes to communicate results of mathematical expression evaluation with each other using asynchronous calls;

wherein each of the nodes is configured to access a non-transitory computer-readable medium comprising program code for a single-node kernel that, when executed, is capable of causing a hardware processor to evaluate mathematical expressions~~;~~

wherein the plurality of nodes comprises:

a first node comprising a first hardware processor configured to access a first memory comprising program code for a user interface and program code for a first single-node kernel, the first single-node kernel configured to interpret user instructions and distribute calls to at least one of a plurality of other nodes for execution; and

a second node comprising a second hardware processor with a plurality of processing cores, wherein the second node is configured to receive calls from the first node, execute at least a first mathematical expression evaluation, and communicate a result of mathematical expression evaluation to a third node;

wherein the third node comprises a third hardware processor with a plurality of processing cores, wherein the third node is configured to receive the result of mathematical expression evaluation from the second node, execute at least a second mathematical expression evaluation using the received result, and communicate the result of the second mathematical expression evaluation to the first node;

wherein the first node is configured to return the result of the second mathematical expression evaluation to the user interface or the script[[.]]~~;~~

wherein one or more of the nodes are configured to:

accept user instructions;

after accepting user instructions, communicate at least some of the user instructions using the communications network interface for the nodes to communicate with each other; and

after communicating at least some of the user instruction using the communications network interface, communicate at least some of the user instructions to one or more since-node kernels.

27. (Previously Presented) The computer cluster of claim 26, wherein the asynchronous calls comprise a first command to create a first packet containing:

an expression to be sent as payload; and

a target node where the expression should be sent;

wherein the first command is configured to be called from within a single-node kernel;

wherein the single-node kernel is configured to send the first packet to a local cluster node module; and

wherein the local cluster node module is configured to forward the expression to the target node.

28. (Previously Presented) The computer cluster of claim 26, wherein the communications network interface comprises at least one of: a local bus, a local area network (LAN), a wide area network (WAN), a storage area network (SAN), a TCP/IP interface over Ethernet, or a wireless network interface.

29. (Previously Presented) A computer cluster comprising:

a plurality of nodes, wherein one or more of the nodes are configured to receive:

a command to start a cluster initialization process for the computer cluster, wherein the cluster initialization process comprises establishing communication among two or more of the nodes; and

an instruction from a user interface or a script;

and

a communications network interface for the nodes to communicate results of mathematical expression evaluation with each other, wherein the communications network interface comprises at least one of: a local bus, a local area network (LAN), a wide area network (WAN), a storage area network (SAN), a TCP/IP interface over Ethernet, or a wireless network interface;

wherein each of the nodes is configured to access a non-transitory computer-readable medium comprising program code for a single-node kernel that, when executed, is capable of causing a hardware processor to evaluate mathematical expressions;

wherein the plurality of nodes comprises:

a first node comprising a first hardware processor configured to access a first memory comprising program code for a user interface and program code for a first single-node kernel, the first single-node kernel configured to interpret user instructions and distribute calls to at least one of a plurality of other nodes for execution; and

a second node comprising a second hardware processor with a plurality of processing cores, wherein the second node is configured to receive calls from the first node, execute at least a first mathematical expression evaluation, and communicate a result of mathematical expression evaluation to a third node;

wherein the third node comprises a third hardware processor with a plurality of processing cores, wherein the third node is configured to receive the result of mathematical expression evaluation from the second node, execute at least a second mathematical expression evaluation using the received result, and communicate the result of the second mathematical expression evaluation to the first node;

and

wherein the first node is configured to return the result of the second mathematical expression evaluation to the user interface or the script;

wherein one or more of the nodes are configured to:

accept user instructions;

after accepting user instructions, communicate at least some of the user instructions using the communications network interface for the nodes to communicate with each other; and

after communicating at least some of the user instructions using the communications network interface, communicate at least some of the user instructions to one or more single-node kernels.

30. (Previously Presented) The computer cluster of claim 29, wherein each of the single-node kernels are configured to call a send command involving creating a packet containing:

an expression to be sent as payload; and

where the expression should be sent;

wherein, upon reception of the send command by a local cluster node module associated with the single-node kernel, the local cluster node module is configured to decode the packet and forward a payload to the cluster node module specified in the packet;

wherein each of the single-node kernels is configured to call a receipt command involving creating a packet specifying which message to test for completion and to then wait for a reply expression to evaluate;

wherein, upon reception of the receipt command by the local cluster node module associated with the single-node kernel, the local cluster node module is configured to decode the packet and use a message specifier to search for any matching expressions listed as completed in a received message queue;

wherein, upon determining that such a completed expression is found, the local cluster node module is configured to send the completed expression to a local single-node kernel associated with the cluster node module in response to the receipt command, and

wherein each of the single-node kernels is configured to receive the completed expression and to update variables used by the single-node kernel during evaluation of expressions.

31. (Previously Presented) A computer cluster node for evaluating expressions in parallel with other computer cluster nodes, the computer cluster node comprising:

a hardware processor configured to access one or more non-transitory memory devices comprising program code for a single-node kernel that, when executed, causes the hardware processor to interpret user instructions, to evaluate mathematical expressions, and to produce results of mathematical expression evaluation, wherein the hardware processor comprises multiple processor cores;

a user connection interface configured to receive a command to start a cluster initialization process for a computer cluster;

a communications network interface to communicate results of evaluation with other computer cluster nodes using a peer-to-peer architecture, wherein the communications network interface comprises at least one of: a local bus, a local area network (LAN), a wide area network (WAN), a storage area network (SAN), a TCP/IP interface over Ethernet, or a wireless network interface; and

program code that, when executed, is capable of causing the hardware processor to:

receive calls from a second node comprising a second hardware processor configures to access a second memory comprising program code for a user interface and program code for a second single-node kernel, the second single-node kernel configured to interpret user instructions and distribute calls to at least one of a plurality of other nodes for execution;

execute, using the hardware processor, at least a first mathematical expression evaluation; and

communicate a result of the first mathematical expression evaluation to a third node comprising a third hardware processor with a plurality of processing cores, wherein the third node is configured to receive the result of mathematical expression evaluation from the computer cluster node, execute at least a second mathematical expression evaluation using the result of the first mathematical expression evaluation, and communicate a result of the second mathematical expression evaluation to the first node;

wherein the user connection interface is configured to return at least one result of mathematical expression evaluation to a user interface or a script; and

wherein the computer cluster node is configured to:

accept user instructions;

after accepting user instructions, communicate at least some of the user instructions using the communications network interface for the nodes to communicate with each other; and

after communicating at least some of the user instructions using the communications network interface, communicate at least some of the user instructions to the single-node kernel.

REMARKS

In response to the Notice of Allowance dated August 31, 2022, Applicant submits the following Amendment. Applicant has amended Claims 7, 8, and 26 to correct a couple of typos.

No Disclaimers or Disavowals

Applicant reserves the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: September 6, 2022

By: /Jordan M. Cox/
Jordan M. Cox
Registration No. 70,875
Registered Practitioner
(949) 760-0404

56229785

Electronic Acknowledgement Receipt	
EFS ID:	46556088
Application Number:	17374789
International Application Number:	
Confirmation Number:	1893
Title of Invention:	CLUSTER COMPUTING
First Named Inventor/Applicant Name:	Zvi Tannenbaum
Customer Number:	20995
Filer:	Jordan Michael Cox/Wendy Castorena
Filer Authorized By:	Jordan Michael Cox
Attorney Docket Number:	ZTANN.002P1C7
Receipt Date:	06-SEP-2022
Filing Date:	13-JUL-2021
Time Stamp:	18:23:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		ZTANN-002P1C7_Amend.pdf	60200 4515aa4af119dde655fbacc2a53687e645b4bf7a	yes	11

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment after Notice of Allowance (Rule 312)	1	1
	Claims	2	10
	Applicant Arguments/Remarks Made in an Amendment	11	11
Warnings:			
Information:			
	Total Files Size (in bytes):	60200	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

20995 7590 08/31/2022

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FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER
ASRES, HERMON

ART UNIT	PAPER NUMBER
2449	

DATE MAILED: 08/31/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/374,789	07/13/2021	Zvi Tannenbaum	ZTANN.002P1C7	1893

TITLE OF INVENTION: CLUSTER COMPUTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	11/30/2022

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

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Commissioner for Patents
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Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20995 7590 08/31/2022
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/374,789	07/13/2021	Zvi Tannenbaum	ZTANN.002P1C7	1893

TITLE OF INVENTION: CLUSTER COMPUTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	11/30/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
ASRES, HERMON	2449	709-223000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/374,789	07/13/2021	Zvi Tannenbaum	ZTANN.002P1C7	1893

20995 7590 08/31/2022

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
ASRES, HERMON	

ART UNIT	PAPER NUMBER
2449	

DATE MAILED: 08/31/2022

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/374,789	Applicant(s) Tannenbaum et al.	
	Examiner HERMON ASRES	Art Unit 2449	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 07/07/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 2-31 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☑ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HERMON ASRES/
Primary Examiner, Art Unit 2449

DETAILED ACTION

REASONS FOR ALLOWANCE

Claims 2-31 are allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance:

In interpreting the claims, in light of the specification the Examiner finds the claimed invention to be patentably distinct from the prior art of record.

Block et al. (2005/0021751) teaches an apparatus, program product and method utilize cluster data port services within a cluster infrastructure to provide reliable and efficient communications between nodes in a clustered computer system. The cluster data port services present an abstracted transport service that encapsulates and manages the establishment of multiple connection paths between a source node, a target node and one or more backup nodes in such a manner that a cluster data port is effectively utilized as single data port from the perspective of a user program. **(See Abstract).**

Fought et al. (6,074,427) teaches a system and method for simulating multiple clusters of independent computer nodes in a single machine. A cluster contains one or more computer nodes interconnected by a communications link. A user can simulate a cluster of n nodes by generating n user-level procedures where each user-level procedure represents the

kernel of a respective node. An additional mechanism is provided which allows a user to exercise the operation of any intended function in any of the nodes in any of the clusters. **(See Abstract).**

Singh (8,601,101) teaches a system and method for each node in a cluster including a peer-to-peer communication channel compiling and maintaining its own cluster membership are disclosed. In one embodiment, each cluster node may be coupled to every other node and commonly-accessible storage through a network. When a node starts up and attempts to join the cluster, it may access cluster information data stored in the commonly-accessible storage. This information may include a list of all nodes that are potential cluster members. Based on the cluster membership information, the joining node may request a peer-to-peer connection with each potential cluster member. When such a request results in establishment of a connection, the joining node may add the name of the target node to its cluster membership list. Likewise, when a member node grants a connection to a node, it may add the joining node to its cluster membership list. **(See Abstract).**

However, the prior art of records fail to teach or suggest individually or in combination as set forth in independent claims 2 filed on 08/04/2021. Claims 3-31 are also allowed for the same reasons.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submission should clearly labeled “Comments on statement of Reason for Allowance”.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HERMON ASRES whose telephone number is (571)272-4257. The examiner can normally be reached Monday to Friday 9AM to 5PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Vivek Srivastava can be reached on (571)272-7304. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HERMON ASRES/
Primary Examiner, Art Unit 2449

Notice of References Cited	Application/Control No. 17/374,789	Applicant(s)/Patent Under Reexamination Tannenbaum et al.	
	Examiner HERMON ASRES	Art Unit 2449	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20050021751-A1	01-2005	Block, Timothy Roy	H04L67/1017	714/E11.073
*	B	US-20070073705-A1	03-2007	Gray; Theodore W.	G06F9/451	1/1
*	C	US-8601101-B1	12-2013	Singh; Servesh Pratap	H04L69/40	370/254
*	D	US-6968359-B1	11-2005	Miller; Robert	G06F9/5061	709/205
*	E	US-20070094532-A1	04-2007	SENGUPTA; Sabyasachi	G06F11/3632	714/E11.207
*	F	US-20030195938-A1	10-2003	Howard, Kevin David	G06F15/163	709/208
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/374,789	Tannenbaum et al.
	Examiner	**Art Unit**
	HERMON ASRES	2449

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/20/2021	03/25/2022	08/25/2022						
	2	=	=	✓						
	3	=	=	✓						
	4	=	=	✓						
	5	=	=	✓						
	6	=	=	✓						
	7	=	=	✓						
	8	=	=	✓						
	9	=	=	✓						
	10	=	=	✓						
	11	=	=	✓						
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	23	=	=	✓						
	24	=	=	✓						
	25	=	=	✓						
	26	=	=	✓						
	27	=	=	✓						
	28	=	=	✓						
	29	=	=	✓						
	30	=	=	✓						
	31	=	=	✓						

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/374,789	Tannenbaum et al.
	Examiner	**Art Unit**
	HERMON ASRES	2449

CLAIM		DATE								
Final	Original	11/20/2021	03/25/2022	08/25/2022						

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/374,789	Tannenbaum et al.
	Examiner	Art Unit
	HERMON ASRES	2449

CPC - Searched*		
Symbol	Date	Examiner

CPC Combination Sets - Searched*		
Symbol	Date	Examiner
H04L41/0213, H04L29/08072, H04L29/06, H04L41/22, H04L41/12	11/20/2021	HA
H04L41/0213, H04L29/08072, H04L29/06, H04L41/22, H04L41/12	03/25/2022	HA
H04L41/0213, H04L29/08072, H04L29/06, H04L41/22, H04L41/12	08/25/2022	HA

US Classification - Searched*			
Class	Subclass	Date	Examiner
709	223	11/20/2021	HA

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Searched East (US Patents, USPGPubs, EPO, JPO, Derwent, IBM)	11/20/2021	HA
See East search attached	11/20/2021	HA
Inventor search performed	11/20/2021	HA
Key word search performed in NPL (ip.com and google scholar)	11/20/2021	HA
Interference search performed	11/20/2021	HA
IPR2020-01608ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo8,082,289	11/20/2021	HA
IPR2021-00019ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo.10,333,768	11/20/2021	HA

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/374,789	Tannenbaum et al.
	Examiner	Art Unit
	HERMON ASRES	2449

IPR2021-00020ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo.10,333,768	11/20/2021	HA
IPR2021-00075ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo8,140,612	11/20/2021	HA
IPR2021-00108ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo8,676,877	11/20/2021	HA
Search updated	03/25/2022	HA
Key word search performed in NPL (ip.com and google scholar)	03/25/2022	HA
IPR2020-01608ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo8,082,289	03/25/2022	HA
IPR2021-00019ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo.10,333,768	03/25/2022	HA
IPR2021-00020ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo.10,333,768	03/25/2022	HA
IPR2021-00075ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo8,140,612	03/25/2022	HA
IPR2021-00108ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo8,676,877	03/25/2022	HA

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
709	223	11/20/2021	HA
709	223	08/25/2022	HA

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/374,789	Tannenbaum et al.
	Examiner	**Art Unit**
	HERMON ASRES	2449

CPC							
Symbol						**Type**	**Version**
H04L	/	41	/	04		F	2013-01-01
G06F	/	9	/	5072		I	2013-01-01
G06F	/	9	/	54		I	2013-01-01
G06F	/	15	/	76		I	2013-01-01

CPC Combination Sets								
Symbol						**Type**	**Set**	**Ranking**	**Version**
	/		/						

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	30	
/HERMON ASRES/ Primary Examiner, Art Unit 2449	25 August 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No.: 20220825

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/374,789	Tannenbaum et al.
	Examiner	Art Unit
	HERMON ASRES	2449

INTERNATIONAL CLASSIFICATION					
CLAIMED					
H04L12/24	/	12	/	24	
G06F9/50	/	9	/	50	
G06F9/54	/	9	/	54	
G06F15/76	/	15	/	76	

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
709	223

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE (Assistant Examiner)	(Date)	Total Claims Allowed: 30	
/HERMON ASRES/ Primary Examiner, Art Unit 2449 (Primary Examiner)	25 August 2022 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

U.S. Patent and Trademark Office

Part of Paper No.: 20220825

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/374,789	Tannenbaum et al.
	Examiner	Art Unit
	HERMON ASRES	2449

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	2	10	11	19	20	28	29								
2	3	11	12	20	21	29	30								
3	4	12	13	21	22	30	31								
4	5	13	14	22	23										
5	6	14	15	23	24										
6	7	15	16	24	25										
7	8	16	17	25	26										
8	9	17	18	26	27										
9	10	18	19	27	28										

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	30	
/HERMON ASRES/ Primary Examiner, Art Unit 2449	25 August 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office Part of Paper No.: 20220825

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	6	((Zvi) near2 (Tannenbaum)).INV.	(USPAT)	OR	OFF	OFF	2015/07/24 08:25 PM
L2	7	((Dean) near2 (Dauger)).INV.	(USPAT)	OR	OFF	OFF	2015/07/24 08:25 PM
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L126	196	(US-0005068-$ | US-0005266-$ | US-0015460-$ | US-0021751-$ | US-0026601-$ | US-0038852-$ | US-0044099-$ | US-0049859-$ | US-0051062-$ | US-0053216-$ | US-0059473-$ | US-0060237-$ | US-0073705-$ | US-0076105-$ | US-0094532-$ | US-0097300-$ | US-0098447-$ | US-0106931-$ | US-0108394-$ | US-0110209-$ | US-0124363-$ | US-0135621-$ | US-0154789-$ | US-0157203-$ | US-0180095-$ | US-0188088-$ | US-0195572-$ | US-0195931-$ | US-0195938-$ | US-0250347-$ | US-0252710-$ | US-0254984-$ | US-0281997-$ | US-1234567-$ | US-10333768-$ | US-1368948-$ | US-17207443-$ | US-20020049859-$ | US-20030005068-$ | US-20030005266-$ | US-20030051062-$ | US-20030135621-$ | US-20030195931-$ | US-20030195938-$ | US-20040098447-$ | US-20040110209-$ | US-20040157203-$ | US-20040195572-$ | US-20040252710-$ | US-20040254984-$ | US-20050015460-$ | US-	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2020/12/30 01:03 PM

		20050021751-$ | US- 20050038852-$ | US- 20050060237-$ | US- 20050076105-$ | US- 20050097300-$ | US- 20050108394-$ | US- 20050154789-$ | US- 20050180095-$ | US- 20050188088-$ | US- 20060026601-$ | US- 20060053216-$ | US- 20060059473-$ | US- 20060106931-$ | US- 20070044099-$ | US- 20070073705-$ | US- 20070094532-$ | US- 20070124363-$ | US- 20080250347-$ | US- 20080281997-$ | US- 31357476-$ | US- 5423046-$ | US- 5881315-$ | US- 5930768-$ | US- 6006259-$ | US- 6067609-$ | US- 6108699-$ | US- 6195680-$ | US- 6202080-$ | US- 6546403-$ | US- 6578068-$ | US- 6604134-$ | US- 6751698-$ | US- 6782537-$ | US- 6968335-$ | US- 6968359-$ | US- 7031944-$ | US- 7093004-$ | US- 7136924-$ | US- 7139882-$ | US- 7174381-$ | US- 7177874-$ | US- 7249357-$ | US- 7315877-$ | US- 7334232-$ | US- 7437460-$ | US- 7472193-$ | US- 7502915-$ | US- 7519652-$ | US- 7533141-$ | US- 7533389-$ | US- 7554949-$ | US- 7568131-$ | US- 7644130-$ | US- 7698390-$ | US- 7716323-$ | US- 7757236-$ | US- 7788314-$ | US- 7835022-$ | US-					

		7937455-$ | US-8082289-$ | US-8117288-$ | US-8140612-$ | US-8402080-$ | US-8402083-$ | US-8601101-$ | US-8676877-$ | US-8849889-$ | US-9405564-$).DID.					
L127	2	("8676877").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2021/01/01 03:35 PM
L128	7	community near5 managed near5 RAN	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2021/01/01 11:00 PM
L129	33851	709/223.ccls.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2021/11/20 08:40 AM
L130	214	(US-0005068-$ | US-0005266-$ | US-0015460-$ | US-0015968-$ | US-0021751-$ | US-0026601-$ | US-0038852-$ | US-0044099-$ | US-0049859-$ | US-0051062-$ | US-0053216-$ | US-0059473-$ | US-0060237-$ | US-0073705-$ | US-0076105-$ | US-0094532-$ | US-0097300-$ | US-0098359-$ | US-0098447-$ | US-0106931-$ | US-0108394-$ | US-0110209-$ | US-0124363-$ | US-0135621-$ | US-0153677-$ | US-0154789-$ | US-0157203-$ | US-0180095-$ | US-0188088-$ | US-0195572-$ | US-0195931-$ | US-0195938-$ | US-0235055-$ | US-0250347-$ | US-0252710-$ | US-0254984-$ | US-0281997-$ | US-1234567-$ | US-	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2021/11/20 08:44 AM

		10333768-$ | US- 17207443-$ | US- 20020049859-$ | US- 20030005068-$ | US- 20030005266-$ | US- 20030051062-$ | US- 20030135621-$ | US- 20030195931-$ | US- 20030195938-$ | US- 20040015968-$ | US- 20040098359-$ | US- 20040098447-$ | US- 20040110209-$ | US- 20040157203-$ | US- 20040195572-$ | US- 20040252710-$ | US- 20040254984-$ | US- 20050015460-$ | US- 20050021751-$ | US- 20050038852-$ | US- 20050060237-$ | US- 20050076105-$ | US- 20050097300-$ | US- 20050108394-$ | US- 20050154789-$ | US- 20050180095-$ | US- 20050188088-$ | US- 20050235055-$ | US- 20060026601-$ | US- 20060053216-$ | US- 20060059473-$ | US- 20060106931-$ | US- 20070044099-$ | US- 20070073705-$ | US- 20070094532-$ | US- 20070124363-$ | US- 20080250347-$ | US- 20080281997-$ | US- 20200153677-$ | US- 5423046-$ | US- 5881315-$ | US- 5930768-$ | US- 53865456-$ | US- 6006259-$ | US- 6067609-$ | US- 6074427-$ | US- 6108699-$ | US- 6195680-$ | US- 6202080-$ | US- 6546403-$ | US- 6578068-$ | US- 6604134-$ | US- 6691216-$ | US- 6751698-$ | US- 6782537-$ | US- 6968335-$ | US- 6968359-$ | US- 7031944-$ | US-					

		7093004-$ | US-7136924-$ | US-7139882-$ | US-7174381-$ | US-7177874-$ | US-7249357-$ | US-7315877-$ | US-7334232-$ | US-7437460-$ | US-7472193-$ | US-7502915-$ | US-7519652-$ | US-7533141-$ | US-7533168-$ | US-7533389-$ | US-7554949-$ | US-7568131-$ | US-7634530-$ | US-7644130-$ | US-7698390-$ | US-7716323-$ | US-7757236-$ | US-7788314-$ | US-7835022-$ | US-7937455-$ | US-8082289-$ | US-8117288-$ | US-8140612-$ | US-8402080-$ | US-8402083-$ | US-8601101-$ | US-8676877-$ | US-8849889-$ | US-9405564-$).DID.					
L131	8	((Zvi) near2 (Tannenbaum)).INV.	(USPAT)	OR	OFF	OFF	2022/03/25 12:54 PM
L132	9	((Dean) near2 (Dauger)).INV.	(USPAT)	OR	OFF	OFF	2022/03/25 12:54 PM
L133	236	(computer with cluster) same nodes same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L134	35	L3 and interpret	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L135	39589	709/223.ccls.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L136	10778	H04L41/0213.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L137	3095	H04L29/08072.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L138	52733	H04L29/06.cpc.	(US-PGPUB; USPAT; EPO; JPO;	OR	OFF	OFF	2022/03/25 12:54 PM

			DERWENT; IBM_TDB)				
L139	21038	H04L41/22.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L140	30044	H04L41/12.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L141	0	L3 and L6	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L142	0	L3 and L7	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L143	15	L3 and L8	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L144	0	L3 and L9	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L145	2	L3 and L10	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L146	109	("20020049859"|"20030005266"|"20030051062"|"20030135621"|"20030195931"|"20030195938"|"20040110209"|"20040157203"|"20040252710"|"20050021751"|"20050038852"|"20050060237"|"20050076105"|"20050108394"|"20050180095"|"20060053216"|"20060106931"|"20070044099"|"20070073705"|"20080250347"|"20080281997"|"5423046"|"5881315"|"5930768"|"6108699"|"6202080"|"6546403"|"6578068"|"6751698"|"6782537"|"6968335"|"7093004"|"7136924"|"7174381"|"7249357"|"7334232"|"7437460"|"7472193"|"7554949"|"7937455"|"8082289"|"8140612"|"8402083"|"8676877").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L147	236	(computer with cluster) same nodes same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L148	16	(computer with cluster) same nodes same kernel and mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM

L149	236	(computer with cluster) same nodes same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L150	11	("8402080").PN.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L151	2	("8849889").PN.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L152	92	US-1234567-$.DID. OR US-5423046-$.DID. OR US-5881315-$.DID. OR US-5930768-$.DID. OR US-6108699-$.DID. OR US-6202080-$.DID. OR US-6546403-$.DID. OR US-6578068-$.DID. OR US-6751698-$.DID. OR US-6782537-$.DID. OR US-6968335-$.DID. OR US-7093004-$.DID. OR US-7136924-$.DID. OR US-7174381-$.DID. OR US-7249357-$.DID. OR US-7334232-$.DID. OR US-7437460-$.DID. OR US-7472193-$.DID. OR US-7554949-$.DID. OR US-7937455-$.DID. OR US-8082289-$.DID. OR US-8140612-$.DID. OR US-8402083-$.DID. OR US-8676877-$.DID. OR US-20020049859-$.DID. OR US-20030005266-$.DID. OR US-20030051062-$.DID. OR US-20030135621-$.DID. OR US-20030195931-$.DID. OR US-20030195938-$.DID. OR US-20040110209-$.DID. OR US-20040157203-$.DID. OR US-20040252710-$.DID. OR US-20050021751-$.DID. OR US-20050038852-$.DID. OR US-20050060237-$.DID. OR US-20050076105-$.DID. OR US-20050108394-$.DID. OR US-20050180095-$.DID. OR US-20060053216-$.DID.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM

		OR US-20060106931-$.DID. OR US-20070044099-$.DID. OR US-20070073705-$.DID. OR US-20080250347-$.DID. OR US-20080281997-$.DID. OR JP-1234567-$.DID. OR JP-0887473-$.DID. OR JP-2002117010-$.DID. OR US-6131999-$.DID.					
L153	6	(computer with cluster) same (nodes) same (single-node with kernel)	(USPAT)	OR	OFF	OFF	2022/03/25 12:54 PM
L154	18	(computer with cluster) same (nodes) same (single-node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L155	18	(computer with cluster) same (nodes) and (single-node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L156	18	(computer with cluster) and (nodes) and (single-node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L157	581	(computer with cluster) and (nodes) and (single with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L158	284	(computer with cluster) same (nodes) and (single with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L159	6	(computer with cluster) same (nodes) and (single with kernel) and 709/223.ccls.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L160	22	(computer with cluster) same (single with node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L161	273	(computer with cluster) and (single with node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L162	2	("8676877").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L163	2	("8676877").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L164	3909	(computer with cluster) and kernel and nodes and request	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L165	686	L34 and mathematical	(US-PGPUB; USPAT;	OR	OFF	OFF	2022/03/25

			EPO; JPO; DERWENT; IBM_TDB)				12:54 PM
L166	350836	L34 and mathematical smae kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L167	52	L34 and mathematical same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L168	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L169	50	(single with node with kernel) same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L170	50	(mathematical with kernel) same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L171	50	(mathematical with kernel) same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L172	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L173	354123	mathematica kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L174	19	mathematica near5 kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L175	23	mathematica with kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L176	11	("8402080").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L177	2	("8849889").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L178	109	("20020049859"|"20030005266"|"20030051062"|"20030135621"|"20030195931"|"20030195938"|"20040110209"|"20040157203"|"20040252710"|"20050021751"|"20050038852"|"20050060237"|"20050076105"|"20050108394"|"20050180095"|"20060053216"|"20060106931"|"20070044099"|"20070073705"|"20080250347"|"20080281997"|"5423046"|"5881315"|"5930768"|"610	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM

		8699"|"6202080"|"6546403"|"6578068"|"6751698"|"6782537"|"6968335"|"7093004"|"7136924"|"7174381"|"7249357"|"7334232"|"7437460"|"7472193"|"7554949"|"7937455"|"8082289"|"8140612"|"8402083"|"8676877").PN.				
L179	26	mathematica with cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L180	68	mathematica same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L181	804620	stephen wolfram mathematica kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L182	103	(stephen near2 wolfram).in.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L183	13	L52 and mathematica and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L184	404	mathematica and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L185	165	L54 and cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L186	23	mathematica with kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L187	0	("gridMathematica").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L188	0	("gridwithMathematica").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L189	26	grid with Mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L190	26	gridMathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L191	20	gridMathematica and wolfram	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L192	26	gridMathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L193	4031	Mathematica	(US-PGPUB; USPAT;	OR	OFF	OFF	2022/03/25

			EPO; JPO; DERWENT; IBM_TDB)				12:54 PM
L194	404	Mathematica and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L195	20445	wolfram	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L196	9640	wolfram.in.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L197	34	L66 and mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L198	91	L66 and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L199	2	("20070073705").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L200	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L201	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L202	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L203	0	("(computerwithnodeswithclister)same(peer-to-peer)and@ad<20060101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L204	0	(computer with nodes with clister) same (peer-to-peer) and @ad<"20060101"	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L205	3	(computer with nodes with cluster) same (peer-to-peer) and @ad<"20060101"	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L206	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L207	13	("8601101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L208	109	(computer with cluster) and kernel and (mathematical with expression)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L209	2	(computer with clusters) same kernel same	(US-PGPUB; USPAT; EPO; JPO;	OR	OFF	OFF	2022/03/25 12:54 PM

		mathematical	DERWENT; IBM_TDB)				
L210	104	(computer with clusters) and kernel same mathematical	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L211	14	(computer with clusters) same kernel same mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L212	130	(computer with clusters) same mathematical	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L213	5	(computer with clusters) same mathematical same expressions	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L214	1	cluster near5 mathematical near5 evaluate	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L215	6	cluster with mathematical with evaluate	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L216	2	("20050038852").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L217	22	("20050021751"|"20070073705"|"20070094532"|"6968359"|"8601101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L218	70	(US-0005068-$ | US-0015460-$ | US-0026601-$ | US-0059473-$ | US-0097300-$ | US-0098447-$ | US-0124363-$ | US-0154789-$ | US-0188088-$ | US-0254984-$ | US-1234567-$ | US-1368948-$ | US-20030005068-$ | US-20040098447-$ | US-20040254984-$ | US-20050015460-$ | US-20050026601-$ | US-20050097300-$ | US-20050154789-$ | US-20050188088-$ | US-20060059473-$ | US-20070124363-$ | US-25376674-$ | US-5195580-$ | US-6006259-$ | US-6067609-$ | US-6604134-$ | US-7031944-$ | US-7177874-$ | US-	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM

		7315877-$ | US-7502915-$ | US-7519652-$ | US-7533141-$ | US-7533389-$ | US-7568131-$ | US-7598390-$ | US-7644130-$ | US-7757236-$ | US-7788314-$ | US-7835022-$ | US-8117288-$ | US-9405564-$).DID.					
L219	7961	(computer with cluster with nodes)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L220	42	(computer with cluster with nodes) same (mathematica$)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L221	18	(computer with cluster with nodes) same (mathematica$) and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L222	767	(computer with cluster) same (mathematica$)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L223	48	(computer with cluster) same (mathematica$) and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L224	767	(computer with cluster) same (mathematica$)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L225	30	(computer with cluster) same (mathematica$) same result$3	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L226	17	(computer with cluster) same (mathematica$ with expression)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L227	20	(high with performance) same cluster same (mathematics mathematica)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L228	193	(high with performance) same cluster and (mathematics mathematica)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L229	2	("7418470").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L230	2	("20030195938").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L231	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO;	OR	ON	ON	2022/03/25 12:54 PM

			DERWENT; IBM_TDB)				
L232	13	("8601101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L233	2	("20030195938").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L234	2	("20030195938").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L235	2	("2003195938").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L236	6	("2004015968").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L237	5	("2004098359").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L238	6	("2004098447").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L239	2	("7139882").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L240	3	("20050021751").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L241	2	("20050235055").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L242	196	(US-0005068-$ | US-0005266-$ | US-0015460-$ | US-0021751-$ | US-0026601-$ | US-0038852-$ | US-0044099-$ | US-0049859-$ | US-0051062-$ | US-0053216-$ | US-0059473-$ | US-0060237-$ | US-0073705-$ | US-0076105-$ | US-0094532-$ | US-0097300-$ | US-0098447-$ | US-0106931-$ | US-0108394-$ | US-0110209-$ | US-0124363-$ | US-0135621-$ | US-0154789-$ | US-	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM

		0157203-$ | US- 0180095-$ | US- 0188088-$ | US- 0195572-$ | US- 0195931-$ | US- 0195938-$ | US- 0250347-$ | US- 0252710-$ | US- 0254984-$ | US- 0281997-$ | US- 1234567-$ | US- 10333768-$ | US- 1368948-$ | US- 17207443-$ | US- 20020049859-$ | US- 20030005068-$ | US- 20030005266-$ | US- 20030051062-$ | US- 20030135621-$ | US- 20030195931-$ | US- 20030195938-$ | US- 20040098447-$ | US- 20040110209-$ | US- 20040157203-$ | US- 20040195572-$ | US- 20040252710-$ | US- 20040254984-$ | US- 20050015460-$ | US- 20050021751-$ | US- 20050038852-$ | US- 20050060237-$ | US- 20050076105-$ | US- 20050097300-$ | US- 20050108394-$ | US- 20050154789-$ | US- 20050180095-$ | US- 20050188088-$ | US- 20060026601-$ | US- 20060053216-$ | US- 20060059473-$ | US- 20060106931-$ | US- 20070044099-$ | US- 20070073705-$ | US- 20070094532-$ | US- 20070124363-$ | US- 20080250347-$ | US- 20080281997-$ | US- 31357476-$ | US- 5423046-$ | US- 5881315-$ | US- 5930768-$ | US- 6006259-$ | US- 6067609-$ | US- 6108699-$ | US- 6195680-$ | US- 6202080-$ | US- 6546403-$ | US- 6578068-$ | US-					

		6604134-$ | US- 6751698-$ | US- 6782537-$ | US- 6968335-$ | US- 6968359-$ | US- 7031944-$ | US- 7093004-$ | US- 7136924-$ | US- 7139882-$ | US- 7174381-$ | US- 7177874-$ | US- 7249357-$ | US- 7315877-$ | US- 7334232-$ | US- 7437460-$ | US- 7472193-$ | US- 7502915-$ | US- 7519652-$ | US- 7533141-$ | US- 7533389-$ | US- 7554949-$ | US- 7568131-$ | US- 7644130-$ | US- 7698390-$ | US- 7716323-$ | US- 7757236-$ | US- 7788314-$ | US- 7835022-$ | US- 7937455-$ | US- 8082289-$ | US- 8117288-$ | US- 8140612-$ | US- 8402080-$ | US- 8402083-$ | US- 8601101-$ | US- 8676877-$ | US- 8849889-$ | US- 9405564-$).DID.					
L243	2	("8676877").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L244	15	community near5 managed near5 RAN	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L245	39589	709/223.ccls.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L246	214	(US-0005068-$ | US- 0005266-$ | US- 0015460-$ | US- 0015968-$ | US- 0021751-$ | US- 0026601-$ | US- 0038852-$ | US- 0044099-$ | US- 0049859-$ | US- 0051062-$ | US-	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM

		0053216-$ | US- 0059473-$ | US- 0060237-$ | US- 0073705-$ | US- 0076105-$ | US- 0094532-$ | US- 0097300-$ | US- 0098359-$ | US- 0098447-$ | US- 0106931-$ | US- 0108394-$ | US- 0110209-$ | US- 0124363-$ | US- 0135621-$ | US- 0153677-$ | US- 0154789-$ | US- 0157203-$ | US- 0180095-$ | US- 0188088-$ | US- 0195572-$ | US- 0195931-$ | US- 0195938-$ | US- 0235055-$ | US- 0250347-$ | US- 0252710-$ | US- 0254984-$ | US- 0281997-$ | US- 1234567-$ | US- 10333768-$ | US- 17207443-$ | US- 20020049859-$ | US- 20030005068-$ | US- 20030005266-$ | US- 20030051062-$ | US- 20030135621-$ | US- 20030195931-$ | US- 20030195938-$ | US- 20040015968-$ | US- 20040098359-$ | US- 20040098447-$ | US- 20040110209-$ | US- 20040157203-$ | US- 20040195572-$ | US- 20040252710-$ | US- 20040254984-$ | US- 20050015460-$ | US- 20050021751-$ | US- 20050038852-$ | US- 20050060237-$ | US- 20050076105-$ | US- 20050097300-$ | US- 20050108394-$ | US- 20050154789-$ | US- 20050180095-$ | US- 20050188088-$ | US- 20050235055-$ | US- 20060026601-$ | US- 20060053216-$ | US-					

		20060059473-$ | US- 20060106931-$ | US- 20070044099-$ | US- 20070073705-$ | US- 20070094532-$ | US- 20070124363-$ | US- 20080250347-$ | US- 20080281997-$ | US- 20200153677-$ | US- 5423046-$ | US- 5881315-$ | US- 5930768-$ | US- 53865456-$ | US- 6006259-$ | US- 6067609-$ | US- 6074427-$ | US- 6108699-$ | US- 6195680-$ | US- 6202080-$ | US- 6546403-$ | US- 6578068-$ | US- 6604134-$ | US- 6691216-$ | US- 6751698-$ | US- 6782537-$ | US- 6968335-$ | US- 6968359-$ | US- 7031944-$ | US- 7093004-$ | US- 7136924-$ | US- 7139882-$ | US- 7174381-$ | US- 7177874-$ | US- 7249357-$ | US- 7315877-$ | US- 7334232-$ | US- 7437460-$ | US- 7472193-$ | US- 7502915-$ | US- 7519652-$ | US- 7533141-$ | US- 7533168-$ | US- 7533389-$ | US- 7554949-$ | US- 7568131-$ | US- 7634530-$ | US- 7644130-$ | US- 7698390-$ | US- 7716323-$ | US- 7757236-$ | US- 7788314-$ | US- 7835022-$ | US- 7937455-$ | US- 8082289-$ | US- 8117288-$ | US- 8140612-$ | US- 8402080-$ | US- 8402083-$ | US-					

		8601101-$ | US-8676877-$ | US-8849889-$ | US-9405564-$).DID.					
L247	22	"7542981"	(US-PGPUB; USPAT; USOCR; FIT (CN, FR, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:55 PM
L248	10	"7627744"	(US-PGPUB; USPAT; USOCR; FIT (CN, FR, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:55 PM
L249	2	"20050251644"	(US-PGPUB; USPAT; USOCR; FIT (CN, FR, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:55 PM
L250	8	((Zvi) near2 (Tannenbaum)).INV.	(USPAT)	OR	OFF	OFF	2022/08/25 12:33 PM
L251	9	((Dean) near2 (Dauger)).INV.	(USPAT)	OR	OFF	OFF	2022/08/25 12:33 PM
L252	238	(computer with cluster) same nodes same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L253	35	L3 and interpret	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L254	39594	709/223.ccls.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L255	10974	H04L41/0213.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L256	1126	H04L29/08072.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L257	23995	H04L29/06.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L258	21775	H04L41/22.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L259	31135	H04L41/12.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L260	0	L3 and L6	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L261	0	L3 and L7	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

L262	0	L3 and L8	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L263	0	L3 and L9	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L264	2	L3 and L10	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L265	110	("20020049859"|"20030005266"|"20030051062"|"20030135621"|"20030195931"|"20030195938"|"20040110209"|"20040157203"|"20040252710"|"20050021751"|"20050038852"|"20050060237"|"20050076105"|"20050108394"|"20050180095"|"20060053216"|"20060106931"|"20070044099"|"20070073705"|"20080250347"|"20080281997"|"5423046"|"5881315"|"5930768"|"6108699"|"6202080"|"6546403"|"6578068"|"6751698"|"6782537"|"6968335"|"7093004"|"7136924"|"7174381"|"7249357"|"7334232"|"7437460"|"7472193"|"7554949"|"7937455"|"8082289"|"8140612"|"8402083"|"8676877").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L266	238	(computer with cluster) same nodes same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L267	16	(computer with cluster) same nodes same kernel and mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L268	238	(computer with cluster) same nodes same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L269	11	("8402080").PN.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L270	2	("8849889").PN.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L271	92	US-1234567-$.DID. OR US-5423046-$.DID. OR US-5881315-$.DID. OR US-5930768-$.DID. OR US-6108699-$.DID. OR	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

		US-6202080-$.DID. OR US-6546403-$.DID. OR US-6578068-$.DID. OR US-6751698-$.DID. OR US-6782537-$.DID. OR US-6968335-$.DID. OR US-7093004-$.DID. OR US-7136924-$.DID. OR US-7174381-$.DID. OR US-7249357-$.DID. OR US-7334232-$.DID. OR US-7437460-$.DID. OR US-7472193-$.DID. OR US-7554949-$.DID. OR US-7937455-$.DID. OR US-8082289-$.DID. OR US-8140612-$.DID. OR US-8402083-$.DID. OR US-8676877-$.DID. OR US-20020049859-$.DID. OR US-20030005266-$.DID. OR US-20030051062-$.DID. OR US-20030135621-$.DID. OR US-20030195931-$.DID. OR US-20030195938-$.DID. OR US-20040110209-$.DID. OR US-20040157203-$.DID. OR US-20040252710-$.DID. OR US-20050021751-$.DID. OR US-20050038852-$.DID. OR US-20050060237-$.DID. OR US-20050076105-$.DID. OR US-20050108394-$.DID. OR US-20050180095-$.DID. OR US-20060053216-$.DID. OR US-20060106931-$.DID. OR US-20070044099-$.DID. OR US-20070073705-$.DID. OR US-20080250347-$.DID. OR US-20080281997-$.DID. OR JP-1234567-$.DID. OR JP-0887473-$.DID. OR JP-2002117010-$.DID. OR US-6131999-$.DID.					
L272	6	(computer with cluster) same (nodes) same (single-node with	(USPAT)	OR	OFF	OFF	2022/08/25 12:33 PM

		kernel)					
L273	18	(computer with cluster) same (nodes) same (single-node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L274	18	(computer with cluster) same (nodes) and (single-node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L275	18	(computer with cluster) and (nodes) and (single-node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L276	697	(computer with cluster) and (nodes) and (single with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L277	288	(computer with cluster) same (nodes) and (single with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L278	6	(computer with cluster) same (nodes) and (single with kernel) and 709/223.ccls.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L279	22	(computer with cluster) same (single with node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L280	374	(computer with cluster) and (single with node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L281	2	("8676877").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L282	2	("8676877").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L283	4425	(computer with cluster) and kernel and nodes and request	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L284	754	L34 and mathematical	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L285	366345	L34 and mathematical smae kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L286	54	L34 and mathematical same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L287	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L288	51	(single with node with kernel) same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

L289	53	(mathematical with kernel) same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L290	53	(mathematical with kernel) same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L291	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L292	369735	mathematica kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L293	19	mathematica near5 kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L294	24	mathematica with kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L295	11	("8402080").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L296	2	("8849889").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L297	110	("20020049859"|"20030005266"|"20030051062"|"20030135621"|"20030195931"|"20030195938"|"20040110209"|"20040157203"|"20040252710"|"20050021751"|"20050038852"|"20050060237"|"20050076105"|"20050108394"|"20050180095"|"20060053216"|"20060106931"|"20070044099"|"20070073705"|"20080250347"|"20080281997"|"5423046"|"5881315"|"5930768"|"6108699"|"6202080"|"6546403"|"6578068"|"6751698"|"6782537"|"6968335"|"7093004"|"7136924"|"7174381"|"7249357"|"7334232"|"7437460"|"7472193"|"7554949"|"7937455"|"8082289"|"8140612"|"8402083"|"8676877").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L298	26	mathematica with cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L299	69	mathematica same cluster	(US-PGPUB; USPAT; EPO; JPO;	OR	OFF	OFF	2022/08/25 12:33 PM

			DERWENT; IBM_TDB)				
L300	826263	stephen wolfram mathematica kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L301	105	(stephen near2 wolfram).in.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L302	14	L52 and mathematica and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L303	418	mathematica and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L304	174	L54 and cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L305	24	mathematica with kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L306	0	("gridMathematica").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L307	0	("gridwithMathematica").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L308	26	grid with Mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L309	26	gridMathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L310	20	gridMathematica and wolfram	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L311	26	gridMathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L312	4149	Mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L313	418	Mathematica and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L314	20790	wolfram	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L315	9710	wolfram.in.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L316	35	L66 and mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

L317	93	L66 and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L318	2	("20070073705").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L319	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L320	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L321	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L322	0	("(computerwithnodeswithclister)same(peer-to-peer)and@ad<20060101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L323	0	(computer with nodes with clister) same (peer-to-peer) and @ad<"20060101"	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L324	3	(computer with nodes with cluster) same (peer-to-peer) and @ad<"20060101"	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L325	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L326	13	("8601101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L327	110	(computer with cluster) and kernel and (mathematical with expression)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L328	2	(computer with clusters) same kernel same mathematical	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L329	139	(computer with clusters) and kernel same mathematical	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L330	14	(computer with clusters) same kernel same mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L331	133	(computer with clusters) same mathematical	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L332	6	(computer with clusters) same mathematical same expressions	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L333	1	cluster near5	(US-PGPUB; USPAT;	OR	OFF	OFF	2022/08/25

		mathematical near5 evaluate	EPO; JPO; DERWENT; IBM_TDB)				12:33 PM
L334	7	cluster with mathematical with evaluate	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L335	2	("20050038852").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L336	22	("20050021751"|"20070073705"|"20070094532"|"6968359"|"8601101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L337	70	(US-0005068-$ | US-0015460-$ | US-0026601-$ | US-0059473-$ | US-0097300-$ | US-0098447-$ | US-0124363-$ | US-0154789-$ | US-0188088-$ | US-0254984-$ | US-1234567-$ | US-1368948-$ | US-20030005068-$ | US-20040098447-$ | US-20040254984-$ | US-20050015460-$ | US-20050026601-$ | US-20050097300-$ | US-20050154789-$ | US-20050188088-$ | US-20060059473-$ | US-20070124363-$ | US-25376674-$ | US-5195580-$ | US-6006259-$ | US-6067609-$ | US-6604134-$ | US-7031944-$ | US-7177874-$ | US-7315877-$ | US-7502915-$ | US-7519652-$ | US-7533141-$ | US-7533389-$ | US-7568131-$ | US-7598390-$ | US-7644130-$ | US-7757236-$ | US-7788314-$ | US-7835022-$ | US-8117288-$ | US-9405564-$).DID.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L338	8340	(computer with cluster with nodes)	(US-PGPUB; USPAT; EPO; JPO;	OR	OFF	OFF	2022/08/25 12:33 PM

			DERWENT; IBM_TDB)				
L339	42	(computer with cluster with nodes) same (mathematica$)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L340	18	(computer with cluster with nodes) same (mathematica$) and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L341	779	(computer with cluster) same (mathematica$)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L342	49	(computer with cluster) same (mathematica$) and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L343	779	(computer with cluster) same (mathematica$)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L344	31	(computer with cluster) same (mathematica$) same result$3	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L345	18	(computer with cluster) same (mathematica$ with expression)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L346	21	(high with performance) same cluster same (mathematics mathematica)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L347	199	(high with performance) same cluster and (mathematics mathematica)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L348	2	("7418470").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L349	2	("20030195938").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L350	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L351	13	("8601101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L352	2	("20030195938").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L353	2	("20030195938").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L354	2	("2003195938").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

L355	6	("2004015968").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L356	5	("2004098359").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L357	6	("2004098447").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L358	2	("7139882").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L359	3	("20050021751").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L360	2	("20050235055").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L361	196	(US-0005068-$ | US-0005266-$ | US-0015460-$ | US-0021751-$ | US-0026601-$ | US-0038852-$ | US-0044099-$ | US-0049859-$ | US-0051062-$ | US-0053216-$ | US-0059473-$ | US-0060237-$ | US-0073705-$ | US-0076105-$ | US-0094532-$ | US-0097300-$ | US-0098447-$ | US-0106931-$ | US-0108394-$ | US-0110209-$ | US-0124363-$ | US-0135621-$ | US-0154789-$ | US-0157203-$ | US-0180095-$ | US-0188088-$ | US-0195572-$ | US-0195931-$ | US-0195938-$ | US-0250347-$ | US-0252710-$ | US-0254984-$ | US-0281997-$ | US-1234567-$ | US-10333768-$ | US-1368948-$ | US-17207443-$ | US-20020049859-$ | US-	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

		20030005068-$ | US- 20030005266-$ | US- 20030051062-$ | US- 20030135621-$ | US- 20030195931-$ | US- 20030195938-$ | US- 20040098447-$ | US- 20040110209-$ | US- 20040157203-$ | US- 20040195572-$ | US- 20040252710-$ | US- 20040254984-$ | US- 20050015460-$ | US- 20050021751-$ | US- 20050038852-$ | US- 20050060237-$ | US- 20050076105-$ | US- 20050097300-$ | US- 20050108394-$ | US- 20050154789-$ | US- 20050180095-$ | US- 20050188088-$ | US- 20060026601-$ | US- 20060053216-$ | US- 20060059473-$ | US- 20060106931-$ | US- 20070044099-$ | US- 20070073705-$ | US- 20070094532-$ | US- 20070124363-$ | US- 20080250347-$ | US- 20080281997-$ | US- 31357476-$ | US- 5423046-$ | US- 5881315-$ | US- 5930768-$ | US- 6006259-$ | US- 6067609-$ | US- 6108699-$ | US- 6195680-$ | US- 6202080-$ | US- 6546403-$ | US- 6578068-$ | US- 6604134-$ | US- 6751698-$ | US- 6782537-$ | US- 6968335-$ | US- 6968359-$ | US- 7031944-$ | US- 7093004-$ | US- 7136924-$ | US- 7139882-$ | US- 7174381-$ | US- 7177874-$ | US- 7249357-$ | US- 7315877-$ | US- 7334232-$ | US- 7437460-$ | US-					

		7472193-$ | US- 7502915-$ | US- 7519652-$ | US- 7533141-$ | US- 7533389-$ | US- 7554949-$ | US- 7568131-$ | US- 7644130-$ | US- 7698390-$ | US- 7716323-$ | US- 7757236-$ | US- 7788314-$ | US- 7835022-$ | US- 7937455-$ | US- 8082289-$ | US- 8117288-$ | US- 8140612-$ | US- 8402080-$ | US- 8402083-$ | US- 8601101-$ | US- 8676877-$ | US- 8849889-$ | US- 9405564-$).DID.					
L362	2	("8676877").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L363	17	community near5 managed near5 RAN	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L364	39594	709/223.ccls.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L365	214	(US-0005068-$ | US- 0005266-$ | US- 0015460-$ | US- 0015968-$ | US- 0021751-$ | US- 0026601-$ | US- 0038852-$ | US- 0044099-$ | US- 0049859-$ | US- 0051062-$ | US- 0053216-$ | US- 0059473-$ | US- 0060237-$ | US- 0073705-$ | US- 0076105-$ | US- 0094532-$ | US- 0097300-$ | US- 0098359-$ | US- 0098447-$ | US- 0106931-$ | US- 0108394-$ | US- 0110209-$ | US- 0124363-$ | US- 0135621-$ | US- 0153677-$ | US-	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

		0154789-$ | US- 0157203-$ | US- 0180095-$ | US- 0188088-$ | US- 0195572-$ | US- 0195931-$ | US- 0195938-$ | US- 0235055-$ | US- 0250347-$ | US- 0252710-$ | US- 0254984-$ | US- 0281997-$ | US- 1234567-$ | US- 10333768-$ | US- 17207443-$ | US- 20020049859-$ | US- 20030005068-$ | US- 20030005266-$ | US- 20030051062-$ | US- 20030135621-$ | US- 20030195931-$ | US- 20030195938-$ | US- 20040015968-$ | US- 20040098359-$ | US- 20040098447-$ | US- 20040110209-$ | US- 20040157203-$ | US- 20040195572-$ | US- 20040252710-$ | US- 20040254984-$ | US- 20050015460-$ | US- 20050021751-$ | US- 20050038852-$ | US- 20050060237-$ | US- 20050076105-$ | US- 20050097300-$ | US- 20050108394-$ | US- 20050154789-$ | US- 20050180095-$ | US- 20050188088-$ | US- 20050235055-$ | US- 20060026601-$ | US- 20060053216-$ | US- 20060059473-$ | US- 20060106931-$ | US- 20070044099-$ | US- 20070073705-$ | US- 20070094532-$ | US- 20070124363-$ | US- 20080250347-$ | US- 20080281997-$ | US- 20200153677-$ | US- 5423046-$ | US- 5881315-$ | US- 5930768-$ | US- 53865456-$ | US- 6006259-$ | US- 6067609-$ | US-					

		6074427-$ | US-6108699-$ | US-6195680-$ | US-6202080-$ | US-6546403-$ | US-6578068-$ | US-6604134-$ | US-6691216-$ | US-6751698-$ | US-6782537-$ | US-6968335-$ | US-6968359-$ | US-7031944-$ | US-7093004-$ | US-7136924-$ | US-7139882-$ | US-7174381-$ | US-7177874-$ | US-7249357-$ | US-7315877-$ | US-7334232-$ | US-7437460-$ | US-7472193-$ | US-7502915-$ | US-7519652-$ | US-7533141-$ | US-7533168-$ | US-7533389-$ | US-7554949-$ | US-7568131-$ | US-7634530-$ | US-7644130-$ | US-7698390-$ | US-7716323-$ | US-7757236-$ | US-7788314-$ | US-7835022-$ | US-7937455-$ | US-8082289-$ | US-8117288-$ | US-8140612-$ | US-8402080-$ | US-8402083-$ | US-8601101-$ | US-8676877-$ | US-8849889-$ | US-9405564-$).DID.					
L366	8	((Zvi) near2 (Tannenbaum)).INV.	(USPAT)	OR	OFF	OFF	2022/08/25 12:33 PM
L367	9	((Dean) near2 (Dauger)).INV.	(USPAT)	OR	OFF	OFF	2022/08/25 12:33 PM
L368	238	(computer with cluster) same nodes same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L369	35	L3 and interpret	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

L370	39594	709/223.ccls.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L371	10974	H04L41/0213.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L372	1126	H04L29/08072.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L373	23995	H04L29/06.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L374	21775	H04L41/22.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L375	31135	H04L41/12.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L376	0	L3 and L6	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L377	0	L3 and L7	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L378	0	L3 and L8	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L379	0	L3 and L9	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L380	2	L3 and L10	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L381	110	("20020049859"|"20030005266"|"20030051062"|"20030135621"|"20030195931"|"20030195938"|"20040110209"|"20040157203"|"20040252710"|"20050021751"|"20050038852"|"20050060237"|"20050076105"|"20050108394"|"20050180095"|"20060053216"|"20060106931"|"20070044099"|"20070073705"|"20080250347"|"20080281997"|"5423046"|"5881315"|"5930768"|"6108699"|"6202080"|"6546403"|"6578068"|"6751698"|"6782537"|"6968335"|"7093004"|"7136924"|"7174381"|"7249357"|"	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

		7334232"|"7437460"|"7472193"|"7554949"|"7937455"|"8082289"|"8140612"|"8402083"|"8676877").PN.					
L382	238	(computer with cluster) same nodes same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L383	16	(computer with cluster) same nodes same kernel and mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L384	238	(computer with cluster) same nodes same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L385	11	("8402080").PN.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L386	2	("8849889").PN.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L387	92	US-1234567-$.DID. OR US-5423046-$.DID. OR US-5881315-$.DID. OR US-5930768-$.DID. OR US-6108699-$.DID. OR US-6202080-$.DID. OR US-6546403-$.DID. OR US-6578068-$.DID. OR US-6751698-$.DID. OR US-6782537-$.DID. OR US-6968335-$.DID. OR US-7093004-$.DID. OR US-7136924-$.DID. OR US-7174381-$.DID. OR US-7249357-$.DID. OR US-7334232-$.DID. OR US-7437460-$.DID. OR US-7472193-$.DID. OR US-7554949-$.DID. OR US-7937455-$.DID. OR US-8082289-$.DID. OR US-8140612-$.DID. OR US-8402083-$.DID. OR US-8676877-$.DID. OR US-20020049859-$.DID. OR US-20030005266-$.DID. OR US-20030051062-$.DID. OR US-20030135621-$.DID. OR US-20030195931-$.DID. OR US-20030195938-$.DID. OR US-20040110209-$.DID. OR US-20040157203-$.DID.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

		OR US-20040252710-$.DID. OR US-20050021751-$.DID. OR US-20050038852-$.DID. OR US-20050060237-$.DID. OR US-20050076105-$.DID. OR US-20050108394-$.DID. OR US-20050180095-$.DID. OR US-20060053216-$.DID. OR US-20060106931-$.DID. OR US-20070044099-$.DID. OR US-20070073705-$.DID. OR US-20080250347-$.DID. OR US-20080281997-$.DID. OR JP-1234567-$.DID. OR JP-0887473-$.DID. OR JP-2002117010-$.DID. OR US-6131999-$.DID.					
L388	6	(computer with cluster) same (nodes) same (single-node with kernel)	(USPAT)	OR	OFF	OFF	2022/08/25 12:33 PM
L389	18	(computer with cluster) same (nodes) same (single-node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L390	18	(computer with cluster) same (nodes) and (single-node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L391	18	(computer with cluster) and (nodes) and (single-node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L392	697	(computer with cluster) and (nodes) and (single with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L393	288	(computer with cluster) same (nodes) and (single with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L394	6	(computer with cluster) same (nodes) and (single with kernel) and 709/223.ccls.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L395	22	(computer with cluster) same (single with node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L396	374	(computer with cluster) and (single with node	(US-PGPUB; USPAT; EPO; JPO;	OR	OFF	OFF	2022/08/25 12:33 PM

		with kernel)	DERWENT; IBM_TDB)				
L397	2	("8676877").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L398	2	("8676877").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L399	4425	(computer with cluster) and kernel and nodes and request	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L400	754	L34 and mathematical	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L401	366345	L34 and mathematical smae kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L402	54	L34 and mathematical same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L403	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L404	51	(single with node with kernel) same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L405	53	(mathematical with kernel) same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L406	53	(mathematical with kernel) same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L407	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L408	369735	mathematica kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L409	19	mathematica near5 kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L410	24	mathematica with kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L411	11	("8402080").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L412	2	("8849889").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L413	110	("20020049859"|"20030005266"|"20030051062"|"20030135621"|"2003	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

		0195931"|"20030195938"|"20040110209"|"20040157203"|"20040252710"|"20050021751"|"20050038852"|"20050060237"|"20050076105"|"20050108394"|"20050180095"|"20060053216"|"20060106931"|"20070044099"|"20070073705"|"20080250347"|"20080281997"|"5423046"|"5881315"|"5930768"|"6108699"|"6202080"|"6546403"|"6578068"|"6751698"|"6782537"|"6968335"|"7093004"|"7136924"|"7174381"|"7249357"|"7334232"|"7437460"|"7472193"|"7554949"|"7937455"|"8082289"|"8140612"|"8402083"|"8676877").PN.				
L414	26	mathematica with cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L415	69	mathematica same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L416	826263	stephen wolfram mathematica kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L417	105	(stephen near2 wolfram).in.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L418	14	L52 and mathematica and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L419	418	mathematica and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L420	174	L54 and cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L421	24	mathematica with kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L422	0	("gridMathematica").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L423	0	("gridwithMathematica").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L424	26	grid with Mathematica	(US-PGPUB; USPAT;	OR	OFF	OFF	2022/08/25

			EPO; JPO; DERWENT; IBM_TDB)				12:33 PM
L425	26	gridMathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L426	20	gridMathematica and wolfram	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L427	26	gridMathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L428	4149	Mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L429	418	Mathematica and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L430	20790	wolfram	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L431	9710	wolfram.in.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L432	35	L66 and mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L433	93	L66 and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L434	2	("20070073705").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L435	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L436	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L437	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L438	0	("(computerwithnodeswithclister)same(peer-to-peer)and@ad<20060101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L439	0	(computer with nodes with clister) same (peer-to-peer) and @ad<"20060101"	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L440	3	(computer with nodes with cluster) same (peer-to-peer) and @ad<"20060101"	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

L441	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L442	13	("8601101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L443	110	(computer with cluster) and kernel and (mathematical with expression)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L444	2	(computer with clusters) same kernel same mathematical	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L445	139	(computer with clusters) and kernel same mathematical	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L446	14	(computer with clusters) same kernel same mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L447	133	(computer with clusters) same mathematical	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L448	6	(computer with clusters) same mathematical same expressions	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L449	1	cluster near5 mathematical near5 evaluate	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L450	7	cluster with mathematical with evaluate	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L451	2	("20050038852").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L452	22	("20050021751"|"20070073705"|"20070094532"|"6968359"|"8601101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L453	70	(US-0005068-$ | US-0015460-$ | US-0026601-$ | US-0059473-$ | US-0097300-$ | US-0098447-$ | US-0124363-$ | US-0154789-$ | US-0188088-$ | US-0254984-$ | US-1234567-$ | US-1368948-$ | US-20030005068-$ | US-20040098447-$ | US-20040254984-$ | US-20050015460-$ | US-	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

		20050026601-$ | US-20050097300-$ | US-20050154789-$ | US-20050188088-$ | US-20060059473-$ | US-20070124363-$ | US-25376674-$ | US-5195580-$ | US-6006259-$ | US-6067609-$ | US-6604134-$ | US-7031944-$ | US-7177874-$ | US-7315877-$ | US-7502915-$ | US-7519652-$ | US-7533141-$ | US-7533389-$ | US-7568131-$ | US-7598390-$ | US-7644130-$ | US-7757236-$ | US-7788314-$ | US-7835022-$ | US-8117288-$ | US-9405564-$).DID.					
L454	8340	(computer with cluster with nodes)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L455	42	(computer with cluster with nodes) same (mathematica$)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L456	18	(computer with cluster with nodes) same (mathematica$) and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L457	779	(computer with cluster) same (mathematica$)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L458	49	(computer with cluster) same (mathematica$) and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L459	779	(computer with cluster) same (mathematica$)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L460	31	(computer with cluster) same (mathematica$) same result$3	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L461	18	(computer with cluster) same (mathematica$ with expression)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L462	21	(high with performance) same cluster same (mathematics mathematica)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

L463	199	(high with performance) same cluster and (mathematics mathematica)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L464	2	("7418470").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L465	2	("20030195938").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L466	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L467	13	("8601101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L468	2	("20030195938").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L469	2	("20030195938").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/25 12:33 PM
L470	2	("2003195938").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L471	6	("2004015968").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L472	5	("2004098359").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L473	6	("2004098447").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L474	2	("7139882").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L475	3	("20050021751").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L476	2	("20050235055").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L477	196	(US-0005068-$ | US-0005266-$ | US-0015460-$ | US-0021751-$ | US-0026601-$ | US-0038852-$ | US-0044099-$ | US-0049859-$ | US-0051062-$ | US-0053216-$ | US-	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

		0059473-$ | US- 0060237-$ | US- 0073705-$ | US- 0076105-$ | US- 0094532-$ | US- 0097300-$ | US- 0098447-$ | US- 0106931-$ | US- 0108394-$ | US- 0110209-$ | US- 0124363-$ | US- 0135621-$ | US- 0154789-$ | US- 0157203-$ | US- 0180095-$ | US- 0188088-$ | US- 0195572-$ | US- 0195931-$ | US- 0195938-$ | US- 0250347-$ | US- 0252710-$ | US- 0254984-$ | US- 0281997-$ | US- 1234567-$ | US- 10333768-$ | US- 1368948-$ | US- 17207443-$ | US- 20020049859-$ | US- 20030005068-$ | US- 20030005266-$ | US- 20030051062-$ | US- 20030135621-$ | US- 20030195931-$ | US- 20030195938-$ | US- 20040098447-$ | US- 20040110209-$ | US- 20040157203-$ | US- 20040195572-$ | US- 20040252710-$ | US- 20040254984-$ | US- 20050015460-$ | US- 20050021751-$ | US- 20050038852-$ | US- 20050060237-$ | US- 20050076105-$ | US- 20050097300-$ | US- 20050108394-$ | US- 20050154789-$ | US- 20050180095-$ | US- 20050188088-$ | US- 20060026601-$ | US- 20060053216-$ | US- 20060059473-$ | US- 20060106931-$ | US- 20070044099-$ | US- 20070073705-$ | US- 20070094532-$ | US- 20070124363-$ | US-					

		20080250347-$ | US-20080281997-$ | US-31357476-$ | US-5423046-$ | US-5881315-$ | US-5930768-$ | US-6006259-$ | US-6067609-$ | US-6108699-$ | US-6195680-$ | US-6202080-$ | US-6546403-$ | US-6578068-$ | US-6604134-$ | US-6751698-$ | US-6782537-$ | US-6968335-$ | US-6968359-$ | US-7031944-$ | US-7093004-$ | US-7136924-$ | US-7139882-$ | US-7174381-$ | US-7177874-$ | US-7249357-$ | US-7315877-$ | US-7334232-$ | US-7437460-$ | US-7472193-$ | US-7502915-$ | US-7519652-$ | US-7533141-$ | US-7533389-$ | US-7554949-$ | US-7568131-$ | US-7644130-$ | US-7698390-$ | US-7716323-$ | US-7757236-$ | US-7788314-$ | US-7835022-$ | US-7937455-$ | US-8082289-$ | US-8117288-$ | US-8140612-$ | US-8402080-$ | US-8402083-$ | US-8601101-$ | US-8676877-$ | US-8849889-$ | US-9405564-$).DID.					
L478	2	("8676877").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
L479	17	community near5 managed near5 RAN	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM

L480	39594	709/223.ccls.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/08/25 12:33 PM
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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
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N111	26795	H04L29/06.cpc.	(US-PGPUB; USPAT)	OR	OFF	OFF	2018/11/22 12:28 PM
N112	8674	H04L41/22.cpc.	(US-PGPUB; USPAT)	OR	OFF	OFF	2018/11/22 12:28 PM
N113	11500	H04L41/12.cpc.	(US-PGPUB; USPAT)	OR	OFF	OFF	2018/11/22 12:28 PM
N114	0	((cluster with initialization) and (mathematical with expression) and (nodes with mathematical) and (single with node with kernel)).clm.	(US-PGPUB; USPAT)	OR	OFF	OFF	2018/11/22 12:30 PM
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PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	17/374789
	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
(Multiple sheets used when necessary)	Examiner	Asres, Hermon
SHEET 1 OF 11	Attorney Docket No.	ZTANN.002P1C7

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number *Number - Kind Code (if known)* Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	7,015,915	03-21-2006	Diard	
	2	7,162,590	01-09-2007	Pruvost et al.	
	3	7,275,123	09-25-2007	Duncan et al.	
	4	7,289,125	10-30-2007	Diard et al.	
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	6	7,562,174	07-14-2009	Danilak	
	7	7,663,633	02-16-2010	Diamond et al.	
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	15	8,941,668	01-27-2015	Diamond	

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NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
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Examiner Signature /HERMON ASRES/	Date Considered 08/25/2022

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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PTO/SB/08 Equivalent

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	Art Unit	2449
(Multiple sheets used when necessary)	Examiner	Asres, Hermon
SHEET 2 OF 11	Attorney Docket No.	ZTANN.002P1C7

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
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Examiner Signature /HERMON ASRES/	Date Considered 08/25/2022

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	Art Unit	2449
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SHEET 3 OF 11	Attorney Docket No.	ZTANN.002P1C7

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Examiner Signature /HERMON ASRES/	Date Considered 08/25/2022

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SHEET 4 OF 11	Attorney Docket No.	ZTANN.002P1C7

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	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
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SHEET 5 OF 11	Attorney Docket No.	ZTANN.002P1C7

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	120	DECISION Granting Institution of Inter Partes Review of U.S. Patent No. 8,082,289, in Case IPR2020-01608, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated May 5, 2021 in 78 pages. [NVIDIA-ACS-0223292]	
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	Art Unit	2449
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	125	Joint Motion to Terminate Under 35 U.S.C. § 317(a) of U.S. Patent No. 8,082,289, in Case IPR2020-01608, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed June 17, 2021 in 6 pages. [NVIDIA-ACS-0223385]	
	126	Joint Motion to Terminate Under 35 U.S.C. § 317(a) of U.S. Patent No. 8,140,612, in Case IPR2021-00075, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed June 17, 2021 in 6 pages. [NVIDIA-ACS-0231729]	
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	128	Notice of Filing Date Accorded to Petition and Time for Filing Patent Owner Preliminary Response of U.S. Patent No. 8,082,289, in Case IPR2020-01608, Patent No. 8,082,289, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as mailed November 10, 2020 in 5 pages. [NVIDIA-ACS-0222837]	
	129	Notice of Filing Date Accorded to Petition and Time for Filing Patent Owner Preliminary Response of U.S. Patent No.10,333,768, in Case IPR2021-00019, Patent No. 10,333,768, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as mailed November 10, 2020 in 5 pages. [NVIDIA-ACS-0224757]	
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	132	Notice of Filing Date Accorded to Petition and Time for Filing Patent Owner Preliminary Response of U.S. Patent No. 8,676,877, in Case IPR2021-00108, Patent No. 8,676,877, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as mailed November 17, 2020 in 6 pages. [NVIDIA-ACS-0232321]	
	133	Notice of Refund of U.S. Patent No. 8,082,289, Case IPR2020-01608, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as mailed June 30, 2021 in 2 pages. [NVIDIA-ACS-0223400]	
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	138	ORDER Conduct of the Proceeding, IPR2020-01608 (Patent 8,082,289), IPR2021-00019 (Patent 10,333,768), IPR2021-00020 (Patent 10,333,768), IPR2021-00075 (Patent 8,140,612), IPR2021-00108 (Patent 8,676,877)1, NVIDIA Corporation v. Advanced Cluster Systems, Inc., Paper 8 as dated March 10, 2021 in 4 pages. [NVIDIA-ACS-0223288]	
	139	ORDER Conduct of the Proceeding, IPR2020-01608 (Patent 8,082,289), IPR2021-00019 (Patent 10,333,768), IPR2021-00020 (Patent 10,333,768), IPR2021-00075 (Patent 8,140,612), IPR2021-00108 (Patent 8,676,877)1, NVIDIA Corporation v. Advanced Cluster Systems, Inc., Paper 6 as dated March 10, 2021 in 4 pages. [NVIDIA-ACS-0231608]	
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	154	Patent Owner's Consolidated Sur-Reply in Support of its Preliminary Responses, Per March 10, 2021 Order in Cases IPR2020-01608 (Patent 8,082,289), IPR2021-00019 (Patent 10,333,768), IPR2021-00020 (Patent 10,333,768), IPR2021-00075 (Patent 8,140,612), IPR2021-00108 (Patent 8,676,877), NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed March 26, 2021 in 13 pages. [NVIDIA-ACS-0231624]	
	155	Patent Owner's Updated Exhibit List in Case No. IPR2020-01608, U.S. Patent No. 8,082,289, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed June 17, 2021 in 5 pages. [NVIDIA-ACS-0223391]	

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	156	Patent Owner's Updated Exhibit List in Case No. IPR2021-00075, U.S. Patent No. 8,140,612, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed June 17, 2021 in 5 pages. [NVIDIA-ACS-0231735]	
	157	Patent Owner's Updated Exhibit List in Case No. IPR2021-00108, U.S. Patent No. 8,676,877, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed June 17, 2021 in 5 pages. [NVIDIA-ACS-0232892]	
	158	Petitioner's Objections to Evidence in Case No. IPR2020-01608, U.S. Patent No. 8,082,289, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed May 19, 2021 in 4 pages. [NVIDIA-ACS-0223378]	
	159	Petitioner's Objections to Evidence in Case No. IPR2021-00075, U.S. Patent No. 8,140,612, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed May 19, 2021 in 4 pages. [NVIDIA-ACS-0231722]	
	160	Petitioner's Objections to Evidence in Case No. IPR2021-00108, U.S. Patent No. 8,676,877, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed May 19, 2021 in 4 pages. [NVIDIA-ACS-0232871]	
	161	Patent Owner's Objections to Admissibility of Evidence Served with Petition for Inter Partes Review in Case No. IPR2020-01608, U.S. Patent No. 8,082,287, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed May 19, 2021 in 8 pages. [NVIDIA-ACS-0223370]	
	162	Patent Owner's Objections to Admissibility of Evidence Served with Petition for Inter Partes Review in Case No. IPR2021-00075, U.S. Patent No. 8,140,612, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed May 19, 2021 in 7 pages. [NVIDIA-ACS-0231715]	
	163	Patent Owner's Objections to Admissibility of Evidence Served with Petition for Inter Partes Review in Case No. IPR2021-00108, U.S. Patent No. 8,676,877, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed May 27, 2021 in 8 pages. [NVIDIA-ACS-0232875]	
	164	Petitioner's Power of Attorney in Case No. IPR2021-00075, U.S. Patent No. 8,140,612, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed October 16, 2020 in 2 pages. [NVIDIA-ACS-0231190]	
	165	Petitioner's Power of Attorney in Case No. IPR2021-00108, U.S. Patent No. 8,676,877, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed October 23, 2020 in 2 pages. [NVIDIA-ACS-0232315]	
	166	Petitioner's Reply to Patent Owner's Preliminary Response in IPR2020-01608 (Patent 8,082,289), IPR2021-00019 (Patent 10,333,768), IPR2021-00020 (Patent 10,333,768), IPR2021-00075 (Patent 8,140,612), IPR2021-00108 (Patent 8,676,877), NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated March 16, 2021 in 12 pages. [NVIDIA-ACS-0231612]	
	167	Petitioner's Request for Refund of Fees of U.S. Patent No. 10,333,768, Case IPR2021-00019, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated May 13, 2021 in 3 pages. [NVIDIA-ACS-0225209]	
	168	Petitioner's Request for Refund of Fees of U.S. Patent No. 10,333,768, Case IPR2021-00020, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated May 13, 2021 in 3 pages. [NVIDIA-ACS-0228604]	
	169	Petitioner's Request for Refund of Post-Institution Fees of U.S. Patent No. 8,082,289, Case IPR2020-01608, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated June 30, 2021 in 4 pages. [NVIDIA-ACS-0223402]	
	170	Petitioner's Request for Refund of Post-Institution Fees of U.S. Patent No. 8,140,612, Case IPR2021-00075, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated June 30, 2021 in 5 pages. [NVIDIA-ACS-0231740]	

Examiner Signature	/HERMON ASRES/	Date Considered	08/25/2022

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.A./

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	17/374789
	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
(Multiple sheets used when necessary)	Examiner	Asres, Hermon
SHEET 11 OF 11	Attorney Docket No.	ZTANN.002P1C7

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	171	Petitioner's Request for Refund of Post-Institution Fees of U.S. Patent No. 8,676,877, Case IPR2021-00108, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated June 30, 2021 in 5 pages. [NVIDIA-ACS-0232897]	
	172	Scheduling Order of U.S. Patent No. 8,082,289, Case IPR2020-01608 and U.S. Patent No. 8,140,612, Case IPR2021-00075, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated May 5, 2021 in 11 pages. [NVIDIA-ACS-0231704]	
	173	Scheduling Order of U.S. Patent No. 8,676,877, Case IPR2021-00108, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated May 13, 2021 in 11 pages. [NVIDIA-ACS-0232860]	
	174	Stipulated Partial Dismissal with Prejudice in Case 1:19-cv-02032-CFC-CJB, Advanced Cluster Systems, Inc v. NVIDIA Corporation, as filed June 14, 2021 in 3 pages. [NVIDIA-ACS-0223382, NVIDIA-ACS-0231726 & NVIDIA-ACS-0232883]	
	175	Termination Due to Settlement After Institution of Trial of U.S. Patent No. 8,082,289, Case IPR2020-01608, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated June 22, 2021 in 4 pages. [NVIDIA-ACS-0223396]	
	176	Termination Due to Settlement After Institution of Trial of U.S. Patent No. 8,676,877, Case IPR2021-00108, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated June 30, 2021 in 4 pages. [NVIDIA-ACS-0232902]	
	177	Ex. 2004 - Nexus Claim Chart - SEM - 289 Patent, pp. 20. [NVIDIA-ACS-0222970]	
	178	Ex. 2005 - Nexus Claim Chart - SET - 289 Patent, pp. 28. [NVIDIA-ACS-0222990]	
	179	Ex. 2006 - Dauger Declaration, February 10, 2021, pp. 29. [NVIDIA-ACS-0223018]	
	180	Exhibit 1002 - File History of USP 8,082,289 B2, pp. 190. [NVIDIA-ACS-0220502]	

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Examiner Signature /HERMON ASRES/	Date Considered 08/25/2022

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Bibliographic Data

Application No: 17/374,789

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /HERMON ASRES/ (Examiner's Signature) | (Initials)

Title: CLUSTER COMPUTING

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
07/13/2021	709	2449	ZTANN.002P1C7
RULE			

APPLICANTS

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Dean E. Dauger, Huntington Beach, CA, UNITED STATES

CONTINUING DATA

This application is a CON of 16449084 06/21/2019 PAT 11128519

16449084 is a CON of 14181112 02/14/2014 PAT 10333768

14181112 is a CON of 13423063 03/16/2012 PAT 8676877

13423063 is a CON of 12040519 02/29/2008 PAT 8140612

12040519 is a CIP of 11744461 05/04/2007 PAT 8082289

11744461 has PRO of 60850908 10/11/2006

11744461 has PRO of 60813738 06/13/2006

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

07/26/2021

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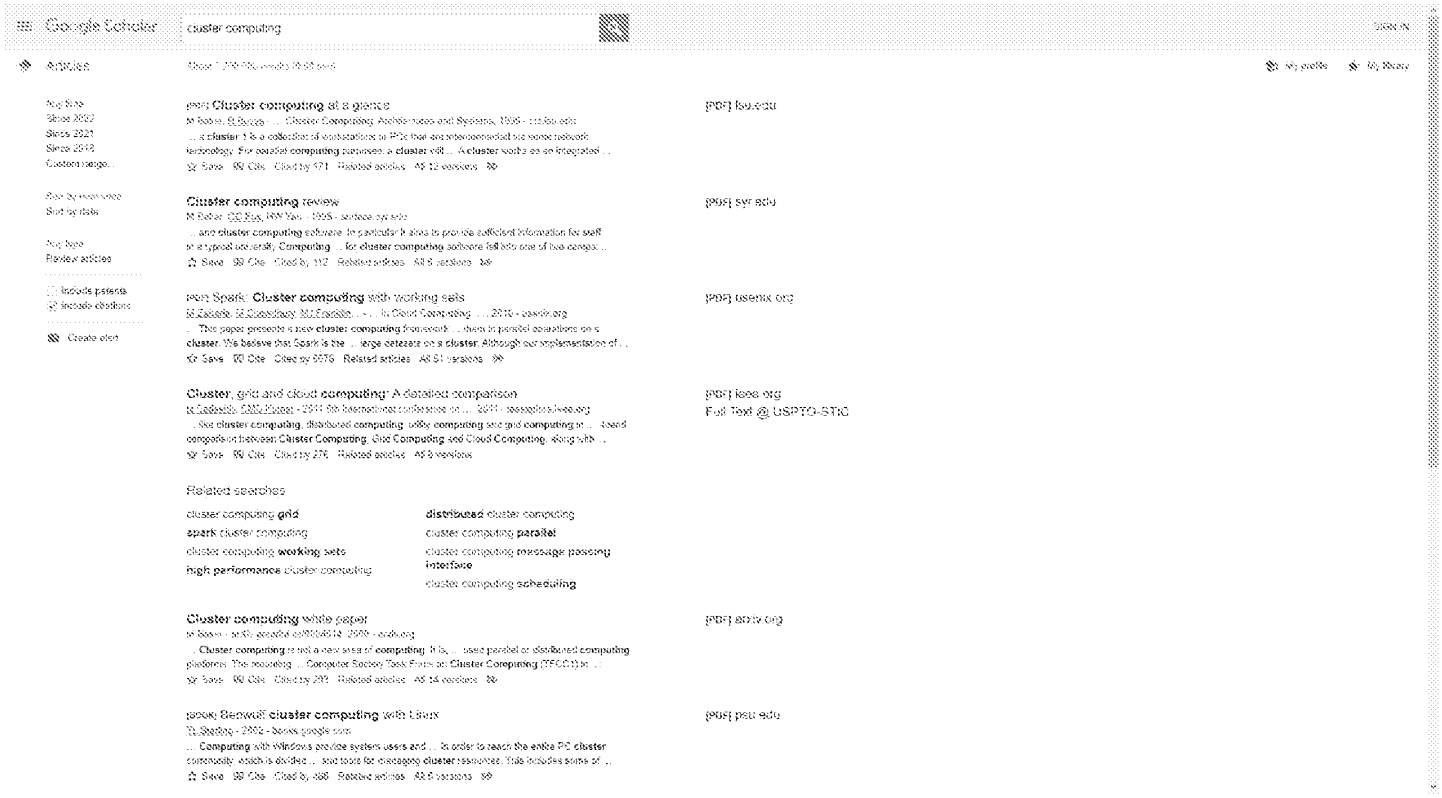
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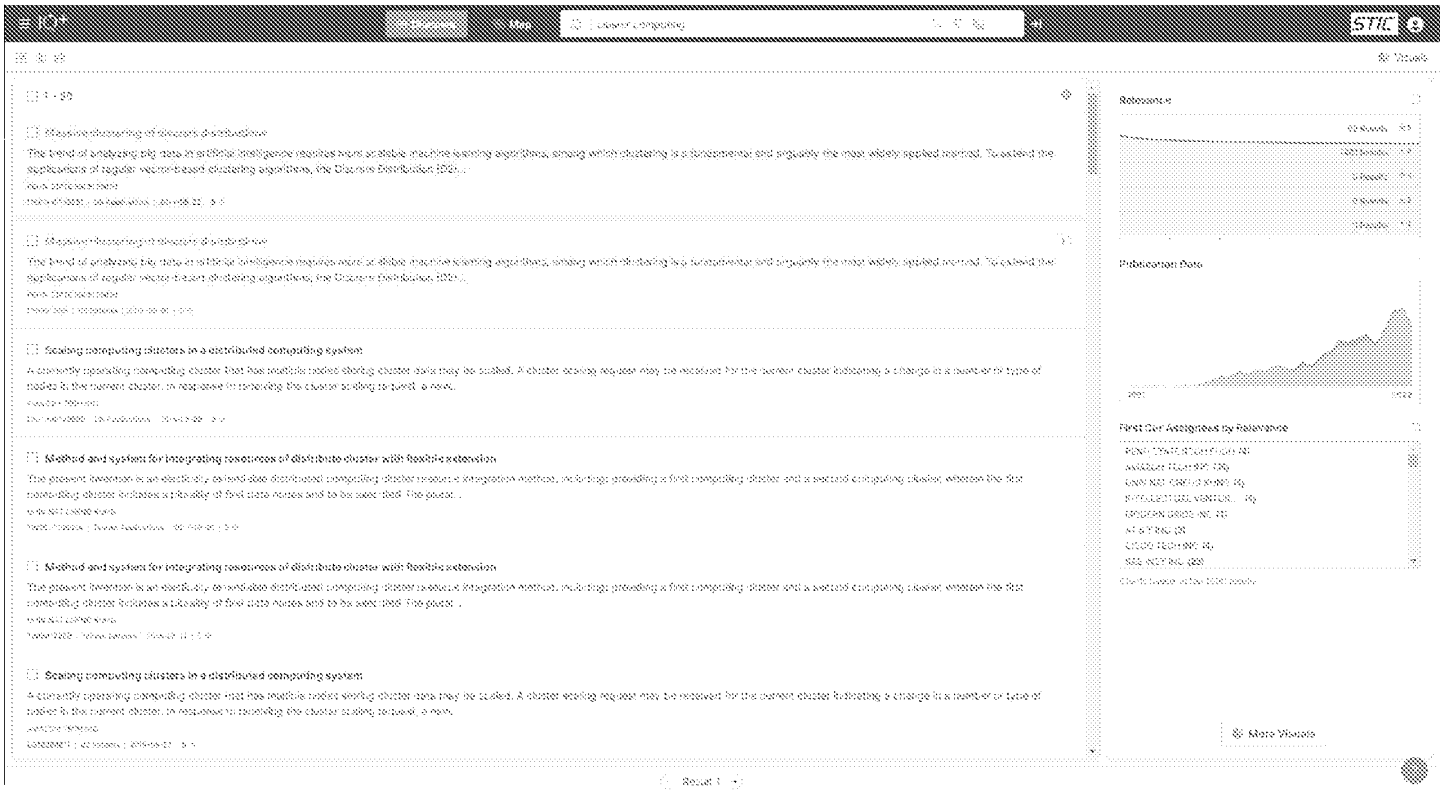
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PRELIMINARY AMENDMENT

First Inventor: Tannenbaum, Zvi	**Conf. No.:** 1893
App. No.: 17/374789	**Filed:** July 13, 2021
Examiner: Asres, Hermon	**Art Unit:** 2449
Title: CLUSTER COMPUTING	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

Prior to examination on the merits, please amend the above-referenced application as provided below.

Amendments to the Claims begin on page 2.

Remarks begin on page 11.

AMENDMENTS TO THE CLAIMS

1. (Canceled)

2. (Currently Amended) A computer cluster comprising:

a plurality of nodes, wherein each of the plurality of nodes comprises a hardware processor, wherein one or more of the nodes are configured to receive a command to start a cluster initialization process for the computer cluster, and wherein each of the nodes is configured to access a non-transitory computer-readable medium comprising program code for a single-node kernel that, when executed, is capable of causing the hardware processor to evaluate mathematical expressions; and

a communications network interface for the nodes to communicate results of mathematical expression evaluation with each other using a peer-to-peer architecture;

wherein the plurality of nodes comprises:

a first node comprising a first hardware processor configured to access a first memory comprising program code for a user interface and program code for a first single-node kernel, the first single-node kernel configured to interpret user instructions and distribute calls to at least one of a plurality of other nodes for execution; and

a second node comprising a second hardware processor with a plurality of processing cores, wherein the second node is configured to receive calls from the first node, execute at least a first mathematical expression evaluation, and communicate a result of the first mathematical expression evaluation to a third node;

wherein the third node comprises a third hardware processor with a plurality of processing cores, wherein the third node is configured to receive the result of the first mathematical expression evaluation from the second node, execute at least a second mathematical expression evaluation using the received result, and communicate the result of the second mathematical expression evaluation to the first node;

wherein the first node is configured to return the result of the second mathematical expression evaluation to the user interface;

wherein one or more of the nodes are configured to:

accept user instructions;

after accepting user instructions, communicate at least some of the user instructions using the communications network interface for the nodes to communicate with each other; and

after communicating at least some of the user instructions using the communications network interface[[ ]], communicate at least some of the user instructions to one or more single-node kernels.

3. (Previously Presented) The computer cluster of claim 2, wherein the communications network interface comprises at least one of: a local bus, a local area network (LAN), a wide area network (WAN), a storage area network (SAN), a TCP/IP interface over Ethernet, or a wireless network interface.

4. (Previously Presented) The computer cluster of claim 2, wherein each of the nodes comprises one or more cluster node modules.

5. (Previously Presented) The computer cluster of claim 2, wherein each single-node kernel is stored in a non-transitory computer-readable medium and configured to accept and execute a request.

6. (Previously Presented) The computer cluster of claim 5, wherein each of the nodes comprises one or more cluster node modules, wherein each of the cluster node modules comprises instructions stored in a non-transitory computer-readable medium, and wherein the instructions, when executed by the hardware processor, cause the cluster node module to communicate with the single-node kernel and with one or more other cluster node modules.

7. (Previously Presented) The computer cluster of claim 6, wherein the plurality of cluster node modules act as a cluster.

8. (Previously Presented) The computer cluster of claim 6, wherein the plurality of cluster node modules communicate with one another to act as a cluster.

9. (Previously Presented) The computer cluster of claim 2, wherein the computer cluster includes the user interface.

10. (Previously Presented) The computer cluster of claim 6, wherein each cluster node module accepts instructions from the user interface and interprets one or more of the instructions.

11. (Previously Presented) The computer cluster of claim 2, wherein the cluster initialization process comprises establishing communication among two or more of the nodes.

12. (Previously Presented) The computer cluster of claim 2, wherein the cluster initialization process comprises configuring access by one or more of the nodes to a computer-readable medium comprising program code for the single-node kernel.

13. (Previously Presented) The computer cluster of claim 12, wherein the cluster initialization process comprises establishing message-passing support among the nodes in the cluster.

14. (Previously Presented) The computer cluster of claim 12, wherein the cluster initialization process comprises launching cluster node modules by the cluster.

15. (Previously Presented) The computer cluster of claim 14, wherein the cluster initialization process comprises assigning a processor identification number to each of the cluster node modules.

16. (Previously Presented) The computer cluster of claim 2, wherein the cluster initialization process comprises:

launching cluster node modules by the cluster; and

after launching the cluster node modules, configuring access by one or more of the nodes to a non-transitory computer-readable medium comprising program code for the single-node kernel.

17. (Previously Presented) The computer cluster of claim 2, wherein the cluster initialization process comprises:

launching cluster node modules by the cluster;

after launching the cluster node modules, establishing communication among two or more of the nodes; and

after establishing communication among two or more of the nodes, assigning a processor identification number to each of the cluster node modules.

18. (Previously Presented) The computer cluster of claim 2, wherein one or more of the nodes are configured to communicate at least some of the user instructions.

19. (Previously Presented) The computer cluster of claim 18, wherein one or more of the nodes are configured to communicate at least some of the user instructions to one or more single-node kernels.

20. (Previously Presented) The computer cluster of claim 2, wherein one or more of the nodes are configured to accept user instructions via one or more of the nodes.

21. (Previously Presented) The computer cluster of claim 20, wherein one or more of the nodes are configured to communicate at least some of the user instructions using the communications network interface for the nodes to communicate with each other.

22. (Previously Presented) The computer cluster of claim 2, wherein one or more of the nodes are configured to transmit at least some of the user instructions that originate from a user interface.

23. (Previously Presented) The computer cluster of claim 2, wherein one or more of the nodes are configured to parallelize at least some of the user instructions before communicating at least some of the user instructions to one or more single-node kernels.

24. (Currently Amended) The computer cluster of claim 2, wherein one or more of the nodes are configured to:

accept user instructions;

after accepting user instructions, communicate at least some of the user instructions using the communications network interface for the nodes to communicate with each other; and

after communicating at least some of the user instructions using the communications network interface[[ ]], communicate at least some of the user instructions to one or more single-node kernels.

25. (Previously Presented) The computer cluster of claim 2, wherein the plurality of nodes are configured to communicate with one another to interpret and translate commands for execution by a plurality of single-node kernels.

26. (Currently Amended) A computer cluster comprising:

a plurality of nodes, wherein one or more of the nodes are configured to receive:

a command to start a cluster initialization process for the computer cluster, wherein the cluster initialization process comprises establishing communication among two or more of the nodes; and

an instruction from a user interface or a script;

and

a communications network interface for the nodes to communicate results of mathematical expression evaluation with each other using asynchronous calls;

wherein each of the nodes is configured to access a non-transitory computer-readable medium comprising program code for a single-node kernel that, when executed, is capable of causing a hardware processor to evaluate mathematical expressions~~;~~

wherein the plurality of nodes comprises:

a first node comprising a first hardware processor configured to access a first memory comprising program code for a user interface and program code for a first single-node kernel, the first single-node kernel configured to interpret user instructions and distribute calls to at least one of a plurality of other nodes for execution; and

a second node comprising a second hardware processor with a plurality of processing cores, wherein the second node is configured to receive calls from the first node, execute at least a first mathematical expression evaluation, and communicate a result of mathematical expression evaluation to a third node;

wherein the third node comprises a third hardware processor with a plurality of processing cores, wherein the third node is configured to receive the result of mathematical expression evaluation from the second node, execute at least a second mathematical expression evaluation using the received result, and communicate the result of the second mathematical expression evaluation to the first node;

wherein the first node is configured to return the result of the second mathematical expression evaluation to the user interface or the script.

wherein one or more of the nodes are configured to:

accept user instructions;

after accepting user instructions, communicate at least some of the user instructions using the communications network interface for the nodes to communicate with each other; and

after communicating at least some of the user instruction using the communications network interface[[ ]], communicate at least some of the user instructions to one or more since-node kernels.

27. (Previously Presented) The computer cluster of claim 26, wherein the asynchronous calls comprise a first command to create a first packet containing:

an expression to be sent as payload; and

a target node where the expression should be sent;

wherein the first command is configured to be called from within a single-node kernel;

wherein the single-node kernel is configured to send the first packet to a local cluster node module; and

wherein the local cluster node module is configured to forward the expression to the target node.

28. (Previously Presented) The computer cluster of claim 26, wherein the communications network interface comprises at least one of: a local bus, a local area network (LAN), a wide area network (WAN), a storage area network (SAN), a TCP/IP interface over Ethernet, or a wireless network interface.

29. (Currently Amended) A computer cluster comprising:

a plurality of nodes, wherein one or more of the nodes are configured to receive:

a command to start a cluster initialization process for the computer cluster, wherein the cluster initialization process comprises establishing communication among two or more of the nodes; and

an instruction from a user interface or a script;

and

a communications network interface for the nodes to communicate results of mathematical expression evaluation with each other, wherein the communications network interface comprises at least one of: a local bus, a local area network (LAN), a wide area network (WAN), a storage area network (SAN), a TCP/IP interface over Ethernet, or a wireless network interface;

wherein each of the nodes is configured to access a non-transitory computer-readable medium comprising program code for a single-node kernel that, when executed, is capable of causing a hardware processor to evaluate mathematical expressions~~;~~

wherein the plurality of nodes comprises:

a first node comprising a first hardware processor configured to access a first memory comprising program code for a user interface and program code for a first single-node kernel, the first single-node kernel configured to interpret user instructions and distribute calls to at least one of a plurality of other nodes for execution; and

a second node comprising a second hardware processor with a plurality of processing cores, wherein the second node is configured to receive calls from the first node, execute at least a first mathematical expression evaluation, and communicate a result of mathematical expression evaluation to a third node;

wherein the third node comprises a third hardware processor with a plurality of processing cores, wherein the third node is configured to receive the result of mathematical expression evaluation from the second node, execute at least a second mathematical expression evaluation using the received result, and communicate the result of the second mathematical expression evaluation to the first node;

and

wherein the first node is configured to return the result of the second mathematical expression evaluation to the user interface or the script;

wherein one or more of the nodes are configured to:

accept user instructions;

after accepting user instructions, communicate at least some of the user instructions using the communications network interface for the nodes to communicate with each other; and

after communicating at least some of the user instructions using the communications network interface[[ ]], communicate at least some of the user instructions to one or more single-node kernels.

30. (Previously Presented) The computer cluster of claim 29, wherein each of the single-node kernels are configured to call a send command involving creating a packet containing:

an expression to be sent as payload; and

where the expression should be sent;

wherein, upon reception of the send command by a local cluster node module associated with the single-node kernel, the local cluster node module is configured to decode the packet and forward a payload to the cluster node module specified in the packet;

wherein each of the single-node kernels is configured to call a receipt command involving creating a packet specifying which message to test for completion and to then wait for a reply expression to evaluate;

wherein, upon reception of the receipt command by the local cluster node module associated with the single-node kernel, the local cluster node module is configured to decode the packet and use a message specifier to search for any matching expressions listed as completed in a received message queue;

wherein, upon determining that such a completed expression is found, the local cluster node module is configured to send the completed expression to a local single-node kernel associated with the cluster node module in response to the receipt command, and

wherein each of the single-node kernels is configured to receive the completed expression and to update variables used by the single-node kernel during evaluation of expressions.

31. (Currently Amended) A computer cluster node for evaluating expressions in parallel with other computer cluster nodes, the computer cluster node comprising:

a hardware processor configured to access one or more non-transitory memory devices comprising program code for a single-node kernel that, when executed, causes the hardware processor to interpret user instructions, to evaluate mathematical expressions, and to produce results of mathematical expression evaluation, wherein the hardware processor comprises multiple processor cores;

a user connection interface configured to receive a command to start a cluster initialization process for a computer cluster;

a communications network interface to communicate results of evaluation with other computer cluster nodes using a peer-to-peer architecture, wherein the communications network interface comprises at least one of: a local bus, a local area network (LAN), a wide area network (WAN), a storage area network (SAN), a TCP/IP interface over Ethernet, or a wireless network interface; and

program code that, when executed, is capable of causing the hardware processor to:

receive calls from a second node comprising a second hardware processor configures to access a second memory comprising program code for a user interface and program code for a second single-node kernel, the second single-node kernel configured to interpret user instructions and distribute calls to at least one of a plurality of other nodes for execution;

execute, using the hardware processor, at least a first mathematical expression evaluation; and

communicate a result of the first mathematical expression evaluation to a third node comprising a third hardware processor with a plurality of processing cores, wherein the third node is configured to receive the result of mathematical expression evaluation from the computer cluster node, execute at least a second mathematical expression evaluation using the result of the first mathematical expression evaluation, and communicate a result of the second mathematical expression evaluation to the first node;

wherein the user connection interface is configured to return at least one result of mathematical expression evaluation to a user interface or a script; and

wherein the computer cluster node is configured to:

accept user instructions;

after accepting user instructions, communicate at least some of the user instructions using the communications network interface for the nodes to communicate with each other; and

after communicating at least some of the user instructions using the communications network interface[[ ]], communicate at least some of the user instructions to the single-node kernel.

REMARKS

Applicant submits this Preliminary Amendment prior to examination. Claims 1-31 were pending in this application. Clarifying amendments are presented herein to independent Claims 2, 24, 26, 29, and 31. No new matter is added by the foregoing amendments. Applicant reserves the right to pursue claims similar to the original claims and/or previously-pending versions of the claims in a continuing application.

No Disclaimers or Disavowals

Applicant reserves the right to pursue at a later date any previously pending or other broader or narrower claims that capture any subject matter supported by the present disclosure, including subject matter found to be specifically disclaimed herein or by any prior prosecution. Accordingly, reviewers of this or any parent, child or related prosecution history shall not reasonably infer that Applicant has made any disclaimers or disavowals of any subject matter supported by the present application.

Other Applications of Assignee

Applicant wishes to draw the Examiner's attention to the following applications of the present application's assignee.

Docket No.	Serial No.	Title	Filed
ZTANN.002A	11/744461	CLUSTER COMPUTING SUPPORT FOR APPLICATION PROGRAMS	05/04/07
ZTANN.002CP1	12/040519	CLUSTER COMPUTING SUPPORT FOR APPLICATION PROGRAMS	02/29/08
ZTANN.002CP1C1	12/465519	AUTOMATIC CLUSTER NODE DISCOVERY AND CONFIGURATION	05/13/09
ZTANN.002P1C2	13/423063	CLUSTER COMPUTING USING SPECIAL PURPOSE MICROPROCESSORS	03/16/12
ZTANN.002P1C3	14/181112	CLUSTER COMPUTING	02/14/14
ZTANN.002P1C5	16/449084	CLUSTER COMPUTING	06/21/19
ZTANN.002P1C6	17/374864	CLUSTER COMPUTING	07/13/21

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: July 19, 2022

By: /Jordan M. Cox/
Jordan M. Cox
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PATENT AND TRADEMARK OFFICE

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APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/374,789	**07/19/2022 05:01:08 PM ET**	**ZTANN.002P1C7**

Title of Invention

CLUSTER COMPUTING

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	1893	FILED BY	Khylo Rhoden
PATENT CENTER #	60795477	FILING DATE	07/13/2021
CUSTOMER #	20995	FIRST NAMED INVENTOR	Zvi Tannenbaum
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Jordan Cox

Documents

TOTAL DOCUMENTS: 3

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
ZTANN002P1C7-PREAMEND.pdf		12	-	139 KB
ZTANN002P1C7-PREAMEND-A.PE.pdf	(1-1)	1	Preliminary Amendment	80 KB
ZTANN002P1C7-PREAMEND-CLM.pdf	(2-10)	9	Claims	110 KB
ZTANN002P1C7-PREAMEND-REM.pdf	(11-12)	2	Applicant Arguments/Remarks Made in an Amendment	103 KB

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ZTANN002P1C7-PREAMEND-A.PE.pdf	ACCD23D4268FE1307571A0C52447708AA2903651037A3B14F086C767869231B5572E34F0661627D1AEB4AC7BCA3CDF186C6E1AFB26278F4ECF436A3022DCB5CE
ZTANN002P1C7-PREAMEND-CLM.pdf	8F834FEF68C07D06C87F3BDA37C34D736985C59F08C6596978DFB28F9808102E1F1D3E66702A7A6D18FFD14486BEA8B5CEE2CD3917B2D078D59CB34C424CF368
ZTANN002P1C7-PREAMEND-REM.pdf	E9386E570D0AE3F8D720A62DFAAA43001765BD5E1E4319FFC0124DA508D4EE4D33D92AEFE2B2D9AC253EFC6CD90624660F270AE168A218554822672F71611E62

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	46128331
Application Number:	17374789
International Application Number:	
Confirmation Number:	1893
Title of Invention:	CLUSTER COMPUTING
First Named Inventor/Applicant Name:	Zvi Tannenbaum
Customer Number:	20995
Filer:	Jordan Michael Cox/Christina Graul
Filer Authorized By:	Jordan Michael Cox
Attorney Docket Number:	ZTANN.002P1C7
Receipt Date:	07-JUL-2022
Filing Date:	13-JUL-2021
Time Stamp:	16:22:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	Source_Code_Distributed_Mathematica-2000_pp159.pdf	4009525 10211057ca66fd36e7b43d43ca7c76a973addb81	no	159

Warnings:

Information:					
2	Non Patent Literature	Source_Code_General_Source_Code-2003_pp173.pdf	8169999 0dfed7e6940d611703c79ddd12b720a35c8e773f	no	173
Warnings:					
Information:					
3	Non Patent Literature	Source_Code_Distributed_Maple-2003_pp2176_Part1.pdf	25152406 153b1b6a0791ac23b41550984d2505abcb504bb2	no	1181
Warnings:					
Information:					
4	Non Patent Literature	Source_Code_Distributed_Maple-2003_pp2176_Part2.pdf	24344341 ca5bcb2985c8c72072065125671779c9114db130	no	995
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Information:					
5	Non Patent Literature	Source_Code_fftw-2003_pp3325_Part1.pdf	25096332 c522d7db2a12d0516a51cd79a341fc7f57cc3e1d	no	305
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Information:					
6	Non Patent Literature	Source_Code_fftw-2003_pp3325_Part2.pdf	25126293 ac7e74fddad5510b72c356cf4d603a7b3ff94a04	no	311
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Information:					
7	Non Patent Literature	Source_Code_fftw-2003_pp3325_Part3.pdf	25165716 07dd52c5972b9e094fdf4cd7c94a1b3004b2d021	no	304
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Information:					
8	Non Patent Literature	Source_Code_fftw-2003_pp3325_Part4.pdf	25122704 82626de07b264633c60cd4a1eaa509ec2b2394cd	no	248
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9	Non Patent Literature	Source_Code_fftw-2003_pp3325_Part5.pdf	25146083 3efcda1a37e8d0eaf90cffb3c4b3037d42f97f89	no	317
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10	Non Patent Literature	Source_Code_fftw-2003_pp3325_Part6.pdf	25107120 2e9cb3eb6c831712e4dcc104b7e60366cff44ea3	no	352
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11	Non Patent Literature	Source_Code_fftw-2003_pp3325_Part7.pdf	25133399 ac8ec8e38e1fededaee71d647dec426ac316036f	no	401
Warnings:					
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12	Non Patent Literature	Source_Code_fftw-2003_pp3325_Part8.pdf	25101394 a31ee9d9f0179e1c6d28e979c26f287dcab86305	no	347
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13	Non Patent Literature	Source_Code_fftw-2003_pp3325_Part9.pdf	25105129 8165ac20c00c4d7dcc9f24c1c440badac0cc708d	no	355
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14	Non Patent Literature	Source_Code_fftw-2003_pp3325_Part10.pdf	25128978 910606a328ac45ce6df005781b71f6387b2f2e94	no	340
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15	Non Patent Literature	Source_Code_fftw-2003_pp3325_Part11.pdf	3083833 02ae05b1dc308508cdc7e37eca7fab373c3e4c52	no	45
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16	Non Patent Literature	Source_Code_matlabpv2-2003_pp4931_Part1.pdf	25112464 30b9624b6fdbbe42934b4d7efced86c8e3306474	no	2461
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17	Non Patent Literature	Source_Code_matlabpv2-2003_pp4931_Part2.pdf	25131337 55ee8b799b1af3367c5ced2391336baec267d356	no	2335
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Information:					
18	Non Patent Literature	Source_Code_matlabpv2-2003_pp4931_Part3.pdf	4319655 6931b353e53bfa58afd8ee6a14536a18f839a73f	no	135
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Information:					
19	Non Patent Literature	Source_Code_Public_CUDA_Brook_Code-2003_pp18573_Part1.pdf	25552642 3340c994c72192d582003ce6ead9b145b5695f40	no	12382
Warnings:					
Information:					
20	Non Patent Literature	Source_Code_Public_CUDA_Brook_Code-2003_pp18573_Part2.pdf	13846337 f26f58cb79b11fbe28705f8899a9012475ce92f7	no	6191
Warnings:					
Information:					
21	Non Patent Literature	Buck_From_Brook_to_CUDA_Presentation_GTC_2009_-_NVIDIA-ACS-0166955_.pdf	2962072 61e9baddad2fed66dce258ab356c5f26476b00e3	no	30
Warnings:					
Information:					
22	Non Patent Literature	NVIDIA_Cuda_Programming_Guide_Ver_10_06-23-2007_-_NVIDIA-ACS-0167649_Part1_.pdf	10920662 324cbab32efb374b241b68524526ab2ca12f8f7a	no	107
Warnings:					
Information:					

23	Non Patent Literature	NVIDIA_Cuda_Programming_Guide_Ver_10_06-23-2007_-_NVIDIA-ACS-0167649_Part2_.pdf	1091189 e9a25fd1ee282d8eb31921f1382a11e2d939824b	no	12
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Information:					
			Total Files Size (in bytes):	424929610	

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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Electronic Acknowledgement Receipt

EFS ID:	46111450
Application Number:	17374789
International Application Number:	
Confirmation Number:	1893
Title of Invention:	CLUSTER COMPUTING
First Named Inventor/Applicant Name:	Zvi Tannenbaum
Customer Number:	20995
Filer:	Jordan Michael Cox/Christina Graul
Filer Authorized By:	Jordan Michael Cox
Attorney Docket Number:	ZTANN.002P1C7
Receipt Date:	07-JUL-2022
Filing Date:	13-JUL-2021
Time Stamp:	16:19:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	Interactive_Supercomputing_-_Parallel_Matlab_Survey_-_NVIDIA-ACS-0234925.pdf	773092 b990ea95cc4d444e88d2acd94862dc9cf212cfdc	no	8

Warnings:

Information:					
2	Non Patent Literature	Interactive_Supercomputing_-_Products_-_NVIDIA-ACS-0234919.pdf	624808 7199c6afb0c174d2c6024a11dcff585578a663d0	no	3
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Information:					
3	Non Patent Literature	Interactive_Supercomputing_-_Resources_-_NVIDIA-ACS-0234922.pdf	239663 d2aedaaf02729552ea841a1e5ca47d39cbbdf1ad	no	3
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Information:					
4	Non Patent Literature	Johnson_-_FFTW_-_NVIDIA-ACS-0234933.pdf	709866 e2cd68a8a2694fca72be456a377e28da7ac6f32c	no	41
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Information:					
5	Non Patent Literature	Kapasi_-_The_Imagine_Stream_Processor_2002_-_NVIDIA-ACS-0167610.pdf	716616 d76b917d7e43e690e1359d87cb7084f1130989c4	no	7
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6	Non Patent Literature	Karonis_-_MPICH2_-_A_Grid-Enabled_Implementation_-_NVIDIA-ACS-0169949.pdf	1168631 5780a549965ca9a4e84aa12f6bb32669a7bad757	no	22
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7	Non Patent Literature	Labonte_-_The_Stream_Virtual_Machine_-_NVIDIA-ACS-0167617.pdf	982284 4ca61067fe3a184ad24722a5f66bb1ae9e13ae1d	no	12
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8	Non Patent Literature	Lecture_Slides_2005-09-03_-_NVIDIA-ACS-0234888.pdf	4737479 dbdec403c0814e6a5d9f4d094bd3293c0ee32d1f	no	2
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9	Non Patent Literature	Lindholm_-_NVIDIA_Tesla_-_NVIDIA-ACS-0167629.pdf	4263111 43b6c87957430d6254431783ad7757be4880bdf1	no	17
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10	Non Patent Literature	Maple_7_Getting_Started_Guide_-_NVIDIA-ACS-0170271.pdf	2098979 6839d44dde4695d764e07819c42b9479eaaf1dc0	no	38
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11	Non Patent Literature	Maple_7_Learning_Guide_-_NVIDIA-ACS-0169971.pdf	7350552 9f6a86ad24282e944dd8205f70264c647f5820c7	no	300
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Information:					
12	Non Patent Literature	Maplesoft_-_Digital_Signal_2004_NVIDIAACS0170309.pdf	1000180 0d652a313cdd639452fb4f108f968ebcef8103f6	no	7
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13	Non Patent Literature	MATLAB_P_Instructions_-_NVIDIA-ACS-0234974.pdf	5022609 dad100352e42c1d132738161fe9252f8f47926cd	no	2
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Information:					
14	Non Patent Literature	Menon_-_MultiMATLAB_-_Integrating_MATLAB_NVIDIAACS0168877.pdf	1010892 dbdb8984d104e086c0a138c7dc932fc42d9bed01	no	18
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15	Non Patent Literature	Mirman_-_Going_Parallel_the_New_way_06-2006_-_NVIDIA-ACS-0234976.pdf	1034310 bb5c42bebf7ae125345ddfeb482e788b00f5b9e0	no	4
Warnings:					
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16	Non Patent Literature	Moore_The_AppleSeed_Project_Clustered_Power_2000_LOWENDMAC_NVIDIA-ACS-0165985.pdf	553055 ad7962ad20f9ec6d4a32a911a64972d3dabbc692	no	3
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17	Non Patent Literature	MPI-2_-_Extensions_oto_the_Message-Passing_Interface_-_NVIDIA-ACS-0235217.pdf	622754 443cdf062980ba36a2409e3c460191ff0977e265	no	11
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18	Non Patent Literature	MPI_Demo_-_NVIDIA-ACS-0234980.pdf	54407 262e41dae04c471ab234cd8742b3484fb92764be	no	4
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19	Non Patent Literature	MPICH_for_Microsoft_-_NVIDIA-ACS-0235213.pdf	135224 7e82d006e10a6283e1361cdce59651fba943935c	no	2
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Information:					
20	Non Patent Literature	LEFOHN_GPGPU_04-20-2005_-_NVIDIA-ACS-0167082_Part1_.pdf	7509521 5cf31faffdba0b41f77cf48539cb6f9603ba4052	no	116
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21	Non Patent Literature	LEFOHN_GPGPU_04-20-2005_-_NVIDIA-ACS-0167082_Part2_.pdf	5631392 da2c7ab0c355c2ebc5b32cbbd6136de83a982b20	no	67
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22	Non Patent Literature	LEFOHN_GPGPU_04-20-2005_-_NVIDIA-ACS-0167082_Part3_.pdf	1660785 b632e6956c3b25e4527b9d244fd5ee1f478323fc	no	14
Warnings:					
Information:					

23	Non Patent Literature	LEFOHN_GPGPU_04-20-2005_-_NVIDIA-ACS-0167082_Part4_.pdf	1605669 d71f15fed4880ec1a76eb2d1083bdec5c007f115	no	14
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24	Non Patent Literature	LEFOHN_GPGPU_04-20-2005_-_NVIDIA-ACS-0167082_Part5_.pdf	1558825 c6f104dfafb02826376e61ece4c658abff7c5cab	no	14
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25	Non Patent Literature	LEFOHN_GPGPU_04-20-2005_-_NVIDIA-ACS-0167082_Part6_.pdf	1722942 2b6eff4205bd74906b6cc098bb7e3bbb67dae648	no	14
Warnings:					
Information:					
26	Non Patent Literature	LEFOHN_GPGPU_04-20-2005_-_NVIDIA-ACS-0167082_Part7_.pdf	2027555 2f12f5b42d9a12ff56dabcf78ed6719f7a300ede	no	14
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27	Non Patent Literature	LEFOHN_GPGPU_04-20-2005_-_NVIDIA-ACS-0167082_Part8_.pdf	6010554 8b0bc8b88271bee2b7c0eff6180e86462aa0c7d6	no	67
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28	Non Patent Literature	LEFOHN_GPGPU_04-20-2005_-_NVIDIA-ACS-0167082_Part9_.pdf	8288597 9a73393f2518af8d4b809c7da9ee5bdc11468b2e	no	119
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29	Non Patent Literature	LEFOHN_GPGPU_04-20-2005_-_NVIDIA-ACS-0167082_Part10_.pdf	4884322 8c039fac9fd13b485d590b7e258228613e0a54c5	no	50
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30	Non Patent Literature	LEFOHN_GPGPU_04-20-2005_-_NVIDIA-ACS-0167082_Part11_.pdf	4822942 7f5cc611fa2d0e2588c26268d5497f0cbdb6444e	no	39
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31	Non Patent Literature	MPICH-A_Portable_Implementation_of_MPI_Home_Page_-_NVIDIA-ACS-0235231.pdf	221729 aaa16da1162e401fcd54c6b04c8adbeb1b3ce5a4	no	3
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32	Non Patent Literature	MPICH2_Home_Page_-_NVIDIA-ACS-0235228.pdf	423646 04ca1935b5a3b4e1ec1171ebf433bf20385f85cc	no	2
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33	Non Patent Literature	MPICH2_License_-_NVIDIA-ACS-0235230.pdf	88929 a13bc8ae27dd153c79aba2c5fe019e3607f08d0e	no	1
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34	Non Patent Literature	Partial_MPI_library_based_on_Sockets_in_Macintosh_OS_X_-_NVIDIA-ACS-0165930.pdf	56379 1fab7ad5c49d0cfa572f05f559185e11fa4178ce	no	1
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35	Non Patent Literature	PCI_Express_Base_Specification_Rev_11_03-28-2005_-_NVIDIA-ACS-0167768.pdf	25683423 cb86b1525fadaa491d44023992ba54f80bc11a54	no	508
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36	Non Patent Literature	Petcu_-_Working_with_multiple_Maple_kernels_-_NVIDIA-ACS-0170367.pdf	557628 ddcddf00a9c3ba7cab1f37afcb817f5eea8c1578	no	11
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37	Non Patent Literature	Petcu_-_A_User-Level_Interface_for_Clustering_-_NVIDIA-ACS-0170316.pdf	466443 096451839ebd479c595547cff41e80e57db06df0	no	7
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38	Non Patent Literature	Petcu_-_Design_and_Implementation_Grid_Extension_for_Maplepdf_-_NVIDIA-ACS-0169935.pdf	1095378 f36880d98c1d87dbf2ef2d6ab0b76d364a8536e1	no	14
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39	Non Patent Literature	Petcu_-_Extending_Maple_to_the_Grid_-_NVIDIA-ACS-0170323.pdf	846856 fa6e8aed10aa43b3e725c93f948bd3b2c20d6215	no	8
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40	Non Patent Literature	Petcu_-_Pavis_-_A_Parallel_Virtual_Environment_-_NVIDIA-ACS-0170331.pdf	390297 8a704c6e3f15af507a18f2c5118922be18054459	no	8
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41	Non Patent Literature	Petcu_-_PVMaple_-_a_Distributed_Approach_-_NVIDIA-ACS-0170339.pdf	399315 58670c5b6ea88399e2837c9330f29371451e4caa	no	8
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42	Non Patent Literature	Petcu_-_Solving_Initial_Value_Problems_-_NVIDIA-ACS-0170347.pdf	551440 d6ee5ec45de5e548653036ad988b6a98baa8387b	no	9
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43	Non Patent Literature	Petcu_-_Survey_of_Symbolic_Computations_on_the_Grid_2005_-_NVIDIA-ACS-0170356.pdf	825761 dd189deba7fe6d30dc72199292207733dee1844d	no	11
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44	Non Patent Literature	Quinn_-_Parallel_Programming_in_C_with_MPI_and_OpenMP_2003_-_NVIDIA-ACS-0235234.pdf	22503891 c79c1b2e048ff4cf094076c3d6d4ddec007a081f	no	516
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45	Non Patent Literature	Running_Star-P_on_Beowulf_-_NVIDIA-ACS-0234985.pdf	196760 bcd0badd013ba7854a7c6b76aa92680db45d8c38	no	5
Warnings:					
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46	Non Patent Literature	Sameh_-_The_Schlumberger_High_Performance_Cluster_at_AUC_-_NVIDIA-ACS-0170378.pdf	778135 b8af867328ffd2c990ca8d963ba58d4904dec578	no	9
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47	Non Patent Literature	Shah_-_Sparce_Matrices_in_MATLAB_P_2004_-_NVIDIA-ACS-0235022.pdf	648798 946ba51f03bfd41c57b4bc9318e546eae8a76979	no	12
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48	Non Patent Literature	Star-P_User_Guide_10-25-2006_-_NVIDIA-ACS-0168895.pdf	21318513 e210c4336c90c32161662d4f337f3d9040b4c6a3	no	211
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49	Non Patent Literature	Sunderam_-_The_PVM_Concurrent_Computing_System_-_NVIDIA-ACS-0170387.pdf	849863 083c3ccd39ec9f2b829c704e1ac477474743e7b0	no	16
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50	Non Patent Literature	Message_Passing_Interface_MPI_standard_-_NVIDIA-ACS-0235215.pdf	157109 2820ae8d8c3bc795305fad2ca0531490b41561ea	no	2
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51	Non Patent Literature	Trefethen_-_MultiMatlab_-_MATLAB_on_Multiple_Processors_-_NVIDIA-ACS-0169109.pdf	1500115 ab59f9e2eb9f672cd08660dcf582d8bf95c17e0e	no	16
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52	Non Patent Literature	Voges_Pope_Computational_Marketing_using_an_Appleseed_2001-NVIDIA-ACS-0166295.pdf	830591 bbb16f8191a39fe62db1d29338ac7d016b19a077	no	11
Warnings:					
Information:					
53	Non Patent Literature	WIRED_Thats_a_Whole_Lot_of_Power_Mac_Slideshow_2002_-_NVIDIA-ACS-0166333.pdf	6805834 49327c75a50de6f4bfc6e4054478f6d2a59c11d9	no	10
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54	Non Patent Literature	Zain-Orchestrating_Production_Computer_Algebrea_2008_-_NVIDIA-ACS-0170434.pdf	699962 b66ce37786b9793d53c82f6dbcbfdee2150fd66c	no	15
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Information:					
55	Non Patent Literature	20210505_-_Decision_-_Granting_Institution_of_IPR_-_IPR2020-01608_-_289_-_NVIDIA-ACS-0223292.pdf	4278451 1d9d545fdd4b5d44e353d06fff598fc4d05c9b8e	no	78
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56	Non Patent Literature	20210505_-_Decision_-_Granting_Institution_of_IPR_-_IPR2021-00075_-_612_-_NVIDIA-ACS-0231637.pdf	3521796 239b2232db9bf569a15cdc1182254c70297649a6	no	67
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57	Non Patent Literature	20210513_-_Decision_-_Granting_Institution_of_IPR_-_IPR2021-00108_-877_-_NVIDIA-ACS-0232790.pdf	3737896 8a4b1d3addd2169de6d02476baaa9e350005fdfd	no	70
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58	Non Patent Literature	20210505_-_Decision_Denying_Institution_of_IPR_-_IPR2021-00019_-_768_-_NVIDIA-ACS-0225177.pdf	2324309 311f97db4228bef66877ede158c3111ab922e6fb	no	32
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59	Non Patent Literature	20210505_-_Decision_Denying_Institution_of_IPR_-_IPR2021-00020_-_768_-_NVIDIA-ACS-0228571.pdf	2221217 7bd2572bf0dcc23edb766cd52c613a290b971e41	no	33
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60	Non Patent Literature	20210617_-_Joint_Motion_to_Terminate_-_IPR2020-01608_-_289_-_NVIDIA-ACS-0223385.pdf	175971 89623bd2cbfba988f54cad0847bae8fb14c03a59	no	6
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Information:					
		Total Files Size (in bytes):	182978051		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	46117185
Application Number:	17374789
International Application Number:	
Confirmation Number:	1893
Title of Invention:	CLUSTER COMPUTING
First Named Inventor/Applicant Name:	Zvi Tannenbaum
Customer Number:	20995
Filer:	Jordan Michael Cox/Christina Graul
Filer Authorized By:	Jordan Michael Cox
Attorney Docket Number:	ZTANN.002P1C7
Receipt Date:	07-JUL-2022
Filing Date:	13-JUL-2021
Time Stamp:	16:20:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	20210617_-_Joint_Motion_to_Terminate_-_IPR2021-00075_-_612_-_NVIDIA-ACS-0231729.pdf	175178 2d9ce430bd7802fa5309b69c0568ad6df7657448	no	6

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2	Non Patent Literature	20210617_-_Joint_Motion_to_Terminate_-_IPR2021-00108_-_877_-_NVIDIA-ACS-0232886.pdf	175550 aff35aea3e16872961e1f209d924a9d161419ac2	no	6
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Information:					
3	Non Patent Literature	20201110_Notice_filing_Date_IPR202001608_289_NVIDIAACS-0222837.pdf	153531 17af4d1284a9fd8b4a43bde7ec1f55e2e03e63a8	no	5
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4	Non Patent Literature	20201110_Notice_of_Filing_Prelim_Response_IPR2021-00019_768_NVIDIAACS0224757.pdf	152936 be544c0c3b4c28f714b89c86f80fdb2855d00552	no	5
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5	Non Patent Literature	20201110_Notice_of_Filing_Date_Time_for_Prelim_Response_IPR202100020_768_Part_B_NVIDIAACS0228113.pdf	153018 86f61cc038e590d9d1f8dbc07e28bbd658a0eba3	no	5
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Information:					
6	Non Patent Literature	20201110_Notice_of_Filing_Date_Prelim_ResponsePR2021-00075_612_NVIDIA-ACS-0231196.pdf	152698 fce127871e16b310413782f24f8f35514e61de63	no	5
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7	Non Patent Literature	20201117_-_Notice_of_Filing_IPR202100108_877_NVIDIAACS0232321.pdf	157907 a9fdaa55853128bc2fdddc0d072e64ccb82fa130	no	6
Warnings:					
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8	Non Patent Literature	20210630_-_Notice_of_Refund_-_IPR2020-01608_-_289_-_NVIDIA-ACS-0223400.pdf	36205 52858514fd386f80e3146f28466ba9c5bc8a83e6	no	2
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9	Non Patent Literature	20210712_-_Notice_of_Refund_-_IPR2021-00075_-_NVIDIA-ACS-0231745.pdf	35838 d77665953b3d148745b4c3897c7049b79c0ff4b0	no	2
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10	Non Patent Literature	20210712_-_Notice_of_Refund_-_IPR2021-00108_-_NVIDIA-ACS-0232906.pdf	35969 16d16b065eea371c9cf7835f0bc758422737bc24	no	2
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11	Non Patent Literature	20210518_-_Notice_of_Refund_-_IPR2021-00019_-_NVIDIA-ACS-0225212.pdf	35962 324801bb132402e34a9c42d74d0efdc6799782c7	no	2
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12	Non Patent Literature	20210517_-_Notice_of_Refund_-_IPR2021-00020_-_NVIDIA-ACS-0228607.pdf	36011 70a0489458e897c0d3258cbfc3ed90b902511591	no	2
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13	Non Patent Literature	20210310_Order_Conduct_of_the_Proceeding_IPR2020-01608_NVIDIAACS0223288.pdf	119105 fb846269c7793fbb356dec65d91944b9e879b4c4	no	4
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14	Non Patent Literature	20210310_Order_Conduct_of_the_Proceeding_IPR2021000075_NVIDIAACS0231608.pdf	119022 3b9a35d085444b92485b712d4656ab4d45a10f9e	no	4
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15	Non Patent Literature	20200918_-_NVIDIA_Petition_for_Inter_Partes_Review_-_NVIDIA-ACS-0222731.pdf	7838936 71c9a931042e2a95909edf2a3412aa7b6abde8c7	no	97
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16	Non Patent Literature	20201023_-_NVIDIA_Petition_for_Inter_Partes_Review_-_NVIDIA-ACS-0232222.pdf	6578605 7016ec4b2e8ba808d7996e7ce221b2cdde93bee0	no	93
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17	Non Patent Literature	20201009_-_ACS_Mandatory_Notices_-_NVIDIA-ACS-0222830.pdf	100164 335c949d0598bef84c98649bc84dc5048de23f71	no	4
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18	Non Patent Literature	20201027_-_ACS_Mandatory_Notices_-_IPR2021-00019_-_768_Part_A_-_NVIDIA-ACS-0224753.pdf	104197 0f4acb756e7600cf9bf74ef38257b4c5966efe1d	no	4
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19	Non Patent Literature	20201027_-_ACS_Mandatory_Notices_-_IPR2021-00019_-_768_Part_B_-_NVIDIA-ACS-0228109.pdf	104303 7f8dba4a4d582d72c89ac35f6f81d7d9f32283c4	no	4
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20	Non Patent Literature	20201016_-_NVIDIA_Petition_for_Inter_Partes_Review_-_NVIDIA-ACS-0231103.pdf	6238135 6c25afcb70d5b30e58342da85f4fb5eb9e0c6e50	no	87
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21	Non Patent Literature	20201112_-_ACS_Mandatory_Notices_-_IPR2021-00108_-_877_-_NVIDIA-ACS-0232317.pdf	103673 fbae969b898993c78be4c2463c96595ab6b24f6e	no	4
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22	Non Patent Literature	20210210_-_ACS_Preliminary_Response_-_IPR2020-01608_-_289_-_NVIDIA-ACS-0222842.pdf	4088878 f2f7df92a01932e34275ae80e12d227822010441	no	76
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23	Non Patent Literature	20210210_-_ACS_Preliminary_Response_-_IPR2021-00019_-_768_-_NVIDIA-ACS-0224762.pdf	3342410 39e2e3b652bf7021faab283d21fe15925f7ec27f	no	68
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24	Non Patent Literature	20210210_-_ACS_Preliminary_Response_-_IPR2021-00020_-_768_-_NVIDIA-ACS-0228118.pdf	3275982 a1307cf4855892eca48f5ed9caa0c126224158ed	no	66
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25	Non Patent Literature	20210210_-_ACS_Preliminary_Response_-_IPR2021-00075_-_612_-_NVIDIA-ACS-0231201.pdf	3669557 2a0707d08fe23f3334a91573b21d7006240d7791	no	66
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26	Non Patent Literature	20210217_-_ACS_Preliminary_Response_-_IPR2021-00108_-_877_-_NVIDIA-ACS-0232327.pdf	3618624 fb33b176a35245e012db40d8caa663de803916a1	no	65
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27	Non Patent Literature	20210617_-_Updated_Exhibit_List_-_IPR2020-01608_-_289_-_NVIDIA-ACS-0223391.pdf	225444 41d3d514ee9e185cc91a0cbb605ad77527e76f56	no	5
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28	Non Patent Literature	20210617_-_Updated_Exhibit_List_-_IPR2021-00075_-_612_-_NVIDIA-ACS-0231735.pdf	284044 3c933fc5220231e49896d5709a086ea99accef01	no	5
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29	Non Patent Literature	20210617_-_Updated_Exhibit_List_-_IPR2021-00108_-_877_-_NVIDIA-ACS-0232892.pdf	287066 c617033def1fbab9b3db6ac74b5cda13039b571a	no	5
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30	Non Patent Literature	20210519_-_NVIDIA_Objections_to_Evidence_-_IPR2020-01608_-_289_-_NVIDIA-ACS-0223378.pdf	65872 7d15d17bed60e92cfa784257debf96fcda4d6af7	no	4
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31	Non Patent Literature	20210519_-_NVIDIA_Objections_to_Evidence_-_IPR2021-00075_-_612_-_NVIDIA-ACS-0231722.pdf	65230 5b9ffa6fa48e7800ed22e0ae491225644148fa1a	no	4
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32	Non Patent Literature	20210519_-_NVIDIA_Objections_to_Evidence_-_IPR2021-00108_-_877_-_NVIDIA-ACS-0232871.pdf	65496 1e5826ee59910d46e9f313f4a092a41be950f0ef	no	4
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33	Non Patent Literature	20210519_-_ACS_Objections_to_Evidence_-_IPR2020-01608_-_289_-_NVIDIA-ACS-0223370.pdf	619753 c3acc849c43771d6a4a45ad32711596b97a0ea18	no	8
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34	Non Patent Literature	20210519_-_ACS_Objections_to_Evidence_-_IPR2021-00075_-_612_-_NVIDIA-ACS-0231715.pdf	511211 a96b1869e7a93229b4f6d93b9b028ebb9a6bc548	no	7
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35	Non Patent Literature	20210527_-_ACS_Objection_to_Admissibility_of_Evidence_-_NVIDIA-ACS-0232875.pdf	535473 c2df2b236b8531c05fd6ebed96defe35537ab63e	no	8
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36	Non Patent Literature	20201016_-_NVIDIA_Power_of_Attorney_-_NVIDIA-ACS-0231190.pdf	85215 277ca0d896026babafe3e62beda042ace3971048	no	2
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37	Non Patent Literature	20201023_-_NVIDIA_Power_of_Attorney_-_NVIDIA-ACS-0232315.pdf	85394 54ee9a7cd5dc89d41322cd3c12cbec4186ef6187	no	2
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38	Non Patent Literature	20210326_-_ACS_Sur-Reply_ISO_Preliminary_Responses_-_NVIDIA-ACS-0231624.pdf	474417 fd691e1b80532807e8a80a6230cb095ab8c40cf4	no	13
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39	Non Patent Literature	20210513_-_NVIDIA_Request_for_Refund_of_Fees_-_IPR2021-00019_-_NVIDIA-ACS-0225209.pdf	61622 884b776ce36cb3bab013126bde9c393da60fbb5c	no	3
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40	Non Patent Literature	20210513_-_NVIDIA_Request_for_Refund_of_Fees_-_IPR2021-00020_-_NVIDIA-ACS-0228604.pdf	61840 c51366869868bf94868ef6b89d745a9122b08e10	no	3
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41	Non Patent Literature	20210630_-_NVIDIA_Request_for_Refund_of_Post-Institution_Fees_-_NVIDIA-ACS-0223402.pdf	95014 767aac50a7bef38c1001fff50a7c42d29d6b386f	no	4
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42	Non Patent Literature	20210630_NVIDIA_Request_for_Refund_of_Post_IPR2021000755_612_NVIDIAACS0231740.pdf	108155 2ca1c41c588f5b7c78698e933f9f418f2a848842	no	5
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43	Non Patent Literature	20210630_-_NVIDIA_Request_for_Refund_of_PostPR202100108_877_NVIDIAACS0232897.pdf	108894 7a128a74589ce7c3955689b9f3e9a2af4785b653	no	5
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44	Non Patent Literature	20210505_-_Scheduling_Order_-_IPR2020-01608__IPR2021-00075_-_289__612_-_NVIDIA-ACS-0231704.pdf	378102 243245a732db5bd7db0c4f0796460effe022d973	no	11
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45	Non Patent Literature	20210513_-_Scheduling_Order_-_IPR2021-00108_-877_-_NVIDIA-ACS-0232860.pdf	367784 b1114354f200767893c82a5aa0c55d989359886a	no	11
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Information:					
46	Non Patent Literature	20210622_-_Termination_Due_to_Settlement_After_Institution_of_Trial_-_NVIDIA-ACS-0223396.pdf	76010 8a821526745837a3a283e61151272d6375e04ddd	no	4
Warnings:					
Information:					
47	Non Patent Literature	20210630_-_Termination_Due_to_Settlement_IPR202100108_877_NVIDIAACS0232902.pdf	77213 7643e3d1c71c1dd65ba8cae13630a1cb9b11fce4	no	4
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Information:					
48	Non Patent Literature	20210210_-_Ex_2006_-_Dauger_Declaration_-_NVIDIA-ACS-0223018.pdf	1506686 04acd65559e0e2cf0c183a4030a75798d10e943e	no	29
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49	Non Patent Literature	20200918_-_Ex_1002_-_US_8082289_B2_File_History_-_NVIDIA-ACS-0220502.pdf	8142280 94eaa3d1e8532651c2389383b0b9e3694ac88859	no	190
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50	Non Patent Literature	Ex_2004_-_Nexus_Claim_Chart_-_SEM_-_289_Patent_-_NVIDIA-ACS-0222970_.pdf	2392959 2baa9af3c903c7a698a8f4484248a2fa335c3f0b	no	20
Warnings:					
Information:					

51	Non Patent Literature	EXT2005.pdf	3180058 a4e4a0d091f746fc0c1e01c0b435c0e9692225d8	no	28
Warnings:					
Information:					
52	Non Patent Literature	DECYK_AppleSeed_Personal_Computing_06-12-2005_-_NVIDIA-ACS-0165931.pdf	384023 3d6385c4448026759b8a5c1c7752ada5546b884a	no	2
Warnings:					
Information:					
53	Non Patent Literature	GRIGORAS_Advanced_Environments_NVIDIAACS0169147.pdf	20094788 95b9f415f0fd42a3be365beaf1c77cbaf17f8f80	no	333
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54	Non Patent Literature	20201106_-_ACS_Mandatory_Notice_-_IPR2021-00075_-_612_-_NVIDIA-ACS-0231192.pdf	104232 1e740a24b1d936c4126d936175f0998584bd6754	no	4
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55	Non Patent Literature	20201029_-_ACS_Updated_Mandatory_Notices_-_NVIDIA-ACS-0222834.pdf	63504 542a7e012b9e475c79fb637f9a75c49e985d904e	no	3
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56	Non Patent Literature	20210316_-_NVIDIA_Reply_to_Preliminary_Response_-_NVIDIA-ACS-0231612.pdf	404875 118cbe093bf6b2e05bb8c91619180caaadfc8fee	no	12
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57	Non Patent Literature	20210614_-_Exhibit_2027_-_NVIDIA-ACS-0223382.pdf	110876 d020e31a927d0939d5b74709b1e0e9adc0e5227c	no	3
Warnings:					
Information:					
		Total Files Size (in bytes):	81625924		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	17/374789
	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
(Multiple sheets used when necessary)	Examiner	Asres, Hermon
SHEET 1 OF 11	Attorney Docket No.	ZTANN.002P1C7

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number *Number - Kind Code (if known)* Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	7,015,915	03-21-2006	Diard	
	2	7,162,590	01-09-2007	Pruvost et al.	
	3	7,275,123	09-25-2007	Duncan et al.	
	4	7,289,125	10-30-2007	Diard et al.	
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	11	7,996,592	08-09-2011	Kim et al.	
	12	8,074,224	12-06-2011	Nordquist et al.	
	13	8,321,849	11-27-2012	Nickolls et al.	
	14	8,539,207	09-17-2013	LeGrand	
	15	8,941,668	01-27-2015	Diamond	

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Examiner Initials	Cite No.	Foreign Patent Document *Country Code-Number-Kind Code* Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	**T[1]**

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	**T[1]**
	16	AppleSeed Development Page, April 12, 2004 https://web.archive.org/web/20050317034217/http:/exodus.physics.ucla.edu/appleseed/dev/developer.html as archived March 17, 2005, pp. 6. [NVIDIA-ACS-0165922]	
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Examiner Signature	Date Considered

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	17/374789
	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
(Multiple sheets used when necessary)	Examiner	Asres, Hermon
SHEET 2 OF 11	Attorney Docket No.	ZTANN.002P1C7

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	19	BRIDGES et al., "Users' Guide to mpich, a Portable Implementation of MPI", September 18, 1995, pp. 35. [NVIDIA-ACS-0235035]	
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	29	BUCK, Ian, "TESLA, GPU Computing, Past, Present, Future", Presentation, 2012, pp. 21. [NVIDIA-ACS-0166828]	
	30	BURNS et al., "LAM: An Open Cluster Environment for MPI", Ohio Supercomputer Center, Colombus, OH, 2001, pp. 8. [NVIDIA-ACS-0168697]	
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Examiner Signature	Date Considered

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	17/374789
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	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
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SHEET 3 OF 11	Attorney Docket No.	ZTANN.002P1C7

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
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	Art Unit	2449
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SHEET 4 OF 11	Attorney Docket No.	ZTANN.002P1C7

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	123	DECISION Denying Institution of Inter Partes Review of U.S. Patent No. 10,333,768, in Case IPR2021-00019, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated May 5, 2021 in 32 pages. [NVIDIA-ACS-0225177]	
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	125	Joint Motion to Terminate Under 35 U.S.C. § 317(a) of U.S. Patent No. 8,082,289, in Case IPR2020-01608, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed June 17, 2021 in 6 pages. [NVIDIA-ACS-0223385]	
	126	Joint Motion to Terminate Under 35 U.S.C. § 317(a) of U.S. Patent No. 8,140,612, in Case IPR2021-00075, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed June 17, 2021 in 6 pages. [NVIDIA-ACS-0231729]	
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	138	ORDER Conduct of the Proceeding, IPR2020-01608 (Patent 8,082,289), IPR2021-00019 (Patent 10,333,768), IPR2021-00020 (Patent 10,333,768), IPR2021-00075 (Patent 8,140,612), IPR2021-00108 (Patent 8,676,877)1, NVIDIA Corporation v. Advanced Cluster Systems, Inc., Paper 8 as dated March 10, 2021 in 4 pages. [NVIDIA-ACS-0223288]	
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	141	Petition for Inter Partes Review of U.S. Patent No. 8,140,612, in Case IPR2021-00075, Patent No. 8,140,612, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated October 16, 2020 in 87 pages. [NVIDIA-ACS-0231103]	
	142	Petition for Inter Partes Review of U.S. Patent No. 8,676,877, in Case IPR2021-00108, Patent No. 8,676,877, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated October 23, 2020 in 93 pages. [NVIDIA-ACS-0232222]	
	143	Patent Owner Mandatory Notices in Case No. IPR2020-01608, U.S. Patent No. 8,082,289, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed October 9, 2020 in 4 pages. [NVIDIA-ACS-0222830]	
	144	Patent Owner Mandatory Notices in Case No. IPR2021-00019, U.S. Patent No. 10,333,768, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed October 27, 2020 in 4 pages. [NVIDIA-ACS-0224753]	
	145	Patent Owner Mandatory Notices in Case No. IPR2021-00020, U.S. Patent No. 10,333,768, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed October 27, 2020 in 4 pages. [NVIDIA-ACS-0228109]	
	146	Patent Owner Mandatory Notices in Case No. IPR2021-00075, U.S. Patent No. 8,140,612, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed November 6, 2020 in 4 pages. [NVIDIA-ACS-0231192]	
	147	Patent Owner Mandatory Notices in Case No. IPR2021-00108, U.S. Patent No. 8,676,877, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed November 12, 2020 in 4 pages. [NVIDIA-ACS-0232317]	
	148	Patent Owner Preliminary Response in Case No. IPR2020-01608, U.S. Patent No. 8,082,289, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed February 10, 2021 in 66 pages. [NVIDIA-ACS-0222842]	
	149	Patent Owner Preliminary Response in Case No. IPR2021-00019, U.S. Patent No. 10,333,768, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed February 10, 2021 in 66 pages. [NVIDIA-ACS-0224762]	
	150	Patent Owner Preliminary Response in Case No. IPR2021-00020, U.S. Patent No. 10,333,768, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed February 10, 2021 in 66 pages. [NVIDIA-ACS-0228118]	
	151	Patent Owner Preliminary Response in Case No. IPR2021-00075, U.S. Patent No. 8,140,612, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed February 10, 2021 in 66 pages. [NVIDIA-ACS-0231201]	
	152	Patent Owner Preliminary Response in Case No. IPR2021-00108, U.S. Patent No. 8,676,877, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed February 17, 2021 in 66 pages. [NVIDIA-ACS-0232327]	
	153	Patent Owner Updated Mandatory Notices in Case No. IPR2020-01608, U.S. Patent No. 8,082,289, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed October 29, 2020 in 3 pages. [NVIDIA-ACS- 0222834]	
	154	Patent Owner's Consolidated Sur-Reply in Support of its Preliminary Responses, Per March 10, 2021 Order in Cases IPR2020-01608 (Patent 8,082,289), IPR2021-00019 (Patent 10,333,768), IPR2021-00020 (Patent 10,333,768), IPR2021-00075 (Patent 8,140,612), IPR2021-00108 (Patent 8,676,877), NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed March 26, 2021 in 13 pages. [NVIDIA-ACS-0231624]	
	155	Patent Owner's Updated Exhibit List in Case No. IPR2020-01608, U.S. Patent No. 8,082,289, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed June 17, 2021 in 5 pages. [NVIDIA-ACS-0223391]	

Examiner Signature	Date Considered

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	17/374789
	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
(Multiple sheets used when necessary)	Examiner	Asres, Hermon
SHEET 10 OF 11	Attorney Docket No.	ZTANN.002P1C7

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	156	Patent Owner's Updated Exhibit List in Case No. IPR2021-00075, U.S. Patent No. 8,140,612, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed June 17, 2021 in 5 pages. [NVIDIA-ACS-0231735]	
	157	Patent Owner's Updated Exhibit List in Case No. IPR2021-00108, U.S. Patent No. 8,676,877, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed June 17, 2021 in 5 pages. [NVIDIA-ACS-0232892]	
	158	Petitioner's Objections to Evidence in Case No. IPR2020-01608, U.S. Patent No. 8,082,289, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed May 19, 2021 in 4 pages. [NVIDIA-ACS-0223378]	
	159	Petitioner's Objections to Evidence in Case No. IPR2021-00075, U.S. Patent No. 8,140,612, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed May 19, 2021 in 4 pages. [NVIDIA-ACS-0231722]	
	160	Petitioner's Objections to Evidence in Case No. IPR2021-00108, U.S. Patent No. 8,676,877, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed May 19, 2021 in 4 pages. [NVIDIA-ACS-0232871]	
	161	Patent Owner's Objections to Admissibility of Evidence Served with Petition for Inter Partes Review in Case No. IPR2020-01608, U.S. Patent No. 8,082,287, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed May 19, 2021 in 8 pages. [NVIDIA-ACS-0223370]	
	162	Patent Owner's Objections to Admissibility of Evidence Served with Petition for Inter Partes Review in Case No. IPR2021-00075, U.S. Patent No. 8,140,612, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed May 19, 2021 in 7 pages. [NVIDIA-ACS-0231715]	
	163	Patent Owner's Objections to Admissibility of Evidence Served with Petition for Inter Partes Review in Case No. IPR2021-00108, U.S. Patent No. 8,676,877, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed May 27, 2021 in 8 pages. [NVIDIA-ACS-0232875]	
	164	Petitioner's Power of Attorney in Case No. IPR2021-00075, U.S. Patent No. 8,140,612, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed October 16, 2020 in 2 pages. [NVIDIA-ACS-0231190]	
	165	Petitioner's Power of Attorney in Case No. IPR2021-00108, U.S. Patent No. 8,676,877, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as filed October 23, 2020 in 2 pages. [NVIDIA-ACS-0232315]	
	166	Petitioner's Reply to Patent Owner's Preliminary Response in IPR2020-01608 (Patent 8,082,289), IPR2021-00019 (Patent 10,333,768), IPR2021-00020 (Patent 10,333,768), IPR2021-00075 (Patent 8,140,612), IPR2021-00108 (Patent 8,676,877), NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated March 16, 2021 in 12 pages. [NVIDIA-ACS-0231612]	
	167	Petitioner's Request for Refund of Fees of U.S. Patent No. 10,333,768, Case IPR2021-00019, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated May 13, 2021 in 3 pages. [NVIDIA-ACS-0225209]	
	168	Petitioner's Request for Refund of Fees of U.S. Patent No. 10,333,768, Case IPR2021-00020, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated May 13, 2021 in 3 pages. [NVIDIA-ACS-0228604]	
	169	Petitioner's Request for Refund of Post-Institution Fees of U.S. Patent No. 8,082,289, Case IPR2020-01608, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated June 30, 2021 in 4 pages. [NVIDIA-ACS-0223402]	
	170	Petitioner's Request for Refund of Post-Institution Fees of U.S. Patent No. 8,140,612, Case IPR2021-00075, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated June 30, 2021 in 5 pages. [NVIDIA-ACS-0231740]	

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T[1] - Place a check mark in this area when an English language Translation is attached.

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	17/374789
	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
(Multiple sheets used when necessary)	Examiner	Asres, Hermon
SHEET 11 OF 11	Attorney Docket No.	ZTANN.002P1C7

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	171	Petitioner's Request for Refund of Post-Institution Fees of U.S. Patent No. 8,676,877, Case IPR2021-00108, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated June 30, 2021 in 5 pages. [NVIDIA-ACS-0232897]	
	172	Scheduling Order of U.S. Patent No. 8,082,289, Case IPR2020-01608 and U.S. Patent No. 8,140,612, Case IPR2021-00075, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated May 5, 2021 in 11 pages. [NVIDIA-ACS-0231704]	
	173	Scheduling Order of U.S. Patent No. 8,676,877, Case IPR2021-00108, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated May 13, 2021 in 11 pages. [NVIDIA-ACS-0232860]	
	174	Stipulated Partial Dismissal with Prejudice in Case 1:19-cv-02032-CFC-CJB, Advanced Cluster Systems, Inc v. NVIDIA Corporation, as filed June 14, 2021 in 3 pages. [NVIDIA-ACS-0223382, NVIDIA-ACS-0231726 & NVIDIA-ACS-0232883]	
	175	Termination Due to Settlement After Institution of Trial of U.S. Patent No. 8,082,289, Case IPR2020-01608, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated June 22, 2021 in 4 pages. [NVIDIA-ACS-0223396]	
	176	Termination Due to Settlement After Institution of Trial of U.S. Patent No. 8,676,877, Case IPR2021-00108, NVIDIA Corporation v. Advanced Cluster Systems, Inc., as dated June 30, 2021 in 4 pages. [NVIDIA-ACS-0232902]	
	177	Ex. 2004 - Nexus Claim Chart - SEM - 289 Patent, pp. 20. [NVIDIA-ACS-0222970]	
	178	Ex. 2005 - Nexus Claim Chart - SET - 289 Patent, pp. 28. [NVIDIA-ACS-0222990]	
	179	Ex. 2006 - Dauger Declaration, February 10, 2021, pp. 29. [NVIDIA-ACS-0223018]	
	180	Exhibit 1002 - File History of USP 8,082,289 B2, pp. 190. [NVIDIA-ACS-0220502]	

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Examiner Signature	Date Considered

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Electronic Patent Application Fee Transmittal					
Application Number:	17374789				
Filing Date:	13-Jul-2021				
Title of Invention:	CLUSTER COMPUTING				
First Named Inventor/Applicant Name:	Zvi Tannenbaum				
Filer:	Jordan Michael Cox/Janet Teeters				
Attorney Docket Number:	ZTANN.002P1C7				
Filed as Small Entity					
Filing Fees for Utility under 35 USC 111(a)					
Description		**Fee Code**	**Quantity**	**Amount**	**Sub-Total in USD($)**
Basic Filing:					
Pages:					
Claims:					
Miscellaneous-Filing:					
Petition:					
Patent-Appeals-and-Interference:					
Post-Allowance-and-Post-Issuance:					
Extension-of-Time:					

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE- 2ND AND SUBSEQUENT REQUEST	2820	1	1000	1000
		Total in USD ($)		**1000**

Electronic Acknowledgement Receipt	
EFS ID:	46104996
Application Number:	17374789
International Application Number:	
Confirmation Number:	1893
Title of Invention:	CLUSTER COMPUTING
First Named Inventor/Applicant Name:	Zvi Tannenbaum
Customer Number:	20995
Filer:	Jordan Michael Cox/Christina Graul
Filer Authorized By:	Jordan Michael Cox
Attorney Docket Number:	ZTANN.002P1C7
Receipt Date:	07-JUL-2022
Filing Date:	13-JUL-2021
Time Stamp:	16:15:15
Application Type:	Utility under 35 USC 111(a)

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Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	E202277G17162429
Deposit Account	111410
Authorized User	Christina Graul
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	AppleSeed_Development_Page_03-17-2005_-_NVIDIA-ACS-0165922.pdf	592527 1e5cc3a2bae6eac816cfc46f21c1cb6db2faf c14	no	6
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2	Non Patent Literature	Balay_-_PETSc_Users_Manual_09-01-2006_-_NVIDIA-ACS-0168513.pdf	9515286 5d3caffaf48f89b9d131ce2747c0b242b147 be8f	no	184
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3	Non Patent Literature	Barnell_-_Migrating_Modeling_and_Simulation_Applications_08-18-2006_-_NVIDIA-ACS-0234890.pdf	1288293 2d5e73a222d62b877ba84f012471289816c ea521	no	8
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4	Non Patent Literature	Bridges_-_Users_Guide_to_mpich_a_Portable_Implementation_of_MPI_09-15-1995_-_NVIDIA-ACS-0235035.pdf	1407070 bfea9213d048777601f6bcfee176764c47a2 379a	no	35
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5	Non Patent Literature	Buck_-_Brook_for_GPUs_Presentation_02-10-2003_-_NVIDIA-ACS-0166705.pdf	503985 273b7784ab1976c4da6c7e3606c6df0c28b 8e54a	no	19
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6	Non Patent Literature	Buck_-_Brook_for_GPUs_2004_-_NVIDIA-ACS-0166724.pdf	1080136 99b350f9d15100320bdf4d187bdf209ca35 d5faa	no	10
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7	Non Patent Literature	Buck_-_Brook_for_GPUs_Presentation_SIGGRAPH2004-_NVIDIA-ACS-0166734_.pdf	2770018 ae5f78629aca8ee41660a5331f2e34786a969668	no	36
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8	Non Patent Literature	Buck_-_Brook_-_A_Streaming_Programming_Language_10-08-2001_-_NVIDIA-ACS-0166693.pdf	373140 7549e272c5f7d0bc563b29c5abb43db11085d0da	no	12
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9	Non Patent Literature	Buck_-_GPU_Computing_with_NVIDIA_CUDA_-_NVIDIA-ACS-0166799_.pdf	3585467 becba8989d85ee68f41956bacf177608a60b1f15	no	29
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10	Non Patent Literature	Buck_-_Stream_Computing_on_Graphics_Hardware_Thesis_-_09-2006_-_NVIDIA-ACS-0166849.pdf	4254634 109b7f84248a6c4c2444af212a814d831a975eb5	no	106
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11	Non Patent Literature	Buck_-_TESLA_GPU_Computing_History_-_NVIDIA-ACS-0166828_.pdf	2089697 dff1a33d5fc4661fe93cfc9a133429a9730a9b94	no	21
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13	Non Patent Literature	Burns_-_LAM_-_An_Open_Cluster_Environment_for_MPI_-_NVIDIA-ACS-0168697.pdf	708823 1de2b5a2f1af88d6c4401def80e0236dd2542d47	no	8
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14	Non Patent Literature	Chpt_4_-_Merrimac_-_The_Streaming_Supercomputer_2003_-_NVIDIA-ACS-0167001.pdf	4681109 6b6a92c05a8812d94d2e54d8c61ef9f368ea5b82	no	55
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15	Non Patent Literature	Cheng_-_Fast_Sorting_on_a_Distributed-Memory_Architecture_-_NVIDIA-ACS-0234898.pdf	599804 1a2f5770b36baecf496044480a1538650bc7427d	no	7
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16	Non Patent Literature	Choy_-_Parallel_MATLAB_-_Doing_It_Right_-_NVIDIA-ACS-0168766.pdf	1753328 9a128660c944e6cbe2841025edfad4cadd75ec22	no	11
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17	Non Patent Literature	Choy_-_MATLAB_P_20_-_A_unified_parallel_MATLAB_-_NVIDIA-ACS-0168705.pdf	817883 12aedbe7987d48564602376bab01949275c6e710	no	6
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18	Non Patent Literature	Choy_-_Star-P_-_High_Productivity_Parallel_Computing_-_NVIDIA-ACS-0234905.pdf	124039 3cd2af7d1203ee295641c9f94daf397ff822be1b	no	2
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19	Non Patent Literature	Buchberger_-_CONCERT_1997_-_NVIDIA-ACS-0169480.pdf	3176446 76d917cf638591571d5bb820e11904d5c8f8a17a	no	60
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20	Non Patent Literature	Choy_Source_Code_Project_status_-_NVIDIA-ACS-0234984.pdf	17834 d07f24dcafad982c150d37a6006c171a145905b0	no	1
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21	Non Patent Literature	Dally_-_A_Streaming_Supercomputer_09-18-2001_-_NVIDIA-ACS-0167056.pdf	1179213 db76ec8d674d18f89a20f752da755f675d12d2bf	no	17
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22	Non Patent Literature	Dauger_Simulation_and_study_of_Fresnel_diffraction_1996_-_NVIDIA-ACS-0165941.pdf	1648369 ad5c0a9bd2f1b5b3f9018767d436ae2b719e9888	no	15
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23	Non Patent Literature	Dauger_Semiclassical_Modeling_Quantum_Mechanical_Mutiparticle_Systems_2001_NVIDIA ACS0166004.pdf	9168115 c49c3c1bc5036ec1c5169388f84de7d9f96fc558	no	291
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24	Non Patent Literature	Dauger_Decyk_Cluster_de_Computo_2006_-_NVIDIA-ACS-0166502.pdf	913065 36cfe07be48e96699e4d2b6363a5c075c9c084af	no	8
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25	Non Patent Literature	Dauger_Supercomputing_Engine_for_Mathematica_Wolfram_2006-_NVIDIA-ACS-0166511.pdf	2932972 143bb434a296ceb8c492860bc61e3145f43c5356	no	20
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26	Non Patent Literature	Decyk_Dauger_Appleseed_parallel_Macintosh_cluster_for_numerically_1999_NVIDIAACS0165956.pdf	28113 e540dbf40aecf466c681c93b4d83fd52e264e54e	no	1
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27	Non Patent Literature	Decyk_AppleSeed_A_Parallel_Macintosh_Cluster_for_Scientific_Computing_2003_-_NVIDIA-ACS-0166369.pdf	1062169 3d47773daa5389953de7eb89e9dced3ec6d7bb5e	no	8
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29	Non Patent Literature	Decyk_Dauger_Kokelaar_Plasma_Physics_1999_NVIDIAACS0165957.pdf	469253 d34c1331eec6ccb8b6c18896ddab8159829636a5	no	10
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32	Non Patent Literature	Edelman_SIAM_Conf_on_Parallel_Processing02-25-2004_NVIDIAACS0234909.pdf	284571 11d0809f99a81439ba16629b31a6c1bed837fb5e	no	3
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37	Non Patent Literature	Dauger_Decyk_Tonge_Semiclassical_Modeling_WWDC_2006_-_NVIDIA-ACS-0166510_.pdf	220573 665660db97dd39934c4b2a8a3c110d78fc91d40f	no	1
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41	Non Patent Literature	Gilbert_-_High-performance_graph_algorithm_-_NVIDIA-ACS-0234912.pdf	208097 11b813a32a4ad7fee35c3df2a608b2d7b6eae327	no	4
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43	Non Patent Literature	Gropp_Installation_Guide_to_mpich_1996_NVIDIA0235131.pdf	1571881 a1c39a3e037e0c353442599b32bd84443f44a4af	no	42
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46	Non Patent Literature	Interactive_Supercomputing_-_Background_-_NVIDIA-ACS-0234916.pdf	106295 2899539264730404f22a1df54d080ab2b8704325	no	2
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47	Non Patent Literature	Interactive_Supercomputing_Delivering_Parallel_Computing_Nov2004_-_NVIDIA-ACS-0234990.pdf	322067 aa70f9ca8733efa619e495a0282df66b9c910f8d	no	15
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48	Non Patent Literature	Interactive_Supercomputing_Delivering_Parallel_Computing_2003_-_NVIDIA-ACS-0235005.pdf	404991 752e018fc0a45909271e3d968d790e5ed4bb2091	no	17
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Warnings:					
Information:					
50	Non Patent Literature	Erez_-_Merrimac_Supercomputing_with_Streams__NVIDIAACS0167081_.pdf	289623 4b0661c3d4c6d9632a797461c7e0c405a70da204	no	1
Warnings:					
Information:					
51	Request for Continued Examination (RCE)	ZTANN-002P1C7_RCE.pdf	1667138 390b1a29685c8af65bb2e91cc74375726b57628a	no	3
Warnings:					
Information:					
52		ZTANN-002P1C7_IDS.pdf	129616 adec2da572b5281693ad5d0b48258552f7b01192	yes	13
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	2	
	Information Disclosure Statement (IDS) Form (SB08)		3	13	
Warnings:					
Information:					
53	Fee Worksheet (SB06)	fee-info.pdf	37894 874780c801535dbf8d46574ef98235ec1d671657	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			100762128		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	17374789	Filing Date	2021-07-13	Docket Number (if applicable)	ZTANN.002P1C7	Art Unit	2449
First Named Inventor	Zvi Tannenbaum			Examiner Name	Hermon Asres		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 111410

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

PTO/SB/30EFS (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Jordan M. Cox/	Date (YYYY-MM-DD)	2022-07-07
Name	Jordan M. Cox	Registration Number	70,875

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

INFORMATION DISCLOSURE STATEMENT

First Inventor: Tannenbaum, Zvi	**Conf. No.:** 1893
App. No.: 17/374789	**Filed:** July 13, 2021
Examiner: Asres, Hermon	**Art Unit:** 2449
Title: CLUSTER COMPUTING	

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

References and Listing

Pursuant to 37 CFR 1.56, an Information Disclosure Statement listing references is provided herewith. Copies of any listed foreign and non-patent literature references are being submitted.

As previously noted, Advanced Cluster Systems, Inc. ("ACS") filed suit against NVIDIA Corporation ("NVIDIA") in the U.S. District Court for the District of Delaware (Case No. 1:19-cv-02032-UNA) on October 28, 2019, alleging infringement of various issued patents, including U.S. Patent Nos. 8,082,289, 8,140,612, 8,676,877, and 10,333,768. Recently, certain documents were received by ACS from NVIDIA during discovery. These documents are hereby disclosed, adding to other documents previously disclosed from the litigation. The litigation is ongoing.

Pursuant to 37 CFR 1.97(g) and (h), Applicant makes no representation that the information is considered to be material to patentability. Additionally, inclusion on this list is not an admission that any of the cited documents are prior art in this application. Further, Applicant makes no representation regarding the completeness of this list, or that better art does not exist.

No Disclaimers

To the extent that anything in the Information Disclosure Statement or the listed references could be construed as a disclaimer of any subject matter supported by the present application, Applicant hereby rescinds and retracts such disclaimer.

Timing of Disclosure

This Information Disclosure Statement is being filed with an RCE and no fee is believed to be required.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: July 7, 2022

By: /Jordan M. Cox/
Jordan M. Cox
Registration No. 70,875
Registered Practitioner
(949) 760-0404

55893603

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

20995 7590 04/08/2022

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
ASRES, HERMON	
ART UNIT	PAPER NUMBER
2449	

DATE MAILED: 04/08/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/374,789	07/13/2021	Zvi Tannenbaum	ZTANN.002P1C7	1893

TITLE OF INVENTION: CLUSTER COMPUTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	07/08/2022

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20995 7590 04/08/2022
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/374,789	07/13/2021	Zvi Tannenbaum	ZTANN.002P1C7	1893

TITLE OF INVENTION: CLUSTER COMPUTING

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	07/08/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
ASRES, HERMON	2449	709-223000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/374,789	07/13/2021	Zvi Tannenbaum	ZTANN.002P1C7	1893

20995 7590 04/08/2022

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
ASRES, HERMON	

ART UNIT	PAPER NUMBER
2449	

DATE MAILED: 04/08/2022

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/374,789	Applicant(s) Tannenbaum et al.	
	Examiner HERMON ASRES	Art Unit 2449	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 02/18/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 2-31 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☑ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HERMON ASRES/
Primary Examiner, Art Unit 2449

DETAILED ACTION

REASONS FOR ALLOWANCE

Claims 2-31 are allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance:

In interpreting the claims, in light of the specification the Examiner finds the claimed invention to be patentably distinct from the prior art of record.

Block et al. (2005/0021751) teaches an apparatus, program product and method utilize cluster data port services within a cluster infrastructure to provide reliable and efficient communications between nodes in a clustered computer system. The cluster data port services present an abstracted transport service that encapsulates and manages the establishment of multiple connection paths between a source node, a target node and one or more backup nodes in such a manner that a cluster data port is effectively utilized as single data port from the perspective of a user program. **(See Abstract).**

Fought et al. (6,074,427) teaches a system and method for simulating multiple clusters of independent computer nodes in a single machine. A cluster contains one or more computer nodes interconnected by a communications link. A user can simulate a cluster of n nodes by generating n user-level procedures where each user-level procedure represents the

kernel of a respective node. An additional mechanism is provided which allows a user to exercise the operation of any intended function in any of the nodes in any of the clusters. **(See Abstract).**

Singh (8,601,101) teaches a system and method for each node in a cluster including a peer-to-peer communication channel compiling and maintaining its own cluster membership are disclosed. In one embodiment, each cluster node may be coupled to every other node and commonly-accessible storage through a network. When a node starts up and attempts to join the cluster, it may access cluster information data stored in the commonly-accessible storage. This information may include a list of all nodes that are potential cluster members. Based on the cluster membership information, the joining node may request a peer-to-peer connection with each potential cluster member. When such a request results in establishment of a connection, the joining node may add the name of the target node to its cluster membership list. Likewise, when a member node grants a connection to a node, it may add the joining node to its cluster membership list. **(See Abstract).**

However, the prior art of records fail to teach or suggest individually or in combination as set forth in independent claims 2 filed on 08/04/2021. Claims 3-31 are also allowed for the same reasons.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submission should clearly labeled “Comments on statement of Reason for Allowance”.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HERMON ASRES whose telephone number is (571)272-4257. The examiner can normally be reached Monday to Friday 9AM to 5PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Vivek Srivastava can be reached on (571)272-7304. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HERMON ASRES/
Primary Examiner, Art Unit 2449

Notice of References Cited	Application/Control No. 17/374,789	Applicant(s)/Patent Under Reexamination Tannenbaum et al.	
	Examiner HERMON ASRES	Art Unit 2449	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20050021751-A1	01-2005	Block, Timothy Roy	H04L67/1008	714/E11.073
*	B	US-20070073705-A1	03-2007	Gray; Theodore W.	G06F9/451	1/1
*	C	US-8601101-B1	12-2013	Singh; Servesh Pratap	H04L69/40	370/254
*	D	US-6968359-B1	11-2005	Miller; Robert	G06F9/5061	709/205
*	E	US-20070094532-A1	04-2007	SENGUPTA; Sabyasachi	G06F11/3632	714/E11.207
*	F	US-20030195938-A1	10-2003	Howard, Kevin David	G06F15/163	709/208
	G					
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/374,789	Tannenbaum et al.
	Examiner	**Art Unit**
	HERMON ASRES	2449

CPC							
Symbol						**Type**	**Version**
H04L	/	41	/	04		F	2013-01-01
G06F	/	9	/	5072		I	2013-01-01
G06F	/	9	/	54		I	2013-01-01
G06F	/	15	/	76		I	2013-01-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	30	
/HERMON ASRES/ Primary Examiner, Art Unit 2449	25 March 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No.: 20220325

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	Examiner	**Art Unit**
	HERMON ASRES	2449

INTERNATIONAL CLASSIFICATION					
CLAIMED					
H04L12/24	/	12	/	24	
G06F9/50	/	9	/	50	
G06F9/54	/	9	/	54	
G06F15/76	/	15	/	76	

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
709	223

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	30	
/HERMON ASRES/ Primary Examiner, Art Unit 2449	25 March 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office — Part of Paper No.: 20220325

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☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	2	10	11	19	20	28	29								
2	3	11	12	20	21	29	30								
3	4	12	13	21	22	30	31								
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6	7	15	16	24	25										
7	8	16	17	25	26										
8	9	17	18	26	27										
9	10	18	19	27	28										

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	30	
/HERMON ASRES/ Primary Examiner, Art Unit 2449	25 March 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office Part of Paper No.: 20220325

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/374,789	Tannenbaum et al.
	Examiner	**Art Unit**
	HERMON ASRES	2449

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/20/2021	03/25/2022							
	2	=	=							
	3	=	=							
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/374,789	Tannenbaum et al.
	Examiner	**Art Unit**
	HERMON ASRES	2449

CLAIM		DATE								
Final	Original	11/20/2021	03/25/2022							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/374,789	Tannenbaum et al.
	Examiner	Art Unit
	HERMON ASRES	2449

CPC - Searched*		
Symbol	Date	Examiner

CPC Combination Sets - Searched*		
Symbol	Date	Examiner
H04L41/0213, H04L29/08072, H04L29/06, H04L41/22, H04L41/12	11/20/2021	HA
H04L41/0213, H04L29/08072, H04L29/06, H04L41/22, H04L41/12	03/25/2022	HA

US Classification - Searched*			
Class	Subclass	Date	Examiner
709	223	11/20/2021	HA

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Searched East (US Patents, USPGPubs, EPO, JPO, Derwent, IBM)	11/20/2021	HA
See East search attached	11/20/2021	HA
Inventor search performed	11/20/2021	HA
Key word search performed in NPL (ip.com and google scholar)	11/20/2021	HA
Interference search performed	11/20/2021	HA
IPR2020-01608ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo8,082,289	11/20/2021	HA
IPR2021-00019ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo.10,333,768	11/20/2021	HA

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/374,789	Tannenbaum et al.
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	HERMON ASRES	2449

IPR2021-00020ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo.10,333,768	11/20/2021	HA
IPR2021-00075ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo8,140,612	11/20/2021	HA
IPR2021-00108ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo8,676,877	11/20/2021	HA
Search updated	03/25/2022	HA
Key word search performed in NPL (ip.com and google scholar)	03/25/2022	HA
IPR2020-01608ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo8,082,289	03/25/2022	HA
IPR2021-00019ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo.10,333,768	03/25/2022	HA
IPR2021-00020ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo.10,333,768	03/25/2022	HA
IPR2021-00075ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo8,140,612	03/25/2022	HA
IPR2021-00108ReviewedforPetitionforInterPartiesReviewofU.S.PatentNo8,676,877	03/25/2022	HA

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
709	223	11/20/2021	HA

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT		
	Application No.	17/374789
	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
(Multiple sheets used when necessary)	Examiner	Asres, Hermon
SHEET 1 OF 12	Attorney Docket No.	ZTANN.002PIC7

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number *Number - Kind Code (if known)* Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	7,542,981	06-02-2009	Choy et al.	
	2	7,627,744	12-01-2009	Maher et al.	
	3	2005/0251644	11-10-2005	Maher et al.	

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Examiner Initials	Cite No.	Foreign Patent Document *Country Code-Number-Kind Code* Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T[1]
	4	WO 2006/050404	05-11-2006	Interactive Supercomputing, Inc.		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	5	"128-Xserve G5 CLUSTER ACHIEVES 1.21 TeraFlop", January 14, 2005, https://www.hpcwire.com/2005/01/14/128-xserve-g5-cluster-achieves-1-21-teraflop/, pp. 2. [NVIDIA-ACS-0239003 - NVIDIA-ACS-0239004]	
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Examiner Signature /HERMON ASRES/	Date Considered 03/25/2022
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.A./

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	17/374789
	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
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SHEET 2 OF 12	Attorney Docket No.	ZTANN.002PIC7

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	15	"Compute Cluster Job Aids", Windows Server 2003 Deployment Kit, 2003, pp. 80. [NVIDIA-ACS-0238212 - NVIDIA-ACS-0238291]	
	16	"Compute Cluster Server: Getting Started", 2006, pp. 1. [NVIDIA-ACS-0238300]	
	17	"Compute Cluster Server Glossary", December 5, 2005, pp. 6. [NVIDIA-ACS-0238292 - NVIDIA-ACS-0238297]	
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	20	COTRONIS et al., "Recent Advances in Parallel Virtual Machine and Message Passing Interface", 8th European PVM/MPI Users' Group Meeting, Santorini/Thera, Greece, September 2001, Proceedings, pp. 456. [NVIDIA-ACS-0170449 - NVIDIA-ACS-0170904] (in 2 parts)	
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Examiner Signature /HERMON ASRES/	Date Considered 03/25/2022

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] - Place a check mark in this area when an English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.A./

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	17/374789
	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
(Multiple sheets used when necessary)	Examiner	Asres, Hermon
SHEET 3 OF 12	Attorney Docket No.	ZTANN.002PIC7

NON PATENT LITERATURE DOCUMENTS			
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	35	Dauger Research, "Parallel Zoology", Dauger Research Vault, 2006, pp. 7. [NVIDIA-ACS-0237202 - NVIDIA-ACS-0237208]	
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	128	**Defendant NVIDIA Corporation's Invalidity Contentions** in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 215 pages.	
	129	**Exhibit A-1 - PVMaple System**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 211 pages.	
	130	**Exhibit A-2 - Distributed Maple System**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 171 pages.	
	131	**Exhibit A-3 - Matlab*P System**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 246 pages.	
	132	**Exhibit A-4 - FFTW**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 467 pages.	
	133	**Exhibit A-5 - Intel Paragon Maple System**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 137 pages.	
	134	**Exhibit A-6 - Stony Brook**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 268 pages.	
	135	**Exhibit A-7 - AppleSeed Pooch System**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 127 pages.	
	136	**Exhibit A-9 - PVMaple References**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 211 pages.	
	137	**Exhibit A-10 - Distributed Maple References**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 170 pages.	

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	138	**Exhibit A-11 - Matlab *P References**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 242 pages.	
	139	**Exhibit A-12 - FFTW References**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 467 pages.	
	140	**Exhibit A-13 - Intel Paragon Maple References**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 137 pages.	
	141	**Exhibit A-14 - Stony Brook Reference**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 268 pages.	
	142	**Exhibit A-15 - AppleSeed Pooch References**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 127 pages.	
	143	**Exhibit B-1 - PVMaple System**, U.S. Patent No. 8,082,289, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 167 pages.	
	144	**Exhibit B-2 - Distributed Maple System**, U.S. Patent No. 8,082,289, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 90 pages.	
	145	**Exhibit B-3 - Matlab*P System**, U.S. Patent No. 8,082,289, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 296 pages.	
	146	**Exhibit B-4 - FFTW**, U.S. Patent No. 8,082,289, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 178 pages.	
	147	**Exhibit B-5 - Intel Paragon Maple System**, U.S. Patent No. 8,082,289, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 128 pages.	
	148	**Exhibit B-6 - Stony Brook**, U.S. Patent No. 8,082,289, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 120 pages.	
	149	**Exhibit B-7 - AppleSeed Pooch System**, U.S. Patent No. 8,082,289, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 194 pages.	
	150	**Exhibit B-9 - PVMaple References**, U.S. Patent No. 8,082,289, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 167 pages.	
	151	**Exhibit B-10 - Distributed Maple References**, U.S. Patent No. 8,082,289, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 91 pages.	
	152	**Exhibit B-11 - Matlab *P References**, U.S. Patent No. 8,082,289, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 296 pages.	

Examiner Signature /HERMON ASRES/	Date Considered 03/25/2022

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[1] - Place a check mark in this area when an English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.A./

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	17/374789
	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
(Multiple sheets used when necessary)	Examiner	Asres, Hermon
SHEET 10 OF 12	Attorney Docket No.	ZTANN.002PIC7

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	153	**Exhibit B-12 - FFTW References**, U.S. Patent No. 8,082,289, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 178 pages.	
	154	**Exhibit B-13 - Intel Paragon Maple References**, U.S. Patent No. 8,082,289, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 128 pages.	
	155	**Exhibit B-14 - Stony Brook Reference**, U.S. Patent No. 8,082,289, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 120 pages.	
	156	**Exhibit B-15 - AppleSeed Pooch References**, U.S. Patent No. 8,082,289, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 189 pages.	
	157	**Exhibit C-1 - PVMaple System**, U.S. Patent No. 8,140,612, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 83 pages.	
	158	**Exhibit C-2 - Distributed Maple System**, U.S. Patent No. 8,140,612, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 54 pages.	
	159	**Exhibit C-3 - Matlab*P System**, U.S. Patent No. 8,140,612, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 122 pages.	
	160	**Exhibit C-4 - FFTW**, U.S. Patent No. 8,140,612, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 102 pages.	
	161	**Exhibit C-5 - Intel Paragon Maple System**, U.S. Patent No. 8,140,612, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 43 pages.	
	162	**Exhibit C-6 - Stony Brook**, U.S. Patent No. 8,140,612, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 81 pages.	
	163	**Exhibit C-7 - AppleSeed Pooch System**, U.S. Patent No. 8,140,612, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 64 pages.	
	164	**Exhibit C-9 - PVMaple References**, U.S. Patent No. 8,140,612, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 83 pages.	
	165	**Exhibit C-10 - Distributed Maple References**, U.S. Patent No. 8,140,612, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 54 pages.	
	166	**Exhibit C-11 - Matlab *P References**, U.S. Patent No. 8,140,612, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 122 pages.	
	167	**Exhibit C-12 - FFTW References**, U.S. Patent No. 8,140,612, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 102 pages.	

Examiner Signature /HERMON ASRES/	Date Considered 03/25/2022
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PTO/SB/08 Equivalent

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	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
(Multiple sheets used when necessary)	Examiner	Asres, Hermon
SHEET 11 OF 12	Attorney Docket No.	ZTANN.002PIC7

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	168	**Exhibit C-13 - Intel Paragon Maple References**, U.S. Patent No. 8,140,612, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 43 pages.	
	169	**Exhibit C-14 - Stony Brook Reference**, U.S. Patent No. 8,140,612, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 81 pages.	
	170	**Exhibit C-15 - AppleSeed Pooch References**, U.S. Patent No. 8,140,612, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 64 pages.	
	171	**Exhibit D-1 - PVMaple System**, U.S. Patent No. 8,676,877, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 75 pages.	
	172	**Exhibit D-2 - Distributed Maple System**, U.S. Patent No. 8,676,877, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 61 pages.	
	173	**Exhibit D-3 - Matlab*P System**, U.S. Patent No. 8,676,877, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 129 pages.	
	174	**Exhibit D-4 - FFTW**, U.S. Patent No. 8,676,877, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 155 pages.	
	175	**Exhibit D-5 - Intel Paragon Maple System**, U.S. Patent No. 8,676,877, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 36 pages.	
	176	**Exhibit D-6 - Stony Brook**, U.S. Patent No. 8,676,877, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 97 pages.	
	177	**Exhibit D-7 - AppleSeed Pooch System**, U.S. Patent No. 8,676,877, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 73 pages.	
	178	**Exhibit D-9 - PVMaple References**, U.S. Patent No. 8,676,877, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 75 pages.	
	179	**Exhibit D-10 - Distributed Maple References**, U.S. Patent No. 8,676,877, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 63 pages.	
	180	**Exhibit D-11 - Matlab *P References**, U.S. Patent No. 8,676,877, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 129 pages.	
	181	**Exhibit D-12 - FFTW References**, U.S. Patent No. 8,676,877, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 155 pages.	
	182	**Exhibit D-13 - Intel Paragon Maple References**, U.S. Patent No. 8,676,877, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 36 pages.	

Examiner Signature	/HERMON ASRES/	Date Considered	03/25/2022

*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] - Place a check mark in this area when an English language Translation is attached.

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PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	17/374789
	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
(Multiple sheets used when necessary)	Examiner	Asres, Hermon
SHEET 12 OF 12	Attorney Docket No.	ZTANN.002PIC7

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	183	**Exhibit D-14 - Stony Brook Reference**, U.S. Patent No. 8,676,877, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 97 pages.	
	184	**Exhibit D-15 - AppleSeed Pooch References**, U.S. Patent No. 8,676,877, as listed in Defendant NVIDIA Corporation's Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated October 5, 2019 in 73 pages. ***[Incorrectly labeled in upper right hand corner of document as Ex. D-7]***	

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Examiner Signature /HERMON ASRES/	Date Considered 03/25/2022
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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
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L44	11	mathematica near5 kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/08 06:39 PM
L45	13	mathematica with kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/08 06:40 PM
L46	10	("8402080").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/08 06:43 PM
L47	2	("8849889").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/08 06:44 PM
L48	101	("20020049859"|"20030005266"|"20030051062"|"20030135621"|"20030195931"|"20030195938"|"20040110209"|"20040157203"|"20040252710"|"20050021751"|"20050038852"|"20050060237"|"20050076105"|"20050108394"|"20050180095"|"20060053216"|"20060106931"|"20070044099"|"20070073705"|"20080250347"|"20080281997"|"5423046"|"5881315"|"5930768"|"6108699"|"6202080"|"6546403"|"6578068"|"6751698"|"6782537"|"6968335"|"7093004"|"7136924"|"7174381"|"7249357"|"7334232"|"7437460"|"7472193"|"7554949"|"7937455"|"8082289"|"8140612"|"8402083"|"8676877").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/08 06:44 PM
L49	17	mathematica with cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/08 06:50 PM
L50	43	mathematica same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/08 06:51 PM
L51	537678	stephen wolfram mathematica kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/08 07:42 PM
L52	50	(stephen near2 wolfram).in.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/08 07:42 PM
L53	1	L52 and mathematica and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/08 07:43 PM
L54	215	mathematica and kernel	(US-PGPUB; USPAT; EPO; JPO;	OR	OFF	OFF	2016/07/08 07:43 PM

			DERWENT; IBM_TDB)				
L55	74	L54 and cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/08 07:43 PM
L56	13	mathematica with kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/08 07:44 PM
L57	0	("gridMathematica").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/09 10:16 AM
L58	0	("gridwithMathematica").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/09 10:16 AM
L59	19	grid with Mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/09 10:16 AM
L60	20	gridMathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/09 10:16 AM
L61	14	gridMathematica and wolfram	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/09 10:21 AM
L62	20	gridMathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/09 10:22 AM
L63	2578	Mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/09 10:22 AM
L64	215	Mathematica and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/09 10:22 AM
L65	15749	wolfram	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/09 10:29 AM
L66	8450	wolfram.in.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/09 10:29 AM
L67	15	L66 and mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/09 10:30 AM
L68	42	L66 and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2016/07/09 10:30 AM
L69	2	("20070073705").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/09 10:44 AM
L70	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/07/09 10:46 AM
L71	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2016/11/07 01:23 PM

L72	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/03/01 07:24 PM
L73	0	("(computerwithnodeswithclister)same(peer-to-peer)and@ad<20060101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/03/01 07:47 PM
L74	0	(computer with nodes with clister) same (peer-to-peer) and @ad<"20060101"	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2017/03/01 07:47 PM
L75	3	(computer with nodes with cluster) same (peer-to-peer) and @ad<"20060101"	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2017/03/01 07:48 PM
L76	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/03/02 05:12 PM
L77	12	("8601101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2017/03/02 05:12 PM
L78	44	(computer with cluster) and kernel and (mathematical with expression)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/18 10:39 PM
L79	0	(computer with clusters) same kernel same mathematical	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/18 10:47 PM
L80	30	(computer with clusters) and kernel same mathematical	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/18 10:47 PM
L81	9	(computer with clusters) same kernel same mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/18 10:48 PM
L82	95	(computer with clusters) same mathematical	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/18 10:50 PM
L83	2	(computer with clusters) same mathematical same expressions	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/18 10:50 PM
L84	0	cluster near5 mathematical near5 evaluate	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/19 11:19 AM
L85	2	cluster with mathematical with evaluate	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/19 11:20 AM
L86	2	("20050038852").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/19 11:22 AM
L87	20	("20050021751"|"20070073705"|"20070094532"|"6968359"|"8601101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/19 11:35 AM

L88	70	(US-0005068-$ | US-0015460-$ | US-0026601-$ | US-0059473-$ | US-0097300-$ | US-0098447-$ | US-0124363-$ | US-0154789-$ | US-0188088-$ | US-0254984-$ | US-1234567-$ | US-1368948-$ | US-20030005068-$ | US-20040098447-$ | US-20040254984-$ | US-20050015460-$ | US-20050026601-$ | US-20050097300-$ | US-20050154789-$ | US-20050188088-$ | US-20060059473-$ | US-20070124363-$ | US-25376674-$ | US-5195580-$ | US-6006259-$ | US-6067609-$ | US-6604134-$ | US-7031944-$ | US-7177874-$ | US-7315877-$ | US-7502915-$ | US-7519652-$ | US-7533141-$ | US-7533389-$ | US-7568131-$ | US-7598390-$ | US-7644130-$ | US-7757236-$ | US-7788314-$ | US-7835022-$ | US-8117288-$ | US-9405564-$).DID.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/19 11:36 AM
L89	4802	(computer with cluster with nodes)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/19 11:49 AM
L90	30	(computer with cluster with nodes) same (mathematica$)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/19 11:50 AM
L91	12	(computer with cluster with nodes) same (mathematica$) and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/19 11:50 AM
L92	230	(computer with cluster) same (mathematica$)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/19 11:51 AM
L93	28	(computer with cluster)	(US-PGPUB; USPAT;	OR	OFF	OFF	2018/02/19

		same (mathematica$) and kernel	EPO; JPO; DERWENT; IBM_TDB)				11:52 AM
L94	230	(computer with cluster) same (mathematica$)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/19 11:54 AM
L95	17	(computer with cluster) same (mathematica$) same result$3	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/19 11:55 AM
L96	8	(computer with cluster) same (mathematica$ with expression)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/19 11:56 AM
L97	15	(high with performance) same cluster same (mathematics mathematica)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/19 12:07 PM
L98	114	(high with performance) same cluster and (mathematics mathematica)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/02/19 12:08 PM
L99	2	("7418470").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/19 12:12 PM
L100	2	("20030195938").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/19 12:13 PM
L101	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/19 12:42 PM
L102	12	("8601101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/19 12:42 PM
L103	2	("20030195938").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/19 12:42 PM
L104	2	("20030195938").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2018/02/19 01:24 PM
L105	2	("2003195938").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/11/22 12:31 PM
L106	6	("2004015968").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/11/22 12:32 PM
L107	5	("2004098359").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/11/22 12:32 PM
L108	6	("2004098447").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2018/11/22 12:32 PM
L123	2	("7139882").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2019/02/05 01:35 PM

L124	3	("20050021751").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2020/12/30 12:43 PM
L125	2	("20050235055").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2020/12/30 01:01 PM
L126	196	(US-0005068-$ | US-0005266-$ | US-0015460-$ | US-0021751-$ | US-0026601-$ | US-0038852-$ | US-0044099-$ | US-0049859-$ | US-0051062-$ | US-0053216-$ | US-0059473-$ | US-0060237-$ | US-0073705-$ | US-0076105-$ | US-0094532-$ | US-0097300-$ | US-0098447-$ | US-0106931-$ | US-0108394-$ | US-0110209-$ | US-0124363-$ | US-0135621-$ | US-0154789-$ | US-0157203-$ | US-0180095-$ | US-0188088-$ | US-0195572-$ | US-0195931-$ | US-0195938-$ | US-0250347-$ | US-0252710-$ | US-0254984-$ | US-0281997-$ | US-1234567-$ | US-10333768-$ | US-1368948-$ | US-17207443-$ | US-20020049859-$ | US-20030005068-$ | US-20030005266-$ | US-20030051062-$ | US-20030135621-$ | US-20030195931-$ | US-20030195938-$ | US-20040098447-$ | US-20040110209-$ | US-20040157203-$ | US-20040195572-$ | US-20040252710-$ | US-20040254984-$ | US-20050015460-$ | US-	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2020/12/30 01:03 PM

		20050021751-$ | US- 20050038852-$ | US- 20050060237-$ | US- 20050076105-$ | US- 20050097300-$ | US- 20050108394-$ | US- 20050154789-$ | US- 20050180095-$ | US- 20050188088-$ | US- 20060026601-$ | US- 20060053216-$ | US- 20060059473-$ | US- 20060106931-$ | US- 20070044099-$ | US- 20070073705-$ | US- 20070094532-$ | US- 20070124363-$ | US- 20080250347-$ | US- 20080281997-$ | US- 31357476-$ | US- 5423046-$ | US- 5881315-$ | US- 5930768-$ | US- 6006259-$ | US- 6067609-$ | US- 6108699-$ | US- 6195680-$ | US- 6202080-$ | US- 6546403-$ | US- 6578068-$ | US- 6604134-$ | US- 6751698-$ | US- 6782537-$ | US- 6968335-$ | US- 6968359-$ | US- 7031944-$ | US- 7093004-$ | US- 7136924-$ | US- 7139882-$ | US- 7174381-$ | US- 7177874-$ | US- 7249357-$ | US- 7315877-$ | US- 7334232-$ | US- 7437460-$ | US- 7472193-$ | US- 7502915-$ | US- 7519652-$ | US- 7533141-$ | US- 7533389-$ | US- 7554949-$ | US- 7568131-$ | US- 7644130-$ | US- 7698390-$ | US- 7716323-$ | US- 7757236-$ | US- 7788314-$ | US- 7835022-$ | US-					

		7937455-$ | US-8082289-$ | US-8117288-$ | US-8140612-$ | US-8402080-$ | US-8402083-$ | US-8601101-$ | US-8676877-$ | US-8849889-$ | US-9405564-$).DID.					
L127	2	("8676877").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2021/01/01 03:35 PM
L128	7	community near5 managed near5 RAN	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2021/01/01 11:00 PM
L129	33851	709/223.ccls.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2021/11/20 08:40 AM
L130	214	(US-0005068-$ | US-0005266-$ | US-0015460-$ | US-0015968-$ | US-0021751-$ | US-0026601-$ | US-0038852-$ | US-0044099-$ | US-0049859-$ | US-0051062-$ | US-0053216-$ | US-0059473-$ | US-0060237-$ | US-0073705-$ | US-0076105-$ | US-0094532-$ | US-0097300-$ | US-0098359-$ | US-0098447-$ | US-0106931-$ | US-0108394-$ | US-0110209-$ | US-0124363-$ | US-0135621-$ | US-0153677-$ | US-0154789-$ | US-0157203-$ | US-0180095-$ | US-0188088-$ | US-0195572-$ | US-0195931-$ | US-0195938-$ | US-0235055-$ | US-0250347-$ | US-0252710-$ | US-0254984-$ | US-0281997-$ | US-1234567-$ | US-	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2021/11/20 08:44 AM

		10333768-$ | US- 17207443-$ | US- 20020049859-$ | US- 20030005068-$ | US- 20030005266-$ | US- 20030051062-$ | US- 20030135621-$ | US- 20030195931-$ | US- 20030195938-$ | US- 20040015968-$ | US- 20040098359-$ | US- 20040098447-$ | US- 20040110209-$ | US- 20040157203-$ | US- 20040195572-$ | US- 20040252710-$ | US- 20040254984-$ | US- 20050015460-$ | US- 20050021751-$ | US- 20050038852-$ | US- 20050060237-$ | US- 20050076105-$ | US- 20050097300-$ | US- 20050108394-$ | US- 20050154789-$ | US- 20050180095-$ | US- 20050188088-$ | US- 20050235055-$ | US- 20060026601-$ | US- 20060053216-$ | US- 20060059473-$ | US- 20060106931-$ | US- 20070044099-$ | US- 20070073705-$ | US- 20070094532-$ | US- 20070124363-$ | US- 20080250347-$ | US- 20080281997-$ | US- 20200153677-$ | US- 5423046-$ | US- 5881315-$ | US- 5930768-$ | US- 53865456-$ | US- 6006259-$ | US- 6067609-$ | US- 6074427-$ | US- 6108699-$ | US- 6195680-$ | US- 6202080-$ | US- 6546403-$ | US- 6578068-$ | US- 6604134-$ | US- 6691216-$ | US- 6751698-$ | US- 6782537-$ | US- 6968335-$ | US- 6968359-$ | US- 7031944-$ | US-					

		7093004-$ | US-7136924-$ | US-7139882-$ | US-7174381-$ | US-7177874-$ | US-7249357-$ | US-7315877-$ | US-7334232-$ | US-7437460-$ | US-7472193-$ | US-7502915-$ | US-7519652-$ | US-7533141-$ | US-7533168-$ | US-7533389-$ | US-7554949-$ | US-7568131-$ | US-7634530-$ | US-7644130-$ | US-7698390-$ | US-7716323-$ | US-7757236-$ | US-7788314-$ | US-7835022-$ | US-7937455-$ | US-8082289-$ | US-8117288-$ | US-8140612-$ | US-8402080-$ | US-8402083-$ | US-8601101-$ | US-8676877-$ | US-8849889-$ | US-9405564-$).DID.					
L131	8	((Zvi) near2 (Tannenbaum)).INV.	(USPAT)	OR	OFF	OFF	2022/03/25 12:54 PM
L132	9	((Dean) near2 (Dauger)).INV.	(USPAT)	OR	OFF	OFF	2022/03/25 12:54 PM
L133	236	(computer with cluster) same nodes same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L134	35	L3 and interpret	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L135	39589	709/223.ccls.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L136	10778	H04L41/0213.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L137	3095	H04L29/08072.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L138	52733	H04L29/06.cpc.	(US-PGPUB; USPAT; EPO; JPO;	OR	OFF	OFF	2022/03/25 12:54 PM

			DERWENT; IBM_TDB)				
L139	21038	H04L41/22.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L140	30044	H04L41/12.cpc.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L141	0	L3 and L6	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L142	0	L3 and L7	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L143	15	L3 and L8	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L144	0	L3 and L9	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L145	2	L3 and L10	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L146	109	("20020049859"|"20030005266"|"20030051062"|"20030135621"|"20030195931"|"20030195938"|"20040110209"|"20040157203"|"20040252710"|"20050021751"|"20050038852"|"20050060237"|"20050076105"|"20050108394"|"20050180095"|"20060053216"|"20060106931"|"20070044099"|"20070073705"|"20080250347"|"20080281997"|"5423046"|"5881315"|"5930768"|"6108699"|"6202080"|"6546403"|"6578068"|"6751698"|"6782537"|"6968335"|"7093004"|"7136924"|"7174381"|"7249357"|"7334232"|"7437460"|"7472193"|"7554949"|"7937455"|"8082289"|"8140612"|"8402083"|"8676877").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L147	236	(computer with cluster) same nodes same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L148	16	(computer with cluster) same nodes same kernel and mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM

L149	236	(computer with cluster) same nodes same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L150	11	("8402080").PN.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L151	2	("8849889").PN.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L152	92	US-1234567-$.DID. OR US-5423046-$.DID. OR US-5881315-$.DID. OR US-5930768-$.DID. OR US-6108699-$.DID. OR US-6202080-$.DID. OR US-6546403-$.DID. OR US-6578068-$.DID. OR US-6751698-$.DID. OR US-6782537-$.DID. OR US-6968335-$.DID. OR US-7093004-$.DID. OR US-7136924-$.DID. OR US-7174381-$.DID. OR US-7249357-$.DID. OR US-7334232-$.DID. OR US-7437460-$.DID. OR US-7472193-$.DID. OR US-7554949-$.DID. OR US-7937455-$.DID. OR US-8082289-$.DID. OR US-8140612-$.DID. OR US-8402083-$.DID. OR US-8676877-$.DID. OR US-20020049859-$.DID. OR US-20030005266-$.DID. OR US-20030051062-$.DID. OR US-20030135621-$.DID. OR US-20030195931-$.DID. OR US-20030195938-$.DID. OR US-20040110209-$.DID. OR US-20040157203-$.DID. OR US-20040252710-$.DID. OR US-20050021751-$.DID. OR US-20050038852-$.DID. OR US-20050060237-$.DID. OR US-20050076105-$.DID. OR US-20050108394-$.DID. OR US-20050180095-$.DID. OR US-20060053216-$.DID.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM

		OR US-20060106931-$.DID. OR US-20070044099-$.DID. OR US-20070073705-$.DID. OR US-20080250347-$.DID. OR US-20080281997-$.DID. OR JP-1234567-$.DID. OR JP-0887473-$.DID. OR JP-2002117010-$.DID. OR US-6131999-$.DID.					
L153	6	(computer with cluster) same (nodes) same (single-node with kernel)	(USPAT)	OR	OFF	OFF	2022/03/25 12:54 PM
L154	18	(computer with cluster) same (nodes) same (single-node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L155	18	(computer with cluster) same (nodes) and (single-node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L156	18	(computer with cluster) and (nodes) and (single-node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L157	581	(computer with cluster) and (nodes) and (single with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L158	284	(computer with cluster) same (nodes) and (single with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L159	6	(computer with cluster) same (nodes) and (single with kernel) and 709/223.ccls.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L160	22	(computer with cluster) same (single with node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L161	273	(computer with cluster) and (single with node with kernel)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L162	2	("8676877").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L163	2	("8676877").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L164	3909	(computer with cluster) and kernel and nodes and request	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L165	686	L34 and mathematical	(US-PGPUB; USPAT;	OR	OFF	OFF	2022/03/25

			EPO; JPO; DERWENT; IBM_TDB)				12:54 PM
L166	350836	L34 and mathematical smae kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L167	52	L34 and mathematical same kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L168	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L169	50	(single with node with kernel) same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L170	50	(mathematical with kernel) same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L171	50	(mathematical with kernel) same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L172	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L173	354123	mathematica kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L174	19	mathematica near5 kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L175	23	mathematica with kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L176	11	("8402080").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L177	2	("8849889").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L178	109	("20020049859"|"20030005266"|"20030051062"|"20030135621"|"20030195931"|"20030195938"|"20040110209"|"20040157203"|"20040252710"|"20050021751"|"20050038852"|"20050060237"|"20050076105"|"20050108394"|"20050180095"|"20060053216"|"20060106931"|"20070044099"|"20070073705"|"20080250347"|"20080281997"|"5423046"|"5881315"|"5930768"|"610	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM

		8699"|"6202080"|"6546403"|"6578068"|"6751698"|"6782537"|"6968335"|"7093004"|"7136924"|"7174381"|"7249357"|"7334232"|"7437460"|"7472193"|"7554949"|"7937455"|"8082289"|"8140612"|"8402083"|"8676877").PN.				
L179	26	mathematica with cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L180	68	mathematica same cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L181	804620	stephen wolfram mathematica kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L182	103	(stephen near2 wolfram).in.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L183	13	L52 and mathematica and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L184	404	mathematica and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L185	165	L54 and cluster	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L186	23	mathematica with kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L187	0	("gridMathematica").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L188	0	("gridwithMathematica").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L189	26	grid with Mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L190	26	gridMathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L191	20	gridMathematica and wolfram	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L192	26	gridMathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L193	4031	Mathematica	(US-PGPUB; USPAT;	OR	OFF	OFF	2022/03/25

			EPO; JPO; DERWENT; IBM_TDB)				12:54 PM
L194	404	Mathematica and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L195	20445	wolfram	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L196	9640	wolfram.in.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L197	34	L66 and mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L198	91	L66 and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L199	2	("20070073705").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L200	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L201	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L202	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L203	0	("(computerwithnodeswithclister)same(peer-to-peer)and@ad<20060101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L204	0	(computer with nodes with clister) same (peer-to-peer) and @ad<"20060101"	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L205	3	(computer with nodes with cluster) same (peer-to-peer) and @ad<"20060101"	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L206	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L207	13	("8601101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L208	109	(computer with cluster) and kernel and (mathematical with expression)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L209	2	(computer with clusters) same kernel same	(US-PGPUB; USPAT; EPO; JPO;	OR	OFF	OFF	2022/03/25 12:54 PM

		mathematical	DERWENT; IBM_TDB)				
L210	104	(computer with clusters) and kernel same mathematical	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L211	14	(computer with clusters) same kernel same mathematica	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L212	130	(computer with clusters) same mathematical	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L213	5	(computer with clusters) same mathematical same expressions	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L214	1	cluster near5 mathematical near5 evaluate	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L215	6	cluster with mathematical with evaluate	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L216	2	("20050038852").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L217	22	("20050021751"|"20070073705"|"20070094532"|"6968359"|"8601101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L218	70	(US-0005068-$ | US-0015460-$ | US-0026601-$ | US-0059473-$ | US-0097300-$ | US-0098447-$ | US-0124363-$ | US-0154789-$ | US-0188088-$ | US-0254984-$ | US-1234567-$ | US-1368948-$ | US-20030005068-$ | US-20040098447-$ | US-20040254984-$ | US-20050015460-$ | US-20050026601-$ | US-20050097300-$ | US-20050154789-$ | US-20050188088-$ | US-20060059473-$ | US-20070124363-$ | US-25376674-$ | US-5195580-$ | US-6006259-$ | US-6067609-$ | US-6604134-$ | US-7031944-$ | US-7177874-$ | US-	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM

		7315877-$ | US-7502915-$ | US-7519652-$ | US-7533141-$ | US-7533389-$ | US-7568131-$ | US-7598390-$ | US-7644130-$ | US-7757236-$ | US-7788314-$ | US-7835022-$ | US-8117288-$ | US-9405564-$).DID.					
L219	7961	(computer with cluster with nodes)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L220	42	(computer with cluster with nodes) same (mathematica$)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L221	18	(computer with cluster with nodes) same (mathematica$) and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L222	767	(computer with cluster) same (mathematica$)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L223	48	(computer with cluster) same (mathematica$) and kernel	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L224	767	(computer with cluster) same (mathematica$)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L225	30	(computer with cluster) same (mathematica$) same result$3	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L226	17	(computer with cluster) same (mathematica$ with expression)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L227	20	(high with performance) same cluster same (mathematics mathematica)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L228	193	(high with performance) same cluster and (mathematics mathematica)	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L229	2	("7418470").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L230	2	("20030195938").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L231	2	("20050021751").PN.	(US-PGPUB; USPAT; EPO; JPO;	OR	ON	ON	2022/03/25 12:54 PM

			DERWENT; IBM_TDB)				
L232	13	("8601101").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L233	2	("20030195938").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L234	2	("20030195938").PN.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/03/25 12:54 PM
L235	2	("2003195938").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L236	6	("2004015968").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L237	5	("2004098359").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L238	6	("2004098447").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L239	2	("7139882").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L240	3	("20050021751").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L241	2	("20050235055").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L242	196	(US-0005068-$ | US-0005266-$ | US-0015460-$ | US-0021751-$ | US-0026601-$ | US-0038852-$ | US-0044099-$ | US-0049859-$ | US-0051062-$ | US-0053216-$ | US-0059473-$ | US-0060237-$ | US-0073705-$ | US-0076105-$ | US-0094532-$ | US-0097300-$ | US-0098447-$ | US-0106931-$ | US-0108394-$ | US-0110209-$ | US-0124363-$ | US-0135621-$ | US-0154789-$ | US-	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM

		0157203-$ | US- 0180095-$ | US- 0188088-$ | US- 0195572-$ | US- 0195931-$ | US- 0195938-$ | US- 0250347-$ | US- 0252710-$ | US- 0254984-$ | US- 0281997-$ | US- 1234567-$ | US- 10333768-$ | US- 1368948-$ | US- 17207443-$ | US- 20020049859-$ | US- 20030005068-$ | US- 20030005266-$ | US- 20030051062-$ | US- 20030135621-$ | US- 20030195931-$ | US- 20030195938-$ | US- 20040098447-$ | US- 20040110209-$ | US- 20040157203-$ | US- 20040195572-$ | US- 20040252710-$ | US- 20040254984-$ | US- 20050015460-$ | US- 20050021751-$ | US- 20050038852-$ | US- 20050060237-$ | US- 20050076105-$ | US- 20050097300-$ | US- 20050108394-$ | US- 20050154789-$ | US- 20050180095-$ | US- 20050188088-$ | US- 20060026601-$ | US- 20060053216-$ | US- 20060059473-$ | US- 20060106931-$ | US- 20070044099-$ | US- 20070073705-$ | US- 20070094532-$ | US- 20070124363-$ | US- 20080250347-$ | US- 20080281997-$ | US- 31357476-$ | US- 5423046-$ | US- 5881315-$ | US- 5930768-$ | US- 6006259-$ | US- 6067609-$ | US- 6108699-$ | US- 6195680-$ | US- 6202080-$ | US- 6546403-$ | US- 6578068-$ | US-					

		6604134-$ | US- 6751698-$ | US- 6782537-$ | US- 6968335-$ | US- 6968359-$ | US- 7031944-$ | US- 7093004-$ | US- 7136924-$ | US- 7139882-$ | US- 7174381-$ | US- 7177874-$ | US- 7249357-$ | US- 7315877-$ | US- 7334232-$ | US- 7437460-$ | US- 7472193-$ | US- 7502915-$ | US- 7519652-$ | US- 7533141-$ | US- 7533389-$ | US- 7554949-$ | US- 7568131-$ | US- 7644130-$ | US- 7698390-$ | US- 7716323-$ | US- 7757236-$ | US- 7788314-$ | US- 7835022-$ | US- 7937455-$ | US- 8082289-$ | US- 8117288-$ | US- 8140612-$ | US- 8402080-$ | US- 8402083-$ | US- 8601101-$ | US- 8676877-$ | US- 8849889-$ | US- 9405564-$).DID.					
L243	2	("8676877").PN.	(US-PGPUB; USPAT; USOCR; FPRS; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L244	15	community near5 managed near5 RAN	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L245	39589	709/223.ccls.	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM
L246	214	(US-0005068-$ | US- 0005266-$ | US- 0015460-$ | US- 0015968-$ | US- 0021751-$ | US- 0026601-$ | US- 0038852-$ | US- 0044099-$ | US- 0049859-$ | US- 0051062-$ | US-	(US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	OFF	2022/03/25 12:54 PM

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PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
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N110	1567	H04L29/08072.cpc.	(US-PGPUB; USPAT)	OR	OFF	OFF	2018/11/22 12:28 PM
N111	26795	H04L29/06.cpc.	(US-PGPUB; USPAT)	OR	OFF	OFF	2018/11/22 12:28 PM
N112	8674	H04L41/22.cpc.	(US-PGPUB; USPAT)	OR	OFF	OFF	2018/11/22 12:28 PM
N113	11500	H04L41/12.cpc.	(US-PGPUB; USPAT)	OR	OFF	OFF	2018/11/22 12:28 PM
N114	0	((cluster with initialization) and (mathematical with expression) and (nodes with mathematical) and (single with node with kernel)).clm.	(US-PGPUB; USPAT)	OR	OFF	OFF	2018/11/22 12:30 PM
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N116	1	((cluster with initialization) and (nodes with mathematical)).clm.	(US-PGPUB; USPAT)	OR	OFF	OFF	2018/11/22 12:30 PM
N117	177	((cluster with initialization)).clm.	(US-PGPUB; USPAT)	OR	OFF	OFF	2018/11/22 12:31 PM

N118	0	N109 and N117	(US-PGPUB; USPAT)	OR	OFF	OFF	2018/11/22 12:31 PM
N119	0	N110 and N117	(US-PGPUB; USPAT)	OR	OFF	OFF	2018/11/22 12:31 PM
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PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	17/374789
	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
(Multiple sheets used when necessary)	Examiner	Asres, Hermon
SHEET 1 OF 2	Attorney Docket No.	ZTANN.002P1C7

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number *Number - Kind Code (if known)* Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document *Country Code-Number-Kind Code* Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T[1]

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	1	**Defendant NVIDIA Corporation's Supplemental Invalidity Contentions** in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 151 pages.	
	2	**Exhibit A-1 - PVMaple System**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 270 pages.	
	3	**Exhibit A-2 - Distributed Maple System**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 261 pages.	
	4	**Exhibit A-3 - Matlab*P System**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 254 pages.	
	5	**Exhibit A-4 - FFTW**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 467 pages.	
	6	**Exhibit A-5 - Intel Paragon Maple System**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 137 pages.	
	7	**Exhibit A-6 - Stony Brook Bluster**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 289 pages.	
	8	**Exhibit A-7 - AppleSeed Pooch System**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 160 pages.	
	9	**Exhibit A-9 - PVMaple References**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 270 pages.	
	10	**Exhibit A-10 - Distributed Maple References**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 262 pages.	
	11	**Exhibit A-11 - Matlab *P References**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 246 pages.	

Examiner Signature	/HERMON ASRES/	Date Considered	03/25/2022

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.A./

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	17/374789
	Filing Date	July 13, 2021
	First Named Inventor	Tannenbaum, Zvi
	Art Unit	2449
(Multiple sheets used when necessary)	Examiner	Asres, Hermon
SHEET 2 OF 2	Attorney Docket No.	ZTANN.002P1C7

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[1]
	12	**Exhibit A-12 - FFTW References**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 467 pages.	
	13	**Exhibit A-13 - Intel Paragon Maple References**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 137 pages.	
	14	**Exhibit A-14 - Stony Brook Cluster References**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 289 pages.	
	15	**Exhibit A-15 - AppleSeed Pooch References**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 163 pages.	
	16	**Exhibit A-17 - MultiMatlab System**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 249 pages.	
	17	**Exhibit A-18 - MultiMatlab References**, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 254 pages.	
	18	**Exhibit A-19 - U.S. Patent No. 10,333,768 ("'768") v. Microsoft Windows Compute Cluster Server 2003 ("CCS")**, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 41 pages.	
	19	**Exhibit A-20 - U.S. Patent No. 10,333,768 ("'768") v. Supercomputing Engine for Mathematica ("SEM")**, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1:19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 126 pages.	

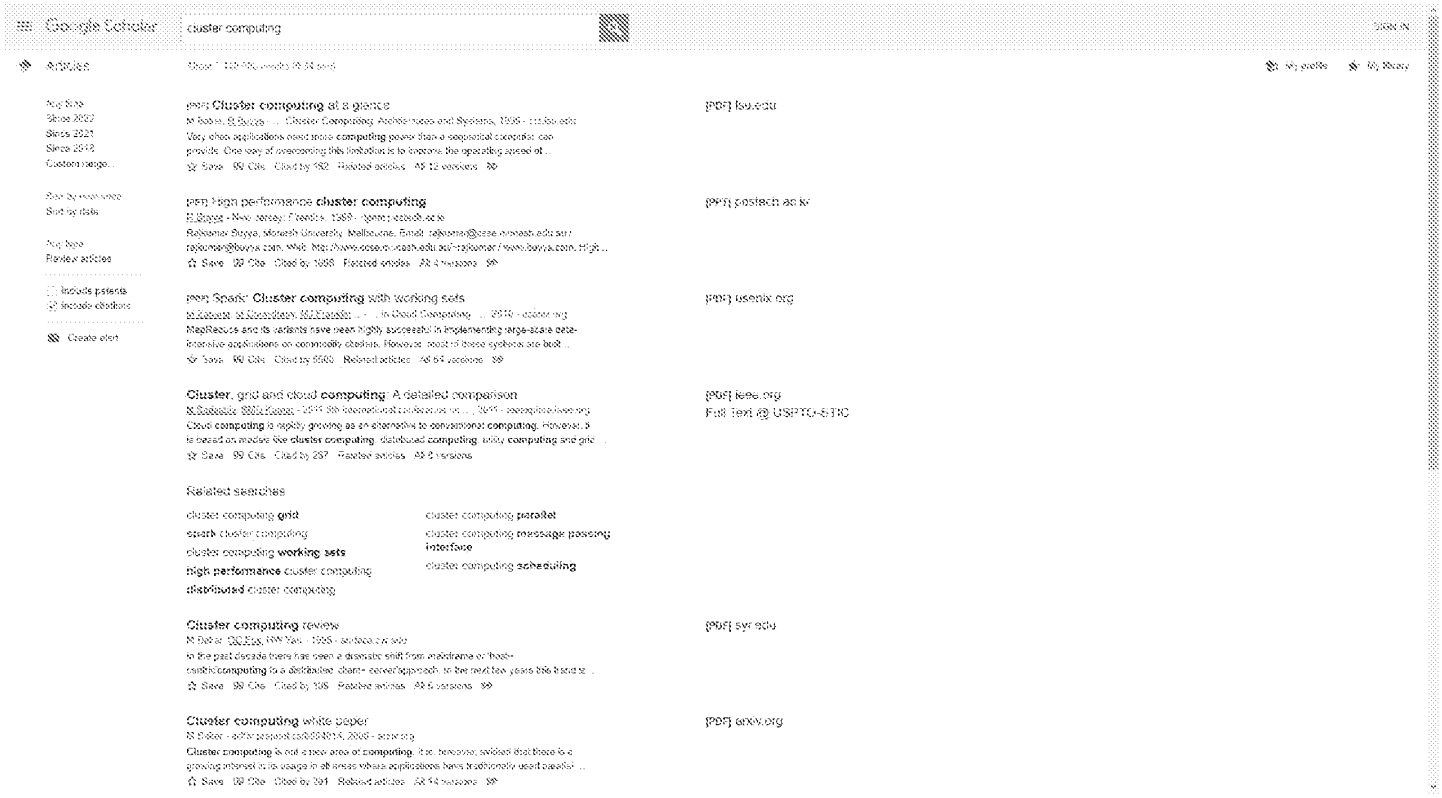
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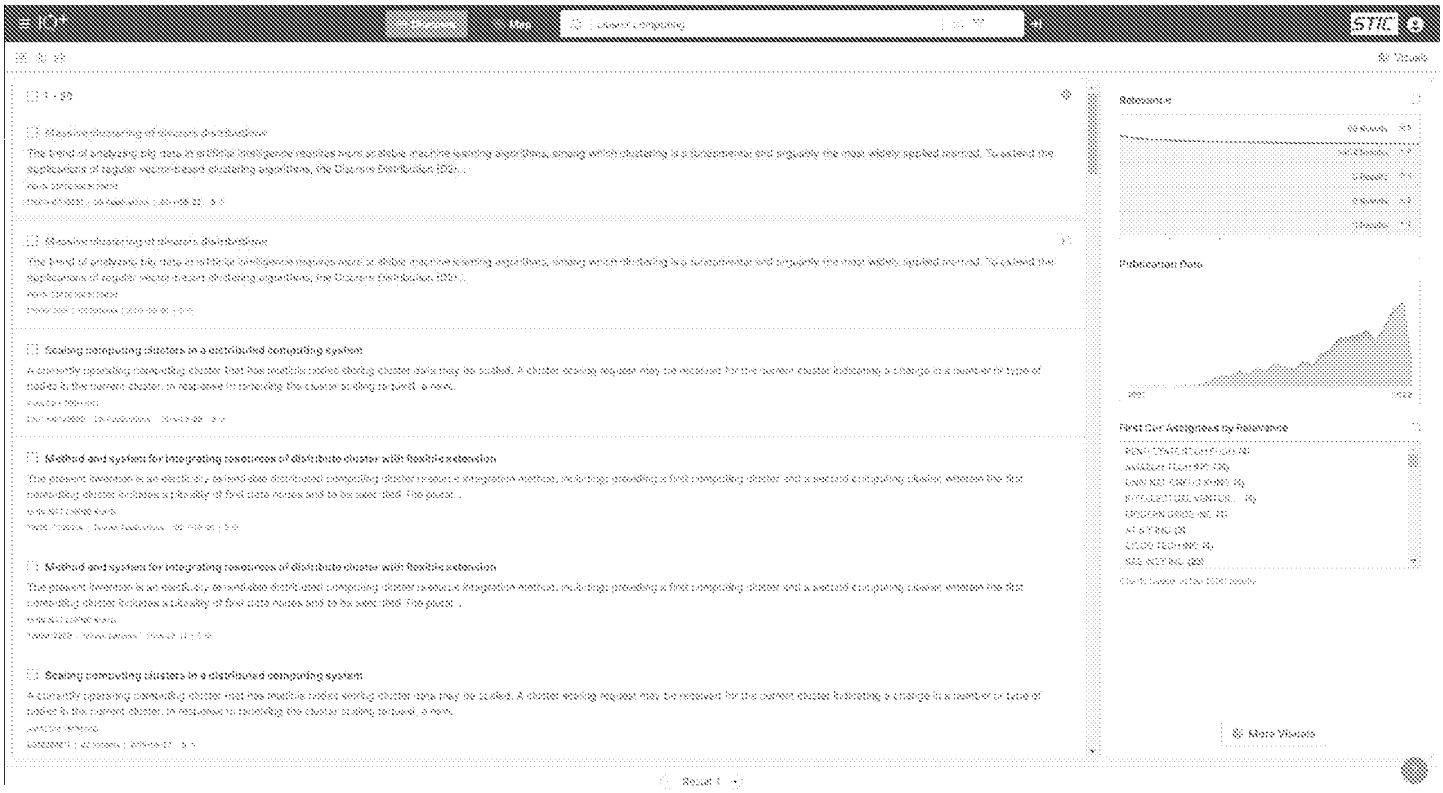
Examiner Signature /HERMON ASRES/	Date Considered 03/25/2022

***Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

T[1] - Place a check mark in this area when an English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.A./


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Dean E. Dauger, Huntington Beach, CA, UNITED STATES

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16449084 is a CON of 14181112 02/14/2014 PAT 10333768

14181112 is a CON of 13423063 03/16/2012 PAT 8676877

13423063 is a CON of 12040519 02/29/2008 PAT 8140612

12040519 is a CIP of 11744461 05/04/2007 PAT 8082289

11744461 has PRO of 60850908 10/11/2006

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FOREIGN APPLICATIONS

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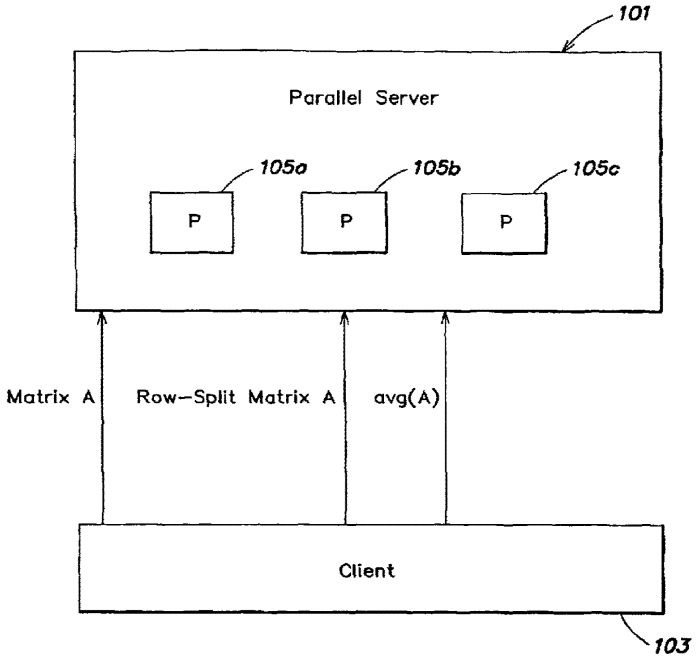
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[Continued on next page]

(54) Title: METHODS AND APPARATUS FOR PARALLEL EXECUTION OF A PROCESS



(57) Abstract: One embodiment of the invention is directed to executing a computer program that manipulates data stored in a distributed manner on a parallel server. At least one portion of the computer program treats the data from a global perspective, wherein commands to the parallel server are not specific to the manner in which the data is distributed on the parallel server. In addition, at least one portion of the computer program treats the data from a local perspective, wherein commands to the parallel server are specific to the manner in which the data is distributed on the parallel server.

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METHODS AND APPARATUS FOR PARALLEL EXECUTION OF A PROCESS

Cross Reference to Related Applications

This application claims the benefit under 35 U.S.C. §119(e) of co-pending U.S. Provisional Application Serial No. 60/623,682, filed October 29, 2004, entitled "A Method And System For An Interactive Parallel Programming Environment" by Long Yin Choy, et. al., the contents of which are incorporated herein by reference.

Field of the Invention

The present invention relates to providing parallel processing capability.

Description of the Related Art

Parallel computing is the concurrent use of multiple processors to solve a computational problem. Large problems may take significant time to solve or may be impossible to solve using only a single processor. Thus, such problems may be divided among multiple processors, each of which solves a portion of the problem.

However, writing program code to solve a computational problem in parallel may present challenges. For example, a programmer may have to devise a complex algorithm to determine an efficient way in which to divide the problem up among the multiple processors, how memory should be allocated and shared among these processors, and how messages should be passed between processors.

As used herein, the term "computer program" refers to a related set of statements or instructions to be used directly or indirectly in a computer in order to bring about a certain result. Different portions of the same computer program may be stored in different files and/or on different computers.

The programmer may also wish to employ pre-existing parallel computing software packages, such as, for example, parallel virtual machine (PVM) or message passing interface (MPI) packages, so that routines for sharing data between processors, spawning additional processes, and other general parallel computing tasks need not be coded from scratch. Thus, the programmer may have to be familiar with such software packages.

Summary

One aspect of the invention is directed to a method of processing a computer program that manipulates a data structure stored on a parallel server comprising a plurality of processors, wherein a portion of the data structure is stored on each of the plurality of processors. The method comprises acts of: (a) executing a first routine based on code in the computer program that causes a first request to perform a first operation on the data structure to be sent to the parallel server, wherein the first routine is a routine that overloads a serial routine that, when executed, causes the first operation to be performed serially; and (b) executing a second routine based on code in the computer program that causes a second request to be sent to the parallel server, wherein the second request includes an instruction to at least one specific processor of the plurality of processors to perform a second operation on the portion of the data structure stored on the at least one specific processor. Another aspect is directed to at least one computer readable medium encoded with instructions that, when executed on a computer system, perform the above-described method.

A further aspect is directed to a computer that executes a computer program for manipulating a data structure stored on a parallel server comprising a plurality of processors, wherein a portion of the data structure is stored on each of the plurality of processors. The computer comprises: an output for sending data to the parallel server; and at least one controller, coupled to the output that: (a) executes a first routine based on code in the computer program that causes a first request to perform a first operation on the data structure to be sent to the parallel server, via the output, wherein the first routine is a routine that overloads a serial routine that, when executed, causes the first operation to be performed serially; and (b) executes a second routine based on code in the computer program that causes a second request to be sent to the parallel server, via the output, wherein the second request includes an instruction to at least one specific processor of the plurality of processors to perform a second operation on the portion of the data structure stored on the at least one specific processor.

Another aspect is directed to a method of processing a computer program written in an interpreted programming language that manipulates a data structure stored on a parallel server comprising a plurality of processors, wherein a portion of the data structure is stored on each of the plurality of processors. The method comprises acts of:

(a) executing a first routine based on code in the computer program that causes a first request to perform a first operation on the data structure to be sent to the parallel server; and (b) executing a second routine based on code in the computer program that causes a second request to be sent to the parallel server, wherein the second request includes an instruction to at least one specific processor of the plurality of processors to perform a second operation on the portion of the data structure stored on the at least one specific processor. A further aspect is directed to at least one computer readable medium encoded with instructions that, when executed on a computer system, perform the above-described method.

Another aspect is directed to a computer that executes a computer program written in a interpreted programming language for manipulating a data structure stored on a parallel server comprising a plurality of processors, wherein a portion of the data structure is stored on each of the plurality of processors. The computer comprises: an output for sending data to the parallel server; and at least one controller, coupled to the output that: (a) executes a first routine based on code in the computer program that causes a first request to perform a first operation on the data structure to be sent to the parallel server, via the output; and (b) executes a second routine based on code in the computer program that causes a second request to be sent to the parallel server, via the output, wherein the second request includes an instruction to at least one specific processor of the plurality of processors to perform a second operation on the portion of the data structure stored on the at least one specific processor.

A further aspect is directed to a method of processing a computer program that manipulates a data structure stored on a parallel server comprising a plurality of processors, wherein a portion of the data structure is physically stored on each of the plurality of processors. The method comprises acts of: (a) executing a first routine based on code in the computer program that causes a first request to perform a first operation on the data structure to be sent to the parallel server; and (b) executing a second routine based on code in the computer program that causes a second request to be sent to the parallel server, wherein the second request defines an abstract splitting of the data structure that defines a plurality of abstract portions of the data structure, and wherein the second request includes an instruction to perform a second operation on at least one of the plurality of abstract portions.

Brief Description of the Drawings

Figure 1A is a block diagram of a system in which global operations on data may be performed;

Figure 1B is a block diagram of a system in which local operations on data may be performed;

Figure 2 is a block diagram of a system adaptable to perform a process of a scientific computing software application in parallel, in accordance with some embodiments for practicing the teachings herein;

Figure 3 is a block diagram of an example of parallel server that executes the server software of Figure 2, in accordance with the methods and systems as taught herein;

Figure 4 is a block diagram of an example of parallel server that executes the server software of Figure 2, in accordance with the methods and systems as taught herein;

Figure 5 is a block diagram of an object that reference local data in accordance with the methods and systems as taught herein;

Figure 6 is a block diagram of a matrix row-distributed on a parallel server.

Figure 7A is a diagram of a stencil-splitting of a matrix in accordance with the methods and systems taught herein; and

Figure 7B is a diagram of a multi-grid splitting of a matrix in accordance with the methods and systems taught herein.

Detailed Description

Many programmers have existing computer programs or computer code that was originally designed to be run serially (i.e., on a single processor). Applicants have appreciated that it often may be desirable to use such serial computer program code in the context of a parallel computing platform, to take advantage of parallel processing capabilities. Achieving this goal, however, is non-trivial.

More specifically, Applicants have appreciated that, in a parallel computing environment, a user may wish to treat data in different ways within the same parallel program. Thus, a user may wish to take a "global" view of the data, in which an object

stored on the parallel server is viewed by the user as a single object, even though the object may be distributed across multiple processors of the parallel computer. As used herein, the term "processor" refers to a processor core and its associated components. Thus, a single integrated circuit or chip that has multiple processor cores may be considered to be multiple processors. Thus, for example, an integrated circuit or chip with two processor cores may be considered to be two processors, an integrated circuit or chip with four processor cores may be considered to be four processors, and an integrated circuit or chip with *n* processor cores may be considered to be *n* processors.

Thus, the user need not be aware of how the object is distributed amongst the multiple processors of the parallel server or what action each individual processor takes to perform an operation on the object in parallel. An example of a series of global view operations is provided in Figure 1A.

The system of Figure 1A includes a parallel server 101 and a client 103, which sends commands to and receives results from parallel server 101. Parallel server 101 includes three processors, 105a, 105b, and 105c, though a user sending global view commands to parallel server 101 through client 103 need not be aware of the number of processors being used in parallel server 101. As shown in Figure 1A, client 103 may create a Matrix A on parallel server 101, which may be, for example, a 3x2 matrix of integer values. Parallel server 101 may distribute the data of Matrix A amongst processors 105a, 105b, and/or 105c in any suitable way and the user need not be aware of how this data is distributed or that it is distributed.

For example, parallel server 101 may row-distribute the data, such that each processor stores one row of Matrix A. That is, processor 105a may store element (0,0) and element (0,1), processor 105b may store element (1,0) and element (1,1) and processor 105c may store element (2,0) and element (2,1). Alternatively, the parallel server may column-distribute the data so that each column of Matrix A is stored on one of the processors 105 of parallel server 101. For example, element (0,0), element (1,0), and element (2,0) may be stored on processor 105a, while element (0,1), element (1,1), and element (2,1) may be stored on processor 105b. Any other suitable distribution of data may be used, as the invention is not limited in this respect.

It should be appreciated that when data is referred to herein as being stored on a particular processor or a particular processor is referred to as storing data, this does not

require that the data be physically stored on the processor. Rather, data being stored on a processor or a processor storing data means that the data is stored in memory that is allocated to or under control of the processor. Likewise, when data is referred to herein as being distributed amongst processors, it is not required that the data be physically stored on the processors, but rather means that the data is stored in one or more memories and each processor is allocated or controls memory that stores at least a portion of the data.

From the user's global view perspective, the manner in which Matrix A is distributed amongst the processors 105 is irrelevant. Client 103 may subsequently create a second matrix, Matrix B, on the parallel server. Matrix B may, for example, also be a 3x2 matrix of integer values and may also be distributed amongst processors 105 in any suitable way. Matrix A and Matrix B need not be distributed amongst the processors in the same way. For example, the parallel server may row-distribute Matrix A, but may column-distribute Matrix B. However, like Matrix A, the manner in which Matrix B is distributed amongst the processors 105 is irrelevant when taking a global view of the data.

Client 103 may next send a command to parallel server 101 to add Matrix A and Matrix B and store the result in a third matrix, Matrix C. Because the user is unaware of how Matrix A and Matrix B are distributed amongst processors 105, the user is unable to instruct each processor on what action to take to add Matrix A and Matrix B. However, parallel server 101 is aware of how these matrices are distributed. Thus, when parallel server 101 receives the command to add Matrix A and Matrix B, each processor 105 may be instructed to take the appropriate actions to add the two matrices. For example, if both Matrix A and Matrix B are row distributed, processor 105a may be instructed to add the content of cells Matrix A(0,0) and Matrix B(0,0) (hereinafter, simply referred to as adding the referenced cells) and to add Matrix A(0,1) and Matrix B(0,1). Likewise, processor 105b may be instructed to add Matrix A(1,0) and Matrix B(1,0) and to add Matrix A(1,1) and Matrix B(1,1). Similarly, processor 105c may be instructed to add Matrix A(2,0) and Matrix B(2,0) and to add Matrix A(2,1) and Matrix B(2,1). The result of the addition of Matrix A and Matrix B is a 3x2 row-distributed matrix (i.e., Matrix C). Parallel server 101 may return a pointer or handle that the client may use to refer to Matrix C. Client 103, using the pointer or handle returned from parallel server 101, may

subsequently request that parallel server return Matrix C to the client. In response, parallel server 103 may instruct each processor 105 to return the portion of Matrix C that it stores. Thus, for example, processor 105a may return Matrix C(0,0) and Matrix C(0,1), processor 105b may return Matrix C(1,0) and Matrix C(1,1), and processor 105c may return Matrix C(2,0) and Matrix C(2,1).

In addition to taking a global view of data, the user may, in some situations take a "local" view of the data. When treating data from a local perspective, a user may be aware of how an object is split amongst processors and may instruct specific processors to perform operations on the portions of the distributed object that they store. Thus, for example, if a user has previously-written serial code that operates on a certain type of data, the user may instruct each processor to execute that code on the portion of the distributed data it stores.

As used herein, a splitting of an object or data structure, such as, for example, a matrix, amongst processors may be an "abstract splitting" or a "physical distribution." In a physical distribution, data is physically distributed among the processors in the manner specified in the splitting. For example, if a matrix is physically row-distributed, then each row of the matrix is stored on a different processor. In an abstract splitting, data is split among abstract processors and the abstract splitting may have little or nothing to do with the way in which data is physically distributed among the physical processors. The term "abstract processor" as used herein, refers to a non-physical virtual processor whose operations may be performed by one or more physical processors. For example, a 2x4 matrix may be physically row-distributed on a parallel server that has two processors, such that one row of the matrix is physically stored on each processor. However, the same matrix may be abstractly split amongst four abstract processors, such that each column of the matrix is abstractly stored on one of the four abstract processors. Thus, for the purposes of performing operations on the matrix, the matrix is treated by the parallel server and the user as if it were column-split among four processors, though the actual physical distribution of the data is a row-distribution among two physical processors.

An example of a series of local view operations is provided in Figure 1B. In Figure 1B, client 103 creates a Matrix A on parallel server 101. As in the example of Figure 1A, Matrix A may be a 3x2 matrix of integers. The user may have previously written a serial routine called, for example, 'avg' that takes as input a 1x2 matrix of

integers, computes the average of the two integers in the matrix, and outputs the average as a 1x1 matrix. Thus, Client 103 may subsequently send a command to parallel server 101 to row-split Matrix A across processors 105a, 105b, and 105c so that each processor has 1x2 matrix that is one row of Matrix A. It should be appreciated that, in some embodiments, processors 105a, 105b, and 105c may be abstract processors and the row-splitting may be an abstract splitting. That is, the data of Matrix A may be physically stored on the physical processors of parallel server 101 in a manner different from the row-splitting described above. Alternatively, in other embodiments, the row-splitting of Matrix A may be a physical distribution. That is, processors 105a, 105b, and 105c may be physical processors and one row of Matrix A may be physically stored on each of these processors.

Client 103 may instruct the parallel server to have each processor 105 execute the previously-written 'avg' routine, using the 1x2 matrix stored on the processor as input. The results of this operation is that there is a 1x1 matrix stored on each of processors 105, wherein the value in each of the 1x1 matrices is the average of the numbers in one of the rows of Matrix A. In embodiments in which Matrix A is abstractly row-split, it should be appreciated that is the abstract processors that each execute the 'avg' routine. At the physical level, depending on how the data is physically distributed among the processors, some or all of the physical processors may execute the 'avg' routine or some physical processors may execute the 'avg' routine multiple times using different portions of the matrix physically stored thereon as input. In some embodiments, the 'avg' routine is not executed at all, but rather the parallel server causes the physical processes to perform operations that would have the same result as executing the 'avg' routine on each processor that stores a row of the row-split matrix.

One embodiment of the invention is directed to providing a utility which allows a user to write a program to be executed on the parallel server that uses both a global view of data and local view of data. That is, a portion of the program may operate on the data globally, while another portion of same program operates on the data locally.

U.S. Patent Application serial no. 11/217,114, titled "METHODS AND APPARATUS FOR PARALLEL EXECUTION OF A PROCESS," filed on August 31, 2005 (hereinafter, "the '114 application"), which is hereby incorporated by reference in its entirety, describes a system in which a user may write parallel programs using a

global view of the data. Specifically, the application describes a system that employs a scientific computing software application to write programs which are then "parallelized" by software on the parallel server. As used herein, the term scientific computing software application refers to a software application capable of solving computational problems that are input by a user. Examples of commercially available scientific computing software applications include MATLAB™, produced and sold by The MathWorks, Natick, Massachusetts, Maple™, produced and sold by Maplesoft, Waterloo, Ontario, Canada, Mathematica™, produced and sold by Wolfram Research, Champaign, Illinois, Octave, produced and distributed by GNU, and Excel™, produced and sold by Microsoft Corporation, Redmond, WA.

The system of the '114 application that allows a user to operate globally on distributed data is described below and may employ a technique referred to as overloading. As used herein, the term overloading refers to having two or more objects or methods that have the same name but have different meanings or functionalities depending on the context in which the object or method is used. For example, which method is called may depend on the number of parameters with which the method is called or the data type of parameters with which the method is called. That is, a programmer may define two methods each named *Area*. The first *Area* method may take as a parameter a user-defined data type called *Triangle* and computes the area of a triangle. The second *Area* method may take as a parameter a user-defined data type called *Circle* and computes the area of a circle. Thus, simply from the line of code "B = *Area*(A)," it cannot be determined which *Area* method is to be called. That is, if the variable A is of the data type *Triangle*, the first *Area* method is called, while if the variable A is of the data type *Circle*, the second *Area* method is called.

As another example, from the programmer's perspective, the method call for the two or more methods that share the same name may be identical. That is, the method name, the number of parameters and the type of parameters are the same for both (or all) of the methods and the decision as to which of the two or methods is called is not made by the programmer at the time of programming. For example, the line of code $x + y$, where both x and y are variables that represent matrices of integers may have different functionality depending on the context in which the line of code is written. Thus, for example, if both x and y are small matrices, an addition routine that performs a normal

matrix addition may be called. However, if either *x* or *y* represents a matrix larger than a certain size an addition routine that performs the matrix addition in parallel may be called. The decision as to which addition routine is to be called may be made in any suitable way as the invention is not limited in this respect. For example, the decision may be made either at compile time, at run time, or at any other suitable time. Further, the decision may be made by any suitable entity, such as the compiler or interpreter of the programming language, or an outside software program (though the compiler, interpreter, or outside software program may be manually configured, e.g., by a programmer, to make these decisions in a certain way).

As in the example above, operators may also be overloaded. For example, the function of the '+' operator in the line of code 'C = A +B' may be different depending on the data types of the operands A and B. That is, if the operands A and B are integers, the '+' operator may be defined to perform a integer addition. However, if the operands A and B are arrays or matrices, the '+' operator may be defined, by the programmer, to perform a matrix addition.

Figure 2 is an example of a system in which polymorphism (e.g., by overloading methods and/or operators) may be used to provide parallel computing capability to a scientific computing software application. The system of Figure 2 includes a scientific computing software application 201, communication software 203, and server software 205.

In one embodiment, operators and/or methods of a program of scientific computing software application 201 may be overloaded. The overloaded methods and/or operators may be defined to pass a message to communication software 203 requesting that a certain operation or process be performed in parallel. Communication software 203, in response to receiving the message, may then send a command to server software 205 to perform the process in parallel. This may be done in any suitable way, as the invention is not limited in this respect. For example, a new data type or class may be defined and operators and/or methods may be overloaded such that when the operators and/or methods are called with a parameter or operand of the newly defined data type, the overloaded method is called.

As an example, the *rand* function in the programming language of a scientific computing software application may be a built-in method of scientific computing

software application 201 that creates an n-by-n matrix of randomly-valued entries, where n is an integer value specified in the parameter of the method. Thus, the line of code in Table 1 creates a 100-by-100 matrix of random numbers and stores the result in the variable 'X.' The server software may then pass out tasks to a plurality of processors, to complete the task or tasks require by the method.

Table 1

X = rand(100);

However, the *rand* method may be overloaded so that if the parameter provided is of the new data type (i.e., as opposed to an integer or scalar), then the overloaded rand method is called rather than the built-in *rand* method. For example, in the line of code in Table 2, the parameter provided to the *rand* method is "100*p." The variable *p* may be an object of the new data type or class which, for the purposes of this example is called the *dlayout* class. The * operator may be the built-in multiplication operator of scientific computing software application 201, which takes two operands. However, the * operator may be overloaded, such that when one or both of its operands are objects of the *dlayout* class, the overloaded operator is called. The overloaded * operator may return an object of the *dlayout* class.

Table 2

X = rand(100*p);

Thus, the operation "100*p" in Table 2 may return a *dlayout* object. The *rand* method may also be overloaded so that when the parameter provided is a *dlayout* object (instead of an integer or scalar), the overloaded *rand* method is called. The overloaded *rand* method may call communication software 203 which sends a command to server software 205 to create a distributed 100-by-100 matrix. The overloaded *rand* method

may return an object of a user-defined data type or class that may be used as a name or handle to reference the matrix created on the parallel server. For example, the overloaded *rand* method may return an object of the user-defined *ddense* class, which is stored in the variable X. Thus, the distributed matrix on the parallel server may be accessed and manipulated using the variable X. For example, as shown in Table 3, a method for computing the eigenvalues of a matrix may be performed on the distributed matrix.

That is, the built-in method *eig* of scientific computing software application 201 may take a matrix or an array as its parameter. However, the *eig* function may be overloaded so that if the parameter provided to the method is an object of the *ddense* class, the overloaded method is called. Like the overloaded *rand* method, the overloaded *eig* method, when called, may call communication software 203 which may send a command to server software 205 to calculate the eigenvalues of the distributed matrix X. The overloaded *eig* method may also return an object of the *ddense* class, which is stored in the variable Y, and may be used as a handle to access the matrix of eigenvalues on the parallel server.

Table 3

Y = eig(X)

Because the overloaded methods and/or operators used to contact the parallel server as well as the parallel algorithms that execute on the parallel server may be provided for the user of the scientific computing software application (i.e., without the user having to code them), the user need not have detailed knowledge of parallel programming. Rather, much of the parallel processing capability is transparent to the user.

For example, continuing with the examples provided above, from the user's perspective, the only difference in the program code needed to create a 100-by-100 matrix of random numbers and compute its eigenvalues is the addition of the tag "*p" in the parameter of the *rand* method, as shown above in Table 2. However, the "*p" tag

causes a distributed matrix to be created on the parallel server and future operations on the matrix to be performed in parallel, without the user having to devise or code an parallel algorithms. In the examples above, the *rand* and *eig* methods and the * operator were overloaded to perform certain operations in parallel, such as creating a distributed matrix on a parallel server and computing its eigenvalues in parallel. However, the invention is not limited in this respect, as any suitable built-in method or operator of the scientific computing software application may be overloaded (e.g., to cause its functionality to be performed in parallel).

In the examples described above in connection with Tables 2 and 3, the user is taking a global view of the data. That is, the objects X and Y are global objects and the user need not be aware of how these objects are distributed amongst the processors of the parallel server. Thus, when the user instructs the parallel server to computer the eigenvalues of the matrix referenced by the variable X, the user need not specify what specific operation each processor of the parallel server needs to take to computer these eigenvalues. Rather, server software 205 is aware of the manner in which the data is distributed and has a routine for computing, in parallel, the eigenvalues of a matrix that is distributed in this manner.

It should be appreciated that, although in the examples above certain data types, classes, methods, and/or operators are described as being user-defined, these data-types, classes, methods, and/or operators need not be defined by the ultimate end user of the scientific computing software application. Indeed, the term user-defined is merely used to distinguish between those classes, methods, and operators that are built-in to the scientific computing software application programming language by its publisher's specification and those that are added in by an external programmer. Thus, in one embodiment, the overloaded methods, operators, and user-defined classes may be provided in a software package that also includes communication software 203 and server software 205. The software package, when installed, may work in conjunction with scientific computing software application 201 to provide the above-described parallel processing functionality.

Further, in the examples above, the built-in methods and operators were only overloaded with a single additional method or operator. However, the invention is not limited in this respect, as a method or operator may be overloaded with any suitable

number of methods or operators. That is, in the example provided above, the * operator was overloaded with a * operator that takes an object of the *dlayout* class as one of its operands and returns a *dlayout* object. However, the * operator could also be overloaded with an operator that takes two *ddense* objects (each of which references a distributed matrix on the parallel server) as its operands, causes a matrix multiplication of the two distributed matrices to be performed in parallel, and returns a *ddense* object that serves as reference to the distributed matrix that results from the matrix multiplication. Thus, in the example above, the * operator may perform one of three different operations, depending on the data types of its operands.

Additionally, in the examples above, two data types or classes were defined (i.e., *dlayout* and *ddense*). It should be appreciated that these class names are provided as examples and any suitable class names or data type names may be used. Moreover, while in the examples above two user-defined data types or classes were used in connection with providing parallel computing capability in scientific computing software application 201, the invention is not limited in this respect, as any suitable number of user-defined data types or classes may be used. Further, any suitable data and methods may be encapsulated in these user defined data types, as the invention is not limited in this respect.

In one embodiment, scientific computing software application 201 and communication software 203 may execute on the processor of a client computer, while server software 205 may execute on multiple processors of one or more parallel servers. However, the invention is not limited in this respect, as scientific software application 201 and communication software 203 may execute on any suitable processor or processors. For example, scientific software application 201 may execute on one of the processors of the parallel server that executes server software 205. In such embodiments, the processor that executes scientific software application 201 and/or communication software 203 may be viewed as the client, while the remaining processors in parallel server 205 (individually and in collections of one or more of them) may be viewed as the parallel server. It should be appreciated that the processor that executes scientific software application 201 and/or communication software 203 may also execute a portion of server software 205. Thus, this processor may be viewed as the client as well as part of the parallel server.

The parallel server that executes server software 205 may be any suitable type of parallel server, as the invention is not limited in this respect. For example, the parallel server may be a symmetric multiprocessing (SMP) system, a massively parallel processor (MPP) system, or may be a Beowulf cluster. In this respect, it should be appreciated that parallel server may include a plurality of separate machines that are linked together so that they may operate on a single problem in parallel. A system having such an architecture may be viewed as a single parallel server, despite being made up of many individual computers that are also capable of operating independently of each other.

In the examples above, overloaded methods and operators are used in scientific computing software application 201 to call and/or pass messages to communication software 203 (which, in turn, sends a command to parallel server 205). These software entities may communicate in any suitable way, as the invention is not limited in this respect. For example, in one embodiment, subroutines of communication software 203 may be linked (either statically or dynamically) into scientific computing software application 201, so that the overloaded methods and/or operators of scientific computing software application may directly call these subroutines. In another embodiment, interprocess communication may be used to communicate between scientific computing software application 201 and communication software 203. Any suitable form of interprocess communication may be used, such as, for example, pipes, signals, message queues, semaphores, shared memory, sockets, or any other suitable form, as the invention is not limited in this respect.

Because scientific computing software applications are intended primarily for computing and modeling, the programming languages of these software applications typically do not provide the capability to perform and/or handle communications over a network. Thus, in one embodiment, communication software 203 may be written in a language (e.g., C or Fortran) that provides network communication capability. However, in embodiments of the invention in which the programming language of scientific computing software application 201 allows a programmer to perform network communications, communication software 203 need not be used, and the overloaded methods and operators of scientific computing software application 201 may

programmed to send commands to server software 205 (i.e., without using communication software 203 as an intermediary).

In embodiments wherein scientific computing software application 201 and communication software 203 reside on a separate machine from server software 205, communication software 203 or (in embodiments where communication software 203 is not used) scientific computing software application 201 may communicate with server software 205 over a network. Any suitable network protocol or protocols may be used, as the invention is not limited in this respect. For example, in some embodiments, the TCP/IP protocol may be used. In embodiments wherein scientific computing software application 201 and communication software reside on a processor of the parallel server that executes server software 205, any suitable method of communication between communication software 203 (or, in some embodiments, scientific computing software application 201) and parallel server 205 may be used. For example, network based communication may be used, even though the communications are not necessarily traveling over a network; interprocess communication may be used; or any other suitable form of communication may be used, as the invention is not limited in this respect.

Solving problems in parallel often involves operating on very large data sets. Consequently, passing results between the client and the parallel server each time they are computed may decrease performance. Thus, in one embodiment, data may remain on the parallel server, unless results are explicitly requested to be sent to the client. For example, as discussed in above, the example line of code in Table 2 causes a command to be sent to the parallel server to create a 100-by-100 matrix distributed matrix of random numbers. The parallel server may create the 100-by-100 matrix in response to the command. If the result of this computation (i.e., the 100-by-100 matrix) were to be sent back to the client rather than keeping the data on the parallel server, 10,000 numbers may have to be sent back to the client. Further, future operations on the matrix to be performed by the parallel server may involve sending the matrix data back to the parallel server from the client so that the parallel server may operate on the data. This sequence may increase network traffic, latency, and overall processing time.

However, if the data remains on the parallel server, the data need not be transferred unless the user of the scientific computing software application explicitly requests to view the data. For example, the 100-by-100 matrix created on the parallel

server using the line of code in Table 4 may remain on the parallel server and only a reference to that data may be returned to the scientific computing software application. In the example, in Table 4, this reference is stored in the *ddense* variable 'X.' Thus, if it is desired to perform future operations on the matrix, the matrix data can be identified and located on the parallel server using this reference.

If a user of a scientific software computing application desires to view a portion of the resulting data, the user may request that this data be returned from the parallel server and displayed. This may be done in any suitable way, as the invention is not limited in this respect. In some embodiments, method and/or operator overloading may be used to request that data stored on the parallel server be returned to the client. For example, the line of code shown in Table 4 may be used to retrieve and display the first element of the distributed matrix created by the line of code in Table 2. Scientific computing software application 201 may provide, for example, a method called *subsref* that is used to access an array or matrix element and invoked by the notation A(R,C), where A is a variable that represents the array or matrix and R,C refers to the row and column of the requested matrix element. The *subsref* function may be overloaded so that if called with a *ddense* variable as its parameter instead of an array or matrix, a command may be sent to the parallel server to return the requested element of the matrix that is referenced by the *ddense* variable.

Table 4

X(1,1)

Server software 205 may operate in any suitable way to receive commands from the client and perform operations in parallel, as the invention is not limited in this respect. Figure 3 is but one example of a suitable configuration of server software 205 for at least some embodiments. In Figure 3, parallel server 301 includes a plurality of processors, 303a, 303b, ..., 303n, and a memory 313. Each of processors 303a-303n includes four software modules: client managers 305a, 305b, ..., 305n; server managers 307a, 307b, ..., 307n; library managers 309a, 309b, ..., 309n; and data managers 311a,