

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION and
ADVANCED MICRO DEVICES, INC.,
Petitioner,

v.

ADVANCED CLUSTER SYSTEMS, INC.,
Patent Owner.

IPR2025-00913
Patent 11,570,034 B2

Before KARL D. EASTHOM, ARTHUR M. PESLAK, and
BRIAN P. MURPHY, *Administrative Patent Judges*.

MURPHY, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background and Summary

Intel Corporation and Advanced Micro Devices (together, “Petitioner”) filed a Petition pursuant to 35 U.S.C. § 311 requesting institution of *inter partes* review of claims 1–30 of U.S. Patent No. 11,570,034 B2 (Ex. 1001, “the ’034 patent”). Paper 3 (“Pet.”). Advanced Cluster Systems, Inc. (“Patent Owner”) timely filed a Patent Owner Preliminary Response. Paper 10 (“Prelim. Resp.”). The Acting Director of the Office denied Patent Owner’s request for discretionary denial and referred the Petition to the Board for a decision on institution. Paper 13.

We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted “unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” Under § 314, the Board may not institute review on fewer than all claims challenged in the petition. *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018). If the Board institutes a review, it will institute “on all of the challenged claims and on all grounds of unpatentability asserted for each claim.” 37 C.F.R. § 42.108(a). Upon consideration of the Petition, the Preliminary Response, and the evidence of record, for the reasons set forth below, we conclude the Petition demonstrates a reasonable likelihood that Petitioner would prevail in showing the unpatentability of at least one challenged claim in the ’034 patent. Accordingly, we institute an *inter partes* review of claims 1–30 of the ’034 patent.

B. Real Parties in Interest and Related Matters

Petitioner identifies Intel Corporation and Advanced Micro Devices, Inc. as the real parties in interest. Pet. 96. Patent Owner, Advanced Cluster Systems, Inc., identifies itself as the real party in interest. Paper 5, 2.

Petitioner and Patent Owner identify the following related matters:

- *Advanced Cluster Systems, Inc. v. Intel Corporation*, No. 7:24-cv-00245 (W.D. Tex.) (pending)
- *Advanced Cluster Systems, Inc. v. Advanced Micro Devices, Inc.*, No. 7:24-cv-00244 (W.D. Tex.) (pending)
- *Advanced Cluster Systems, Inc. v. NVIDIA Corporation*, No. 1:19-cv-02032 (D. Del.) (dismissed)
- *NVIDIA Corporation v. Advanced Cluster Systems, Inc.*, IPR2021-00019 (PTAB) (institution denied)
- *NVIDIA Corporation v. Advanced Cluster Systems, Inc.*, IPR2021-00020 (PTAB) (institution denied)
- *Intel Corp. v. Advanced Cluster Systems, Inc.*, IPR2025-00794 (PTAB) (pending Director rehearing request)
- *Intel Corp. v. Advanced Cluster Systems, Inc.*, IPR2025-00795 (PTAB) (pending Director rehearing request)
- *Advanced Micro Devices, Inc. v. Advanced Cluster Systems, Inc.*, IPR2025-00862 (PTAB) (Director discretionary denial)
- *Advanced Micro Devices, Inc. v. Advanced Cluster Systems, Inc.*, IPR2025-00863 (PTAB) (Director discretionary denial)
- *Intel Corp. and Advanced Micro Devices, Inc. v. Advanced Cluster Systems, Inc.*, IPR2025-00914 (PTAB) (pending)
- *Intel Corp. and Advanced Micro Devices, Inc. v. Advanced Cluster Systems, Inc.*, IPR2025-00915 (PTAB) (pending)

- *Intel Corp. and Advanced Micro Devices, Inc. v. Advanced Cluster Systems, Inc.*, IPR2025-00916 (PTAB) (pending).

Pet. 96; Paper 5, 2–3.

C. The '034 Patent

The '034 patent is titled “Cluster Computing” and issued on January 31, 2023 from an application filed on July 13, 2021. *Id.* at codes (45), (54), (22). The '034 patent “relates to the field of cluster computing generally and to systems and methods for adding cluster computing functionality to a computer program, in particular.” *Id.* at 1:15–18. Cluster computing is a system that enables a group of two or more processing nodes—“computers, microprocessors, and/or processor cores”—to communicate with one another to accomplish programmed tasks “as though they were a single computer.” *Id.* at 1:22–25. The '034 patent distinguishes cluster computing from multi-node distributed or grid computing systems where the processing nodes “do not communicate with each other as peers” and “do not need to share data between the jobs during the computational process.” *Id.* at 1:48–56; *see* Prelim. Resp. 3–4 (“Nodes in such systems could not dynamically exchange instructions with one another at runtime, and expression evaluation across nodes was limited, static, and highly constrained.”) (citing Ex. 1001, 1:48–67).

Figure 1 of the '034 patent, reproduced below, “is a block diagram of one embodiment of [] computer cluster 100 wherein computer systems 110, 120, 130 communicate with one another via a communications network 102.” *Id.* at 5:1–4.¹

¹ Quotations from patent documents may omit or de-emphasize bold numerals.

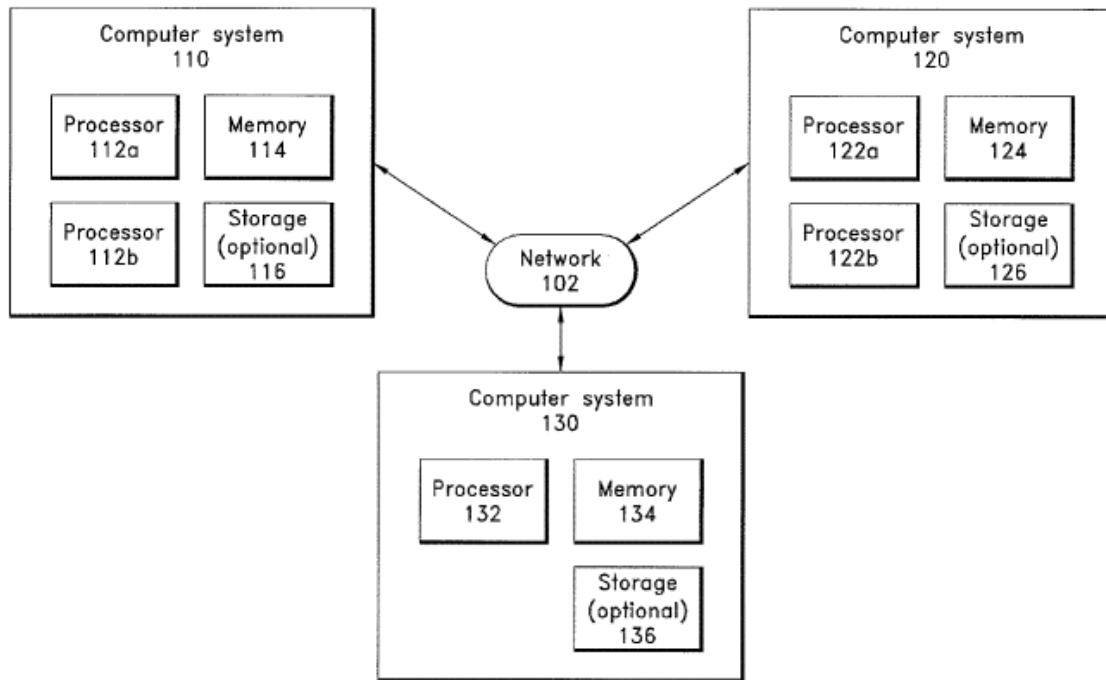


FIG. 1

Figure 1 of the '034 patent illustrates “a computer cluster 100 wherein computer systems 110, 120, 130 communicate with one another via a communications network 102.” *Id.*

In Figure 1, each computer system (110, 120, 130) includes one or more processors (112a, 112b, 122a, 122b, 132), memory (114, 124, 134), and optional storage (116, 126, 136). *Id.* at 6:60–67. Each computer system also includes a network interface (not shown) for connecting to communications network 102, which can include one or more of a LAN, a WAN, an intranet, a wireless network, and/or the Internet. *Id.* at 6:67–7:4. “Each processor can contain one or more processor cores that are capable of single-threaded execution” of software code. *Id.* at 5:11–14.

Embodiments of the '034 patent include enabling a software package to benefit from being run on a plurality of clustered processing nodes. *Id.* at 2:10–14. “One embodiment allows a user to create applications, using a high-level language such as Mathematica, that are able to run on a computer

cluster having supercomputer-like performance.” *Id.* at 2:14–17. “One embodiment provides access to such high-performance computing through a Mathematica Front End, a command line interface, one or more high-level commands, or a programming language such as C or FORTRAN.” *Id.* at 2:17–21. For example, a user interface allows a user to add Message Passing Interface (“MPI”) calls to an interactive programming environment, such as the Mathematica Front End, which enables node-to-node (peer-to-peer) communication to effect cluster processing of the Mathematica computations. *Id.* at 2:28–33, 4:64–67.

Figure 2 of the ’034 patent, reproduced below, “is a block diagram showing relationships among software modules running on one embodiment of a computer cluster 100.” *Id.* at 5:21–23.

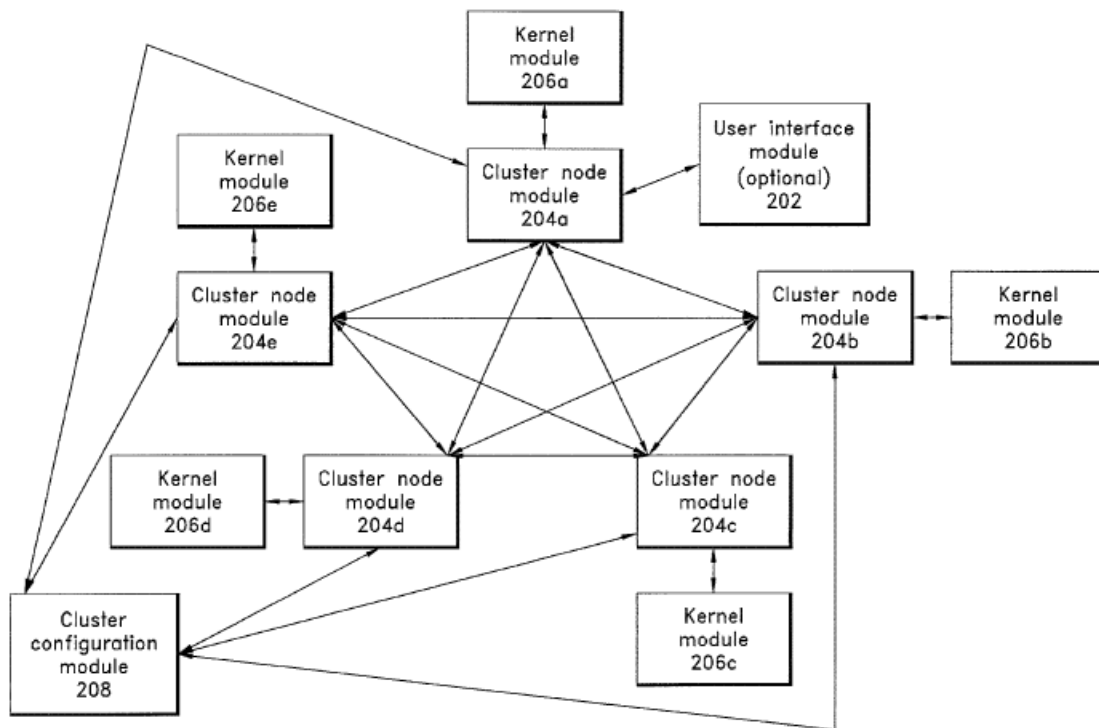


FIG. 2

Figure 2 depicts a cluster of software modules enabled for communication “between any two or more cluster node modules.” *Id.* at 6:14–17.

In the embodiment of Figure 2, user interface module 202 communicates with first cluster node module 204a, which is in communication with all of the other cluster node modules 204b–204e. *Id.* at 5:47–51, 11:18–26. The node-to-node communication architecture allows the user interface module to access kernel modules 206a–206e through cluster node 204a. *Id.* at 11:18–26. Kernel modules 206a–206e each include single-threaded software code for executing instructions (tasks) provided to the program, *e.g.* via the user interface module, and each kernel is associated with one processor (112a, 112b, 122a, 122b, or 132 in Figure 1). *Id.* at 1:33–36, 11:33–35. For example, “MPI calls and advanced cluster commands are used to parallelize program code received from an optional user interface module [] and distribute tasks among the kernel modules.” *Id.* at 6:20–23. Cluster configuration module 208 communicates with cluster node modules 204a–204e to “initialize[] the cluster node modules to provide cluster computing support for [] computer cluster 100.” *Id.* at 11:39–43.

In the embodiment of Figure 2, the initialized cluster node modules “provide communications among kernel modules 206a-e while the tasks are executing.” *Id.* at 6:23–25, 11:45–48. The ’034 patent notes that “single-threaded software code typically does not benefit from multiple processor cores in a computer system,” but in the patented system “two kernel modules (for example, kernel modules 206a, 206b) loaded into memory [] of computer system 110 could exploit at least some of the processing bandwidth of [] two processors 112a, 112b.” *Id.* at 5:25–30. Results of the mathematical expression evaluations executed by the kernel modules “are communicated back to the first cluster module 204a via the cluster node modules 204a-e, which communicates them to the user interface module.” *Id.* at 6:26–29. In short, “[i]ntercommunication provided by cluster

computing permits exchange of information between nodes during the course of a parallel computation” to improve computational performance. *Id.* at 6:30–36.

D. Illustrative Claim

Petitioner challenges claims 1–30 of the ’034 patent. Pet. 27–94. Claims 1, 25, 28, and 30 are the independent claims. Claims 2–24 depend, directly or indirectly, from claim 1. Claims 26–27 depend directly from claim 25. Claim 29 depends from claim 28. Claim 1, reproduced below with Petitioner’s bracketed identifiers, illustrates the claimed subject matter:

[1.0] A computer cluster comprising:

[1.1.1] a plurality of nodes, wherein each of the plurality of nodes comprises a hardware processor, [1.1.2] wherein one or more of the nodes are configured to receive a command to start a cluster initialization process for the computer cluster, and [1.1.3] wherein each of the nodes is configured to access a non-transitory computer-readable medium comprising program code for a single-node kernel that, when executed, is capable of causing the hardware processor to evaluate mathematical expressions; and

[1.2] a communications network interface for the nodes to communicate results of mathematical expression evaluation with each other using a peer-to-peer architecture;

[1.3.0] wherein the plurality of nodes comprises:

[1.3.1] a first node comprising a first hardware processor configured to access a first memory comprising program code for a user interface and program code for a first single-node kernel, [1.3.2] the first single-node kernel configured to interpret user instructions and distribute calls to at least one of a plurality of other nodes for execution; and

[1.4.1] a second node comprising *a second hardware processor with a plurality of processing cores*, [1.4.2] wherein the second node is configured to receive calls from the first node, execute at least a first mathematical expression evaluation, and

communicate a result of the first mathematical expression evaluation to a third node;

[1.5.1] wherein the third node comprises *a third hardware processor with a plurality of processing cores*, [1.5.2] wherein the third node is configured to receive the result of the first mathematical expression evaluation from the second node, execute at least a second mathematical expression evaluation using the received result, and communicate the result of the second mathematical expression evaluation to the first node;

[1.6] wherein the first node is configured to return the result of the second mathematical expression evaluation to the user interface;

[1.7.0] wherein one or more of the nodes are configured to:

[1.7.1] accept user instructions;

[1.7.2] after accepting user instructions, communicate at least some of the user instructions using the communications network interface for the nodes to communicate with each other; and

[1.7.3] after communicating at least some of the user instructions using the communications network interface, communicate at least some of the user instructions to one or more single-node kernels.

Ex. 1001, 29:30–30:13 (emphases added).

E. Prior Art and Asserted Grounds

Petitioner asserts claims 1–30 are unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–25, 27–28, 30	103(a) ²	Menon, ³ Trefethen, ⁴ RS6000, ⁵ POEref, ⁶
26, 29	103(a)	Menon, Trefethen, RS6000, POEref, MPIref ⁷

Pet. 14. Petitioner relies on the declaration of Chandrajit L. Bajaj, Ph.D. (Ex. 1003) in support of the Petition. Patent Owner relies on the declaration of Melissa Smith, Ph.D. (Ex. 2017) in support of the Preliminary Response.

² The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), includes revisions to 35 U.S.C. §§ 102 and 103 that became effective after the filing date of the earliest priority application that led to the challenged patent. Hence, this *inter partes* review is governed by the pre-AIA provisions of 35 U.S.C. §§ 102 and 103.

³ *MultiMATLAB: Integrating MATLAB with High-Performance Parallel Computing*, Menon et al., SC '97: Proceedings of the 1997 ACM/IEEE Conference on Supercomputing 1997 (“Menon”) (Ex. 1005).

⁴ *MultiMATLAB: MATLAB on Multiple Processors*, Trefethen et al., 1996 Computer Science Technical Report, Cornell University 1996 (“Trefethen”) (Ex. 1006).

⁵ RS6000 SP: Planning Vol. 1, *Hardware and Physical Environment*, IBM 2001 (“RS6000”) (Ex. 1007).

⁶ Operation and Use, Volume 1, *Using the Parallel Operating Environment*, IBM 2001 (“POEref”) (Ex. 1008).

⁷ *MPI: A Message-Passing Interface Standard*, Message Passing Interface Forum, 1994 (“MPIref”) (Ex. 1017).

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner contends:

A person of ordinary skill in the art (“POSITA”) in June 2006 would have been someone knowledgeable of and familiar with computer cluster systems and cluster computing techniques available at the time. Such a POSITA would have a bachelor’s degree in computer science, computer engineering, electrical engineering, or an equivalent training, and approximately two years of experience working in the field of cluster computing or parallel processing and would be knowledgeable regarding high-level scientific computing languages. Additional work experience can substitute for specific educational background, and vice versa.

Pet. 12 (citing Ex. 1003 ¶¶ 18–23); *see also* Ex. 1003 ¶¶ 24–27 (addressing level of ordinary skill in the art). Patent Owner does not address the level of skill in the art directly, although Dr. Smith characterizes the level of ordinary skill in the field of cluster computing at the time of the ’034 patent in a manner consistent with the Petition and Dr. Bajaj. *See generally* Prelim. Resp.; *see also* Ex. 2017 ¶¶ 21–22 (POSITA having “Bachelor’s degree in computer science, electrical engineering, or an equivalent field, and two years of academic or industry experience in cluster computing and parallel computation techniques”).

In determining the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (citing *Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986)). “These factors are not exhaustive but are merely a

guide to determining the level of ordinary skill in the art.” *Daiichi Sankyo Co. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007). There is uncontested evidence in the record before us that reflects the knowledge and experience of a POSITA.

For purposes of this Decision, we adopt the Petition’s formulation of the level of ordinary skill in the art, which is consistent with the description in the ’034 patent, the prior art of record, and the testimony of both experts.

B. Claim Construction

In this *inter partes* review, we apply the same claim construction standard that would be used in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b). In applying this standard, we generally give claim terms their ordinary and customary meaning as would be understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005) (en banc). Claim terms “are generally given their ordinary and customary meaning” as understood by a POSITA at the time of the invention. *Phillips*, 415 F.3d at 1312. When construing a disputed claim limitation, “we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner relies on the ordinary and customary meaning of the claim terms consistent with the *Phillips* standard. Pet. 12–13 (citing 37 C.F.R. § 42.100(b)). The Petition addresses the construction of “*peer-to-peer architecture*” recited in independent claims 1 and 30 of the ’034 patent, a limitation we need not construe to decide the institution question. *Id.* at 13;

see, e.g., *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“[C]laim terms need only be construed ‘to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Patent Owner contends that “no claim construction is required” to address the Petition’s asserted deficiencies. Prelim. Resp. 6.

Patent Owner also contends, however, that the Petition relies on a “novel claim construction” of limitations [1.4.1] and [1.5.1]—“*second [third] hardware processor with a plurality of processing cores*”—to support Petitioner’s obviousness argument. *Id.* at 11–12.⁸ Patent Owner challenges the Petition’s reliance on “single core processors on different chips,” such as the Power3 single-core processors of the Symmetric Multi-Processor (“SMP”) configuration disclosed in the RS6000 reference, as a disclosure of limitations [1.4.1] and [1.5.1]. *Id.* Patent Owner contends that such single-core processors on different chips do not satisfy limitations [1.4.1] and [1.5.1] because the ’034 patent “claims only multicore processors.” Prelim. Resp. 5 (citing Ex. 1001, 7:15–27).

Petitioner responds in part as follows:

To the extent PO is implicitly arguing that RS6000’s “four, eight, twelve, or sixteen 375 MHz 630FP 64-bit processors” do not teach the recited “cores,” Patent Owner’s argument excludes embodiments described in the ’034 patent’s specification. The ’034 patent describes “[p]rocessor cores [as] generally independent microprocessors.” Ex.1001, 5:14–15. Patent Owner’s attempt to exclude RS6000 from the scope of the claims

⁸ Pursuant to the Board’s Order on Related Matter Updates (Paper 14), the parties filed the September 26, 2025 Claim Construction Order entered in the co-pending District Court litigation in this proceeding. Ex. 1085. The District Court Claim Construction Order did not construe the claim phrase “*hardware processor with a plurality of processing cores*.” *Id.*

correspondingly excludes the embodiments described in the '034 patent where the processor has independent microprocessors. Patent Owner's attempt to distinguish RS6000's Symmetric MultiProcessor as a "configuration" (Paper 8, 24) also fails because a "Symmetric MultiProcessor configuration" is no different than the '034 patent's description of a configuration of independent microprocessors. *Id.*

Paper 9, 30.⁹ It is apparent there is a dispute over the plain meaning of Limitations [1.4.1] and [1.5.1], "*a second [third] hardware processor with a plurality of processing cores,*" recited in the independent claims.¹⁰ The parties are ordered to propose and support a particularized plain meaning or other construction of Limitations [1.4.1], [1.5.1], and [30.1.2] in their briefs. The parties are ordered to analyze the relevant claim language and cite to the specification and prosecution history in support of their claim construction, where applicable, with particular attention to the description of a hardware processor with a plurality of processing cores in the '034 patent. *See, e.g.,* Ex. 1001, 5:11–37, 7:14–36, 9:50–10:3.

We address the Petition Grounds 1 and 2 below.

C. Asserted Obviousness of Claims 1–25, 27–28, and 30

Ground 1 in the Petition contends that claims 1–25, 27–28, and 30 of the '034 patent are obvious over Menon in view of Trefethen, RS6000 and POEref. Pet. 16–87 (citing Ex. 1003 ¶¶ 65–89, 104–108, 113–115, 118, 121–122, 157–465). The Petition asserts that Menon in view of Trefethen, RS6000 and POEref discloses, teaches, suggests or otherwise renders obvious all of the limitations recited in the claims. *Id.* Patent Owner

⁹ Paper 9 is Petitioners' Opposition to Patent Owner's Request for Discretionary Denial filed August 27, 2025.

¹⁰ Independent claim 30 similarly recites "*wherein the hardware processor comprises multiple processor cores*" in limitation [30.1.2].

contends Petitioner has failed to meet its burden to show a reasonable likelihood that at least one of the challenged claims is unpatentable, because the references do not “describe nodes comprising a hardware processor with multiple processing cores” as recited in Limitations [1.4.1] and [1.5.1]. Prelim. Resp. 1–2, 7–13 (citing Ex. 2017 ¶¶ 27–34). Patent Owner further contends the Petition fails to establish that Menon, Trefethen, RS6000, POEref, and MPIref (Exhibits 1005–1008 and 1017) qualify as prior art printed publications under 35 U.S.C. § 102(a). *Id.* at 13–33.

“In an *inter partes* review, the burden of persuasion is on the petitioner to prove ‘unpatentability by a preponderance of the evidence,’ 35 U.S.C. § 316(e), and that burden never shifts to the patentee.” *In re Magnum Oil Tools Int’l Ltd.*, 829 F.3d 1364, 1375 (Fed. Cir. 2016) (quoting *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015)); *see also Aqua Products, Inc. v. Matal*, 872 F.3d 1290, 1306 (Fed. Cir. 2017 (en banc (quoting *Magnum Oil*))).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (quoting 35 U.S.C. § 103(a)). Obviousness is resolved based on underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). A party who petitions the Board for a determination of obviousness must show that “a skilled artisan would have been motivated to

combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.” *Procter & Gamble Co. v. Teva Pharms. USA, Inc.*, 566 F.3d 989, 994 (Fed. Cir. 2009) (quoting *Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1361 (Fed. Cir. 2007)).

We assess Petitioner’s evidence and argument according to the above-referenced obviousness standard. We determine that the Petition satisfies the reasonable likelihood of prevailing standard under 35 U.S.C. § 314(a). We begin our analysis with a discussion of the Menon, Trefethen, RS6000, and POEref references.

1. Overview of Menon (Ex. 1005)

Menon, titled “MultiMATLAB: Integrating MATLAB with High-Performance Parallel Computing,” is directed to a computing environment architecture that enables MATLAB to operate in parallel on multiple microprocessors. Ex.1005, Title, Abstract. Menon describes MultiMATLAB as “a general extension” of the MATLAB computing platform for running “high-performance parallel routines.” *Id.* at Abstract. MultiMATLAB comprises several microprocessors, each configured to run a MATLAB process that communicates “with other processes through a communication layer that runs over the parallel platform’s interconnection network.” *Id.* at 3, Fig. 1. The communication layer uses Message Passing Interface (“MPI”) to communicate “over the parallel platform’s interconnection network.” Ex.1005, 3, 5. Menon Figure 1 is reproduced below:

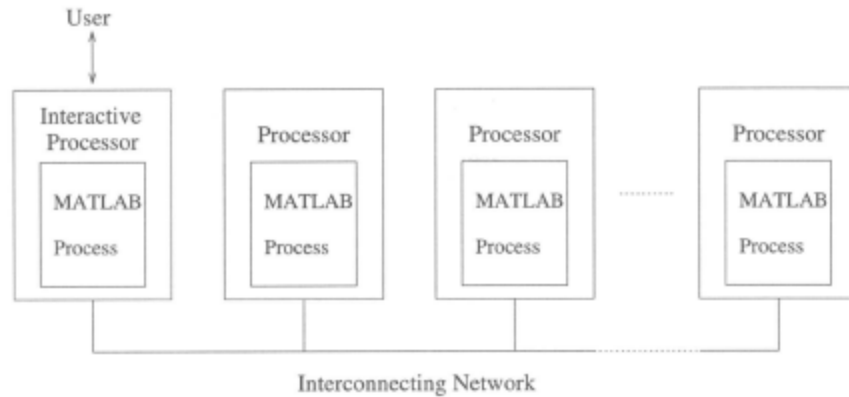


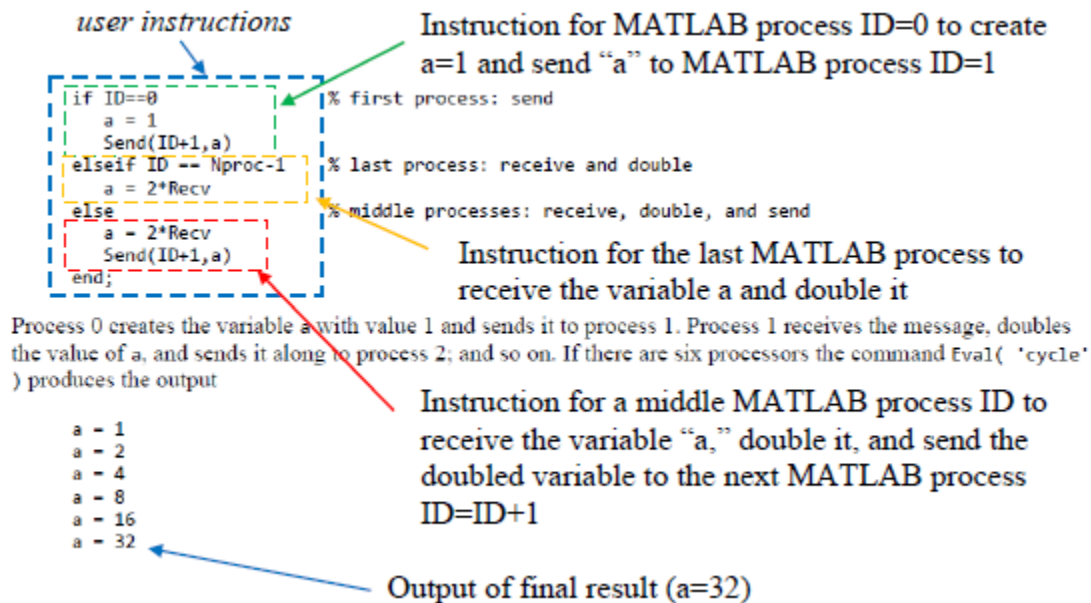
Figure 1: MultiMATLAB Architecture

As shown in Figure 1, in Menon’s MultiMATLAB architecture a user “interacts directly with ... the interactive process,” and the “other processes wait for commands from the interactive MATLAB process.” *Id.* at 3, 6. Menon discloses using MultiMATLAB on a “parallel platform,” such as “the IBM SP2” and “IBM RS6000,” to calculate mathematical expressions. *Id.* at 2, 5, 11. Menon explains that MultiMATLAB works with different parallel programming paradigms, including “SPMD/Message passing” that provides “point to point” communication. *Id.* at 8–10; Table 1. Menon discloses that MultiMATLAB uses “MEX Routines,” an “interface module,” “indirection table,” and a “communication layer” to provide direct point-to-point communication between modules. Ex.1003, ¶¶ 104–106; Ex. 1005, 3, 5.

2. Overview of Trefethen (Ex. 1006)

Trefethen, titled “MultiMATLAB: MATLAB on Multiple Processors,” discloses a system “that enables one to run MATLAB conveniently on multiple processors,” such as in the “IBM SP2,” “for fast and convenient execution of easily parallelizable numerical computations on multiple processors.” Ex. 1006, 1 (Abstract); *see also id.* at 3–9. Trefethen discloses that “point-to-point communication is accomplished by send and

receive commands.” *Id.* at 5–6. Trefethen teaches the use of “Send” and “Recv” commands to allow direct communication among nodes, as shown in annotated form in the Petition, reproduced below:



Pet. 21 (annotated Ex.1006, 6). The sample code shown above illustrates:

- node 0 sending data “a = 1” to node 1,
- node 1 performing a mathematical calculation (multiply “a” by 2) and sending the result to node 2,
- node 2 performing a mathematical calculation (multiply “a” by 2) and sending the result to the next node (“and so on”), and
- the result (a=32) is output to the user.

Id. (citing Ex. 1003 ¶ 115; Ex. 1006, 6).

3. Overview of RS6000 (Ex. 1007)

RS6000, titled “RS/6000 SP: Planning Vol. 1, Hardware and Physical Environment,” is asserted to be an IBM product manual for the IBM SP2 system used in Menon. Pet. 15, 21–22 (citing Ex.1003 ¶ 118–120; Ex.1007,

1–2;¹¹ Ex. 1010, 6; Ex. 1029; Ex. 1038). RS6000 discloses that the “RS6000 SP is IBM’s family of scalable, parallel computing solutions” and that the system includes POWER3 processors for executing “both serial and parallel applications.” Ex. 1007, 1. RS6000 discloses that “[t]he IBM RS/6000 SP System is scalable from one to 128 processor nodes” and that it uses “four, eight, twelve, or sixteen 375 MHz 630FP 64-bit processors per node.” *Id.* at 2, 9.

4. *Overview of POEref (Ex. 1008)*

POEref, titled, “Operation and Use, Volume 1, Using the Parallel Operating Environment” is asserted to be an IBM product manual for “the IBM Parallel Environment (PE)” and “its Parallel Operating Environment (POE)” running on an RS6000 system, as referenced in Menon. Pet. 15, 22 (citing Ex.1003 ¶¶ 121–125; Ex.1005, 6; Ex.1008, 11¹²; Ex. 1029; Ex. 1039). POEref discloses an initialization process where a user enters the “poe” command, such that “[w]hen you invoke **poe**, the Partition Manager allocates processor nodes for each task and initializes the local environment. It then loads your program, and reproduces your local environment, on each processor node.” Ex.1008, 46.

5. *Analysis of Claim 1 in View of Menon, Trefethen, RS6000, and POEref*

Petitioner asserts that claim 1 would have been obvious over Menon, Trefethen, RS6000, and POEref. Pet. 22–53 (citing Ex. 1003 ¶¶ 65–89, 118, 124, 132–133, 157–243). Our analysis of independent claim 1 applies

¹¹ We cite to the exhibit page numbers added to the lower right corner of Ex. 1007, rather than the internal page numbers of RS6000.

¹² We cite to the exhibit page numbers added to the lower right corner of Ex. 1008, rather than the internal page numbers of POEref.

equally to independent claims 25, 28, and 30. For the reasons articulated below, on the present record at this stage of the proceeding, we determine Petitioner has established a reasonable likelihood of showing that at least independent claims 1, 25, 28, and 30 of the '034 patent are unpatentable as obvious over Menon, Trefethen, RS6000, and POEref.

Motivation to Combine and Analogous Art

The Petition offers several motivations to combine Menon, Trefethen, RS6000, and POEref in the manner claimed in the '034 patent with a reasonable expectation of success, which we find sufficient on the present record.

The Petition first asserts that Menon and Trefethen are analogous prior art because they pertain to the same “field of cluster computing” as the '034 patent and “are reasonably pertinent to the problem of the '034 patent, namely, executing a single program on multiple nodes.” Pet. 22 (citing Ex.1001, 1:14–15; Ex.1003, ¶¶ 65–69; Ex. 1005, 2; Ex. 1006, Abstract). The Petition points out that Menon expressly cites and builds on the MultiMATLAB system taught by Trefethen. *Id.* (citing Ex. 1003 ¶ 71; Ex. 1005, 1–2). The Petition also contends that:

Accordingly, Menon and Trefethen together represent a combination of prior art elements according to known methods (executing MATLAB code on a multiprocessor system) to yield the predictable result discussed in both papers: the MultiMATLAB system executing MATLAB in parallel to perform mathematical calculations.

Id. at 22–23 (citing Ex. 1003 ¶ 70; Ex.1005, Abstract; Ex. 1006, 2–7). The Petition further contends that a POSITA would have found it predictable to combine Trefethen with Menon with a reasonable expectation of success

“because researchers had a strong desire to parallelize MATLAB.” *Id.* at 23–24 (Ex. 1003 ¶ 73; Ex. 1005, 2; Ex. 1006, 11–12.)

The Petition next explains the asserted motivation for combining RS6000 with Menon, namely, because RS6000 provides an overview of the IBM SP2 multiprocessor and Menon teaches the use of “IBM SP2, a modern high performance distributed memory multiprocessor” in the MultiMATLAB system. *Id.* at 24–25 (citing Ex. 1003 ¶¶ 78–81; Ex.1005, 5–6, 14; Ex. 1007, 1, 11). The Petition also analyzes the POEref reference as in the field of cluster computing. *Id.* at 26 (citing Ex.1008, 11 (“PE Software is designed to run on an ... RS/6000 network cluster”)); (further citing Ex.1001, 1:14–15; Ex.1003 ¶¶ 82–85). The Petition further contends that a POSITA would have been motivated to combine the teachings of POEref with Menon “because Menon suggests the combination by teaching that MultiMATLAB uses ‘POE, IBM's Parallel Operating Environment.’” *Id.* at 26–27 (citing Ex.1005, 6); (further citing Ex. 1003 ¶¶ 86–89; Ex. 1005, 14; Ex. 1008, 11, 46).

Patent Owner does not address the Petition’s contentions regarding motivation to combine the cited references with a reasonable expectation of success. Prelim. Resp. 7–33.

On the present record at this stage of the proceeding, we determine that Menon, Trefethen, RS6000, and POEref are analogous art in the same field of cluster computing as the ’034 patent. We further determine that, on the present record, the Petition sufficiently supports a motivation to combine Menon, Trefethen, RS6000, and POEref with a reasonable expectation of success for the reasons articulated in the Petition and Dr. Bajaj’s cited declaration paragraphs.

We now turn to the question of whether the Petition demonstrates a reasonable likelihood that Menon, Trefethen, RS6000, and POEref disclose, teach, suggest, or otherwise render obvious claim 1 of the '034 patent.

Limitation [1.0]: *“A computer cluster comprising:”*

The Petition contends that Menon discloses Limitation [1.0] because Menon discloses a “MultiMATLAB architecture” providing “high-performance parallel routines” using a cluster of multiple nodes, where each node “runs a MATLAB process” and “communicate[s] with other processes through a communication layer.” Pet. 27 (citing Ex.1005, 2–3). The Petition particularly points out that the IBM SP2 system “execute[s] parallel programs on . . . a **networked cluster** of . . . RS/6000 processors.” *Id.* at 28 (citing Ex.1008, 1); (further citing Ex. 1003 ¶¶ 157–163; Ex. 1005, 13, Figs. 1, 7, 8). Petitioner’s contention is consistent with the cited disclosures in Menon and POEref, further supported by Dr. Bajaj’s declaration testimony.

Patent Owner does not address this limitation. Prelim. Resp. 7–33.

On the present record, Menon, POEref, and the Bajaj Declaration adequately support Petitioner’s contention that Menon discloses Limitation [1.0].

Limitation [1.1.1]: *“a plurality of nodes, wherein each of the plurality of nodes comprises a hardware processor,”*

The Petition contends that Menon in view of RS6000 renders Limitation [1.1.1] obvious because Menon teaches running “MultiMATLAB” on “the IBM SP2” with “32 processors” (“a plurality of nodes”). Pet. 29 (citing Ex. 1003 ¶¶ 124, 164–166; Ex.1005, 5, 13, Fig. 1 (annotated); Ex. 1007, 1–2). The Petition illustrates a plurality of nodes in the MultiMATLAB architecture with an annotated version of Menon Figure 1, reproduced below:

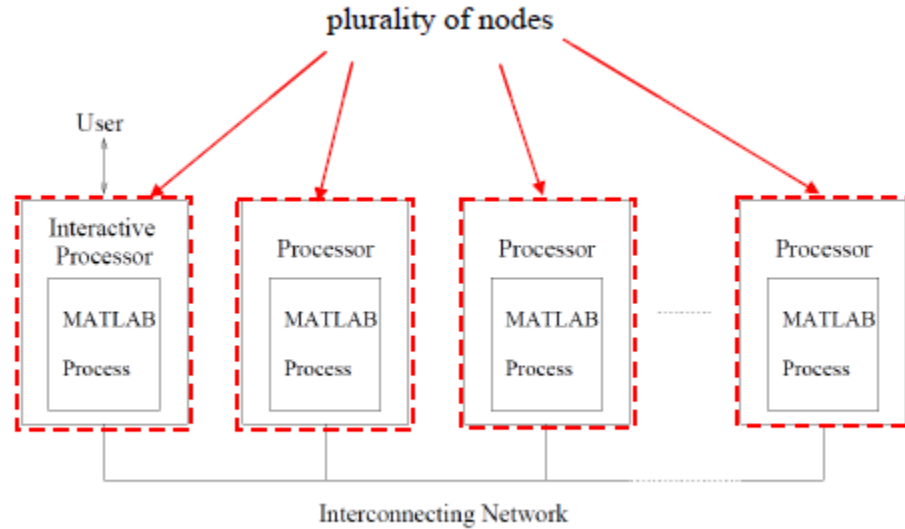


Figure 1: MultiMATLAB Architecture

Id. Thus, the Petition contends that Menon discloses running MultiMATLAB using 32 processor nodes on an IBM SP2, and RS6000 “teaches that each IBM SP2 node has a symmetric multiprocessor, rendering obvious” Limitation [1.1.1]. *Id.* (citing Ex. 1003 ¶¶ 164–166). Dr. Bajaj testifies that each processor node “can have up to sixteen processors.” Ex. 1003 ¶ 164.

Patent Owner does not address this limitation. Prelim. Resp. 7–33.

On the present record, Menon, RS6000 and the Bajaj Declaration adequately support Petitioner’s contention that Menon renders obvious Limitation [1.1.1].

Limitation [1.1.2]: “*wherein one or more of the nodes are configured to receive a command to start a cluster initialization process for the computer cluster, and*”

The Petition contends that Menon discloses an interactive process node in the MultiMATLAB architecture (see annotated Figure 1, above) that receives a user command “to start the MATLAB processes using IBM’s POE [Parallel Operating Environment].” Pet. 30 (citing Ex. 1003 ¶¶ 167–170; Ex. 1005, 4; Ex. 1008, 46). The Petition also contends that, upon

initialization, the non-interactive MATLAB process nodes wait for commands. *Id.* The Petition further contends that POEref discloses a “poe” command that “initializes a local environment and reproduces that local environment on each remote processor node,” which renders Limitation [1.1.2] obvious. *Id.* Dr. Bajaj testifies as follows:

The user invokes the initialization process using the “poe” command:

When you invoke **poe**, the Partition Manager allocates processor nodes for each task and initializes the local environment. It then loads your program, and reproduces your local environment, on each processor node. The Partition Manager also passes the option list to each remote node. ... If you are using the dynamic message passing interface, the appropriate communication subsystem library implementation (IP or US) is automatically loaded at this time.

Ex. 1003 ¶ 168 (citing Ex. 1005, 6).

Patent Owner does not address this limitation. Prelim. Resp. 7–33.

On the present record, Menon, POEref, and the Bajaj Declaration adequately support Petitioner’s contention that Menon and POEref render obvious Limitation [1.1.2].

Limitation [1.1.3]: “*wherein each of the nodes is configured to access a non-transitory computer-readable medium comprising program code for a single-node kernel that, when executed, is capable of causing the hardware processor to evaluate mathematical expressions; and*”

The Petition first points out that the ’034 patent identifies MATLAB as an example of a single-node kernel capable of executing a process. Pet. 31 (citing Ex. 1001, 4:14–21); *see also* Ex. 1001, 4:21–28 (referencing MATLAB® application software). Below is an annotated version of Menon

Figure 2 from the Petition that illustrates a MATLAB single-node kernel:

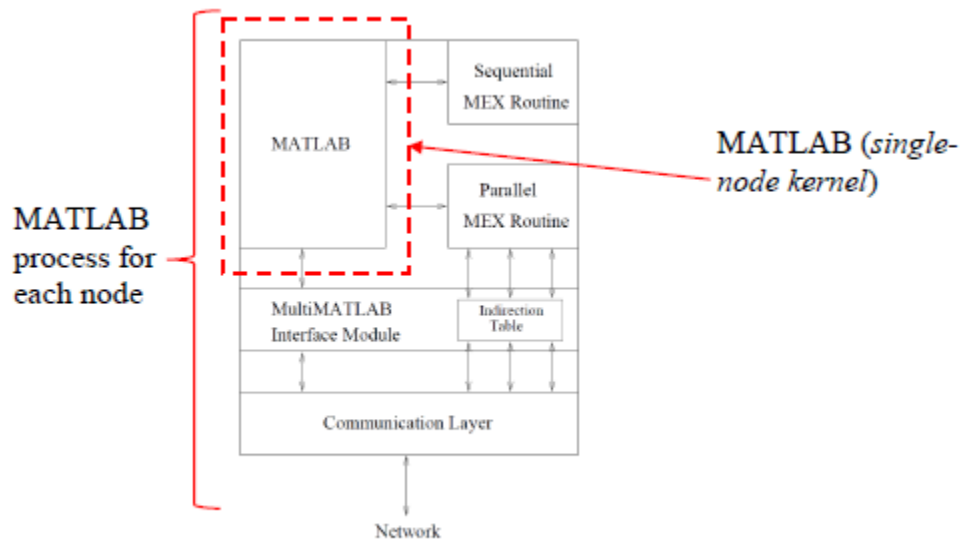


Figure 2: MATLAB Process Address Space

Pet. 32 (citing Ex. 1003 ¶ 133; Ex. 1005, Fig. 2 (annotated)). The Petition contends that “a POSITA would recognize MATLAB is *program code* executed by a *hardware processor*,” with “each node executing a *single-node kernel*.” *Id.* (citing Ex.1003 ¶ 174; Ex.1005, 3; Ex.1006, 2; Ex.1007, 3). The Petition further contends that “MATLAB (*a single-node kernel*) causes the hardware processor of the IBM SP2 node to perform mathematical calculations (*program code ... capable of causing a hardware processor to evaluate mathematical expressions*),” and that MATLAB program code is accessed from a *computer-readable medium*. *Id.* at 32–33 (citing Ex. 1003 ¶¶ 171–182; Ex. 1005, 11–13, Figs. 2, 5; Ex. 1006, 2–6; Ex. 1007, 6, 10; Ex. 1018, 67–68). Dr. Bajaj testifies that:

Menon and Trefethen teach MATLAB is capable of causing a processor to evaluate mathematical expressions, as illustrated by the “MultiMATLAB implementations of the conjugate gradients algorithm on the IBM SP2” discussed in Menon and mathematical evaluations such as arithmetic operations (e.g., doubling a value, calculating square root of numbers, etc.), singular value decomposition, fast Fourier transform,

polynomial zerofinding, and matrix operations (e.g., calculations of eigenvalues and condition number of Hilbert matrices, etc.) discussed in Trefethen.

Ex. 1003 ¶ 175 (citing Ex. 1005, 11–13; Ex. 1006, 2–6).

Patent Owner does not address this limitation. Prelim. Resp. 7–33.

On the present record, Menon, Trefethen, RS6000, and the Bajaj Declaration adequately support Petitioner’s contention that the cited references render obvious Limitation [1.1.3].

Limitation [1.2]: *“a communications network interface for the nodes to communicate results of mathematical expression evaluation with each other using a peer-to-peer architecture;”*

The Petition contends that Menon and Trefethen describe MultiMatlab running on an IBM SP2, where the processor nodes are linked by a network via “MEX routine” commands that use a “point to point . . . communication” paradigm. Pet. 34–36 (citing Ex. 1003 ¶ 188; Ex. 1005, 3–5, 9, Table 1; Ex. 1006, 4, 6, 10). The Petition provides annotated Figure 1 from Menon that depicts an interconnection network linking the MultiMATLAB processor nodes:

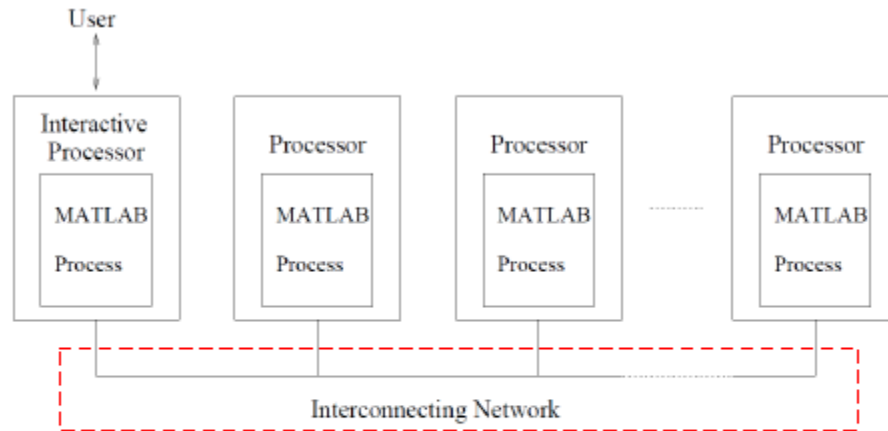


Figure 1: MultiMATLAB Architecture

Ex.1005, FIG. 1 (annotated); Ex.1003, ¶145

Interconnecting network connecting each MATLAB process on a processor node to the others

Id. at 34–35 (citing Ex. 1003 ¶ 145; Ex. 1005, 5, Fig. 1 (annotated)). The Petition contends that Menon’s point-to-point communication paradigm, where each node can communicate tasks and data directly with any other node, renders obvious the recited “*peer-to-peer architecture.*” *Id.* at 36–37 (citing Ex. 1003 ¶ 149; Ex. 1005, 9, Table 1 (annotated)).

The Petition relies on Trefethen as teaching an example script for a MATLAB process using point-to-point commands to communicate “*results of mathematical expression evaluation*” directly to another processor node in a six-processor cluster. *Id.* at 37–38 (citing Ex. 1003 ¶ 190; Ex.1006, 3–4, 6). The Petition further relies on the detailed description in RS6000 of the IBM SP2’s network hardware for connecting the nodes, including Ethernet adapters and a switch that “provide[s] a message-passing network that connects all processor nodes with a minimum of four paths between every pair of nodes.” *Id.* at 38–39 (citing Ex. 1003 ¶¶ 183–193; Ex. 1007, 2, 4, 10). The Petition argues that Menon, in view of Trefethen and RS6000 renders obvious Limitation [1.2]. *Id.* at 39 (citing Ex. 1003 ¶¶ 183–193).

Patent Owner does not address this limitation. Prelim. Resp. 7–33.

On the present record, Menon, Trefethen, RS6000, and the Bajaj Declaration adequately support Petitioner’s contention that the cited references render obvious Limitation [1.2].

Limitation [1.3.0]: *“wherein the plurality of nodes comprises:*

Limitation [1.3.1]: *“a first node comprising a first hardware processor configured to access a first memory comprising program code for a user interface and program code for a first single-node kernel, ”*

The Petition contends a POSITA would recognize that MATLAB is program code executed by a hardware processor, where each node executes a single-node kernel. Pet. 40 (citing Ex.1003, ¶ 199; Ex.1005, 3; Ex.1006, 2; Ex.1007, 3). The Petition emphasizes Menon’s disclosure that “[t]he user interacts directly with one MATLAB process, called the interactive process,” such that a user can “specify geometries, differential equations, and boundary conditions.” *Id.* (citing Ex.1005, 3, 6). The Petition argues that Menon in view of RS6000 renders obvious Limitations [1.3.0] and [1.3.1]. *Id.* at 39–40 (citing Ex. 1003 ¶¶ 195–200).

Patent Owner does not address this limitation. Prelim. Resp. 7–33.

On the present record, Menon, Trefethen, RS6000, and the Bajaj Declaration adequately support Petitioner’s contention that the cited references render obvious Limitations [1.3.0] and [1.3.1].

Limitation [1.3.2]: *“the first single-node kernel configured to interpret user instructions and distribute calls to at least one of a plurality of other nodes for execution; and”*

The Petition explains that Menon teaches an example of a user providing user instructions with “an Eval routine for parallel evaluation.” Pet. 40 (citing Ex.1005, 4). Trefethen teaches that MATLAB interprets the user instruction and calls the Eval MEX routine so that “the calls

‘cond(hilb(ID))’ are distributed to the MATLAB processes on processor ID=4 and ID=5 for each to perform.” *Id.* at 41 (citing Ex.1003 ¶ 203; Ex.1006, 4). The Petition contends that Menon in view of Trefethen render obvious Limitation [1.3.2]. *Id.* at 42 (citing Ex. 1003 ¶¶ 201–206).

Patent Owner does not address this limitation. Prelim. Resp. 7–33.

On the present record, Menon, Trefethen, and the Bajaj Declaration adequately support Petitioner’s contention that the cited references render obvious Limitation [1.3.2].

Limitation [1.4.1]: “*a second node comprising a second hardware processor with a plurality of processing cores,*”

Limitation [1.5.1]: “*wherein the third node comprises a third hardware processor with a plurality of processing cores,*”

The Petition contends that Menon discloses executing a series of MATLAB processes on 32 IBM SP2 processor nodes, as depicted in annotated Menon Figure 1, to illustrate “*a second [third] node comprising a second [third] hardware processor.*” Pet. 42–43, 45–46 (citing Ex. 1003 ¶¶ 168, 177; Ex. 1005, Fig. 1 (annotated); Ex. 1007, 2, 9). We reproduce below Menon Figure 1 (annotated) from the Petition:

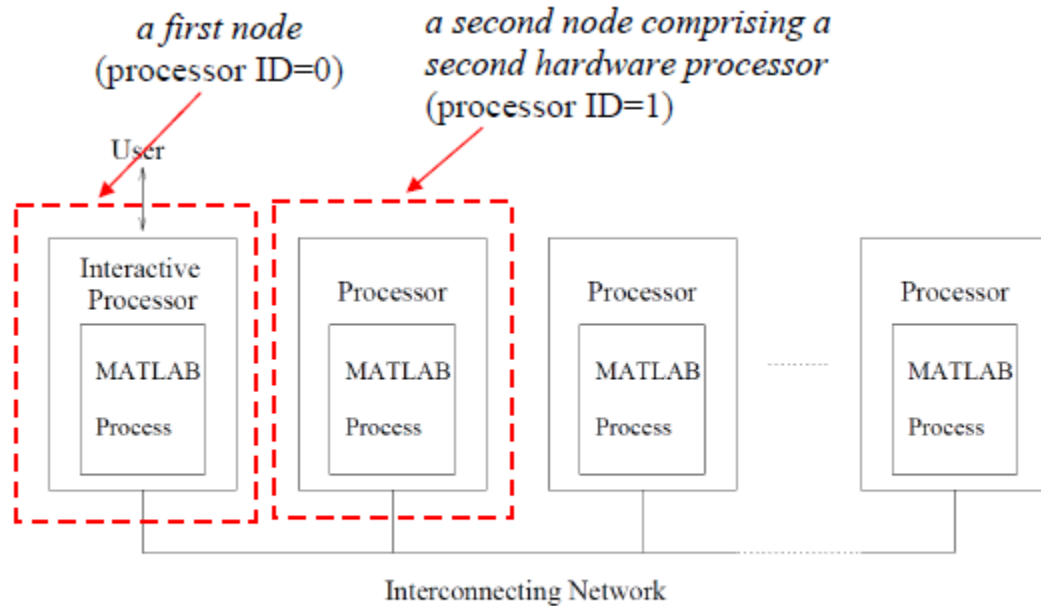


Figure 1: MultiMATLAB Architecture

Ex.1005, FIG. 1 (annotated); Ex.1003, ¶168

Id. Annotated Figure 1 depicts the MultiMATLAB architecture as including an interactive processor (“a first node”), as well as second and third nodes up to the n^{th} nodes, each comprising a MATLAB processor (“a second [third] hardware processor”).

The Petition further contends that RS6000 teaches “a second [third] hardware processor with a plurality of processing cores,” as follows:

RS6000 teaches that each node has a “Symmetric MultiProcessor (SMP)” (“hardware processor”) and that each SMP includes “four, eight, twelve, or sixteen 375 MHz 630FP 64-bit processors” (*plurality of processing cores*). Thus, each node has a hardware processor with a plurality of processing cores.

Menon and RS6000 teaching 32 IBM SP2 processor nodes, where each IBM SP2 node has a symmetric multiprocessor having up to sixteen processors (each having a core), renders obvious this limitation.

Id. at 43 (citing Ex. 1003 ¶¶ 207–210; Ex. 1007, 2, 9), 45–46 (citing Ex. 1003 ¶¶ 216–217). RS6000 discloses that “POWER 3 SMP High

Nodes . . . have four, eight, twelve, or sixteen [] processors *per node*.” Ex. 1007, 9 (emphasis added). Dr. Bajaj testifies that each node in the IBM SP2 system comprises an SMP multiprocessor that has “up to sixteen processors (each having a core).” Ex. 1003 ¶¶ 207–209, 216–217 (citing Ex. 1005, Fig. 1 (annotated); Ex. 1007, 2, 9). Dr. Bajaj concludes that, because each SP2 system node is comprised of a plurality of single-core microprocessors, Menon and RS6000 teach “*a hardware processor with a plurality of processing cores*” and render obvious Limitations [1.4.1] and [1.5.1]. *Id.* ¶¶ 209–210, 216–217.

Patent Owner contends that Limitations [1.4.1] and [1.5.1]) “recite[] a multicore processor, not a system with multiple processors or a multi-processor node.” Prelim. Resp. 7–12 (citing Smith Declaration Ex. 2017 ¶¶ 27–32). Patent Owner emphasizes that “the RS/6000 reference (Exhibit 1007) is discussing the number of processors and not the number of *processing cores within* its processors.” *Id.* at 9 (citing Ex. 2017 ¶¶ 27, 30). Dr. Smith likewise testifies that “the RS/6000 SMP configuration uses multiple hardware processors—but says nothing about each of the hardware processors having multiple processing cores.” Ex. 2017 ¶ 31; *see also id.* ¶¶ 28 (“The RS/6000 reference [] never states that any individual hardware processor has multiple processing cores.”), 30 (RS6000 “says nothing about the number of processing cores per hardware processor”).

As Petitioner notes, Patent Owner’s argument distinguishing Limitations [1.4.1] and [1.5.1] from Menon in view of RS6000 would appear to exclude the embodiment described in the ’034 patent where the claimed “*hardware processor*” for each node includes a plurality of independent single-core microprocessors. Paper 9, 29–30 (“Patent Owner’s argument excludes embodiments described in the ’034 patent’s specification.” (citing

Ex. 1001, 5:14–15)); *see also* Ex. 1001, 5:11–16 (“[E]ach processor can contain one or more processor cores that are capable of single-threaded execution. Processor cores are generally independent microprocessors, but more than one can be included in a single-chip package.”), 7:15–25 (“[t]he processors [] can be one or more general purpose single-core or multi-core microprocessors”). Patent Owner’s argument, in particular, appears to distinguish the IBM SP2 system taught by Menon and RS6000 because Patent Owner views each of the claimed “*second node*” and “*third node*” to require a single-chip multi-core microprocessor, to the exclusion of a plurality of single-core microprocessors.

On the present record, subject to receiving further argument and evidence from the parties as discussed above in the Claim Construction section and as ordered below regarding the construction of Limitations [1.4.1] and [1.5.1], we determine Petitioner has adequately supported its contention that Menon in view of RS6000 renders Limitations [1.4.1] and [1.5.1] obvious.

Limitation [1.4.2]: “*wherein the second node is configured to receive calls from the first node, execute at least a first mathematical expression evaluation, and communicate a result of the first mathematical expression evaluation to a third node;*”

Limitation [1.5.2]: “*wherein the third node is configured to receive the result of the first mathematical expression evaluation from the second node, execute at least a second mathematical expression evaluation using the received result, and communicate the result of the second mathematical expression evaluation to the first node;*”

The Petition contends that Menon teaches MEX routines having code to implement standard variants of MPI calls that enable point-to-point communication of tasks and data directly between nodes. Pet. 44 (citing Ex. 1005, 9). The Petition points out that each MATLAB process is assigned an

“identification number” and “wait[s] for commands from the interactive MATLAB process.” *Id.* (citing Ex.1005, 6). The Petition further establishes that Trefethen discloses a MultiMATLAB configuration with user instructions that cause: (i) the interactive MATLAB process to create variable *a* with a starting value (e.g. “*a=1*”) and communicate the variable to the next MATLAB process, and (ii) sequential MATLAB processes to receive variable *a* from the previous MATLAB process, double the value of the received variable (e.g. “*a=2**”), and send the result to the next MATLAB process. *Id.* (citing Ex.1006, 6 (annotated)). The Petition contends that the aforementioned teachings of Menon in view of Trefethen render obvious Limitations [1.4.2] and [1.5.2]. *Id.* at 45 (citing Ex. 1003 ¶¶ 211–215), 46–48 (citing Ex. 1003 ¶¶ 218–225).

Patent Owner does not address these limitations. Prelim. Resp. 7–33.

On the present record, Menon, Trefethen, and the Bajaj Declaration adequately support Petitioner’s contention that the cited references render obvious Limitations [1.4.2] and [1.5.2].

Limitation [1.6]: “*wherein the first node is configured to return the result of the second mathematical expression evaluation to the user interface;*”

The Petition explains that Menon discloses “[t]he user interacts directly with one MATLAB process, called the interactive process.” Pet. 48 (citing Ex.1005, 3). The Petition also explains that Trefethen discloses mathematical results being “sent to the user’s screen” when “one wishes to monitor the progress of computations on several processors graphically.” *Id.* (citing Ex.1006, 7). The Petition further explains that when the MATLAB process at processor ID=2 completes the operation of doubling the variable it has received from processor ID=1, MATLAB sends the result to the

interactive processor (“*a first node*”) to provide the result to the user (output result from third node, “*a=4*”) (see Limitation [1.5.2]). *Id.* The Petition contends that Menon’s interactive MATLAB process, in view of Trefethen’s use of MATLAB to display output and results on the user’s screen, render obvious this limitation. *Id.* at 49 (citing Ex.1003 ¶¶ 226–228).

Patent Owner does not address these limitations. Prelim. Resp. 7–33.

On the present record, Menon, Trefethen, and the Bajaj Declaration adequately support Petitioner’s contention that the cited references render obvious Limitation [1.6].

Limitation [1.7.0]: “*wherein one or more of the nodes are configured to:* [1.7.1] “*accept user instructions;*”

The Petition contends that Menon discloses a MultiMATLAB interactive processor having code for a user interface that allows users to input equations into MultiMATLAB. Pet. 49 (citing Ex. 1003 ¶ 231; Ex. 1005, Fig. 1 annotated)). We reproduce below Menon’s annotated Figure 1 from the Petition that depicts the MultiMATLAB architecture with an interactive processor node:

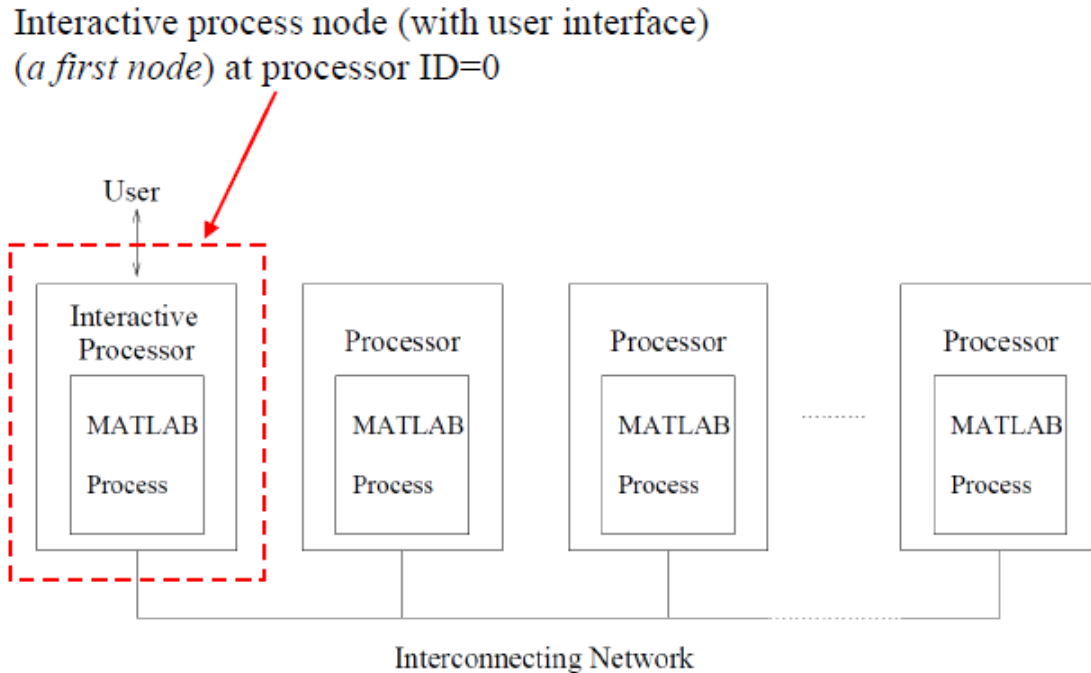


Figure 1: MultiMATLAB Architecture

Ex.1005, FIG. 1 (annotated); Ex.1003, ¶231

Id. The Petition contends that Menon’s disclosure of an interactive processor node (“one or more of the nodes”) that includes a user interface for receiving “user instructions,” in view of Trefethen’s teaching that MATLAB receives user instructions via an “m-file” input into MATLAB, renders obvious this limitation. *Id.* at 50 (citing Ex.1003 ¶¶ 230–234).

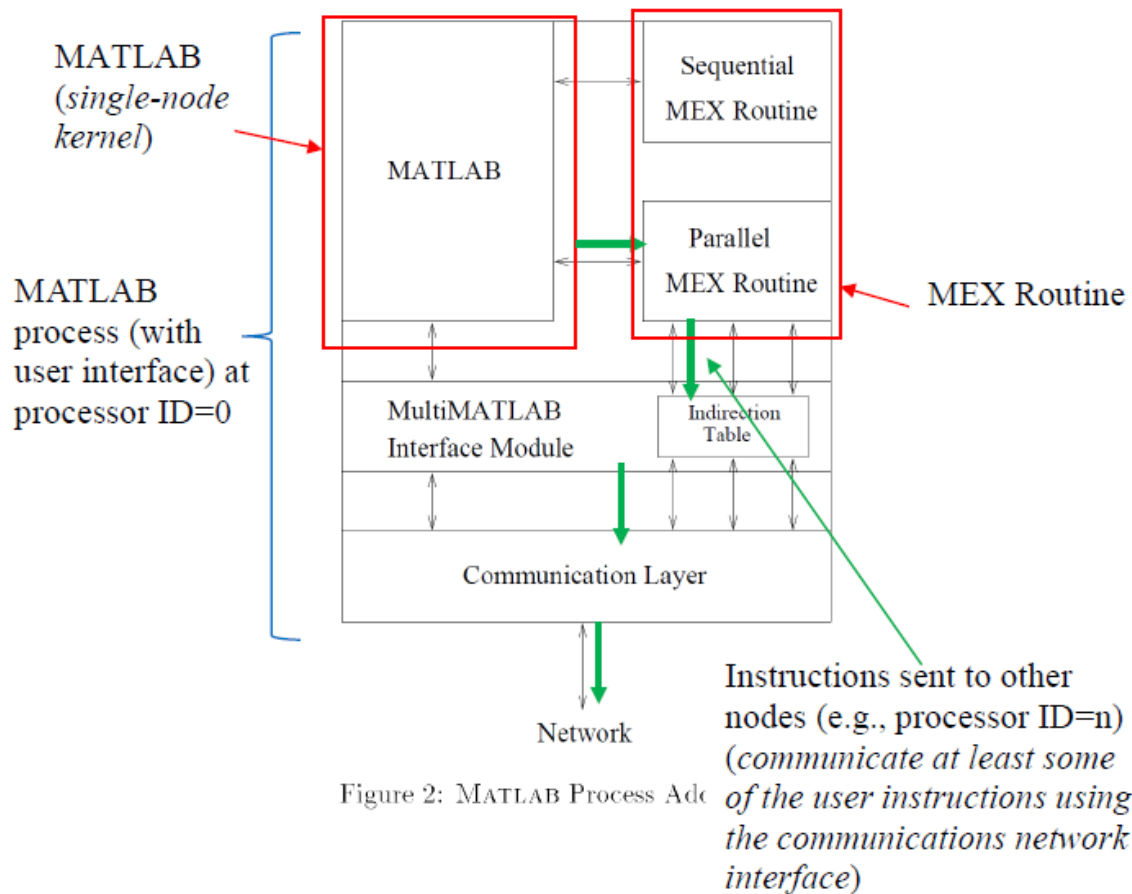
Patent Owner does not address these limitations. Prelim. Resp. 7–33.

On the present record, Menon, Trefethen, and the Bajaj Declaration adequately support Petitioner’s contention that the cited references render obvious Limitations [1.7.0] and [1.7.1].

[1.7.2] “after accepting user instructions, communicate at least some of the user instructions using the communications network interface for the nodes to communicate with each other; and”

The Petition explains that Menon discloses an interactive processor node (e.g., ID=0) in MultiMATLAB that sends commands to the other

MATLAB process nodes via a MEX Routine. Pet. 50–51 (citing Ex.1005, 4). The MEX Routine receives “MATLAB process IDs and a MATLAB command . . . [and] sends the commands over the underlying communication layer to the processes corresponding to the specified IDs.” *Id.* (quoting Ex. 1005, 4). Menon Figure 2 in the Petition depicts the process by which the interactive processor node sends commands to other MATLAB process nodes using the communication layer and interconnecting network. *Id.* at 51 (citing Ex. 1003 ¶ 238; Ex. 1005, Fig. 2 (annotated)). We reproduce annotated Figure 2 below from the Petition:



Ex.1005, FIG. 2 (annotated); Ex.1003, ¶238

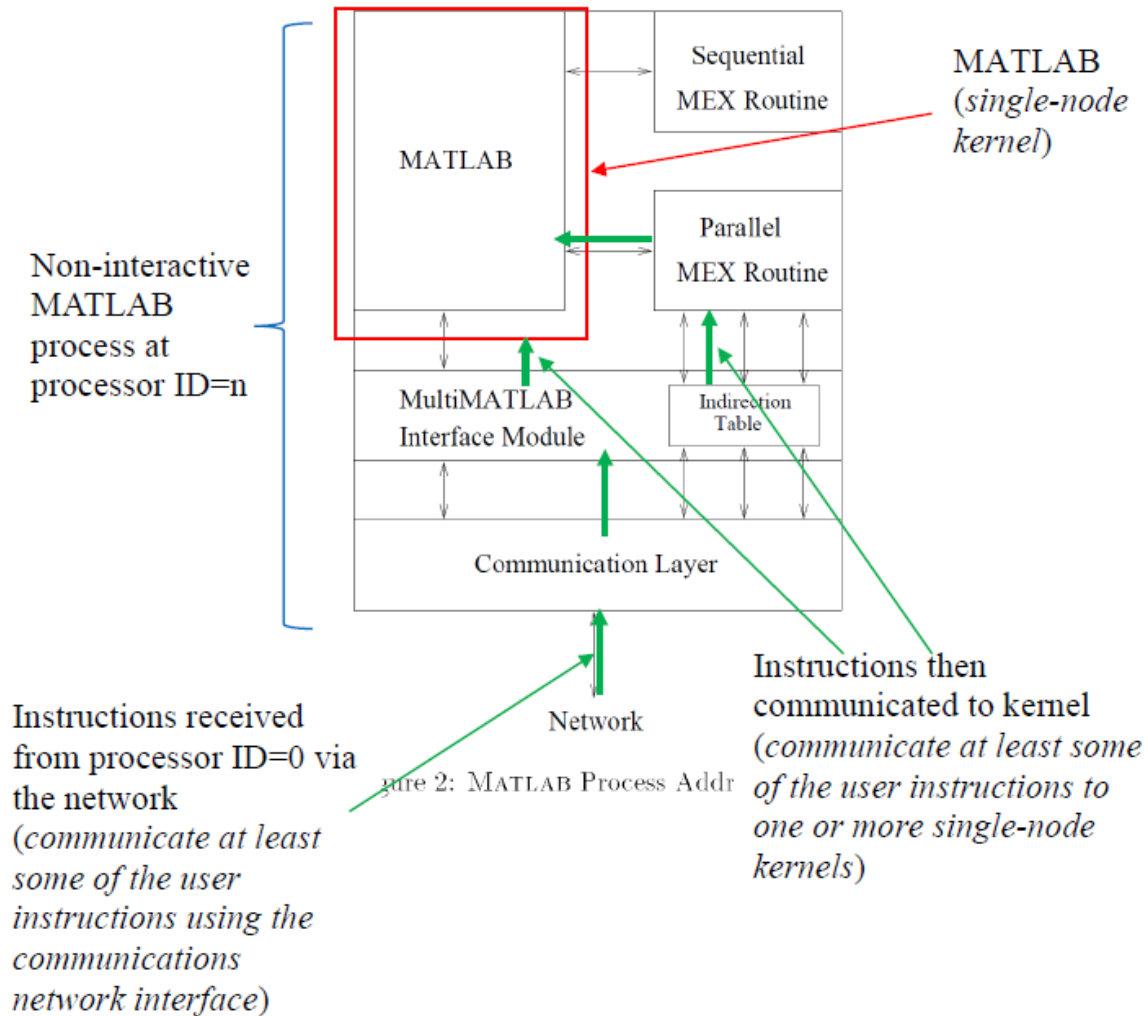
Id. The Petition contends that Menon in view of Trefethen renders obvious Limitation [1.7.2]. *Id.* at 51–52 (citing Ex. 1003 ¶¶ 235–239).

Patent Owner does not address this limitation. Prelim. Resp. 7–33.

On the present record, Menon, Trefethen, and the Bajaj Declaration adequately support Petitioner’s contention that the cited references render obvious Limitation [1.7.2].

Limitation [1.7.3]: *“after communicating at least some of the user instructions using the communications network interface, communicate at least some of the user instructions to one or more single-node kernels.”*

The Petition contends that Trefethen provides examples of commands, specified by ID number in “*user instructions*,” that are processed by the identified MATLAB process. Pet. 52 (citing Ex.1006, 3–7). For example, a user provides the instruction “Eval([4 5] , ‘cond(hilb(ID))’)” to the interactive MATLAB process node, and the calls “cond(hilb(ID))” (“*at least some of the user instructions*”) are distributed to the MATLAB process nodes (processor ID=4 and ID=5) for each to perform the instructed call. *Id.* (citing Ex. 1003 ¶ 242; Ex.1006, 4). We reproduce below annotated Figure 2 from the Petition that depicts the process by which user instruction calls are provided to “*one or more single-node kernels*” for processing:



Ex.1005, FIG. 2 (annotated); Ex.1003, ¶242

Id. at 53 (citing Ex. 1003 ¶ 242; Ex. 1005, Fig. 2 (annotated)). The Petition contends that Menon in view of Trefethen renders obvious Limitation [1.7.3]. *Id.* at 52–53 (citing Ex. 1003 ¶¶ 240–243).

Patent Owner does not address this limitation. Prelim. Resp. 7–33.

On the present record, Menon, Trefethen, and the Bajaj Declaration adequately support the Petition’s contention that the cited references render obvious Limitation [1.7.3].

6. Conclusion for Ground 1

For the reasons given above, we determine on the present record that the Petition adequately supports the assertion that Menon in combination with Trefethen, RS6000, and POEref discloses, teaches, suggests, or otherwise renders obvious independent claim 1.

We have reviewed the Petition’s argument and evidence in support of the contention that claims 2–25, 27–28, and 30 are also obvious over Menon in combination with Trefethen, RS6000, and POEref. Pet. 54–87 (citing Ex. 1003 ¶¶ 244–465). Patent Owner does not address the limitations recited in claims 2–25, 27–28, and 30 in the Preliminary Response. Prelim. Resp. 7–33. At this stage of the proceeding, we determine the argument and evidence presented in the Petition demonstrate a reasonable likelihood Petitioner would prevail in showing the unpatentability of claims 1–25, 27–28, and 30 as obvious over Menon in view of Trefethen, RS6000, and POEref.

D. Asserted Obviousness of Claims 26 and 29

The Petition adds MPIref to Menon, Trefethen, RS6000, and POEref to contend that claims 26 and 29 of the ’034 patent are obvious. Pet. 87–94 (citing Ex. 1003 ¶¶ 126–128, 467–544). Patent Owner does not address the limitations recited in claims 26 and 29. Prelim. Resp. 7–33. On the present record, Menon, Trefethen, RS6000, POEref, MPIref, and the Bajaj Declaration adequately support the Petition’s contention that the cited references render obvious claims 26 and 29.

E. Whether The Petition Has Demonstrated that Exhibits 1005–1008 and 1017 Qualify As Printed Publications

The Federal Circuit instructs that “[t]o qualify as a printed publication, a reference ‘must have been sufficiently accessible to the public

interested in the art.” *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1348 (Fed. Cir. 2016) (citing *In re Cronyn*, 890 F. 3d 1158, 1160 (Fed. Cir. 1989)). “A reference will be considered publicly accessible if it was ‘disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it.” *Id.* (citing *Kyocera Wireless Corp. v. Int’l Trade Comm’n*, 545 F.3d 1340, 1350 (Fed. Cir. 2008)). Further, the question of whether a document qualifies as a “printed publication” for the purposes of 35 U.S.C. § 102 “involves a case-by-case inquiry into the facts and circumstances surrounding the reference’s disclosure to a member of the public.” *Medtronic, Inc. v. Barry*, 891 F.3d 1368, 1380 (Fed. Cir. 2018) (citing *In re Klopfenstein*, 380 F.3d 1345, 1350 (Fed. Cir. 2004)).

At this stage of the proceeding, Petitioner “must identify, with particularity, evidence sufficient to establish a reasonable likelihood that the reference was publicly accessible before the critical date of the challenged patent and therefore that there is a reasonable likelihood that it qualifies as a printed publication.” *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29, 13 (PTAB Dec. 20, 2019) (precedential). The reasonable likelihood standard “is lower than the ‘preponderance’ standard to prevail in in a final written decision.” *Id.* The Petition relies on June 13, 2006 as the earliest possible priority date for the ’034 patent and contends that Exhibits 1005–1008 and 1017 qualify as “printed publications” published prior to June 13, 2006. Pet. 11 (“The ’034 patent’s earliest possible priority date is June 13, 2006”), 14–16.

1. Menon (Ex. 1005)

The Petition contends that Menon “is a paper authored by Vijay Menon and Anne Trefethen of the Cornell research team” and “qualifies as a

printed publication because it was published and distributed at the Proceedings of the 1997 ACM/IEEE Conference on Supercomputing 1997 [SC '97].” Pet. 14 (citing Ex. 1005; Ex. 1026; Ex. 1027). The Petition also contends that Menon was “published and distributed on Cornell’s website at least as early as 2001.” *Id.* (citing Ex. 1023; Ex. 1029). The Petition further contends that “Menon was reasonably located by POSITAs because it had been cited 17 times in papers prior to the priority date of the ’034 patent.” *Id.* (citing Ex. 1003 ¶¶ 121–123; Ex. 1028, 4–9; Ex. 1029, 1–3).

Patent Owner contends that the Petition’s evidence of the public accessibility of Menon is insufficient to qualify Menon as a printed publication under 35 U.S.C. § 102. Prelim. Resp. 13–32. Patent Owner contends that the Petition fails to show that Menon was presented at the SC ’97 conference, made publicly available on the Cornell Website, or otherwise made available to the public prior to June 13, 2006. *Id.* For example, Patent Owner contends that the declaration of IEEE custodian Gordan MacPherson, which states that IEEE conference proceedings including the Menon reference “were made available no later than the last day of conference” (Ex. 1027 ¶ 11), lacks “a foundational basis.” Prelim. Resp. 28–29. According to Patent Owner, the custodian “does not purport to have witnessed Exhibit 1005 being made available . . . nor does he include any business records that can corroborate his testimony or otherwise explain how or to who Exhibit 1005 was allegedly made available.” *Id.* at 29. Patent Owner further contends that the Petition offers no “evidence or explanation for how an interested person would have located particular URL addresses where Exhibit 1005 was allegedly accessible—only the bare and conclusory statement of Petitioner’s expert.” *Id.* at 27–28 (citing Ex. 1003 ¶ 110).

Based on the present record at this stage of the proceeding, we determine that the Petition shows a reasonable likelihood of establishing that Menon qualifies as a printed publication.

First, Mr. MacPherson is the Director, Board Governance & Policy Development at IEEE and testifies that “[i]t is the regular practice of IEEE to publish articles including article abstracts and make them available to the public through IEEE Xplore,” and that IEEE maintains copies of publications in the ordinary course of its business. Ex. 1027 ¶¶ 1, 7, 9. Mr. McPherson also testifies that “[t]he article and abstract from IEEE Xplore show the date of publication” by “populat[ing] this information using metadata associated with the publication.” *Id.* ¶ 10. Mr. McPherson further testifies that “[c]opies of the [SC ’97] conference proceedings were made available no later than the last day of conference.” *Id.* ¶ 11. Additionally, the footer of each page in Menon explicitly recites: “Proceedings of the ACM/IEEE SC97 Conference (SC’97),” which is consistent with Mr. MacPherson’s declaration testimony and further supports Petitioner’s contention that Menon was presented and distributed at the SC ’97 conference.

Second, the Internet Archive Affidavit supports Petitioner’s contention that Menon was publicly available on the Cornell website prior to June 13, 2006, the earliest possible priority date of the ’034 patent. Ex. 1029. The declaration states that the copy of Menon attached as Exhibit A is a “true and accurate cop[y] of browser screenshots . . . of the archived files for the URLs and the dates specified in the attached coversheet of each screen shot.” *Id.* ¶ 6. The dates shown on Exhibit A to the Internet Archive Affidavit indicate that Menon was available on the Cornell website by November 18, 2003, if not earlier. *Id.* Ex. A at 5–10. Patent Owner’s

argument, that the Petition has not shown the archived link chains “were navigable at any point in time prior to the critical date,” does not undermine the Petition’s contention of public accessibility to the extent each archived link in the chain is dated before June 13, 2006. Prelim. Resp. 17–18. In any event, Patent Owner’s link chain argument can be pursued during discovery.

Patent Owner also challenges the admissibility of the Petition’s evidence that Menon was cited in numerous technical publications, as unauthenticated hearsay. *Id.* at 31–33 (citing Pet. 14–16; Ex. 1003 ¶¶ 110, 112, 116–117, 129–130).¹³ The Petition asserts that 17 hyper-linked articles identified at pages 4–9 of Exhibit 1028 contain citations to Menon, thereby showing that Menon would have been reasonably located by a person of ordinary skill in the art prior to June 13, 2006. Pet. 14 (citing Ex. 1003 ¶¶ 110–112; Ex. 1028, 4–9); *see Blue Calypso*, 815 F.3d at 1350 (“a published article with an express citation to the potentially invalidating reference would similarly provide the necessary guidance”). Dr. Bajaj states that Menon was “cited 17 times in papers with online publication dates” prior to June 13, 2006. Ex. 1003 ¶ 110. For example, the first link on page 5 of Exhibit 1028 leads to an article dated March 15, 2006 that cites Menon in footnote 19. Ex. 1028, 5 (link to Karpievitch Y and Almeida J. (2006). “*mGrid: A load-balanced distributed computing environment for the remote execution of the user-defined Matlab code.*” BMC Bioinformatics. 10.1186/1471-2105-7-139. 7:1. Online publication date: 15-Mar-2006, available at <https://doi.org/10.1186/1471-2105-7-139>).

¹³ Patent Owner raises the same argument with respect to Trefethen and MPIref. Prelim. Resp. 31-33. The Board’s practice is to rule on motions to exclude evidence under the procedures set forth in 37 C.F.R. § 42.64.

On the present record at this stage of the proceeding, we determine the Petition adequately supports the contention that Menon was publicly available prior to June 13, 2006.

2. Trefethen (Ex. 1006)

The Petition contends that Trefethen “qualifies as a printed publication because it was published and distributed on the webpage of one of its authors at least as early as 2001” and “was published on a Cornell University website no later than May 10, 1996.” Pet. 14–15 (citing Ex. 1023; Ex. 1029). The Petition also contends that Trefethen was “reasonably located by POSITAs because it had been cited 10 times in papers prior to the priority date of the ’034 patent.” *Id.* at 15 (citing Ex. 1003 ¶¶ 116–117; Ex. 1035, 2–3). The Petition further contends that a “POSITA seeking to understand MultiMATLAB’s capabilities would have consulted the Cornell website dedicated to MultiMATLAB, which contained links to [Trefethen and Menon].” *Id.* at 23 (citing Ex. 1023).

Patent Owner responds that “there is no evidence that Exhibit 1006 was reachable as alleged from the webpage of the author prior to the critical date.” Prelim. Resp. 25. Patent Owner also argues that “there is no evidence that interested members of the public could have found the particular internet address of Exhibit 1006 or the internet address of the author’s webpage with reasonable diligence if they did not already know about them,” and Patent Owner challenges the testimony of Dr. Bajaj as “conclusory.” *Id.* at 25–26 (citing Ex. 1003 ¶ 116). Patent Owner next contends “there is no evidence that Exhibit 1006 was indexed or cataloged in a library or published in a journal prior to the critical date” and that Dr. Bajaj’s supporting testimony is “facially insufficient.” *Id.*

Our determination, that the evidence in the Petition is sufficient to support a reasonable likelihood that Menon was publicly accessible prior to June 13, 2006, applies equally to Trefethen. We add the following reasoning for emphasis.

While indexing and cataloging is an important consideration, the lack of indexing and cataloging is not dispositive. As the Federal Circuit explained in *Blue Calypso*, “we found that a particular article that was available only through an on-line publication was publicly accessible . . . [because] the particular on-line publication was well known to the community interested in the subject matter of the reference.” *Blue Calypso*, 815 F. 3d at 1349 (citing *Voter Verified, Inc. v. Premier Election Sols., Inc.*, 698 F.3d 1374, 1380 (Fed. Cir. 2012)). Here, Dr. Bajaj testifies that “Cornell was recognized at the relevant timeframe as a pioneer in ‘the development of high-performance “cluster” computers made by linking off-the-shelf computers in parallel,’” and an ordinarily skilled artisan “interested in computer cluster systems and cluster computing techniques and exercising reasonable diligence would have located Trefethen either from the Cornell website and/or the ACM Digital Library, as evidenced by the aforementioned 10 citations to Trefethen.” Ex. 1003 ¶ 117 (quoting Ex. 1033, 2; citing Ex. 1034, 1). Dr. Bajaj’s testimony is in line with the court’s reasoning in *Blue Calypso*.

After reviewing the evidentiary record at this stage of the proceeding, we find that Petitioner has demonstrated a reasonable likelihood that Trefethen qualifies as a printed publication.

3. *RS6000 (Ex. 1007), POEref (Ex. 1008), MPIref (Ex. 1017)*

The Petition contends that RS6000 “is a product manual by IBM in support of the IBM RS6000 SP computing solution.” Pet. 15. According to

the Petition, “RS6000 qualifies as a printed publication because it was cataloged and indexed in IBM’s online document library at least as early as 2002 on IBM’s website.” *Id.* (citing Ex. 1003 ¶¶ 1119–120; Ex. 1007; Ex. 1029; Ex. 1038). The Petition also contends that “Menon describes the MultiMATLAB architecture on an ‘IBM SP2’ and RS6000 provides details of that system.” Pet. 25 (citing Ex. 1005, Abstract, 6) n.2 (explaining that “‘IBM SP2’ is the same as ‘IBM RS/6000 SP.’” (citing Ex.1010, 6 (“the SP2 was renamed to simply the SP”))). The Petition further contends that a “POSITA seeking to understand MultiMATLAB would be motivated to review the documentation corresponding to the systems expressly discussed in Menon.” *Id.* at 26 (citing Ex. 1003 ¶¶ 86–87; Ex.1005, 6).

The Petition contends that POEref “is a product manual published by IBM in support for the Parallel Operating Environment running on an RS/6000 system.” Pet. 15. The Petition also contends that “POEref qualifies as a printed publication because it was catalogued and indexed in IBM’s online document library at least as early as 2001” and “was distributed with the IBM SP2 systems and published at least as early as 2001.” *Id.* (citing Ex. 1003 ¶¶ 123–125; Ex. 1008, 157; Ex. 1029; Ex. 1036, 14; Ex. 1039; Ex. 1047).

The Petition contends that “MPIref qualifies as a printed publication because it was distributed to POSITAs using FTP mail servers by the University of Tennessee and Oak Ridge National Library in 1994.” Pet. 15–16 (citing Ex. 1003 ¶ 129; Ex. 1017, cover page; Ex. 1029, 1–3). The Petition also contends that MPIref “was published on MPI Forum’s website no later than July 3, 1998” and “was reasonably located by POSITAs because it had been cited 74 times in papers with online publications dates before the earliest priority date of the ’034 patent.” *Id.* at 16 (citing Ex.

1003 ¶¶ 129–130; Ex. 1029, 1–3; Ex. 1037, 2–16). The Petition further contends that Menon “expressly cite[s] to ‘the MPI communication standard’” and “MPIref is the MPI communication standard referenced by Menon.” *Id.* at 89–90 (quoting Ex.1005, 5; citing Ex. 1003 ¶¶ 470–471; Ex.1017, 1 (“MPI: A Message-Passing Interface Standard”)).

With regard to the RS6000 and POEref, Patent Owner contends that “the Petition provides no evidence of library indexing or cataloging” and “also fails to demonstrate that Exhibits 1007 and 1008 were publicly accessible by practical searchability because it fails to offer any evidence that a query of any search engine before the critical date would have led to the particular URL addresses where the references were allegedly available.” Prelim. Resp. 16. Patent Owner also contends that the link chain on the IBM website reveals different pages for the links each with different archival dates such that Petitioner “provide[s] no proof that these pages and links existed at the same time or were even navigable.” *Id.* at 6. With respect to Dr. Bajaj’s testimony that POEref was distributed with the associated software according to a license agreement, Patent Owner argues the testimony relies on hearsay that the Board “cannot rely on.” *See id.* at 19 (citing Ex. 1003 ¶ 124).

Our analysis and determination, that the evidence in the Petition is sufficient to support a reasonable likelihood that Menon and Trefethen were publicly accessibility prior to June 13, 2006, applies equally to RS6000, POEref, and MPIref. We add the following reasoning for emphasis.

The Petition presents sufficient evidence to establish a reasonable likelihood that artisans of ordinary skill were aware of IBM SP2 and POE products at least through publication of Menon and via distribution of POEref with the product. *See* Pet. 14–15. The Petition also adequately

supports the contention that RS6000 and POEref were “sufficiently accessible to the public interested in the art” via the links to which Petitioner cites, in order to implement known MultiMATLAB products in the known POE system for which the known IBM SP2 was designed. *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d at 1348; *see* Ex. 1005, 5; Ex. 1008, 157. Further as to POEref, the Petition shows “Menon describes using POE to initialize the MATLAB processes,” and “MultiMATLAB uses ‘POE, IBM's Parallel Operating Environment,’” so that an artisan of ordinary skill “seeking to understand MultiMATLAB would be motivated to review the documentation corresponding to the systems expressly discussed in Menon.” Pet. 26 (quoting Ex. 1005, 6; citing Ex. 1003 ¶¶ 86–87).

Patent Owner’s further argument, that statements in POEref and MPIref cited in the Petition are hearsay (Prelim. Resp. 19, 21, 31), can be pursued during discovery and pursuant to our objection and motion to exclude process. 37 C.F.R. § 42.64. We note that the Board is the fact finder in this proceeding, not a jury, and the Hearsay Rules include various exceptions that may apply to hearsay statements in RS6000, POEref, and MPIref. Regardless, as Petitioner shows, “Menon describes that a POSITA would look to use the MPI standard because of MPI’s ‘broad popularity, its suitability to high performance parallel computing, and the virtually universal availability of vendor-optimized versions on modern parallel computers.’” Pet. 90 (quoting Ex. 1005, 5 (“IBM’s proprietary version of MPI [is] specifically optimized for the SP2”)) (citing Ex. 1003 ¶ 470). This evidence further supports the Petition’s contention that an artisan of ordinary skill would have been motivated and able to locate MPIref as documentation of IBM’s optimized MPI for use in the SP2 system.

After reviewing the evidentiary record at this stage of the proceeding, we determine the Petition has demonstrated a reasonable likelihood that RS6000, MPIref, and POEref qualify as printed publications under 35 U.S.C. § 102.

III. CONCLUSION

For the foregoing reasons, we determine Petitioner has established a reasonable likelihood of prevailing in its challenge to the patentability of at least one claim in the '034 patent. Therefore, we institute *inter partes* review of all challenged claims on all grounds. *See SAS*, 584 U.S. at 365.

At this stage of the proceeding, the Board has not made a final determination as to the patentability of any challenged claims or any underlying factual or legal issues. A final determination will be made based on the record as developed during the *inter partes* review. Any final determination will be based on the record developed during trial. Any argument not asserted in a timely-filed brief, such as a response to the Petition, may be deemed forfeited or waived, even if that argument appears in the Preliminary Response.

ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–30 of the '034 patent is instituted with respect to all grounds set forth in the Petition;

FURTHER ORDERED that the parties shall propose and support a specific plain meaning or other construction for limitations [1.4.1] and [1.5.1] in their briefs. The parties are ordered to analyze the relevant claim language and cite to the specification and prosecution history in support of

their claim construction where applicable, with particular attention to the description of processors and processor cores in the '034 patent;

FURTHER ORDERED that the parties shall construe the meaning of Limitation [30.1.2] in independent claim 30; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '034 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

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