

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

ADVANCED CLUSTER SYSTEMS, INC.,
Patent Owner.

Case IPR2025-00913
U.S. Patent No. 11,570,034

PATENT OWNER'S SUR-REPLY

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I. THE BOARD SHOULD REJECT PETITIONER'S PROPOSED CLAIM CONSTRUCTION

The “hardware processor with a plurality of processing cores” limitation is recited in independent claims 1, 25, 28, and 30. Ex. 1001, 29:47, 32:24, 33:47, 34:33. Petitioner proposes the limitation reads on “one or more single-core or multi-core microprocessors with a plurality of processing cores.” Reply 1–2. That construction is incorrect because it conflates the recited “processor” with separate “microprocessors,” removes the structural requirement that the cores be within the recited processor, and cannot be reconciled with the specification passages Intel itself cites.

A. Petitioner's Construction Reads the Plural-Cores Requirement Out of the Claim

Petitioner claims to seek the plain and ordinary meaning, but in reality, reads limitations into the claims by relying on exemplary specification language to allege “a clear definition.” Reply 1; *id.* Section II.A. header. Nowhere did the patentee act as its own lexicographer to define “hardware processor with a plurality of processing cores” as meaning “one or more single-core or multi-core microprocessors with a plurality of processing cores,” nor did it make any clear and unmistakable disavowal. *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365-67 (Fed. Cir. 2012).

The claim language is “a hardware processor with a plurality of processing cores.” Ex. 1001, claim 1. The grammar is precise: a singular processor; a plurality of cores; the cores are within — contained in or part of — the recited processor. Petitioner’s construction inverts both requirements. By substituting “one or more . . . microprocessors,” Petitioner allows multiple separate microprocessors to count as the recited “hardware processor,” and by treating each separate microprocessor as supplying a “core,” Petitioner treats separate processors as the claimed cores. The claim language permits neither substitution.

The drafter knew how to claim a multi-processor system. The specification distinguishes between systems with multiple separate processors and individual processors with multiple cores. Ex. 1001, 5:11–37, 7:14–36, 9:50–10:3. The claim recites only the latter.

B. The Specification Distinguishes a Processor Containing Cores from a Configuration of Independent Microprocessors

The three specification passages Petitioner cites describe exemplary architectural configurations.

Column 5 states: “[E]ach processor **can** contain one or more processor cores that are capable of single-threaded execution. Processor cores are generally independent microprocessors, but more than one can be included in a single chip package.” Ex. 1001, 5:11–16. (Emphasis added). The passage describes a processor that contains processor cores. The phrase “more than one can be included in a single

chip package,” that Petitioner ignores, affirmatively describes the multi-core configuration; nothing in the text supports Petitioner’s reading that cores need not be in the same package. Reply 9

Column 7 states: “Processors 112a-b **can be** one or more general purpose single-core or multi-core microprocessors such as, for example, a Pentium® processor . . . a Core 2 Duo® processor . . . a Xeon® processor . . . an Athlon® processor. . . a MIPS® processor” Ex. 1001, 7:14–25. (Emphasis added). The enumerated examples are individual single-core or multi-core microprocessor models. None is a Symmetric MultiProcessor system or a multi-processor configuration, nor a definition of a “hardware processor with a plurality of processing cores.”

Column 9 repeats the same architecture. Ex. 1001, 9:50–10:3. That is likewise described in the singular: “the processor 132.”

Read together, these passages describe two distinct exemplary configurations: (i) a single processor containing multiple processing cores, and (ii) a system containing multiple processors, each a single-core or multi-core microprocessor. The claim language requires the first configuration, not the second. The specification’s reference to alternative system arrangements describes the broader landscape; it does not transform the recitation of a singular-processor with a plurality of processing cores into a multi-processor-system recitation nor does it constitute the patentee

“act[ing] as his own lexicographer,” or a clear and unmistakable disavowal .
Thorner, 669 F.3d at 1365-67.

Petitioner’s expert’s Supplemental Declaration is of no help. Paragraphs 9-23 of the Supplemental Declaration, Ex. 1163, are nearly verbatim repetitions of the conclusory petition assertions for which it is offered to support and are devoid of any technical reasoning. *Xerox Corp v. Bytemark, Inc.* IPR2022-00624, Paper 9, 15 (Aug. 24, 2022) (precedential) (according “little weight” to declaration testimony that contains a verbatim restatement of a petition’s conclusory assertions); 37 C.F.R. § 42.65(a).

C. PO’s Construction Does Not Exclude Specification Embodiments

Petitioner argues that Patent Owner’s (“PO”) construction excludes embodiments described in the specification because the specification permits a processor to be “one or more . . . single-core or multi-core microprocessors.” Reply 8–9 (citing *Verizon Servs. Corp. v. Vonage Holdings Corp.*, 503 F.3d 1295, 1305 (Fed. Cir. 2007)). The argument misreads PO’s construction, the specification, and the case law.

PO’s proposed interpretation properly excludes a single-core microprocessor and a configuration in which separate single-core microprocessors are aggregated and counted as the recited processor. Reply 8. Those configurations are excluded by the claim language itself. A single-core microprocessor has only one core.

Additionally, aggregating multiple single-core microprocessors does not produce a single processor with plural cores; it produces a system with multiple processors, each having one core.

Verizon held only that constructions excluding a preferred embodiment are disfavored, not categorically prohibited. 503 F.3d at 1305. The Federal Circuit has repeatedly declined to extend that presumption into the rule Petitioner advocates: that a construction must encompass **every** configuration described in the specification, regardless of claim language. *Baran v. Med. Device Techs., Inc.*, 616 F.3d 1309, 1316 (Fed. Cir. 2010) (“It is not necessary that each claim read on every embodiment”). PO’s construction follows *Phillips*; claim language is read in light of, but not rewritten to match, every passage of the specification. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1315–17 (Fed. Cir. 2005) (en banc).

D. Petitioner’s New “MIPS Coprocessor” Theory (Ex. 1168) Is Reply-Stage and Wrong on the Merits

Petitioner’s Reply argues, for the first time, that the specification’s reference to a MIPS processor supports treating multiple separate microprocessors as “processing cores,” because MIPS architecture defines “coprocessors.” Reply 9 (citing new Ex. 1168). The argument should be refused under § 42.23(b) and is incorrect on the merits.

The MIPS32 manual (Ex. 1168) — was not cited in the Petition. The Petition’s claim-construction analysis, Pet. 10–13, makes no reference to MIPS coprocessors.

A petitioner may not introduce a new claim-construction theory and supporting evidence in Reply when those materials were available at filing. 37 C.F.R. § 42.23(b); Office Patent Trial Practice Guide, 84 Fed. Reg. 64,280 (Nov. 21, 2019); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016).

MIPS “coprocessors” are not “processing cores.” MIPS coprocessors are functional units — for example, system control coprocessors and floating-point coprocessors — that supplement the processor’s main execution path. Ex. 1168, 43. The specification’s reference to MIPS lists it alongside Core 2 Duo and Athlon as examples of “single-core or multi-core microprocessors” — the specification does not describe MIPS as a multi-microprocessor system. Ex. 1001, 7:24.

II. RS6000 DOES NOT DISCLOSE A “HARDWARE PROCESSOR WITH A PLURALITY OF PROCESSING CORES”

A. The Petition Mapped RS6000’s SMP at the System Level, Not Cores Within a Single Processor

The Petition’s theory rested on RS6000’s “Symmetric MultiProcessor (SMP)” hardware. Pet. 42–43 (citing Ex. 1007, 2, 9). RS6000 describes an SMP node that includes “four, eight, twelve, or sixteen 375 MHz 630FP 64-bit processors” arranged in modular four-processor cards and processor slots. Ex. 1007, 9–10.

Smith explained that a POSITA reading RS6000 would understand the SMP as a multi-processor system, not as a single processor with internal cores. Ex. 2017

¶¶27–35. The SMP processors share memory and bus resources at the system level, but execute instructions independently and are packaged as separate devices. Treating those separate devices as “cores within a single processor” ignores the Patent’s distinction between a multi-processor system and a processor containing cores.

B. Petitioner’s POWER3-Execution-Units Mapping Relies on a New Embodiment of RS6000 that was First Identified in Reply and Should Be Refused under § 42.23(b)

Petitioner’s Reply now offers a new and different identification: a **single** POWER3 chip with eight execution units, each treated as a “core.” Reply 12; Ex. 1163 ¶¶33–41.

Axonics, Inc. v. Medtronic, Inc. permits a petitioner to argue and present evidence under a patent owner’s new claim construction, but only when the petitioner “relies on the same embodiments for each invalidity ground as were identified in the petition.” 75 F.4th 1374, 1384 (Fed. Cir. 2023). The post-*Axonics* decision in *Rembrandt* confirms that permissible Reply elaboration must rest on “the same legal ground” based on “the same prior art reference[s]” and the same embodiment. *Rembrandt Diagnostics, LP v. Alere, Inc.*, 76 F.4th 1376, 1383–85 (Fed. Cir. 2023).

Petitioner’s Reply does not satisfy that test and PO objects to Petitioner’s new unpatentability theory. The Petition asserted that RS6000 disclosed “a ‘Symmetric

MultiProcessor (SMP)’ (‘hardware processor’) and that each SMP includes ‘four, eight, twelve, or sixteen 375 MHz 630FP 64-bit processors’ (plurality of processing cores).” Pet. 42-43. The POR refuted this theory. POR 17-21. Rather than defend it, Petitioner now relies upon Bajaj’s Supplemental Declaration to advance a different RS6000 embodiment — POWER3 execution units inside one chip — to satisfy the same limitation. Ex. 1163 ¶¶33-41. This structural substitution falls squarely inside the rule of *Intelligent Bio-Sys* that a Reply may not introduce a new prior-art structure to satisfy a disputed claim element.

1. The Petition Did Not Map POWER3 Execution Units as Cores

The Petition’s discussion of RS6000 was at the SMP level. Pet. 42–43 (citing Ex. 1007 2, 9). The Petition did not cite Ex. 1010 for execution-unit detail. The Petition did **not** describe POWER3 internals, nor did it identify execution units as the structure satisfying the cores limitation. Rather it is newly identified in the Reply. Reply 12; Ex. 1163 ¶¶33–41.

2. The Reply Identification Is a Different Structure, Not an Elaboration of the Same Theory

Apple v. Andrea permits a petitioner to elaborate in Reply on the same prior-art structure identified in the Petition. 949 F.3d 697, 706–07 (Fed. Cir. 2020). *Anacor Pharms., Inc. v. Iancu* permits responsive evidence directed to the same combination. 889 F.3d 1372, 1380–81 (Fed. Cir. 2018). Neither permits substituting

a new embodiment — to satisfy a disputed claim element. This is exactly what the Reply does; identify a different structure — POWER3 execution units within one chip — to satisfy the cores limitation. Rule 42.23(b)’s requirement that a Reply “must comply with the content requirements for a petition” bars supplying new prior-art structures or theories not identified in the Petition. *See* Office Patent Trial Practice Guide, 84 Fed. Reg. 64,280, 64,299 (Nov. 21, 2019).

The relief PO requests is targeted: refuse to consider Ex. 1163 ¶¶38–41 to the extent Petitioner relies on those paragraphs to identify POWER3 execution units as the claimed cores. *Rembrandt*, 76 F.4th at 1383–85 (recognizing the Board’s refusal to consider a new theory first raised in Reply).

C. POWER3 Execution Units Are Not “Processing Cores”

Even considering the execution-units’ identification, it fails on the merits. The specification describes “processing cores” as “processing units capable of single-threaded execution.” Ex. 1001, 7:27–29. An execution unit in a superscalar core is a pipeline functional unit — for example, the POWER3 *See* “superscalar core [is] comprised of eight execution units” that “allows concurrent operation of fixed-point, load/store, branch, and floating-point instructions.” Ex. 1010, 57. Multiple execution units within a single superscalar core allow concurrent operation of instructions issued from one instruction stream; they do not independently execute separate instruction streams. They are not “processing units capable of single-threaded

execution.” This is confirmed by Bajaj, who quotes the specification’s “units capable of single-threaded execution” and Ex. 1010’s “eight execution units” and concludes — without independent technical reasoning — that “execution units” satisfy the specification’s description of “processing cores.” Ex. 1163, ¶40. That kind of conclusory expert testimony is entitled to little weight. *Xerox*, IPR2022-00624, Paper 9, 15 (Aug. 24, 2022) (precedential); *see* 37 C.F.R. § 42.65(a).

Treating each execution unit as a “core” would convert every superscalar single-core processor into a multi-core processor. That is not the claim language. Dr. Smith addressed the RS6000 reference at the system level and explained that a POSITA would read it as a multi-processor configuration, not a processor with internal cores. Ex. 2017 ¶¶27–35.

The specification draws the distinction Petitioner ignores: processors at the system level (Ex. 1001 col. 5:11–37, 7:14–36, 9:50–10:3) versus cores within a single processor (*id.* col. 5:14–16). Petitioner’s Reply treats those distinct levels as interchangeable. The specification teaches they are not.

Under *Phillips*, claim language identifying a processor with internal cores cannot be stretched to encompass either separate processors at the system level or pipeline subcomponents within a single processor. 415 F.3d at 1315–17. Petitioner’s two RS6000 theories operate at structurally distinct levels from the level the claim recites. The first theory points outside the claimed processor — to separate

processors at the system level. The second theory points inside one processor — to functional units that share the processor's instruction stream and execution control. Neither identifies “a hardware processor with a plurality of processing cores,” meaning the cores must be within the claimed processor. Ex. 1001, claim 1.

III. MENON/TREFETHEN DOES NOT DISCLOSE THE CLAIMED 1→2→3→1 ORDER OF OPERATIONS

The Petition relied on Menon and Trefethen to teach an order in which the first node calls the second node, the second node performs a mathematical evaluation and communicates the result to the third node, and the third node performs a mathematical evaluation and communicates the result back to the first node. Pet. 44–49. The Reply argues that Trefethen's example script (Ex. 1006, 6) describes the same sequence. Reply 14–23. The argument fails for the reasons addressed below.

A. Petitioner's Own “Peer-to-Peer Architecture” Construction Forecloses Reliance on Trefethen's Cycle.m Example

Claims 1 and 30 of the '034 Patent require the communication network between the nodes to be a “peer-to-peer architecture.” Pet. 34; Ex. 1003, ¶50; Ex. 1001 Claim 30 Petitioner adopted, as its claim construction for “peer-to-peer architecture,” the requirement that the architecture be one “in which each node can communicate tasks and data with other nodes without the tasks and data being required to go through a central server or master node.” Pet. 12; Ex. 1003, ¶¶ 63–

65.¹ Petitioner expressly informed the Board that “Petitioners and its expert used this construction.” Pet. 12. Petitioner cannot retreat from that construction in Reply. *VidStream LLC v. Twitter, Inc.*, 981 F.3d 1060, 1067 (Fed. Cir. 2020); *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1331 (Fed. Cir. 2019) (“[a]n IPR petitioner may not raise in reply an entirely new rationale for its challenge”).

Under its construction, Petitioner's Trefethen mapping fails. Trefethen describes the MultiMATLAB system as a master/slave architecture in which a single “master process” launches and controls “slave processes,” each MATLAB process “transmits its output to the master process as soon as it is ready,” and the master collects and serializes that output to the user terminal. Ex. 1006, 3–4; Pet. 47; Ex. 1003, ¶ 221; Reply 15. That is the opposite of the peer-to-peer architecture claim construction which the Petition committed to apply.

The Reply confirms that in implementing Trefethen's EVAL (cycle.m) the “output [of each node] is sent to the master process as soon as it is ready,” Reply 15 citing Ex. 1006, 4. But routing every node's output through a central master is the architectural feature Petitioner's own construction excludes.

¹ The district court in the underlying parallel proceeding construed the term in a similar manner. Ex. 1085 14.

**B. Petitioner's Litigation Cross-References Cannot Substitute for
Petition-Stage Identifications**

Petitioner cites PO's preliminary infringement contentions in the parallel district court litigation (Ex. 1022) and invokes *Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995), to argue that PO conceded user-authored application code is within claim scope. Reply 19–20. Neither argument supports Petitioner's prior-art identification.

Ex. 1022 describes Intel's accused Habana AI accelerator products (Gaudi HLS-1, HLS-Gaudi2, Gaudi 3) and Xeon Scalable Processors, and uses Intel's HCCL Demo source code to provide notice how the hardware of those accused products implement the claim limitations. The contentions explain how the accused products, as Intel manufactures and markets them, satisfy the claim limitations. They do not describe what Trefethen discloses. The accused products implement modern hardware and a kernel dispatch architecture; that does not transform Trefethen's 1996 hardcoded 1996 MATLAB script into the kernel-dispatch architecture the claims recite. Litigation contentions describing an accused product's architecture do not shift claim scope; they apply the construction the court adopted to particular accused features. *Phillips* controls claim construction here, not the contents of an infringement contention. 415 F.3d at 1315–17. Additionally, *Southwall* is immaterial as Petitioner has not identified any prosecution history arguments that PO conceded the scope of its claims.

IV. PETITIONER DID NOT ESTABLISH MOTIVATION TO COMBINE MENON AND TREFETHEN

Even if the processing cores element and the $1 \rightarrow 2 \rightarrow 3 \rightarrow 1$ element were taught individually, Petitioner did not establish that a person of ordinary skill in the art would combine the references in the way the claims require.

A. Menon's Redesign Rationale Identifies the Trefethen Architecture as Architecturally Limited

Menon describes the Trefethen MultiMATLAB architecture and identifies limitations: tight coupling to MPICH, lack of extensibility, and performance constraints. Ex. 1005, 2–3; *see also* POR 42-43. Menon then describes a redesigned architecture using vendor-specific MPI implementations and parallel MEX routines, with the explicit purpose of overcoming those fundamental limitations. Ex. 1005, 2–3; *see also* POR 43-44. A person of ordinary skill in the art reading Menon would adopt the redesigned architecture — not return to the Trefethen architecture Menon redesigned away from. The Reply's framing that "Menon builds on Trefethen" (Reply 25) describes the conceptual lineage but does not address Menon's specific architectural changes. Moreover, Petitioner's expert's reiteration of Petitioner's statement regarding a motion to combine Menon and Trefethen, verbatim, without addressing these fundamental deficiencies does not establish that a POSITA would be motivated to make the combination. *Compare* Ex. 1163 ¶70 *with* Reply 24-25; *Xerox*, IPR2022-00624, Paper 9, 15 (Aug. 24, 2022) (precedential).

**B. Petitioner's Common-Authorship and "MEX Routines"
Arguments Do Not Cure the Motivation Failure**

Petitioner's Reply argues that Menon and Trefethen share two authors, both papers describe "aspects of the same system," and "Menon explicitly cites Trefethen and explains that Menon builds on the teachings of Trefethen." Reply 25–26 (citing Ex. 1005, 1–2; Ex. 1003, ¶71; Petition, 22). None of those facts supplies the motivation the claims require.

Common authorship is not a substitute for motivation evidence. Two authors writing two papers about the same general system does not establish that a POSITA reading either paper would be motivated to combine the references in the specific way Petitioner now proposes — a chained result-passing architecture across separate processing cores within a single chip.

Petitioner's invocation of "MEX routines" proves the opposite of what Petitioner claims. Reply 26. Menon's MEX-routines extension was Menon's response to limitations Menon expressly identified in Trefethen's architecture: "tight coupling" to MPICH and lack of "extensibility." Ex. 1005, 2–3. MEX routines are not the architectural change Petitioner needs to bridge the obviousness gap. Petitioner needs to show that a POSITA would substitute a different processor organization (a single multi-core chip, or POWER3 execution units inside one chip) for Trefethen's discrete-processor architecture, while preserving Menon's reported

parallel-efficiency results. Adding software routines for extensibility is not the same as changing the underlying processor organization.

Petitioner also relies on Bajaj's Supplemental Declaration ¶¶73–74. Reply 26. Those paragraphs are themselves Reply-stage additions not present in Bajaj's original declaration. Like Bajaj's other supplemental paragraphs (¶¶33–41 on POWER3 execution units), ¶¶73–74 are subject to the same § 42.23(b) objection: a Petitioner cannot use a supplemental declaration to supply motivation evidence the Petition was required to identify with particularity. 35 U.S.C. § 312(a)(3); 37 C.F.R. § 42.104(b)(4).

Menon does not supply motivation to preserve Trefethen's earlier architecture; it supplies the reason to move past it. Menon expressly presents a “new MultiMATLAB architecture redesigned” for performance and extensibility, then identifies the “first MultiMATLAB architecture” as more tightly coupled to MPICH/P4, unable to use vendor-specific MPI implementations, unable to support extensions via parallel MEX routines, and subject to performance limitations. Ex.1005, 2, 14. That is a concrete redesign to avoid identified architectural limitations, not a mere preference among equivalent options. Under *DePuy Spine*, a reference that discourages the proposed path or undercuts the rationale for pursuing it defeats motivation and reasonable expectation of success. *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009). Menon

therefore teaches away from reconstructing the Trefethen architecture that Menon redesigned to avoid.

C. Architectural Differences Defeat Reasonable Expectation of Success

Multi-core and shared-resource processor arrangements raise cache-coherency, shared-cache, and false-sharing issues at the architectural level that are not present in the discrete-processor architecture of RS6000 and the MultiMATLAB systems described in Menon and Trefethen. Those issues affect the same performance dimension Petitioner invokes from Menon (parallel efficiency).

Petitioner's Reply rests its motivation theory on the same POWER3-execution-units architecture that itself is impermissible under § 42.23(b). With that underlying structural identification removed, the Reply's motivation argument falls with it: there is no cognizable basis on the Petition record for substituting a different processor organization while expecting Menon's performance results to translate.

KSR permits combining elements according to known methods to yield predictable results. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418–21 (2007). It does not authorize the Board to fill an evidentiary gap with hindsight, especially where the references teach away from such combination. *DePuy Spine*, 567 F.3d at 1327. Menon's redesign rationale and reported performance results do not support Petitioner's proposed architectural reconstruction.

Petitioner's mid-stream pivot from Menon's reported 32-node SP2 architecture to a single POWER3 chip is the textbook hindsight reconstruction *KSR* forbids. The Petition relied on Menon's specific architectural arrangement — 32 IBM SP2 processor nodes — to support the motivation and expectation-of-success showing for combining Menon and Trefethen. Pet. 22; Ex. 1003, ¶71; Ex. 1005, 1–2. Petitioner cannot retroactively substitute a fundamentally different architectural arrangement (a single POWER3 chip with eight execution units) and rely on Menon's performance results to bridge the obviousness gap. The architectural substitution itself raises motivation and reasonable-expectation-of-success questions Petitioner has not addressed, and *KSR* does not permit a tribunal to bridge that gap with hindsight. *KSR*, 550 U.S. at 421; *DePuy Spine*, 567 F.3d at 1327.

V. PETITIONER DID NOT ESTABLISH THAT THE FIVE REFERENCES ARE PRINTED PUBLICATIONS

The issue is not whether Menon, Trefethen, RS6000, POEref, and MPIref could in some abstract sense qualify as prior art. The issue is whether the Petition — not theories added in Reply — meets the preponderance-of-the-evidence standard on public accessibility. It does not. The Petition's printed-publication showing relied on facial indicia of the references (cover pages, conference designations, IBM library listings) and a small set of Petition-stage exhibits. Pet. 14-16. The Reply now relies on Ex. 1086 (Hsieh-Yee declaration) and dozens of supporting exhibits to establish public accessibility through library cataloging

records, MARC records, WorldCat records, Academia Sinica records, and Internet Archive captures. Reply 27-34. Petitioner has not disputed the insufficiency of the Petition's original showing; instead, Petitioner has added new theories. That confirms the Board must evaluate whether the Reply's new evidence merely corroborates the Petition-stage theories or supplies missing public-access channels. Ex. 1086 may corroborate public-access theories the Petition identified; it should not supply new theories as substitutes for theories the Petition omitted. And on the link-chain theory Petitioner does carry forward from the Petition, the record contains no evidence — only assumption — that the hyperlink chain Petitioner asks the Board to walk actually existed in the form Petitioner needs.

A. *Hulu* Requires Petition-Stage Identification of Public-Access Evidence with Particularity

Printed-publication status is not presumed. The petitioner must identify, with particularity, evidence sufficient to establish a reasonable likelihood that an asserted reference was publicly accessible before the critical date. *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29, at 13-16 (Dec. 20, 2019) (precedential). Reply evidence may corroborate that showing; it may not establish a public-access channel the Petition never identified. *VidStream LLC v. Twitter, Inc.*, 981 F.3d 1060, 1064-67 (Fed. Cir. 2020). The statutory and regulatory framework reinforces the same line. 35 U.S.C. § 312(a)(3); 37 C.F.R. § 42.104(b)(2), (b)(5). Public accessibility is the touchstone. *In re Hall*, 781 F.2d

897, 898-99 (Fed. Cir. 1986); *In re Lister*, 583 F.3d 1307, 1311-17 (Fed. Cir. 2009); *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1348-50 (Fed. Cir. 2016).

B. The Petition Relied on Facial Indicia; Ex. 1086 Improperly Adds New Channels

For each of the five references, the Petition relied on the references' facial indicia and a small set of ACM/Internet-Archive exhibits. Pet. 14-16. Ex. 1086 introduces library cataloging records and expands the public-accessibility theory beyond what the Petition presented.

The reference-by-reference picture is consistent. For Menon, the Petition cited Ex. 1005 (the reference itself), Exs. 1026 and 1027 (SC97 proceedings), Ex. 1028 (citation count), and Exs. 1023 and 1029 (Cornell webpages and Internet Archive affidavit). Pet. 14. Hsieh-Yee's declaration adds WorldCat records (Ex. 1090) and Academia Sinica MARC records (Ex. 1091) — library cataloging records the Petition did not cite. Ex. 1086, ¶¶28-70. Internet Archive captures of Menon (Ex. 1092) corroborate the same kind of evidence the Petition already relied on (Ex. 1029); the WorldCat and Sinica records, by contrast, supply a new evidentiary channel. For Trefethen, the Petition cited Ex. 1023 (Cornell), Ex. 1029 (Internet Archive affidavit), and Ex. 1035 (ACM citations). Pet. 14-15. Hsieh-Yee adds Washington State University MARC records (Ex. 1101) — again, library cataloging records the Petition did not cite. Ex. 1086, ¶¶71-104. The same pattern

repeats for RS6000, POEref, and MPIref. Reply 27-34; Ex. 1086, ¶¶105-180. The targeted objection is to the new library-cataloging-records theory that the Petition never identified, not to corroboration of the Internet Archive evidence the Petition already presented.

The relevant question is reference-specific: for each reference, does Ex. 1086 corroborate a public-access channel the Petition identified, or does it supply a new channel? The Petition identified facial indicia and ACM citations. Ex. 1086 supplies library cataloging records and Internet Archive captures as the public-access basis. That is a new evidentiary theory, not corroboration.

C. *VidStream* Permits Reply Corroboration of the Same Theory; It Does Not Permit Substitution

VidStream addressed reply evidence that corroborated the publication date of the same asserted reference after the patent owner challenged the publication date. 981 F.3d at 1064-67. The Federal Circuit approved that use because the petition had identified the publication and the reply evidence supported the same publication theory. *VidStream* did not authorize a petitioner to use a reply declaration as the first identification of a distinct public-access channel.

The objection here is targeted. Patent Owner does not ask the Board to exclude Ex. 1086 wholesale. Ex. 1086 may corroborate Petition-stage identifications. It should not become the first source of theories that the Petition was required to identify with particularity. As applied to each reference, the Board

should rely on Ex. 1086 only for corroboration of public-access channels the Petition presented.

D. Petitioner's "Link Chain" Theory Rests on an Assumption That No Wayback Capture Establishes

Petitioner's preponderance burden on public accessibility cannot be carried by assumption of a missing predicate fact. *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (the Board "must base its decision on arguments . . . advanced by a party," and may not "fill in" the petition's gaps); *Hulu*, IPR2018-01039, Paper 29 at 13 (petitioner must "identify with particularity" evidence of public accessibility, with no presumption in its favor); *In re Lister*, 583 F.3d at 1316-17 (mere existence of a record is not evidence that a POSITA could reach the underlying reference).

Petitioner's printed-publication theory for Menon, Trefethen, RS6000, POEref, and MPIref rests on a chain of hyperlinks. Petitioner asks the Board to find that a POSITA, exercising reasonable diligence, could have started at a root webpage and clicked through one or more intermediate pages to arrive at the prior-art reference. *See* Pet. 14-16; Ex. 1086 ¶¶46-53 (Menon), ¶¶76-77 (Trefethen), ¶¶112-118 (RS6000), ¶¶128-136 (POEref), ¶¶153-180 (MPIref). Each step in the chain is authenticated only by a separate Wayback Machine capture — and each capture bears its own archival date.

A hyperlink does not traverse time. A Wayback Machine capture proves only what content existed at one URL on one date. That a 2003 capture of a Cornell index page (Ex. 1023, capture 20031118185911) contains a string formatted as a link to Trefethen says nothing about what content sat at the linked URL in 2001 or in 1996 — the dates on which Petitioner asserts public accessibility. The same gap pervades the RS6000 chain: the entry-point Product Documentation Library was archived April 10, 2001 (capture 20010410025356); the Volume 1 landing page was not archived until June 17, 2001 (20010617011337); the section pages Petitioner actually offers as RS6000 (Ex. 1007) were not archived until July 26, 2001 (20010726184202; 20010726183314) and August 2001 (Ex. 1038, 1-5); and the parallel pSeries entry path runs from October 24, 2001 (20011024235023) to December 4, 2001 (20011204190353). The chain spans ten months. For POEref the chain is worse: Petitioner's own expert concedes "Internet Archive . . . has not archived POE-2001." Ex. 1086 ¶128. The chain never reaches the document at any date.

The Board cannot supply the missing link. To prove a POSITA could have actually navigated the chain on the asserted critical date, Petitioner needed to tie the separately dated captures together into a navigable public-access path at the relevant date — either through contemporaneous evidence or testimony establishing that each intermediate page existed and contained the same link in the

relevant state. Petitioner has neither. Asking the Board to assume that all linked pages existed identically on a single date is precisely the gap-filling *Magnum Oil* forbids. 829 F.3d at 1380. The preponderance burden on each reference's public accessibility is therefore unmet.

Additionally, with respect to RS6000, the Hsieh-Yee links the Reply relies on for accessibility of RS6000 differ from the evidence presented in the Petition. And Bajaj's declarations do not state that he actually traversed any of these pages in a reasonably diligent manner to locate the alleged RS6000 reference. Hsieh-Yee's declaration does not corroborate the pages relied upon in the Petition by Bajaj, but rather cites different pages accessed after the fact in 2026. Ex. 1086 ¶¶112-119. Neither Bajaj nor Hsieh-Yee provides evidence that RS6000 was viewed or downloaded from the IBM website prior to the critical date. *Blue Calypso*, 815 F.3d at 1349. It is Petitioner's burden to clearly and consistently present its evidence in the Petition that a POSITA could have located the documents exercising reasonable diligence. The record lacks sufficient evidence from Bajaj that this was the case, and Hsieh-Yee's declaration cannot fill that gap: Hsieh-Yee may authenticate cataloging and archival records, but her expertise does not extend to the technical-diligence inference about how a cluster-computing POSITA would have located IBM/Cornell materials through the asserted path at

the relevant time. Compare Pet. 12 with Ex. 1086 ¶¶7. The Board should not condone Petitioner's hindsight do-over analysis.

Finally, the Hsieh-Yee usage-record case for RS6000, Ex. 1086 ¶¶120-123, is also unavailing. The URL contained in the bibliography of Ex. 1112 (<http://publibfp.boulder.ibm.com/epubs/pdf/da70bmst.pdf>) is a "dead link." The contents of that link, at a URL entirely different from what Bajaj identified, are unknown, and it is speculative to assume the link's contents are the same as RS6000 solely based on the title, especially given the ease with which web pages could be edited in the relevant time period.

E. *Suffolk Techs* Required Contemporaneous Access Evidence; Petitioner Has None

Petitioner's reliance on *Suffolk Techs. v. AOL, Inc.*, 752 F.3d 1358, 1365 (Fed. Cir. 2014), for the proposition that subsequent citation establishes accessibility (Reply 28-33), misreads the case. *Suffolk Techs* addressed a Usenet post where access was established by replies posted to the same Usenet group during the critical period; the court relied on contemporaneous evidence that interested researchers actually accessed the post in the forum where it was published. *Id.* at 1361, 1365. Here, Petitioner offers no contemporaneous evidence that any skilled person actually accessed Menon, Trefethen, RS6000, POEref, or MPIref through the cataloging records or citation chains the Reply now invokes. Citations in later publications by other authors prove only that those authors had

heard of the references, not that the references were publicly accessible to a POSITA on the priority date. Mere proof of subsequent awareness is the very “mere existence” theory *In re Lister* rejected. 583 F.3d at 1316-17.

The Reply’s citation-counts theory — that Menon, Trefethen, RS6000, and MPIref are publicly accessible because they were later cited by other publications (Reply 28-33, citing Exs. 1028, 1035, and the Hsieh-Yee declaration) — fails on the same logic. Citation counts establish that some authors knew of the references after the priority date; they do not establish that the references were publicly accessible to a POSITA on the priority date. The Reply identifies no contemporaneous evidence — testimony, library records dated before the priority date, or cataloging entries timestamped before the critical date — connecting the later-cited references to a publicly navigable channel on the priority date. *Blue Calypso*, 815 F.3d at 1350 (public accessibility “must be assessed on a case-by-case basis”); *In re Lister*, 583 F.3d at 1314 (“mere existence” is insufficient).

VI. CONCLUSION

Petitioner has not proven by a preponderance of the evidence that claims 1–30 are unpatentable. Patent Owner respectfully requests that the Board confirm the patentability of all challenged claims.

Dated: May 29, 2026

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATION

Pursuant to 37 C.F.R. § 42.24(d), Patent Owner certifies that this Sur-Reply complies with the type-volume limits of 37 C.F.R. § 42.24 because, according to the word count provided by the word-processing system used to prepare this paper, it contains 5,595 words, excluding the parts of the document exempted by 37 C.F.R. § 42.24.

Dated: May 29, 2026

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), the undersigned certifies that a true and correct copy of the foregoing Patent Owner's Sur-Reply was served in its entirety on May 29, 2026 by filing this document through the Patent Trial and Appeal Board End to End (PTACTS) System, and by causing true and correct copies to be served by electronic mail on Petitioner's lead and back-up counsel of record at the following email addresses:

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