

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

ADVANCED CLUSTER SYSTEMS, INC.,
Patent Owner.

IPR2025-00913
Patent 11,570,034 B2

Before KARL D. EASTHOM, ARTHUR M. PESLAK, and
BRIAN P. MURPHY, *Administrative Patent Judges*.

MURPHY, *Administrative Patent Judge*.

JUDGMENT

Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

A. Background and Summary

Intel Corporation (“Petitioner”) filed a Petition pursuant to 35 U.S.C. § 311 requesting institution of *inter partes* review of claims 1–30 of U.S. Patent No. 11,570,034 B2 (Ex. 1001, “the ’034 patent”). Paper 3 (“Pet.”). Advanced Cluster Systems, Inc. (“Patent Owner”) timely filed a Patent Owner Preliminary Response. Paper 10 (“Prelim. Resp.”). The Acting Director of the Office denied Patent Owner’s request for discretionary denial and referred the Petition to the Board for a decision on institution. Paper 13. On November 7, 2025, we issued a decision to institute *inter partes* review of claims 1–30 of the ’034 patent pursuant to 35 U.S.C. § 314 based on the challenges set forth in the Petition. Paper 16 (“Institution Decision” or “DI”).

Subsequent to institution, Patent Owner filed a Response. Paper 22 (“Resp.”). Petitioner filed a Reply, and Patent Owner filed a Sur-Reply. Paper 24 (“Reply”); Paper 25 (“Sur-Reply”). We heard oral argument from the parties in a consolidated oral hearing for IPR2025-00913–00916 on August 13, 2026. Paper 30 (“Tr.”).

We have jurisdiction under 35 U.S.C. § 6. This is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of claims 1–30 of the ’034 patent. We conclude Petitioner has demonstrated by a preponderance of the evidence that claims 1–30 of the ’034 patent are unpatentable.

B. Real Parties in Interest and Related Matters

Petitioner identifies Intel Corporation and Advanced Micro Devices, Inc. as the real parties in interest.¹ Pet. 96. Patent Owner, Advanced Cluster Systems, Inc., identifies itself as the real party in interest. Paper 5, 2.

The Parties identify the following related matters involving the '034 patent:

- *Advanced Cluster Systems, Inc. v. Intel Corporation*, No. 7:24-cv-00245 (W.D. Tex.) (stayed); and
- *Advanced Cluster Systems, Inc. v. Advanced Micro Devices, Inc.*, No. 7:24-cv-00244 (W.D. Tex.) (dismissed).

Pet. 96; Paper 5, 2; Paper 18; Paper 23.

The Parties identify the following matters involving patents related to the '034 patent:²

- *Advanced Cluster Systems, Inc. v. NVIDIA Corporation*, No. 1:19-cv-02032 (D. Del.) (dismissed);
- *NVIDIA Corporation v. Advanced Cluster Systems, Inc.*, IPR2021-00019 (PTAB) (institution denied);
- *NVIDIA Corporation v. Advanced Cluster Systems, Inc.*, IPR2021-00020 (PTAB) (institution denied);
- *Intel Corp. v. Advanced Cluster Systems, Inc.*, IPR2025-00794 (PTAB) (Director discretionary denial);
- *Intel Corp. v. Advanced Cluster Systems, Inc.*, IPR2025-00795 (PTAB) (Director discretionary denial);

¹ Advanced Micro Devices, Inc. was terminated as a party to this *inter partes* review proceeding and in related proceedings IPR2025-00914, 00915, and 00916 by Order granting Joint Motion to Terminate Proceedings as to Petitioner Advanced Micro Devices, Inc. Papers 20, 21.

² Patent Owner also identifies a series of patents and patent applications related to the '034 patent. Paper 5; Paper 23.

- *Advanced Micro Devices, Inc. v. Advanced Cluster Systems, Inc.*, IPR2025-00862 (PTAB) (Director discretionary denial);
- *Advanced Micro Devices, Inc. v. Advanced Cluster Systems, Inc.*, IPR2025-00863 (PTAB) (Director discretionary denial);
- *Intel Corp. v. Advanced Cluster Systems, Inc.*, IPR2025-00914 (PTAB) (pending);
- *Intel Corp. v. Advanced Cluster Systems, Inc.*, IPR2025-00915 (PTAB) (pending);
- *Intel Corp. v. Advanced Cluster Systems, Inc.*, IPR2025-00916 (PTAB) (pending);
- *Request for Ex Parte Reexamination of U.S. Patent No. 10,333,768*, Control No. 90/015,706.

Pet. 96; Paper 5, 2–3; Paper 18; Paper 23.

C. The '034 Patent

The '034 patent is titled “Cluster Computing” and issued on January 31, 2023 from an application filed on July 13, 2021. Ex. 1001, codes (22), (45), (54). The '034 patent “relates to the field of cluster computing generally and to systems and methods for adding cluster computing functionality to a computer program, in particular.” *Id.* at 1:15–18. Cluster computing enables “a group of two or more computers, microprocessors, and/or processor cores (‘nodes’)” to communicate with one another to accomplish programmed tasks “as though they were a single computer.” *Id.* at 1:22–25. The '034 patent distinguishes cluster computing from multi-node distributed (grid) computing where processing nodes “do not communicate with one another as peers” and “do not need to share data between the jobs during the computational process.” *Id.* at 1:48–56.

Figure 1 of the '034 patent, reproduced below, is a block diagram of a computer cluster where “computer systems 110, 120, 130 communicate with one another via a communications network 102.” *Id.* at 5:1–4.³

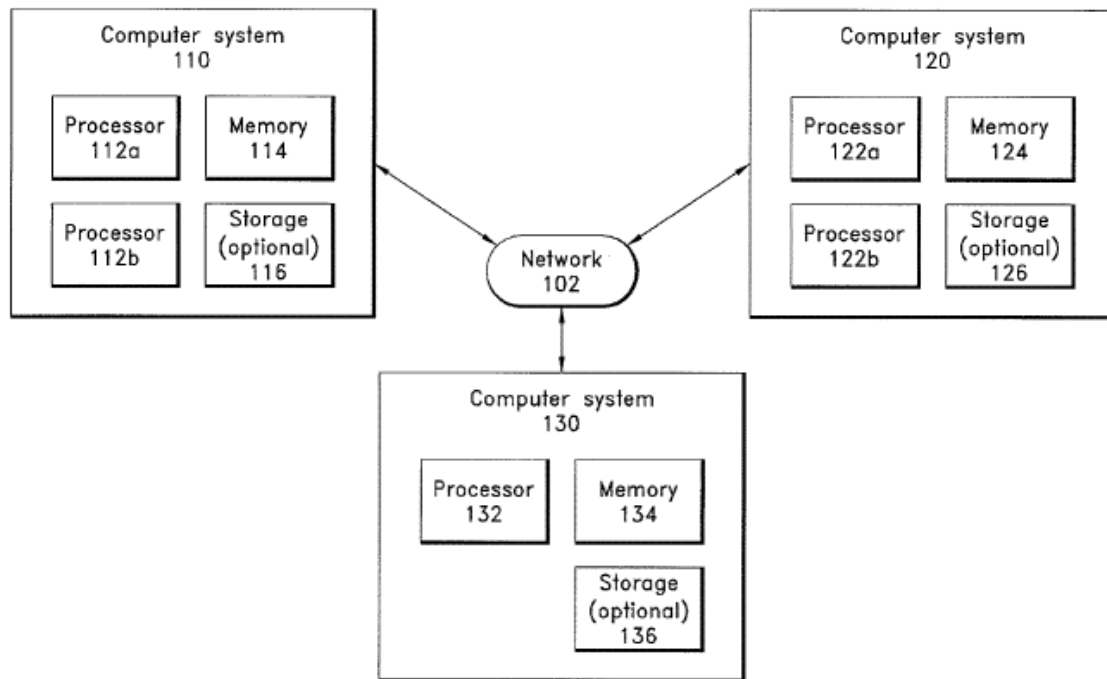


FIG. 1

Figure 1 of the '034 patent illustrates “a computer cluster 100 wherein computer systems 110, 120, 130 communicate with one another via a communications network 102.” *Id.*

In Figure 1, each computer system (110, 120, 130) includes one or more processors (112a, 112b, 122a, 122b, 132), memory (114, 124, 134), and optional storage (116, 126, 136). *Id.* at 6:60–67. Each computer system also includes a network interface (not shown) for connecting to communications network 102, which can include one or more of a LAN, a WAN, an intranet, a wireless network, and/or the Internet. *Id.* at 6:67–7:4. “A computer system can include one or more processors, and each processor

³ Quotations from patent documents may omit or de-emphasize bold numerals.

can contain one or more processor cores that are capable of single-threaded execution” of software code. *Id.* at 5:11–14.

Figure 2 of the '034 patent, reproduced below, “is a block diagram showing relationships among software modules running on one embodiment of a computer cluster 100.” *Id.* at 5:21–23.

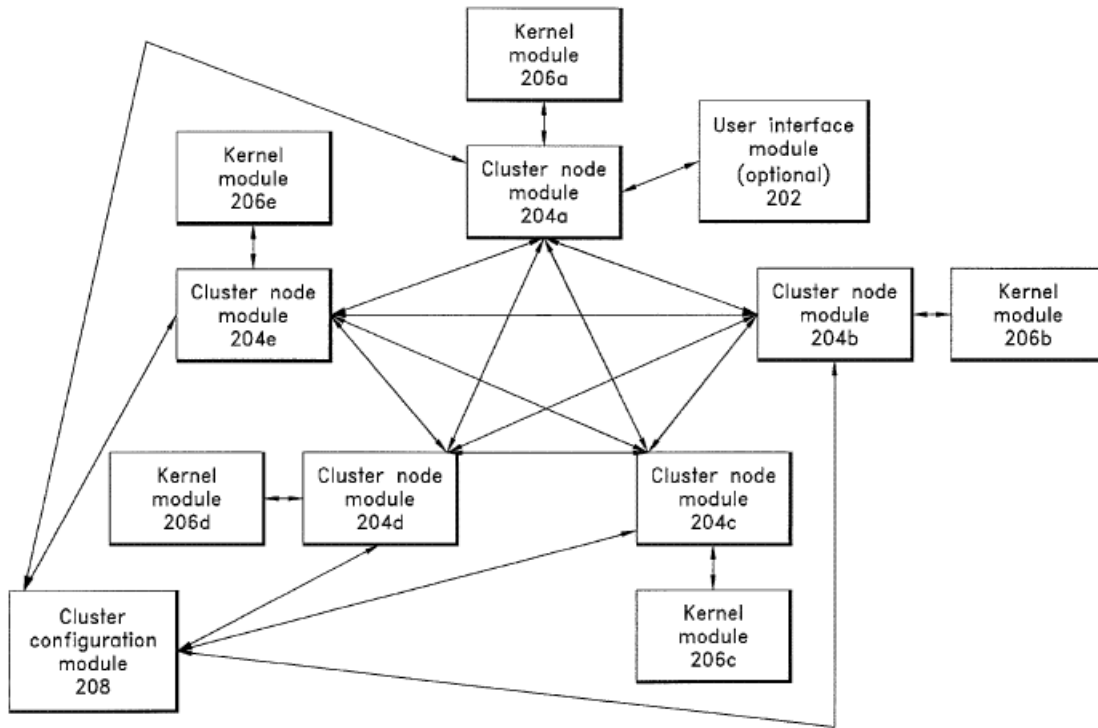


FIG. 2

Figure 2 depicts a cluster of software modules enabled for communication “between any two or more cluster node modules.” *Id.* at 6:14–17.

In the embodiment of Figure 2, user interface module 202 communicates with first cluster node module 204a, which is in communication with all other cluster node modules 204b–204e. *Id.* at 5:47–51, 11:18–26. The node-to-node communication architecture allows the user interface module to access kernel modules 206a–206e through cluster node 204a. *Id.* at 11:18–26. Kernel modules 206a–206e each include single-threaded software code for executing instructions (tasks) provided to the

program, *e.g.* via the user interface module, and each kernel is associated with one processor (112a, 112b, 122a, 122b, or 132 in Figure 1). *Id.* at 1:33–36, 11:33–35. For example, “MPI calls and advanced cluster commands are used to parallelize program code received from an optional user interface module . . . and distribute tasks among the kernel modules.” *Id.* at 6:20–23. Cluster configuration module 208 communicates with cluster node modules 204a–204e to “initialize[] the cluster node modules to provide cluster computing support for . . . computer cluster 100.” *Id.* at 11:39–43.

The initialized cluster node modules “provide communications among kernel modules 206a-e while the tasks are executing.” *Id.* at 6:23–25, 11:45–48. The ’034 patent notes that “single-threaded software code typically does not benefit from multiple processor cores in a computer system,” but in the patented system “two kernel modules (for example, kernel modules 206a, 206b) loaded into the memory . . . of computer system 110 could exploit at least some of the processing bandwidth of the two processors 112a, 112b.” *Id.* at 5:18–30. Results of the mathematical expression evaluations executed by the kernel modules “are communicated back to the first cluster node module 204a via the cluster node modules 204a-e, which communicates them to the user interface module.” *Id.* at 6:26–29.

In short, “[i]ntercommunication provided by cluster computing permits exchange of information between nodes during the course of a parallel computation” to improve computational performance. *Id.* at 6:30–36.

D. Illustrative Claim

Petitioner challenges claims 1–30 of the ’034 patent. Pet. 27–94. Claims 1, 25, 28, and 30 are the independent claims. Claims 2–24 depend,

directly or indirectly, from claim 1. Claims 26–27 depend directly from claim 25. Claim 29 depends from claim 28. Claim 1, reproduced below with Petitioner’s bracketed identifiers, illustrates the claimed subject matter:

[1.0] A computer cluster comprising:

[1.1.1] a plurality of nodes, wherein each of the plurality of nodes comprises a hardware processor, [1.1.2] wherein one or more of the nodes are configured to receive a command to start a cluster initialization process for the computer cluster, and [1.1.3] wherein each of the nodes is configured to access a non-transitory computer-readable medium comprising program code for a single-node kernel that, when executed, is capable of causing the hardware processor to evaluate mathematical expressions; and

[1.2] a communications network interface for the nodes to communicate results of mathematical expression evaluation with each other using a peer-to-peer architecture;

[1.3.0] wherein the plurality of nodes comprises:

[1.3.1] a first node comprising a first hardware processor configured to access a first memory comprising program code for a user interface and program code for a first single-node kernel, [1.3.2] the first single-node kernel configured to interpret user instructions and distribute calls to at least one of a plurality of other nodes for execution; and

[1.4.1] a second node comprising *a second hardware processor with a plurality of processing cores*, [1.4.2] wherein the second node is configured to receive calls from the first node, execute at least a first mathematical expression evaluation, and communicate a result of the first mathematical expression evaluation to a third node;

[1.5.1] wherein the third node comprises *a third hardware processor with a plurality of processing cores*, [1.5.2] wherein the third node is configured to receive the result of the first mathematical expression evaluation from the second node, execute at least a second mathematical expression evaluation

using the received result, and *communicate the result of the second mathematical expression evaluation to the first node*;

[1.6] *wherein the first node is configured to return the result of the second mathematical expression evaluation to the user interface*;

[1.7.0] wherein one or more of the nodes are configured to:

[1.7.1] accept user instructions;

[1.7.2] after accepting user instructions, communicate at least some of the user instructions using the communications network interface for the nodes to communicate with each other; and

[1.7.3] after communicating at least some of the user instructions using the communications network interface, communicate at least some of the user instructions to one or more single-node kernels.

Ex. 1001, 29:30–30:13 (emphases added).

E. Prior Art and Asserted Grounds

Petitioner asserts claims 1–30 are unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–25, 27–28, 30	103(a) ⁴	Menon, ⁵ Trefethen, ⁶ RS6000, ⁷

⁴ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), includes revisions to 35 U.S.C. §§ 102 and 103 that became effective after the filing date of the earliest priority application that led to issuance of the challenged patent. Hence, this *inter partes* review is governed by the pre-AIA provisions of 35 U.S.C. §§ 102 and 103.

⁵ *MultiMATLAB: Integrating MATLAB with High-Performance Parallel Computing*, Menon et al., SC '97: Proceedings of the 1997 ACM/IEEE Conference on Supercomputing 1997 (“Menon”) (Ex. 1005).

⁶ *MultiMATLAB: MATLAB on Multiple Processors*, Trefethen et al., 1996 Computer Science Technical Report, Cornell University 1996 (“Trefethen”) (Ex. 1006).

⁷ RS/6000 SP: Planning Vol. 1, *Hardware and Physical Environment*,

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
		POEref, ⁸
26, 29	103(a)	Menon, Trefethen, RS6000, POEref, MPIref ⁹

Pet. 14. Petitioner relies on the expert Declaration of Chandrajit L. Bajaj, Ph.D. (Ex. 1003) in support of the Petition.¹⁰ Patent Owner relies on the expert Declaration of Melissa Smith, Ph.D. (Ex. 2017) in support of the Response and Sur-Reply. Petitioner relies on the Supplemental Declaration of Dr. Bajaj (Ex. 1163) and Declaration of expert librarian Ingrid Hsieh-Yee, Ph.D. (Ex. 1086) in support of the Reply.

II. ANALYSIS

A. Level of Ordinary Skill in the Art

Petitioner contends:

A person of ordinary skill in the art (“POSITA”) in June 2006 would have been someone knowledgeable of and familiar with computer cluster systems and cluster computing techniques available at the time. Such a POSITA would have a bachelor’s degree in computer science, computer engineering, electrical engineering, or an equivalent training, and approximately two years of experience working in the field of cluster computing or parallel processing and would be knowledgeable regarding high-level scientific computing languages. Additional work experience can substitute for specific educational background, and vice versa.

IBM 2001 (“RS6000”) (Ex. 1007).

⁸ Operation and Use, Volume 1, *Using the Parallel Operating Environment*, IBM 2001 (“POEref”) (Ex. 1008).

⁹ *MPI: A Message-Passing Interface Standard*, Message Passing Interface Forum, 1994 (“MPIref”) (Ex. 1017).

¹⁰ The Petition relies on fact declarations to support the public accessibility of Menon, Trefethen, RS6000, POEref, and MPIref, an issue we address in section II.E. below. Pet. 14–16; *see* Exs. 1027, 1029, 1047–1049).

Pet. 12 (citing Ex. 1003 ¶¶ 18–23); *see also* Ex. 1003 ¶¶ 24–27 (addressing level of ordinary skill in the art). Patent Owner does not address the level of skill in the art, although Dr. Smith characterizes the level of ordinary skill in the field of cluster computing at the time of the '034 patent in a manner consistent with the Petition and Dr. Bajaj. *See* Resp. *generally*; *see also* Ex. 2017 ¶¶ 21–22 (“a POSITA would have had a Bachelor’s degree in computer science, electrical engineering, or an equivalent field, and two years of academic or industry experience in cluster computing and parallel computation techniques”).

In determining the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (citing *Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986)). “These factors are not exhaustive but are merely a guide to determining the level of ordinary skill in the art.” *Daiichi Sankyo Co. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007). There is uncontested evidence in the record before us that reflects the knowledge and experience of a POSITA.

We adopt the Petition’s formulation of the level of ordinary skill in the art, which is consistent with the '034 patent, the prior art of record, and the testimony of both experts.

B. Claim Construction

In this *inter partes* review, we apply the same claim construction standard that would be used in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b). Applying that standard, we generally give claim

terms their ordinary and customary meaning as would be understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005) (en banc). Claim terms “are generally given their ordinary and customary meaning” as understood by a POSITA at the time of the invention. *Phillips*, 415 F.3d at 1312. When construing a disputed claim limitation, “we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

The Petition relies on the ordinary and customary meaning of the claim terms consistent with the *Phillips* standard. Pet. 12–13 (citing 37 C.F.R. § 42.100(b)). The Petition also addresses the construction of “*peer-to-peer architecture*” recited in independent claims 1 and 30 of the ’034 patent, a limitation we need not construe to resolve the parties’ dispute in this proceeding. *Id.* at 13; *see, e.g., Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“[C]laim terms need only be construed ‘to the extent necessary to resolve the controversy.’”) (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Patent Owner’s Response construes the claim language recited as “a [second/third] hardware processor with a plurality of processing cores” in limitations [1.4.1] and [1.5.1]. Resp. 10–16.¹¹ We address Patent Owner’s claim construction contentions below.

¹¹ The same language is recited in independent claims 25 and 28. Independent claim 30 recites “*the hardware processor comprises multiple processor cores.*” Resp. 10–11.

Construction of “a . . . hardware processor with a plurality of processing cores”

In our Institution Decision, we ordered the parties to analyze and construe the claim phrase “*a . . . hardware processor with a plurality of processing cores*,” as recited in limitations [1.4.1] and [1.5.1], “with particular attention to the description of processors and processor cores in the ’034 patent.” DI 14, 49–50. We begin with a discussion of what the claim language in dispute does not recite.

The claim language at issue does not recite a “single multi-core processor,” “multi-core” processor, or “singular ‘hardware processor’ that ‘comprises’ (or ‘with’) multiple ‘processing cores’” as Patent Owner contends. Resp. 11–12, 21; *see also* Ex. 1163 ¶ 22 (“The claim does not recite ‘single chip,’ ‘single package,’ ‘single die,’ or ‘single multi-core microprocessor.’”). Nor do the claims recite a plurality of processing cores “within” a single-chip package or read as “multi-core within a processor” as argued by Patent Owner. Resp. 12–14; Sur-Reply 2; *see* Reply 6 (citing Ex. 1163 ¶ 23 (“Thus, the phrase ‘with a plurality of processing cores’ identifies the required processing resources associated with the hardware processor; it does not import a packaging limitation.”)). The claims do recite a hardware processor “*with*” a plurality of processing cores; a critical distinction even Patent Owner reads as open-ended, i.e., as a hardware processor that “comprises” a plurality of processing cores. *See* Resp. 11 (“the claims require a singular ‘hardware processor’ that ‘comprises’ (or ‘with’) multiple ‘processing cores’”). Consequently, the claim language does not support Patent Owner’s proposed construction of “*a . . . hardware processor with a plurality of processing cores*” as a single multi-core processor.

Patent Owner makes a distinction between a “processor” and “the cores it contains” in reliance on a parsed description in the ’034 patent specification:

The specification explains: “Each processor can contain one or more processor cores that are capable of single-threaded execution. Processor cores are generally independent microprocessors, but more than one can be included in a single-chip package.”

Id. at 12¹² (partially quoting Ex. 1001, 5:11–16); Sur-Reply 2. The quoted description does not support Patent Owner’s contention that the claimed “a . . . hardware processor with a plurality of processing cores” must be limited to a “single multi-core processor” that “locates multiple cores within a ‘single-chip package,’” i.e. limited to a single multi-core microprocessor such as “a Core 2 Duo is one processor package with two cores.” Resp. 12–13, 21 (citing Ex. 1001, 7:15–25). The description quoted above from column 5, moreover, describes a “processor” that “can contain one or more processor cores” each of which can be an independent microprocessor. Reply 2–3 (citing Ex. 1001, 5:11–16; Ex. 1163 ¶¶ 10–14). As Petitioner emphasizes, the specification distinguishes a “processor” from a “microprocessor” and describes a “processor” that “can be one or more general purpose single-core or multi-core microprocessors,” rather than limiting a “processor” to a single multi-core microprocessor. Reply 3–5 (citing Ex. 1001, 7:14–36, Fig. 1; Ex. 1163 ¶¶ 15–18).

Patent Owner concedes that the specification “expressly contemplate[es] ‘single-core or multi-core microprocessors.’” Resp. 13 (citing Ex. 1001, 7:15–25). Patent Owner then makes an inconsistent

¹² The ’034 patent claims recite a “hardware processor;” the specification refers to a “processor,” “processors,” and “microprocessors.”

argument attempting to limit the claims “to a specific hardware model” by referencing an example of a single multi-core microprocessor described in the ’034 patent: “a Core 2 Duo is a single processor chip with two integrated cores—not two processors on a board.” *Id.* at 16 (citing Ex. 2017 ¶¶ 26, 33). Patent Owner’s reasoning is circular. The claim language does not limit a hardware processor to a single chip processor with two integrated cores, and the Core 2 Duo microprocessor is but one example among others described in the ’034 patent, such as the MIPS processor “composed of a plurality of individual microprocessors (called ‘coprocessors’).” Reply 8–9 (citing Ex. 1001, 7:24, 9:59; Ex. 1163 ¶ 27; Ex. 1168, 14, 20); *see also* Ex. 1001, 7:16–25 (listing commercially available microprocessors). The description in the specification of a “processor” that can be one or more general purpose single-core or multi-core microprocessors indicates that the claims are not limited to a single multi-core processor in a single chip package (a single multi-core microprocessor). Thus, the claim language and specification undercut Patent Owner’s proposed construction.

We further note the ’034 patent describes a “processing core” functionally as a “processing unit[] capable of single-threaded execution” of program code, without requiring multiple processing cores within a single chip package. *Id.* at 7:27–31, 8:46–48, 9:62–64; *see* Resp. 13–14 (arguing “Petitioner’s proposed reading strips the ‘single-chip package’ language of meaning”). As Petitioner correctly points out, the specification makes clear that single-threaded execution of program code is implemented in a computer system that “can include *one or more processors*, and each processor can contain *one or more processor cores* that are capable of single-threaded execution.” Reply 2–3 (quoting Ex. 1001, 5:11–16) (citing

Ex. 1163 ¶¶ 9–14). We find Petitioner’s analysis to be consistent with the functional description of a processing core in the ’034 patent.

Patent Owner further argues:

Moreover, even if some disclosure in the specification could be read to describe broader hardware implementations, it does not follow that these particular claim limitations must be construed to capture that breadth. It is well established that when a construction is supported by the intrinsic evidence that “the claims of the patent need not encompass all disclosed embodiments” *if including other embodiments would contradict the plain language of the claim*, and it is common for different claims to cover different embodiments. Here, *the claim language explicitly reads as multi-core within a processor*, the specification confirms that usage, and Petitioner’s alternative construction would *rewrite the claims* to fit RS6000 rather than apply the claims against RS6000.

Id. at 14 (emphasis added) (citing *TIP Sys., LLC v. Phillips & Brooks/Gladwin, Inc.*, 529 F.3d 1364, 1373 (Fed. Cir. 2008); *Baran v. Med. Device Techs., Inc.*, 616 F.3d 1309, 1316 (Fed. Cir. 2010)). The claim language and specification do not support Patent Owner’s argument. The ’034 patent claim language does not explicitly recite, or read as being limited to, a single multi-core processor (or multiple processing cores within a single-chip package). Nor does a claim construction of “one or more single-core or multi-core microprocessors with a plurality of processing cores,” as proposed by Petitioner and described in the specification, contradict or rewrite the claim language. Reply 1–6.

Patent Owner’s Response, moreover, avoids addressing the ’034 patent’s use of modifiers such as “can include,” “can contain,” “can be included,” “for example,” “one embodiment,” and “one or more” in the relevant descriptions cited by the parties. Resp. 11–16; *see also* Reply 2–6 (citing Ex. 1001, 5:11–16, 7:15–34, 9:51–10:1); Sur-Reply 1–5. Those

modifiers reflect exemplary description of alternative embodiments claimed as “a . . . *hardware processor with a plurality of processing cores*,” and we find nothing in the specification of the ’034 patent that would require limiting the claim phrase to a single multi-core processor (or multiple processing cores within a single chip package) as argued by Patent Owner. We will not read a preferred embodiment from the specification into claim language that is not so limited. *See SuperGuide Corp. v. DirecTV Enterprises, Inc.*, 358 F.3d 870, 875 (Fed. Cir. 2004) (care should be taken “not to import into a claim limitations that are not part of the claim”); *see also In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993) (“limitations are not to be read into the claims from the specification”); *see also IQIRIS Techns. LLC v. Point Blank Enterprises, Inc.*, 130 F.4th 998, 1004 (Fed. Cir. 2025) (“It is the claims, not the preferred embodiments, that define the metes and bounds of the patentee’s invention.”) (citing *Phillips*).

We also credit Dr. Bajaj’s un rebutted testimony regarding the ’034 patent specification and the meaning of the claimed “*hardware processor*”:

In summary, the specification describes the following:

- a processor can contain one or more independent microprocessors (Ex. 1001, 5:11–16):
- a processor can be one or more single-core or multi-core microprocessors (Ex. 1001, 7:14–36); and
- a processor can be multiple microprocessors (Ex. 1001, 9:50–10:3).

Based on this clear disclosure in the ’034 specification, a POSITA would understand that the plain and ordinary meaning of “a hardware processor with a plurality of processing cores” is “one or more single-core or multi-core microprocessors with a plurality of processing cores.”

Ex. 1163 ¶¶ 19–20 (citing Ex. 1001, 5:11–37, 7:14–36, 9:50–10:3). We find Dr. Bajaj’s testimony to be consistent with the ’034 patent claim language and description of a processor, microprocessor, and processing core as discussed above.¹³

Patent Owner’s Sur-Reply repeats the argument of the Response that the claim language “*a . . . hardware processor with a plurality of processing cores*” means “a singular processor; a plurality of cores; the cores are within — contained in or part of — the recited processor.” Sur-Reply 2 (underlining added). As stated above, Patent Owner’s argument rewrites the claim language by substituting a closed form, where a plurality of processing cores are “within” a single processor, for the open form actually claimed: “*a hardware processor with a plurality of processing cores*.” Patent Owner’s further Sur-Reply argument, that the patentee did not act as lexicographer or “make any clear and unmistakable disavowal” in the specification, undercuts its own argument attempting to limit the claim language to a single multi-core processor. *Id.* at 1.

Patent Owner even agrees that the three specification passages cited in Petitioner’s Reply “describe *exemplary* architectural configurations” and the “enumerated *examples* are individual *single-core or multi-core* microprocessor models.” *Id.* at 2–3 (emphases added). Yet, Patent Owner insists that “nothing in the text supports Petitioner’s reading that cores need not be in the same package” and that Patent Owner’s “proposed

¹³ Dr. Smith does not construe “*a . . . hardware processor with a plurality of processing cores*.” See Ex. 2017 ¶¶ 8–9 (“I have not analyzed nor expressed any opinion . . . about any subject that is not expressly included in the section labeled “SUBSTANTIVE TESTIMONY.”). Dr. Smith applies Patent Owner’s proposed “plain and ordinary meaning” of “*hardware processor*” to the prior art. *Id.* ¶¶ 26–36.

interpretation properly excludes a single-core microprocessor.” *Id.* at 3–4. Patent Owner’s arguments are internally inconsistent, inconsistent with the claim language, specification, and unrebutted extrinsic evidence of record, and inconsistent with governing case law prohibiting the exclusion of exemplary embodiments absent clear disavowal, disclaimer, or lexicography. Reply at 7–10 (citing *Verizon v. Vonage Holdings*, 503 F.3d 1295, 1305 (Fed. Cir. 2007) (rejecting proposed claim interpretation that would exclude disclosed examples in the specification)); *see also Verizon*, 503 F.3d at 1306 (“To operate as a disclaimer, the statement in the prosecution history must be clear and unambiguous, and constitute a clear disavowal of scope.”).¹⁴

In sum, the claims do not recite “a single multi-core processor” or “a processor within a single chip package,” and there is no basis to exclude embodiments of a hardware processor configured with multiple single-core or multi-core microprocessors described in the specification. We agree with Petitioner’s analysis that the plain and ordinary meaning of “*a . . . hardware processor with a plurality of processing cores*” is one or more single-core or multi-core microprocessors with a plurality of processing cores. Reply 1–2.

C. Asserted Obviousness of Claims 1–25, 27–28, and 30

Ground 1 in the Petition contends that claims 1–25, 27–28, and 30 of the ’034 patent are obvious over Menon in view of Trefethen, RS6000 and POEref. Pet. 16–87 (citing Ex. 1003 ¶¶ 65–89, 104–108, 113–115, 118, 121–122, 157–465). The Petition asserts that Menon, Trefethen, RS6000 and POEref disclose, teach, suggest or otherwise render obvious all

¹⁴ Patent Owner does not cite to any portion of the prosecution history in support of its proposed construction.

limitations recited in the claims. *Id.* Patent Owner contends Petitioner has failed to meet its burden to show by a preponderance of the evidence that all challenged claims are unpatentable, a contention based on a “small number of dispositive issues that run through every instituted ground and every challenged independent claim.” Resp. 3–6 (summarizing six arguments). For the reasons that follow, we determine the Petition establishes by a preponderance of the evidence that claims 1–25, 27–28, and 30 of the ’034 patent are obvious over Menon, Trefethen, RS6000 and POEref.

“In an *inter partes* review, the burden of persuasion is on the petitioner to prove ‘unpatentability by a preponderance of the evidence,’ 35 U.S.C. § 316(e), and that burden never shifts to the patentee.” *In re Magnum Oil Tools Int’l Ltd.*, 829 F.3d 1364, 1375 (Fed. Cir. 2016) (quoting *Dynamic Drinkware, LLC v. Nat’l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015)); *see also Aqua Products, Inc. v. Matal*, 872 F.3d 1290, 1306 (Fed. Cir. 2017 (en banc (quoting *Magnum Oil*)).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time the invention was made. *See KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007) (quoting 35 U.S.C. § 103(a)). Obviousness is resolved based on underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). A party who petitions the Board for a determination of obviousness must show that “a skilled artisan would have been motivated to

combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.” *Procter & Gamble Co. v. Teva Pharms. USA, Inc.*, 566 F.3d 989, 994 (Fed. Cir. 2009) (quoting *Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1361 (Fed. Cir. 2007)).

We begin our analysis with a discussion of the Menon, Trefethen, RS6000, and POEref references.

Menon and Trefethen are authored by the same research group at Cornell University and together disclose integrating MATLAB software with a high-performance parallel computing platform that uses multiple microprocessors—the IBM SP2 parallel operating platform. Ex. 1005, 1 (Abstract), 2, 5–6; Ex. 1006, 1–2, 10, 12. The MultiMATLAB system disclosed in Menon-Trefethen utilizes a form of cluster computing that relies on point-to-point (“peer-to-peer”) communication among nodes through an interconnecting network. Ex. 1005, 3–4, 9–10, Figs. 1–2, Table 1 (SPMD Communication commands); *see also* Pet. 16–21.¹⁵ RS6000 is part of the IBM installation manual for the SP2 platform. Ex. 1007. POEref is the operation manual for the IBM Parallel Operating Environment (“POE”) in which the SP2 platform operates to initialize MATLAB. Ex. 1008. A more detailed summary of each reference follows.

1. Overview of Menon (Ex. 1005)

Menon, titled “MultiMATLAB: Integrating MATLAB with High-Performance Parallel Computing,” is directed to a computing environment architecture that enables MATLAB to operate in parallel on multiple

¹⁵ The ’034 patent “disclosure is not limited to a single software program; the systems and methods can be used with other application software such as, for example, . . . MATLAB®.” Ex. 1001, 4:21–24.

microprocessors. Ex.1005, Title, Abstract. Menon describes MultiMATLAB as “a general extension” of the MATLAB computing platform disclosed in Trefethen for running “high-performance parallel routines.” *Id.* at Abstract. MultiMATLAB comprises several microprocessors, each configured to run a MATLAB process (a node) that communicates “with other processes through a communication layer that runs over the parallel platform’s interconnection network.” *Id.* at 3, Fig. 1.

The communication layer uses Message Passing Interface (“MPI”) to communicate “over the parallel platform’s interconnection network.” Ex. 1005, 3, 5. Menon Figure 1 is reproduced below:

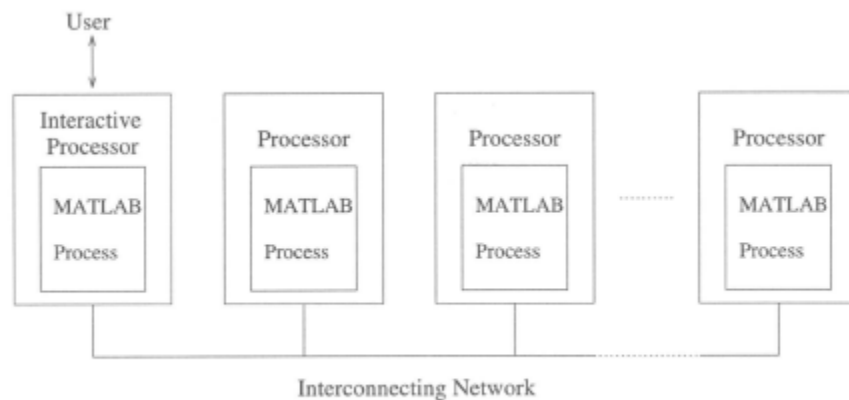


Figure 1: MultiMATLAB Architecture

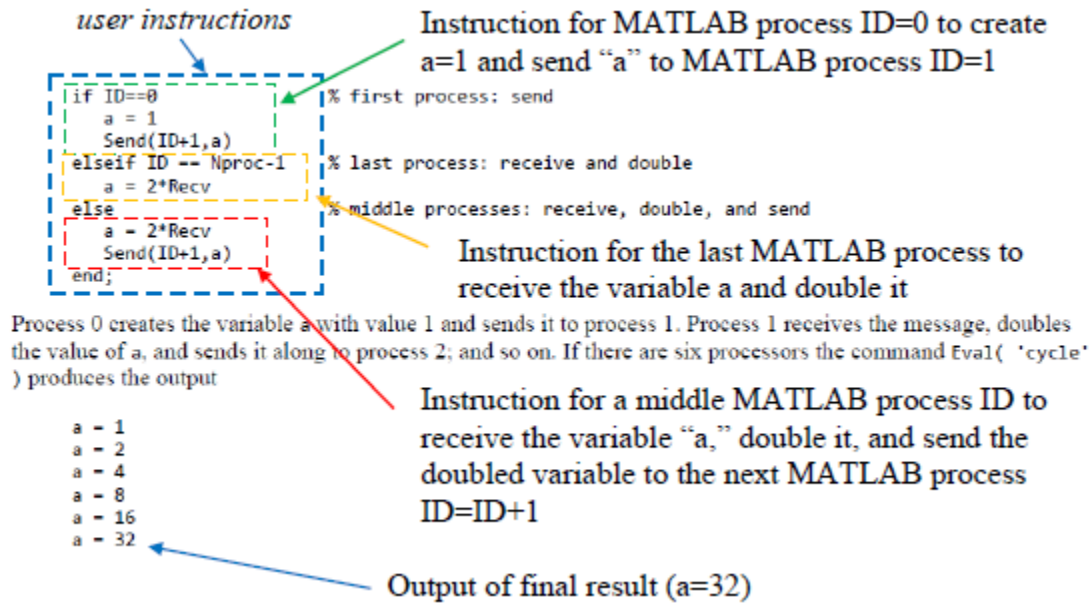
As shown in Figure 1, in Menon’s MultiMATLAB architecture a user “interacts directly with ... the interactive process,” and the “other processes wait for commands from the interactive MATLAB process.” *Id.* at 3, 6. Menon discloses using MultiMATLAB on a “parallel platform,” such as “the IBM SP2” and “IBM RS6000,” to evaluate mathematical expressions. *Id.* at 2, 5, 11. Menon explains that MultiMATLAB works with different parallel programming paradigms, including “SPMD/Message passing” that provides “point to point” communication. *Id.* at 8–10; Table 1. Menon

further discloses that MultiMATLAB uses “MEX Routines,”¹⁶ an “interface module,” “indirection table,” and a “communication layer” to provide direct point-to-point communication for sending and receiving data between modules (nodes). Ex. 1003 ¶¶ 104–106; Ex. 1005, 3, 5, 9, Table 1.

2. Overview of Trefethen (Ex. 1006)

Trefethen, titled “MultiMATLAB: MATLAB on Multiple Processors,” pre-dates Menon and discloses a system “that enables one to run MATLAB conveniently on multiple processors,” such as in the “IBM SP2,” “for fast and convenient execution of easily parallelizable numerical computations on multiple processors.” Ex. 1006, 1 (Abstract); *see also id.* at 3–9. Trefethen discloses that “point-to-point communication is accomplished by send and receive commands.” *Id.* at 5–6. Trefethen teaches the use of “Send” and “Recv” commands to allow direct communication among nodes, as shown in annotated form in the Petition, reproduced below:

¹⁶ MEX is an interface system that allows MATLAB users to execute commands originally written in C or Fortran programming language, such as Send and Recv, commands. Ex. 1006, 10; Ex. 1023, 6–7.



Pet. 21 (annotated Ex.1006, 6). The sample code shown above illustrates:

- node 0 sending data “a = 1” to node 1,
- node 1 performing a mathematical calculation (multiply “a” by 2) and sending the result to node 2,
- node 2 performing a mathematical calculation (multiply “a” by 2) and sending the result to the next node (“and so on”), and
- the result (a=32) is output to the user.

Id. (citing Ex. 1003 ¶ 115; Ex. 1006, 6).

3. Overview of RS6000 (Ex. 1007)

RS6000, titled “RS/6000 SP: Planning Vol. 1, Hardware and Physical Environment,” is an IBM product manual for the IBM SP2 system used in Menon. Pet. 15, 21–22 (citing Ex. 1003 ¶ 118–120; Ex. 1007, 1–2;¹⁷ Ex. 1010, 6; Ex. 1029; Ex. 1038). RS6000 discloses that the “RS/6000 SP is IBM’s family of scalable, parallel computing solutions” and that the system

¹⁷ We cite to the exhibit page numbers added to the lower right corner of Ex. 1007, rather than the internal page numbers of RS6000.

includes POWER3 processors for executing “both serial and parallel applications.” Ex. 1007, 1. RS6000 discloses that “[t]he IBM RS/6000 SP System is scalable from one to 128 processor nodes” and that it uses “four, eight, twelve, or sixteen 375 MHz 630FP 64-bit processors per node.” *Id.* at 2, 9.

4. Overview of POEref (Ex. 1008)

POEref, titled, “Operation and Use, Volume 1, Using the Parallel Operating Environment” is an IBM product manual for “the IBM Parallel Environment (PE)” and “its Parallel Operating Environment (POE)” running on an RS6000 system, as referenced in Menon. Pet. 15, 22 (citing Ex. 1003 ¶¶ 121–125; Ex. 1005, 6; Ex. 1008, 11¹⁸; Ex. 1029; Ex. 1036; Ex. 1039; Ex. 1047). POEref discloses an initialization process where a user enters the “poe” (parallel operating environment) command, such that “[w]hen you invoke poe, the Partition Manager allocates processor nodes for each task and initializes the local environment. It then loads your program, and reproduces your local environment, on each processor node.” Ex. 1008, 46.

5. Analysis of Claim 1 in View of Menon, Trefethen, RS6000, and POEref

Petitioner asserts that claim 1 would have been obvious over Menon, Trefethen, RS6000, and POEref. Pet. 22–53 (citing Ex. 1003 ¶¶ 65–89, 118, 124, 132–133, 157–243). Our Institution Decision addressed in detail the Petition’s argument and evidence that the combination of Menon, Trefethen, RS6000, and POEref discloses, teaches, suggests, or otherwise renders obvious independent claim 1 of the ’034 patent. DI 22–39 (Paper 16). We do not repeat that analysis here, except to address Patent Owner’s

¹⁸ We cite to the exhibit page numbers added to the lower right corner of Ex. 1008, rather than the internal page numbers of POEref.

arguments, including arguments that the asserted references do not disclose, teach, suggest, or otherwise render obvious claim limitations [1.4.1], [1.5.1], [1.4.2], [1.5.2], and [1.6] or the comparable limitations in dependent claim 2 and independent claims 25, 28, and 30. Resp. 21–40. *See Redline Detection, LLC v. Star Envirotech, Inc.*, 811 F.3d 435, 450 (Fed. Cir. 2015) (“arguments on appeal that were not presented to the [PTAB]” are waived) (citing *In re Watts*, 354 F.3d 1362, 1367 (Fed. Cir. 2004)).

Our analysis of limitations [1.4.1], [1.5.1], [1.4.2], [1.5.2], and [1.6], as contested by Patent Owner, applies equally to independent claims 25, 28, and 30 and all other claims that depend therefrom. For the reasons articulated below and after review of the full record, we determine the Petition establishes by a preponderance of the evidence that claims 1–25, 27–28, and 30 of the ’034 patent are unpatentable as obvious over Menon, Trefethen, RS6000, and POEref. *See* Pet. 16–87 (citing Ex. 1003 ¶¶ 65–89, 104–108, 113–115, 118, 121–122, 157–465). We begin with Patent Owner’s arguments for limitations [1.4.1] and [1.5.1].

a. The asserted prior art need not disclose a single multi-core processor; limitations [1.4.1] and [1.5.1]

Patent Owner’s first argument relies on its proposed claim construction of “a . . . hardware processor with a plurality of processing cores” as limited to a single multi-core processor. Resp. 3, 17–19. Patent Owner argues the asserted prior art combination does not disclose the claimed hardware processor recited in limitations [1.4.1] and [1.5.1], “because RS6000 describes an SMP node populated with multiple discrete single-core processors, not a multi-core processor as required by the claims” *Id.* at 17 (citing Ex. 2017 ¶¶ 24–36); *see also id.* at 17 (“the properly construed claims require a single hardware processor that includes

multiple processor cores”), 17–18 (“RS6000’s SMP ‘configuration’—a node populated with multiple discrete single-core processors—does not disclose the required multicore processor limitation, as confirmed by Dr. Smith”), 19 (“[A]n SMP node . . . contains multiple separate, single-core CPU chips installed on one or more processor cards, *rather than a single processor chip that includes multiple cores.*”) (emphasis added). We give Dr. Smith’s cited testimony little weight because it applies Patent Owner’s proposed claim construction without analyzing the construction. *See, e.g.*, Ex. 2017 ¶¶ 28 (“The RS/6000 reference (Ex. 1007) never states that any individual hardware processor has multiple processing cores.”), 30 (“This [RS6000 Ex. 1007, 9] describes the number of hardware processors per node but says nothing about the number of processing cores per hardware processor.”), 31 (same).

For the reasons given above in our claim construction analysis of “*a . . . hardware processor with a plurality of processing cores,*” we find Patent Owner’s first argument to be unavailing because the prior art need not disclose a single multi-core processor (or multiple processing cores within a single chip package).

b. Motivation to combine and asserted teaching away

The Petition contends that Menon and Trefethen are analogous prior art because they pertain to the same “field of cluster computing” as the ’034 patent and “are reasonably pertinent to the problem of the ’034 patent, namely, executing a single program on multiple nodes.” Pet. 22 (citing Ex. 1001, 1:14–15; Ex. 1003, ¶¶ 65–69; Ex. 1005, 2; Ex. 1006, Abstract). The Petition emphasizes that Menon expressly cites and builds on the MultiMATLAB system taught by Trefethen. *Id.* (citing Ex. 1003 ¶ 71; Ex. 1005, 1–2). The Petition contends that:

Accordingly, Menon and Trefethen together represent a combination of prior art elements according to known methods (executing MATLAB code on a multiprocessor system) to yield the predictable result discussed in both papers: the MultiMATLAB system executing MATLAB in parallel to perform mathematical calculations.

Id. at 22–23 (citing Ex. 1003 ¶ 70; Ex. 1005, Abstract; Ex. 1006, 2–7). The Petition further contends that a POSITA would have found it predictable to combine Trefethen with Menon with a reasonable expectation of success “because researchers had a strong desire to parallelize MATLAB.” *Id.* at 23–24 (citing Ex. 1003 ¶ 73; Ex. 1005, 2; Ex. 1006, 11–12.)

The Petition next explains the asserted motivation for combining RS6000 with Menon, namely because RS6000 provides an overview of the IBM SP2 multiprocessor and Menon teaches the use of “IBM SP2, a modern high performance distributed memory multiprocessor” used in the MultiMATLAB system. *Id.* at 24–25 (citing Ex. 1003 ¶¶ 78–81; Ex. 1005, 5–6, 14; Ex. 1007, 1, 11). The Petition also explains why POEref pertains to the field of cluster computing in a parallel operating environment. *Id.* at 26 (citing Ex. 1008, 11 (“PE Software is designed to run on an ... RS/6000® network cluster”)); (further citing Ex. 1001, 1:14–15; Ex. 1003 ¶¶ 82–85). The Petition contends that a POSITA would have been motivated to combine the teachings of POEref with Menon “because Menon suggests the combination by teaching that MultiMATLAB uses ‘POE, IBM's Parallel Operating Environment.’” *Id.* at 26–27 (citing Ex. 1005, 6); (further citing Ex. 1003 ¶¶ 86–89; Ex. 1005, 14; Ex. 1008, 11, 46). We agree with Petitioner's analysis.

We find the Petition's argument and evidence of a motivation to combine the asserted prior art references in the manner claimed to be

compelling, persuasive, consistent with the disclosures in the references, which include internal cross-references to each other, and supported by the expert testimony of Dr. Bajaj.

Addressing Patent Owner's motivation to combine arguments

Patent Owner argues that the “generalized desire” to parallelize high-level mathematical computing environments “does not supply a reason to combine these references in the specific manner required by the claims, nor does it explain why a POSITA would have selected and implemented the particular multicore, result-return, and ordered sequence architecture recited in the claims.” Resp. 41. Patent Owner next argues that Menon is a redesign of Trefethen not an extension, amounts to “an architectural replacement of Trefethen,” and that Petitioner’s combination is governed by hindsight rather than a “combination of prior art elements according to known methods.” *Id.* at 42–43. Patent Owner further contends that Menon identifies “fundamental deficiencies” in the earlier Trefethen architecture that “does not permit extensions via parallel MEX routines.” *Id.* at 43–44 (citing Ex. 1005, 14).

As explained in detail below in subsection II.C.5.c., the Petition establishes by a preponderance of the evidence that, rather than teaching fundamental deficiencies, “Trefethen provides example code describing the sequence of operations that MultiMATLAB’s interconnected nodes perform,” and that Menon-Trefethen teaches what Patent Owner refers to as the “1→2→3→1” order of operations recited in ’034 patent claim limitations [1.4.2], [1.5.2], and [1.6]. Reply 13–15 (citing Ex. 1163 ¶¶ 42–48); *see also* Pet. 21, 39–49 (citing Ex. 1003 ¶¶ 113–115, 202–228; Ex. 1005, 3, 6, FIG. 1; Ex. 1006, 2, 4, 6–7); Resp. 32–35 (referencing “The

Claimed Three-Node Execution Chain” and “Specific 1→2→3→1 Order of Operations”).

Petitioner provides additional testimony from Dr. Bajaj in reply that a POSITA would have been motivated to combine Menon and Trefethen in the manner claimed in the '034 patent:

- Menon suggesting the combination by **expressly citing** Trefethen and explaining that *Menon builds on the teachings of Trefethen*. Ex.1005, 1-2; Petition, 22, Ex.1003, ¶71;
- Menon and Trefethen both describe aspects of how the same MultiMATLAB system enables MATLAB to perform parallel mathematical calculations. Ex.1005, Abstract, 16; Ex.1006, 2; Petition, 22-23; Ex.1003, ¶72; [and]
- Menon and Trefethen together represent a combination of prior art elements according to known methods (executing MATLAB code on a multi-node system) to yield the predictable result discussed in both references: the MultiMATLAB system *executing MATLAB in parallel to perform mathematical calculations*. Ex.1005, Abstract; Ex.1006, 2-7; Petition, 23; Ex.1003, ¶70.

Reply 24–25 (citing Ex. 1163 ¶¶ 70–72) (emphases added). Dr. Bajaj further testifies as follows:

A POSITA would have had an especially strong reason to read these references together *because they address the same project, the same MATLAB-based parallel-computing problem, and the same MultiMATLAB command environment*. Menon expressly identifies Trefethen’s MultiMATLAB work and then describes a redesigned architecture that preserves the same user-level objective—parallel MATLAB computations—while improving implementation details and extensibility.

A POSITA therefore would not view the references as mutually exclusive alternatives. Rather, a POSITA would understand Trefethen as teaching specific MultiMATLAB commands and examples, including Eval, Send, Recv, and the

cycle example, and Menon as teaching *how the MultiMATLAB architecture was implemented and improved in a later version.*

Ex. 1163 ¶¶ 71–72 (emphases added). We find the above reasoning persuasive and adopt it as our own.

Petitioner and Dr. Bajaj demonstrate a sound technical motivation for a POSITA—someone having a bachelor’s degree in computer science, computer engineering, or electrical engineering and two years of experience working in the field of cluster computing or parallel processing—to combine Menon and Trefethen: to improve MATLAB’s operational performance and extensibility in a parallel operating environment. Menon builds on Trefethen to improve and extend the parallel processing capabilities of MultiMATLAB: “This system will enable users to access high-performance parallel routines from within the MATLAB environment, to extend the environment with new parallel routines, and to use these routines to develop parallel applications with the MATLAB language.” Ex. 1005 Abstract. Menon is *intended* to be read in conjunction with Trefethen, as would be expected from two references generated by the same research group at the same university addressed to the same technical subject matter about a year apart. Ex. 1005, 1; Ex. 1006, Ex. 1086 ¶¶ 65, 101, 102. The very first citation in Menon is to Trefethen. Ex. 1005, 2, 16.

In contrast, Patent Owner’s Response and Sur-Reply rely on unsupported attorney argument to assert a lack of motivation to combine references. *See* Resp. 41–48; Sur-Reply 14–18. Patent Owner contends Petitioner’s argument “reduces to the unremarkable proposition that researchers wanted to parallelize high-level mathematical computing environments,” which Patent Owner asserts is an insufficient reason to combine the references because “[m]otivation must be tied to the claimed

configuration, not to an abstract goal.” Resp. 41–42 (citing *KSR*, 550 U.S. at 418). Patent Owner’s argument overlooks Petitioner’s evidence that Menon specifically references, builds on, and expands the teachings of Trefethen—published by the same Cornell research team—to improve MATLAB’s parallel computing performance and extensibility. Moreover, in an obviousness inquiry, there is no requirement that an artisan’s reasons for modifying the prior art be the same as that of the patent applicant. *See In re Kemp*, 97 F. 3d 1427, 1430 (Fed. Cir. 1996) (“Although the motivation to combine here differs from that of the applicant, the motivation in the prior art to combine the references does not have to be identical to that of the applicant to establish obviousness.”) (citing *In re Dillon*, 919 F.2d 688, 693 (Fed. Cir. 1990) (en banc)).

Patent Owner also contends that Petitioner fails to “explain why a POSITA would have selected and implemented the particular multicore, result-return, and ordered sequence architecture recited in the claims.” Resp. 41–42. Patent Owner’s argument, however, is not consistent with the evidence and plain meaning of “*a . . . hardware processor with a plurality of processing cores*” discussed above. Patent Owner’s argument also does not rebut Petitioner’s evidence—particularly Dr. Bajaj’s testimony—supporting a motivation to combine, and the argument is inconsistent with governing case law. Dr. Bajaj explains why Menon-Trefethen teaches the result-return and ordered sequence architecture recited in the claim, further explained in subsection II.C.5.c. below. It is sufficient motivation to establish that “if a technique has been used to improve one device, and a [POSITA] would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.” *KSR*, 550 U.S. at 417. Petitioner has established that Menon-Trefethen

teaches the $1 \rightarrow 2 \rightarrow 3 \rightarrow 1$ and result-return technique claimed in the patent and that such use of that known technique for its intended purpose was not beyond a POSITA's skill.

Patent Owner further contends the asserted combination of prior art references would not yield the claimed system “without additional inventive steps.” Resp. 45. Patent Owner argues, for example, that there is no disclosure of a “*hardware processor*” (as defined by Patent Owner) or a return of evaluation results to the “*first node*” *Id.* at 45–47. Patent Owner’s argument fails for the reasons stated above and as explained in subsection II.C.5.c. below. Consequently, we find the Petition establishes that an ordinarily skilled artisan would have been motivated to combine Menon and Trefethen with a reasonable expectation of success. *See Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1381 (Fed. Cir. 2023) (explaining that it is sufficient for motivation to combine “that there was a known problem . . . in the art, that Bauman[] . . . helped address that issue, and that combining the teachings of Kabemoto and Bauman wasn’t beyond the skill of an ordinary artisan. Nothing more is required to show a motivation to combine under *KSR*”).

Teaching away

“A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.” *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994). Patent Owner argues that Menon teaches away from a combination with Trefethen because “Menon expressly states that Trefethen’s first-generation architecture is inadequate for the objectives that

motivated the newer design.” Resp. 48–50. The evidence does not support Patent Owner’s position.

First, Patent Owner’s teaching away argument is inconsistent with the strong evidence of a motivation to combine Menon and Trefethen discussed above. Second, Patent Owner’s teaching away argument is contrary to the evidence of record for the reasons given in Petitioner’s Reply. Reply 25–27 (e.g., “Menon explicitly cites Trefethen and explains that Menon builds on the teachings of Trefethen.”) (citing Pet. 22–23; Ex. 1003 ¶ 71; Ex. 1005, 1–3; Ex. 1163 ¶¶ 73–77). We are further persuaded by Dr. Bajaj’s reply testimony:

Menon does not “distinguish” the “MultiMATLAB” teachings of Trefethen. Menon explicitly cites Trefethen and explains that Menon builds on the teachings of Trefethen. Menon describes *enhancing* the system of Trefethen. For example, Menon describes a list of “goals” already achieved by MultiMATLAB and then states that the architecture has been “redesigned to achieve two further goals.” One of these two “further goals” is “extensibility.” Menon achieves this extensibility by adding “MEX routines” to the system of Trefethen. The “MEX routines” do not show an “incompatibility” between Menon and Trefethen. Instead, Menon’s addition of the “MEX routines” to MultiMATLAB shows that such a modification was within the capabilities of a POSITA because the authors of the Menon paper actually implemented the modification.

Ex. 1163 ¶ 74 (citing Ex. 1003 ¶ 71; Ex. 1005, 1–3). Dr. Bajaj’s testimony is un rebutted, credible, and supported by the record.

We agree with Dr. Bajaj’s reasoning, which is based on direct quotes in Menon. We further agree with Dr. Bajaj’s conclusion that Menon does not teach away from the combination with Trefethen. *Id.* ¶ 75. Menon’s description of building on and enhancing the teachings of Trefethen—the

earlier work of the same research group at Cornell—by adding MEX routines to achieve high-performance parallel computing and extensibility for MATLAB, demonstrates a classic motivation for a POSITA to combine the teachings of Menon and Trefethen. RS6000 and POEref are specifically referenced in Menon-Trefethen and add operational details of the parallel operating platform that teach a POSITA how to implement the MultiMATLAB system with a reasonable expectation of success. Such facts are inconsistent with Patent Owner’s teaching away and lack of motivation arguments.

For the reasons given above, we determine that Menon, Trefethen, RS6000, and POEref are analogous art in the same field of cluster computing as the ’034 patent. We further determine that Petitioner establishes by a preponderance of the evidence a motivation for a POSITA to combine Menon, Trefethen, RS6000, and POEref with a reasonable expectation of success, and that Menon does not teach away from Trefethen.

c. *The asserted references teach limitations [1.4.2], [1.5.2], and [1.6]*

Limitations [1.4.2], [1.5.2], and [1.6] recite the following:

Limitation [1.4.2]: “*wherein the second node is configured to receive calls from the first node, execute at least a first mathematical expression evaluation, and communicate a result of the first mathematical expression evaluation to a third node;*”

Limitation [1.5.2]: “*wherein the third node is configured to receive the result of the first mathematical expression evaluation from the second node, execute at least a second mathematical expression*

evaluation using the received result, and communicate the result of the second mathematical expression evaluation to the first node;

Limitation [1.6]: *“wherein the first node is configured to return the result of the second mathematical expression evaluation to the user interface.”*

Limitations [1.4.2], [1.5.2], and [1.6] recite data passing operations between nodes. Patent Owner characterizes the claimed data passing operations as the “1→2→3→1 Order of Operations” (or “Three-Node Execution Chain”). Resp. 21–38. Limitation [1.4.2] recites a “*second node*” that “*receives calls from the first node*” (1→2), executes a calculation (“*execute at least a first mathematical expression evaluation*”), and “*communicate[s] a result*” of the calculation “*to a third node*” (2→3). Limitation [1.5.2] recites “*the third node . . . receive[s] the result*” of the calculation executed at the “*second node*,” executes a second calculation (“*execute at least a second mathematical expression evaluation*”), and communicates “*the result of the second mathematical expression evaluation to the first node*” (“3→1”). Limitation [1.6] recites “*the first node is configured to return the result*” of the second calculation received from the third node “*to the user interface*.” Resp. 34–35; Reply 13.

Petitioner contends the Menon-Trefethen combination teaches limitations [1.4.2], [1.5.2], and [1.6], and thus the “1→2→3→1” operation order coined by Patent Owner. Pet. 39–49; Reply 13–16 (citing Ex. 1005, 6, Fig. 1 (annotated); Ex. 1006, 2, 4, 6–7; Ex. 1003 ¶¶ 211–228; Ex. 1163 ¶¶ 42–48). Petitioner first establishes that Menon teaches a MultiMATLAB system with interconnected nodes (a “first node,” “second node,” and “third node”), as shown in annotated Menon Figure 1 reproduced below:

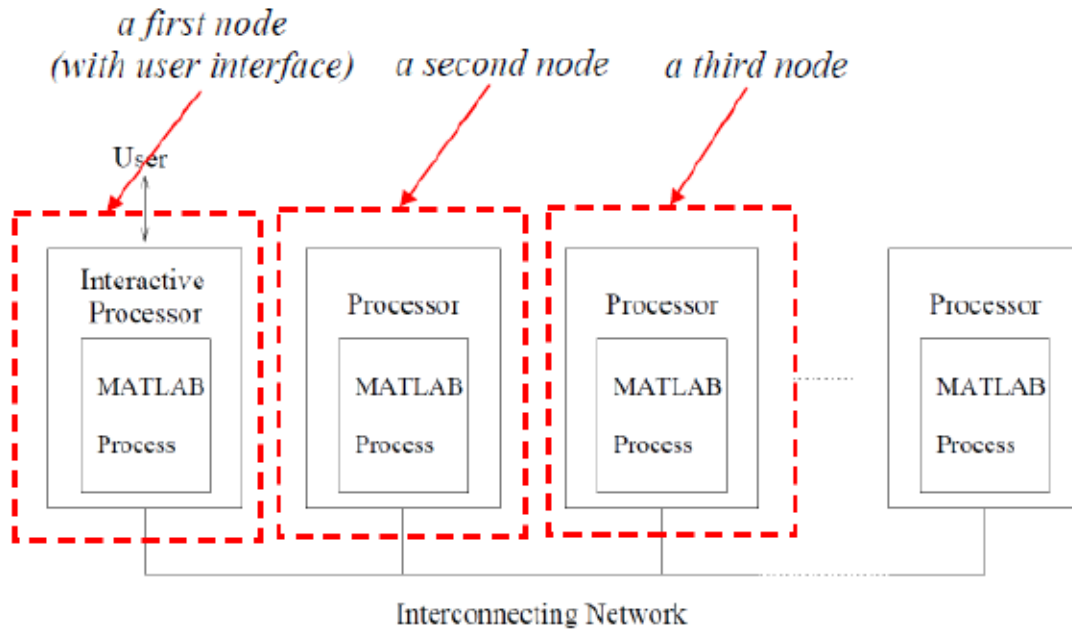


Figure 1: MultiMATLAB Architecture

Reply 14 (citing Ex. 1005, 3, 6, Fig. 1 (annotated)) (also citing Pet. 39–46; Ex. 1003 ¶ 217; Ex. 1163 ¶ 43). The Petition explains that each MATLAB process or “node” is assigned an “identification number” and “wait[s] for commands from the interactive MATLAB process.” Pet. 44 (citing Ex. 1005, 6). The interactive MATLAB process is the first node that interacts with and receives instructions from a user. *Id.*

The Petition then traces exemplary MATLAB user instructions for calling Eval MEX routines to run on a plurality of processors in the interconnecting node system. Pet. 40–41 (citing Ex. 1003 ¶¶ 202–203; Menon Ex. 1005, Abstract, 3, 4; Trefethen Ex. 1006, 4). The Petition specifically traces user instructions for “executing a series of MATLAB processes on 32 IBM SP2 processor nodes.” *Id.* at 41–43 (citing Ex. 1003 ¶¶ 168, 205–210; Ex. 1005, Fig. 1; Ex. 1006, 6 (annotated); Ex. 1007, 2, 9). For example, MATLAB calls an Eval MEX routine to send commands over the interconnecting network (cluster communication layer) to execute single-

threaded processes, such as the “m-file cycle.m” processes for doubling variable a , on a plurality of nodes. *Id.*

Limitations [1.4.2] and [1.5.2]

The Petition explains that Menon teaches MEX routines having code to implement standard variants of MPI (message passing interface) calls to enable point-to-point communication among nodes, which allows MATLAB processes to communicate tasks and data directly with each other. Pet. 44 (citing Ex. 1005, 9). The Petition and Reply explain that Trefethen provides example code for the m-file cycle.m sequence of operations executed by MultiMATLAB’s interconnecting node system:

```
if ID==0           % first process: send
    a = 1
    Send(ID+1,a)
elseif ID == Nproc-1 % last process: receive and double
    a = 2*Recv
else                % middle processes: receive, double, and send
    a = 2*Recv
    Send(ID+1,a)
end;
```

Process 0 creates the variable a with value 1 and sends it to process 1. Process 1 receives the message, doubles the value of a , and sends it along to process 2; and so on. If there are six processors the command Eval('cycle') produces the output

```
a = 1
a = 2
a = 4
a = 8
a = 16
a = 32
```

Pet. 45 (citing Ex. 1003 ¶¶ 211–215; Ex. 1006, 6 (annotated); Reply 14–15 (citing Ex. 1006, 6 (annotated)) (also citing Pet. 38; Ex. 1003 ¶ 190; Ex. 1163 ¶ 44). Petitioner also explains why Menon-Trefethen teaches limitations [1.4.2] and [1.5.2], as follows:

As described above, (i) Process 0 (i.e., the first node) “creates the variable a with a value 1” and sends the variable to process 1 (i.e., the second node), then (ii) process 1 (second node) “receives the message” from the process 0 (first node) and “doubles the value of a ” (now $a=2$), and “sends it along” to process 2 (i.e., the third node) [**limitation 1.4.2**]. Trefethen further describes that each MATLAB process transmits its output

“to the master process” (i.e., the first node) “as soon as it is ready.” **[limitation 1.5.2]**.

Reply 15 (quoting Ex. 1006, 4, 6) (also citing Pet. 21, 47; Ex. 1003 ¶¶ 114, 221) (bold brackets added).

In sum, the Petition contends:

Menon’s teaching of a point-to-point system for passing messages among processors with identification numbers, in view of Trefethen’s disclosure of using point-to-point message passing to send calls from a first processor that are received by a second processor, where the second processor then sends a mathematical result to a third processor, renders obvious this limitation **[1.4.2]**.

Pet. 45 (citing Ex. 1003 ¶¶ 211–215) (bold brackets added). The Petition explains that Trefethen further discloses each MATLAB process transmits its output “to the master process as soon as it is ready.” *Id.* at 47 (citing Ex. 1006, 4). The Petition contends that a “POSITA would recognize Trefethen’s ‘master process’ as Menon’s interactive MATLAB process that provides the output to the user,” i.e., a POSITA would recognize the output is sent “to the interactive MATLAB process (*first node*),” thereby rendering limitation **[1.5.2]** obvious. *Id.* at 47–48 (citing Ex. 1003 ¶¶ 218–225).

Patent Owner’s arguments regarding the “1→2→3→1 order of operations” do not undermine Petitioner’s showing that Menon-Trefethen describes the claimed order as summarized above. The arguments also do not distinguish limitations **[1.4.2]** and **[1.5.2]** from Menon-Trefethen, in part because the arguments imply additional unrecited claim limitations. For example, Patent Owner characterizes the Menon-Trefethen architecture as a “master-controlled dispatch model” in which “a user interacts with an ‘interactive process’” (the first node) “and other processes” (the second and third nodes) “wait for commands from that interactive process.” Resp. 35

(citing Ex. 1005, 3, 6). As Petitioner correctly points out, Patent Owner’s argument overlooks the fact that independent claims 1 and 30 recite “*program code for a first single-node kernel . . . configured to interpret user instructions and distribute calls to at least one of a plurality of other nodes for execution*” (limitation [1.3]), while the other nodes wait to receive calls. Reply 17 (citing Ex. 1001, 29:47–51; 34:33–35; Ex. 1163 ¶¶ 49–51). Thus, we fail to see how Patent Owner’s master-controlled dispatch model argument distinguishes the claim language at issue.

Patent Owner also argues that Trefethen’s script “passes a value from process to process using hardcoded send/receive instructions” and “does not show a first node issuing an evaluation request to a second node.” Resp. 36 (citing Ex. 1001, 29:52–30:4; Ex. 1006, 5–6). First, Patent Owner’s argument acknowledges that Menon-Trefethen passes a computed value, “a=1,” “a=2,” etc. (“*communicates a result*”) from node-to-node. Reply 17–18. Second, Patent Owner fails to explain why or how the claim language in limitation [1.4.2]—“*the second node is configured to receive calls from the first node*”¹⁹—is distinguishable from Menon-Trefethen or otherwise limits the first node to “issuing an evaluation request to a second node.” Resp. 36–37 (citing Ex. 1006, 5–6). Nor does Patent Owner explain why the claim language would exclude “fully scripted” datapassing operations where each node executes “a single programmed routine.” *Id.*; see Reply 17–18 (mapping limitation [1.4.2] and [1.5.2] to Trefethen) (citing Ex. 1163 ¶¶ 52–53).

The ’034 patent specification explains that a kernel “typically includes

¹⁹ Limitation [1.3.2] consistently recites “*the first single-node kernel configured to interpret user instructions and distribute calls to at least one of a plurality of other nodes for execution*”).

program code for interpreting high-level code, commands, and/or instructions supplied by a user or a script into low-level code.” Ex. 1001, 23:1–5; *see* Reply 19 (citing Ex. 1001, 23:1–5). Menon-Trefethen similarly describes MATLAB interpreting program code and instructions supplied by user commands and scripts, and “Patent Owner fails to identify any distinction between ‘user-authored application code’ and the ‘scripts’ as described in the specification, much less the Challenged Claims.” Reply 19 (citing Ex. 1005, 14 (“this MATLAB code”), Ex. 1006, 4–5 (examples of user commands); *see also* Ex. 1006, 5–6 (example “m-file”); Ex. 1016, 4 (m-files are “scripts”); Ex. 1163 ¶¶ 54–55). Dr. Bajaj’s unrebutted testimony further establishes that “[a] POSITA understand[s] that the ‘m-file’ examples in Trefethen are scripts that contain user instructions.” Ex. 1163 ¶ 55.

Arguments disconnected from the specific claim language and relevant description in the ’034 patent specification do not move the needle, particularly when Petitioner provides persuasive rebuttal argument supported by the claim language and specification, citations to Menon-Trefethen, and unrebutted expert opinion testimony from Dr. Bajaj.²⁰ *Compare* Resp. 36–40 *with* Reply 18–22 (citing Ex. 1001, 14:34–35, 16:42–17:10, 23:1–5; Ex. 1003 ¶¶ 211–228; Ex. 1005, 14; Ex. 1006, 4–6; Ex. 1163 ¶¶ 54–63; Pet. 44–49).

Limitations [1.5.2] and [1.6]

Menon discloses that “[t]he user interacts directly with one MATLAB process, called the interactive process,” i.e., the claimed “*first node*.” Ex.

²⁰ Patent Owner did not depose Dr. Bajaj or submit a supplemental declaration of Dr. Smith with its Response.

1005, 3; *see* Pet. 40, 48 (citing Ex. 1005, 3). As previously stated, Trefethen discloses that each MATLAB process executes a calculation and transmits the output “to the master process as soon as it is ready.” Ex. 1006, 4; *see* Pet. 47 (quoting Ex. 1006, 4) (citing Ex. 1003 ¶¶ 221). Trefethen clarifies that MATLAB “send[s] screen output to the master process,” in other words computed results are “sent to the user’s screen . . . when one wishes to monitor the progress of computations on several processors graphically.” Ex. 1006, 5, 7; *see* Pet. 47–49 (quoting Ex. 1006, 7). The Petition contends that when the MATLAB process at processor ID=2 (“*the third node*”) doubles variable “*a*” it has received from processor ID=1 (“*the second node*”), the MATLAB process sends output result “*a=4*” to the interactive processor (“*the first node*”) for display on the user’s screen (“*the first node is configured to return the result of the second mathematical expression evaluation to the user interface*”), thus teaching limitations [1.5.2] and [1.6]. Pet. 48–49 (citing Ex. 1003 ¶¶ 226–228; Ex. 1005, 3; Ex. 1006, 7); *see also* Pet. at 46 (identifying first, second, and third nodes in MultiMATLAB architecture) (citing Ex. 1003 ¶ 177; Ex. 1005, Fig. 1 (annotated)); Reply 15–16 (citing Ex. 1006, 6–7; Ex. 1163 ¶¶ 44–48).

We agree with Petitioner that Menon-Trefethen teaches “sending the output, when ready, to the interactive MATLAB process (*first node*)” in accordance with limitation [1.5.2] because, as explained by Dr. Bajaj:

A POSITA would recognize that the “master process” described by Trefethen would be the interactive process of Menon, because the interactive process is the MATLAB process in the MultiMATLAB architecture with which the user interacts. As a specific example, as soon as the MATLAB process at processor ID=2 completes the operation of doubling the variable that it has received from processor ID=1, the MATLAB process uses that processor ID=2 (*third node*) to send (*communicate*) the variable

that it has received and then doubled (*the result of the second mathematical expression evaluation*) to the interactive processor (*to the first node*).

Ex. 1003 ¶ 221 (citing Ex. 1005, 3; Ex. 1011, 23²¹); Pet. 47–48 (citing Ex. 1003 ¶ 221); Reply 22 (citing Pet. 46–49; Ex. 1003 ¶¶ 218–228; Ex. 1163 ¶¶ 62–63). Dr. Bajaj further explains a “master process” is a “pseudo-master [that] is arbitrarily chosen to be the task [that] all the peers know a priori who to send the results back to.” Ex. 1003 ¶ 221 n.3 (citing Ex. 1011, 23). In the context of Menon-Trefethen, “the ‘master’ process is the process with which the user is directly interacting in a peer-to-peer paradigm, and not a ‘master’ in a master/slave paradigm.” *Id.*

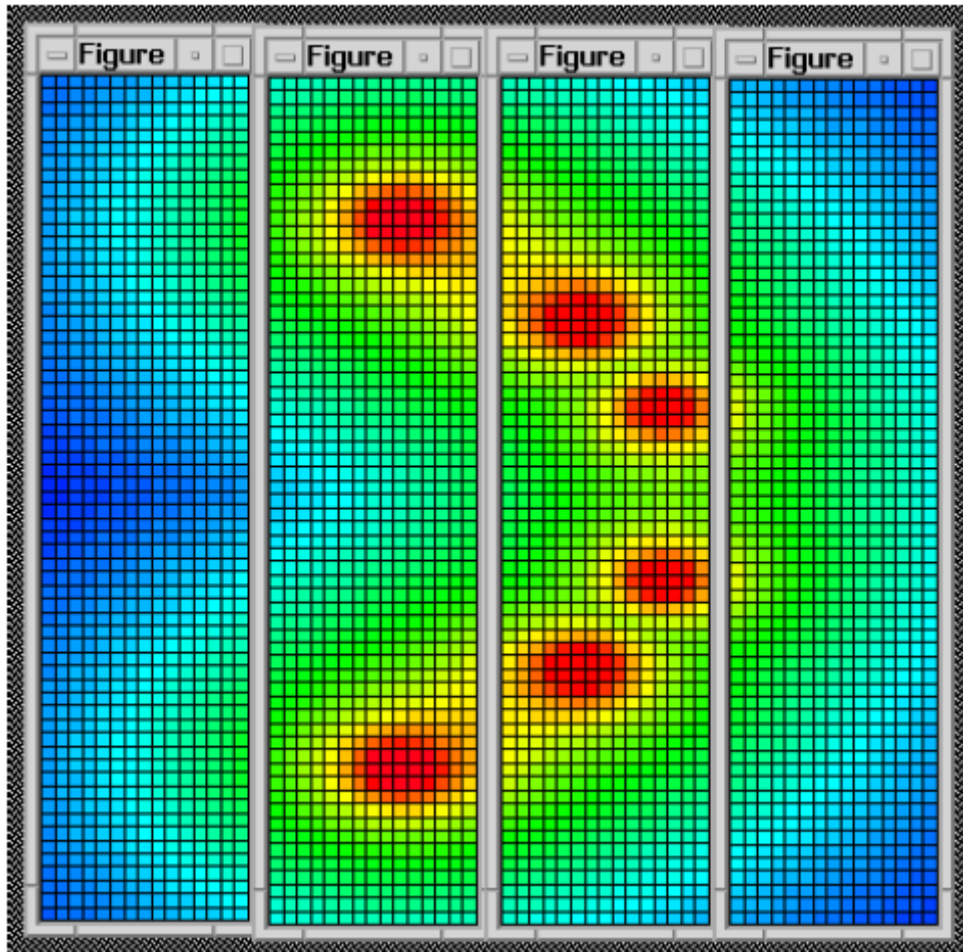
Dr. Baja also explains why Menon-Trefethen teaches limitation [1.6]:

Menon discloses that “[t]he user interacts directly with one MATLAB process, called the interactive process, and operates within that process’s MATLAB environment.” An example of said interaction is taught by Trefethen, which teaches “produc[ing] plots in a distributed fashion that are then *sent to the user’s screen*. This can be particularly useful when one wishes to *monitor the progress of computations on several processors graphically*.” In particular, Trefethen teaches “set[ting] up a MATLAB figure window in each process and arrang[ing] them in a grid on the screen. This is easily done using standard MATLAB handle graphics commands.” In other words, “*the progress of computations on several processors,*” such as the results of computations performed by the processors of the MultiMATLAB architecture and *returned to the interactive processor, are presented to the user at the user’s screen*.

Ex. 1003 ¶ 227 (emphases added) (quoting Ex. 1005, 3; Ex. 1006, 7); *see* Pet. 48–49. We find Dr. Bajaj’s testimony compelling; Dr. Bajaj explains

²¹ We cite the exhibit page number rather than the internal document page number of Ex. 1011.

quoted disclosures in Menon and Trefethen from the perspective of a POSITA. Trefethen even provides a graphic example of a “4 by 1 grid of windows” that displays computational output—“computed . . . pseudospectra” of a “Grcar matrix”—to a user:



Ex. 1006, 7–8. We find Dr. Bajaj’s testimony quoted above to be persuasive and consistent with the disclosures in Menon-Trefethen.

Patent Owner argues: “the prior art references do not disclose any return mechanism that delivers *computed values* from one node to another *for further use*, let alone through the claimed path back to the user interface.” Resp. 22–23 (emphases added). Patent Owner contends that Trefethen’s disclosure of sending computational outputs to the user’s screen

(“screen output”) does not satisfy limitations [1.5.2] and [1.6] because there is no disclosure of “any mechanism by which the value computed on a remote node is returned to the originating process as data for further use.” *Id.* at 23–24. Patent Owner’s argument devolves to the proposition that Trefethen’s return of “screen output” is not “data” or a “computed value.” *Id.* at 26 (“Trefethen is explicit that, as described, the system does not return data values from a remote process to the master in response to Eval().”); *see* Tr. 53:4–20 (Q: “So your whole distinction is that screen output is not data?” A: “Correct.”).

The disclosures in Trefethen, in view of Dr. Bajaj’s unrebutted testimony, do not support Patent Owner’s argument. Trefethen teaches that “in keeping with our orientation toward SPMD programming, each command passed to Eval was executed on all MATLAB processes” and “output is sent to the master process as soon as it is ready.” Ex. 1006, 4. As counsel for Petitioner explained at the oral hearing:

And so we have a command in the SPMD programming language described in Trefethen where you can actually send something directly to another node. It's not just the send and receive. Eval also lets you do this. Eval also lets you target a particular node. So we have that teaching within Trefethen as well. That's how you can send tasks and commands between different nodes.

Tr. 67:21–68:2 (referencing Ex. 1006, 4). Counsel’s explanation is further supported by unrebutted testimony from Dr. Bajaj:

Trefethen discloses that a user “connected to a node of the IBM SP2, running MATLAB,” in a MultiMATLAB architecture that includes additional MATLAB processes, *can execute on all the MATLAB processes using Eval, “[t]he standard MultiMATLAB command for executing commands on one or more processors.*” That is, “[e]ach command passed to Eval was executed on all MATLAB processes.” The outputs from the

MATLAB processes are “sent to the master process as soon as it is ready,” i.e., *without order or synchronicity between the MATLAB processes*. In the context of SPMD point-to-point communication, a “master process” is a “pseudo-master [that] is arbitrarily chosen to be the task [that] all the peers know a priori who to send the results back to.”

Trefethen also *discloses peer-to-peer communication*, in that “[m]ore general point-to-point communication is *accomplished by send and receive commands*, which can be executed on any of the MATLAB processes.” For example, “SPMD programs can be built upon Send and Recv commands.”

Ex. 1003 ¶¶ 113–114 (citing Ex. 1006, 3–5; Ex. 1011, 23) (emphases added); *see also id.* at ¶¶ 45–47, 115, 220–221, 227; Ex. 1163 ¶¶ 62–69. In short, Trefethen discloses and teaches a mechanism for communicating a result of a mathematical computation at each node directly to the pseudo-master interactive process node (“*first node*”) in a peer-to-peer architecture, e.g. by executing the example script (m-file) “cycle.m” and SPMD program commands on MultiMATLAB.

Patent Owner further contends that:

1. In Trefethen “data movement is handled by separate commands, not by Eval () returning values” (Resp. 27 (citing Ex. 1006, 5));
2. In Trefethen “*numeric values are displayed*; they are not returned into the master’s workspace as usable variables” (emphasis added) (Resp. 27–28);
3. “If the system were designed to return evaluated results as data, one would expect a Get operation or an assignment of the

received value into a variable that is then transmitted back.

Trefethen does not show that.”²² (Resp. 28);

4. “Menon is silent about any return value, feedback channel, or mechanism for capturing the result of a remote evaluation in the initiating process’s environment.” (Resp. 29); and
5. Dr. Bajaj’s Declaration testimony that reads Menon-Trefethen onto limitations [1.5.2] and [1.6] is “not supported by disclosure in the references and contradict[s] Trefethen’s express statements about what was communicated . . . and about master-only data transfer.” (Resp. 31–32) (citing Ex. 1003 ¶ 221; Ex. 1006, 6) (*see also* Resp. 38–40, 53–57; Sur-Reply 17–18).

We disagree.

One problem with Patent Owner’s argument is that the claims recite the communication of a “*result*” to the first node, not “data” or a “value.” As Petitioner correctly notes, the challenged claims “recite no requirement that the ‘*result of the mathematical expression evaluation*’ communicated by the third node to the first node must be ‘data’ as Patent Owner argues.” Reply 23. Patent Owner acknowledges that “numeric values are displayed” to the user in Trefethen’s system, and the user interfaces with the interactive processor (“*first node*”). Resp. 27–28; *see also* Ex. 1006, Abstract (MultiMATLAB uses “Eval, Send, [and] Recv” to “pass commands and data between [] these various [MATLAB] processes.”). Patent Owner, moreover, references specific operational mechanisms (Send, Recv, and Get commands)

²² Patent Owner’s argument crosses the line into providing expert opinion testimony without citing any expert testimony in support. *See also, e.g.* Resp. 27–28 (“Get . . . commands would be superfluous if Eval () automatically returned computed values.”).

in Trefethen without explaining why such mechanisms would be excluded by the claims, and without addressing Petitioner’s contentions directed to the specific claim language. *Compare* Resp. 27–28 *with* Reply 23–24 (citing Ex. 1163 ¶¶ 66–69 (“Nor does the claim language require any particular ‘mechanism’ for the communication of the claimed result that would exclude communicating screen output”). Patent Owner’s argument is not supported by expert testimony, and Dr. Bajaj’s Declaration testimony regarding limitations [1.4.2], [1.5.2], and [1.6] (Ex. 1003 ¶¶ 45–47, 113–115, 211–228; Ex. 1163 ¶¶ 62–69) is credible, consistent, and uncontested.

Patent Owner’s further argument, that Dr. Bajaj’s expert opinion regarding Menon-Trefethen’s disclosure of sending screen output to the user’s screen amounts to unsupported “gap-filling,” rings hollow. Resp. 31–32 (citing Ex. 1003 ¶ 221). “[E]xtrinsic evidence may be considered when it is used to explain, but not expand, the meaning of a reference.” *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991) (citing *Scripps Clinic & Research Foundation v. Genentech, Inc.*, 927 F.2d 1565, 1576–77 (Fed. Cir. 1991)). Dr. Bajaj has done precisely that; he explains what a POSITA would know from reading Menon and Trefethen, nothing more. There is no gap-filling as asserted by Patent Owner. *See* Resp. 32–33 (“reliance on expert assertion to bridge the gap is legally insufficient”), 38–40 (“gap is not plainly filled” by prior art; “gap-filling the Federal Circuit and the Board do not permit”); Sur-Reply 17–18 (*KSR* “does not authorize the Board to fill an evidentiary gap with hindsight”).

Nor does Patent Owner address or rebut the documentary evidence corroborating Dr. Bajaj’s opinion testimony that a POSITA would know the master process that receives computed results from the other nodes in Menon-Trefethen’s peer-to-peer cluster system—“the task with rank

MASTERID, all the peers know a prior who to send the results back to”—is the interactive process (“*first node*”). Ex. 1003 ¶ 221 (citing Ex. 1011, 23²³); *see also id.* ¶¶ 45, 114 (explaining peer-to-peer communication in the MultiMATLAB architecture). Patent Owner criticizes Dr. Bajaj’s testimony but relies solely on attorney argument to contend the claimed “*peer-to-peer architecture*” (limitation [1.2]) as construed by Petitioner is not taught by Menon-Trefethen, which allegedly operates by “routing every node’s output through a central master.” Sur-Reply 12²⁴; *see also* Resp. 53–54 (“Dr. Bajaj repeatedly supplies critical claim elements by mere unsupported assertion.”). Such argument is devoid of supporting evidence and fails to undermine Petitioner’s showing. Moreover, as explained above, in Menon-Trefethen “the ‘master’ process is the process with which the user is directly interacting in a peer-to-peer paradigm, and not a ‘master’ in a master/slave paradigm.” Ex. 1003 ¶ 221 n.3 (citing Ex. 1011, 23).

We are bound to follow the Supreme Court’s guidance on the question of obviousness:

Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; *and the background knowledge possessed by a person having ordinary skill in the art*, all in order to determine whether there was an

²³ The quote is from a textbook titled “High Performance Cluster Computing Vol. 2,” published in 1999 by Prentice Hall, Inc. Ex. 1011, 1–3.

²⁴ Patent Owner’s Response did not address the construction of “*peer-to-peer architecture*,” and the argument should have been raised in the Response rather than for the first time in Patent Owner’s Sur-Reply. *See Apple Inc. v. e-Watch, Inc.*, IPR2015-00412, Paper 50, 44 (PTAB May 6, 2016) (“‘Respond,’ in the context of 37 C.F.R. § 42.23(b), does not mean embark in a new direction with a new approach”).

apparent reason to combine the known elements in the fashion claimed by the patent at issue.

KSR, 550 U.S. at 418 (emphasis added). Dr. Bajaj illuminates interrelated teachings of the peer-to-peer MultiMATLAB cluster computing system taught by Menon-Trefethen from the perspective of a POSITA. Dr. Bajaj provides specific citations to the references, corroborating documentary evidence, and technical explanations that relate features of the MultiMATLAB system to the actual claim language, particularly the SPMD program commands and MEX routine data passing operations taught by Menon-Trefethen.

As for Patent Owner’s argument that the claims require the computed value to be returned “to the originating process as data for further use” (Resp. 24), Dr. Bajaj explains that “the first node *does* put the result to ‘further use’ after receiving the result: the first node displays the result on the screen for the user to review.” Ex. 1163 ¶ 64. Even so, as Petitioner correctly points out, “the claims contain no such language requiring any ‘further use’ after the result is received by the first node.” Reply 23 (citing Ex. 1163 ¶ 65). We agree.²⁵

In sum, we determine Menon-Trefethen teaches that the first node (interactive process) receives the result from the third node (non-interactive process, e.g. “a=4”) and displays the result as screen output via the user interface in accordance with limitations [1.5.2] (“*third node is configured to . . . communicate the result of the second mathematical expression*

²⁵ Patent Owner’s argument, that Menon-Trefethen does not teach “two distinct mathematical expression evaluations executed at two different nodes” (Resp. 37), is similarly unavailing for the reasons set forth in Petitioner’s Reply. Reply 20–21.

evaluation to the first node”) and [1.6] (“*wherein the first node is configured to return the result . . . to the user interface*”). See Reply 22–24 (citing, *inter alia*, Ex. 1163 ¶¶ 62–69). Nothing more is required.

6. Conclusion for Ground 1

For the reasons given above, we determine the Petition establishes by a preponderance of the evidence that the combination of Menon, Trefethen, RS6000, and POEref renders obvious claims 1–25, 27–28, and 30.

D. Asserted Obviousness of Claims 26 and 29

Ground 2 of the Petition adds MPIref (Ex. 1017) to Menon, Trefethen, RS6000, and POEref to contend that claims 26 and 29 of the ’034 patent are obvious. Pet. 87–94 (citing, *inter alia*, Ex. 1003 ¶¶ 85, 126–128, 467–544; Ex. 1017, ii–iii, 1–2, 15–21, 40). Patent Owner relies on the arguments addressed to the independent claims, discussed in sections II.A.–C. above and II.E. below, for its assertion that Petitioner has not established the obviousness of dependent claims 26 and 29 by a preponderance of the evidence. See Resp. 3–6 (“This case turns on a small number of dispositive issues that run through every instituted ground and every challenged independent claim.”). Having considered the arguments and evidence in the Petition, Patent Owner’s Response, Reply, and Sur-Reply addressed to claims 26 and 29, we determine the Petition establishes by a preponderance of the evidence that the combination of Menon, Trefethen, RS6000, POEref, and MPIref discloses, teaches, suggests, or otherwise renders obvious independent claims 26 and 29.

E. Petitioner Has Demonstrated that Exhibits 1005–1008 and 1017 Qualify As Printed Publications

The Federal Circuit instructs that “[t]o qualify as a printed publication, a reference ‘must have been sufficiently accessible to the public

interested in the art.” *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1348 (Fed. Cir. 2016) (citing *In re Cronyn*, 890 F. 3d 1158, 1160 (Fed. Cir. 1989)). “A reference will be considered publicly accessible if it was ‘disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it.” *Id.* (citing *Kyocera Wireless Corp. v. Int’l Trade Comm’n*, 545 F.3d 1340, 1350 (Fed. Cir. 2008)). The question of whether a document qualifies as a “printed publication” for the purposes of 35 U.S.C. § 102 “involves a case-by-case inquiry into the facts and circumstances surrounding the reference’s disclosure to members of the public.” *Medtronic, Inc. v. Barry*, 891 F.3d 1368, 1380 (Fed. Cir. 2018) (citing *In re Klopfenstein*, 380 F.3d 1345, 1350 (Fed. Cir. 2004)).

We discuss below the parties’ arguments and evidence addressing the facts and circumstances surrounding the publication of the asserted references.

1. Overview of the evidence and arguments

The Petition provides substantial supporting evidence that Menon, Trefethen, RS6000, POEref, and MPIref were publicly accessible to a POSITA exercising reasonable diligence prior to June 13, 2006, the earliest possible priority date for the ’034 patent. Pet. 11, 14–16; Reply 27–34.

Patent Owner argues that Petitioner has failed to prove public accessibility and “none of its references qualifies as prior art.” Resp. 58–59. As one example, Patent Owner contends “Petitioner provides no evidence that a POSITA using typical search methods at the time could have located” RS6000 and POEref (Exs. 1007–1008). *Id.* at 59. Patent Owner’s argument directed to the two IBM manuals asserts that Petitioner has not shown “link chains” or a web page that would allow “users to search for [the references]

by topic.” *Id.* Patent Owner similarly argues that “Petitioner offers no evidence that anyone outside the MPI Forum ever knew of or accessed the draft [MPIref].” Resp. 61. The evidence of record strongly supports Petitioner.

The publication evidence submitted with the Petition includes five declarations in support.²⁶ Bajaj Declaration Ex. 1003 ¶¶ 110–112 (Menon), 116–117 (Trefethen), 119–120 (RS6000), 123–125 (POEref), and 129–130 (MPIref); Ex. 1027 (IEEE Declaration); Ex. 1029 (Internet Archive Declaration); Ex. 1047 (IBM Declaration); Ex. 1048 (Internet Archive Declaration); Ex. 1049 (exhibits to Ex. 1048). The IEEE Declaration of Gordon MacPherson (Ex. 1027) is directed to the publication of the Menon reference. The Internet Archive Declaration of Mina Ching (Ex. 1029) is directed to establishing the date of archived website URLs for accessing Menon, Trefethen, RS6000, POEref, and MPIref. The IBM Declaration of Carol Edwards (Ex. 1047) is directed to the publication of POEref. The Internet Archive Declaration of Tanya Zeif (Ex. 1048) is directed to establishing the date of archived website URLs for accessing MPIref (June 24, 1997 (Ex. 1049, 11)) and “Mathworks,” which provides a detailed discussion of MATLAB (March 31, 2004 (Ex. 1049, 248)). *See also* Ex. 1003 ¶¶ 129, 130 (“Menon, while citing to MPIref, provided a website address of Argonne National Laboratory (<http://www.mcs.anl.gov/mpi>) for retrieving MPIref.”) (citing Ex. 1005, 16).

Patent Owner’s arguments, summarized above, do not undermine Petitioner’s evidence, which is specific, consistent, and persuasive in

²⁶ Patent Owner did not depose any of Petitioner’s declarants or submit rebuttal declarations with its Response.

establishing public accessibility of the references prior to June 13, 2006. Petitioner is not required to prove a searchable link chain as argued by Patent Owner. Resp. 59–62; Sur-Reply 19, 22–25; *see Medtronic*, 891 F.3d at 1380 (“Because there are many ways in which a reference may be disseminated to the interested public, ‘public accessibility’ has been called the touchstone in determining whether a reference constitutes a ‘printed publication’ bar under 35 U.S.C. § 102(b).”) (citing *Blue Calypso*, 815 F.3d at 1348). Petitioner’s burden is to establish by a preponderance of the evidence that each reference was publicly accessible to a POSITA exercising reasonable diligence prior to June 13, 2006. *Id.* We find Petitioner has satisfied that burden.

Petitioner’s Reply is supported by the comprehensive expert librarian Declaration of Dr. Ingrid Hsieh-Yee. Ex. 1086; Ex. 1087 (Curriculum Vitae). Patent Owner objects to Petitioner’s reliance on Dr. Hsieh-Yee’s Declaration in Reply as advancing “new theories” of public accessibility. Sur-Reply 19 (“Petitioner has added new theories”). Patent Owner further contends that Reply evidence “may corroborate” a showing of public accessibility but “may not establish a public-access channel the Petition never identified.” *Id.* (citing *VidStream LLC v. Twitter, Inc.*, 981 F.3d 1060, 1064-67 (Fed. Cir. 2020)). We are not persuaded.

In *VidStream*, the Federal Circuit rejected a very similar argument that “the Board violated its own rules in considering evidence that was not provided with the IPR petitions, but only with the replies,” and that by relying on reply evidence the Board “departed from the specific grounds of unpatentability set forth in the petitions and thus exceeded its statutory authority.” *VidStream*, 981 F.3d at 1064, 1066. The Federal Circuit found nothing wrong with the Board’s reliance on a declaration of Dr. Hsieh-Yee

submitted with petitioner’s reply brief in the *VidStream* case, which cited Machine-Readable Cataloging (“MARC”) records of the type Petitioner relies on here to establish the date a reference was cataloged in a public library. *Id.* at 1063, 1066–1067; *see, e.g.*, Reply 29 (“MARC records” (Ex. 1091) “showing Menon was cataloged in the Academia Sinica Library on ‘December 14, 1998’” (citing Ex. 1086 ¶¶ 37–43)), 30 (“MARC records” (Ex. 1101) showing that Trefethen was cataloged by “Washington State University Library” on “November 3, 1997” (citing Ex. 1086 ¶¶ 79–85)). The *VidStream* court found “the Board acted appropriately, for the Board permitted both sides to provide evidence concerning the reference date of the [prior art] in pursuit of the correct answer.” *VidStream*, 981 F.3d at 1065. We have followed the same course here.

In short, *VidStream* fully supports the Board’s reliance on additional evidence of public accessibility submitted in support of Petitioner’s Reply, including Dr. Hsieh-Yee’s expert librarian Declaration.

Petitioner’s Reply evidence and arguments, moreover, do not constitute new theories, and the Board may consider such reply arguments and evidence when deciding the question of public accessibility. *See Rembrandt Diagnostics, LP v. Alere, Inc.*, 76 F.4th 1376, 1384–1385 (Fed. Cir. 2023) (reply argument not improper if it “simply expands on previously raised arguments” or “is offered ‘to explain, repel, counteract, or disprove the evidence of the adverse party’”) (citations omitted). Petitioner’s Reply and Dr. Hsieh-Yee’s Declaration are direct rebuttal to Patent Owner’s arguments. We are unmoved by Patent Owner’s new theories argument.

For example, Petitioner replies to Patent Owner’s argument that “Petitioner has not proven that the SC’97 conference proceedings (including Menon) were actually disseminated to the public in 1997” (Resp. 63–64), by

arguing “Menon qualifies as a printed publication because it was published and distributed at the Proceedings of the 1997 ACM/IEEE Conference on Supercomputing 1997.” Reply 27 (citing Ex. 1005; Ex. 1026; Ex. 1027). Petitioner further supports the argument with evidence of Menon being catalogued, indexed, and actually referenced in publications dated 1998, 1999, and 2000. *Id.* at 28–29 (citing, *inter alia*, Ex. 1086 ¶¶ 28–70). Petitioner’s Reply expands on its Petition argument by citing Dr. Hsieh-Yee’s Declaration to establish that “Menon was sufficiently disseminated and was located by POSITAs” who cited Menon in articles published prior to June 13, 2006. *Id.* at 27–28 (citing Ex. 1086 ¶¶ 54–63; Ex. 1094, 16 (note 14); Ex. 1095, 19 (note 2)²⁷; Ex. 1096, 14 (note 17); Ex. 1097, 72).

Patent Owner’s Sur-Reply does not challenge the facts established in Dr. Hsieh-Yee’s Declaration with any cross-examination testimony of Dr. Hsieh-Yee. Sur-Reply at 18–21. Nor does Patent Owner cite inconsistent documentary evidence of record. *Id.*; *see also id.* at 20 (acknowledging that “Internet Archive captures of Menon (Ex. 1092) corroborate the same kind of evidence the Petition already relied on (Ex. 1029)”). Patent Owner’s position appears to be that Petitioner is not permitted to rebut Patent Owner’s arguments with evidence submitted in reply; a position that is unfounded. We find that Dr. Hsieh-Yee’s expert librarian declaration is reliable and persuasive rebuttal testimony corroborated by documentary evidence of publication dates for each asserted reference prior to the June 13, 2006 priority date of the ’034 patent.

²⁷ We cite the exhibit page number rather than the internal page number of the document.

In sum, we find Petitioner did not add new theories of public accessibility in its Reply, but rather responded properly to Patent Owner’s arguments by introducing rebuttal evidence that each prior art reference at issue was publicly accessible to a POSITA exercising reasonable diligence before June 13, 2006, and therefore qualifies as a prior art printed publication pursuant to 35 U.S.C. § 102.

Patent Owner also challenges the admissibility of the Petition’s publication evidence regarding all asserted prior art references and expresses an intent to “address those issues in a forthcoming motion to exclude.” Resp. 66. As we noted in our Decision to Institute, “[t]he Board’s practice is to rule on motions to exclude evidence under the procedures set forth in 37 C.F.R. § 42.64.” DI 43 n.13. Motions to exclude were due July 23, 2026, but none were filed. Paper 17, 13. Accordingly, Patent Owner has waived its right to challenge the admissibility of Petitioner’s evidence. 37 C.F.R. § 42.64(c) (“A motion to exclude evidence must be filed to preserve any objection.”).

We address specific publication evidence for each reference and additional Patent Owner arguments below.

2. Menon (Ex. 1005)

The Petition contends that Menon “is a paper authored by Vijay Menon and Anne Trefethen of the Cornell research team” and “qualifies as a printed publication because it was published and distributed at the Proceedings of the 1997 ACM/IEEE Conference on Supercomputing 1997 [SC ’97].” Pet. 14 (citing Ex. 1005; Ex. 1026; Ex. 1027). The Petition also contends that Menon was “published and distributed on Cornell’s website at least as early as 2001.” *Id.* (citing Ex. 1023; Ex. 1029). The Petition further contends that “Menon was reasonably located by POSITAs because it had

been cited 17 times in papers prior to the priority date of the '034 patent.”
Id. (citing Ex. 1003 ¶¶ 121–123; Ex. 1028, 4–9; Ex. 1029, 1–3).

The Declaration of Gordon MacPherson, Director, Board Governance & Policy Development at The Institute of Electrical and Electronics Engineers, Inc. (“IEEE”), establishes that Menon was publicly accessible to attendees of the IEEE SC '97 conference in November 1997. Mr. MacPherson testifies as follows:

7. It is the regular practice of IEEE to publish articles and other writings including article abstracts and make them available to the public through IEEE Xplore. IEEE maintains copies of publications in the ordinary course of its regularly conducted activities.

8. The [Menon] article below has been attached as Exhibit A to this declaration:

9. I obtained a copy of Exhibit A through IEEE Xplore, where it is maintained in the ordinary course of IEEE’s business. Exhibit A is a true and correct copy of the Exhibit as it existed on or about March 4, 2025.

10. The article and abstract from IEEE Xplore show the date of publication. IEEE Xplore populates this information using the metadata associated with the publication.

11. [Menon] was published in SC '97: Proceedings of the 1997 ACM/IEEE Conference on Supercomputing, held on November 15–21, 1997, in San Jose, CA, USA. *Copies of the conference proceedings were made available no later than the last day of [the] conference.* . . .

Ex. 1027, 1–2 (emphasis added).

Patent Owner’s argument, that Petitioner has not proved Menon was “actually disseminated to the public in 1997” and Exhibit A to the MacPherson Declaration is “uncorroborated” by IEEE Xplore and “does not display any publication date for Menon,” is unavailing. Resp. 63–64. Mr.

MacPherson’s un rebutted testimony is clear and specific: “[c]opies of the [SC ’97] conference proceedings were made available no later than the last day of conference,” i.e., no later than November 21, 1997. Ex. 1027 ¶ 11. Mr. MacPherson’s testimony is at least partially corroborated by the formal copyright notice and International Standard Book Number (“ISBN”) assigned to Menon and printed in the footer at the bottom of all 18 pages of Menon:

Proceedings of the ACM/IEEE SC97 Conference (SC’97)
0-89791-985-8/97 \$ 17.00 © 1997 IEEE

Ex. 1027, 4–21; *see also* Ex. 1005. We note the 1997 copyright date for the SC ’97 proceedings, which is consistent with the last three digits of the ISBN—“8/97”—indicating a date of August 1997.

Even so, there is little doubt that Menon was publicly available before the June 13, 2006 priority date of the ’034 patent, the legally relevant consideration here, given Dr. Hsieh-Yee’s authoritative and un rebutted testimony:

The ACM metadata record shows Menon was published on November 15, 1997. . . . [L]ibrary records inform my opinion that the conference proceedings containing Menon became publicly discoverable and accessible in libraries no later than December 1998. . . .

Public access to the conference proceedings containing *Menon* was actually earlier than July 1998. The General Information webpage of the SC’97 conference website, archived on February 26, 1998 (Ex. 1093), informed users that the conference proceedings [were] available online, and *interested users could use workstations at the conference to view the conference proceedings during the November 1997 conference. These dates inform my opinion that the SC’97 conference proceedings containing Menon was publicly accessible as early as November 1997, and no later than February 1998* when the

webpage was archived by Internet Archive. Copies of the conference main page, table of contents, technical papers, and abstracts of technical papers archived in April 1998 (included in **Ex. 1093**), confirm that *Menon* was included in the SC'97 conference, and the conference proceedings [were] publicly discoverable on the Internet no later than April 1998.

Ex. 1086 ¶¶ 65, 67 (emphasis added); *see also id.* at ¶¶ 28–70 (establishing authenticity and public availability of Menon).

The Internet Archive Affidavit of Mina Ching further supports Petitioner's contention that Menon was publicly available on the Cornell website prior to June 13, 2006. Ex. 1029. The Affidavit states that the copy of Menon attached as Exhibit A is a “true and accurate cop[y] of browser screenshots . . . of the archived files for the URLs and the dates specified in the attached coversheet of each screen shot.” *Id.* ¶ 6. The dates shown on Exhibit A to the Affidavit indicate that Menon was available on the Cornell website no later than November 18, 2003. *Id.* Ex. A at 5–10. Patent Owner's argument, that “Petitioner offers no evidence that the Menon PDF was indexed or that anyone actually located it on Cornell's site within the relevant timeframe” (Resp. 65), does not undermine the Petition's contention of public accessibility, at least to the extent each archived link was accessible before June 13, 2006.²⁸ *See also* Ex. 1003 ¶ 110 (Menon “has been cited 17 times in papers with online publication dates between the

²⁸ For example, the link on page 5 of Exhibit 1028 leads to an article dated March 15, 2006 that cites Menon in footnote 19. Ex. 1028, 5 (Karpievitch Y and Almeida J. (2006). “*mGrid: A load-balanced distributed computing environment for the remote execution of the user-defined Matlab code.*” BMC Bioinformatics. 10.1186/1471-2105-7-139. 7:1. Online publication date: 15-Mar-2006, available at <https://doi.org/10.1186/1471-2105-7-139>). The earliest citation to Menon is July 1, 1998. *Id.* at 7 (FN 5 in linked article).

original publication of Menon and the earliest priority date of the '034 patent.” (citing Ex. 1028, 4–9)). We find the Internet Archive Affidavit of Mina Ching and the Declaration of Dr. Bajaj provide persuasive support for Petitioner’s argument.

For the reasons given above, we determine Petitioner has established by a preponderance of the evidence that Menon was publicly accessible before June 13, 2006 and qualifies as a prior art printed publication under 35 U.S.C. § 102.

3. Trefethen (Ex. 1006)

The Petition contends that Trefethen “qualifies as a printed publication because it was published and distributed on the webpage of one of its authors at least as early as 2001” and “was also published on a Cornell University website no later than May 10, 1996.” Pet. 14–15 (citing Ex. 1023; Ex. 1029). The Petition also contends that Trefethen was “reasonably located by POSITAs because it had been cited 10 times in papers prior to the priority date of the '034 patent.” *Id.* at 15 (citing Ex. 1003 ¶¶ 116–117; Ex. 1035, 2–3). The Petition further contends that a “POSITA seeking to understand MultiMATLAB’s capabilities would have consulted the Cornell website dedicated to MultiMATLAB, which contained links to [Trefethen and Menon].” *Id.* at 23 (citing Ex. 1003 ¶ 72; Ex. 1023).

Patent Owner responds that “Petitioner offers no competent evidence that such a hyperlink existed or that anyone actually found the page in the 1990s.” Resp. 61–62 (citing Ex. 1023). Patent Owner also argues that “[t]he record contains no proof of indexing, public discoverability, or that the site was accessed by any member of the public,” such that “one would have needed to know the exact URL to load the page – which is not public accessibility unless that URL was advertised or indexed somewhere.” *Id.* at

62 (citing Ex. 1029). Patent Owner further emphasizes that “it is undisputed that before the June 2006 critical date, Trefethen had not been formally published in any journal or conference, nor is there evidence it was available in libraries. Petitioner relies entirely on alleged web availability.” *Id.* at 62–63 (citing *Blue Calypso*, 815 F.3d at 1349).

First, although indexing and cataloging is an important consideration, the lack of indexing and cataloging is not dispositive. As the Federal Circuit explained in *Blue Calypso*, “we found that a particular article that was available only through an on-line publication was publicly accessible . . . [because] the particular on-line publication was well known to the community interested in the subject matter of the reference.” *Blue Calypso*, 815 F.3d at 1349 (citing *Voter Verified, Inc. v. Premier Election Sols., Inc.*, 698 F.3d 1374, 1380 (Fed. Cir. 2012)). Here, Dr. Bajaj testifies as follows:

During the relevant timeframe, researchers commonly made their findings available on websites, particularly the websites associated with their research institution, here Cornell University. *A POSITA working with the MultiMATLAB system would have consulted the Cornell website dedicated to MultiMATLAB, which contained links to both papers.* Co-author Vijay Menon likewise included links to both papers within his web page on the Cornell website. Furthermore, the authors “Vijay Menon” and “Anne E. Trefethen” are common across both papers. The authors Menon and Trefethen were both at the same university, Cornell University, *working on the same research team to develop the MultiMATLAB system.* Accordingly, any POSITA seeking to understand MultiMATLAB would have been presented with both papers to consider.

Ex. 1003 ¶ 72 (citing Ex. 1005, 1; Ex. 1006, 1; Ex. 1023, 40–41) (emphases added). Dr. Bajaj continues:

Cornell was recognized at the relevant timeframe as a *pioneer in “the development of high-performance ‘cluster’*

computers made by linking off-the-shelf computers in parallel.” Further, “[t]he ACM Digital Library (DL) is the world’s most comprehensive database of full-text articles and bibliographic literature covering computing and information technology.” Accordingly, a POSITA interested in computer cluster systems and cluster computing techniques and exercising reasonable diligence would have located Trefethen either from the Cornell website and/or the ACM Digital Library, as evidenced by the afore-mentioned 10 citations to Trefethen papers with online publication dates in between the original publication of Trefethen and the earliest priority date of the ’679 patent.

Ex. 1003 ¶ 117 (quoting Ex. 1033, 2; quoting Ex. 1034, 1; citing Ex. 1035, 2–3) (emphasis added). Dr. Bajaj’s testimony is consistent with the evidence of record, unrebutted, and in line with the Federal Circuit’s reasoning in *Blue Calypso*.

Patent Owner does not offer cross-examination testimony of Dr. Bajaj. Patent Owner does not offer rebuttal testimony that would call into question Dr. Bajaj’s testimony that Cornell was a recognized leader in the field of high-performance cluster computing during the timeframe in question. We credit Dr. Bajaj’s testimony that, given the prominence of the Cornell research team, a POSITA exercising reasonable diligence would have located Trefethen from the Cornell website or ACM Digital Library.

Dr. Hsieh-Yee adds further weight to Petitioner’s argument. Dr. Hsieh-Yee testifies that Trefethen was disseminated and actually located by POSITAs:

Based on the records and documents I have reviewed, it is my opinion that *Trefethen* was published in May 1996, and was archived by Internet Archive on May 10, 1996, making this work discoverable on the Internet on that date. In 1996, 1997 and beyond, interested users could use search engines to search for MultiMATLAB or MATLAB to discover *Trefethen*. They could

also use search engines to discover the lead author’s webpage and follow the link for MultiMATLAB on that webpage to access *Trefethen*. The Washington State University Library cataloged *Trefethen* on November 3, 1997, making this work discoverable at this library on that date. *Three early citations were published in 1997 and 1998, and became publicly accessible at libraries in 1998 and 1999.* The earliest citation is a dissertation completed and approved in September 1997.

Ex. 1086 ¶ 104 (emphasis added); *see also id.* ¶¶ 76–104. We agree with Petitioner; a preponderance of the evidence establishes that “Trefethen was cataloged, indexed, and read and used by POSITAs” prior to June 13, 2006. Reply 31 (citing Ex. 1023; Ex. 1029; Ex. 1035, 2–3; Ex. 1003 ¶¶ 116–117; Ex. 1086 ¶¶ 71–104).

Patent Owner’s rebuttal evidence consists of one instance of self-citation in Menon, which Patent Owner argues is an indication that “[c]itation alone does not prove that the public could locate [Trefethen].” Resp. 63 (citing Ex. 1005, 1–2). Such evidence is weak and unavailing when weighed against the substantial evidence presented by Petitioner. Moreover, even without a known URL or hyperlink to Trefethen, the citations to Trefethen in Menon and other prior art references provide additional motivation for a POSITA, exercising reasonable diligence, to supplement the teachings of Menon by locating Trefethen on the Cornell website or ACM Digital Library. We find Petitioner establishes by a preponderance of the evidence that a POSITA exercising reasonable diligence would have located Trefethen from the Cornell website or ACM Digital Library prior to June 13, 2006.

For the reasons given above, we determine Petitioner has established by a preponderance of the evidence that Trefethen was publicly accessible

before June 13, 2006 and qualifies as a prior art printed publication under 35 U.S.C. § 102.

4. *RS6000 (Ex. 1007), POEref (Ex. 1008), MPIref (Ex. 1017)*

The Petition contends that RS6000 “is a product manual by IBM in support of the IBM RS6000 SP computing solution.” Pet. 15. According to Petitioner, “RS6000 qualifies as a printed publication because it was cataloged and indexed in IBM’s online document library at least as early as 2002 on IBM’s website.” *Id.* (citing Ex. 1003 ¶¶ 119–120; Ex. 1007; Ex. 1029; Ex. 1038). The Petition also explains that “Menon describes the MultiMATLAB architecture on an ‘IBM SP2’ and RS6000 provides details of that system.” Pet. 25 (citing Ex. 1005, Abstract, 6) n.2 (explaining that “‘IBM SP2’ is the same as ‘IBM RS/6000 SP’” (citing Ex. 1010, 6 (“the SP2 was renamed to simply the SP”))). The Petition further contends that a “POSITA seeking to understand MultiMATLAB would be motivated to review the documentation corresponding to the systems expressly discussed in Menon.” *Id.* at 26 (citing Ex. 1003 ¶¶ 86–87; Ex. 1005, 6).

The Petition contends that POEref “is a product manual published by IBM in support for the Parallel Operating Environment running on an RS/6000 system.” Pet. 15. The Petition also contends that “POEref qualifies as a printed publication because it was catalogued and indexed in IBM’s online document library at least as early as 2001” and “was distributed with the IBM SP2 systems and published at least as early as 2001.” *Id.* (citing Ex. 1003 ¶¶ 123–125; Ex. 1008, 157; Ex. 1029; Ex. 1036, 14; Ex. 1039; Ex. 1047).

The Petition contends that “MPIref qualifies as a printed publication because it was distributed to POSITAs using FTP mail servers by the University of Tennessee and Oak Ridge National Library in 1994.” Pet. 15–

16 (citing Ex. 1003 ¶¶ 129; Ex. 1017, cover page; Ex. 1029, 1–3 (Exhibit B)). The Petition also contends that MPIref “was published on MPI Forum’s website no later than July 3, 1998” and “was reasonably located by POSITAs because it had been cited 74 times in papers with online publications dates before the earliest priority date of the ’034 patent.” *Id.* at 16 (citing Ex. 1003 ¶¶ 129–130; Ex. 1029, 1–3; Ex. 1037, 2–16). The Petition further contends that Menon “expressly cite[s] to ‘the MPI communication standard’” and “MPIref is the MPI communication standard referenced by Menon.” *Id.* at 89–90 (quoting Ex. 1005, 5; citing Ex. 1003 ¶¶ 470–471; Ex. 1017, 1 (“MPI: A Message-Passing Interface Standard”)).

Most of Patent Owner’s arguments contesting the public accessibility of RS6000, POEref, and MPIref have been addressed above. Resp. 59–61.

Having considered the evidence of record, we determine the Petition presents evidence establishing that artisans of ordinary skill were aware of the IBM SP2 product and POE at least through publication of Menon and via distribution of POEref with the IBM SP2 product. *See* Pet. 14–15 (citing Ex. 1003 ¶¶ 119–120, 123–125; Ex. 1007; Ex. 1008, 157; Ex. 1029; Ex. 1036, 14; Ex. 1038; Ex. 1039; Ex. 1047). For example, POEref provides specific instructions for locating “IBM product information for RS/6000 SP products on the World Wide Web”:

Most of the RS/6000 SP hardware and software books are available from the IBM Web site at:

<http://www.ibm.com/servers/eserver/pseries>

The serial and parallel programs that you find in the IBM Parallel Environment for AIX: Hitchhiker’s Guide are also available from this Web site, in the same location as the PE online library.

You can view a book, download a Portable Document Format (PDF) version of it, or download the sample programs from the IBM Parallel Environment for AIX: Hitchhiker's Guide.

At the time this manual was published, the Web address of the RS/6000 SP Product Documentation Library page was:

http://www.rs6000.ibm.com/resource/aix_resource/sp_books

Ex. 1008, 157. Dr. Hsieh-Yee testifies:

My research found that archived webpages on the IBM website show *POE-2001* was available no later than February 2002 and continued to be available beyond early 2004. Internet Archive does not archive every web file or resource, and it has not archived *POE-2001*. Changes in IBM servers and system architecture may have contributed to this situation. I have obtained several archived webpages from the IBM website to show how interested users could discover *POE-2001* in 2002, 2003, and 2004, and how this document was presented as available for online browse or download on IBM webpages in those years. These webpages are presented in **Ex. 1113** in this declaration. In addition, two citing documents are included to show *POE-2001* was known and used by researchers in 2004 and 2005.

Ex. 1086 ¶ 128. Dr. Hsieh-Yee's testimony is un rebutted. Further as to POEref, the Petition shows "Menon describes using POE to initialize the MATLAB processes," and "MultiMATLAB uses 'POE, IBM's Parallel Operating Environment,'" so that an artisan of ordinary skill "seeking to understand MultiMATLAB would be motivated to review the documentation corresponding to the systems expressly discussed in Menon." Pet. 26 (quoting Ex. 1005, 6; citing Ex. 1003 ¶¶ 86–87). We agree with Petitioner's analysis supported by Dr. Hsieh-Yee's Declaration testimony. Pet. 14–15; Reply 31–33 (citing Ex. 1086 ¶¶ 105–148).

For the reasons given above, we find that a preponderance of the evidence supports Petitioner's contention that RS6000 and POEref were

accessible to a POSITA exercising reasonable diligence prior to June 13, 2006.

Petitioner further shows “Menon describes that a POSITA would look to use the MPI standard because of MPI’s ‘broad popularity, its suitability to high performance parallel computing, and the virtually universal availability of vendor-optimized versions on modern parallel computers.’” Pet. 90 (quoting Ex.1005, 5 (“IBM’s proprietary version of MPI [is] specifically optimized for the SP2”)) (citing Ex. 1003 ¶ 470). This evidence further supports the Petition’s contention that an artisan of ordinary skill would have been motivated and able to locate MPIref as documentation of IBM’s optimized MPI for use in the SP2 system.

Patent Owner contends that “Petitioner offers no evidence that anyone outside the MPI Forum ever knew of or accessed the draft [MPIref].” Resp. 61. Petitioner again replies with authoritative evidence from Dr. Hsieh-Yee:

Based on the documents and records I have reviewed, it is my opinion that *MPI-1994* became publicly accessible by November 1994 when a citing document was published, and when the National Science Library of Canada created their original MARC record for this standard. *MPI-1994* was definitely available no later than July 1998 when it was first archived by Internet Archive.

Ex. 1086 ¶ 182; Reply 33–34 (citing Ex. 1086 ¶¶ 149–182). Patent Owner’s unsupported Sur-Reply contention, that “Petitioner offers no contemporaneous evidence that any skilled person actually accessed” the references “through the cataloging records or citation chains the Reply now invokes” (Sur-Reply 25), is make weight; the argument does not undermine the substantial evidence of record satisfying Petitioner’s burden of proof by a preponderance of the evidence that MPIref was publicly accessible to a POSITA exercising reasonable diligence prior to June 13, 2006.

5. Conclusion as to Public Accessibility

For the reasons given above, we determine Petitioner has established by a preponderance of the evidence that Menon, Trefethen, RS6000, POEref, and MPIref were publicly accessible prior to June 13, 2006 and qualify as prior art printed publications under 35 U.S.C. § 102.

III. CONCLUSION

We conclude Petitioner has established by a preponderance of the evidence that claims 1–30 of the '034 patent are unpatentable. In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not shown Unpatentable
1–25, 27– 28, 30	103(a)	Menon, Trefethen, RS6000, POEref	1–25, 27–28, 30	
26, 29	103(a)	Menon, Trefethen, RS6000, POEref, MPIref	26, 29	
Overall Outcome			1–30	

ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has shown by a preponderance of the evidence that claims 1–30 of the '034 patent are unpatentable;

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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