IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

INTELLECTUAL VENTURES I LLC, *Plaintiff,*	§	
-v-	§	**6:23-CV-00309-ADA**
TCL ELECTRONICS HOLDINGS LTD. F/K/A TCL MULTIMEDIA TECHNOLOGY HOLDINGS, LTD., TCL INDUSTRIES HOLDINGS CO., LTD., *Defendants.*	§	

CLAIM CONSTRUCTION ORDER AND MEMORANDUM IN SUPPORT THEREOF

Before the Court are the Parties' claim construction briefs: Defendants TCL Electronics Holdings Ltd. f/k/a TCL Multimedia Technology Holdings, Ltd. and TCL Industries Holdings Co., Ltd.'s Opening brief (ECF No. 30) and Plaintiff Intellectual Ventures I LLC's Response brief (ECF No. 32). The Court provided preliminary constructions for the disputed terms one day before the hearing. The Court held the *Markman* hearing on September 9, 2024. ECF No. 42. During that hearing, the Court informed the Parties of the final constructions for most of the disputed terms. *Id.* This Order does not alter any of those constructions.

I. DESCRIPTION OF THE ASSERTED PATENTS

Plaintiff asserts U.S. Patent Nos. 7,089,443 and 7,6234,39. The descriptions of each patent are as follows.

A. U.S. Patent No. 7,089,443

At the time of the invention, further increases in microprocessor clock frequency (which correlates with microprocessor performance) were limited by wire delays. '443 Patent at 1:25–37.

Another problem that could limit increasing the clock frequency is the need to "distribute the clock across a progressively larger die to increasing numbers of latches while meeting a decreasing clock skew budget." *Id.* at 1:37–40. The specification describes that the "inevitable conclusion reached by industrial researchers is that in order to continue the current pace of clock frequency increases, microprocessor designers will eventually be forced to abandon singly-clocked globally synchronous systems in favor of some form of asynchrony[.]" *Id.* at 1:40–45.

The specification describes that the present invention is "directed to a multiple clock domain (MCD) microarchitecture, which uses a globally-asynchronous, locally-synchronous (GALS) clocking style." *Id.* The specification describes that in an MCD microprocessor "each functional block operates with a separately generated clock, and synchronizing circuits ensure reliable inter-domain communication. Thus, fully synchronous design practices are used in the design of each domain." *Id.* at 4:16–19. Because a GALS microarchitecture uses individual clocks for each domain (*i.e.*, "locally-synchronous"), there is no single "global" clock that all domains use (*i.e.*, "globally-asynchronous"). *See, e.g., id.* at 4:21–33.

B. U.S. Patent No. 7,6234,39

The '439 Patent is directed towards cyclic diversity in multi-antenna systems. '439 Patent at Abstract. The claimed invention aims to improve signal reception and/or decrease the error rates in environments with potential interference. The specification describes that

> With cyclic delay diversity, each tone or subcarrier is cyclically shifted (e.g., in the baseband processing portion of the MA transmitter device 102, FIG. 1) by a defined amount of samples, resulting in a circular shift of all of the samples involved (e.g., 64 samples plus 16 samples of the data and guard interval, respectively).

Id. at 3:52–57. The specification describes that one method embodiment includes "providing an orthogonal frequency division multiplexing (OFDM) packet corresponding to a first transmit antenna, and cyclically advancing, or the periodic equivalent, one or more sections of the OFDM

packet corresponding to a second transmit antenna, the duration of the cyclic advance having a duration less than a guard interval." *Id.* at 4:35–41. Figure 8 illustrates 4-sample cyclic advance diversity as implemented by the communication system 600 shown in Figure 6.

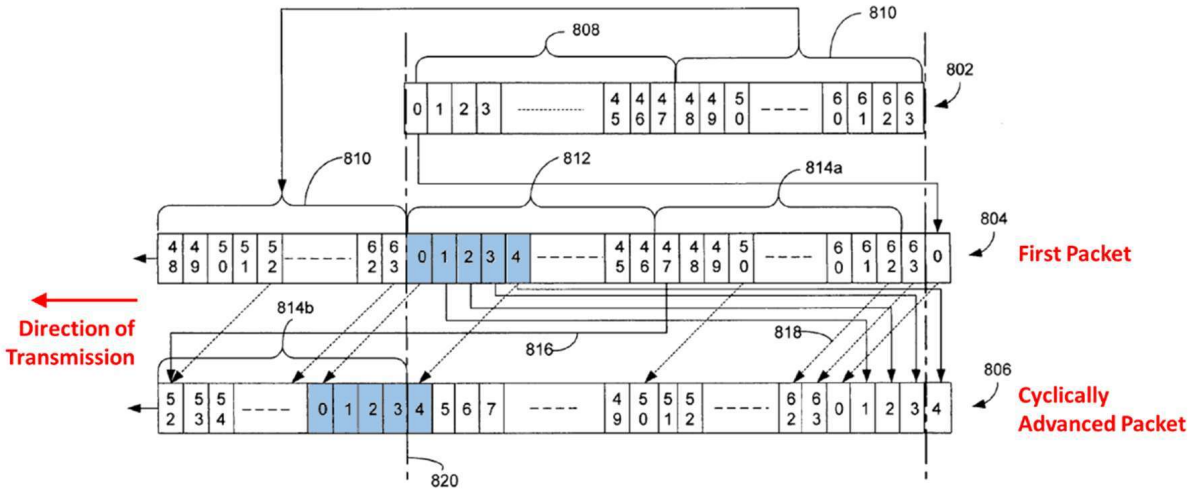

FIG. 8

Id. at Figure 8 (annotations added by Defendants).

II. LEGAL STANDARD

A. General principles

The general rule is that claim terms are generally given their plain-and-ordinary meaning. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*); *Azure Networks, LLC v. CSR PLC*, 771 F.3d 1336, 1347 (Fed. Cir. 2014), *vacated on other grounds*, 575 U.S. 959, 959 (2015) ("There is a heavy presumption that claim terms carry their accustomed meaning in the relevant community at the relevant time.") (internal quotation omitted). The plain-and-ordinary meaning of a term is the "meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Phillips*, 415 F.3d at 1313.

The "only two exceptions to [the] general rule" that claim terms are construed according to their plain-and-ordinary meaning are when the patentee (1) acts as his/her own lexicographer or (2) disavows the full scope of the claim term either in the specification or during prosecution. *Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). The Federal Circuit has counseled that "[t]he standards for finding lexicography and disavowal are exacting." *Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014). To act as his/her own lexicographer, the patentee must "clearly set forth a definition of the disputed claim term" and "'clearly express an intent' to [define] the term." *Thorner,* 669 F.3d at 1365.

"Like the specification, the prosecution history provides evidence of how the PTO and the inventor understood the patent." *Phillips*, 415 F.3d at 1317. "[D]istinguishing the claimed invention over the prior art, an applicant is indicating what a claim does not cover." *Spectrum Int'l, Inc. v. Sterilite Corp.*, 164 F.3d 1372, 1379 (Fed. Cir. 1998). The doctrine of prosecution disclaimer precludes a patentee from recapturing a specific meaning that was previously disclaimed during prosecution. *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1323 (Fed. Cir. 2003). "[F]or prosecution disclaimer to attach, our precedent requires that the alleged disavowing actions or statements made during prosecution be both clear and unmistakable." *Id.* at 1325–26. Accordingly, when "an applicant's statements are amenable to multiple reasonable interpretations, they cannot be deemed clear and unmistakable." *3M Innovative Props. Co. v. Tredegar Corp.*, 725 F.3d 1315, 1326 (Fed. Cir. 2013).

A construction of "plain and ordinary meaning" may be inadequate when a term has more than one "ordinary" meaning or when reliance on a term's "ordinary" meaning does not resolve the parties' dispute. *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co*., 521 F.3d 1351, 1361

(Fed. Cir. 2008). In that case, the Court must describe what the plain-and-ordinary meaning is. *Id.*

"Although the specification may aid the court in interpreting the meaning of disputed claim language . . ., particular embodiments and examples appearing in the specification will not generally be read into the claims." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988). "[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004).

Although extrinsic evidence can be useful, it is "less significant than the intrinsic record in determining 'the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 862 (Fed. Cir. 2004)). Technical dictionaries may be helpful, but they may also provide definitions that are too broad or not indicative of how the term is used in the patent. *Id.* at 1318. Expert testimony may also be helpful, but an expert's conclusory or unsupported assertions as to the meaning of a term are not. *Id.*

B. Order of method steps

When analyzing whether an order exists between steps of method claim, the presumption is that limitations may be performed in any order. *Altiris, Inc. v. Symantec Corp.*, 318 F.3d 1363, 1369 (Fed. Cir. 2003). Courts first look at the "claim language to determine if, as a matter of logic or grammar, they must be performed in the order written" and, if not, whether the specification "directly or implicitly requires such a narrow construction." *Id.* at 1369–70.

III. LEGAL ANALYSIS

A. Term #1: "operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another"

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
#1: "operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another" U.S. Patent Nos. 7,089,443, Claim 8	Plain and ordinary meaning	"synchronously" means "using the same clock with a fixed phase relationship" and "asynchronously" means "using independent clocks with no known phase relationship"

<u>The Parties' Positions:</u>

Defendants contend that "the phrase is ambiguous regarding what it means for the clock domains to operate synchronously while at the same time operating asynchronously." Opening at 3. By way of example, Defendants contend that "if operating each domain synchronously is interpreted to mean that all of the domains run on a singular clock or at the same frequency as each other, then it is unclear how the domains could also operate asynchronously relative to one other." *Id.*

With respect to "asynchronous," Defendants contend that this type of operation requires using independent clocks for each of the domains in the MCD microarchitecture. *Id.* at 4. Defendants contend that the specification describes that prior art systems incorporated a "'limited amount of asynchrony,' where different microprocessor components, such as the memory bus and processor core, 'run … off of a ***different clock*** … in order to allow a single system to accommodate processors of different frequencies.'" *Id.* (citing '443 Patent at 1:55-60) (emphasis and ellipses in

Defendants' brief). Defendants contend that the specification describes that the "'the present invention' is directed to an MCD microarchitecture in which each domain operates with 'separately generated' and 'completely independent' clocks." *Id.* (citing '443 Patent at 4:13–19, Abstract, 4:23–33, 7:29–30, 10:29–31, 10:39–40).

Defendants contend that the specification also "explains that the asynchronous operation of the invention requires that these independent clocks have no known phase relationship with respect to each other." *Id.* By way of example, Defendants contend that the specification "contrasts global synchronization schemes, which require 'control[ling] the phase relationships of the clocks' in all domains, with the globally ***asynchronous*** design of the '443 Patent, which instead uses '***independent clocks with no known phase relationship***.'" *Id.* (citing '443 Patent at 6:32–44) (emphases and alteration in Defendants' brief).

Defendants contend that the extrinsic evidence supports its argument that there is a "lack of a known phase relationship among the asynchronous clock domains." *Id.* at 4–5 (citing Opening, Ex. C at 46).

With respect to "synchronous," Defendants contend that the specification "generally explains that synchronous designs refer to 'singly-clocked' systems." *Id.* at 5 (citing '443 Patent at 1:44–45, 4:51–54). Defendants contend that the specification "makes clear that the 'synchronous' operation of the domains in its invention does not refer to ***global*** synchronization but instead applies to the ***local*** clock timing within each individual domain." *Id.* (emphases in Defendants' brief). More specifically, Defendants contend that "'the present invention' of the '443 Patent is directed to an MCD microarchitecture that uses globally-asynchronous and ***locally-synchronous*** clocking, wherein 'fully synchronous design practices are used ***in the design of each domain***.'" *Id.* (citing '443 Patent at 4:13–21) (emphases in Defendants' brief). Based on that,

Defendants contend that "when the claim language refers to the 'synchronous' operation of each domain, it is referring to each individual domain using a singular local clock (i.e., the functions within a domain use the same local clock)." *Id.*

Defendants contend that "synchronous operation within a domain requires that the clock signals used in that domain have a fixed phase relationship." *Id.* More specifically, Defendants contend that in the "Summary of the Invention" section, the specification "makes clear that the local clock within each individual domain is phase-locked (i.e., fixed) by a local Phase Lock Loop (PLL) circuit." *Id.* (citing '443 Patent at 4:25–28, 9:49–51).

Defendants contend that the extrinsic evidence supports its contention that "synchronous" operation means that there is a "fixed phase relationship of all clocking signals[.]" *Id.* at 6 (citing Opening, Ex. C at 971).

Defendants contend that a construction of plain-and-ordinary meaning "would not resolve the ambiguities for the jury, risking the misapplication of constructions contrary to the intrinsic and extrinsic evidence[.]" *Id.* (citing cases).

In its response, Plaintiff contends that Defendants' proposed construction "would inject ambiguity into an otherwise unambiguous term by contradicting the intrinsic record." Response at 2.

Plaintiff first contends that Defendants "removes the terms 'synchronously' and 'asynchronously' from the context of the claim element they are part of to further its argument that the terms are 'ambiguous.'" *Id.* Plaintiff contends that the specification describes "operations within each domain are synchronous, while operations between domains are asynchronous." *Id.* at 3. Plaintiff contends that this approach was known in the art as "globally-asynchronous, locally-synchronous clocking style, often abbreviated as GALS." *Id.* (citing'443 Patent at Abstract, 4:13–

25). Plaintiff contends that "[g]iven that GALS clocking methodologies were well-understood at the time, and described throughout the specification consistently with such knowledge, no construction other than the terms' plain and ordinary meaning is required." *Id.* (citing'443 Patent 4:13–25, 4:25–29, 4:51–5:4; M. Krstic, et. al. GLOBALLY ASYNCHRONOUS, LOCALLY SYNCHRONOUS CIRCUITS: OVERVIEW AND OUTLOOK, *IEEE Design & Test of Computers*, Vol. 24, no. 5, pp. 430-441, Sept.-Oct. 2007, available at https://ieeexplore.ieee.org/abstract/document/4338463).

Plaintiff next contends that Defendants' proposed construction "reads extraneous limitations into the claim based on cherry-picked citations that are inconsistent with the specification's disclosure as a whole." *Id.* More specifically, with respect to "with no known phase relationship," Plaintiff contends that the passage that Defendants cite to (6:32–45) describes "why the inventors chose to use hardware arbitration for inter-domain synchronization rather than using restrictions on the phase relationship and relative clock frequencies, *not* how the synchronous or asynchronous functionality works." *Id.* at 3–4 (emphasis in Plaintiff's brief).

With respect to the passage Defendants rely on for support for their proposed construction for "asynchronous" (6:32–44), Plaintiff contends that this passage actually discusses that the inventors describe that

> their improved solution for inter-domain synchronization that allows different domains to operate asynchronously *relative to one another* even when there is no known phase relationship between domains at all—the worst-case scenario from a synchronization overhead perspective. In other words, the specification does not describe the claimed asynchrony as *requiring* there be no known phase relationship between domains, but simply states that even in scenarios where that is the case, the claimed queue-based technique can facilitate the operations of the different domains more efficiently than prior-art solutions.

Id. at 4 (emphases in Plaintiff's brief).

Plaintiff further contends that, by contrast, the specification "clearly describes that there *can* be a known phase relationship between asynchronous domains." *Id.* (emphasis in Plaintiff's brief). In particular, Plaintiff contends that

> because of the ultimate requirement of inter-domain synchronization— *i.e.*, 'that data generated in one domain and needed in another must cross a domain boundary'—logically there must be some way to know the phases of each domain in the MCD so that the synchronization can take place. Otherwise, no amount of asynchronous operation between domains could be tolerated. Thus, rather than supporting [Defendants'] improperly narrow construction, the specification teaches away from it.

Id. (citing '443 Patent at 10:25–27). Plaintiff contends that the specification describes using a simulator to model the synchronization costs resulting from inter-domain clock rate differences where "[i]nitially, all clocks are randomized in terms of their starting times, but the time of the next clock pulse in a domain can be determined by adding the domain cycle time to the starting time and then adding the jitter time for that cycle to the total sum." *Id.* at 4–5 (citing '443 Patent at 10:43–55). Plaintiff contends that this allows the "system to accurately account for synchronization costs resulting from inter-domain clock rate differences." *Id.* at 5.

With respect to "synchronous," Plaintiff contends that Defendants' proposed construction is "internally inconsistent and creates ambiguity where none previously existed" as it requires "clock domain … have a phase relationship with itself." *Id.* Plaintiff contends that the phrase "fixed phase" does not appear in the intrinsic record. *Id.*

Plaintiff contends that a POSITA "would not consider [Defendants'] definitions consistent with the plain meaning of the disputed terms, and as described above, they are in fact inconsistent with the intrinsic record itself." *Id.* at 6. Rather, Plaintiff contends that "[t]he claim specifies that each domain is clocked separately at a clock frequency and has a voltage applied separately. This is all that is required in terms of explanation[.]" *Id.*

The Court's Analysis:

After reviewing the parties' arguments and considering the applicable law, the Court agrees with Plaintiff that this term should be construed according to its plain-and-ordinary meaning for the reasons that follow. ***First***, the "heavy presumption" is that terms should be construed according to their plain-and-ordinary meaning. *Azure Networks*, 771 F.3d at 1347.

Second, Defendants do not expressly allege lexicography or disclaimer, which are the only two exceptions to the general rule that a term should be construed as having its plain-and-ordinary meaning. *Thorner*, 669 F.3d at 1365.

Third, given that both "synchronous" and "asynchronous" are terms of art—with well-understood meanings to a POSITA—plain-and-ordinary meaning is the appropriate construction for both terms. For example, U.S. Patent No. 5,309,561, which is intrinsic evidence as it is cited on the face of the '443 Patent, is entitled "Synchronous processor unit with interconnected, separately clocked processor sections which are automatically synchronized for data transfer operations." *V-Formation, Inc. v. Benetton Grp. SpA*, 401 F.3d 1307, 1311 (Fed. Cir. 2005) ("The Federal Circuit has established that prior art cited in a patent or cited in the prosecution history of the patent constitutes intrinsic evidence."). The '561 Patent uses the term "synchronous" over a dozen times—including in the claims several times—and describes that "[m]any, if not all, processor units in use today are synchronous machines in that operations are performed in synchronous fashion, to the tune of a periodic clock signal ('clock')." '561 Patent at 1:14–17. Similarly, U.S. Patent No. 5,710,910, which is also cited on the face of the '443 Patent, also uses the term "synchronous" over a dozen times. *See generally* '910 Patent. The '910 Patent describes that "synchronous" clocking is "conventional." *See, e.g.*, '910 Patent at 1:36–39, 1:62–65. Other

patents cited on the face of the '443 Patent also use the term "synchronous" in their respective specifications. *See generally* U.S. Patent Nos. 5,796,995, 6,463,547.

Similarly, the '910 Patent is entitled "Asynchronous self-tuning clock domains and method for transferring data among domains" and uses the term "asynchronous" over two dozen times in its specification, in addition to the claims. *See generally* '910 Patent.

Furthermore, the term "globally-asynchronous locally-synchronous" is a term of art. For example, at least two references in the IEEE journal paper that Plaintiff cites to have a title that includes the term "globally-asynchronous locally-synchronous" or "GALS," and that were published before the filing date of the provisional application that the '443 Patent claims priority to (2003). *See, e.g.*, Daniel Chapiro, *Globally-Asynchronous Locally-Synchronous Systems* (1984); J. Muttersbach, T. Villiger and W. Fichtner, *Practical design of globally-asynchronous locally-synchronous systems*, in PROC. OF THE SIXTH INT'L SYMP. ON ADVANCED RESEARCH IN ASYNCHRONOUS CIRCUITS AND SYS. 52 (2000). Because "globally-asynchronous locally-synchronous" is a term of art with a well-understood meaning to a POSITA, that further confirms that "synchronous" and "asynchronous" are also terms of art with well-understood meanings to a POSITA. Accordingly, a plain-and-ordinary meaning construction is appropriate.

Fourth, with respect to Defendants' proposed construction for "synchronous," the Court agrees with Plaintiff that it is illogical. More specifically, the specification describes that each of the "locally synchronous" clock domains uses a <u>single</u> clock. '443 Patent at 4:16–18 ("In an MCD microprocessor each functional block operates with **<u>a separately generated clock</u>**"), 4:51–54 ("The preferred embodiment uses four domains, one of which includes the L2 cache, so that domains may vary somewhat in size and **<u>still be covered by a single clock</u>**."), 10:65–11:2

("During this initial run we collect a trace of all primitive events (temporally contiguous operations performed on behalf of a single instruction by hardware **in a single clock domain**), and of the functional and data dependences among these events.") (emphases added to all passages). Therefore, because "locally synchronous" refers to the clocking within a single clock domain, the Court agrees with Plaintiff that "using the same clock with a fixed phase relationship" in Defendants' proposed construction illogical because it requires that one clock signal has a fixed phrase relationship with itself.

Fifth, with respect to Defendants' argument that descriptions of a PLL in the specification support the inclusion of "using the same clock with a fixed phase relationship" in its proposed construction for "synchronous," the Court disagrees. Rather than lock-in a fixed phase relationship between two clock signals, the specification appears to describe that the PLL helps provide a variable clock frequency. *Id.* at 9:49–50 ("Frequency changes require the PLL to re-lock."); 4:25–32 ("The global clock distribution network is greatly simplified, requiring only the distribution of the externally generated clock to the local Phase Lock Loop (PLL) in each domain. The independence of each local domain clock implies no global clock skew requirement, permitting potentially higher frequencies within each domain and greater scalability in future process generations."); *see also* Ian Collins, *Phase-Locked Loop (PLL) Fundamentals*, ANALOG DEVICES (July 2018), https://www.analog.com/en/resources/analog-dialogue/articles/phase-locked-loop-pll-fundamentals.html. Therefore, rather than varying the phase, the PLL helps vary the clock frequency.[1] Accordingly, the Court concludes that a POSITA would not understand that the

[1] To the extent that Defendants' "fixed phase relationship" describes a fixed phase offset, an ideal PLL (*i.e.*, one without jitter or skew) does not have a phase offset, namely, there is no constant phase shift between the input, *e.g.*, global clock, and the output, *e.g.*, local clock.

passages that Defendants cite supports construing "synchronously" as "using the same clock with a fixed phase relationship."

Sixth, with respect to "with no known phase relationship" in Defendants' proposed construction for "asynchronous," the Court concludes there is no intrinsic support for the addition of that limitation. Defendants cite 6:32–44 of the '443 Patent as support for that phrase. That passage recites:

> Some synchronization schemes restrict the phase relationship and relative frequencies of the clocks, thereby eliminating the need for hardware arbitration. Unfortunately, these schemes impose significant restrictions on the possible choices of frequencies. In addition, the need to control the phase relationships of the clocks means that global clock synchronization is required. Our design specifically recognizes the overhead associated with independent clocks with no known phase relationship. We believe this overhead to be unavoidable in an MCD processor: one of the motivating factors for the design is the recognition that traditional global clock distribution will become increasingly difficult in the future.

'443 Patent at 6:32–44 (citation omitted). The first sentence describes one approach describes one trade-off in the prior art, namely, eliminating the need for hardware arbitration by restricting the phase relationship and relative frequencies of the clocks. *Id.* The second and third sentences describe shortcomings of the prior art, namely, that "these schemes impose significant restrictions on the possible choices of frequencies" and "the need to control the phase relationships of the clocks means that global clock synchronization is required." The next sentence contrasts the invention with the prior art, namely, that the invention does not limit the restrict the phase relationship and relative frequencies of the clocks, but rather uses "independent clocks with no known phase relationship," at the cost of incurring some overhead. This sentence, however, does not necessarily mean that the phase relationship between clocks are necessarily unknowable, but rather, this sentence describes the worst case scenario, namely, where the phase relationship between clocks are not known. But because this sentence only represents one scenario—the worst

case scenario—the Court concludes that including "with no known phase relationship" is incorrect as the worst case scenario is not a "clear and unambiguous disavowal of claim scope." *Saffran v. Johnson & Johnson*, 712 F.3d 549, 559 (Fed. Cir. 2013).

Therefore, for the reasons described above, the Court finds that the term should be construed according to its plain-and-ordinary meaning.

B. Term #2: "generating a first OFDM packet" / "cyclically advancing the first OFDM packet . . . to generate a shifted version of the first OFDM packet"

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction
"generating a first OFDM packet" / "cyclically advancing the first OFDM packet . . . to generate a shifted version of the first OFDM packet" U.S. Patent No. 7,623,439, Claims 1, 8	Plain and ordinary meaning	Order of steps: "generating a first OFDM packet..." must occur before "cyclically advancing the first OFDM packet ... to generate a shifted version of the first OFDM packet"

<u>The Parties' Positions:</u>

Claim 1, a method claim, which is similar to Claim 8, an apparatus claim, recites;

1. A method for transmitting orthogonal frequency division multiplexing (OFDM) signals comprising:

[a] generating a first OFDM packet for transmission including a guard interval portion and a symbol data portion each comprised of a plurality of samples;

[b] cyclically advancing the first OFDM packet by shifting the samples in a first direction an amount less than a sample duration of the guard interval portion to generate a shifted version of the first OFDM packet for transmission in which at least a non-zero number of the samples from the symbol data portion of the first OFDM packet are shifted into the guard interval portion of the shifted version and a same non-zero number of samples from the guard interval portion of the first OFDM packet are shifted out of the guard interval portion of the shifted version; and

[c] substantially simultaneously transmitting the first OFDM packet and the shifted version of the OFDM packet.

'739 Patent, Claim 1 (annotations added).

Defendants contend that "the claims require some of the recited steps to be performed in order, because certain steps depend upon an OFDM packet generated during a previous step." Opening at 10. Defendants specifically contend that Limitation [b] must follow Limitation [a] because the claim language describes that the packet needs to be created in Limitation [a] before it can be shifted in Limitation [b]. *Id.* at 10–11. Defendants contend that the claim language also describes that "the transmitting step [1C] must necessarily follow steps [1A] and [1B] because it needs the original OFDM packet from [1A] and the shifted version from [1B] in order to substantially simultaneously transmit both packets." *Id.* at 11 n.1. Defendants contend that "if the packet generation step [1A] were not performed first to create '***a*** first OFDM packet,' there would be no antecedent basis for '***the*** first OFDM packet' referred to in packet shifting step [1B]." *Id.* (citing cases) (emphases in Defendants' brief).

Defendants contend that "every embodiment discussed in the specification requires this order." *Id.* at 11 (citing *Mformation Techs., Inc. v. Research in Motion Ltd.*, 764 F.3d 1392. 1400 (Fed. Cir. 2014)). More specifically, Defendants contend that "the method of Figure 10 begins with the step of providing an OFDM packet. After that, a cyclic advancement is performed on the OFDM packet generated in the previous step." *Id.* at 12 (citing '439 Patent at Figure 10 (Blocks 1002, 1004); 9:1–10). Defendants contend that "***nowhere*** does the '439 Patent disclose any embodiments in which the shifted version of the OFDM packet is created ***before*** the original OFDM packet itself is generated." *Id.* (emphases in Defendants' brief).

Defendants contend that "boilerplate language [in the specification] that 'alternate implementations' in which 'functions may be executed out of order from that shown or discussed' are allegedly included within the patent's scope…[t]his boilerplate language does not override the

order required by the plain language of the claims and the only disclosed embodiments." *Id.* (citing '439 Patent at 9:11–20).

With respect to Claim 8, an apparatus claim, Defendants contend that "system claims can have an order of steps when they are similar to the method claim." *Id.* (citing cases). Defendants contend that "system claim 8 of the '439 Patent contains virtually identical limitations as method claim 1, including the same referential language back to the results of prior steps[.]" *Id.* at 12–13.

In its response, Plaintiff contends that the presumption is that there is no ordering between limitations of a method claim or a system claim. Response at 6.

With respect to Defendants' antecedent basis argument, Plaintiff contends that Defendants misstate the relevant caselaw. *Id.* at 7. Plaintiff further contends that Defendants' argument is "illogical and quickly disproven using common sense alone." *Id.* More specifically, Plaintiff contends that antecedent basis does not impose a temporal requirement between serial instances of a term. *Id.* Plaintiff contends that, by contrast, if Defendants are correct then "every single method claim that uses the terms 'the' or 'said' would be limited to a particular ordering of its steps." *Id.*

Plaintiff contends that the claim language "expressly does *not* impose any requirement about whether the first packet is generated before the step of cyclically advancing is performed." *Id.* (emphasis in Plaintiff's brief). More specifically, Plaintiff contends that the claims "explicitly recite that both the first OFDM packet and the shifted packet are transmitted 'substantially simultaneously.'" *Id.* at 7–8. Plaintiff contends that "[b]y expressly requiring that both packets be transmitted at substantially the same time, the claim makes it clear that one packet does not have to be generated before the other in order to practice the claim." *Id.* at 8.

Plaintiff contends that Defendants' argument regarding the specification also fail because it is "an undisguised attempt to import features of the preferred embodiments into the claims." *Id.* Plaintiff further contends that the specification "explicitly discloses" that there is not ordering. *Id.* More specifically, Plaintiff contends that Figure 6 of the specification depicts "transmit processors 608 and 614 both receive the same incoming data, TX data 1, and operate thereupon in parallel, producing unshifted and cyclically shifted versions of the OFDM symbols." *Id.* Based on that, Plaintiff contends that "the specification discloses an embodiment that [Defendants'] construction improperly excludes." *Id.*

Plaintiff contends that the limitations of Claim 8, an apparatus claim, are not limiting for the same reasons that the limitations of Claim 1 are not limiting. *Id.*

<u>The Court's Analysis:</u>

For brevity and simplicity, in its analysis, the Court will refer to the "generating a first OFDM packet…" limitation as "generating," the "cyclically advancing the first OFDM packet ... to generate a shifted version of the first OFDM packet" limitation as "shifting," and the "substantially simultaneously transmitting the first OFDM packet" / "substantially simultaneously cause the transmission of the first OFDM packet" limitations as "transmitting."

After reviewing the parties' arguments and considering the applicable law, the Court concludes that:

- "generating" **starts and ends before** "shifting" for Claim 1, but not for Claim 8.
- "transmitting" **starts after the starts of, but not necessarily after the ends of,** both [1] "generating" and [2] "shifting."

With respect to the first bullet, the Court concludes that, as a matter of logic, the language of Claim 1 requires that the "generating" step must occur before the "shifting" step. *Altiris*, 318 F.3d 1369–70. Logically, an OFDM packet cannot be shifted until it is first generated, and if the OFDM packet has not been generated, then there is nothing to shift. Therefore, the "generating" step must start and end before the "shifting" step, which is enough to overcome the presumption that there is no order between these two steps. *Id.* at 1369–70.

With respect to Plaintiff's argument that "[b]y expressly requiring that both packets be transmitted at substantially the same time, the claim makes it clear that one packet does not have to be generated before the other in order to practice the claim[,]" the Court does not find that argument persuasive. In particular, the step that Plaintiff points to ("substantially simultaneously transmitting the first OFDM packet and the shifted version of the OFDM packet") only describes that the transmissions of the original OFDM packet and the shifted version only need to be substantially simultaneously, *i.e.*, partially, but not fully, overlapping. But this limitation only describes what happens during transmission. It does not describe what happens prior to transmission, let alone whether shifting can precede generating. Furthermore, even if the transmit processor starts transmitting the shifted OFDM packet before transmitting the non-shifted OFDM packet, that does not necessarily mean that the shifted OFDM packet was shifted before it was generated. Rather, it only means that the transmission start time of the non-shifted OFDM packet was delayed more than the transmission start time of the shifted OFDM packet. Therefore, Plaintiff's argument that "expressly requiring that both packets be transmitted at substantially the same time" means that there is no order between the "generating" and "shifting" steps is unavailing.

With respect to Plaintiff's argument that requiring that the "generating" step to occur before the "shifting" step would improperly limit the claim to a disclosed embodiment, the Court disagrees as the Federal Circuit has not held there cannot be an specific ordering of method steps if said ordering would limit the claim to a disclosed embodiment, nor does Plaintiff identify any such case. Rather, courts first look at the "claim language to determine if, as a matter of logic or grammar, they must be performed in the order written" and, if not, whether the specification "directly or implicitly requires such a narrow construction." *Id.* at 1369–70.

With respect to apparatus Claim 8, while the "generating" and "shifting" limitations appear to be similar to the "generating" and "shifting" steps in method Claim 1, the Court concludes that there is no ordering between the "generating" and "shifting" limitations in Claim 8; more specifically that the "shifting" limitation does not need to necessarily follow the "generating" limitation. The key difference between method Claim 1 and apparatus Claim 8 is that latter requires two transmit processors, and thus has an element of parallelism. '439 Patent, Claim 8, Limitations [a], [b]. Apparatus Claim 8 discloses that the first transmit processor does the "generating" while the second transmit processor does the "shifting." *Id.* But there does not appear to be any requirement in the claim language—nor did Defendants identify any such claim language—that the second transmit processor must shift what the first transmit processor generated. While the second transmit processor could certainly shift what the first transmit processor generated, what could also happen is that (1) both transmit processors could generate their own packets (hereinafter "parallel packet generation") and (2) the second transmit processor could then shift the packet it generated. In this scenario, the second transmit processor could generate a packet (unclaimed) and then shift that packet (claimed) before the first transmit processor generates a packet (claimed). Therefore, it is ***not*** a matter of logic (or grammar) that

"generating" by the first transmit processor must precede "shifting" by the second transmit processor. Furthermore, there does not appear to be any description in the claims that the second transmit processor is not capable of generating a packet.

With respect to Defendants' antecedent basis argument (the antecedent basis for "the first OFDM packet," is "a first OFDM packet," which indicate a temporal relationship between those two instances of "first OFDM packet"), the Court disagrees. More specifically, antecedent basis is simply a way to draft claims and does not necessarily impose a temporal ordering between the two. Furthermore, the Court agrees with Plaintiff that "every single method claim that uses the terms 'the' or 'said' would be limited to a particular ordering of its steps," which tends to indicate that Defendants' argument is incorrect. Response at 7.

With respect to Defendants' argument in the hearing that there is no description of parallel packet generation in the text at 6:6–55 of the '439 Patent, the Court disagrees for at least two reasons. Hrg. Tr. at 20:21–21:4. First, even if that is true, that description is directed towards a specific embodiment and it would be improper to limit the claim scope only to embodiments that exclude parallel packet generation, at least absent a disclosure in the specification that "directly or implicitly requires such a narrow construction." *Altiris*, 318 F.3d at 1369–70. Second, given that the claim is a "comprising" claim, it does not necessarily exclude parallel packet generation.

To the extent that Defendants argue that connection 630 in Figure 6 depicts that the first transmit processor generates the OFDM Packet, transmits across connection 630, and then finally second transmit processor shifts it, the Court again disagrees. More specifically, connection 630 only shows that some data could be transmitted from the first transmit processor to the second transmit processor, but not necessarily that the data being transmitted is necessarily the generated packet (or that that generated packet is then shifted).

Furthermore, the specification does not disclose that generated OFDM packets are transmitted across connection 630. Rather, the specification only discloses that "transmit processors 608 and 614 encode and interleave the incoming data (designated TX data1 at TX data rate1 at module 604, which is also provided to module 606 as represented by connection 630)." '439 Patent at 6:42–45.

Even assuming that the specification did disclose that transmit processor 608 transmitted the generated OFDM packet across connection 630 to transmit processor 614, it would be improper to limit the claim scope to this embodiment, at least absent a disclosure in the specification that "directly or implicitly requires such a narrow construction." *Altiris*, 318 F.3d at 1369–70.

With respect to the second bullet, the Court concludes that, as a matter of logic, the language of Claims 1 and 8 require that the "generating" and "shifting" limitations must occur before the "transmit" limitation. *Altiris*, 318 F.3d 1369–70. Logically, an OFDM packet (or a shifted OFDM packet) cannot be transmitted until it is first generated (or first generated and shifted), and if the OFDM packet has not been generated (or first generated and shifted), then there is nothing to transmit. Therefore, the "generating" and "shifting" limitations must start before the "transmitting" limitation. But these two limitations do not necessarily need to end before the "transmitting" limitation begins because the transmit processor, for example, may start transmitting the non-shifted OFDM packet while the shifted OFDM packet is still being generated and shifted. Rather, all the claim requires is that the transmission of the later packet, *e.g.*, the shifted OFDM packet, only needs to start such that the transmission of the two packets is substantially simultaneous.

Therefore, for the reasons described above, the Court finds that the "generating" step **starts and ends before** "shifting" step for method Claim 1, but there is no order for the "generating" and

"shifting" limitations for apparatus Claim 8. Furthermore, the Court finds that the "transmitting" limitation **starts after the starts of, but not necessarily after the ends of,** both the "generating" and "shifting" limitations.

IV. CONCLUSION

In conclusion, for the reasons described herein, the Court adopts the below constructions as its final constructions.

SIGNED this 10th day of September, 2024.

ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE

Term	Plaintiff's Proposed Construction	Defendants' Proposed Construction	Court's Final Construction
#1: "operating the microprocessor such that each domain operates synchronously, while the domains operate asynchronously relative to one another" U.S. Patent Nos. 7,089,443, Claim 8	Plain and ordinary meaning	"synchronously" means "using the same clock with a fixed phase relationship" and "asynchronously" means "using independent clocks with no known phase relationship"	Plain-and-ordinary meaning
"generating a first OFDM packet" / "cyclically advancing the first OFDM packet . . . to generate a shifted version of the first OFDM packet" U.S. Patent No. 7,623,439, Claims 1, 8	Plain and ordinary meaning	Order of steps: "generating a first OFDM packet..." must occur before "cyclically advancing the first OFDM packet ... to generate a shifted version of the first OFDM packet"	Claim 1: "generating a first OFDM packet…" **starts and ends before** "cyclically advancing the first OFDM packet ... to generate a shifted version of the first OFDM packet"; Claim 8: No order. The "transmitting" / "transmission" **starts after the starts of, but not necessarily after the ends of,** both [1] "generating a first OFDM packet…" and [2] "cyclically advancing the first OFDM packet…"