

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,

Petitioner,

v.

ADVANCED CLUSTER SYSTEMS, INC.,

Patent Owner.

IPR2025-00915

U.S. Patent No. 11,563,621

CORRECTED PATENT OWNER RESPONSE

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PATENT OWNER’S EXHIBIT LIST

<u>Exhibit</u>	<u>Description</u>
2001	DocketNavigator Statistics for Motion Success for Stay Pending IPR (Post-Institution) for Judge Albright
2002	J. Albright Standing Order Governing Proceedings (OGP) 4.4 – Patent Cases (Jan 23, 2024)
2003	DocketNavigator Statistics for Time-to-Milestones for Judge Albright
2004	Advanced Cluster Systems, Inc. v. Intel Corporation, Amended Scheduling Order (D.I. 54)
2005	Advanced Cluster Systems, Inc. v. Advanced Micro Devices, Inc., Scheduling Order (D.I. 36)
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2008	<i>Intellectual Ventures I LLC v. TCL Elects. Holdings Ltd.</i> , No. 6:23-cv-309-ADA (W.D. Tex. Sept. 10, 2024) (D.I. 44)
2009	<i>Acquis, LLC v. Hon Hai Precision Indus Co. Ltd.</i> , No. 6:23-cv-264-ADA (W.D. Tex. May 31, 2024) (D.I. 46)
2010	<i>ParkerVision, Inc. v. MediaTek Inc. et al.</i> , No. 6:22-cv-01163-ADA (W.D. Tex. April 29, 2024)
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2012	<i>AlmondNet, Inc. v. Amazon.com, Inc., et al.</i> , No. 6:21-cv-00898-ADA (W.D. Tex. June 19, 2025)
2013	Intel Corporation’s Amended Invalidity Contention Cover Pleading (Apr. 25, 2025)
2014	[EXHIBIT NOT USED]
2015	AMD’s Preliminary Invalidity & Subject-Matter Eligibility Contentions Cover Pleading (Corrected Apr. 25, 2025)
2016	AMD’s Preliminary Invalidity Contention – Chart A-8
2017	<i>Advanced Cluster Systems, Inc. v. Intel Corporation</i> , Order Appointing Technical Advisor (D.I. 71)
2018	<i>Advanced Cluster Systems, Inc. v. Advanced Micro Devices, Inc.</i> , Order Appointing Technical Advisor (D.I. 53)
2019	FAQ: The Sustainable Data Center – More Energy Efficient AI (available at https://www.intel.com/content/www/us/en/contentdetails/791405/faq-the-sustainable-data-center-ai-usecase.html?wapkw=sustainability&DocID=791405)
2020	NVIDIA Company Overview (May 2025) (available at https://investor.nvidia.com/events-andpresentations/presentations/presentation-details/2025/Company-Overview-5-25/default.aspx)
2021	Intel Corporation’s Answer and Counterclaims to First Amended Complaint, <i>Advanced Cluster Systems, Inc. v. Intel Corporation</i> , 7:24-cv-00245-ADA (W.D. Tex. Feb. 5, 2025) (D.I. 41)
2022	Considered 02/18/2022 IDS Submitted in U.S. Patent Appln. No. 17/374,789

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<u>Exhibit</u>	<u>Description</u>
2023	Exhibit A-18 - MultiMatlab References, U.S. Patent No. 10,333,768, as listed in Defendant NVIDIA Corporation's Supplemental Invalidity Contentions in Case No. 1 :19-cv-2032-CFC, Advanced Cluster Systems, Inc., v. NVIDIA Corporation as dated August 17, 2021 in 254 pages (submitted with IDS in U.S. Patent Appln. No. 17/374,789) (ACS_0065212-0065465)
2024	<i>Advanced Cluster Systems, Inc. v. Intel Corporation</i> , Case No. 7:24-cv-00245-ADA (D.I. 79), Minute Entry Markman Hearing Proceedings Held 08/18/2025
2025	<i>VirtaMove, Corp. v. Microsoft Corp.</i> , Case No. 1:25-cv-00794-ADA (D.I. 33), Order Granting Motion to Dismiss
2026	<i>Yeti Coolers, LLC v. Waterbear Global, LLC</i> , Case No. 1:24-cv1251-ADA (D.I. 35, 35-1), Unopposed Motion to Extend Scheduling Order Deadlines and Proposed Order
2027	Intel Corporation's Third Amended Preliminary Invalidity And Subject-Matter Eligibility Contentions (Aug. 28, 2025)
2028 (New)	Patent Owner's Objections Under 37 C.F.R. § 42.64(b)(1) (Served Dec. 3, 2025)

I. INTRODUCTION

Patent Owner Advanced Cluster Systems, Inc. (“ACS”) hereby files this Response to the Petition in IPR2025-00915 challenging claims 1–30 of U.S. Patent No. 11,563,621 (“the ’621 Patent”). Petitioner contends that claims 1–3, 5–16, and 18–30 would have been obvious under pre-AIA § 103 over Menon in view of Trefethen, RS6000, and MPIref, and that claims 4 and 17 would have been obvious over the same combination further in view of POEref. The Petition’s obviousness grounds cannot withstand merits scrutiny. Institution was based on a preliminary record, with a final determination to be made on the full record developed at trial. On that full record, Petitioner cannot carry its burden to prove unpatentability by a preponderance of the evidence.

A. The ’621 Patent And The Claimed Distributed Computing Architecture

The ’621 Patent is directed to cluster computing systems that provide cluster computing functionality to high-level computing environments—particularly environments in which users express computations as mathematical expressions and that depend on interactive workflows. (Ex. 1001, 1:15–18; 11:19–58.) The patent distinguishes cluster computing from distributed systems that merely run separate jobs on separate nodes without peer-level intercommunication between nodes during computation. (Ex. 1001, 1:48–67.) In the claimed systems, cluster node modules

communicate tasks and data during computation, enabling coordinated multi-stage evaluation and result propagation across nodes. (Ex. 1001, 29:19-34:17.)

The patent's disclosed architecture includes, *inter alia*, a user interface module, cluster node modules, and single-node kernel modules. (Ex. 1001, 4:42-6:42.) The kernel modules execute program code and evaluate mathematical expressions; the cluster node modules provide peer-to-peer communications among kernel modules while those evaluations execute; and the user interface module enables users to issue instructions into the system and receive results. *Id.* The patent's figures and written description describe a peer-to-peer communication framework between nodes, in which results of mathematical expression evaluations are communicated back through the cluster node modules to the user interface module. *Id.* The claims recite that architecture by requiring, among other things, (i) peer-to-peer communication of evaluation results and (ii) an evaluation flow across multiple nodes, including task and data transmission without routing through a master node. (Ex. 1001, 29:19-34:17.)

B. The Narrow, Dispositive Issues That Control This Case

This case turns on a focused set of dispositive issues that run through every instituted ground and every challenged claim. Patent Owner herein demonstrates that Petitioner's theories depend on rewriting the prior art architectures, and relying on conclusory expert assertions rather than what the references actually teach.

First, Petitioner cannot satisfy the requirement of claim 1 that a first cluster node module is configured to receive commands from a user interface with the commands first passing through the first kernel and similar language of the claim 13 that a first cluster node module is configured to first receive first commands from a user interface.

Menon and Trefethen, do not describe the interconnections of the user interface to the disclosed MATLAB architecture, and Petitioner nor its expert can rewrite the references to disclose this structure.

Second, the prior art does not disclose a first cluster node module that is logically positioned between a user interface and the first kernel that is required by claims 2, 24 and 27. Rather, Petitioner impermissibly reads the word “logically” out of the claim language, changing the claims to recite a first cluster node module that is positioned between a user interface and the first kernel.

Third, as explained in Section IV.C, Petitioner fails to prove the “same die” structural limitation of claims 20 and 25. Those claims do not merely require multiple processors in the same node or on the same board; they require that “the first processor and the second processor reside on the same die,” which, in ordinary technical usage and under the intrinsic record, means fabricated together on a single semiconductor substrate. (Ex. 1001, 31:47–48, 32:37–38.) Petitioner’s proof on this point rests almost entirely on RS6000 documentation stating that certain SP2 nodes

used four processors “on one card” mounted in one slot. (Ex. 1007, 10–12.) Nothing in that disclosure equates a card with a die, and the same manual makes clear that the SP2 architecture uses multiple discrete processor chips per card. Petitioner then layers on generalized assertions and later multicore materials to leap from a multi-chip card to on-die integration. (Ex. 1003, ¶¶383–386, 412; Pet. 97–98, 101.) That is not contemporaneous evidence that the claimed die-level integration was disclosed or would have been implemented in the asserted timeframe. Petitioner’s attempt to bridge that gap with inference and hindsight falls well short of its burden for claims 20 and 25 and their dependents.

Beyond these core structural deficiencies, Petitioner’s grounds also fail for lack of a legally sufficient motivation to combine and reasonable expectation of success, as set forth in Section V. Petitioner’s motivation theory with respect to Menon and Trefethen reduces to the generic assertion that a POSITA would have wanted to “parallelize MATLAB more effectively” and therefore would have combined Menon, Trefethen, RS6000, MPIref, and POEref to arrive at the claimed architecture. (Pet. 23–24). That is precisely the type of high-level goal that *KSR* and its progeny caution cannot substitute for a record-based rationale tied to the specific claimed configuration.

Menon itself underscores why the combination Petitioner proposes is not the straightforward path its theories assume: the authors describe the first-generation

MultiMATLAB system (Trefethen-like) as limited, identify concrete architectural shortcomings, and present Menon as a redesign—not a simple extension—intended to overcome those limitations. (Ex. 1005, 10–11.) In that context, it is not enough for Petitioner to say that a POSITA might have tried to mix and match old and new architectures; it must show a reason to do so with a reasonable expectation of success, which is absent here. On this record, a skilled artisan would not have viewed bolting the criticized first-generation architecture back into the redesigned system as a predictable path to the claimed invention.

Relatedly, as detailed in Section VI, Menon’s treatment of the earlier architecture amounts to teaching away from the very combination Petitioner proposes. Menon does not treat Trefethen’s design as a suitable foundation for the desired high-level, interactive cluster environment; it explains that the first-generation architecture suffers from structural constraints, including tight coupling to the MATLAB interpreter and incompatibility with parallel MEX extensions, that motivated a “completely different” design. (Ex. 1005, 10–11.)

Under Federal Circuit precedent, a reference teaches away when it criticizes, discredits, or otherwise discourages the path a petitioner proposes such that a POSITA would be led in a different direction. That is exactly what happens here: Menon’s authors—who knew the earlier system best—do not describe extending that architecture to achieve the features claimed in the ’621 Patent; they explain why

that approach is inadequate and why a different architecture is needed. That discussion undermines any suggestion that a POSITA would have chosen to rely on the criticized first-generation system as the platform for implementing the claimed peer-to-peer cluster architecture.

Section VII further shows that Petitioner's expert testimony cannot cure these substantive defects. Dr. Bajaj repeatedly relies on conclusory assertions that MultiMATLAB effectively performs peer-to-peer routing, that MPI's internal queues satisfy claim-required data structures, and that on-die processor integration would have been a routine design choice, often without tying those assertions to any specific disclosure in the prior art. Conclusory expert testimony, however, is not substantial evidence and cannot carry a petitioner's burden in an IPR. Where, as here, the written references depict a master-controlled system, and cards rather than dies, the Board must credit the documents over an expert's *ipse dixit*. Petitioner is bound by the theories and citations in its Petition, and those theories do not bridge the gaps in the prior art.

Separately, as set forth in Section VIII, Petitioner's grounds also fail because Petitioner has not carried its threshold burden to establish that several of its core references qualify as printed publications under 35 U.S.C. § 311(b). As explained there, Petitioner relies on fragmentary web citations, unsponsored screenshots, and post-hoc expert assertions rather than competent evidence showing public

accessibility at the relevant time. Where a reference's status as prior art is not established, it cannot support an obviousness ground, and Petitioner's failure on this threshold issue independently defeats the affected grounds.

Finally, as outlined in Section IX, Patent Owner has preserved several evidentiary and threshold issues that provide additional, independent bases to reject or narrow Petitioner's case. Patent Owner timely objected under 37 C.F.R. § 42.64(b)(1) to foundation and authentication of Petitioner's public-accessibility evidence, and the use of unsworn or hearsay materials to establish critical facts.

In sum, when the prior art is read for what it plainly discloses—not for what Petitioner and its expert now wish it had disclosed—each of these narrow but critical issues is decided against Petitioner. Any one of them independently defeats the instituted grounds for the corresponding claims. Taken together, they show that the Petition's obviousness theories cannot withstand scrutiny on the full trial record, and that claims 1–30 of the 621 Patent should be confirmed.

C. Petitioner Cannot Meet Its Burden On Any Instituted Ground

Petitioner bears the burden to prove unpatentability by a preponderance of the evidence, and that burden never shifts. Petitioner must therefore establish that the asserted references disclose each required limitation under the proper claim constructions and that any proposed combination is supported by a legally sufficient rationale. As shown below, Petitioner's instituted grounds fail on the core limitations

addressed in Section IV: they (1) attempt to rewrite a master-controlled, interactive-process architecture into the claimed masterless, peer-to-peer task-routing system; and (2) do not prove the “same die” processor limitation. The sections that follow address each of these failures in turn, in the order that most efficiently resolves the instituted grounds.

II. PROCEDURAL BACKGROUND AND GOVERNING LEGAL STANDARDS

A. Instituted Grounds And Challenged Claims

Intel Corporation (“Petitioner”) is now the only petitioner in this proceeding. (Paper 15, 2.) The Board instituted *inter partes* review of claims 1–30 of the ’621 Patent and instituted on all asserted grounds. The instituted grounds allege that claims 1–3, 5–16, and 18–30 would have been obvious over Menon in view of Trefethen, RS6000, and MPIref, and that claims 4 and 17 would have been obvious over the same combination further in view of POEref. Patent Owner addresses the instituted grounds on the merits under the claims’ plain and ordinary meaning. (Paper 15, 11.)

B. Petitioner’s Burden Of Proof Never Shifts

Petitioner bears the burden of proving unpatentability by a preponderance of the evidence, and that burden never shifts to Patent Owner. 35 U.S.C. § 316(e); *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1375 (Fed. Cir. 2016). Accordingly, Petitioner must establish that the asserted references disclose each required

limitation under the proper constructions and that any asserted combination is supported by a legally sufficient rationale.

C. Limits On Expert Testimony And Impermissible Gap-Filling

The Board's merits determinations must rest on evidence, not conclusory expert narrative used to supply missing disclosures. Conclusory expert testimony is not substantial evidence. *TQ Delta, LLC v. Cisco Sys., Inc.*, 942 F.3d 1352, 1359–60 (Fed. Cir. 2019). And neither “common sense” nor expert intuition may be used to fill a missing claim element where the prior art is silent on the specific limitation at issue. *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362–63 (Fed. Cir. 2016). These principles apply with particular force where, as here, Petitioner's theories depend on attributing result-return and chained evaluation behaviors to prior art references that do not disclose these claimed requirements.

D. Reliance On The Existing Evidentiary Record

Patent Owner does not submit an expert declaration with this Response because it is not necessary for the Board to resolve the issues presented. The dispositive issues are resolved by the intrinsic record and the asserted references. Patent Owner's rebuttal relies on direct quotations from the references and record citations showing that Petitioner's theories depend on mischaracterizations of the references and on impermissible gap-filling.

III. CLAIM CONSTRUCTION

A. Governing Claim Construction Principles

The Board applies the *Phillips* standard. Claim terms are given their ordinary and customary meaning as understood by a POSITA at the time of the invention, in light of the intrinsic record. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–17 (Fed. Cir. 2005) (en banc). (Paper 15, 11.)

IV. PETITIONER FAILS TO ESTABLISH A *PRIMA FACIE* CASE OF OBVIOUSNESS

Petitioner advances two instituted obviousness grounds. The first ground alleges that claims 1–3, 5–16, and 18–30 of the '621 Patent would have been obvious over Menon in view of Trefethen, RS6000, and MPIref. The second ground alleges that claims 4 and 17 would have been obvious over the same combination further in view of POEref. Although Petitioner relies on multiple references, it advances a unitary theory: that MultiMATLAB (Menon/Trefethen), implemented on IBM SP hardware (RS6000), and—where applicable—augmented by MPIref and launched through IBM's parallel environment (POEref) discloses or renders obvious the '621 Patent's claimed peer-to-peer cluster computing architecture for evaluating mathematical expressions and returning results to a user interface.

Those instituted theories fail for multiple independent reasons. The sections that follow address these structural defects in the order that resolves the instituted grounds most directly.

A. Petitioner Fails to Disclose A First Cluster Node Module Configured To Receive Commands From A User Interface (Limitations [1.4.2] and [13.4.2])

Independent claim 1 requires “a first cluster node . . . configured to: receive first commands from a user interface without the first commands first passing through the first kernel” (Ex. 1001, 29:29-34.) Claim 13 recites similar language that “a first cluster node module . . . [is] configured to: first receive first commands from a user interface. . . .” (*Id.* 30:53-56.) These are not aspirational statements, they are architectural constraints that define the claimed computer cluster.

1. Menon and Trefethen Are Silent Regarding The Interconnectivity Of The User Interface MultiMATLAB Architecture

The asserted prior art does not describe the user interface flow path. Menon describes a MultiMATLAB system in which the user interacts with an interactive process. (Ex. 1005, 3.) Menon explains that “[t]he user interacts directly with one MATLAB process, called the interactive process” (*Id.*). Menon’s Figure 1 illustrates this user interaction. (*Id.*).

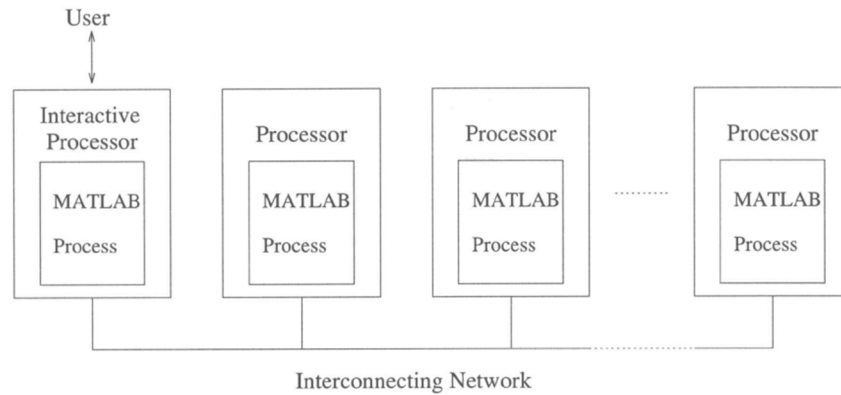


Figure 1: MultiMATLAB Architecture

Ex. 1005, Figure 1

Notably, Menon does not provide the details as to what components of the Interactive Process the user communicates. Menon's Figure 2 provides further details of the MATLAB process that is shown in its Figure 1.

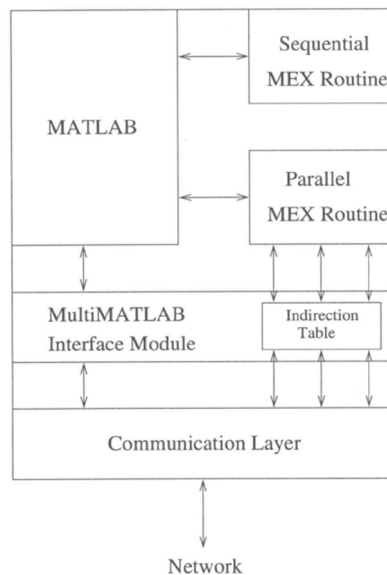


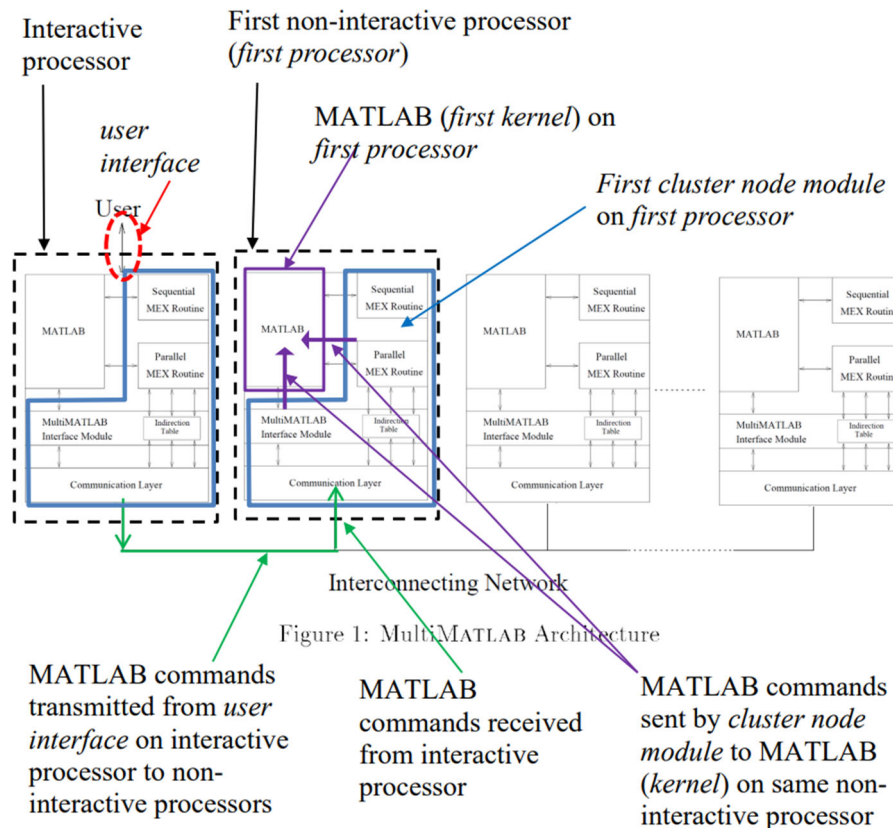
Figure 2: MATLAB Process Address Space

Ex. 1005, Figure 2

Menon's Figure 2, fails to specify any details as to the components, if any, of the MATLAB process to which the user interface is connected or with which the user communicates.

2. Petitioner's Invalidity Theory Is Hindsight Reconstruction

Faced with this gap, Petitioner generates an annotated figure based on the combination of Menon's Figures 1 and 2.



Ex.1005, FIGs. 1 and 2 (combined and annotated); Ex.1003, ¶212

In doing so, Petitioner moves the line representing communication between the user and the Interactive Processor (red circle in the Petition) to touch its annotated blue

box, that Petitioner alleges is a cluster node module on the Interactive Processor. This is not a disclosure. It is impermissible hindsight reconstruction.

Obviousness requires evidence that the prior art teaches or suggests the claimed architecture and that a POSITA would have been motivated to implement it with a reasonable expectation of success. It is not enough to show that the system could be modified to behave like the claim. See *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362–63 (Fed. Cir. 2016) (rejecting gap-filling by “common sense” where the art is silent); *In re Lee*, 277 F.3d 1338, 1343–45 (Fed. Cir. 2002) (conclusory assertions cannot substitute for evidence); *ActiveVideo Networks, Inc. v. Verizon Commc’ns, Inc.*, 694 F.3d 1312, 1327–28 (Fed. Cir. 2012) (hindsight reconstruction is insufficient).

While Menon discloses a graphical user interface (Ex. 1005, 6), Petitioner has presented no evidence that such an interface is part of the alleged cluster node module of the Interactive Processor. Trethefen does not cure Menon’s deficiencies. Trethefen discloses various commands, but like Menon fails to disclose that any of these user commands are received at the cluster node module, without first passing through the first kernel (MATLAB (Pet 34 identifying MATLAB as a kernel).)

3. Expert Testimony Cannot Rewrite Menon And Trefethen's Lack of Disclosure

Petitioner relies on expert assertions in an effort to justify its hindsight reconstruction, but expert *ipse dixit* cannot replace what the references do not disclose. Where the prior art does not describe the MATLAB architecture's user interface interconnectivity, an expert cannot simply assert that it effectively communicates with a cluster node module. The Board must evaluate what the references actually teach.

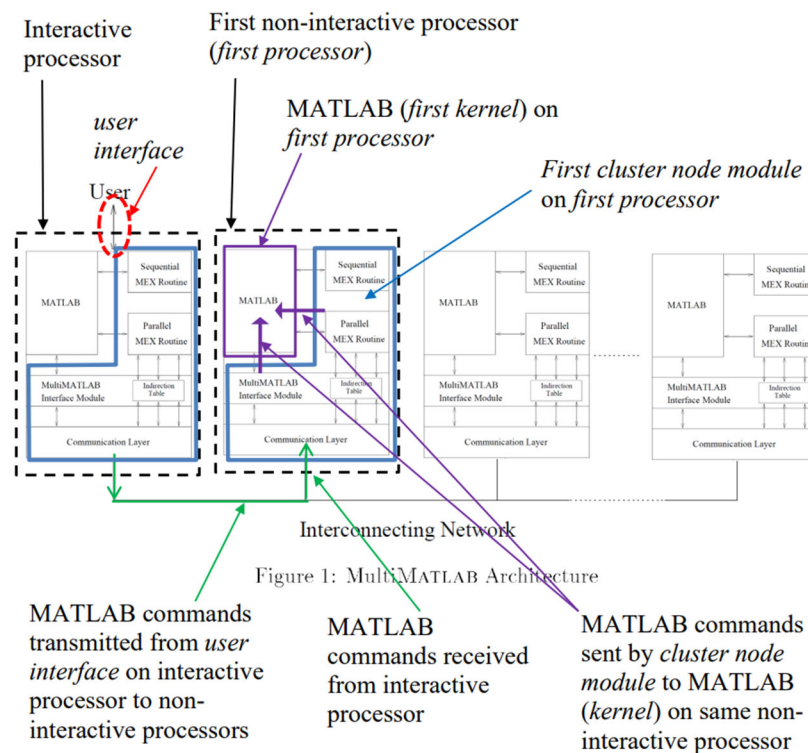
Dr. Bajaj acknowledges that Menon discloses a graphical user interface. (Ex. 1003, ¶ 209.) This graphical user interface, however, is not illustrated in Menon's Figures 1 or 2, and nothing in Menon or Trefethen disclose how any such graphical interface connects to the Interactive Processor or other components of the MATLAB process. When Dr. Bajaj asserts that a command entered by the user is received by the first cluster node module without the command first passing through the first kernel, such assertion is made without any citation to Menon or Trefethen. (Ex. 1003, ¶213; *id.* ¶359 (limitation [13.4.2] referring back to the reasoning of limitation [1.4.2].))

Petitioner has failed to show that the combination of Menon and Trefethen disclose the limitations [1.4.2] and [13.4.2] of challenged Claims 1 and 13.

B. Petitioner Fails to Disclose A First Cluster Node Module That Is Logically Positioned Between A User Interface And The First Kernel (Limitations [2.0], [24.4.3] And [27.4.3])

Dependent claim 2 and independent claims 24 and 27 require that “the first cluster node module is logically positioned between the user interface and the first kernel.” (Ex. 1001, 29:63-65; 32:7-9; 59-61.) These are architectural requirements of the claimed computer cluster.

Petitioner relies upon its generated combination of Menon’s Figures 1 and 2 for the assertion that Menon discloses this limitation. (Pet. 68, 100, 103.)



Ex.1005, FIGs. 1 and 2 (combined and annotated); Ex.1003, ¶288

Petitioner’s theory is that the annotated purple MATLAB box is a first kernel on the first non-interactive processor, and the blue box of the non-interactive

processor is the first kernel. (Pet. 68.) Through this annotated generated figure, Petitioner then alleges that the first cluster node module of the non-interactive processor is logically between the first kernel of the non-interactive processor and the user interface of the interactive processor. (*Id.*) Petitioner’s reasoning, however, ignores the entirety of the Interactive Processor. The Interactive Processor is an intermediary between the user interface and the first non-interactive processor and its components. Even assuming Petitioner’s assertion that the annotated blue box of the first non-interactive processor is a cluster node module, that cluster node module is logically positioned between the first kernel and the first Interactive Processor—not between the first kernel and the user interface.

Petitioner has failed to show that Menon discloses that “the first cluster node module is logically positioned between the user interface and the first kernel.

C. Petitioner Fails to Prove the “Same Die” Limitation ([20.0], [25.0])

Claims 20 and 25 of the ’621 Patent impose a specific structural limitation: “wherein the first processor and the second processor reside on the same die.” (Ex. 1001, 31:47–48; 32:37–38.) This language requires that two processors be integrated on a single semiconductor substrate—a single chip. It is not satisfied by processors that are merely co-located within the same node, mounted on the same card (Ex. 1007, 10 (“four ... processors mounted on one card”)), or installed in the same slot.

The distinction matters. The '621 Patent's specification differentiates among processors, processor cores, and system-level constructs such as nodes. (*See, e.g.*, Ex. 1001, 5:11–16 (explaining that each processor can contain one or more processor cores, that processor cores are generally independent microprocessors, and that more than one core can be included in a single chip package); 6:60–67 (describing computer systems in a cluster as including one or more processors); 11:33–35 (associating each kernel module with a processor corresponding to a node in the cluster).)

The specification acknowledges that computing systems may include different physical arrangements. (Ex. 1001, 5:11–16.) But, having disclosed a range of possible implementations, the patentees deliberately claimed a narrower one. A disclosure that processors are merely located on the same card, within the same node, or within the same package therefore cannot satisfy—or render obvious—the distinct, die-level integration that the claims require.

Petitioner relies on the IBM RS/6000 SP2 documentation to argue that the prior art taught multiple processors in a single cluster node. In particular, Petitioner points to language stating that certain high-performance SP2 nodes included “[f]our processors (on one card, mounted in one slot).” (Pet. 97–98; Ex. 1007.) From that disclosure, Petitioner asserts that it would have been an obvious design choice to

integrate those processors onto a single die, characterizing such integration as a routine consolidation and invoking *In re Larson*. (Pet. 98; Ex. 1003 ¶¶ 383–386.)

Petitioner’s reasoning fails. First, the RS/6000 SP2 documentation does not describe, suggest, or even contemplate two processors sharing a semiconductor die. When the manual states that four processors are “on one card, mounted in one slot,” it is describing four discrete processor chips mounted together on a circuit board to form an SMP node. Nothing in Ex. 1007 equates a “card” with a “die,” and nothing in that reference suggests fabricating multiple processors on a single silicon substrate. To the contrary, the same documentation describes scaling processor count by adding additional cards or slots (Ex. 1007, at 3 (“Tall frames ... eight drawers ... each ... divided into two slots”; “four nodes ... in a tall frame”); *id.* at 5 (node “mounted in one slot”)), reinforcing that each processor is a separate chip rather than part of a single integrated circuit.

The Petition relies on early-2000s materials describing multi-core CPUs to argue that integrating multiple processors on one die was a known design trend. (Pet. 97-98; Exs. 1050, 1051.) But those references post-date the relevant timeframe by several years and reflect technological advances that had not yet occurred in 1996–1997. In the mid-1990s, the established approach to increasing computing power was to deploy multiple discrete processors in parallel—through SMP systems or

clusters (Ex. 1007, at 1–3 (“scalable ... parallel computing”; “SMP ... nodes”))—not to integrate multiple CPUs onto a single chip.

Second, invoking *In re Larson* does not cure the defect. That case addressed a mechanical substitution in which a known multi-part assembly was replaced with a one-piece construction without introducing new functionality or technological complexity. *In re Larson*, 340 F.2d 965, 968 (CCPA 1965) (“use of a one piece construction ... merely a matter of obvious engineering choice”). Semiconductor processor integration in the 1990s is not analogous.

Combining two processors onto a single silicon die required advances in fabrication technology, integration density, thermal management, and architectural design that Menon and the RS/6000 SP2 materials do not even address, much less disclose or suggest. Treating a multi-core processor as merely a “one-piece” version of a multi-chip board collapses a significant technological leap into hindsight.

Importantly, Petitioner never supplies record evidence that the “first” and “second” processors in its asserted mapping actually reside on the same die, nor does it articulate a non-conclusory rationale—tied to the cited combination—explaining why a person of ordinary skill in the mid-1990s would have modified the RS/6000 SP2 architecture to integrate multiple processors onto a single chip with a reasonable expectation of success. Assertions that such integration was an engineering choice amount to little more than hindsight reconstruction.

At institution, that failure of proof is dispositive. Petitioner bears the burden to show, by a preponderance of the evidence, that each challenged claim limitation is taught or suggested by the asserted prior art. A card-level disclosure does not meet a die-level requirement, and later-developed multi-core technology cannot be used to supply a missing limitation in earlier references. Where, as here, the Petition relies on inference and *post hoc* reasoning rather than disclosure, it fails to establish a reasonable likelihood that claims 20 and 25 are unpatentable.

V. NO MOTIVATION TO COMBINE AND NO REASONABLE EXPECTATION OF SUCCESS

Petitioner bears the burden to prove that a POSITA would have been motivated to combine the asserted references to achieve the claimed invention and would have had a reasonable expectation of success in doing so. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007); *Procter & Gamble Co. v. Teva Pharms. USA, Inc.*, 566 F.3d 989, 994 (Fed. Cir. 2009). As shown herein, Petitioner has failed to meet this burden.

A. Petitioner Offers Only A General Goal, Not A Record-Based Motivation to Build the Claimed System

Petitioner's motivation-to-combine Menon and Trefethen argument reduces to the unremarkable proposition that researchers wanted to parallelize high-level mathematical computing environments. (Paper 15, 28) (quoting Petitioner's motivation: "because researchers had a strong desire to parallelize MATLAB") (Pet.

24). That generalized desire does not supply a reason to combine these references in the specific manner required by the claims, nor does it explain why a POSITA would have selected and implemented the particular multicore, result-return, and ordered sequence architecture recited in the claims.

Motivation must be tied to the claimed configuration, not to an abstract goal. *See KSR*, 550 U.S. at 418 (obviousness requires an articulated reason to combine to achieve the claimed invention, not hindsight). Here, Petitioner’s asserted reasons to combine do not explain how or why a POSITA would arrive at the claimed inventions, as opposed to any number of other master-controlled, node-parallel arrangements that were commonplace at the time.

B. Menon Is A Redesign, Not An Extension, Of Trefethen

Petitioner’s proposed combination treats Menon as if it were an incremental extension of Trefethen that a POSITA could merge into a predictable, unified MultiMATLAB system. (Pet. 23 (asserting Menon “builds on” the MultiMATLAB system taught by Trefethen); *id.* (asserting Menon and Trefethen “together represent a combination of prior art elements according to known methods ... to yield the predictable result” of MultiMATLAB executing MATLAB in parallel).) The Menon paper itself refutes that premise. Menon expressly distinguishes the first MultiMATLAB architecture (Trefethen) from the newer one, describing the first as “different” and identifying performance and extensibility limitations that prompted

a new design. (Ex. 1005, 14 (stating “The first MultiMATLAB architecture is different from the newer one described in this paper” and noting it was “more tightly coupled to MPICH... resulting in some performance limitations” and “does not permit extensions via parallel MEX routines”).) Thus, Menon itself explains it is an architectural replacement of Trefethen. The authors plainly did not view the original architecture as a stable platform for layering on capabilities; they viewed it as limited and therefore built a different architecture.

This matters because Petitioner’s asserted combination assumes compatibility and predictability: that one can take Trefethen’s architecture and simply layer Menon’s improvements on top, plus RS6000 hardware details and POE initialization, to arrive at the claimed peer-to-peer, ordered sequence evaluation system with multicore nodes. (Pet. 23 (asserting Menon and Trefethen “together represent a combination of prior art elements according to known methods ... to yield the predictable result” of MultiMATLAB executing MATLAB in parallel); Pet. 24-25 (asserting motivation to combine RS6000 with Menon because Menon uses the IBM SP2/RS6000 SP system); Pet. 107-08 (asserting motivation to combine POEref with Menon because Menon teaches MultiMATLAB uses POE).) That is not a “combination of prior art elements according to known methods.” Rather, Petitioner attempts to use the claims as a blueprint to redesign the prior art—precisely what obviousness law forbids.

C. Menon Identifies Fundamental Deficiencies In The Earlier Architecture

Menon explains why the earlier architecture of Trefethen was deficient. Menon states that the first architecture was more tightly coupled to a specific MPI implementation, resulting in performance limitations, and—critically—that it “does not permit extensions via parallel MEX routines.” (Ex. 1005, 14.) Menon identifies structural limits that prevented the first architecture (Trefethen) from supporting the kinds of extensions and performance that users wanted.

Petitioner’s theory requires the Board to assume that, notwithstanding Menon’s express critique of Trefethen, a POSITA would have considered it straightforward to merge or augment the older system to achieve the claimed invention. That is implausible on the record. The Menon authors who knew the first system best did not describe a path of incremental improvement; they described the need for a different architecture entirely. When the prior art itself identifies fundamental constraints that prevented extension, it undermines any claim that a POSITA would have been motivated to take the very path the art implies is not viable. *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1326–27 (Fed. Cir. 2009) (A reference that teaches away weighs against a finding of obviousness.). This is not simply relevant to teaching away (addressed separately); it also defeats Petitioner’s motivation and expectation showing. Menon says the old

design cannot support the extension, thus Petitioner cannot simultaneously claim that combining the old design (Trefethen) with other references would predictably yield the claimed architecture. This point is fatal to Petitioner's proposed combination.

D. The Proposed Combination Would Not Yield The Claimed System

Even accepting Petitioner's "desire to parallelize MATLAB" narrative, the proposed combination still would not yield the claimed system without additional inventive steps. Several independent problems remain unsolved by the cited references.

The asserted references' control model is not the claimed control model. Menon expressly describes an "interactive process" from which the other MATLAB processes "wait for commands," i.e., a master-controlled dispatch architecture, not the '621 Patent's peer-to-peer task-transmission model in which cluster node modules can transmit tasks among themselves "without transmitting the tasks through a master node" (claims 1, 13, 24) or "directly transmit" tasks (claim 27). Petitioner cannot convert MultiMATLAB's master/interactive-process dispatch into the claimed peer-to-peer architecture simply by invoking MPI's generic point-to-point capabilities; the system itself must be configured so that the claimed cluster node modules perform the inter-node task delegation recited in the '621 Patent's

claims, rather than routing all task initiation through the interactive/master process, and Menon does not describe such a configuration.

When a proposed combination would still lack multiple required elements, Petitioner cannot demonstrate reasonable expectation of success. Reasonable expectation of success is a distinct requirement; it cannot be presumed where the proposed combination still lacks multiple required elements. *In re Cyclobenzaprine Hydrochloride Extended-Release Capsule Patent Litig.*, 676 F.3d 1063, 1070–71 (Fed. Cir. 2012) (reasonable expectation of success is a separate, fact-based requirement and is not satisfied by a generalized motivation to try or by hindsight reconstruction). A POSITA cannot reasonably expect success in achieving the claimed invention from the combination Petitioner proposes when the combination, as disclosed, does not provide the necessary hardware architecture or the required result-return and ordered sequence evaluation functionality. Petitioner’s argument collapses into “a POSITA could have invented the missing parts,” which is not a substitute for proof that the claimed invention would have been obvious based on the teachings of the prior art references.

E. Petitioner’s Theory Relies On Impermissible Hindsight

Petitioner’s motivation and expectation narrative is built on hindsight. It starts with the claim requirements and then constructs a pathway through disparate statements in the references to say the system could be made to behave that way. But

the contemporaneous record does not show that pathway. It shows the opposite: Trefethen's first-generation MultiMATLAB had architectural limitations; Menon redesigned it; the claimed features remain absent from both; and Petitioner then impermissibly fills those disclosure gaps with using the claims as the guide.

The Federal Circuit has repeatedly cautioned that obviousness analysis cannot be driven by the inventor's disclosure. *Intercontinental Great Brands LLC v. Kellogg N. Am. Co.*, 869 F.3d 1336, 1349–50 (Fed. Cir. 2017) (improper to use hindsight and treat the patent as a roadmap for selecting and combining prior art); *In re Dembiczak*, 175 F.3d 994, 999 (Fed. Cir. 1999) (warning against hindsight reconstruction using the inventor's disclosure as a blueprint). A petitioner must identify record-based reasons why a skilled artisan would have been led to the claimed invention and would have had a reasonable expectation of success. Here, Petitioner's asserted motivation is essentially a generalized desire to parallelize high-level computing environments. (Pet. 24 (asserting "researchers had a strong desire to parallelize MATLAB" as motivation to combine Menon and Trefethen).) That desire does not supply a reason to combine these particular references in this particular way to achieve the claimed architecture, especially where the references themselves criticize the earlier design and do not disclose the missing elements. Nor does it supply a reasonable expectation that the combination would succeed in producing the claimed multicore peer-to-peer ordered sequence evaluation system.

Petitioner's theory therefore rests on impermissible hindsight, and the Board should reject it on that basis as an independent ground for denying unpatentability.

For these reasons, Petitioner has not met its burden to establish motivation to combine or reasonable expectation of success for any instituted ground.

VI. MENON TEACHES AWAY FROM PETITIONER'S PROPOSED COMBINATIONS

Petitioner's combination theory is undermined by the prior art itself. A reference teaches away when it criticizes, discredits, or otherwise discourages the path Petitioner proposes such that a POSITA would be led in a different direction. *In re Gurley*, 27 F.3d 551, 553 (Fed. Cir. 1994); *DePuy Spine*, 567 F.3d at 1326. That is precisely the situation here. Menon does not present Trefethen's first-generation MultiMATLAB work as a stable platform to extend; it presents it as an architecture with meaningful limitations that required a different approach. (Ex. 1005, 14 (stating "the first MultiMATLAB architecture is different from the newer one," was "more tightly coupled to MPICH ... resulting in some performance limitations," could not use vendor-optimized MPI implementations, and "does not permit extensions via parallel MEX routines").) Petitioner's theory nevertheless treats Trefethen's first-generation system as a foundational building block and urges the Board to accept that one would have simply combined Trefethen's earlier

architecture with Menon’s later work (and other IBM materials) to reach the claimed invention. Menon teaches away from that combination.

A. Express Criticism Of The First-Generation MultiMATLAB Architecture

Menon is explicit: “The first MultiMATLAB architecture is different from the newer one described in this paper.” (Ex. 1005, 14.) Menon then explains why. It states that the first system was tightly coupled to a particular MPI implementation, resulting in performance limitations, and that it could not take advantage of vendor-optimized MPI implementations. *Id.* Menon further identifies that the earlier architecture was not designed to support later, desired extensions. *Id.* Menon expressly states that Trefethen’s first-generation architecture as inadequate for the objectives that motivated the newer design.

Plainly this is not an invitation to combine first- and second-generation architectures. The earlier approach had structural constraints that prompted the Menon authors to move away from it. Where the authors of a reference describe an earlier system as limited and emphasize that their newer system is architecturally different to address those limitations, the reference is discouraging reliance on the earlier system as a platform for the very improvements the newer system enables. *DePuy Spine*, 567 F.3d at 1326–27 (teaching away where a POSITA would be discouraged from the proposed approach, undermining obviousness); *In re Gurley*,

27 F.3d at 553 (teaching away when the reference suggests the proposed path is undesirable or unlikely to work). That is teaching away in the straightforward sense: the reference tells the skilled artisan that the earlier path is not the path to the desired result.

Petitioner's combination theory depends on the opposite premise: that the earlier architecture is a viable foundation on which to build, and that a POSITA would naturally rely upon it with other disclosures to reach a peer-to-peer, ordered sequence evaluation system with multicore hardware. Menon's critique makes that premise untenable. If Trefethen's first system was architecturally constrained in the ways Menon describes, a POSITA would understand that the "obvious" direction was to adopt the newer architecture and abandon the earlier one.

B. Incompatibility With Parallel MEX Extensions

Menon's most pointed teaching-away statement is directed to extensibility: the first MultiMATLAB architecture "does not permit extensions via parallel MEX routines." (Ex. 1005, 14.) It is difficult to imagine clearer teaching away language in a technical paper. The Menon authors plainly state that the earlier Trefethen system is not compatible with a class of extensions that were important enough to be featured as a primary advantage of the newer system.

Petitioner's obviousness story is built around combining references to supply missing functionality. Petitioner's approach requires the Board to assume that, even

if the earlier system did not originally have certain capabilities, a POSITA would have found it straightforward to add them using later-developed concepts and tools. Menon says the opposite: the architecture itself does not permit such extensions. When a reference teaches that a specific approach cannot support a desired extension, it discourages a POSITA from pursuing that approach to achieve that extension. *DePuy Spine*, 567 F.3d at 1326.

Petitioner may argue that Menon's statement is limited to parallel MEX routines and not to other features. But that argument misses the point. Parallel MEX extensibility is but one concrete example Menon gives that the first architecture was not a reliable foundational architecture.

C. Teaching Away Undermines Any Motivation To Combine

Teaching away is not merely an additional argument; it directly undermines Petitioner's required motivation-to-combine showing. An obviousness theory premised on combining references must be supported by a reason why a POSITA would have pursued the combination with a reasonable expectation of success. Where the prior art discourages the path, that reason is missing. *In re Gurley*, 27 F.3d at 553. Here, Menon's critique of the first architecture and its explicit statement that Trefethen's earlier system does not permit the relevant extensions makes it unreasonable to conclude that a POSITA would have been motivated to use the first-generation architecture as a basis for achieving the claimed invention.

This teaching away is especially significant in this case because the references at issue are not unrelated; they are sequential works by related authors on the same project. The authors had every incentive to reuse their earlier work if a straightforward upgrade path existed. Instead, Menon describes the new architecture as different and identifies limitations that the earlier architecture could not overcome. That contemporaneous evidence—coming from the project’s own developers—strongly supports Patent Owner’s position that the path Petitioner proposes is not the path the prior art taught. It also reinforces the lack of reasonable expectation of success discussed in Section V: when the designers of the system themselves state that certain extensions are not permitted by the first architecture, it is not credible for Petitioner to argue that a POSITA would have expected to achieve the patent’s more demanding architectural requirements by combining the earlier and later references.

Accordingly, Menon’s teaching away provides an independent and compelling reason to reject Petitioner’s proposed combinations.

VII. PETITIONER’S EXPERT TESTIMONY CANNOT CURE MISSING CLAIM LIMITATIONS

Petitioner’s instituted grounds depend on using expert narrative to supply what the asserted references do not disclose. That approach is legally insufficient. The Board’s final written decision must rest on what the prior art actually teaches

and on a supported rationale for combination—not on conclusory expert assertions that rewrite the references or fill gaps by hypothesis. In this proceeding, Petitioner bears the burden of persuasion throughout. 35 U.S.C. § 316(e); *Magnum Oil Tools*, 829 F.3d at 1375. Petitioner cannot meet that burden by asking the Board to accept Dr. Bajaj’s conclusions in lieu of documentary proof of claim limitations. Where a claim limitation is missing from the asserted references, expert testimony cannot manufacture it. *Arendi S.A.R.L.*, 832 F.3d at 1362–63 (common sense and expert intuition cannot fill gaps where the prior art is silent).

This proceeding illustrates those principles in a straightforward way. Petitioner’s obviousness case for the ’621 Patent’s claims rests at critical points on expert *ipse dixit*—most notably in asserting that MultiMATLAB allegedly implements peer-to-peer task transmission without a master node—without pointing to actual disclosures in Menon, Trefethen, RS6000, or MPIref that describe the claimed ’621 Patent’s control and task-routing model. (Ex. 1001, 29:56–59; 31:11–14; 32:30–33, 33:15-17.) As explained above, Petitioner’s expert’s assertions either lack support in the cited references or are inconsistent with their express description of an interactive/master process that issues Eval () commands to worker processes, and they therefore cannot satisfy Petitioner’s burden to prove unpatentability of the challenged ’621 Patent claims .

A. Conclusory Assertions Are Not Substantial Evidence

An expert's opinion is not self-proving. PTAB decisions must be supported by substantial evidence, and conclusory expert testimony—unsupported by underlying facts in the cited references—is not substantial evidence. *TQ Delta*, 942 F.3d at 1359–60. The Board's rules reflect the same principle: “[e]xpert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.” 37 C.F.R. § 42.65(a).

Here, Dr. Bajaj repeatedly attempts to supply critical claim limitations by unsupported assertion. Petitioner's obviousness case depends at key points on expert *ipse dixit*—most notably in asserting that the MultiMATLAB prior art references allegedly implement the claimed user-interface-to-cluster-node control path (in which the user interface sends commands to a first cluster node module without those commands passing through the first kernel) and the claimed peer-to-peer task-transmission architecture (requiring that cluster node modules transmit tasks to one another without routing tasks through a master node). Petitioner identifies no disclosure in Menon, Trefethen, RS6000, or MPIref that describes this specific control and task-routing model. (Ex. 1003 ¶¶ 69–74, 169–175, 261–273; Pet. 22–27, 58–64.) Those mappings either lack support in the cited references or conflict with the express description of a master-controlled interactive MATLAB process in which other processes wait for commands issued by the interactive process. (Ex.

1005, 3, 6; Ex. 1006, 3–6; Ex. 1003 ¶¶ 69–74, 215–220.) As a result, Petitioner’s expert assertions cannot satisfy Petitioner’s burden to prove unpatentability of the challenged claims by a preponderance of the evidence.

Federal Circuit precedent does not allow such patching. *Magnum Oil Tools* makes clear that a petitioner cannot satisfy its burden with conclusory assertions; the petitioner must affirmatively prove unpatentability with evidence and reasoned explanation. 829 F.3d at 1380–81. Petitioner’s reliance on expert *ipse dixit* is thus legally inadequate. Where the references are silent or inconsistent with the expert’s narrative, Petitioner has not met its burden.

B. Conflicts with the Written Record Must Be Resolved Against Petitioner

When expert testimony conflicts with the plain disclosure of a prior art reference, the reference controls. The Board errs by crediting expert opinion that contradicts or fills gaps in what the reference actually teaches. *In re Lee*, 277 F.3d at 1343–45. That principle is particularly important in IPR proceedings, where the Board’s task is to determine what the prior art discloses based on record evidence, not to accept conclusory expert assertions untethered from the cited references. *See also Arendi S.A.R.L.*, 832 F.3d at 1362–63.

Petitioner’s expert-driven theories collide with the written record at every turn on the core limitations addressed in Section IV. On peer-to-peer task transmission,

Petitioner and Dr. Bajaj ask the Board to treat MultiMATLAB’s master-driven Eval () dispatch as if it were a masterless, worker-initiated routing scheme, even though Menon describes a user who “interacts directly with” an “interactive process” and states that the other processes “wait for commands” from that interactive process. (Ex. 1005, 3, 6; Pet. 41–42, 110; Ex. 1003 ¶¶ 69–74.) Trefethen similarly frames execution in terms of user-entered Eval commands sent to other processes. (Ex. 1006, 3.)

On the “same die” limitation, Petitioner relies on expert inference rather than disclosure, with Dr. Bajaj asserting that RS6000’s disclosure of multiple processors mounted on a single card satisfies the claim requirement that two processors reside on the same die, and further invoking later multicore developments to bridge the gap. (Pet. 96–97; Ex. 1003 ¶¶ 383–386.) But the contemporaneous RS6000 documentation describes multiple discrete processor chips mounted on a card, not two processors fabricated on a single die, and nowhere suggests such on-die integration. (Ex. 1007, 11–12.)

In each instance, the expert narrative seeks to rewrite architectures and data structures that the prior art expressly describes in different, more limited terms. Under Federal Circuit precedent and 37 C.F.R. § 42.65(a), the Board should credit the actual disclosures in Menon, Trefethen, RS6000, and MPIref over these

hindsight reconstructions and treat the gaps in the prior art as genuine failures of proof, not opportunities for expert *ipse dixit* to fill in missing limitations.

The Board should therefore resolve such conflicts against Petitioner and reject any mapping that depends on contradicting the references.

C. Petitioner Is Bound by the Theories in the Petition

Petitioner must stand or fall on the theories it advanced in the Petition. It may not use reply briefing or post-institution argument to introduce new rationales or new combinations to cure deficiencies in its original case. *Magnum Oil Tools*, 829 F.3d at 1381 (rejecting attempts to shift burden or introduce new arguments to patch the petition); *see also*, 37 C.F.R. § 42.23(b) (reply may respond only to arguments raised in the corresponding opposition/patent owner response).

This principle is critical here because Petitioner's instituted ground has identifiable, dispositive proof failures. Petitioner's mapping of the return and chained-evaluation limitations relies on Menon's interactive process and Trefethen's scripts/output, supplemented by Dr. Bajaj's characterizations. If that mapping fails on the merits—as it does—Petitioner cannot salvage the case by pivoting to a new interpretation of Eval () returning results, or a new explanation of how the three-node chain is disclosed elsewhere. Those would be new theories and would improperly expand the petition. Petitioner's burden is to prove unpatentability based on the instituted case, and that instituted case cannot be repaired by a moving target.

Accordingly, the Board should evaluate Petitioner’s ground based on the asserted evidence and the petition’s own mappings. When that is done, the conclusion follows: Petitioner’s expert testimony cannot cure missing claim limitations, cannot contradict the written record, and cannot substitute for the disclosures that Petitioner was required to prove.

VIII. THE CITED REFERENCES ARE NOT “PRINTED PUBLICATIONS”

Petitioner bears the burden to prove that “Menon” (Ex.1005), “Trefethen” (Ex.1006), “RS/6000” (Ex.1007), “POEref” (Ex.1008), and “MPIref” (Ex.1017) qualify as a “printed publication.” To qualify, a reference must be “disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art, exercising reasonable diligence, can locate it.” *Kyocera Wireless Corp. v. Int’l Trade Comm’n*, 545 F.3d 1340, 1350 (Fed. Cir. 2008); *In re Lister*, 583 F.3d 1307, 1311 (Fed. Cir. 2009). Competent evidence is required. *Medtronic, Inc. v. Barry*, 891 F.3d 1368, 1380 (Fed. Cir. 2018); *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1348–51 (Fed. Cir. 2016). Because Petitioner has not proven public accessibility, none of its references qualifies as prior art, and all grounds fail.

A. IBM Technical Manuals (RS/6000 and POEref, Exs. 1007–1008)

Petitioner asserts that the IBM manuals were indexed in IBM’s online library by 2001–2002 and thus qualify as printed publications. But Petitioner offers no

evidence that the manuals were ever publicly accessible. At most, they were hosted on an IBM repository. Petitioner must show that interested researchers could have found them through reasonable diligence. *Samsung Elecs. Co. v. Infobridge Pte. Ltd.*, 929 F.3d 1363, 1369 (Fed. Cir. 2019). Yet Petitioner provides no evidence that a POSITA using typical search methods at the time could have located them.

The Petition cites printouts of IBM webpage “link chains” (Exs.1038, 1039) and an Internet Archive timestamp (Ex.1029) to suggest the manuals were hosted on IBM’s website by 2001. But these printouts do not show how the public could have navigated to the manuals. There is no evidence of any IBM webpage from that time listing the manuals or allowing users to search for them by topic.

Dr. Bajaj did not base his conclusions on any evidence that the manuals were indexed or searchable on IBM’s website, and the record includes none. (Ex. 1003 ¶¶130, 134-135.) At most, the manuals might have been accessible to someone who knew the exact URL—not “sufficiently accessible to the public interested in the art.” *In re Cronyn*, 890 F.2d 1158, 1161 (Fed. Cir. 1989). Petitioner cites no evidence that anyone ever accessed or even knew of the manuals before the critical date. Their mere presence on an IBM server is like the unindexed thesis in *Cronyn*—public-facing, but undiscoverable. *See also Blue Calypso*, 815 F.3d at 1348.

Petitioner’s evidence shows the manuals were on IBM’s server by 2005, but not that they were searchable via internet engines. Although Petitioner notes the

manuals shipped with RS/6000/SP2 systems, distribution to customers or user groups is not public accessibility without evidence they reached non-customers. *Medtronic*, 891 F.3d at 1380. Nothing shows the manuals were disseminated beyond IBM's customer base or made available in libraries or public forums.

B. MPI Forum Draft Standard (“MPIref,” Ex. 1017)

Petitioner contends that Exhibit 1017 (“MPIref”) was distributed via FTP servers and posted on the MPI Forum's website in 1994, and thus qualifies as a printed publication. But Petitioner's evidence does not show actual public accessibility. It cites only language within the draft stating it was “processed by LaTeX on May 4, 1994” and “made available” by the working group—statements in past tense, embedded in the document, and uncorroborated. Such assertions, without evidence of indexing, searchability, or public dissemination, are insufficient. *In re Klopfenstein*, 380 F.3d 1345, 1350 (Fed. Cir. 2004).

Petitioner also relies on Dr. Bajaj, who asserts that the MPI draft was available via an FTP “mail server” and linked from certain websites. See Ex. 1003 ¶¶140-142. But Petitioner offers no evidence that anyone outside the MPI Forum ever knew of or accessed the draft. There is no contemporaneous documentation—no listserv announcement or public notice—and Dr. Bajaj does not claim he or anyone else retrieved it. The cited web link does not yield the document. At most, Petitioner shows possible access by insiders, not public accessibility. Courts and the Board

have held that distribution to a closed group or those already aware of the work is insufficient. *Samsung Elecs. Co. v. Infobridge Pte. Ltd.*, 929 F.3d 1363, 1374–75 (Fed. Cir. 2019); *Argentum Pharm. LLC v. Research Corp. Techs.*, IPR2016-00204, Paper 19 at 11–12 (PTAB May 23, 2016).

C. Cornell “MultiMATLAB” Web Article (“Trefethen,” Ex. 1006)

Petitioner alleges that Trefethen (Ex. 1006) was publicly accessible via a Cornell University webpage and that one of the authors linked to it from a personal homepage. (Petition at 15; Ex. 1003 ¶¶127-128.) But Petitioner offers no competent evidence that such a hyperlink existed or that anyone actually found the page in the 1990s. (Ex. 1023.) The record contains no proof of indexing, public discoverability, or that the site was accessed by any member of the public.

First, the archived evidence contradicts Petitioner’s story of an author’s webpage hyperlink. The very webpage that was supposed to be the gateway to Trefethen does not actually reference or link to the article. At best, one would have needed to know the exact URL to load the page – which is not public accessibility unless that URL was advertised or indexed somewhere.

Second, even if Trefethen resided on a Cornell server in 1996, Petitioner offers no evidence that anyone knew of it or could find it. “Public accessibility requires more than technical accessibility.” *Samsung Elecs. Co. v. Infobridge Pte. Ltd.*, 929 F.3d 1363, 1369 (Fed. Cir. 2019). Petitioner cites no search index, library, or

database that cataloged Trefethen, nor any proof that Cornell’s computer science pages were indexed or publicly visible in the 1990s. The record contains no evidence that the department or author webpages were discoverable by a POSITA. Cornell’s popularity is not evidence that Trefethen was publicly available.

Third, it is undisputed that before the June 2006 critical date, Trefethen had not been formally published in any journal or conference, nor is there evidence it was available in libraries. Petitioner relies entirely on alleged web availability. But posting a document on a personal website does not make it a printed publication unless the site was publicly known or indexed. *Blue Calypso*, 815 F.3d at 1349 (Fed. Cir. 2016). Petitioner cites no evidence that anyone would have known of Ms. Trefethen’s personal page or located the article on Cornell’s server.

Finally, Petitioner’s claim that Trefethen was “cited 10 times” before the relevant date does not establish public accessibility. (Petition at 15; Ex. 1003 ¶127; Ex. 1035 at 2–3.) Citation alone does not prove that the public could locate the document. Indeed, one such citation appears in the Menon paper itself (Ex. 1005 at 1–2)—an instance of self-citation, not evidence of dissemination.

D. SC’97 Conference Paper (“Menon,” Ex. 1005)

Unlike the other references, Exhibit 1005 (“Menon”) was part of a known academic conference. Petitioner argues that Menon “was published and distributed at the Proceedings of the 1997 ACM/IEEE Conference on Supercomputing” and

thus is a printed publication. Petition at 14 (citing Ex. 1005; Ex. 1027 ¶ 11.) Petitioner further notes that Menon later became available on Cornell’s website by 2003 and was cited by numerous subsequent papers. *Id.*; Ex. 1003 ¶¶121-123; Ex. 1028.

First, however, Petitioner has not proven that the SC’97 conference proceedings (including Menon) were actually disseminated to the public in 1997. Petitioner relies heavily on the declaration of Gordon MacPherson, an IEEE publications custodian (Ex. 1027), who stated that copies of the SC’97 proceedings “were made available no later than the last day of the conference.” But MacPherson does not explain how or to whom the proceedings were distributed. Moreover, MacPherson provides no foundation for his knowledge. He does not claim to have been present at SC’97, nor to have personally overseen distribution of the proceedings. He provides no supporting documentation or contemporaneous evidence to corroborate his statement. Aside from his bare assertion, there is nothing in the record to indicate that anyone actually obtained Menon during or shortly after the SC’97 conference.

Notably, MacPherson’s declaration references an attached “Exhibit A”—purportedly a copy of Menon retrieved from IEEE Xplore in March 2025—and claims that the IEEE Xplore entry “show[s] the date of publication.” (Ex. 1027 ¶ 10.) But upon inspection, “Exhibit A” (Ex. 1027 at 3–21) does not display any

publication date for Menon. Petitioner did not provide the IEEE Xplore abstract or bibliographic metadata page, so the supposed evidence of publication date is missing from the record. As a result, MacPherson's assertion that IEEE Xplore confirms a 1997 publication date is uncorroborated.

Apart from IEEE's internal records, Petitioner suggests that Menon was available through other channels: a Cornell website and the Supercomputing '97 conference website. (Petition at 14–15; Ex. 1003 ¶¶121-122.) But Petitioner offers no evidence that the Menon PDF was indexed or that anyone actually located it on Cornell's site within the relevant timeframe. (Ex. 1029 (archived Cornell webpage lacking indexing metadata or navigable links)). As for the SC'97 website, Petitioner's expert merely suggested that conference papers could have been accessible there, but submitted no evidence that the site actually hosted full papers for public download or that it was indexed or known to the broader community. (Ex. 1003 ¶121.) Moreover, Exhibits 1030 and 1031 relate to the conference, but do not identify any URL for a SC'97 webpage where Menon was allegedly available. Petitioner has failed to show that any member of the public—who did not attend SC'97—could have found or accessed the Menon paper.

Even if Menon eventually became publicly available, the question is when and how it became available, and whether that meets the legal standard for a printed publication. *See Medtronic*, 891 F.3d at 1380. Petitioner must prove that Menon

entered the public domain no later than the critical date and has failed to do so. As a result, Petitioner fails to meet its burden, and all grounds relying on Menon fail.

E. Petitioner's Citation-Based Arguments Will Be Addressed Separately

In an attempt to patch the holes in its public accessibility showing, Petitioner points to lists of other publications that cite the Menon, Trefethen, and MPIref references (Exhibits 1028, 1035, and 1037). Petitioner invites the Board to infer that, because certain papers (published before 2006) have bibliographic citations to these references, the references must have been publicly available. That argument raises both evidentiary and substantive issues, including whether the cited references correspond to the asserted exhibits and whether they were publicly accessible at the relevant time. Patent Owner will address those issues in a forthcoming motion to exclude.

IX. PRESERVED EVIDENTIARY ISSUES

Patent Owner preserves its objections regarding the foundation for Petitioner's public-accessibility evidence. (Ex. 2028 at 2-4.)

X. CONCLUSION

For all these reasons, Petitioner has not met its burden to prove unpatentability by a preponderance of the evidence. The asserted prior art does not disclose or suggest the limitations required by independent claims 1, 13, 24, and 27, dependent claim 2, and the "same die" processor integration of claims 20 and 25.

Petitioner attempts to supply these missing limitations through expert narrative, but expert *ipse dixit* and hindsight reasoning cannot replace what Menon, Trefethen, RS6000, and MPIref actually disclose.

Nor has Petitioner carried its distinct burden to show a record-based motivation to combine these references with a reasonable expectation of success; Menon's own critique of the first-generation MultiMATLAB architecture teaches away from using that system as the very foundation for the claimed architecture, and confirms that the straightforward path was to abandon, not extend, the earlier design.

Petitioner also has not carried its threshold burdens on the record to establish that its key references qualify as printed publications and to support critical public-accessibility facts with competent evidence. Where a reference's prior-art status is not proven, it cannot sustain an obviousness ground, and where Petitioner's evidentiary showing rests on unsupported or inadmissible materials, it cannot satisfy Petitioner's burden of proof. These independent defects further confirm that Petitioner has not proven unpatentability of any challenged claim.

On this evidentiary record, the Board should confirm claims 1–30 of the '621 Patent.

IPR2025-00915 CORRECTED PATENT OWNER RESPONSE
Inter Partes Review of U.S. Patent 11,563,621

Dated: February 6, 2026

Respectfully submitted,

/David P. Lindner/

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CERTIFICATE OF TYPE-VOLUME LIMITATIONS

Pursuant to 37 C.F.R. § 42.24(d), Patent Owner certifies that this Patent Owner Response complies with the type-volume limits of 37 C.F.R. § 42.24 because it contains 9,725 words, according to the word-processing system used to prepare this brief, excluding the parts exempted by 37 C.F.R. § 42.24.

Dated: February 6, 2026

Respectfully submitted,

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), the undersigned certifies that I caused a true and correct copy of the foregoing Corrected Patent Owner Response to be served in its entirety on February 6, 2026, by filing this document through the U.S. Patent Office's P-TACTS Filing System, as well as causing true and correct copies be delivered by electronic mail on Petitioner's lead and backup counsel at the following email addresses of record:

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