IBM RS/6000

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By

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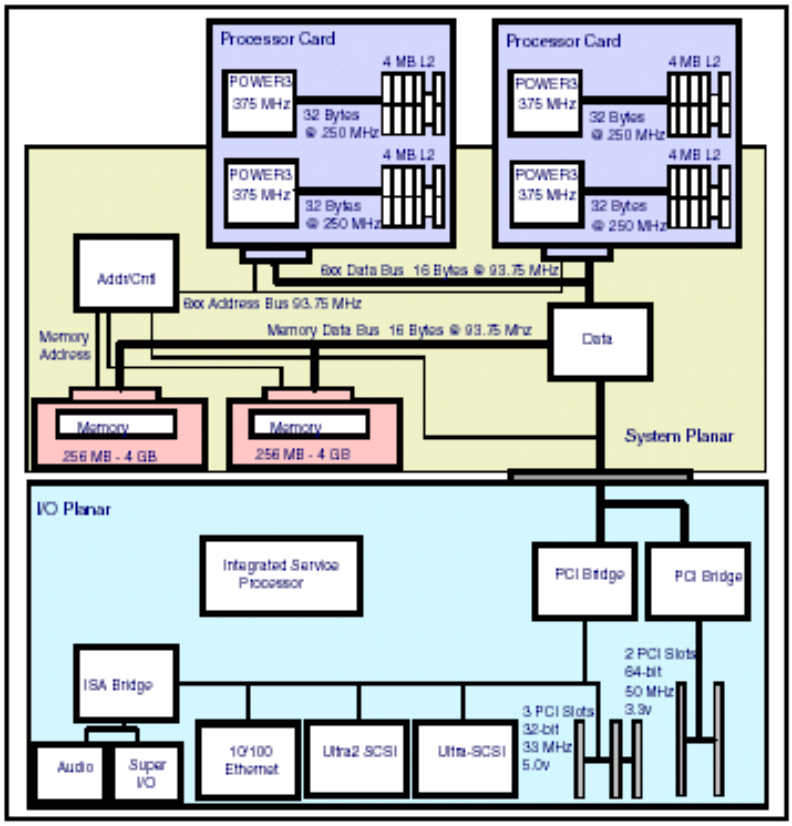
IBM first announced the RS/6000 in February 1990. This is a family of super scalar workstations and servers based upon IBM's POWER (Performance Optimized With Enhanced RISC) architecture. When the RS/6000 fist came out the I/O buses were based on the Micro Channel Architecture. They have since moved to using Peripheral Component Interface (PCI) Architecture. IBM introduced the POWER 2 in 1993, which led to several improvements. I'm going to focus on the POWER 3 because of the level of information that I found on it. The POWER3 was designed with room for growth and is made for high performance and visual computing applications. IBM expects to be able to use it for the next 3 generations of RS/6000 processors. As of 2000, over 1.1 million systems in the RS/6000 family had been shipped. The picture below shows the general system block layout.



As you can see in the in the diagram above, you can have several processors in the machine. The POWER3 can have up to 8 375MHz processors. Each processor has it's own L2 cache of 4 MB and shares up to 8 GB of ram. The PCI architecture has a limit on the number of slots (adapters) that it can support. The POWER3 comes with 2 PCI bridges, one to support 64-bit 50 MHz slots and one to support 32-bit 33MHz slots. It also has SCSI and Ethernet controllers built in and an ISA bridge to

support audio and Super I/O. The POWER3 is designed to allow concurrent operation of floating-point instructions, Load/store instructions, branch instructions, and fixed-point instructions. The features of the POWER3 that exceed its predecessor are a second load-store unit, improved memory access speed, and speculative execution.

The diagram of the logical block is below. It is targeting a clock frequency of up to 600 MHz. This is made possible by more advanced chip manufacturing and the use of copper technology. The specifications for the POWER3 include a superscalar design with integrated integer, floating-point and branch units. Also 32kb of instruction cache and 64kb 128-way set associative data cache. Other specifications are having 15 million transistors and real memory support for up to 4GB.

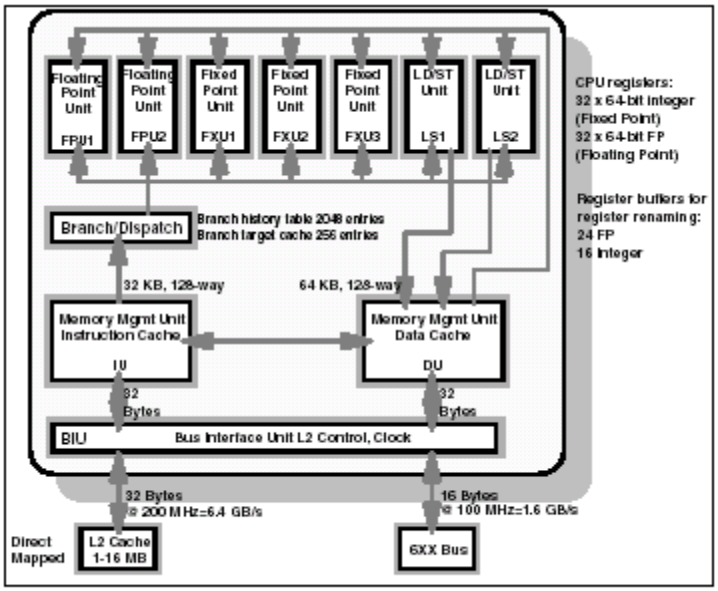


Figure 6. POWER3 Microprocessor Logical Block Diagram

It uses 64-bit technology, but can also run 32-bit applications. Some advantages to using 64-bit computer include large file support and the ability to support very large memory. You can also have large applications with the use of virtual address support. With the large file support it can address programs over 2GB in size. The table below is the only memory map that I could find for the RS/6000. This is based off of the AIX operating system. AS you can see it show support for both the 32-bit and the 64-bit programs. 64-bit computing expands addressibility, addressibility creates potential for higher capacity, and a balanced 64-bit system design will realize the potential by delivering higher system performance

Figure 1. AIX 4.3 Virtual Address Space Layout				
		Size	**64-bit Address Space**	**32-bit Address Space**
1 Million TB X *Above 4 GB*		64,000 TB	Program stack	N/A
		384,000 TB	Reserved	
		64,000 TB	Shared library text & data	
		64,000 TB	Privately loaded programs	
		64,000 TB	Shared objects (default)	
		384,000 TB	Program text & data	
Below 4GB (Segment #)	15	256 MB	Reserved	Shared library data
	14	256 MB	Available to application	Available to application
	13	256 MB	Shared library information	Shared library text
	3-12	2.56 GB	Available to application	Available to application
	2	256 MB	Available to application	Program data & stack
	1	256 MB	Available to application	Program text
	0	256 MB	Kernel	Kernel

An interesting command I found lets you switch from one to the other so the computer would expect little-endian or big-endian. I could not find out which one the computer preferred in its normal form. The commands are –mlittle-endian and –mbig-endian.

The POWER3 is capable of executing up to 8 instructions per cycle at its peak rate. Two floating-point, two load/store, two single-cycle integer, a multi-cycle integer, and a branch instruction are the operations it can do at once. It does all this even though its 64kb data cache is only half the size of its predecessor. It has an advanced core, a dedicated L2 cache and a aggressive prefetching mechanism that improves the memory access speed.

The memory sizes on this computer can go from big to huge. The L2 cache maybe from scaled from 1 MB to 16MB. The RAM may be from 512MB to 8GB. And hard drives run from 18.2GB to 587.2GB on the 610 model 6C1. The registers are 64-bits,

but in the information that I could find, even calling IBM, I could not find out how many registers that it has.

The POWER3 is a 64-bit PowerPC implementation with a 32-bit backside L2 cache interface. The 64-bit address space in L2 cache is actually manages by an 80-bit virtual addresses and 40-bit real memory addresses which will support 1 terabyte. The level-one cache L1 is an efficient interleaved cache capable of two loads; one store and one cache line reload per cycle.

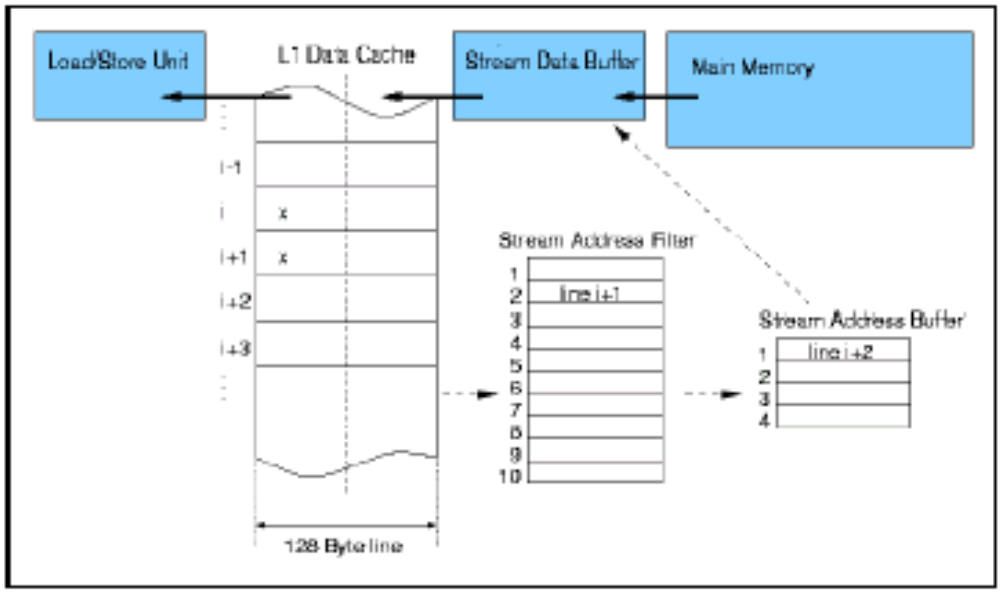


Figure 2. Data Prefetch Overview

Some improvements that have been made over the previous models include increased clock speed, and dedicated integer and load/store units. Other improvements are a peak execution rate of 8 instructions per cycle and cache improvements including L2 cache. In next generation, the POWER3-II, IBM plans to increase clock frequency by 50% by tuning and moving to copper technology. In the POWER3-III IBM plans to increase the clock speed by 40% over the POWER3-II by tuning and moving to IBM's Silicon on Insulator (SOI) technology. Other advancements include moving from 8 to 16 CPU's and a gigabyte internal switch network

In Conclusion, The IBM RS/6000 is a awesome line of computers. The multiple processors and the ability to have to vast amount of scalable memory almost blows my mind. But this is a business computer or a web server, not something you have in you room. The architecture is well planned and IBM has a destination for the future. I think that this line will be around for a while to come.

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