

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

ADVANCED CLUSTER SYSTEMS, INC.,
Patent Owner.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

Record of Oral Hearing
Held: August 13, 2026

Before: KARL D. EASTHOM, ARTHUR M. PESLAK,
SCOTT RAEVSKY, and
BRIAN P. MURPHY, *Administrative Patent Judges*.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

APPEARANCES:

ON BEHALF OF THE PETITIONER:

ANDREW S. EHMKE, ESQ.
DANIEL SMITH, ESQ.
Haynes Boone, LLP
6000 Headquarters Drive, Suite 200
Plano, TX 75024
(972) 739-6900
andy.ehmke@haynesboone.com
dan.smith@haynesboone.com

ON BEHALF OF THE PATENT OWNER:

DAVID P. LINDNER, ESQ.
Crowell & Moring LLP
300 North LaSalle Drive, Suite 2500
Chicago, IL 60654
(312) 222-8123
dlindner@crowell.com

The above-entitled matter came on for hearing on August 13, 2026,
commencing at 10:00 a.m.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

P R O C E E D I N G S

- - - - -

JUDGE EASTHOM: Good morning. This hearing involves four cases, each challenging a different patent and styled as Intel Corporation versus Advanced Cluster Systems Inc. It's IPR2025-00913, -00914, -00915, and -00915 (sic). To my side, here's Judge Murphy, and then remotely we have Judge Raevsky on my left, and Judge Peslak on the right.

Judge Peslak and I will preside over each of the four cases, with Judge Murphy presiding with us on the first two, and Judge Raevsky on the last two. Can we have appearances from Petitioner, please, first?

MR. EHMKE: Thank you, Your Honor. My name is Andrew Ehmke, lead counsel on behalf of Intel. Joining me at the counsel's table is Dan Smith.

JUDGE EASTHOM: Great. Thank you both. You're going to be presenting, Mr. Ehmke?

MR. EHMKE: I will be presenting, yes.

JUDGE EASTHOM: Okay. Thank you. And then, can we have appearance by Patent Owner, please?

MR. LINDNER: Good morning, Your Honor. David Lindner from Crowell & Moring on behalf of Patent Owner, Advanced Cluster Systems, Inc.

JUDGE EASTHOM: Welcome. Okay. Per our hearing order, and as requested by the parties, each side will have 60 minutes total, with the

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 clock behind me showing the total available time remaining. Petitioner has a
2 burden of showing unpatentability and will present argument first. Patent
3 Owner will respond.

4 And with any time reserved, Petitioner and Patent Owner will
5 provide rebuttal and surrebuttal, respectively. Petitioner, you may begin.
6 And please let me know if you want to reserve any rebuttal time. It's subject
7 to change, obviously, but what's your estimated?

8 MR. EHMKE: I would like to reserve 10 minutes.

9 JUDGE EASTHOM: Okay. Great. I'm just going to show the
10 total time on the clock here.

11 MR. EHMKE: That'll be just fine. Thank you.

12 JUDGE EASTHOM: Yes.

13 MR. EHMKE: And can the remote judges hear me fine through
14 this microphone? Judge Peslak?

15 JUDGE PESLAK: I can. Yes.

16 MR. EHMKE: All right. Thank you. Thank you. The story of
17 these patents starts with some third-party software called Mathematica and
18 MATLAB. And what Mathematica and MATLAB are, are software
19 programs that let you solve complicated mathematical equations and
20 computations.

21 And the way they would originally work is you'd have one copy of
22 Mathematica or one copy of MATLAB running on a single computer. So
23 when you're performing your calculations, you'd be limited to the computing
24 power of that given computer. If we turn to Slide 2. Turn to Slide 2.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 What we have here in the upper left is the field of the patents. And
2 what the patents proposed to do is add something called cluster computing
3 functionality to these existing programs. And some of the existing programs
4 there are listed in the detailed description. We see it's Mathematica and
5 MATLAB.

6 And what this cluster computing functionality did was take that
7 original program and bolt some functionality onto it. So what you could do
8 then is rather than having one copy on one computer, you could have
9 multiple copies running on multiple computers in parallel.

10 And then they would communicate through this bolted-on extra
11 functionality so they could all work together and perform complicated
12 computations, working and using the power of all those different computers
13 together. The issue with this solution, though, it was published by a series
14 of researchers out of Cornell University nearly a decade prior to the priority
15 dates of these patents.

16 We have Exhibit 1005 and Exhibit 1006, just some excerpts here
17 on the screen. This is the Menon and Trefethen paper. And what they were
18 describing is a system called MultiMATLAB. And what MultiMATLAB
19 was, was an extension to MATLAB where you bolted on some functionality
20 so that you could have multiple copies of MATLAB running in parallel, and
21 you could send data and tasks back and forth.

22 It was the exact same solution. And not only was it the same
23 solution, it had the same architecture as that described in the patents, has the
24 same sequence of operations, and uses even the same message-passing

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 protocols. So let's go into the details of the teachings of the prior art.

2 And we'll go to Slide 3. And what we've done here on Slide 3 is
3 set forth all the different issues that are open in this proceeding. And we've
4 identified which of the respective proceedings a particular issue applies to.
5 And I'll start with the claim construction of the hardware processor.

6 As we move to Slide 4. This pertains to the '034 Patent in the
7 '00913 proceeding. We turn to Slide 5, we see the operative language here,
8 "A hardware processor with a plurality of processing cores." And when
9 we're thinking about the claim construction of a hardware processor, we
10 recall that we only need to construe the term necessary to the extent to
11 resolve the dispute between the parties.

12 And here, the dispute is about whether a hardware processor can be
13 one or more microprocessors. And the specification answers that question
14 for us. If we turn to Slide 6, we have this first excerpt from the
15 specification. This is column 5 where we introduce this concept of a
16 processor can contain one or more processor cores. And the processor cores
17 are generally independent microprocessors.

18 JUDGE MURPHY: So Counsel, what's the distinction the patent
19 is making between cores and processors?

20 MR. EHMKE: Between core and processor. Well, the processor,
21 in a sense, is the container. And it can contain one or more cores. So we
22 have that parent-child relationship between the processor and the cores.

23 JUDGE MURPHY: The core is actually executing the function?

24 MR. EHMKE: Yes. Right. Because what we have there with the

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 cores is then it tells us that the cores are generally independent
2 microprocessors. Or also tells us later in the specification when we're
3 thinking about a single chip package, that the core is a unit for execution.

4 So when we're talking about the operation, the execution, it's the
5 microprocessor performing the execution. And the concept of the hardware
6 processor is describing what it is that we have that's going to be performing
7 the execution.

8 JUDGE MURPHY: Thank you.

9 MR. EHMKE: So when we look at this phrasing here in column 5,
10 it introduces two concepts, one of which Judge Murphy touched on, is this
11 relationship between the processor and the microprocessor. The terms are
12 not used synonymously. A processor can contain microprocessors. A
13 processor can contain cores.

14 The second concept that it introduces is this notion of these
15 different embodiments of one or more. And here it uses the phrase one or
16 more processor cores, and that those processor cores are generally
17 independent microprocessors. We see both of these concepts reinforced in
18 the next portion of the specification as we turn to Slide 7.

19 Slide 7, this is the excerpt from the patent of column 7. And it
20 describes that, "The processors can be one or more general purpose, single-
21 core or multi-core microprocessors." So we see both of those concepts
22 reinforced. Again, there's the relationship and distinction between a
23 processor and a microprocessor.

24 And we're also seeing the multiple embodiments, the one or more

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 microprocessors. A processor can be one microprocessor, a processor can
2 be more than one microprocessor. And then we see this reinforced a third
3 time as we turn to Slide 8 in column 9. Column 9, again, talks about a
4 processor can be microprocessors, plural.

5 We have the relationship being established between a processor
6 and microprocessor. And we have it being established that we could have a
7 plurality of microprocessors. Then if we look at all that in summary on
8 Slide 9, we see that the specification, when it's talking about processors, a
9 processor can contain one or more independent microprocessors.

10 A processor can be one or more microprocessors. A processor can
11 be microprocessors. We see this repeated throughout the specification when
12 we're talking about the different embodiments with respect --

13 JUDGE MURPHY: Oh, I think, isn't the issue that Patent Owner
14 is raising, does it have to be single-core as opposed to a single or a single
15 multi-core?

16 MR. EHMKE: Right. And I would say that that's precisely one of
17 the issues here, is that that's one of the embodiments, right? If we have a
18 single processor, we still have to ask how many cores are there in that single
19 processor? And there are multiple ways that we can get to that answer. The
20 first way is, well, how many microprocessors do you have?

21 Because the specification, as I turn back to Slide 6, the
22 specification says one way to count the number of cores is you count the
23 number of independent microprocessors. Because here, the specification is
24 saying that the cores are generally these independent microprocessors.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 So that's how we get to the plurality of cores in this embodiment, is
2 we have a plurality of independent microprocessors. Another way to get to
3 the plurality of cores is to have a microprocessor that has a number of
4 execution units. That's the other way the specification tells us that we can
5 get to a plurality of cores.

6 And so, we outlined in our briefing that when you look at this one
7 or more notion with respect to microprocessors, you have many different
8 permutations. You could have one single-core chip, but the specification
9 -- or excuse me, the claim language removes that because that doesn't have a
10 plurality of cores.

11 So we just have a single single-core microprocessor. But if I have
12 a single multi-core microprocessor, I have a plurality of cores. If I have
13 multiple single-core processors, I have a plurality of cores. And if I have
14 multiple multi-core microprocessors, I have a plurality of cores. Does that
15 answer your question, Your Honor?

16 JUDGE MURPHY: Yes.

17 MR. EHMKE: And so when we have this concept of all these
18 different embodiments described in specifications, we see that the prior art is
19 teaching at least one of these embodiments. I've moved to Slide 10. On
20 Slide 10, what we described is the RS6000, which was the documentation
21 for the IBM system used in the Menon and Trefethen papers.

22 What it describes is that you have this IBM SP2 processor node,
23 and that node has a symmetric multiprocessor. And that's what we mapped
24 to the hardware processor limitation. Well, we still have to answer the

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 question of how many cores does the symmetric multiprocessor have.

2 We turn to Slide 11. We see that the symmetric multiprocessor
3 includes 4, 8, 12, or 16 64-bit microprocessors. And so, we have the
4 embodiment specifically described in the specification of a plurality of
5 independent microprocessors. So here we're showing a hardware processor,
6 the symmetric multi-processor, having a plurality of independent
7 microprocessors.

8 In this case, it's got anywhere from 4 to 16. That's the plurality of
9 cores. That renders hardware with a plurality of cores obvious. Now, if we
10 turn to Slide 12 and we look at Patent Owner's argument here, Patent Owner
11 is referring to a hardware processor as a single processor package.

12 First, that's not in the claims, is the count of the single processor
13 package. And what it's effectively doing is bringing in the -- bringing in an
14 embodiment from the specification and trying to limit the scope of the claim
15 to the embodiment where you have only the one microprocessor.

16 But even if we go that far and we say the claim should only be
17 narrowed to only the embodiment with the single microprocessor, the prior
18 art renders that obvious as well. As we've been discussing throughout this
19 on Slide 13, we're going to count the number of processing cores.

20 And when we're in the environment where we have multiple
21 independent microprocessors, we're just going to count those independent
22 microprocessors. But the specification tells us that the other way, if we're
23 dealing with just a single chip, to get the total number of processing cores,
24 and we had this quote from the specification at the bottom.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 To get the total number of processing cores, well, let's look for the
2 processing units capable of single-threaded execution. Let's look for
3 execution units. And that's what the prior art discloses. We turn to Slide 14.
4 These microprocessors in the RS6000 --

5 JUDGE PESLAK: Mr. Ehmke?

6 MR. EHMKE: Yes. Yes, Your Honor.

7 JUDGE PESLAK: Can you explain what an execution unit is?
8 You're throwing out that term and you haven't really explained how that ties
9 back to a core.

10 MR. EHMKE: Sure. So what I'm referring to with respect to that,
11 Your Honor, is at the bottom of Slide 13 from the specification of the '034
12 Patent. And the specification provides us some insight of how we're going
13 to count the total number of processing cores.

14 So to figure out what the processing cores are, it gives us an
15 example of what one of those processing cores can be. It's a processing unit
16 capable of single-threaded execution. So we're going to have some logical
17 component inside our processor that's capable of getting a single thread of
18 code, and perform that execution. That becomes an execution unit. That's
19 from the specification itself.

20 JUDGE PESLAK: So you're saying that if there's four cores, then
21 there's four executions, single-threaded execution units?

22 MR. EHMKE: Yes. If you're going that direction. That if there
23 are four cores, and I want to be careful with this, Your Honor. There's
24 multiple ways to determine if there are four cores, according to the

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 specification. One way to determine if there are four cores is, are there four
2 independent microprocessors?

3 The other way is we have this scenario where we just have a single
4 microprocessor, how do we determine if that's a multi-core microprocessor?
5 And the specification tells us that to determine if it's a single-core -- excuse
6 me, a single microprocessor with a plurality of cores, we're going to count
7 the execution units in that microprocessor. We lose Judge Peslak.

8 JUDGE EASTHOM: Yes. Let's go off the record for a moment.
9 Judge Peslak just froze on us. Sorry, Counsel.

10 (Whereupon, the above-entitled matter went off the record at 10:27
11 a.m. and resumed at 10:28 a.m.)

12 MR. EHMKE: It's understandable, Your Honor. These happen.

13 JUDGE EASTHOM: I stopped the clock.

14 MR. EHMKE: I think he's back.

15 MR. EHMKE: At what point did I lose you, Your Honor?

16 JUDGE PESLAK: I (INDISCERNIBLE).

17 MR. EHMKE: I provided vast discussion of why these are
18 unpatentable. No. So going back in more seriousness to your question,
19 Your Honor, if you're asking how do we determine the number of cores
20 when we just have a single microprocessor when we're dealing with that
21 particular embodiment?

22 What the specification tells us is to determine the total number of
23 processing cores. It gives example of what you do, is you count up these
24 things called processing units capable of single-threaded execution. So

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 we're going to look for this concept of single-threaded execution. Do we
2 have these units that can handle single-threaded execution?

3 And if you do, if you've got multiple of those, then you're a multi-
4 core single processor chip. Of course, there's the other embodiment where
5 there's more than one microprocessor, in which case you just simply count
6 the number of independent microprocessors.

7 JUDGE PESLAK: So how many execution units are there in
8 RS6000?

9 MR. EHMKE: Very good question. So in the RS6000, we've got
10 multiple embodiments here. The first embodiment is we have the symmetric
11 multi-processor that has 4, 8, 12, or 16 independent microprocessors. So
12 with respect to that embodiment, we're going to count the number of the
13 independent microprocessors.

14 And so it has at least four cores, because it has four independent
15 microprocessors. We also have the other embodiment where there's just a
16 single chip. And that's this POWER3 architecture that's used in the RS6000.
17 If we look at just one of those chips, the RS6000 has eight execution units.

18 And that's the direct quote from the discussion of the RS6000, the
19 POWER3 chip. It has eight execution units. And so even in the
20 embodiment where there's just a single microprocessor, there's eight
21 execution units, which is what the specification tells us we count to
22 determine if there's a plurality of cores.

23 JUDGE MURPHY: And Counsel, just for clarity. So in the
24 petition, you're relying on the SMP?

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 MR. EHMKE: Correct.

2 JUDGE MURPHY: Multi-processor embodiment?

3 MR. EHMKE: Correct.

4 JUDGE MURPHY: And the POWER3 was in your reply?

5 MR. EHMKE: Was a response to Patent Owner's attempt to
6 narrow this claim scope. Yes.

7 JUDGE MURPHY: All right. So you're saying that's in response
8 to their proposed claim construction?

9 MR. EHMKE: Correct. That their proposed claim construction
10 doesn't overcome the evidence that was included in the original petition.
11 The POWER3 chip documentation, Exhibit 1010, was actually in the
12 original petition.

13 JUDGE MURPHY: Well, it --

14 MR. EHMKE: Yes. Yes. And yes, to your point --

15 JUDGE MURPHY: The evidence is there, but it wasn't in your
16 petition because you relied on the SMP?

17 MR. EHMKE: Correct. The SMP teaches the embodiment where
18 there's a plurality of independent microprocessors.

19 JUDGE MURPHY: Okay.

20 MR. EHMKE: Yes.

21 JUDGE EASTHOM: Just for clarity, RS6000, does that describe
22 the SMP? Are they the same thing?

23 MR. EHMKE: Yes. So yes, there's a bunch of terminology
24 because it's IBM's documentation. So you have in the Menon and Trefethen

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 papers, they describe the functionality of the MultiMATLAB system. And
2 in those papers, they specifically say they're running it on the IBM SP2
3 computer hardware. The RS6000 is the documentation for the IBM SP2
4 system.

5 JUDGE EASTHOM: Is the SP2 system, is that a -- that's a -- you
6 said it's multi-core or multi-processor. But is it a single chip? Is it on a
7 single die?

8 MR. EHMKE: Okay. So yes. So going to that issue. So again,
9 just sort of following the hierarchy here. So we have the RS6000 is
10 describing the IBM SP2 computer hardware. In that computer hardware,
11 there's something called a node. And in that node is the SMP, which is what
12 we've mapped to the hardware processor.

13 So we've got the MultiMATLAB running on the IBM SP2, which
14 has nodes, which has the symmetric multiprocessor, which has the POWER3
15 microprocessor, which has the eight execution units. Right? So that's our
16 hierarchy. So now to your question of residing on the same die.

17 And I'll actually skip way ahead in my slide deck, Your Honor,
18 and go directly to that, to make sure I speak correctly on the issue. I've
19 moved all the way ahead to Slides 45 and 46. So I'll let everyone scroll with
20 me here.

21 JUDGE PESLAK: Counsel?

22 MR. EHMKE: Yes.

23 JUDGE PESLAK: I have a couple preliminary questions before
24 you go into this.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 MR. EHMKE: Sure. Sure. Go ahead.

2 JUDGE PESLAK: As I read, the spec of these patents doesn't
3 mention the word die. This is only in the claims, correct?

4 MR. EHMKE: That is correct.

5 JUDGE PESLAK: And your expert, Dr. Bajaj, doesn't provide an
6 opinion on the meaning that a person of ordinary skill in the art would attach
7 to the word die?

8 MR. EHMKE: He did not provide an express construction.
9 Correct. He applied the plain and ordinary meaning.

10 JUDGE PESLAK: Okay. And there's nothing in the record from
11 an IEEE dictionary or other kind of treatise about what the definition of die
12 is?

13 MR. EHMKE: I believe the parties have briefed that it's their
14 understanding that the die is a semiconductor substrate.

15 JUDGE PESLAK: Okay. So where is that in the briefing?

16 MR. EHMKE: In Patent Owner's response and the Petitioner
17 reply.

18 JUDGE PESLAK: Okay. All right. Go ahead.

19 MR. EHMKE: Okay. So you raised the question of, well, what
20 does the RS6000 teach with respect to the same die, which is going to the
21 '621 Patent, and the dependent claims there of the first processor and second
22 processor reside in the same die.

23 And this is a great segue because we have to have the concept in
24 our heads, even though we switched patents, it's the same specification. And

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 so we have a first processor and a second processor. So we have all these
2 different embodiments of what a processor can be.

3 Is it independent microprocessors? Is it a set of cores together?

4 And so what we pointed to in the RS6000, as we moved to Slide 46, is the
5 first thing we noticed, that RS6000 is teaching four microprocessors on a
6 card. And we included evidence that the card contains a single
7 semiconductor substrate.

8 So we have already a teaching of four independent
9 microprocessors on the same surface, on the same die, on the same substrate.

10 And so, when we're looking at the concept of a first processor, second
11 processor --

12 JUDGE EASTHOM: Are you saying a card is a die?

13 MR. EHMKE: We're saying a card is an example of a
14 semiconductor substrate, which is what we've agreed that that's what a die is.
15 Because you have to think about it, because a processor can be multiple
16 independent microprocessors. And so, we have to have something upon
17 which independent microprocessors are residing. And so that's the card in
18 this particular example. Then we went on to say, well, if we had this notion
19 of we've got multiple core --

20 JUDGE PESLAK: Counsel, this is Judge --

21 MR. EHMKE: Yes.

22 JUDGE PESLAK: This is Judge Peslak again. Where did Patent
23 Owner say in their briefing that a substrate is a die?

24 MR. EHMKE: I think they said it three times in their patent owner

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 response, Your Honor. And I'll pull the exact page numbers up for you here
2 just momentarily. But it was three times throughout the Patent Owner
3 response that they argued that you have to show -- to establish a die, you've
4 got to show that it's on a semiconductor substrate.

5 And I'll get those page numbers for you shortly. Then we said not
6 only does the prior art teach four processors on the same surface on the same
7 card, it was known to POSITAs that one way you could implement this, is
8 you could use the technology of processor scaling to put 256 on the same
9 die.

10 Not just one or two, but they knew how to put 256 on the same die.
11 And we included evidence that they in fact were doing that, that they could
12 have a semiconductor die with a first core and a second core. So we
13 attempted to cover all the different embodiments of a way a processor could
14 be.

15 Whether you've got multiple independent microprocessors all on
16 the same surface, or if you're going to merge them all together and put them
17 all on the single semiconductor substrate as a die. We showed that as well,
18 all in the original petition. Thank you.

19 Your Honor, if you look at pages 3, 7, and 19 in the '621 Patent
20 Owner response. Three, 17 and 19, excuse me. Patent Owner argued that in
21 order to establish a die, you need to show a semiconductor substrate.

22 JUDGE EASTHOM: So your position in the petition was that you
23 have some processors on a card, and it was well known to put multiple
24 processors on a semiconductor die?

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 MR. EHMKE: Yes.

2 JUDGE EASTHOM: And so it would've been obvious to --

3 MR. EHMKE: Correct.

4 JUDGE EASTHOM: Okay.

5 MR. EHMKE: Because POSITAs were actually doing that. We
6 included some evidence that this isn't a hypothetical modification, it's -- if
7 you've got multiple processors on a single thing, you could have them on a
8 card, you could have them on a die. You could merge them together and
9 manufacture them in that particular way. Do we still have everybody?

10 JUDGE EASTHOM: Judge Peslak, can you hear us?

11 JUDGE PESLAK: Yes, I'm back now.

12 JUDGE EASTHOM: Great. We can hear you.

13 JUDGE PESLAK: So I really have two questions about your
14 position here in this case, Mr. Ehmke, on this particular limitation. You cite
15 to Exhibit 1050 and 1051 here for the knowledge of one of ordinary skill in
16 the art. But those aren't part of your combination here.

17 MR. EHMKE: That is correct.

18 JUDGE PESLAK: So we have some guidance from the director
19 that says we can't use expert testimony to supply a missing claim limitation.
20 Isn't that what you're trying to do here?

21 MR. EHMKE: No, Your Honor. Because we also have the
22 embodiment where you have a first processor, which is a plurality of
23 independent microprocessors, and a second processor, which is a plurality of
24 independent microprocessors. And that's what the card is showing. We're

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 showing at least four. We're showing 16 microprocessors all in the same
2 semiconductor substrate. That onto itself renders the claim obvious.

3 JUDGE PESLAK: But didn't you put that in your reply?

4 MR. EHMKE: No. As I have on Slide 46 here, Your Honor, the
5 very first sentence is we're pointing to the processors mounted on one card.
6 That was our original position in the petition, is that these processors
7 mounted on this card renders this claim obvious.

8 JUDGE PESLAK: But where does the petition say that they're
9 mounted on the same die? Where in RS6000 does it say they're mounted on
10 the same die?

11 MR. EHMKE: They're mounted on the same card, which a
12 POSITA understands to be a semiconductor substrate, and we included
13 evidence of that. And a semiconductor substrate is the die.

14 JUDGE PESLAK: So in your reply then, you added --

15 MR. EHMKE: Extra evidence establishing what POSITAs
16 understood with respect to a card.

17 JUDGE PESLAK: But didn't you then change your position that
18 the four processors weren't just mounted on a card, but within each
19 processor, they were multi-cores?

20 MR. EHMKE: No.

21 JUDGE PESLAK: It's on page 13 of your reply. Isn't that what
22 you were trying to get across there?

23 MR. EHMKE: Well, what we discussed in the original petition,
24 Your Honor, is that if you've got four processors mounted on a card,

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 POSITAs also knew that they could be mounted altogether, that you could
2 have 256 of them. So if you have four processors or 16 processors mounted
3 on a card, that renders obvious that they'd be on a single semiconductor
4 substrate. So no, we didn't attempt to change our positions.

5 JUDGE PESLAK: Well, let me read from your reply then.

6 MR. EHMKE: Okay.

7 JUDGE PESLAK: Because the single POWER3 chip has, quote,
8 eight execution units. And that thus teaches a single chip package having
9 eight processing cores, which are defined by the '621 specification as a unit
10 capable of execution. Accordingly, to the extent Patent Owner argues that
11 Claims 20 and 25 require a multi-core processor.

12 RS6000's use of the multi-core POWER3 microprocessor renders
13 the claim obvious even under this overly narrow interpretation. Isn't this
14 new evidence you put in the reply?

15 MR. EHMKE: Well, in response to Patent Owner's argument, I
16 did narrow this down to just a single microprocessor, yes. We were replying
17 to that issue of whether or not it should be a single microprocessor. Because
18 again, we've got multiple embodiments here that we're talking about.

19 And the petition was relying on this concept of I've got four
20 independent microprocessors sitting on a single semiconductor substrate.
21 Patent Owner argued, no, no, no. It's got to be one microprocessor. We
22 said, even if you go that far, the prior art is teaching that as well. We're not
23 switching arguments there, Your Honor, we're rebutting and responding to
24 Patent Owner's argument requiring this to be narrowed down to just a single

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 microprocessor.

2 JUDGE PESLAK: Okay. I understand your argument.

3 MR. EHMKE: Okay.

4 JUDGE RAEVSKY: Counsel, I want to explore this further. So
5 what I'm hearing is that you're saying a printed circuit board is a
6 semiconductor substrate. Is that correct?

7 MR. EHMKE: That it has a semiconductor substrate, yes.

8 JUDGE RAEVSKY: How do you distinguish "has" versus "is"
9 here in this context?

10 MR. EHMKE: Well, that's not the totality of the circuit board.
11 There are other things that are on the card. And I just want to make sure that
12 when we're talking about, are these chips mounted on something? They're
13 mounted on a semiconductor substrate. There's more to the card than just
14 the substrate. So I don't want to say that a card is solely equal to the
15 substrate. That's my only point of distinction there, Your Honor.

16 JUDGE RAEVSKY: So you're not taking the position that the
17 printed circuit board itself alone is the semiconductor substrate?

18 MR. EHMKE: That it does have one and it teaches it. Yes, I am
19 saying that. Right. The four processors are --

20 JUDGE RAEVSKY: So what exactly is --

21 MR. EHMKE: The four processors are mounted on this card. And
22 the claim simply requires that we have to have the processors residing on the
23 die. So the four processors are mounted on the card, and that card has a
24 single semiconductor substrate on it so that the processors are mounted to

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 something. That renders obvious the die.

2 JUDGE RAEVSKY: From your briefing, it seems to suggest that
3 you're relying on the PCB itself as a substrate. But what you're saying now,
4 I understand there's something else on the PCB that constitutes the substrate.
5 What would that be?

6 MR. EHMKE: Well, that's going to be the metal, Your Honor,
7 that's the semiconductor substrate. Right?

8 JUDGE RAEVSKY: So the contacts? The metal contacts on the
9 PCB?

10 MR. EHMKE: Yes. Yes. And again --

11 JUDGE RAEVSKY: Are you saying the metal contacts on the
12 PCB constitute a die?

13 MR. EHMKE: No. The substrate layer that lets them
14 communicate constitutes the die, right? The chips don't exist in a vacuum.
15 They wouldn't be able to communicate with anything. So they're mounted to
16 the board, right? And this is the extra evidence we included in the reply,
17 showing that this is what POSITAs understood, that when you're mounting
18 onto a card, you're mounting onto the semiconductor substrate layer in that
19 card.

20 JUDGE RAEVSKY: So the semiconductor substrate layer in the
21 card is what I'm having a hard time identifying. You seem to suggest that it
22 includes metal contacts. The card itself, the PCB, would have some
23 dielectric. Is it a combination of the metal contacts and the dielectric?

24 MR. EHMKE: Again, I don't think we need to go so far into the

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 -- I mean, that's one of the points that Patent Owner is raising, is trying to
2 read in the claim this notion of how you fabricate this die, how you fabricate
3 the card, or are you supposed to have on die integration, right? None of that
4 exists in the claim.

5 None of that exists in the specification. All we're relying on here
6 and what Patent Owner relied on is the baseline knowledge of skill of
7 residing on the same die, because there's no discussion in the specification
8 providing any sort of meaning to that. We're just relying on the baseline
9 knowledge of a POSITA.

10 And what a baseline knowledge of POSITA is, is we included
11 through our expert declaration, as well as through supplemental evidence, is
12 that a card has a substrate layer, and that's what you're mounting the
13 microprocessors to. And the claim simply says, we need to be residing on
14 the same die.

15 JUDGE RAEVSKY: It feels like we might be in need of greater
16 guidance on what a die means. And I have an additional concern, which is it
17 seems in your briefing that you're trying to hold Patent Owner to saying that
18 a die means a semiconductor substrate, whereas I read their Patent Owner
19 response as saying a die is a semiconductor substrate, i.e., a single chip.
20 And that seems to be an omission in your reply. How would you address
21 that now?

22 MR. EHMKE: Well, I guess I am holding Patent Owner because
23 they argued that in order to show that the prior art teaches the die, you need
24 to show a single semiconductor substrate. And we responded and said, well,

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 that's what we did because we pointed to the card.

2 And then we included evidence to show why that card taught that
3 single semiconductor substrate layer. And so to the extent that there was
4 this perceived gap, we showed that POSITAs understood that when you're
5 mounting processors to a card, you're mounting them to a substrate layer.
6 Which is what Patent Owner argued is what's required to meet the scope of
7 the claim, is to show that the prior art teaches the substrate layer.

8 JUDGE RAEVSKY: So you disagree with the Patent Owner that
9 it has to be a single chip, fundamentally?

10 MR. EHMKE: Correct.

11 JUDGE RAEVSKY: Okay. I understand your position.

12 MR. EHMKE: Okay. And the questions on reside on the same --

13 JUDGE EASTHOM: Oh, can we stop for a minute? I think we
14 have another freeze --

15 MR. EHMKE: Okay.

16 JUDGE EASTHOM: -- of Judge Peslak.

17 MR. EHMKE: I think --

18 JUDGE EASTHOM: I'll stop the time, and we're off the record.

19 JUDGE EASTHOM: Okay. We'll go back on the record here.

20 MR. EHMKE: So I was just asking, Judge Peslak, if there are any
21 further questions on reside on the die.

22 JUDGE EASTHOM: Okay.

23 JUDGE PESLAK: I don't have any further questions on that.

24 MR. EHMKE: Okay. So then I will flip back to Slide 15 to

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 discuss the next issue, which is the one, two, three, one sequence of
2 operation. And in some form or fashion, this applies across all of the
3 patents. Moving to Slide 16, just generally discussing what we refer to by
4 the one, two, three, one sequence of operation, is we've got these different
5 nodes running Mathematica or running MATLAB.

6 We've got node 1, node 2, and node 3. And we're going to start at
7 node 1, and we're going to send a value from node 1 to node 2, and it's going
8 to go directly to node 2. Node 2 is going to perform a mathematical
9 expression evaluation. It's going to do some form of math. Then it's going
10 to go from node 2 to node 3.

11 Node 3 is going to do some math. Node 3 is going to send that
12 back to node 1, and then that result is going to be sent up to the user. One of
13 the ways to accomplish this, as the specification describes, is using
14 instructions supplied by the user or a script.

15 And it also talks about, as we're performing these mathematical
16 evaluations on the different nodes. So when node 2 is performing its
17 mathematical evaluation and node 3 is performing its mathematical
18 evaluation, that these routines that are being performed might be the same
19 operation on the different nodes.

20 So let's get into what the prior art discusses as we go to Slide 17.
21 What we have here is a depiction from Menon of the basic MultiMATLAB
22 node architecture. We've got three different nodes, each running a software
23 processor. There's the interactive processor, and then there's the second
24 processor, and third processor.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 And then we have a connecting network that allows them to
2 communicate. Well, how do they communicate? Are they able to
3 communicate directly with each other? Well, what Menon describes as we
4 turn to Slide 18, is using this architecture called SPMD message passing.

5 And what the SPMD message passing is, is to accommodate
6 applications that require a fine degree of communication that provides point-
7 to-point communication. Here's a set of commands. And it provides a table
8 of the commands. Look more closely at the table of the SPMD.

9 JUDGE MURPHY: And Counsel, you're reading point to point as
10 the claimed peer-to-peer communication?

11 MR. EHMKE: Correct. Yes. And there's a lot more to it than just
12 the point to point, Your Honor. But yes. So if we go to Slide 19 with
13 respect to the SPMD communication, to facilitate the fine degree of
14 communication, to facilitate the point-to-point communication, we have this
15 send function and the receive function that we've highlighted here in this
16 table.

17 The send function sends data from one process to another. And the
18 receive function is the corollary. It receives data sent from another process.
19 So if we think about what Menon is teaching in totality, it's saying, for
20 applications that want a fine degree of control, that want point to point, you
21 have send function so you can send data from one process to another
22 process.

23 And you have the receive function to receive data sent from
24 another process. But we can go even further than that. We go to Slide 20, in

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 the Trefethen paper describing MultiMATLAB. Trefethen describes, as we
2 go to Slide 21, using SPMD communications. So this is one of these
3 programs that wants the fine degree of control.

4 And it's built on the send and receive command. And we see those
5 examples there. Let's walk through how this code operates. As we go to
6 Slide 22, we have the one-to-two process. What happens here? The first
7 node, the first process performs a send. It's going to send a value to the next
8 process.

9 It's using the send command. It's point-to-point. It's going from
10 one process to another. That send command then has the corollary receive
11 command at the second node. The receive command is going to receive the
12 value that was sent from the first node. Well, then what happens? We'll go
13 to Slide 23.

14 The second node, having used the receive command to receive that
15 data from the other process, is then going to perform its mathematical
16 calculation. In this example, it's a very simple calculation. It's going to
17 perform the doubling operation. It's going to multiply it by two.

18 So we have the initial value, which was a one, being sent to the
19 second node. It performs this doubling operation to turn it into two. And
20 then it sends that value of two to the third node using the send function to
21 send from one process to another process.

22 The third node uses the receive function to receive that value,
23 which was four -- or excuse me, which was two. It then performs its
24 mathematical calculation of multiplying it by two, turning it into four, so we

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 can produce this output of A equals four. That's the three to one.

2 But we can go into further detail of that three-to-one step as we go
3 to Slide 25. What Trefethen says is as you're performing these calculations,
4 as each node is performing its calculations, we can send the output to the
5 master process, the originating process, as soon as it's ready. And why are
6 we doing that?

7 Again, Trefethen tells us, as you're performing computations on
8 multiple processors, you might want to plot that. You might want to graph
9 that on your originating process and send that to the user's screen. Why? So
10 the user can monitor the progress of these calculations.

11 So as we're performing all these calculations in this example of
12 doubling it by two each time, we're sending results back, including the result
13 from node 3, sending it back to the first node, and sending it to the user
14 screen. And Trefethen gives us a summary of this code.

15 As we turn to Slide 26, and we look at this paragraph from
16 Trefethen describing the operation of its code. Process 0 creates the variable
17 A with a value of one, and sends that to the next process, process 1. Process
18 1 receives that message, performs its math, it doubles it, sends that result to
19 the next process, and so on. So we can get the value of four being sent back
20 to the user.

21 JUDGE MURPHY: Well, Counsel, but it's that last part that's the
22 dispute, right? I mean, Trefethen says it's the output is produced.

23 MR. EHMKE: Yes.

24 JUDGE MURPHY: And it sends it to the master process. And so

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 the issue is with respect to the claim language, why does that mean it's sent
2 back to the first node or the interactive process in the Menon Trefethen
3 system?

4 MR. EHMKE: Because that's where the interactive process is. In
5 Menon, if we go back, if we look at on Slide 24 in the bottom left, in
6 Menon's architecture, you have as the first processor in this particular case,
7 that's where the interactive portion is. That's where the user is interacting
8 with the system. It's on this first node.

9 And so, for it to be sent to the user's screen, so the user can
10 monitor the calculations, it's got to be sent to where the user is, and where
11 the user's interacting with it. That's the first node. And so we have the value
12 of four from Trefethen being sent as soon as it's ready so the user can
13 monitor the results of the computation's calculations.

14 Where is the user? The user's at node 1. That's where the
15 interactive portion is. So it's going from the third node, which calculates the
16 value of four. It's being sent to the interactive process so it can be sent to the
17 user screen. That's node 1.

18 JUDGE MURPHY: And what about Dr. Bajaj's testimony to the
19 notion that this is a pseudomaster?

20 MR. EHMKE: Correct. Because one of --

21 JUDGE MURPHY: How does that play into it?

22 MR. EHMKE: Right. One of the issues here is this concept of the
23 phrasing of master and slave, right? And so Patent Owner has kind of used
24 the phrase, originating process. The prior art references the master process.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 And so we just wanted to be clear that even though we're sending it to the
2 master process as taught in the prior art, it's not a master slave arrangement.

3 So that's why it's called a pseudomaster. It's because we don't have
4 the scenario where the master process is the gatehouse and clearing for all of
5 the intermediate results, right? The results are not going from node 1, must
6 go to the master, and then the master sends that intermediate result to node
7 2.

8 Node 2 performs a calculation, sends it to the master. The master
9 takes that result and sends it to node 3. That's the master slave arrangement.
10 And that's not the embodiment we pointed to at all. We pointed -- oh, we
11 may have lost Judge Raevsky. Judge Raevsky, are you back?

12 JUDGE RAEVSKY: I am back.

13 MR. EHMKE: Okay. All right. So that is why -- so there is this
14 concept of -- right? And the claims even mention it, require it that you have
15 somebody starts the process and then there's other people awaiting
16 instructions. And so there's the master, someone that kicks things off.

17 But in terms of the communication path of these intermediate
18 results, Trefethen and Menon are very clear with the send and receive
19 function that it's the individual nodes that are able to communicate directly
20 with each other and pass --

21 JUDGE MURPHY: Right. But the point is, the claim says
22 communicate the result from the third node to the first node.

23 MR. EHMKE: Yes.

24 JUDGE MURPHY: And if that third node here in the example is

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 A equals four --

2 MR. EHMKE: Yes.

3 JUDGE MURPHY: -- what Trefethen says is you send the result
4 or the output to the master process. Correct? That's what it says.

5 MR. EHMKE: Yes.

6 JUDGE MURPHY: So that the user can view it on the screen or
7 display it on the -- display the results on the screen. It doesn't say send it
8 back to the first node or send it back --

9 MR. EHMKE: The first node is the master in that scenario.

10 JUDGE MURPHY: And that's where I want to explore that.

11 MR. EHMKE: Okay. Okay.

12 JUDGE MURPHY: My understanding is that the record requires
13 Dr. Bajaj's testimony on that point to say that a person of ordinary skill
14 would know when you say return it to the master process, that is returning it
15 to the interactive process or the first node in the Menon Trefethen system.

16 MR. EHMKE: Right.

17 JUDGE MURPHY: MultiMATLAB system.

18 MR. EHMKE: Sure. And on Slide 28, we actually have Dr.
19 Bajaj's testimony where he discussed, one, this notion of a pipeline sequence
20 that POSITAs understood that you have this sequencing aspect to it.
21 POSITAs also knew that you could have a peer-to-peer network where every
22 node could communicate its results to other nodes.

23 So he had that baseline. He set forth that baseline knowledge of a
24 POSITA, and then he applied it and analyzed this code in Trefethen and

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 Menon. He annotated what it was doing. He then provided plain language
2 discussing and showing that it goes to one, two, three, back to the one,
3 which is where the interactive processor is.

4 JUDGE MURPHY: Yes. And your slide is referencing his
5 testimony at Exhibit 1003, paragraph 45?

6 MR. EHMKE: 114, Your Honor.

7 JUDGE MURPHY: Oh, I see. Yes. On the right.

8 MR. EHMKE: Okay. 45 and 114.

9 JUDGE MURPHY: Right.

10 MR. EHMKE: And it's throughout his declaration as well. This is
11 discussed multiple times throughout his declaration.

12 JUDGE MURPHY: And what about his testimony? It's actually
13 in paragraph 221 where he goes into the notion of what a pseudomaster is
14 and what a person of ordinary skill would understand. He seems to be, I'll
15 call it corroborating or trying to establish a basis for saying that a person of
16 ordinary skill would know this.

17 MR. EHMKE: Pull that up here so we can look at it. And I'm
18 sorry, which paragraph again are you referring to?

19 JUDGE MURPHY: Paragraph 221, Exhibit 1003.

20 MR. EHMKE: It's too slow. Scrolling to it here.

21 JUDGE MURPHY: You see that toward the bottom of the
22 paragraph where it begins, "A POSITA would recognize that the, quote,
23 master process, close quote, described by Trefethen would be the interactive
24 process of Menon."

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 MR. EHMKE: Yes.

2 JUDGE MURPHY: So my point is, he's explaining what is
3 described or --

4 MR. EHMKE: Correct. Right.

5 JUDGE MURPHY: The code example --

6 MR. EHMKE: To your potential concern, right, he is doing with
7 this analysis of making sure that we understand that as we're looking at the
8 teachings of Menon and Trefethen, when Trefethen is saying master process,
9 right? We then have Menon's teachings of having an interactive processor.
10 He is stitching together to make sure that's very clear that that master
11 process as described in Trefethen is the interactive process of Menon, which
12 is node 1.

13 JUDGE MURPHY: And is there any rebuttal testimony to that?

14 MR. EHMKE: No, Your Honor.

15 JUDGE MURPHY: And it's my understanding -- I mean, Patent
16 Owner's Counsel can speak, but was Dr. Bajaj deposed?

17 MR. EHMKE: No, Your Honor.

18 JUDGE MURPHY: Thank you.

19 MR. EHMKE: And you've already addressed this, Your Honor, as
20 we have in Slide 29, Patent Owner has a number of arguments, but they're
21 not supported by an expert declaration, it's just attorney arguments. We've
22 touched on them briefly already here. The master control dispatch
23 argument, the eval for further use, the pre-written code, and distinct
24 mathematical expression.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 JUDGE MURPHY: Counsel, can you speak closer to the
2 microphone?

3 MR. EHMKE: I'm sorry, yes.

4 JUDGE MURPHY: Thank you.

5 MR. EHMKE: I love to wander, and I need to not do that. On the
6 first issue of the master control dispatch issue, Patent Owner makes the
7 argument here that the prior art does not teach that the second node is
8 configured to send an intermediate evaluation result to the third node.
9 We've just talked through that at length.

10 That's specifically what the send and receive function do, as I turn
11 to Slide 31. That's the entire point and purpose of the send and receive
12 functions, is to have this fine degree of control, to have point-to-point
13 communication, to send results from one function -- excuse me, from one
14 process to the next process.

15 And then the example code shows the intermediate results of being
16 passed. One times two equals two, that intermediate value is passed to the
17 third node. It's specifically teaching those.

18 JUDGE MURPHY: What's your rebuttal to their response that,
19 well, it's not the same when you have hard coded pre-programmed send and
20 receive instructions or get commands, that type of thing?

21 MR. EHMKE: I'll go to Slide 33, Your Honor. This is the pre-
22 written code argument in the fully scripted code. The specification
23 specifically tells us that you're supposed to use scripts and instructions from
24 a user. That's the embodiment described in the specification. Patent

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 Owner's argument is attempting to read out the very thing that they
2 described. That's our --

3 JUDGE MURPHY: Yes. Thank you, Counsel.

4 MR. EHMKE: -- response on that issue. And then on the last
5 issue where they argue, as we go to Slide 34, about distinct mathematical
6 expressions, that the claims require these distinct mathematical expressions.
7 I'll note the very last sentence in their argument here, that the prior art is a
8 single program routine that each node executes with each node's performing
9 the same doubling operation.

10 If you recall, that's exactly what the specification describes. The
11 specification describes that when you're performing these parallel
12 evaluations, you would have the same operations being performed on the
13 nodes. Patent Owner is confirming the prior art is teaching the exact
14 embodiment described in the specification.

15 JUDGE EASTHOM: Can you shift and respond to your friend's
16 argument that with respect to these five references, no one would be able to
17 go through the hyperlinks that you presented as part of a path to get to them
18 and publicly accessible?

19 MR. EHMKE: Sure.

20 JUDGE EASTHOM: Part of the time, I think one of the
21 arguments (INDISCERNIBLE) was that some of these links are dead now or
22 they didn't all exist at the same time.

23 MR. EHMKE: Sure. Well, and the test is not whether the link is
24 alive today. Of course, it's whether or not a POSITA could have combined

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 these references and found the references in the relevant time period. And
2 we included evidence on the notion of print publication, for example. I've
3 gone to Slide 68.

4 And I'll let everyone scroll to that. What we have in the slide deck
5 here, just for shorthand, there's a bunch of other evidence in the record on
6 this as well of why these qualify as printed publications. And particularly
7 with respect to Menon, we know it was identified and found by POSITAs
8 because they -- POSITAs wrote papers that specifically cited to these papers.

9 And the papers that these POSITAs wrote are all pre the priority
10 date of the patent. So we know people could find Menon because they did
11 find it, and we included evidence in the record showing that they did find it.
12 Same thing with Trefethen. We showed that POSITAs could find it because
13 they did find it.

14 With respect to the RS6000, RS6000 was posted to IBM's website,
15 and we showed how POSITAs would follow the links. This is IBM's online
16 document library. This is their library. And we showed how they were
17 cataloged and indexed. So you could find the documentation for the
18 RS6000.

19 On Slide 70, we included a declaration from IBM attesting to the
20 publication of the POE reference. And we showed how you would go to the
21 IBM's online document library and you could follow those links. In fact,
22 POSITAs did. We included a paper showing that it had been cited to by a
23 POSITA. So the evidence shows that POSITAs did find and could find the
24 prior art through a number of different --

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 JUDGE EASTHOM: And then just real briefly, how about their
2 argument that the new evidence that you supplied with Dr. Yee, I think it is,
3 is --

4 MR. EHMKE: Yes.

5 JUDGE EASTHOM: -- out of bounds. Wasn't in the petition.

6 MR. EHMKE: Well, Patent Owner said they would file a motion
7 to exclude. They did not. But that's neither here nor there. We included a
8 copious amount of printed publication evidence with the original petition,
9 and the Board analyzed that in their decisions on the institution, finding that
10 at that point there was sufficient evidence.

11 Patent Owner then argued in their Patent Owner response on the
12 issue of printed publication. And so, we included further evidence in
13 response to their arguments of why it did in fact qualify as a printed
14 publication.

15 JUDGE EASTHOM: You're approaching your limit if you want to
16 wrap it up or --

17 MR. EHMKE: I think we've hit pretty -- there's a couple
18 dependent claims that we've briefed. I don't think we need to go into detail
19 on them. Those are straightforward issues.

20 JUDGE EASTHOM: Judge Peslak or Judge Raevsky, any
21 questions?

22 JUDGE PESLAK: I don't have any more questions.

23 JUDGE EASTHOM: All right. Thank you, Counsel.

24 MR. EHMKE: Thank you.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 JUDGE EASTHOM: You have 10:49 left on the screen there for
2 your rebuttal.

3 MR. EHMKE: Thank you, Your Honor.

4 JUDGE EASTHOM: Before we get started, did you want any
5 rebuttal time?

6 MR. LINDNER: Yes, Your Honor. If I could also reserve 10
7 minutes, please.

8 JUDGE EASTHOM: Sure. Mr. Lindner, when you're ready, just
9 introduce yourself again for the record, please. Did you say 10 minutes?
10 I'm sorry.

11 MR. LINDNER: Yes. Yes, please.

12 JUDGE EASTHOM: Oh, thanks.

13 MR. LINDNER: Good morning, Your Honor. It's David Lindner
14 on behalf of Patent Owner, Advanced Cluster Systems, Inc. As was noted at
15 the beginning of today's hearing, Petitioner bears the burden to prove
16 unpatentability by a preponderance of the evidence throughout these
17 proceedings, and that's a burden that never shifts.

18 As was kind of noted in the Petitioner's presentation, there are a
19 handful of failures in proof that come up throughout the petitions. Three
20 specifically which if any one of those proofs fail, warrant upholding the
21 validity of all four challenged patents across all four petitions.

22 The first one I'd like to address is with respect to the printed
23 publications, which we were just talking about, and specifically RS6000.
24 Petitioner contended that the RS6000 was a printed publication because it's

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 available on IBM's online document website, which is what they had shown
2 on their Slide number 70.

3 But public accessibility under the case law requires more than just
4 technical availability. It requires an interested individual searching for the
5 art to be able to find it with reasonable certainty. And what --

6 JUDGE MURPHY: Well, it's with reasonable diligence.

7 MR. LINDNER: Sorry. Sorry. Sorry. With reasonable diligence.
8 Thank you, Judge Murphy. And there's been no showing in the record as to
9 any reasonable diligence as to how somebody would've gotten to the IBM
10 webpage in the first place. Dr. Bajaj's --

11 JUDGE EASTHOM: Wasn't the RS6000 cited in Menon?

12 MR. LINDNER: The RS6000 is not cited in the bibliography of
13 Menon at all.

14 JUDGE EASTHOM: Okay. I'm sorry. Yes. I was mistaken.

15 MR. LINDNER: There's a reference to the RS -- to the SP2 in
16 Menon, but the SP2 is not the RS6000. As Counsel addressed during his
17 presentation, the SP2 is different than the -- or the RS was renumbered. But
18 there's nothing in Menon itself to indicate and direct anybody to the IBM
19 webpage.

20 JUDGE EASTHOM: So the RS6000 is documentation that
21 describes the SP2? Is that what --

22 MR. LINDNER: That is correct.

23 JUDGE EASTHOM: Wouldn't someone want to look up for that
24 documentation if they have that disclosure in Menon?

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 MR. LINDNER: I mean, there's no showing and there's no
2 evidence in the record as to how they would know to get to the online
3 documentation webpage for IBM. Dr. Bajaj and both the --

4 JUDGE EASTHOM: They wouldn't know that was an IBM
5 product? Is that what you're saying?

6 MR. LINDNER: They wouldn't know --

7 JUDGE EASTHOM: IBM SP2 is what Menon describes. Section
8 5.2.

9 MR. LINDNER: Correct. It describes --

10 JUDGE EASTHOM: It seems to me that provides a little bit of
11 push for a POSITA to look for that, right?

12 MR. LINDNER: It might provide a push, but there's nothing to
13 indicate how they would get to the IBM webpage.

14 JUDGE EASTHOM: Okay. I understand your argument.

15 MR. LINDNER: Right. I mean, Dr. Bajaj starts at a bunch of
16 hyperlinked webpages, but he's already at the webpage. And the same thing
17 with the supplemental declaration from the librarian. She starts already and
18 says -- I think it's in paragraph 113 of her declaration, says, "I'm starting at
19 the webpage." But how you got to the webpage --

20 JUDGE MURPHY: Well, but it's --

21 MR. LINDNER: -- that's not in the record.

22 JUDGE MURPHY: But Dr. Yee also provides unrebutted
23 evidence that people actually found it and cited it.

24 MR. LINDNER: Well, there's one usage case, it's from a computer

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 science student. And in there, there's a reference to an RS6000 paper.
2 There's no understanding as to how that individual found the paper, what's
3 contained in that paper. It's a dead link, and there was an IBM declaration
4 that was provided for the POE reference. That's the declaration at 1047, but
5 there's no similar declaration from IBM with respect to the RS6000
6 document.

7 JUDGE MURPHY: No, understood. But you start from the
8 baseline that the Menon reference specifically cites the RS6000.

9 MR. LINDNER: Well, it's --

10 JUDGE EASTHOM: The SP2.

11 JUDGE MURPHY: No. Well, it also cites this IBM RS6000 on
12 page 5.

13 JUDGE EASTHOM: Oh, thank you. Thank you.

14 JUDGE MURPHY: 1005. That's what it says. It says
15 successfully run it on IBM RS6000 and Sun SPARC workstations, and the
16 IBM SP2.

17 MR. LINDNER: Right. But the RS6000 is different than the IBM
18 SP2. It's referenced.

19 JUDGE MURPHY: Understood. But my only point is, a person
20 of ordinary skill reads that, knows they need to find the RS6000. It's on
21 IBM's website, and people found it. So that's the evidence. That's not
22 rebutted. Those are facts, right?

23 MR. LINDNER: Yes. Yes. I mean, we know that a student
24 received a paper. We don't know how he found it.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 JUDGE MURPHY: So why would that be a failure of proof under
2 the legal test of a person of ordinary skill or person of interest exercising
3 reasonable diligence?

4 MR. LINDNER: Because --

5 JUDGE MURPHY: Knowing that Menon references the RS6000,
6 knowing that IBM has a website where you can find these things.

7 MR. LINDNER: Well, there's no testimony in the record
8 explaining that IBM has a website and where you can find it.

9 JUDGE MURPHY: It's in the document. It's in the back of the
10 document, the RS6000 document. And they cited it in the petition. I mean,
11 what more do you want?

12 MR. LINDNER: We can then turn to the issue of what is shown
13 with respect to the 1, 2, 3, 1 operation. So there's a little bit of gaps in what
14 is shown in -- between Menon and Trefethen. It is Petitioner's petition -- or
15 position --

16 JUDGE EASTHOM: What slide are we on?

17 MR. LINDNER: Slide 19.

18 JUDGE EASTHOM: Thank you.

19 MR. LINDNER: That --

20 JUDGE MURPHY: Just so we're clear, we're on Petitioner's Slide
21 19?

22 MR. LINDNER: Yes. Petitioner's Slide 19. Correct. The
23 contention as to how Menon and Trefethen teach the 1, 2, 3 operation, is
24 based on the SPMD communication protocol. And that's the send and

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 receive. And in Trefethen's example, it's provided, as you step through the
2 proposed program that was annotated by Dr. Bajaj, and as you step through
3 it on the slides here --

4 JUDGE EASTHOM: This is Slide --

5 MR. LINDNER: Slide 21.

6 JUDGE EASTHOM: -- 21. Thank you.

7 MR. LINDNER: The last process is the one when it says -- well, if
8 we step through it, the first command is send ID plus 1, A. So you're
9 sending A to the next node. The middle process has a receive and has a send
10 command. The last process, which is A equals two times receive, just has a
11 receive command. There is no send command in this example. When we go
12 through the process, the --

13 JUDGE EASTHOM: It says send equals -- I'm looking at Slide
14 29. It says send ID plus 1, A, right after --

15 MR. LINDNER: Slide, you said 29?

16 JUDGE EASTHOM: 21, the one you were on. Did you move to
17 another one?

18 MR. LINDNER: Yes, I can go back.

19 JUDGE EASTHOM: Please let us know when --

20 MR. LINDNER: Yes. I thought you moved to a different slide.

21 JUDGE EASTHOM: Oh, sorry. Okay.

22 MR. LINDNER: So the last process here, when it's supposed to be
23 going from node 3 back to the first node, node 1 is the box highlighted in
24 green with A equals two times receive.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 JUDGE EASTHOM: And then right below it says -- on my slide,
2 it says, send ID plus 3, comma, A.

3 MR. LINDNER: That's not for the last transition.

4 JUDGE EASTHOM: Oh, okay.

5 MR. LINDNER: So if we look at --

6 JUDGE EASTHOM: So it just --

7 MR. LINDNER: If we look at Slide 20 --

8 JUDGE EASTHOM: You're saying that it just goes -- this just
9 goes to the interactive processor by itself?

10 MR. LINDNER: Well, what we're saying is that when Trefethen
11 wanted to send data to a node, it used a send command.

12 JUDGE EASTHOM: So where did this go, this A equal to
13 receive? Where did they --

14 MR. LINDNER: Well, Petitioner tells you that it goes back to the
15 interactive node. But there is no send command there. So the data itself
16 never gets there.

17 JUDGE EASTHOM: So you're saying that a person wants to use
18 this MATLAB process, and then they enter these commands, and then they
19 never see the result?

20 MR. LINDNER: Well, the assumption here is that they're using
21 -- and it's hard to see because it's not fully boxed in on Slide 24, but
22 Trefethen in the paragraph on Slide 24, it begins process 0. It ends with a
23 command Eval, open paren, cycle, close paren, produces the output. And
24 what that is telling you is that just the value is sent back to the screen for the

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 user. It's not actually sending the data back to the first node.

2 JUDGE EASTHOM: Oh, I see your argument. So your argument
3 is that value is different than data?

4 MR. LINDNER: Correct. And we know that because in --

5 JUDGE EASTHOM: How does that -- what is that -- what's -- so
6 what --

7 JUDGE MURPHY: Well, why is that not within the scope of the
8 claim?

9 MR. LINDNER: Because you can't do anything with just the
10 value. When the master node or the first node gets the data back -- which is
11 what's required for the data to be transferred. When the master node gets
12 that back, it can do something with the data. When it gets just a value back,
13 it can't do anything with just the value.

14 JUDGE MURPHY: That's the further use argument you make.
15 But the claim doesn't say anything about -- excuse me, the master node using
16 that output. It just says receive a result from the third node.

17 MR. LINDNER: Well, at least in the '913 and the '914 cases, they
18 do have claims that require transferring by the peer-to-peer network. And
19 that peer-to-peer network requires transferring data.

20 JUDGE MURPHY: Yes.

21 MR. LINDNER: And so at least under the '913 and the '914 case,
22 there's no data that's being transferred because you wouldn't be -- if you're
23 transferring only a value, then you're not transferring --

24 JUDGE EASTHOM: But you're saying the value A equals 32,

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 that's not data, that's not a -- I thought that was (INDISCERNIBLE) 111
2 something --

3 MR. LINDNER: That's just as Trefethen explains it, and so we
4 need to go by what the reference itself is teaching. When it describes that
5 Eval command, it describes that they've not communicated between
6 processes except to send screen output to the master process. And that's at
7 Exhibit 1006, page 5.

8 And so under Trefethen's teaching, it is only teaching -- it's not
9 teaching transferring the data back, it's only providing a value to the screen.

10 JUDGE MURPHY: Yes, but it --

11 JUDGE EASTHOM: I don't understand how the value gets there
12 if it's not in data form. What do you think? It's just going to transfer an
13 image, or is that what you're saying?

14 MR. LINDNER: I mean, I'm going by what the reference itself
15 teaches. And the reference teaches that they're not transferring, they're not
16 communicating between processes except for screen output. And so again, I
17 mean, that's something that hasn't -- that at least Petitioner hasn't explained
18 is if they're going to contend that the value is data.

19 JUDGE EASTHOM: I don't have any other questions. I think I
20 understand your argument.

21 MR. LINDNER: Judge Murphy, did you have a --

22 JUDGE MURPHY: Yes. So I'm trying to square this with the
23 claim language. The claim requires returning the result. It doesn't say value,
24 it doesn't say data. It says return the result of the second mathematical

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 expression evaluation to the user interface. That's the return result. Excuse
2 me, that's limitation 1.6.

3 1.5.2 says, "Communicate the result of the second mathematical
4 expression evaluation to the first node." Petitioner is saying, yes, that's the
5 interactive process node. So the question is, are you saying returning a
6 result or communicating a result is not satisfied by Trefethen because -- tell
7 me why.

8 MR. LINDNER: Yes. I mean, yes, we are saying it's not satisfied
9 because it's not actually sending the result itself. It's sending a screen
10 output.

11 JUDGE MURPHY: You're saying the screen output that reflects a
12 result is not --

13 MR. LINDNER: Is not the result. The master processor can't do
14 anything with that screen output.

15 JUDGE EASTHOM: Is there any evidence of that?

16 MR. LINDNER: That the master processor can't do anything with
17 the output?

18 JUDGE EASTHOM: Yes. Well, it's --

19 MR. LINDNER: I think it's a plain -- I mean, our position is it's a
20 plain reading of the reference.

21 JUDGE EASTHOM: Okay.

22 JUDGE MURPHY: Well, but they have testimony from Dr. Bajaj
23 that says differently. And it's fairly extensive, and it's corroborated with
24 other documentation and quotes from Menon and Trefethen. So it's a

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 question of how you're reading the claim, right?

2 I mean, what in the claim prohibits the pathway that Petitioner's
3 Counsel explained to us that Menon and Trefethen (INDISCERNIBLE)?
4 What in the claim language is restrictive enough that returning screen output
5 is not satisfactory?

6 MR. LINDNER: Well, I think there's I think two points to your
7 question, Judge. I mean, one is -- again, if it's the result, it's the output. And
8 so you need to be able to process that output at the master would be one
9 point. The other point is that we don't actually know how this Eval function
10 is operating.

11 Petitioners have drawn this nice annotated figure showing that data
12 is returned from the third node to the first node on Slide 24. But that's all,
13 again, being used by process of an Eval command, which is not described in
14 Trefethen.

15 And Petitioner's position is that when you're transferring data
16 between nodes, you're using send and receive. And what's missing from
17 transferring from three to one in Trefethen is any send command. So you're
18 right, there is no evidence in the record, but I don't know what's happening
19 under the hood of Eval.

20 JUDGE MURPHY: But why does the claim require that you know
21 how it happens? All you need to know is that it happens.

22 MR. LINDNER: Well, because we need to know because if it
23 went -- if it backtracked the way that it got there, and that the third node got
24 data from the second node, and it sent the data back to the second node,

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 well, now it's going backwards and going one, two, three, three, two, one.

2 And so therefore it's not going three to one.

3 JUDGE MURPHY: Well, the claim doesn't say, send it directly to
4 the first node. It says communicate the result to the first node. Doesn't
5 matter how it does it.

6 MR. LINDNER: Well, but it does matter how it does it, because if
7 it goes -- if it gets communicated back to the first node through the second
8 node, then it isn't doing -- it isn't performing the one, two, three, one
9 operation.

10 JUDGE MURPHY: Well, one, two, three, one is your
11 nomenclature, it's not what the claim says. The claim says, communicate the
12 result from the third node to the first node. It doesn't say how you do it.

13 MR. LINDNER: Well --

14 JUDGE MURPHY: Right? I mean, the nomenclature is fine
15 because it makes the briefing a little more streamlined, but it's the claim
16 language that matters. That's what I'm struggling with, right? And it doesn't
17 say return the data or the value. It says return the result of the calculation,
18 the second calculation.

19 MR. LINDNER: Right. And under the --

20 JUDGE MURPHY: From the third node to the first node.

21 MR. LINDNER: And under the --

22 JUDGE MURPHY: That's it.

23 MR. LINDNER: -- construction of peer-to-peer network, it does
24 require transferring data the way that the parties have -- the term that the

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 parties have agreed and as it was construed by the District Court.

2 JUDGE MURPHY: I have one more follow-up. If in the patent
3 itself, column 23, right at the top, it's lines 1 to 5. Counsel was --

4 MR. LINDNER: Uh-huh.

5 JUDGE MURPHY: One of the slides Counsel put up, he
6 discussed this. So I want your reaction to that, right? So at the top of
7 column 23, lines 1 to 5, it talks about -- oh, I'll just read it. "A kernel
8 module 206 typically includes program code for interpreting high level code,
9 commands, and/or instructions supplied by a user or a script into low level
10 code such as, for example, machine language or assembly language."

11 And so Counsel's point was, well, look, the patent contemplates
12 using script or pre-programmed code. That's one way to do it, there are
13 others. That's not restrictive, that's open-ended. That's exemplary. And so
14 that's how -- it strikes me, that's how the claim is being -- it says
15 communicate the result to the first node, return the result to the user
16 interface.

17 And one way to do it is with script pre-programmed instructions or
18 any other mechanism that's not in the claim. And you're saying using send
19 and receive instructions or an Eval return call doesn't satisfy that. And so
20 I'm posing the question, why not?

21 MR. LINDNER: Well --

22 JUDGE MURPHY: Why does it matter how it does it as long as a
23 result is being communicated?

24 MR. LINDNER: Well, I think the reason it matters is because of

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 the teaching of the prior art. The prior art is teaching that you're only
2 communicating between the nodes by way of the send and receive. And so,
3 if Trefethen can't communicate back to its first node using its teaching,
4 which is the send and receive, then it can't disclose that limitation.

5 JUDGE MURPHY: So does this boil down to you're saying when
6 Trefethen says return screen output to the master process, which apparently
7 everyone agrees goes back to the interactive process or first node, so it can
8 appear on the user screen. You're saying that's not -- that doesn't satisfy the
9 claim because there's no communication?

10 MR. LINDNER: Because it is not -- the last node is not actually
11 sending it. I mean, again, we don't know how Eval is working. But
12 Trefethen teaches that the only way to communicate between the nodes is by
13 using the send commands.

14 JUDGE MURPHY: But see, that's where I come back to -- so Dr.
15 Bajaj says, it does that because Trefethen teaches you to send the output,
16 right? Send the output to the master process. And the evidence is that
17 master process is the MATLAB process, which sends it back to the
18 interactive processor, which is the first node that interfaces with the user. So
19 you know it's sending it, you just don't know exactly how.

20 MR. LINDNER: Well, again, I mean, that's Dr. Bajaj's
21 interpretation of the --

22 JUDGE MURPHY: Oh, but he's the expert.

23 MR. LINDNER: Right. Right.

24 JUDGE MURPHY: It's his testimony.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 MR. LINDNER: Right.

2 JUDGE MURPHY: You didn't depose him. You don't have an
3 expert. That's the evidence.

4 MR. LINDNER: I understand. But Trefethen teaches, again, that
5 to communicate between the nodes, you're using send and receive. And in
6 the script that they want to use, there's no sending back to the first node.

7 JUDGE MURPHY: Okay.

8 JUDGE EASTHOM: But you said before, I thought your
9 argument was, well, Trefethen does send something. Somehow it sends the
10 result of display result, right? You agree it to send a -- now you -- but you're
11 -- I thought your only distinction was Trefethen doesn't say it's data.

12 MR. LINDNER: Well, Trefethen says that you can use an Eval,
13 but Trefethen tells you that using that eval function does not transfer
14 between nodes. It says that they only send screen output to the master
15 process.

16 JUDGE EASTHOM: Screen output. Okay. So your whole
17 distinction is that screen output is not data?

18 MR. LINDNER: Correct.

19 JUDGE EASTHOM: Is that right?

20 MR. LINDNER: Correct.

21 JUDGE EASTHOM: I mean, okay.

22 MR. LINDNER: On the issue of claim construction -- actually,
23 before I get there, I just want to also touch on the motivation to combine
24 Trefethen and Menon. Trefethen and Menon both are directed or describing

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 a MultiMATLAB process. But Menon describes its MultiMATLAB as a
2 redesigned configuration of Trefethen.

3 It tells us that it's redesigned, that Trefethen was very different or
4 was different than what's being described in the Menon paper. And so
5 Patent Owner's position is that there is no teaching of a rationale to combine
6 Menon and Trefethen together even to achieve the piece together operation
7 of how it would perform the one, two, three, one operation.

8 So I just wanted to at least touch on that. We don't think there's
9 been a rationale articulated as to why that you would combine the two
10 references. And for that reason, if you can't -- there's no motivation to
11 combine. Again, you'd never arrive at the proposed combination, and that
12 would be a fatal issue in all four of the petitions because the combination is
13 used in all four of the petitions on all the grounds.

14 JUDGE EASTHOM: I thought the part of the rationale, sorry, that
15 it was that Menon creates sort of two different improvements to Trefethen.
16 They're both using the MultiMATLAB, but then Menon has these MEX
17 routines and so you can get some more.

18 MR. LINDNER: Yes. I mean, so they are both using
19 MultiMATLAB. And they're both improving -- and what they're doing is
20 they were both improving on MATLAB. But Menon isn't improving.
21 There's nothing to suggest that Menon is improving on Trefethen.

22 JUDGE EASTHOM: Well, they cited two improvements that
23 actually Menon spells out on one of the pages. One was that it --

24 MR. LINDNER: The --

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 JUDGE EASTHOM: That a little bit -- that there's more --

2 MR. LINDNER: Performance and extensibility.

3 JUDGE EASTHOM: Extensibility. Thank you.

4 MR. LINDNER: Yes. Yes. Right. And that's on, it's Exhibit
5 1005, page 2. And again, that section there was -- the beginning of it was
6 describing what Trefethen, the earlier concept of MATLAB, what the
7 improvements it made -- sorry, let me correct myself. Trefethen, the earlier
8 implementation of MultiMATLAB --

9 JUDGE EASTHOM: Right.

10 MR. LINDNER: -- that was describing the improvements that
11 Trefethen made to MATLAB.

12 JUDGE EASTHOM: Right. Made it into MultiMATLAB.

13 MR. LINDNER: It made it into MultiMATLAB. The additional
14 performance and extensibility that Menon then describes and the rest of the
15 paper is describing, are other improvements that are being made to
16 MATLAB, not to the Trefethen MultiMATLAB, but to MATLAB itself. So
17 MATLAB --

18 JUDGE EASTHOM: It's using MultiMATLAB, so why wouldn't
19 they improve?

20 MR. LINDNER: I don't think it is using MultiMATLAB.

21 JUDGE EASTHOM: You don't think Menon's using
22 MultiMATLAB?

23 MR. LINDNER: I think Menon is describing ways to redesign and
24 build a new MultiMATLAB. They use the same terminology, but I think

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 that Menon is describing a new way or a new version of MultiMATLAB.

2 JUDGE EASTHOM: Okay. And how does that defeat the
3 extensibility and the improvements? The other improvement?

4 MR. LINDNER: Well, I mean Menon is coming up with its own
5 improvements. Menon relies on this MEX routine in order to perform the
6 one, two, three, one --

7 JUDGE EASTHOM: Right.

8 MR. LINDNER: -- operation that we were just talking about. The
9 MEX routines weren't available in Trefethen.

10 JUDGE EASTHOM: Right.

11 MR. LINDNER: So again, it's not that Menon is building on
12 Trefethen, it's that Menon is building on MATLAB. And so just because the
13 papers are citing one another isn't a rationale to combine references. I mean,
14 in Menon's abstract, again, Exhibit 1005, page 1, it says, "This paper
15 presents a new MultiMATLAB system designed to provide high
16 performance on microprocessors while maintaining the functionality and
17 usability of the MATLAB environment."

18 So again, Menon is talking about creating some new features for a
19 MultiMATLAB configuration. The fact that they are both using
20 MultiMATLAB, I mean, it makes sense that they're both using that
21 terminology because they were similar authors. But just because they're
22 using the same terminology, just because there's an overlap of authors,
23 doesn't provide a motivation to combine the references.

24 JUDGE RAEVSKY: Counsel?

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 MR. LINDNER: Yes.

2 JUDGE RAEVSKY: Can I clarify? Did you say that Trefethen
3 does not employ the MEX routines?

4 MR. LINDNER: That is what Menon says.

5 JUDGE RAEVSKY: Okay. Because I believe it does mention
6 MEX, at least on page 10 of Trefethen. Can you clarify why that's not
7 relevant to the MEX routines in Menon?

8 MR. LINDNER: Could you just help me? You said on page 5 of
9 Trefethen.

10 JUDGE RAEVSKY: On page 10 of Trefethen, third full
11 paragraph, it refers to the standard MATLAB Fortran C++ interface system
12 known as MEX. I'm just wondering how Menon's implementation of MEX
13 might differ in a relevant way for assessing the combinability of these
14 references.

15 MR. LINDNER: I'm not fully certain what that reference is. I will
16 look into it in Trefethen. But my rationale and my reasoning for saying that
17 Trefethen did not employ -- well, I think I might know the clarification now.
18 Trefethen -- sorry. Take that back. Menon on Exhibit 1005, page 14 when
19 discussing Trefethen says it does not permit extensions via parallel MEX
20 routines as described in section 4. So it may be that Trefethen was using a
21 MEX command, but it was not using a MEX command via parallel routines.

22 JUDGE RAEVSKY: Okay. Understood.

23 JUDGE EASTHOM: And just to be clear, because I want to ask
24 your friends too, the way I read the petition was that they're using Menon

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 basically for most of the limitations, and then they use the Trefethen for this
2 '321 business. Is that to show an example of the '321 specific example?

3 MR. LINDNER: That's my understanding of how they're trying to
4 combine the --

5 JUDGE EASTHOM: Okay. Okay. Thanks.

6 MR. LINDNER: But again, we get back into that script that we
7 were talking about.

8 JUDGE EASTHOM: Right.

9 MR. LINDNER: We don't think that the Trefethen script
10 employed on the Menon system would function as it's being described.

11 JUDGE EASTHOM: Okay.

12 MR. LINDNER: With respect to claim construction, there was a
13 lot of discussion from Petitioner about portions of the specification. But I
14 think the grounding principle here is that we need to start and look at the
15 claims themselves. And I also think there's a dispute as to what is -- I think
16 it was phrased as the dispute between the parties is what is the hardware
17 processor.

18 And we don't think that that's the dispute. The dispute is the
19 processor with or comprising a plurality of cores. And so, if you follow the
20 general principles of claim construction, the claim terms are provided in
21 their plain and ordinary meaning. And there's two exceptions to that.
22 Disavowal or an explicit act of lexicography.

23 Neither of those are present in this situation. Petitioner hasn't
24 asserted that Patentee acted as their own lexicographer when preparing the

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 application. And so with neither of those exceptions applying, the portions
2 of the specification that were cited to and are referenced throughout, those
3 are just exemplary embodiments, or just examples.

4 But that's nothing to say that that language from the specification
5 should be imported into the claims. The claim language is very clear. It
6 talks about a single processor with or in regards to --

7 JUDGE MURPHY: Where does the claim say a single processor?

8 MR. LINDNER: Sorry. Sorry. It says a hardware processor.

9 Thank you.

10 JUDGE MURPHY: Right. It doesn't say single processor.

11 MR. LINDNER: Correct. Thank you for the correction, Judge. It
12 says a hardware processor, but it's referring to a hardware processor with or
13 comprising a plurality of cores. And so, we think the dispute is, are the
14 cores within the processor, or can you take discrete processors, which is the
15 case of the RS6000 where there's 4, 6, 8, or 12 processors that are mounted
16 to that board, can you take those individual processors and call that a
17 plurality of cores because each processor may have one core in it? And so
18 that's where we think the dispute is, lies.

19 JUDGE RAEVSKY: Counsel?

20 MR. LINDNER: Yes.

21 JUDGE RAEVSKY: Doesn't a hardware, the word "a," a
22 hardware processor imply one or more hardware processors? And if so, how
23 would you address that in the context of your argument?

24 MR. LINDNER: Well, it could. I mean, yes, a could be one or

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 more, but again, it's still with a plurality of processing cores. So if you have
2 one or you have more than one, each has to have a plurality of processing
3 cores. And so --

4 JUDGE RAEVSKY: Does the claim explicitly require each? I
5 don't have it in front of me this second.

6 MR. LINDNER: Sorry, you drifted off a little bit at the end of
7 your question.

8 JUDGE RAEVSKY: Does the claim explicitly require each?
9 Does it recite each?

10 MR. LINDNER: It requires a second hardware processor with a
11 plurality of cores, and a third hardware processor with a plurality of
12 processing cores.

13 JUDGE RAEVSKY: So currently you read that to mean, one or
14 more hardware processors with a plurality of cores without requiring each
15 since it's not recited?

16 MR. LINDNER: Well, I think the with tells you the location of the
17 cores. Again, if we kind of step through some of the maturations here, the
18 proposal from Petitioner for their construction was one or more single-core
19 or multi-core microprocessors with a plurality of processing cores.

20 So I think this is kind of what you're getting at, Your Honor, if you
21 replace a hardware processor with one or more. But that proposed
22 construction has a problem in that you would have the possibility of having
23 one single-core with a plurality of processing cores.

24 I mean, I don't understand how you can have one single-core

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 microprocessor with a plurality of processing cores. And so we think that
2 when you view it in -- again, in reading the patent as a whole that the claim
3 language itself is kind of telling you, look, yes, there can be one processor,
4 there can be multiple processors, but what was specifically claimed here was
5 a processor with a plurality of cores.

6 It makes a distinction because when it refers earlier in the claim to
7 the first processor, it just says a first hardware processor. It isn't limiting it
8 by whether or not there's a plurality of cores in it. And so if you aren't tying
9 the plurality of cores to the hardware processor claim language, then any
10 hardware processor would satisfy any one of those first, second, or third
11 hardware processors.

12 JUDGE EASTHOM: But you agree that the -- you seem to
13 concede that the specification, your patent specification provides for the
14 reading that Petitioner is using. You've just said that those are just
15 exemplary embodiments, and that it's not restricted to those. But they do
16 provide a broad reading basis for that claim, right?

17 MR. LINDNER: I mean, yes, they provide examples, yes. But
18 we're not under the canons of claim construction, we're not supposed to be
19 reading limitations or embodiments from the specification of the claims,
20 right?

21 JUDGE MURPHY: Well, that's their point, right? The spec says
22 single-core or multi-core.

23 MR. LINDNER: I mean, but they haven't -- I mean, we -- I don't
24 think there's been an argument that we act in a -- the Patentee acted as its

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 own lexicographer. And so if that's the case, then we shouldn't --

2 JUDGE MURPHY: I think that's also their point. That didn't
3 happen, so it's open-ended. It's exemplary. I mean, why should we restrict?
4 You're limiting the claim to a single multi-core processor. That's your
5 argument. Why should we do that?

6 MR. LINDNER: I think the claim language itself is dictating that.

7 JUDGE MURPHY: Well, the claim language doesn't say single,
8 and it doesn't say multi-core.

9 MR. LINDNER: It says a plurality of cores.

10 JUDGE MURPHY: Right.

11 MR. LINDNER: Right?

12 JUDGE MURPHY: Yes, that's their point. So why should we
13 limit it to a single multi-core processor? Which is only one of several
14 examples described in the patent.

15 MR. LINDNER: Well, I think the other examples -- as I kind of
16 just said, I mean, you can't have one single microprocessor with a plurality
17 of cores. So I mean, they've come up with taking --

18 JUDGE EASTHOM: Well, they made a more subtle distinction.
19 They said a microprocessor might be a core, but a processor can have
20 several microprocessors or several -- a processor is something that can be a
21 bunch of different microprocessors or cores. I thought they were -- you're
22 saying every time it says processor, it has to be a single microprocessor.

23 MR. LINDNER: Well, I'm just saying that under their proposed
24 -- their proposed construction has faults in it, in that their proposed

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 construction would present a scenario where the construction is, I think not
2 -- it's illogical. Their proposed construction would account for a situation
3 where you could have one single-core microprocessor with a plurality of
4 cores.

5 JUDGE EASTHOM: I don't think so because they're not
6 construing a single processor.

7 MR. LINDNER: But, I mean, that's their -- in their reply, that's
8 their proposed construction.

9 JUDGE EASTHOM: For a single processor?

10 MR. LINDNER: For the term in dispute, a hardware processor
11 with a plurality of cores, their proposed construction is one or more single-
12 core or multi-core microprocessors with a plurality of processing cores.

13 JUDGE EASTHOM: Okay.

14 MR. LINDNER: That's their reply on pages 1 to 2.

15 JUDGE MURPHY: Yes. And that's in column 7 at lines 15 to 18.

16 MR. LINDNER: Right. But again, the point is, is that -- I mean,
17 there's no way to -- I mean, that is some language from the specification, but
18 there's no way to have one single-core microprocessor with a plurality of
19 processing cores.

20 JUDGE MURPHY: Yes, that's nonsensical.

21 MR. LINDNER: Right. And so, the point is, is that yes, there are
22 some descriptions and explanations in the specification, but that's not -- we
23 can't -- those were just examples, and I don't know how we can have a claim
24 construction that would result in that situation.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 JUDGE EASTHOM: Okay.

2 MR. LINDNER: The last point I just wanted to briefly touch on
3 which was raised earlier is we would also agree that -- so whoever asked the
4 question earlier -- that the card is not a substrate, or that a card is not a
5 semiconductor substrate with respect to residing on the same die.

6 And I do think that that was the argument that we, as we perceived
7 it from the briefing, was that Petitioner was arguing to say that the RS6000
8 card substrate is what they were equating with a die. And we disagree with
9 that for the reasons that are articulated in our briefing, but just wanted to
10 kind of address that question. With that, I'll reserve the rest of my time. Do
11 you have any other questions?

12 JUDGE EASTHOM: I don't. Thanks for asking. Anybody?

13 JUDGE RAEVSKY: Yes. I have one question on that. So on
14 page 9 and 10 of the reply, Petitioner says that you acknowledge that the
15 same die means a single semiconductor substrate. Is that a fair
16 characterization of your position?

17 MR. LINDNER: I don't think that was.

18 JUDGE RAEVSKY: If you need to find it, that's the very last
19 sentence on the bottom of page 9, continuing onto the top sentence of page
20 10.

21 MR. LINDNER: Yes. And I think in our surreply, we said that
22 that was not the case. On pages 4 to 5 of our surreply, we said that we did
23 not consider card level mounting to be the die that's required by those
24 dependent claims.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 JUDGE RAEVSKY: Thank you.

2 JUDGE EASTHOM: But you don't dispute that a die is a -- I
3 mean, a semiconductor substrate, do you?

4 MR. LINDNER: No. No. Right. I mean, yes, we've said that a
5 die is a semiconductor substrate, we just don't think that the card --

6 JUDGE EASTHOM: You don't think a card is a semiconductor?

7 MR. LINDNER: A card or the substrate of a card is a
8 semiconductor substrate.

9 JUDGE EASTHOM: Right. Okay.

10 MR. LINDNER: Correct.

11 JUDGE EASTHOM: The way I read their petition was they also
12 had an obviousness argument. They said that semiconductor substrates with
13 multiple processor cores were known. And I don't think there's any dispute
14 about that. They cited Exhibit 1051. And then they said, well, given that
15 these are all on the same card.

16 And then they cited a CCPA case that said, in making things out of
17 many -- making many things into one would've been obvious, how do you
18 respond to that? It seems they're just making an integral argument.

19 MR. LINDNER: Yes. So I don't recall if those exhibits were cited
20 in the petition. I'd have to go back and look at the --

21 JUDGE EASTHOM: I thought they were, but I could be wrong.

22 MR. LINDNER: Yes, I'd have to go back and look to see.

23 JUDGE PESLAK: They're definitely cited in the petition.

24 MR. LINDNER: Okay. Okay. Thank you. As far as the

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 combination, I think the case that they're relying on is a mechanical
2 combination of multiple parts into one. Not a semiconductor, but even the
3 teaching or suggestion that the processors of the RS6000 could be combined
4 into one defeats the entire purpose of the RS6000.

5 RS6000 talks about this SMP configuration. It's a node
6 configuration about upscaling and downscaling. And so if you wanted to
7 have more processors, you could put more cards into the system. If you
8 wanted less cards, you could take some of the cards out. So each card had, I
9 think, four processors on it.

10 So if you needed eight processors, you could put two cards in. But
11 if you're combining all of these onto now one semiconductor die, now you
12 don't have the ability in that.

13 JUDGE EASTHOM: Or you could just go buy a die with more on
14 there, right?

15 MR. LINDNER: I mean, I don't think you're not -- scaling it up is
16 -- allows for in the teaching of the reference.

17 JUDGE EASTHOM: Okay. But you don't dispute that there were
18 -- that multiple processors on the die was known.

19 MR. LINDNER: I think. Right. I mean, they've cited some
20 references about that, yes.

21 JUDGE EASTHOM: Okay. I appreciate. Thank you.

22 MR. LINDNER: Thank you.

23 JUDGE EASTHOM: You have 12:45 left for rebuttal. You can
24 begin whenever you're ready, Mr. Ehmke.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 MR. EHMKE: Thank you, Your Honor. I'm trying to work
2 through the technical difficulties here. The screen is not displaying. Got it.
3 Got it. I got it. We're good. So just real briefly, the first thing I want to
4 address is one of the arguments Patent Owner made about the Trefethen
5 teaching of only being sent and received as the only thing that they teach,
6 passing information back and forth with respect to reference.

7 Specifically, the reference to the Eval command. I'm looking at,
8 and I have on the screen here Exhibit 1006. And I believe this is page 4.
9 Let's double-check here. Yes.

10 JUDGE MURPHY: Did you say page 4?

11 MR. EHMKE: Yes. Page 4 of 14. And there's this kind of this
12 paragraph in the center here, right below, we see the ANS set of times. We
13 see in the above examples and keeping with our orientation toward SPMD
14 programming, each command passed to Eval is evaluated on all the
15 processes.

16 Alternatively, one can select a subset of the processes by passing
17 two arguments to the Eval command. The first being the vector of process
18 IDs. Thus, it gives the example, Eval four space five, and extends this task
19 of perform the Hildebrand equation evaluation. That's being passed to nodes
20 4 and nodes 5.

21 And so we have a command in the SPMD programming language
22 described in Trefethen where you can actually send something directly to
23 another node. It's not just the send and receive. Eval also lets you do this.
24 Eval also lets you target a particular node. So we have that teaching within

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 Trefethen as well. That's how you can send tasks and commands between
2 different nodes.

3 JUDGE MURPHY: Yes. I mean, the point I'm focused on is how
4 is the output or result from the code sent or communicated in the language of
5 the claim? How is that communicated to the first node? The evidence, as I
6 understand it, is Dr. Bajaj says it's returned to the, quote, master process.
7 And a person of ordinary skill would know it goes to the first node or the
8 interactive process in the Menon Trefethen MultiMATLAB system. Yes.

9 MR. EHMKE: So is your question why is it going to a particular
10 node or how is it going from node to node?

11 JUDGE MURPHY: How? Because Counsel is saying Trefethen
12 doesn't tell you.

13 MR. EHMKE: Which I guess I find odd because as you pointed
14 out during the questioning, is Trefethen tells us we're going to be producing
15 output. We get this output of one. We get this output of two. We get this
16 output of four. We get graphs being plotted and sent to the user screen.

17 We have the monitor -- user monitoring the results of the
18 calculations. And so to reach that conclusion is to say that Trefethen doesn't
19 send the results. It doesn't? When it specifically says, output the result as
20 soon as it's ready, gives us example code where it shows what the results of
21 the calculations are, and says it's going to produce that output.

22 And it's telling us that it's being sent to the user screen so the user
23 can monitor the results. Our expert looked at that and reached the
24 conclusion that the prior art is teaching that we get that value of A equals

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 four at the third node. We're going to produce that output and send it to the
2 user's screen.

3 Trefethen is teaching that we have that output being sent from
4 node 3 to the first node. We have the cluster node module taught in Menon,
5 which handles all the communication layers, the MEX routines, the
6 intermediate table that puts the information onto the network. We've got
7 Menon's teaching -- excuse me. I'm going to go to slide -- that's the repeat
8 on Slide 38.

9 So we have all these teachings together along with our expert's
10 understanding of the pipeline process of the peer-to-peer networking,
11 looking at this code and reaching the conclusion of the results just don't go
12 nowhere. There's been no point and purpose to the system. The results are
13 being sent to the user's screen.

14 We're getting A equals four, just calculated at node 3. The user's
15 screen is located at node 1. The result is at node 3 and shows up on the user
16 screen at node 1. The claim simply says we need to return the result to the
17 user's screen.

18 JUDGE MURPHY: And in Menon and Trefethen, that's being
19 done through the Eval command?

20 MR. EHMKE: The Eval command is one of the ways you can
21 kick off the process. So the Eval command says I want you to evaluate
22 script M, which is that example.

23 JUDGE EASTHOM: Does Slide 26 have an example of that?

24 MR. EHMKE: Slide 26. Yes. On Slide 26, they have the example

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 of the cycle.m file. And so, the way the user will kick this off on the
2 interactive process is they'll say Eval cycle M. Cycle M is then sent to all
3 the other nodes for them to then perform their role in it. So at cycle M, at
4 the first node, the first node asks itself, who am I? Which ID am I?

5 Am I ID zero? Am I ID one? Am I the last process? And so then
6 it performs its portion of the code. And so if it's ID equals zero, it's the first
7 process. It's going to -- I'm now on Slide 22. That first process, ID zero, is
8 going to send its intermediate result. But we also get to monitor the result
9 because we see A equals one. Right?

10 Again, that's what Trefethen is teaching. We're going to be
11 sending our results and producing those results so the user can monitor.
12 That's why we get the A equals one. And then it goes to the next node. And
13 the next node performs its calculation, it doubles it. It turns into two.

14 And we know it turned into two because we have to monitor it as it
15 happens. The result is sent as soon as it's ready. We get the A equals two.
16 It's sent to the user's screen, and we're sending the data as necessary because
17 we might want to plot the graphs. Judge Murphy, it looks like you had a
18 question.

19 JUDGE MURPHY: Yes. Counsel, can you go to Trefethen
20 bottom of page 7? And I guess it carries over to the top of page 8 too. The
21 subtitle is number -- it's section 3, multi-processor graphics.

22 MR. EHMKE: Yes.

23 JUDGE MURPHY: And this is one of the citations from your
24 briefing.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 MR. EHMKE: Yes.

2 JUDGE MURPHY: Referenced some of this anyway.

3 MR. EHMKE: Yes. Correct.

4 JUDGE MURPHY: In particular that the -- it may be desirable to
5 produce plots in a distributed fashion that are then sent to the user's screen.
6 And that's useful when one wishes to monitor the progress of computations
7 --

8 MR. EHMKE: Yes.

9 JUDGE MURPHY: -- on several processors graphically. So that's
10 what you talked about in your briefing. Can you explain how that works?
11 In context of the claim requirement, right? To return the result --

12 MR. EHMKE: Correct. Yes.

13 JUDGE MURPHY: -- to the first node, and then to the user
14 interface.

15 MR. EHMKE: Right. Because as you pointed out, we have the
16 calculation, I guess we're caring about what's happening at the third node.
17 So the third node is getting a result. It's performing a mathematical
18 calculation expression evaluation to generate a result. Then that result is
19 returned to the first node. Then the first node provides that result to the user
20 interface. Right?

21 So first off, there's no further use being required there at all. We're
22 just have that calculation that occurs at the third node. And then it's getting
23 sent to the first node ostensibly to be displayed to the user. It's being sent to
24 the user interface. So Trefethen teaches, and yes, we rely heavily on this

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 section because there's this concept of, this is useful when one wishes to
2 monitor the progress of your calculation.

3 Which means we want to see the results, including the intermediate
4 results, right? If we're monitoring the progress of the calculations, we're not
5 just always looking at the final result. We might be looking at an
6 intermediate reason. And in the sample code in Trefethen, there's, I think,
7 considering six processors.

8 It's how we get from 1 to 32 on it. But we definitely see that when
9 we get to that third node, we're monitoring the result of that third node. We
10 get the value of A equals four is being provided to the user. We're
11 producing the output. A equals four. And that's the output from that third
12 node.

13 JUDGE MURPHY: And how do you know that from Trefethen?

14 MR. EHMKE: How do I know that from Trefethen? Because of
15 the calculations being performed. We start with the value of A equals one.
16 But our output is four. Okay? But we have these different nodes performing
17 the math. And so at the first node, A equals one. Then, that value is sent
18 using the send command to the first node, which would be node 2 in the
19 process, right? The computer science, then we've got starting with zero
20 versus one.

21 JUDGE MURPHY: Understood.

22 MR. EHMKE: Right. So that value of one is being sent to the
23 next node, which performs a mathematical computation. In this case, it's
24 multiplying it by two. So now the A equals two. Well, that's not the output

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 I'm looking at right now. Sure, I get the A equal two as an output, but I then
2 get another output.

3 That value of two is being sent from that second node to the third
4 node, and being multiplied by two again. So now I know A equals four.
5 Logically, as I read the code, A equals four. And I get an output produced of
6 A equals four. And the math and the computer science code tells me that
7 where did that happen at?

8 It started at node 1, got multiplied at node 2. It got multiplied at
9 node 3, A equals four. And then I get an output at the interactive process of
10 what? Of A equals four. That was the value that came from the third node.
11 That's how Trefethen teaches it, is the code walks through what happens
12 with the send and receive.

13 The code walks through and gives us comments and code in the
14 code itself of what happens at the first process, what happens in the middle
15 process, what happens at the last process. We have that commentary. We
16 have the closing paragraph by Trefethen describing what happens, that it
17 starts at the -- at process zero.

18 It gets doubled and sent to the next process. And then it produces
19 that the output A equals four. And then I have my expert's testimony
20 applying the knowledge of a POSITA, analyzing that code, and also
21 reaching the conclusion as described in Trefethen of A equals four is being
22 sent back to the first node.

23 JUDGE MURPHY: Setting aside the expert testimony for a
24 moment. In Trefethen --

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 JUDGE EASTHOM: Hold one second. Sorry. I just want to let
2 him -- we're going to go into extending more time if --

3 JUDGE MURPHY: Sure.

4 JUDGE EASTHOM: -- you -- help yourself. Please. I want to
5 just keep track.

6 JUDGE MURPHY: So on pages 7 and 8 of Trefethen, you've
7 given one example from the code where A starts as one and it's doubled
8 sequentially.

9 MR. EHMKE: Yes.

10 JUDGE MURPHY: And it says the user can monitor that on the
11 screen. And then on page 8, bottom of page 7, page 8, it gives a different
12 example, the so-called "Grcar" matrix, whatever that is. But it's your point
13 that we know it must go to the first node because the user can see the results
14 being displayed --

15 MR. EHMKE: Yes.

16 JUDGE MURPHY: -- in this fashion?

17 MR. EHMKE: And it's telling that it's sending the data to the
18 master process as soon as it's ready, which is where the user is. And then it
19 gives these examples of we're going to plot graphs and show you the
20 immediate results. We're going to show you A equals four. And we're
21 sending the results as soon as they're ready to the master process, which is
22 where the user is sitting. That's what Trefethen tells us.

23 JUDGE MURPHY: And is using an Eval MEX routine within the
24 scope of the claim to execute that last part of the function?

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 MR. EHMKE: Yes. I mean, because the claims -- one of the
2 claims says is that the nodes are awaiting instructions. And the Eval
3 command in the prior art is one way of distributing the instructions to all the
4 nodes. You say Eval, cycle M, and then that script that we see gets
5 distributed out to them. So Eval is one way to kick off the whole process.

6 JUDGE MURPHY: And is that within the scope of the claim?

7 MR. EHMKE: Yes. I guess I'm not -- yes.

8 JUDGE MURPHY: The language communicate the result to the
9 first node.

10 MR. EHMKE: Yes. Yes. And I would say (INDISCERNIBLE)
11 more specific code in the cycle M is specifically showing we're using the
12 different SPMD messaging techniques to effectuate the communicating the
13 results.

14 JUDGE MURPHY: Got it. Thank you.

15 MR. EHMKE: Yes. I had two other issues. I don't want to take
16 up too much more time If I don't have it allotted.

17 JUDGE EASTHOM: Please try to wrap it up shortly because
18 we're going to extend the time to your friend.

19 MR. EHMKE: I just want to focus on, this happened in the
20 briefing and it's happening here today as well, is processor versus
21 microprocessor. But the claim is about a processor. And the specification
22 then describes a processor in terms of a microprocessor. The claim does not
23 say one microprocessor. It doesn't say a microprocessor.

24 It says processor and the specification draws a distinction between

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 those terms. And then the last thing, the purported illogic about the
2 proposed claim construction. We actually addressed that in our reply
3 specifically. We walked through here. I've got the Petitioner's reply on page
4 8 where we showed that this language contemplates all these different
5 permutations, one of which could be a processor with one single-core
6 microprocessor.

7 And then we said, the claim language though specifically excludes
8 that. So there's this description of all these different permutations. But we
9 recognize that the claim excluded the scenario where that if you have one
10 single-core microprocessor, that that fell outside the scope of the claim. So
11 we don't believe it was illogical. We specifically addressed that point.

12 JUDGE EASTHOM: I don't think there's any more questions.
13 Thank you very much, Counsel.

14 MR. EHMKE: Thank you, Your Honor.

15 JUDGE EASTHOM: Appreciate your input. I'll add 3:40 to your
16 friend. I shorted some time also I have to add. Okay. You really had 12:45,
17 so I have to add -- why did I say 3:40? 3:36.

18 MR. LINDNER: Yes. 16:30.

19 JUDGE EASTHOM: It'll be another four minutes.
20 (INDISCERNIBLE). Oh, sorry, you may begin.

21 MR. LINDNER: Thank you, Your Honor. Just a few brief points.
22 With respect to the Eval command, which is what was just discussed. Yes.
23 So that's discussed on page 6 -- Sorry, page 3 of Exhibit 1006 under the
24 heading 2.1. And that's what I've got up on the screen.

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 And that's where there's this discussion of the Eval, I think, four or
2 five in the command that was just discussed. But when you continue
3 reading that section, when you get to section 2.2, which is the put and get,
4 that is where Trefethen tells the reader that so far we have not communicated
5 between processes except to send screen output to the master process.

6 So when it's discussing the Eval command, Trefethen makes a
7 point to distinguish between put and get, and then send and receive, which
8 come below in section 2.3, from the Eval command. Which, again, is the
9 discussion we were having before about is Eval sending, communicating
10 back, or what is it communicating back?

11 Trefethen is telling us that except for screen output, they haven't
12 communicated between the nodes. We don't actually know the architecture
13 of Trefethen, because Trefethen doesn't describe the architecture. And so
14 we don't know the configuration of how it was being described as Eval.

15 The figure with the different MultiMATLAB scenarios, that is
16 from Menon. But that's not from Trefethen, and so we don't know when
17 Trefethen says the screen output is returned to the master process. We don't
18 know what that architecture is because Trefethen didn't go into that detail.

19 JUDGE EASTHOM: But regardless, this goes back to your
20 argument that the screen output is not data, right?

21 MR. LINDNER: Correct. Correct.

22 JUDGE EASTHOM: Okay.

23 MR. LINDNER: Correct. And then the only other point that I
24 wanted to just quickly touch on, it was the last point about the claim

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

1 language and the illogical nature. While they may have said that the claim
2 excluded that scenario in their reply briefing on page 80, the proposed
3 construction that they're offering would still allow that scenario to occur.

4 JUDGE EASTHOM: I'm sorry, say that again, please.

5 MR. LINDNER: So they tried to walk back this example about the
6 single processor with a plurality of processing cores on page 8 of their reply
7 brief. But the construction, they didn't change their proposed construction.
8 And so that illogical scenario still results if Petitioner's proposed
9 construction is adopted.

10 JUDGE EASTHOM: Well, I thought their point was they captured
11 all your disclosures at that paragraph except for one, which is illogical to the
12 claim language. So your claim language is excluding that specific
13 embodiment.

14 MR. LINDNER: But the proposed construction they still offer
15 would allow for that --

16 JUDGE EASTHOM: Okay.

17 MR. LINDNER: -- construction --

18 JUDGE EASTHOM: Well --

19 MR. LINDNER: -- or that scenario. And so my point is, is that if
20 they thought that there was something that needed to be distinguished, then
21 they should have changed their proposed construction as well. Because right
22 now, their proposed construction would still permit an illogical reading of
23 the claim.

24 JUDGE EASTHOM: Okay. Or did you have more? I'm sorry.

IPR2025-00913 (Patent 11,570,034)

IPR2025-00914 (Patent 12,021,679)

IPR2025-00915 (Patent 11,563,621)

IPR2025-00916 (Patent 11,811,582)

1 MR. LINDNER: No. Nothing further.

2 JUDGE EASTHOM: Do you have any more? Anybody? Okay.

3 Great. Well, I just want to thank, on behalf of the panel, both parties'

4 excellent presentation. That will help us -- it will help us resolve this. We

5 appreciate that.

6 (Whereupon, the above-entitled matter went off the record at 12:14

7 p.m.)

IPR2025-00913 (Patent 11,570,034)
IPR2025-00914 (Patent 12,021,679)
IPR2025-00915 (Patent 11,563,621)
IPR2025-00916 (Patent 11,811,582)

PETITIONER:

Andrew Ehmke
David McCombs
Dan Smith
Dagim Tilahun
HAYNES AND BOONE, LLP
andy.ehmke.ipr@haynesboone.com
david.mccombs.ipr@haynesboone.com
dan.smith.ipr@haynesboone.com
dagim.tilahun.ipr@haynesboone.com
Brian Ferguson

Brian Ferguson
Chaoxuan Liu
WINSTON & STRAWN LLP
beferguson@winston.com
ccliu@winston.com

James Kappos
jwk92657@gmail.com

PATENT OWNER:

David Lindner
Jon Gurka
CROWELL & MORING, LLP
dlindner@crowell.com
jgurka@crowell.com

Reynaldo Barcelo
BARCELO, HARRISON & WALKER, LLP
rey@bhiplaw.com