PTO/SB/08a (07-09)
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	4

Complete if Known	
Application Number	NEW
Filing Date	
First Named Inventor	Jungmin Ha
Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	1630-1332PUS2

U.S. PATENT DOCUMENTS

Examiner initial *	Cite No.	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US-2009/0205712 - A1	08-20-2009	COUSINS	
	2	US-2011/0100459 - A1	05-05-2011	YOON et al.	
	3	US-2011/0275175 - A1	11-10-2011	MINSEK et al.	
	4	US-2012/0298175 - A1	11-29-2012	VAN ROOSMALEN et al.	
	5	US-2012/0318340 - A1	12-20-2012	HENG et al.	
	6	US-2014/0073105 - A1	03-13-2014	ISOGAI	
	7	US-2014/0299187 - A1	10-09-2014	CHANG et al.	
	8	US-2015/0086729 - A1	03-26-2015	Gortzen et al.	
	9	US-2015/0129037 - A1	05-14-2015	NAM et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initial *	Cite No. 1	Foreign Patent Document Country[3] Code	Number[4] Kind Code (if known)[5]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
	10	KR	10-1442011 - B1	09-29-2014			☐
	11	KR	10-2011-0059366 - A	06-02-2011			☐
	12	KR	10-2012-0120260 - A	11-01-2012			☐
	13	KR	10-2015-0053551 - A	05-18-2015			☐
	14	CN	103703567 - A	04-02-2014			☐
	15	JP	2000-340812 - A	12-08-2000			☐

Examiner Signature		Date Considered	

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not Considered. Include copy of this form with next communication to applicant. 1. Applicant's unique citation design number (optional). 2 See Kinds Codes of USPTO patent Documents. at www.uspto.gov or MPEP 901.04. 3. Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4. For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5. Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. 6. Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450 Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.
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Sheet	2	of	4

Complete if Known	
Application Number	NEW
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First Named Inventor	Jungmin Ha
Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	1630-1332PUS2

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FOREIGN PATENT DOCUMENTS

Examiner Initial *	Cite No. 1	Foreign Patent Document Country[3] Code	Number[4] Kind Code (if known)[5]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
	16	WO	2009/094578 - A2	07-30-2009			
	17	JP	2009-295715 - A	12-17-2009			
	18	WO	2010/151478 - A1	12-29-2010			
	19	JP	2010-186862 - A	08-26-2010			
	20	JP	2011-181963 - A	09-15-2011			
	21	JP	2011-512689 - A	04-21-2011			

Examiner Signature		Date Considered	

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	3	of	4

Complete if Known	
Application Number	NEW
Filing Date	
First Named Inventor	Jungmin Ha
Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	1630-1332PUS2

U.S. PATENT DOCUMENTS

Examiner initial *	Cite No.	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initial *	Cite No. 1	Foreign Patent Document Country[3] Code	Number[4] Kind Code (if known)[5]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
	22	WO	2013/094052 - A1	06-27-2013			
	23	JP	2014-203999 - A	10-27-2014			
	24	JP	2014-204128 - A	10-27-2014			
	25	JP	2014-523653 - A	09-11-2014			
	26	JP	2014-53452 - A	03-20-2014			
	27	CN	201812825 - U	04-27-2011			

Examiner Signature		Date Considered	

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	4	of	4

Complete if Known	
Application Number	NEW
Filing Date	
First Named Inventor	Jungmin Ha
Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	1630-1332PUS2

U.S. PATENT DOCUMENTS

Examiner initial *	Cite No.	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initial *	Cite No. 1	Foreign Patent Document Country[3] Code	Number[4] Kind Code (if known)[5]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
	28	CN	203760493 - U	08-06-2014			
	29	EP	2787541 - A1	10-08-2014			
	30	EP	2797124 - A1	10-29-2014			

Examiner Signature		Date Considered	

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not Considered. Include copy of this form with next communication to applicant. 1. Applicant's unique citation design number (optional). 2 See Kinds Codes of USPTO patent Documents. at www.uspto.gov or MPEP 901.04. 3. Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4. For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5. Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. 6. Applicant is to place a check mark here if English language Translation is attached.

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PTO/AIA/15 (03-13)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	1630-1332PUS2
First Named Inventor	Jungmin HA
Title	SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [✓] **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. [ ] **Applicant asserts small entity status.** See 37 CFR 1.27
3. [ ] **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. [✓] **Specification** [*Total Pages* 59] Both the claims and abstract must start on a new page. *(See MPEP § 608.01(a) for information on the preferred arrangement)*
5. [✓] **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 18]
6. **Inventor's Oath or Declaration** [*Total Pages* 3] *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   - a. [ ] Newly executed (original or copy)
   - b. [✓] A copy from a prior application (37 CFR 1.63(d))
7. [✓] **Application Data Sheet** ** See note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. [ ] **CD-ROM or CD-R** in duplicate, large table, or Computer Program (*Appendix*)
   - [ ] Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** (*if applicable, items a. – c. are required*)
   - a. [ ] Computer Readable Form (CRF)
   - b. [ ] Specification Sequence Listing on:
     - i. [ ] CD-ROM or CD-R (2 copies); or
     - ii. [ ] Paper
   - c. [ ] Statements verifying identity of above copies

ADDRESS TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**

ACCOMPANYING APPLICATION PAPERS

10. [ ] **Assignment Papers** (cover sheet & document(s)) Name of Assignee
11. [ ] **37 CFR 3.73(c) Statement** (*when there is an assignee*) [✓] **Power of Attorney**
12. [ ] **English Translation Document** (*if applicable*)
13. [✓] **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    - [ ] Copies of citations attached
14. [ ] **Preliminary Amendment**
15. [ ] **Return Receipt Postcard** (*MPEP § 503*) (*Should be specifically itemized*)
16. [ ] **Certified Copy of Priority Document(s)** (*if foreign priority is claimed*)
17. [ ] **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. [✓] **Other:** PTO/AIA/82A - Transmittal for Power of Attorney

***Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS

[✓] The address associated with Customer Number: 02292 **OR** [ ] Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone		Email	

Signature	DAVID A. BILODEAU USPTO #42,325	Date	JUL 06 2017
Name (Print/Type)	Esther H. Chong	Registration No. (Attorney/Agent)	40953

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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BFP

PTO/SB/17 (03-13)
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FEE TRANSMITTAL

Complete if known	
Application Number	NEW Conf. No.: N/A
Filing Date	Concurrently Herewith
First Named Inventor	Jungmin HA
Examiner Name	Not Yet Assigned
Art Unit	Not Yet Assigned
Practitioner Docket No.	1630-1332PUS2

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

TOTAL AMOUNT OF PAYMENT ($) 1,600.00

METHOD OF PAYMENT (check all that apply)

☐ Check ☑ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 02-2448 Deposit Account Name: Birch, Stewart, Kolasch & Birch, LLP

For the above-identified deposit account, the Director is hereby authorized to (check all that apply):

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayment of fee(s)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES (U = undiscounted fee; S = small entity fee; M = micro entity fee)

	FILING FEES			SEARCH FEES			EXAMINATION FEES			
Application Type	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**Fees Paid ($)**
Utility	280	140*	70	600	300	150	720	360	180	1,600.00
Design	180	90	45	120	60	30	460	230	115	
Plant	180	90	45	380	190	95	580	290	145	
Reissue	280	140	70	600	300	150	2,160	1,080	540	
Provisional	260	130	65	0	0	0	0	0	0	

* The $140 small entity status filing fee for a utility application is further reduced to $70 for a small entity status applicant who files the application via EFS-Web.

2. EXCESS CLAIM FEES

Fee Description	**Undiscounted Fee ($)**	**Small Entity Fee ($)**	**Micro Entity Fee ($)**
Each claim over 20 (including Reissues)	80	40	20
Each independent claim over 3 (including Reissues)	420	210	105
Multiple dependent claims	780	390	195

Total Claims		**Extra Claims**	**Fee ($)**		**Fee Paid ($)**
20	-20 or HP =	_____ x	_____	=	0.00

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		**Extra Claims**	**Fee ($)**		**Fee Paid ($)**
1	-3 or HP =	_____ x	_____	=	0.00

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims

Fee ($)	**Fee Paid ($)**
_____	0.00

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $400 ($200 for small entity) ($100 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		**Extra Sheets**		**Number of each additional 50 or fraction thereof**		**Fee ($)**		**Fee Paid ($)**
77	- 100 =	_____	/ 50 =	_____ (round **up** to a whole number)	x	_____	=	0.00

4. OTHER FEE(S) **Fees Paid ($)**

Non-English specification, $130 fee (no small or micro entity discount) 0.00

Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, $400 fee ($200 small or micro entity) _____

Other (e.g., late filing surcharge): _____ _____

SUBMITTED BY

Signature	DAVID A. BILODEAU USPTO #42,325	Registration No. (Attorney/Agent) 40953	Telephone 703-205-8000
Name (Print/Type)	Esther H. Chong		Date JUL 06 2017

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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BAA

DAVID A. BILODEAU
USPTO #42,325

Docket No.: 1630-1332PUS2
(Patent)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application of:	Jungmin HA et al.		
Application No.:	NEW	Confirmation No.:	Not Yet Assigned
Filed:	Concurrently Herewith	Art Unit:	Not Yet Assigned
For:	SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME	Examiner:	Not Yet Assigned

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

Applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on the attached PTO/SB/08.

II. COPIES

☐ a. Copies of foreign patent documents, non-patent literature and other information are provided.

☑ b. REFERENCES PREVIOUSLY CITED OR SUBMITTED: Copies of any information not provided can be found in one or more of the following applications which has been relied upon for an earlier filing date under 35 U.S.C. § 120:

U.S. Application No. and U.S. Filing Date

14/953,264 filed November 27, 2015

III. CONCISE EXPLANATION OF THE RELEVANCE/OTHER INFORMATION

☐ a. NON-ENGLISH LANGUAGE DOCUMENTS: A concise explanation of the relevance of all non-English language patents, publications, or other information listed on the attached PTO/SB/08 form(s) is indicated thereon by a check mark at column T to designate the submission of one or more of the following: an English language abstract (as a partial translation); a machine-generated translation; a full or partial translation; and/or a statement of relevance.

☐ b. ENGLISH LANGUAGE SEARCH REPORT OR FOREIGN PATENT OFFICE COMMUNICATION: An English language version of the search report or Foreign Patent Office communication that indicates the degree of relevance is attached.

☐ c. OTHER: The following additional information is provided.

IV. STATEMENT UNDER 37 C.F.R. § 1.97(e)

The undersigned hereby states that:

☐ a. Each item of information contained in the IDS was first cited in any communication from a foreign patent office in a counterpart foreign application not more than **three months** prior to the filing of the IDS. *See 37 C.F.R § 1.97(e)(1)*. This statement does not relate to English language counterparts not listed in a communication from the foreign patent office. Such English language counterparts are provided to aid the Examiner's consideration of non-English items first cited in the communication from the foreign patent office; or

☐ b. No item of information contained in the IDS was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of IDS was known to any individual designated in 37 C.F.R. § 1.56(c) more than **three months** prior to the filing of the IDS. *See 37 C.F.R. § 1.97(e)(2)*; or

☐ c. Some of the items of information in the IDS were cited in a communication from a foreign patent office. Such items were first cited in a communication from a foreign patent office in a counterpart foreign application not more than **three months** prior to the filing of this IDS. *See 37 C.F.R. § 1.97(e)(1).* This statement does not relate to English language counterparts not listed in a communication from the foreign patent office. Such English language counterparts are provided to aid the Examiner's consideration of non-English items first cited in the communication from the foreign patent office. As to the remaining items of information, to the knowledge of the person signing the certification after making reasonable inquiry, such remaining items were not known to any individual designated in 37 C.F.R. § 1.56(c) more than **three months** prior to the filing of this statement. *See 37 C.F.R. § 1.97(e)(2).*

V. STATEMENT UNDER 37 C.F.R. § 1.704(d)(1)

Patent Term Adjustment Reduction Should Not Apply

☐ The undersigned hereby states:

This Information Disclosure Statement is in compliance with 37 C.F.R. §§ 1.97 and 1.98 and will not be considered a failure to engage in reasonable efforts to conclude prosecution (processing or examination) of the present application under 37 C.F.R. § 1.704(c)(6), (c)(8), (c)(9), or (c)(10), because each item of information contained in the Information Disclosure Statement:

☐ (i) Was first cited in any communication from a patent office in a counterpart foreign or international application or from the Office, and this communication was not received by any individual designated in § 1.56(c) more than **thirty days** prior to the filing of the information disclosure statement *(see 37 C.F.R. § 1.704(d)(1)(i))*; or

☐ (ii) Is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in § 1.56(c) more than **thirty days** prior to the filing of the information disclosure statement *(see 37 C.F.R. § 1.704(d)(1)(ii))*.

VI. FEES

☑ a. This Information Disclosure Statement is being filed concurrently with the filing of a new patent application or Request for Continued Examination. No fee is required.

☐ b. This Information Disclosure Statement is being filed within three months of the filing date of an application. *See 37 C.F.R. § 1.97(b)(1) and 37 C.F.R. § 1.97(b)(2).* No fee is required.

☐ c. This Information Disclosure Statement is being filed before the mailing date of a first Action on the merits. *See 37 C.F.R. § 1.97(b)(3).* No fee is required. If a first Office Action on the merits has issued, please consider this IDS under 37 C.F.R. § 1.97(c) and see the statement under 37 C.F.R. § 1.97(e) above. If no statement has been made, charge our deposit account for the required fee.

☐ d. This Information Disclosure Statement is being filed before the mailing date of a Final Office Action or before the mailing date of a Notice of Allowance or before an action that otherwise closes prosecution in the application. *See 37 C.F.R. § 1.97(c)(1).*

☐ No statement. The fee as required by 37 C.F.R. § 1.17(p) is provided.

or

☐ See the above statement. No fee is required.

☐ e. This Information Disclosure Statement is being filed on or after the mailing date of a Final Office Action, on or after the mailing date of a Notice of Allowance, or on or after an action that otherwise closes prosecution in the application (*see 37 C.F.R. § 1.97(d)*), see the statement above. The fee as required by 37 C.F.R. § 1.17(p) is provided.

VII. PAYMENT OF FEES

☐ The required fee is listed on the attached Fee Transmittal.

☑ No fee is required.

If the Examiner has any questions concerning this IDS, please contact the undersigned. If it is determined that this IDS has been filed under the wrong rule, the USPTO is requested to consider this IDS under the proper rule and charge the appropriate fee to Deposit Account No. 02-2448.

Dated: JUL 06 2017

Respectfully submitted,

By: DAVID A. BILODEAU
USPTO #42,325

Esther H. Chong
Registration No.: 40953
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road, Suite 100 East
Falls Church, VA 22042
703-205-8000

Attachment(s):
☑ PTO/SB/08
☐ Document(s)
☐ Foreign Patent Office Communication(s)
☐ Foreign Search Report(s)
☐ Fee
☐ Other:

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	NEW
Filing Date	Concurrently Herewith
First Named Inventor	Jungmin HA
Title	SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME
Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	1630-1332PUS2

SIGNATURE of Applicant or Patent Practitioner

Signature		Date (Optional)	JUL 06 2017
Name	Esther H. Chong DAVID A. BILODEAU USPTO #42,325	Registration Number	40953
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

BFR

PTO/AIA/82B (07-12)
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the above-identified patent application.

☑ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

02292

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

Name Registration	Number	Name Registration	Number

Please recognize or change the correspondence address for the above-identified patent to:

☑ The address associated with the above-mentioned Customer Number.

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant:

☐ Inventor or Joint Inventor

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient *Proprietary* Interest (*e.g.*, a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

SIGNATURE of Applicant for Patent

Signature		Date	Sep. 17, 2012
Name	Saeng-Gyu Jeon	Telephone	+82 02 2102-0100
Title and Company	Vice President, LG Electronics Inc.		

NOTE: Signature - This form must be signed by the applicant or applicant's representative in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below *.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

COPY

Attorney Docket No. 1630-1332PUS1

BIRCH, STEWART, KOLASCH & BIRCH, LLP
P.O. Box 747 • Falls Church, Virginia 22040-0747
Telephone: (703) 205-8000 • Facsimile: (703) 205-8050 • Email: mailroom@bskb.com

DECLARATION AND ASSIGNMENT FOR PATENT AND DESIGN APPLICATIONS

UNITED STATES PATENT RIGHTS, OR
UNITED STATES PLUS ALL FOREIGN PATENT RIGHTS

Title of Invention ⇨ SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME

As a below named inventor (hereinafter designated as the undersigned), I hereby declare that:

This declaration is directed to the application attached hereto.

Application not Attached ⇨ If the application is not attached hereto, the application is as identified by the attorney docket number as set forth above and/or the following:

Enter Appln. No. ⇨ United States Application Number or PCT International Appln. No. 14/953,264

Enter Filing Date ⇨ filed on November 27, 2015.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I have reviewed and understand the contents of the above-identified application, including the claims.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

WHEREAS, the undersigned has invented certain new and useful improvements described in the application identified.

Insert Name of Assignee ⇨ WHEREAS, LG ELECTRONICS INC.

Insert Address of Assignee ⇨ of 128, Yeoui-daero, Yeongdeungpo-gu, Seoul, 07336, Republic of Korea

its heirs, successors, legal representatives and assigns (hereinafter designated as the Assignee) is desirous of acquiring the entire right, title and interest in and to said invention and in and to any Letters Patent(s) that may be granted therefor in the United States of America and

Check Box if Appropriate ⇨ ☐ **in any foreign countries.**

NOW, THEREFORE, for good and valuable consideration, the receipt of which is hereby acknowledged, the undersigned has sold, assigned and transferred, and by these presents does (do) sell, assign and transfer unto said Assignee the full and exclusive right to the said invention in the United States of America, its territories, dependencies and possessions and the entire right, title and interest in and to any and all Letters Patent(s) which may be granted therefor in the United States of America, its territories, dependencies and possessions, and if the box above is designated, in any and all foreign countries; and to any and all divisions, reissues, continuations, conversions and extensions thereof for the full term or terms for which the same may be granted.

The undersigned agrees to execute all papers necessary in connection with this application and any continuing, divisional, conversion or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.

The undersigned agrees to execute all papers necessary in connection with any interference which may be declared concerning this application or continuation, division, conversion or reissue thereof or Letters Patent(s) or reissue patent issued thereon and to cooperate with the Assignee in every way possible in obtaining and producing evidence and proceeding with such interference.

The undersigned agrees to execute all papers and documents and to perform any act which may be necessary in connection with claims or provisions of the International Convention for the Protection of Industrial Property or similar agreements.

The undersigned agrees to perform all affirmative acts which may be necessary to obtain a grant of (a) valid United States of America patent(s) or a grant of (a) valid United States of America and any foreign patent(s) to the Assignee and to vest all rights therein hereby conveyed to said Assignee as fully and entirely as the same would have been held by the undersigned if this Assignment and sale had not been made.

The undersigned hereby authorizes and requests the Patent and Trademark Office Officials in the United States of America and in any foreign countries to issue any and all Letters Patent(s) resulting from said application or any continuing, divisional conversion or reissue applications thereof to the said Assignee, as Assignee of the entire interest, and hereby covenants that he has the full right to convey the entire interest herein assigned, and that he has not executed, and will not execute, any agreement in conflict herewith.

The undersigned hereby grants the law firm of Birch, Stewart, Kolasch & Birch, LLP the power to insert any further identification which may be necessary or desirable in order to comply with the rules of the U.S. Patent and Trademark Office.

The undersigned hereby covenants that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment.

The undersigned hereby acknowledges that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

In witness whereof, executed by the undersigned on the date opposite the undersigned name.

LEGAL NAME OF INVENTOR

Inventor's Name ⇨ Inventor: Jungmin HA Date: 2016. 3. 2

Inventor's Signature ⇨ Signature:

An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use a separate form for each inventor; or check the box below and complete the attached page(s) to list additional inventors.

☒ Additional inventors are being named on the 1 supplemental sheet attached hereto.

Attorney Docket No. 1630-1332PUS1

SUPPLEMENTAL SHEET FOR DECLARATION AND ASSIGNMENT

ADDITIONAL INVENTORS
Supplemental Sheet Page 1 of 1

LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Sungjin KIM Date: 2016. 3. 2

Inventor's Signature ⇨ Signature:

LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Juhwa CHEONG Date: 2016. 3. 2

Inventor's Signature ⇨ Signature:

LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Junyong AHN Date: 2016. 3. 2

Inventor's Signature ⇨ Signature:

LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Hyungwook CHOI Date: 2016. 3. 2

Inventor's Signature ⇨ Signature:

LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Wonjae CHANG Date: 2016. 3. 2

Inventor's Signature ⇨ Signature:

LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Jaesung KIM Date: 2016. 3. 2

Inventor's Signature ⇨ Signature: KIM JAE SUNG

LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Date:

Inventor's Signature ⇨ Signature:

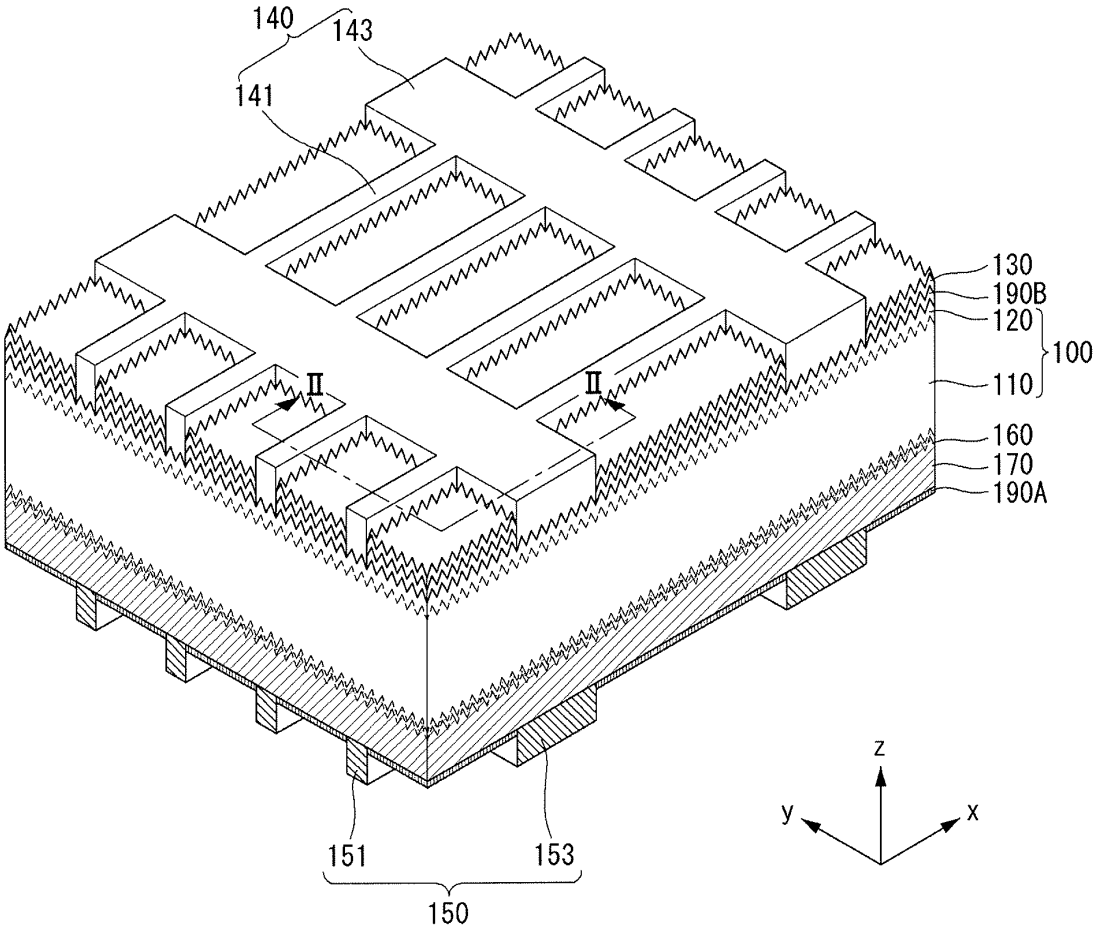
LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Date:

Inventor's Signature ⇨ Signature:

BSKB-DECASSIGN\(09-12)

FIG. 1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II
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170
190A
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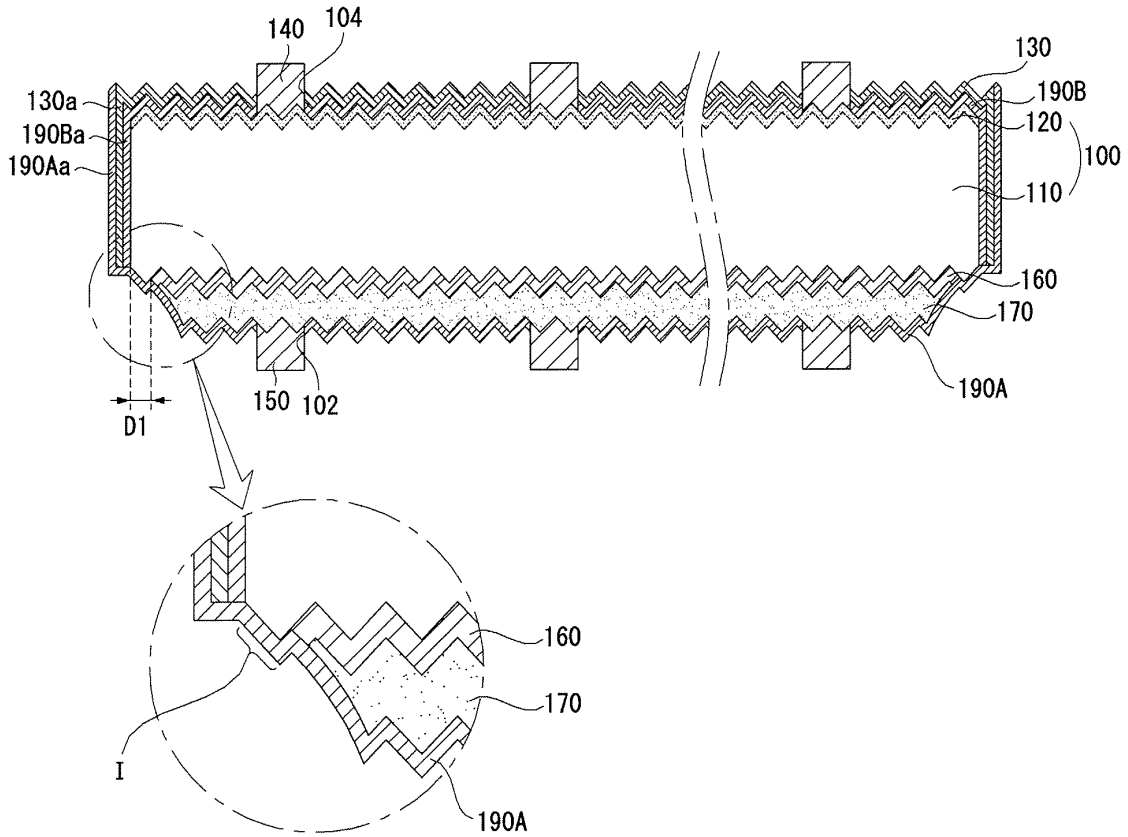
153
150
z
y
x

FIG. 2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130a
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190Aa
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170
190A
150
102
D1
160
170
I
190A

FIG. 3

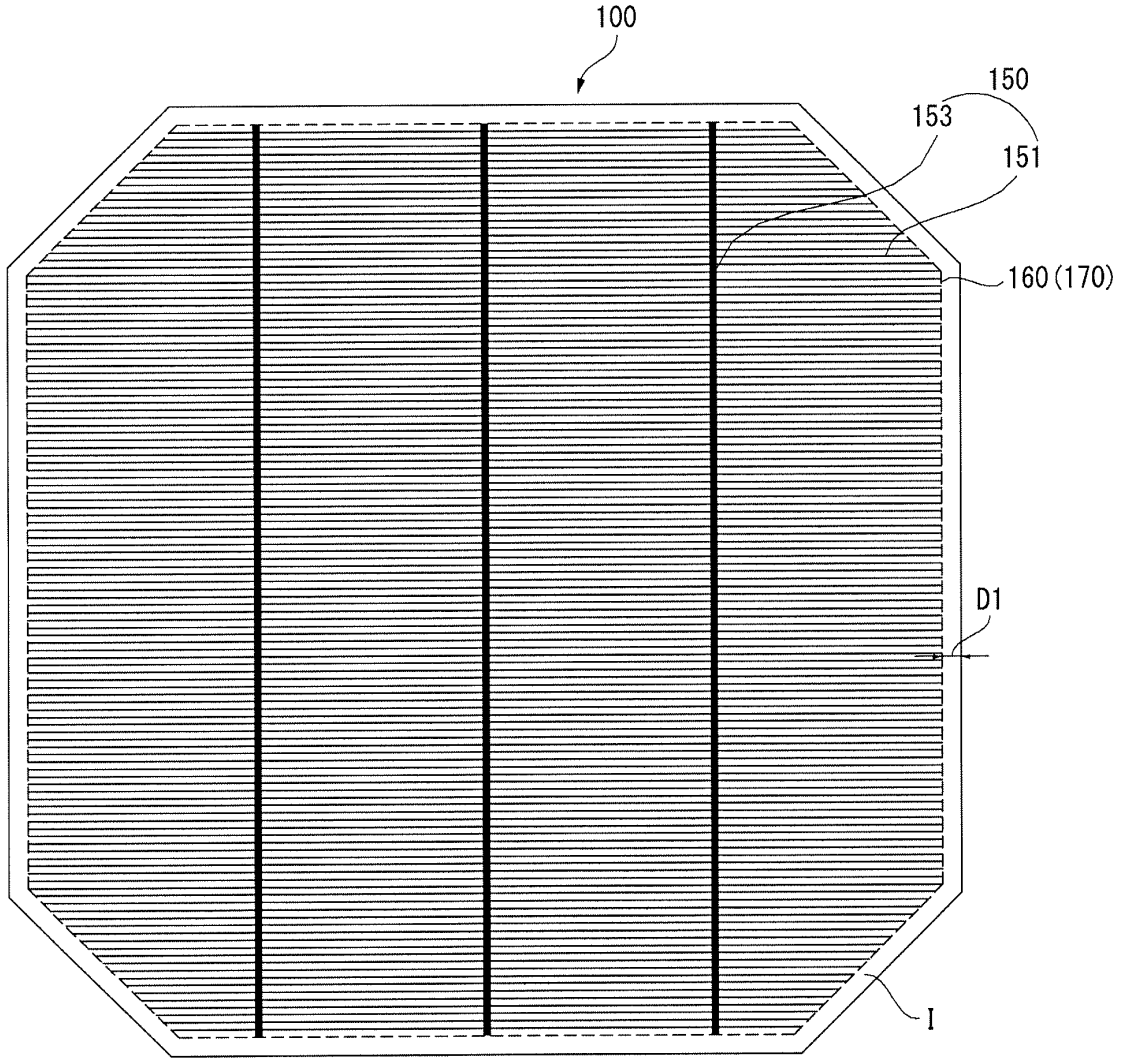


FIG. 4

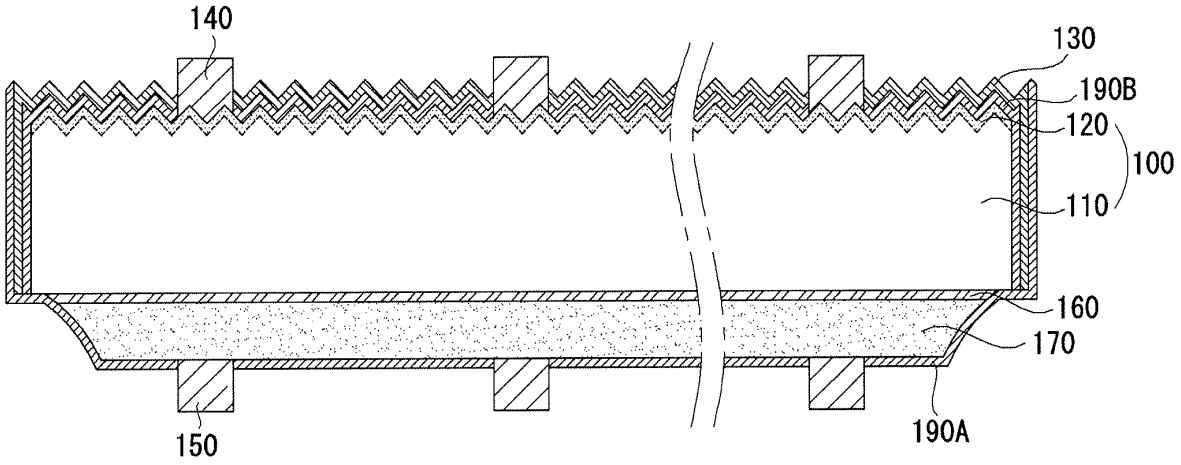
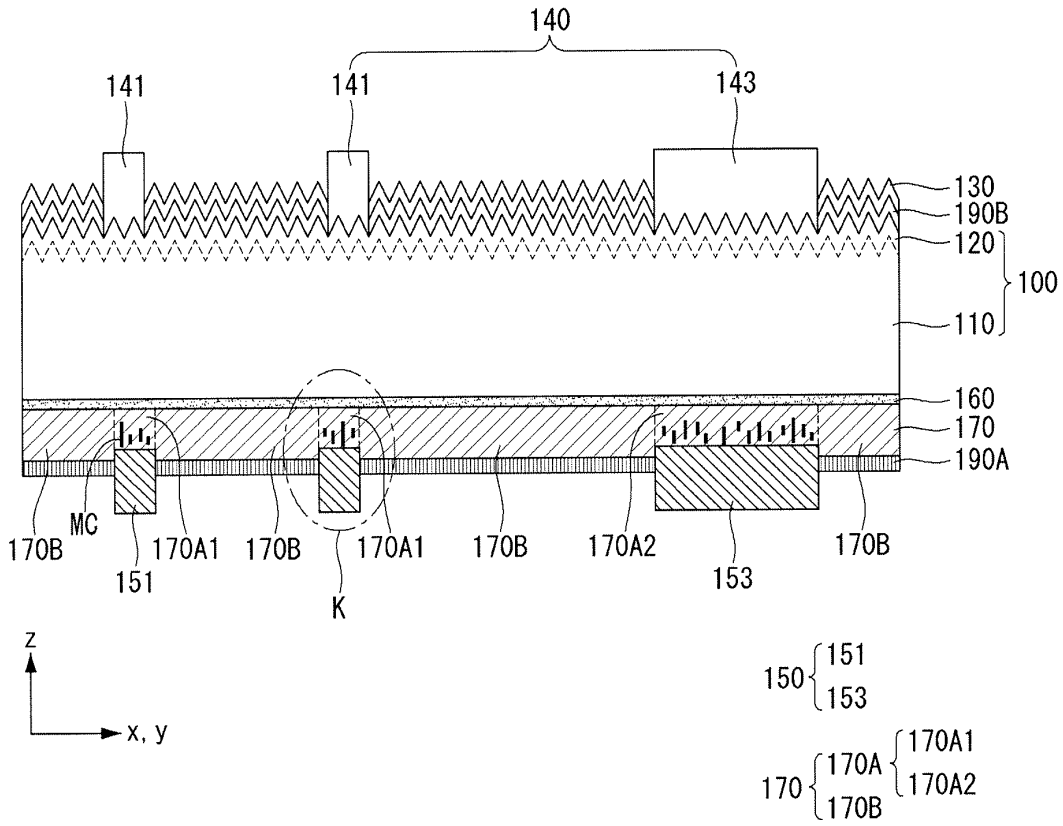


FIG. 5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190A
170B
MC
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170A1
170B
K
170A1
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170A2
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170B
z
x, y
150
151
153
170
170A
170A1
170A2
170B

FIG. 6

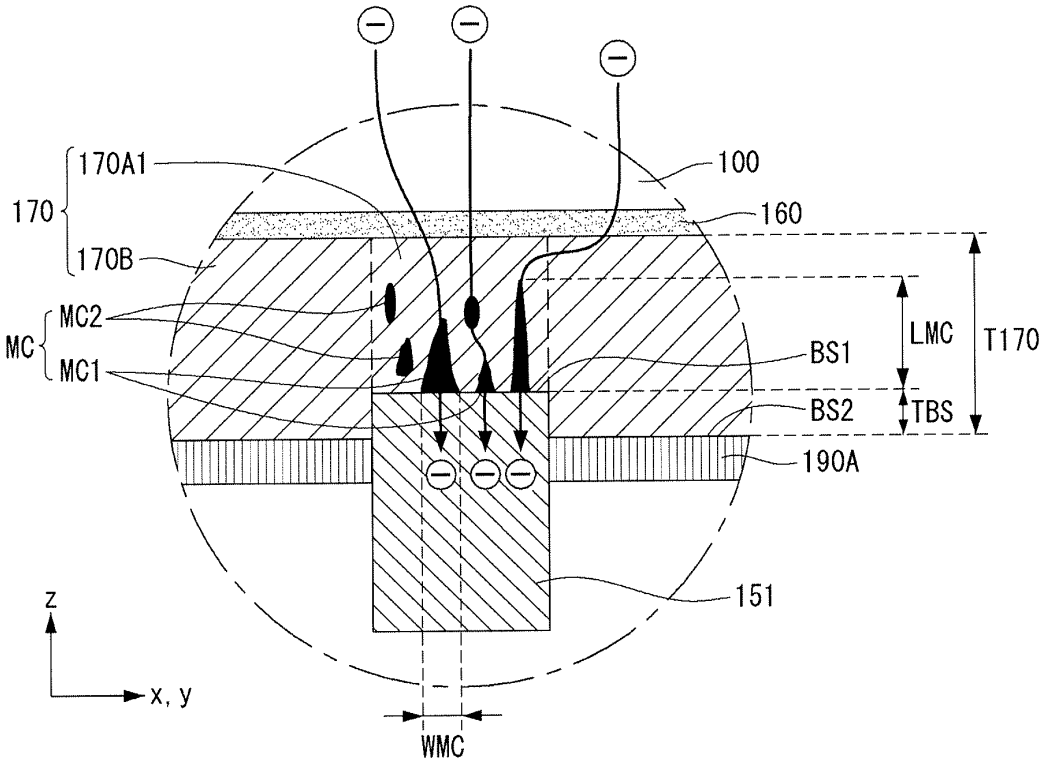

170A1
170
170B
100
160
MC2
MC
MC1
BS1
LMC
T170
BS2
TBS
190A
151
z
x, y
WMC

FIG. 7

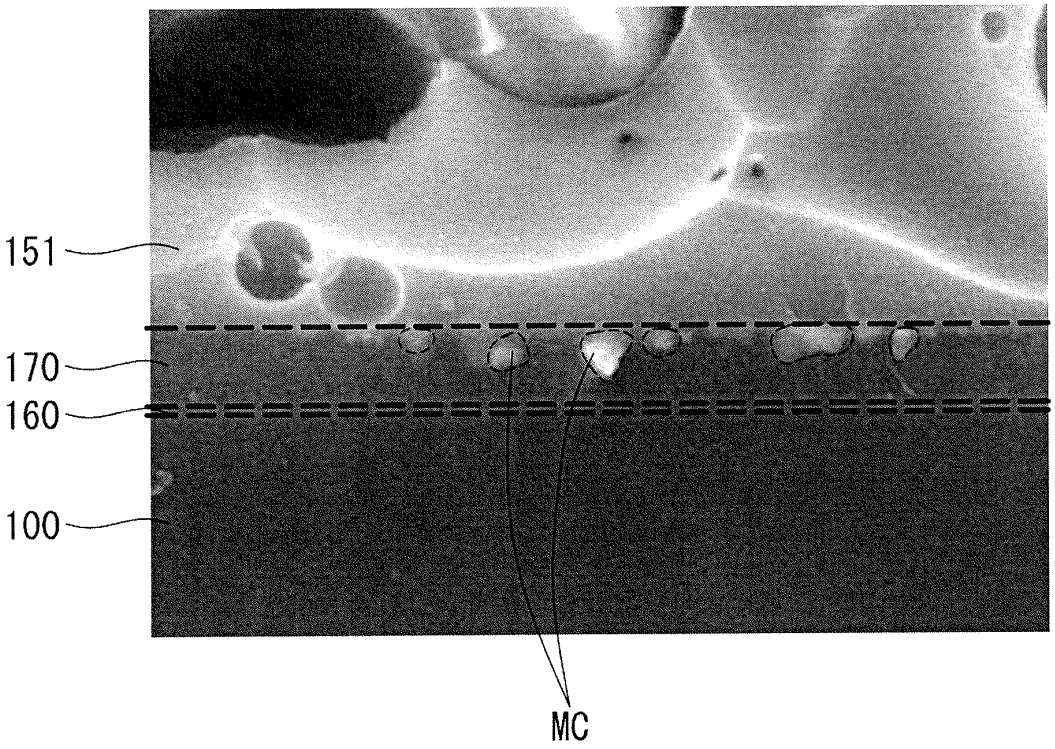


FIG. 8

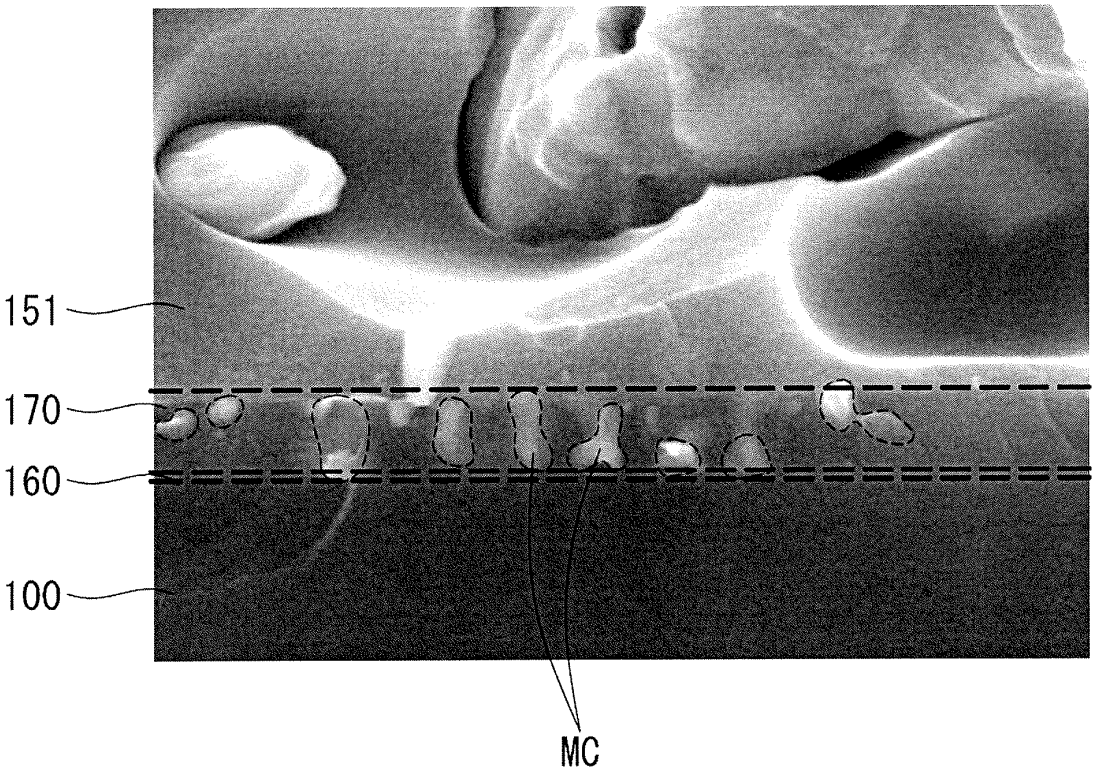
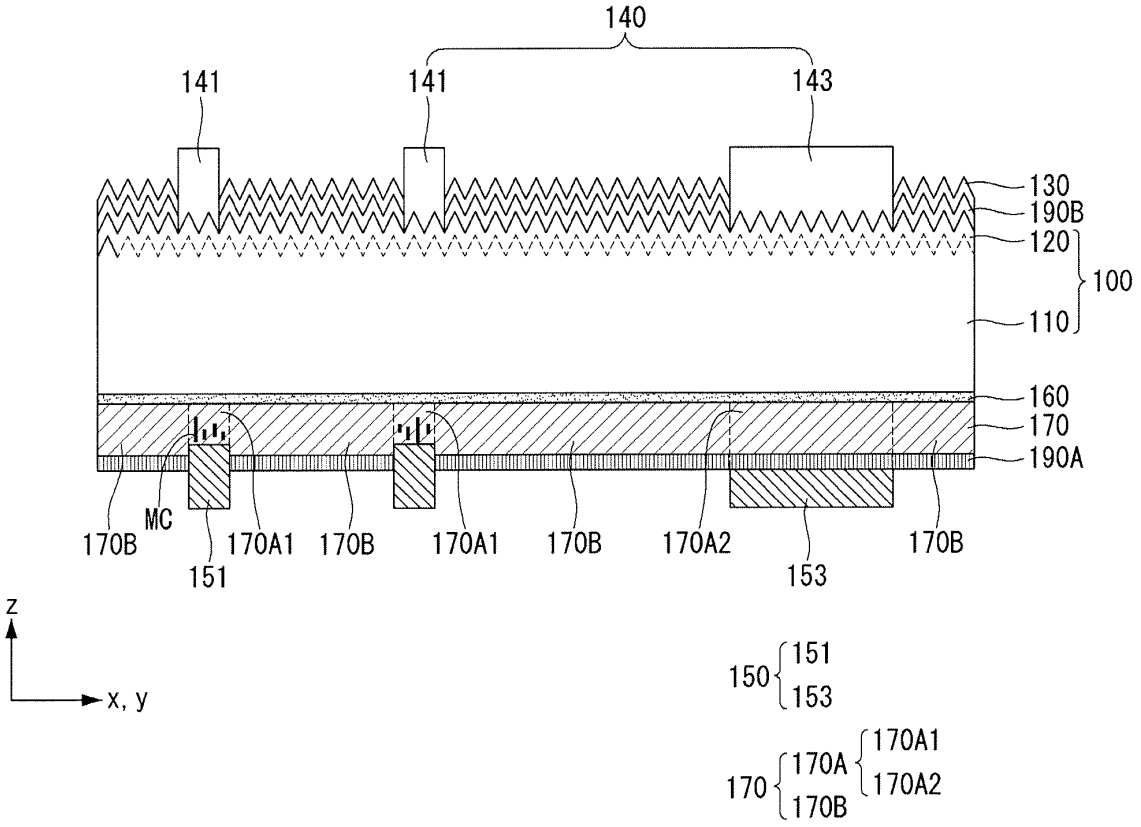


FIG. 9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170A1
170B
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170B
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x, y
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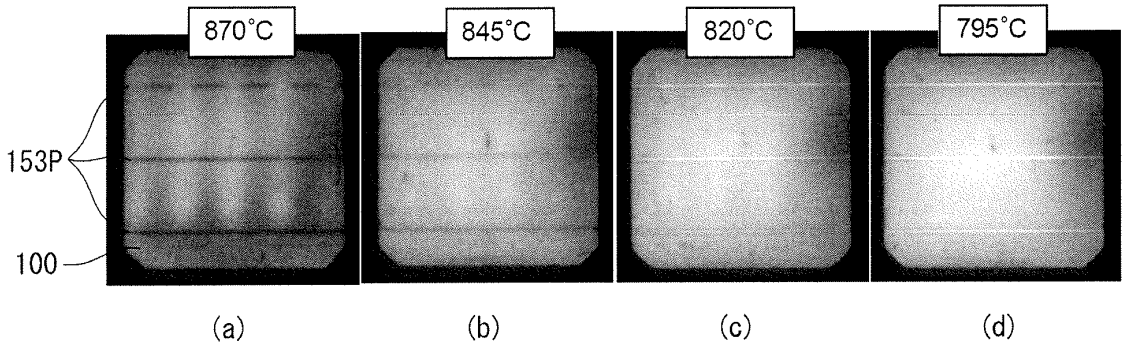
151
153
170
170A
170A1
170A2
170B

FIG. 10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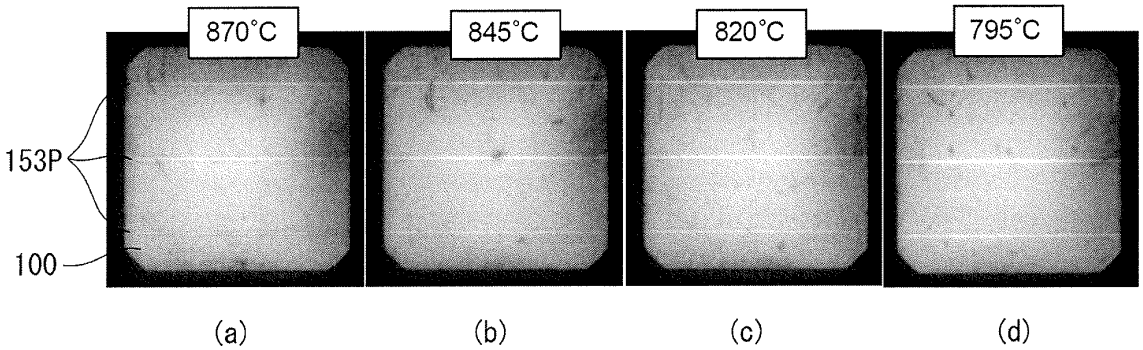
845°C
820°C
795°C
153P
100
(a)
(b)
(c)
(d)

FIG. 11


870°C
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820°C
795°C
153P
100
(a)
(b)
(c)
(d)

FIG. 12

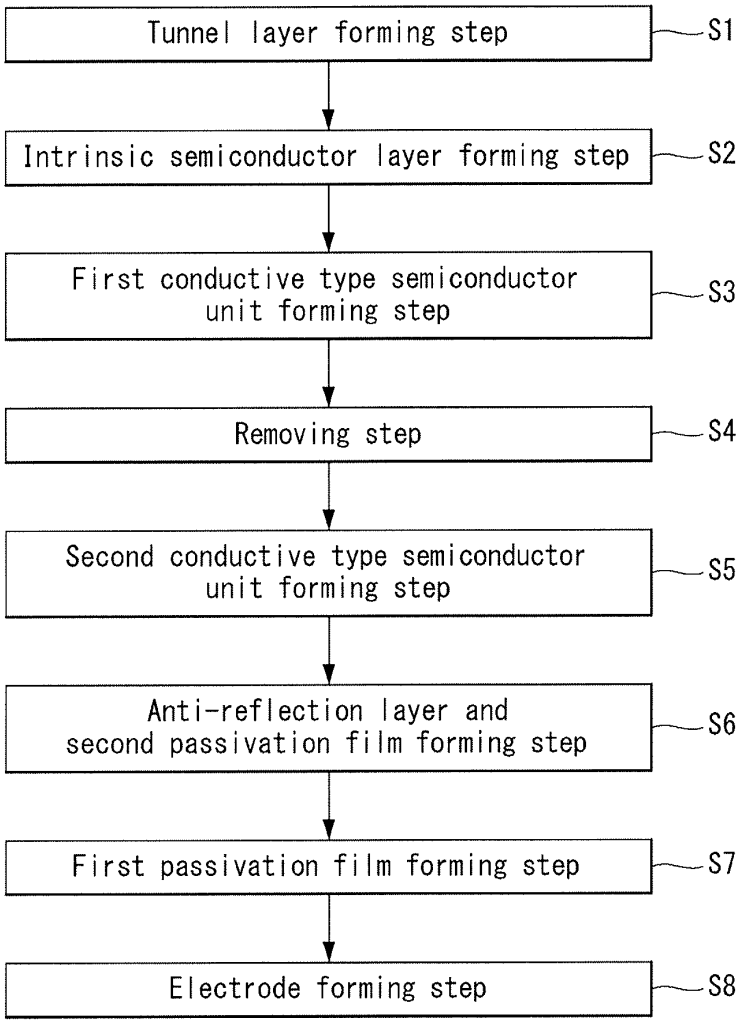

Tunnel layer forming step
S1
Intrinsic semiconductor layer forming step
S2
First conductive type semiconductor unit forming step
S3
Removing step
S4
Second conductive type semiconductor unit forming step
S5
Anti-reflection layer and second passivation film forming step
S6
First passivation film forming step
S7
Electrode forming step
S8

FIG. 13A

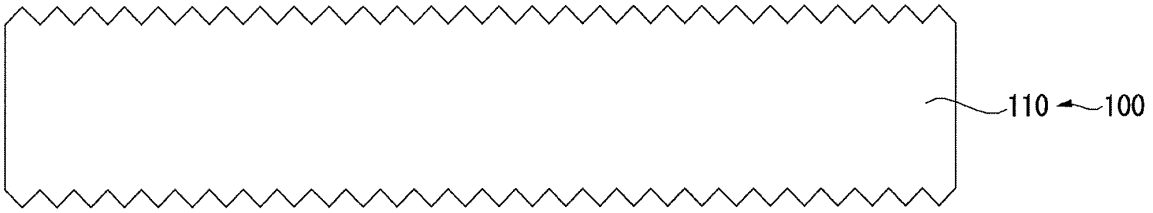


FIG. 13B

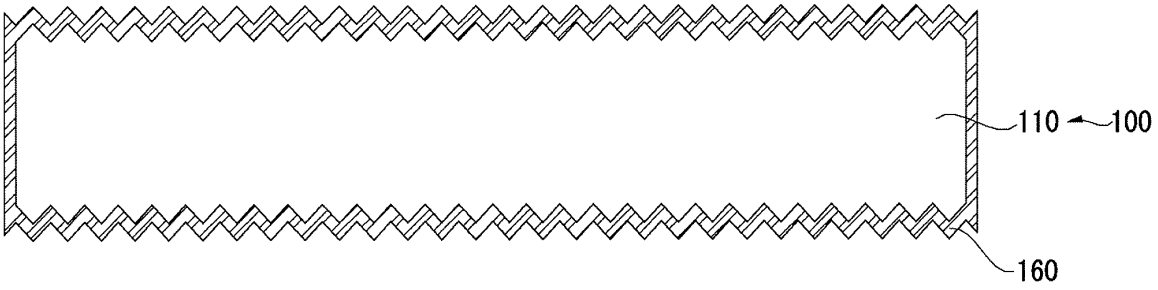


FIG. 13C

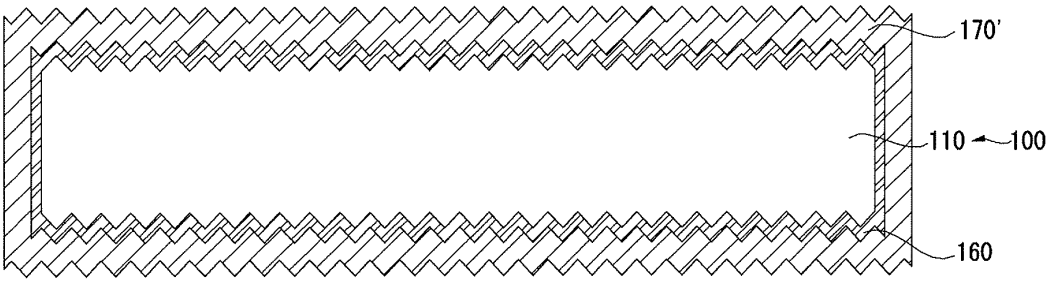


FIG. 13D

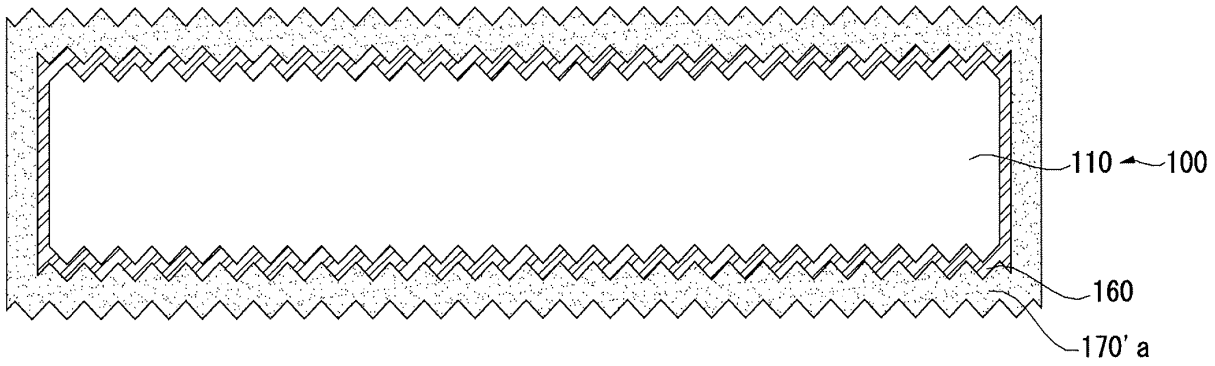


FIG. 13E

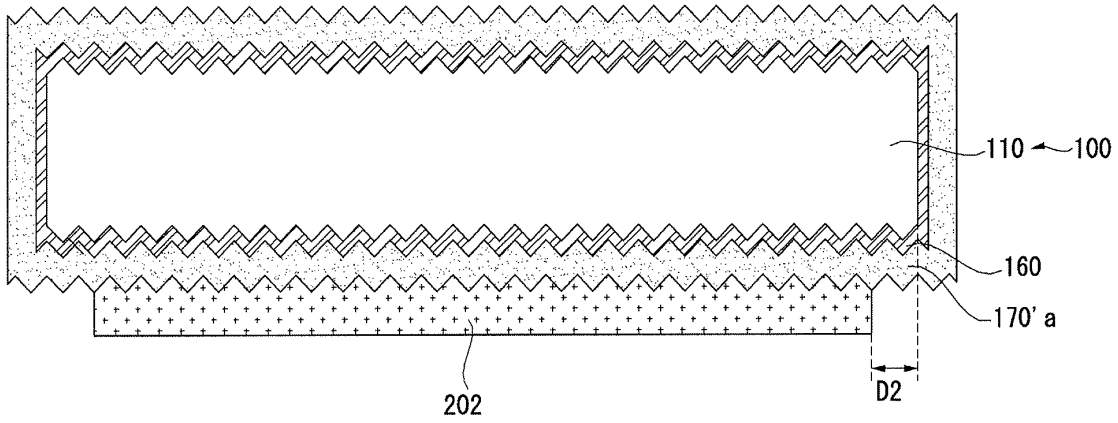


FIG. 13F

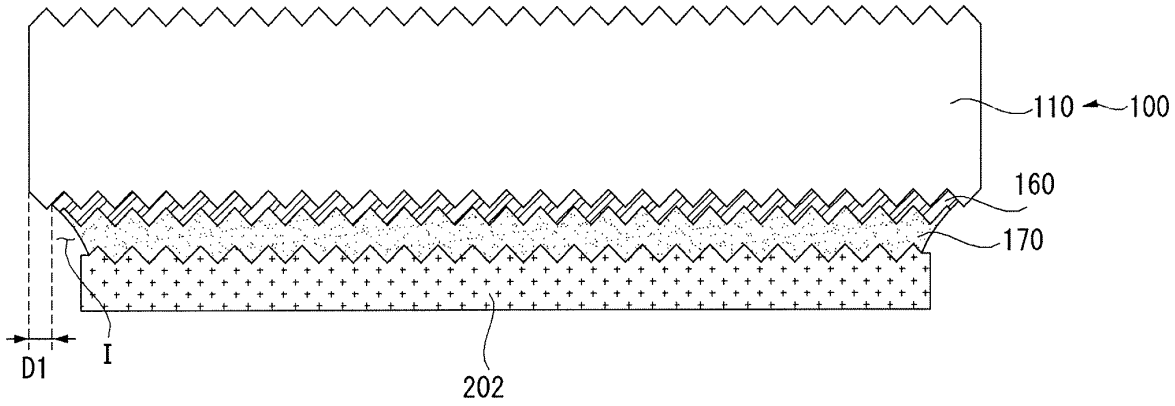


FIG. 13G

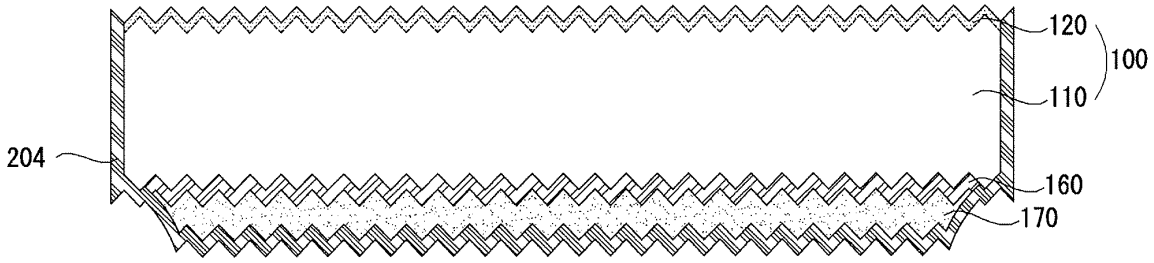


FIG. 13H

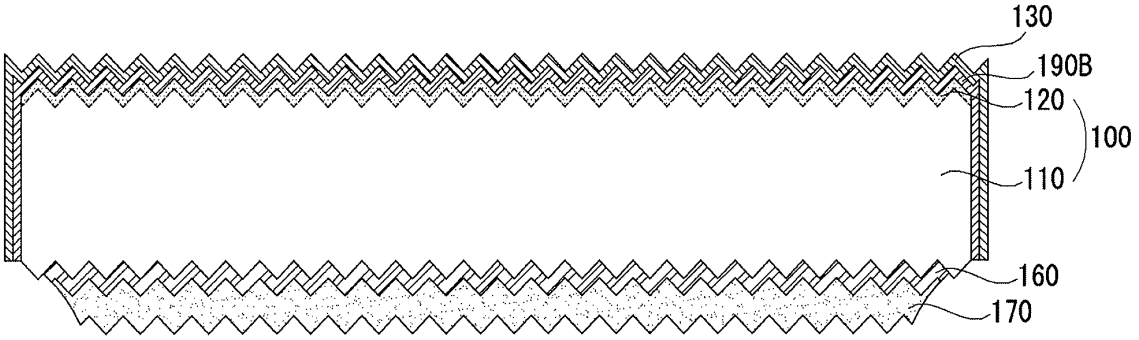


FIG. 13I

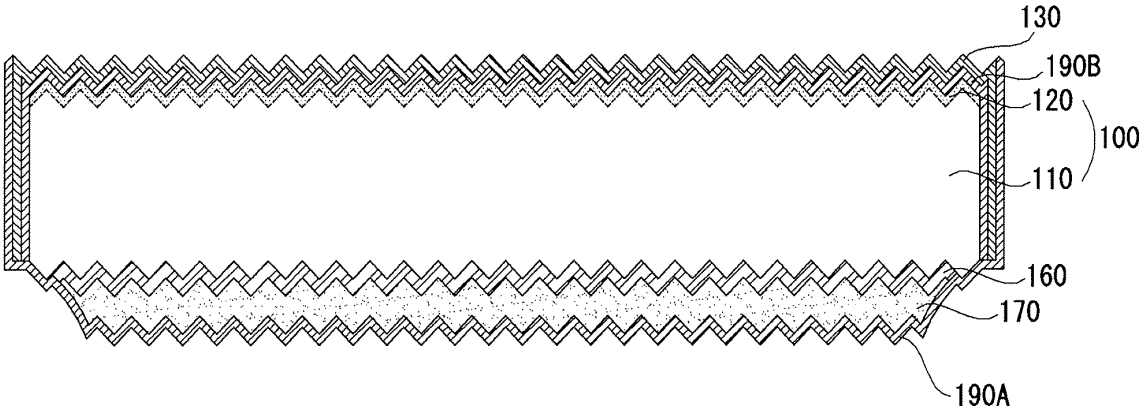


FIG. 13J

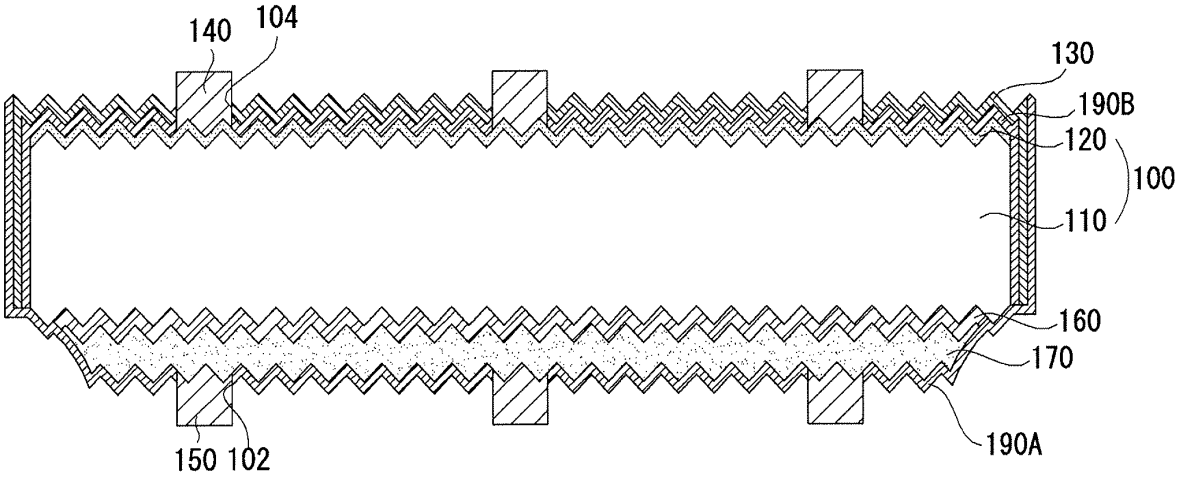


FIG. 14

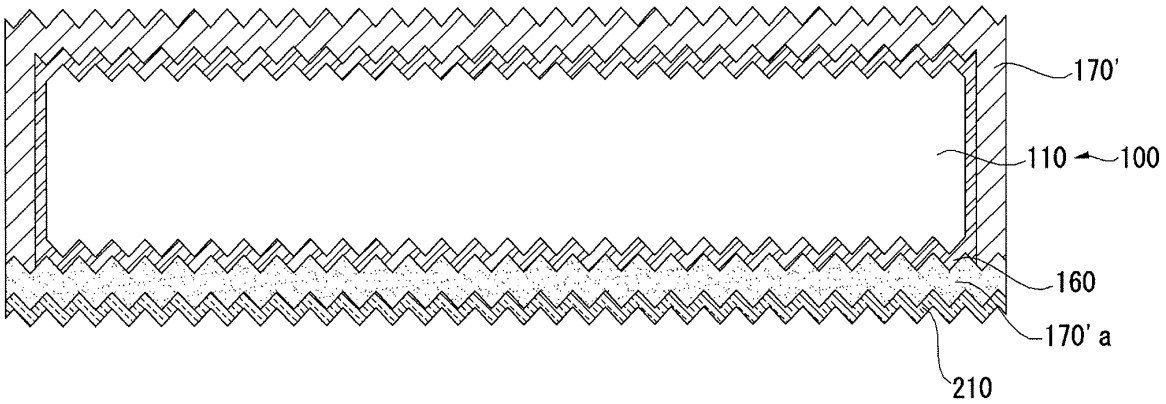


FIG. 15

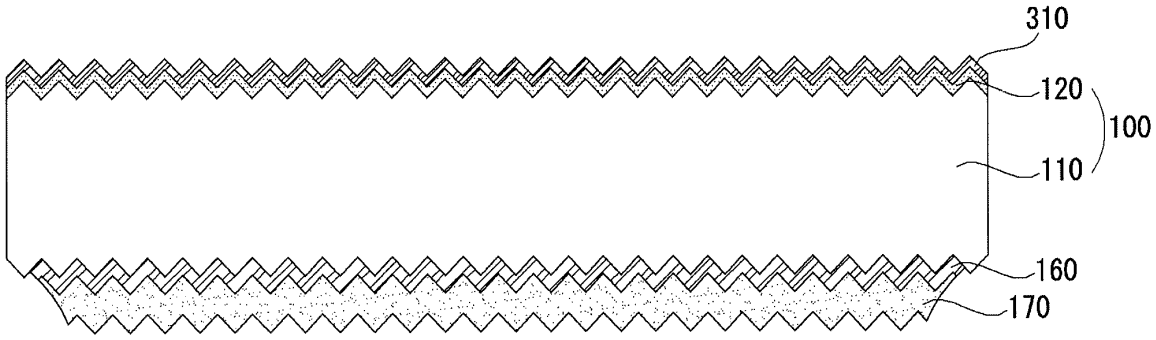

310
120
100
110
160
170

FIG. 16

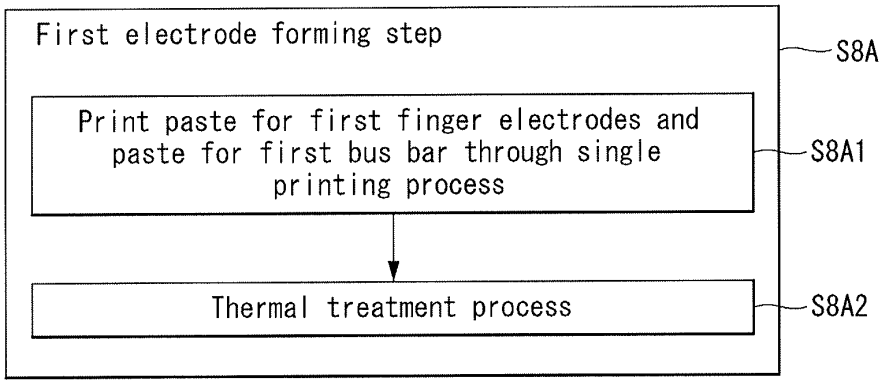
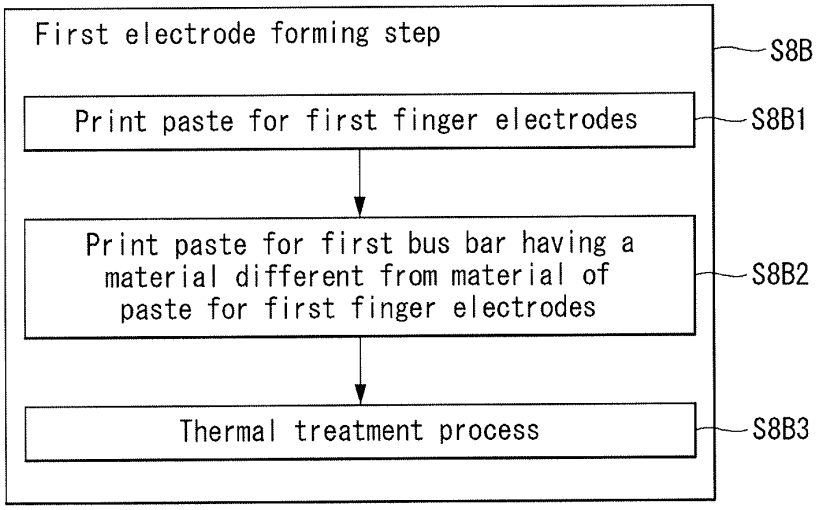

First electrode forming step
S8A
Print paste for first finger electrodes and paste for first bus bar through single printing process
S8A1
Thermal treatment process
S8A2

FIG. 17


First electrode forming step
S8B
Print paste for first finger electrodes
S8B1
Print paste for first bus bar having a material different from material of paste for first finger electrodes
S8B2
Thermal treatment process
S8B3

SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation of U.S. Patent Application No. 14/953,264 filed on November 27, 2015, which claims priority to and the benefit of Korean Patent Application No. 10-2014-0168624 filed in the Korean Intellectual Property Office on November 28, 2014 and Korean Patent Application No. 10-2015-0122846 filed in the Korean Intellectual Property Office on August 31, 2015, the entire contents of all these applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] **Field of the Invention**

[0003] Embodiments of the present invention relate to a solar cell and a method for manufacturing the same.

[0004] **Discussion of the Related Art**

[0005] Recently, as the exhaustion of existing energy resources, such as petroleum and coal, is expected, there is a growing interest in alternative energy sources which will replace the existing energy resources. A solar cell as the alternative energy sources generates electric power from solar energy and has been in the spotlight because the solar cell uses energy resources that are abundant and the solar cell has no problem from an environmental pollution point of view.

[0006] A solar cell includes substrates made of semiconductors having different conductive types, such as a p type and an n type, a second conductive type semiconductor region (or emitter layer), and electrodes respectively connected to the substrates and the second conductive type semiconductor region. A p-n junction is formed at the interface of the substrate and the second conductive type semiconductor region.

[0007] When light is incident on such a solar cell, a plurality of electron-hole pairs are generated from the semiconductors. The generated electron-hole pairs are separated into electrons and holes. The separated electrons and holes move toward the n type semiconductor and the p type semiconductor, for example, toward the second conductive type semiconductor region and the substrate, respectively, and are collected by the electrodes electrically connected to the substrates and the second conductive type

semiconductor region. The electrodes are connected by lines, thereby obtaining power.

SUMMARY OF THE INVENTION

[0008] A solar cell according to an example of the present invention includes a semiconductor substrate, a tunnel layer on the first surface of the semiconductor substrate, a first conductive type semiconductor region on the tunnel layer and configured to include impurities of a first conductive type, a second conductive type semiconductor region on a second surface which is the opposite surface of the semiconductor substrate and configured to include impurities of a second conductive type opposite the first conductive type, a first passivation film on the first conductive type semiconductor region, a first electrode formed on the first passivation film and connected to the first conductive type semiconductor region through an opening portion formed in the first passivation film, a second passivation film on the second conductive type semiconductor region, and a second electrode formed on the second passivation film and connected to the second conductive type semiconductor region through an opening portion formed in the second passivation film.

[0009] In this instance, the first electrode may include a plurality of first finger electrodes spaced apart from each other and extended in parallel in a first direction, and the second electrode may include a plurality of second finger electrodes spaced apart from each other and extended in parallel in the first direction.

[0010] Furthermore, the first electrode may further include a first bus bar configured to interconnect the plurality of first finger electrodes, and the second electrode may further include a second bus bar configured to interconnect the plurality of second finger electrodes.

[0011] In this instance, the first conductive type semiconductor region may be made of a polycrystalline silicon material, and the second conductive type semiconductor region may be made of a single crystal silicon material.

[0012] Furthermore, an isolation portion for preventing a contact between the first conductive type semiconductor region and the second conductive type semiconductor region may be formed on any one of the first surface, side, and second surface of the semiconductor substrate.

[0013] For example, the isolation portion may exclude the tunnel layer and the first conductive type semiconductor region, and may be in the edge portion of any one of the

first surface, side, and second surface of the semiconductor substrate. The first passivation film may cover any one of the first surface, side, and second surface of the semiconductor substrate along with the isolation portion.

[0014] In this instance, the width of the isolation portion may be 1 nm to 1 mm. The thickness of the edge region in the first conductive type semiconductor region may be progressively decreased toward the isolation portion.

[0015] Furthermore, the first passivation film may include a side portion extending up the side of the semiconductor substrate.

[0016] Moreover, the second passivation film may include a side portion formed on the side surface of the semiconductor substrate. The side portion of the first passivation film on the side of the semiconductor substrate may be on the side portion of the second passivation film.

[0017] Furthermore, a first boundary surface in which the first conductive type semiconductor region and the first electrode come into contact with each other may be closer to the semiconductor substrate than a second boundary surface in which the first conductive type semiconductor region and the first passivation film come into contact with each other.

[0018] In this instance, a plurality of metal crystals extracted from the first electrode may be in an electrode forming region which belongs to the first conductive type semiconductor region and in which the first electrode may be formed. That is, the metal crystals may not be in a non-forming region which belongs to the first conductive type semiconductor region and in which the first electrode may not be formed. Furthermore, the metal crystals may not be in the tunnel layer.

[0019] The plurality of metal crystals may be in direct contact with the first electrode or may be spaced apart from the first electrode.

[0020] In this instance, all of the plurality of first finger electrodes and the first bus bar may be connected to the first conductive type semiconductor region through the first passivation film.

[0021] In this instance, all of the plurality of first finger electrodes and the first bus bar may have a single layer or double layer structure. In some embodiments, the plurality of first finger electrodes may have a single layer structure, and the first bus bar may have a double layer structure.

[0022] In this instance, the plurality of metal crystals may be in a region which belongs

to the first conductive type semiconductor region and in which the plurality of first finger electrodes is formed and a region which belongs to the first conductive type semiconductor region and in which the first bus bar is formed.

[0023] In some embodiments, the plurality of first finger electrodes may be connected to the first conductive type semiconductor region through the first passivation film. The first bus bar may be configured to not penetrate the first passivation film and may be formed on the back surface of the first passivation film.

[0024] In this instance, the plurality of metal crystals may be in a region which belongs to the first conductive type semiconductor region and in which the first finger electrodes are formed. The plurality of metal crystals may not be in a region which belongs to the first conductive type semiconductor region and in which the first bus bar is formed.

[0025] In this instance, the plurality of first finger electrodes and the first bus bar may have different compositions. For example, a content of a frit glass per unit volume which is included in the plurality of first finger electrodes may be greater than a content of a frit glass per unit volume which is included in the first bus bar.

[0026] Furthermore, a content of a frit glass per unit volume which is included in the plurality of first finger electrodes may be identical with a content of a frit glass per unit volume which is included in the first bus bar.

[0027] Furthermore, content of a metal material per unit volume which is included in the plurality of first finger electrodes may be greater than content of a metal material per unit volume which is included in the first bus bar.

[0028] Furthermore, a method for manufacturing a solar cell according to an example of the present invention includes a tunnel layer forming operation of forming a tunnel layer on the first surface of a semiconductor substrate, an intrinsic semiconductor layer forming operation of forming an intrinsic semiconductor layer on the tunnel layer formed on the first surface of the semiconductor substrate, a first conductive type semiconductor region forming operation of forming a first conductive type semiconductor region by doping impurities of a first conductive type into the intrinsic semiconductor layer formed on the first surface of the semiconductor substrate, a second conductive type semiconductor region forming operation of forming a second conductive type semiconductor region by doping impurities of a second conductive type into the second surface of the semiconductor substrate, a first passivation film forming operation of forming a first passivation film on the first conductive type semiconductor

region, and an electrode forming operation of forming a first electrode connected to the first conductive type semiconductor region and a second electrode connected to the second conductive type semiconductor region.

[0029] In this instance, the method may further include the operation of forming an opening portion in the first passivation film after the first passivation film forming operation.

[0030] The operation of forming the opening portion in the first passivation film may be performed by thermal treatment in the electrode forming operation.

[0031] The electrode forming operation may include a first electrode forming operation of forming the first electrode. The first electrode forming operation may include printing a paste for first finger electrodes for forming the first finger electrodes and a paste for a first bus bar for forming the first bus bar on the first passivation film and performing thermal treatment on the pastes. During such a thermal treatment process, the paste for the first finger electrodes and the paste for the first bus bar may perforate the first passivation film and may be connected to the first conductive type semiconductor region. In this instance, the opening portion may be formed in the first passivation film.

[0032] In the first electrode forming operation, the highest temperature for the thermal treatment may be between 795°C to 870°C.

[0033] In the first electrode forming operation, the paste for the first finger electrodes and the paste for the first bus bar may be printed through a single process. In this instance, a material included in the paste for the first finger electrodes may be identical with a material included in the paste for the first bus bar.

[0034] Furthermore, in some embodiments, in the first electrode forming operation, the paste for the first finger electrodes and the paste for the first bus bar may be printed using separate printing processes. In this instance, a material included in the paste for the first finger electrodes and a material included in the paste for the first bus bar may be different.

[0035] Furthermore, the tunnel layer forming operation may include forming the tunnel layer on the first and second surfaces of the semiconductor substrate. The intrinsic semiconductor layer forming operation may include forming the intrinsic semiconductor layer on the tunnel layers formed on the first and second surfaces of the semiconductor substrate. The method may further include a removing operation of removing the

tunnel layer and the intrinsic semiconductor layer or the first conductive type semiconductor region placed at least on the second surface of the semiconductor substrate prior to the second conductive type semiconductor region forming operation after the first conductive type semiconductor region forming operation.

[0036] The removing operation may include forming an isolation portion by removing the tunnel layer placed on one side of the semiconductor substrate and an edge portion of the first conductive type semiconductor region. The first passivation film may cover the first surface of the semiconductor substrate along with the isolation portion.

[0037] More specifically, the removing operation may include forming a mask layer having a smaller area than the semiconductor substrate on the first conductive type semiconductor region on the other side of the semiconductor substrate, etching the first conductive type semiconductor region and the tunnel layer placed in a portion in which the mask layer has not been formed, and removing the mask layer.

[0038] Furthermore, the method may further include forming a second passivation film covering the second conductive type semiconductor region between the operation of forming the second conductive type semiconductor region and the operation of forming the first passivation film. The second passivation film may be placed on the side of the semiconductor substrate, and the first passivation film may be placed on the second passivation film.

BRIEF DESCRIPTION OF THE DRAWINGS

[0039] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiments of the invention and together with the description serve to explain the principle of the invention.

[0040] FIGS. 1 to 3 are diagrams illustrating a solar cell according to a first embodiment of the present invention;

[0041] FIG. 4 is a cross-sectional view of a solar cell for illustrating a modified example of the first embodiment of the present invention;

[0042] FIGS. 5 to 7 depict a solar cell according to a second embodiment of the present invention;

[0043] FIG. 8 depicts a comparison example different from the second embodiment of the present invention;

[0044] FIG. 9 is a diagram illustrating a solar cell according to a third embodiment of the present invention;

[0045] FIG. 10 is a comparison example photograph of the degree of the deterioration of a semiconductor substrate 100 according to firing temperatures in a thermal treatment process, which was taken through photo luminescence (PL), if the material of a paste for first bus bar is the same as the material of a paste for first finger electrodes;

[0046] FIG. 11 is photograph of the degree of the deterioration of the semiconductor substrate according to firing temperatures in a thermal treatment process, which was taken through photo luminescence (PL), if the material of the paste for the first bus bar is different from the material of the paste for the first finger electrodes in accordance with the third embodiment of the present invention;

[0047] FIG. 12 is a flowchart illustrating an example of a method for manufacturing a solar cell according to a first embodiment of the present invention;

[0048] FIGS. 13A to 13J are cross-sectional views of the method for manufacturing a solar cell according to the flowchart of FIG. 12;

[0049] FIG. 14 is a diagram illustrating a modified example of the method for manufacturing a solar cell according to the first embodiment;

[0050] FIG. 15 is a diagram illustrating another modified example of the method for manufacturing a solar cell according to the first embodiment;

[0051] FIG. 16 is a flowchart illustrating an example of a method for manufacturing a solar cell according to a second embodiment of the present invention; and

[0052] FIG. 17 is a flowchart illustrating an example of a method for manufacturing a solar cell according to a third embodiment of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0053] Embodiments of the present invention are described more fully hereinafter with reference to the accompanying drawings. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present invention. In order to clarify a description of the present invention, a description of parts not related to the description is omitted, and the same reference numbers are used throughout the specification to refer to the same or like parts.

[0054] In the drawings, the thickness of layers and an area has been enlarged for better

understanding and ease of description. When it is described that a part, such as a layer, film, area, or substrate, is "over" or "on" another part, the part may be "directly" on another part or a third part may be present between the two parts. In contrast, when it is described that a part is "directly on" another part, it means that a third part is not present between the two parts. Furthermore, when it is described that a part is "generally" formed on another part, it means the part is not formed on the entire surface (or front surface) of another part and is also not formed in part of the edge of the entire surface.

[0055] Furthermore, expressions, such as "the first" and "the second", are used to distinguish one part from the other part, and the present invention is not limited thereto.

[0056] Furthermore, a "front surface" may be one surface of a semiconductor substrate on which direct light is incident, and a "back surface" may be the opposite surface of the semiconductor substrate on which direct light is not incident or on which reflected light other than direct light may be incident.

[0057] Furthermore, if two values are the same, it means that the two values are the same within an error range of 10% or less.

[0058] Solar cells and methods for manufacturing the same according to embodiments of the present invention are described in detail below.

[0059] FIGS. 1 to 3 are diagrams illustrating a solar cell according to a first embodiment of the present invention.

[0060] FIG. 1 is a partial perspective view of the solar cell according to the first embodiment of the present invention, FIG. 2 is the entire cross-sectional view of the solar cell according to the first embodiment of the present invention, and FIG. 3 is the entire plan view of the back surface of the solar cell according to the first embodiment of the present invention.

[0061] Furthermore, FIG. 4 is a cross-sectional view of a solar cell for illustrating a modified example of the first embodiment of the present invention.

[0062] As shown in FIG. 1, an example of a solar cell according to an embodiment of the present invention includes a semiconductor substrate 100, a second conductive type semiconductor region 120, an anti-reflection layer 130, a tunnel layer 160, a first conductive type semiconductor region 170, a first passivation film 190A, a second passivation film 190B, a second electrode 140, and a first electrode 150.

[0063] In FIG. 1, the solar cell according to an embodiment of the present invention

has been illustrated as including the anti-reflection layer 130 and the second passivation film 190B, but the anti-reflection layer 130 and the second passivation film 190B may be omitted in some embodiments. However, an example in which the anti-reflection layer 130 and the second passivation film 190B are included in the solar cell is described below because better efficiency is obtained if the anti-reflection layer 130 and the second passivation film 190B are included from a viewpoint of efficiency of the solar cell.

[0064] The semiconductor substrate 100 may be made of a crystalline semiconductor including a single semiconductor material (e.g., a group 4 element). For example, the semiconductor substrate 100 may be made of a single crystal or polycrystalline semiconductor (e.g., single crystal or polycrystalline silicon). In particular, the semiconductor substrate 100 may be made of a single crystal semiconductor (e.g., a single crystal semiconductor wafer, more specifically, a single crystal silicon wafer).

[0065] If the semiconductor substrate 100 is made of a single crystal semiconductor (e.g., single crystal silicon) as described above, the solar cell is based on the semiconductor substrate 100 made of a single crystal semiconductor having less defects because it has high crystallizability. Accordingly, the solar cell can have excellent electrical characteristics. In embodiments of the invention, crystallizability may refer to a degree to which a material may be crystallize or crystallizable, for example.

[0066] Furthermore, the front surface and/or back surface of the semiconductor substrate 100 may be textured and may have concave-convex portions. For example, an external surface of the concave-convex portions may be formed of the (111) face of the semiconductor substrate 100 and may have a pyramid shape having an irregular size.

[0067] If the concave-convex portions are formed in the front surface of the semiconductor substrate 100 by texturing as described above and thus the surface roughness of the front surface is increased, the reflectance of light incident through the front surface of the semiconductor substrate 100 can be reduced.

[0068] Accordingly, an optical loss can be minimized because the amount of light which reaches a pn junction formed by a base region 110 and the first or second conductive type semiconductor region 170 or 120 is increased. In the present embodiment, the concave-convex portions have been illustrated as being formed in the front and back surfaces of the semiconductor substrate 100, thereby effectively preventing the reflection of light incident through both surfaces.

[0069] However, the present invention is not limited to the example. Accordingly, as shown in FIG. 4, the concave-convex portions may be formed only in the front surface of the semiconductor substrate 100, and concave-convex portions may not be formed in the back surface of the semiconductor substrate 100.

[0070] In this instance, the back surface of the semiconductor substrate 100 in which the tunnel layer 160 is formed may be formed to have smaller surface roughness than the front surface thereof so that the tunnel layer 160 is formed more stably and uniformly. Alternatively, the present invention may be modified in various ways, for example, concave-convex portions may not be formed in the front and back surfaces of the semiconductor substrate 100.

[0071] Referring back to FIG. 2, in the present embodiment, the semiconductor substrate 100 may include the base region 110 doped with impurities of a first or second conductive type at a low doping concentration and configured to have the first or second conductive type.

[0072] In this instance, the base region 110 of the semiconductor substrate 100 may have a lower doping concentration, higher resistance, or lower carrier concentration than one of the first and second conductive type semiconductor regions 170 and 120, which has the same conductive type as the base region 110.

[0073] The first conductive type semiconductor region 170 having the first conductive type may be placed on one surface (e.g., the back surface) of the semiconductor substrate 100. For example, the tunnel layer 160 may be formed on the semiconductor substrate 100, and the first conductive type semiconductor region 170 may be formed on the tunnel layer 160.

[0074] In this instance, the tunnel layer 160 may be disposed on the back surface of the semiconductor substrate 100 and may have a direct contact with the semiconductor substrate 100.

[0075] Such a tunnel layer 160 may be generally formed in portions other than an isolation portion I in the back surface of the semiconductor substrate 100. In this instance, "generally formed" may include "generally formed closely" and "some areas are not inevitably formed." Accordingly, the tunnel layer 160 can be easily formed because a separate patterning process is not required. However, the present invention is not limited to such an example.

[0076] Such a tunnel layer 160 may generate a tunneling effect. More specifically,

the tunnel layer 160 may function as a kind of barrier for electrons and holes.

[0077] That is, the tunnel layer 160 may not transmit minority carriers. After the minority carriers are accumulated in a portion neighboring the tunnel layer 160, only majority carriers having energy of a specific level or higher may pass through the tunnel layer 160. The majority carriers having energy of a specific level or higher may easily pass through the tunnel layer 160 by a tunneling effect.

[0078] Furthermore, the tunnel layer 160 may also function as a diffusion barrier for preventing the dopant of the first conductive type semiconductor region 170 from being diffused into the semiconductor substrate 100. The tunnel layer 160 may include various materials through which majority carriers can be tunneled. For example, the tunnel layer 160 may include oxides, nitrides, a semiconductor, and a conductive polymer.

[0079] In particular, the tunnel layer 160 may be formed of a silicon oxide (SiOx) layer including silicon oxide. The reason for this is that the silicon oxide layer has an excellent passivation characteristic and carriers can easily tunnel through the silicon oxide layer.

[0080] In some embodiments, the tunnel layer 160 may be made of a dielectric material including SiCx having strong durability even in a high temperature process or may be made of SiNx, hydrogenated SiNx, AlOx, SiON, or hydrogenated SiON.

[0081] Furthermore, in order to sufficiently implement the tunneling effect, the thickness of the tunnel layer 160 may be smaller than the thickness of each of the first and the second passivation films 190A and 190B and the first and the second conductive type semiconductor regions 170 and 120.

[0082] For example, the thickness of the tunnel layer 160 may be 0.5 nm ~ 2.5 nm. In this instance, the tunnel layer 160 may be formed by an oxidation process, an LPCVD process, or a PECVD deposition process, for example.

[0083] The thickness of the tunnel layer 160 is limited to the range of 0.5 nm ~ 2.5 nm in order to implement the tunneling effect. The range of 0.5 nm ~ 2.5 nm may be slightly exceeded. In this instance, however, the tunneling effect may be reduced.

[0084] More specifically, the tunnel layer 160 is formed to have the thickness of 0.5 nm or higher because it is practically very difficult to form the tunnel layer 160 having a thickness of less than 0.5 nm. Furthermore, the tunnel layer 160 is formed to have the thickness of 2.5 nm or less because the tunneling effect is meager if the thickness

exceeds 2.5 nm.

[0085] The first conductive type semiconductor region 170 may be placed on the back surface of the semiconductor substrate 100, may include impurities of the first conductive type having a higher concentration than the impurities of the first conductive type included in the semiconductor substrate 100, and may include a polycrystalline silicon material.

[0086] That is, the first conductive type semiconductor region 170 may be formed on the back surface of the tunnel layer 160 formed on the back surface of the semiconductor substrate 100 and may be isolated from the semiconductor substrate 100, as shown in FIG. 1.

[0087] The first conductive type semiconductor region 170 may be brought into contact with and formed on the tunnel layer 160, thereby simplifying the structure of the solar cell and maximizing the tunneling effect of the tunnel layer 160.

[0088] If the first conductive type semiconductor region 170 is not formed within the semiconductor substrate 100, the first conductive type semiconductor region 170 is formed on the back surface of the semiconductor substrate 100, but spaced apart from the semiconductor substrate 100 as shown in FIGS. 1 and 2, and the first conductive type semiconductor region 170 includes a polycrystalline silicon material formed on the back surface of the tunnel layer 160, the open voltage Voc of the solar cell can be further improved.

[0089] Furthermore, the first conductive type semiconductor region 170 is not formed within the semiconductor substrate 100, but is formed outside the semiconductor substrate 100. Accordingly, the characteristics of the semiconductor substrate 100 can be prevented from being deteriorated because thermal damage to the semiconductor substrate 100 is minimized in the process of forming the first conductive type semiconductor region 170 from a viewpoint of a manufacturing process. Accordingly, an embodiment of the present invention can further improve efficiency of the solar cell.

[0090] The thickness of the first conductive type semiconductor region 170 may be 50 nm ~ 500 nm.

[0091] The first conductive type semiconductor region 170 may include the same semiconductor material (more specifically, a silicon semiconductor material) as the semiconductor substrate 100. Accordingly, a difference between the characteristics of the second conductive type semiconductor region 120 and the semiconductor substrate

100 can be minimized because the second conductive type semiconductor region 120 has similar characteristics as the semiconductor substrate 100.

[0092] In this instance, since the first conductive type semiconductor region 170 is formed on the semiconductor substrate 100 separately from the semiconductor substrate 100, the first conductive type semiconductor region 170 may have a crystal structure different from the crystal structure of the semiconductor substrate 100 so that it is easily formed on the semiconductor substrate 100.

[0093] For example, the first conductive type semiconductor region 170 may be formed by doping impurities of the first conductive type into an amorphous silicon material, a fine crystal silicon material, or a polycrystalline silicon material which may be easily manufactured using various methods, such as deposition.

[0094] In particular, if the first conductive type semiconductor region 170 includes a polycrystalline silicon material, carriers can smoothly move because the first conductive type semiconductor region 170 has excellent electrical conductivity and the tunneling of carriers can be smoothly generated in the tunnel layer 160 made of oxide.

[0095] The second conductive type semiconductor region 120 is placed on the opposite surface of the semiconductor substrate 100, for example, on the front surface of the semiconductor substrate 100 on which light is incident. The second conductive type semiconductor region 120 may include impurities of the second conductive type which is opposite the conductive type of the semiconductor substrate 100, for example, a conductive type of an n type.

[0096] For example, in the present embodiment, the second conductive type semiconductor region 120 may be formed into a doping region formed by doping impurities of the second conductive type into part of the semiconductor substrate 100.

[0097] For example, the second conductive type semiconductor region 120 may be formed by diffusing the impurities of the second conductive type into the front surface of the semiconductor substrate 100. In this instance, the second conductive type semiconductor region 120 may be made of the same silicon material as the semiconductor substrate 100.

[0098] For example, if the semiconductor substrate 100 is formed of a wafer made of a polycrystalline silicon material, the second conductive type semiconductor region 120 may also be made of a polycrystalline silicon material. Furthermore, the second conductive type semiconductor region 120 in which the semiconductor substrate 100 is

formed of a wafer made of a single crystal silicon material may also be made of a single crystal silicon material.

[0099] The base region 110 and the second conductive type semiconductor region 120 may have the same crystal structure and semiconductor material as the semiconductor substrate 100, but may have different conductive types or different doping concentrations.

[00100] More specifically, if the base region 110 has the first conductive type, the base region 110 and the second conductive type semiconductor region 120 may have different conductive types. If the base region 110 has the second conductive type, the second conductive type semiconductor region 120 may have a higher doping concentration than the base region 110.

[00101] If the base region 110 has the first conductive type, the first conductive type semiconductor region 170 having the first conductive type has the same conductive type as the semiconductor substrate 100 and may form a back surface field (BSF) region which has a higher doping concentration than the semiconductor substrate 100 and forms a BSF. The second conductive type semiconductor region 120 having the second conductive type has a conductive type different from that of the base region 110 and may form an emitter region forming a pn junction along with the base region 110.

[00102] Accordingly, the second conductive type semiconductor region 120 forming the emitter region is placed on the front surface side of the semiconductor substrate 100, thereby being capable of minimizing the path of light regioned with the pn junction.

[00103] However, the present invention is not limited to the example. For example, if the base region 110 has the second conductive type, the first conductive type semiconductor region 170 forms the emitter region, and the second conductive type semiconductor region 120 has the same conductive type as the semiconductor substrate 100 and may form a front surface field (FSF) region which has a higher doping concentration than the semiconductor substrate 100 and forms a FSF.

[00104] A p type dopant used as the impurities of the first or second conductive type may include group 3 elements, such as boron (B), aluminum (Al), gallium (Ga), and indium (In). An n type dopant used as the impurities of the first or second conductive type may include group 5 elements, such as phosphorous (P), arsenic (As), bismuth (Bi), and antimony (Sb). However, the present invention is not limited to the examples, and various dopants may be used as the impurities of the first or second conductive type.

[00105] In the present embodiment, the first conductive type semiconductor region 170 formed separately from the semiconductor substrate 100 may be placed on the back surface side of the semiconductor substrate 100, and the second conductive type semiconductor region 120 forming part of the semiconductor substrate 100 may be placed on the front surface side of the semiconductor substrate 100.

[00106] If the first conductive type semiconductor region 170 having a crystal structure different from that of the semiconductor substrate 100 is placed on the front surface side of the semiconductor substrate 100, the amount of light reaching the pn junction may be reduced because the absorption of light in the first conductive type semiconductor region 170 is increased. Accordingly, the first conductive type semiconductor region 170 may be placed on the back surface side of the semiconductor substrate 100, but the present invention is not limited thereto.

[00107] The passivation films 190A and 190B may be generally formed on the first and the second conductive type semiconductor regions 170 and 120 other than opening portions 102 and 104 respectively corresponding to the first and the second electrodes 150 and 140. Each of the passivation films 190A and 190B may be formed of an undoped passivation film not separately including a dopant.

[00108] More specifically, the first passivation film 190A may be generally formed on (e.g., brought into contact with) the portions of the first conductive type semiconductor region 170 other than the opening portion 102. The second passivation film 190B may be generally formed on (e.g., brought into contact with) the portions of the second conductive type semiconductor region 120 other than the opening portion 104.

[00109] Furthermore, the anti-reflection layer 130 may be placed on the second passivation film 190B.

[00110] The passivation films 190A and 190B are brought into contact with and formed on the first and the second conductive semiconductor regions 170 and 120, thereby being capable of immobilizing defects present in the first and the second conductive type semiconductor regions 170 and 120.

[00111] Accordingly, the open voltage Voc of the solar cell can be increased because the recombination sites of minority carriers are removed. The anti-reflection layer 130 can reduce the reflectance of light incident on the front surface of the semiconductor substrate 100.

[00112] Accordingly, the amount of light reaching the pn junction formed at the

interface of the base region 110 and the first conductive type semiconductor region 170 can be increased because the reflectance of light incident through the front surface of the semiconductor substrate 100 is lowered. Accordingly, the short circuit current Isc of the solar cell can be increased. As a result, efficiency of the solar cell can be improved because the open voltage and short circuit current of the solar cell are increased by the passivation films 190A and 190B and the anti-reflection layer 130 as described above.

[00113] For example, the passivation film 190A, 190B or the anti-reflection layer 130 may have a single film selected from the group consisting of a silicon nitride film, a silicon nitride film including hydrogen, a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, MgF_2, ZnS, TiO_2, and CeO_2 or may have a multi-layer structure in which two or more films selected from the group are combined.

[00114] For example, if a contacted conductive semiconductor region of the first and the second conductive semiconductor regions 170 and 120 has an n type, a corresponding one of the first and the second passivation films 190A and 190B may include a silicon oxide film or a silicon nitride film having fixed positive charges. If the contacted conductive semiconductor region has a p type, the corresponding passivation film may include an aluminum oxide film having fixed negative charges. Furthermore, the anti-reflection layer 130 may include silicon nitride, for example.

[00115] More specifically, in an embodiment of the present invention, the first passivation film 190A brought into contact with the first conductive type semiconductor region 170 may be formed of a silicon nitride film, may have a refractive index of 1.9 ~ 2.1, and may have a thickness of 30 nm ~ 50 nm.

[00116] Furthermore, the second passivation film 190B brought into contact with the second conductive type semiconductor region 120 may have a dual-layer structure in which an aluminum oxide film and a silicon nitride film are sequentially stacked on the second conductive type semiconductor region 120. In this instance, the aluminum oxide film may have a refractive index of 1.5 ~ 1.7 and a thickness of 5 nm ~ 10 nm. The silicon nitride film of the second passivation film 190B may have a refractive index of 1.9 ~ 2.1 and a thickness of 70 nm ~ 120 nm.

[00117] However, the present invention is not limited to the examples. The passivation films 190A and 190B and the anti-reflection layer 130 may include various materials.

[00118] The first electrode 150 is placed on (e.g., brought into contact with) on the first conductive type semiconductor region 170 and electrically connected to the first conductive type semiconductor region 170. The first electrode 150 may be electrically connected to the first conductive type semiconductor region 170 through the opening portion 102 formed in the first passivation film 190A (i.e., by penetrating the first passivation film 190A).

[00119] In this instance, the first electrode 150 penetrates the first passivation film 190A and is connected to the first conductive type semiconductor region 170, but may be connected to a surface of the first conductive type semiconductor region 170.

[00120] Likewise, the second electrode 140 is placed on (e.g., brought into contact with) the second conductive type semiconductor region 120 and electrically connected to the second conductive type semiconductor region 120. The second electrode 140 may be electrically connected to the first conductive type semiconductor region 170 through the opening portion 104 formed in the second passivation film 190B and the anti-reflection layer 130 (i.e., through the second passivation film 190B and the anti-reflection layer 130).

[00121] The first and the second electrodes 150 and 140 may include various materials (more specifically, metal) and may have various shapes.

[00122] For example, the first electrode 150 may include a plurality of first finger electrodes 151 and a plurality of first bus bars 153, as shown in FIG. 1.

[00123] The plurality of first finger electrodes 151 may be spaced apart from each other on the back surface of the first conductive type semiconductor region 170, may be extended in a first direction x, and may collect carriers moved toward the first conductive type semiconductor region 170.

[00124] Furthermore, the plurality of first bus bars 153 may be placed on the same layer as the plurality of first finger electrodes 151 on the first conductive type semiconductor region 170, may electrically connect the plurality of first finger electrodes 151, and may be extended in a second direction y crossing the plurality of first finger electrodes 151.

[00125] Furthermore, the second electrode 140 may include a plurality of second finger electrodes 141 and a plurality of second bus bars 143, as shown in FIG. 1.

[00126] The plurality of second finger electrodes 141 may be placed on the second conductive type semiconductor region 120, may be electrically connected to the second

conductive type semiconductor region 120, may be spaced apart from each other, and may be extended in the first direction x.

[00127] The plurality of second finger electrodes 141 may collect carriers, for example, holes moved toward the second conductive type semiconductor region 120.

[00128] Furthermore, the plurality of second bus bars 143 may be placed on the same layer as the plurality of second finger electrodes 141 on the second conductive type semiconductor region 120, may electrically connect the plurality of second finger electrodes 141, and may be extended in the second direction y crossing the plurality of second finger electrodes 141.

[00129] In the solar cell having such a structure, the tunnel layer 160 and the first conductive type semiconductor region 170 placed on the back surface of the semiconductor substrate 100 may be spaced apart from the edge of the back surface of the semiconductor substrate 100 (or the side of the semiconductor substrate 100) at a first distance D1.

[00130] Accordingly, the area of each of the tunnel layer 160 and the first conductive type semiconductor region 170 may be smaller than the area of the semiconductor substrate 100. The first distance D1 may mean the shortest distance of distances between the edge of the back surface of the semiconductor substrate 100 and the tunnel layer 160 and the first conductive type semiconductor region 170.

[00131] That is, the isolation portion I in which the tunnel layer 160 and the first conductive type semiconductor region 170 (including the first electrode 150 connected to the first conductive type semiconductor region 170 in addition to the tunnel layer 160 and the first conductive type semiconductor region 170) are not formed may be placed at the edge of the back surface of the semiconductor substrate 100. In this instance, the first passivation film 190A may be formed to cover one surface of the semiconductor substrate 100, including the isolation portion I.

[00132] The isolation portion I may block a contact between the first conductive type semiconductor region 170 and the second conductive type semiconductor region 120 in any one of the first surface, side, and second surface of the semiconductor substrate 100. For example, the isolation portion I may function as an edge isolator for isolating the first conductive type semiconductor region 170 from the edge of the back surface of the semiconductor substrate 100.

[00133] That is, when the second conductive type semiconductor region 120 is formed,

the impurities of the second conductive type may be diffused into the side of or the edge of the back surface of the semiconductor substrate 100, and thus the first conductive type semiconductor region 170 and the second conductive type semiconductor region 120 may be unwantedly short-circuited in the side of or the edge of the back surface of the semiconductor substrate 100. In the present embodiment, such a problem can be fundamentally prevented by removing the first conductive type semiconductor region 170 from the edge of the back surface of the semiconductor substrate 100.

[00134] Furthermore, the area of the second conductive type semiconductor region 120 can be maximized because the second conductive type semiconductor region 120 is generally formed on the front surface of the semiconductor substrate 100.

[00135] The isolation portion I may be formed in the entire edge of the back surface of the semiconductor substrate 100 and may have a closed shape, as shown in FIG. 3. Furthermore, a specific step or operation is present between portions in which the isolation portion I and the tunnel layer 160 and the first conductive type semiconductor region 170 have been formed.

[00136] For example, the first distance D1 (i.e., the width of the isolation portion I) may be 1 mm or less. If the first distance D1 exceeds 1 mm, efficiency may be deteriorated because the area of the first conductive type semiconductor region 170 is reduced. For example, the first distance D1 may be 1 nm to 1 mm. If the first distance D1 is less than 1 mm, the effect of the isolation portion I may not be sufficient. However, the present invention is not limited to the above values. The first distance D1 may have a different value depending on the size of the semiconductor substrate 100, for example.

[00137] The first conductive type semiconductor region 170 may have a shape having a smaller area as the first conductive type semiconductor region 170 becomes distant from the semiconductor substrate 100. In this instance, the side of the first conductive type semiconductor region 170 may be formed to be not vertical to the semiconductor substrate 100 (e.g., approximately slanted) as the first conductive type semiconductor region 170 becomes distant from the semiconductor substrate 100.

[00138] That is, as shown in FIG. 2, the thickness of the edge region of the first conductive type semiconductor region 170 may be gradually decreased toward the isolation portion I.

[00139] For example, the area of the first conductive type semiconductor region 170

may be reduced as the first conductive type semiconductor region 170 becomes distant from the semiconductor substrate 100, so the side of the first conductive type semiconductor region 170 may be formed to be rounded. The side of the tunnel layer 160 may be placed so that it is extended along with the side of the first conductive type semiconductor region 170 and may have a rounded shape similar to the first conductive type semiconductor region 170.

[00140] The reason for this is that a wet process is used in the process of forming the isolation portion I by removing the first conductive type semiconductor region 170 and the tunnel layer 160. This is described later. In some embodiments, the sides of the first conductive type semiconductor region 170 and the tunnel layer 160 may have various shapes in addition to the rounded shape.

[00141] Furthermore, the first passivation film 190A placed on the back surface side of the semiconductor substrate 100 may be placed on the first conductive type semiconductor region 170 in the portion in which the tunnel layer 160 and the first conductive type semiconductor region 170 are present and may come into contact with the back surface of the semiconductor substrate 100 in the isolation portion I.

[00142] That is, the first passivation film 190A may be directly brought into contact with and formed on the back surface of the semiconductor substrate 100 near the edge of the semiconductor substrate 100, may be extended from the edge of the semiconductor substrate 100, may be brought into contact with and formed on the sides of the tunnel layer 160 and the first conductive type semiconductor region 170 while covering the sides, may be extended from the sides, and may be brought into contact with and formed on the top surface of the first conductive type semiconductor region 170 while covering the top surface.

[00143] In an embodiment of the present invention, in the process of manufacturing the solar cell, the isolation portion I may be formed by removing the tunnel layer 160 and the first conductive type semiconductor region 170 placed in the edge of the back surface of the semiconductor substrate 100.

[00144] Accordingly, the first passivation film 190A may be formed to cover an edge portion of the back surface of the semiconductor substrate 100 which has been exposed by removing the tunnel layer 160 and the second conductive type semiconductor region 160, that is, the isolation portion I.

[00145] Accordingly, the isolation portion I can prevent a passivation characteristic

from being deteriorated. In this instance, the structure of the solar cell and the process of manufacturing the solar cell can be simplified because the first passivation film 190A is used without forming a separate film for protecting the isolation portion I.

[00146] Furthermore, the first passivation film 190A may include a side portion 190Aa extended up to the top of the side of the semiconductor substrate 100. If the side portion 190Aa of the first passivation film 190A is used, the first passivation film 190A may be formed to cover the upper side of the back surface of the semiconductor substrate 100 generally and stably.

[00147] Furthermore, the second passivation film 190B and the anti-reflection layer 130 may include side portions 190Ba and 130a extended up to the top of the side of the semiconductor substrate 100.

[00148] In this instance, the second passivation film 190B may be placed close to the semiconductor substrate 100 on the side of the semiconductor substrate 100, and the first passivation film 190A may be placed on the second passivation film 190B.

[00149] More specifically, the side portion 190Ba of the second passivation film 190B may come into contact with the side of the semiconductor substrate 100. The side portion 130a of the anti-reflection layer 130 may come into contact with the side portion 190Ba of the second passivation film 190B. The side portion 190Aa of the first passivation film 190A may come into contact with the side portion 130a of the anti-reflection layer 130.

[00150] Accordingly, the second conductive type semiconductor region 120 can be stably passivated because the second passivation film 190B is first formed and the first passivation film 190A is then formed in the process of forming the first passivation film 190A. This is described in more detail later.

[00151] However, the present invention is not limited to the example. For example, at least one of the side portions 190Aa, 190Ba, and 130a may not be provided on the side of the semiconductor substrate 100, or sequence in which the side portions 190Aa, 190Ba, and 130a are stacked may be changed.

[00152] A plane shape of the first electrode 150 is described in detail with reference to FIG. 3, and a plane shape of the second electrode 140 is then described in detail.

[00153] Referring to FIG. 3, the first electrode 150 may include the plurality of first finger electrodes 151 spaced apart from each other at a specific pitch. In FIG. 3, the first finger electrodes 151 have been illustrated as being parallel and as being parallel in

the edge of the semiconductor substrate 100, but the present invention is not limited thereto.

[00154] Furthermore, only one first bus bar 153 may be included. As shown in FIG. 3, a plurality of the first bus bars 153 having a pitch greater than the pitch between the first finger electrodes 151 may be included.

[00155] The width of the first bus bar 153 may be greater than the width of the first finger electrode 151, but the present invention is not limited thereto. Accordingly, the width of the first bus bar 153 may be the same as or smaller than the width of the first finger electrode 151.

[00156] When viewed from a cross section, both the first finger electrodes 151 and first bus bar 153 of the first electrode 150 may be formed to penetrate the first passivation film 190A. That is, the opening portion 102 may be formed in accordance with all of the first finger electrodes 151 and first bus bar 153 of the first electrode 150.

[00157] However, the present invention is not limited to the example. For example, the first finger electrodes 151 of the first electrode 150 may be formed to penetrate the first passivation film 190A, and the first bus bar 153 may be formed on the first passivation film 190A. In this instance, the opening portion 102 may be formed to have a shape corresponding to the first finger electrodes 151, but may not be formed in a portion in which only the first bus bar 153 is placed.

[00158] As described above, in the present embodiment, the isolation portion I may be formed in the portion in which the tunnel layer 160 and the first conductive type semiconductor region 170 are not formed along the edge of the semiconductor substrate 100. Accordingly, the first electrode 150 formed on the first conductive type semiconductor region 170 may not be formed in the isolation portion I.

[00159] Accordingly, the ends of the first finger electrodes 151 and bus bar 153 of the first electrode 150 may be spaced apart from the edge of the semiconductor substrate 100 at least at the first distance D1.

[00160] Furthermore, the second finger electrodes 141 and second bus bar 142 of the second electrode 140 may be respectively formed in accordance with the first finger electrodes 151 and first bus bar 153 of the first electrode 150.

[00161] The contents described in connection with the first finger electrodes 151 and first bus bar 153 of the first electrode 150 may be applied to the second finger electrodes 141 and second bus bar 142 of the second electrode 140 without a change except the

contents described in connection with the isolation portion I.

[00162] Furthermore, the contents related to the first passivation film 190A in the first electrode 150 may be applied to the second passivation film 190B and the anti-reflection layer 130 in the second electrode 140 without a change.

[00163] In this instance, the width and pitch of the first finger electrodes 151 and first bus bar 153 of the first electrode 150 may be the same as or different from the width and pitch of the second finger electrodes 141 and second bus bar 142 of the second electrode 140.

[00164] However, the present invention is not limited to the example. For example, the first electrode 150 and the second electrode 140 may have different plane shapes and may be modified in various ways.

[00165] As described above, in the present embodiment, since the first and the second electrodes 150 and 140 of the solar cell have a specific pattern, the solar cell has a bi-facial structure in which light may be incident on the front and back surfaces of the semiconductor substrate 100.

[00166] Accordingly, efficiency of the solar cell can be improved because the amount of light used in the solar cell is increased. However, the present invention is not limited to the bi-facial structure. For example, the solar cell may have a structure in which the first electrode 150 is generally formed on the back surface side of the semiconductor substrate 100 and may have various structures.

[00167] In this instance, if the isolation portion I is formed on the back surface of the semiconductor substrate 100, the first conductive type semiconductor region 170 and the second conductive type semiconductor region 120 can be effectively prevented from being unnecessarily interconnected.

[00168] Furthermore, a surface of the semiconductor substrate 100 on which the isolation portion I is placed may be covered and passivated by the first passivation film 190A covering the first conductive type semiconductor region 170.

[00169] Accordingly, problems attributable to surface recombination can be minimized because the isolation portion I is passivated by such a simple structure. That is, efficiency and reliability of a solar cell can be improved and a defective ratio of the solar cell can be reduced by the simple structure.

[00170] In the first embodiment of the present invention, an example in which the first electrode 150 penetrates the first passivation film 190A and the first electrode 150 is

connected to the first conductive type semiconductor region 170, but is connected to a surface of the first conductive type semiconductor region 170 has been described.

[00171] In some embodiments, however, the first electrode 150 penetrates the first passivation film 190A and is connected to the first conductive type semiconductor region 170, but at least part of the first electrode 150 may be depressed and formed in the first conductive type semiconductor region 170. This is described in more detail below.

[00172] FIGS. 5 to 7 depict a solar cell according to a second embodiment of the present invention.

[00173] FIG. 5 is a cross-sectional view of the solar cell taken along line Ⅱ-Ⅱ of FIG. 1. Furthermore, FIG. 6 is an enlarged view of a portion K in FIG. 5, and FIG. 7 is a real photograph of a contact portion between the first electrode 150 and the first conductive type semiconductor region 170.

[00174] Furthermore, FIG. 8 depicts a comparison example different from the second embodiment of the present invention.

[00175] A description of contents redundant with the contents described with reference to FIGS. 1 to 4 is omitted.

[00176] For reference, in FIG. 5, a region that belongs to the first conductive type semiconductor region 170 and that is placed in the space between the first finger electrode 151 and the tunnel layer 160 is called a finger forming region 170A1. A region that belongs to the first conductive type semiconductor region 170 and that is placed in the space between the first bus bar 153 and the tunnel layer 160 is called a bus bar forming region 170A2. The remaining regions of the first conductive type semiconductor region 170 other than the finger forming region 170A1 and the bus bar forming region 170A2 is called a non-forming region 170B. Furthermore, the finger forming region 170A1 and the bus bar forming region 170A2 are collectively called an electrode forming region 170A.

[00177] In the solar cell according to the second embodiment of the present invention, at least part of the first electrode 150 may penetrate the first passivation film 190A and may be depressed into the first conductive type semiconductor region 170 and electrically connected to the first conductive type semiconductor region 170, as shown in FIGS. 5 and 6.

[00178] For example, both the first finger electrode 151 and first bus bar 153 of the

first electrode 150 may be depressed and formed in the first conductive type semiconductor region 170.

[00179] In other words, as shown in FIG. 6, the location of a first boundary surface BS1 in which the first conductive type semiconductor region 170 and the first electrode 150 come into contact with each other may be more depressed and formed toward the semiconductor substrate 100 than the location of a second boundary surface BS2 in which the first conductive type semiconductor region 170 and the first passivation film 190A come into contact with each other.

[00180] Accordingly, the distance between the semiconductor substrate 100 and the first boundary surface BS1 may be smaller than the distance between the semiconductor substrate 100 and the second boundary surface BS2.

[00181] In this instance, all of the plurality of first finger electrodes 151 and the first bus bar 153 may be formed to have a single layer or double layer structure. In some embodiments, the plurality of first finger electrodes 151 may be formed to have a single layer structure, and the first bus bar 153 may be formed to have a double layer structure.

[00182] In FIG. 6, the first finger electrode 151 has been illustrated as being an example. Like the first finger electrode 151, the first bus bar 153 may have the same structure in which it has been depressed into the first conductive type semiconductor region 170.

[00183] As described above, the structure in which the first electrode 150 has been depressed into the first conductive type semiconductor region 170 may be formed when a paste for the first electrode perforates the first passivation film 190A and penetrates the first conductive type semiconductor region 170 in a thermal treatment process in the state in which the paste for the first electrode for forming the first electrode 150 has been patterned and formed on the back surface of the first passivation film 190A.

[00184] If the first electrode 150 is formed by the process of printing and thermally treating the paste for the first electrode as described above, there are advantages in that a cost is relatively low compared to a plating method and a process time can be reduced.

[00185] In this instance, a difference TBS between the heights of the first boundary surface BS1 and the second boundary surface BS2 may be set to 1 nm ~ 20 nm. The difference between the heights of the first and the second boundary surfaces BS1 and BS2 may vary depending on the time taken for the thermal treatment process for forming the first electrode 150 and content of frit glass included in the paste for the first

electrode.

[00186] FIGS. 5 and 6 have illustrated an example in which all of the plurality of first bus bars 153 and the plurality of first finger electrodes 151 forming the first electrode 150 have been depressed into the first conductive type semiconductor region 170.

[00187] However, the present invention is not necessarily limited to the example. For example, only the plurality of first finger electrodes 151 of the first electrode 150 may be depressed and formed in the first conductive type semiconductor region 170. The example in which only the plurality of first finger electrodes 151 has been depressed into the first conductive type semiconductor region 170 as described above is described in detail later with reference to FIG. 9 and related drawings.

[00188] Accordingly, in the solar cell according to an embodiment of the present invention, as shown in FIG. 6, the first electrode 150 may be depressed into the first conductive type semiconductor region 170, and the first conductive type semiconductor region 170 and the first electrode 150 may come into contact with each other in the first boundary surface BS1 of the first conductive type semiconductor region 170.

[00189] In this instance, as shown in FIG. 5, a plurality of metal crystals MC extracted from the first electrode 150 may be placed in the electrode forming region 170A of the first conductive type semiconductor region 170 in which the first electrode 150 has been formed, as described above.

[00190] For example, as shown in FIG. 6, the plurality of metal crystals MC extracted from the first finger electrode 151 may be placed in the finger forming region 170A1 of the first conductive type semiconductor region 170 in which the first finger electrode 151 is formed.

[00191] Only the electrode finger forming region 170A1 of the electrode forming region 170A of the first conductive type semiconductor region 170 has been illustrated in FIG. 6. Likewise, the plurality of metal crystals MC extracted from the first bus bar 153 may be placed in the bus bar forming region 170A2, as shown in FIG. 5.

[00192] The plurality of metal crystals MC has relatively low resistance compared to the first conductive type semiconductor region 170 made of polycrystalline silicon. Accordingly, as shown in FIG. 6, carriers which have moved from the semiconductor substrate 100 to the first conductive type semiconductor region 170 through the tunnel layer 160, for example, electrons may directly move to the first electrode 150 through the metal crystals MC or may jump between the metal crystals MC and the metal

crystals MC and move to the first electrode 150.

[00193] Accordingly, the plurality of metal crystals MC may function to help carriers to move to the first electrode 150 more easily.

[00194] Accordingly, the metal crystals MC may narrow a substantial distance between the semiconductor substrate 100 and the first electrode 150 due to its low resistance.

[00195] Furthermore, when the first electrode 150 is connected to the first conductive type semiconductor region 170, the metal crystals MC are formed in the direction of the semiconductor substrate 100 on the basis of the first boundary surface BS1, that is, the boundary of the first electrode 150 and the first conductive type semiconductor region 170. Accordingly, contact resistance between the first electrode 150 and the first conductive type semiconductor region 170 can be further lowered.

[00196] Accordingly, if the plurality of metal crystals MC is further included in the first conductive type semiconductor region 170 between the first electrode 150 and the tunnel layer 160 as in the embodiment of the present invention shown in FIG. 6, efficiency of the solar cell can be further improved.

[00197] As shown in FIG. 5, the metal crystals MC may be placed in the electrode forming region 170A of the first conductive type semiconductor region 170 in which the first electrode 150 has been formed, but may not be placed in the non-forming region 170B of the first conductive type semiconductor region 170 in which the first electrode 150 has not been formed.

[00198] The reason why the metal crystals MC are placed in the electrode forming region 170A of the first conductive type semiconductor region 170, but are not placed in the non-forming region 170B of the first conductive type semiconductor region 170 as described above is that metal extracted from the first electrode 150 during the thermal treatment process for forming the first electrode 150 is recrystallized to form the plurality of metal crystals MC.

[00199] For example, the plurality of first electrodes 150 may be formed to include at least one conductive metal material. In this instance, the conductive metal material included in the plurality of first electrodes 150 may be at least one selected from the group consisting of nickel (Ni), copper (Cu), silver (Ag), aluminum (Al), tin (Sn), zinc (Zn), indium (In), titanium (Ti), and gold (Au) and a combination of them, for example, but may include other conductive metal materials.

[00200] In this instance, the plurality of metal crystals MC may include the same metal material as a metal material included in the first electrode 150 because the metal crystals MC are formed when the metal material included in the first electrode 150 is extracted and recrystallized.

[00201] Accordingly, if the first electrode 150 includes silver (Ag), for example, the metal crystals MC may also include silver (Ag).

[00202] Furthermore, as shown in FIGS. 6 and 7, the metal crystals MC are placed in the first conductive type semiconductor region 170, but may not be placed in the tunnel layer 160.

[00203] That is, if the metal crystals MC are placed in the tunnel layer 160 as in the comparison example of FIG. 8, the functions of the tunnel layer 160 may be deteriorated. If the metal crystals MC penetrate the back surface of the semiconductor substrate 100 through the tunnel layer 160, an open voltage (Voc) characteristic appearing due to the structure of the semiconductor substrate 100 – the tunnel layer 160 - the first conductive type semiconductor region 170 may be deteriorated, thereby being capable of deteriorating the semiconductor substrate 100.

[00204] If the semiconductor substrate 100 is deteriorated as described above, a characteristic of the semiconductor substrate 100, for example, a characteristic, such as a carrier life time, may be deteriorated.

[00205] If the metal crystals MC are placed in the first conductive type semiconductor region 170, but are not placed in the tunnel layer 160 as in the embodiment of the present invention, however, the deterioration of the characteristic described above can be prevented.

[00206] As shown in FIG. 6, some metal crystals MC1 of the plurality of metal crystals MC may have a direct contact with the first electrode 150. Furthermore, at least one metal crystal MC2 of the plurality of metal crystals MC may be spaced apart from the first electrode 150 and placed in the first conductive type semiconductor region 170.

[00207] In this instance, the length LMC of the plurality of metal crystals MC from the first electrode 150 to the direction of the tunnel layer 160 may be 2/3 or less of the thickness of the first conductive type semiconductor region 170. If the length LMC of the metal crystals MC is limited to 2/3 of the thickness of the first conductive type semiconductor region 170 as described above, damage to the tunnel layer 160 or the

semiconductor substrate 100 attributable to the excessive length LMC of the metal crystals MC can be prevented.

[00208] Some of the plurality of metal crystals MC may have a reduced width WMC from the first electrode 150 to the direction of the tunnel layer 160. That is, as shown in FIG. 6 or 7, the width WMC in the surface direction (x, y) of a portion that belongs to the metal crystal MC and that neighbors the first electrode 150 may be smaller than the width of a portion that belongs to the metal crystal MC and that is adjacent to the semiconductor substrate 100.

[00209] Such a size of the metal crystal MC may be determined in proportion to a firing temperature of the thermal treatment process for forming the first electrode 150.

[00210] That is, the length or width of the metal crystal MC is characterized in that it is increased as the firing temperature of thermal treatment process for forming the first electrode 150 rises and it is reduced as the firing temperature of thermal treatment process for forming the first electrode 150 drops. The length or width of the metal crystal MC may be increased as the width of the first electrode 150, that is, the source of the metal crystal MC, is increased.

[00211] If the firing temperature of the thermal treatment process for forming the first electrode 150 is excessively low, however, contact resistance between the first electrode 150 and the first conductive type semiconductor region 170 may be increased.

[00212] Accordingly, in the second embodiment of the present invention, an example in which all of the first finger electrodes 151 and first bus bar 153 of the first electrode 150 have been depressed into the first conductive type semiconductor region 170 and the metal crystals MC have been formed in both the finger forming region 170A1 and bus bar forming region 170A2 of the first conductive type semiconductor region 170 has been described. In order to further improve efficiency of the solar cell, only the first finger electrodes 151 may be depressed into the first conductive type semiconductor region 170 and the metal crystals MC may be placed only in the finger forming region 170A1, but may not be placed in the bus bar forming region 170A2. This is described in detail below with reference to FIGS. 9 to 11.

[00213] FIG. 9 is a diagram illustrating a solar cell according to a third embodiment of the present invention.

[00214] In a description related to FIG. 9, a description of portions redundant with the contents described in connection with the second embodiment is omitted, and portions

different from the contents of the second embodiment are chiefly described.

[00215] As shown in FIG. 9, in the solar cell according to the third embodiment of the present invention, at least part of the first electrode 150 may be depressed and formed in the first conductive type semiconductor region 170, but only the plurality of first finger electrodes 151 of the first electrode 150 may penetrate the first passivation film 190A and may be depressed and formed in the first conductive type semiconductor region 170.

[00216] In this instance, the metal crystals MC may be formed only in the finger forming region 170A1 of the first conductive type semiconductor region 170, and the plurality of first bus bars 153 may not be depressed into the first conductive type semiconductor region 170, but may be formed on the back surface of the first passivation film 190A.

[00217] Accordingly, the metal crystals MC may not be formed in the bus bar forming region 170A2 of the first conductive type semiconductor region 170.

[00218] As described above, only the plurality of first finger electrodes 151 of the first electrode 150 may penetrate the first passivation film 190A and may be depressed into the first conductive type semiconductor region 170 so that the metal crystals MC are formed only in the finger forming region 170A1 of the first conductive type semiconductor region 170, and the first bus bar 153 may be formed on the first passivation film 190A.

[00219] As described above with reference to FIGS. 6 to 8, if the metal crystals MC are not formed in the bus bar forming region 170A2 of the first conductive type semiconductor region 170 as described above, the metal crystals MC are not placed in the tunnel layer 160, and thus there can be prevented the phenomenon in which the semiconductor substrate 100 is deteriorated because the metal crystals MC penetrate the tunnel layer 160 and are connected to the semiconductor substrate 100.

[00220] More specifically, the width of the first bus bar 153 is relatively greater than the width of the first finger electrode 151 as described above with reference to FIGS. 1 and 5. Accordingly, in the thermal treatment process, the metal crystals MC having a relatively great length or width may penetrate the tunnel layer 160 and may be short-circuited with the semiconductor substrate 100, as shown in FIG. 8. Accordingly, the semiconductor substrate 100 may be deteriorated. If the metal crystals MC are not formed in the bus bar forming region 170A2 of the first conductive type semiconductor region 170, such a deterioration phenomenon can be prevented.

[00221] Accordingly, the solar cell according to the third embodiment of the present invention has a structure in which only the first finger electrodes 151 of the first finger electrodes 151 and first bus bar 153 of the first electrode 150 penetrate the first passivation film 190A and are depressed and formed in the first conductive type semiconductor region 170. Accordingly, only the first conductive type semiconductor region 170 and the first finger electrodes 151 come into contact with each other in the first boundary surface BS1 of the first conductive type semiconductor region 170, the plurality of metal crystals MC may be placed only in the finger forming region 170A1 which belongs to the electrode forming region 170A of the first conductive type semiconductor region 170 and in which the first finger electrode 151 is formed, and the plurality of metal crystals MC may not be placed in the bus bar forming region 170A2 of the first conductive type semiconductor region 170 which overlaps the first bus bar 153.

[00222] To this end, in an embodiment of the present invention, the plurality of first finger electrodes 151 and the plurality of first bus bars 153 may have different compositions.

[00223] More specifically, content of frit glass per unit volume, which is included in the plurality of first bus bars 153, may be smaller than content of frit glass per unit volume, which is included in the plurality of first finger electrodes 151, or content of frit glass may not be included in the plurality of first bus bars 153.

[00224] Accordingly, in the thermal treatment process for forming the first electrode 150, while the plurality of metal crystals MC is extracted into the finger forming region 170A1 when the first finger electrode 151 penetrates the first passivation film 190A and is depressed into the first conductive type semiconductor region 170, the first bus bar 153 can be prevented from penetrating the first passivation film 190A and from being depressed into the first conductive type semiconductor region 170 or such a depression can be minimized.

[00225] Moreover, although the first bus bar 153 penetrates the first passivation film 190A and is depressed into the first conductive type semiconductor region 170, the deterioration phenomenon in which the metal crystals MC extracted from the first bus bar 153 penetrate the tunnel layer 160 and are short-circuited with the semiconductor substrate 100 as shown in FIG. 8 can be prevented.

[00226] In this instance, the deterioration of the semiconductor substrate 100 may be

checked from FIGS. 10 and 11.

[00227] FIG. 10 is a comparison example photograph of the degree of the deterioration of the semiconductor substrate 100 according to firing temperatures in the thermal treatment process, which was taken through photo luminescence (PL), if the material of a paste for the first bus bar is the same as the material of a paste for the first finger electrode. FIG. 11 is photograph of the degree of the deterioration of the semiconductor substrate 100 according to firing temperatures in the thermal treatment process, which was taken through photo luminescence (PL), if the material of a paste 153P for the first bus bar is different from the material of a paste for the first finger electrodes in accordance with the third embodiment of the present invention.

[00228] From the PL images showing the open voltages Voc of the semiconductor substrate 100, the deterioration phenomenon occurring because the metal crystals MC penetrate the tunnel layer 160 and are short-circuited with the semiconductor substrate 100 depending on the temperature of the thermal treatment process can be checked.

[00229] As some region of the semiconductor substrate 100 becomes darker in the PL image, it means the open voltage is reduced and thus the deterioration of the semiconductor substrate 100 is increased. As some region of the semiconductor substrate 100 becomes brighter, it means that the open voltage is sufficiently high and thus the deterioration of the semiconductor substrate 100 is reduced or is not present.

[00230] More specifically, if a shade region is increased in the PL image as the temperature of the thermal treatment process rises, it means that the open voltage is reduced and the deterioration of the semiconductor substrate 100 is increased because the metal crystals MC penetrate the tunnel layer 160 and are short-circuited with the semiconductor substrate 100. If a shade region is not increased in the PL image as the temperature of the thermal treatment process rises, it means that the open voltage is sufficiently high and the deterioration of the semiconductor substrate 100 is small or is almost not present because the metal crystals MC do not penetrate the tunnel layer 160 or the semiconductor substrate 100.

[00231] In FIGS. 10 and 11, images of the paste 153P for the first bus bar having a relatively great width have been illustrated, but images of a paste for the first finger electrodes having a very small width are not illustrated. The paste for the first finger electrodes may intersect the paste 153P for the first bus bars and may be formed.

[00232] FIG. 10 shows an instance where the paste 153P for the first bus bars having

the same material as the paste for the first finger electrodes was used, and FIG. 11 shows an instance where the paste 153P for the first bus bars having a material different from the material of the paste for the first finger electrodes as described above with reference to FIG. 9 was used.

[00233] In FIG. 10, the paste 153P for the first bus bars and the paste for the first finger electrodes have the same material. Accordingly, the paste 153P for the first bus bars may also pcnctratc thc first passivation film 190A and may be depressed and formed in the first conductive type semiconductor region 170, so the metal crystals MC may be formed in the bus bar forming region 170A2 of the first conductive type semiconductor region 170.

[00234] Accordingly, if the temperature of the thermal treatment process for forming the first electrode 150 is relatively low, for example, about 820°C or 795°C as shown in (c) and (d) of FIG. 10, the semiconductor substrate 100 is not deteriorated because there is almost no metal crystal MC which is extracted from the paste for the first electrode and subsides into the first conductive type semiconductor region 170. In this instance, efficiency of the solar cell may be reduced because contact resistance of the first finger electrodes 151 may be relatively high.

[00235] If the temperature of the thermal treatment process for forming the first electrode 150 is relatively high, for example, about 870°C or 845°C as shown in (a) and (b) of FIG. 10, the shade region is increased in the semiconductor substrate 100 and the deterioration of the semiconductor substrate 100 is relatively increased.

[00236] The reason for this is that the deterioration of the semiconductor substrate 100 is increased because the metal crystals MC extracted from the paste 153P for the first bus bars are placed in the first conductive type semiconductor region 170 and such metal crystals MC penetrate the tunnel layer 160 and are connected to the semiconductor substrate 100.

[00237] As described above with reference to FIG. 9, if the first finger electrodes 151 and the first bus bar 153 are made of different materials in accordance with the third embodiment of the present invention, it may be seen that the shade region of the semiconductor substrate 100 is rarely increased even in (a) and (b) of FIG. 11 in which the temperature of the thermal treatment process is relatively high as well as in (c) and (d) of FIG. 11 in which the temperature of the thermal treatment process is relatively low.

[00238] The reason for this is that the semiconductor substrate 100 is not deteriorated

because the paste 153P for the first bus bars does not penetrate the first passivation film 190A or although the paste 153P for the first bus bars penetrates the first passivation film 190A and connects to the first conductive type semiconductor region 170 and thus the metal crystals MC are formed in the first conductive type semiconductor region 170, the metal crystals MC are not placed in the tunnel layer 160 if the paste 153P for the first bus bars and the paste for the first finger electrodes are made of different materials.

[00239] As described above, the solar cell according to the third embodiment of the present invention can prevent the deterioration of the semiconductor substrate 100 and have further improved efficiency because the solar cell maintains a sufficient high open voltage Voc by forming the first finger electrodes 151 and the first bus bar 153 using different materials.

[00240] The structures of the solar cells according to embodiments of the present invention have been described so far. Hereinafter, methods for manufacturing solar cells are described.

[00241] FIG. 12 is a flowchart illustrating an example of a method for manufacturing a solar cell according to a first embodiment of the present invention. FIGS. 13A to 13J are cross-sectional views of the method for manufacturing a solar cell according to the flowchart of FIG. 12.

[00242] Furthermore, FIG. 14 is a diagram illustrating a modified example of the method for manufacturing a solar cell according to the first embodiment. FIG. 15 is a diagram illustrating another modified example of the method for manufacturing a solar cell according to the first embodiment.

[00243] As shown in FIG. 12, an example of the method for manufacturing a solar cell according to the first embodiment of the present invention may include a tunnel layer forming step (operation) S1, an intrinsic semiconductor layer forming step (operation) S2, a first conductive type semiconductor region forming step (operation) S3, a removing step (operation) S4, a second conductive type semiconductor region forming step (operation) S5, an anti-reflection layer and second passivation film forming step (operation) S6, a first passivation film forming step (operation) S7, and an electrode forming step (operation) S8.

[00244] In this example, the removing step S4 and the anti-reflection layer and second passivation film forming step S6 have been illustrated as being included. In some embodiments, the removing step S4 and the anti-reflection layer and second passivation

film forming step S6 may be omitted.

[00245] An example in which the removing step S4 and the anti-reflection layer and second passivation film forming step S6 are included, for convenience of description, is described below.

[00246] As a preliminary step (operation) for manufacturing a solar cell according to the first embodiment of the present invention, the concave-convex portions may be formed by performing a texturing process on the front and back surfaces of the semiconductor substrate 100, as shown in FIG. 13A.

[00247] Wet or dry texturing may be used as the texturing technique for the semiconductor substrate 100.

[00248] The wet texturing may be performed by dipping the semiconductor substrate 100 into a texturing solution and is advantageous in that the process time is short. The dry texturing may be performed by cutting a surface of the semiconductor substrate 100 using a diamond grill or a laser. In the dry texturing, the concave-convex portions may be uniformly formed, but the process time is long and the semiconductor substrate 100 may be damaged.

[00249] In addition, the semiconductor substrate 100 may be textured using reactive ion etch (RIE). As described above, in an embodiment of the present invention, the semiconductor substrate 100 may be textured using various methods.

[00250] For a simple illustration, concave-convex portions have been illustrated as being not formed on the side of the semiconductor substrate 100 by the texturing. Furthermore, it may be difficult to clearly recognize the concave-convex portions by the texturing because the semiconductor substrate 100 has a very small thickness.

[00251] However, the present invention is not limited to the above description. For example, the concave-convex portions according to the texturing may be provided on the side of the semiconductor substrate 100. Furthermore, the texturing of the semiconductor substrate 100 may be performed in a subsequent process.

[00252] As shown in FIG. 12, the tunnel layer forming step S1 for forming the tunnel layer 160 on one surface of the semiconductor substrate 100 may be performed in the state in which the concave-convex portions have been provided in the semiconductor substrate 100 as described above.

[00253] In the tunnel layer forming step S1, for example, as shown in FIG. 13B, the tunnel layer 160 may be generally formed on one surface and the other surface of the

semiconductor substrate 100. In this instance, the tunnel layer 160 may also be generally formed on the side of the semiconductor substrate 100.

[00254] If the tunnel layer 160 is generally formed on the surfaces of the semiconductor substrate 100 as described above, the tunnel layer 160 formed on the other surface (i.e., the front surface) and side of the semiconductor substrate 100 may be removed in the removing step S4.

[00255] If the tunnel layer 160 is formed on only one surface of the semiconductor substrate 100, the removing step S4 may be omitted.

[00256] In this instance, the tunnel layer 160 may be formed by thermal oxidation, chemical oxidation, or deposition (e.g., an atmospheric pressure chemical vapor deposition (APCVD) method or a low-pressure chemical vapor deposition (LPCVD) method), for example. Additionally, after the tunnel layer 160 having a thin thickness is formed, the thickness or density of the tunnel layer 160 may be increased by subsequent thermal treatment within a furnace.

[00257] However, the present invention is not limited to such methods. The tunnel layer 160 may be formed by various other methods. In this instance, the tunnel layer 160 may be formed of a silicon oxide layer.

[00258] For example, in the present embodiment, the tunnel layer 160 may be formed in a gas atmosphere, including a source gas, at a temperature higher than normal temperature and pressure smaller than atmospheric pressure. In the present embodiment, the source gas includes an oxygen gas, and thus the tunnel layer 160 may be formed of an oxide layer.

[00259] More specifically, at a high temperature, the tunnel layer 160 may be formed of a thermal oxide (e.g., thermal silicon oxide) layer formed by a reaction of oxygen and the semiconductor material (e.g., silicon) of the semiconductor substrate 100.

[00260] In the present embodiment, the source gas does not include all source materials forming the tunnel layer 160, but may include only an oxygen gas of the oxide forming the tunnel layer 160 and may not include other source materials.

[00261] For example, if the tunnel layer 160 includes silicon oxide, it includes only an oxygen gas as the source gas, but does not include a gas including silicon, that is, other source material. Accordingly, the tunnel layer 160 may be formed by a thermal oxidation process in which oxygen included in the oxygen gas is diffused into the semiconductor substrate 100 and reacts with the semiconductor material.

[00262] In some embodiments, in a deposition process, a silane (SiH_4) gas including silicon, together with an oxygen gas including oxygen, may be supplied as the source gas. In this instance, oxygen separated from the oxygen gas may chemically react with silicon separated from the silane gas by thermal decomposition, thereby being capable of forming silicon oxide. When the tunnel layer 160 is formed, a gas atmosphere may include various gases in addition to the oxygen gas, that is, the source gas.

[00263] Furthermore, pressure when the tunnel layer 160 is formed may be lower than atmospheric pressure. In this instance, although the tunnel layer 160 is formed by a thermal oxidation process using a relatively high temperature (e.g., 600°C or more), the tunnel layer 160 can maintain low growth speed due to the low pressure. Accordingly, the thickness of the tunnel layer 160 can be significantly reduced.

[00264] For example, when the tunnel layer 160 is formed, a temperature may be set to 600°C to 800°C and pressure may be set to 600 Torr or less in order to effectively control the thickness of the tunnel layer 160.

[00265] As described above, in the present embodiment, when the tunnel layer 160 is formed, both the temperature and pressure need to be controlled. Accordingly, the tunnel layer 160 according to the present embodiment may not be formed in a conventional furnace whose pressure cannot be controlled, and the tunnel layer 160 has to be formed in an apparatus whose temperature and pressure can be controlled.

[00266] Accordingly, in the present embodiment, the tunnel layer 160 may be formed by a thermal oxidation process within deposition apparatus. In this instance, since low pressure needs to be implemented, the tunnel layer 160 may be formed in a low-pressure chemical vapor deposition apparatus.

[00267] An intrinsic semiconductor layer 170' formed on the tunnel layer 160 is formed by a deposition apparatus. Accordingly, if the tunnel layer 160 is formed in the deposition apparatus, the tunnel layer 160 and the intrinsic semiconductor layer 170' can be formed by an in-situ process for consecutively forming the tunnel layer 160 and the intrinsic semiconductor layer 170' in the same deposition apparatus (more specifically, a low-pressure chemical vapor deposition apparatus).

[00268] If the tunnel layer 160 and the intrinsic semiconductor layer 170' are formed by an in-situ process as described above, a manufacturing cost and a manufacturing time can be significantly reduced because the manufacturing process is significantly simplified.

[00269] A temperature within the deposition apparatus is controlled by applying heat (e.g., heating) or removing heat (e.g., cooling) for a long time, and a lot of time is taken to stabilize the temperature. In contrast, a gas atmosphere and pressure may be controlled by the type and amount of gas supplied to the deposition apparatus. Accordingly, a gas atmosphere and pressure can be more easily controlled than a temperature.

[00270] In the present embodiment, a difference between a temperature at which the tunnel layer 160 is formed and a temperature in the process of depositing the intrinsic semiconductor layer 170' may be set to 200°C or less (i.e., 0°C to 200°C). More specifically, a difference between a temperature at which the tunnel layer 160 is formed and a temperature in the process of depositing the intrinsic semiconductor layer 170' may be set to 100°C or less (i.e., 0°C to 100°C).

[00271] The reason for this is that a difference between a temperature at which the tunnel layer 160 is formed and a temperature in the process of depositing the intrinsic semiconductor layer 170' can be reduced because the tunnel layer 160 is formed at low pressure and thus the temperature at which the tunnel layer 160 is formed can be relatively raised. Accordingly, efficiency of the in-situ process of consecutively forming the tunnel layer 160 and the intrinsic semiconductor layer 170' can be further improved because a temperature that is relatively difficult to control can be maintained without a great change or variance as described above.

[00272] In contrast, a gas atmosphere in the process of depositing the intrinsic semiconductor layer 170' may be different from a gas atmosphere when the tunnel layer 160 is formed, and pressure in the process of depositing the intrinsic semiconductor layer 170' may be the same as or different from pressure when the tunnel layer 160 is formed. This is described in more detail later in a subsequent description of the deposition process of the intrinsic semiconductor layer 170'.

[00273] After the tunnel layer forming step S1 is completed as described above, the intrinsic semiconductor layer forming step S2 for forming the intrinsic semiconductor layer 170' on the tunnel layer 160 formed on one surface of the semiconductor substrate 100 may be performed as shown in FIG. 12.

[00274] For example, as shown in FIG. 13C, in the intrinsic semiconductor layer forming step S2, the intrinsic semiconductor layer 170' may be generally formed on the tunnel layer 160 formed on one surface and the other surface of the semiconductor

substrate 100. In this instance, the intrinsic semiconductor layer 170' may also be generally formed on the tunnel layer 160 placed on the side of the semiconductor substrate 100.

[00275] If the intrinsic semiconductor layer 170' is placed on both sides of the semiconductor substrate 100 as described above, the doping and damage of the front surface of the semiconductor substrate 100 can be effectively prevented in the process of doping the intrinsic semiconductor layer 170' in order to form the first conductive type semiconductor region 170.

[00276] In the present embodiment, the intrinsic semiconductor layer 170' may be formed by chemical vapor deposition. More specifically, the intrinsic semiconductor layer 170' may be formed by low-pressure chemical vapor deposition.

[00277] Accordingly, the intrinsic semiconductor layer 170' may be formed by the tunnel layer 160 and the in-situ process as described above, but the present invention is not limited thereto. The in-situ process may not be applied to the tunnel layer 160 and the intrinsic semiconductor layer 170'.

[00278] A gas used in the process of depositing the intrinsic semiconductor layer 170' may include a gas (e.g., a silane gas) including a semiconductor material which forms the intrinsic semiconductor layer 170'. In the present embodiment, since the intrinsic semiconductor layer 170' is deposited so that the gas atmosphere has the intrinsic property, the gas atmosphere may include only the gas including the semiconductor material.

[00279] Accordingly, a supply gas can be simplified, and the purity of the formed intrinsic semiconductor layer 170' can be improved, but the present invention is not limited thereto. A separate gas for accelerating the deposition process of the intrinsic semiconductor layer 170' or improving the characteristics of the intrinsic semiconductor layer 170' may be further used.

[00280] Furthermore, in the deposition process of the intrinsic semiconductor layer 170', the size of a crystal grain and crystallizability may be controlled by injecting the gas, including the semiconductor material, along with a nitrogen oxide (N_2O) gas and/or an oxygen (O_2) gas.

[00281] The deposition temperature of the intrinsic semiconductor layer 170' may be the same as or lower than a temperature when the tunnel layer 160 is formed. In particular, if the deposition temperature of the intrinsic semiconductor layer 170' is

lower than a temperature when the tunnel layer 160 is formed, a characteristic of the intrinsic semiconductor layer 170' which directly takes part in photoelectric conversion can become uniform.

[00282] In some embodiments, the deposition temperature of the intrinsic semiconductor layer 170' may be 500°C to 700°C. Such a deposition temperature is suitable for depositing the intrinsic semiconductor layer 170' having a crystal structure different from that of the semiconductor substrate 100.

[00283] The temperature of the tunnel layer 160 is set to be the same as or similar to the deposition temperature of the intrinsic semiconductor layer 170' as described above. Accordingly, the process can be simplified because the time taken to control a temperature and the time taken to stabilize a temperature are not required.

[00284] Furthermore, deposition pressure of the intrinsic semiconductor layer 170' may be lower than atmospheric pressure, for example, 600 Torr or less (e.g., 1 Torr to 600 Torr). To maintain the deposition pressure less than 1 Torr may be limited on the nature of the process, and the deposition pressure of less than 1 Torr may be difficult to apply to actual mass production because the process time of the intrinsic semiconductor layer 170' is greatly increased.

[00285] If the deposition pressure exceeds 600 Torr, the uniformity of the intrinsic semiconductor layer 170' may be deteriorated. In some embodiments, the deposition pressure of the intrinsic semiconductor layer 170' may be the same as or smaller than pressure when the tunnel layer 160 is formed.

[00286] In particular, if the deposition pressure of the intrinsic semiconductor layer 170' is smaller than pressure when the tunnel layer 160 is formed, a characteristic of the intrinsic semiconductor layer 170' which directly takes part in photoelectric conversion can become uniform.

[00287] This is described in more detail. A gas including a semiconductor material (e.g., silicon) is thermally decomposed and the semiconductor material is deposited on the tunnel layer 160, thereby being capable of forming the intrinsic semiconductor layer 170'.

[00288] If a temperature and/or pressure of the intrinsic semiconductor layer 170' are increased in order to increase deposition speed, the distribution of crystallizability within the intrinsic semiconductor layer 170' is increased. If the distribution of crystallizability within the intrinsic semiconductor layer 170' is increased, the

characteristics of the intrinsic semiconductor layer 170' may not become uniform because the crystallizability of the intrinsic semiconductor layer 170' takes part in moving speed of carriers.

[00289] In contrast, the tunnel layer 160 is formed in a very thin thickness, and the crystallizability of the tunnel layer 160 does not have an influence on the characteristics of the tunnel layer 160. Although the intrinsic semiconductor layer 170' needs to be formed in a thicker thickness than the tunnel layer 160, the deposition temperature and/or pressure of the intrinsic semiconductor layer 170' are set to be smaller than those when the tunnel layer 160 is formed in order to improve the characteristics of the intrinsic semiconductor layer 170'.

[00290] However, the present invention is not limited to such an example. A gas atmosphere, temperature, and pressure of the intrinsic semiconductor layer 170' may be changed in various ways.

[00291] As described above, the intrinsic semiconductor layer 170' may be formed by changing the type of gas supplied after the tunnel layer 160 is formed and controlling the amount of a supplied gas.

[00292] For example, the intrinsic semiconductor layer 170' may be formed by removing a gas (e.g., an oxygen gas, a nitrogen gas, or a chlorine gas), used when the tunnel layer 160 is formed after the tunnel layer 160 is formed, by pumping and purging, and then injecting a gas (e.g., a gas including a semiconductor material) for forming the intrinsic semiconductor layer 170'.

[00293] Accordingly, the process of forming the tunnel layer 160 and the intrinsic semiconductor layer 170' can be simplified. Furthermore, if the semiconductor substrate 100 on which the tunnel layer 160 has been formed is taken out from an apparatus after the tunnel layer 160 is formed as in a prior art, there is a problem in that the tunnel layer 160 is contaminated by impurities or the thickness of the tunnel layer 160 is increased due to an additional oxidation.

[00294] In the present embodiment, the tunnel layer 160 is not externally exposed until the intrinsic semiconductor layer 170' is formed because the intrinsic semiconductor layer 170' is consecutively formed in an apparatus in which the tunnel layer 160 has been formed. Accordingly, a problem occurring because the tunnel layer 160 is externally exposed before the intrinsic semiconductor layer 170' is formed can be prevented.

[00295] For reference, if plasma-enhanced chemical vapor deposition (PECVD) is used, a separate crystallization annealing process needs to be performed so that the intrinsic semiconductor layer 170' has a polycrystalline structure after it is formed. Accordingly, the structure becomes complicated, and performance may be deteriorated. Furthermore, since PECVD is a one-sided process, it may be difficult to generally form the intrinsic semiconductor layer 170' on both sides of the semiconductor substrate 100.

[00296] Thereafter, as shown in FIG. 12, the first conductive type semiconductor region forming step S3 may be performed.

[00297] In the first conductive type semiconductor region forming step S3, the first conductive type semiconductor region 170 may be formed by doping impurities of the first conductive type into the intrinsic semiconductor layer 170' formed on one surface of the semiconductor substrate 100.

[00298] More specifically, in the first conductive type semiconductor region forming step S3, as shown in FIG. 13D, a first conductive type semiconductor region 170'a may be formed on the entire surface of the semiconductor substrate 100 by doping impurities of the first conductive type into the intrinsic semiconductor layer 170' formed on the entire surface of the semiconductor substrate 100.

[00299] In this instance, in the present embodiment, the impurities of the first conductive type may be doped using a thermal diffusion method. The reason for this is that the thermal diffusion method is capable of doping while minimizing the deterioration of the characteristics of the tunnel layer 160. In contrast, if an ion implantation method is used, the characteristics of the tunnel layer 160 may be deteriorated due to activation thermal treatment performed at high temperature after ion implantation.

[00300] For example, as shown in FIG. 13D, the first conductive type semiconductor region 170'a may be generally formed by thermal treatment in a gas atmosphere including the impurities of the first conductive type.

[00301] If the first conductive type semiconductor region 170'a has an n type, thermal treatment may be performed in a gas atmosphere including $POCl_3$. If the first conductive type semiconductor region 170'a has a p type, thermal treatment may be performed in a gas atmosphere including BBr_3.

[00302] The process of forming the first conductive type semiconductor region 170'a can be simplified using a gas including the impurities of the first conductive type as

described above. In this instance, doping may be performed on the front surface and side of the semiconductor substrate 100 in addition to the back surface of the semiconductor substrate 100 due to such a process.

[00303] In the present embodiment, since portions of the intrinsic semiconductor layer 170' to be removed in a subsequent process are present on the front surface and side of the semiconductor substrate 100, a problem in that the front surface and side of the semiconductor substrate 100 are unnecessarily doped with the impurities of the first conductive type can be fundamentally prevented.

[00304] In an alternative embodiment, that is, a modified example, as shown in FIG. 14, the first conductive type semiconductor region 170'a may be formed by forming a first doping layer 210, including impurities of the first conductive type, on the intrinsic semiconductor layer 170' placed at least on the back surface side of the semiconductor substrate 100 and diffusing the impurities of the first conductive type included in the first doping layer 210 through thermal treatment.

[00305] For example, the first doping layer 210 may include phosphorous silicate glass (PSG) or boron silicate glass (BSG). The first doping layer 210 may be easily formed by deposition.

[00306] For example, the first doping layer 210 may be formed by atmospheric pressure chemical vapor deposition and may be formed on the back surface and/or side of the semiconductor substrate 100, but may not be formed on the front surface of the semiconductor substrate 100. Accordingly, the first conductive type semiconductor region 170'a may be formed on only the back surface and/or side of the semiconductor substrate 100, and the intrinsic semiconductor layer 170' may remain intact on the front surface of the semiconductor substrate 100.

[00307] Next, as shown in FIG. 13E, a mask layer 202 may be formed on the first conductive type semiconductor region 170'a placed on the back surface side of the semiconductor substrate 100 so that the mask layer 202 corresponds to the first conductive type semiconductor region (170 in FIG. 13F) to be left other than the isolation portion (I in FIG. 13F, hereinafter the same).

[00308] More specifically, the area of the mask layer 202 may be smaller than that of the semiconductor substrate 100. Accordingly, the first conductive type semiconductor region (170 in FIG. 13F) that remains other than the isolation portion I may have a smaller area than the semiconductor substrate 100 by removing an unwanted portion of

the first conductive type semiconductor region 170'a.

[00309] For example, the mask layer 202 may be spaced apart from each side (or the edge) of the semiconductor substrate 100 at a specific second distance D2. If the area of the mask layer 202 is the same as or greater than the area of the semiconductor substrate 100, it may be difficult to effectively remove the unwanted portion of the first conductive type semiconductor region 170'a which is adjacent to the side of the semiconductor substrate 100 on the back surface side of the semiconductor substrate 100.

[00310] The second distance D2 may be controlled so that the first distance D1 between the first conductive type semiconductor region 170'a and the edge of the back surface of the semiconductor substrate 100 has a required value. For example, the second distance D2 may have a value of 1 mm or less (e.g., 1 nm to 1 mm) so that the first distance D1 has a value of 1 mm or less (e.g., 1 nm to 1 mm), but the present invention is not limited thereto. The second distance D2 may have values other than 1 mm or less.

[00311] The mask layer 202 may include a material which is not removed in the process of removing part (i.e., the edge D2 of the other surface, side, or one surface of the semiconductor substrate 100) of the first conductive type semiconductor region 170'a including the semiconductor material.

[00312] For example, the mask layer 202 not etched by an etch solution which is used in the process of removing part of the first conductive type semiconductor region 170'a may include oxide, nitride, or resin. For example, the mask layer 202 may be formed of a silicon nitride layer so that the mask layer 202 is formed by a simple process.

[00313] As shown in FIG. 12, the removing step S4 may be performed prior to the second conductive type semiconductor region forming step S5 after the first conductive type semiconductor region forming step S3.

[00314] In the removing step S4, for example, the tunnel layer 160 and the intrinsic semiconductor layer 170' or the first conductive type semiconductor region 170'a placed on the other surface of the semiconductor substrate 100 in FIG. 13E may be removed.

[00315] Furthermore, in the removing step S4, portions of the first conductive type semiconductor region 170'a and the tunnel layer 160 not covered by the mask layer 202 in FIG. 13E may be removed, so the isolation portion I may be formed.

[00316] The tunnel layer 160 and the first conductive type semiconductor region 170'a are moved as described above, so the tunnel layer 160 and the first conductive type semiconductor region 170, such as those shown in FIG. 13F, may be formed.

[00317] In the removing step S4, wet etch using an alkali solution (e.g., a KOH solution), for example, may be performed on the first conductive type semiconductor region 170'a and the tunnel layer 160.

[00318] In accordance with such wet etch, the first conductive type semiconductor region 170'a and the tunnel layer 160 placed in the isolation portion I on the front surface, side, or back surface of the semiconductor substrate 100 can be removed by a simple and easy process.

[00319] The first conductive type semiconductor region 170'a may be removed selectively and easily using the alkali solution. The tunnel layer 160 having a very small thickness, albeit being an oxide, may also be removed when the first conductive type semiconductor region 170'a is removed.

[00320] Accordingly, as shown in FIG. 13F, the first conductive type semiconductor region 170 and the tunnel layer 160 each formed to have a smaller area than the semiconductor substrate 100 and spaced apart from the edge of the back surface of the semiconductor substrate 100 at the first distance D1 may be formed.

[00321] The first conductive type semiconductor region 170 and the tunnel layer 160 may have a shape having an area reduced as they become distant from the semiconductor substrate 100 and the sides thereof may be formed to be rounded by the wet etch.

[00322] However, the present invention is not limited to the above description. Part of the first conductive type semiconductor region 170 and the tunnel layer 160 may be removed by various methods, such as RIE and dry etch, and the first conductive type semiconductor region 170 and the tunnel layer 160 may have a different shape.

[00323] The mask layer 202 may be removed after part of the first conductive type semiconductor region 170 and the tunnel layer 160 is removed so that the isolation portion I is formed. The mask layer 202 may be removed by various methods depending on a material.

[00324] For example, if the mask layer 202 includes an oxide or a nitride, it may be removed by a process using diluted hydrofluoric acid. The mask layer 202 may be removed by a separate process or may be naturally removed by a cleaning process

including a solution including diluted hydrofluoric acid.

[00325] After the removing step S4 is performed as described above, as shown in FIG. 12, the second conductive type semiconductor region forming step S5 for forming the second conductive type semiconductor region 120 by doping impurities of the second conductive type on the other surface of the semiconductor substrate 100 may be performed.

[00326] More specifically, as shown in FIG. 13G, in the second conductive type semiconductor region forming step S5, the second conductive type semiconductor region 120 may be formed by doping impurities of the second conductive type on the front surface side of the semiconductor substrate 100.

[00327] The second conductive type semiconductor region 120 may be formed by known various methods. For example, the second conductive type semiconductor region 120 may be formed by a thermal diffusion method. The reason for this is that the thermal diffusion method is capable of doping while minimizing the deterioration of the characteristics of the tunnel layer 160. In contrast, if an ion implantation method is used, the characteristics of the tunnel layer 160 may be deteriorated due to activation thermal treatment performed at high temperature after ion implantation.

[00328] If the thermal diffusion method is used, in the second conductive type semiconductor region forming step S5, as shown in FIG. 13G, the second conductive type semiconductor region 120 may be formed on the front surface of the semiconductor substrate 100 by forming a capping film 204 on the side and back surface of the semiconductor substrate 100 and performing thermal treatment in a gas atmosphere including impurities of the second conductive type.

[00329] If the second conductive type semiconductor region 120 has a p type, the thermal treatment may be performed in a gas atmosphere including BBr_3. If the second conductive type semiconductor region 120 has an n type, the thermal treatment may be performed in a gas atmosphere including $POCl_3$. After the second conductive type semiconductor region 120 is formed through such thermal treatment, the capping film 204 may be removed. Various films capable of preventing the doping of the impurities of the second conductive type may be used as the capping film 204. The capping film 204 may be removed by a removing method depending on a material.

[00330] In the second conductive type semiconductor region forming step S5, for another example, as shown in FIG. 15, the second conductive type semiconductor region

120 may be formed by forming a second doping layer 310, including impurities of the second conductive type, on the front surface of the semiconductor substrate 100 and diffusing the impurities of the second conductive type, included in the second doping layer 310, into the semiconductor substrate 100 through thermal treatment.

[00331] The second doping layer 310 may include boron silicate glass (BSG) or phosphorous silicate glass (PSG). The second doping layer 310 may be easily formed by deposition. In this instance, the second doping layer 310 may be formed by atmospheric pressure chemical vapor deposition and may not be formed on the back surface of the semiconductor substrate 100.

[00332] Thereafter, as shown in FIG. 12, the anti-reflection layer and second passivation film forming step S6 may be performed.

[00333] In the anti-reflection layer and second passivation film forming step S6, the second passivation film 190B and the anti-reflection layer 130 may be sequentially formed on the second conductive type semiconductor region 120.

[00334] In the anti-reflection layer and second passivation film forming step S6, for example, as shown in FIG. 13H, the second passivation film 190B and the anti-reflection layer 130 may be sequentially formed on the side of the semiconductor substrate 100 in addition to the front surface of the second conductive type semiconductor region 120.

[00335] The second passivation film 190B or the anti-reflection layer 130 may be formed by various methods, such as a vacuum deposition method, a chemical vapor deposition method, spin coating, screen printing, or spray coating.

[00336] If one-sided deposition, such as plasma-enhanced chemical vapor deposition (PECVD), is used when the second passivation film 190B or the anti-reflection layer 130 is formed, the second passivation film 190B or the anti-reflection layer 130 may be formed on only the front surface and/or side of the semiconductor substrate 100. Accordingly, a separate patterning process for the second passivation film 190B or the anti-reflection layer 130 is not required.

[00337] Thereafter, as shown in FIG. 12, the first passivation film forming step S7 for forming the first passivation film 190A on the first conductive type semiconductor region 170 may be performed.

[00338] For example, as shown in FIG. 13I, the first passivation film 190A may be formed on the first conductive type semiconductor region 170 placed on the back

surface side of the semiconductor substrate 100, the isolation portion I placed in the edge of the back surface of the semiconductor substrate 100, and the second passivation film 190B and the anti-reflection layer 130 placed on the side of the semiconductor substrate 100.

[00339] Accordingly, after edge isolation according to the isolation portion I is performed, the isolation portion I may also be passivated while the first passivation film 190A is formed without a separate process.

[00340] The first passivation film 190A may be formed by various methods, such as a vacuum deposition method, a chemical vapor deposition method, spin coating, screen printing, or spray coating.

[00341] If one-sided deposition, such as plasma-enhanced chemical vapor deposition (PECVD), is used when the first passivation film 190A or the anti-reflection layer 130 is formed, the first passivation film 190A may be formed on only the back surface and/or side of the semiconductor substrate 100. Accordingly, a separate patterning process for the first passivation film 190A is not required.

[00342] In the present embodiment, an example in which the second passivation film 190B covering the front surface side of the semiconductor substrate 100 is first formed and the first passivation film 190A covering the back surface side of the semiconductor substrate 100 is then formed has been described.

[00343] In this instance, the characteristics of the first conductive type semiconductor region 170 can be prevented from being deteriorated or damaged in the process of forming the first passivation film 190A. The reason for this is that the characteristics of the first conductive type semiconductor region 170 may be very important, in particular, if the first conductive type semiconductor region 170 is an emitter region.

[00344] However, the present invention is not limited to the example. For example, after the first passivation film 190A covering the back surface side of the semiconductor substrate 100 is formed, the second passivation film 190B covering the front surface side of the semiconductor substrate 100 may be formed.

[00345] In this instance, the first passivation film 190A covering the back surface side of the semiconductor substrate 100 may be placed on (e.g., brought into contact with) the side of the semiconductor substrate 100, and the second passivation film 190B covering the front surface side of the semiconductor substrate 100 may be placed on (e.g., brought into contact with) on the first passivation film 190A.

[00346] After the first passivation film 190A is formed as described above, as shown in FIGS. 12 and 13J, the electrode forming step S8 for forming the first electrode 150 connected to the first conductive type semiconductor region 170 and the second electrode 140 connected to the second conductive type semiconductor region 120 may be performed.

[00347] The electrode forming step S8 may include the step (operation) of forming the opening portion 102 in the first passivation film 190A. Accordingly, in the electrode forming step S8, the first and the second opening portions 102 and 104 may be formed in the first and the second passivation films 190A and 190B by a patterning process, for example. Next, the first and the second electrodes 150 and 140 may be formed while the first and the second opening portions 102 and 104 are filled with metal for forming the first and the second electrodes 150 and 140.

[00348] In this instance, the first and the second opening portions 102 and 104 may be formed by laser ablation using a laser or various methods using an etch solution, an etch paste, and a photo process. Furthermore, the first and the second electrodes 150 and 140 may be formed by various methods, such as a plating method or a deposition method.

[00349] Accordingly, the isolation portion I can be formed by a simple process, and a problem attributable to surface recombination can be prevented by passivating the isolation portion I using the first passivation film 190A. Accordingly, productivity can be improved because a defective ratio of solar cells is reduced through a simple process.

[00350] In some embodiments, in the electrode forming step S8, the first and the second electrodes 150 and 140 may be formed by coating pastes for forming the first and the second electrodes 150 and 140 on the first and the second passivation films 190A and 190B using screen printing and then using a thermal treatment method, such as fire through or laser firing contact (or laser firing contact).

[00351] If the first electrode and the second electrode are formed using a printing method and a thermal treatment method as described above, the first and the second opening portions 102 and 104 are naturally formed when the first and the second electrodes 150 and 140 are formed. Accordingly, the manufacturing process can be further simplified because a separate process for forming the first and the second opening portions 102 and 104 is not required.

[00352] An example in which the first electrode and the second electrode are formed

using a printing method and a thermal treatment method as described above is described in more detail below.

[00353] FIG. 16 is a flowchart illustrating an example of a method for manufacturing a solar cell according to a second embodiment of the present invention. FIG. 17 is a flowchart illustrating an example of a method for manufacturing a solar cell according to a third embodiment of the present invention.

[00354] The remaining steps (operations) of FIGS. 16 and 17 other than a first electrode forming step are the same as those of FIGS. 12 and 13A to 15, and thus different portions are chiefly described.

[00355] Accordingly, as in the manufacturing method of the first embodiment, each of the methods for manufacturing a solar cell according to the second embodiment and third embodiment of the present invention may include the tunnel layer forming step S1, the intrinsic semiconductor layer forming step S2, the first conductive type semiconductor region forming step S3, the removing step S4, the second conductive type semiconductor region forming step S5, the anti-reflection layer and second passivation film forming step S6, the first passivation film forming step S7, and the electrode forming step S8.

[00356] The remaining steps (operations) other than the electrode forming step S8 may be the same as those of the first embodiment, and thus a description thereof is omitted.

[00357] In the second embodiment or the third embodiment, the electrode forming step S8 may include the step of forming the first electrode and the step of forming the second electrode. In this instance, the step of forming the second electrode may be the same as that of the method for manufacturing a solar cell according to the first embodiment of the present invention, or the first electrode forming step S8 according to the second embodiment or the third embodiment may be applied to the step of forming the second electrode without a change. Accordingly, in an embodiment of the present invention, a detailed description of the method for forming the second electrode is omitted because it is not specially limited.

[00358] The step of forming the first electrode in the second embodiment or the third embodiment is described in detail because it is different from that in the first embodiment.

[00359] In the method for manufacturing a solar cell according to the second

embodiment or the third embodiment, the first electrode forming step S8 may include a process for printing a paste for the first finger electrodes for forming the first finger electrodes and a paste for the first bus bar for forming the first bus bar on the first passivation film 190A and a thermal treatment process.

[00360] In the thermal treatment process, the paste for the first finger electrodes and the paste for the first bus bar may perforate the first passivation film and may be connected to the first conductive type semiconductor region. Accordingly, the step of forming the opening portion in the first passivation film may be performed during the thermal treatment process of the electrode forming step.

[00361] More specifically, in the method for manufacturing a solar cell according to the second embodiment of the present invention, a first electrode forming step S8A may include a process S8A1 for printing the paste for the first finger electrodes and the paste for the first bus bar on the first passivation film 190A through a single printing process and a thermal treatment process S8A2.

[00362] In this instance, a material included in the paste for the first finger electrodes for forming the first finger electrodes 151 and a material included in the paste for the first bus bar for forming the first bus bar 153 may be the same.

[00363] Thereafter, the paste for the first finger electrodes and the paste for the first bus bar perforate the first passivation film 190A and are connected to the first conductive type semiconductor region 170 through the thermal treatment process. Accordingly, the paste for the first finger electrodes and the paste for the first bus bar may be partially depressed into the first conductive type semiconductor region 170 and then fired, thereby forming the first finger electrodes 151 and the first bus bar 153, such as those shown in FIG. 5.

[00364] Furthermore, during the thermal treatment process, metal may be extracted from the paste for the first finger electrodes and the paste for the first bus bar and recrystallized. Accordingly, the metal crystals MC may be formed in the electrode forming region 170A of the first conductive type semiconductor region 170.

[00365] In this instance, the highest temperature of the thermal treatment process may be between 700°C to 900°C, more specifically, between 795°C to 870°C.

[00366] If the highest temperature of the thermal treatment process is 795°C or more, the paste for the first finger electrodes and the paste for the first bus bar can perforate the first passivation film 190A and can be connected to the first conductive type

semiconductor region 170.

[00367] If the highest temperature of the thermal treatment process is 870°C or less, the metal crystals MC recrystallized when metal is extracted from the paste for the first finger electrodes and the paste for the first bus bar can be prevented from penetrating the tunnel layer 160.

[00368] Furthermore, in the method for forming a solar cell according to the third embodiment of the present invention, a first electrode forming step S8B may include a process S8B1 for printing the paste for the first finger electrodes on the first passivation film 190A in order to form the first finger electrodes 151, a process S8B2 for printing the paste for the first bus bar having a material different from the material of the paste for the first finger electrodes on the first passivation film 190A in order to form the first bus bar 153, and a thermal treatment process S8B3, as shown in FIG. 17.

[00369] In FIG. 17, the process S8B1 for printing the paste for the first finger electrodes has been illustrated as being first performed and the process S8B2 for printing the paste for the first bus bar has been illustrated as being then performed, but sequence of the two processes may be reversed.

[00370] As described above, the first finger electrodes 151 and the first bus bar 153, such as those shown in FIG. 9, may be formed through the first electrode forming step S8, such as that shown in FIG. 17.

[00371] As described above, in the method for forming a solar cell according to the third embodiment of the present invention, the paste for the first finger electrodes and the paste for the first bus bar may be performed by the separate printing processes S8B1 and S8B12.

[00372] Furthermore, in this instance, a material included in the paste for the first finger electrodes and a material included in the paste for the first bus bar may be different.

[00373] More specifically, content of frit glass per unit volume which is included in the paste for the first bus bar may be smaller than content of frit glass per unit volume which is included in the paste for the first finger electrodes, or frit glass may not be included in the paste for the first bus bar.

[00374] The reason for this is that while the paste for the second finger electrodes perforates the first passivation film 190A and is depressed into the first conductive type semiconductor region 170 in the thermal treatment process for forming the first

electrode 150, the paste for the first bus bar perforates the first passivation film 190A, but is rarely depressed into the first conductive type semiconductor region 170 although it is connected to the first conductive type semiconductor region 170 or the paste for the first bus bar does not perforate the first passivation film 190A.

[00375] In this instance, the metal crystals MC may not be formed in the bus bar forming region 170A2 of the first conductive type semiconductor region 170, and the semiconductor substrate 100 can be prevented from being deteriorated.

[00376] Furthermore, content of frit glass per unit volume which is included in the plurality of first finger electrodes 151 may be the same as content of frit glass per unit volume which is included in the second electrode 140.

[00377] After the paste for the second electrode is coated, the second electrode 140 may also perforate the anti-reflection layer 130 and may be connected to the second conductive type semiconductor region 120. If content of frit glass per unit volume which is included in the paste for the second finger electrodes is the same as that included in the second electrode 140, speed at which the paste for the second electrode perforates the anti-reflection layer 130 and is depressed into the second conductive type semiconductor region 120 and speed at which the paste for the second finger electrodes perforates the first passivation film 190A and is depressed into the first conductive type semiconductor region 170 in the same thermal treatment process may become approximately the same.

[00378] Accordingly, temperatures in the thermal treatment processes for forming the second electrode 140 and the first electrode 150 may become the same, and speed at which the first finger electrodes 151 are depressed into the first conductive type semiconductor region 170 can be limited.

[00379] Furthermore, content of a metal material per unit volume which is included in the plurality of first finger electrodes 151 may be greater than content of a metal material per unit volume which is included in the plurality of first bus bars 153.

[00380] For example, content of a metal material per unit volume which is included in the plurality of first finger electrodes 151 may be 80 wt% or more to 95 wt% or less. Content of a metal material per unit volume which is included in the plurality of first bus bars 153 may be 60 wt% or more 80 wt% or less.

[00381] If content of a metal material per unit volume which is included in the first finger electrodes 151 is 80 wt% or more 95 wt% or less as described above, the metal

crystals MC can be sufficiently formed as described above with reference to FIG. 6 and resistance of the first finger electrodes 151 having relatively narrow widths can be sufficiently lowered in the state in which the paste for the second finger electrodes has perforated the first passivation film 190A and is depressed into the first conductive type semiconductor region 170.

[00382] Furthermore, if content of a metal material per unit volume which is included in the first bus bar 153 is 60 wt% or more 80 wt% or less, the metal crystals MC may not be formed in the bus bar forming region 170A2 of the first conductive type semiconductor region 170 due to the metal material included in the paste for the first bus bars although part of the paste for the first bus bars perforates the first passivation film 190A and is connected to the first conductive type semiconductor region 170, or the metal crystals MC may not be formed in the tunnel layer 160 as described above with reference to FIG. 7 although the metal crystals MC are formed in the bus bar forming region 170A2.

[00383] Furthermore, content of a metal material per unit volume which is included in the plurality of first finger electrodes 151 may be the same as content of a metal material per unit volume which is included in the second electrode 140.

[00384] If the first finger electrodes 151 and the first bus bar 153 having different materials are formed as described above, the deterioration of the semiconductor substrate 100 can be prevented, and the deterioration of efficiency of the solar cell can be further prevented.

[00385] As described above, the deterioration of the semiconductor substrate 100 may be generated during the thermal treatment process for forming the first electrode 150. If a temperature in the thermal treatment process is too low, the deterioration of efficiency of the solar cell can be prevented because contact resistance of the first electrode 150 is excessively increased.

[00386] The embodiments of the present invention have been described in detail above, but the scope of the present invention is not limited thereto. The scope of the present invention also includes a variety of modifications and changes which are defined in the appended claims and which will be performed by those skilled in the art using the basic concept of the present invention.

WHAT IS CLAIMED IS:

1. A method for manufacturing a solar cell, comprising:

a tunnel layer forming step of forming a tunnel layer on a first surface of a semiconductor substrate;

a first conductive type semiconductor region forming step of forming a first conductive type semiconductor region on the first surface of the semiconductor substrate;

a second conductive type semiconductor region forming step of forming a second conductive type semiconductor region by doping impurities of a second conductive type into a second surface of the semiconductor substrate;

a first passivation film forming step of forming a first passivation film on the first conductive type semiconductor region; and

an electrode forming step of forming a first electrode connected to the first conductive type semiconductor region and a second electrode connected to the second conductive type semiconductor region.

2. The method of claim 1, further comprising a step of forming an opening portion in the first passivation film after the first passivation film forming step.

3. The method of claim 2, wherein the step of forming the opening portion in the first passivation film is performed by thermal treatment in the electrode forming step.

4. The method of claim 3, wherein the electrode forming step comprises a first electrode forming step of forming the first electrode, and

wherein the first electrode forming step comprises printing a paste for first finger electrodes for forming the first finger electrodes and a paste for a first bus bar for forming the first bus bar on the first passivation film and performing thermal treatment on the pastes.

5. The method of claim 4, wherein in the first electrode forming step, a highest temperature for the thermal treatment is between 795□ to 870□.

6. The method of claim 4, wherein in the first electrode forming step, the paste for the first finger electrodes and the paste for the first bus bar are printed through a single process.

7. The method of claim 6, wherein a material included in the paste for the first finger electrodes is identical with a material included in the paste for the first bus bar.

8. The method of claim 4, wherein in the first electrode forming step, the paste for the first finger electrodes and the paste for the first bus bar are printed using separate printing processes.

9. The method of claim 8, wherein a material included in the paste for the first finger electrodes and a material included in the paste for the first bus bar are different.

10. The method of claim 1, further comprising an intrinsic semiconductor layer forming step of forming an intrinsic semiconductor layer on the tunnel layer formed on the first surface of the semiconductor substrate between the tunnel layer forming step and the first conductive type semiconductor region forming step, and,

in the first conductive type semiconductor region forming step, impurities of a first conductive type is doped into the intrinsic semiconductor layer formed on the first surface of the semiconductor substrate.

11. The method of claim 1, wherein the first surface of a semiconductor substrate is a back surface of a semiconductor substrate.

12. The method of claim 1, wherein the tunnel layer forming step comprises forming the tunnel layer on the first and second surfaces of the semiconductor substrate.

13. The method of claim 1, further comprising a removing step of removing the tunnel layer and the first conductive type semiconductor region placed at least on the second surface of the semiconductor substrate prior to the second conductive type semiconductor region forming step after the first conductive type semiconductor region forming step.

14. The method of claim 1, the first conductive type semiconductor region is formed by a thermal expansion of impurities of a first conductive type.

15. The method of claim 13, wherein the removing step comprises forming an isolation portion by removing the tunnel layer placed on a first side of the semiconductor substrate and an edge portion of the first conductive type semiconductor region.

16. The method of claim 15, wherein the first passivation film covers the first surface of the semiconductor substrate along with the isolation portion.

17. The method of claim 15, wherein the removing step comprises:

forming a mask layer having a smaller area than the semiconductor substrate on the first conductive type semiconductor region on a second side of the semiconductor substrate;

etching the first conductive type semiconductor region and the tunnel layer placed in a portion in which the mask layer has not been formed; and

removing the mask layer.

18. The method of claim 1, further comprising forming a second passivation film covering the second conductive type semiconductor region between the step of forming the second conductive type semiconductor region and the step of forming the first passivation film.

19. The method of claim 18, wherein the second passivation film is placed on a side of the semiconductor substrate, and the first passivation film is placed on the second passivation film.

20. The method of claim 1, wherein the first electrode is a front electrode positioned on a front surface of the semiconductor substrate, and the second electrode is a back electrode positioned on a back surface of the semiconductor substrate.

ABSTRACT

A method for manufacturing a solar cell can include a tunnel layer forming step of forming a tunnel layer on a first surface of a semiconductor substrate, a first conductive type semiconductor region forming step of forming a first conductive type semiconductor region on the first surface of the semiconductor substrate, a second conductive type semiconductor region forming step of forming a second conductive type semiconductor region by doping impurities of a second conductive type into a second surface of the semiconductor substrate, a first passivation film forming step of forming a first passivation film on the first conductive type semiconductor region and an electrode forming step of forming a first electrode connected to the first conductive type semiconductor region and a second electrode connected to the second conductive type semiconductor region.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	1630-1332PUS2
	Application Number	
Title of Invention	SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME	

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Application Information:

Title of the Invention	SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME		
Attorney Docket Number	1630-1332PUS2	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	18	**Suggested Figure for Publication (if any)**	

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For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

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This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
10-2014-0168624	KR	2014-11-28	

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
10-2015-0122846	KR	2015-08-31	

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	1630-1332PUS2
	Application Number	
Title of Invention	SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☒ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

PTO/AIA/14 (11-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	1630-1332PUS2
	Application Number	
Title of Invention	SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	LG ELECTRONICS INC.		
Mailing Address Information For Applicant:			
Address 1	128, Yeoui-daero, Yeongdeungpo-gu		
Address 2			
City	Seoul	**State/Province**	
Country	KR	Postal Code	07336
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	1630-1332PUS2
	Application Number	
Title of Invention	SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

Organization Name	LG ELECTRONICS INC.

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	128, Yeoui-daero, Yeongdeungpo-gu		
Address 2			
City	Seoul	**State/Province**	
Country i	KR	Postal Code	07336
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/David Bilodeau/			Date (YYYY-MM-DD)	2017-07-06
First Name	David	Last Name	Bilodeau	Registration Number	42325

Additional Signature may be generated within this form by selecting the Add button. Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	1630-1332PUS2
	Application Number	
Title of Invention	SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jungmin HA
Filer:	David Alan Bilodeau
Attorney Docket Number:	1630-1332PUS2

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1600**

Electronic Acknowledgement Receipt	
EFS ID:	29707959
Application Number:	15643180
International Application Number:	
Confirmation Number:	7835
Title of Invention:	SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jungmin HA
Customer Number:	2292
Filer:	David Alan Bilodeau/ROLONDA LEE
Filer Authorized By:	David Alan Bilodeau
Attorney Docket Number:	1630-1332PUS2
Receipt Date:	06-JUL-2017
Filing Date:	
Time Stamp:	17:34:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1600
RAM confirmation Number	070717INTEFSW17351000
Deposit Account	022448
Authorized User	ROLONDA LEE
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2017-07-06-ContinuationApplication-1630-1332PUS2.pdf	6190024 239aa261481c7e08306f765282825bbe7532132d	yes	93

Multipart Description/PDF files in .zip description

Document Description	Start	End
Transmittal of New Application	1	1
Miscellaneous Incoming Letter	2	2
Transmittal Letter	3	7
Information Disclosure Statement (IDS) Form (SB08)	8	11
Power of Attorney	12	13
Oath or Declaration filed	14	16
Drawings-only black and white line drawings	17	34
Specification	35	88
Claims	89	92
Abstract	93	93

Warnings:

Information:

2	Application Data Sheet	2017-07-06-ADS-1630-1332PUS2.pdf	1823320 9d0761d3f8d8b383c1fb65f5b9982d781b5706a4	no	10

Warnings:

Information:

3	Fee Worksheet (SB06)	fee-info.pdf	34768 575d9abf1c64e4cc4bbcee4070f82e10956a1b2a	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	8048112	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/643,180	07/06/2017	2827	1600	1630-1332PUS2	20	1

CONFIRMATION NO. 7835

FILING RECEIPT

2292
BIRCH STEWART KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
FALLS CHURCH, VA 22042-1248

OC000000092781450

Date Mailed: 07/17/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jungmin HA, Seoul, KOREA, REPUBLIC OF;
Sungjin KIM, Seoul, KOREA, REPUBLIC OF;
Juhwa CHEONG, Seoul, KOREA, REPUBLIC OF;
Junyong AHN, Seoul, KOREA, REPUBLIC OF;
Hyungwook CHOI, Seoul, KOREA, REPUBLIC OF;
Wonjae CHANG, Seoul, KOREA, REPUBLIC OF;
Jaesung KIM, Seoul, KOREA, REPUBLIC OF;

Applicant(s)

LG ELECTRONICS INC., Seoul, KOREA, REPUBLIC OF;

Assignment For Published Patent Application

LG ELECTRONICS INC., Seoul, KOREA, REPUBLIC OF

Power of Attorney: The patent practitioners associated with Customer Number 02292

Domestic Priority data as claimed by applicant

This application is a CON of 14/953,264 11/27/2015 PAT 9722104

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
REPUBLIC OF KOREA 10-2014-0168624 11/28/2014
REPUBLIC OF KOREA 10-2015-0122846 08/31/2015

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 07/13/2017

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/643,180**

Projected Publication Date: 10/26/2017

Non-Publication Request: No

Early Publication Request: No

Title

SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME

Preliminary Class

365

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor

community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/643,180

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1600

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT A	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT A	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT A	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT B	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT B	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT B	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

대 한 민 국 특 허 청
KOREAN INTELLECTUAL PROPERTY OFFICE

별첨 사본은 아래 출원의 원본과 동일함을 증명함.

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특 허 청 장
COMMISSIONER

【서지사항】

【서류명】 특허출원서

【출원구분】 특허출원

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【특허고객번호】 1-2002-012840-3

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【대리인번호】 9-2007-100122-0

【포괄위임등록번호】 2007-071744-8

【발명의 국문명칭】 태양 전지

【발명의 영문명칭】 SOLAR CELL

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【국적】 KR

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【국적】 KR

【취지】 위와 같이 특허청장에게 제출합니다.

대리인 특허법인로얄 (서명 또는 인)

【수수료】

【출원료】	0	면	46,000	원
【가산출원료】	40	면	0	원
【우선권주장료】	0	건	0	원
【심사청구료】	0	항	0	원
【합계】	46,000 원			

【발명의 설명】

【발명의 명칭】

태양 전지{SOLAR CELL}

【기술분야】

<1> 본 발명은 태양 전지에 관한 것이다.

【배경기술】

<2> 최근 석유나 석탄과 같은 기존 에너지 자원의 고갈이 예측되면서 이들을 대체할 대체 에너지에 대한 관심이 높아지고 있다. 그 중에서도 태양 전지는 태양 에너지로부터 전기 에너지를 생산하는 전지로서, 에너지 자원이 풍부하고 환경오염에 대한 문제점이 없어 주목 받고 있다.

<3> 일반적인 태양 전지는 p형과 n형처럼 서로 다른 도전성 타입(conductive type)의 반도체로 이루어진 기판(substrate) 및 에미터부(emitter layer), 그리고 기판과 에미터부에 각각 연결된 전극을 구비한다. 이때, 기판과 에미터부의 계면에는 p-n 접합이 형성되어 있다.

<4> 이러한 태양 전지에 빛이 입사되면 반도체에서 복수의 전자-정공쌍이 생성되고, 생성된 전자-정공쌍은 전자와 정공으로 각각 분리되어 전자와 정공은 n형의 반도체와 p형 반도체쪽으로, 예를 들어 에미터부와 기판쪽으로 이동하고, 기판과 에미터부와 전기적으로 연결된 전극에 의해 수집되며, 이 전극들을 전선으로 연결하여 전력을 얻는다.

【발명의 내용】

【해결하려는 과제】

<5> 본 발명은 태양 전지를 제공하는데 그 목적이 있다.

【과제의 해결 수단】

<6> 본 발명의 일례에 따른 태양 전지는 제1 도전성 타입의 불순물을 함유하는 반도체 기판; 반도체 기판의 전면에 위치하고 제1 도전성 타입과 반대인 제 2 도전성 타입의 불순물을 함유하는 에미터부; 반도체 기판의 후면 위에 위치하고, 유전체 재질을 포함하는 터널층; 터널층의 후면 위에 위치하고, 제1 도전성 타입의 불순물이 반도체 기판보다 고농도로 도핑된 다결정 실리콘 재질을 포함하는 후면 전계부; 후면 전계부의 후면에 위치하며, 유전체 재질의 후면 보호막; 에미터부와 연결되는 제1 전극; 및 후면 전계부와 연결되는 제2 전극;을 포함하고, 제2 전극의 적어도 일부는 후면 전계부 내부로 함입된다.

<7> 여기서, 후면 전계부와 제2 전극이 서로 접촉하는 제1 경계면은 후면 전계부와 후면 보호막이 서로 접촉하는 제2 경계면보다 반도체 기판 방향으로 더 인접하여 위치한다.

<8> 이때, 후면 전계부 중에서 제2 전극이 형성되는 전극 형성 영역에는 복수의 금속 결정을 더 포함할 수 있고, 이와 같은 금속 결정은 후면 전계부 중에서 제2 전극이 형성되지 않는 비형성 영역에는 위치하지 않을 수 있다.

<9> 또한, 금속 결정은 터널층 내에는 위치하지 않을 수 있다.

<10> 여기서, 복수의 금속 결정은 제2 전극에 포함된 금속 물질과 동일한 금속 물질을 포함할 수 있다.

<11> 이와 같은 복수의 금속 결정의 중 일부는 제2 전극과 직접 접촉될 수 있고, 복수의 금속 결정의 중 적어도 하나 이상은 제2 전극과 이격될 수 있다.

<12> 아울러, 복수의 금속 결정은 제2 전극으로부터 터널층 방향으로의 길이가 후면 전계부 두께의 2/3 이하일 수 있으며, 복수의 금속 결정 중 일부는 제2 전극으로부터 터널층 방향으로 진행할수록 폭이 감소할 수 있다.

<13> 여기서, 제2 전극은 후면 전계부의 후면에서 보았을 때, 제1 방향으로 길게 형성되는 복수의 제2 핑거 전극과, 제1 방향과 교차하는 제2 방향으로 길게 형성되며, 복수의 제2 핑거 전극이 공통으로 접속되는 제2 버스바를 포함할 수 있다.

<14> 이때, 복수의 제2 핑거 전극은 후면 보호막을 관통하여 후면 전계부 내부로 함입되어 형성되고, 복수의 제2 버스바는 후면 보호막의 후면 위에 형성될 수 있다.

<15> 여기서, 후면 전계부의 제1 경계면에서 후면 전계부와 제2 핑거 전극은 서로 접촉하고, 후면 전계부의 전극 형성 영역 중에서 제2 핑거 전극이 형성되는 핑거 형성 영역에는 복수의 금속 결정을 더 포함할 수 있다.

<16> 그리고, 후면 전계부의 전극 형성 영역 중에서 제2 버스바가 형성되는 버스바 형성 영역에는 복수의 금속 결정이 위치하지 않을 수 있다.

<17> 이를 위해, 복수의 제2 핑거 전극에 포함되는 재질과 복수의 제2 버스바에

포함되는 재질은 서로 다르게 형성될 수 있다.

<18> 구체적으로, 복수의 제2 버스바에 포함되는 단위 부피당 글래스 프릿의 함유량은 복수의 제2 핑거 전극에 포함되는 단위 부피당 글래스 프릿의 함유량보다 작을 수 있다.

<19> 이때, 복수의 제2 핑거 전극에 포함되는 단위 부피당 글래스 프릿의 함유량은 제1 전극에 포함되는 단위 부피당 글래스 프릿의 함유량과 동일할 수 있다.

<20> 또한, 복수의 제2 핑거 전극에 포함되는 단위 부피당 금속 물질의 함유량은 복수의 제2 버스바에 포함되는 단위 부피당 금속 물질의 함유량보다 많을 수 있다.

<21> 구체적으로, 복수의 제2 핑거 전극에 포함되는 단위 부피당 금속 물질의 함유량은 80wt%이상 95wt%이하이고, 복수의 제2 버스바에 포함되는 단위 부피당 금속 물질의 함유량은 60wt%이상 80wt%이하일 수 있다.

<22> 이때, 복수의 제2 핑거 전극에 포함되는 단위 부피당 금속 물질의 함유량은 제1 전극에 포함되는 단위 부피당 금속 물질의 함유량과 동일할 수 있다.

【발명의 효과】

<23> 본 발명에 따른 태양 전지는 제2 전극의 적어도 일부가 후면 전계부 내로 함입되어 형성되도록 하여, 태양 전지의 효율을 보다 증가시킬 수 있다.

【도면의 간단한 설명】

<24> 도 1 내지 도 4는 본 발명의 제1 실시예에 따른 태양 전지를 설명하기 위한 도이다.

도 5는 본 발명의 제1 실시예와 다른 비교예를 설명하기 위한 도이다.

도 6은 본 발명의 제2 실시예에 따른 태양 전지를 설명하기 위한 도이다.

도 7은 제2 버스바 페이스트(153P)의 재질이 제2 핑거 페이스트의 재질과 동일한 경우, 열처리 공정시 소성 온도에 따른 반도체 기판(110)의 열화 정도를 PL(photo luminescence) 촬영한 비교예 사진이다.

도 8은 본 발명의 제2 실시예에 따라 제2 버스바 페이스트(153P)의 재질과 제2 핑거 페이스트의 재질이 서로 다른 경우, 열처리 공정시 소성 온도에 따른 반도체 기판(110)의 열화 정도를 PL(photo luminescence) 촬영한 사진이다.

【발명을 실시하기 위한 구체적인 내용】

<25> 아래에서는 첨부한 도면을 참고로 하여 본 발명의 실시예에 대하여 본 발명이 속하는 기술 분야에서 통상의 지식을 가진 자가 용이하게 실시할 수 있도록 상세히 설명한다. 그러나 본 발명은 여러 가지 상이한 형태로 구현될 수 있으며 여기에서 설명하는 실시예에 한정되지 않는다. 그리고 도면에서 본 발명을 명확하게 설명하기 위해서 설명과 관계없는 부분은 생략하였으며, 명세서 전체를 통하여 유사한 부분에 대해서는 유사한 도면 부호를 붙였다.

<26> 도면에서 여러 층 및 영역을 명확하게 표현하기 위하여 두께를 확대하여 나타내었다. 층, 막, 영역, 판 등의 부분이 다른 부분 "위에" 있다고 할 때, 이는 다른 부분 "바로 위에" 있는 경우뿐 아니라 그 중간에 다른 부분이 있는 경우도 포함한다. 반대로 어떤 부분이 다른 부분 "바로 위에" 있다고 할 때에는 중간에 다른

부분이 없는 것을 뜻한다. 또한 어떤 부분이 다른 부분 위에 "전체적"으로 형성되어 있다고 할 때에는 다른 부분의 전체 면(또는 전면)에 형성되어 있는 것뿐만 아니라 가장 자리 일부에는 형성되지 않은 것을 뜻한다.

<27> 또한, 전면이라 함은 직사광이 입사되는 반도체 기판의 일면일 수 있으며, 후면이라 함은 직사광이 입사되지 않거나, 직사광이 아닌 반사광이 입사될 수 있는 반도체 기판의 반대면일 수 있다.

<28> 아울러, 어떠한 두 개의 값이 동일하다는 것은 오차 범위 10% 이하에서 동일하다는 것을 의미한다.

<29> 그러면 첨부한 도면을 참고로 하여 본 발명에 따른 태양 전지에 대하여 설명한다.

<30> 도 1 내지 도 4는 본 발명의 제1 실시예에 따른 태양 전지를 설명하기 위한 도이고, 도 5는 본 발명의 제1 실시예와 다른 비교예를 설명하기 위한 도이다.

<31> 보다 구체적으로, 도 1은 본 발명의 제1 실시예에 따른 태양 전지의 일부 사시도이고, 도 2는 도 1에 도시한 태양 전지를 Ⅱ-Ⅱ선을 따라 잘라 도시한 단면도이다. 아울러, 도 3은 도 2에서 K 부분을 확대한 확대도이고, 도 4는 제2 전극(150)과 후면 전계부(170)의 접촉 부분에 대한 실물 사진을 도시한 것이다.

<32> 도 1에 도시된 바와 같이, 본 발명에 따른 태양 전지의 일례는 반도체 기판(110), 에미터부(120), 반사 방지막(130), 터널층(160), 후면 전계부(170), 후면 보호막(190), 제1 전극(140) 및 제2 전극(150)을 포함한다.

<33> 도 1에서는 본 발명에 따른 태양 전지가 반사 방지막(130)을 포함하는 것을 일례로 도시하고 있으나, 본 발명은 이와 다르게 반사 방지막(130)이 생략되는 것도 가능하다. 그러나, 태양 전지의 효율을 고려했을 때, 반사 방지막(130)이 포함되는 것이 더 나은 효율이 발생하므로, 반사 방지막(130)이 포함되는 것을 일례로 설명한다.

<34> 반도체 기판(110)은 제1 도전성 타입, 예를 들어 p형 도전성 타입의 불순물을 함유하는 실리콘으로 이루어진 반도체 반도체 기판(110)이다. 일례로, 반도체 기판(110)은 단결정 실리콘 또는 다결정 실리콘으로 이루어진 반도체 웨이퍼가 사용될 수 있다.

<35> 반도체 기판(110)이 p형의 도전성 타입을 가질 경우, 붕소(B), 갈륨, 인듐 등과 같은 3가 원소의 불순물을 함유한다. 하지만, 이와는 달리, 반도체 기판(110)은 n형 도전성 타입일 수 있고, 실리콘 이외의 다른 반도체 물질로 이루어질 수도 있다. 반도체 기판(110)이 n형의 도전성 타입을 가질 경우, 반도체 기판(110)은 인(P), 비소(As), 안티몬(Sb) 등과 같이 5가 원소의 불순물을 함유할 수 있다. 이하에서는 반도체 기판(110)이 n형의 도전성 타입을 가지는 경우를 일례로 설명한다.

<36> 도 1 및 도 2에 도시된 바와 같이, 반도체 기판(110)의 표면은 텍스처링(texturing)처리되어 있는 요철면인 텍스처링 표면(texturing surface)을 가질 수 있다.

<37> 에미터부(120)는 빛이 입사되는 반도체 기판(110)의 전면에 위치하며, 반도

체 기판(110)의 도전성 타입과 반대인 제2 도전성 타입, 예를 들어, n형의 도전성 타입의 불순물을 함유하여 반도체 반도체 기판(110)과 p-n 접합을 이룬다.

<38> 이와 같은 p-n 접합에 의해 외부로부터 반도체 기판(110)에 빛이 입사되어 생성된 캐리어인 전자-정공 쌍은 전자와 정공으로 분리되어 전자는 n형 쪽으로 이동하고 정공은 p형 쪽으로 이동한다. 따라서, 반도체 기판(110)이 p형이고 에미터부(120)가 n형일 경우, 분리된 정공은 반도체 기판(110)쪽으로 이동하고 분리된 전자는 에미터부(120)쪽으로 이동할 수 있다.

<39> 그러나, 이와 달리, 반도체 기판(110)이 n형의 도전성 타입을 가질 경우, 에미터부(120)는 p형의 도전성 타입을 가진다. 이 경우, 분리된 전자는 반도체 기판(110)쪽으로 이동하고 분리된 정공은 에미터부(120)쪽으로 이동할 수 있다.

<40> 에미터부(120)가 n형의 도전성 타입을 가질 경우, 에미터부(120)는 인(P), 비소(As), 안티몬(Sb) 등과 같이 5가 원소의 불순물을 반도체 기판(110)에 도핑하여 형성될 수 있고, 반대로 p형의 도전성 타입을 가질 경우, 붕소(B), 갈륨, 인듐 등과 같은 3가 원소의 불순물을 반도체 기판(110)에 도핑하여 형성될 수 있다.

<41> 이와 같은 에미터부(120)는 반도체 기판(110)의 전면 표면에 제2 도전성 타입의 불순물이 확산되어 형성될 수 있으며, 이와 같은 경우, 에미터부(120)는 반도체 기판(110)과 동일한 실리콘 재질로 형성될 수 있다.

<42> 일례로, 반도체 기판(110)이 다결정 실리콘 재질의 웨이퍼로 형성된 경우, 에미터부(120)도 다결정 실리콘 재질로 형성될 수 있으며, 반도체 기판(110)이 단

결정 실리콘 재질의 웨이퍼로 형성되는 에미터부(120)도 단결절 실리콘 재질로 형성될 수 있다.

<43> 반사 방지막(130)은 에미터부(120) 위에 위치하며, 알루미늄 산화막(AlOx), 실리콘 질화막(SiNx), 실리콘 산화막(SiOx) 및 실리콘 산화질화막(SiOxNy) 중 적어도 하나로 형성될 수 있고, 단일막 또는 다층막으로 형성될 수 있다.

<44> 도 1 및 도 2에서는 반사 방지막(130)이 단일막으로 형성된 경우를 일례로 도시하였으나, 반드시 단일막에 한정되지는 않는다.

<45> 이와 같은 반사 방지막(130)은 태양 전지로 입사되는 빛의 반사도를 줄이고 특정한 파장 영역의 선택성을 증가시켜, 태양 전지의 효율을 높인다.

<46> 제1 전극(140)은 에미터부(120) 위에 직접 접하여 배치되며, 에미터부(120)와 전기적으로 연결되어 있다. 이와 같은 제1 전극(140)은 도 1에 도시된 바와 같이, 복수의 제1 핑거 전극(141) 및 복수의 제1 버스바(143)를 포함할 수 있다.

<47> 여기서, 복수의 제1 핑거 전극(141)은 에미터부(120) 위에 위치하여 에미터부(120)와 전기적으로 연결되어 있고, 서로 이격하여 제1 방향(x)으로 뻗어있을 수 있다.

<48> 이와 같은 복수의 제1 핑거 전극(141)은 도 1 및 도 2에 도시된 바와 같이, 반도체 기판(110)이 n 타입인 경우, p 타입의 에미터부(120)쪽으로 이동한 캐리어, 예를 들면, 정공을 수집할 수 있다.

<49> 그리고, 복수의 제1 버스바(143)는 에미터부(120) 위에서 복수의 제1 핑거

전극(141)과 동일 층에 위치하고, 복수의 제1 핑거 전극(141)을 서로 전기적으로 연결시키며, 복수의 제1 핑거 전극(141)과 교차하는 제2 방향(y)으로 뻗어있을 수 있다.

<50> 이와 같은 복수의 제1 버스바(143)는 태양 전지를 서로 연결시키는 인터커넥터(미도시)와 연결되며, 복수의 제1 핑거 전극(141)에 의해 수집되어 이동하는 캐리어를 수집하여 외부 장치로 출력한다.

<51> 복수의 제1 핑거 전극(141)과 제1 버스바(143)는 적어도 하나의 도전성 금속 물질로 이루어져 있고, 이들 도전성 금속 물질의 예는 니켈(Ni), 구리(Cu), 은(Ag), 알루미늄(Al), 주석(Sn), 아연(Zn), 인듐(In), 티타늄(Ti), 금(Au) 및 이들의 조합으로 이루어진 군으로부터 선택된 적어도 하나일 수 있지만, 이외의 다른 도전성 금속 물질로 이루어질 수 있다.

<52> 이와 같은 제1 전극(140)은 반도체 기판(110)의 전면에 반사 방지막(130)이 형성된 이후, 제1 전극(140)을 형성하기 위한 제1 전극 페이스트를 반사 방지막(130)의 전면 위에 패터닝하여 도포한 이후, 열처리 공정을 통하여 제1 전극 페이스트가 반사 방지막(130)을 뚫고 에미터부(120)에 접속되어 소성되면서 형성될 수 있다.

<53> 이를 위해, 제1 전극(140)은 전술한 금속 물질 이외에 글래스 프릿(glass frit)을 함유할 수 있다.

<54> 터널층(160)은 반도체 기판(110)의 후면 위에 배치되며, 유전체 재질을 포함

할 수 있다.

<55> 일례로, 터널층(160)은 도 1 및 도 2에 도시된 바와 같이, 반도체 기판(110)의 후면 위에 형성되되, 반도체 기판(110)의 후면 위에 직접 접촉되어 형성될 수 있다.

<56> 아울러, 터널층(160)은 반도체 기판(110)의 후면 전체 영역 위에 형성될 수 있다.

<57> 이와 같은 터널층(160)은 반도체 기판(110)에서 생성된 캐리어를 후면 전계부(170) 방향으로 통과시키며, 반도체 기판(110)의 후면에 대한 패시베이션 기능을 수행할 수 있다. 아울러, 이와 같은 터널층(160)은 태양 전지의 개방 전압(Voc)를 상승시키는 역할을 할 수 있다.

<58> 이와 같은, 터널층(160)은 600℃ 이상의 고온 공정에도 내구성이 강한 SiCx 또는 SiOx로 형성되는 유전체 재질로 형성될 수 있다. 그러나 이 외에도 silicon nitride (SiNx), hydrogenerated SiNx, aluminum oxide (AlOx), silicon oxynitride (SiON) 또는 hydrogenerated SiON로 형성되는 것도 가능하다.

<59> 또한, 터널층(160)의 두께(T160)는 0.5nm ~ 2.5nm사이로 형성될 수 있다. 이와 같은 터널층(160)은 Oxidation 공정이나 LPCVD 공정 또는 PECVD 증착 공정에 의해 형성될 수 있다.

<60> 여기서, 터널층(160)의 두께(T160)를 0.5nm ~ 2.5nm 로 한정하는 것은 터널링 효과를 구현하기 위함이고, 이와 같은 한정 범위를 0.5nm ~ 2.5nm 범위를 조금

넘어서는 경우도 가능하나, 터널링의 효과가 감소할 수 있다.

<61> 보다 구체적으로, 터널층(160)의 두께(T160)를 0.5nm 이상으로 하는 것은 실질적으로 0.5nm 미만으로 터널층(160)을 형성하는 것은 현실적으로 매우 어렵고, 터널층(160)의 두께(T160)를 2.5nm 이하로 하는 것은 2.5nm를 넘어서는 경우 터널링 효과가 거의 일어나지 않을 수 있기 때문이다.

<62> 아울러, 이와 같은 터널층(160)은 반도체 기판(110)의 후면 표면에 대한 패시베이션 기능도 일부 수행할 수 있다.

<63> 다음, 후면 전계부(170)는 반도체 기판(110)의 후면 표면 위에 위치하고, 제1 도전성 타입의 불순물이 반도체 기판(110)보다 고농도로 함유되며, 다결정 실리콘 재질을 포함할 수 있다.

<64> 즉, 이와 같은 후면 전계부(170)는 도 1 및 도 2에 도시된 바와 같이, 반도체 기판(110)의 후면에 형성된 터널층(160)의 후면 위에 형성되어, 반도체 기판(110)과 이격되어 형성될 수 있다.

<65> 후면 전계부(170)가 반도체 기판(110) 내에 형성되지 않고, 도 1 및 도 2에 도시된 바와 같이, 후면 전계부(170)가 반도체 기판(110)의 후면 위에 형성되되, 반도체 기판(110)과 직접 접촉하지 않고 이격되어, 터널층(160)의 후면 위에 다결정 실리콘 재질로 형성된 경우, 태양 전지의 개방 전압(Voc)을 더욱 향상시킬 수 있다.

<66> 아울러, 반도체 기판(110) 내에 후면 전계부(170)를 형성하지 않고 반도체

기판(110)의 외부에 후면 전계부(170)를 형성하므로, 제조 공정상 후면 전계부(170)를 형성하는 과정에서, 반도체 기판(110)에 대한 열손상을 최소화할 수 있어, 반도체 기판(110)의 특성이 저하되는 것을 방지할 수 있다. 따라서, 도 1 및 도 2에 도시된 바와 같은 태양 전지는 효율을 더 향상시킬 수 있다.

<67> 이와 같은, 후면 전계부(170)의 두께(T170)는 50㎚ ~ 500㎚ 사이로 형성될 수 있다.

<68> 제2 전극(150)은 후면 전계부(170)의 후면 위에 배치되며, 후면 전계부(170)와 전기적으로 연결되어 있다. 이와 같은 제2 전극(150)은 도 1 및 도 2에 도시된 바와 같이, 복수의 제2 핑거 전극(151) 및 복수의 제2 버스바(153)를 포함할 수 있다.

<69> 여기서, 복수의 제2 핑거 전극(151)은 후면 전계부(170)의 후면 위에 서로 이격하여 제1 방향(x)으로 뻗어있을 수 있으며, 후면 전계부(170) 쪽으로 이동한 캐리어, 예를 들면, 정공을 수집할 수 있다.

<70> 그리고, 복수의 제2 버스바(153)는 후면 전계부(170) 위에서 복수의 제2 핑거 전극(151)과 동일 층에 위치하고, 복수의 제2 핑거 전극(151)을 서로 전기적으로 연결시키며, 복수의 제2 핑거 전극(151)과 교차하는 제2 방향(y)으로 뻗어 있을 수 있다.

<71> 이와 같은 복수의 제2 버스바(153)는 태양 전지를 서로 연결시키는 인터커넥터(미도시)와 연결되며, 제2 핑거 전극(151)에 의해 수집되어 이동하는 캐리어를

수집하여 외부 장치로 출력한다.

<72> 여기서, 제2 버스바(153)의 길이 방향은 제1 버스바(143)의 길이 방향과 동일하고, 제2 핑거 전극(151)의 길이 방향도 제1 핑거 전극(141)의 길이 방향과 동일할 수 있으며, 제2 전극(150)의 재질은 제1 전극(140)의 재질과 동일할 수 있다.

<73> 이와 같은 제2 전극(150)은 후면 전계부(170) 위에 후술할 후면 보호막(190)이 형성된 상태에서 후면 보호막(190)의 위에 제2 전극(150)을 형성하기 위한 제2 전극 패이스트를 패터닝하여 형성한 상태에서 열처리 공정을 통하여 형성될 수 있다.

<74> 여기서, 제2 핑거 전극(151)의 폭은 일례로, 150um ~ 400um 사이일 수 있으며, 제2 버스바(153)의 폭은 제2 핑거 전극(151)의 폭보다 크게 형성되되, 1mm ~ 3mm 사이의 범위에서 결정될 수 있다. 그러나, 이에 반드시 한정되는 것은 아니고, 다른 폭을 가질 수도 있다.

<75> 다음, 후면 보호막(190)은 도 1 및 도 2에 도시된 바와 같이, 후면 전계부(170)의 후면 중에서 제2 전극(150)이 형성된 영역을 제외한 전체 영역 위에 위치할 수 있다.

<76> 이와 같은 후면 보호막(190)은 유전체 재질로 형성될 수 있으며, 단층 또는 다수의 층으로 형성될 수 있고, 후면 전계부(170)의 극성을 고려하여 특정 고정 전하를 가질 수 있다.

<77> 이와 같은 후면 보호막(190)의 재질은 SiCx, SiOx, silicon nitride (SiNx),

hydrogenerated SiNx, aluminum oxide (AlOx), silicon oxynitride (SiON) 또는 hydrogenerated SiON 중 적어도 하나로 형성될 수 있다.

<78> 이와 같은 후면 보호막(190)은 후면 전계부(170)의 후면 표면을 패시베이션 하는 기능을 수행할 수 있다.

<79> 도 1 및 도 2에서, 이와 같은 구조를 갖는 본 실시예에 따른 태양 전지의 동작은 다음과 같다.

<80> 태양 전지로 빛이 조사되어 반사 방지막(130)과 에미터부(120)를 통해 반도체의 반도체 기판(110)으로 입사되면 빛 에너지에 의해 반도체의 반도체 기판(110)에서 전자-정공 쌍이 발생한다. 이때, 반사 방지막(130)에 의해 반도체 기판(110)으로 입사되는 빛의 반사 손실이 줄어들어 반도체 기판(110)으로 입사되는 빛의 양이 증가한다.

<81> 이들 전자-정공 쌍은 반도체 기판(110)과 에미터부(120)의 p-n접합에 의해 서로 분리되어 정공과 전자는, 예를 들어, p형의 도전성 타입을 갖는 에미터부(120)와 n형의 도전성 타입을 갖는 반도체 기판(110)쪽으로 각각 이동한다. 이처럼, 에미터부(120)쪽으로 이동한 정공은 제1 핑거 전극(141)에 의해 수집되어 제1 버스바(143)로 전달되고, 반도체 기판(110)의 후면 쪽에 위치한 후면 전계부(170)로 이동한 전자는 제2 핑거 전극(151)에 의해 수집되어 제2 버스바(153)로 전달될 수 있다.

<82> 아울러, 서로 인접한 태양 전지 각각의 제1, 2 버스바(143, 153)를 서로 인

터커넥터(미도시)로 연결하면 전류가 흐르게 되고, 이를 외부에서 전력으로 이용할 수 있게 된다.

<83> 한편, 본 발명에 따른 태양 전지는 도 1 내지 도 3에 도시된 바와 같이, 제2 전극(150)의 적어도 일부는 후면 전계부(170) 내부로 함입되어 형성될 수 있다. 구체적 일례로, 제2 전극(150)을 형성하는 제2 핑거 전극(151)과 제2 버스바(153) 모두가 후면 전계부(170) 내부로 함입되어 형성될 수 있다.

<84> 다시 말하면, 후면 전계부(170)와 제2 전극(150)이 서로 접촉하는 제1 경계면(BS1)이 후면 전계부(170)와 후면 보호막(190)이 서로 접촉하는 제2 경계면(BS2)보다 반도체 기판(110) 방향으로 더 인접하여 형성되어 위치할 수 있다.

<85> 도 3에서는 제2 핑거 전극(151)을 일례로 도시하였지만, 제2 버스바(153)도 제2 핑거 전극(151)과 마찬가지로 후면 전계부(170) 내부로 함입된 동일한 구조를 가질 수 있다.

<86> 이와 같이, 제2 전극(150)이 후면 전계부(170) 내부로 함입되는 형상은 제2 전극(150)을 형성하기 위한 제2 전극 페이스트를 후면 보호막(190)의 후면에 패터닝하여 형성한 상태에서 열처리 공정을 통하여 제2 전극 페이스트가 후면 보호막(190)을 뚫고 후면 전계부(170) 내부로 침투하면서 접속될 때 나타날 수 있는 형상이다.

<87> 이와 같이, 제2 전극 페이스트를 이용하여 제2 전극(150)을 형성하면, 도금법에 비하여 상대적으로 비용이 저렴하고 공정 시간을 단축할 수 있는 장점이

있다.

<88> 여기서, 제1 경계면(BS1)과 제2 경계면(BS2)의 높이 차이는 1nm ~ 20nm 사이로 형성될 수 있으며, 이와 같은 제1, 2 경계면(BS1, BS2)의 높이 차이(TBS)는 제2 전극(150)을 형성하기 위한 열처리 공정의 시간 및 제2 전극 페이스트에 포함되는 글래스 프릿(glass frit)의 함유량에 따라 달라질 수 있다.

<89> 도 1 내지 도 3에서는 제2 전극(150)을 형성하는 복수의 제2 버스바(153)와 복수의 제2 핑거 전극(151) 모두가 후면 전계부(170) 내부로 함입된 경우를 일례로 도시하였지만, 반드시 이에 한정되는 것은 아니고, 제2 전극(150) 중 복수의 제2 핑거 전극(151)만 후면 전계부(170) 내부로 함입되어 형성될 수도 있다. 이와 같이, 복수의 제2 핑거 전극(151)만 후면 전계부(170) 내부로 함입된 구성에 대해서는 도 6 이하에서 보다 구체적으로 설명한다.

<90> 따라서, 본 발명에 따른 태양 전지는 도 3에 도시된 바와 같이, 제2 전극(150)이 후면 전계부(170) 내부로 함입되어, 후면 전계부(170)의 제1 경계면(BS1)에서 후면 전계부(170)와 제2 전극(150)은 서로 접촉할 수 있다.

<91> 이때, 도 2에 도시된 바와 같이, 후면 전계부(170) 중에서 제2 전극(150)이 형성되는 전극 형성 영역(1700A)에는 복수의 금속 결정(MC)을 더 포함할 수 있다.

<92> 일례로, 도 3에 도시된 바와 같이, 후면 전계부(170) 중에서 제2 핑거 전극(151)이 형성되는 핑거 형성 영역(1700F)에는 복수의 금속 결정(MC)을 더 포함할 수 있다. 도 3에서는 후면 전계부(170)의 전극 형성 영역(1700A) 중에서 전극 핑거

형성 영역(1700F)만 도시하였으나, 버스바 형성 영역(1700B)에도 동일하게 복수의 금속 결정(MC)을 더 포함할 수 있다.

<93> 참고로, 도 2를 참조하면, 후면 전계부(170) 중에서, 제2 핑거 전극(151)과 터널층(160) 사이의 공간에 위치하는 후면 전계부(170)의 영역은 핑거 형성 영역(1700F)이라 하고, 제2 버스바(153)와 터널층(160) 사이의 공간에 위치하는 후면 전계부(170)의 영역은 버스바 형성 영역(1700B)이라 하고, 후면 전계부(170) 중에서 핑거 형성 영역(1700F)과 버스바 형성 영역(1700B)을 제외한 나머지 영역을 비형성 영역(170NO)이라 한다. 아울러, 핑거 형성 영역(1700F)과 버스바 형성 영역(1700B)을 통칭하여 전극 형성 영역(1700A)이라 한다.

<94> 이와 같은 복수의 금속 결정(MC)은 다결정 실리콘으로 형성되는 후면 전계부(170)와 비교하여 상대적으로 저항이 낮아, 도 3에 도시된 바와 같이, 반도체 기판(110)으로부터 터널층(160)을 통과하여 후면 전계부(170)로 이동한 캐리어, 예를 들어 전자들이 금속 결정(MC)을 통하여 제2 전극(150)으로 직접 이동하거나, 금속 결정(MC)과 금속 결정(MC) 사이를 점프하여 제2 전극(150)으로 이동할 수 있다. 따라서, 이와 같은 복수의 금속 결정(MC)들은 캐리어가 제2 전극(150)으로 보다 용이하게 이동할 수 있도록 도와주는 역할을 할 수 있다.

<95> 따라서, 이와 같은 금속 결정(MC)은 낮은 저항으로 인하여, 반도체 기판(110)과 제2 전극(150) 사이의 실질적인 거리를 보다 좁혀줄 수 있다.

<96> 또한, 금속 결정(MC)은 제2 전극(150)이 후면 전계부(170)에 접속될 때, 제2 전극(150)과 후면 전계부(170)의 경계인 제1 경계면(BS1)을 중심으로 반도체 기판

(110) 방향으로 형성되기 때문에, 제2 전극(150)과 후면 전계부(170) 사이의 접촉 저항을 보다 낮출 수 있다.

<97> 따라서, 도 3에 도시된 본 발명과 같이, 제2 전극(150)과 터널층(160) 사이의 후면 전계부(170) 내부에 복수의 금속 결정(MC)을 더 포함하는 경우, 태양 전지의 효율이 보다 향상될 수 있다.

<98> 이와 같은 금속 결정(MC)은 후면 전계부(170) 중에서 제2 전극(150)이 형성되는 전극 형성 영역(170OA)에 위치하고, 후면 전계부(170) 중에서 제2 전극(150)이 형성되지 않는 비형성 영역(170NO)에는 금속 결정(MC)이 위치하지 않을 수 있다.

<99> 이와 같이, 금속 결정(MC)이 후면 전계부(170) 중에서 전극 형성 영역(170OA)에만 위치하고, 비형성 영역(170NO)에는 위치하지 않는 것은 이와 같은 복수의 금속 결정(MC)이 제2 전극(150)을 형성하기 위한 열처리 공정 중에서 제2 전극(150)으로부터 빠져나온 금속이 재결정화되어 형성되기 때문이다.

<100> 일례로, 복수의 제2 전극(150)은 적어도 하나의 도전성 금속 물질을 포함하여 형성될 수 있다. 여기서, 복수의 제2 전극(150)에 포함되는 도전성 금속 물질은 일례로, 니켈(Ni), 구리(Cu), 은(Ag), 알루미늄(Al), 주석(Sn), 아연(Zn), 인듐(In), 티타늄(Ti), 금(Au) 및 이들의 조합으로 이루어진 군으로부터 선택된 적어도 하나일 수 있지만, 이외의 다른 도전성 금속 물질로 이루어질 수 있다.

<101> 여기서, 복수의 금속 결정(MC)은 제2 전극(150)을 형성하기 위한 열처리 공

정 중에 전술한 제2 전극(150)에 포함된 금속 물질이 빠져나와 재결정화되면서 형성될 수 있어, 제2 전극(150)에 포함된 금속 물질과 동일한 금속 물질을 포함할 수 있다. 따라서, 일례로, 제2 전극(150)이 은(Ag)을 포함하는 경우, 금속 결정(MC)도 은(Ag)을 포함할 수 있다.

<102> 또한, 도 3 및 도 4에 도시된 바와 같이, 금속 결정(MC)은 후면 전계부(170) 내에는 위치하지만, 터널층(160) 내에는 위치하지 않을 수 있다.

<103> 즉, 도 5에 도시된 비교예와 같이, 이와 같은 금속 결정(MC)이 터널층(160) 내에 위치하는 경우 터널층(160)의 기능이 저하될 수 있고, 금속 결정(MC)이 터널층(160)을 관통하여 반도체 기판(110)의 후면 내부로 침투되는 경우, 반도체 기판(110) ? 터널층(160) - 후면 전계부(170)로 형성된 구조에 의해 나타나는 개방 전압(Voc) 특성이 저하되어, 반도체 기판(110)이 열화될 수 있다.

<104> 이와 같이, 반도체 기판(110)이 열화되는 경우, 반도체 기판(110)의 특성, 일례로 캐리어 라이프 타임(carrier life time)과 같은 특성이 저하될 수 있다.

<105> 그러나, 본 발명과 같이 금속 결정(MC)이 후면 전계부(170) 내에는 위치하지만, 터널층(160) 내에는 위치하지 않는 경우, 이와 같은 특성 저하를 방지할 수 있다.

<106> 이와 같은 복수의 금속 결정(MC)의 중 일부(MC1)는 도 3에 도시된 바와 같이, 제2 전극(150)과 직접 접촉될 수 있고, 아울러, 복수의 금속 결정(MC)의 중 적어도 하나(MC2) 이상은 제2 전극(150)과 이격되어 후면 전계부(170) 내에 위치할

수 있다.

<107> 여기서, 복수의 금속 결정(MC)은 제2 전극(150)으로부터 터널층(160) 방향으로의 길이(LMC)가 후면 전계부(170) 두께의 2/3 이하일 수 있다. 이와 같이, 금속 결정(MC)의 길이(LMC)를 후면 전계부(170) 두께의 2/3 이하로 한정하는 것은 금속 결정(MC)의 길이(LMC)가 과도하게 길게 되어, 전술한 바와 같이, 터널층(160)이나 반도체 기판(110)을 손상시키지 않도록 하기 위함이다.

<108> 복수의 금속 결정(MC) 중 일부는 제2 전극(150)으로부터 터널층(160) 방향으로 진행할수록 폭(WMC)이 감소할 수 있다. 즉, 도 3이나 도 4에 도시된 바와 같이, 금속 결정(MC)에서 제2 전극(150) 쪽에 인접한 부분의 면 방향(x, y) 폭(WMC)은 반도체 기판(110) 쪽에 인접한 부분의 폭보다 작을 수 있다.

<109> 이와 같은 금속 결정(MC)의 크기는 제2 전극(150)을 형성하기 위한 열처리 공정의 소성 온도에 비례하여 크기가 결정될 수 있다.

<110> 즉, 금속 결정(MC)의 길이나 폭은 제2 전극(150)을 형성하기 위한 열처리 공정의 소성 온도가 높을수록 커지고, 낮을수록 작아지는 특성이 있으며, 금속 결정(MC)의 소스인 제2 전극(150)의 폭이 증가할수록 금속 결정(MC)의 길이나 폭이 증가할 수 있다.

<111> 그러나, 제2 전극(150)을 형성하기 위한 열처리 공정의 소성 온도가 과도하게 낮은 경우, 제2 전극(150)과 후면 전계부(170) 사이의 접촉 저항이 증가할 수 있다.

<112> 따라서, 본 발명의 제1 실시예에서는 제2 전극(150)을 형성하는 제2 핑거 전극(151)과 제2 버스바(153) 모두가 후면 전계부(170) 내부로 함입되어, 후면 전계부(170) 중에 핑거 형성 영역(1700F)과 버스바 형성 영역(1700B) 모두에 금속 결정(MC)이 형성되는 경우를 일례로 설명하였으나, 효율을 보다 향상시키기 위해, 제2 핑거 전극(151)만 후면 전계부(170) 내부로 함입되고, 핑거 형성 영역(1700F)에만 금속 결정(MC)이 형성될 수도 있다. 이에 대해 보다 구체적으로 이하의 도 6 내지 도 8을 참조하여 설명한다.

<113> 도 6은 본 발명의 제2 실시예에 따른 태양 전지를 설명하기 위한 도이다.

<114> 도 6에 대한 설명에서는 앞선 제1 실시예에서 설명한 내용과 중복되는 부분에 대한 설명은 생략하고, 제1 실시예와 다른 부분을 위주로 설명한다.

<115> 도 6에 도시된 바와 같이, 본 발명의 제2 실시예에 따른 태양 전지는 제2 전극(150)의 적어도 일부가 후면 전계부(170) 내부로 함입되게 하되, 제2 전극(150) 중 복수의 제2 핑거 전극(151)만 후면 보호막(190)을 관통하여 후면 전계부(170) 내부로 함입되어 형성되도록 형성할 수 있다.

<116> 이때에는, 금속 결정(MC)이 후면 전계부(170)의 핑거 형성 영역(1700F)에만 형성되고, 복수의 제2 버스바(153)는 후면 전계부(170) 내부로 함입되지 않고, 후면 보호막(190)의 후면 위에 형성될 수 있다.

<117> 따라서, 후면 전계부(170) 중에서 버스바 형성 영역(1700B)에는 금속 결정(MC)이 형성되지 않을 수 있다.

<118> 이와 같이, 제2 전극(150) 중에서 복수의 제2 핑거 전극(151)만 후면 보호막(190)을 뚫고 후면 전계부(170) 내로 함입되도록 하여 후면 전계부(170) 중에서 핑거 형성 영역(170OF)에만 금속 결정(MC)이 형성되도록 하고, 제2 버스바(153)는 후면 보호막(190) 위에 형성되도록 하여 후면 전계부(170) 중에서 버스바 형성 영역(170OB)에는 금속 결정(MC)이 형성되지 않도록 하는 것은 앞선 도 3 내지 도 5에서 설명한 바와 같이, 금속 결정(MC)이 터널층(160) 내에 위치하지 않도록 하거나 터널층(160)을 뚫고 반도체 기판(110) 내에 접속되지 않도록 하기 위함이다.

<119> 보다 구체적으로 설명하면, 제2 버스바(153)의 경우, 앞선 도 1 및 도 2에서 설명한 바와 같이, 폭이 제2 핑거 전극(151)에 비하여 상대적으로 크기 때문에, 열처리 공정시 상대적으로 큰 길이나 폭을 갖는 금속 결정(MC)이 후면 전계부(170)에 형성되어, 도 5에 도시된 바와 같이, 금속 결정(MC)이 터널층(160) 내에 위치하거나 반도체 기판(110)과 접속될 수 있는데, 이를 사전에 차단하기 위함이다.

<120> 따라서, 본 발명의 제2 실시예에 따른 태양 전지는 제2 핑거 전극(151)과 제2 버스바(153) 중에서 제2 핑거 전극(151)만 후면 보호막(190)을 뚫고 후면 전계부(170) 내부로 함입되어 형성된 구조를 가지고 있으므로, 후면 전계부(170)의 제1 경계면(BS1)에서 후면 전계부(170)와 제2 핑거 전극(151)만 서로 접촉하고, 후면 전계부(170)의 전극 형성 영역(170OA) 중에서 제2 핑거 전극(151)이 형성되는 핑거 형성 영역(170OF)에만 복수의 금속 결정(MC)을 포함할 수 있고, 제2 버스바(153)와 중첩되는 후면 전계부(170)의 버스바 형성 영역(170OB)에는 복수의 금속 결정(MC)이 위치하지 않을 수 있다.

<121> 이를 위해, 본 발명은 복수의 제2 핑거 전극(151)에 포함되는 재질과 복수의 제2 버스바(153)에 포함되는 재질을 서로 다르게 할 수 있다.

<122> 보다 구체적으로, 제2 핑거 전극(151)이 후면 보호막(190)을 뚫고 후면 전계부(170) 내부로 함입되도록 하고, 제2 버스바(153)가 후면 보호막(190)을 뚫고 후면 전계부(170) 내부로 함입되는 것을 방지하거나 최소화하기 위하여, 복수의 제2 버스바(153)에 포함되는 단위 부피당 글래스 프릿의 함유량은 복수의 제2 핑거 전극(151)에 포함되는 단위 부피당 글래스 프릿의 함유량보다 작거나 없을 수 있다.

<123> 즉, 제2 버스바(153)를 형성하기 위한 제2 버스바 페이스트의 단위 부피당 글래스 프릿의 함유량을 제2 핑거 전극(151)을 형성하기 위한 제2 핑거 페이스트에 포함된 단위 부피당 글래스 프릿의 함유량보다 작게 하거나 글래스 프릿이 포함되지 않도록 할 수 있다.

<124> 이와 같이 하는 이유는, 제2 전극(150)을 형성하기 위한 열처리 공정에서, 제2 핑거 페이스트가 후면 보호막(190)을 뚫고 후면 전계부(170)로 함입되는 동안 제2 버스바 페이스트가 후면 보호막(190)을 뚫고 후면 전계부(170)에 접속되더라도 후면 전계부(170) 내부로 거의 함입되지 못하게 하거나, 아예 후면 보호막(190)을 뚫지 못하게 하기 위함이다.

<125> 이와 같이 함으로써, 후면 전계부(170)의 버스바 형성 영역(1700B)에 금속 결정(MC)이 형성되지 않도록 할 수 있고, 반도체 기판(110)이 열화되는 것을 방지할 수 있다.

<126> 아울러, 복수의 제2 핑거 전극(151)에 포함되는 단위 부피당 글래스 프릿의 함유량은 제1 전극(140)에 포함되는 단위 부피당 글래스 프릿의 함유량과 동일할 수 있다.

<127> 이는, 제1 전극(140)도 제1 전극 페이스트를 도포한 후, 반사 방지막(130)을 뚫고 에미터부(120)에 접속하여 형성될 수 있는데, 제2 핑거 페이스트에 포함된 단위 부피당 글래스 프릿의 함유량을 제1 전극(140)과 동일하게 함으로써, 동일한 열처리 공정에서 제1 전극 페이스트가 반사 방지막(130)을 뚫고 에미터부(120)로 함입되는 속도와 제2 핑거 페이스트가 후면 보호막(190)을 뚫고 후면 전계부(170)로 함입되는 속도를 서로 대략적으로 동일하게 할 수 있다.

<128> 이로 인하여, 제1 전극(140)과 제2 전극(150)을 형성하기 위한 열처리 공정의 온도를 서로 동일하게 하면서도, 제2 핑거 전극(151)의 속도를 제한할 수 있다.

<129> 또한, 복수의 제2 핑거 전극(151)에 포함되는 단위 부피당 금속 물질의 함유량은 복수의 제2 버스바(153)에 포함되는 단위 부피당 금속 물질의 함유량보다 많을 수 있다.

<130> 보다 구체적 일례로, 복수의 제2 핑거 전극(151)에 포함되는 단위 부피당 금속 물질의 함유량은 80wt%이상 95wt%이하이고, 복수의 제2 버스바(153)에 포함되는 단위 부피당 금속 물질의 함유량은 60wt%이상 80wt%이하일 수 있다.

<131> 이와 같이, 제2 핑거 전극(151)에 포함되는 단위 부피당 금속 물질의 함유량은 80wt%이상 95wt%이하로 하는 것은 제2 핑거 페이스트가 후면 보호막(190)을 뚫

고 후면 전계부(170) 내로 함입된 상태에서, 금속 결정(MC)이 앞선 도 3에서 설명한 바와 같이 충분히 형성되도록 하고, 상대적으로 폭이 좁은 제2 핑거 전극(151)의 저항을 충분히 낮추기 위함이다.

<132> 아울러, 제2 버스바(153)에 포함되는 단위 부피당 금속 물질의 함유량은 60wt%이상 80wt%이하가 되도록 함으로써, 제2 버스바 페이스트 중 일부가 후면 보호막(190)을 뚫고 후면 전계부(170)에 접속되더라도, 제2 버스바 페이스트에 포함된 금속 물질에 의해 후면 전계부(170)의 버스바 형성 영역(1700B)에 금속 결정(MC)이 형성되지 않도록 하거나, 금속 결정(MC)이 설사 형성된다 하더라도, 앞선 도 4에서 설명한 바와 같이, 금속 결정(MC)이 터널층(160) 내부에 형성되더라도 반도체 기판(110)에 접속되어 형성되지 않도록 방지할 수 있다.

<133> 아울러, 복수의 제2 핑거 전극(151)에 포함되는 단위 부피당 금속 물질의 함유량은 제1 전극(140)에 포함되는 단위 부피당 금속 물질의 함유량과 동일할 수 있다.

<134> 이와 같이 서로 다른 재질을 갖는 제2 핑거 전극(151)과 제2 버스바(153)를 형성함으로써, 반도체 기판(110)의 열화를 방지할 수 있고, 태양 전지의 효율이 저하되는 것을 보다 방지할 수 있다.

<135> 앞서 설명한 바와 같이, 반도체 기판(110)의 열화는 제2 전극(150)을 형성하기 위한 열처리 공정 중에 발생할 수 있고, 열처리 공정의 온도가 너무 낮으면 제2 전극(150)의 접촉 저항이 과도하게 높아져 태양 전지의 효율을 방지할 수 있다.

<136> 여기서, 반도체 기판(110)의 열화는 다음의 도 7과 도 8에서 확인할 수 있다.

<137> 도 7은 제2 버스바 패이스트(153P)의 재질이 제2 핑거 패이스트의 재질과 동일한 경우, 열처리 공정시 소성 온도에 따른 반도체 기판(110)의 열화 정도를 PL(photo luminescence) 촬영한 비교예 사진이고, 도 8은 본 발명의 제2 실시예에 따라 제2 버스바 패이스트(153P)의 재질과 제2 핑거 패이스트의 재질이 서로 다른 경우, 열처리 공정시 소성 온도에 따른 반도체 기판(110)의 열화 정도를 PL(photo luminescence) 촬영한 사진이다.

<138> 반도체 기판(110)의 개방 전압(Voc)를 보여주는 PL 이미지는 열처리 공정 온도에 따라 금속 결정(MC)이 반도체 기판(110)에 침투함에 따른 열화를 볼 수 있다.

<139> PL 이미지에서 반도체 기판(110)의 일부 영역이 어두워질수록 개방 전압이 감소하여 반도체 기판(110)의 열화가 심화되는 것을 의미하고, 밝아질수록 개방 전압이 충분한 상태로 높아 반도체 기판(110)의 열화가 작거나 거의 없는 것을 의미한다.

<140> 보다 구체적으로, PL 이미지에서 열처리 공정 온도가 증가함에 따라 음영 영역이 증가하는 경우, 금속 결정(MC)이 터널층(160)이나 반도체 기판(110)으로 침투하여 개방 전압이 감소하여 반도체 기판(110)의 열화가 심화되는 것을 의미하고, 열처리 공정 온도가 증가함에 따라 음영 영역이 증가하지 않는 경우, 금속 결정(MC)이 터널층(160)이나 반도체 기판(110)으로 침투하지 않아, 개방 전압이 충분히

높은 상태로 유지되어 반도체 기판(110)의 열화가 작거나 거의 없는 것을 의미한다.

<141> 도 7 및 도 8에서는 상대적으로 폭이 큰 제2 버스바(153)의 이미지만 보이고, 제2 핑거 전극(151)의 이미지는 폭이 너무 작아 보이지 않으나, 실질적으로 각각의 제2 버스바(153)에는 복수의 제2 핑거 전극(151)이 교차하여 형성된다.

<142> 도 7에서는 제2 핑거 페이스트와 동일한 재질의 제2 버스바 페이스트(153P)를 사용한 경우이고, 도 8은 앞선 도 6에서 설명한 바와 같이 제2 핑거 페이스트와 다른 재질의 제2 버스바 페이스트(153P)를 사용한 경우이다.

<143> 도 7에서는 제2 버스바(153)와 제2 핑거 전극(151)의 동일한 재질이 서로 동일하므로, 제2 버스바 페이스트(153P)도 후면 보호막(190)을 뚫고 후면 전계부(170)에 함입되어 형성되고, 후면 전계부(170)의 버스바 형성 영역(1700B) 내로 금속 결정(MC)이 형성될 수 있다.

<144> 따라서, 제2 전극(150)을 형성하기 위한 열처리 공정 온도가 도 7의 (c) 및 (d)와 같이, 820℃나 795℃ 정도로 상대적으로 낮은 경우, 후면 전계부(170) 내에 금속 결정(MC)이 거의 형성되지 않고, 반도체 기판(110)의 열화가 거의 발생하지 않으나, 이와 같은 경우, 제2 핑거 전극(151)의 접촉 저항이 상대적으로 높게 형성될 수 있어 태양 전지의 효율이 감소할 수 있다.

<145> 그러나, 제2 전극(150)을 형성하기 위한 열처리 공정 온도가 도 7의 (a) 및 (b)와 같이, 870℃나 845℃ 정도로 상대적으로 높은 경우, 반도체 기판(110)에 음

영 영역이 증가하고 상대적으로 심화되어, 제2 버스바 페이스트(153P)에 의해 형성된 후면 전계부(170)의 금속 결정(MC)이 터널층(160)이나 반도체 기판(110)으로 침투되어 반도체 기판(110)의 열화가 심화되는 것을 알 수 있다.

<146> 그러나, 앞선 도 6에서 설명한 바와 같이, 본 발명의 제2 실시예에 따라 제2 핑거 전극(151)과 제2 버스바(153)의 재질을 서로 다르게 한 경우, 열처리 공정 온도가 상대적으로 낮은 도 8의 (c) 및 (d)의 경우는 물론, 상대적으로 높은 도 8의 (a) 및 (b)에서도 반도체 기판(110)의 음영 영역이 거의 증가되지 않는 것을 확인할 수 있다.

<147> 이는, 제2 핑거 전극(151)과 제2 버스바(153)의 재질을 서로 다르게 함으로써, 제2 버스바(153)가 후면 보호막(190)을 뚫고 후면 전계부(170)에 접속되지 않거나, 접속되더라고 제2 버스바(153)에 의해 형성되는 후면 전계부(170)의 금속 결정(MC)이 터널층(160)이나 반도체 기판(110) 내로 침투하지 않기 때문이다.

<148> 이와 같이, 본 발명의 제2 실시예에 따른 태양 전지는 제2 핑거 전극(151)과 제2 버스바(153)의 재질을 서로 다르게 함으로써, 태양 전지의 개방 전압(Voc)을 충분히 높을 상태로 유지여 반도체 기판(110)의 열화를 방지하고, 태양 전지의 효율을 보다 향상시킬 수 있다.

<149> 이상에서 본 발명의 실시예에 대하여 상세하게 설명하였지만 본 발명의 권리범위는 이에 한정되는 것은 아니고 다음의 청구범위에서 정의하고 있는 본 발명의 기본 개념을 이용한 당업자의 여러 변형 및 개량 형태 또한 본 발명의 권리범위에 속하는 것이다.

【특허청구범위】

【청구항 1】

제1 도전성 타입의 불순물을 함유하는 반도체 기판;

상기 반도체 기판의 전면에 위치하고 상기 제1 도전성 타입과 반대인 제 2 도전성 타입의 불순물을 함유하는 에미터부;

상기 반도체 기판의 후면 위에 위치하고, 유전체 재질을 포함하는 터널층;

상기 터널층의 후면 위에 위치하고, 상기 제1 도전성 타입의 불순물이 상기 반도체 기판보다 고농도로 도핑된 다결정 실리콘 재질을 포함하는 후면 전계부;

상기 후면 전계부의 후면에 위치하며, 유전체 재질의 후면 보호막;

상기 에미터부와 연결되는 제1 전극; 및

상기 후면 전계부와 연결되는 제2 전극;을 포함하고,

상기 제2 전극의 적어도 일부는 상기 후면 전계부 내부로 함입되어 있는 태양 전지.

【청구항 2】

제1 항에 있어서,

상기 후면 전계부와 상기 제2 전극이 서로 접촉하는 제1 경계면은 상기 후면 전계부와 상기 후면 보호막이 서로 접촉하는 제2 경계면보다 상기 반도체 기판 방향으로 더 인접하여 위치하는 태양 전지.

【청구항 3】

제1 항에 있어서,

상기 후면 전계부 중에서 상기 제2 전극이 형성되는 전극 형성 영역에는 복수의 금속 결정을 더 포함하는 태양 전지.

【청구항 4】

제3 항에 있어서,

상기 금속 결정은 상기 후면 전계부 중에서 상기 제2 전극이 형성되지 않는 비형성 영역에는 위치하지 않는 태양 전지.

【청구항 5】

제3 항에 있어서,

상기 금속 결정은 상기 터널층 내에는 위치하지 않는 태양 전지.

【청구항 6】

제3 항에 있어서,

상기 복수의 금속 결정은 상기 제2 전극에 포함된 금속 물질과 동일한 금속 물질을 포함하는 태양 전지.

【청구항 7】

제3 항에 있어서,

상기 복수의 금속 결정의 중 일부는 상기 제2 전극과 직접 접촉되는 태양 전지.

【청구항 8】

제3 항에 있어서,

상기 복수의 금속 결정의 중 적어도 하나 이상은 상기 제2 전극과 이격되어 있는 태양 전지.

【청구항 9】

제3 항에 있어서,

상기 복수의 금속 결정은 상기 제2 전극으로부터 상기 터널층 방향으로의 길이가 상기 후면 전계부 두께의 2/3 이하인 태양 전지.

【청구항 10】

제3 항에 있어서,

상기 복수의 금속 결정 중 일부는 상기 제2 전극으로부터 상기 터널층 방향으로 진행할수록 폭이 감소하는 태양 전지.

【청구항 11】

제1 항에 있어서,

상기 제2 전극은 상기 후면 전계부의 후면에서 보았을 때, 제1 방향으로 길게 형성되는 복수의 제2 핑거 전극과, 상기 제1 방향과 교차하는 제2 방향으로 길게 형성되며, 상기 복수의 제2 핑거 전극이 공통으로 접속되는 제2 버스바를 포함하는 태양 전지.

【청구항 12】

제11 항에 있어서,

상기 복수의 제2 핑거 전극은 상기 후면 보호막을 관통하여 상기 후면 전계부 내부로 함입되어 형성되고,

상기 복수의 제2 버스바는 상기 후면 보호막의 후면 위에 형성되는 태양 전지.

【청구항 13】

제11 항에 있어서,

상기 후면 전계부의 상기 제1 경계면에서 상기 후면 전계부와 상기 제2 핑거 전극은 서로 접촉하고,

상기 후면 전계부의 전극 형성 영역 중에서 상기 제2 핑거 전극이 형성되는 핑거 형성 영역에는 복수의 금속 결정을 더 포함하는 태양 전지.

【청구항 14】

제11 항에 있어서,

상기 후면 전계부의 전극 형성 영역 중에서 상기 제2 버스바가 형성되는 버스바 형성 영역에는 상기 복수의 금속 결정이 위치하지 않는 태양 전지.

【청구항 15】

제11 항에 있어서,

상기 복수의 제2 핑거 전극에 포함되는 재질과 상기 복수의 제2 버스바에 포

함되는 재질은 서로 다른 태양 전지.

【청구항 16】

제11 항에 있어서,

상기 복수의 제2 버스바에 포함되는 단위 부피당 글래스 프릿의 함유량은 상기 복수의 제2 핑거 전극에 포함되는 단위 부피당 글래스 프릿의 함유량보다 작은 태양 전지.

【청구항 17】

제16 항에 있어서,

상기 복수의 제2 핑거 전극에 포함되는 단위 부피당 글래스 프릿의 함유량은 상기 제1 전극에 포함되는 단위 부피당 글래스 프릿의 함유량과 동일한 태양 전지.

【청구항 18】

제11 항에 있어서,

상기 복수의 제2 핑거 전극에 포함되는 단위 부피당 금속 물질의 함유량은 상기 복수의 제2 버스바에 포함되는 단위 부피당 금속 물질의 함유량보다 많은 태양 전지.

【청구항 19】

제18 항에 있어서,

상기 복수의 제2 핑거 전극에 포함되는 단위 부피당 금속 물질의 함유량은 80wt%이상 95wt%이하이고,

상기 복수의 제2 버스바에 포함되는 단위 부피당 금속 물질의 함유량은 60wt%이상 80wt%이하인 태양 전지.

【청구항 20】

제18 항에 있어서,

상기 복수의 제2 핑거 전극에 포함되는 단위 부피당 금속 물질의 함유량은 상기 제1 전극에 포함되는 단위 부피당 금속 물질의 함유량과 동일한 태양 전지.

【요약서】

【요약】

본 발명은 태양 전지에 관한 것이다.

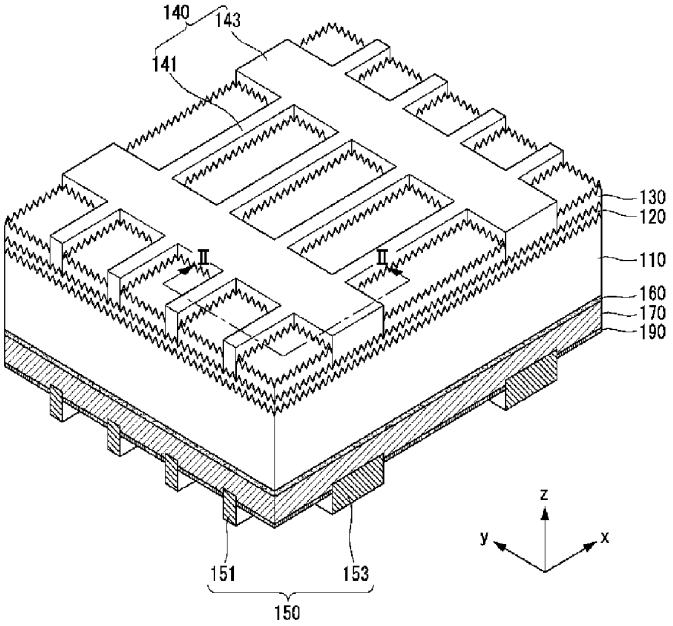
본 발명의 일례에 따른 태양 전지는 제1 도전성 타입의 불순물을 함유하는 반도체 기판; 반도체 기판의 전면에 위치하고 제1 도전성 타입과 반대인 제 2 도전성 타입의 불순물을 함유하는 에미터부; 반도체 기판의 후면 위에 위치하고, 유전체 재질을 포함하는 터널층; 터널층의 후면 위에 위치하고, 제1 도전성 타입의 불순물이 반도체 기판보다 고농도로 도핑된 다결정 실리콘 재질을 포함하는 후면 전계부; 후면 전계부의 후면에 위치하며, 유전체 재질의 후면 보호막; 에미터부와 연결되는 제1 전극; 및 후면 전계부와 연결되는 제2 전극;을 포함하고, 제2 전극의 적어도 일부는 후면 전계부 내부로 함입된다.

【대표도】

도 1

【도면】

【도 1】



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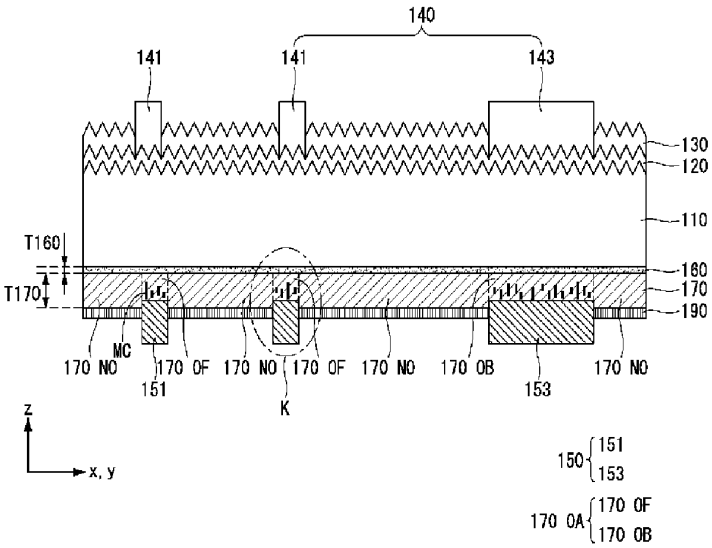
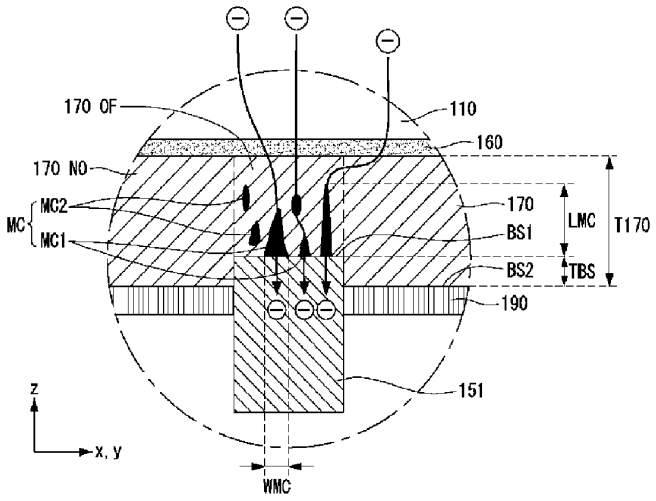

140
141
141
143
130
120
110
T160
160
T170
170
190
MC
170 NO
170 OF
170 NO
170 OF
170 NO
170 OB
170 NO
151
K
153
z
x, y
150
151
153
170 OA
170 OF
170 OB

【도 3】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160
170 NO
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MC2
MC1
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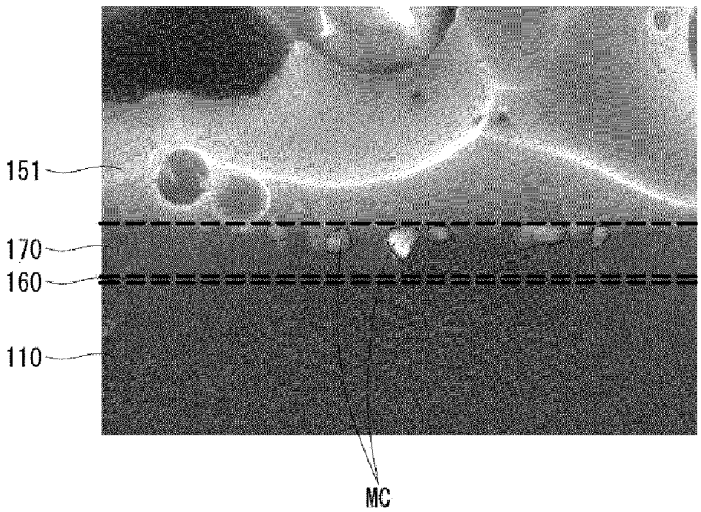
BS1
BS2
LMC
TBS
T170
190
151
z
x, y
WMC

【도 4】



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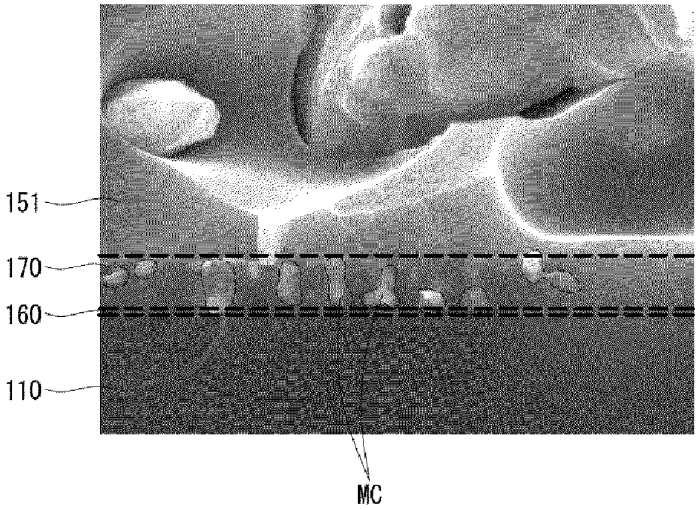
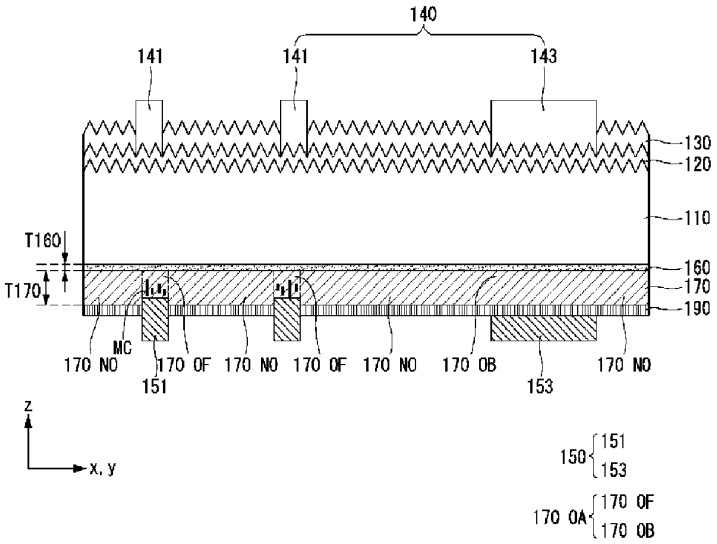


【도 6】


140
141
141
143
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120
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T160
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T170
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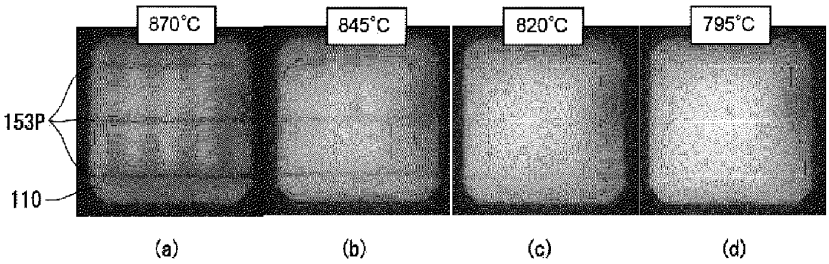
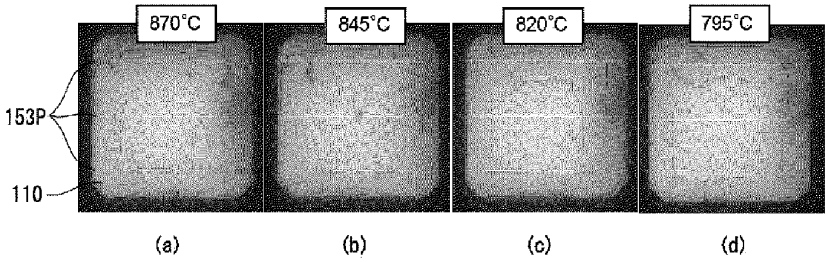
190
MC
170 NO
170 OF
170 NO
170 OF
170 NO
170 OB
170 NO
151
153
z
x, y
150
151
153
170 OA
170 OF
170 OB

【도 7】


870°C
845°C
820°C
795°C
153P
110
(a)
(b)
(c)
(d)

【도 8】



대 한 민 국 특 허 청
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2017년 07월 18일

특 허 청 장
COMMISSIONER

【서지사항】

【서류명】 특허출원서

【참조번호】 01

【출원구분】 특허출원

【출원인】

【명칭】 엘지전자 주식회사

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【대리인번호】 9-1998-000238-3

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【발명의 국문명칭】 태양 전지 및 이의 제조 방법

【발명의 영문명칭】 SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME

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【취지】 위와 같이 특허청장에게 제출합니다.

대리인 박병창 (서명 또는 인)

【수수료】

【출원료】	0	면	46,000	원
【가산출원료】	50	면	0	원
【우선권주장료】	0	건	0	원
【심사청구료】	20	항	1,023,000	원

【합계】 1,069,000 원

【수수료 자동납부번호】 301-0128-1620-71

【발명의 설명】

【발명의 명칭】

태양 전지 및 이의 제조 방법{SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME}

【기술분야】

<1> 본 발명은 태양 전지 및 이의 제조 방법에 관한 것으로서, 좀더 상세하게는, 반도체 기판을 포함하는 태양 전지 및 이의 제조 방법에 관한 것이다.

【배경기술】

<2> 최근 석유나 석탄과 같은 기존 에너지 자원의 고갈이 예상되면서 이들을 대체할 대체 에너지에 대한 관심이 높아지고 있다. 그 중에서도 태양 전지는 태양광 에너지를 전기 에너지로 변환시키는 차세대 전지로서 각광받고 있다.

<3> 이러한 태양 전지는 다양한 층 및 전극을 설계에 따라 형성하는 것에 의하여 제조될 수 있다. 태양 전지에서는 다양한 층 및 전극의 설계에 따라 효율이 달라질 수 있다. 태양 전지의 상용화를 위해서는 태양 전지의 효율을 최대화하고 제조 방법을 단순화하는 것이 요구된다.

【발명의 내용】

【해결하려는 과제】

<4> 본 발명은 높은 효율 및 생산성을 가지는 태양 전지 및 이의 제조 방법을 제공하고자 한다.

【과제의 해결 수단】

<5> 본 발명의 실시예에 따른 태양 전지는, 반도체 기판의 일면 위에 위치하는 터널링층; 상기 터널링층 위에 위치하는 제1 도전형 영역; 상기 제1 도전형 영역 위에서 상기 제1 도전형 영역을 패시베이션하는 제1 절연막; 상기 반도체 기판의 타면 쪽에 위치하며 도핑 영역으로 구성되는 제2 도전형 영역; 상기 제1 도전형 영역에 연결되는 제1 전극; 및 상기 제2 도전형 영역에 연결되는 제2 전극을 포함한다. 상기 반도체 기판의 일면의 가장자리 부분에 상기 터널링층 및 상기 제1 도전형 영역이 위치하지 않는 아이솔레이션부가 위치한다. 상기 제1 절연막이 상기 아이솔레이션부가 위치하는 상기 반도체 기판의 일면 위를 덮는다.

<6> 본 발명의 실시예에 따른 태양 전지의 제조 방법은, 반도체 기판의 일면 및 타면 위에 각기 터널링층을 형성하는 단계; 상기 반도체 기판의 양측에서 각기 상기 터널링층 위에 진성 반도체층을 형성하는 단계; 적어도 상기 반도체 기판의 일측에 위치하는 상기 진성 반도체층의 부분에 제1 도전형 도펀트를 도핑하여 제1 도전형 영역을 형성하는 단계; 적어도 상기 반도체 기판의 타측에 위치한 상기 터널링층 및 상기 진성 반도체층 또는 상기 제1 도전형 영역을 전체적으로 제거하는 단계; 상기 반도체 기판의 타측에 제2 도전형 도펀트를 도핑하여 도핑 영역으로 구성되는 제2 도전형 영역을 형성하는 단계; 상기 제1 도전형 영역을 덮는 제1 절연막을 형성하는 단계; 및 상기 제1 도전형 영역에 연결되는 제1 전극 및 상기 제2 도전형 영역에 연결되는 제2 전극을 포함하는 전극을 형성하는 단계를 포함한다. 상기 제거하는 단계에서 상기 반도체 기판의 일측에 위치한 상기 터널링층 및 상기

제1 도전형 영역의 가장자리 부분을 함께 제거하여 아이솔레이션부를 형성한다. 상기 제1 절연막이 상기 아이솔레이션부가 위치하는 상기 반도체 기판의 일측 위를 덮는다.

【발명의 효과】

<7> 본 발명의 실시예에 따르면, 반도체 기판의 후면에 아이솔레이션부를 형성하여 제1 도전형 영역과 제2 도전형 영역이 불필요하게 서로 연결되는 것을 효과적으로 방지할 수 있다. 그리고 터널링층 및 제1 도전형 영역이 제거되어 형성된 아이솔레이션부가 위치하는 반도체 기판의 표면은 제1 도전형 영역을 덮는 제1 절연막에 의하여 덮여서 패시베이션될 수 있다. 이에 의하여 간단한 구조 및 공정에 의하여 아이솔레이션부를 패시베이션하여 표면 재결합 등에 의한 문제를 최소화할 수 있다. 즉, 간단한 구조 및 공정에 의하여 태양 전지의 효율 및 신뢰성을 향상할 수 있으며 불량률을 낮춰 생산성을 향상할 수 있다.

【도면의 간단한 설명】

<8> 도 1은 본 발명의 일 실시예에 따른 태양 전지를 도시한 단면도이다.

도 2는 도 1에 도시한 태양 전지의 개략적인 후면 평면도이다.

도 3은 본 발명의 일 변형예에 따른 태양 전지를 도시한 단면도이다.

도 4a 내지 도 4j는 본 발명의 일 실시예에 따른 태양 전지의 제조 방법을 도시한 단면도들이다.

도 5는 본 발명의 일 변형예에 따른 따른 태양 전지의 제조 방법의 일 공정

을 도시한 단면도들이다.

도 6은 본 발명의 다른 변형에에 따른 따른 태양 전지의 제조 방법의 일 공정을 도시한 단면도들이다.

【발명을 실시하기 위한 구체적인 내용】

<9> 이하에서는 첨부한 도면을 참조하여 본 발명의 실시예를 상세하게 설명한다. 그러나 본 발명이 이러한 실시예에 한정되는 것은 아니며 다양한 형태로 변형될 수 있음은 물론이다.

<10> 도면에서는 본 발명을 명확하고 간략하게 설명하기 위하여 설명과 관계 없는 부분의 도시를 생략하였으며, 명세서 전체를 통하여 동일 또는 극히 유사한 부분에 대해서는 동일한 도면 참조부호를 사용한다. 그리고 도면에서는 설명을 좀더 명확하게 하기 위하여 두께, 넓이 등을 확대 또는 축소하여 도시하였는바, 본 발명의 두께, 넓이 등은 도면에 도시된 바에 한정되지 않는다.

<11> 그리고 명세서 전체에서 어떠한 부분이 다른 부분을 "포함"한다고 할 때, 특별히 반대되는 기재가 없는 한 다른 부분을 배제하는 것이 아니며 다른 부분을 더 포함할 수 있다. 또한, 층, 막, 영역, 판 등의 부분이 다른 부분 "위에" 있다고 할 때, 이는 다른 부분 "바로 위에" 있는 경우뿐 아니라 그 중간에 다른 부분이 위치하는 경우도 포함한다. 층, 막, 영역, 판 등의 부분이 다른 부분 "바로 위에" 있다고 할 때에는 중간에 다른 부분이 위치하지 않는 것을 의미한다. 그리고 "제1", "제2" 등의 표현은 서로 간의 구별을 위하여 사용한 것일 뿐 본 발명이 이에 한정되

는 것은 아니다.

<12> 이하, 첨부한 도면을 참조하여 본 발명의 실시예에 따른 태양 전지 및 이의 제조 방법을 상세하게 설명한다.

<13> 도 1은 본 발명의 일 실시예에 따른 태양 전지를 도시한 단면도이고, 도 2는 도 1에 도시한 태양 전지의 개략적인 후면 평면도이다.

<14> 도 1을 참조하면, 태양 전지(100)는, 반도체 기판(110)과, 반도체 기판(110)의 일면 쪽에 위치하며 제1 도전형을 가지는 제1 도전형 영역(20)과, 반도체 기판(110)의 타면 쪽에 위치하며 제2 도전형을 가지는 제2 도전형 영역(30)을 포함할 수 있다. 전극(42, 44)은 제1 도전형 영역(20)에 연결되는 제1 전극(42)과, 제2 도전형 영역(30)에 연결되는 제2 전극(44)을 포함한다. 그리고 태양 전지(100)는, 제1 패시베이션막(24), 제2 패시베이션막(34), 반사 방지막(36)과 같은 절연막을 더 포함할 수 있다. 이를 상세하게 설명한다.

<15> 반도체 기판(110)은 단일 반도체 물질(일 예로, 4족 원소)를 포함하는 결정질 반도체로 구성될 수 있다. 일 예로, 반도체 기판(110)은 단결정 또는 다결정 반도체(일 예로, 단결정 또는 다결정 실리콘)로 구성될 수 있다. 특히, 반도체 기판(110)은 단결정 반도체(예를 들어, 단결정 반도체 웨이퍼, 좀더 구체적으로는, 단결정 실리콘 웨이퍼)로 구성될 수 있다. 이와 같이 반도체 기판(110)이 단결정 반도체(예를 들어, 단결정 실리콘)로 구성되면, 태양 전지(100)가 결정성이 높아 결함이 적은 단결정 반도체로 구성되는 반도체 기판(110)을 기반으로 하게 된다. 이에 따라 태양 전지(100)가 우수한 전기적 특성을 가질 수 있다.

<16> 반도체 기판(110)의 전면 및/또는 후면은 텍스쳐링(texturing)되어 요철을 가질 수 있다. 요철은, 일 예로, 외면이 반도체 기판(110)의 (111)면으로 구성되며 불규칙한 크기를 가지는 피라미드 형상을 가질 수 있다. 텍스쳐링에 의해 반도체 기판(110)의 전면 등에 요철이 형성되어 전면의 표면 거칠기가 증가되면, 반도체 기판(110)의 전면 등을 통하여 입사되는 광의 반사율을 낮출 수 있다. 따라서 베이스 영역(10)과 제1 또는 제2 도전형 영역(20, 30)에 의하여 형성된 pn 접합까지 도달하는 광량을 증가시킬 수 있어, 광 손실을 최소화할 수 있다. 본 실시예에서는 요철이 반도체 기판(110)의 전면 및 후면에 요철이 형성되어 양면으로 입사되는 광의 반사를 효과적으로 방지하는 것을 예시하였다.

<17> 그러나 본 발명이 이에 한정되는 것은 아니다. 따라서, 도 3에 도시한 바와 같이, 반도체 기판(110)의 전면에만 요철이 형성되고 반도체 기판(110)의 후면에는 요철이 형성되지 않을 않을 수도 있다. 이에 의하면 터널링층(22)이 형성되는 반도체 기판(110)의 후면을 전면보다 작은 표면 거칠기를 가지도록 형성하여, 터널링층(22)이 좀더 안정적이고 균일하게 형성될 수 있다. 또는, 반도체 기판(110)의 전면 및 후면에 요철이 형성되지 않는 등 다양한 변형이 가능하다.

<18> 다시 도 1을 참조하면, 본 실시예에서 반도체 기판(110)은 제1 또는 제2 도전형 도펀트가 낮은 도핑 농도로 도핑되어 제1 또는 제2 도전형을 가지는 베이스 영역(10)을 포함한다. 이때, 반도체 기판(110)의 베이스 영역(10)은 이와 동일한 도전형을 가지는 제1 및 제2 도전형 영역(20, 30) 중 하나보다 낮은 도핑 농도, 높은 저항 또는 낮은 캐리어 농도를 가질 수 있다.

<19> 반도체 기판(110)의 일면(일 예로, 후면) 위에 제1 도전형을 가지는 제1 도전형 영역(20)이 위치할 수 있다. 일 예로, 반도체 기판(110) 위에 터널링층(22)이 형성되고, 터널링층(22) 위에 제1 도전형 영역(20)이 형성될 수 있다.

<20> 일 예로, 터널링층(22)은 반도체 기판(110)의 후면에 접촉 형성되어 구조를 단순화하고 터널링 효과를 향상할 수 있다. 이때, 터널링층(22)은 반도체 기판(110)의 후면에서 아이솔레이션부(I)를 제외한 부분에 전체적으로 형성될 수 있다. 여기서 전체적으로 형성되었다 함은 빈틈 없이 모두 형성된 것뿐 아니라 불가피하게 일부 영역이 형성되지 않는 것도 포함한다. 이에 의하여 별도의 패터닝 공정이 요구되지 않아 터널링층(22)을 쉽게 형성할 수 있다. 그러나 본 발명이 이에 한정되는 것은 아니다.

<21> 터널링층(22)은 전자 및 정공에게 일종의 배리어(barrier)로 작용하여, 소수 캐리어(minority carrier)가 통과되지 않도록 하고, 터널링층(22)에 인접한 부분에서 축적된 후에 일정 이상의 에너지를 가지는 다수 캐리어(majority carrier)만이 터널링층(22)을 통과할 수 있도록 한다. 이때, 일정 이상의 에너지를 가지는 다수 캐리어는 터널링 효과에 의하여 쉽게 터널링층(22)을 통과할 수 있다. 또한, 터널링층(22)은 제1 도전형 영역(20)의 도펀트가 반도체 기판(110)으로 확산하는 것을 방지하는 확산 배리어로서의 역할을 수행할 수 있다. 이러한 터널링층(22)은 다수 캐리어가 터널링 될 수 있는 다양한 물질을 포함할 수 있는데, 일례로, 산화물, 질화물, 반도체, 전도성 고분자 등을 포함할 수 있다. 특히, 터널링층(22)이 실리콘 산화물을 포함하는 실리콘 산화물층으로 구성될 수 있다. 실리콘 산화물층은 패시

베이션 특성이 우수하며 캐리어가 터널링되기 쉬운 막이기 때문이다.

<22> 터널링 효과를 충분하게 구현할 수 있도록 터널링층(22)의 두께가 제1 및 제2 패시베이션막(24, 34), 제1 또는 제2 도전형 영역(20, 30)의 두께보다 작을 수 있다. 일 예로, 터널링층(22)의 두께가 2nm 이하일 수 있고, 일 예로, 0.1nm 내지 1.5nm(좀더 구체적으로는, 0.5nm 내지 1.5nm)일 수 있다. 터널링층(22)의 두께가 2nm를 초과하면 터널링이 원할하게 일어나지 않아 태양 전지(100)의 효율이 저하될 수 있고, 터널링층(22)의 두께가 0.1nm 미만이면 원하는 품질의 터널링층(22)을 형성하기에 어려움이 있을 수 있다. 충분한 터널링 효과를 위해서는 터널링층(22)의 두께가 0.1nm 내지 1.5nm(좀더 구체적으로 0.5nm 내지 1.5nm)일 수 있다. 그러나 본 발명이 이에 한정되는 것은 아니며 터널링층(22)의 두께가 다양한 값을 가질 수 있다.

<23> 제1 도전형 영역(20)은 제1 도전형 도펀트를 포함하여 제1 도전형을 가지는 영역일 수 있다. 일 예로, 제1 도전형 영역(20)은 터널링층(22)에 접촉하여 형성되어 태양 전지(100)의 구조가 단순화되고 터널링층(22)의 터널링 효과가 최대화될 수 있다. 그러나 본 발명이 이에 한정되는 것은 아니다.

<24> 제1 도전형 영역(20)은 반도체 기판(110)과 동일한 반도체 물질(좀더 구체적으로, 단일 반도체 물질, 일례로, 실리콘)을 포함할 수 있다. 그러면, 제2 도전형 영역(30)이 반도체 기판(110)과 유사한 특성을 가져 서로 다른 반도체 물질을 포함할 경우에 발생할 수 있는 특성 차이를 최소화할 수 있다. 다만, 제1 도전형 영역(20)이 반도체 기판(110) 위에서 반도체 기판(110)과 별개로 형성되므로, 반도체

기판(110) 위에서 쉽게 형성될 수 있도록 제1 도전형 영역(20)이 반도체 기판(110)과 다른 결정 구조를 가질 수 있다.

<25> 예를 들어, 제1 도전형 영역(20)은 증착 등의 다양한 방법에 의하여 쉽게 제조될 수 있는 비정질 반도체, 미세 결정 반도체, 또는 다결정 반도체(일 예로, 비정질 실리콘, 미세 결정 실리콘, 또는 다결정 실리콘) 등에 제1 도전형 도펀트를 도핑하여 형성될 수 있다. 특히, 제1 도전형 영역(20)은 다결정 반도체(일 예로, 다결정 실리콘)을 포함할 수 있다. 그러면 우수한 전기 전도도를 가져 캐리어의 이동을 원활하게 할 수 있고, 산화물 등으로 구성된 터널링층(22)에서 캐리어의 터널링이 원활하게 일어나도록 유도할 수 있다.

<26> 본 실시예에서 제1 도전형 영역(20)을 반도체 기판(110)과 별개로 형성하여 반도체 기판(110) 내부에 도핑 영역 형성 시에 발생할 수 있는 결함 또는 개방 전압 저하의 문제를 저감할 수 있다. 이에 의하여 태양 전지(100)의 개방 전압을 향상할 수 있다.

<27> 반도체 기판(110)의 다른 일면(일 예로, 전면) 쪽에 제2 도전형을 가지는 제2 도전형 영역(30)이 위치할 수 있다. 일 예로, 본 실시예에서는 제2 도전형 영역(30)이 반도체 기판(110)의 일부에 제2 도전형 도펀트가 도핑되어 형성된 도핑 영역으로 구성될 수 있다. 그러면, 베이스 영역(10)과 제2 도전형 영역(30)은 반도체 기판(110)과 동일한 결정 구조 및 반도체 물질을 포함하면서 도전형이 서로 다르거나 또는 도핑 농도가 서로 다를 수 있다. 구체적으로, 베이스 영역(10)이 제1 도전형을 가지는 경우에는 베이스 영역(10)과 제2 도전형 영역(30)의 도전형이 서로 다

르고, 베이스 영역(10)이 제2 도전형을 가지는 경우에는 제2 도전형 영역(30)의 도핑 농도가 베이스 영역(10)의 도핑 농도보다 높다.

<28> 베이스 영역(10)이 제1 도전형을 가지게 되면, 제1 도전형을 가지는 제1 도전형 영역(20)이 반도체 기판(110)과 동일한 도전형을 가지면서 반도체 기판(110)보다 높은 도핑 농도를 가지는 후면 전계(back surface field, BSF)를 형성하는 후면 전계 영역을 구성하고, 제2 도전형을 가지는 제2 도전형 영역(30)이 베이스 영역(10)과 다른 도전형을 가져 베이스 영역(10)과 pn 접합을 형성하는 에미터 영역을 구성한다. 그러면, 반도체 기판(110)의 전면 쪽에 에미터 영역을 구성하는 제2 도전형 영역(30)이 위치하여 pn 접합에 접합하는 광의 경로를 최소화할 수 있다.

<29> 그러나 본 발명이 이에 한정되는 것은 아니다. 다른 예로, 베이스 영역(10)이 제2 도전형을 가지게 되면, 제1 도전형 영역(20)이 에미터 영역을 구성하고 제2 도전형 영역(30)이 반도체 기판(110)과 동일한 도전형을 가지면서 반도체 기판(110)보다 높은 도핑 농도를 가지는 전면 전계(front surface field, FSF)를 형성하는 전면 전계 영역을 구성한다.

<30> 제1 또는 제2 도전형 도펀트로 사용되는 p형 도펀트로는 보론(B), 알루미늄(Al), 갈륨(Ga), 인듐(In) 등의 3족 원소를 들 수 있고, n형 도펀트로는 인(P), 비소(As), 비스무스(Bi), 안티몬(Sb) 등의 5족 원소를 들 수 있다. 그러나 본 발명이 이에 한정되는 것은 아니며 다양한 도펀트가 제1 또는 제2 도전형 도펀트로 사용될 수 있다.

<31> 여기서, 본 실시예에서는 반도체 기판(110)과 별개로 형성되는 제1 도전형

영역(20)이 반도체 기판(110)의 후면 쪽에 위치하고, 반도체 기판(110)의 일부를 구성하는 제2 도전형 영역(30)이 반도체 기판(110)의 전면 쪽에 위치한다. 반도체 기판(110)과 다른 결정 구조를 가지는 제1 도전형 영역(20)이 반도체 기판(110)의 전면 쪽에 위치하면 제1 도전형 영역(20)에서의 광 흡수가 증가되어 pn 접합에 도달하는 광량이 저하될 수 있으므로, 제1 도전형 영역(20)을 반도체 기판(110)의 후면 쪽에 위치시킨 것이다. 그러나 본 발명이 이에 한정되는 것은 아니다.

<32> 제1 및 제2 도전형 영역(20, 30) 위에는 제1 및 제2 전극(42, 44)에 대응하는 개구부(102, 104)를 제외하고 절연막이 전체적으로 형성될 수 있다. 이러한 절연막은 별도로 도펀트를 포함하지 않는 언도프트 절연막으로 구성될 수 있다.

<33> 구체적으로, 제1 도전형 영역(20) 위에는 개구부(102)를 제외한 부분에 제1 절연막이 전체적으로 형성(일 예로, 접촉)될 수 있고, 제2 도전형 영역(30) 위에는 개구부(104)를 제외한 부분에 제2 절연막이 전체적으로 형성(일 예로, 접촉)될 수 있다. 본 실시예에서는 제1 절연막으로 제1 도전형 영역(20) 위에 형성(일 예로, 접촉)하는 제1 패시베이션막(24)을 사용하고, 제2 절연막으로 제2 도전형 영역(30) 위에 형성(일 예로, 접촉하는) 제2 패시베이션막(34) 및 이 위에 형성(일 예로, 접촉)하는 반사 방지막(36)을 사용하는 것을 예시하였다. 그러나 본 발명이 이에 한정되는 것은 아니며 절연막은 원하는 기능에 따라 다양한 배치를 가질 수 있다.

<34> 패시베이션막(24, 34)은 도전형 영역(20, 30)에 접촉하여 형성되어 도전형 영역(20, 30)의 표면 또는 벌크 내에 존재하는 결함을 부동화 시킨다. 이에 의하여 소수 캐리어의 재결합 사이트를 제거하여 태양 전지(100)의 개방 전압(Voc)을 증가

시킬 수 있다. 반사 방지막(36)은 반도체 기판(110)의 전면으로 입사되는 광의 반사율을 감소시킨다. 이에 의하여 반도체 기판(110)의 전면을 통해 입사되는 광의 반사율이 낮추는 것에 의하여 베이스 영역(10)과 제1 도전형 영역(20)의 계면에 형성된 pn 접합까지 도달되는 광량을 증가시킬 수 있다. 이에 따라 태양 전지(100)의 단락 전류(Isc)를 증가시킬 수 있다. 이와 같이 패시베이션막(24, 34) 및 반사 방지막(36)에 의해 태양 전지(100)의 개방 전압과 단락 전류를 증가시켜 태양 전지(100)의 효율을 향상할 수 있다.

<35> 일례로, 패시베이션막(24, 34) 또는 반사 방지막(36)은 실리콘 질화막, 수소를 포함한 실리콘 질화막, 실리콘 산화막, 실리콘 산화 질화막, 알루미늄 산화막, MgF_2, ZnS, TiO_2 및 CeO_2로 이루어진 군에서 선택된 어느 하나의 단일막 또는 2개 이상의 막이 조합된 다층막 구조를 가질 수 있다. 일 예로, 패시베이션막(24, 34)은, 도전형 영역(20, 30)이 n형을 가지는 경우에는 고정 양전하를 가지는 실리콘 산화막, 실리콘 질화막 등을 포함할 수 있으며, p형을 가지는 경우에는 고정 음전하를 가지는 알루미늄 산화막 등을 포함할 수 있다. 일 예로, 반사 방지막(36)은 실리콘 질화물을 포함할 수 있다. 그러나 본 발명이 이에 한정되는 것은 아니며 패시베이션막(24, 34), 그리고 반사 방지막(36)이 다양한 물질을 포함할 수 있다.

<36> 제1 전극(42)은 제1 도전형 영역(20) 위에 위치(일 예로, 접촉)하여 제1 도전형 영역(20)에 전기적으로 연결된다. 제1 전극(42)은 제1 패시베이션막(24)에 형성된 개구부(102)를 통하여(즉, 제1 패시베이션막(24)을 관통하여) 제1 도전형 영

역(20)에 전기적으로 연결될 수 있다. 이와 유사하게 제2 전극(44)은 제2 도전형 영역(30) 위에 위치(일 예로, 접촉)하여 제2 도전형 영역(30)에 전기적으로 연결된다. 제2 전극(44)은 제2 패시베이션막(34) 및 반사 방지막(36)에 형성된 개구부(104)를 통하여(즉, 제2 패시베이션막(34) 및 반사 방지막(36)을 관통하여) 제1 도전형 영역(20)에 전기적으로 연결될 수 있다. 이러한 제1 및 제2 전극(42, 44)은 다양한 물질(좀더 구체적으로, 금속)을 포함하고 다양한 형상을 가질 수 있다. 제1 및 제2 전극(42, 44)의 형상에 대해서는 추후에 도 2를 참조하여 상세하게 설명한다.

<37> 반도체 기판(110)의 후면 위에 위치한 터널링층(22) 및 제1 도전형 영역(20)은 반도체 기판(110)의 후면의 가장자리(또는 반도체 기판(110)의 측면)과 일정한 제1 거리(D1)만큼 이격되어 위치한다. 이에 따라 터널링층(22) 및 제1 도전형 영역(20) 각각의 면적은 반도체 기판(110)의 면적보다 작을 수 있다. 여기서 제1 거리(D1)는 터널링층(22) 및 제1 도전형 영역(20)은 반도체 기판(110)의 후면의 가장자리 사이의 거리 중 가장 짧은 거리를 의미할 수 있다.

<38> 즉, 반도체 기판(110)의 후면의 가장자리에는 터널링층(22) 및 제1 도전형 영역(20)(이와 함께, 제1 도전형 영역(20)에 연결되는 제1 전극(42))이 형성되지 않는 아이솔레이션부(I)가 위치할 수 있다. 아잇올레이션부(I)는 반도체 기판(110)의 후면의 가장자리로부터 제1 도전형 영역(20)을 이격시켜 에지 아이솔레이션(edge isolation)의 역할을 할 수 있다. 즉, 제2 도전형 영역(30)의 형성 시에 제2 도전형 도펀트가 반도체 기판(110)의 측면 또는 후면의 가장자리까지 확산되어 반

도체 기판(110)의 측면 또는 후면의 가장자리에서 제1 도전형 영역(20)과 제2 도전형 영역(30)이 원하지 않게 단락될 수 있는데, 본 실시예에서는 반도체 기판(110)의 후면 가장자리에서 제1 도전형 영역(20)을 제거하여 이러한 문제를 원천적으로 방지할 수 있다. 그리고 반도체 기판(110)의 전면에 위치하는 제2 도전형 영역(30)은 반도체 기판(110)의 전면에서 전체적으로 형성할 수 있어, 제2 도전형 영역(30)의 면적을 최대화할 수 있다.

<39> 아이솔레이션부(I)는, 도 2에 도시한 바와 같이, 반도체 기판(110)의 후면 가장자리 전체를 따라 형성되어 폐쇄된 형상(closed shape)를 가질 수 있다. 그리고 아이솔레이션부(I)와 터널링층(22) 및 제1 도전형 영역(20)이 형성된 부분 사이에는 일정한 단차가 존재하게 된다.

<40> 일 예로, 제1 거리(D1)(즉, 아이솔레이션부(I)의 폭)이 1mm 이하일 수 있다. 제1 거리(D1)가 1mm를 초과하면, 제1 도전형 영역(20)의 면적이 작아져서 효율이 저하될 수 있다. 일 예로, 제1 거리(D1)가 1nm 내지 1mm 일 수 있다. 제1 거리(D1)가 1mm 미만이면, 아이솔레이션부(I)에 의한 효과가 충분하지 않을 수 있다. 그러나 본 발명이 이에 한정되는 것은 아니며 반도체 기판(110)의 크기 등에 따라 상술한 제1 거리(D1)가 다른 값을 가질 수도 있다.

<41> 제1 도전형 영역(20)은 반도체 기판(110)으로부터 멀어질수록 면적이 작아지는 형상을 가질 수 있다. 이때, 제1 도전형 영역(20)은 반도체 기판(110)으로부터 멀어질수록 면적이 작아지도록 측면이 반도체 기판(110)과 수직이 되지 않도록(일 예로, 대략적으로 경사지게) 형성될 수 있다. 일 예로, 제1 도전형 영역(20)은 반

도체 기판(110)으로부터 멀어질수록 면적이 작아지면서 측면이 라운드지게 형성될 수 있다. 터널링층(22)의 측면은 제1 도전형 영역(20)의 측면과 연장되도록 위치할 수 있으며, 제1 도전형 영역(20)과 유사하게 라운드진 형상을 가질 수 있다. 이는 제1 도전형 영역(20)과 터널링층(22)을 제거하여 아이솔레이션부(I)를 형성하는 공정에서 습식 공정 등을 사용하였기 때문인데, 이에 대해서는 후술한다. 그러나 제1 도전형 영역(20) 및 터널링층(22)의 측면 형상 등은 이 외에도 다양한 형상을 가질 수도 있다.

<42> 그리고 반도체 기판(110)의 후면 쪽에 위치한 제1 절연막(즉, 제1 패시베이션막(24))은 터널링층(22) 및 제1 도전형 영역(20)이 있는 부분에서는 제1 도전형 영역(20) 위에 위치하고, 아이솔레이션부(I)에서는 반도체 기판(110)의 후면 위에 위치(좀더 구체적으로는, 접촉)한다. 즉, 제1 패시베이션막(24)은 반도체 기판(110)의 가장자리 부근에서 반도체 기판(110)의 후면에 접촉하여 형성되고, 이로부터 연장되어 터널링층(22) 및 제1 도전형 영역(20)의 측면들을 덮으면서 이들과 접촉하여 형성되고, 이로부터 연장되어 제1 도전형 영역(20)의 상부면을 덮으면서 이들과 접촉하여 형성된다.

<43> 본 실시예에서는 태양 전지(100)의 제조 공정 중에 반도체 기판(110)의 후면의 가장자리에 위치한 터널링층(22) 및 제1 도전형 영역(22)을 제거하여 아이솔레이션부(I)를 형성한다. 이에 따라 제1 패시베이션막(24)을 터널링층(22) 및 제2 도전형 영역(22)이 제거되어 노출된 반도체 기판(110)의 후면의 가장자리 부분(즉, 아이솔레이션부(I)에 대응하는 부분)을 덮도록 형성한다. 이에 의하여 아이솔레이

션부(I)에 의하여 패시베이션 특성이 저하되는 것을 방지한다. 이때, 별도의 패시베이션막을 사용하지 않고 제1 패시베이션막(24)을 사용하여 태양 전지(100)의 구조 및 제조 공정이 복잡해지는 것을 방지할 수 있다.

<44> 그리고 제1 절연막인 제1 패시베이션막(24)은 반도체 기판(110)의 측면 위까지 연장되는 측면부(24a)를 포함할 수 있다. 제1 패시베이션막(24)의 측면부(24a)를 구비하면 제1 패시베이션막(24)이 반도체 기판(110)의 후면 쪽 위를 전체적으로 안정적으로 덮으면서 형성될 수 있다.

<45> 제2 절연막인 제2 패시베이션막(34) 및 반사 방지막(36)도 반도체 기판(110)의 측면 위까지 연장되는 측면부(34a, 36a)를 포함할 수 있다. 이때, 반도체 기판(110)의 측면에서 제2 절연막이 반도체 기판(110)에 더 가까이 위치하고, 제1 절연막이 제2 절연막 위에 위치할 수 있다. 좀더 구체적으로는, 제2 패시베이션막(34)의 측면부(34a)가 반도체 기판(110)의 측면에 접촉하고, 반사 방지막(36)의 측면부(36a)가 제2 패시베이션막(34)의 측면부(34a)에 접촉하고, 제1 패시베이션막(24)의 측면부(24a)가 반사 방지막(36)의 측면부(36a)에 접촉할 수 있다. 이에 의하면, 제1 패시베이션막(24)을 형성하는 공정에서 제2 도전형 영역(30)을 안정적으로 보호할 수 있도록 제2 절연막을 먼저 형성한 다음 제1 절연막을 형성하였기 때문인데, 이에 대해서는 추후에 좀더 상세하게 설명한다.

<46> 그러나 본 발명이 이에 한정되는 것은 아니며, 반도체 기판(110)의 측면에 측면부(24a, 34a, 36a) 중 적어도 하나가 구비되지 않거나 이들의 적층 순서가 달라질 수도 있다.

<47> 도 2를 참조하여 제1 전극(42)의 평면 형상을 상세하게 설명한 다음, 제2 전극(44)의 평면 형상을 상세하게 설명한다.

<48> 도 2를 참조하면, 제1 전극(42)은 일정한 피치를 가지면서 서로 이격되는 복수의 핑거 전극(42a)을 포함할 수 있다. 도면에서는 핑거 전극(42a)이 서로 평행하며 반도체 기판(110)의 가장자리에 평행한 것을 예시하였으나 본 발명이 이에 한정되는 것은 아니다. 그리고 제1 전극(42)은 핑거 전극들(42a)과 교차하는 방향으로 형성되어 핑거 전극(42a)을 연결하는 버스바 전극(42b)을 포함할 수 있다. 이러한 버스바 전극(42b)은 하나만 구비될 수도 있고, 도 2에 도시된 바와 같이, 핑거 전극(42a)의 피치보다 더 큰 피치를 가지면서 복수 개로 구비될 수도 있다. 이때, 핑거 전극(42a)의 폭보다 버스바 전극(42b)의 폭이 클 수 있으나, 본 발명이 이에 한정되는 것은 아니다. 따라서, 버스바 전극(42b)의 폭이 핑거 전극(42a)의 폭과 동일하거나 그보다 작은 폭을 가질 수 있다.

<49> 단면에서 볼 때, 제1 전극(42)의 핑거 전극(42a) 및 버스바 전극(42b)은 모두 제1 절연막인 패시베이션막(24)을 관통하여 형성될 수도 있다. 즉, 개구부(102)가 제1 전극(42)의 핑거 전극(42a) 및 버스바 전극(42b)에 모두 대응하여 형성될 수 있다. 그러나 본 발명이 이에 한정되는 것은 아니다. 다른 예로, 제1 전극(42)의 핑거 전극(42a)이 제1 패시베이션막(24)을 관통하여 형성되고, 버스바 전극(42b)이 제1 패시베이션막(24) 위에 형성될 수 있다. 이 경우에는 개구부(102)가 핑거 전극(42a)에 대응하는 형상으로 형성되고, 버스바 전극(42b)만 위치한 부분에는 형성되지 않을 수 있다.

<50> 앞서 설명한 바와 같이 본 실시예에서는 반도체 기판(110)의 가장자리를 따라 터널링층(22) 및 제1 도전형 영역(20)이 형성되지 않는 형성되는 아이솔레이션부(I)가 형성된다. 이에 따라 제1 도전형 영역(20) 위에 형성되는 제1 전극(42)이 아이솔레이션부(I)에는 형성되지 않는다. 이에 따라 제1 전극(42)의 핑거 전극(42a) 및 버스바 전극(44b)의 단부는 반도체 기판(110)의 가장자리와 적어도 제1 거리(D1)만큼 이격되어 위치하게 된다.

<51> 제2 전극(44)은 제1 전극(42)의 핑거 전극(42a) 및 버스바 전극(42b)에 각기 대응하는 핑거 전극 및 버스바 전극을 포함할 수 있다. 제2 전극(44)의 핑거 전극 및 버스바 전극에 대해서는 아이솔레이션부(I)에 대한 내용을 제외하고는 제1 전극(42)의 핑거 전극(42a) 및 버스바 전극(42b)에 대한 내용이 그대로 적용될 수 있다. 그리고 제1 전극(42)에서 제1 절연막인 제1 패시베이션막(24)에 관련된 내용은 제2 전극(44)에서 제2 절연막인 제2 패시베이션막(34) 및 반사 방지막(36)에 그대로 적용될 수 있다. 이때, 제1 전극(42)의 핑거 전극(42a) 및 버스바 전극(42b)의 폭, 피치 등은 제2 전극(44)의 핑거 전극 및 버스바 전극의 폭, 피치 등과 서로 동일할 수도 있고 서로 다를 수 있다.

<52> 그러나 본 발명이 이에 한정되는 것은 아니며 제1 전극(42)과 제2 전극(44)의 평면 형상이 서로 다른 것도 가능하며, 그 외의 다양한 변형이 가능하다.

<53> 상술한 바와 같이 본 실시예에서는 태양 전지(100)의 제1 및 제2 전극(42, 44)이 일정한 패턴을 가져 태양 전지(100)가 반도체 기판(110)의 전면 및 후면으로 광이 입사될 수 있는 양면 수광형(bi-facial) 구조를 가진다. 이에 의하여 태양 전

지(100)에서 사용되는 광량을 증가시켜 태양 전지(100)의 효율 향상에 기여할 수 있다. 그러나 본 발명이 이에 한정되는 것은 아니며 제1 전극(42)이 반도체 기판(110)의 후면 쪽에서 전체적으로 형성되는 구조를 가지는 것도 가능하다. 그 외의 다양한 변형이 가능하다.

<54> 이때, 반도체 기판(110)의 후면에 아이솔레이션부(I)를 형성하여 제1 도전형 영역(20)과 제2 도전형 영역(30)이 불필요하게 서로 연결되는 것을 효과적으로 방지할 수 있다. 그리고 터널링층(22) 및 제1 도전형 영역(20)이 제거되어 형성된 아이솔레이션부(I)가 위치하는 반도체 기판(110)의 표면은 제1 도전형 영역(20)을 덮는 제1 절연막(제1 패시베이션막(24))에 의하여 덮여서 패시베이션될 수 있다. 이에 의하여 간단한 구조에 의하여 아이솔레이션부(I)를 패시베이션하여 표면 재결합 등에 의한 문제를 최소화할 수 있다. 즉, 간단한 구조에 의하여 태양 전지(100)의 효율 및 신뢰성을 향상하고 불량률을 낮출 수 있다.

<55> 이러한 태양 전지(100)의 제조 방법을 도 4a 내지 도 4j를 참조하여 상세하게 설명한다. 이미 설명한 내용에 대해서는 상세한 설명을 생략하고 설명하지 않은 내용에 대해서만 상세하게 설명한다.

<56> 도 4a 내지 도 4j는 본 발명의 일 실시예에 따른 태양 전지의 제조 방법을 도시한 단면도들이다.

<57> 도 4a에 도시한 바와 같이, 반도체 기판(110)의 전면 및 후면에 텍스쳐링 공정을 수행하여 요철을 형성한다. 반도체 기판(110)의 텍스쳐링으로는 습식 또는 건식 텍스쳐링을 사용할 수 있다. 습식 텍스쳐링은 텍스쳐링 용액에 반도체 기판

(110)을 침지하는 것에 의해 수행될 수 있으며, 공정 시간이 짧은 장점이 있다. 건식 텍스처링은 다이아몬드 그릴 또는 레이저 등을 이용하여 반도체 기판(110)의 표면을 깍는 것으로, 요철을 균일하게 형성할 수 있는 반면 공정 시간이 길고 반도체 기판(110)에 손상이 발생할 수 있다. 그 외에 반응성 이온 식각(RIE) 등에 의하여 반도체 기판(110)을 텍스처링 할 수도 있다. 이와 같이 본 발명에서는 다양한 방법으로 반도체 기판(110)을 텍스처링 할 수 있다.

<58> 간략한 도시를 위하여 도면에서는 반도체 기판(110)의 측면에는 텍스처링에 의한 요철이 구비되지 않은 것으로 도시하였다. 또한, 반도체 기판(110)의 두께가 매우 작은 편이므로 텍스처링에 의한 요철이 명확하게 인식되기 어려울 수도 있다. 그러나 본 발명이 이에 한정되는 것은 아니다. 반도체 기판(110)의 측면에도 텍스처링에 의한 요철이 구비될 수 있다. 그리고 반도체 기판(110)의 텍스처링은 이후의 공정 중에 수행할 수도 있다.

<59> 도 4b에 도시한 바와 같이, 반도체 기판(110)의 양면 각각에 전체적으로 터널링층(22)을 형성한다. 이때, 터널링층(22)은 반도체 기판(110)의 측면에도 전체적으로 형성될 수 있다.

<60> 여기서, 터널링층(22)은, 일례로, 열적 산화, 화학적 산화, 증착(일 예로, 상압 화학 기상 증착법(APCVD), 저압 화학 기상 증착법(LPCVD)) 등에 의하여 형성될 수 있다. 추가적으로 얇은 두께로 터널링층(22)을 형성한 후에 로(furnace) 내에서의 후속 열처리 등에 의하여 터널링층(22)의 두께 또는 밀도를 증가시킬 수도 있다. 그러나 본 발명이 이에 한정되는 것은 아니며 다양한 방법에 의하여 터널링

층(22)이 형성될 수 있다. 여기서, 터널링층(22)이 실리콘 산화물층으로 이루어질 수 있다.

<61> 일 예로, 본 실시예에서 터널링층(22)은 상온보다 높은 온도 및 상압보다 작은 압력에서 원료 기체를 포함하는 기체 분위기에서 형성될 수 있다. 본 실시예에서는 원료 기체가 산소 기체를 포함하여 터널링층(22)이 산화물층으로 구성될 수 있다. 좀더 구체적으로는, 높은 온도에서 터널링층(22)이 산소와 반도체 기판(110)의 반도체 물질(예를 들어, 실리콘)이 반응하여 형성되는 열적 산화물(thermal oxide material)(예를 들어, 열적 실리콘 산화물)층으로 구성될 수 있다. .

<62> 이때, 본 실시예에서는 원료 기체가 터널링층(22)을 구성하는 모든 원료 물질을 포함하지 않으며, 터널링층(22)을 구성하는 산화물 중에 산소 기체만을 포함하며 다른 원료 물질을 포함하지 않는다. 예를 들어, 터널링층(22)이 실리콘 산화물을 포함할 때, 원료 기체로 산소 기체만을 구비할 뿐 다른 원료 물질인 실리콘을 포함하는 기체를 포함하지 않는다. 이에 따라 산소 기체의 산소가 반도체 기판(110)의 내부로 확산하여 반도체 물질과 반응하는 열적 산화 공정에 의하여 터널링층(22)이 형성된다. 이와 달리, 증착 공정 등에서는 산소를 포함하는 산소 기체와 함께 실리콘을 포함하는 실란(SiH_4) 기체를 원료 기체로 함께 공급한다. 그러면, 열분해에 의하여 산소 기체에서 분리된 산소와 실란 기체에서 분리된 실리콘이 화학적으로 반응하여 실리콘 산화물을 형성하게 된다. 터널링층(22)을 형성할 때 기체 분위기는 원료 기체인 산소 기체 외에도 다양한 기체를 포함할 수 있다.

<63> 그리고 터널링층(22)을 형성할 때의 압력을 상압보다 낮게 하여, 상대적으로 높은 온도(일 예로, 600℃ 이상)에 의한 열적 산화 공정으로 터널링층(22)을 형성하더라도 낮은 압력에 의하여 터널링층(22)의 성장 속도를 낮게 유지할 수 있다. 이에 의하여 터널링층(22)의 두께를 크게 줄일 수 있다. 일 예로, 터널링층(22) 형성 시 온도를 600℃ 내지 800℃로 하고 압력을 600 Torr 이하로 하여 터널링층(22)의 두께를 효과적으로 제어할 수 있다.

<64> 이와 같이 본 실시예에서는 터널링층(22)을 형성할 때 온도와 압력을 함께 제어하여야 하므로 압력 조절이 불가능한 종래의 로(furnace)에서 본 실시예의 터널링층(22)을 형성할 수 없고, 온도 및 압력 조절이 모두 가능한 장비 내에서 터널링층(22)을 형성하여야 한다. 이에 따라 본 실시예에서는 터널링층(22)은 증착 장비 등의 내부에서 열적 산화 공정에 의하여 형성될 수 있다. 이때, 낮은 압력을 구현하여야 하므로 터널링층(22)이 저압 화학 기상 증착 장비(low pressure chemical vapor deposition apparatus) 내에서 형성될 수 있다.

<65> 터널링층(22) 위에 형성되는 반도체층(도 4c의 참조부호 30)이 증착 장비에 의하여 형성되므로 터널링층(22)을 증착 장비에서 형성하게 되면, 터널링층(22)과 진성 반도체층(200)을 동일한 증착 장비(좀더 구체적으로는, 저압 화학 기상 증착 장비) 내에서 연속적으로 수행되는 인-시츄(in-situ) 공정에 의하여 형성될 수 있다. 이와 같이 터널링층(22)과 진성 반도체층(200)을 인-시츄 공정에 의하여 형성하게 되면, 제조 공정을 크게 단순화할 수 있어 제조 비용, 제조 시간 등을 크게 절감할 수 있다.

<66> 증착 장비 내의 온도는 긴 시간 동안 열을 가하거나 열을 식히는 것에 의하여 조절되며 온도를 안정화하는 데 시간이 많이 소요되는 반면, 기체 분위기 및 압력은 증착 장비 내로 공급되는 기체의 종류, 양 등에 의하여 조절될 수 있다. 따라서, 기체 분위기 및 압력은 온도보다 쉽게 제어될 수 있다.

<67> 이를 고려하여 본 실시예에서는 터널링층(22)의 형성 온도와 진성 반도체층(200)의 증착 공정의 온도 차이가 200℃ 이내(즉, 0℃ 내지 200℃)가 되도록 할 수 있다. 좀더 구체적으로는, 터널링층(22)의 형성 온도와 진성 반도체층(200)의 증착 공정의 온도 차이를 100℃ 이내(즉, 00℃ 내지 100℃)가 되도록 할 수 있다. 이는 터널링층(22)을 저압에서 형성하므로 터널링층(22)의 형성 온도를 상대적으로 높일 수 있어서 진성 반도체층(200)의 증착 공정과의 온도 차이를 줄일 수 있기 때문이다. 이와 같이 상대적으로 조절이 힘든 온도를 큰 변화 없이 유지할 수 있어 터널링층(22)과 진성 반도체층(200)을 연속적으로 형성하는 인-시츄 공정의 효율을 좀더 향상할 수 있다. 반면, 진성 반도체층(200)의 증착 공정의 기체 분위기는 터널링층(22)의 형성 시의 기체 분위기와 다르고, 진성 반도체층(200)의 증착 공정의 압력은 터널링층(22)의 형성 시의 압력과 같거나 이와 다를 수 있다. 이에 대해서는 추후에 진성 반도체층(200)의 증착 공정을 설명하면서 좀더 상세하게 설명한다.

<68> 도 4c에 도시한 바와 같이, 반도체 기판(110)의 양측 각각에서 터널링층(22) 위에 전체적으로 진성 반도체층(200)을 형성한다. 이때, 진성 반도체층(200)은 반도체 기판(110)의 측면 위에 위치한 터널링층(22) 위에도 전체적으로 형성될 수 있다. 이와 같이 진성 반도체층(200)이 양면에 위치하면 제1 도전형 영역(20)을 도핑

하는 공정에서 반도체 기판(110)의 전면의 도핑, 손상 등을 효과적으로 방지할 수 있다.

<69> 본 실시예에서 진성 반도체층(200)은 화학 기상 증착에 의하여 형성될 수 있고, 좀더 구체적으로는 저압 화학 기상 증착에 의하여 형성될 수 있다. 이에 따라 앞서 설명한 바와 같이 진성 반도체층(200)이 터널링층(22)과 인-시츄 공정에 의하여 형성될 수 있다. 그러나 본 발명이 이에 한정되는 것은 아니며 터널링층(22) 및 진성 반도체층(200)에 인-시츄 공정이 적용되지 않을 수도 있다.

<70> 진성 반도체층(200)의 증착 공정에 사용되는 기체는 진성 반도체층(200)을 구성하는 반도체 물질을 포함하는 기체(예를 들어, 실란 기체)를 포함할 수 있다. 본 실시예에서는 진성을 가지도록 진성 반도체층(200)을 증착하므로 기체 분위기가 반도체 물질을 포함하는 기체만으로 구성될 수 있다. 이에 의하여 공급 기체를 단순화할 수 있고, 형성되는 진성 반도체층(200)의 순도를 향상할 수 있다. 그러나 본 발명이 이에 한정되는 것은 아니며 진성 반도체층(200)의 증착 공정을 촉진하거나, 진성 반도체층(200)의 특성을 향상하기 위한 별도의 기체 등을 더 사용될 수 있다. 그리고 진성 반도체층(200)의 증착 공정에서는 반도체 물질을 포함하는 기체 외에도 산화질소(N_2O) 기체 및/또는 산소(O_2) 기체를 함께 주입하여 결정립 크기, 결정성 등을 조절할 수 있다.

<71> 진성 반도체층(200)의 증착 온도는 터널링층(22)의 형성 시의 온도와 동일하거나 이보다 작을 수 있다. 특히, 진성 반도체층(200)의 증착 온도를 터널링층(22)

형성 시의 온도보다 작게 하면, 광전 변환에 직접적으로 관여하는 진성 반도체층(200)의 특성을 균일하게 할 수 있다. 또는, 진성 반도체층(200)의 증착 온도는 500℃ 내지 700℃일 수 있다. 이는 반도체 기판(110)과 다른 결정 구조를 가지는 진성 반도체층(200)을 증착하기에 적합한 온도로 한정된 것이다. 앞서 설명한 바와 같이, 터널링층(22)의 온도를 진성 반도체층(200)의 증착 온도와 동일 또는 유사하게 하였으므로, 온도를 조절하기 위한 시간, 온도를 안정화하기 위한 시간 등이 필요하지 않아 공정을 단순화할 수 있다.

<72> 그리고 진성 반도체층(200)의 증착 압력은 상압보다 낮은 압력, 일 예로, 600 Torr 이하(일 예로, 1 Torr 내지 600 Torr)일 수 있다. 증착 압력을 1 Torr 미만으로 유지하는 것은 공정 상 한계가 있을 수 있고 진성 반도체층(200)의 공정 시간이 크게 길어져서 실제 양산에 적용되기 어려울 수 있다. 증착 압력이 600 Torr를 초과하면, 진성 반도체층(200)의 균일도가 저하될 수 있다. 또는, 진성 반도체층(200)의 증착 압력은 터널링층(22)의 형성 시 압력과 같거나 이보다 작을 수 있다. 특히, 진성 반도체층(200)의 증착 압력을 터널링층(22) 형성 시의 압력보다 작게 하면, 광전 변환에 직접적으로 관여하는 진성 반도체층(200)의 특성을 균일하게 할 수 있다.

<73> 이를 좀더 상세하게 설명한다. 반도체 물질(예를 들어, 실리콘)을 포함하는 기체가 열분해되어 반도체 물질이 터널링층(22) 위에 증착되는 것에 의하여 진성 반도체층(200)이 형성된다. 그런데, 증착 속도를 증가시키기 위하여 온도 및/또는 압력을 증가시키게 되면 진성 반도체층(200) 내부에서 결정성의 산포가 커지게 된

다. 진성 반도체층(200)의 결정성은 캐리어의 이동 속도 등에 관여하게 되므로, 진성 반도체층(200)의 결정성의 산포가 커지면 진성 반도체층(200)의 특성이 불균해질 수 있다. 반면, 터널링층(22)은 아주 얇은 두께로 형성되며 결정성이 터널링층(22)의 특성에 큰 영향을 미치지 않는다. 이를 고려하여, 진성 반도체층(200)이 터널링층(22)보다 두꺼운 두께로 형성되어야 함에도 불구하고 진성 반도체층(200)의 증착 온도 및/또는 압력을 터널링층(22)의 형성 시보다 낮게 하여 진성 반도체층(200)의 특성을 향상하는 것이다.

<74> 그러나 본 발명이 이에 한정되는 것은 아니며 진성 반도체층(200)의 기체 분위기, 온도, 압력 등은 다양하게 변화될 수 있다.

<75> 이와 같이 진성 반도체층(200)은 터널링층(22)의 형성 후에 공급되는 기체의 종류를 변경하고 공급되는 기체의 양을 조절하는 것에 의하여 형성될 수 있다. 예를 들어, 터널링층(22)의 형성이 완료된 후에 터널링층(22)의 형성 시에 사용되었던 기체(예를 들어, 산소 기체, 질소 기체, 염소 기체 등)을 펌핑(pumping) 및 퍼지(purge)에 의하여 제거한 후에, 진성 반도체층(200)을 형성하기 위한 기체(예를 들어, 반도체 물질을 포함하는 기체 등)를 주입하는 것에 의하여 진성 반도체층(200)을 형성할 수 있다.)

<76> 이에 따라 터널링층(22) 및 진성 반도체층(200)의 형성 공정을 단순화할 수 있다. 또한, 종래와 같이 터널링층을 형성한 다음 터널링층이 형성된 반도체 기판을 장비 외부로 꺼내게 되면, 터널링층이 불순물에 오염되거나 추가적인 산화에 의하여 터널링층의 두께가 두꺼워지는 문제가 있었다. 본 실시예에서는 터널링층(2

2)을 형성한 장비 내에서 진성 반도체층(200)을 연속하여 형성하므로 터널링층(22)이 진성 반도체층(200) 형성 전에 외부로 노출되지 않는다. 따라서 터널링층(22)이 진성 반도체층(200) 형성 전에 외부로 노출되어 발생할 수 있는 문제를 방지할 수 있다.

<77> 참고로, 플라스마 화학 기상 증착(PECVD)을 사용하는 경우에는 진성 반도체층(200)을 형성한 후에 다결정 구조를 가지게 하기 위하여 별도의 결정화 어닐링 공정을 수행하여야 한다. 이에 따라 구조가 복잡해지고 성능 또한 낮을 수 있다. 또한, 플라스마 화학 기상 증착은 단면 공정으로 반도체 기판(110)의 양측 각각에 전체적으로 진성 반도체층(200)을 형성하기 어려울 수 있다.

<78> 이어서, 도 4d에 도시한 바와 같이, 적어도 반도체 기판(110)의 후면 쪽에 위치한 진성 반도체층(200)을 제1 도전형 도펀트로 도핑하여 제1 도전형 영역(20a)을 형성한다. 이때, 본 실시예에서는 열 확산법에 의하여 제1 도전형 도펀트를 도핑할 수 있다. 열 확산법이 터널링층(22)의 특성 저하를 최소화하면서 도핑이 가능하기 때문이다. 반면, 이온 주입법 등은 이온 주입 후에 고온에서 이루어지는 활성화 열처리에 의하여 터널링층(22)의 특성이 저하될 수 있다.

<79> 일 예로, 도 4d에 도시한 바와 같이, 제1 도전형 도펀트를 포함하는 기체 분위기에서 열처리하는 것에 의하여 전체적으로 제1 도전형 영역(20a)을 형성할 수 있다. 제1 도전형 영역(20a)이 n형을 가질 경우에는 $POCl_3$를 포함하는 기체 분위기에서 열처리할 수 있다. 또는, 제1 도전형 영역(20a)이 p형을 가질 경우에는 BBr_3를

포함하는 기체 분위기에서 열처리할 수 있다.

<80> 이와 같이 제1 도전형 도펀트를 포함하는 기체를 사용하여 제1 도전형 영역(20a)을 형성하는 공정을 단순화할 수 있다. 다만, 이러한 공정에 의하여 반도체 기판(110)의 후면 쪽과 함께 반도체 기판(110)의 전면 및 측면 쪽에서도 도핑이 이루어진다. 본 실시예에서는 반도체 기판(110)의 전면 및 측면 쪽에 후속 공정에서 제거될 진성 반도체층(200)의 부분이 존재하므로, 반도체 기판(110)의 전면 및 측면이 불필요하게 제1 도전형 도펀트로 도핑되는 것을 원천적으로 방지할 수 있다.

<81> 다른 예로, 도 5에 도시한 바와 같이, 적어도 반도체 기판(110)의 후면 쪽에 위치한 진성 반도체층(200) 위에 제1 도전형 도펀트를 포함하는 제1 도핑층(210)을 형성하고, 열처리에 의하여 제1 도핑층(210) 내에 포함된 제1 도전형 도펀트를 확산시켜 제1 도전형 영역(20a)을 형성할 수 있다. 일 예로, 제1 도핑층(210)은 인 실리케이트 유리(phosphorus silicate glass, PSG), 보론 실리케이트 유리(boron silicate glass, BSG) 등을 포함할 수 있다. 이러한 제1 도핑층(210)은 증착 등에 의하여 쉽게 형성할 수 있다.

<82> 일 예로, 제1 도핑층(210)은 상압 화학 기상 증착 등에 의하여 형성되어 반도체 기판(110)의 후면 및/또는 측면 쪽에 형성되고 전면에는 형성되지 않는다. 이에 따라 제1 도전형 영역(20a)이 반도체 기판(110)의 후면 및/또는 측면 쪽에만 형성되고 전면에는 진성 반도체층(200)이 그대로 잔존할 수 있다.

<83> 이어서, 도 4e에 도시한 바와 같이, 반도체 기판(110)의 후면 쪽에 위치한 제1 도전형 영역(20a) 위에 아이솔레이션부(도 4f의 참조부호 I, 이하 동일) 이외

에서 잔존하여야 할 제1 도전형 영역(도 4f의 참조부호 20, 이하 동일)에 대응하도록 마스크층(202)을 형성한다. 좀더 구체적으로, 마스크층(202)의 면적은 반도체 기판(110)의 면적보다 작을 수 있다. 이에 의하여 원하지 않는 제1 도전형 영역(20a)의 부분을 제거하여 아이솔레이션부(I) 이외에서 잔존하는 제1 도전형 영역(도 4f의 참조부호 20, 이하 동일)이 반도체 기판(110)보다 작은 면적을 가지도록 할 수 있다.

<84> 일 예로, 마스크층(202)은 반도체 기판(110)의 각 측면(또는 가장자리)로부터 일정한 제2 거리(D2)만큼 이격될 수 있다. 마스크층(202)이 반도체 기판(110)과 동일하거나 이보다 큰 면적을 가지면 반도체 기판(110)의 후면에서 반도체 기판(110)의 측면에 인접하여 위치한 제1 도전형 영역(20a)의 부분을 효과적으로 제거하기 어려울 수 있다. 제2 거리(D2)는 제1 도전형 영역(20)이 반도체 기판(110)의 후면 가장자리로부터 이격된 제1 거리(D1)가 원하는 값을 가질 수 있도록 제어될 수 있다. 일 예로, 제1 거리(D1)가 1mm 이하(일 예로, 1nm 내지 1mm)의 값을 가질 수 있도록 제2 거리(D2)가 1mm 이하(일 예로, 1nm 내지 1mm)의 값을 가질 수 있다. 그러나 본 발명이 이에 한정되는 것은 아니며 제2 거리(D2)가 이와 다른 값을 가질 수도 있다.

<85> 마스크층(202)은 반도체 물질을 포함하는 제1 도전형 영역(20a)을 제거하는 공정에서 제거되지 않는 물질을 포함할 수 있다. 예를 들어, 제1 도전형 영역(20a)을 제거하는 공정에서 사용되는 식각 용액에 식각되지 않는 마스크층(202)은 산화물, 질화물, 수지 등을 포함할 수 있다. 일 예로, 마스크층(202)이 실리콘 질화

물층으로 구성되어 단순한 공정으로 마스크층(202)을 형성할 수 있다.

<86> 이어서, 도 4f에 도시한 바와 같이, 마스크층(202)에 의하여 덮여지지 않은 제1 도전형 영역(20) 및 터널링층(22)의 부분을 제거하여 아이솔레이션부(I)를 형성한다. 일 예로, 제1 도전형 영역(20) 및 터널링층(22)은 알칼리 용액(일 예로, KOH 용액)을 이용한 습식 식각에 의하여 제거될 수 있다. 습식 식각에 의하면 간단하고 쉬운 공정에 의하여 반도체 기판(110)의 전면, 측면 및 후면의 아이솔레이션부(I)에 위치한 제1 도전형 영역(20) 및 터널링층(22)을 제거할 수 있다. 알칼리 용액에 의하여 제1 도전형 영역(20)을 선택적으로 쉽게 제거할 수 있으며, 비록 산화물이지만 매우 작은 두께를 가지는 터널링층(22)도 쉽게 제1 도전형 영역(20)이 제거될 때 함께 제거될 수 있다. 이에 의하여 반도체 기판(110)보다 작은 면적을 가지며 반도체 기판(110)의 후면 가장자리로부터 제1 거리(D1)만큼 떨어진 제1 도전형 영역(20) 및 터널링층(22)을 형성할 수 있다.

<87> 습식 식각에 의하여 제1 도전형 영역(20) 및 터널링층(22)이 반도체 기판(110)으로부터 멀어지면서 면적이 작아지는 형상을 가질 수 있고, 측면이 라운드지게 형성될 수 있다. 그러나 본 발명이 이에 한정되는 것은 아니다. 제1 도전형 영역(20) 및 터널링층(22)의 일부가 반응성 이온 식각, 건식 식각 등의 다양한 방법에 의하여 제거될 수 있고, 제1 도전형 영역(20) 및 터널링층(22)의 형상이 다른 형상을 가질 수 있다.

<88> 아이솔레이션부(I)를 형성하도록 제1 도전형 영역(20) 및 터널링층(22)의 일부를 제거한 후에 이후에 마스크층(202)을 제거할 수 있다. 마스크층(202)은 물질

에 따라 다양한 방법에 의하여 제거될 수 있다. 일 예로, 마스크층(202)이 산화물, 질화물 등을 포함할 때에는 희석된 불산을 사용한 공정에 의하여 제거될 수 있다. 마스크층(202)은 별도의 공정에 의하여 제거될 수도 있고, 희석된 불산을 포함하는 용액을 포함하는 세정 공정에 의하여 자연스럽게 제거될 수도 있다. 그러나 본 발명이 이에 한정되는 것은 아니며 마스크층(202)의 제거 방법으로 알려진 다양한 방법이 사용될 수 있다.

<89> 이어서, 도 4g에 도시한 바와 같이, 반도체 기판(110)의 전면 쪽에 제2 도전형 영역(30)을 형성한다. 제2 도전형 영역(30)은 제2 도전형 도펀트를 반도체 기판(110)에 도핑하여 반도체 기판(110)의 일부를 구성하는 도핑 영역으로 구성될 수 있다.

<90> 제2 도전형 영역(30)은 알려진 다양한 방법에 의하여 형성될 수 있다. 예를 들어, 제2 도전형 영역(30)이 열 확산법에 의하여 형성될 수 있다. 열 확산법이 터널링층(22)의 특성 저하를 최소화하면서 도핑이 가능하기 때문이다. 반면, 이온 주입법 등은 이온 주입 후에 고온에서 이루어지는 활성화 열처리에 의하여 터널링층(22)의 특성이 저하될 수 있다.

<91> 일 예로, 도 4g에 도시한 바와 같이, 반도체 기판(110)의 측면 및 후면에 캡핑막(204)을 형성하고 제2 도전형 도펀트를 포함하는 가스 분위기에서 열처리하는 것에 의하여 반도체 기판(110)의 전면에 제2 도전형 영역(30)을 형성할 수 있다. 제2 도전형 영역(30)이 p형을 가질 경우에는 BBr_3를 포함하는 기체 분위기에서 열처

리할 수 있다. 또는, 제2 도전형 영역(30)이 n형을 가질 경우에는 $POCl_3$를 포함하는 기체 분위기에서 열처리할 수 있다. 제2 도전형 영역(30)이 형성된 후에는 캡핑막(204)을 제거할 수 있다. 캡핑막(204)은 제2 도전형 도펀트의 도핑을 막을 수 있는 다양한 막이 사용될 수 있으며, 물질에 따른 제거 방법에 의하여 제거될 수 있다.

<92> 다른 예로, 도 6에 도시한 바와 같이, 반도체 기판(110)의 전면 위에 제2 도전형 도펀트를 포함하는 제2 도핑층(310)을 형성하고, 열처리에 의하여 제2 도핑층(310) 내에 포함된 제2 도전형 도펀트를 반도체 기판(110)의 내부로 확산시켜 제2 도전형 영역(30)을 형성할 수 있다. 일 예로, 제2 도핑층(310)은 보론 실리케이트 유리(boron silicate glass, BSG), 인 실리케이트 유리(phosphorus silicate glass, PSG) 등을 포함할 수 있다. 이러한 제2 도핑층(310)은 증착 등에 의하여 쉽게 형성할 수 있다. 일 예로, 제2 도핑층(310)은 상압 화학 기상 증착 등에 의하여 형성되어 반도체 기판(110)의 후면에는 형성되지 않는다.

<93> 이어서, 도 4h에 도시한 바와 같이, 반도체 기판(110)의 전면 쪽에 제2 절연막을 형성한다. 예를 들어, 반도체 기판(110)의 전면 쪽에서 제2 도전형 영역(30) 위에 제2 패시베이션막(34) 및 반사 방지막(36)을 형성한다. 이때, 반도체 기판(110)의 측면에도 절연층(즉, 제2 패시베이션막(34) 및 반사 방지막(36))이 함께 형성될 수 있다. 예를 들어, 반도체 기판(110)의 전면 쪽에 위치한 절연막 중 적어도 일부(일 예로, 제2 패시베이션막(34))이 제2 도전형 영역(30)에 접촉할 수 있다.

<94> 제2 패시베이션막(34) 또는 반사 방지막(36)은 진공 증착법, 화학 기상 증착법, 스핀 코팅, 스크린 인쇄 또는 스프레이 코팅 등과 같은 다양한 방법에 의하여 형성될 수 있다. 이때, 제2 패시베이션막(34) 또는 반사 방지막(36)의 형성 시에 플라스마 유도 화학 기상 증착(PECVD)과 같은 단면 증착을 사용하면 전면 및/또는 측면에만 제2 패시베이션막(34) 또는 반사 방지막(36)을 형성할 수 있다. 따라서 제2 패시베이션막(34) 또는 반사 방지막(36)을 위한 별도의 패터닝 공정을 구비하지 않아도 된다.

<95> 이어서, 도 4i에 도시한 바와 같이, 반도체 기판(110)의 후면 쪽에 제1 절연막을 형성한다. 예를 들어, 반도체 기판(110)의 후면 쪽에서 제1 도전형 영역(20) 및 반도체 기판(110)의 후면 위에 제1 패시베이션막(24)을 형성한다. 이때, 반도체 기판(110)의 측면 쪽에도 절연층(즉, 제1 패시베이션막(24))이 함께 형성될 수 있다.

<96> 좀더 구체적으로, 제1 패시베이션막(24)은 제1 도전형 영역(20)의 위, 제1 도전형 영역(20) 및 터널링층(22)의 측면 위, 반도체 기판(110)의 후면 위, 그리고 반도체 기판(110)의 측면 위에 연속적으로 연장되어 형성될 수 있다. 이때, 제1 패시베이션막(24)은 제1 도전형 영역(20)의 위, 제1 도전형 영역(20) 및 터널링층(22)의 측면 위, 그리고 반도체 기판(110)의 후면 위에 접촉할 수 있다. 이에 의하여 아이솔레이션부(I)에 의한 에지 아이솔레이션이 이루어진 후에 별도의 공정 없이 제1 패시베이션막(24)을 형성하면서 아이솔레이션부(I)를 함께 패시베이션할 수 있다.

<97> 일 예로, 제1 패시베이션막(24)은 진공 증착법, 화학 기상 증착법, 스핀 코팅, 스크린 인쇄 또는 스프레이 코팅 등과 같은 다양한 방법에 의하여 형성될 수 있다. 이때, 제1 패시베이션막(24) 또는 반사 방지막(36)의 형성 시에 플라스마 유도 화학 기상 증착(PECVD)과 같은 단면 증착을 사용하면 후면 및/또는 측면에만 제1 패시베이션막(24)을 형성할 수 있다. 따라서 제1 패시베이션막(24)을 위한 별도의 패터닝 공정을 구비하지 않아도 된다.

<98> 본 실시예에서는 반도체 기판(110)의 전면 쪽은 덮는 제2 절연막을 먼저 형성한 후에 반도체 기판(110)의 후면 쪽을 덮는 제1 절연막을 형성하는 것을 예시하였다. 이에 의하면 제1 절연막을 형성하는 공정 중에 제1 도전형 영역(20)의 특성이 저하되거나 손상되는 것을 방지할 수 있다. 특히, 제1 도전형 영역(20)이 에미터 영역일 때에는 제1 도전형 영역(20)의 특성이 매우 중요할 수 있기 때문이다. 그러나 본 발명이 이에 한정되는 것은 아니다. 본 실시예에서는 반도체 기판(110)의 후면 쪽을 덮는 제1 절연막을 먼저 형성한 후에 반도체 기판(110)의 전면 쪽을 덮는 제2 절연막을 형성할 수도 있다. 이 경우에는 이에 따라 반도체 기판(110)의 측면에 반도체 기판(110)의 후면 쪽을 덮는 제1 절연막이 위치(일 예로, 접촉)하고, 이 위에 반도체 기판(110)의 전면 쪽을 덮는 제2 절연막이 위치(일 예로, 접촉)할 수 있다.

<99> 이어서, 도 4j에 도시한 바와 같이, 제1 및 제2 도전형 영역(20, 30)에 각기 연결되는 제1 및 제2 전극(42, 44)을 형성한다.

<100> 일 예로, 패터닝 공정에 의하여 제1 및 제2 절연막에 제1 및 제2 개구부

(102, 104)를 형성하고, 그 이후에 제1 및 제2 개구부(102, 104) 내를 채우면서 제1 및 제2 전극(42, 44)을 형성한다. 이때, 제1 및 제2 개구부(102, 104)는 레이저를 이용한 레이저 어블레이션, 또는 식각 용액 또는 식각 페이스트 등을 이용한 다양한 방법에 의하여 형성될 수 있다. 그리고 제1 및 제2 전극(42, 44)은 도금법, 증착법 등의 다양한 방법에 의하여 형성될 수 있다.

<101> 다른 예로, 제1 및 제2 전극 형성용 페이스트를 제1 및 제2 절연막에 각기 스크린 인쇄 등으로 도포한 후에 파이어 스루(fire through) 또는 레이저 소성 컨택(laser firing contact) 등을 하여 상술한 형상의 제1 및 제2 전극(42, 44)을 형성하는 것도 가능하다. 이 경우에는 제1 및 제2 전극(42, 44)을 형성할 때 자연스럽게 제1 및 제2 개구부(102, 104)가 형성되므로, 별도로 제1 및 제2 개구부(102, 104)를 형성하는 공정을 추가하지 않아도 된다.

<102> 이에 따르면 단순한 공정에 의하여 아이솔레이션부(I)를 형성할 수 있으며 아이솔레이션부(I)를 제1 절연막인 제1 패시베이션막(24)에 의하여 패시베이션하여 표면 재결합에 의한 문제를 방지할 수 있다. 이에 의하여 간단한 공정에 의하여 태양 전지(100)의 불량률을 낮춰 생산성을 향상할 수 있다.

<103> 상술한 바에 따른 특징, 구조, 효과 등은 본 발명의 적어도 하나의 실시예에 포함되며, 반드시 하나의 실시예에만 한정되는 것은 아니다. 나아가, 각 실시예에서 예시된 특징, 구조, 효과 등은 실시예들이 속하는 분야의 통상의 지식을 가지는 자에 의하여 다른 실시예들에 대해서도 조합 또는 변형되어 실시 가능하다. 따라서 이러한 조합과 변형에 관계된 내용들은 본 발명의 범위에 포함되는 것으로 해석되

어야 할 것이다.

【부호의 설명】

<104> 100: 태양 전지

110: 반도체 기판

22: 터널링층

20: 제1 도전형 영역

30: 제2 도전형 영역

24: 제1 패시베이션막

34: 제2 패시베이션막

36: 반사 방지막

42: 제1 전극

44: 제2 전극

【특허청구범위】

【청구항 1】

반도체 기판의 일면 위에 위치하는 터널링층;

상기 터널링층 위에 위치하는 제1 도전형 영역;

상기 제1 도전형 영역 위에서 상기 제1 도전형 영역을 패시베이션하는 제1 절연막;

상기 반도체 기판의 타면 쪽에 위치하며 도핑 영역으로 구성되는 제2 도전형 영역;

상기 제1 도전형 영역에 연결되는 제1 전극; 및

상기 제2 도전형 영역에 연결되는 제2 전극

을 포함하고,

상기 반도체 기판의 일면의 가장자리 부분에 상기 터널링층 및 상기 제1 도전형 영역이 위치하지 않는 아이솔레이션부가 위치하고,

상기 제1 절연막이 상기 아이솔레이션부가 위치하는 상기 반도체 기판의 일면 위를 덮는 태양 전지.

【청구항 2】

제1항에 있어서,

상기 제1 절연막이 상기 아이솔레이션부가 위치하는 상기 반도체 기판의 일면에 접촉하는 태양 전지.

【청구항 3】

제1항에 있어서,

상기 아이솔레이션부의 폭이 1㎜ 이하인 태양 전지.

【청구항 4】

제3항에 있어서,

상기 아이솔레이션부의 폭이 1㎚ 내지 1㎜ 이하인 태양 전지.

【청구항 5】

제1항에 있어서,

상기 반도체 기판으로부터 멀어질수록 상기 제1 도전형 영역의 면적이 작아지는 태양 전지.

【청구항 6】

제1항에 있어서,

상기 제1 도전형 영역의 측면이 라운드진 형상을 가지는 태양 전지.

【청구항 7】

제1항에 있어서,

상기 제1 절연막은 상기 반도체 기판의 측면 위까지 연장되는 측면부를 포함하는 태양 전지.

【청구항 8】

제7항에 있어서,

상기 제2 도전형 영역 위에 위치하는 제2 절연막을 더 포함하고,

상기 제2 절연막이 상기 반도체 기판의 측면 위에 형성되는 측면부를 포함하고,

상기 반도체 기판의 측면 위에서 상기 제1 절연막의 측면부가 상기 제2 절연막의 측면부 위에 위치하는 태양 전지.

【청구항 9】

반도체 기판의 일면 및 타면 위에 각기 터널링층을 형성하는 단계;

상기 반도체 기판의 양측에서 각기 상기 터널링층 위에 진성 반도체층을 형성하는 단계;

적어도 상기 반도체 기판의 일측에 위치하는 상기 진성 반도체층의 부분에 제1 도전형 도펀트를 도핑하여 제1 도전형 영역을 형성하는 단계;

적어도 상기 반도체 기판의 타측에 위치한 상기 터널링층 및 상기 진성 반도체층 또는 상기 제1 도전형 영역을 전체적으로 제거하는 단계;

상기 반도체 기판의 타측에 제2 도전형 도펀트를 도핑하여 도핑 영역으로 구성되는 제2 도전형 영역을 형성하는 단계;

상기 제1 도전형 영역을 덮는 제1 절연막을 형성하는 단계; 및

상기 제1 도전형 영역에 연결되는 제1 전극 및 상기 제2 도전형 영역에 연결

되는 제2 전극을 포함하는 전극을 형성하는 단계

를 포함하고,

상기 제거하는 단계에서 상기 반도체 기판의 일측에 위치한 상기 터널링층 및 상기 제1 도전형 영역의 가장자리 부분을 함께 제거하여 아이솔레이션부를 형성하고,

상기 제1 절연막이 상기 아이솔레이션부가 위치하는 상기 반도체 기판의 일측 위를 덮는 태양 전지의 제조 방법.

【청구항 10】

제9항에 있어서,

상기 제1 절연막이 상기 아이솔레이션부가 위치하는 상기 반도체 기판의 일측에 접촉하는 태양 전지의 제조 방법.

【청구항 11】

제9항에 있어서,

상기 아이솔레이션부의 폭이 1㎜ 이하인 태양 전지의 제조 방법.

【청구항 12】

제10항에 있어서,

상기 아이솔레이션부의 폭이 1㎚ 내지 1㎜ 이하인 태양 전지의 제조 방법.

【청구항 13】

제9항에 있어서,

상기 제거하는 단계는,

상기 반도체 기판의 타측에서 상기 제1 도전형 영역 위에 상기 반도체 기판보다 작은 면적을 가지는 마스크층을 형성하는 단계;

상기 마스크층이 형성되지 않은 부분에 위치한 상기 제1 도전형 영역 및 상기 터널링층을 식각하는 단계; 및

상기 마스크층을 제거하는 단계

를 포함하는 태양 전지의 제조 방법.

【청구항 14】

제13항에 있어서,

상기 반도체 기판의 후면 가장자리와 상기 마스크층의 가장자리 사이의 거리가 1㎜ 이하인 태양 전지의 제조 방법.

【청구항 15】

제9항에 있어서,

상기 제거하는 단계가 반응성 이온 식각(reactive ion etching, RIE) 또는 습식 식각에 의하여 수행되는 태양 전지의 제조 방법.

【청구항 16】

제9항에 있어서,

상기 반도체 기판으로부터 멀어질수록 상기 제1 도전형 영역의 면적이 작아지는 태양 전지의 제조 방법.

【청구항 17】

제9항에 있어서,

상기 제1 도전형 영역의 측면이 라운드진 형상을 가지는 태양 전지의 제조 방법.

【청구항 18】

제9항에 있어서,

상기 제2 도전형 영역을 형성하는 단계와 상기 제1 절연막을 형성하는 단계 사이에, 상기 제2 도전형 영역을 덮는 제2 절연막을 형성하는 단계를 더 포함하고,

상기 반도체 기판의 측면 위에 상기 제2 절연막이 위치하고 상기 제2 절연막 위에 상기 제1 절연막이 위치하는 태양 전지의 제조 방법.

【청구항 19】

제9항에 있어서,

상기 제1 도전형 영역을 형성하는 단계 또는 상기 제2 도전형 영역을 형성하는 단계는 열 확산법을 이용하는 태양 전지의 제조 방법.

【청구항 20】

제9항에 있어서,

상기 터널링층 또는 상기 진성 반도체층은 저압 화학 기상 증착 장비에서 형성되는 태양 전지의 제조 방법.

제출 일자 : 2015-08-31

【요약서】

【요약】

본 발명의 실시예에 따른 태양 전지는, 반도체 기판의 일면 위에 위치하는 터널링층; 상기 터널링층 위에 위치하는 제1 도전형 영역; 상기 제1 도전형 영역 위에서 상기 제1 도전형 영역을 패시베이션하는 제1 절연막; 상기 반도체 기판의 타면 쪽에 위치하며 도핑 영역으로 구성되는 제2 도전형 영역; 상기 제1 도전형 영역에 연결되는 제1 전극; 및 상기 제2 도전형 영역에 연결되는 제2 전극을 포함한다. 상기 반도체 기판의 일면의 가장자리 부분에 상기 터널링층 및 상기 제1 도전형 영역이 위치하지 않는 아이솔레이션부가 위치한다. 상기 제1 절연막이 상기 아이솔레이션부가 위치하는 상기 반도체 기판의 일면 위를 덮는다.

【대표도】

도 1

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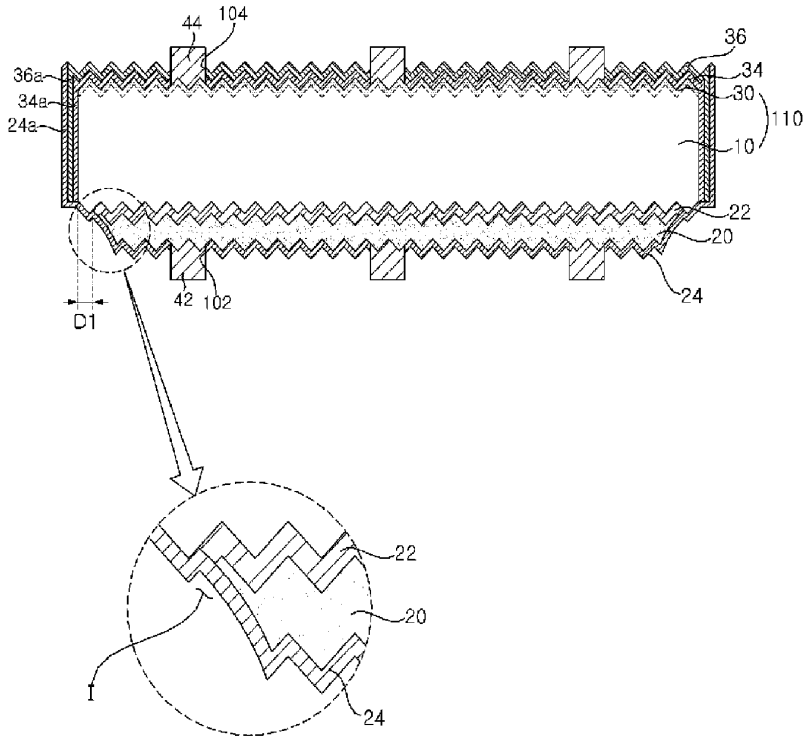
【도면】

【도 1】



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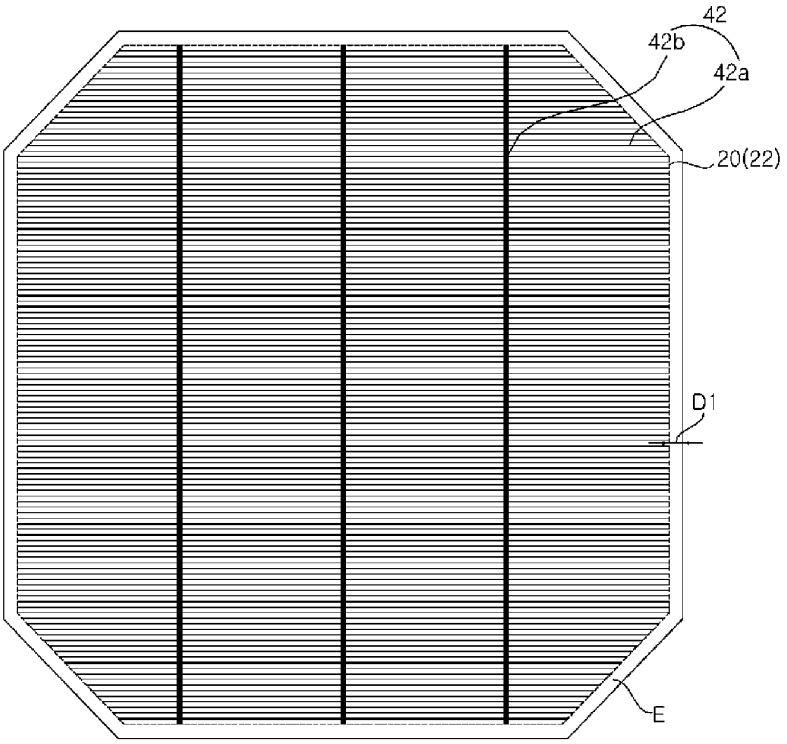

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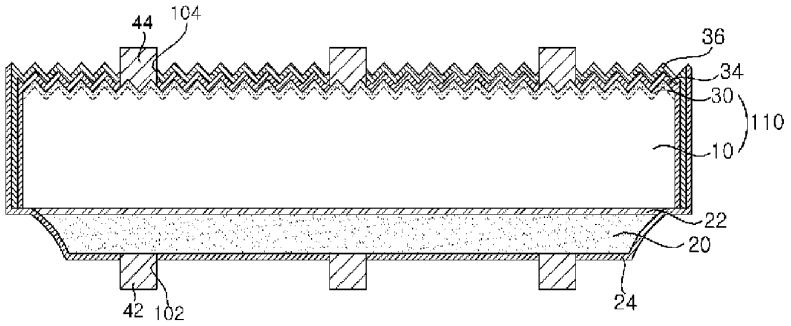

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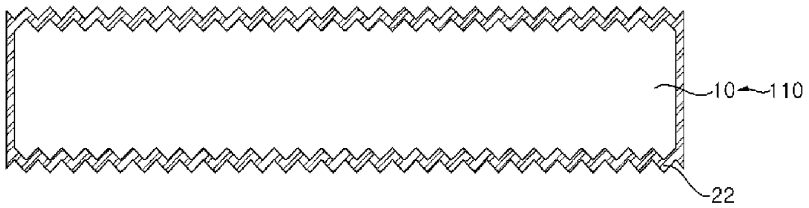

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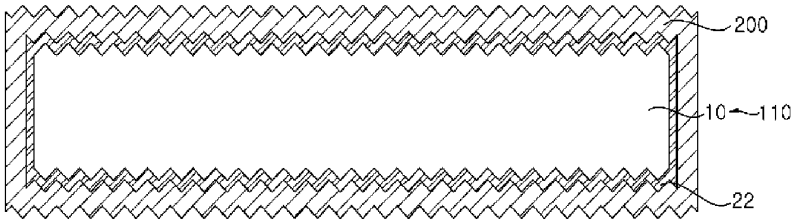

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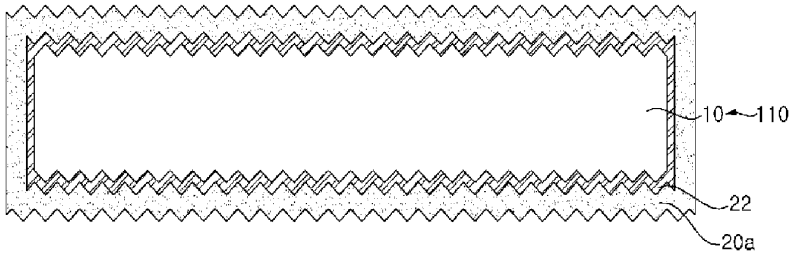

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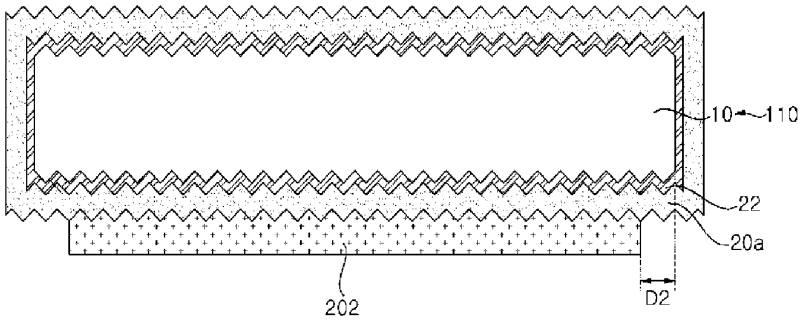

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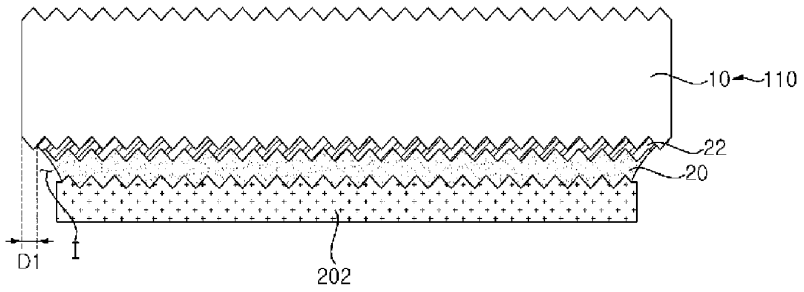

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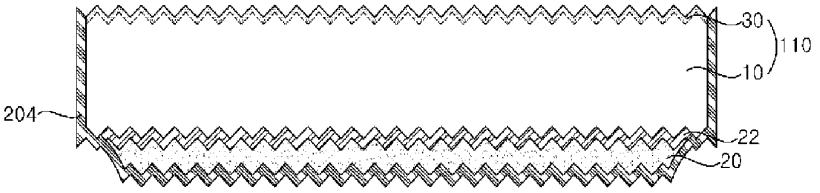

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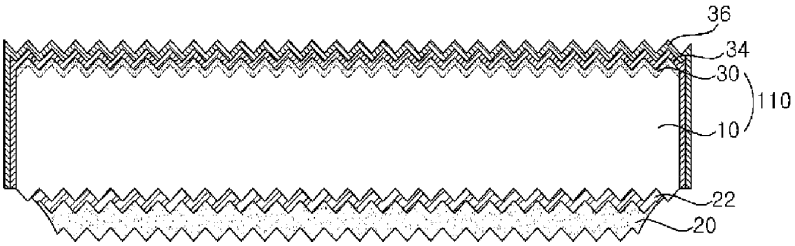

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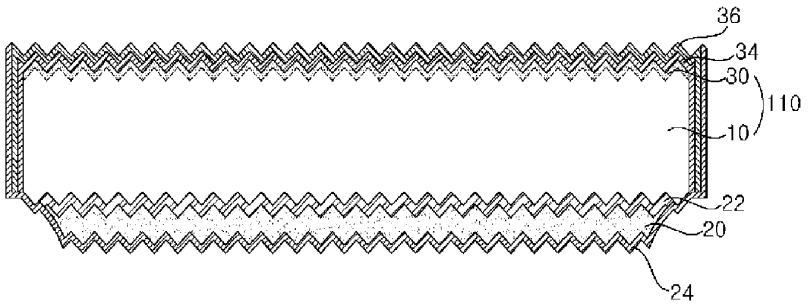

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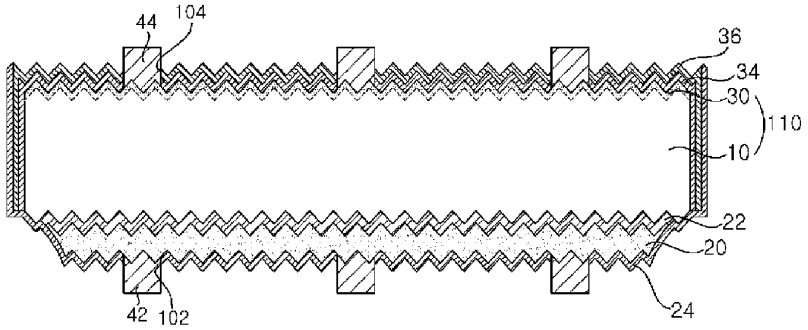

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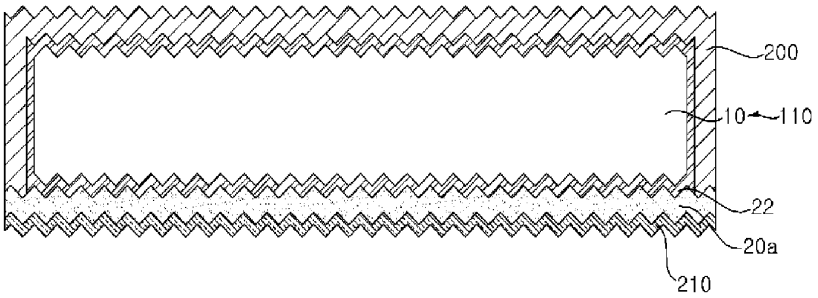

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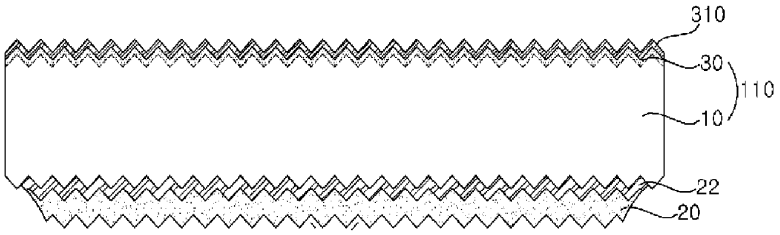

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	1

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First Named Inventor	Jungmin Ha
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Attorney Docket Number	1630-1332PUS2

U.S. PATENT DOCUMENTS

Examiner initial *	Cite No.	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initial *	Cite No. 1	Foreign Patent Document Country[3] Code	Number[4] Kind Code (if known)[5]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
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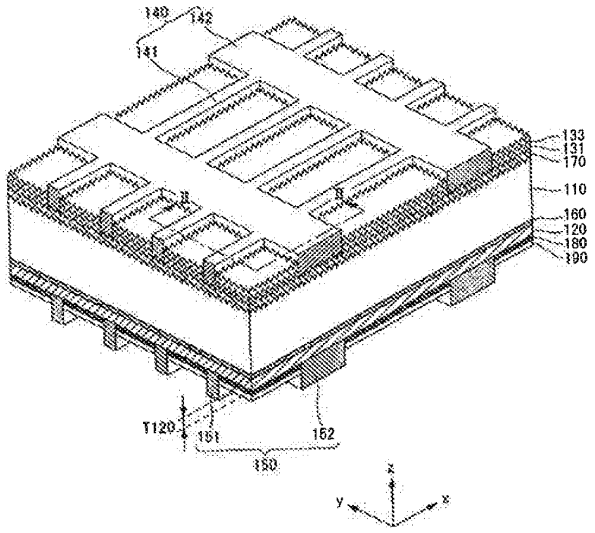
(54) SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME

(57) A solar cell and a method for manufacturing the same are disclosed. The solar cell includes a semiconductor substrate containing impurities of a first conductive type, a tunnel layer positioned on the semiconductor substrate, an emitter region positioned on the tunnel layer and containing impurities of a second conductive type opposite the first conductive type, a dopant layer positioned on the emitter region and formed of a dielectric material containing impurities of the second conductive type, a first electrode connected to the semiconductor substrate, and a second electrode configured to pass through the dopant layer and connected to the emitter region.

FIG. 1



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Description

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2014-0152372 filed in the Korean Intellectual Property Office on November 4, 2014, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present disclosure relates to a solar cell and a method for manufacturing the same.

Description of the Related Art

[0003] Recently, as existing energy sources such as petroleum and coal are expected to be depleted, interests in alternative energy sources for replacing the existing energy sources are increasing. Among the alternative energy sources, solar cells for generating electric energy from solar energy have been particularly spotlighted.

[0004] A solar cell generally includes semiconductor parts, which respectively have different conductive types, for example, a p-type and an n-type and thus form a p-n junction, and electrodes respectively connected to the semiconductor parts of the different conductive types.

[0005] When light is incident on the solar cell, a plurality of electron-hole pairs are produced in the semiconductor parts and are separated into electrons and holes by the incident light. The electrons move to the n-type semiconductor part, and the holes move to the p-type semiconductor part. Then, the electrons and the holes are collected by the different electrodes respectively connected to the n-type semiconductor part and the p-type semiconductor part. The electrodes are connected to each other using electric wires to thereby obtain electric power.

SUMMARY OF THE INVENTION

[0006] In one aspect, there is a solar cell including a semiconductor substrate containing impurities of a first conductive type, a tunnel layer positioned on the semiconductor substrate, an emitter region positioned on the tunnel layer and containing impurities of a second conductive type opposite the first conductive type, a dopant layer positioned on the emitter region and formed of a dielectric material containing impurities of the second conductive type, a first electrode connected to the semiconductor substrate, and a second electrode configured to pass through the dopant layer, and connected to the emitter region.

[0007] A doping concentration of the second conductive type impurities contained in the emitter region in a first portion of the emitter region contacting the second electrode may be higher than the doping concentration in a second portion of the emitter region contacting the tunnel layer.

[0008] A doping concentration of the second conductive type impurities contained in the emitter region may increase in the emitter region in going away from the tunnel layer.

[0009] More specifically, a first doping concentration of the second conductive type impurities in the first portion of the emitter region contacting the second electrode may be higher than a second doping concentration of the second conductive type impurities in the second portion of the emitter region contacting the tunnel layer.

[0010] For example, the first doping concentration may be $5*10^{19}/cm^3$ to $5*10^{21}/cm^3$, and the second doping concentration may be $5*10^{18}/cm^3$ to $5*10^{20}/cm^3$.

[0011] The doping concentration of the emitter region may successively decrease linearly or nonlinearly in the emitter region in going from the first portion to the second portion.

[0012] The emitter region may be formed of a polycrystalline silicon material. A crystallinity of the emitter region may increase in the emitter region in going away from the tunnel layer.

[0013] A thickness of the emitter region may be 50 nm to 150 nm, and a thickness of the dopant layer may be 25 nm to 150 nm.

[0014] The solar cell may further include a hydrogen injection layer positioned on a back surface of the dopant layer and formed of a dielectric material containing hydrogen at a higher concentration than that of the dopant layer.

[0015] The solar cell may further include a front surface field region positioned on a front surface of the semiconductor substrate and containing impurities of the first conductive type at a higher concentration than that of the semiconductor substrate. The tunnel layer, the emitter region, and the dopant layer may be positioned on a back surface of the semiconductor substrate.

[0016] In another aspect, there is a method for manufacturing a solar cell, the method including a layer forming operation of sequentially forming a tunnel layer, an intrinsic amorphous silicon layer, and a dopant layer on a back surface of a semiconductor substrate formed of a crystalline silicon material containing impurities of a first conductive type, the dopant layer being formed of a dielectric material containing impurities of a second conductive type opposite the first conductive type; a thermal processing operation of, after the layer forming operation, forming a front surface field region on a front surface of the semiconductor substrate through one successive thermal process, in which a temperature in a furnace is maintained or raised, recrystallizing the intrinsic amorphous silicon layer into an intrinsic polycrystalline silicon layer, and diffusing and activating the impurities of the second conductive type of the dopant layer into the recrystallized intrinsic polycrystalline silicon layer to form an emitter region; and an electrode forming operation of,

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after the thermal processing operation, forming a first electrode connected to the front surface of the semiconductor substrate and forming a second electrode connected to the emitter region.

[0017] The layer forming operation may further include a process for forming a capping layer formed of a dielectric material not containing impurities of the second conductive type on a back surface of the dopant layer.

[0018] The method may further include, between the thermal processing operation and the electrode forming operation, an operation of removing a capping layer formed on the back surface of the semiconductor substrate and an oxide layer formed on a front surface of the front surface field region in the thermal processing operation; and an operation of forming a hydrogen injection layer formed of a dielectric layer containing hydrogen on the back surface of the dopant layer, on which the capping layer is removed.

[0019] The forming of the emitter region may include a dehydrogenation process for removing hydrogen contained in the intrinsic amorphous silicon layer; a recrystallization process for recrystallizing the intrinsic amorphous silicon layer into the intrinsic polycrystalline silicon layer; and an emitter region activating process for diffusing and activating the impurities of the second conductive type contained in the dopant layer into the recrystallized intrinsic polycrystalline silicon layer.

[0020] The forming of the front surface field region may include a front surface field region activating process for diffusing and activating impurities of the first conductive type into the front surface of the semiconductor substrate. The front surface field region activating process may be performed along with the emitter region activating process.

[0021] The thermal processing operation may include a first thermal process for maintaining the temperature of the furnace at a first temperature, a second thermal process for changing the temperature of the furnace from the first temperature to a second temperature higher than the first temperature, a third thermal process for maintaining the temperature of the furnace at the second temperature, a fourth thermal process for changing the temperature of the furnace from the second temperature to a third temperature higher than the second temperature, and a fifth thermal process for maintaining the temperature of the furnace at the third temperature.

[0022] The first to fifth thermal processes may be successively performed in the same furnace.

[0023] A second thermal process time of the second thermal process may be longer than a first thermal process time of the first thermal process and a third thermal process time of the third thermal process. The third thermal process time may be equal to or longer than the first thermal process time.

[0024] For example, the first thermal process may maintain the temperature of the furnace at the first temperature of 350 °C to 450 °C for 5 minutes to 15 minutes. The third thermal process may maintain the temperature of the furnace at the second temperature of 500 °C to 600 °C for 10 minutes to 20 minutes.

[0025] The second thermal process may increase the temperature of the furnace from the first temperature to the second temperature for 15 minutes to 25 minutes.

[0026] The fifth thermal process may maintain the temperature of the furnace at the third temperature of 800 °C to 1000 °C for 15 minutes to 30 minutes. The fourth thermal process may increase the temperature of the furnace from the second temperature to the third temperature for 5 minutes to 15 minutes.

[0027] The dehydrogenation process may be performed through the first to third thermal processes. The recrystallization process may be performed through the fourth thermal process.

[0028] The emitter region activating process and the front surface field region activating process may be performed through the fifth thermal process.

[0029] The solar cell and the method for manufacturing the same according to the present disclosure are configured so that the doping concentration of impurities of the second conductive type contained in the emitter region increases as the emitter region is far away from the tunnel layer. Hence, a recombination of carriers in the emitter region can be reduced, and contact characteristic between the emitter region and the second electrode can be further improved.

[0030] Furthermore, the method for manufacturing the solar cell according to the present disclosure simultaneously forms the front surface field region and the emitter region through one successive thermal process, of which a temperature is maintained or raised, and thus can further reduce manufacturing time.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

FIGS. 1 and 2 illustrate a solar cell according to an example embodiment of the invention;

FIG. 3 illustrates a doping concentration of an emitter region of the solar cell shown in FIG. 1;

FIG. 4 illustrates a doping concentration of an emitter region according to a comparative example different from an example embodiment of the invention;

FIG. 5 is a flow chart illustrating a method for manufacturing a solar cell according to an example embodiment of the invention;

FIGS. 6A to 6E depicts reference figures of each stage illustrated in the flow chart of FIG. 5; and

FIG. 7 illustrates changes in a temperature over time in a thermal processing operation of a method for manufacturing a solar cell according to an example

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embodiment of the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0032] Reference will now be made in detail to embodiments of the invention, examples of which are illustrated in the accompanying drawings. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts. It will be noted that a detailed description of known arts will be omitted if it is determined that the detailed description of the known arts can obscure the embodiments of the invention.

[0033] In the drawings, the thickness of layers, films, panels, regions, etc., are exaggerated for clarity. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. Further, it will be understood that when an element such as a layer, film, region, or substrate is referred to as being "entirely" on other element, it may be on the entire surface of the other element and may not be on a portion of an edge of the other element.

[0034] In the following description, a "front surface" may be one surface of a semiconductor substrate, on which light is directly incident, and a "back surface" may be a surface opposite the one surface of the semiconductor substrate, on which light is not directly incident or reflective light may be incident.

[0035] Exemplary embodiments of the invention are described with reference to FIGS. 1 to 7.

[0036] FIGS. 1 and 2 illustrate a solar cell according to an example embodiment of the invention. More specifically, FIG. 1 is a partial perspective view of the solar cell according to the embodiment of the invention, and FIG. 2 is a cross-sectional view taken along line II-II of FIG. 1.

[0037] As shown in FIGS. 1 and 2, a solar cell according to the embodiment of the invention may include a semiconductor substrate 110, a tunnel layer 160, an emitter region 120, a dopant layer 180, a hydrogen injection layer 190, a front surface field region 170, a passivation layer 131, an anti-reflection layer 133, a first electrode 140, and a second electrode 150.

[0038] In the embodiment disclosed herein, the anti-reflection layer 133, the passivation layer 131, and the hydrogen injection layer 190 may be omitted, if desired or necessary. However, when the solar cell includes the anti-reflection layer 133, the passivation layer 131, and the hydrogen injection layer 190 as shown in FIGS. 1 and 2, efficiency of the solar cell may be further improved. Thus, the embodiment of the invention is described using the solar cell including the anti-reflection layer 133, the passivation layer 131, and the hydrogen injection layer 190 as an example.

[0039] The semiconductor substrate 110 may be formed of crystalline silicon material containing impurities of a first conductive type. For example, the semiconductor substrate 110 may be formed using a single crystal wafer or a polycrystalline wafer.

[0040] The impurities of the first conductive type may be p-type impurities, for example, impurities of a group III element, such as boron (B), gallium (Ga), and indium (In). Alternatively, the impurities of the first conductive type may be n-type impurities, for example, impurities of a group V element, such as phosphorus (P), arsenic (As), and antimony (Sb). The impurities of the first conductive type may be doped on the semiconductor substrate 110. In the following description, the embodiment of the invention is described using an example where the first conductive type is the n-type.

[0041] A front surface of the semiconductor substrate 110 may be textured to form a textured surface corresponding to an uneven surface having a plurality of uneven portions or having uneven characteristics, so as to minimize a reflectance of incident light.

[0042] When light is incident on the semiconductor substrate 110, electron-hole pairs are produced in the semiconductor substrate 110.

[0043] The tunnel layer 160 may be entirely formed on one surface, for example, a back surface of the semiconductor substrate 110. The tunnel layer 160 may pass through carriers produced in the semiconductor substrate 110 and may perform a passivation function with respect to the back surface of the semiconductor substrate 110.

[0044] The tunnel layer 160 may be formed of a dielectric material. More specifically, the tunnel layer 160 may be formed of silicon carbide (SiCx) or silicon oxide (SiOx) having strong durability at a high temperature equal to or higher than 600 °C. In addition, the tunnel layer 160 may be formed of silicon nitride (SiNx), hydrogenated SiNx, aluminum oxide (AlOx), silicon oxynitride (SiON), or hydrogenated SiON.

[0045] Unlike this, if the tunnel layer 160 is formed of a material including amorphous silicon (a-Si), the tunnel layer 160 cannot obtain a desired tunneling effect because amorphous silicon is weak or susceptible to the high temperature equal to or higher than 600 °C.

[0046] A thickness of the tunnel layer 160 may be 0.5 nm to 2.5 nm.

[0047] The emitter region 120 may directly contact the tunnel layer 160 and may be positioned on the entire back surface of the tunnel layer 160.

[0048] The emitter region 120 may be formed by doping impurities of a second conductive type opposite the first conductive type on a polycrystalline silicon material layer. For example, the emitter region 120 may be formed of polycrystalline silicon material containing impurities of the second conductive type.

[0049] In other words, the emitter region 120 may con-

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tain impurities of the second conductive type, for example, p-type impurities. For example, the emitter region 120 may contain impurities of a group III element, such as boron (B), gallium (Ga), and indium (In).

[0050] The emitter region 120 may form a p-n junction along with the semiconductor substrate 110 with the tunnel layer 160 interposed therebetween. In another example, if the first conductive type of the semiconductor substrate 110 is the p-type, the emitter region 120 may be of the n-type.

[0051] The polycrystalline silicon material layer of the emitter region 120 may be obtained by re-crystallizing an amorphous silicon material layer.

[0052] Accordingly, the polycrystalline silicon material of the emitter region 120 may have almost the same crystallinity throughout the emitter region 120. Alternatively, the crystallinity of the polycrystalline silicon material of the emitter region 120 may increase as the emitter region 120 is far away from the tunnel layer 160.

[0053] Namely, the crystallinity in a first portion PT1 of the emitter region 120 connected to the second electrode 150 may be relatively high, and the crystallinity in a second portion PT2 of the emitter region 120 closer to the tunnel layer 160 than the first portion PT1 may be relatively low.

[0054] Accordingly, a contact resistance between the emitter region 120 and the second electrode 150 may be further improved by the relatively higher crystallinity in the first portion PT1 of the emitter region 120 connected to the second electrode 150.

[0055] When the emitter region 120 including the re-crystallized polycrystalline silicon material is formed at the back surface of the tunnel layer 160 in a state where the tunnel layer 160 is positioned on the back surface of the semiconductor substrate 110, an open-circuit voltage of the solar cell may be further improved, and a damage of the semiconductor substrate 110 resulting from heat generated in a manufacturing process of the solar cell may be minimized. Hence, the solar cell with high efficiency may be implemented.

[0056] A thickness T120 of the emitter region 120 may be 50 nm to 150 nm.

[0057] When the thickness T120 of the emitter region 120 is equal to or greater than 50 nm, a function of the emitter region 120 forming the p-n junction along with the semiconductor substrate 110 may be secured. When the thickness T120 of the emitter region 120 is equal to or less than 150 nm, a process time may be minimized through the optimization of the thickness T120 of the emitter region 120 while the function of the emitter region 120 is maintained. Other thicknesses may be used for the emitter region 120.

[0058] A doping concentration of the impurities of the second conductive type contained in the emitter region 120 may increase as the emitter region 120 is far away from the tunnel layer 160. Hence, carriers are recombined in the second portion PT2 of the emitter region 120 relatively closer to the semiconductor substrate 110 due to the impurities of the second conductive type, and a loss amount of carriers may be further reduced. As a result, passivation characteristic may be further improved. Further, the contact resistance between the emitter region 120 and the second electrode 150 may be further improved in the first portion PT1 of the emitter region 120 connected to the second electrode 150 due to a relatively higher doping concentration.

[0059] Changes in the doping concentration of the emitter region 120 will be separately described in detail with reference to FIG. 3.

[0060] The dopant layer 180 is positioned on the emitter region 120 and may contain impurities of the second conductive type. A dielectric material of the dopant layer 180 may include at least one of silicon nitride (SiNx), silicon oxide (SiOx), silicon oxynitride (SiOxNy), silicon carbide (SiCx), or aluminum oxide (AlOx). Thus, the dopant layer 180 may contain SiOx:B containing boron (B) as an example of the impurities of the second conductive type.

[0061] The dopant layer 180 functions to diffuse the impurities of the second conductive type contained in the dielectric material into an intrinsic polycrystalline silicon layer in a process for forming the emitter region 120. After the emitter region 120 is formed, the dopant layer 180 receives hydrogen from the hydrogen injection layer 190 formed on a back surface of the dopant layer 180 and may perform a passivation function with respect to the back surface of the emitter region 120.

[0062] A thickness of the dopant layer 180 may be 25 nm to 150 nm. When the thickness of the dopant layer 180 is equal to or greater than 25 nm, a minimum amount of impurities of the second conductive type to be diffused into the emitter region 120 may be secured. When the thickness of the dopant layer 180 is equal to or less than 150 nm, the process time may be minimized through the optimization of the thickness of the dopant layer 180 while an amount of impurities of the second conductive type is properly secured. Further, an effusion speed of hydrogen contained in the intrinsic polycrystalline silicon layer for forming the emitter region 120 may be properly controlled in a dehydrogenation process. Other thicknesses may be used for the dopant layer 180.

[0063] The hydrogen injection layer 190 positioned on the back surface of the dopant layer 180 may be formed of a dielectric material containing hydrogen at a higher concentration than the dielectric material of the dopant layer 180.

[0064] After the formation of the emitter region 120 is completed, the hydrogen injection layer 190 may be formed on the back surface of the dopant layer 180. In an electrode forming operation involving a thermal processing, hydrogen of the high concentration contained in the hydrogen injection layer 190 may be diffused into the dopant layer 180, so that the dopant layer 180 has the passivation function.

[0065] The hydrogen injection layer 190 may have a refractive index different from the dopant layer 180, so

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that light, which is incident on the solar cell and is transmitted by the semiconductor substrate 110, is again incident on the semiconductor substrate 110.

[0066] The dielectric material of the hydrogen injection layer 190 may include at least one of SiNx, SiOx, SiOxNy, SiCx, or AlOx.

[0067] The front surface field region 170 is positioned at the front surface of the semiconductor substrate 110 and may be more heavily doped than the semiconductor substrate 110 with impurities of the first conductive type.

[0068] The front surface field region 170 may be formed by diffusing impurities of the first conductive type into the front surface of the semiconductor substrate 110. Hence, the front surface field region 170 may be formed of the same crystalline silicon material as the semiconductor substrate 110.

[0069] For example, when the semiconductor substrate 110 is formed of a single crystal silicon material, the front surface field region 170 may be formed of the single crystal silicon material. Alternatively, when the semiconductor substrate 110 is formed of a polycrystalline silicon material, the front surface field region 170 may be formed of the polycrystalline silicon material.

[0070] The passivation layer 131 is positioned directly on a front surface of the front surface field region 170 and may perform a passivation function with respect to the front surface of the front surface field region 170. The passivation layer 131 may be formed of a dielectric material containing hydrogen. For example, the passivation layer 131 may be formed of at least one of SiNx, SiOx, SiOxNy, or AlOx.

[0071] The anti-reflection layer 133 is positioned on a front surface of the passivation layer 131. The anti-reflection layer 133 may improve transmission of light incident on the solar cell and reduce a reflectance of the light. Hence, the anti-reflection layer 133 may make a large amount of light be incident on the semiconductor substrate 110.

[0072] The anti-reflection layer 133 may be formed of a dielectric material containing hydrogen. For example, the anti-reflection layer 133 may be formed of at least one of SiNx, SiOx, SiOxNy, or AlOx.

[0073] The first electrode 140 is positioned on the front surface of the semiconductor substrate 110. The first electrode 140 may pass through the anti-reflection layer 133 and the passivation layer 131 and may be connected to the front surface field region 170.

[0074] The first electrode 140 may include a plurality of first finger electrodes 141 and a plurality of first bus bars 142 connected to the plurality of first finger electrodes 141.

[0075] The first finger electrodes 141 may be electrically and physically connected to the front surface field region 170. The first finger electrodes 141 may be separated from one another and may extend in parallel with one another in a first direction x. The first finger electrodes 141 may collect carriers (for example, electrons) moving to the front surface field region 170.

[0076] The first bus bars 142 may be electrically and physically connected to the emitter region 120 and may extend in parallel with one another in a second direction y crossing the first finger electrodes 141.

[0077] The first bus bar 142 may be positioned on the same layer as the first finger electrode 141 and may be electrically and physically connected to the first finger electrode 141 at a location crossing the first finger electrode 141.

[0078] As shown in FIG. 1, the plurality of first finger electrodes 141 may have a stripe shape extending in the first direction x, and the plurality of first bus bars 142 may have a stripe shape extending in the second direction y. Hence, the first electrode 140 may have a lattice shape at the front surface of the semiconductor substrate 110.

[0079] The plurality of first bus bars 142 may collect not only carrier moving from the front surface field region 170 contacting the first bus bars 142 but also carriers collected by the plurality of first finger electrodes 141.

[0080] The first bus bars 142 have to collect carriers collected by the first finger electrodes 141 crossing the first bus bars 142 and have to move the collected carriers in a desired direction. Therefore, a width of each first bus bar 142 may be greater than a width of each first finger electrode 141.

[0081] The plurality of first bus bars 142 may be connected to an external device and may output the collected carriers (for example, electrons) to the external device.

[0082] The plurality of first finger electrodes 141 and the plurality of first bus bars 142 of the first electrode 140 may be formed of at least one conductive material, for example, silver (Ag).

[0083] The second electrode 150 is positioned on the back surface of the semiconductor substrate 110. The second electrode 150 may pass through the dopant layer 180 and the hydrogen injection layer 190 and may be connected to the emitter region 120.

[0084] As shown in FIGS. 1 and 2, the second electrode 150 may include a plurality of second finger electrodes 151 and a plurality of second bus bars 152 connected to the plurality of second finger electrodes 151 in the same manner as the first electrode 140. The second electrode 150 may have the same pattern as the first electrode 140. Other patterns may be used for the second electrode 150.

[0085] The second electrode 150 may collect carriers (for example, holes) moving to the emitter region 120.

[0086] FIGS. 1 and 2 show that the emitter region 120 is positioned on the back surface of the semiconductor substrate 110 and the front surface field region 170 is positioned on the front surface of the semiconductor substrate 110, as an example. In another example, the emitter region 120 may be positioned on the front surface of the semiconductor substrate 110, and the front surface field region 170 may be positioned on the back surface of the semiconductor substrate 110. The another example may be equally applied to the embodiment of the invention.

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[0087] In the solar cell according to the embodiment of the invention, the doping concentration of the impurities of the second conductive type contained in the emitter region 120 may entirely increase as the emitter region 120 is far away from the tunnel layer 160.

[0088] This is described in detail below with reference to FIG. 3.

[0089] FIG. 3 illustrates a doping concentration of the emitter region of the solar cell shown in FIG. 1. FIG. 4 illustrates a doping concentration of an emitter region according to a comparative example different from the embodiment of the invention.

[0090] More specifically, FIGS. 3 and 4 show an example of a doping concentration depending on the cross-section of the emitter region 120 and the semiconductor substrate 110. In FIGS. 3 and 4, x-axis denotes a depth toward the semiconductor substrate 110 from the back surface of the emitter region 120 contacting the second electrode 150, and y-axis denotes a doping concentration.

[0091] FIG. 3 shows an example of the doping concentration when the thickness T120 of the emitter region 120 is about 150 nm, for example. However, the thickness T120 of the emitter region 120 may be variously determined between 50 nm and 150 nm. Further, the doping concentration shown in FIG. 3 is merely an example and thus may be variously changed.

[0092] As shown in FIG. 3, the doping concentration of the emitter region 120 according to the embodiment of the invention may be higher than a doping concentration of the semiconductor substrate 110.

[0093] A first doping concentration C1 of second conductive type impurities in the first portion PT1 (at a depth of 0 nm) of the emitter region 120 contacting the second electrode 150 may be higher than a second doping concentration C2 of second conductive type impurities in the second portion PT2 (at a depth of 150 nm) of the emitter region 120 contacting the tunnel layer 160.

[0094] The first portion PT1 indicates a contact portion of the emitter region 120 and the second electrode 150 or a contact portion of the emitter region 120 and the dopant layer 180. The second portion PT2 indicates a contact portion of the emitter region 120 and the tunnel layer 160.

[0095] In FIG. 3, for example, the first doping concentration C1 is $1.2*10^{21}/cm^3$, and the second doping concentration C2 is $1.3*10^{20}/cm^3$. However, the first doping concentration C1 may be determined between $5*10^{19}/cm^3$ and $5*10^{21}/cm^3$, and the second doping concentration C2 may be determined between $5*10^{18}/cm^3$ and $5*10^{20}/cm^3$ and may be lower than the first doping concentration C1.

[0096] The doping concentration of the emitter region 120 may increase as the emitter region 120 is far away from the tunnel layer 160. More specifically, as the emitter region 120 goes from the first portion PT1 to the second portion PT2, the doping concentration of the emitter region 120 may successively decrease linearly or nonlinearly.

[0097] In FIG. 3, for example, as the emitter region 120 goes from the first portion PT1 to the second portion PT2, the doping concentration of the emitter region 120 successively and nonlinearly decreases from the first doping concentration C1 to the second doping concentration C2. However, the doping concentration of the emitter region 120 may successively and linearly decrease.

[0098] The characteristic of the emitter region 120, in which the doping concentration of the emitter region 120 increases as the emitter region 120 is far away from the tunnel layer 160, may be generated in a thermal processing operation of diffusing the second conductive type impurities of the dopant layer 180 into a polycrystalline silicon layer recrystallized through a process for recrystallizing an intrinsic amorphous silicon layer into a polycrystalline silicon layer by performing one successive thermal process, of which the temperature changes, in a state where an intrinsic amorphous silicon layer is firstly formed. Hence, the emitter region 120 is formed.

[0099] In the second portion PT2 of the emitter region 120 relatively close to the semiconductor substrate 110, carriers may be recombined by impurities, and a loss amount of carriers may be further reduced due to the above characteristic of the emitter region 120, in which the doping concentration of the emitter region 120 increases as the emitter region 120 is far away from the tunnel layer 160. Hence, the passivation characteristic may be further improved. In the first portion PT1 of the emitter region 120 connected to the second electrode 150, the contact resistance between the emitter region 120 and the second electrode 150 may be further improved due to the relatively higher doping concentration of the emitter region 120.

[0100] Unlike the embodiment of the invention shown in FIG. 3, in the comparative example of FIG. 4, when impurities of the second conductive type are diffused in a state an intrinsic polycrystalline silicon layer is deposited and formed, a doping concentration of the emitter region 120 does not entirely increase as the emitter region 120 goes from the first portion PT1 to the second portion PT2. In this instance, the doping concentration of the emitter region 120 slightly changes, but is entirely uniform around $1.5*10^{20}/cm^3$.

[0101] It may be difficult for the comparative example of FIG. 4 to secure the same effect as the embodiment of the invention. Namely, when the comparative example increases the doping concentration so as to improve the contact characteristic between the emitter region 120 and the second electrode 150, an amount of carriers recombined in the emitter region 120 may increase because the doping concentration of the emitter region 120 itself entirely increases. Hence, the characteristic of the emitter region 120 may be reduced. When the comparative example decreases the doping concentration so as to improve the characteristic of the emitter region 120, the contact resistance between the emitter region 120 and the second electrode 150 may increase. Hence, charac-

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teristic of a short circuit current of the solar cell may be reduced.

[0102] So far, the embodiment of the invention described an example of the structure of the solar cell. Hereinafter, the embodiment of the invention will describe an example of a method for manufacturing the solar cell.

[0103] FIG. 5 is a flow chart illustrating a method for manufacturing the solar cell according to the embodiment of the invention. FIGS. 6A to 6E depicts reference figures of each stage illustrated in the flow chart of FIG. 5.

[0104] As shown in FIG. 5, the method for manufacturing the solar cell according to the embodiment of the invention may include a layer forming operation S1, a thermal processing operation S2, an operation S3 of removing a capping layer and an oxide layer, a hydrogen injection layer forming operation S4, and an electrode forming operation S5.

[0105] The operation S3 for removing a capping layer and an oxide layer and the hydrogen injection layer formation operation S4 may be omitted, if necessary or desired. However, when the method for manufacturing the solar cell includes the operations S3 and S4, the efficiency of the solar cell thus manufactured may be further improved. Thus, the embodiment of the invention is described using the method for manufacturing the solar cell including the operations S3 and S4 as an example.

[0106] As shown in FIG. 5, in the layer forming operation S1, a tunnel layer forming process P1, an intrinsic amorphous silicon layer forming process P2, a dopant layer forming process P3, and a capping layer forming process P4 may be performed.

[0107] More specifically, referring to FIG. 6A, in the tunnel layer forming process P1, SiCx or SiOx may be deposited on the back surface of the semiconductor substrate 110 formed of crystalline silicon material containing impurities of the first conductive type to form the tunnel layer 160 on the entire back surface of the semiconductor substrate 110.

[0108] Next, in the intrinsic amorphous silicon layer forming process P2, an intrinsic amorphous silicon layer 120A may be formed on the entire back surface of the tunnel layer 160 through the deposition. In this instance, a thickness of the intrinsic amorphous silicon layer 120A may be determined between 50 nm and 150 nm.

[0109] Next, in the dopant layer forming process P3, the dopant layer 180 formed of a dielectric material containing impurities of the second conductive type, for example, boron (B) may be formed on an entire back surface of the intrinsic amorphous silicon layer 120A. In this instance, a thickness of the dopant layer 180 may be determined between 25 nm and 150 nm.

[0110] Next, a capping layer CAP formed of a dielectric material not containing impurities of the second conductive type may be formed on the entire back surface of the dopant layer 180. The dielectric material forming the capping layer CAP may be at least one of SiOx, SiNx, SiOxNy, or SiCx not containing impurities of the second conductive type. For example, it may be more advantageous in the manufacturing process that the capping layer CAP is formed of SiOx so as to easily perform the subsequent operation S3 of removing the capping layer and the oxide layer.

[0111] In a front surface field region forming process P5 of the subsequent thermal processing operation S2, the capping layer CAP may prevent impurities of the first conductive type from being diffused into the intrinsic amorphous silicon layer 120A. When a dehydrogenation process P61 of the subsequent thermal processing operation S2 is performed, the capping layer CAP may control an amount and a speed of hydrogen emitted from the intrinsic amorphous silicon layer 120A.

[0112] In this instance, a sum of a thickness of the capping layer CAP and the thickness of the dopant layer 180 may be determined between 50 nm and 150 nm.

[0113] Thus, when the thickness of the dopant layer 180 is 150 nm, the capping layer forming process P4 may be omitted.

[0114] The tunnel layer forming process P1, the intrinsic amorphous silicon layer forming process P2, the dopant layer forming process P3, and the capping layer forming process P4 of the layer forming operation S1 may be performed in-situ.

[0115] Namely, the processes P1 to P4 of the layer forming operation S1 may be successively performed while moving in a vacuum state between chambers, in which each of the processes P1 to P4 is performed in a vacuum state without being exposed in an atmosphere between the processes P1 to P4. Hence, the process time may be further reduced.

[0116] It is preferable, but not required, that the layer forming operation S1 may be performed using a plasma enhanced chemical vapor deposition (PECVD) method performed at a temperature equal to or lower than 300 °C. Alternatively, an atmospheric pressure chemical vapor deposition (APCVD) method or a low pressure chemical vapor deposition (LPCVD) method may be used.

[0117] After the layer forming operation S1 is performed, the thermal processing operation S2 may be performed.

[0118] The thermal processing operation S2 may be performed in a furnace through one successive thermal process, so as to form the front surface field region 170 and the emitter region 120.

[0119] The one successive thermal process, of which a temperature is maintained or raised, is to successively provide a thermal process, of which a temperature is maintained or raised without a fall in the temperature during a period of the thermal processing operation S2. When the temperature falls, one cycle of one thermal processing operation S2 is completed. The thermal process for maintaining or raising the temperature may be performed several times.

[0120] Accordingly, the thermal processing operation S2 according to the embodiment of the invention forms the front surface field region 170 and the emitter region 120 through only the one successive thermal process, in

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which the temperature does not fall and is maintained or raised, in one furnace. Hence, manufacturing time may be further reduced.

[0121] The successive thermal process, of which the temperature is maintained or raised, is described in detail later with reference to FIG. 7.

[0122] In the thermal processing operation S2, the front surface field region forming process P5 for forming the front surface field region 170 on the front surface of the semiconductor substrate 110 and an emitter region forming process P6 for recrystallizing the intrinsic amorphous silicon layer 120A into an intrinsic polycrystalline silicon layer 120C and diffusing impurities of the second conductive type of the dopant layer 180 into the recrystallized intrinsic polycrystalline silicon layer 120C to form the emitter region 120 may be performed together.

[0123] The front surface field region forming process P5 may include an impurity injection process P51 and a front surface field region activating process P52.

[0124] In the impurity injection process P51, $POCl_3$ gas containing impurities of the first conductive type may be injected into the furnace. In the front surface field region activating process P52, as shown in FIG. 6B, phosphorus (P) corresponding to impurities of the first conductive type in the $POCl_3$ gas may be diffused into the front surface of the semiconductor substrate 110 and activated.

[0125] In this instance, phosphorus (P) of the $POCl_3$ gas may be prevented from being diffused into the intrinsic amorphous silicon layer 120A or the intrinsic polycrystalline silicon layer 120C by the capping layer CAP and the dopant layer 180 on the back surface of the semiconductor substrate 110.

[0126] The front surface field region activating process P52 may be performed through a thermal process of 800 °C to 1000 °C.

[0127] An oxide layer SOL may be unnecessarily formed on the front surface of the front surface field region 170 in the front surface field region activating process P52. The oxide layer SOL may be removed together when the capping layer CAP is removed later.

[0128] The embodiment of the invention described that the front surface field region forming process P5 of the thermal processing operation S2 in the flow chart shown in FIG. 5 includes the impurity injection process P51 for injecting the $POCl_3$ gas containing impurities of the first conductive type into the furnace, as an example. However, a dopant source may be formed.

[0129] Namely, the front surface field region forming process P5 may apply a dopant paste containing impurities of the first conductive type or form the dopant paste on the front surface of the semiconductor substrate 110 in a SOD (spin on dopant) method instead of performing the impurity injection process P51 before the thermal processing operation S2 after the layer forming operation S1, and then may diffuse and activate the impurities of the first conductive type into the front surface of the semiconductor substrate 110 in the front surface field region activating process P52 of the thermal processing operation S2.

[0130] Alternatively, the front surface field region forming process P5 may previously implant the dopant paste formed on the front surface of the semiconductor substrate 110 onto the front surface of the semiconductor substrate 110 using a laser irradiation device before the thermal processing operation S2 after the layer forming operation S1, and then may perform the front surface field region activating process P52.

[0131] Next, the emitter region forming process P6 may include the dehydrogenation process P61, a recrystallization process P62, and an emitter region activating process P63.

[0132] The dehydrogenation process P61 is a thermal process for removing hydrogen contained in the intrinsic amorphous silicon layer 120A. In other words, the dehydrogenation process P61 diffuses hydrogen contained in the intrinsic amorphous silicon layer 120A by increasing a temperature of the furnace and discharges hydrogen to the outside of the intrinsic amorphous silicon layer 120A through the dopant layer 180 and the capping layer CAP.

[0133] When an amount or a speed of discharging of the hydrogen contained in the intrinsic amorphous silicon layer 120A is excessively large, the intrinsic amorphous silicon layer 120A may be damaged. On the contrary, when the amount or the speed is small, the manufacturing time may increase. It is preferable, but not required, that the temperature in the furnace is optimized so as to optimize the amount or the speed of the discharging of the hydrogen.

[0134] In this instance, the temperature in the furnace may be controlled between 350 °C and 600 °C, for example.

[0135] The recrystallization process P62 is a process for recrystallizing the intrinsic amorphous silicon layer 120A into the intrinsic polycrystalline silicon layer 120C. The recrystallization process P62 may be performed by further increasing the temperature of the furnace when the dehydrogenation process P61 is almost completed. In the recrystallization process P62, the intrinsic amorphous silicon layer 120A may start to be recrystallized between about 600 °C and 650 °C.

[0136] Thus, the recrystallization process P62 may be performed at a temperature higher than the dehydrogenation process P61 and may be successively performed subsequent to the dehydrogenation process P61. The recrystallization process P62 may be performed by increasing the temperature of the furnace by about 800 °C to 1000 °C from a temperature of the dehydrogenation process P61.

[0137] Through the recrystallization process P62, the crystallization of the intrinsic amorphous silicon layer 120A may start from the first portion PT1 contacting the dopant layer 180 and may be proceeded toward the second portion PT2 contacting the tunnel layer 160.

[0138] Thus, the crystallinity of the first portion PT1 may be higher than the crystallinity of the second portion

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PT2. Further, as the emitter region 120 goes from the first portion PT1 to the second portion PT2, the crystallinity may gradually decrease. However, a reduction pattern of the crystallinity may be differently formed depending on time and the temperature of the recrystallization process P62.

[0139] The emitter region activating process P63 is a process for diffusing and activating impurities of the second conductive type contained in the dopant layer 180 shown in FIG. 6B into the recrystallized intrinsic polycrystalline silicon layer 120C. The emitter region activating process P63 may be performed by maintaining a maximum temperature of the recrystallization process P62.

[0140] Namely, the emitter region activating process P63 may be performed by maintaining the temperature of the furnace at 800 °C to 1000 °C.

[0141] The emitter region 120, in which impurities of the second conductive type are doped on the intrinsic polycrystalline silicon layer 120C through the emitter region activating process P63, may be completed.

[0142] During the emitter region activating process P63, the recrystallization process P62 may be continuously performed. Because impurities of the second conductive type are diffused from the first portion PT1 contacting the dopant layer 180 toward the second portion PT2 contacting the tunnel layer 160, the first doping concentration C1 of the first portion PT1 may be higher than the second doping concentration C2 of the second portion PT2. The doping concentration of the second conductive type impurities may successively decrease as the emitter region 120 goes from the first portion PT1 to the second portion PT2.

[0143] As described above, the thermal processing operation S2 for simultaneously forming the emitter region 120 and the front surface field region 170 may be performed through one successive thermal process, of which the temperature is maintained or raised. The one successive thermal process, of which the temperature is maintained or raised, may greatly reduce the manufacturing time of the solar cell and may improve the efficiency of the solar cell.

[0144] As shown in FIG. 5, after the thermal processing operation S2 is completed, the operation S3 of removing the capping layer and the oxide layer and the hydrogen injection layer forming operation S4 may be performed before the electrode forming operation S5. However, the above operations are not necessary, and some of the above operations may be omitted.

[0145] In the operation S3 of removing the capping layer and the oxide layer, as shown in FIG. 6C, the capping layer CAP formed on the back surface of the semiconductor substrate 110 and the oxide layer SOL formed on the front surface of the semiconductor substrate 110 in the thermal processing operation S2 may be removed using a general etchant removing the oxide layer SOL.

[0146] In the embodiment disclosed herein, when the capping layer CAP is formed of, for example, SiOx, the operation S3 of removing the capping layer and the oxide layer may be more easily performed using the same etchant as the etchant removing the oxide layer SOL.

[0147] If the capping layer CAP is omitted in the layer forming operation S1, the operation of removing the capping layer CAP may be omitted.

[0148] Next, in the hydrogen injection layer forming operation S4, as shown in FIG. 6D, the hydrogen injection layer 190 which is formed of the dielectric material containing hydrogen at the high concentration, may be formed on the back surface of the dopant layer 180, on which the capping layer CAP is removed.

[0149] Because the hydrogen injection layer 190 contains hydrogen at the high concentration, the passivation function of the dopant layer 180 and the tunnel layer 160 may be improved by supplying hydrogen to the dopant layer 180 and the tunnel layer 160 in the subsequent electrode forming operation S5.

[0150] In this instance, a hydrogen concentration of the hydrogen injection layer 190 may be equal to or higher than a hydrogen concentration of the dopant layer 180, to which hydrogen is supplied.

[0151] Further, as shown in FIG. 6D, a first electrode paste P140 for forming the first electrode 140 and a second electrode paste P150 for forming the second electrode 150 may be respectively patterned and applied on the front surface and the back surface of the semiconductor substrate 110 in a state where the passivation layer 131 and the anti-reflection layer 133 are formed on the front surface of the front surface field region 170.

[0152] Next, as shown in FIGS. 5 and 6E, in the electrode forming operation S5, the first electrode paste P140 may pass through the passivation layer 131 and the anti-reflection layer 133 through the thermal processing of the semiconductor substrate 110 to form the first electrode 140 connected to the front surface of the semiconductor substrate 110. Further, the second electrode paste P150 may pass through the hydrogen injection layer 190 and the dopant layer 180 through the thermal processing of the semiconductor substrate 110 to form the second electrode 150 connected to the emitter region 120.

[0153] The embodiment of the invention mainly described the method forming each of the components of the solar cell so as to describe the method for manufacturing the solar cell. Hereinafter, one successive thermal process, of which the temperature of the thermal processing operation S2 is maintained or raised, is described in detail.

[0154] FIG. 7 illustrates changes in a temperature over time in the thermal processing operation S2 of the method for manufacturing the solar cell according to the embodiment of the invention.

[0155] As shown in FIG. 7, a plurality of thermal processes may constitute one thermal processing operation S2. Namely, the plurality of thermal processes may form one cycle of the thermal processing operation S2.

[0156] The thermal processing operation S2 according to the embodiment of the invention may include first to

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sixth thermal processes HT1 to HT6. More specifically, as shown in FIG. 7, the temperature of the thermal processing operation S2 does not fall and is maintained or raised in the first to fifth thermal processes HT1 to HT5 and falls in the sixth thermal process HT6. Hence, one successive thermal operation S2, of which the temperature changes, may be performed.

[0157] The first to sixth thermal processes HT1 to HT6 may be successively performed in the same furnace.

[0158] More specifically, as shown in FIG. 7, a temperature of the furnace in the first thermal process HT1 may be maintained at a first temperature K1, and the temperature of the furnace in the second thermal process HT2 may increase from the first temperature K1 to a second temperature K2 higher than the first temperature K1. The temperature of the furnace in the third thermal process HT3 may be maintained at the second temperature K2.

[0159] The dehydrogenation process P61 of the intrinsic semiconductor layer may be performed in the first to third thermal processes HT1 to HT3.

[0160] In the embodiment disclosed herein, a second thermal process time T2 of the second thermal process HT2 may be longer than a first thermal process time T1 of the first thermal process HT1 and a third thermal process time T3 of the third thermal process HT3, and the third thermal process time T3 may be equal to or longer than the first thermal process time T1.

[0161] More specifically, as shown in FIG. 7, the first thermal process HT1 may maintain the temperature of the furnace at the first temperature K1 of 350 °C to 450 °C for the first thermal process time T1 of 5 minutes to 15 minutes. The third thermal process HT3 may maintain the temperature of the furnace at the second temperature K2 of 500 °C to 600 °C for the third thermal process time T3 of 10 minutes to 20 minutes, which is equal to or longer than the first thermal process timeT1.

[0162] The second thermal process HT2 may increase the temperature of the furnace from the first temperature K1 to the second temperature K2 for the second thermal process time T2 of 15 minutes to 25 minutes, which is longer than the first thermal process timeT1 and the third thermal process timeT3.

[0163] The dehydrogenation process P61 of the intrinsic amorphous silicon layer 120A may be optimally performed depending on the temperature and the process time of the first to third thermal processes HT1 to HT3.

[0164] The fourth thermal process HT4 may increase the temperature of the furnace from the second temperature K2 to a third temperature K3 of 800 °C to 1000 °C higher than the second temperature K2 for a fourth thermal process time T4 of 5 minutes to 15 minutes.

[0165] The intrinsic amorphous silicon layer 120A may be recrystallized through the fourth thermal process HT4 and may be changed into the intrinsic polycrystalline silicon layer 120C.

[0166] The fifth thermal process HT5 may maintain the temperature of the furnace at the third temperature K3 of 800 °C to 1000 °C for a fifth thermal process time T5 of 15 minutes to 30 minutes, thereby diffusing and activating boron (B) corresponding to the second conductive type impurities of the dopant layer 180 into the recrystallized intrinsic polycrystalline silicon layer 120C. Hence, the emitter region 120 may be formed. Further, phosphorus (P) corresponding to the first conductive type impurities of $POCl_3$ gas injected into the furnace may be diffused and activated into the front surface of the semiconductor substrate 110 to form the front surface field region 170.

[0167] Namely, the recrystallization process P62 and the emitter region activating process P63 may be continuously performed together in the fifth thermal process HT5.

[0168] As described above, the method for manufacturing the solar cell according to the embodiment of the invention may simultaneously perform the emitter region activating process P63 and the front surface field region activating process P52 through the fifth thermal process HT5.

[0169] Next, the sixth thermal process HT6 may reduce the temperature of the furnace from the third temperature K3 to the first temperature K1 for a sixth thermal process time T6. Hence, one thermal processing operation S2 may be completed. The sixth thermal process time T6 is not particularly limited.

[0170] The method for manufacturing the solar cell according to the embodiment of the invention may diffuse and activate the first conductive type impurities and the second conductive type impurities through only one thermal process of the high temperature, unlike the general manufacturing method using at least two thermal processes performed at a high temperature equal to or higher than 800 °C. Hence, a degradation of the semiconductor substrate 110 may be prevented, and an open-circuit voltage and the efficiency of the solar cell may be further improved.

[0171] The embodiment of the invention may diffuse and activate the second conductive type impurities at the same time as the recrystallization of the intrinsic amorphous silicon layer 120A into the intrinsic polycrystalline silicon layer 120C. Thus, the doping concentration of the emitter region 120 may increase as the emitter region 120 is far away from the tunnel layer 160.

[0172] Accordingly, the embodiment of the invention may further simplify the manufacturing process of the solar cell and may further improve the efficiency of the solar cell.

[0173] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations

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and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

Claims

1. A solar cell comprising:

   a semiconductor substrate containing impurities of a first conductive type;
   a tunnel layer positioned on the semiconductor substrate;
   an emitter region positioned on the tunnel layer and containing impurities of a second conductive type opposite the first conductive type;
   a dopant layer positioned on the emitter region and formed of a dielectric material containing impurities of the second conductive type;
   a first electrode connected to the semiconductor substrate; and
   a second electrode configured to pass through the dopant layer, and connected to the emitter region.

2. The solar cell of claim 1, wherein a doping concentration of the second conductive type impurities contained in the emitter region in a first portion of the emitter region contacting the second electrode is higher than the doping concentration in a second portion of the emitter region contacting the tunnel layer,
   wherein a first doping concentration of the second conductive type impurities in a first portion of the emitter region contacting the second electrode is $5*10^{19}/cm^3$ to $5*10^{21}/cm^3$, and
   wherein a second doping concentration of the second conductive type impurities in a second portion of the emitter region contacting the tunnel layer is lower than the first doping concentration, and is $5*10^{18}/cm^3$ to $5*10^{20}/cm^3$.

3. The solar cell of claim 1 or 2, wherein a doping concentration of the second conductive type impurities contained in the emitter region increases in the emitter region in going away from the tunnel layer, and
   wherein the doping concentration of the emitter region successively decreases linearly or nonlinearly in the emitter region in going from the first portion to the second portion.

4. The solar cell of any one preceding claim, wherein the emitter region is formed of a polycrystalline silicon material, and
   wherein a crystallinity of the emitter region increases in the emitter region in going away from the tunnel layer.

5. The solar cell of any one preceding claim, wherein a thickness of the emitter region is 50 nm to 150 nm, and
   wherein a thickness of the dopant layer is 25 nm to 150 nm.

6. The solar cell of any one preceding claim, further comprising
   a hydrogen injection layer positioned on a back surface of the dopant layer and formed of a dielectric material containing hydrogen at a higher concentration than that of the dopant layer, and
   a front surface field region positioned on a front surface of the semiconductor substrate and containing impurities of the first conductive type at a higher concentration than that of the semiconductor substrate,
   wherein the tunnel layer, the emitter region, and the dopant layer are positioned on a back surface of the semiconductor substrate.

7. A method for manufacturing a solar cell, the method comprising:

   a layer forming operation of sequentially forming a tunnel layer, an intrinsic amorphous silicon layer, and a dopant layer on a back surface of a semiconductor substrate formed of a crystalline silicon material containing impurities of a first conductive type, the dopant layer being formed of a dielectric material containing impurities of a second conductive type opposite the first conductive type;
   a thermal processing operation of, after the layer forming operation, forming a front surface field region on a front surface of the semiconductor substrate through one successive thermal process, in which a temperature in a furnace is maintained or raised, recrystallizing the intrinsic amorphous silicon layer into an intrinsic polycrystalline silicon layer, and diffusing and activating the impurities of the second conductive type of the dopant layer into the recrystallized intrinsic polycrystalline silicon layer to form an emitter region; and
   an electrode forming operation of, after the thermal processing operation, forming a first electrode connected to the front surface of the semiconductor substrate and forming a second electrode connected to the emitter region.

8. The method of claim 7, wherein the layer forming operation further includes a process for forming a capping layer formed of a dielectric material not containing impurities of the second conductive type on a back surface of the dopant layer.

9. The method of claim 8, further comprising, between the thermal processing operation and the electrode

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forming operation:

an operation of removing a capping layer formed on the back surface of the semiconductor substrate and an oxide layer formed on a front surface of the front surface field region in the thermal processing operation; and
an operation of forming a hydrogen injection layer formed of a dielectric layer containing hydrogen on the back surface of the dopant layer, on which the capping layer is removed.

10. The method of any one of claims 7 to 9, wherein the forming of the emitter region includes:

a dehydrogenation process for removing hydrogen contained in the intrinsic amorphous silicon layer;
a recrystallization process for recrystallizing the intrinsic amorphous silicon layer into the intrinsic polycrystalline silicon layer; and
an emitter region activating process for diffusing and activating the impurities of the second conductive type contained in the dopant layer into the recrystallized intrinsic polycrystalline silicon layer, and wherein the forming of the front surface field region includes a front surface field region activating process for diffusing and activating impurities of the first conductive type into the front surface of the semiconductor substrate, and
wherein the front surface field region activating process is performed along with the emitter region activating process, and
wherein the thermal processing operation includes:

a first thermal process for maintaining the temperature of the furnace at a first temperature;
a second thermal process for changing the temperature of the furnace from the first temperature to a second temperature higher than the first temperature;
a third thermal process for maintaining the temperature of the furnace at the second temperature;
a fourth thermal process for changing the temperature of the furnace from the second temperature to a third temperature higher than the second temperature; and
a fifth thermal process for maintaining the temperature of the furnace at the third temperature.

11. The method of claim 10, wherein the first to fifth thermal processes are successively performed in the same furnace,

wherein a second thermal process time of the second thermal process is longer than a first thermal process time of the first thermal process and a third thermal process time of the third thermal process, and
wherein the third thermal process time is equal to or longer than the first thermal process time.

12. The method of claim 10 or 11, wherein the first thermal process maintains the temperature of the furnace at the first temperature of 350 °C to 450 °C for 5 minutes to 15 minutes,
wherein the third thermal process maintains the temperature of the furnace at the second temperature of 500 °C to 600 °C for 10 minutes to 20 minutes,
wherein the second thermal process increases the temperature of the furnace from the first temperature to the second temperature for 15 minutes to 25 minutes,
wherein the fifth thermal process maintains the temperature of the furnace at the third temperature of 800 °C to 1000 °C for 15 minutes to 30 minutes, and
wherein the fourth thermal process increases the temperature of the furnace from the second temperature to the third temperature for 5 minutes to 15 minutes.

13. The method of any one of claims 10 to 12, wherein the dehydrogenation process is performed through the first to third thermal processes.

14. The method of any one of claims 10 to 13, wherein the recrystallization process is performed through the fourth thermal process.

15. The method of any one of claims 10 to 14, wherein the emitter region activating process and the front surface field region activating process are performed through the fifth thermal process.

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FIG. 1

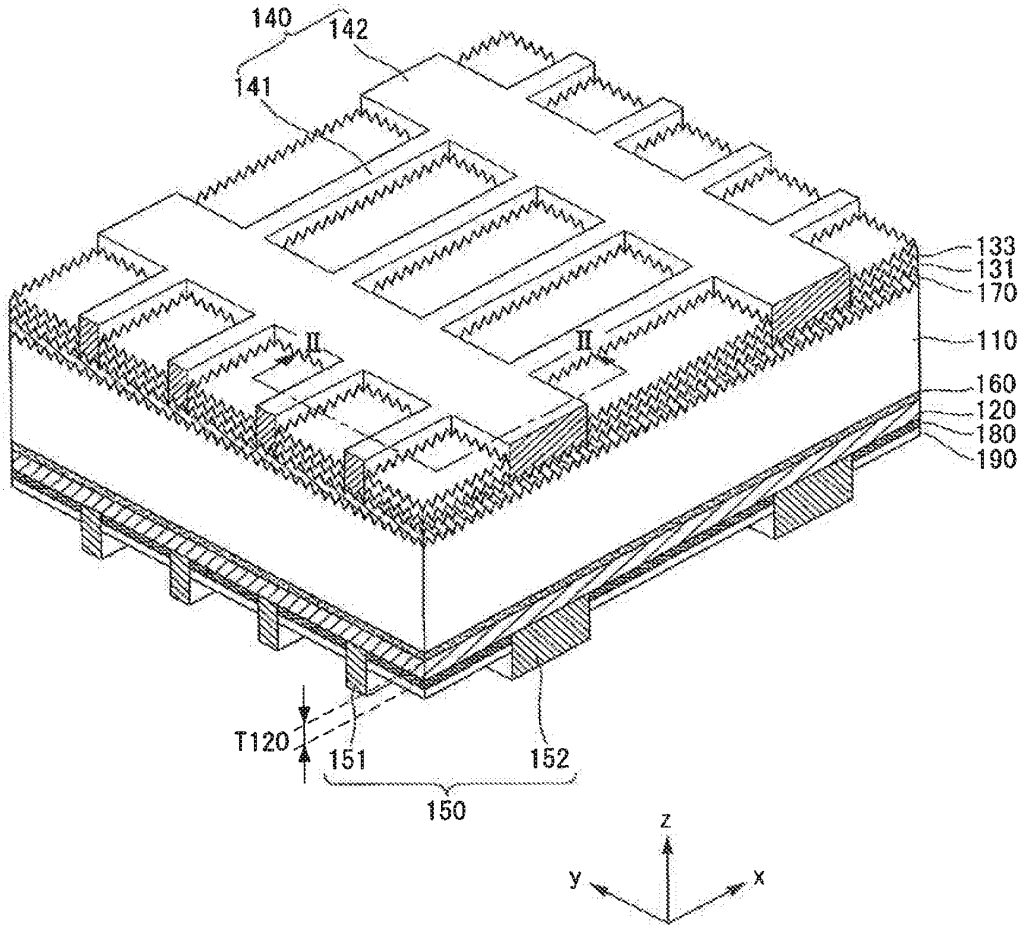

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FIG. 2

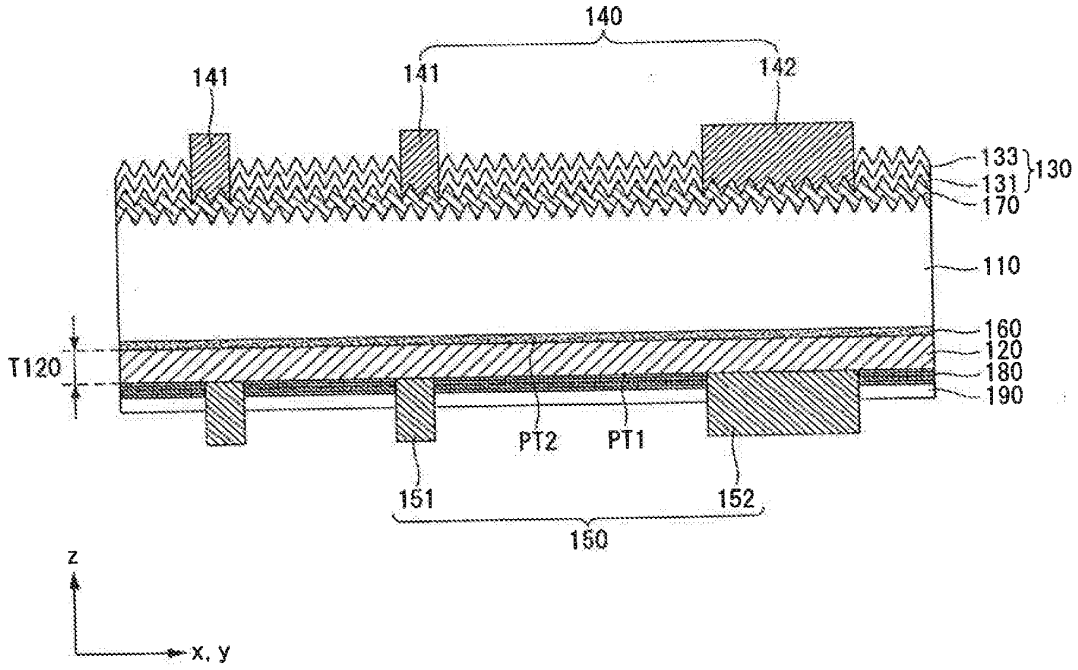

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FIG. 3

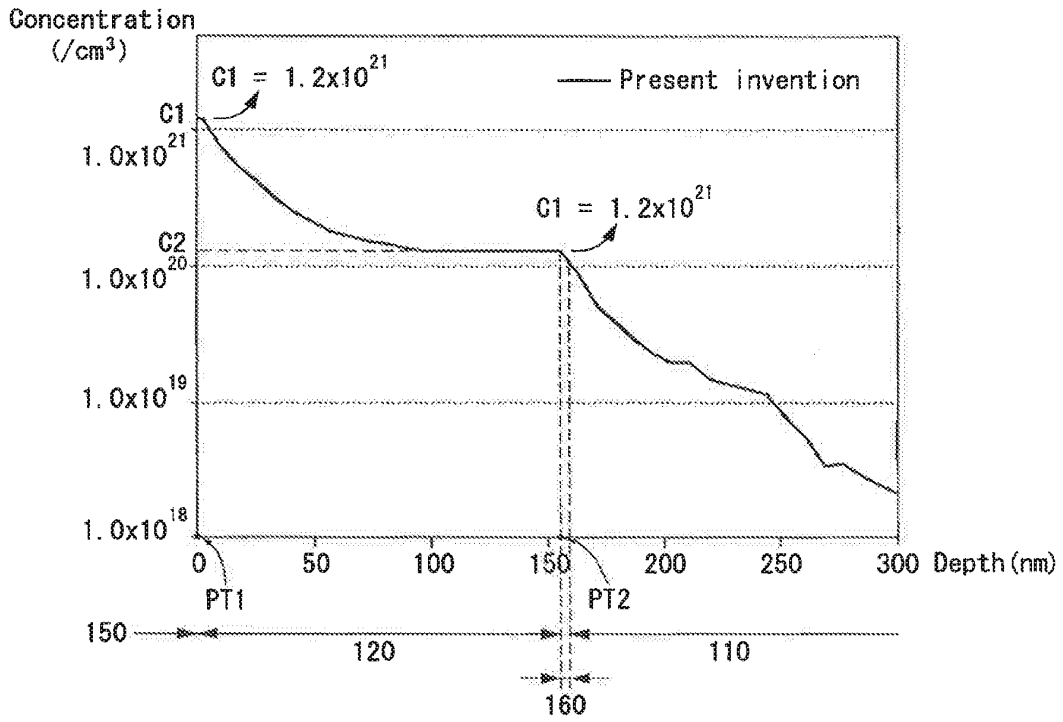

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FIG. 4

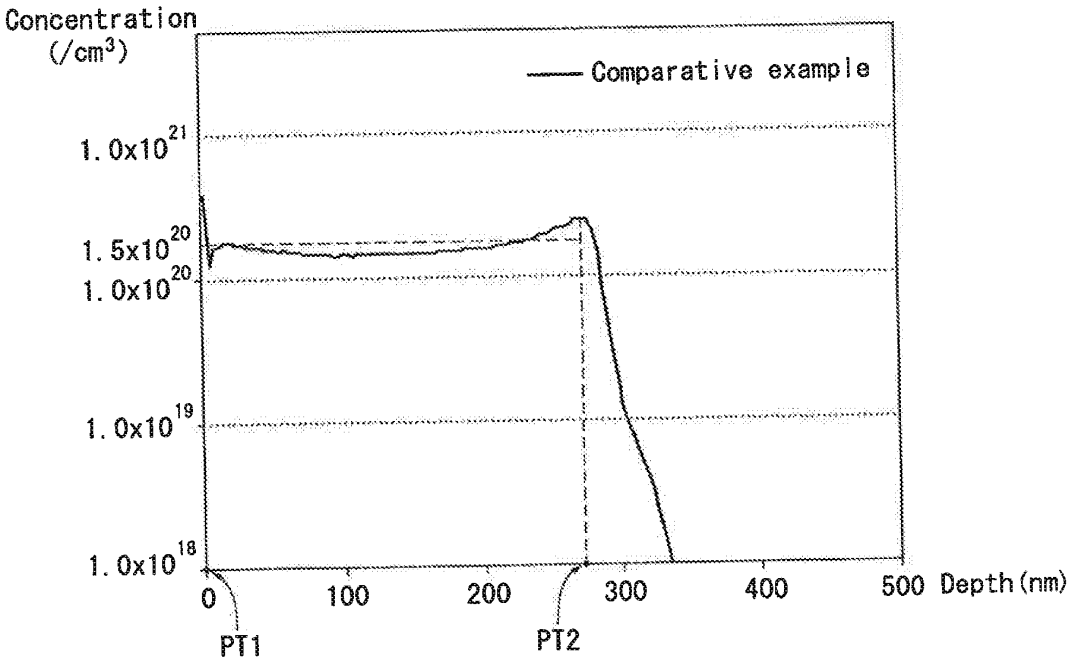

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FIG. 5

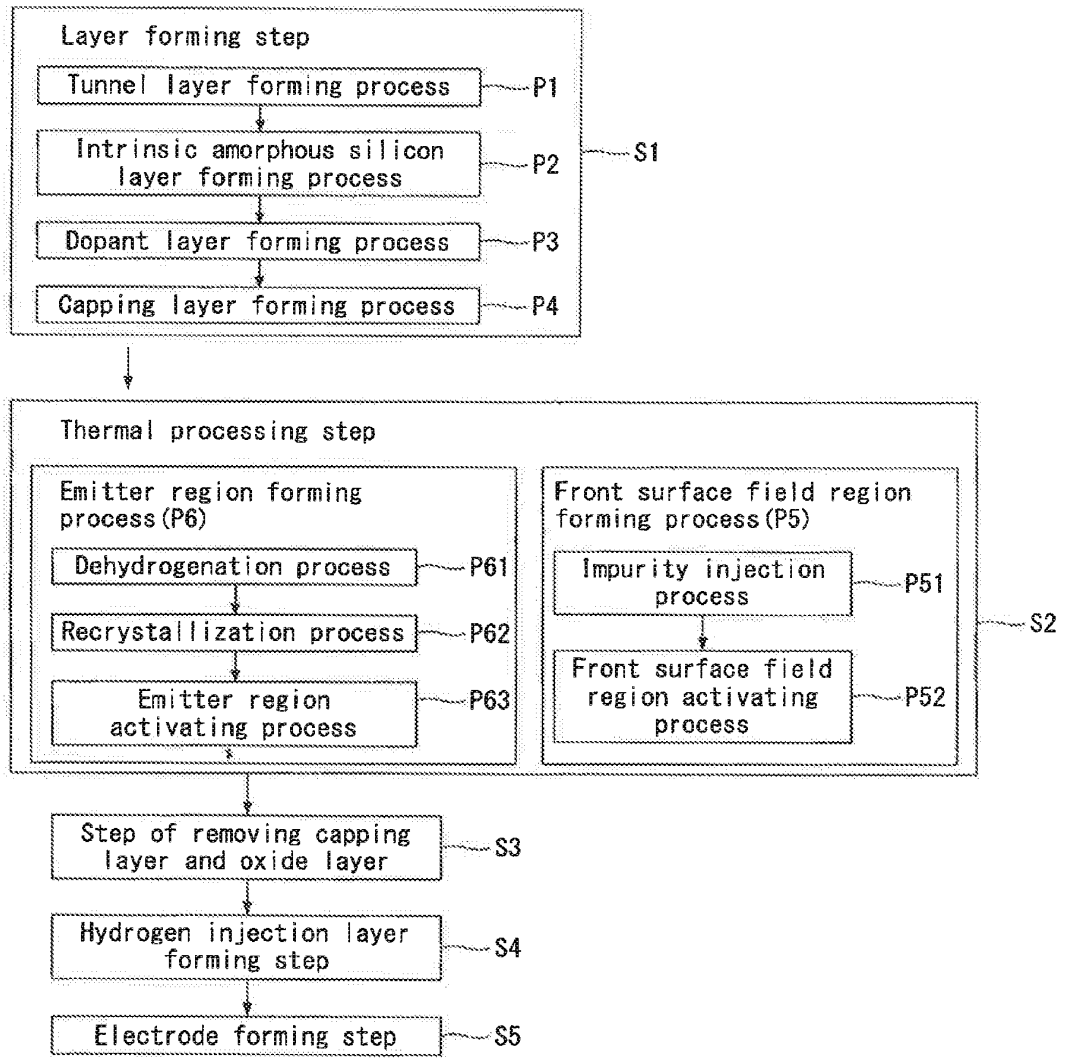

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FIG. 6A

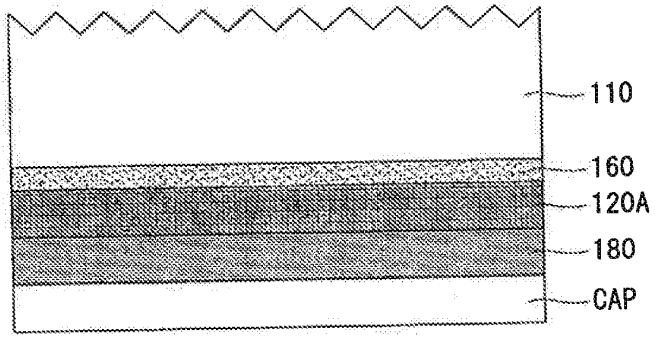

FIG. 6B

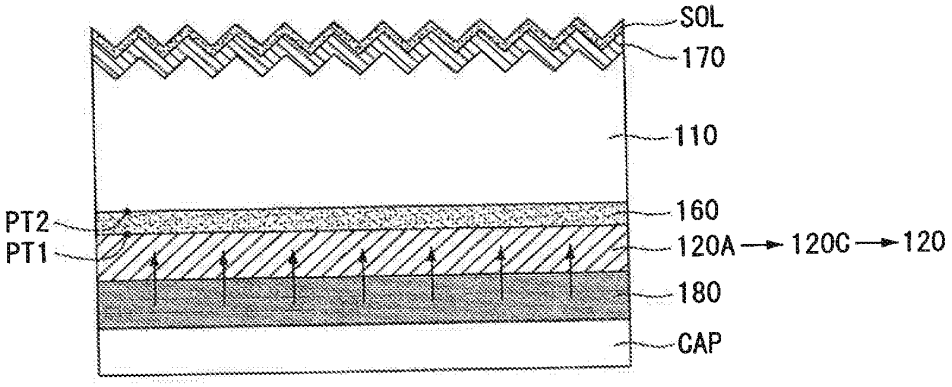

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FIG. 6C

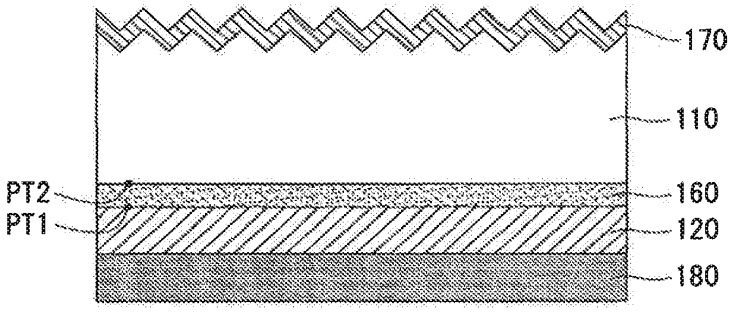

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FIG. 6D

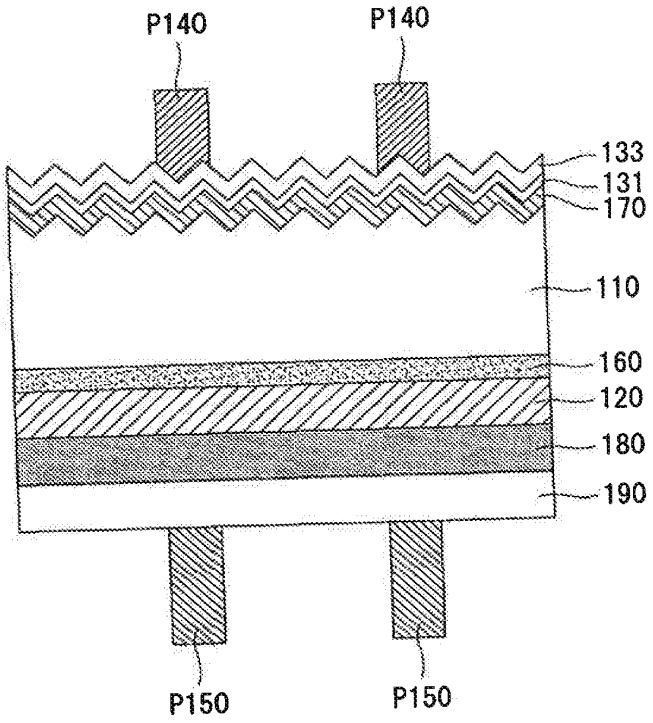

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FIG. 6E

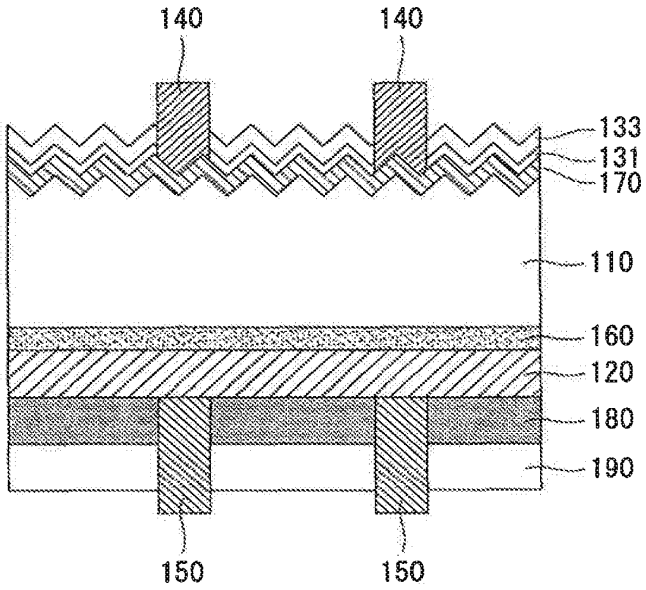

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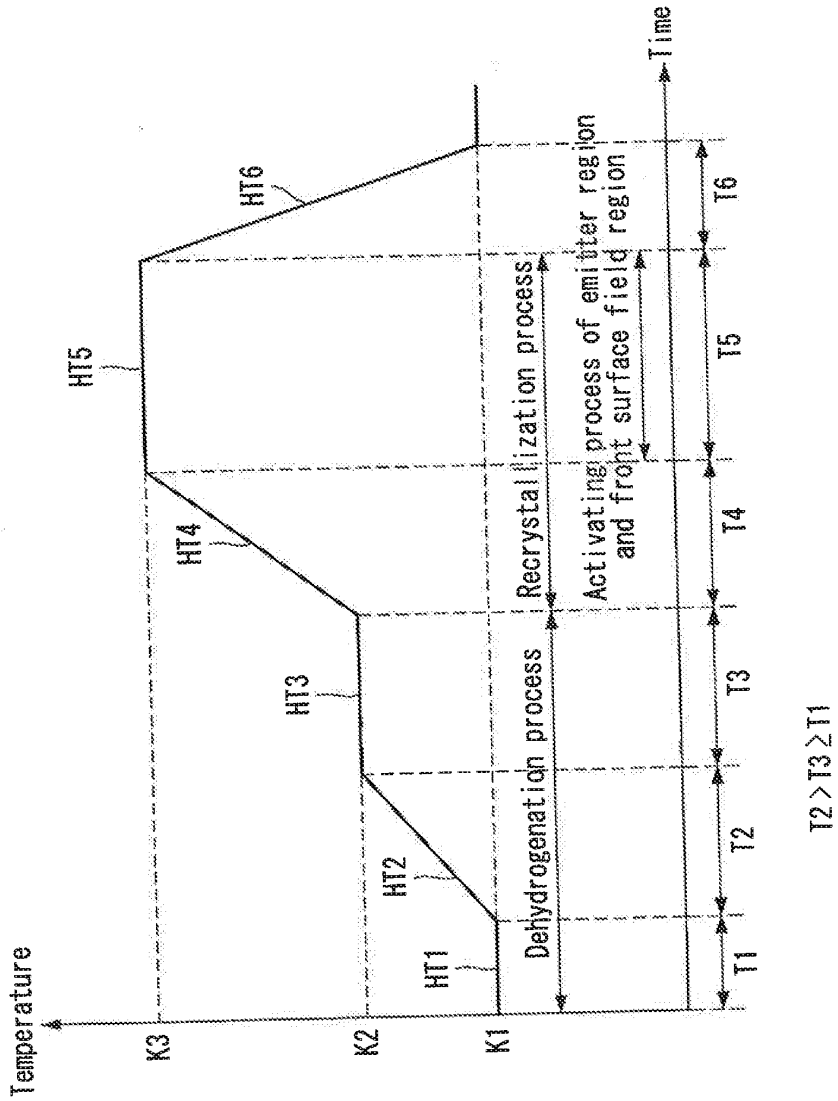
FIG. 7



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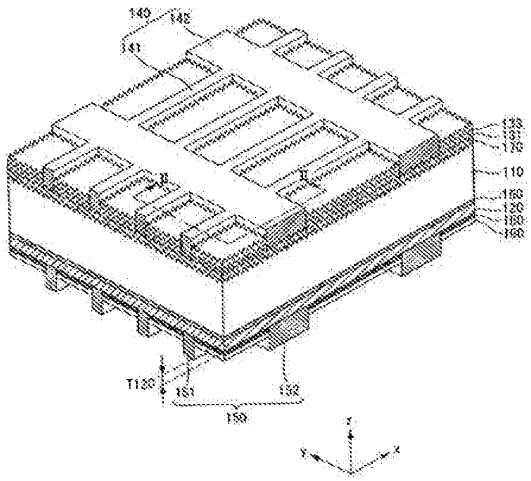
(54) SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME

(57) A solar cell and a method for manufacturing the same are disclosed. The solar cell includes a semiconductor substrate containing impurities of a first conductive type, a tunnel layer positioned on the semiconductor substrate, an emitter region positioned on the tunnel layer and containing impurities of a second conductive type opposite the first conductive type, a dopant layer positioned on the emitter region and formed of a dielectric material containing impurities of the second conductive type, a first electrode connected to the semiconductor substrate, and a second electrode configured to pass through the dopant layer and connected to the emitter region.

FIG. 1



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EUROPEAN SEARCH REPORT

Application Number
EP 15 00 3144

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Berlin	8 April 2016	Rodríguez-Gironés, M

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EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

BNSDOCID: <EP_____3018719A3_I_>

Petitioner Canadian Solar (USA) Inc., Ex. 1006, p. 239

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 15 00 3144

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

08-04-2016

Patent document cited in search report		Publication date	Patent family member(s)			Publication date
			PH	12014502088	A1	24-11-2014
			SG	11201405888P	A	30-10-2014
			TW	201340351	A	01-10-2013
			US	2013247965	A1	26-09-2013
			US	2015243803	A1	27-08-2015
			US	2016071996	A1	10-03-2016
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EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

BNSDOCID: <EP_____3018719A3_I_>

Petitioner Canadian Solar (USA) Inc., Ex. 1006, p. 240

Electronic Acknowledgement Receipt

EFS ID:	30436255
Application Number:	15643180
International Application Number:	
Confirmation Number:	7835
Title of Invention:	SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jungmin HA
Customer Number:	2292
Filer:	Esther Hyeri Chong/Alan Bishop/cmd
Filer Authorized By:	Esther Hyeri Chong
Attorney Docket Number:	1630-1332PUS2
Receipt Date:	21-SEP-2017
Filing Date:	06-JUL-2017
Time Stamp:	15:38:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2017-09-21-SignedIDSTrans-1630-1332PUS2.pdf	327674 e7f8a1c41542c11eb10e0bb75adaa276ffce3cc5	yes	6

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	5
	Information Disclosure Statement (IDS) Form (SB08)	6	6

Warnings:					
Information:					
2	Non Patent Literature	2017-09-11-EPOA15003390dated2017-07-07-1630-1332PUS2.pdf	181955 a246e81ccb3d220d2453c8ff769f2e3cf02a414b	no	4
Warnings:					
Information:					
3	Foreign Reference	IDS-EP3018719-1630-1332PUS2.pdf	2011212 056d66ee094b5f5755bc36d482f8da1b6ed6c70b	no	28
Warnings:					
Information:					
		Total Files Size (in bytes):	2520841		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: 1630-1332PUS2
(Patent)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application of:	Jungmin HA et al.		
Application No.:	15/643,180	Confirmation No.:	7835
Filed:	July 06, 2017	Art Unit:	1758
For:	SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME	Examiner:	CHERN, CHRISTINA

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

Applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on the attached PTO/SB/08.

II. COPIES

☑ a. Copies of foreign patent documents, non-patent literature and other information are provided.

☐ b. REFERENCES PREVIOUSLY CITED OR SUBMITTED: Copies of any information not provided can be found in one or more of the following applications which has been relied upon for an earlier filing date under 35 U.S.C. § 120:

U.S. Application No. and U.S. Filing Date

III. CONCISE EXPLANATION OF THE RELEVANCE/OTHER INFORMATION

☐ a. NON-ENGLISH LANGUAGE DOCUMENTS: A concise explanation of the relevance of all non-English language patents, publications, or other information listed on the attached PTO/SB/08 form(s) is indicated thereon by a check mark at column T to designate the submission of one or more of the following: an English language abstract (as a partial translation); a machine-generated translation; a full or partial translation; and/or a statement of relevance.

☑ b. ENGLISH LANGUAGE SEARCH REPORT OR FOREIGN PATENT OFFICE COMMUNICATION: An English language version of the search report or Foreign Patent Office communication that indicates the degree of relevance is attached.

☑ c. OTHER: The following additional information is provided.

A copy of the European Office Action, dated July 7, 2017, for European Application No. 15003390.0 is provided.

IV. STATEMENT UNDER 37 C.F.R. § 1.97(e)

The undersigned hereby states that:

☑ a. Each item of information contained in the IDS was first cited in any communication from a foreign patent office in a counterpart foreign application not more than **three months** prior to the filing of the IDS. *See 37 C.F.R § 1.97(e)(1).* This statement does not relate to English language counterparts not listed in a communication from the foreign patent office. Such English language counterparts are provided to aid the Examiner's consideration of non-English items first cited in the communication from the foreign patent office; or

☐ b. No item of information contained in the IDS was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of IDS was known to any individual designated in 37 C.F.R. § 1.56(c) more than **three months** prior to the filing of the IDS. *See 37 C.F.R. § 1.97(e)(2)*; or

☐ c. Some of the items of information in the IDS were cited in a communication from a foreign patent office. Such items were first cited in a communication from a foreign patent office in a counterpart foreign application not more than **three months** prior to the filing of this IDS. *See 37 C.F.R. § 1.97(e)(1).* This statement does not relate to English language counterparts not listed in a communication from the foreign patent office. Such English language counterparts are provided to aid the Examiner's consideration of non-English items first cited in the communication from the foreign patent office. As to the remaining items of information, to the knowledge of the person signing the certification after making reasonable inquiry, such remaining items were not known to any individual designated in 37 C.F.R. § 1.56(c) more than **three months** prior to the filing of this statement. *See 37 C.F.R. § 1.97(e)(2).*

V. STATEMENT UNDER 37 C.F.R. § 1.704(d)(1)

Patent Term Adjustment Reduction Should Not Apply

☐ The undersigned hereby states:

This Information Disclosure Statement is in compliance with 37 C.F.R. §§ 1.97 and 1.98 and will not be considered a failure to engage in reasonable efforts to conclude prosecution (processing or examination) of the present application under 37 C.F.R. § 1.704(c)(6), (c)(8), (c)(9), or (c)(10), because each item of information contained in the Information Disclosure Statement:

☐ (i) Was first cited in any communication from a patent office in a counterpart foreign or international application or from the Office, and this communication was not received by any individual designated in § 1.56(c) more than **thirty days** prior to the filing of the information disclosure statement *(see 37 C.F.R. § 1.704(d)(1)(i))*; or

☐ (ii) Is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in § 1.56(c) more than **thirty days** prior to the filing of the information disclosure statement *(see 37 C.F.R. § 1.704(d)(1)(ii))*.

VI. FEES

☐ a. This Information Disclosure Statement is being filed concurrently with the filing of a new patent application or Request for Continued Examination. No fee is required.

☑ b. This Information Disclosure Statement is being filed within three months of the filing date of an application. *See 37 C.F.R. § 1.97(b)(1) and 37 C.F.R. § 1.97(b)(2).* No fee is required.

☐ c. This Information Disclosure Statement is being filed before the mailing date of a first Action on the merits. *See 37 C.F.R. § 1.97(b)(3).* No fee is required. If a first Office Action on the merits has issued, please consider this IDS under 37 C.F.R. § 1.97(c) and see the statement under 37 C.F.R. § 1.97(e) above. If no statement has been made, charge our deposit account for the required fee.

☐ d. This Information Disclosure Statement is being filed before the mailing date of a Final Office Action or before the mailing date of a Notice of Allowance or before an action that otherwise closes prosecution in the application. *See 37 C.F.R. § 1.97(c)(1).*

☐ No statement. The fee as required by 37 C.F.R. § 1.17(p) is provided.

or

☐ See the above statement. No fee is required.

☐ e. This Information Disclosure Statement is being filed on or after the mailing date of a Final Office Action, on or after the mailing date of a Notice of Allowance, or on or after an action that otherwise closes prosecution in the application (*see 37 C.F.R. § 1.97(d)*), see the statement above. The fee as required by 37 C.F.R. § 1.17(p) is provided.

VII. PAYMENT OF FEES

☐ The required fee is listed on the attached Fee Transmittal.

☑ No fee is required.

If the Examiner has any questions concerning this IDS, please contact the undersigned. If it is determined that this IDS has been filed under the wrong rule, the USPTO is requested to consider this IDS under the proper rule and charge the appropriate fee to Deposit Account No. 02-2448.

Dated: SEP 21 2017

Respectfully submitted,

By _____

Esther H. Chong
Registration No.: 40953
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road, Suite 100 East
Falls Church, VA 22042
703-205-8000

Attachment(s):
☑ PTO/SB/08
☑ Document(s)
☑ Foreign Patent Office Communication(s)
☐ Foreign Search Report(s)
☐ Fee
☐ Other:

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/643,180	07/06/2017	Jungmin HA	1630-1332PUS2

CONFIRMATION NO. 7835

PUBLICATION NOTICE

OC000000095038528

2292
BIRCH STEWART KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
FALLS CHURCH, VA 22042-1248

Title:SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME

Publication No.US-2017-0309761-A1
Publication Date:10/26/2017

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

2292 7590 03/02/2018
BIRCH STEWART KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
FALLS CHURCH, VA 22042-1248

EXAMINER
CHERN, CHRISTINA

ART UNIT	PAPER NUMBER
1758	

DATE MAILED: 03/02/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/643,180	07/06/2017	Jungmin HA	1630-1332PUS2	7835

TITLE OF INVENTION: SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	06/04/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

2292 7590 03/02/2018
BIRCH STEWART KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
FALLS CHURCH, VA 22042-1248

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/643,180	07/06/2017	Jungmin HA	1630-1332PUS2	7835

TITLE OF INVENTION: SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	06/04/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHERN, CHRISTINA	1758	136-255000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Petitioner Canadian Solar (USA) Inc., Ex. 1006, p. 250

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/643,180	07/06/2017	Jungmin HA	1630-1332PUS2	7835

2292 7590 03/02/2018
BIRCH STEWART KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
FALLS CHURCH, VA 22042-1248

EXAMINER
CHERN, CHRISTINA

ART UNIT	PAPER NUMBER
1758	

DATE MAILED: 03/02/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/643,180	Applicant(s) HA ET AL.	
	Examiner CHRISTINA CHERN	Art Unit 1758	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-11,14 and 17-20*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☒ All b) ☐ Some *c) ☐ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/CHRISTINA CHERN/
Primary Examiner, Art Unit 1758

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in an interview with Bradford Fritz (# 63,406) on 2/20/2018.

The application has been amended as follows:

Please see attached claim listing amendments.

2. Claims 1-11, 14, and 17-20 are allowed.

3. The following is an examiner's statement of reasons for allowance:

The closest prior arts are considered to be represented by Heng et al. (US 2012/0318340) and Chang et al. (US 2014/0299187).

While Heng and Chang teach some of the claimed features of the method as recited in the claims, the references, alone or in combination, do not teach or render obvious the claimed features of the removing step as recited and the first passivation film covering the first surface of the semiconductor substrate along with the isolation portion.

Therefore, the claims were found to be allowable over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTINA CHERN whose telephone number is (408)918-7559. The examiner can normally be reached on Mon.-Fri., 9:00 AM-5:30 PM PST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jennifer Michener can be reached on (571) 272-1424. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/CHRISTINA CHERN/
Primary Examiner, Art Unit 1758

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BIB DATA SHEET

CONFIRMATION NO. 7835

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/643,180	07/06/2017 **RULE**	136	1758	1630-1332PUS2

APPLICANTS
LG ELECTRONICS INC., Seoul, KOREA, REPUBLIC OF;

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Jaesung KIM, Seoul, KOREA, REPUBLIC OF;

**** CONTINUING DATA ****************************
This application is a CON of 14/953,264 11/27/2015 PAT 9722104

**** FOREIGN APPLICATIONS ****************************
REPUBLIC OF KOREA 10-2014-0168624 11/28/2014
REPUBLIC OF KOREA 10-2015-0122846 08/31/2015

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
07/13/2017

Foreign Priority claimed	☑ Yes ☐ No		STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	☑ Yes ☐ No	☐ Met after Allowance	KOREA, REPUBLIC OF	18	20	1
Verified and Acknowledged	/CHRISTINA CHERN/ Examiner's Signature	Initials				

ADDRESS
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UNITED STATES

TITLE
SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME

FILING FEE RECEIVED		
1600	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1998944	(solar PV optoelectr$4 photovoltaic photocell photoelectric photodiode) (solar PV optoelectr$4 photovoltaic photocell photoelectric photodiode) with (device cell panel array module)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 10:41
S2	2	"20120318340"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 10:42
S3	6	"2014204128"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 11:02
S4	3	"20140204128"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 11:02
S5	1	"2011512689"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 11:03
S7	16	"2787541"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 11:16
S8	2	"20140299187"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 11:28
S9	14948	H01L31/00,02,0216,02167,0248,0352.cpc.	US-PGPUB;	OR	ON	2017/03/14

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:42
S10	163	(S1 S9) and tunnel and (front light) with (passivati$2) and (rear back) with (passivati$2) and (emitter second adj conducti$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 11:43
S11	1998944	(solar PV optoelectr$4 photovoltaic photocell photoelectric photodiode) (solar PV optoelectr$4 photovoltaic photocell photoelectric photodiode) with (device cell panel array module)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 14:26
S12	14948	H01L31/00,02,0216,02167,0248,0352.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 14:26
S13	163	(S11 S12) and tunnel and (front light) with (passivati$2) and (rear back) with (passivati$2) and (emitter second adj conducti$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 14:26
S14	721	(S11 S12) and oxide with layer same (rear back) and (front light) with (passivati$2) and (rear back) with (passivati$2) and (emitter second adj conducti$2) not S13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 14:26
S15	1998944	(solar PV optoelectr$4 photovoltaic photocell photoelectric photodiode) (solar PV optoelectr$4 photovoltaic photocell photoelectric photodiode) with (device cell panel array module)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 17:39
S16	14948	H01L31/00,02,0216,02167,0248,0352.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 17:39
S17	163	(S15 S16) and tunnel and (front light) with (passivati$2) and (rear back) with (passivati$2) and (emitter second adj conducti$2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2017/03/14 17:39

			IBM_TDB			
S18	499	(S15 S16) and (silicon adj dioxide "SiO.sub.2" "sio.sub.x" "SiN.sub.x" "SiN.sub.2" "Al.sub.2O.sub.3") same (rear back) and (front light) with (passivati$2) and (rear back) with (passivati$2) and (emitter second adj conducti$2) not S17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 17:39
S19	337	(S15 S16) and (silicon adj dioxide "SiO.sub.2" "sio.sub.x" "SiN.sub.x" "SiN.sub.2" "Al.sub.2O.sub.3") with (rear back) and (front light) with (passivati$2) and (rear back) with (passivati$2) and (emitter second adj conducti$2) not S17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 17:40
S20	86	(S15 S16) and (silicon adj dioxide "SiO.sub.2" "sio.sub.x" "SiN.sub.x" "SiN.sub.2" "Al.sub.2O.sub.3") with (rear back) and (front light) with (passivati$2) and (rear back) with (passivati$2) and edge with isolati$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/14 17:52
S21	4	"20110100459"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/20 10:29
S22	2000303	(solar PV optoelectr$4 photovoltaic photocell photoelectric photodiode) (solar PV optoelectr$4 photovoltaic photocell photoelectric photodiode) with (device cell panel array module)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/20 11:48
S23	14961	H01L31/00,02,0216,02167,0248,0352.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/20 11:48
S24	2000303	(solar PV optoelectr$4 photovoltaic photocell photoelectric photodiode) (solar PV optoelectr$4 photovoltaic photocell photoelectric photodiode) with (device cell panel array module)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/20 11:48
S25	14961	H01L31/00,02,0216,02167,0248,0352.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/20 11:48
S26	163	(S24 S25) and tunnel and (front light) with (passivati$2) and (rear back) with (passivati$2) and (emitter second adj conducti$2)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2017/03/20 11:48

			EPO; JPO; DERWENT; IBM_TDB			
S27	247	(S22 S23) and tunnel$3 and (front light first) with (passivati$2) and (rear back second) with (passivati$2) and (emitter second adj conducti$2) not S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/20 11:48
S28	94	(S22 S23) and tunnel$3 and (front light first) with (passivati$2) and (rear back second) with (passivati$2) same (side edge) and (emitter second adj conducti$2) not S26	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/03/20 11:50
S33	2224046	(solar PV optoelectr$4 photovoltaic photocell photoelectric photodiode) (solar PV optoelectr$4 photovoltaic photocell photoelectric photodiode) with (device cell panel array module)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/12 15:57
S34	16533	H01L31/00,02,0216,02167,0248,0352.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/12 15:57
S35	85	(S33 S34) and tunnel$3 same intrinsic same (BSF FSF surface adj field conducti$2 adj layer)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/02/12 15:57

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L15	4386	H01L31/00,02,0216,02167,0248,0352.cpc.	US-PGPUB; USPAT	OR	ON	2018/02/14 16:59
L16	690530	(solar PV optoelectr$4 photovoltaic photocell photoelectric photodiode) (solar PV optoelectr$4 photovoltaic photocell photoelectric photodiode) with (device cell panel array module)	US-PGPUB; USPAT	OR	ON	2018/02/14 16:59
L17	5	(l15 l16) and (remov$3 etch$3) with tunnel$3 same (front light adj receiving).clm.	US-PGPUB; USPAT	OR	ON	2018/02/14 17:00
L18	36	(l15 l16) and (remov$3 etch$3) with tunnel$3 same (surface).clm.	US-PGPUB; USPAT	OR	ON	2018/02/14 17:11
S29	639294	(solar PV optoelectr$4 photovoltaic photocell photoelectric photodiode) (solar PV optoelectr$4 photovoltaic photocell	US-PGPUB; USPAT	OR	ON	2017/03/20 11:43

		photoelectric photodiode) with (device cell panel array module)				
S30	4072	H01L31/00,02,0216,02167,0248,0352.cpc.	US-PGPUB; USPAT	OR	ON	2017/03/20 11:43
S31	0	(S29 S30) and tunnel$3 same passivati$2 same (second with conducti$2 emitter) same isolati$2 with (part portion).clm.	US-PGPUB; USPAT	OR	ON	2017/03/20 11:46
S32	0	(S29 S30) and (silicon with oxide silicon with dioxide silicon with nitride aluminum with oxide) same passivati$2 same (second with conducti$2 emitter) same isolati$2 with (part portion).clm.	US-PGPUB; USPAT	OR	ON	2017/03/20 11:47

2/14/2018 5:12:56 PM
C:\Users\cchern\Documents\EAST\Workspaces\15643180.wsp

PTO/SB/08a (07-09)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	1

Complete if Known	
Application Number	15/643,180
Filing Date	July 06, 2017
First Named Inventor	Jungmin Ha
Art Unit	1758
Examiner Name	CHERN. CHRISTINA
Attorney Docket Number	1630-1332PUS2

U.S. PATENT DOCUMENTS

Examiner Initial *	Cite No.	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initial *	Cite No. 1	Foreign Patent Document Country[3] Code Number[4] Kind Code (if known)[5]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
	1	EP 3018719 - A2	05-11-2016			☐
						☐
						☐
						☐
						☐
						☐

Examiner Signature	/CHRISTINA CHERN/	Date Considered	02/14/2018

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not Considered. Include copy of this form with next communication to applicant. 1. Applicant's unique citation design number (optional). 2 See Kinds Codes of USPTO patent Documents. at www.uspto.gov or MPEP 901.04. 3. Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4. For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5. Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. 6. Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450 Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assisstance in completing the form, call 1-800-PTO-9199 (1-800-786.9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /C.C/

EXAMINER'S AMENDMENT

1. (Currently Amended) A method for manufacturing a solar cell, comprising:

a tunnel layer forming step of forming a tunnel layer on a first surface of a semiconductor substrate, a second surface of the semiconductor substrate and a side of the semiconductor substrate;

a first conductive type semiconductor region forming step of forming a first conductive type semiconductor region on the first surface of the semiconductor substrate and the second surface of the semiconductor substrate;

a second conductive type semiconductor region forming step of forming a second conductive type semiconductor region by doping impurities of ~~a~~ the second conductive type into the second~~a second~~ surface of the semiconductor substrate;

a removing step of removing the tunnel layer and the first conductive type semiconductor region placed at least on the second surface of the semiconductor substrate prior to the second conductive type semiconductor region forming step after the first conductive type semiconductor region forming step;

a first passivation film forming step of forming a first passivation film on the first conductive type semiconductor region; and

an electrode forming step of forming a first electrode connected to the first conductive type semiconductor region and a second electrode connected to the second conductive type semiconductor region,

wherein the removing step further comprises forming an isolation portion by removing the tunnel layer on the side of the semiconductor substrate and an edge portion of the first conductive type semiconductor region, and

wherein the first passivation film covers the first surface of the semiconductor substrate along with the isolation portion.

2. (Original) The method of claim 1, further comprising a step of forming an opening portion in the first passivation film after the first passivation film forming step.

3. (Original) The method of claim 2, wherein the step of forming the opening portion in the first passivation film is performed by thermal treatment in the electrode forming step.

4. (Currently Amended) The method of claim 3, wherein the electrode forming step comprises a first electrode forming step of forming the first electrode, and

wherein the first electrode forming step comprises printing a paste ~~for first finger electrodes~~ for forming ~~the~~ first finger electrodes and a paste ~~for a first bus bar~~ for forming ~~the~~ a first bus bar on the first passivation film and performing thermal treatment on the pastes.

5. (Currently Amended) The method of claim 4, wherein in the first electrode forming step, a highest temperature for the thermal treatment is between 795° C to 870° C~~795 to 870~~.

6. (Original) The method of claim 4, wherein in the first electrode forming step, the paste for the first finger electrodes and the paste for the first bus bar are printed through a single process.

7. (Currently Amended) The method of claim 6, wherein a material ~~included~~ in the paste for the first finger electrodes is identical ~~with~~ to a material ~~included~~ in the paste for the first bus bar.

8. (Original) The method of claim 4, wherein in the first electrode forming step, the paste for the first finger electrodes and the paste for the first bus bar are printed using separate printing processes.

9. (Currently Amended) The method of claim 8, wherein a material ~~included~~ in the paste for the first finger electrodes and a material ~~included~~ in the paste for the first bus bar are different.

10. (Currently Amended) The method of claim 1, further comprising an intrinsic semiconductor layer forming step of forming an intrinsic semiconductor layer on the tunnel layer formed on the first surface of the semiconductor substrate between the tunnel layer forming step and the first conductive type semiconductor region forming step, and,

in the first conductive type semiconductor region forming step, impurities of ~~a~~ the first conductive type is doped into the intrinsic semiconductor layer formed on the first surface of the semiconductor substrate.

11. (Currently Amended) The method of claim 1, wherein the first surface of ~~a~~ the semiconductor substrate is ~~a~~ the back surface of ~~a~~ the semiconductor substrate.

12. (Canceled)

13. (Canceled)

14. (Original) The method of claim 1, the first conductive type semiconductor region is formed by a thermal expansion of impurities of a first conductive type.

15. (Canceled)

16. (Canceled)

17. (Currently Amended) The method of claim 1~~claim 15~~, wherein the removing step further comprises:

forming a mask layer having a smaller area than the semiconductor substrate on the first conductive type semiconductor region on the first surface~~a second side~~ of the semiconductor substrate;

etching the first conductive type semiconductor region and the tunnel layer ~~placed~~ in a portion in which the mask layer is not ~~has not been~~ formed; and

removing the mask layer.

18. (Currently Amended) The method of claim 1, further comprising forming an additional~~a second~~ passivation film covering the second conductive type semiconductor region between the step of forming the second conductive type semiconductor region and the step of forming the first passivation film.

19. (Currently Amended) The method of claim 18, wherein the

additional~~second~~ passivation film is ~~placed~~ formed on ~~a~~ the side of the semiconductor substrate, and the first passivation film is ~~placed~~ formed on the additional~~second~~ passivation film.

20. (Currently Amended) The method of claim 1, wherein the first electrode is a front electrode positioned on the second~~a front~~ surface of the semiconductor substrate, and the second electrode is a back electrode positioned on the first~~a back~~ surface of the semiconductor substrate.

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15643180	HA ET AL.
	Examiner	**Art Unit**
	CHRISTINA CHERN	1758

CPC						
Symbol					**Type**	**Version**
H01L		31	/	022433	F	2013-01-01
H01L		31	/	02168	I	2013-01-01
H01L		31	/	022425	I	2013-01-01
H01L		31	/	0747	I	2013-01-01
H01L		31	/	0201	I	2013-01-01
H01L		31	/	02167	I	2013-01-01
H01L		31	/	03685	I	2013-01-01
H01L		31	/	077	I	2013-01-01
H01L		31	/	1824	I	2013-01-01
H01L		31	/	1864	I	2013-01-01
H01L		31	/	1868	I	2013-01-01
Y02E		10	/	50	A	2013-01-01
			/			
			/			
			/			

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 16	
/CHRISTINA CHERN/ Primary Examiner.Art Unit 1758 (Primary Examiner)	02/14/2018 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 12

U.S. Patent and Trademark Office

Part of Paper No. 20180214

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15643180	HA ET AL.
	Examiner	**Art Unit**
	CHRISTINA CHERN	1758

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
		H	0	1	L	31 / 18 (2006.01.01)					
CROSS REFERENCE(S)		H	0	1	L	31 / 0216 (2014.01.01)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)										

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 16	
/CHRISTINA CHERN/ Primary Examiner.Art Unit 1758 (Primary Examiner)	02/14/2018 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 12

U.S. Patent and Trademark Office

Part of Paper No. 20180214

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15643180	HA ET AL.
	Examiner	**Art Unit**
	CHRISTINA CHERN	1758

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	13	17												
2	2	14	18												
3	3	15	19												
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11	11														
	12														
	13														
12	14														
	15														
	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 16	
/CHRISTINA CHERN/ Primary Examiner.Art Unit 1758 (Primary Examiner)	02/14/2018 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 12

U.S. Patent and Trademark Office

Part of Paper No. 20180214

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15643180	HA ET AL.
	Examiner	**Art Unit**
	CHRISTINA CHERN	1758

CPC- SEARCHED		
Symbol	**Date**	**Examiner**
H01L31/00,02,0216,02167,0248,0352	2/13/2018	CC

CPC COMBINATION SETS - SEARCHED		
Symbol	**Date**	**Examiner**

US CLASSIFICATION SEARCHED			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
Text limited search in the cited CPC subgroups. See search history.	2/13/2018	CC
Inventor name search in PALM	2/13/2018	CC
Reviewed parent application14/953,264	2/13/2018	CC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
H01L31	00,02,0216,02167,0248,0352	2/14/2018	CC

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 4

Complete if Known	
Application Number	NEW
Filing Date	
First Named Inventor	Jungmin Ha
Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	1630-1332PUS2

U.S. PATENT DOCUMENTS

Examiner initial *	Cite No.	Document Number Number - Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	US-2009/0205712 - A1	08-20-2009	COUSINS	
	2	US-2011/0100459 - A1	05-05-2011	YOON et al.	
	3	US-2011/0275175 - A1	11-10-2011	MINSEK et al.	
	4	US-2012/0298175 - A1	11-29-2012	VAN ROOSMALEN et al.	
	5	US-2012/0318340 - A1	12-20-2012	HENG et al.	
	6	US-2014/0073105 - A1	03-13-2014	ISOGAI	
	7	US-2014/0299187 - A1	10-09-2014	CHANG et al.	
	8	US-2015/0086729 - A1	03-26-2015	Gortzen et al.	
	9	US-2015/0129037 - A1	05-14-2015	NAM et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initial *	Cite No. 1	Foreign Patent Document Country[3] Code	Number[4] Kind Code (if known)[5]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
	10	KR	10-1442011 - B1	09-29-2014			
	11	KR	10-2011-0059366 - A	06-02-2011			
	12	KR	10-2012-0120260 - A	11-01-2012			
	13	KR	10-2015-0053551 - A	05-18-2015			
	14	CN	103703567 - A	04-02-2014			
	15	JP	2000-340812 - A	12-08-2000			

Examiner Signature	/CHRISTINA CHERN/	Date Considered	02/14/2018

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Sheet	2	of	4

Complete if Known	
Application Number	NEW
Filing Date	
First Named Inventor	Jungmin Ha
Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	1630-1332PUS2

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	16	WO	2009/094578 - A2	07-30-2009			
	17	JP	2009-295715 - A	12-17-2009			
	18	WO	2010/151478 - A1	12-29-2010			
	19	JP	2010-186862 - A	08-26-2010			
	20	JP	2011-181963 - A	09-15-2011			
	21	JP	2011-512689 - A	04-21-2011			

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Sheet	3	of	4

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Application Number	NEW
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First Named Inventor	Jungmin Ha
Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	1630-1332PUS2

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	22	WO	2013/094052 - A1	06-27-2013			☐
	23	JP	2014-203999 - A	10-27-2014			☐
	24	JP	2014-204128 - A	10-27-2014			☐
	25	JP	2014-523653 - A	09-11-2014			☐
	26	JP	2014-53452 - A	03-20-2014			☐
	27	CN	201812825 - U	04-27-2011			☐

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Application Number	NEW
Filing Date	
First Named Inventor	Jungmin Ha
Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	1630-1332PUS2

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FOREIGN PATENT DOCUMENTS

Examiner Initial *	Cite No. 1	Foreign Patent Document Country[3] Code	Number[4] Kind Code (if known)[5]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
	28	CN	203760493 - U	08-06-2014			
	29	EP	2787541 - A1	10-08-2014			
	30	EP	2797124 - A1	10-29-2014			

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Alexandria, Virginia 22313-1450
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CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

2292 7590 03/02/2018
BIRCH STEWART KOLASCH & BIRCH, LLP
8110 Gatehouse Road
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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/643,180	07/06/2017	Jungmin HA	1630-1332PUS2	7835

TITLE OF INVENTION: SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0	$0	$1000	06/04/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHERN, CHRISTINA	1758	136-255000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Birch, Stewart, Kolasch & Birch, LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: LG ELECTRONICS INC.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): Seoul, Republic of Korea

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
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- ☐ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
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Authorized Signature: Esther Chong — Date: JUN 03 2018
Typed or printed name: Esther H. Chong — Registration No. 40953

RCR

Electronic Patent Application Fee Transmittal

Application Number:	15643180
Filing Date:	06-Jul-2017
Title of Invention:	SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jungmin HA
Filer:	Esther Hyeri Chong/Mary Mejia
Attorney Docket Number:	1630-1332PUS2

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

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EFS ID:	32783384
Application Number:	15643180
International Application Number:	
Confirmation Number:	7835
Title of Invention:	SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME
First Named Inventor/Applicant Name:	Jungmin HA
Customer Number:	2292
Filer:	Esther Hyeri Chong/Mary Mejia
Filer Authorized By:	Esther Hyeri Chong
Attorney Docket Number:	1630-1332PUS2
Receipt Date:	01-JUN-2018
Filing Date:	06-JUL-2017
Time Stamp:	15:09:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	060418INTEFSW15094600
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2018-06-01-IssueFeeTransmittal-1630-1332PUS2.pdf	303181 9766e5c3217b5f15b5257da302bcb26eed1eeb57	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30178 7fa472d24bfbe7d03aeeb5546ed20f272a51a7c1	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	333359		

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
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<u>New International Application Filed with the USPTO as a Receiving Office</u>
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UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/643,180	07/03/2018	10014419	1630-1332PUS2	7835

2292 7590 06/13/2018
BIRCH STEWART KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
FALLS CHURCH, VA 22042-1248

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Jungmin HA, Seoul, KOREA, REPUBLIC OF;
LG ELECTRONICS INC., Seoul, KOREA, REPUBLIC OF;
Sungjin KIM, Seoul, KOREA, REPUBLIC OF;
Juhwa CHEONG, Seoul, KOREA, REPUBLIC OF;
Junyong AHN, Seoul, KOREA, REPUBLIC OF;
Hyungwook CHOI, Seoul, KOREA, REPUBLIC OF;
Wonjae CHANG, Seoul, KOREA, REPUBLIC OF;
Jaesung KIM, Seoul, KOREA, REPUBLIC OF;

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IR103 (Rev. 10/09)

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT7595422

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
JUNGMIN HA	03/02/2016
SUNGJIN KIM	03/02/2016
JUHWA CHEONG	03/02/2016
JUNYONG AHN	03/02/2016
HYUNGWOOK CHOI	03/02/2016
WONJAE CHANG	03/02/2016
JAESUNG KIM	03/02/2016

RECEIVING PARTY DATA

Name:	LG ELECTRONICS INC.
Street Address:	128, YEOUI-DAERO, YEONGDEUNGPO-GU
City:	SEOL
State/Country:	KOREA, REPUBLIC OF
Postal Code:	07336

PROPERTY NUMBERS Total: 5

Property Type	Number
Application Number:	16250463
Patent Number:	10230009
Patent Number:	10014419
Patent Number:	11239379
Patent Number:	11133426

CORRESPONDENCE DATA

Fax Number: (703)770-7900

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: (703) 770-7901

Email: docket_ip@pillsburylaw.com, chad.hammerlind@pillsburylaw.com, amanda.childs@pillsburylaw.com, nicole.banks@pillsburylaw.com

Correspondent Name: PILLSBURY WINTHROP SHAW PITTMAN LLP

Address Line 1: P.O. BOX 10500

Address Line 2: ATTN. DOCKETING DEPT.

Address Line 4:	MCLEAN, VIRGINIA 22102
ATTORNEY DOCKET NUMBER:	066061-0571463
NAME OF SUBMITTER:	NICOLE BANKS
SIGNATURE:	/Nicole Banks/
DATE SIGNED:	10/18/2022
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 3
source=066061-0571463 Parent Assignment - Inventors to LG#page3.tif
source=066061-0571463 Parent Assignment - Inventors to LG#page4.tif
source=066061-0571463 Parent Assignment - Inventors to LG#page5.tif

BIRCH, STEWART, KOLASCH & BIRCH, LLP
P.O. Box 747 • Falls Church, Virginia 22040-0747
Telephone: (703) 205-8000 • Facsimile: (703) 205-8050 • Email: mailroom@bskb.com

DECLARATION AND ASSIGNMENT FOR PATENT AND DESIGN APPLICATIONS

UNITED STATES PATENT RIGHTS, OR
UNITED STATES PLUS ALL FOREIGN PATENT RIGHTS

Title of Invention ⇨ SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME

As a below named inventor (hereinafter designated as the undersigned), I hereby declare that:

This declaration is directed to the application attached hereto.

Application not Attached ⇨ If the application is not attached hereto, the application is as identified by the attorney docket number as set forth above and/or the following:

Enter Appln. No. ⇨ United States Application Number or PCT International Appln. No. 14/953,264

Enter Filing Date ⇨ filed on November 27, 2015.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I have reviewed and understand the contents of the above-identified application, including the claims.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

WHEREAS, the undersigned has invented certain new and useful improvements described in the application identified.

Insert Name of Assignee ⇨ WHEREAS, LG ELECTRONICS INC.

Insert Address of Assignee ⇨ of 128, Yeoui-daero, Yeongdeungpo-gu, Seoul, 07336, Republic of Korea

its heirs, successors, legal representatives and assigns (hereinafter designated as the Assignee) is desirous of acquiring the entire right, title and interest in and to said invention and in and to any Letters Patent(s) that may be granted therefor in the United States of America and

Check Box if Appropriate ⇨ ☐ **in any foreign countries.**

NOW, THEREFORE, for good and valuable consideration, the receipt of which is hereby acknowledged, the undersigned has sold, assigned and transferred, and by these presents does (do) sell, assign and transfer unto said Assignee the full and exclusive right to the said invention in the United States of America, its territories, dependencies and possessions and the entire right, title and interest in and to any and all Letters Patent(s) which may be granted therefor in the United States of America, its territories, dependencies and possessions, and if the box above is designated, in any and all foreign countries; and to any and all divisions, reissues, continuations, conversions and extensions thereof for the full term or terms for which the same may be granted.

The undersigned agrees to execute all papers necessary in connection with this application and any continuing, divisional, conversion or reissue applications thereof and also to execute separate assignments in connection with such applications as the Assignee may deem necessary or expedient.

The undersigned agrees to execute all papers necessary in connection with any interference which may be declared concerning this application or continuation, division, conversion or reissue thereof or Letters Patent(s) or reissue patent issued thereon and to cooperate with the Assignee in every way possible in obtaining and producing evidence and proceeding with such interference.

The undersigned agrees to execute all papers and documents and to perform any act which may be necessary in connection with claims or provisions of the International Convention for the Protection of Industrial Property or similar agreements.

The undersigned agrees to perform all affirmative acts which may be necessary to obtain a grant of (a) valid United States of America patent(s) or a grant of (a) valid United States of America and any foreign patent(s) to the Assignee and to vest all rights therein hereby conveyed to said Assignee as fully and entirely as the same would have been held by the undersigned if this Assignment and sale had not been made.

The undersigned hereby authorizes and requests the Patent and Trademark Office Officials in the United States of America and in any foreign countries to issue any and all Letters Patent(s) resulting from said application or any continuing, divisional conversion or reissue applications thereof to the said Assignee, as Assignee of the entire interest, and hereby covenants that he has the full right to convey the entire interest herein assigned, and that he has not executed, and will not execute, any agreement in conflict herewith.

The undersigned hereby grants the law firm of Birch, Stewart, Kolasch & Birch, LLP the power to insert any further identification which may be necessary or desirable in order to comply with the rules of the U.S. Patent and Trademark Office.

The undersigned hereby covenants that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with this assignment.

The undersigned hereby acknowledges that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

In witness whereof, executed by the undersigned on the date opposite the undersigned name.

LEGAL NAME OF INVENTOR

Inventor's Name ⇨ Inventor: Jungmin HA Date: 2016. 3. 2.

Inventor's Signature ⇨ Signature:

An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use a separate form for each inventor; or check the box below and complete the attached page(s) to list additional inventors.

☒ Additional inventors are being named on the 1 supplemental sheet attached hereto.

Attorney Docket No. 1630-1332PUS1

SUPPLEMENTAL SHEET FOR DECLARATION AND ASSIGNMENT

ADDITIONAL INVENTORS
Supplemental Sheet Page 1 of 1

LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Sungjin KIM Date: 2016. 3. 2

Inventor's Signature ⇨ Signature:

LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Juh wa CHEONG Date: 2016. 3. 2

Inventor's Signature ⇨ Signature:

LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Junyong AHN Date: 2016. 3. 2

Inventor's Signature ⇨ Signature:

LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Hyungwook CHOI Date: 2016. 3. 2

Inventor's Signature ⇨ Signature:

LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Wonjae CHANG Date: 2016. 3. 2

Inventor's Signature ⇨ Signature:

LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Jaesung KIM Date: 2016. 3. 2

Inventor's Signature ⇨ Signature: KIM JAE SUNG

LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Date:

Inventor's Signature ⇨ Signature:

LEGAL NAME OF JOINT INVENTOR, IF ANY

Inventor's Name ⇨ Inventor: Date:

Inventor's Signature ⇨ Signature:

BSKB-DECASSIGN\(09-12)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

POWER OF ATTORNEY BY ASSIGNEE
(REVOCATION OF PRIOR POWERS AND EXCLUSION OF INVENTIVE ENTITY)

In re PATENTs/PATENT application(s) assigned to:

Assignee: Shangrao Jinko solar Technology Development Co., LTD

Address: NO. 3 YINGBIN ROAD, SHANGRAO ECONOMIC AND TECHNICAL DEVELOPMENT ZONE, JIANGXI PROVINCE, CHINA

The above assignee (hereinafter "Assignee") hereby revokes all powers of attorney previously given and hereby appoints and authorizes the attorneys associated with

Customer Number 00909
(the customer number associated with the attorneys of
Pillsbury Winthrop Shaw Pittman LLP)

to prosecute and transact all business in the U.S. Patent and Trademark Office connected with the following matters, and any applications claiming priority to one or more of the following matters; and to the exclusion of the inventive entity or any prior assignees:

U.S. Patent Application No. or U.S. Patent No.	Filing Date
US12/812910	2010/7/14
US15/076111	2016/3/21
US16/560384	2019/9/4
US17/540983	2021/12/2
US14/478935	2014/9/5
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US9362752	2016/6/7
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US10170646	2019/1/1
US10566487	2020/2/18
US9947810	2018/4/17
US9722104	2017/8/1
US10014419	2018/7/3
US10230009	2019/3/12
US11239379	2022/2/1
US11133426	2021/9/28
US11164984	2021/11/2

Direct correspondence to the address associated with Customer Number **00909.**

Assignee hereby authorizes the aforesaid attorneys to accept and follow instructions from its authorized representatives, **Beijing Uni-intel Patent and Trademark Law Firm**, as to any actions to be taken in the U.S. Patent and Trademark Office regarding the above-identified application. In the event of a change in the person(s) from whom instructions may be taken, the aforesaid attorneys will be so notified by Assignee.

The undersigned confirms that he or she is authorized to act on behalf of the assignee.

Shangrao Jinko solar Technology Development Co., LTD

Signed: Xiande Li

Name: Xiande Li

Title: President

Date: 2022.09.21

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
15/643,180	**11/07/2022 02:16:54 PM ET**	**1630-1332PUS2**

Title of Invention

SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	10014419
CONFIRMATION #	7835	FILED BY	Nicole Banks
PATENT CENTER #	61150534	FILING DATE	07/06/2017
CUSTOMER #	2292	FIRST NAMED INVENTOR	Jungmin HA
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Chad Hammerlind

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
066061 Power of Attorney - Shangrao Jinko solar Technology Development Co., LTD filed 07NOV2022.pdf	4	Power of Attorney	877 KB
066061-0571520 Statement under 37 CFR 373c filed 07NOV2022.pdf	3	Assignee showing of ownership per 37 CFR 3.73	114 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)

066061 Power of Attorney - Shangrao Jinko solar Technology Development Co., LTD filed 07NOV2022.pdf	0331ECB111A0D5B4789152E9D9DA52825ACCEB89182E2B78BF527611A4F993FC5B0CE4FF5287A9D0FF39A02A3244170D2CAE1A499E0CF2732B3A6BD50C71F466
066061-0571520 Statement under 37 CFR 373c filed 07NOV2022.pdf	96028A6DD76A10DA48AC638A3FA778B67913CF56E457CA7229CFEEF7F5C5DA286D464D7C2A765EA3F1330EB0B364B5656F32DF227F94268AEEC6F052F375CC90

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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PTO/AIA/96 (08-12)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Shangrao Jinko solar Technology Development Co., LTD

Application No./Patent No.: 10,014,419 Filed/Issue Date: July 03, 2018

Titled: SOLAR CELL AND METHOD FOR MANUFACTURING THE SAME

Shangrao Jinko solar Technology Development Co., LTD, a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: INVENTORS To: LG ELECTRONICS INC.

The document was recorded in the United States Patent and Trademark Office at Reel 061448, Frame 0929, or for which a copy thereof is attached.

2. From: LG ELECTRONICS INC. To: Shangrao Jinko solar Technology Development Co., LTD

The document was recorded in the United States Patent and Trademark Office at Reel 061572, Frame 0487, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

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5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

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6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Chad Hammerlind/	November 7, 2022
Signature	Date
Chad Hammerlind	67,565
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/643,180	07/06/2017	Jungmin HA	

CONFIRMATION NO. 7835

POA ACCEPTANCE LETTER

909
Pillsbury Winthrop Shaw Pittman, LLP
PO Box 10500
McLean, VA 22102

OC000000136800215

Date Mailed: 11/10/2022

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/07/2022.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/nrhayden/

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/643,180	07/06/2017	Jungmin HA	1630-1332PUS2

CONFIRMATION NO. 7835

POWER OF ATTORNEY NOTICE

2292
BIRCH STEWART KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
Falls Church, VA 22042-1248

OC000000136800206

Date Mailed: 11/10/2022

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/07/2022.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/nrhayden/