Progress in Surface Passivation of Heavily Doped n-Type and p-Type Silicon by Plasma-Deposited AlO_x/SiN_x Dielectric Stacks

Shubham Duttagupta, Fa-Jun Ma, Serena Fen Lin, Thomas Mueller, Armin G. Aberle, and Bram Hoex

***Abstract*—We report an outstanding level of surface passivation for both n^+ and p^+ silicon by AlO_x/SiN_x dielectric stacks deposited in an inline plasma-enhanced chemical vapor deposition (PECVD) reactor for a wide range of sheet resistances. Extremely low emitter saturation current densities (J_{0e}) of 12 and 200 fA/cm^2 are obtained on 165 and 25 Ω/sq n^+ emitters, respectively, and 8 and 45 fA/cm^2 on 170 and 30 Ω/sq p^+ emitters, respectively. Using contactless corona–voltage measurements and device simulations, we demonstrate that the surface passivation mechanism on both n^+ and p^+ silicon is primarily due to a relatively low interface defect density of $<10^{11}$ eV^{-1}cm^{-2} in combination with a moderate fixed negative charge density of (1–2) $\times$ 10^{12} cm^{-2}. From advanced modeling, the fundamental surface recombination velocity parameter is shown to be in the order of 10^4 cm/s for PECVD AlO_x/SiN_x passivated heavily doped n^+ and p^+ silicon surfaces.**

***Index Terms*—Aluminum oxide/silicon nitride (AlO_x/SiN_x) stacks, boron-doped emitters, crystalline silicon, phosphorus-doped emitters, plasma-enhanced chemical vapor deposition (PECVD), surface passivation.**

I. Introduction

In recent years, amorphous aluminum oxide (AlO_x) has received tremendous interest from the photovoltaic community for its application as a surface passivation film for crystalline silicon wafer solar cells. AlO_x films provide excellent surface passivation on lightly doped n-type and p-type silicon as well as on heavy doped p^+ silicon [1]–[5]. In addition to a low interface defect density ($\sim 10^{11}$ eV^{-1}cm^{-2}), a distinguished property of AlO_x is the presence of a high negative charge density (10^{12}–10^{13} cm^{-2}, in units of elementary charges) in the film. This is especially beneficial on p-type c-Si surfaces as the minority carriers (electrons) are effectively shielded from the c-Si surface. Because of its excellent surface passivation properties on p-type surfaces, AlO_x has mainly been considered for the application in p-type passivated emitter and rear cell cells, p-type aluminum local back-surface field (Al-LBSF) cells, and n-type passivated emitter and rear locally diffused cells [6], [7].

Excellent passivation of heavily doped n^+ and p^+ silicon surfaces is very important for high-efficiency Si wafer solar cells. Some solar cell structures, such as interdigitated back-contact (IBC) solar cells, require simultaneous passivation of both dopant polarities [8], [9]. For this application, preferentially a suitable dielectric is needed that can passivate both n^+ and p^+ silicon surfaces simultaneously. Thick ($\sim$100 nm) thermal silicon oxide (SiO_2) films or stacks consisting of a thin (5–30 nm) SiO_2 film capped by a 50–100-nm-thick silicon nitride (SiN_x) film are often used due to their ability to passivate both n^+ and p^+ silicon surfaces [8]–[12]. However, low-temperature ($<$400 °C) surface passivation is typically preferred for the fabrication of industrial high-efficiency silicon wafer solar cells, due to its potential cost effectiveness, lower thermal budget, and the possibility for inline processing. Recently, Mihailetchi *et al*. reported excellent results for p^+ surfaces passivated by a stack consisting of an ultrathin oxide grown by hot HNO_3 and then capped with a SiN_x film [13]. Although no specific results are available in regards to its capability of passivating n^+ silicon surfaces, it can be considered a good method for passivating both n^+ and p^+ silicon surfaces simultaneously as these layers have already been used for large-area screen-printed IBC solar cells showing good efficiencies [14]–[17]. However, it should be noted that these devices showed moderate implied V_{oc} (iV_{oc}) in the range of 660–680 mV and also resulted in moderate solar cell open-circuit voltages of $V_{oc} < 650$ mV [14]–[17]. It is also suggested in these publications that an optimized dielectric is still needed that can passivate both n^+ and p^+ silicon surfaces simultaneously in order to achieve higher open-circuit voltage, and therefore, higher solar cell efficiency.

AlO_x films provide excellent surface passivation on p^+ silicon for an arbitrary sheet resistance [2], [18], [19]. Recently it has been shown that n^+-doped Si in a certain sheet resistance range can also be passivated by Al_2O_3 films grown by plasma-assisted and O_3-based atomic layer deposition (ALD), however, the results are not yet competitive [20], [21]. In addition, PA-ALD is not yet an industrially feasible technique. Thus, it is of great interest to investigate if negatively charged AlO_x films deposited by the industrial PECVD can provide excellent passivation on both n^+ and p^+ silicon surfaces.

In this study, we demonstrate that PECVD AlO_x/SiN_x dielectric stacks can provide excellent passivation on both heavily doped n^+ and p^+ silicon surfaces that are relevant for the industrial solar cell application. These results are primarily explained

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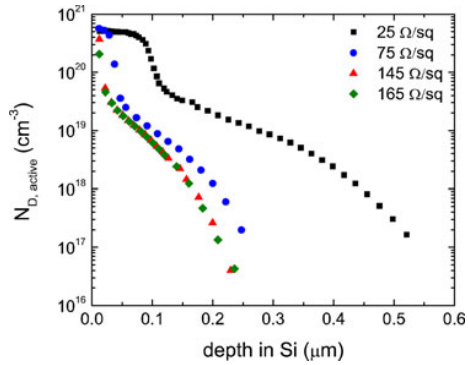

Fig. 1. Phosphorus dopant profile of n^+pn^+ samples measured by ECV profiling. The sheet resistance values determined by four-point probe measurements are shown in the graph.

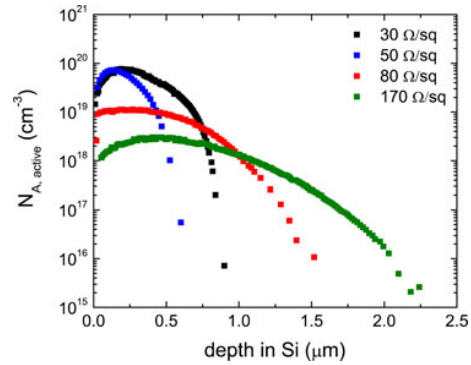

Fig. 2. Boron dopant profile of p^+np^+ samples measured by ECV profiling. The sheet resistance values determined by four-point probe measurements are shown in the graph.

by a low midgap interface defect density of $<10^{11}$ eV^{-1}cm^{-2}, which is beneficial for both n^+ and p^+ silicon surfaces. The stacks developed in this study feature a relatively moderate fixed negative charge density of (1–2) $\times$ 10^{12} cm^{-2}, as determined by contactless corona–voltage (*C*–*V*) experiments. Based on device simulations, we show that moderate fixed charge densities in the range of -10^{12} cm^{-2}–10^{12} cm^{-2} do not significantly affect the emitter saturation current density of typical industrial n^+ diffusions. Thus, the passivation is mainly ruled by the excellent electronic quality of the interface or low interface defect density.

II. Experimental Details

Symmetrical n^+pn^+ carrier lifetime structures were fabricated using an industrial $POCl_3$ diffusion process. The sheet resistance of the n^+ emitter was varied by changing the temperature and time of the $POCl_3$ diffusion. The phosphorus dopant profiles of the n^+pn^+ samples used in this study were measured with the electrochemical voltage (ECV) method, as shown in Fig. 1. The p-type Si wafers were monocrystalline (Cz method, boron-doped, 5–8 Ωcm), about 150 μm thick, pseudosquare (125 mm $\times$ 125 mm), and with a (100) surface orientation.

The p^+np^+ structures were fabricated by an industrial BBr_3 diffusion process. The p^+ emitter sheet resistance was varied by varying the process conditions during the BBr_3 diffusion and by a postdiffusion oxidation, as explained in detail elsewhere [18]. The boron dopant profiles of the p^+np^+ samples used in this study were measured by the ECV method, as shown in Fig. 2. The n-type Si wafers were monocrystalline (Cz, phosphorus-doped, 6–8 Ωcm), about 150 μm thick, pseudosquare (125 mm $\times$ 125 mm), and with a (100) surface orientation. After the diffusion process, the phosphorus or borosilicate glass layers were removed by dipping in HF solution, followed by rinsing in deionised water.

Prior to the deposition of the PECVD dielectric films, the samples were cleaned using the Radio Corporation of America (RCA) clean with a final HF dip followed by water rinsing and drying to ensure an H-terminated surface. The sheet resistance of the p^+ and n^+ diffusions was unaffected by the predeposition cleaning as confirmed by four-point probe measurements. The n^+pn^+ and p^+np^+ samples with various sheet resistances were coated on both sides with 30-nm AlO_x capped with 70-nm SiN_x, using an industrial inline microwave-powered remote PECVD reactor (SiNA-XS, Roth & Rau, Germany). We emphasize that all samples (n^+pn^+ and p^+np^+) were processed without any change in the PECVD process conditions. The deposition conditions are summarized in Table I.

After the PECVD processes, the samples received an activation anneal in an industrial fast firing furnace (Ultraflex, Despatch, USA) for a few seconds at a set peak temperature of $>$800 °C, similar to the cofiring step applied to the screen-printed metallization of industrial silicon wafer solar cells. The effective minority carrier lifetime ($\tau_{\rm eff}$) of the lifetime samples was measured using a contactless flash-based photoconductance decay tester (WCT-120, Sinton Instruments), in both the quasi-steady-state and the transient mode [22]. From the $\tau_{\rm eff}$ measurement, the emitter saturation current density (J_{0e}) per side of the n^+pn^+ and p^+np^+ samples was extracted from the slope of the Auger-corrected inverse lifetime versus injection level curve under high-injection conditions ($\Delta n \sim 10^{15}$ to 10^{16} cm^{-3} in our case), using the relation proposed by Kane and Swanson [23];

$$\frac{1}{\tau_{\rm eff}} - \frac{1}{\tau_{\rm Auger}} = \frac{1}{\tau_{\rm SRH}} + 2\frac{J_{0e}\,(N_d + \Delta n)}{q n_i^2 W} \qquad (1)$$

where $\tau_{\rm Auger}$ and $\tau_{\rm SRH}$ are the Auger lifetime and the Shockley–Read–Hall lifetime in the bulk of the sample [24], respectively, N_d and Δn are the doping concentration and the excess carrier concentration (or "injection level") in the bulk of the sample, q is the elementary charge, n_i is the intrinsic carrier concentration (8.6×10^9 cm^{-3} at 298 K) [25], and W is the thickness of the sample. In addition, contactless *C*–*V* measurements (PV-2000, Semilab SDI Inc., USA) were carried out to extract the fixed charge density (Q_f) and the interface defect density ($D_{\rm it}$) of the dielectric films on undiffused Si samples. The details of the measurement system and extraction procedure of Q_f and $D_{\rm it}$ are explained elsewhere [26]–[29].

III. Results and Discussion

Fig. 3 shows the measured injection level dependence of the Auger-corrected inverse effective carrier lifetime of industrially fired n^+pn^+ samples passivated on both sides by a PECVD AlO_x/SiN_x dielectric stack. The results cover a wide range of industry relevant sheet resistances (25–165 Ω/sq).

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TABLE I
EXPERIMENTAL DETAILS USED FOR THE DEPOSITION OF THE DIELECTRIC FILMS IN THIS STUDY

Dielectric	Process gas	Deposition temperature (°C)	Reactor pressure (mbar)	Plasma power (W)
AlO_x	$Al(CH_3)_3 + N_2O + Ar$	450	0.10	1500
SiN_x	$SiH_4 + NH_3$	200	0.20	3000

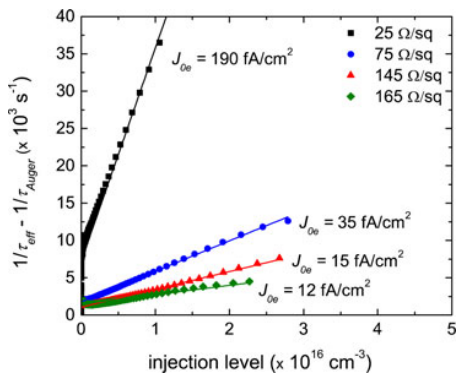

Fig. 3. Measured injection level dependence of the Auger-corrected inverse effective lifetime of industrially fired n^+pn^+ samples symmetrically passivated by PECVD AlO_x/SiN_x dielectric stacks (symbols). The sheet resistance of the n^+ emitters determined by four point probe measurements is shown in the legend. The J_{0e} values obtained from the straight-line fits (solid lines) are also shown.

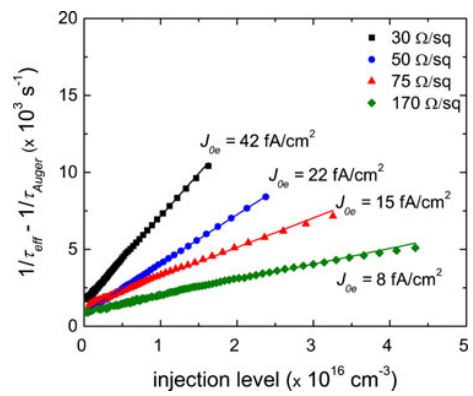

Fig. 4. Measured injection level dependence of the Auger-corrected inverse effective lifetime of industrially fired p^+np^+ samples symmetrically passivated by PECVD AlO_x/SiN_x dielectric stacks (symbols). The sheet resistance of the p^+ emitters determined by four point probe measurements is shown in the legend. The J_{0e} values obtained from the straight-line fits (solid lines) are also shown.

It is emphasized that we observe a linear relationship for all lifetime samples, allowing the extraction of J_{0e} values using (1). This was not always the case in the work of Hoex *et al.*, where it was mentioned that the relationship was not linear for 100–200 Ω/sq n^+ emitters passivated by PA-ALD Al_2O_3 [20]. This was attributed to the very high negative fixed charge density (up to 10^{13} cm^{-2}) of PA-ALD Al_2O_3 films, which strongly increased the minority carrier (hole) density at the n^+ surface in their work, and thereby, caused an injection level dependent J_{0e}. In this study, we show an excellent level of surface passivation with extremely low J_{0e} values of 12 fA/cm^2 for 165 Ω/sq planar n^+ emitters passivated by PECVD AlO_x/SiN_x dielectric stacks after an industrial firing process. As a matter of fact, the J_{0e} values obtained in this study are similar to, or even better than, the best values reported in the literature for n^+ emitters passivated by PECVD SiN_x [30]. These results are also significantly better than those obtained for n^+ emitters passivated by Al_2O_3 grown by ALD techniques reported so far [20], [21].

Identical PECVD stacks were also used to passivate p^+ emitters. Fig. 4 shows the measured injection level dependence of the Auger-corrected inverse effective carrier lifetimes of industrially fired p^+np^+ samples passivated on both sides with an AlO_x/SiN_x dielectric stack. The lifetime samples show a clear linear relationship, indicating again that (1) can be used to extract the J_{0e} value of this emitter. An extremely low J_{0e} value of 8 fA/cm^2 was obtained for a 170-Ω/sq emitter, which is comparable with the values obtained for p^+ emitters passivated by Al_2O_3 films grown by the PA-ALD [2]. It should be noted that in our earlier work, p^+np^+ samples were passivated on both sides with an AlO_x/SiN_x dielectric stack deposited under slightly different processing conditions [18]. In this study, both n^+pn^+ and p^+np^+ samples were processed simultaneously with 100 °C higher deposition temperature for AlO_x and ∼100 °C lower deposition temperature for capping SiN_x layer. This resulted in better interface quality and more importantly, a reduced fixed charge density. These stacks also provide excellent results on p^+ Si surfaces for a wide range of sheet resistance with similar J_{0e} values as reported earlier [18].

Table II summarizes the experimentally measured effective lifetime ($\tau_{\rm eff}$ at $\Delta n = 10^{15}$ cm^{-3}), emitter saturation current density (J_{0e}), and implied $V_{\rm oc}$ ($iV_{\rm oc}$) for n^+pn^+ and p^+np^+ samples symmetrically passivated by an industrially fired AlO_x/SiN_x dielectric stack. Note that effective lifetime and implied $V_{\rm oc}$ also depends on factors such as bulk doping level and bulk effective minority carrier lifetime of the used silicon wafer and the optical properties of the passivation coating, hence, care must be taken when comparing experimental values between different experiments. $V_{\rm oc,limit}$ represents the one-Sun open-circuit voltage limit of a solar cell at 25 °C calculated from the experimentally measured J_{0e} and assuming a short-circuit current density ($J_{\rm sc}$) of 40 mA/cm^2 with an ideal diode law ($n = 1$) by [22], [31]:

$$V_{\rm oc,limit} = n\frac{kT}{q}\ln\left(\frac{J_{\rm sc}}{J_{0e}} + 1\right) \tag{2}$$

where n is the diode ideality factor, which is considered one in this calculation. kT/q is 25.9 mV at 25 °C with k, T, q being the Boltzmann constant, absolute temperature in Kelvin and the elementary charge, respectively.

Fig. 5 shows the experimentally obtained J_{0e} values for n^+ and p^+ emitters passivated by industrially fired PECVD

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TABLE II
EXPERIMENTALLY DETERMINED EFFECTIVE LIFETIME ($\tau_{\rm eff}$) AT $\Delta n = 10^{15}$ cm^{-3}, SATURATION CURRENT DENSITY (J_{0e}) PER SIDE AND IMPLIED $V_{\rm oc}$ ($iV_{\rm oc}$) FOR n^+pn^+ AND p^+np^+ SAMPLES SYMMETRICALLY PASSIVATED BY AN AlO_x/SiN_x STACK

	Sheet resistance for phosphorus-diffused n^+ surface on p-type Si (Ω/sq.)				Sheet resistance for boron-diffused p^+ surface on n-type Si (Ω/sq.)			
	25	**75**	**145**	**165**	**30**	**50**	**80**	**170**
τ_{eff} **(µs)**	94	465	770	700	484	841	700	930
J_{0e} **(fA/cm^2)**	190	35	15	12	45	22	15	8
iV_{oc} **(mV)**	640	688	706	703	670	690	700	712
$V_{oc,\,limit}$ **(mV)**	670	713	735	741	707	725	735	751

The $V_{\rm oc,limit}$ was calculated by (2) using the measured J_{0e} values.

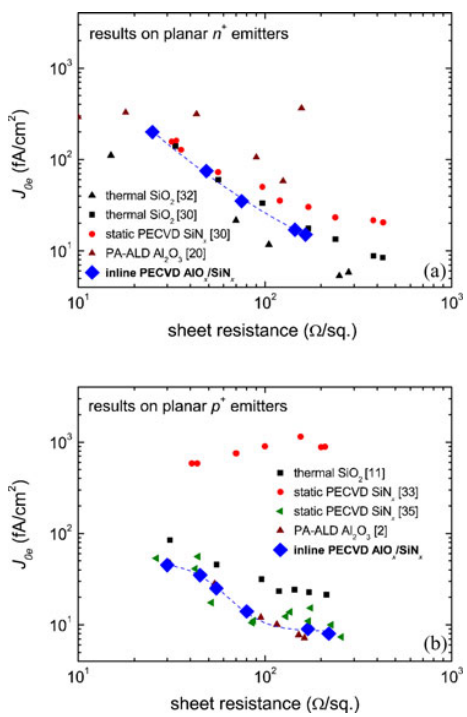

Fig. 5. Experimentally obtained J_{0e} values (diamonds in this work) for (a) n^+ emitters and (b) p^+ emitters passivated by industrially fired PECVD AlO_x/SiN_x stacks (the dotted lines are guides to the eye). Each of our J_{0e} values is the average result of a batch of 10 samples. Also shown, for comparison, are state-of-the-art J_{0e} values reported in the literature for planar n^+ and p^+ emitters passivated by thermal SiO_2, PECVD SiN_x, and ALD-grown Al_2O_3.

AlO_x/SiN_x stacks. For comparison, the best published results from the literature are included as well. It should be noted that the preparation of the n^+ and p^+ emitters in the various studies were different and most likely resulted in different dopant profiles for a comparable sheet resistance. This potentially affects the Auger recombination losses in these emitters. However, the general trend can be used for comparison. It is evident from Fig. 5 that thermal SiO_2 is a good candidate for both dopant polarities, showing excellent surface passivation of n^+ emitters and a decent surface passivation for p^+ emitters after either *alneal* (aluminum-annealing) or forming gas anneal (FGA) [11], [30], [32]. PECVD SiN_x provides excellent passivation of n^+ emitters after FGA [30]. Generally, these SiN_x films provide a compromised level of surface passivation on p^+ emitters [11], [33]. Only limited reports are available were PECVD SiN_x provides a good level of surface passivation on p^+ emitters, however, the underlying mechanism is not yet properly understood [34], [35]. Similarly PA-ALD Al_2O_3 films provide only a moderate passivation on n^+ emitters [see Fig. 5(a)], however, p^+ surfaces with an arbitrary sheet resistance can be well passivated with PA-ALD Al_2O_3 films [2], [20]. Based on the experimental results presented in this study, it is clear that our industrially fired PECVD AlO_x/SiN_x stacks provide an excellent level of surface passivation on both n^+ and p^+ emitters, for the entire investigated sheet resistance range. Hence, our work demonstrates that these PECVD AlO_x/SiN_x stacks can be used to simultaneously passivate all c-Si surfaces that are of relevance in today's PV industry.

To obtain more insight into the interface properties such as fixed charge density (Q_f) and interface defect density (D_{it}) of our industrially fired AlO_x/SiN_x stacks, contactless C–V measurements were performed on undiffused Si samples. These measurements revealed that the industrially fired AlO_x/SiN_x dielectric stacks on c-Si used in this study have a comparatively low midgap interface defect density of $<10^{11}$ eV^{-1}cm^{-2} in combination with a moderate negative fixed charge density in the range of (1–2) $\times$ 10^{12} cm^{-2}. Note that the fixed charge density in the dielectric stack is highly dependent on the deposition conditions and the postdeposition treatments used, as will be reported in detail in a separate study.

Understanding the surface passivation of p^+ Si surfaces by negatively charged dielectrics is relatively straightforward. A low interface defect density provides excellent chemical passivation. In addition, the negative fixed charge density reduces the minority carrier concentration at p^+ Si surfaces (for the B surface concentrations investigated in this study) providing field-effect passivation. Understanding the passivation of n^+ Si surfaces by negatively charged dielectrics is, however, not straightforward. For this purpose, we used advanced computer modeling (TCAD, Sentaurus) to study the role of field-effect passivation for heavily doped n^+ surfaces. In these simulations, we take both the fundamental hole surface recombination

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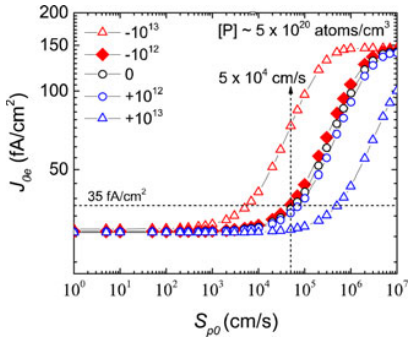

Fig. 6. Simulated J_{0e} as a function of the S_{p0} at the c-Si/dielectric interface for high (10^{13} cm^{-2}) and moderate (10^{12} cm^{-2}) fixed charge densities of both polarities in the dielectric film. A symmetrical n^+pn^+ sample was used with a 75-Ω/sq diffusion per side (the experimental measured diffusion profile from Fig. 1 was used in the simulation).

velocity parameter (S_{p0}) and the interface fixed charge (Q_f) into account, similar to the approach presented by Girish *et al.* [36] and Aberle *et al.* [37], and furthermore, using the physical models from [38] and [39], S_{p0} is the surface recombination velocity parameter for holes assuming flat band conditions and can be expressed by

$$S_{p0} \equiv \nu_{\rm th}\sigma_p N_{\rm st} \tag{3}$$

where $v_{\rm th}$ is the thermal velocity, σ_p is the capture cross-section for holes, and $N_{\rm st}$ is the number of surface states per unit area [40]. Using the measured n^+ dopant profile of the 75 Ω/sq diffusion from Fig. 1, J_{0e} versus S_{n0} curves for various fixed charge densities were determined. The results are shown in Fig. 6. From Fig. 6, it is clear that positive fixed charge densities are beneficial for the passivation of the 75-Ω/sq n^+ Si diffusion, resulting in significantly lower J_{0e} values for similar S_{p0} values. On the other side, a very high negative fixed charge density of 10^{13} cm^{-2} is found to be detrimental and results in higher J_{oe} values, in good agreement with the experimental results reported by Hoex *et al.* for n^+ Si passivated by Al_2O_3 films grown by the PA-ALD [20].

For moderate fixed interface charge densities in the range of -10^{12} cm^{-2} to $+10^{12}$ cm^{-2}, it can be seen that the fixed charge is hardly affecting the J_{0e} over the whole investigated S_{p0} range, and hence, the passivation is predominantly ruled by chemical passivation in this case. It should be noted that a similar trend (effect of fixed charge) was observed on other n^+ diffusions used in this study; however, the fixed charge range will depend on the surface dopant concentration. The results in Fig. 6 also allow us to extract the S_{p0} value at the interface between the c-Si wafer and the AlO_x/SiN_x stack. Taking the measured J_{0e} value of 35 fA/cm^2 and the measured Q_f of -10^{12} cm^{-2}, we can see that this results in a S_{p0} value of $\sim 5 \times 10^4$ cm/s. This value is in the similar order to the S_{n0} (electron surface recombination velocity parameter) value obtained by our PECVD AlO_x/SiN_x stack on heavily doped p^+ Si surfaces, which is in the range of 10^4 cm/s [41]. We observe that the S_{p0} value obtained in this study is slightly better than the S_{p0} reported by Altermatt *et al.* ($> 10^5$ cm/s) for n^+ Si having a surface dopant density of $\sim 2 \times 10^{20}$ atoms/cm^3 passivated by FGA thermal SiO_2 [39]. Hence, these results indicate that heavily doped n^+ Si surfaces can be passivated as effectively as heavily doped p^+ Si surfaces using a negatively charged PECVD AlO_x/SiN_x stack.

IV. Conclusion

In conclusion, we have shown that both n^+-type and p^+-type c-Si surfaces in a very wide sheet resistance range are well passivated by an industrially fired PECVD AlO_x/SiN_x dielectric stack. This is an important step forward in surface passivation with AlO_x/SiN_x dielectric stacks, as some high-efficiency c-Si solar cell designs (for example, all back-contact and bifacial Si solar cells) require passivation of both dopant polarities. Based on contactless *C–V* measurements and device simulations, we show that a negatively-charged AlO_x/SiN_x stack with lower charge density can provide excellent passivation on both n^+-type and p^+-type c-Si surfaces, provided the interface defect density remains low. In combination with the excellent results obtained on undiffused c-Si surfaces, our work demonstrates that all c-Si surfaces of relevance in today's PV industry can be well passivated by a firing stable, low-temperature deposited, and industrially feasible dielectric stack.

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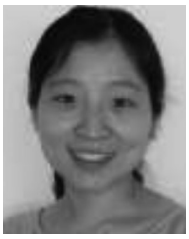

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