UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

RUNERGY USA INC. AND RUNERGY ALABAMA INC.

Petitioners,

v.

TRINA SOLAR CO., LTD.
Patent Owner.

Patent No. 9,722,104
Issued: August 1, 2017
Filed: November 27, 2015
Inventor: Jungmin Ha, *et al*.
Title: Solar Cell and Method for Manufacturing the Same
Inter Partes Review No. IPR2025-00007

DECLARATION OF SANJAY BANERJEE REGARDING U.S. PATENT NO. 9,722,104

I, Sanjay Banerjee, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: October 4, 2024

Sanjay Banerjee

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Appendix A – Materials Relied On

I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for Runergy USA Inc. and Runergy Alabama Inc. (collectively "Runergy U.S." or "Petitioners") as an expert witness in the above-captioned proceeding. I have been asked to provide my opinions about the state of the art of the technology related to U.S. Patent 9,722,104 (the "104 Patent") (EX1001) and on the patentability of claims 1-11 of this patent. The following is my written declaration on these topics.

B. Background and Qualifications

2. I currently serve as the Cockrell Family Regents Chair Professor of Electrical and Computer Engineering and Director of the Microelectronics Research Center at the University of Texas at Austin ("UT"). Prior to this position, I was first an Assistant Professor (September 1987 - August 1990) and later an Associate Professor (September 1990 - August 1993) at UT, before being named a Professor in September 1993. Prior to starting my academic work at UT, I was a member of the technical staff at Texas Instruments (Corporate R&D) from the time I completed my doctoral studies in 1983 until August 1987.

3. I received my Ph.D. in Electrical Engineering from the University of Illinois in 1983. I also received an M.S. in Electrical Engineering from the University of Illinois in 1981. I received a B. Tech. in Electronics from the Indian Institute of Technology at Kharagpur in 1979.

4. I have more than 40 years of experience in the field of electrical engineering, including extensive experience in semiconductor development and fabrication including that of solar cells, passivation, and dielectric materials. For example, I am a named author on 24 publications and conference proceedings relating to solar cells, as can be seen from my CV, EX1004.

5. I am a Fellow of the Institute of Electrical and Electronics Engineers ("IEEE"), the American Physical Society ("APS"), and the American Association for the Advancement of Science ("AAAS"). I have served on numerous professional and government committees in the electrical engineering field, including chairing multiple IEEE committees, meetings, and programs, serving on Morgan & Claypool's editorial board, and serving as a member on the International Technology Roadmap for Semiconductors ("ITRS").

6. I have taught courses in Semiconductor Physics, Solid State Electronic Devices, and Microelectronic Device Fabrication at UT. In particular, I have taught an undergraduate course every year for 30 years on Semiconductor Devices out of a textbook, "Solid State Electronic Devices," by Ben Streetman and Sanjay Banerjee (ISBN 0-13-335603). I provided a version of my textbook, the Sixth Edition copyrighted 2008, to counsel for Runergy U.S., which is submitted in this proceeding as EX1030. EX1030 is an authentic, true and correct copy of Solid State Electronic Devices as it was publicly available and sold from 2008 onward.

EX1030 is the copy of Solid State Electronic Devices I was using to teach courses in that time frame, years before 2015, and my students were required to obtain copies from book stores, the library, online, or any other means.

7. Several of my lectures out of the textbook relate to solar cells. In addition, I have delivered many courses to industry professionals on Semiconductor Devices and Memory and Semiconductor Processing. As a principal investigator, I have been the advisor to over 80 Doctoral and Masters students.

8. I am the co-author of several books and invited book chapters covering the area of electronic and semiconductor devices, including: Dopant Diffusion, Solid State Electronic Devices (three editions). I have authored or coauthored more than 1,000 papers and presentations in the areas of semiconductor devices and electronics development over the course of my career.

9. I have been the recipient of fifty grants to fund my research from a variety of funding agencies, including the National Science Foundation ("NSF"), DARPA, the Department of Energy, Semiconductor Research Corporation, the Department of Defense-Multidisciplinary University Research Initiative, and the Office of Naval Research. A number of the sponsored research grants on which I have been a principal or coinvestigator have related to solar cells and various deposition techniques for optoelectronic devices, including for example,

"Optoelectronic Devices by Photo-enhanced Chemical Vapor Deposition," (National Science Foundation, August 1988-July 1993).

10. I have received numerous other awards recognizing my extensive work in the electrical engineering field. For example, I was on the Advisory Board, and the Silicon Solar Cell Thrust Lead for the Bay Area Photovoltaics Consortium funded by the U.S. Department of Energy. This and other awards are described in more detail in my CV, submitted as EX1004.

C. Compensation and Prior Testimony

11. I am being compensated at a rate of $650.00 per hour for my time spent on this matter. I am also being reimbursed for reasonable and customary expenses associated with my work in this matter. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

12. I have previously submitted declarations in multiple IPR proceedings and have also testified as an expert witness in Federal Court and the ITC, as summarized in EX1004 at 1.

D. Information Considered

13. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this declaration and those listed as exhibits in **Appendix A**, attached to this declaration.

14. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions—including documents that may not yet have been provided to me.

15. My analysis of the materials produced in this investigation is ongoing and I will continue to review any new material as it is provided. This declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

II. LEGAL STANDARDS FOR PATENTABILITY

16. I am not a lawyer and am not providing any legal opinions. In providing my opinions in this declaration, I am relying upon certain basic legal principles that have been explained to me by counsel and which I am summarizing below.

17. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious from what was known before the invention was made.

18. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as "prior art" and

generally includes patents and printed publications (*e.g.*, books, journal publications, articles on websites, product manuals, *etc*.).

19. I understand that in this proceeding the Petitioner has the burden of proving that the claims are anticipated by or obvious from the prior art by a preponderance of the evidence. I understand that "a preponderance of the evidence" is evidence sufficient to show that a fact is more likely true than it is not.

20. I understand that in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. The claims after being construed in this manner are then to be compared to the information in the prior art.

21. I understand that in this proceeding, the information that may be evaluated is limited to patents and printed publications. My analysis below compares the claims to patents and printed publications that are prior art to the claims.

22. I understand that there are various ways in which prior art may render a patent claim unpatentable based on prior art patents and printed publications. First, the prior art can be shown to "anticipate" the claim. Second, the prior art can be shown to have made the claim "obvious" to a person of ordinary skill in the art. My understanding of the legal standards is set forth below.

A. Anticipation

23. I understand that the following standards govern the determination of whether a patent claim is "anticipated" by the prior art.

24. I have applied these standards in my evaluation of whether the claims would have been anticipated by the prior art.

25. I understand that the "prior art" includes patents and printed publications that existed before the earliest filing date (the "effective filing date") of the claim in the patent. I also understand that a patent will be prior art if it was filed before the effective filing date of the claimed invention, while a printed publication will be prior art if it was publicly available before that date.

26. I understand that, for a patent claim to be "anticipated" by the prior art, each and every requirement of the claim must be found, expressly or inherently, in a single prior art reference as recited in the claim. I understand that claim limitations that are not expressly described in a prior art reference may still be there if they are "inherent" to the thing or process being described in the prior art. I understand that a limitation can be "inherent" if that limitation is necessarily present in or the natural result of the elements explicitly disclosed by the prior art.

27. I understand that if a reference incorporates other documents by reference, the incorporating reference and the incorporated reference(s) should be treated as a single prior art reference for purposes of analyzing anticipation.

28. I understand that it is acceptable to consider evidence other than the information in a particular prior art document to determine if a feature is necessarily present in or inherently described by that reference.

B. <u>Obviousness</u>

29. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

30. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)[1]) as follows:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

31. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my

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[1] I understand from counsel that the America Invents Act ("AIA") versions of 35 U.S.C. §§ 102 & 103 apply to these proceedings.

evaluation of whether the claims would have been considered obvious as of the priority date of the patent.

32. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

33. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

34. I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this

evidence must be specifically connected to the invention rather than being associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of "objective factors" suggesting the claimed methods are not obvious, and reserve my right to address any such evidence if it is identified in the future.

35. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I understand that when the prior art does not expressly disclose a claim limitation, inherency may also supply a missing claim limitation in an obviousness analysis. I understand that inherency is established in the context of obviousness when the limitation at issue necessarily must be present, or the natural result of the combination of elements explicitly disclosed by the prior art. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

36. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one

device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using that technique to improve the other device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

37. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the "ordinary innovation" and experimentation that does no more than yield predictable results, which are inferences and creative steps that a person of ordinary skill in the art would employ.

38. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents/publications; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

39. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words "teaching, suggestion, and motivation." I understand that in 2007, the Supreme Court issued its decision in *KSR Int'l Co. v. Teleflex, Inc.,* 550 U.S. 398, where the Court rejected the previous requirement of a "teaching, suggestion, or motivation to combine" known elements of prior art for

purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that *KSR* confirms that any motivation that would have been known to a person of skill in the art, including common sense, or derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

40. I understand that a person of ordinary skill attempting to solve a problem will not be led only to those elements of prior art designed to solve the same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond the particular application being described in a reference, that if something can be done once it is obvious to do it multiple times, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents/publications together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

41. I understand that obviousness does not require that the features of a secondary reference be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have suggested to a Skilled Artisan. The disclosures of the prior art references need not be physically combinable. Combining the teachings of references should be the focus of the analysis.

42. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or leads away from the line of inquiry disclosed in the reference(s). A reference does not "teach away" from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (*e.g.*, because it would not work or explicit statements saying the combination should not be made).

43. I understand that a person of ordinary skill is also a person of ordinary creativity.

44. I further understand that in many fields, it may be that there is little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem

and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was "obvious to try" may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

III. THE 104 PATENT

A. Effective Filing Date of the 104 Patent

45. The 104 Patent, titled "Solar Cell and Method for Manufacturing the Same," was filed on November 27, 2015. EX1001. Based on the information on the face of the 104 Patent, it claims foreign priority to Korean Patent App. No. 10-2014-0168624, filed November 28, 2014, and Korean Patent App. No. 10-2015-0122846, filed August 31, 2015.

46. I have reviewed a translation of the November 28, 2014, Korean patent application (No. 10-2014-0168624) (EX1007), and based on my review, it is my opinion that the November 2014 Korean application does not support the 104

Patent's claim to priority. Every issued claim of the 104 Patent requires "*an isolation portion for preventing a contact between the first conductive type semiconductor region and the second conductive type semiconductor region, wherein the isolation portion excludes the tunnel layer and the first conductive type semiconductor region, and is in an edge portion of the first surface of the semiconductor substrate*." EX1001, cl. 1. I also understand from my review of the prosecution history of the 104 Patent that the "isolation portion" was deemed critical to patentability by the Examiner before issuing the patent. *See* ¶¶57-63 below.

47. The claimed isolation portion, however, was not disclosed in the November 2014 priority application. EX1007. The text does not mention or discuss isolation portions, let alone disclose all of the details of the isolation portion as claimed. EX1007. Likewise, none of the figures of the November 2014 application depict an isolation portion of any kind. EX1007. Thus, it is my opinion that the written description of the November 2014 Korean application does not support a priority claim for the 104 Patent claims.

48. I have also reviewed a translation of the August 31, 2015, Korean patent application (No. 10-2015-022846). EX1008. Based on my review, it is my opinion that the first mention of the "isolation portion" is in the August 31, 2015

priority application. Therefore, it is my opinion that the effective filing date of the 104 Patent is August 31, 2015.

B. Person of Ordinary Skill in the Art

49. I have reviewed the 104 Patent specification and its claims. Based on my experience in the field and the information disclosed in the 104 Patent that I discuss in this Declaration, I believe the person of ordinary skill in the art in the 104 Patent's field of solar cell design or manufacture in 2014-2015 ("Skilled Artisan") would have been someone with an advanced degree involving the disciplines of electrical engineering, applied physics, chemistry, or materials science, and at least two years of experience designing, developing, or researching in the field. Alternatively, that person would have had a bachelor's degree in electrical engineering, applied physics, or materials science, and at least three years of experience designing, developing, or researching in the field. By that definition, I was a Skilled Artisan before November 27, 2015, the filing date of U.S. Patent No. 9,722,104, as well as August 31, 2015 or November 28, 2014, the filing date of Korean applications No. 10-2015-022846 and No. 10-2014-0168624, respectively.

C. Overview of the 104 Patent

50. The 104 Patent discloses a solar cell as shown in Figures 2 and 3. Figure 2 shows a cross-section view of the solar cell, while Figure 3 shows a backside plan view of the same solar cell.

FIG. 2

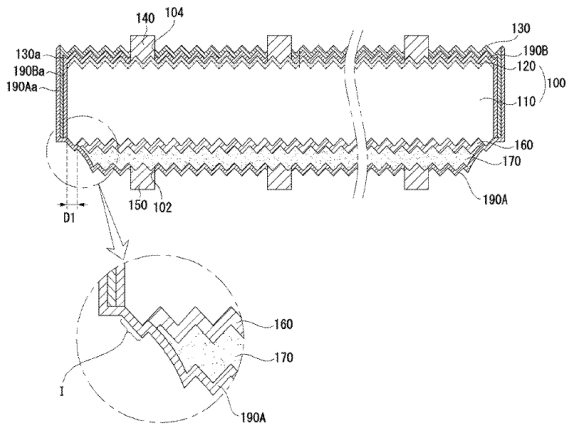
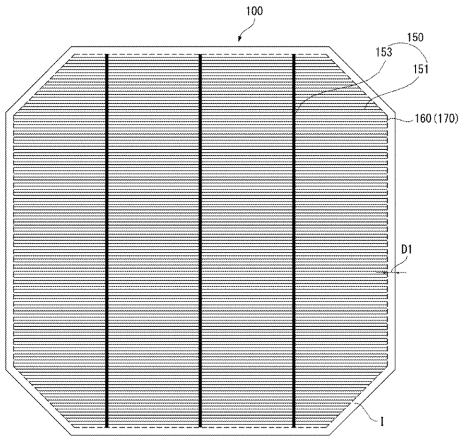


FIG. 3



51. The solar cell comprises a semiconductor substrate 100 that includes a base region 110 doped with impurities (or also called "dopants"), e.g., of a first conductive type. EX1001, 7:31-35. On the back surface of the substrate 100 (i.e., the bottom side in Figure 2), a "first conductive type semiconductor region 170" is formed having the same dopant conductive type as the substrate. EX1001, 7:43-42, 8:41-46. This "first conductive type semiconductor region 170" may be made of "polycrystalline silicon material" or otherwise called a "polysilicon layer." EX1001, 2:15-18; 8: 41-46, Abstract. By having the same dopant type as the substrate, the polysilicon first conductive type semiconductor region forms a "back surface field (BSF) region which has a higher doping concentration than the

semiconductor substrate 100" and can be referred to as a polysilicon BSF layer. EX1001, 10:10-16.

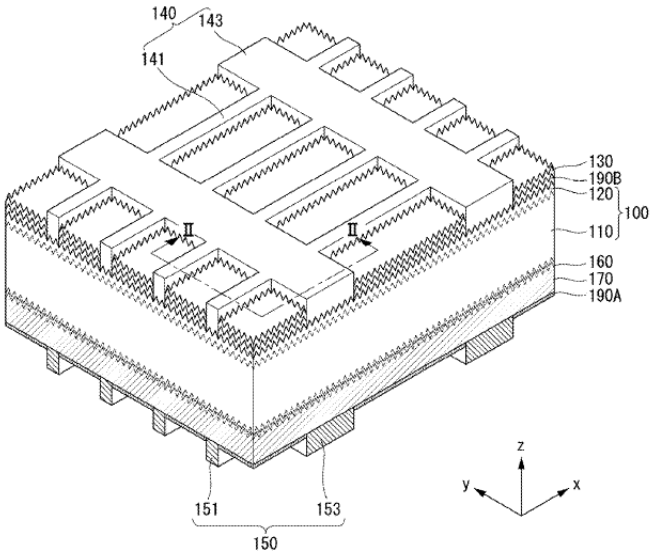
52. Between the polysilicon BSF layer (first conductive type semiconductor region) 170 and the substrate's base region 110, a tunnel layer 160 is formed. EX1001, 7:45-51. The tunnel layer 160 may include oxides. *Id*., 8:8-12.

53. On the front side of the solar cell, (i.e., the top sun-facing surface in Figure 2), a "second conductive type semiconductor region 120" is placed on the front surface of the substrate 100. EX1001, 9:38-41. This "second conductive type semiconductor region 120" includes dopants of different conductive type than the base region 110 and forms an emitter region, which also forms a pn junction along with the base region 110. EX1001, 10:16-25. The "second conductive type semiconductor region" is also referred to as the emitter region. EX1001, 10:21-20.

54. Passivation films 190A and 190B are formed on the polysilicon BSF layer (first conductive type semiconductor region) 170 and the emitter region (second conductive type semiconductor region) 120, respectively. EX1001, 10:61-11:8. First (back) and second (front) electrodes 150 and 140 respectively contact the polysilicon BSF layer (first conductive type semiconductor region) 170 and the emitter region (second conductive type semiconductor region) 120, through holes in the passivation films 190A and 190B. EX1001, 12:1-23. The electrodes may

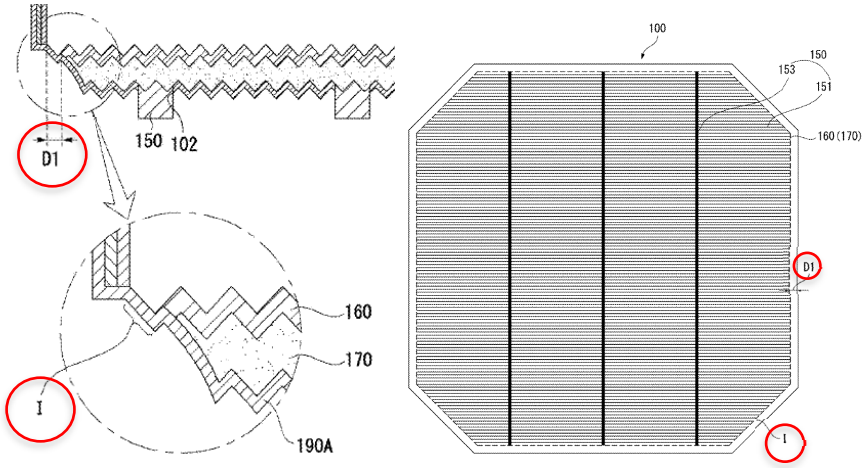
comprise smaller "finger" electrodes 151/141, and larger bus bars 153/143 that connect the finger electrodes, as shown in Figure 1. EX1001, 12:27-44.

FIG. 1



55. The solar cell also has an "isolation portion I" shown magnified in the inset of Figure 2. The "isolation portion I" is also shown as the white space along the periphery of the solar cell shown in the plan view of Figure 3. The "isolation portion I" has a width of "D1" from the outer physical boundary of the substrate 100.

FIG. 3



56. The 104 Patent explains that the tunnel layer 160 and polysilicon BSF layer (first conductive type semiconductor region) 170 "may be spaced apart from the edge of the back surface of the semiconductor substrate 100 (or the side of the semiconductor substrate 100) at a first distance D1." EX1001, 12:60-65. "That is, the isolation portion I in which the tunnel layer 160 and the first conductive type semiconductor region 170 … are not formed may be placed at the edge of the back surface of the semiconductor substrate 100." *Id.*, 13:6-12. By not forming (i.e., excluding) the tunnel layer 160 and the polysilicon BSF layer (first conductive type semiconductor region) 170 at the edge of the substrate's back surface, the "isolation portion I" blocks contact between the polysilicon BSF layer (first conductive type semiconductor region) 170 and emitter region (second conductive type semiconductor region) 120. This contact would have otherwise resulted when "impurities of the second conductive type may be diffused into the side or the edge of the back surface of the semiconductor substrate 100" during formation of the

emitter region (second conductive type semiconductor region) 120. EX1001, 13:16-35. This unwanted contact between the polysilicon BSF layer (first conductive type semiconductor region) 170 and emitter region (second conductive type semiconductor region) 120 would have resulted in unwanted short-circuit if not prevented. *Id*.

D. <u>The Prosecution History</u>

57. I have also reviewed the prosecution history of the 104 Patent to understand what the Examiner had considered during prosecution and the reasons why the claims were allowed. I recite below a summary of the prosecution history of the 104 Patent.

58. The 104 Patent was filed with 38 claims. The Examiner required restriction to (Group I) "Claims 1-25, drawn to a solar cell," or (Group II) "Claims 26-38, drawn to a method for manufacturing a solar cell." EX1005, 378. The Examiner further restricted the solar cell claims in Group I, and the Applicants elected the species "directed to a solar cell comprising an isolation portion" (application claims 1-10 and 16-18). EX1005, 380, 607.

59. Application Claim 1 of the 104 Patent initially did not contain the "isolation portion" limitations. EX1005, 56. After the election of species to the isolation portion feature and without a subsequent Office Action, the Examiner initiated an interview "propos[ing] to incorporate the claim limitations from

[application] claims 5 and 6 into claim 1 to put the application in condition for allowance," which the applicants accepted. EX1005, 607, 705.

60. The claim limitations in application claims 5 and 6 related to the "isolation portion" limitation. EX1005, 57. In the reasons for allowance, the Examiner noted that the amendments to claim 1 added the following limitations:

> *an isolation portion for preventing a contact between the first conductive type semiconductor region and the second conductive type semiconductor region*
>
> *wherein the isolation portion excludes the tunnel layer and the first conductive type semiconductor region, and is in an edge portion of the first surface of the semiconductor substrate, and*
>
> *wherein the first passivation film covers the first surface of the semiconductor substrate and the isolation portion together.*

EX1005, 702.

61. The Examiner stated that the closest prior art were Yoon (U.S. 2011/0100459) and Gortzen (U.S. 2015/0086729). According to the Examiner, Yoon did not disclose that "the isolation portion excludes the tunnel layer," and Gortzen did not disclose "an isolation portion for preventing a contact between the first conductive type semiconductor region and the second conductive type semiconductor region is in an edge portion of the first surface of the semiconductor substrate, and wherein the first passivation film covers the first surface of the semiconductor substrate and the isolation portion together." EX1005, 703. In the

claims of the 104 Patent, the claimed "first surface" is the surface with the tunnel layer, and is the back surface of the solar cell. EX1005, 701-02.

62. U.S. Patent No. 10,014,419 (the "419 Patent") was filed as a continuation of the 104 Patent with 20 method claims. The applicants authorized an Examiner's amendment to add, among other things, the following elements to claim 1 to obtain allowance:

> *a removing step of removing the tunnel layer and the first conductive type semiconductor region placed at least on the second surface of the semiconductor substrate prior to the second conductive type semiconductor region forming step after the first conductive type semiconductor region forming step:*
>
> *wherein the removing step further comprises forming an isolation portion by removing the tunnel layer on the side of the semiconductor substrate and an edge portion of the first conductive type semiconductor region, and*
>
> *wherein the first passivation film covers the first surface of the semiconductor substrate along with the isolation portion.*

EX1006, 254, 264.

63. The Examiner stated that the closest prior art were Heng (U.S. 2012/0318340) and Chang (U.S. 2014/0299187). According to the Examiner, Heng and Chang did not disclose "the claimed features of the removing step as recited and the first passivation film covering the first surface of the semiconductor substrate along with the isolation portion." EX1006, 254.

E. Claim Construction

64. For purposes of my opinions in this proceeding, I applied each claim term's ordinary and customary meaning to the Skilled Artisan read in light of the specification and prosecution history.

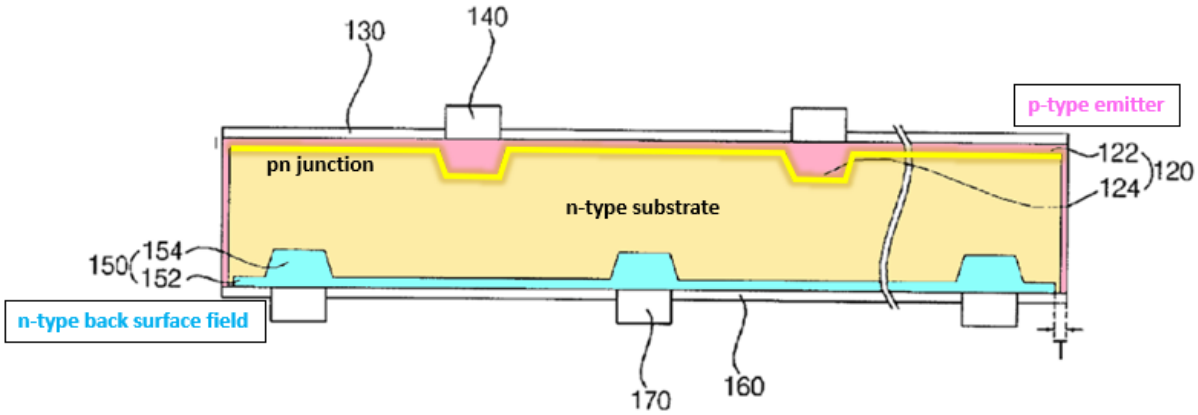
IV. BACKGROUND OF THE TECHNOLOGY

65. I understand from counsel for Runergy U.S. that Jin (EX1009), Feldmann (EX1012), Chang (EX1013), Watabe (EX1014), and Seo (EX1015) each qualifies as prior art, and I have been asked to assume them to be so.

66. A solar cell converts solar radiation (sunlight) into electricity. An individual cell, when exposed to sunlight, generates a flow of electricity to external circuits. A solar cell typically has multiple layers of silicon and other materials, including a base silicon substrate. Two variants of silicon are commonly used for the base substrate: (i) silicon, which has a monocrystalline lattice; and (ii) multicrystalline silicon, which has multiple crystalline regions that are not aligned with each other. In a standard solar cell, impurity elements, typically boron or phosphorus, are introduced into the silicon layers to alter the layers' conductive properties in a process known as "doping." EX1021-Quirk, 34-38. For example, boron has one less valence electron than silicon, and thus silicon doped with boron has an absence of electrons (i.e., "holes") compared to pure silicon, and is known as a "p-type" material or positive-type material. *Id*., 36-37. Conversely, silicon

doped with phosphorous has an excess of electrons, and is known as an "n-type" material or negative-type material. *Id.*, 36. Techniques for doping silicon and polysilicon layers were well established by 2015.

67. For a solar cell to generate electrical current, an interface between the n-type and p-type layers must be formed, which is commonly known as the "pn" junction. The layer that is oppositely doped from the substrate is known as the "emitter." For example, Figure 3 of Jin (EX1009) below shows a basic example of a solar cell including an n-type silicon substrate 110 (yellow) and a p-type silicon emitter layer 120 (pink), thereby forming a pn junction at the interface of the substrate 110 and emitter layer 120. EX1009-Jin, ¶¶29, 47. Figure 3 also shows an n-type silicon back surface field layer (teal) that has the same dopant type as the substrate. *Id.*, ¶47.



68. To form an emitter or back surface field region, dopants may be introduced into silicon via a thermal diffusion method. EX1021-Quirk, 475;

EX1022-Luque, 272-73; EX1009-Jin, ¶¶78; EX1013-Chang, ¶98; EX1012-Feldmann, §2.2. In thermal diffusion, the substrate is exposed to a dopant vapor; at a high temperature, individual dopants penetrate (i.e., diffuse) a small distance into exposed silicon and substitute for silicon atoms. *See, e.g.*, EX1021-Quirk, 478, Fig. 17.3 (reproduced below); EX1022-Luque, 272, Fig. 7.6.

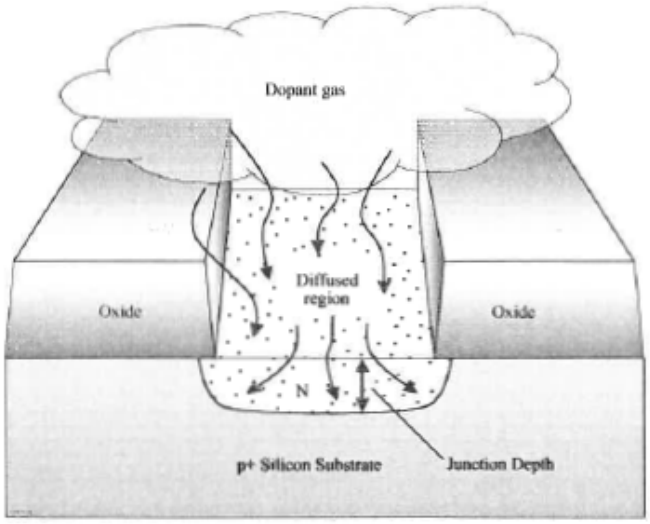
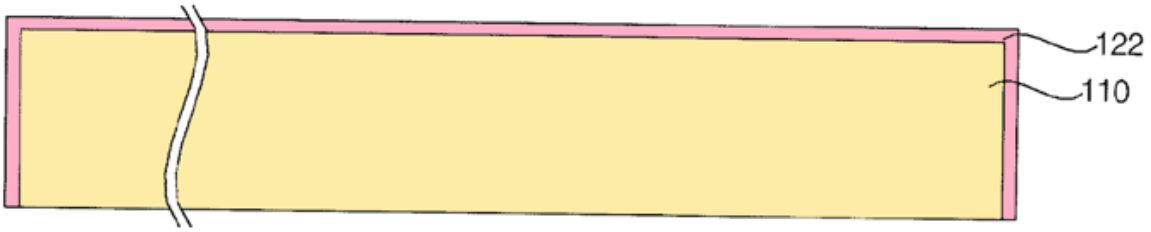


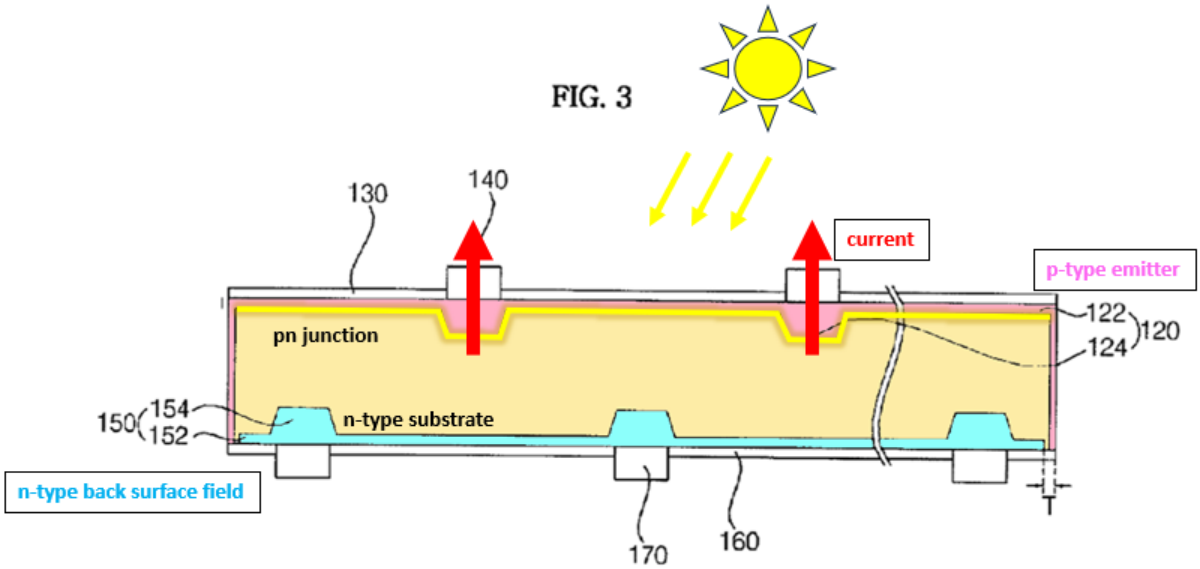
FIGURE 17.3 Doped Region in a Silicon Wafer

As a result, a flat-lying substrate exposed to dopant vapor during thermal diffusion will have dopants diffused into not only the top surface of the substrate, but also the exposed lateral side surfaces. This phenomenon is illustrated, for example, in Figure 7(b) of Jin below, in which the yellow n-type substrate 110 is diffused with p-type dopants to form the pink emitter layer 120 ("second area 122"), resulting in p-type doping along both the top and the lateral sides of the substrate. EX1009-Jin, ¶78, Fig. 7(b).



(b)

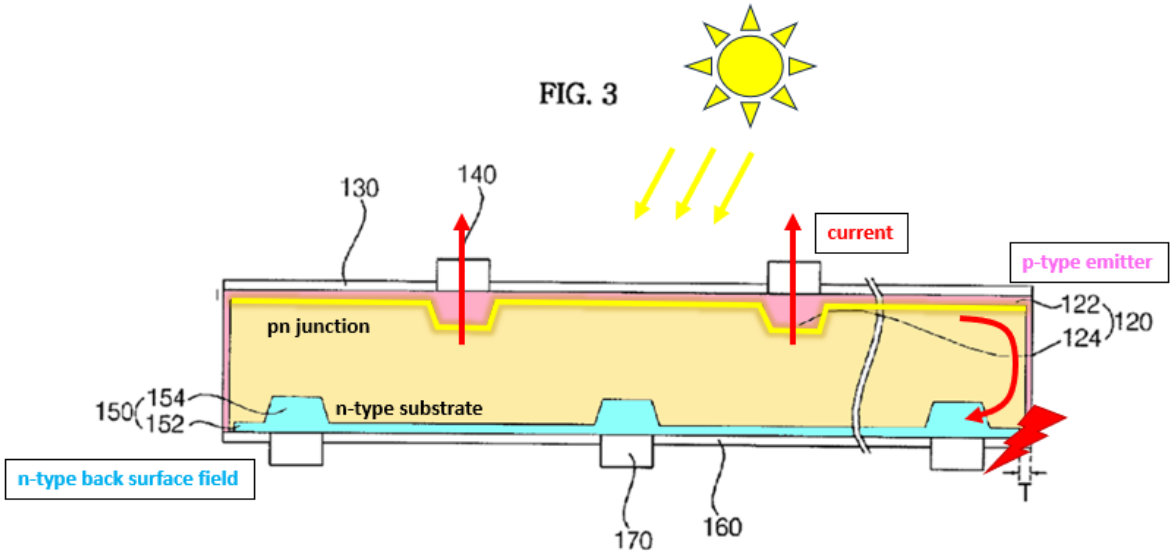
69. The difference of electrostatic potential of the p-type and n-type regions enables the solar cell to generate current. As excess electrons from the n-type region near the pn junction diffuse into the p-type region, they recombine with the holes, while excess holes from the p-type region recombine with excess electrons in the n-region, resulting in a potential difference across the pn junction. In the process, the exposed positively charged donor impurities in the n-region and negatively charged acceptor impurities in the p-region form a depletion region. The electric field from the positive donors to the negative acceptors creates the electrostatic potential difference. When solar radiation reaches the solar cell, photons with energy greater than the bandgap create free electron/hole pairs. The freed electrons and holes are mobile, and because of the potential difference across the pn junction, the electrons flow out of the n-region and the holes flow out of the p-region resulting in the flow of current.



70. Because solar cells generate electricity through creation and movement of electron-hole pairs, it was well known that maximizing the number of electrons and holes exiting a cell via electrodes improves efficiency. However, because of the dopants present on the side of the substrate, when the back surface field layer is subsequently formed on the back surface, the heavily doped p+ emitter and heavily doped n+ back surface field region may come in contact on the sides of the wafers. When this happens, the electrical pathway for the electrons and holes can become shorted between the emitter region and the back surface field along the side of the substrate, reducing the current output to the electrodes. Accordingly, the need to electrically isolate the emitter region from the back surface field was well known in the field. For example, Daniel Kray, in a paper titled "Study on the edge isolation of industrial silicon solar cells with waterjet-

guided laser, Solar Energy Materials & Solar Cells" published July 2007, recognized that the emitter diffusion wrapping around the side of the wafer substrate could result in "very low fill factors." EX1026, §1. Kray therefore discussed various techniques for edge isolation by laser scribing. *Id.* Kray also proposed to perform edge isolation on the back side of the cell to prevent damage to the front side emitter. *Id.*

71. As illustrated in Figure 3 below, Jin also recognized and solved this shorting problem by using a mask during formation of the back surface field layer 150 to leave a "gap T" between back surface field and the edge of the substrate 110, noting that if there is not enough separation, "the back surface field layer 150 and the emitter layer 120 may be shorted due to diffusion of impurities, which may be a cause for degrading the efficiency of the solar cell 100." EX1009-Jin, ¶60. Chang likewise observed that the back surface field may be formed over the entire substrate "excluding pre-designated or inevitably formed regions such as periphery region, isolation region or the like." EX1013-Chang, ¶62. Ensuring that the emitter and back surface field layers remain isolated and do not short was thus well known in the art before 2015.



72. Another known way to increase solar cell efficiency is to increase the number of electrons and holes exiting through the electrodes by preventing them from "recombining" before exiting. "Recombination" happens when an electron freed by a photon collides with (and fills) a hole before reaching an electrode, preventing both the electron and hole from contributing to the output current and reducing efficiency. One well-known mechanism of recombination is "surface recombination," whereby electrons or holes recombine at surfaces or interfaces between different materials, though other recombination mechanisms exist. In surface recombination, broken bonds at the surface of the silicon substrate or its interface with many other materials (e.g., metals) introduce defect states for recombination.

73. For years before 2015, different techniques were known to reduce surface recombination at the back surface of the solar cell and thus improve

efficiency. As one example, decades before 2015, Lindholm replaced the then-"conventional" back surface field (formed by diffusing the silicon substrate directly) with a doped polysilicon layer deposited on the substrate's back surface, which Lindholm described as "a new class of designs for high efficiency solar cells" that "show[ed] improvements" over conventional solar cells. EX1010-Lindholm, Abstract. Lindholm credited the improvements to "a decrease in effective surface recombination velocity." *Id*. Lindholm reported that, compared to the conventional BSF control cells, "the polysilicon-back solar cells show improvements in red spectral response (RSR) and open-circuit voltage." *Id*., Abstract, §I.

74. As another example, Kwark reported that "incorporating a thin, tunnelable interfacial oxide" on polysilicon layers "impedes the flow of holes" and "achieve[d] J_{oe}[2] of less than 2×10^{-14} A/cm^2, an improvement of several decades [factors of ten] over shallow diffused emitters." EX1011-Kwark, Abstract, §5. Applying both of these teachings, Feldmann disclosed a solar cell made using a "TOPCon" (tunnel oxide passivated contact) structure "based on an ultra-thin tunnel oxide (SiO2) and a phosphorus-doped silicon layer, which significantly

---

[2] J_{oe} or J_0 refers to saturation current density, which is a measure of electron/hole recombination.

reduce the surface recombination" where the electrodes contact the rear surface of the cell, and which resulted in "conversion efficiency of 23.0% for n-type cells". EX1012-Feldmann, Abstract. Following Feldmann, Chang (in addition to a peripheral isolation region) also implemented an oxide tunneling layer between a polysilicon back surface field and the substrate, such that "recombination sites on the back surface of the semiconductor substrate are thus efficiently removed." EX1013-Chang, ¶10. As a result, "carriers causing photoelectric conversion are efficiently transferred" and "efficiency of the solar cells can be further improved." *Id*.

V. DETAILED OVERVIEW OF THE PRIOR ART

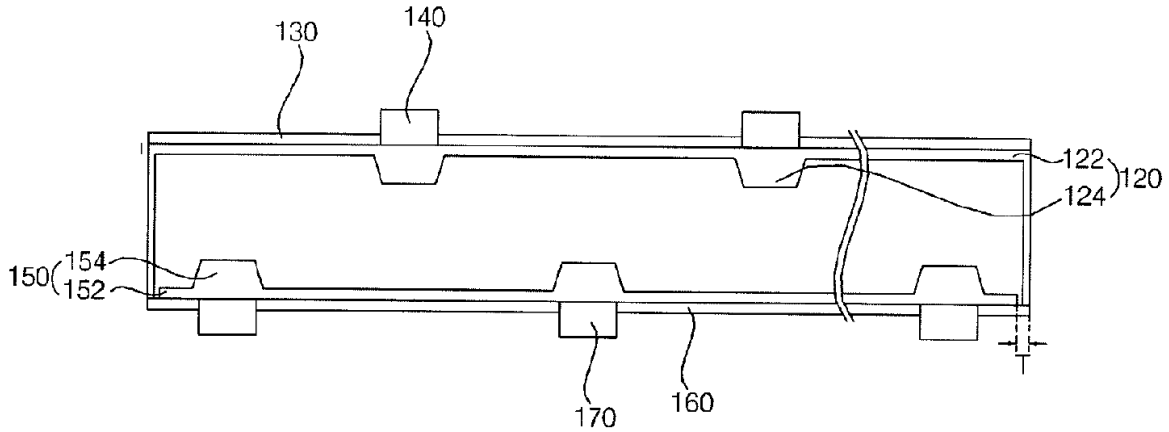
A. Jin (EX1009)

75. I understand that U.S. Patent App. Publication No. 2013/0056051 to Y. Jin, *et al*. ("Jin") was not considered by the Examiner during the 104 Patent's prosecution. Jin was published on March 7, 2013, which was before the effective filing date of 104 Patent of August 31, 2015.

76. Jin discloses a bifacial solar cell having a "silicon semiconductor substrate of a first conductive type," an emitter layer formed on the front (sun-facing) side, and a back surface field (BSF) layer formed on the opposite/back side. EX1009, Abstract, Fig. 3. The emitter layer has a different conductive type than the substrate, while the BSF layer has the same conductive type as the substrate.

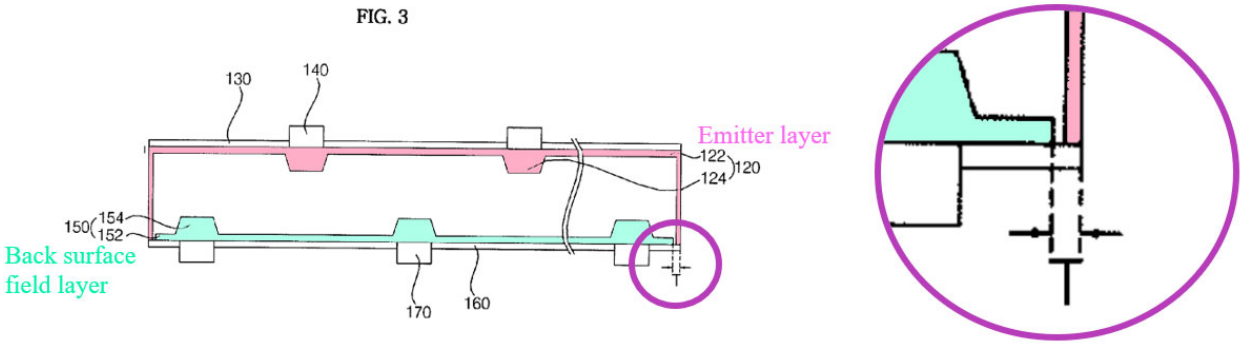
Id., Abstract. Specifically, Jin discloses that "if the substrate 110 is of an N-conductive type, for example, the back surface field layer 150 may be doped with an N-type impurity (e.g., P[hosphorus]), while the emitter layer 120 may be doped with a P-type impurity (e.g., B[oron])." *Id.*, ¶47. Both the emitter layer 120 and the BSF layer 150 can be formed in the substrate by a "heat diffusion method." *Id.*, ¶¶78, 84.

FIG. 3



77. As shown in Jin's Figure 3, the emitter layer 120 is formed not just on the front surface of the substrate; but it also extends vertically down on both lateral surfaces of the substrate. And the BSF layer 150 is formed on the back surface of the substrate but short of the edge of the substrate. Jin explained that by forming the BSF 150 "separated from the edge of the substrate 110," the BSF would be electrically isolated from the emitter layer 120, thus preventing short-circuiting of the emitter and BSF regions and degrading the solar cell efficiency. EX1009,

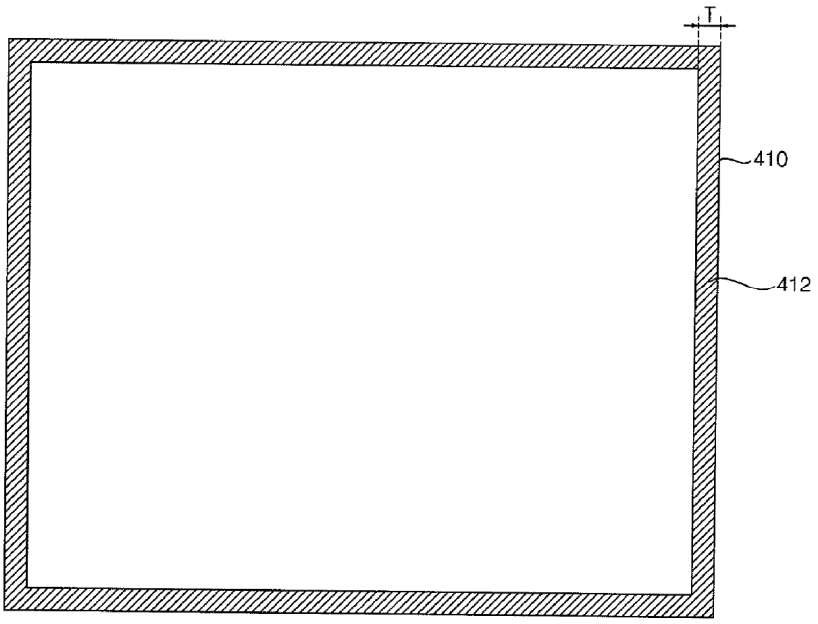
¶¶57-60, 85-86. Jin refers to this isolation gap as "gap T" or "distance T," which is seen in annotated and magnified Figure 3 below. *Id.*, ¶¶57, 85-86, 90.



78. The isolation gap T is created using a mask to shield the perimeter of the rear surface of the substrate 110 when doping to form the back surface field 150. EX1009, ¶¶83-86, Fig. 9[3]. Jin explains that by using the mask 410 with "a part 412 [as shown in Fig 9 reproduced below] to cover or overlap the edge part of the rear surface of the substrate 110, the fourth area 152 of the [BSF] layer 150 is formed." *Id.*, ¶83.

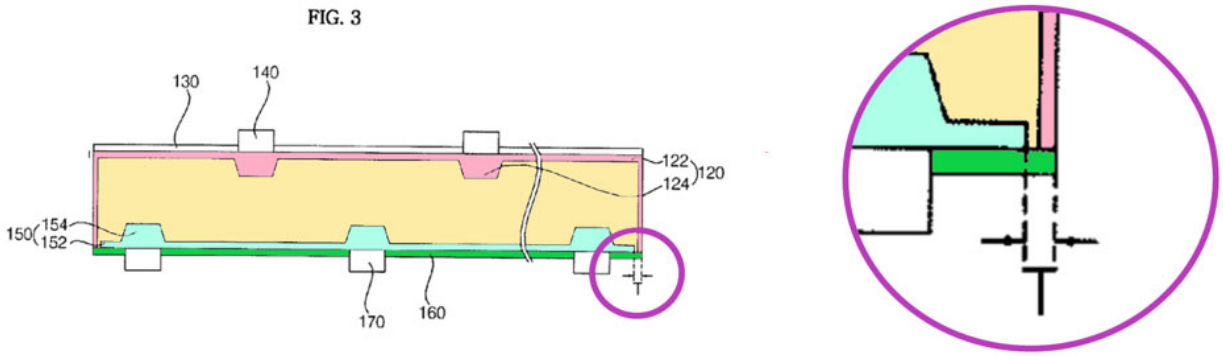
[3] The method of manufacturing the solar cell of Figs. 1-3 is disclosed with respect to Figs. 7-12. EX1009, ¶78.

FIG. 9



(a)

79. Further, on both sides of the solar cell, front and back passivation films 130 and 160 are formed on the emitter layer 120 and BSF layer 150, respectively. EX1009, ¶¶37, 50, Fig. 3. If the substrate is N-type, Jin explains that film 160 on the backside can function both as an anti-reflection film and a passivation layer. *Id.*, ¶50. As seen from Figure 3, the passivation layer 160 extends to the edge of the substrate and covers both the substrate and isolation gap "T" at the substrate's edge portion.



80. Finally, front and rear finger electrodes 140/170 connect to the emitter layer 120 and BSF 150, respectively. EX1009, ¶26, 39-40, 52-53, Figs. 1, 3. The front and rear finger electrodes are further connected together by front and rear surface bus electrodes 180/190, respectively. EX1009, ¶¶38, 54, Fig. 1.

81. The only difference between Jin and Claim 1 of the 104 Patent is the inclusion of a tunnel layer in between the substrate and the BSF layer of the solar cell. But substituting Jin's diffused BSF with a deposited polysilicon BSF layer and an interfacial oxide layer would have been obvious to the Skilled Artisan before August 31, 2015.

B. <u>Lindholm (EX1010) and Kwark (EX1011)</u>

82. In 1985, Lindholm *et al*. published a paper titled "Heavily Doped Polysilicon-Contact Solar Cells." EX1010. In this paper, Lindholm "reported the first use of a (silicon)/(heavily doped polysilicon)/(metal) structure to replace the conventional high-low junction or back-surface field (BSF) structure, of silicon

solar cells." EX1010, Abstract, §I. "Conventional" BSF refers to a BSF layer formed by diffusion of the dopants into the substrate (just like the diffused BSF layer in Jin). Conventional BSF solar cells were used as controls in Lindholm's experiments. EX1010, §II. ("Phosphorus diffusion formed a 1 -μm-thick BSF region for the n-base BSF controls.").

83. For the experimental "Polysilicon-Contact Solar Cells," Lindholm deposited polysilicon layers (which were "in situ doped" with the same dopants as the conventional BSF controls) on the surface of the substrate, instead of diffusing the dopants into the substrate. EX1010 §II. ("About 2000-A-thick layers of n+ and p+ polysilicon were deposited (in situ doped) at 670 °C in an atmospheric pressure CVD reactor.").

84. Lindholm reported that compared to the conventional BSF controls, "**the polysilicon-back solar cells show improvements** in red spectral response (RSR) and open-circuit voltage." EX1010, Abstract, §I ("**The resulting solar cells show large improvements** in red spectral response (RSR) and **moderate improvements** in open-circuit voltage V_{oc}, when compared with control cells made with the conventional back-surface-field (BSF) structure…."). This improvement over conventional BSF solar cells was understood by Lindholm to result from "a decrease in effective surface recombination velocity." EX1010,

Abstract, §III, Table 1 (showing reduced effective surface recombination velocity *S* of polysilicon "poly-Si BSF" cells compared to control conventional BSF cells).

85. Following Lindholm, in 1987, Kwark published a paper reporting on the effects of "intentionally grown chemical oxide ['chemox']," formed between the substrate and a SIPOS film or a polysilicon film, on surface recombination. EX1011, Abstract, §1.[4] Kwark compared the observed saturation currents J_{oe} of the SIPOS contacts against poly-silicon contacts without and with chemox. EX1011, §4.3. Kwark found the incorporation of the chemox showed "improved performance" of the polysilicon contacts resulting in lower recombination and that for polysilicon contacts, the interfacial oxide layer was required for this improvement. EX1011, §5. In comparison, the extra step for forming a chemox layer was not required for SIPOS to result in lower recombination because the built-in source of oxygen in SIPOS would inherently aid in the formation of the interfacial oxide layer. EX1011, §4.2. Kwark concluded that "[t]he similarity of results for <u>the chemox poly-silicon contacts</u> and SIPOS contacts suggests that <u>these</u>

---

[4] Kwark refers to the grown chemical oxide layer using the shorthand "chemox." EX1011, §4.2.2. "SIPOS" refers to "semi-insulating polysilicon" which is formed by introducing a small amount of oxygen bearing species into the chemical vapor deposition of polysilicon. EX1011, §1.

both obtain their improved performance through incorporating a thin, tunnelable interfacial oxide that impedes the flow of holes." EX1011, §5. Thus, Kwark taught that for polysilicon layers, an intentionally formed oxide layer would be necessary to achieve reduced recombination.

86. Another contemporaneous paper by the same authors, "Kwark II," also taught that addition of chemox between polysilicon and the substrate "greatly decreases the J_{oe}," which "translates into potential improvements of energy conversion efficiency for solar cells." EX1024, 742, 745; Kwark II provided data comparing polysilicon emitters with and without the oxide layer, and noted "the large difference [i.e., decrease in performance] when the interfacial oxide is missing." *Id.*, 745, Fig. 4.

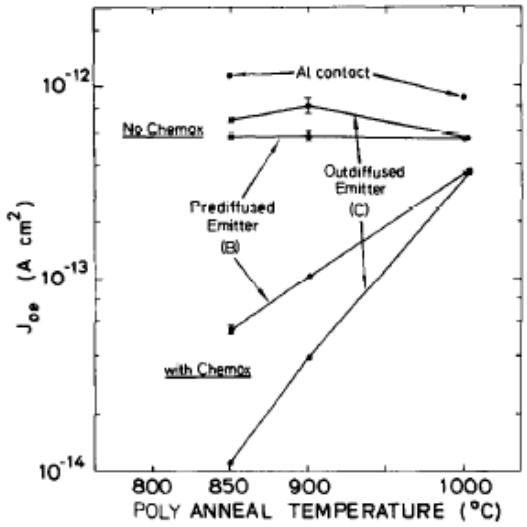


Fig. 9. Experimental J_{oe} vs anneal temperature for polysilicon contacted emitters.

C. **Feldmann (EX1012)**

87. Following Lindholm and Kwark, Feldmann *et al*. published a paper in 2013 titled "Passivated rear contacts for high-efficiency n-type Si solar cells providing high interface passivation quality and excellent characteristics," in Solar Energy Materials & Solar Cells volume 120 (2014) on pages 270-274 ("Feldmann"). EX1012. I understand that Feldmann was not considered by the Examiner during the 104 Patent's prosecution and it was published before the effective filing date of 104 Patent of August 31, 2015.

88. In this paper, Feldmann confirmed Lindholm and Kwark's findings and demonstrated that combining the polysilicon BSF layer of Lindholm with the interfacial oxide layer of Kwark would significantly improve the efficiency of the solar cell. Citing to both Lindholm's and Kwark's studies (EX1010 and EX1011), Feldmann explained that "[o]ur approach, which we have called TOPCon (Tunnel Oxide Passivated Contact) is based on these prior approaches and consists of an ultra-thin tunnel oxide and a phosphorus-doped silicon layer." EX1012, §1. In particular, Feldmann reported that "solar cells with the TOPCon structure have shown excellent performance" and that "the best cell has an independently confirmed efficiency of 23.0%." *Id*., §3. According to Feldmann, the TOPCon structure "significantly reduce[s] the surface recombination at the metal-semiconductor interface." *Id*., Abstract. Feldmann also explained that "the tunnel

oxide is a vital part of this passivated contact and that it is required to achieve excellent interface passivation." *Id*.

89. Feldmann's TOPCon solar cell is depicted in Figure 3, below. The solar cell comprises an n-type (n-base) substrate with a "p^+-emitter" ("boron-diffused emitter") (green), a passivation film (yellow), and an anti-reflection coating (blue) on the front sun-facing side of the substrate. EX1012-Feldmann, Fig. 3, §2.1. On the backside of the substrate is the TOPCon structure consisting of the ultra-thin tunnel oxide (SiO_2) (light blue) and the phosphorus-doped polysilicon layer (red).[5] *Id*. (Coloring in original).

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[5] Although Feldmann does not expressly call its "phosphorus-doped silicon layer" a polysilicon layer, the Skilled Artisan would understand that it was in fact a polysilicon layer because the silicon layer was annealed (i.e., heated) to between 600-1000 °C. This annealing step crystallizes the initially amorphous silicon to polysilicon. EX1012-Feldmann, §2 ("Subsequently, a 20 nm thick phosphorus-doped Si layer was deposited on both sides. Afterwards, the samples' passivation was activated in a tube furnace process with plateau temperatures in the range of 600 °C < T_{anneal} < 1000 °C."). EX1021-Quirk, 499-501; EX1030-Streetman, 159-61.

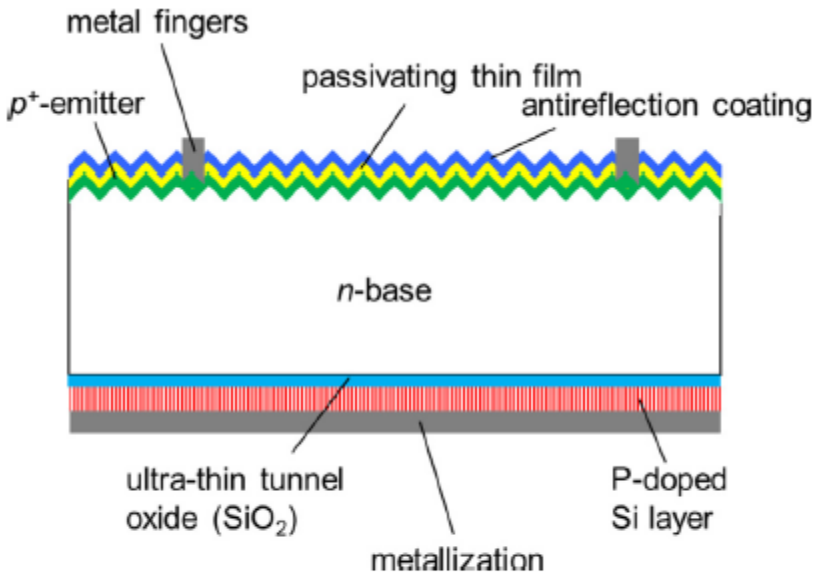


Fig. 3. Schematic of the solar cell structure with the passivated rear contact. The solar cells feature a diffused boron-doped emitter at the front side which is passivated by atomic layer deposited (ALD) aluminum oxide Al_2O_3 and a plasma-enhanced chemical vapor deposited (PECVD) silicon nitride SiN_x.

90. Applying Feldmann's teaching and replacing the TOPCon structure for the diffused BSF layer in Jin would result in a solar cell that meets all of the limitations of Claim 1 of the 104 Patent and most of the dependent claims.

D. <u>Chang (EX1013)</u>

91. Following Feldmann's publication, U.S. Patent App. Publication No. 2014/0299187 to J. Chang, *et al.* ("<u>Chang</u>") further demonstrates the obviousness of the 104 Patent claims. Chang was filed on April 2, 2014, and published on October 9, 2014, which was before the effective filing date of the 104 Patent, August 31, 2015.

92. Chang disclosed a bifacial solar cell having a frontside emitter layer 20, a backside polysilicon BSF layer 30, and a tunnel oxide layer 44 in between the

substrate 10 and the backside polysilicon BSF layer 30, as depicted in Figures 1 and 8. EX1013, ¶¶36, 61, Figs. 1, 8. Figures 1 and 8 are alternative embodiments that differ only in the frontside layers. The backside layers of both Figures 1 and 8 are the same. *Id.*, ¶101.

FIG. 1

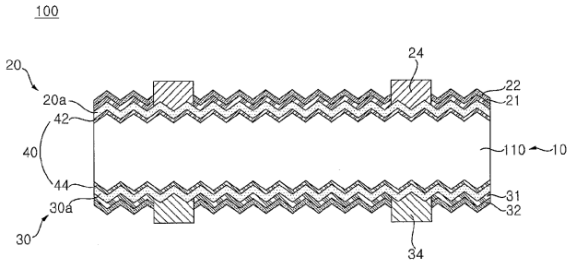


FIG. 8

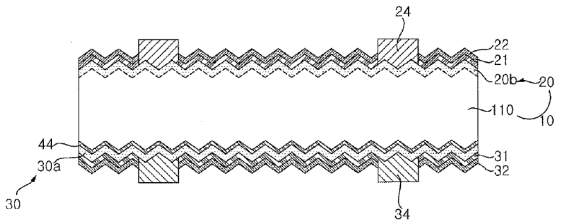


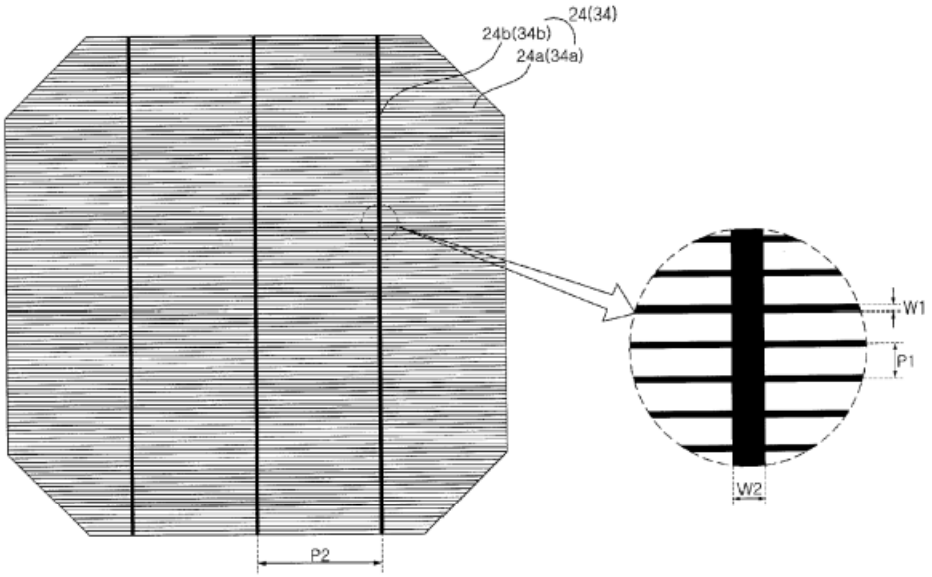
Figure 8 is akin to a solar cell resulting from the combination of Jin and Feldmann that replaces the diffused BSF of Jin with a TOPCon structure, as taught by Feldmann. Figure 1 extends Feldmann's approach to likewise include a tunnel oxide 42 and polysilicon layer 20 on the front side to form the emitter region 20. *Id.*, ¶¶36, 45.

93. Regardless, with respect to the backside structure consisting of the tunnel oxide layer 44 and polysilicon BSF layer 30, Chang taught an embodiment where these two layers are not formed all the way to the edge of the substrate, and thus forming an "isolation region" at the periphery of the backside surface. EX1013, ¶¶36, 56, 62.

94. Chang's solar cell includes a monocrystalline silicon substrate 10 with a base area 110 doped with an n-type dopant such as phosphorous. EX1013, ¶¶38-40. A p-type emitter area 20 on the front surface of the substrate 10 forms a pn junction with the base area 110. *Id.*, ¶¶36, 40. A tunnel oxide layer (second tunneling layer 44) is formed over the entire area of the back surface of the substrate 10 except in an isolation region at the periphery of the substrate. *Id.*, ¶¶36, 56, 60. An n-type polysilicon (polycrystalline) back surface field area 30 is formed over the second tunneling layer 44, again except in an isolation region at the periphery of the substrate 10. *Id.*, ¶¶36, 61-62. Thus, in Chang, at the periphery of the back surface, the tunnel oxide layer and back surface field are excluded at the isolation region. Moreover, a first passivation film 21 on the front side of the substrate passivates defects in the emitter area 20, and a second passivation film 31 on the back side of the substrate passivates defects in the back surface field area 30. *Id.*, ¶¶36, 51-53, 63-65.

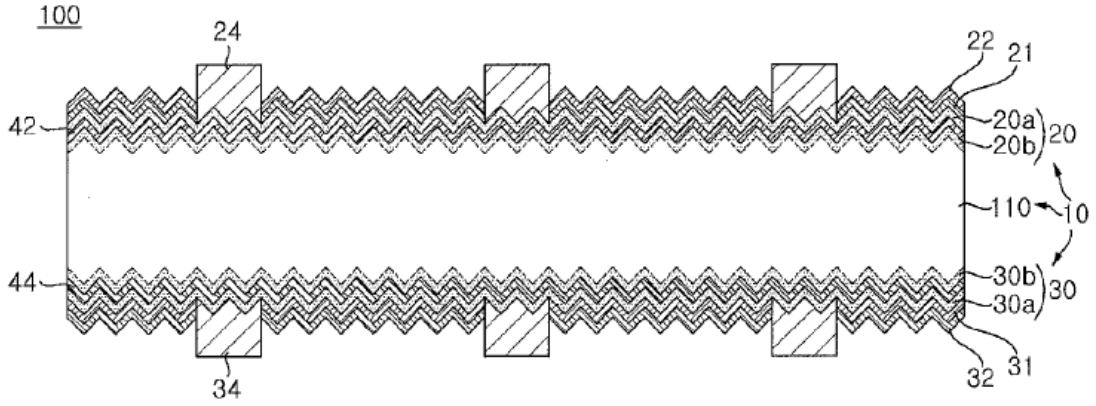
95. First and second electrodes 24/34 connect to the emitter area 20 and the back surface field area 30, respectively, through openings in the passivation films 21/31. EX1013, ¶¶36, 55, 67. The first and second electrodes 24/34 each include parallel finger electrodes 24a/34a connected together by bus bar electrodes 24b/34b. *Id.*, ¶69, Fig. 2.

FIG. 2



96. Chang discloses a number of different configurations of the backside polysilicon BSF layer 30 and tunnel oxide layer 44. For example, in Fig. 1, the BSF layer 30 is described as "include[ing] a first portion 30a formed on the second tunneling layer 44." EX1013, ¶61. In Fig. 11, Chang discloses that the tunnel oxide layer 44 is interposed between two conductive layers 30a and 30b. *Id.*, ¶125. Starting from the back surface of the substrate, the "second portion 30b" of the BSF 30 is formed by diffusing dopants into the back surface of the substrate 10 and "may be 5 nm to 100 nm" in thickness. *Id.*, ¶¶128, 130, 136.

FIG. 11



The tunnel oxide 44 is then formed on the "second portion 30b." On the tunnel oxide 44 is then formed the "first portion 30a" of the BSF 30, the first portion being made of polysilicon (polycrystalline silicon). *Id.*, ¶¶61, 125. Chang discloses that "the thickness of the [polysilicon] first portion 30a may be 50 nm to 500 nm." *Id.*, ¶136. Chang further explains that the "first portion 30a" in Fig. 11 is the same as the "first portion 30a" described with respect to Fig. 1, i.e., it can be made of deposited polysilicon. EX1013, ¶¶61, 127. Thus Chang discloses that the polysilicon portion of the BSF 30 that is formed over the tunnel oxide 44 of Figs. 1, 8, and 11, i.e., "first portion 30a," can be up to 500 nm thick.

E. <u>Watabe (EX1014)</u>

97. Japanese Patent Publication No. JP 2010186862A to inventor Watabe, et al., was filed on February 12, 2009 and published on August 26, 2010 before the effective filing date of the 104 Patent of August 31, 2015. EX1014, face. I

understand that Watabe was submitted in an IDS filed January 9, 2017 during prosecution of the 104 Patent. EX1005, 386.

98. Watabe discloses that the finger and bus bar electrodes of a solar cell are commonly made by screen printing and firing silver paste to bond the paste to the substrate of the solar cell. EX1014, ¶2. Because the power output of each solar cell is small, multiple solar cells are connected together by soldering wires to the bus bar electrodes. *Id.*, ¶4. Copper, a metal with high electrical conductivity, is "very inexpensive compared to silver," but it has "poor solder wettability compared to that of silver." *Id.*, ¶¶3-4. Connecting solar cells together by soldering to copper bus bar electrodes increases the risk of a degraded solder connection, compromising reliability. *Id.*, ¶4.

99. Watabe discloses forming the finger electrodes by screen printing and firing a conductive paste containing copper (or a copper compound), such that the copper is bonded directly to the solar cell substrate. *Id.*, ¶¶9-10, 16. Watabe explains that since the finger electrodes are typically not used in the connections between solar cells, the fingers can be made with copper "for cost reduction while maintaining internal resistance compared to silver paste." *Id.*, ¶4, 9-10.

100. The bus bar electrodes, however, are used to connect between solar cells. *Id.*, ¶4. Recognizing that copper does not solder well to the coupling wires, Watabe discloses that "at least the bus-bar electrode has a multilayer structure with

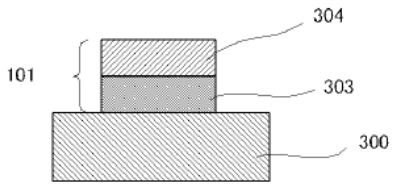
two or more layers." *Id.*, ¶¶4, 12. Specifically, Watabe discloses that the first electrode layer of the bus bar electrode that is "directly bonded to the semiconductor substrate is composed of a conductive paste containing copper or copper compound fine particles." *Id.*, ¶¶13, 17. Then, "the uppermost electrode layer that is bonded to the wiring is formed using a paste containing a substance other than copper such as silver, [such that] the bonding strength to the wiring is maintained without compromising solar cell performance." *Id*.

101. Watabe discloses that the finger and bus bar structure is formed "on at least one side of the semiconductor substrate" and discloses an example in which the electrodes are formed on the "light-receiving surface." *Id.*, ¶¶9-10, 28. Bifacial solar cells like that of Jin and Chang can receive light on both the front and back sides of the solar cell. Thus, the Skilled Artisan would understand that by using the "at least one side" language, Watabe contemplated that the structure could be used on both sides of the substrate. The Skilled Artisan would further understand that when the electrode structure of Watabe is used in the bifacial Jin/Feldmann and Chang/Jin solar cells, such electrode structure would be used on both the front sun-facing side and the rear side of the substrate.

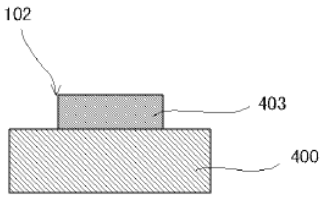
102. Watabe discloses various embodiments of the finger electrodes and bus electrodes in Figs. 2-6. Specifically, with respect to Fig. 3, Watabe discloses that the bus bar electrode can be a dual layer structure with copper 303 adhering to

the substrate 300 and silver on the outermost layer 304 to increase "the reliability of the bonding strength to wiring by soldering." *Id.* ¶28. In Fig. 4, Watabe discloses that the finger electrode can be a single layer structure of copper 403. *Id.*

【図 3】



【図 4】

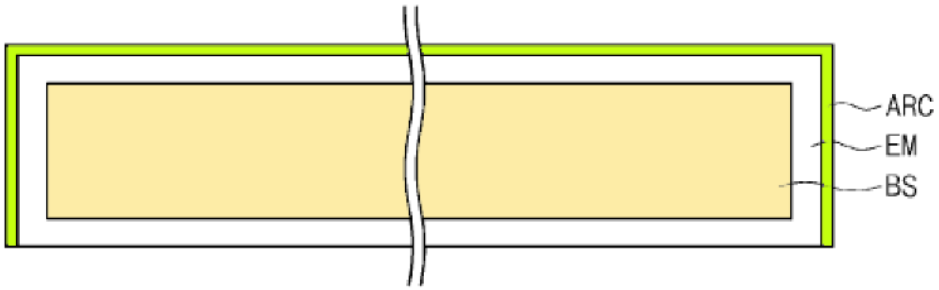


F. <u>Seo (EX1015)</u>

103. U.S. Patent No. 8,647,914 to Seo ("Seo") issued on February 11, 2014, which was before the effective filing date of the 104 Patent of August 31, 2015. EX1015, face. I understand that Seo was not considered by the Examiner during the 104 Patent's prosecution.

104. Seo teaches a solar cell with a base substrate BS, an emitter layer EM on its front surface, and a back surface field on its rear surface. EX1015, 3:44-50, 4:11-13, 5:32-35, Fig. 1. As shown in Figure 2C of Seo, after the emitter EM is formed, an "anti-reflection layer ARC is formed directly on the emitter layer EM" using chemical vapor deposition, resulting in the anti-reflection layer ARC being deposited on both the front and lateral sides of the substrate BS. *Id.*, 6:39-48.

Fig. 2C



After etching/removing the EM layer on the backside (FIG. 2E), a backside "passivation layer PSV may be formed by depositing at least two of… silicon oxide (SiO_x), silicon nitride (SiN_x), and silicon oxynitride (SiON)," resulting in the passivation layer PSV being deposited on both the back and lateral sides of the substrate BS and on top of the anti-reflection layer ARC as shown in Figure 2F. *Id.*, 7:60-66. Seo observes that the passivation layer PSV is "in a region corresponding to the edge region EDG and on the side surfaces of the base substrate BS." *Id.*, 4:60-63.

Fig. 2E

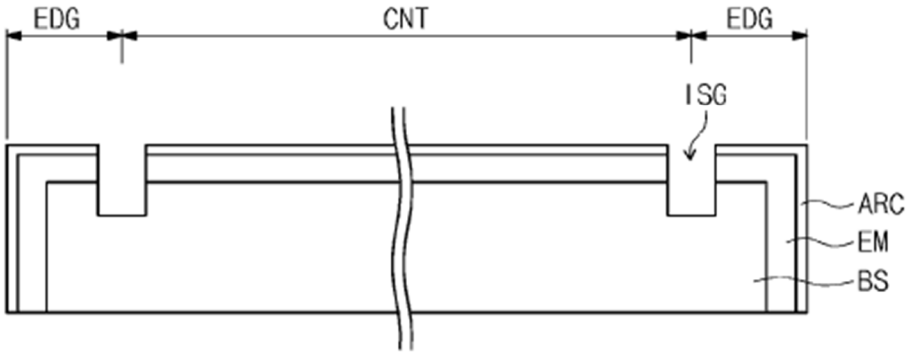
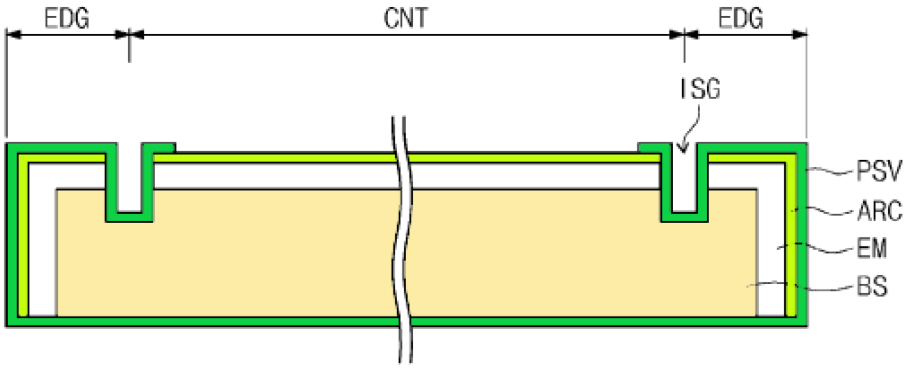


Fig. 2F

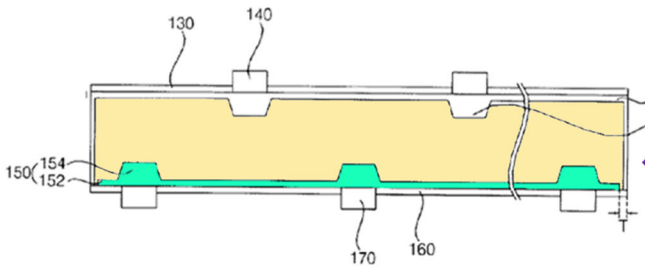


VI. CLAIMS 1-6 AND 9-10 ARE UNPATENTABLE AS OBVIOUS OVER JIN AND FELDMANN

105. In my opinion, the combination of Jin and Feldmann would have rendered Claims 1-6 and 9-10 obvious and unpatentable. The combination would have been nothing more than substituting the diffused BSF layer 150 (green) of Jin with the phosphorous-doped polysilicon layer (red) of Feldmann along with the beneficial tunnel oxide layer (blue) on the backside of the substrate of Jin's solar cell. EX1009-Jin, ¶41; EX1012-Feldmann, Fig. 3, §2.1. The resulting solar cell would meet all limitations of *e.g.*, Claim 1, as illustrated below using a modified Jin Figure 3.

Jin

FIG. 3



Feldmann

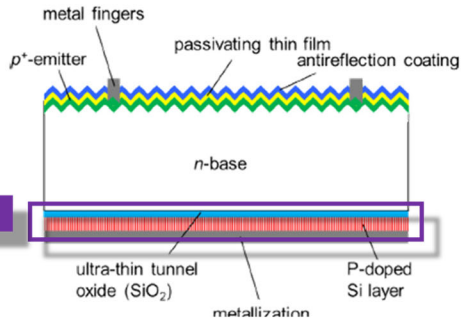
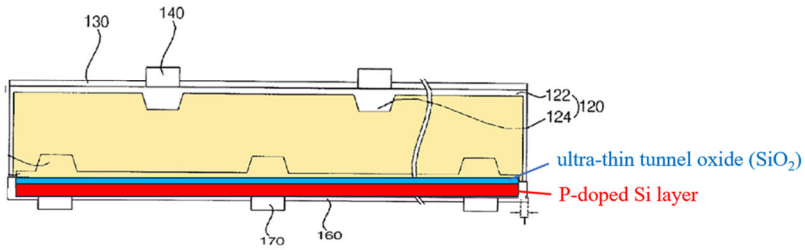


FIG. 3



Proposed Combination

A. Motivation to Modify Jin with Feldmann

106. Jin and Feldmann are analogous art because each is in the same field of endeavor—solar cell design. EX1009-Jin, Abstract, ¶¶3,7; EX1012-Feldmann, Abstract, 271. Each is reasonably pertinent to the problems of efficiencies of solar cell designs. EX1009-Jin, Abstract, ¶¶6-7; EX1012-Feldmann, Abstract, 271.

107. The Skilled Artisan would have been motivated to replace Jin's BSF layer 150 with a tunnel oxide layer and polysilicon layer because Feldmann and others taught that making this substitution would reduce surface recombination and improve solar cell efficiency.

108. First, it was known and suggested for decades that heavily-doped polysilicon, like that disclosed in Feldmann, could be used to replace a BSF layer, like that used by Jin. In 1985, Lindholm proposed "the first use of a (silicon)/(heavily doped polysilicon)/(metal) structure to replace the conventional high-low junction or back-surface field (BSF) structure, of silicon solar cells." EX1010-Lindholm, Abstract, §I. Lindholm reported that "**[c]ompared with BSF** and back-ohmic-contact (BOC) control samples, **the polysilicon-back solar cells show improvements** in red spectral response (RSR) and open-circuit voltage." *Id.*, Abstract, §I ("**The resulting solar cells show** **large improvements** in red spectral response (RSR) and **moderate improvements** in open-circuit voltage V_{oc}, when compared with control cells made with the conventional back-surface-field (BSF) structure…."). This improvement over conventional back-surface field solar cells was understood by Lindholm to result from "a decrease in effective surface recombination velocity." *Id.*, Abstract, §III, Table 1. The Skilled Artisan would thus have been motivated to specifically replace Jin's BSF 150 with a polysilicon BSF layer, as encouraged by Lindholm, to reduce surface recombination.

109. In addition, it had also been known for decades that an interfacial oxide layer in between the polysilicon and the substrate could be used to improve solar cells. A 1987 article by Kwark investigated "[e]mitters both with and without an intentionally grown chemical oxide ['chemox'] under the SIPOS [Semi-

Insulating Poly-crystalline Silicon] or poly-silicon film." EX1011-Kwark, Abstract, §1.[6] Kwark concluded an intentionally formed interfacial oxide ("chemox") layer was required for polysilicon contacts to result in lower recombination, while for SIPOS, such oxide layer would inherently formed. Kwark taught that "[t]he similarity of results [i.e., lower recombination] for **the chemox poly-silicon contacts** and SIPOS contacts suggests that **these both obtain their improved performance through incorporating a thin, tunnelable interfacial oxide** that impedes the flow of holes." *Id.*, §5. Another contemporaneous paper by the same authors also taught that addition of chemox between polysilicon and the substrate "greatly decreases the J_{oe}," which "translates into potential improvements of energy conversion efficiency for solar cells." EX1024-Kwark II, 742, 745. Kwark II provided data comparing polysilicon emitters with and without the oxide layer, and noted "the large difference [i.e., decrease in performance] when the interfacial oxide is missing." *Id.*, 745, Fig. 4. A Skilled Artisan would thus have been further motivated to incorporate a tunnel oxide (SiO_2) with a polysilicon layer to further reduce recombination, as encouraged by Kwark and Kwark II.

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[6] Kwark refers to the grown chemical oxide layer using the shorthand "chemox." EX1011, §4.2.2.

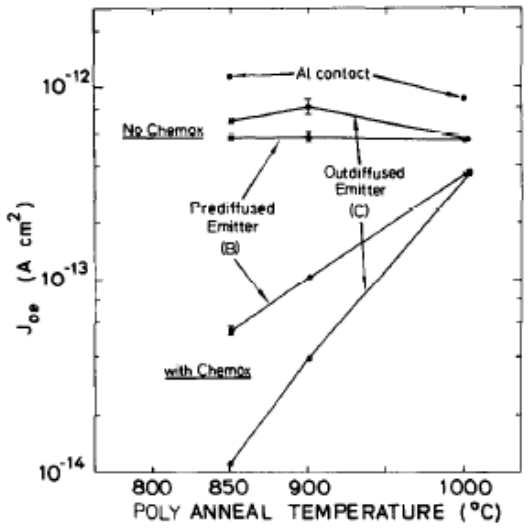


Fig. 9. Experimental J_{oe} vs anneal temperature for polysilicon contacted emitters.

110. Feldmann's 2013 paper confirmed Lindholm and Kwark's teachings by demonstrating that combining the polysilicon BSF layer of Lindholm and the interfacial oxide layer of Kwark would significantly improve the efficiency of the solar cell. Citing to both Lindholm's and Kwark's studies (EX1010 and EX1011), Feldmann explained that "[o]ur approach, which we have called TOPCon (Tunnel Oxide Passivated Contact) is based on these prior approaches." EX1012-Feldmann, §1. Consistent with Lindholm and Kwark's observations, Feldmann also reported that the TOPCon structure "significantly reduce[s] the surface recombination at the metal–semiconductor interface," making the tunnel oxide "a vital part of this passivated contact and that it is required to achieve excellent interface passivation." *Id.*, Abstract. Further, the conversion efficiency of

Feldmann's TOPCon solar cells reached "23.0% for n-type cells." *Id.*, Abstract, §3.

111. A Skilled Artisan reviewing Feldmann alone or including the teachings of Lindholm and Kwark would thus have been motivated to replace the diffused back surface field of Jin with a heavily doped polysilicon BSF along with a thin tunnel oxide between the substrate and polysilicon layer, as taught by these references to reduce surface recombination and improve solar cell efficiency.

112. Jin's solar cell is bifacial and can absorb sunlight from both the front and back surfaces. EX1009-Jin, ¶42. Feldmann's solar cell is monofacial and only absorbs sunlight from the front its front surface. EX1012-Feldmann, §2.2 ("the rear is fully metalized"). The Skilled Artisan, however, would not have been dissuaded from modifying Jin's back surface field layer 150 with Feldmann's TOPCon structure because, as discussed above, Feldmann, Lindholm, and Kwark all taught that adding the tunnel oxide layer between the substrate and BSF would increase efficiency by reducing recombination.

113. Jin discloses that the emitter 120 is formed by doping the substrate 110 using a heat diffusion method, resulting in the emitter 120 covering the top and side surfaces of the substrate. EX1009-Jin, ¶78, Fig. 3. Because the emitter extends down the sides of the substrate, Jin discloses that the back surface field layer 150 is formed "separated from the edge of the substrate 110" to prevent

shorting with the emitter 120. *Id.*, ¶58. Feldmann's emitter is likewise formed by diffusion. EX1012-Feldmann, §1 ("diffused boron-doped emitter on the front side.). Thus Feldmann's solar cell, like Jin's, is susceptible to shorting between the emitter and back surface field. Therefore, the modified Jin/Feldmann solar cell would benefit from Jin's gap-T isolation region to prevent shorting. In addition, the Skilled Artisan would have been motivated to have both the polysilicon layer and the tunnel oxide layer be separated from the edge of the substrate with Jin's gap-T isolation region. If the tunnel oxide layer were to extend to the edge, the exposed portions of the oxide could trap impurities and create negative fixed oxide charges, which could then create a p-type inversion in the n-type base substrate, leading to a leakage path to the p-type emitter on the front of the solar cell. And, as discussed in §V.D above, following Feldmann, Chang disclosed a bifacial solar cell with Feldmann's TOPCon structure and Jin's isolation region, in which both the polysilicon layer and the tunnel oxide layer are separated from the edge of the substrate by an isolation region.

114. In the combination, Jin's modified isolated solar cell would continue to function as before, but with the expected additional improvement provided by the phosphorous-doped polysilicon BSF layer and ultra-thin tunnel oxide taught by Feldmann. Replacing the phosphorus-diffused back surface field of Jin with a tunnel oxide and phosphorous-doped deposited polysilicon, as taught by Feldmann,

merely substitutes one element for another already known in the field, yielding a predictable result. *See also*, *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

B. <u>Reasonable Expectation of Success</u>

115. The Skilled Artisan would have considered the Jin/Feldmann combination to be merely an arrangement of old elements (and their corresponding fabrication steps) with each performing the same function it had been known to perform (the back surface field 150 of Jin, acting to reduce electron-hole recombination and isolated by a gap T along the edges, replaced with an ultra-thin tunnel oxide layer of SiO_2 and a layer of phosphorus-doped polysilicon, similarly reducing recombination and isolated by Jin's gap T) and yielding no more than what one would expect from such an arrangement (a solar cell with improved performance). The Skilled Artisan would have been aware of numerous routine techniques for making the Jin/Feldmann solar cell, all of which would have been well within the level of ordinary skill in the art.

116. As a first example, Jin discloses a mask in Figure 9 that would be used to cover the periphery or edge portion of the back surface of the substrate. Such masking technique, known as shadow masking was well known to the Skilled Artisan. The Skilled Artisan would know, for example, that reusable metal "shadow masks" have been used in the masking and forming of layers in solar

cells. For example, Scherff discloses a reusable metal mask used for structuring the emitter and back surface field regions of an interdigitated back contact solar cell. EX1031-Scherff, Abstract. Scherff discloses that various layers can be deposited and plasma etched through openings in the mask. *Id.*, §2.

117. The metal shadow mask, in a shape or form as shown in Fig. 9 of Jin, would be placed on the substrate to cover the periphery of the surface of the substrate before depositing the tunnel oxide layer and phosphorous-doped polysilicon layer. The Skilled Artisan would be aware that deposition techniques such as plasma enhanced chemical vapor deposition (PECVD) or atomic layer deposition (ALD) could be used to deposit the tunnel oxide and the polysilicon layer in the area not covered by the metal mask. EX1031-Scherff §2.1. For example, Chang discloses that the tunneling layer may be formed "by a method such as thermal growth or deposition (for example, plasma-enhanced chemical vapor deposition chemical (PECVD), atomic layer deposition (ALD) or the like" and that the conductive type areas "may be formed of an amorphous, microcrystalline, or polycrystalline semiconductor" and may be formed by "deposition (for example, plasma enhanced chemical vapor deposition chemical (PECVD)) or the like."). EX1013-Chang ¶146. Since the metal mask is not chemically bonded to the wafer, it could simply be lifted off the substrate after formation of the oxide and polysilicon layers. And the oxide and polysilicon

layers would not have been formed (and thus excluded) in the area covered by the mask, i.e., the Gap-T isolation region.

118. As a second example, when forming the back surface field, the Skilled Artisan would use a silicon nitride mask around the periphery of the substrate. In this example, the Skilled Artisan would first deposit a silicon nitride (SiNx) layer on the entire back of the substrate and use the mask shown in Fig. 9 of Jin to protect the silicon nitride along the periphery of the back of the substrate while etching out the center portion of the silicon nitride layer. Etching of the silicon nitride would be performed using, for example, a dry etch. The remaining silicon nitride would form a mask over the periphery of the back of the substrate. The Skilled Artisan would then use Feldmann's step of growing an ultra-thin wet chemical oxide layer in the center portion of the substrate not covered by the silicon nitride mask, followed by deposition of the phosphorus-doped polysilicon layer over the entire substrate including the silicon nitride mask. EX1012-Feldmann §2.1. Afterwards, to form Jin's gap-T isolation region, the Skilled Artisan would use a chemical wet etch to etch out the silicon nitride mask and then mechanically remove the portion of the polysilicon that was deposited over the silicon nitride mask. Thus, the oxide layer and polysilicon layer would have been excluded in the gap-T isolation region.

119. As a third example, instead of using the silicon nitride mask for both the tunnel oxide and polysilicon layer, after growth of the chemical oxide layer in the second example above, the silicon nitride mask could have been removed by selective etching before the deposition of the polysilicon layer. A metal shadow mask as described above, could have been placed over the substrate and the Skilled Artisan could have deposited Feldmann's phosphorous-doped polysilicon layer on top of the tunnel oxide using, for example, plasma enhanced chemical vapor deposition (PECVD) through the opening in the metal mask. The metal mask could have been lifted off after polysilicon deposition, instead of wet chemical etching and mechanical removing of the polysilicon at the edge portion, leaving the oxide and polysilicon layers only in the areas not covered by the masks.

120. As a fourth example, and another alternative to using the silicon nitride mask for both the tunnel oxide and polysilicon layers, the Skilled Artisan could have chosen to remove the silicon nitride mask after growing the chemical oxide layer. The phosphorus-doped polysilicon layer could have been deposited over the entire back side of the substrate. A mask, such as the reverse of the mask shown in Fig. 9 of Jin, could have been used to protect the polysilicon over the tunnel oxide while the remaining polysilicon in the edge portion or the periphery of the back of the substrate was removed by using a wet etch or a plasma etch.

121. As a fifth example, the Skilled Artisan would form the tunnel oxide, for example by using Feldmann's step of growing an ultra-thin wet chemical oxide layer over the entire back side of the substrate followed by deposition of the phosphorus-doped polysilicon layer. EX1012-Feldmann §2.1. The Skilled Artisan would then use a mask, such as the reverse of the mask shown in Fig. 9 of Jin (i.e., a mask smaller than the substrate) to protect the polysilicon over the tunnel oxide in the center. The remaining polysilicon and tunnel oxide in the edge portion or the periphery of the back of the substrate would then be removed using an etch, such as a wet etch.

122. In short, there are many ways known to the Skilled Artisan to form the isolation region gap-T in the combined Jin/Feldmann solar cell. And after the formation of Feldmann's TOPCon structure, the Skilled Artisan would continue with Jin's steps of forming the front and backside passivation/anti-reflection layers and the metal electrodes.

123. Combining Jin/Feldmann as described here would have been well within the level of ordinary skill in the art. It would not have resulted in any unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success. The combination would simply have been the combination of well-known prior art steps in solar cell and semiconductor fabrication to yield predictable results. Likewise, substituting

Jin's diffused back surface field with an ultra-thin oxide layer and in-situ doped polysilicon layer would have been a simple substitution of one known element and corresponding fabrication steps for another to obtain predictable results, as taught by Feldmann, Lindholm, and Kwark. EX1012-Feldmann, Abstract; EX1010-Lindholm, Abstract; EX1011-Kwark, §4.3. It would have further constituted use of a known technique (growing an oxide layer and depositing doped polysilicon) to improve similar devices (Jin's solar cell) in the same way. It is nothing more than applying a known technique to a known device ready for improvement to yield predictable results. *Id*.

C. <u>Jin and Feldmann Disclosed All Claimed Limitations</u>

1. Claim 1

a) [1.a] Preamble

124. Jin and Feldmann both disclose "*a solar cell,*" as shown by the remaining elements. EX1009-Jin, Abstract, ¶3, Figs. 1, 3; EX1012-Feldmann, Abstract, §1, Fig. 3.

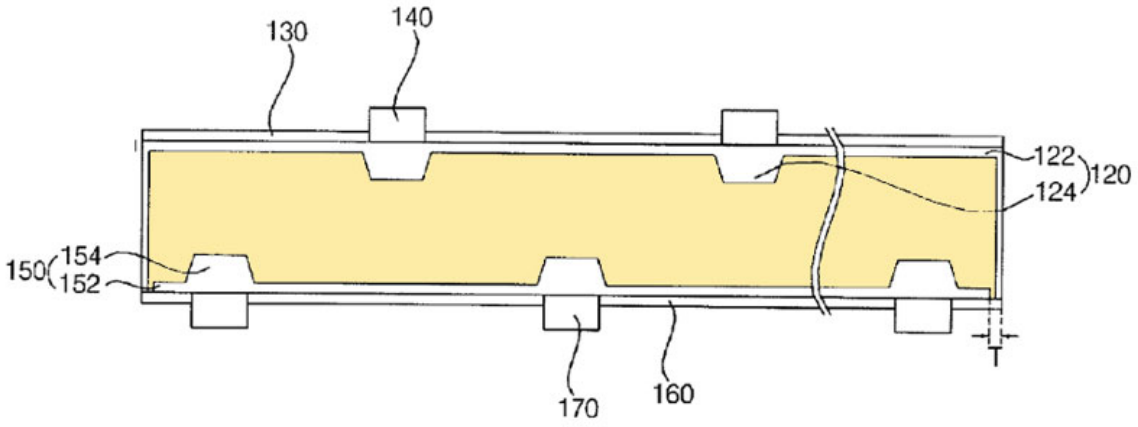
b) [1.b] Semiconductor Substrate

125. Claim 1 first recites: "*a semiconductor substrate*." Both Jin and Feldmann disclose this element.

126. Jin discloses that its solar cell 100, as shown in Figure 3, has a "silicon semiconductor substrate 110 [yellow] of a first conductive type."

EX1009-Jin, ¶26, Fig. 3[7]. In the particular combination asserted here, substrate 110 is doped with phosphorous (P) "and [is] implemented as an N-type" semiconductor. EX1009-Jin, ¶¶26-27.

FIG. 3



127. Feldmann likewise discloses a solar cell using an "n-type" silicon wafer, which is a silicon semiconductor substrate. EX1012-Feldmann, 271.

c) [1.c] Tunnel Layer

128. Claim 1 next recites: "*a tunnel layer on a first surface of the semiconductor substrate.*" In the claims of the 104 Patent, the "first" surface is the

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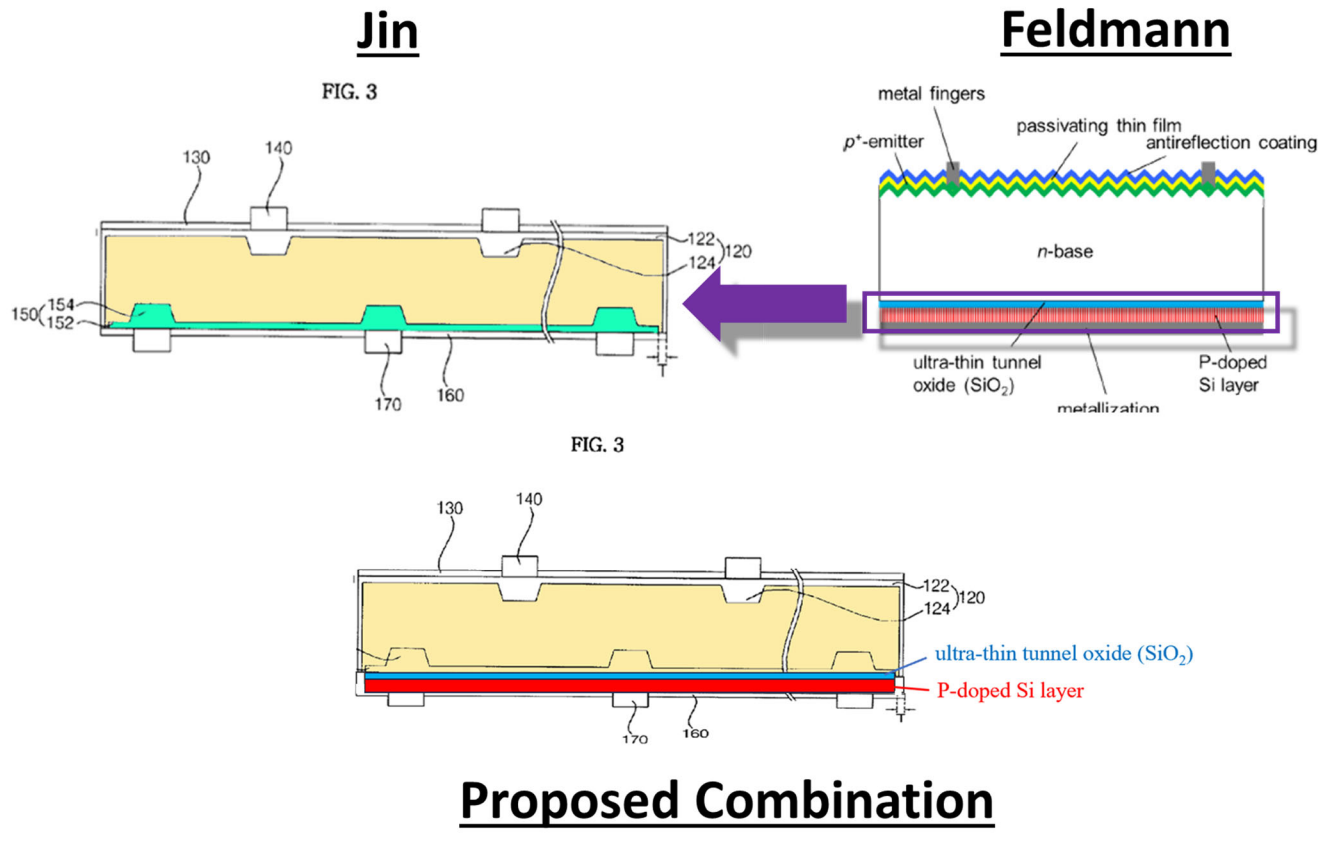
[7] Jin Figure 2 identifies the silicon substrate 110. Figure 3 shows a cross-section of the same solar cell as Figure 1 but from a wider perspective. EX1009-Jin, ¶¶11-13, Figs. 1-3.

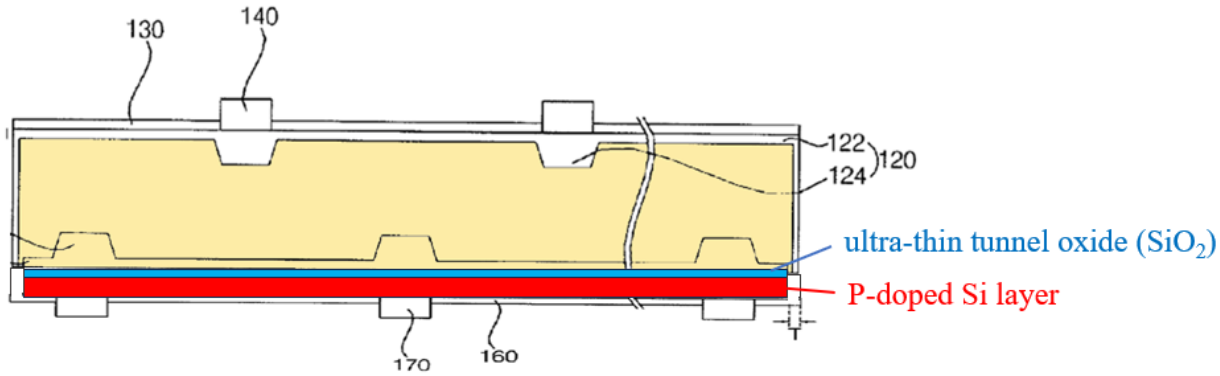
back side while the "second" surface is the front sun-facing side. EX1001, 6:27-34, 7:42-48, Fig. 2. As described above, in the proposed combination of Jin and Feldmann, Jin's diffused BSF layer 150 is replaced with the TOPCon structure of Feldmann, i.e., the ultra-thin tunnel oxide (SiO_2) (blue) and phosphorus-doped polysilicon layer (red). EX1012-Feldmann, §2.1, Fig. 3; *see* ¶¶105-113 above. According to the 104 Patent, tunnel layer 160 "may be formed of silicon oxide (SiO_x)" and has a thickness between 0.5-2.5 nm. EX1001, 8:11-12, 8:30-32. Feldmann's "ultra-thin wet chemical oxide layer" is likewise a silicon oxide (SiO_2) layer of about 14 angstroms, which is 1.4 nm. EX1012-Feldmann, §2.1, Fig. 3. In addition, Feldmann's ultra-thin tunnel oxide layer (SiO_2), which is formed on the rear surface of Feldmann's solar cell, is likewise formed on the rear surface of the Jin's silicon substrate 110. EX1012-Feldmann, Fig. 3; EX1009-Jin, ¶26, Fig. 3.



d) [1.d] First Conductive Type Semiconductor Region

129. Claim 1 next recites: "*a first conductive type semiconductor region on the tunnel layer and containing impurities of a first conductive type*." As described above, in the proposed combination of Jin and Feldmann asserted here, Jin's diffused phosphorous-doped BSF layer 150 is replaced with the TOPCon structure of Feldmann, i.e., the ultra-thin tunnel oxide (SiO_2) (blue) and phosphorus-doped polysilicon layer (red). EX1009-Jin, ¶78; EX1012-Feldmann, §2.1, Fig. 3; *see* ¶¶105-113 above. Phosphorous is an n-type dopant. EX1009-Jin, ¶47.

Combination of Jin and Feldmann



130. Feldmann's "P-doped Si layer" ("*first conductive type semiconductor region*") is formed on the ultra-thin tunnel oxide (SiO_2) layer ("*tunnel layer*"). EX1012-Feldmann, Abstract, §2.1, Fig. 3. Feldmann teaches that to make the disclosed solar cells with TOPCon, after growing the ultra-thin tunnel oxide layer on the silicon wafer, a "20 nm thick phosphorus-doped Si layer [is] deposited **on**" the front surface of the wafer, thereby being formed on the oxide layer. *Id.*, §2.1 (emphasis added).

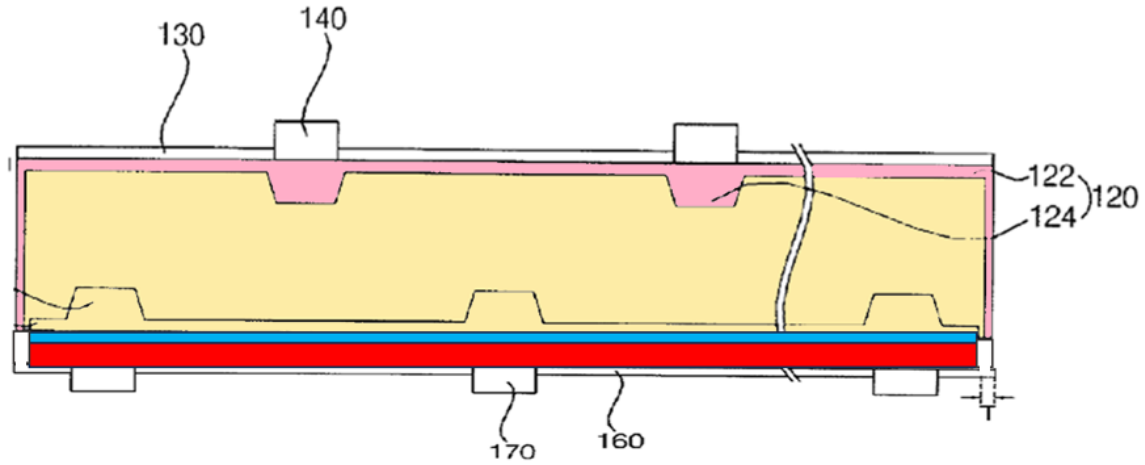
131. Feldmann's "P-doped Si layer" is doped with phosphorous (P). EX1012-Feldmann, Fig. 3, Abstract ("Our structure is based on an ultra-thin tunnel oxide (SiO2) and a phosphorous-doped silicon layer…."), §2.1 ("phosphorus-doped Si layer"), §3 ("It has been shown that our TOPCon structure based on a tunnel oxide and phosphorus doped Si layer passivates the surface effectively…."). Phosphorous-doped silicon is a well-known n-type semiconductor, as observed by Jin and the 104 Patent. EX1009-Jin, ¶27 ("[S]ilicon may be doped with an

impurity of group 5 element such as P, As, and Sb, and be implemented as an N-type."), ¶¶47, 49, 73-74; EX1001, 10:38-41, ("An n type dopant used as the impurities of the first or second conductive type may include group 5 elements, such as phosphorous (P)…."). Feldmann's phosphorus-doped Si layer thus has "*impurities of a first conductive type,*" *i.e*., phosphorous impurities which are n-type.

e) [1.e] Second Conductive Type Semiconductor Region

132. Claim 1 next recites: "*a second conductive type semiconductor region on a second surface opposite to the first surface of the semiconductor substrate and containing impurities of a second conductive type opposite to the first conductive type*." Jin discloses a solar cell with an emitter layer 120 (pink) on the front "*second surface*" of the silicon substrate 110, opposite to the rear "*first surface*" where the ultra-thin tunnel oxide (SiO_2) layer (blue) is located. EX1009-Jin, ¶29, Fig. 3.

Combination of Jin and Feldmann



133. In the proposed combination of Jin and Feldmann, the silicon substrate 110 is doped with phosphorous and is an n-type semiconductor. *See* ¶¶125-127; EX1009-Jin, ¶¶26-27. Jin teaches that "if the substrate 110 is an N-type, the emitter layer 120 is doped with a P-type impurity," and that by doping the substrate 110 and emitter layer 120 with "opposite types of impurities," a P-N junction is formed. EX1009-Jin, ¶29. Jin further discloses that boron (B) is an example of a P-type impurity. *Id.*, ¶27. The emitter layer 120 thus has "*impurities of a second conductive type [boron p-type impurities] opposite to the first conductive type*" of the "*first conductive type semiconductor region*" (Feldmann's phosphorous-doped Si layer), which is n-type. *See supra* ¶¶ 129-131. Jin also discloses that the substrate 110 is a "semiconductor substrate," and that the emitter layer 120 is formed by doping the substrate 110, such that the emitter layer 120 is also "*a second conductive type semiconductor region*" as claimed. EX1009-Jin

¶¶26, 29. Similar to Jin, Feldmann likewise discloses a boron-doped "p+ emitter" on the front side of the substrate, and thus would similarly have an "*a second conductive type semiconductor region on a second surface opposite to the first surface of the semiconductor substrate and containing impurities of a second conductive type opposite to the first conductive type*," as claimed. EX1012-Feldmann, §2.2, Fig. 3.

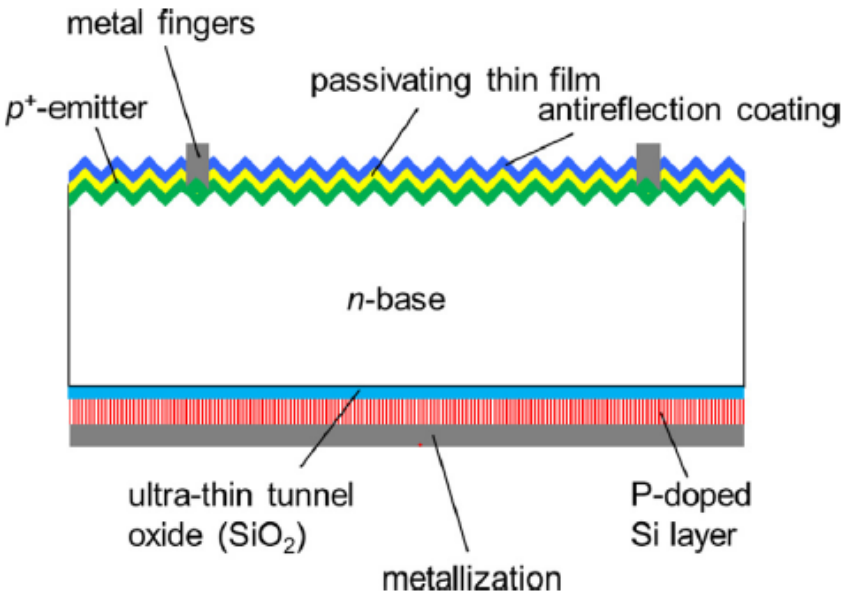


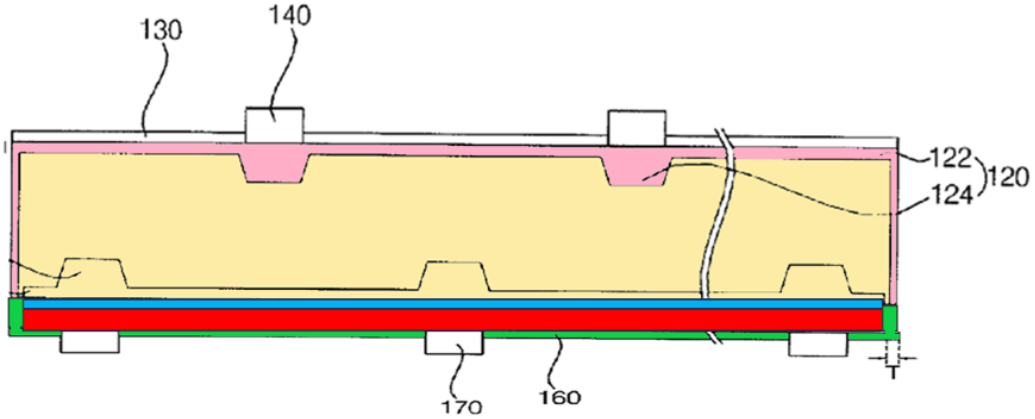
Fig. 3. Schematic of the solar cell structure with the passivated rear contact. The solar cells feature a diffused boron-doped emitter at the front side which is passivated by atomic layer deposited (ALD) aluminum oxide Al_2O_3 and a plasma-enhanced chemical vapor deposited (PECVD) silicon nitride SiN_x.

f) [1.f] First Passivation Film

134. Claim 1 next recites: "*a first passivation film on the first conductive type semiconductor region*." Jin discloses this element. As seen in modified Figure 3, anti-reflection film 160 (green) is on the rear surface of the solar cell, on the phosphorous-doped polysilicon layer (red) ("*the first conductive type*

semiconductor region"). EX1009-Jin, ¶50 ("a second anti-reflection film 160 is disposed on the back surface field layer 150"). Jin teaches that when the substrate 110 is n-type, the anti-reflection film 160 (green) "performs the function of a passivation layer" corresponding to the claimed "*first passivation film.*" *Id*. In the Jin/Feldmann combination, the substrate is likewise n-type doped. *See* ¶¶125-127.

Combination of Jin and Feldmann

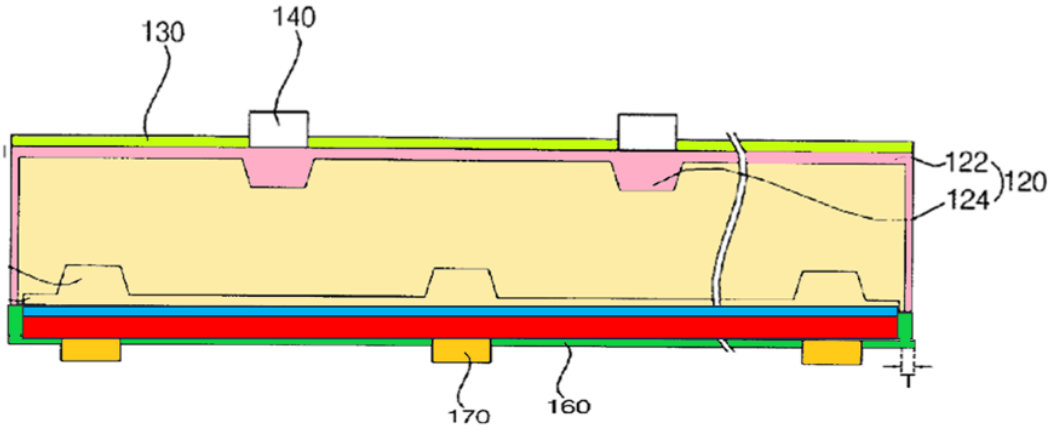


135. Moreover, the 104 Patent explains that the *first passivation film* (190A) may be made of the same materials as an anti-reflection layer, including silicon nitride, silicon oxide, silicon oxynitride, MgF_2, ZnS, TiO_2, and CeO_2. EX1001, 11:33-39. The anti-reflection film 160 in Jin can also be made of these same materials. EX1009-Jin, ¶50. In other words, Jin's anti-reflection film 160 is made of the same materials and performs the same function as the claimed "*first passivation film*" and would be compatible with the combined Jin/Feldmann solar cell.

g) [1.g] First Electrode

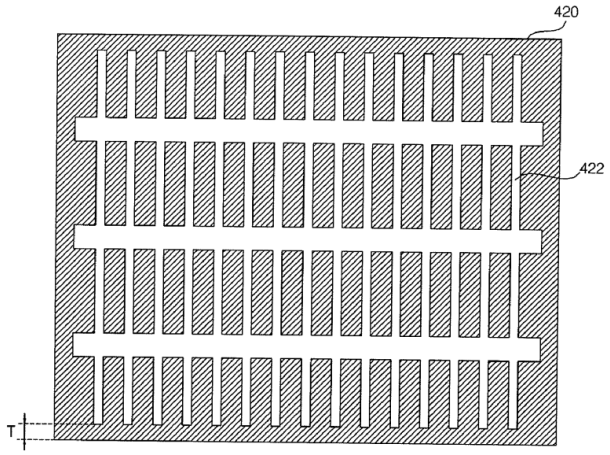
136. Claim 1 next recites: "*a first electrode formed on the first passivation film and connected to the first conductive type semiconductor region through an opening formed in the first passivation film*." Jin discloses rear finger electrodes 170 (orange) connected to the back surface layer 150, replaced with Feldmann's TOPCon structure. EX1009-Jin, ¶26, 52-53, Fig. 3; *see* ¶¶105-113 above. In the proposed combination of Jin/Feldmann, the rear finger electrodes 170 (orange) are formed on and connect to the phosphorous-doped polysilicon layer (red) through gaps in the second anti-reflection film 160 (green) formed, for example, by screen printing on the second anti-reflection film. EX1009-Jin, ¶52-53, 99-101, Figs. 3, 11. During screen printing, the heat treatment applied to the paste causes "a fire-through phenomenon in which the printed paste penetrates the first anti-reflection film 130 through use of a glass frit" and "makes contact with the first area 124 of the emitter layer 120." *Id.* ¶99, 101 ("the rear finger lines 170 may be formed in a similar way as the front finger lines 140"). The fire-through process creates openings in the passivation layer 160. *Id.* Likewise, laser ablation removes portions of the anti-reflection film in the areas where the electrodes are to be deposited. *Id.* ¶¶53, 100.

Combination of Jin and Feldmann



137. To form the rear finger electrodes 170 ("first finger electrodes") and rear surface bus electrode 190 ("first bus bar"), Jin teaches to use a mask pattern 420 with openings 422 "formed to have a grid shape to correspond to the back surface finger lines 170 and the back surface bus electrodes 190." EX1009-Jin, ¶¶88-89 ("The openings 422 of the … mask 420 may be formed not only at positions corresponding to where the rear finger lines 170 are to be formed, but also at positions corresponding to where the rear surface electrodes (190 of FIG. 1) are to be formed…."), Fig. 10.

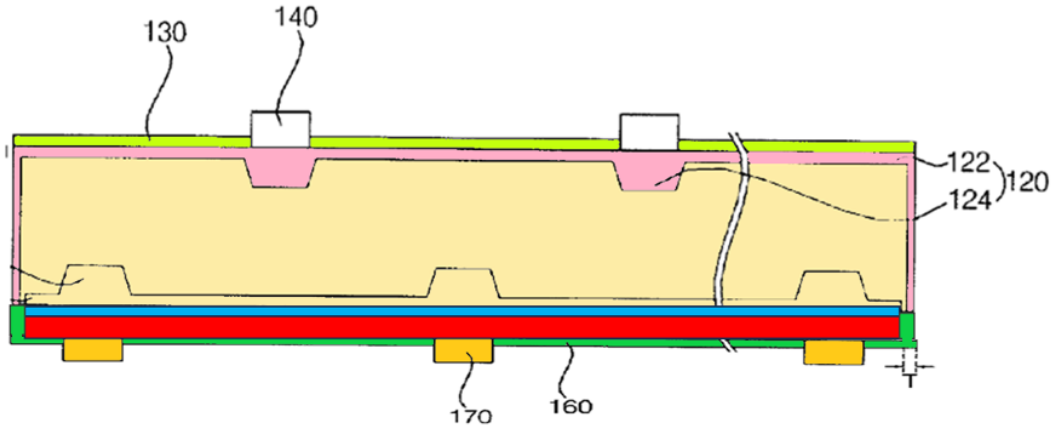
FIG. 10



(a)

138. Jin subsequently explains that the "[t]he front finger lines 140, for example, may be formed in such a way that paste for front surface electrodes is screen printed on the area on the substrate 110 where the front finger lines 140 are to be formed by using a mask." EX1009-Jin, ¶99. Jin further explains that "the rear finger lines 170 may be formed in a similar way as the front finger lines 140." *Id*., ¶101. The Skilled Artisan would understand that because the mask pattern 420 includes openings for both the finger electrodes and surface bus electrodes, when used to form the rear electrodes, the mask would form both the rear finger lines 170 and rear surface bus electrodes 190 at the same time. By using the same mask 420 to form the back surface finger lines 170 and the back surface bus electrodes 190, all the back surface finger lines 170 and the back surface bus electrodes 190 would be formed through the anti-reflection film 160 (green) to connect to the "P-doped Si layer" (red).

Combination of Jin and Feldmann



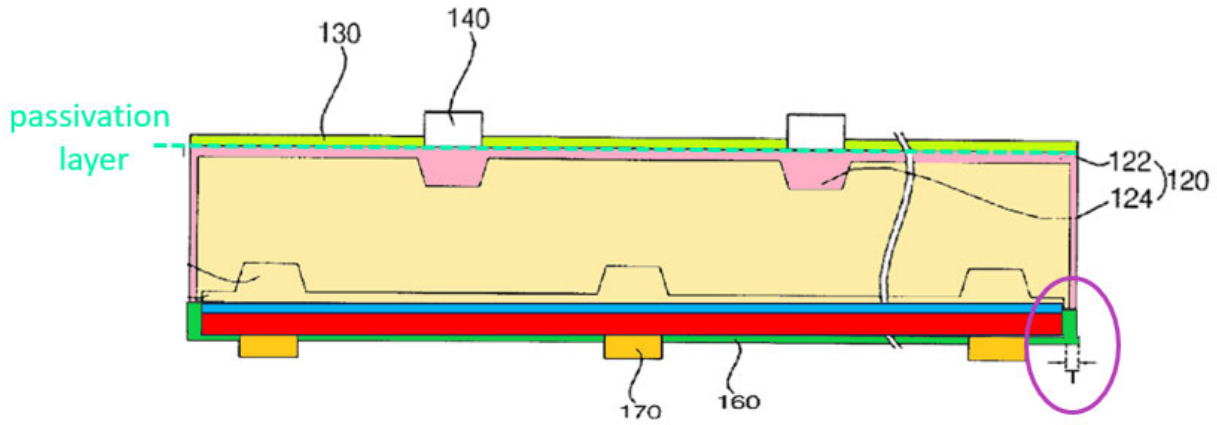
h) [1.h] Second Passivation Film

139. Claim 1 next recites: "*a second passivation film on the second conductive type semiconductor region*." Jin discloses that "if the substrate 110 is an N-type, a passivation layer may be further included between the emitter layer 120 and the first [front side] anti-reflection film 130." EX1009-Jin, ¶37, Fig. 3. In the proposed combination of Jin and Feldmann, the silicon substrate 110 is an n-type semiconductor. *See* ¶¶125-127. Thus, Jin discloses a passivation layer between the emitter layer 120 and the anti-reflection film 130. Moreover, in order for Jin's passivation layer[8] to be between the emitter layer 120 (pink) and the front

[8] Jin's front side passivation layer is not shown in Figure 3 but would be between the emitter layer 120 (pink) and the front side anti-reflection film 130 (light green).

side anti-reflection film 130 (light green), it must be **on** the emitter layer 120 ("*the second conductive type semiconductor region*").

Combination of Jin and Feldmann



140. Indeed, an example of this structure can be readily seen in Fig. 3 of Feldmann where a thin passivating film (yellow) is on the p+ emitter (green) and is between the emitter (green) and the front side anti-reflection coating (blue). EX1012-Feldmann, §2.2, Fig. 3.

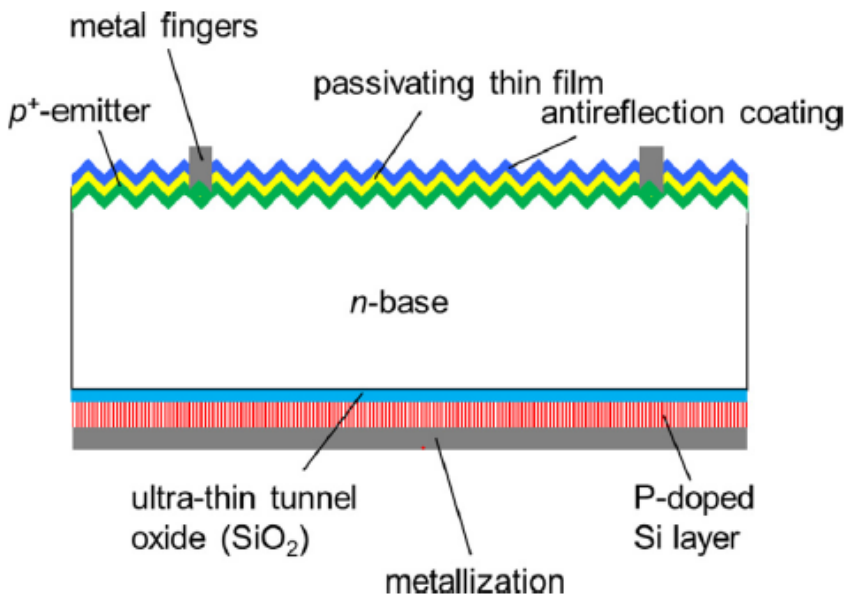


Fig. 3. Schematic of the solar cell structure with the passivated rear contact. The solar cells feature a diffused boron-doped emitter at the front side which is passivated by atomic layer deposited (ALD) aluminum oxide Al_2O_3 and a plasma-enhanced chemical vapor deposited (PECVD) silicon nitride SiN_x.

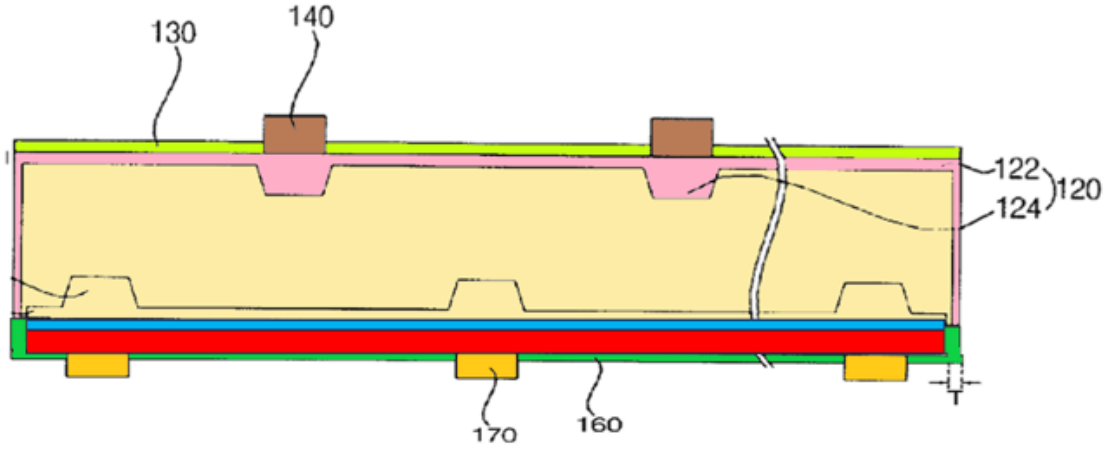
i) [1.i] Second Electrode

141. Claim 1 next recites: "*a second electrode formed on the second passivation film and connected to the second conductive type semiconductor region through an opening formed in the second passivation film*." Jin discloses front finger electrodes 140 connected to the emitter layer 120. EX1009-Jin, ¶26, Fig. 3. The front finger electrodes 140 (brown) are coupled together by a front surface bus electrode 180. EX1009-Jin, ¶38, Fig. 1.

142. The front finger electrodes 140 (brown) are formed on and connect to the emitter layer 120 (pink) through gaps in the passivation film. While the passivation film is not shown in Fig. 3, as discussed above in ¶¶139-140, it is between the emitter layer 120 (pink) and the anti-reflection film 130 (light green).

The gaps in the passivation film are formed, for example, by screen printing or ablation of the passivation film. EX1009-Jin, ¶¶38-40, 100 ("Also, the front finger lines 140 may be formed by removing of the first anti-reflection film 130 and/or the passivation layer by using laser ablation….") Figs. 3, 11. During screen printing, the heat treatment applied to the paste causes "a fire-through phenomenon in which the printed paste penetrates the first anti-reflection film 130 through use of a glass frit," creating openings in the passivation layer. *Id.* ¶99. Likewise, laser ablation removes portions of the anti-reflection film in the areas where the electrodes are to be deposited. *Id.* ¶100.

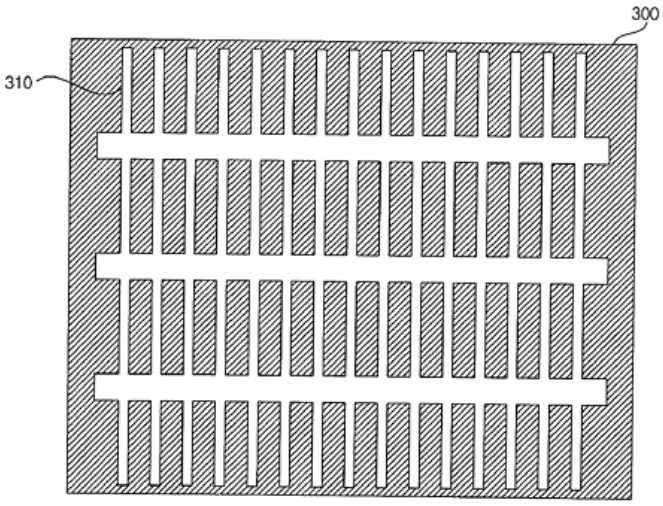
Combination of Jin and Feldmann



143. To form the front finger electrodes 140 ("*second finger electrodes*") and front surface bus electrode 180 ("*second bus bar*"), Jin teaches to use a mask pattern 300 with openings 310 "formed to have a grid shape to correspond to the

front finger lines 140 and the front surface bus electrodes 180." EX1009-Jin, ¶81 ("The openings 310 [of mask 300] may be formed not only at the positions where the front finger lines 140 are to be formed, but also at the positions where the front surface bus electrodes (180 of FIG. 1) are to be formed."), Figs. 8; *see also id.* ¶ 97, Fig. 10.

FIG. 8

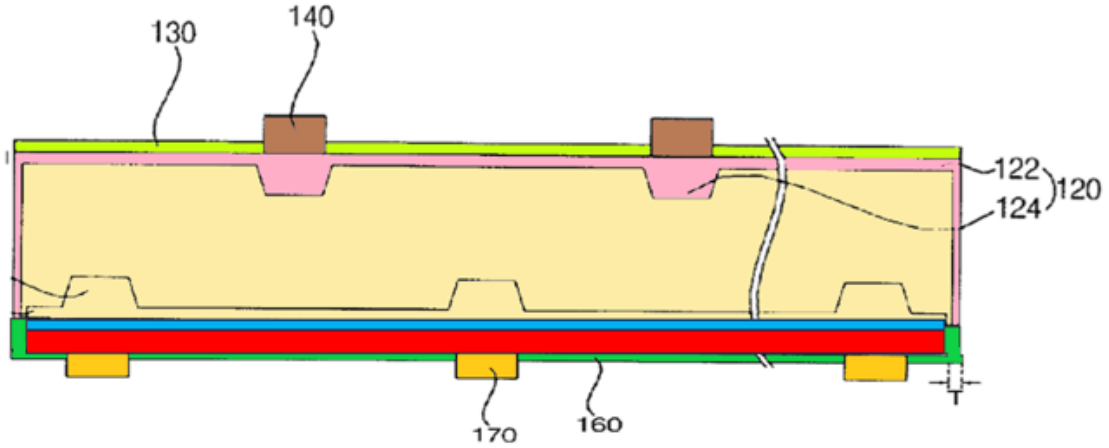


(a)

144. Jin subsequently explains that the "[t]he front finger lines 140, for example, may be formed in such a way that paste for front surface electrodes is screen printed on the area on the substrate 110 where the front finger lines 140 are to be formed by using a mask." EX1009-Jin, ¶99. The Skilled Artisan would understand that because the mask patterns 300/420 include openings for both the finger electrodes and surface bus electrodes, when used to form the rear electrodes, the mask would form both the front finger lines 140 and front surface bus

electrodes 180 at the same time. By using the same mask 300/420 to form the front surface finger lines 140 and the front surface bus electrodes 180, all the front surface finger lines 140 and the front surface bus electrodes 180 would be formed through the anti-reflection film 160 (green) on the "P-doped Si layer" (red).

Combination of Jin and Feldmann



145. Feldmann likewise discloses and shows front electrodes (metal fingers) penetrating the anti-reflection coating (blue) and passivating thin film (yellow) to connect with the p+ emitter (green). EX1012-Feldmann, §2.2, Fig. 3.

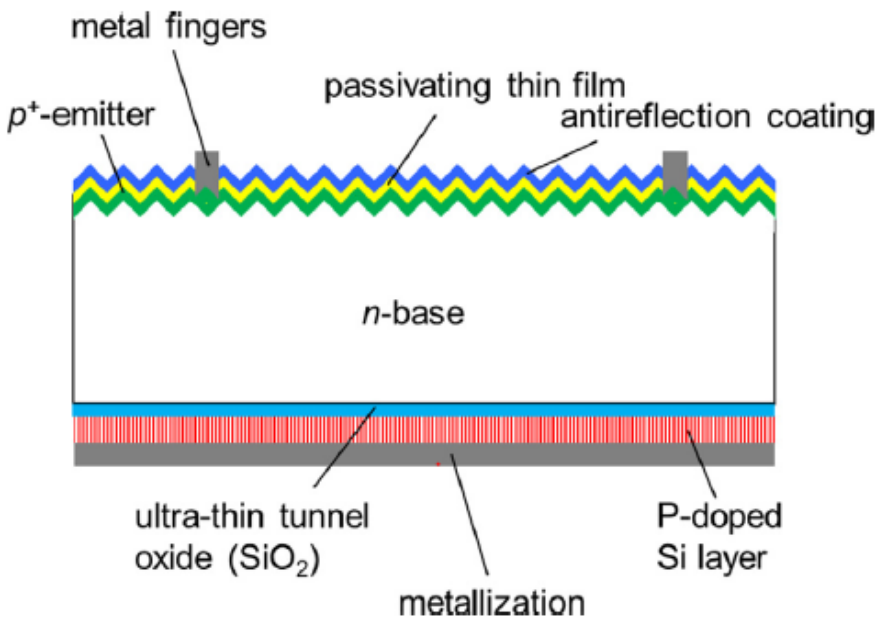


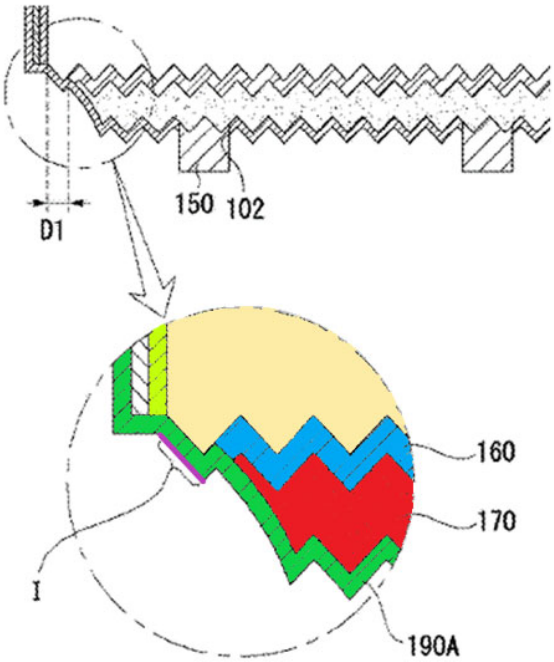
Fig. 3. Schematic of the solar cell structure with the passivated rear contact. The solar cells feature a diffused boron-doped emitter at the front side which is passivated by atomic layer deposited (ALD) aluminum oxide Al_2O_3 and a plasma-enhanced chemical vapor deposited (PECVD) silicon nitride SiN_x.

j) [1.j] Isolation Portion

146. Claim 1 next recites: "*an isolation portion for preventing a contact between the first conductive type semiconductor region and the second conductive type semiconductor region, wherein the isolation portion excludes the tunnel layer and the first conductive type semiconductor region, and is in an edge portion of the first surface of the semiconductor substrate*." In the proposed combination of Jin and Feldmann, gap T is an "isolation portion" as claimed.

147. As shown in Fig. 2 of the 104 Patent (excerpted below), the isolation portion I represents the area "in which the tunnel layer 160 and the first conductive type semiconductor region 170… are not formed." EX1001, 13:6-23, Fig. 2. As

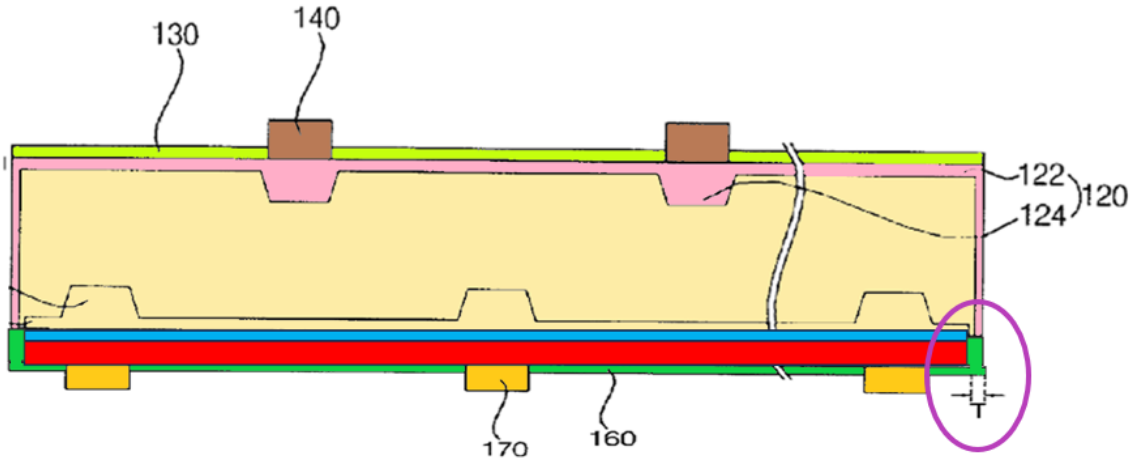
the 104 Patent explains, when the second conductive type semiconductor region 120 (i.e., the front side emitter) is formed, dopants diffusing into the side or edge of the substrate may result in electrical shorting between the first 170 and second 120 conductive type semiconductor regions. EX1001, 13:24-35. The isolation portion I separates the edge of the tunnel oxide 160 and first conductive type semiconductor region 170 from the edge of the back surface of the substrate 100 by a distance D1, and thus "function[s] as an edge isolator for isolating the first conductive type semiconductor region 170 from the edge of the back surface of the semiconductor substrate 100." EX1001, 12:60-13:23, Fig. 2.



148. Jin likewise discloses an isolation area, which Jin refers to as a gap T separating the edge of the back surface field layer 150 and the edge of the silicon

substrate 110. EX1009-Jin, ¶¶57-58, Fig. 3. Like the 104 Patent's isolation portion, Jin's gap T isolates and inhibits electrical shorting between the back surface field layer 150 and the emitter layer 120 (pink) caused by diffusion of dopants along the edges of the substrate 110 when forming the BSF 150. EX1009-Jin, ¶¶58-60. In the proposed combination of Jin/Feldmann, the gap T would thus separate the edge of the ultra-thin tunnel oxide (SiO_2) (blue) and phosphorus doped Si layer (red) of Feldmann from the edge of the silicon substrate 110 to prevent short-circuiting with the emitter layer 120 (pink) ("*for preventing a contact between the first conductive type semiconductor region and the second conductive type semiconductor region*").

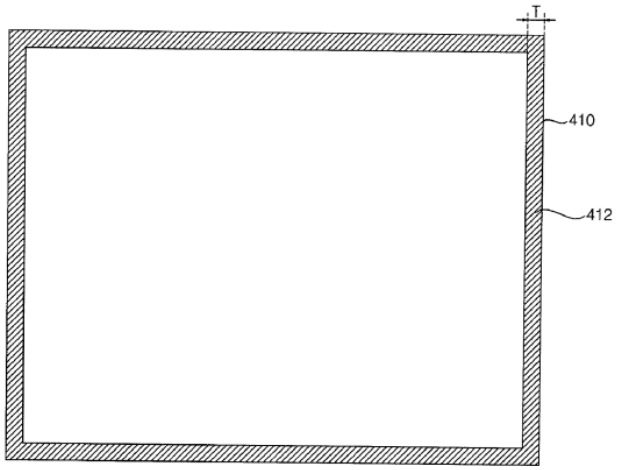
Combination of Jin and Feldmann



149. The Gap T "*excludes the tunnel layer and the first conductive type semiconductor region*." Jin's Gap T is created by forming a mask pattern with a width T to cover the edges of the rear surface of the silicon substrate, and then

doping the substrate; the mask prevents dopants from becoming implanted in the perimeter region, thereby preventing electrical contact with the emitter layer 120 (pink). EX1009-Jin, ¶¶83-85, Fig. 9.[9] In Jin, the result of the mask pattern is a gap that excludes the back surface field 150 around the edges of the substrate. As I discussed in ¶¶115-122 above, this same mask configuration would be used to exclude the "ultra-thin tunnel oxide (SiO_2)" (blue)and "P-doped Si layer" (red) in the proposed combination of Jin/Feldmann from being formed around the edge portion or periphery of the substrate. EX1012-Feldmann, Abstract, §2.1.

FIG. 9



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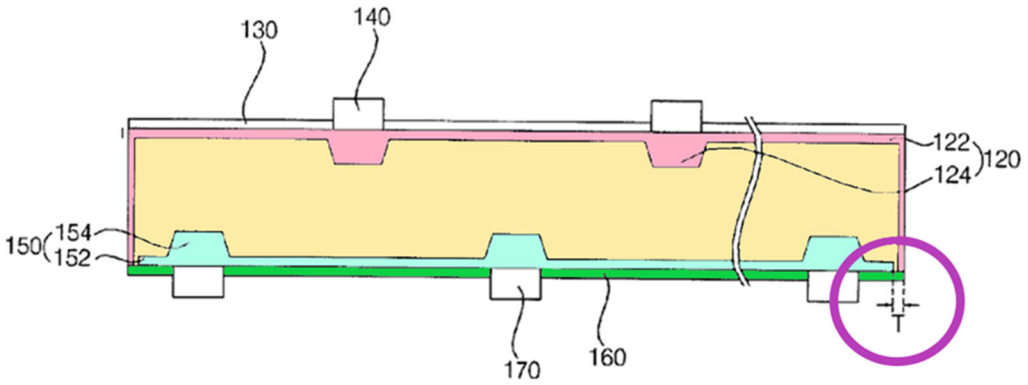
[9] Figure 9 of Jin and its related discussion describe the formation of the embodiment depicted in Figure 3. EX1009-Jin, ¶78.

150. Finally, the gap T "*is in an edge portion of the first surface of the semiconductor substrate*." As shown in Figures 3 and 9 above, the gap T is "measured from the edge part of the rear surface of the substrate 110." EX1009-Jin, ¶¶57-60, 85-86, Figs. 3, 9.

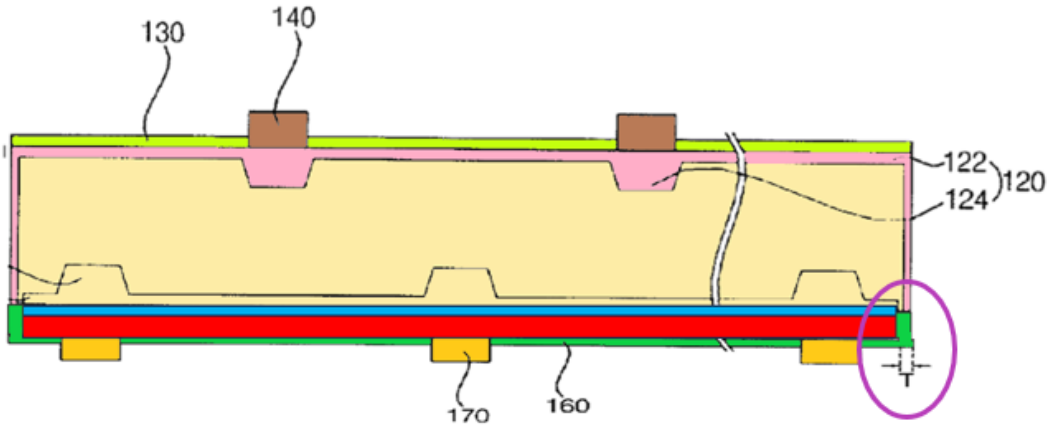
k) [1.k] First Passivation Film Covering Isolation Portion

151. Claim 1 next recites: "*wherein the first passivation film covers the first surface of the semiconductor substrate and the isolation portion together*." As discussed in ¶¶134-135 above, Jin's anti-reflection layer 160 (green) corresponds to the "first passivation film" of Claim 1, and it satisfies this element as well. As Fig. 3 demonstrates, the second anti-reflection film 160 (green) covers the rear ("*first surface*") of the substrate 110 and the gap T ("*isolation portion*") discussed in ¶¶146-150. EX1009-Jin, ¶¶50-51, 57, Fig. 3. In the combined Jin/Feldmann solar cell, Jin's anti-reflection layer 160 (green) functioning as a passivation layer would similarly cover the isolation gap T and the substrate at the edge portion such that there would not be exposed silicon surface that would act as recombination sites.

FIG. 3



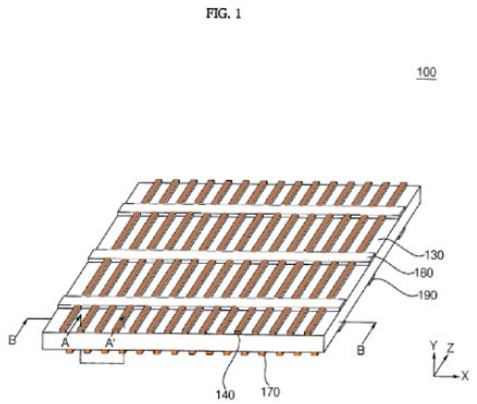
Combination of Jin and Feldmann

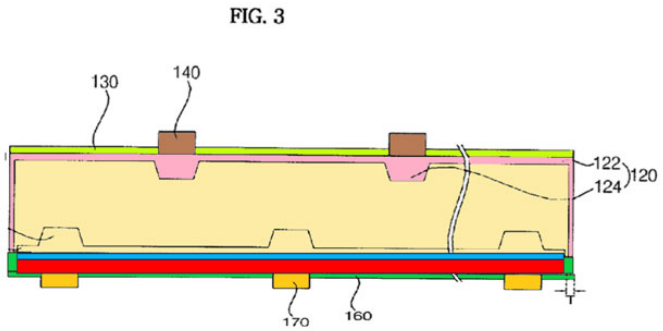


2. Claim 2 – Finger Electrodes

152. Claim 2 depends from claim 1 and requires that the first (back) electrodes "*comprises a plurality of first finger electrodes spaced apart from each other and extended in parallel in a first direction*" and that the second (front) electrodes "*comprises a plurality of second finger electrodes spaced apart from each other and extended in parallel in the first direction*." Jin discloses that the front and backside electrodes comprise "front **finger** electrodes" 140 and "rear

finger electrodes" 170, respectively. EX1009-Jin, ¶26, 38-40, 52-54, Fig. 3. *See* ¶¶136, 141-143. The finger electrodes 140 (brown) and 170 (orange) are shown as thin parallel lines extending into the page in Figs 1, 3. By being parallel to each other, the "*plurality of first finger electrodes*" and the "*plurality of second finger electrodes*" naturally extend in the same "*first direction*."

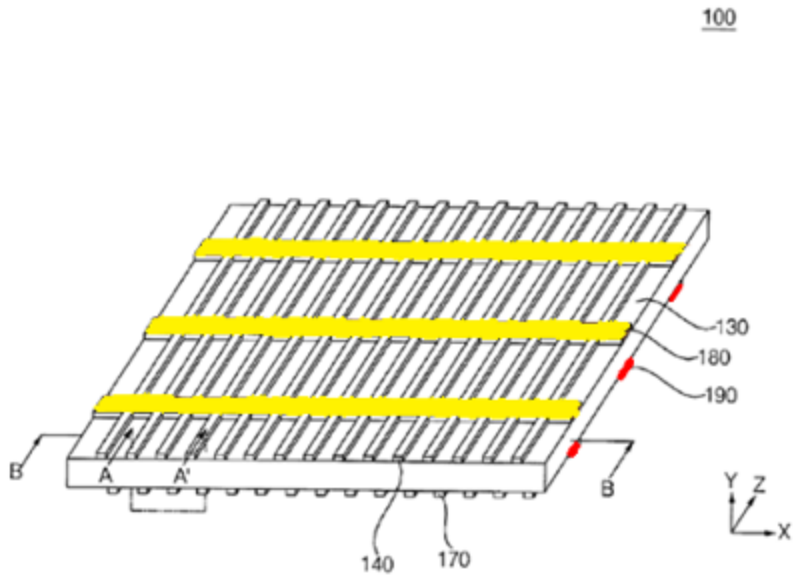




3. Claim 3 – Bus Bars

153. Claim 3 depends from Claim 2 and requires that the first (back) electrode "*further comprises a first bus bar connected to the plurality of first finger electrodes*" and that the second (front) electrodes "*further comprises a second bus bar connected to the plurality of second finger electrodes*." Jin discloses that the front finger electrodes 140 "adjoin front surface bus electrode 180" (yellow) and rear finger electrodes 170 "adjoin[] to a rear surface bus electrode 190" (red), as shown in Figure 1 below. EX1009-Jin, ¶¶38, 54, Fig. 1.

FIG. 1



4. Claim 4 – Polycrystalline and Single Crystal Silicon

154. Claim 4 depends from claim 1 and recites: "*wherein the first conductive type semiconductor region includes a polycrystalline silicon material, and the second conductive type semiconductor region includes a single crystal silicon material*."

155. As described above, in the proposed combination of Jin and Feldmann asserted here, Jin's diffused phosphorous-doped BSF layer 150 is replaced with the TOPCon structure of Feldmann, i.e., the ultra-thin tunnel oxide (SiO_2) (blue) and phosphorus-doped polysilicon layer (red) ("*the first conductive type semiconductor region*"). EX1009-Jin, ¶78; EX1012-Feldmann, §2.1, Fig. 3; *see* ¶¶105-113 above. Feldmann's "P-doped Si layer" is a polysilicon layer, which is synonymous with

polycrystalline silicon. Feldmann teaches to anneal the phosphorus-doped Si layer after depositing the silicon on the wafer. EX1012-Feldmann, §2.1. Annealing was a well-known method for converting deposited silicon to polysilicon. EX1021-Quirk, 499-501; EX1030-Streetman, 159-61. Likewise, the 104 Patent discloses that annealing is performed on the deposited semiconductor layer 170 to form the polysilicon layer 170. EX1001, 29:15-19 ("a separate crystallization annealing process needs to be performed so that the intrinsic semiconductor layer 170' has a polycrystalline structure after it is formed").

156. Jin does not explicitly disclose the crystalline structure of its silicon substrate 110, from which the emitter layer 120 is formed. *See* EX1009-Jin, ¶29. However, Feldmann disclosed that the wafers used to form Feldmann's TOPCon solar cells were "(100)-oriented floating zone (FZ) silicon wafers," which are single-crystalline, (100)-oriented crystal structures. EX1012-Feldmann, §2.1; EX1030-Streetman, 7-10. It was well known that single-crystalline silicon was commonly used to form solar cells. In fact, just a few years prior to August 31, 2015, the effective filing date of the 104 Patent, roughly 90% of the world's solar cells were made using either single-crystalline or polycrystalline silicon. EX1034-Saga, Abstract; EX1022-Luque, 206. It would have been obvious to a Skilled Artisan to try using monocrystalline silicon for the Jin/Feldmann solar cell substrate and emitter layer given Jin's silence on this point, Feldmann's teaching to

use 100 orientation monocrystalline silicon, and because monocrystalline silicon was one of the two most prevalent options in use in the industry.

157. A Skilled Artisan would also have been motivated to use a single-crystalline silicon substrate (and emitter layer) in the Jin/Feldmann solar cell, as taught by Feldmann, because it was well known that single-crystalline cells have higher efficiencies than polycrystalline cells, and therefore were more attractive from an efficiency point of view. EX1034-Saga, 5. Moreover, a Skilled Artisan would have understood that Jin's solar cell would be compatible with a single-crystalline substrate/emitter layer, as none of Jin's teachings are directly dependent on the crystalline type of the silicon, and Jin is silent on this point.

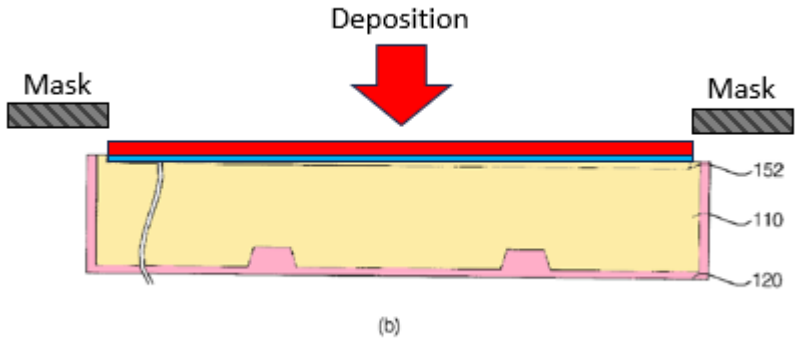
5. Claim 5 – Isolation Width

158. Claim 5 depends from claim 1 and recites: "*wherein a width of the isolation portion is 1 nm to 1 mm*." Jin disclosed that the width of gap T ("*isolation portion*") "may range from 2 to 300 μm," which is between 1 nm and 1 mm. EX1009-Jin, ¶¶60, 86.

6. Claim 6 – Decreasing Polysilicon Thickness

159. Claim 6 depends from claim 1 and recites: "*wherein a thickness of an edge region in the first conductive type semiconductor region progressively decreases towards the isolation portion.*" A Skilled Artisan would understand and find it obvious that the thickness of the phosphorous-doped polysilicon layer in the

Jin/Feldmann solar cell would taper at the edges, towards the gap T isolation region. As I explained above in ¶¶115-123, one well known and readily-achievable way to construct Feldmann's TOPCon structure in the combined Jin and Feldmann solar cell would be to use a metal "shadow" mask process like that taught by Scherff. In particular, a metal mask shaped like the mask shown in Fig. 9 of Jin would be placed over the substrate to cover the periphery of the surface of the substrate before depositing the phosphorous-doped polysilicon layer using, for example, PECVD or ALD. EX1031-Scherff, §§1-2. Unlike a mask physically bonded to the substrate, a metal mask is placed very close to the surface of the substrate but remains detachable. *Id*. The polysilicon material is then deposited through the opening in the mask, as illustrated below in a modified version of Jin's Figure 9(b). *See id*.



160. As a Skilled Artisan would have understood, the metal mask is not perfectly abutting against the substrate surface, but rather is a very small distance from the surface. EX1031-Scherff, §1. As a result, during the deposition process,

small amounts of the polysilicon would collect in the "shadow" region underneath the mask. Thus, using a shadow-mask process to form Jin/Feldmann's combined solar cell would result in the phosphorous-doped polysilicon layer (red) tapering in thickness near the edges of the mask opening rather than forming an abrupt edge, such that "*a thickness of an edge region in the first conductive type semiconductor region progressively decreases towards the isolation portion*"—gap T—which is formed in the masked regions at the edge of the substrate. EX1009-Jin, ¶¶83-85, Fig. 9.

161. This tapering that would occur underneath the metal mask is illustrated, for example, in Figure 4 of a paper depicting the "overspray" that occurs under the edges of a shadow mask when there is separation between the mask and the substrate surface. EX1032-Decker, 97, Fig. 4. The uneven deposition of material under the edges of the mask is caused by the mask blocking the trajectory of particles approaching the substrate surface from straight above or from the outside, while allowing particles approaching over the opening but at an angle to settle beneath the mask, similar to the penumbra formed as a light source is partially blocked. *See id.* Even as the separation distance nears zero, a slight curvature remains in the formation of the deposited layer. *Id*. The type of deposition can also play a role in the tapering effect; for example, sputtering results

in a less defined deposition pattern with even more rounded edges. *Id.*, 97-98, Fig. 5.

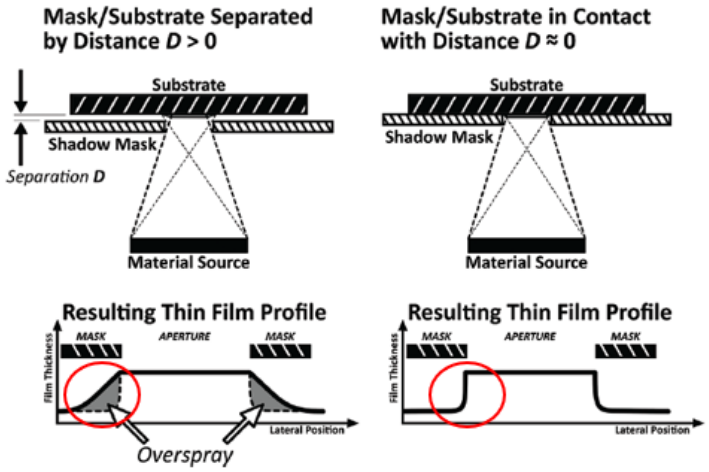


Figure 4. Thin film height profile for deposition with shadow mask separated by distance *D* from substrate (left) and shadow mask in close contact with substrate (right).

162. The tapering effect caused by shadow masking was a well-known phenomenon in the art by 2015, as others had known and commented on it years earlier. For example, a 2006 paper reported that "[s]puttered atoms arrive at substrates with various incident angles because of scattering by atmospheric gasses. Then the pattern edges thin down by deposition of particles shaded from the mask pattern." EX1033-Okuyama, 2890, Fig. 4.

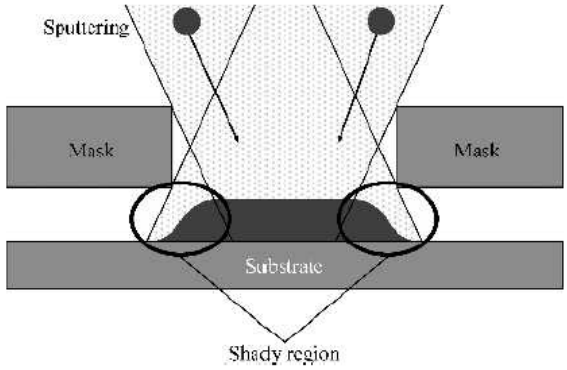


FIG. 4. Schematic of the "shadow effect" that appeared through the mask pattern. The pattern edges thin down because of deposition of shaded sputtered atoms under the mask edges (indicated by the oval).

163. Accordingly, depositing a phosphorous-doped polysilicon layer using a metal shadow mask approach in Jin/Feldmann would result in a taper in the polysilicon layer (red) at the edges of the mask into the mask "shadow" regions, towards the gap T isolation region, as depicted in modified Figs. 3 and 9 from Jin below. A Skilled Artisan would therefore find claim 6 obvious in view of Jin/Feldmann, in light of well-known phenomena that occur during the manufacturing process.

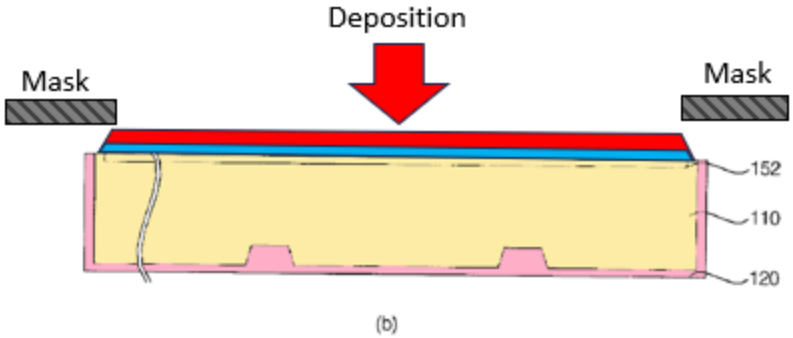
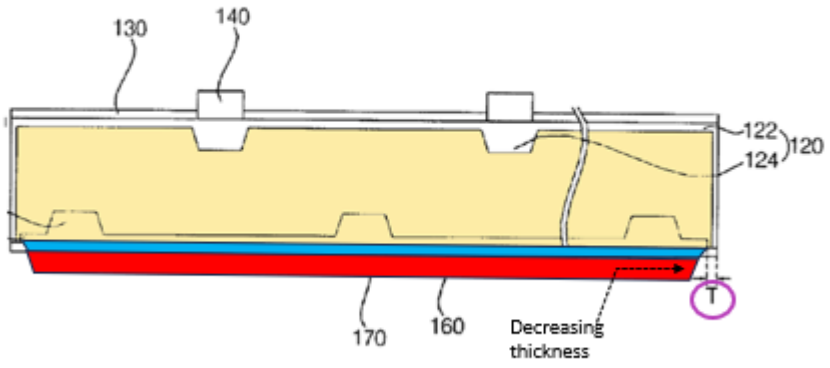


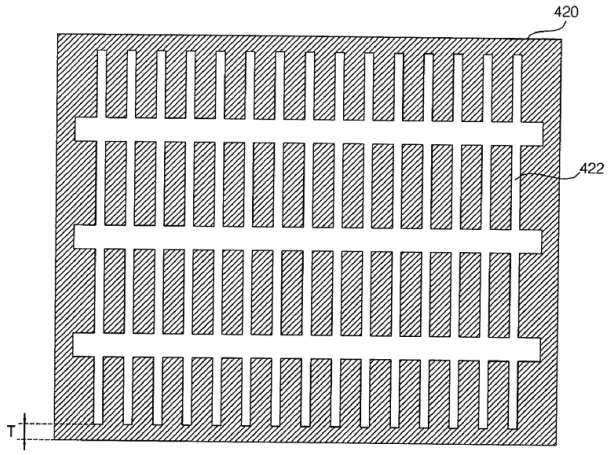
FIG. 3



7. Claim 9 – Electrodes Connected to the First Conductive Type Semiconductor Region

164. Claim 9 depends from claim 3 and recites: "*wherein all of the plurality of first finger electrodes and the first bus bar are connected to the first conductive type semiconductor region through the first passivation film*." To form the rear finger electrodes 170 ("*first finger electrodes*") and rear surface bus electrode 190 ("*first bus bar*"), Jin teaches to use a mask pattern 420 with openings 422 "formed to have a grid shape to correspond to the back surface finger lines 170 and the back surface bus electrodes 190." EX1009-Jin, ¶¶88-89 ("The openings 422 of the … mask 420 may be formed not only at positions corresponding to where the rear finger lines 170 are to be formed, but also at positions corresponding to where the rear surface electrodes (190 of FIG. 1) are to be formed…."), Fig. 10.

FIG. 10



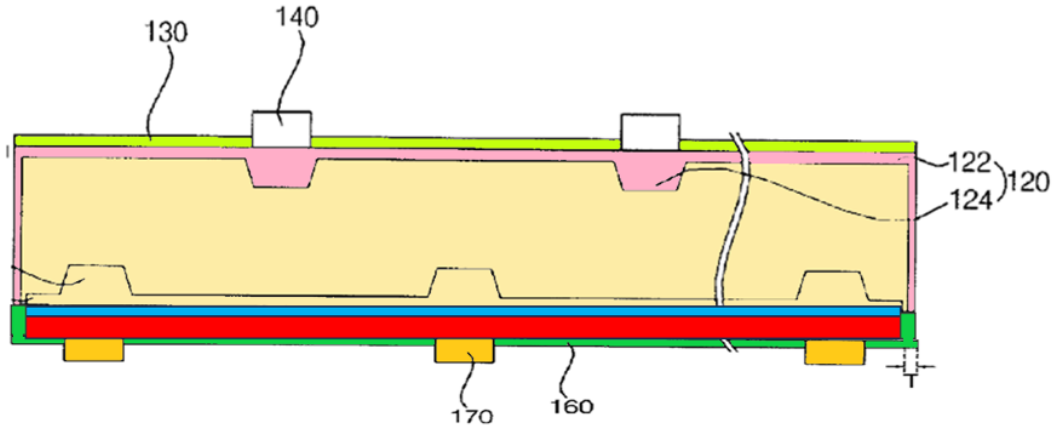
(a)

165. Jin subsequently explains that the "[t]he front finger lines 140, for example, may be formed in such a way that paste for front surface electrodes is screen printed on the area on the substrate 110 where the front finger lines 140 are to be formed by using a mask." EX1009-Jin, ¶99. Jin further explains that "the rear finger lines 170 may be formed in a similar way as the front finger lines 140. *Id*., ¶101. The Skilled Artisan would understand that because the mask pattern 420 includes openings for both the finger electrodes surface bus electrodes, when used to form the rear electrodes, the mask would form both the rear finger lines 170 and rear surface bus electrodes 190 at the same time.

166. As discussed in ¶136 above, the rear finger electrodes 170 (orange) connect to the phosphorous-doped polysilicon layer (red) (which is the "*first conductive type semiconductor region*") through gaps in the second anti-reflection film 160 (green) formed, for example, by screen printing or laser ablation of the

second anti-reflection film. EX1009-Jin, ¶52-53, 99-101, Figs. 3, 11. During screen printing, the heat treatment applied to the paste causes "a fire-through phenomenon in which the printed paste penetrates the first anti-reflection film 130 through use of a glass frit." *Id.* ¶99, 101. Likewise, laser ablation removes portions of the anti-reflection film in the areas where the electrodes are to be deposited. *Id.* ¶¶53, 100. By using the same mask 420 to form the back surface finger lines 170 and the back surface bus electrodes 190, all the back surface finger lines 170 and the back surface bus electrodes 190 would connect through the anti-reflection film 160 (green) to connect to the "P-doped Si layer" (red).

Combination of Jin and Feldmann



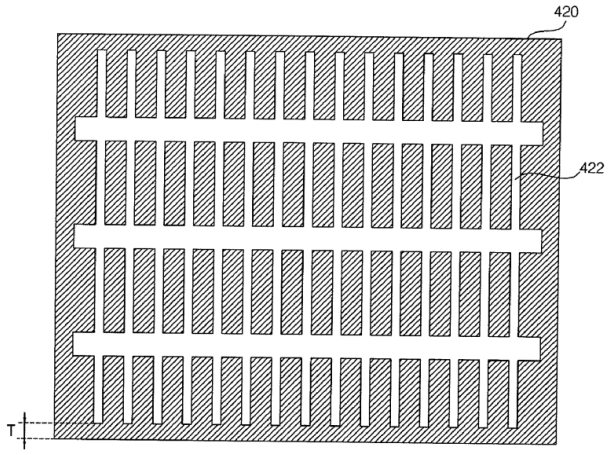
8. Claim 10 – Single Layer Electrodes

167. Claim 10 depends from claim 9, and recites: "*wherein all of the plurality of first finger electrodes and the first bus bar have a single layer or double layer structure*." Jin teaches to use a mask pattern 420 to form both the rear

finger electrodes 170 and rear surface bus electrode 190 at the same time. EX1009-Jin, ¶¶88-89 ("The openings 422 of the … mask 420 may be formed not only at positions corresponding to where the rear finger lines 170 are to be formed, but also at positions corresponding to where the rear surface electrodes (190 of FIG. 1) are to be formed….”), Fig. 10.

168. Jin further explains that the rear finger electrodes 170 can be fabricated by screen printing using a paste comprising Ag (silver). EX1009-Jin, ¶52. Such a process would result in a single layer of silver. EX1022-Luque, 277-78 ("The oxides forming the glass frit melt, enabling silver grains to sinter and form a continuous conductor so that the layer can present low sheet resistance.”). The Skilled Artisan would understand that screen printing using the mask pattern 420 would result in both the rear finger electrodes 170 and rear surface bus electrode 190 having a single layer structure of silver. EX1009-Jin, ¶89.

FIG. 10



(a)

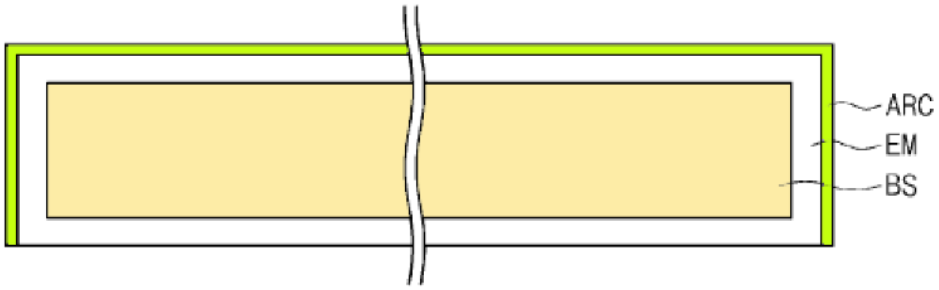
VII. CLAIMS 7 & 8 ARE UNPATENTABLE OVER JIN AND FELDMANN, IN FURTHER VIEW OF SEO

169. Jin discloses a solar cell having a passivation layer over an emitter 120 on the front side of a substrate 110, and an anti-reflection film 160 that "performs the function of a passivation layer" on a back surface field layer 150 on the back side of the substrate 110. EX1009-Jin, ¶¶37, 50, Fig. 3. According to Jin, the passivation film is formed by depositing an oxide film on the emitter 120, and then the anti-reflection film 130 is formed by any of several known methods, including chemical vapor deposition. *Id.*, ¶¶97-98. Chemical vapor deposition (CVD) is a common technique for forming thin films of dielectrics, including silicon oxide. EX1030-Streetman, 162. Although Figure 3 of Jin does not depict the passivation layer or anti-reflection film 160 on the lateral side surfaces of the substrate 110, Jin does not indicate that the lateral sides of the substrate 110 are masked during these processes, or that the passivation layer and anti-reflection film 160 are subsequently removed from the lateral sides of the substrate. Thus, a Skilled Artisan would expect that the chemical vapor deposition technique used by Jin to create these layers would result in their formation on the lateral sides of the substrate. EX1009-Jin, ¶98; EX1015-Seo, 6:39-48, Fig. 1.

170. Seo explicitly illustrates the details of the chemical vapor deposition formation technique taught by Jin. Specifically, Seo teaches a solar cell with a base substrate BS, an emitter layer EM on its front surface, and a back surface field

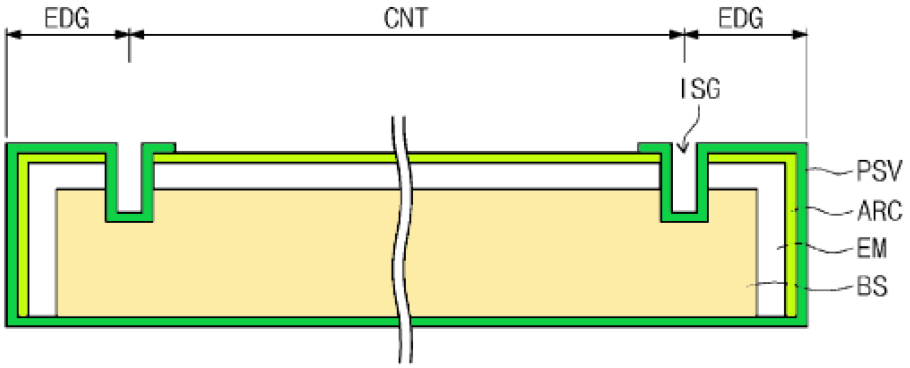
on its rear surface. EX1015-Seo, 3:44-50, 4:11-13, 5:32-35, Fig. 1. As shown in Figure 2C of Seo, after the emitter EM is formed, an "anti-reflection layer ARC is formed directly on the emitter layer EM" using chemical vapor deposition, one of the techniques identified by Jin, resulting in the anti-reflection layer ARC being deposited on the front and lateral sides of the substrate BS. *Id.*, 6:39-48, Fig. 1; EX1009-Jin, ¶98.

Fig. 2C

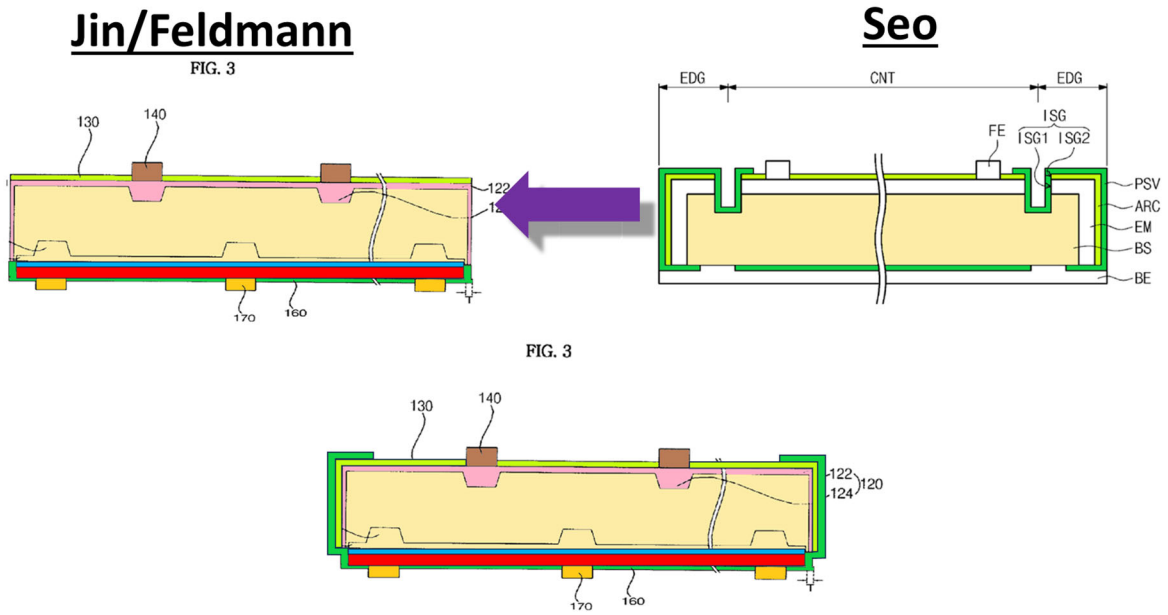


171. Thereafter, "[t]he passivation layer PSV may be formed by depositing at least two of… silicon oxide (SiO_x), silicon nitride (SiN_x), and silicon oxynitride (SiON)," resulting in the passivation layer PSV being deposited on the back and lateral sides of the substrate BS and on top of the previously deposited anti-reflection layer ARC as shown in Figure 2F. EX1015-Seo, 7:60-66. Seo observes that the passivation layer PSV is "in a region corresponding to the edge region EDG and on the side surfaces of the base substrate BS." *Id.*, 4:60-63.

Fig. 2F



172. Thus, Seo discloses the results of Jin's chemical vapor deposition process for depositing the passivation layer and anti-reflection film 130. The proposed combination of Seo with Jin/Feldmann simply applies the structure of Seo's anti-reflection layer ARC and passivation layer PSV formed by CVD (which would have been known to the Skilled Artisan) to Jin's passivation layer and anti-reflection film 160, respectively, deposited using the same technique.



Proposed Combination

A. Motivation to "Modify" Jin and Feldmann with Seo

173. Jin, Feldmann, and Seo are analogous art because each is in the same field of endeavor—solar cell design. EX1009-Jin, Abstract, ¶¶3,7; EX1012-Feldmann, Abstract, 271; EX1015-Seo, Abstract, 1:11-13. Each is reasonably pertinent to the problems of efficiencies of solar cell designs. EX1009-Jin, Abstract, ¶¶6-7; EX1012-Feldmann, Abstract, 271; EX1015-Seo, 7:1-11, 9:21-23, 9:31-34, Fig. 5.

174. The combination of Jin/Feldmann with Seo simply applies the configuration of Seo's ARC and PSV layers to Jin's front passivation layer and rear anti-reflection film 160, respectively. Seo is simply being used to supply details about Jin's passivation layer and anti-reflection film 160 that Jin did not

explicitly disclose. A Skilled Artisan would have been motivated to look to Seo to understand the details not disclosed by Jin regarding Jin's fabrication process because both Jin and Seo disclose the same deposition technique—chemical vapor deposition—for these layers. Moreover, a Skilled Artisan would be motivated to build the combination of Jin/Feldmann such that the passivation layer and anti-reflection film 160 cover the lateral sides of the substrate—as taught by Seo—because eliminating the passivation layer and anti-reflection film 160 from the lateral sides would require either additional process steps to mask the substrate's lateral sides during fabrication of these layers, or additional etching steps to physically remove these layers after their fabrication. Such steps would increase complexity, drive up costs, and increase the risk of manufacturing error. In addition, passivating the lateral sides of the substrate would further reduce edge leakage current caused by surface recombination at the lateral sides of the substrate, resulting in higher open circuit voltage. EX1022-Luque, 313-14 ("Surface passivation of unmetallized regions can be further improved by oxidation."). Surface recombination is lowered by passivation because dielectrics, such as silicon oxides (the passivation material disclosed by Jin), tie up dangling bonds on the surface of the silicon, which act as sources of electron-hole pair recombination. *See* EX1021-Quirk, 227-28. By contrast, eliminating the

passivation layer and anti-reflection film 160 from the lateral sides of the substrate would not result in any benefit to the solar cell.

B. Reasonable Expectation of Success

175. The Skilled Artisan would have considered the Jin/Feldmann and Seo combination to be merely an arrangement of like elements (and their corresponding fabrication steps) with each performing the same function it had been known to perform (the passivation layer and anti-reflection film 160 of Jin, and the anti-reflection layer ARC and passivation layer PSV of Seo, respectively) and yielding no more than what one would expect from such an arrangement (a solar cell made using Jin's manufacturing process having the passivation/anti-reflection film configuration shown in Seo). On the front sun-facing side, Seo's side anti-reflection layer ARC and Jin's passivation layer may both be formed using silicon oxide (SiOx), such that a Skilled Artisan would understand the two layers to be interchangeable and serve equivalent functions. EX1009-Jin, ¶37; EX1015-Seo, 4:45-47. Likewise, on the back side, both Jin's second anti-reflection film 160 and Seo's passivation layer PSV may be formed from silicon oxide (SiOx), silicon nitride (SiNx), or silicon oxynitride (SiON), and "perform[] the function of a passivation layer." EX1009-Jin, ¶50; EX1015-Seo, 5:12-15.

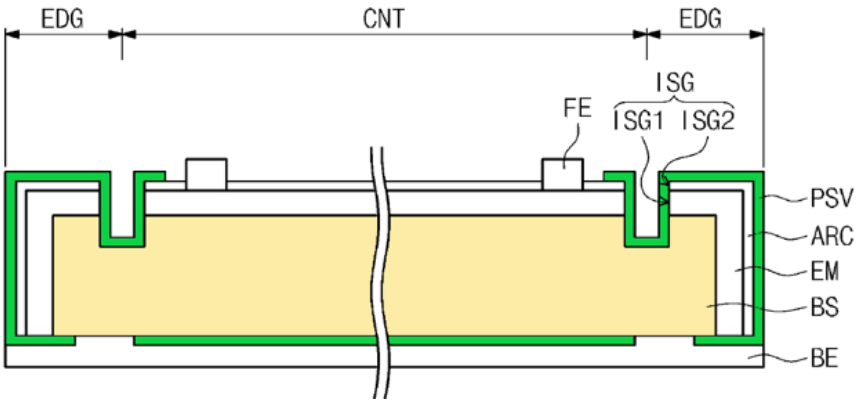
176. Combining Jin/Feldmann and Seo as described here would have been well within the level of ordinary skill in the art. It would not have resulted in any

unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success. The combination would simply require the omission of any additional (and unnecessary) steps in Jin's solar cell manufacturing process to shield or remove anti-reflection/passivation layers from the lateral sides of the substrate, to yield predictable results.

1. Claim 7 – First Passivation on Substrate Sides

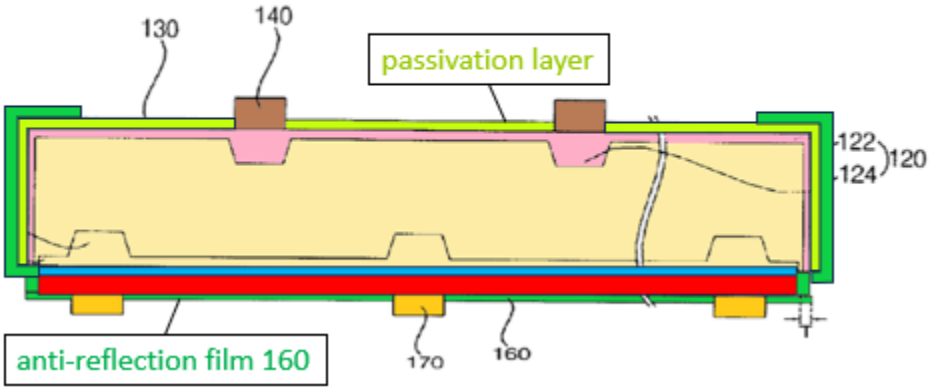
177. Claim 7 depends from claim 1 and recites: "*wherein the first passivation film comprises a side portion extending up a side surface of the semiconductor substrate*." Seo disclosed a passivation layer PSV on the back side and extending up "**<u>on the side surfaces of the base substrate BS</u>**," as shown in dark green in Figure 1 below. EX1015-Seo, 4:60-62, Fig. 1.

Fig. 1



178. As discussed above in ¶¶134-135, Jin's back side anti-reflection film 160 is a "*first passivation film*" as claimed. In the proposed combination, Jin's second anti-reflection film 160 is implemented by chemical vapor deposition (EX1009-Jin, ¶98), the same technique used by Seo, resulting in the layout of Seo's passivation layer PSV, as illustrated in modified Figure 1 of Jin below. *See* ¶¶169-172.

Combination of Jin, Feldmann, and Seo

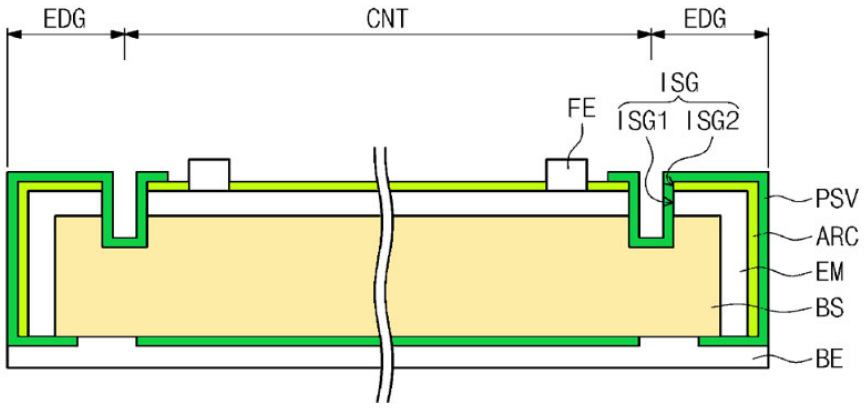


2. Claim 8 – Second Passivation on Substrate Sides

179. Claim 8 depends from claim 7 and recites: "*wherein the second passivation film comprises a side portion formed on the side surface of the semiconductor substrate, and the side portion of the first passivation film on the side surface of the semiconductor substrate is on the side portion of the second passivation film*." Here, the claimed "*second passivation film*" corresponds to the front passivation film, and the claimed "*first passivation film*" corresponds to the back passivation film.

180. Seo discloses an "antireflection layer ARC" (light green) on the front and extending down the lateral sides of the substrate, satisfying the "*second passivation film comprises a side portion formed on the side surface of the semiconductor substrate*" portion of the claim. EX1015-Seo, 4:43-51, 4:60-63. As discussed above in ¶¶177-178 Seo discloses a passivation layer PSV (dark green) on the back side and extending up the lateral sides, corresponding to the claimed *first passivation film.* Seo further discloses that "[t]he passivation layer PSV [*first passivation film*] is on the anti-reflection layer ARC [*second passivation film*] in a region corresponding to the edge region EDG **<u>and on the side surfaces of the base substrate BS</u>**." *Id.*, 4:60-63, Fig. 1.

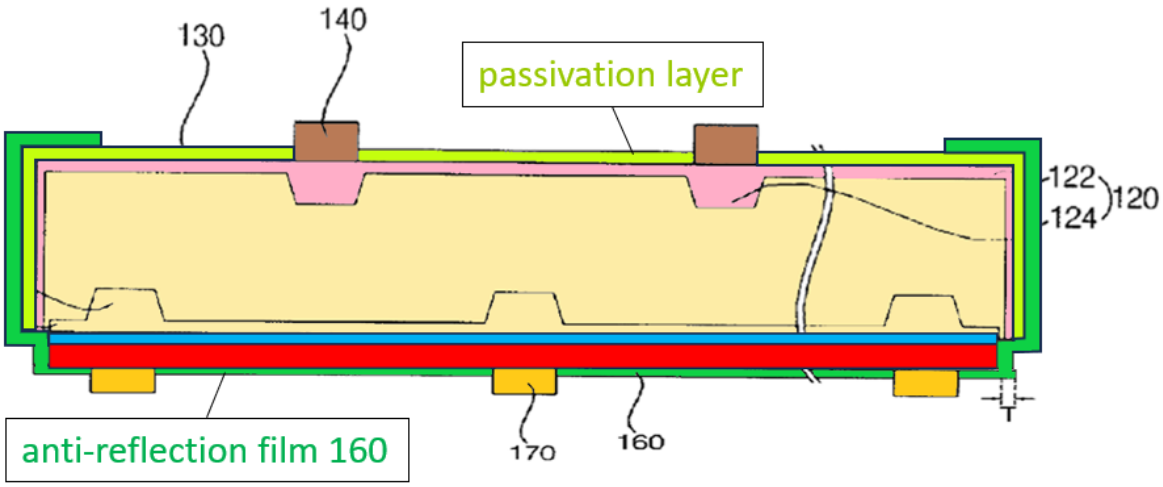
Fig. 1



181. As discussed above in ¶¶139-140, Jin likewise discloses a passivation layer on the emitter layer 120 that corresponds to the claimed "*second passivation film.*" Moreover, Seo discloses that the antireflection layer ARC may be made of

"silicon oxide," the same material as Jin's passivation layer. EX1015-Seo, 4:45-47; EX1009-Jin, ¶37. A Skilled Artisan would therefore understand that Seo's antireflection layer ARC functions as a passivation layer as taught by Jin. In the proposed combination, Jin's passivation layer is implemented using the layout of Seo's anti-reflection layer ARC (light green) in the modified Figure 1 of Jin below. *See* ¶¶169-172. Moreover, a Skilled Artisan would understand the benefit to forming Jin's front passivation layer first, *then* the rear anti-reflection film 160, as Seo teaches, because the front sun-facing surface is the most important surface for efficient operation of the solar cell for converting solar radiation into electrical current. Most photons will be absorbed and converted into electron-hole pairs formed via the light-incident surface. Damage to the emitter layer during manufacturing therefore results in defects that have an inordinate negative impact on the operation of the cell. Accordingly, manufacturers generally first passivate the front surface of the cell to provide a protective barrier for the front emitter layer, before flipping the substrate over to form the rear passivation layer.

Combination of Jin, Feldmann, and Seo



VIII. CLAIM 11 IS UNPATENTABLE OVER JIN AND FELDMANN, IN FURTHER VIEW OF WATABE

182. The bifacial solar cell of Jin/Feldmann in combination with the single layer copper finger and dual layer copper/silver bus bar electrodes of Watabe would have rendered Claim 11 obvious and unpatentable. The combination would have been nothing more than replacing the screen printed silver finger and bus electrodes of Jin with the screen printed copper finger electrodes and screen printed copper and silver bus electrodes as disclosed in Watabe. EX1009-Jin, ¶¶52, 88-89; EX1014-Watabe, ¶¶16-17, 28-29. The resulting solar cell would meet all limitations of Claim 11.

A. Motivation to Modify Jin/Feldmann with Watabe

183. Jin, Feldmann, and Watabe are analogous art because each is in the same field of endeavor, solar cell design, and each is reasonably pertinent to

improvements in solar cell designs. EX1009-Jin, Abstract, ¶3; EX1012-Feldmann, Abstract, 271; EX1014-Watabe, Abstract, ¶1.

184. Jin discloses that both the rear finger 170 and rear surface bus electrodes 190 can be made by screen printing using silver paste, resulting in a single layer of silver. EX1009-Jin, ¶52. Watabe similarly discloses that its finger and bus electrodes can be made by screen printing. EX1014-Watabe, ¶28. To reduce cost, Watabe discloses a dual layer bus bar structure "in which the first electrode layer that is bonded directly to the substrate is formed with a copper paste and the uppermost electrode that is bonded to the connecting wiring is formed with a silver paste." *Id.*, ¶9. Watabe explains that copper has high electrical conductivity and is inexpensive when compared to silver. *Id.*, ¶3. However, copper has "poor solder wettability compared to that of silver" and therefore connecting solar cells together by soldering to copper bus bar electrodes increases the risk of a degraded solder connection, compromising reliability. *Id.*, ¶4. Thus, Watabe discloses the double layer bus bar structure, which does not impair performance and provides a reduction in cost. *Id.*, ¶9.

185. The Skilled Artisan reviewing Jin would have been motivated to replace the rear screen printed silver finger 170 and bus electrodes 190 of Jin with the screen printed copper finger and copper/silver bus electrodes of Watabe to provide for "a significant reduction in solar cell production costs without

compromising solar cell performance and while maintaining the reliability of soldering to the wiring." EX1014-Watabe, ¶14. Watabe discloses that the finger and bus bar structure is formed "on at least one side of the semiconductor substrate" and thus contemplates that the invention could be used on both sides of a bi-facial solar cell. *Id.*, ¶9. In the combination, the solar cell of Jin/Feldmann would continue to function as before, but with the benefit of lower cost. *Id.*, ¶14.

B. <u>Reasonable Expectation of Success</u>

186. The Skilled Artisan would have considered the Jin/Feldmann/Watabe combination to be merely an arrangement of old elements (and their corresponding fabrication steps) with each performing the same function it had been known to perform, with the screen printed silver fingers and bus bar of Jin replaced by the screen printed copper fingers and copper/silver bus bar of Watabe.

187. Combining Jin/Feldmann/Watabe as described here would have been well within the level of ordinary skill in the art. It would not have resulted in any unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success. The combination would simply have been the combination of well-known prior art steps in solar cell and semiconductor fabrication to yield predictable results. Likewise, substituting Jin's screen printed silver rear surface electrode with the screen printed copper finger and copper/silver bus bar electrodes of Watabe would have been a simple

substitution of one known element and corresponding fabrication step for another to obtain predictable results.

1. Claim 11 – Single Layer Finger, Dual Layer Bus Bar Electrodes

188. Claim 11 depends from claim 9 and recites: "*wherein: the plurality of first finger electrodes have a single layer structure, and the first bus bar has a double layer structure*." Jin discloses that the rear finger electrodes 170 and the rear bus electrodes 190 can be fabricated by screen printing using a paste comprising silver. EX1009-Jin, ¶52, 89.

189. Watabe likewise discloses screen printing to form the finger and bus electrodes. However, to decrease costs, Watabe screen prints the finger electrodes using a copper paste. EX1014-Watabe, ¶9 ("the finger electrode is composed of a printed and fired conductive paste containing copper or copper compound fine particles"). To maintain solderability and adhesive strength to the wiring between cells, Watabe discloses screen printing the bus electrodes first with copper and then with silver. *Id.*, ¶¶12, 28. Specifically Watabe states "[p]referably, at least the bus-bar electrode has a multilayer structure with two or more layers." *Id.*, ¶12. Watabe's screen printed copper finger corresponds to the claimed "the plurality of first finger electrodes have a single layer structure" while Watabe's screen printed copper/silver bus electrodes correspond to the claimed "*the first bus bar has a double layer structure*." Applying Watabe's teaching to the solar cell of

Jin/Feldmann would result in solar cell with finger electrodes "*hav[ing] a single layer structure*" and copper/silver bus electrodes "*ha[ving] a double layer structure.*"

IX. CLAIMS 1-6 AND 9-10 ARE UNPATENTABLE OVER CHANG AND JIN

190. The combination Chang and Jin would have rendered Claims 1-6 and 9-10 obvious and unpatentable.

191. Chang disclosed a solar cell having an isolation region on the backside of the substrate in which the tunnel oxide ("tunneling layer 44") and "back surface field area" (BSF) 30 are not formed at the periphery or edge of the substrate. EX1013-Chang, ¶¶56, 62.

192. During prosecution of the 419 Patent, the Examiner noted that Chang did not disclose "the claimed features of the removing step as recited and the first passivation film covering the first surface of the semiconductor substrate along with the isolation portion." EX1006, 254. The claims of the 419 Patent were method claims that, as amended by the Examiner, included a "removing step of removing the tunnel layer and the first conductive type semiconductor region" to form the isolation portion. *Id.*, 264. Here, the claims of the challenged 104 Patent do not include any such step of "removing" deposited tunnel or polysilicon layer to form the isolation portion on the back surface of the solar cell. Rather, the challenged claims only require the existence of the isolation portion.

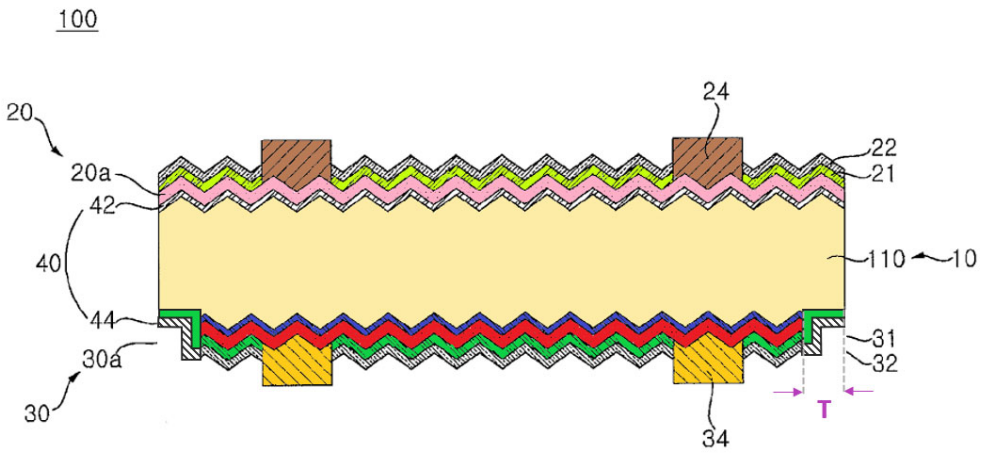
193. With respect to the Examiner's assertion that Chang did not disclose "the first passivation film covering the first surface of the semiconductor substrate along with the isolation portion," the Examiner is partially correct in that Chang's Fig. 1 shows that the rear passivation film (second passivation film) 31 covers the entirety of the rear conductive type area (back surface field area) 30 and the rear tunnel layer (second tunnelling layer) 44. However, the Examiner did not appreciate that Chang's specification specifically states that the "second tunneling layer 44" and the "back surface field area 30" (both formed on the back surface of the substrate) may be "entirely formed" over the back surface of the substrate. Chang provided a special definition of "entirely formed" to mean "that an element such as a layer is formed over an entire surface without an empty area or a non-coverage area, or is ***formed in an entire area excluding pre-designated or inevitably formed regions such as periphery region, isolation region, or the like***." EX1013-Chang, ¶¶56, 62. That is, Chang discloses an isolation region at the periphery of the substrate that excludes the tunnel oxide and polysilicon layers.

194. Chang further discloses that the second passivation film 31 "may be formed in a substantially entire region over the front surface of the back surface field area 30, excluding a region corresponding to the second electrode 34." EX1013-Chang, ¶63. Notably, when referring to the second passivation film 31, Chang does not use the specially defined term "entirely formed" but instead

describes the passivation film 31 as being formed "in a substantially entire region" excluding only the regions corresponding to the rear electrodes (second electrode 34). Nevertheless, to improve upon the bifacial solar cell of Chang, the Skilled Artisan would have looked to Jin to understand details of Chang's isolation region, including the formation of the passivation layer over the isolation region, to the extent not expressly disclosed in Chang.

195. Jin also disclosed a bifacial solar cell with an isolation region. In particular, Jin taught that the back surface field of the solar cell is formed separated from the edge of the substrate by a "gap" or distance T. EX1009-Jin, ¶57, Fig. 3. The purpose of the gap T is to isolate the back surface field from the emitter layer on the front side to prevent electrical short-circuiting. EX1009-Jin, ¶¶57-58. Jin's anti-reflection/passivation layer 160 also covers the gap T and the substrate together, as seen in Figure 3.

196. Jin thus provides details about Chang's isolation region that are not expressly disclosed by Chang. In the proposed combination, Chang's isolation portion would be implemented using Jin's teaching to separate Chang's second tunneling layer 44 (blue) and back field surface area 30 (red) from the edge of the substrate by a gap T, and covered by the passivation layer/anti-reflection layer, as depicted in the modified Chang Figure 1 below.



A. <u>Motivation to "Modify" Chang with Jin</u>

197. Chang and Jin are analogous art because each is in the same field of endeavor—solar cell design. EX1013-Chang, Abstract, ¶¶3, 9; EX1009-Jin, Abstract, ¶¶3,7. Each is reasonably pertinent to the problems of efficiencies of solar cell designs. EX1013-Chang, ¶¶7-8, 10-11; EX1009-Jin, Abstract, ¶¶6-7. Further, both Chang and Jin were originally assigned to LG Electronics Inc. EX1013-Chang, face; EX1009-Jin, face.

198. The combination of Chang and Jin asserted here requires no modification to Chang's device; Jin is being used to supply details about Chang's isolation region that Chang presumed was already known. A Skilled Artisan would have been motivated to look to Jin to understand the details missing from Chang regarding Chang's isolation region, because others taught and understood that the isolation region was an important tool for preventing the emitter and back surface field from being shorted.

199. Chang mentions the "isolation region" four times, explaining that the tunneling layer, emitter, and back side field are **not** formed in the isolation region. EX1013-Chang, ¶¶45, 51, 56, 62. A Skilled Artisan would have understood to look to other, similar references, such as Jin, to ascertain more information regarding Chang's isolation region. EX1009-Jin, ¶¶57-60. Furthermore, it was well known that isolating the emitter and back surface field was beneficial to the proper functioning of solar cells.

200. As early as 2007, Kray had observed that "[a]n interesting option is the performance of edge isolation on the rear side of the cell because this prevents the damaging of the front side emitter where most of the photogeneration takes place." EX1026-Kray, §1. Both Chang and Jin likewise teach backside isolation regions. *See* ¶¶75-81, 91-96 above.

201. A Skilled Artisan reviewing Chang would therefore understand the importance of implementing the isolation region in Chang's device, and would therefore be motivated to look to other references, such as Jin (which was assigned to the same original assignee as Chang, LG Electronics, EX1009-Jin, face; EX1013-Chang, face) to understand details regarding Chang's isolation region.

B. Reasonable Expectation of Success

202. The Skilled Artisan would have considered the Chang/Jin combination to be merely an arrangement of old elements (and their corresponding

fabrication steps) with each performing the same function it had been known to perform (the solar cell of Chang having an isolation region at the periphery, made using the details of the isolation and "gap T" spacing disclosed by Jin) and yielding no more than what one would expect from such an arrangement (a solar cell with improved performance). Specifically, the Skilled Artisan would use the mask shown in Fig. 9 of Jin to form the second tunneling layer 44 and back surface field area 30 of Chang, thereby creating the gap T isolation region at the periphery between the back surface field and the edge of the substrate. The Skilled Artisan would have been aware of numerous routine techniques for making the Chang/Jin solar cell.

203. For example, Jin discloses the use of a mask in Figure 9 that would be used to cover the periphery or edge portion of the back surface of the substrate. Such masking technique, known as shadow masking was well known to the Skilled Artisan. The Skilled Artisan would know that reusable metal "shadow masks" have been used in the masking and forming of layers in solar cells. For example, Scherff discloses a reusable metal mask used for structuring the emitter and back surface field regions of an interdigitated back contact solar cell. EX1031-Scherff, Abstract. Scherff discloses that various layers can be deposited and plasma etched through openings in the mask. *Id*., §2.

204. The metal shadow mask, in a shape or form as shown in Fig. 9 of Jin, would be placed on the substrate to cover the periphery of the surface of the substrate before depositing the second tunneling layer 44 and back surface field (conductive type) area 30 of Chang. Chang discloses that the tunneling layer may be formed by "deposition (for example, plasma-enhanced chemical vapor deposition chemical (PECVD), atomic layer deposition (ALD)) or the like" and that the conductive type areas "may be formed of an amorphous, microcrystalline, or polycrystalline semiconductor" and may be formed by "deposition (for example, plasma enhanced chemical vapor deposition chemical (PECVD)) or the like."). EX1013-Chang ¶146. The Skilled Artisan would be aware that these techniques could be used to deposit the second tunneling layer 44 and back surface field (conductive type) area 30 in the area not covered by the metal mask. EX1031-Scherff §2.1 (disclosing PECVD deposition through openings in a mask). Since the metal mask is not chemically bonded to the wafer, it can simply be lifted off the substrate after formation of the tunneling layer and back surface field. And the second tunneling layer 44 and back surface field) area 30 would not have been formed (and thus excluded) in the area covered by the mask as disclosed in Chang. EX1013-Chang ¶¶56, 62 (second tunneling layer 44 and back surface field area 30 are "formed in an entire area excluding pre-designated or inevitably formed regions such as periphery region, isolation region or the like.").

205. As a second example, when forming the back surface field, the Skilled Artisan would use a silicon nitride mask around the periphery of the substrate. In this example, the Skilled Artisan would first deposit a silicon nitride (SiNx) layer on the entire back of the substrate and use the mask shown in Fig. 9 of Jin to protect the silicon nitride along the periphery of the back of the substrate while etching out the center portion of the silicon nitride layer. Etching of the silicon nitride could be performed using, for example, a dry etch. The remaining silicon nitride would form a mask over the periphery of the back of the substrate. The Skilled Artisan could then use Chang's thermal growth, for example, reacting oxygen with silicon to form the second tunneling layer 44, followed by Chang's thermal growth, for example, thermal low pressure chemical vapor deposition (LPCVD) to form the back surface field (conductive type) area 30. EX1013-Chang, ¶146. Afterwards, the Skilled Artisan can use a chemical wet etch to etch out the silicon nitride mask and then mechanically remove the portion of the polysilicon back surface field area that was deposited over the silicon nitride mask. Thus, the second tunneling layer 44 and back surface field area 30 would have been excluded in the isolation region. *Id.*, ¶¶56, 62.

206. As a third example, instead of using the silicon nitride mask for both the tunneling layer and BSF, after growth of the tunneling layer 44 in the second example above, the silicon nitride mask could also be removed by selective etching

before the deposition of the polysilicon back surface field area 30. A metal shadow mask as described above, could be placed over the substrate and the Skilled Artisan could then deposit Chang's back surface field area 30 using, "for example, plasma-enhanced chemical vapor deposition (PECVD) or the like" through the opening in the metal mask. EX1013-Chang, ¶146. The metal mask could then be lifted off after deposition of the back surface field area, instead of having to perform a wet chemical etching and mechanical removing of the polysilicon back surface field in the isolation region, leaving the tunneling layer 44 and BSF 30 only in the areas not covered by the masks.

207. As a fourth example, and another alternative to using the silicon nitride mask for both the second tunneling layer 44 and back surface field area 30, the Skilled Artisan could have chosen to remove the silicon nitride mask after growing the thermal oxide tunneling layer. The polysilicon back surface field area 30 could then be deposited over the entire back side of the substrate. A mask, such as the reverse of the mask shown in Fig. 9 of Jin, could be used to protect the polysilicon back surface field 30 over the tunneling layer 44 while the remaining polysilicon in the edge portion or the periphery of the back of the substrate is removed by using a wet etch or a plasma etch to form Chang's isolation region.

208. As a fifth example, the Skilled Artisan would form the tunnelling layer 44, "for example, by a method such as thermal growth or deposition (for

example, plasma-enhanced chemical vapor deposition chemical (PECVD), atomic layer deposition (ALD)) or the like" along with one of Chang's techniques for forming the polysilicon conductive type layer 30 "for example, thermal growth, deposition (for example, plasma enhanced chemical vapor deposition chemical (PECVD)) or the like." EX1013-Chang ¶146. The Skilled Artisan could then use a mask, such as the reverse of the mask shown in Fig. 9 of Jin (i.e., a mask smaller than the substrate) to protect the polysilicon back surface field over the tunneling layer in the center. The remaining polysilicon back surface field and tunnel oxide in the edge portion or the periphery of the back of the substrate can then be removed using an etch, such as a wet etch.

209. In short, there are many ways known to the Skilled Artisan to form the isolation area in the combined Chang/Jin solar cell. And after the formation of Chang's TOPCon structure, the Skilled Artisan would continue with Chang's steps of forming the front and back side passivation/anti-reflection layers and the metal electrodes.

210. Combining Chang and Jin as described here would have been well within the level of ordinary skill in the art. It would not have resulted in any unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success. *Id*. The combination would simply have been the combination of well-known prior art

steps in solar cell and semiconductor fabrication to yield predictable results. *Id*. Likewise, implementing Chang's isolation region as taught by Jin would have been a simple use of a known technique to improve similar devices (Chang's solar cell) in the same way. It is nothing more than applying a known technique to a known device ready for improvement to yield predictable results. *Id*.

C. Chang and Jin Disclosed All Claimed Limitations

1. Claim 1

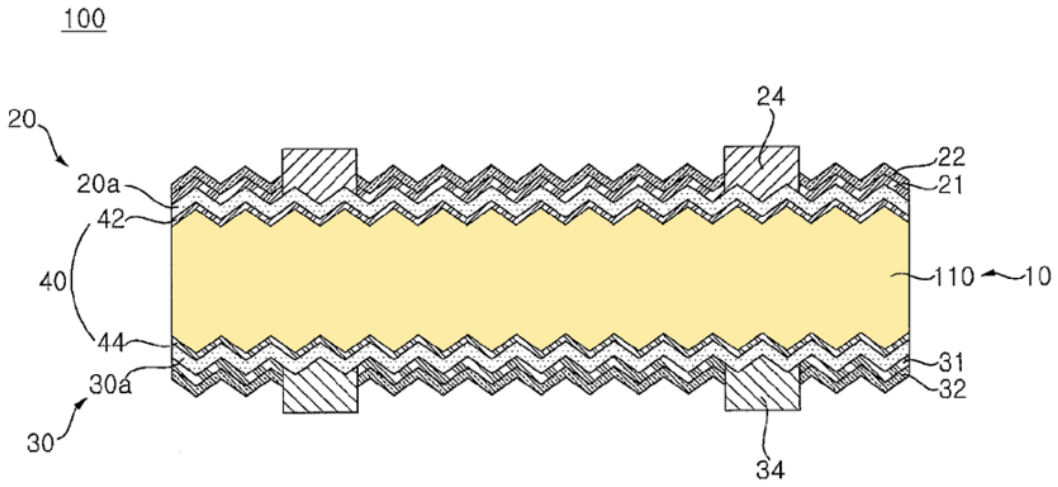
a) [1.a] Preamble

211. Chang and Jin both disclose "*a solar cell,*" as shown by the remaining elements. *E.g.*, EX1013-Chang, Abstract, ¶¶3, 35, Figs. 1, 2; EX1009-Jin, Abstract, ¶3, Figs. 1, 3.

b) [1.b] Semiconductor Substrate

212. Claim 1 first recites: "*a semiconductor substrate*." Chang discloses this element. Chang's Figure 1 shows a solar cell with a silicon "semiconductor substrate 10" including a base area 110 (yellow). EX1013-Chang, ¶38, Fig. 1. The base area 110 has "a relatively low doping concentration of a first conductive type dopant," such as "an n-type impurity". EX1009-Jin, ¶¶38-40. Chang describes the base area 110 as being composed of "a semiconductor silicon wafer." *Id*.

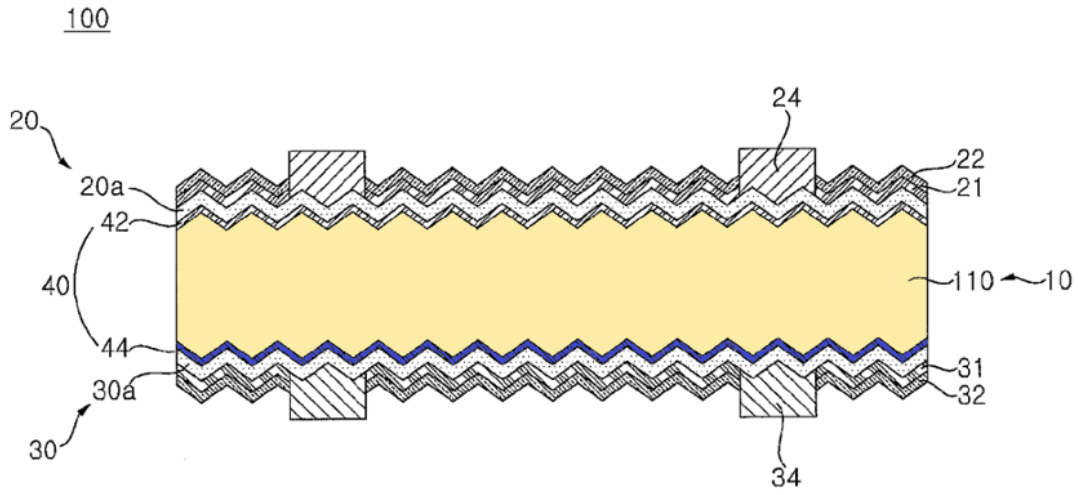
FIG. 1



c) [1.c] Tunnel Layer

213. Claim 1 next recites: "*a tunnel layer on a first surface of the semiconductor substrate.*" Chang discloses this element. The solar cell in Chang's Figure 1 has a "tunneling layer 44" (blue below) formed over the back surface of the substrate 10. EX1013-Chang, ¶¶56, 60, Fig. 1. Chang describes that this "tunneling layer 44" may be an oxide such as silicon oxide. EX1013-Chang, ¶58. In this context, the back surface is the "*first surface*" of Claim 1.

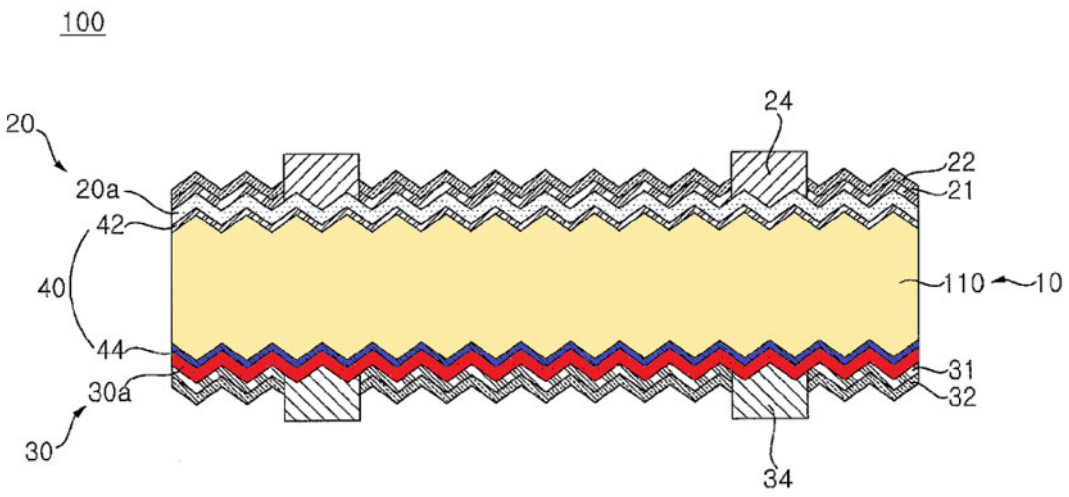
FIG. 1



d) [1.d] First Conductive Type Semiconductor Region

214. Claim 1 next recites: "*a first conductive type semiconductor region on the tunnel layer and containing impurities of a first conductive type*." Chang discloses this element. Chang's Figure 1 shows a "back surface field area 30" (red) being a layer on the "tunneling layer 44" on the back surface of the substrate 10. EX1013-Chang, ¶¶61-62, Fig. 1. Chang discloses that "the back surface field area 30 may include [] polycrystalline silicon," which is synonymous with polysilicon. EX1013-Chang, ¶61. Chang also discloses that the back surface field area 30 "can be easily manufactured by various methods" as a polycrystalline "semiconductor." EX1013-Chang, ¶61.

FIG. 1



215. Moreover, Chang teaches that "the back surface field area 30… ha[s] the same conductive type (for example, p-type or n-type) as the semiconductor substrate 10." EX1013-Chang, ¶61. Thus, Chang's polysilicon back surface field layer also has "*impurities of a first conductive type*," *e.g.,* n-type impurities. .

e) [1.e] Second Conductive Type Semiconductor Region

216. Claim 1 next recites: "*a second conductive type semiconductor region on a second surface opposite to the first surface of the semiconductor substrate and containing impurities of a second conductive type opposite to the first conductive type*." Chang discloses this element. Chang's Figure 1 shows an "emitter area 20" (pink) ("*a second conductive type semiconductor region*") at the

front "second surface" of the substrate 10, opposite to the back "first surface" where the "tunneling layer 44" is located. EX1013-Chang, ¶¶36-37, Fig. 1. The emitter area 20 may be formed of "a polycrystalline, amorphous, or microcrystalline semiconductor." EX1013-Chang, ¶50. Chang discloses that when the base area 110 or substrate 10 is an n-type semiconductor, "the emitter area 20 forming a pn junction with the base area 110 is p-type." *Id.*,EX1013-Chang, ¶¶40, 50 ("emitter area 20 … having a different conductive type… from the semiconductor substrate 10"). Thus, Chang's doping of the "emitter area 20" satisfies the requirement of "*containing impurities of a second conductive type [p-type] opposite to the first conductive type [n-type]*."

217. To the extent Trina contends that the "emitter area 20" in Figure 1 does not satisfy the "on a second surface" limitation because there exists the intervening tunnel layer 42, the Skilled Artisan would find it obvious to alternatively use the "emitter area 20" of Chang's Fig. 8. Specifically, Fig. 8 is an alternative embodiment to Figure 1, having the exact same back side layers as Fig. 1. EX1013-Chang, ¶101 ("a previous process may be used on the back surface"). The back side layers are even denoted with the same numerical identifiers. The only difference is the front side layers. Instead of having a polysilicon layer on the front (second) surface as in Figure 1, the "emitter area 20" in Figure 8 is formed by thermal diffusion of dopants into the substrate 10, in the same way as described for

forming the emitter region of the 104 Patent. Compare EX1013-Chang, ¶98 ("Referring to FIG. 8, … the emitter area 20 includes a second portion 20b including a doping area formed in the semiconductor substrate 10….. The emitter area 20 may be formed by … for example, thermal diffusion …."); EX1001 at 10:21-25 ("the second conductive type semiconductor region 120 forming the emitter region is placed on the front surface side of the semiconductor substrate 100"), 32:6-16 ("the second conductive type semiconductor region 120 may be formed by a thermal diffusion method.").

FIG. 1

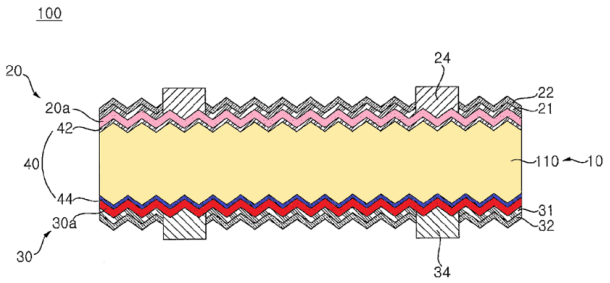
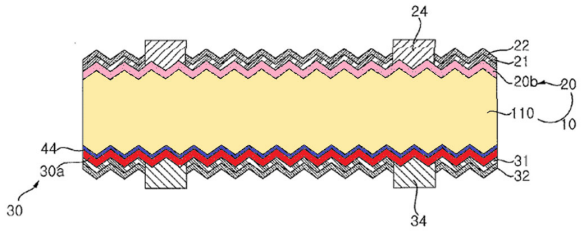


FIG. 8



218. The "emitter area 20" in FIG. 8 also has "*impurities of a second conductive type [p-type] opposite to the first conductive type [n-type]*" because Chang describes the "the emitter area 20 [is] formed by doping the semiconductor substrate 10 with a dopant having a conductive type different from the semiconductor substrate 10." EX1013-Chang, ¶98. Thus, either Chang's Figure 1 or Figure 8 solar cell embodiment would satisfy the "second conductive type semiconductor region" limitation of Claim 1.

f) [1.f] First Passivation Film

219. Claim 1 next recites: "*a first passivation film on the first conductive type semiconductor region*." Chang discloses this element. As seen in Figure 1 or Figure 8, a passivation film 31 (green) is on the back surface field layer 30 (red) ("*first conductive type semiconductor region*"). EX1013-Chang, ¶63 ("passivation film 31 is formed on the back surface field area 30"), Fig. 1. The passivation film 31 "passivates defects present in the back surface field area 30." *Id.*, ¶¶64-65.

FIG. 1

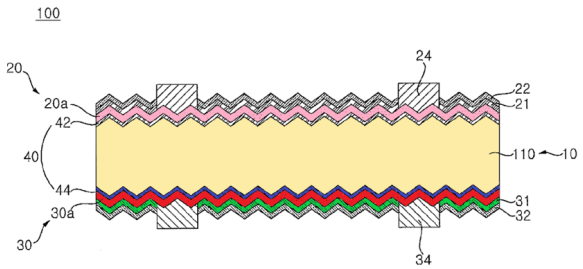
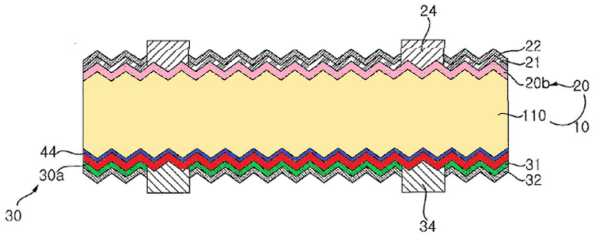


FIG. 8



g) [1.g] First Electrode

220. Claim 1 next recites: "*a first electrode formed on the first passivation film and connected to the first conductive type semiconductor region through an opening formed in the first passivation film*." Chang discloses this element. As seen in Figure 1 and Figure 8, "electrode 34" (orange) is formed on the passivation film 31 and "is electrically connected to the back surface field area 30 [*first conductive type semiconductor region*] via an opening formed in the second passivation film 31." EX1013-Chang, ¶¶67, 36, Figs. 1, 8. According to Chang,

electrode 34 may comprise finger electrodes 34a that "pass through the second passivation film 31" and bus bar electrodes 34b "formed on the second passivation film 31." EX1013-Chang, ¶70.

FIG. 1

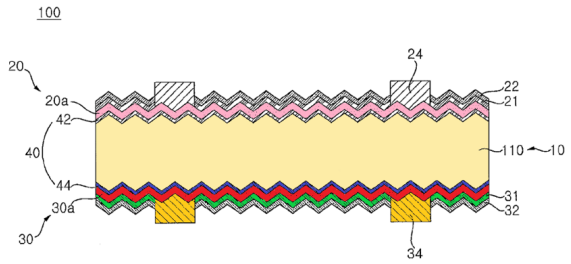
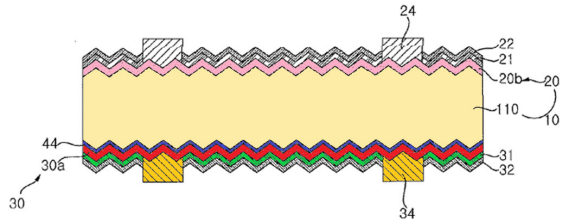


FIG. 8



h) [1.h] Second Passivation Film

221. Claim 1 next recites: "*a second passivation film on the second conductive type semiconductor region*." Chang discloses this element. As seen from Figure 1, a "passivation film 21" (light green) is "formed on the emitter area 20 (more specifically, a first portion 20a)." EX1013-Chang, ¶¶51, 36, Fig. 1; The "passivation film 21 passivates defects present in the emitter area 20." *Id.*, ¶52. Likewise, as seen in Fig. 8, the "passivation film 21 … may be formed on the emitter area 20." *Id.*, ¶100.

FIG. 1

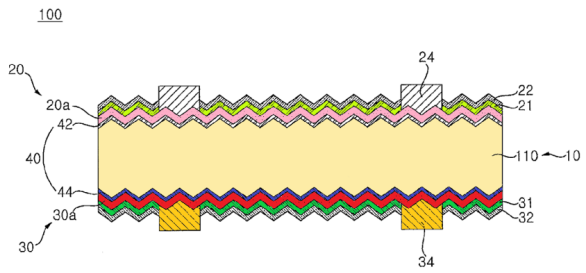
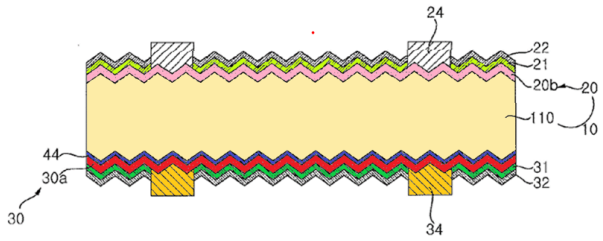


FIG. 8



i) [1.i] Second Electrode

222. Claim 1 next recites: "*a second electrode formed on the second passivation film and connected to the second conductive type semiconductor region through an opening formed in the second passivation film*." Chang discloses this element. As seen from Fig. 1, "electrode 24" (brown) is formed on the front passivation film 21 and "is electrically connected to the emitter area 20 via an opening formed in the [] passivation film 21." EX1013-Chang, ¶¶55, 36, Fig. 1. Likewise, Figure 8 shows the same electrode 24 being electrically connected to the emitter area 20. According to Chang, electrode 24 may comprise finger electrodes 24a that "pass through the first passivation film 21" and bus bar electrodes 24b "formed on the first passivation film 21." EX1013-Chang, ¶70.

FIG. 1

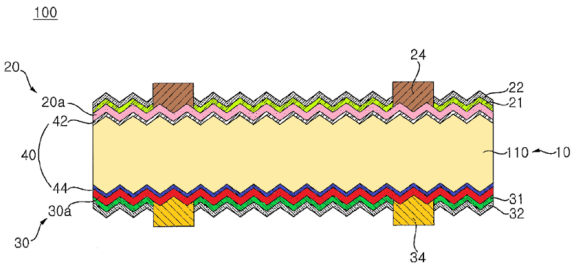
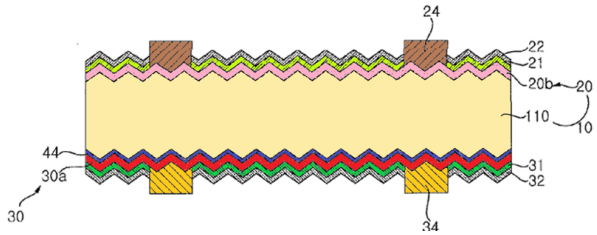


FIG. 8



j) [1.j] Isolation Portion

223. Claim 1 next recites: "*an isolation portion for preventing a contact between the first conductive type semiconductor region and the second conductive type semiconductor region, wherein the isolation portion excludes the tunnel layer and the first conductive type semiconductor region, and is in an edge portion of the first surface of the semiconductor substrate*." Chang discloses this element. First, Chang discloses an "isolation region" (synonymous to "isolation portion") that excludes the "tunneling layer 44" and "back surface field area 30" ("*first conductive type semiconductor region*"). EX1013-Chang, ¶¶56, 62. In particular, Chang discloses that the "tunneling layer 44 is entirely formed over" the back surface of the substrate 10, and the back surface field area 30 "may be entirely formed over the second tunneling layer." *Id*. However, Chang especially defined "entirely formed" in its specification to include an embodiment with less than completely formed layers over the substrate surface. As Chang explains:

> As used herein, the expression "entirely formed" means that an element such as a layer is formed over an entire surface without an empty area

> or a non-coverage area, or *is formed over in an entire area* ***excluding*** *pre-designated or inevitably formed regions such as* ***periphery region****,* ***isolation region*** *or the like*.

Id. (emphasis added). In other words, by especially defining the phrase "entirely formed" as quoted above, Chang taught an embodiment with an isolation region where the tunneling layer 44 and back surface field area 30 are not formed, and therefore excluded, at the back surface of the substrate.

224. Second, to a Skilled Artisan in this field, "isolation" means the introduction of a non-conductive separation, which can either be physical, electrical, or both, between two electrical or conductive components in order to prevent them from inadvertently cross-talking. For example, in a 2009 textbook I co-authored, we described the need to place layers of SiO2, an insulator, around MOSFETs in a semiconductor to "provide critical electrical isolation" between neighboring transistors. EX1030-Streetman, 270. We referred to the SiO2 layers as "isolation or field regions." *Id*. Further, the concept of isolation or edge isolation was well known in the solar cell art to prevent shorting of the front emitter and back surface field. For example, U.S. Patent Publication No. 2012/0003781 issued to Yun on January 5, 2012, disclosed a groove penetrating through a "second conductive type semiconductor layer" to isolate the front from the rear surface of the cell:

> In order to form the n-type emitter layer 320, **since the doping material is doped on the edge portion** of the silicon substrate 310 in a process

> of doping the n-type material, **the front and rear surfaces of the silicon substrate 310 are electrically connected** to each other, which may be a cause of **reducing the efficiency** of the solar cell. Therefore, the **edge isolation** process should be performed without exception in order to isolate the front and rear surfaces or the upper and lower surfaces of the silicon substrate 310.

EX1036, ¶¶9, 66, Fig. 4. Yun refers to this isolating groove as an "edge isolation region." *Id*. ¶10.

225. Thus, by Chang's reference to an "isolation region," the Skilled Artisan would understand that this region electrically isolates, and thus prevents contact between, the conductive front emitter area 20 from the conductive back surface field 30.

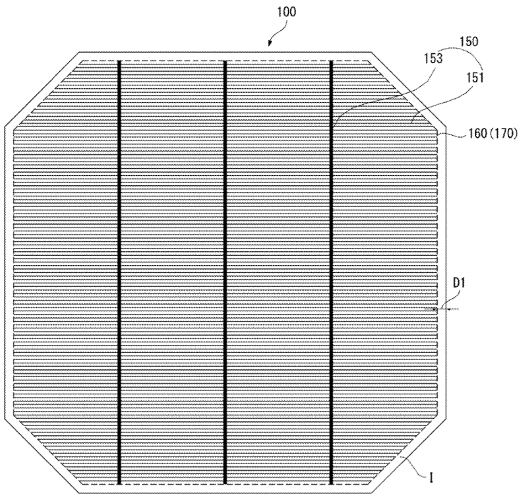
226. In Chang's solar cell, when the tunneling layer 44 and back surface field 30 are not formed in a certain portion or region of the back surface, i.e., the isolation region, it leaves a physical gap. And this physical gap prevents the conductive front emitter area 20 from contacting the conductive back surface field 30.

227. Third, Chang specifically refers to the "periphery region," which denotes the location where the solar cell excludes the formation of the tunneling layer 44 and back surface field area 30, i.e., the location of the "isolation region." EX1013-Chang, ¶¶56, 62. Webster Dictionary defines "periphery" as "the perimeter of a circle or other close curve, also: the perimeter of a polygon."

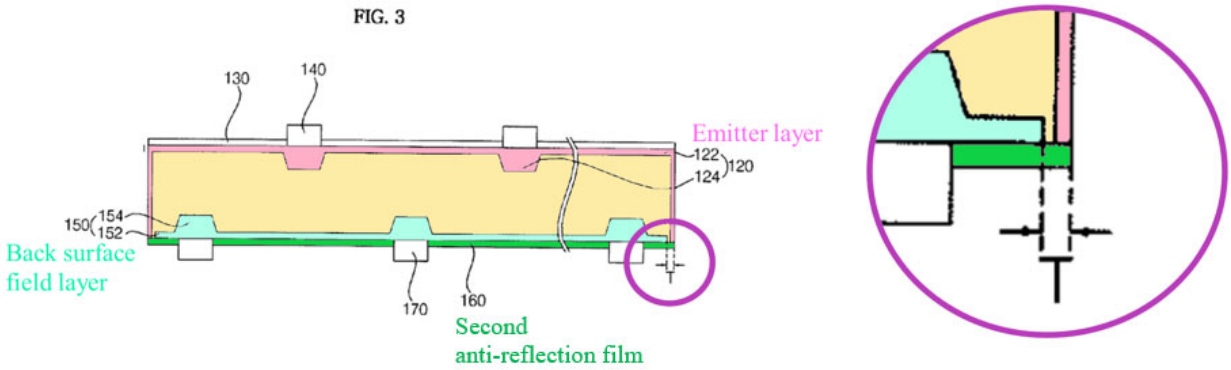
EX1027-Webster, 865. The Oxford College Dictionary defines "periphery" as "the outer limits or edge of an area or object." EX1029-Oxford, 1020.

228. Accordingly, in my opinion the Skilled Artisan would understand that Chang's "periphery region" refers to the solar cell/substrate's perimeter or edge portion, as seen for example in peripheral white space of Figure 3 of the 104 Patent. Thus, the Skilled Artisan would understand that the electrically isolated region (or "isolation region") where the tunneling layer 44 and back surface field are not formed is in the "edge portion" of the substrate, just as in Figure 3 of the 104 Patent. *Id*. And since the tunneling layer 44 in Chang formed on the back surface of the substrate, and the back surface field 30 is formed on the tunneling layer 44, the Skilled Artisan would further understand that the isolation region in Chang is "*in an edge portion of the first surface of the semiconductor substrate*," as claimed by Claim 1 of the 104 Patent.

FIG. 3



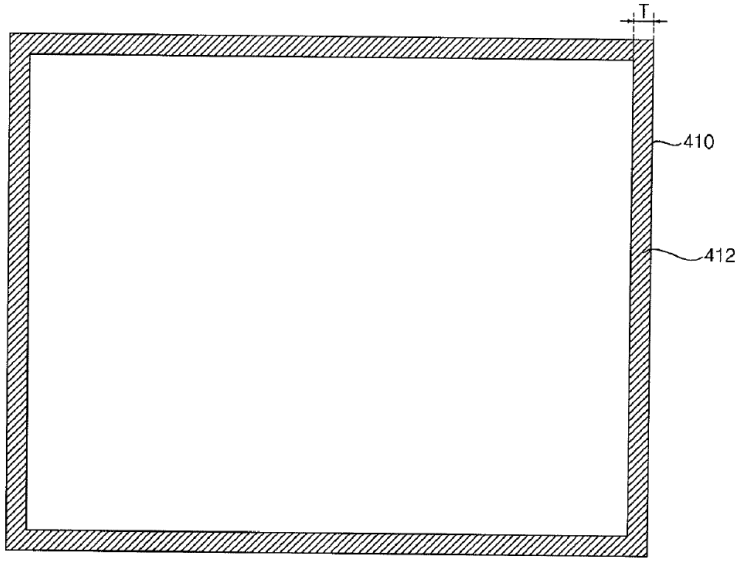
229. The "isolation region" of Chang, described as being in the "periphery region," can be better visualized via Jin, another patent issued to L.G. Electronics. Jin teaches additional details and visually illustrates isolation regions like those in Chang. For example, Figure 3 of Jin shows a gap T where the back surface field layer 150 is not formed, and this separates the back surface field layer 150 from the edge of the back surface of the silicon substrate 110 ("*in an edge portion of the first surface of the semiconductor substrate*"). EX1009-Jin, ¶¶57-58, Fig. 3.



230. Like Chang, the emitter layer 120 of Jin is formed by "heat diffusion" which is understood to be the same as the "thermal diffusion" of Chang's Fig. 8 embodiment. In thermal diffusion, the dopants not only diffuse into the front surface of the substrate, but also diffuses into the lateral side surfaces. Thus, like Chang, to prevent contact between the conductive front emitter layer 120 and the back surface field layer 150 in Jin, a gap T is formed where the back surface field is not formed all the way to the edge or periphery of the back surface. This way, there is no contact between the front emitter layer and the back surface field. Jin

explains that this is done through a mask, as shown in Figure 9a, that covers the periphery or edge of the substrate during the formation of the back surface field.

FIG. 9



(a)

231. Chang's isolation region corresponds to Jin's gap T, which (like the isolation portion of the 104 Patent) inhibits electrical shorting between the back surface field layer and the emitter layer ("*for preventing a contact between the first conductive type semiconductor region and the second conductive type semiconductor region*") caused by conductive dopants being present along the edge of the substrate's back surface.

232. Thus, Chang discloses the "*isolation portion*" of Claim 1 along with all of its accompanying limitations.

k) [1.k] First Passivation Film Covering Isolation Portion

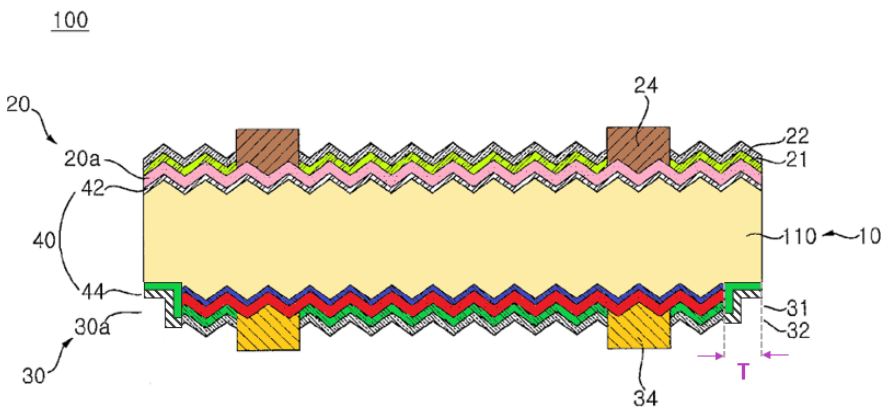
233. Claim 1 next recites: "*the first passivation film covers the first surface of the silicon semiconductor substrate and the isolation portion together*." As discussed in ¶219 above, Chang's "passivation film 31" corresponds to the "*first passivation film*" of Claim 1, and it satisfies this element as well.

234. Here, Chang discloses that the passivation film 31 "may be formed in a substantially entire region over the front surface of the back surface field area 30, excluding a region corresponding to the second electrode 34." EX1013-Chang, ¶63, Fig. 1. And, as discussed in ¶¶223-232 above, Chang discloses an isolation region, which would be covered by the passivation film 31.

235. Notably, Chang does **not** use the especially defined expression of "entirely formed" to describe the passivation film 31's coverage over the silicon back surface. Instead, Chang describes the second passivation film using the general phrase "formed in a substantially entire region" over the back surface field area, which does not have any such exclusions except for the electrode locations. EX1013-Chang, ¶63. That is, Chang expressly identifies the electrode 34 as the only exclusion of the passivation film 31; conversely, Chang does not indicate that the isolation region is excluded from the second passivation film. *Id*. The Skilled Artisan would therefore understand that the use of the phrase "formed in a substantially entire region" means that the second passivation film covers the entire

substrate 10, including the isolation regions, but excluding the second electrode 34, as depicted in modified Figure 1 of Chang below.

FIG. 1

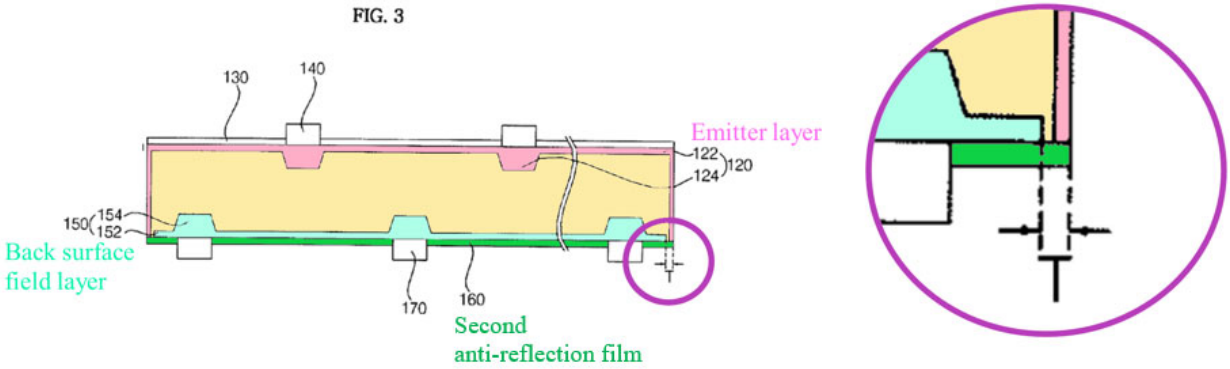


236. Chang explains that the "passivation film 31" not only "passivates defects in the back surface field area 30," it functions to "remove[] recombination sites of minority carriers and thereby increases an open circuit voltage of the solar cell 100." EX1013-Chang, ¶64. It was well known that a bare silicon surface provides recombination sites, and the isolation region constitutes an area of bare silicon surface that was well known to likewise need passivation and removal of recombination sites. Thus, the Skilled Artisan would be motivated to passivate the isolation region, as shown in Jin. *Id*.

237. For example, Jin teaches expressly to cover the back surface of the substrate with a passivation layer even over the isolation regions. In particular, Jin

discloses a second anti-reflection film 160 on the back surface of the substrate. EX1009-Jin, ¶50, Fig. 3. Jin also teaches that when the substrate is n-type (as it is here), the second anti-reflection film 160 "performs the function of a passivation layer" ("*first passivation film*"). Id., ¶50. Fig. 3 of Jin shows that the second-anti-reflection film covers the area Jin refers to as "gap T," which, like the 104 Patent's isolation portion, inhibits electrical shorting. EX1001, 12:60-13:23, Fig. 2; EX1009-Jin, ¶¶58-60. Thus, Jin makes explicit what is already true of Chang's second passivation film: that it would cover the entire substrate back surface, including Chang's isolation region.

238. Even if Trina argues that Chang does not disclose covering the isolation region with the passivation layer 31, such would have been obvious to the Skilled Artisan, as a taught expressly by Jin.



2. Claim 2 – Finger Electrodes

239. Claim 2 depends from claim 1 and requires that the first (back) electrode "*comprises a plurality of first finger electrodes spaced apart from each*

other and extended in parallel in a first direction" and that the second (front) electrode "*comprises a plurality of second finger electrodes spaced apart from each other and extended in parallel in the first direction*." Chang discloses these elements. For example, Chang describes its front and back electrodes 24/34 to "include a plurality of finger electrodes 24a and 34a … and being disposed in parallel to each other." EX1013-Chang, ¶69, Fig. 2. The fingers are shown as thin horizontal lines in Figure 2, and colored orange in the magnified callout. By being parallel to each other, the "plurality of finger electrodes 24a and 34a" naturally extend in the same "*first direction*."

FIG. 2

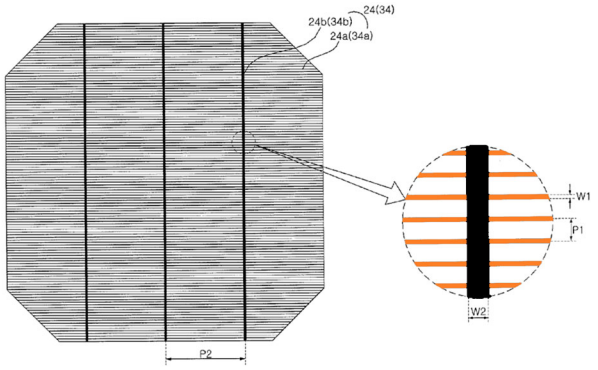
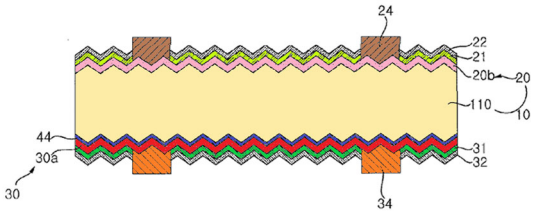


FIG. 8

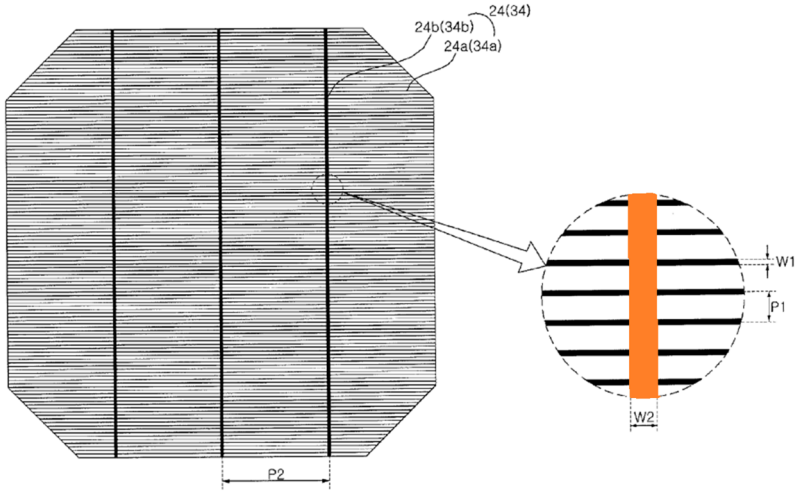


3. Claim 3 – Bus Bars

240. Claim 3 depends from Claim 2 and requires that the first (back) electrode "*further comprises a first bus bar connected to the plurality of first finger electrodes*" and that the second (front) electrodes "*further comprises a second bus bar connected to the plurality of second finger electrodes*." Chang discloses these

elements. Specifically, Chang discloses that "the first and second electrodes 24 and 34 may include bus bar electrodes 24b and 34b which are formed in a direction crossing a direction in which the finger electrodes 24a and 34a are disposed and connect the finger electrodes 24a and 34a." EX1013-Chang, ¶69, Fig. 2. The bus bar are the three vertical black lines shown in Figure 2, and colored orange in the magnified callout.

FIG. 2



4. Claim 4 – Polycrystalline and Single-Cryst Silicon

241. Claim 4 depends from claim 1 and recites: "*wherein the first conductive type semiconductor region includes a polycrystalline silicon material, and the second conductive type semiconductor region includes a single crystal silicon material*." Chang discloses that "the back surface field area 30 ["*first*

conductive type semiconductor region"] may include [] polycrystalline silicon," which is synonymous with polysilicon. EX1013-Chang, ¶61. Chang also discloses that the base area 110 of the silicon substrate 10 may be made of a monocrystalline semiconductor, including monocrystalline silicon. EX1013-Chang, ¶38. In Figure 8, the emitter area 20 ("*second conductive type semiconductor region*") "ha[s] the same crystalline structure as the base area 110," i.e. monocrystalline silicon. EX1013-Chang, ¶98. Monocrystalline silicon is single-crystal silicon.

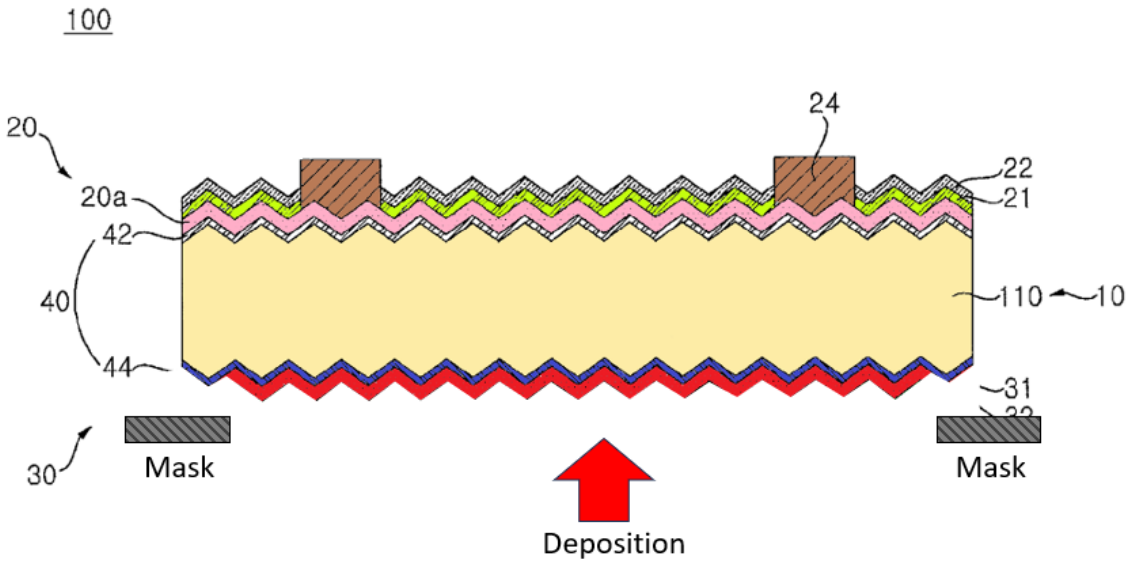
5. Claim 5 – Isolation Width

242. Claim 5 depends from claim 1 and recites: "*wherein a width of the isolation portion is 1 nm to 1 mm*." Jin disclosed that the width of the gap T ("*isolation portion*") "may range from 2 to 300 μm," which is between 1 nm and 1 mm. EX1009-Jin, ¶¶60, 86.

6. Claim 6 – Decreasing Polysilicon

243. Claim 6 depends from claim 1 and recites: "*wherein a thickness of an edge region in the first conductive type semiconductor region progressively decreases towards the isolation portion.*" A Skilled Artisan would understand and find it obvious that the thickness of the back surface field area 30 in the Chang/Jin combination would taper at the edges, towards Chang's periphery isolation region. As I explained above in ¶¶202-210 and 223-232, one well-known and readily

achievable way to construct Chang's back surface field area 30 in the Chang/Jin combination, with Chang's isolation region on the periphery, would be to use a "shadow" mask process like that taught by Scherff. In particular, a metal mask shaped like the mask of Jin shown in Fig. 9 would be placed over the substrate to cover the periphery of the surface of the substrate before depositing the back surface field area 30 using, for example, PECVD or ALD. EX1031-Scherff, §2. Unlike a mask physically bonded to the substrate, a metal mask is placed very close to the surface of the substrate but remains detachable. *Id*. The polysilicon material forming Chang's back surface field area 30 is then deposited through the opening in the mask, as illustrated below in a modified version of Chang's Fig. 1. *See id*.



244. As a Skilled Artisan would have understood, the metal mask is not perfectly abutting against the substrate surface, but rather is a very small distance

from the surface. EX1031-Scherff, §1. As a result, during the deposition process, small amounts of the polysilicon would collect in the "shadow" region underneath the mask. Thus, using a shadow-mask process to form Chang's isolation region would result in the back surface field area 30 (red) tapering in thickness near the edges of the mask opening rather than forming an abrupt edge, such that "*a thickness of an edge region in the first conductive type semiconductor region progressively decreases towards the isolation portion*" that is formed in the masked regions at the edge of the substrate. EX1009-Jin, ¶¶83-85, Fig. 9.

245. This tapering that would occur underneath the metal mask is illustrated, for example, in Figure 4 of a paper depicting the "overspray" that occurs under the edges of a shadow mask when there is separation between the mask and the substrate surface. EX1032-Decker, 97, Fig. 4. The uneven deposition of material under the edges of the mask is caused by the mask blocking the trajectory of particles approaching the substrate surface from straight above or from the outside, while allowing particles approaching over the opening but at an angle to settle beneath the mask, similar to the penumbra formed as a light source is partially blocked. *See id*. Even as the separation distance nears zero, a slight curvature remains in the formation of the deposited layer. *Id*. The type of deposition can also play a role in the tapering effect; for example, sputtering results

in a less defined deposition pattern with even more rounded edges. *Id.*, 97-98, Fig. 5.

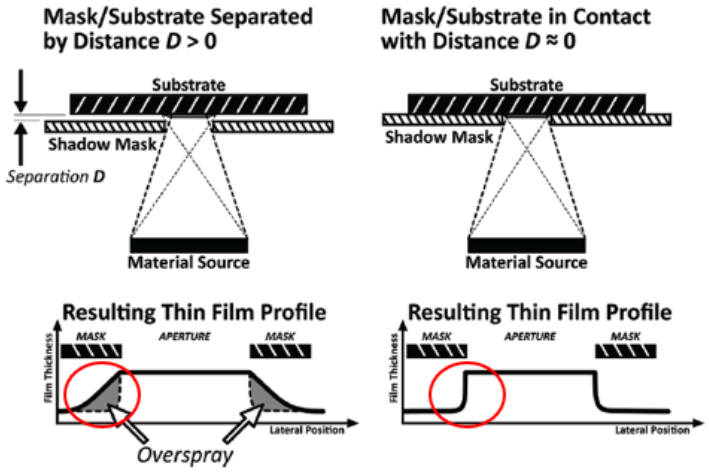


Figure 4. Thin film height profile for deposition with shadow mask separated by distance *D* from substrate (left) and shadow mask in close contact with substrate (right).

246. The tapering effect caused by shadow masking was a well-known phenomenon in the art by 2015, as others had known and commented on it years earlier. For example, a 2006 paper reported that "[s]puttered atoms arrive at substrates with various incident angles because of scattering by atmospheric gasses. Then the pattern edges thin down by deposition of particles shaded from the mask pattern." EX1033-Okuyama, 2890, Fig. 4.

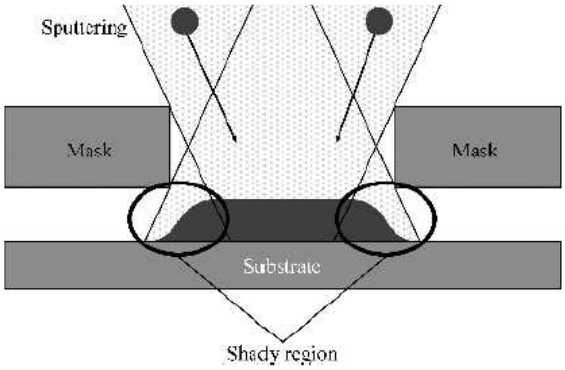
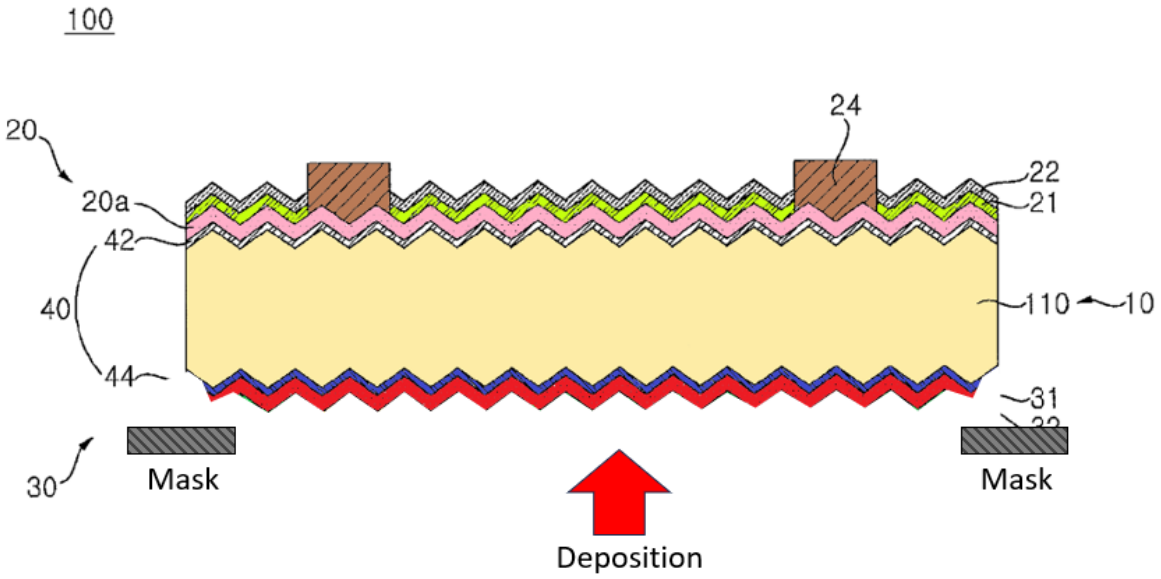
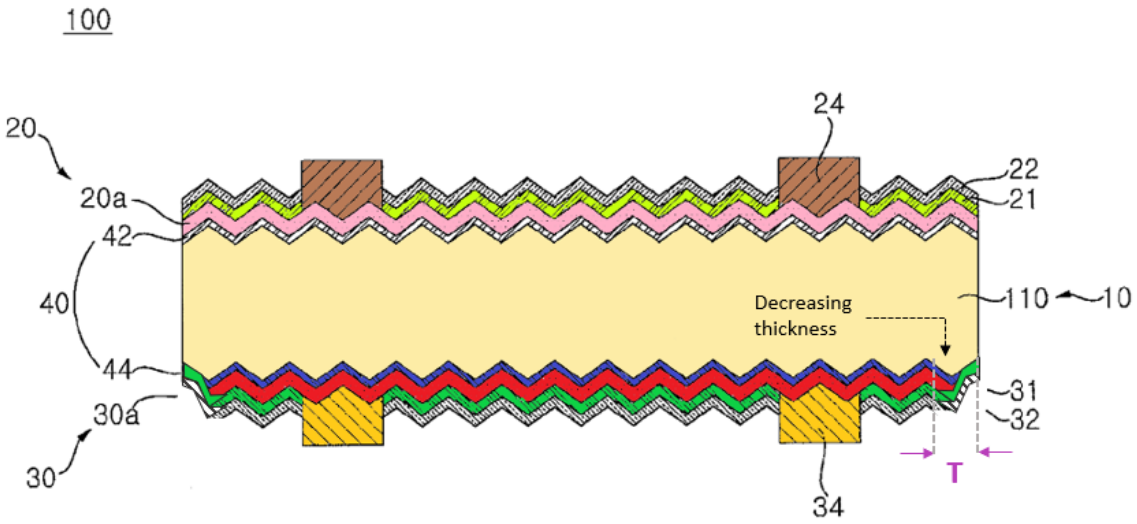


FIG. 4. Schematic of the "shadow effect" that appeared through the mask pattern. The pattern edges thin down because of deposition of shaded sputtered atoms under the mask edges (indicated by the oval).

247. Accordingly, depositing Chang's back surface field area 30 using a metal shadow mask approach would result in a taper in the back surface field area 30 (red) at the edges of the mask into the mask "shadow" regions, towards the isolation region, as depicted in modified Fig. 1 from Chang below. A Skilled Artisan would therefore find claim 6 obvious in view of Chang/Jin, in light of well-known phenomena that occur during the manufacturing process.





7. Claim 9 – Electrodes Connected to the First Conductive Type Semiconductor Region

248. Claim 9 depends from claim 3 and recites: "*wherein all of the plurality of first finger electrodes and the first bus bar are connected to the first conductive type semiconductor region through the first passivation film*." Chang discloses that "the finger electrode 34a and the bus bar electrode 34b of the second electrode 34 may pass through the second passivation film 31 and the second anti-reflective film 32." EX1013-Chang, ¶70, Figs. 1-2, 8. In addition, "[t]he second electrode 34 is electrically connected to the back surface field area 30 via an opening formed in the second passivation film 31." *Id.*, ¶67, 69, Figs. 1, 8. The "back surface field area 30" is the "*first conductive type semiconductor region.*"

8. Claim 10 – Single Layer Electrodes

249. Claim 10 depends from claim 9, and recites: "*wherein all of the plurality of first finger electrodes and the first bus bar have a single layer or*

double layer structure." Although Chang does not expressly disclose the structure of the finger electrode 34a and the bus bar electrode 34b, Chang explains that they "may be formed by a variety of methods such as coating, deposition, printing or the like" and that "the invention is not limited to materials, formation method and the like, of the first and second electrodes 24 and 34." EX1013-Chang, ¶71.

250. Jin on the other hand teaches to use a mask pattern 420 to form both the rear finger electrodes 170 and rear surface bus electrode 190 at the same time. EX1009-Jin, ¶¶88-89 ("The openings 422 of the … mask 420 may be formed not only at positions corresponding to where the rear finger lines 170 are to be formed, but also at positions corresponding to where the rear surface electrodes (190 of FIG. 1) are to be formed…."), Fig. 10.

251. Jin further explains that the rear finger electrodes 170 can be fabricated by screen printing using a paste comprising Ag (silver). EX1009-Jin, ¶52. Such a process would result in a single layer of silver. EX1022-Luque, 277-78 ("The oxides forming the glass frit melt, enabling silver grains to sinter and form a continuous conductor so that the layer can present low sheet resistance."). The Skilled Artisan would understand that screen printing using the mask pattern 420 would result in both the finger electrode 34a and the bus bar electrode 34b of Chang having a single layer structure of silver.

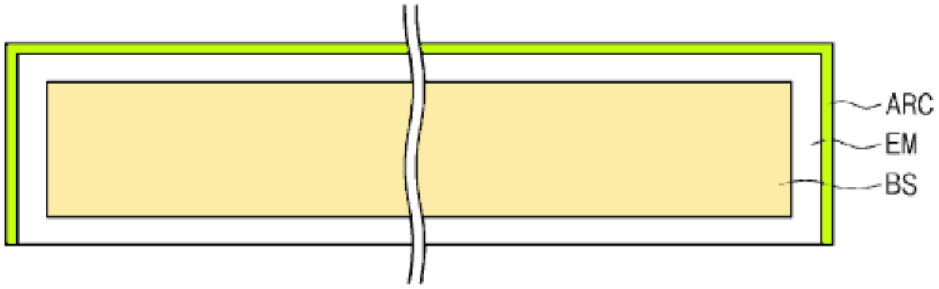
X. CLAIMS 7 & 8 ARE UNPATENTABLE OVER CHANG AND JIN, IN FURTHER VIEW OF SEO

252. Chang discloses a solar cell having a first (front) passivation film 21 over an emitter area 20 on the front side of substrate base area 110, and a second (rear) passivation film 31 on a back surface field layer 30 on the back side of the substrate 110. EX1013-Chang, ¶¶51, 63, Figs. 1, 8. Chang instructs that passivation films may be formed by chemical vapor deposition. EX1013-Chang, ¶150. Chemical vapor deposition (CVD) is a common technique for forming thin films of dielectrics, including silicon oxide and silicon nitride. EX1030-Streetman, 162; EX1022-Luque, 283-84. Although Figs. 1 and 8 of Chang do not depict the passivation films 21/31 on the lateral sides of the substrate 110, Chang does not indicate that the lateral sides of the substrate 110 are masked during the processes for depositing the passivation films 21/31, or that the passivation films 21/31 are subsequently removed from the lateral sides of the substrate. Thus, a Skilled Artisan would expect the chemical vapor deposition technique used by Chang to create these layers would result in their formation on the lateral sides of the substrate. EX1013-Chang, ¶150; EX1015-Seo, 6:39-48, Fig. 1.

253. Seo explicitly illustrates the details of the chemical vapor deposition formation technique taught by Chang. Specifically, Seo teaches a solar cell with a base substrate BS, an emitter layer EM on its front surface, and a back surface field on its rear surface. EX1015-Seo, 3:44-50, 4:11-13, 5:32-35, Fig. 1. As shown in

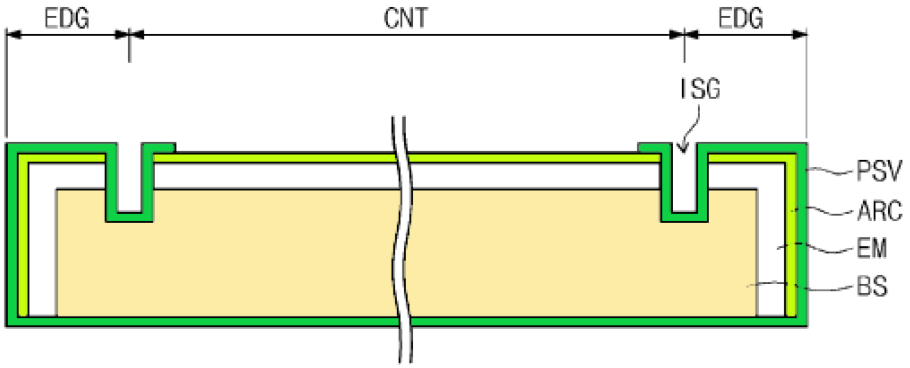
Figure 2C of Seo, after the emitter EM is formed, an "anti-reflection layer ARC is formed directly on the emitter layer EM" using chemical vapor deposition, one of the same techniques identified by Chang, resulting in the anti-reflection layer ARC being deposited on the front and lateral sides of the substrate BS. *Id.*, 6:39-48, Fig. 1; EX1013-Chang, ¶150.

Fig. 2C

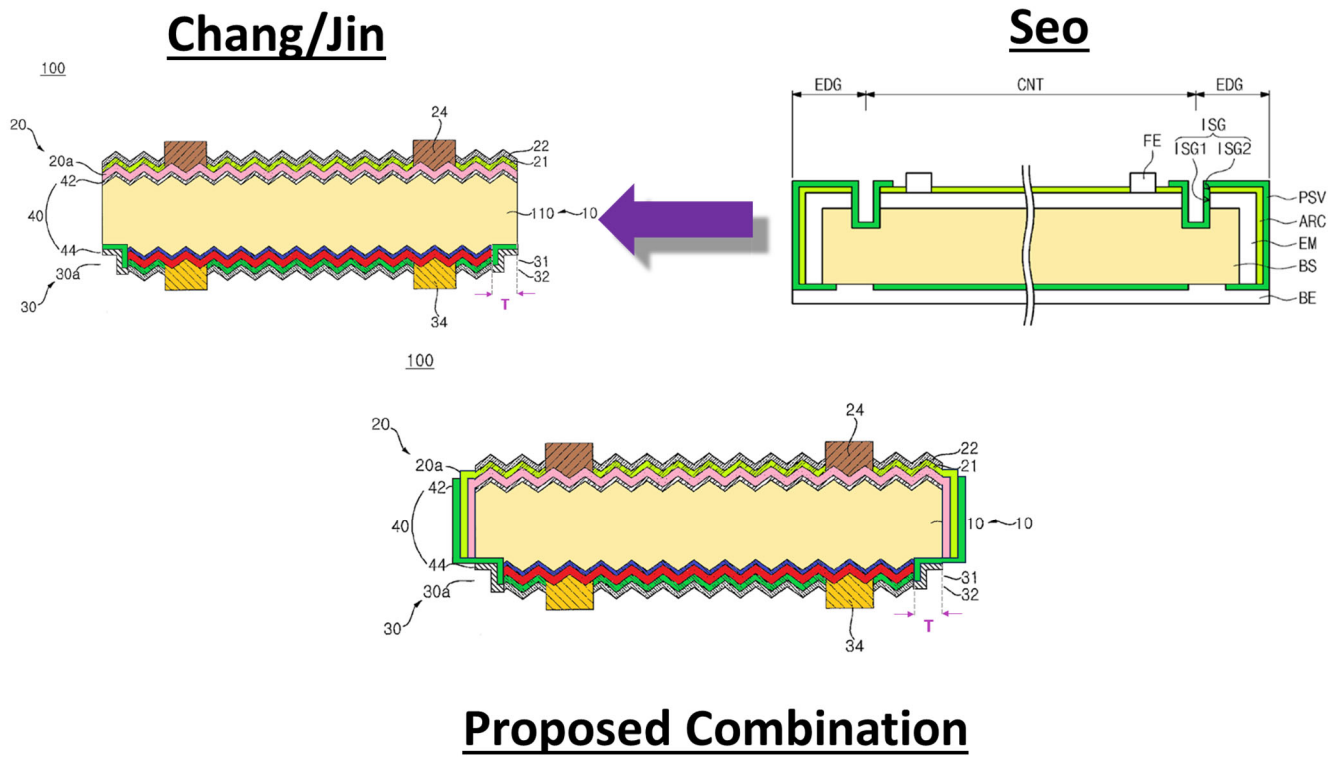


254. Thereafter, "[t]he passivation layer PSV may be formed by depositing at least two of… silicon oxide (SiO_x), silicon nitride (SiN_x), and silicon oxynitride (SiON)," resulting in the passivation layer PSV being deposited on the back and lateral sides of the substrate BS and on top of the previously deposited anti-reflection layer ARC as shown in Figure 2F. EX1015-Seo, 7:60-66. Seo observes that the passivation layer PSV is "in a region corresponding to the edge region EDG and on the side surfaces of the base substrate BS." EX1015-Seo, 4:60-63.

Fig. 2F



255. Thus, Seo discloses the results of Chang's chemical vapor deposition process for depositing Chang's passivation films 21/31. The proposed combination of Seo with Chang/Jin simply applies the structure of Seo's anti-reflection layer ARC and passivation layer PSV formed by CVD (which would have been known to the Skilled Artisan) to Chang's passivation films 21/31, respectively, deposited with the same technique.



Proposed Combination

A. Motivation to "Modify" Chang and Jin with Seo

256. Chang, Jin, and Seo are analogous art because each is in the same field of endeavor—solar cell design. EX1013-Chang, Abstract, ¶¶3, 9; EX1009-Jin, Abstract, ¶¶3, 7; EX1015-Seo, Abstract, 1:11-13. Each is reasonably pertinent to the problems of efficiencies of solar cell designs. EX1013-Chang, ¶¶7-8, 10-11; EX1009-Jin, Abstract, ¶¶6-7; EX1015-Seo, 7:1-11, 9:21-23, 9:31-34, Fig. 5.

257. The combination of Chang/Jin and Seo simply applies the configuration of Seo's ARC and PSV layers to Chang's passivation films 21/31. Seo is simply being used to supply details about Chang's passivation films 21/31 that Chang did not explicitly disclose. A Skilled Artisan would have been

motivated to look to Seo to understand the details not disclosed by Chang regarding Chang's fabrication process because both Chang and Seo disclose the same deposition technique—chemical vapor deposition—for these layers. Moreover, a Skilled Artisan would be motivated to build the combination of Chang/Jin such that the passivation films 21/31 cover the lateral sides of the substrate—as taught by Seo—because eliminating the passivation films from the lateral sides would require either additional process steps to mask the substrate's lateral sides during fabrication of these layers, or additional etching steps to physically remove these layers after their fabrication. Such steps would increase complexity, drive up costs, and increase the risk of manufacturing error. In addition, passivating the lateral sides of the substrate would further reduce edge leakage current caused by surface recombination at the lateral sides of the substrate, resulting in larger open circuit voltage. EX1022-Luque, 313-14 ("Surface passivation of unmetallized regions can be further improved by oxidation."). Surface recombination is lowered by passivation because dielectrics, such as silicon oxides (the passivation material disclosed by Chang), tie up dangling bonds on the surface of the silicon, which act as sources of electron-hole pair recombination. *See* EX1021-Quirk, 227-28. By contrast, eliminating the passivation films 21/31 from the lateral sides of the substrate would not result in any benefit to the solar cell.

B. Reasonable Expectation of Success

258. The Skilled Artisan would have considered the Chang/Jin and Seo combination to be merely an arrangement of like elements (and their corresponding fabrication steps) with each performing the same function it had been known to perform (the passivation films 21/31 of Chang, and the anti-reflection layer ARC and passivation layer PSV of Seo, respectively) and yielding no more than what one would expect from such an arrangement (a solar cell made using Chang's manufacturing process having the passivation film configuration shown in Seo). On the front sun-facing side, Seo's anti-reflection layer ARC and Chang's passivation film 21 may both be formed using silicon oxide (SiOx), such that a Skilled Artisan would understand the two layers to be interchangeable and serve equivalent functions. EX1013-Chang, ¶53; EX1015-Seo, 4:45-47. Likewise, on the back side, both Chang's passivation film 31 and Seo's passivation layer PSV may be formed from silicon oxide (SiOx) or silicon nitride (SiNx). EX1013-Chang, ¶65; EX1015-Seo, 5:12-15.

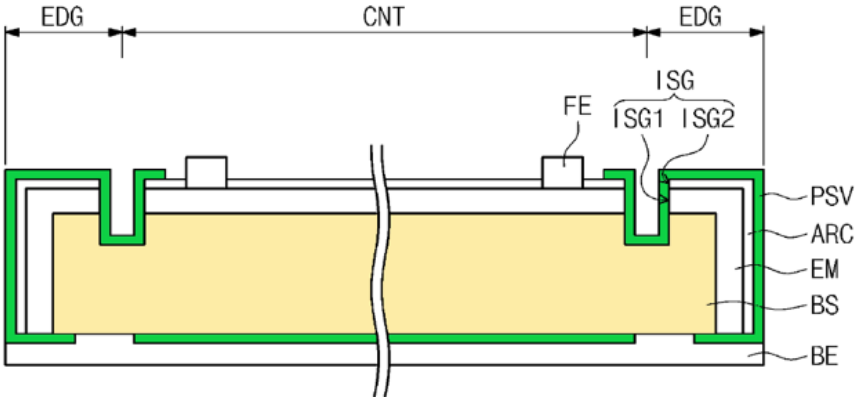
259. Combining Chang/Jin and Seo as described here would have been well within the level of ordinary skill in the art. It would not have resulted in any unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success. The combination would simply require the omission of any additional (and unnecessary) steps in

Chang's solar cell manufacturing process to shield or remove passivation films from the side of the substrate, to yield predictable results.

1. Claim 7 – First Passivation on Substrate Sides

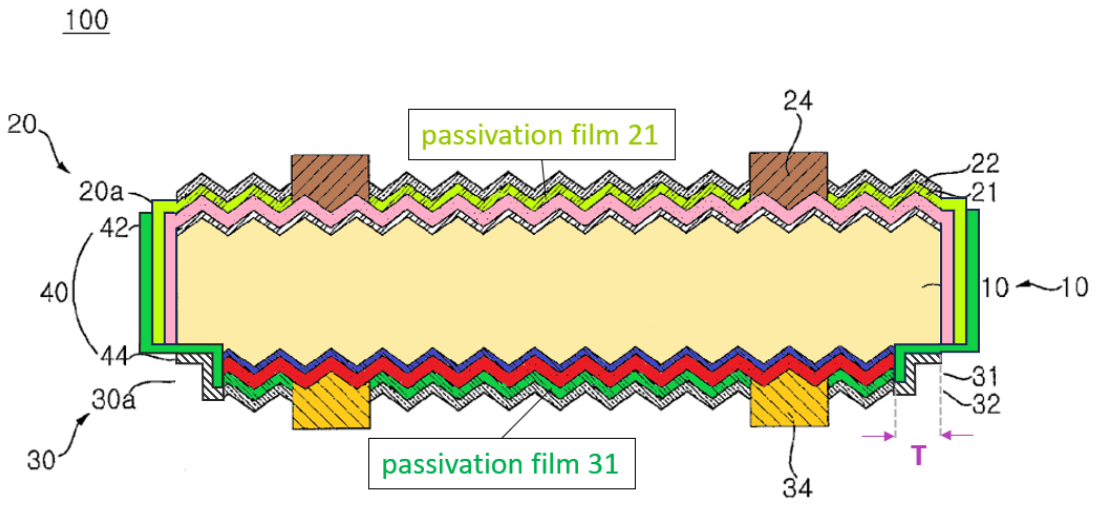
260. Claim 7 depends from claim 1 and recites: "*wherein the first passivation film comprises a side portion extending up a side surface of the semiconductor substrate*." Seo disclosed a passivation layer PSV "**on the side surfaces of the base substrate BS**," as shown in dark green in Figure 1 below. EX1015-Seo, 4:60-62, Fig. 1.

Fig. 1



261. As discussed above in ¶¶219, Chang's passivation film 31 is a "*first passivation film*" as claimed. In the proposed combination, Chang's passivation film 31 is implemented by chemical vapor deposition (EX1013-Chang, ¶150), the same technique used by Seo, resulting in the layout of Seo's passivation layer PSV, as illustrated in modified Figure 1 of Chang below. *See* ¶¶252-255. above. The

same combination could also be implemented using Chang's embodiment depicted in Figure 8, the only difference would be the absence of the tunneling layer 42 on the front side of the solar cell.



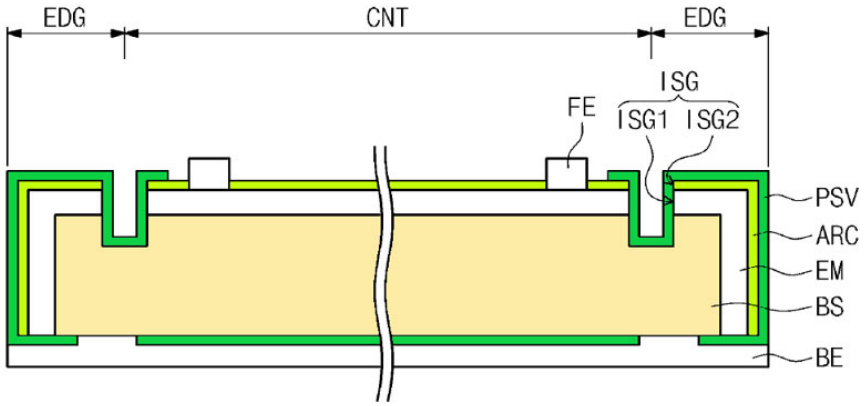
2. Claim 8 – Second Passivation on Substrate Sides

262. Claim 8 depends from claim 7 and recites: "*wherein the second passivation film comprises a side portion formed on the side surface of the semiconductor substrate, and the side portion of the first passivation film on the side surface of the semiconductor substrate is on the side portion of the second passivation film*." Here, the claimed "*second passivation film*" corresponds to the front passivation film, and the "*first passivation film*" corresponds to the back passivation film.

263. Seo discloses an "antireflection layer ARC" (light green) on the front and extending down the lateral sides of the substrate, satisfying the "*the second*

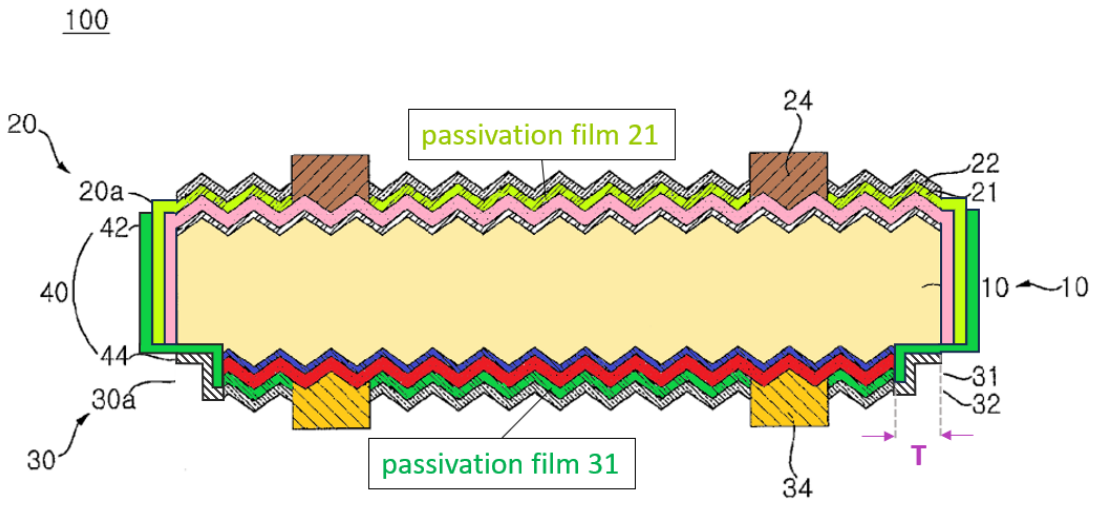
passivation film comprises a side portion formed on the side surface of the semiconductor substrate" portion of the claim. EX1015-Seo, 4:43-51, 4:60-63. As discussed above in ¶¶260-261, Seo discloses a passivation layer PSV (dark green) on the back side and extending up the lateral sides, corresponding to the claimed *first passivation film.* Seo further discloses that "[t]he passivation layer PSV [*first passivation film*] is on the anti-reflection layer ARC [*second passivation film*] in a region corresponding to the edge region EDG **<u>and on the side surfaces of the base substrate BS</u>**." *Id.*, 4:60-63, Fig. 1.

Fig. 1



264. As discussed above in ¶221, Chang likewise discloses a passivation film 21 on the emitter area 20 that corresponds to the claimed "*second passivation film.*" Moreover, Seo discloses that the antireflection layer ARC may be made of "silicon oxide," the same material as Chang's passivation film 21. EX1015-Seo, 4:45-47; EX1013-Chang, ¶53. A Skilled Artisan would therefore understand that

Seo's antireflection layer ARC functions as a passivation layer as taught by Chang. In the proposed combination, Chang's passivation layer is implemented using the layout of Seo's antireflection layer ARC (light green) in modified Figure 1 of Chang below. *See* ¶¶252-255 above. Moreover, a Skilled Artisan would understand the benefit to forming Chang's front passivation film 21 first, *then* the rear passivation film 31, as Seo teaches, because the front sun-facing surface is the most important surface for efficient operation of the solar cell for converting solar radiation into electrical current. Most photons will be absorbed and converted into electron-hole pair formation via the light-incident surface. Damage to the emitter layer during manufacturing therefore results in defects that have an inordinate negative impact on the operation of the cell. Accordingly, manufacturers generally first passivate the front surface of the cell to provide a protective barrier for the front emitter layer, before flipping the substrate over to form the rear passivation layer. As with claim 7, the same combination could also be implemented using Chang's embodiment depicted in Fig. 8, the only difference would be the absence of the tunneling layer 42 on the front side of the solar cell.



XI. CLAIM 11 IS UNPATENTABLE OVER CHANG AND JIN, IN FURTHER VIEW OF WATABE

265. The bifacial solar cell of Chang/Jin in combination with the single layer copper finger and dual layer copper/silver bus bar electrodes of Watabe would have rendered Claim 11 obvious and unpatentable. As discussed above in ¶¶249-251, Chang does not expressly disclose the structure of the finger and bus bar electrodes, explaining that they "may be formed by a variety of methods such as coating, deposition, printing or the like" EX1013-Chang, ¶71. Jin, however, discloses that the finger and bus bar electrodes can be formed by screen printing using a silver paste. EX1009-Jin, ¶52. The combination of Chang/Jin and Watabe would have been nothing more than replacing the screen printed silver finger and bus electrodes of Jin with the screen printed copper finger electrodes and screen printed copper and silver bus electrodes as disclosed in Watabe. EX1009-Jin,

¶¶52, 88-89; EX1014-Watabe, ¶¶16-17, 28-29. The resulting solar cell would meet all limitations of Claim 11.

A. Motivation to Modify Chang/Jin with Watabe

266. Chang, Jin, and Watabe are analogous art because each is in the same field of endeavor, solar cell design, and each is reasonably pertinent to improvements in solar cell designs. Chang, Abstract, ¶3; EX1009-Jin, Abstract, ¶3; EX1014-Watabe, Abstract, ¶1.

267. Jin discloses that both the rear finger 170 and rear surface bus electrodes 190 can be made by screen printing using silver paste, resulting in a single layer of silver. EX1009-Jin, ¶52. Watabe similarly discloses that its finger and bus electrodes can be made by screen printing. EX1014-Watabe, ¶28. To reduce cost, Watabe discloses a dual layer bus bar structure "in which the first electrode layer that is bonded directly to the substrate is formed with a copper paste and the uppermost electrode that is bonded to the connecting wiring is formed with a silver paste. *Id.*, ¶9. Watabe explains that copper has high electrical conductivity and is inexpensive when compared to silver. *Id.*, ¶3. However, copper has "poor solder wettability compared to that of silver" and therefore connecting solar cells together by soldering to copper bus bar electrodes increases the risk of a degraded solder connection, compromising reliability. *Id.*, ¶4. Thus,

Watabe discloses the double layer bus bar structure, which does not impair performance and provides a reduction in cost. *Id.*, ¶9.

268. The Skilled Artisan reviewing Chang/Jin would have been motivated to replace the front and rear screen printed silver finger 170 and bus electrodes 190 of Jin with the screen printed copper finger and copper/silver bus electrodes of Watabe to provide for "a significant reduction in solar cell production costs without compromising solar cell performance and while maintaining the reliability of soldering to the wiring." EX1014-Watabe, ¶14. Watabe discloses that finger and bus bar structure is formed "on at least one side of the semiconductor substrate" and thus contemplates that the invention could be used on both sides of a bi-facial solar cell. *Id.*, ¶9. In the combination, the solar cell of Chang/Jin would continue to function as before, but with the benefit of lower cost. *Id.*, ¶14.

B. <u>Reasonable Expectation of Success</u>

269. The Skilled Artisan would have considered the Chang/Jin/Watabe combination to be merely an arrangement of old elements (and their corresponding fabrication steps) with each performing the same function it had been known to perform, with the screen printed silver fingers and bus bar of Jin replaced by the screen printed copper fingers and copper/silver bus bar of Watabe.

270. Combining Chang/Jin/Watabe as described here would have been well within the level of ordinary skill in the art. It would not have resulted in any

unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success. The combination would simply have been the combination of well-known prior art steps in solar cell and semiconductor fabrication to yield predictable results. Likewise, substituting Jin's screen printed silver rear surface electrode with the screen printed copper finger and copper/silver bus bar electrodes of Watabe would have been a simple substitution of one known element and corresponding fabrication step for another to obtain predictable results.

1. Claim 11 – Single Layer Finger, Dual Layer Bus Bar Electrodes

271. Claim 11 depends from claim 9 and recites: "*wherein: the plurality of first finger electrodes have a single layer structure, and the first bus bar has a double layer structure*." Chang discloses that its rear finger and bus bar electrodes "may be formed by a variety of methods such as coating, deposition, printing or the like" EX1013-Chang ¶71. Jin discloses that the rear finger electrodes 170 and the rear bus electrodes 190 can be fabricated by screen printing using a paste comprising silver. EX1009-Jin, ¶52, 89.

272. Watabe likewise discloses screen printing to form the finger and bus electrodes. However, to decrease costs, Watabe screen prints the finger electrodes using a copper paste. EX1014-Watabe, ¶9 ("the finger electrode is composed of a printed and fired conductive paste containing copper or copper compound fine

particles"). To maintain solderability and adhesive strength to the wiring between cells, Watabe discloses screen printing the bus electrodes first with copper and then with silver. *Id.*, ¶¶12, 28. Specifically Watabe states "[p]referably, at least the bus-bar electrode has a multilayer structure with two or more layers." *Id.*, ¶12. Watabe's screen printed copper finger corresponds to the claimed "*the plurality of first finger electrodes have a single layer structure*" while Watabe's screen printed copper/silver bus electrodes correspond to the claimed "*the first bus bar has a double layer structure*."

XII. OBJECTIVE INDICIA OF NON-OBVIOUSNESS

273. The objective indicia of non-obviousness are also lacking. I have not seen evidence of a commercially successful product with nexus to the 104 Patent. I understand that Trina has sued Runergy in the District of Delaware for patent infringement of the 104 Patent, and that in its complaint against Runergy, Trina does not even allege that it practices the 104 Patent. Trina does allege that it commercially sells "TOPCon" modules, but Trina makes no mention in any of its materials of an "isolation portion" located on the edge of the backside surface of the solar cell—the only feature that led the PTO Examiner deemed novel to allow the claims during prosecution. *See* ¶¶57-63 above. The novel features that Trina touts of its TOPCon products are unrelated to the claims. EX1023 ("The 210R rectangular cell, the selective boron emitter, the backside microstructure reflector,

and the highly doped TOPCon structure with PECVD are four innovations key to the new-generation TOPCon Advanced technology," said Dr. Chen Yifeng, associate vice president of technology at Trina Solar. "These have enabled the delivery of potential production efficiency of 26%, with a modular power output of up to 700W.").

274. There is also no evidence of unexpected results for the claimed invention, or any long felt and unsolved need. An "isolation portion" on the backside surface of the solar cell to prevent shunting of the electric current was well known, as seen from Jin. And there is nothing unexpected in adopting this feature in TOPCon cells, by replacing the diffused BSF of Jin with a BSF of a TOPCon structure. Indeed, this very structure was publicly disclosed by Chang before the priority date of the 104 Patent. Finally, there is no evidence of failure or skepticism by others, copying, praise for the alleged invention of the 104 Patent, or any other indicia of non-obviousness.

275. And even if Trina should come forward with some evidence of these secondary consideration factors, in my opinion it would not be sufficient to overcome the strong of obviousness.

Appendix A:

Materials Relied On

Materials Relied On

The list of documents that I relied upon in forming my opinions is below.

Exhibit #	Reference Name
1001	U.S. Patent No. 9,722,104 ("104 Patent")
1005	File History of U.S. Patent No. 9,722,104
1006	File History of U.S. Patent No. 10,014,419
1007	Korean Patent App. No. 10-2014-0168624 with certified translation
1008	Korean Patent App. No. 10-2015-0122846 with certified translation
1009	U.S. Patent App. Publication No. 2013/0056051 to Y. Jin, *et al.* ("Jin")
1010	F.A. Lindholm, *et al*., Heavily Doped Polysilicon-Contact Solar Cells, IEE Electron Device Letters, Vol. EDL-6, No. 7, (IEEE 1985) ("Lindholm")
1011	Y.H. Kwark, *et al*., N-Type SIPOS and Poly-Silicon Emitters, Solid-Stare Electronics, Vol. 30, No. 11, 1121-l 125 (1987) ("Kwark")
1012	F. Feldmann, *et al*., "Passivated rear contacts for high-efficiency n-type Si solar cells providing high interface passivation quality and excellent characteristics," Solar Energy Materials & Solar Cells 120 (2014) 270-274 (2013 Elsevier B.V.) ("Feldmann")
1013	U.S. Patent App. Publication No. 2014/0299187 to J. Chang, *et al.* ("Chang")
1014	Japanese Patent App. Publication No. JP 2010-186862 to T. Watabe, *et al*. ("Watabe") with certified translation
1015	U.S. Patent No. 8,647,914 to K. Seo, *et al*. ("Seo")
1020	June 21, 2022 USPTO Director's Memo
1021	M. Quirk, *et al*., Semiconductor Manufacturing Technology (Prentice-Hall Inc. 2001)

Exhibit #	Reference Name
1022	A. Luque, *et al*., Handbook of Photovoltaic Science and Engineering (John Wiley & Sons Ltd. 2003)
1023	Trina Solar n-type TOPCon Advanced technology steps onto the world stage, with efficiency reaching 26% in mass production and 700W+ in module power, *available at* https://www.trinasolar.com/us/trina-solar-n-type-vertex-to-reach-700gw (last visited August 19, 2024)
1024	Y. H. Kwark, *et al*. SIPOS Heterojunction contacts to silicon, 1984 International Electron Devices Meeting (1984): 742-745 ("Kwark II")
1025	SY Lien, *et al.*, Tri-layer antireflection coatings (SiO2/SiO2—TiO2/TiO2) for silicon solar cells using a sol-gel technique, Solar Energy Materials & Solar Cells 90, 2710-2719 (2006)
1026	D. Kray, *et al.*, Study on the edge isolation of industrial silicon solar cells with waterjet-guided laser, Solar Energy Materials & Solar Cells, 91, 1638–1644 (2007)
1027	Merriam-Webster's Collegiate Dictionary, 10th Ed. (Merriam-Webster, Inc. 1998) (definition of "periphery")
1028	S. Duttagupta, *et al*., Progress in Surface Passivation of Heavily Doped n-Type and p-Type Silicon by Plasma-Deposited AlOx/SiNx Dielectric Stacks, IEEE Journal of Photovoltaics, Vol. 3, No. 4 (October 2013)
1029	Oxford College Dictionary, 2nd Ed. (Oxford University Press, Inc. 2002)
1030	B. Streetman and S. Banerjee, Solid State Electronic Devices, 6th Ed. (Prentice-Hall Inc. 2006)
1031	M. Scherff, Novel method for preparation of interdigitated back contacted a-Si:H/c-Si heterojunction solar cells, 26th European Photovoltaic Solar Energy Conference and Exhibition (2011)
1032	W. Decker, *et al*., "Novel low pressure sputtering source and improved vacuum deposition of small patterned features using precision shadow

Exhibit #	Reference Name
	masks," 59th Annual Technical Conference Proceedings (Society of Vacuum Coaters 2016)
1033	H. Okuyama, *et al.*, Position-selective growth of carbon nanotubes on Ni catalysts/Mo underlayers by thermal chemical vapor deposition, J. Mater. Res., Vol. 21, No. 11 (Materials Research Society 2006)
1034	T. Saga, Advances in crystalline silicon solar cell technology for industrial mass production, NPG Asia Materials, Volume 2, 96–102 (2010)
1036	U.S. Patent Pub. No. 2012/0003781 to Yun, *et al*. ("Yun")