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DECEMBER 9-12, 1984

TECHNICAL DIGEST

Late News!
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1984 International Electron Devices Meeting
TECHNICAL DIGEST

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WELCOMING STATEMENT FROM THE GENERAL CHAIRMAN



Nino Masnari
General Chairman



Hank Geipel
Technical Program
Chairman

On behalf of the conference committee, I would like to welcome you to the 1984 International Electron Devices Meeting, the international forum for the presentation of the latest electron device research and development results. The rapid and continuing growth of the electron device field, as reflected in this year's program, is a measure of the vitality of IEEE as we celebrate its 100th anniversary. This also represents the first return of IEDM to San Francisco after the successful initial 1982 west coast meeting.

The strong, international nature of the meeting is reflected in this year's program which contains 204 papers selected from 524 submitted abstracts from 22 countries around the world. These papers comprise 30 technical sessions covering six major categories: Solid State Devices; Device Technology; Integrated Circuits; Quantum Electronics and Compound Semiconductor Devices; Detectors, Sensors, and Displays; and Electron Tubes. The plenary session will feature three highlighted presentations on microelectronics, GaAs IC technology, and megabit DRAMs, as well as presentation of the J.J. Ebers Award and the 1983 Best Student Paper Award. The broadening scope of the meeting is also indicated by the five panel sessions covering the important areas of Computer Automated Manufacturing of Integrated Circuits, Future Directions of Power Tube Research and Development, High-Speed Monolithic Digital and Analog Devices, Multilayer Interconnection Technology, and Next Generation VLSI Power Supply Standards. The meeting will again feature a short course on Sunday on silicon processing covering device isolation, process and device characterization, oxidation and diffusion, and wafer cleaning and gettering.

The traditional Tuesday luncheon will feature a talk by Dr. A.S. Grove of Intel on the challenges encountered in the management of today's high-technology corporations. The luncheon will also be the setting for the presentation of the 1984 Frederik Philips Award to Dr. John Galt of Sandia National Laboratories.

On behalf of the IEEE Electron Devices Society, which sponsors the IEDM, I wish to express my appreciation and congratulations to the members of the Conference Committee for the outstanding job that they have done in planning and organizing the 1984 meeting. In addition, the authors are to be commended for their efforts towards technical excellence in their papers. It is with pleasure that I welcome them and all attendees to the 1984 International Electron Devices Meeting.

Nino Masnari
General Chairman

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11:10 a.m.
30.6 SOI-CMOS 4K SRAM WITH HIGH DOSE OXYGEN IMPLANTED SUBSTRATE, C-E. Chen, T. Blake, L. Hite, S. Malhi, B. Mao and H. Lam, *Texas Instruments, Inc., Dallas, TX* 702

11:35 a.m.
30.7 A P-TYPE BURIED LAYER FOR PROTECTION AGAINST SOFT ERRORS IN HIGH DENSITY CMOS STATIC RAMS, H. Momose, T. Wada, I. Kamohara, M. Isobe, J. Matsunaga and H. Nozawa, *Toshiba Corporation, Kawasaki, JAPAN* 706

SESSION 31: Quantum Electronics and Compound Semiconductor Devices—Photodetectors 711

Wednesday, December 12, 9:00 a.m.
Franciscan Room

Co-Chairmen: M. A. Pollack
V. Diadiuk

9:00 a.m.
INTRODUCTION

9:05 a.m.
31.1 ULTRA-HIGH SPEED PHOTODETECTORS, (Invited Paper), S. Y. Wang, *Hewlett-Packard Laboratories, Palo Alto, CA* 712

9:30 a.m.
31.2 FAST InGaAs PHOTOCONDUCTIVE DETECTORS WITH SPEED ENHANCED BY BERYLLIUM ION BOMBARDMENT, P. Downey and R. Martin, *AT&T Bell Laboratories, Holmdel, NJ;* R. Nahory, *Bell Communications Research, Murray Hill, NJ;* O. Lorimor, *AT&T Bell Laboratories, Murray Hill, NJ* 716

9:55 a.m.
31.3 ION IMPLANTED LATERAL IN $_{.2}Ga_{.8}As/GaAs$ STRAINED-LAYER SUPERLATTICE PHOTODETECTOR, G. Bulman, D. Myers, J. Wiczer, L. Dawson, R. Biefeld and T. Zipperian, *Sandia National Laboratories, Albuquerque, NM* 718

10:20 a.m.
31.4 NEW PSEUDO-QUANTERNARY GaInAsP SEMICONDUCTORS: A HIGH SPEED "HIGH-LOW" AVALANCHE PHOTODIODE WITH $Ga_{.47}In_{.53}As$/InP GRADED GAP SUPERLATTICE, F. Capasso, A. Hutchinson and N. Olsson, *AT&T Bell Laboratories, Murray Hill, NJ;* H. Cox and S. Hummel, *Bell Communications Research, Murray Hill, NJ* 722

10:45 a.m.
31.5 FULLY OPTICALLY AND ELECTRICALLY INTERFACED, MONOLITHIC 1×12 ARRAY of $In_{.53}Ga_{.47}As$/InP p-i-n PHOTODIODES, M. Brown, S. Forrest, P. Hu, D. Kaplan, M. Koza, Y. Ota, J. Potopowicz, C. Seabury and M. Washington, *AT&T Bell Laboratories, Murray Hill, NJ* 726

11:10 a.m.
31.6 GaInAs, AlInAs SCHOTTKY BARRIER DIODES AND GaInAs/AlInAs HETEROJUNCTION DIODE AS INTERNAL PHOTOEMISSION DETECTORS, K. Hsieh, *Hughes Research Lab., Malibu, CA;* L. Eastman, *Cornell University, Ithaca, NY* 728

11:35 a.m.
31.7 A HIGH SPEED, LOW VOLTAGE SILICON PHOTODIODE WITH BURIED ISOLATION REGION, G. Chang, A. Hartman, M. Robinson, T. Riley and K. Lee, *AT&T Bell Laboratories, Murray Hill, NJ* 732

SESSION 32: Device Technology—Advanced Bipolar Technology 737

Wednesday, December 12, 1:30 p.m.
Continental Ballroom 4,5

Co-Chairmen: J. Aitken
A. Wieder

1:30 p.m.
INTRODUCTION

1:35 p.m.
32.1 CONDUCTION MECHANISM OF POLYSILICON EMITTERS WITH THIN INTERFACIAL OXIDE LAYERS, H. Schaber, B. Benna, L. Treitinger and A. Wieder, *Siemens AG, Munchen, FRG* 738

2:00 p.m.
32.2 SIPOS HETEROJUNCTION CONTRACTS TO SILICON, Y. Kwark, R. Swanson and R. Sinton, *Stanford University, Stanford, CA* 742

2:25 p.m.
32.3 A SILICON BIPOLAR TRANSISTOR WITH A HYDROGENATED AMORPHOUS EMITTER, M. Ghannam, J. Nijs, R. DeKeersmaecker and R. Mertens, *Katholieke Universiteit Leuven, Heverlee, BELGIUM* 746

2:50 p.m.
32.4 SELF-ALIGNED BIPOLAR TRANSISTORS WITH ENHANCED EFFICIENCY POLYSILICON EMITTERS, A. Cuthbertson and P. Ashburn, *Southampton University, Southampton, Hampshire, ENGLAND* 749

3:15 p.m.
32.5 NEW SELF-ALIGNED COMPLEMENTARY BIPOLAR TRANSISTORS USING SELECTIVE-OXIDATION MASK, H. Sadamatsu, M. Inoue, A. Matsuzawa, A. Kanda and H. Shimoda, *Matsushita Electric Industrial Co., Ltd., Osaka, JAPAN* 753

3:40 p.m.
32.6 MODELLING OF POLYSILICON DOPANT DIFFUSION FOR SHALLOW-JUNCTION BIPOLAR TECHNOLOGY, G. Barbuscia, G. Chin and R. Dutton, *Stanford University, Stanford, CA;* T. Alvarez, *Motorola, Mesa, AZ;* L. Arledge, *Texas Instruments, Dallas, TX* 757

4:05 p.m.
32.7 **2 MICRON MERGED BIPOLAR-CMOS TECHNOLOGY,** A. Alvarez, P. Meller and B. Tien, *Motorola Inc., Mesa, AZ* 761

SESSION 33: Solid State Devices—Lightly-Doped Drain MOSFETs 765

Wednesday, December 12, 1:30 p.m.
Continental Ballroom 6,7,8,9
Co-Chairmen: J. R. Sokel
G. Merkel

1:30 p.m.
INTRODUCTION

1:35 p.m.
33.1 **STATE-OF-THE-ART OF MOS MODELLING,** (Invited Paper), A. Schutz and C. Werner, *SIEMENS Research and Development Center, Munchen, WEST GERMANY* 766

2:00 p.m.
33.2 **OPTIMIZATION OF LIGHTLY DOPED DRAIN MOSFETS USING A NEW QUASIBALLISTIC SIMULATION TOOL,** C. Werner, R. Kuhnert and L. Risch, *Siemens AG, Munchen, FRG* 770

2:25 p.m.
33.3 **HOT CARRIER DEGRADATION MODES AND OPTIMIZATION OF LDD MOSFETs,** H. Katto, K. Okuyama, S. Meguro, R. Nagai and S. Ikeda, *Hitachi Ltd., Tokyo, JAPAN* 774

2:50 p.m.
33.4 **EFFECTS OF FIELD BORON DOSE ON SUBSTRATE CURRENT IN NARROW CHANNEL LDD MOSFETs,** S. Sawada, Y. Matsumoto, S. Shinozaki and O. Ozawa, *Toshiba Corporation, Kawasaki-city, JAPAN* 778

3:15 p.m.
33.5 **CHARACTERIZATION OF As-P DOUBLE DIFFUSED DRAIN STRUCTURE,** K. Balasubramanyan, M. Hargrove, M. Lin, D. Hoyniak, J. LaRue, and D. Thomas, *IBM, Essex Junction, VT;* H. Hanafi, *IBM, Yorktown Heights, NY* 782

3:40 p.m.
33.6 **MECHANISM OF HOT ELECTRON INDUCED DEGRADATION IN LDD NMOS-FET,** Y. Toyoshima, H. Nihira, M. Wada and K. Kanzaki, *Toshiba Corporation, Kawasaki, JAPAN* 786

SESSION 34: Device Technology—SOI and 3-D Technologies 791

Wednesday, December 12, 1:30 p.m.
Imperial Ballroom
Co-Chairmen: D. Bartelink
S. Malhi

1:30 p.m.
INTRODUCTION

1:35 p.m.
34.1 **3-D SOI/CMOS** (Invited Paper), M. Nakano, *Fujitsu, Ltd., Kawasaki, JAPAN* 792

2:00 p.m.
34.2 **FABRICATION OF HIGH SPEED 1 MICRON FIPOS/CMOS,** K. Anzai, F. Otoi, M. Ohnishi and H. Kitabayashi, *OKI Electric Industry Co., Ltd., Tokyo, JAPAN* 796

2:25 p.m.
34.3 **ADVANCES IN OXIDIZED POROUS SILICON FOR SOI,** L. A. Nesbit, *IBM Corporation, Essex Junction, VT* 800

2:50 p.m.
34.4 **ELECTRICAL CHARACTERIZATION OF OXYGEN IMPLANTED SILICON SUBSTRATES,** D. Foster, A. Butler and P. Bolbot, *Plessey Research (Caswell) Ltd., Caswell, Towcester, Northants, U.K.* 804

3:15 p.m.
34.5 **DEVICE PERFORMANCES OF A SUBMICRON SOI TECHNOLOGY,** A. Auberton-Herve, J. Joly, J. Hode, J. Gautier and P. Jeuch, *LETI/Commissariat a l'Energie Atomique, Grenoble, FRANCE* 808

3:40 p.m.
34.6 **MERGED CMOS/BIPOLAR TECHNOLOGIES AND MICROWAVE MESFETS UTILIZING ZONE-MELTING-RECRYSTALLIZED SOI FILMS,** B. Tsaur, H. Choi, C. K. Chen, C. L. Chen, R. Mountain and J. Fan, *Massachusetts Institute of Technology, Lexington, MA* 812

4:05 p.m.
34.7 **PROMISING NEW FABRICATION PROCESS DEVELOPED FOR STACKED LSIs,** M. Yasumoto, H. Hayama and T. Enomoto, *NEC Corporation, Kawasaki, JAPAN* 816

SESSION 35: Electron Tubes—Fast Wave Tubes 821

Wednesday, December 12, 1:30 p.m.
Hilton Plaza
Co-Chairmen: J. M. Baird
T. Kageyama

1:30 p.m.
INTRODUCTION

1:35 p.m.
35.1 **SURVEY OF PHYSICS RESEARCH IN MICROWAVE DEVICES** (Invited Paper), G. Bekefi, *Massachusetts Institute of Technology, Cambridge, MA* 822

2:00 p.m.
35.2 **A 60 GHz, 200 kW CW GYROTRON WITH HIGH OUTPUT MODE PURITY,** H. Jory, K. Felch, R. Bier, L. Fox, H. Huey, L. Ives, N. Lopez, J. Manca, J. Shively and S. Spang, *Varian Associates, Inc., Palo Alto, CA* 826

2:25 p.m.
35.3 **A 100 GHz, 500 kW GYROTRON OSCILLATOR,** W. DeHope, J. Eldridge, P. Ferguson, S. Hart, A. Krycuk, V. Matranga, J. Sandoval, M. Schmitt, J. Tancredi, C. Thorington and M. Wozniak, *Hughes Aircraft Co., Torrance, CA* 830

2:50 p.m.
35.4 **DESIGN CONSIDERATIONS FOR A 100 kW CW, 140 GHz GYROTRON OSCILLATOR,** K. Felch, R. Bier, L. Fox, H. Huey, L. Ives, H. Jory and S. Spang, *Varian Associates, Inc., Palo Alto, CA* 834

3:15 p.m.
35.5 **PERFORMANCE OF A THREE CAVITY GYROKLYSTRON,** W. Bollen and C. Sedlak, *Mission Research Corp., Alexandria, VA;* A. Ganguly, B. Arfin and R. Parker, *Naval Research Laboratory, Washington, DC* 838

3:40 p.m.
35.6 **FOURTH HARMONIC GYROMAGNETRON DEVELOPMENT,** L. Barnett, J. Baird, U. Shrivastava and R. Grow, *University of Utah, Salt Lake City, UT* 842

4:05 p.m.
35.7 **PENIOTRON AMPLIFIER RESULTS,** G. Döhler, D. Gallagher, C. Lowrie, R. Moats and F. Scafuri, *Northrop Corporation, Rolling Meadows, IL* 845

NOTE: The following paper was not available at time of publication.

9:05 a.m.
28.1 **X-RAY LITHOGRAPHY FOR HIGH RESOLUTION** (Invited Paper), A. Heuberger, *Fraunhofer-Institut fur Mikrostrukturtechnik, Berlin, FRG*

SIPOS HETEROJUNCTION CONTACTS TO SILICON

Young H. Kwark, Ron Sinton, Richard M. Swanson

110 McCullough Building, Stanford Electronics Laboratories
Stanford, CA. 94305 (415)497-0503

Abstract: Using SIPOS films (SiO_x, x <2) as an emitter contact has been previously shown to reduce the emitter saturation current, J_{oe}, by at least a factor of fifty when compared to a conventional emitter structure with a metallic contact. Previous attempts to explain this J_{oe} reduction have focused on the bulk properties of the SIPOS films. Experimental results of this study which attained J_{oe} values of $2 \times 10^{-}14$ A/cm^2, suggest that an interfacial layer between the SIPOS and underlying silicon may play an important, if not dominant, role with the implication that the high oxygen concentrations previously used may not be essential for J_{oe} reduction. This would permit the use of lower oxygen content SIPOS films whose lower bulk resistivities would allow utilization of these films in structures such as scaled VLSI bipolar devices and high concentration point contact solar cells where series resistance is detrimental to device performance.

Introduction: Deliberate introduction of controlled amounts of an oxygen bearing species such as nitrous oxide into the deposition ambient normally used for chemical vapor deposition of polysilicon produces SIPOS, a class of silicon oxides which exhibits a wide range of physical properties (1). It is possible to tailor film characteristics such as the refractive index, by altering the oxygen partial pressure in the deposition ambient. The addition of a dopant species converts these films from semi-insulating to a form that can be made sufficiently conductive after annealing to make them interesting for electronic applications (2). Incorporation of these films into the emitter structure of an NPN bipolar transistor had been found to reduce the emitter saturation current fifty fold (3); this translates into potential improvements of energy conversion efficiency for solar cells and enhanced high frequency performance of bipolar structures.

Matsushita (3) hypothesized that large amounts of oxygen in his SIPOS films produce a bandgap larger than for monocrystalline silicon. In N-type SIPOS emitter contacts the lining up of the equilibrium Fermi levels results in a barrier in the valence band which blocks hole transport and accounts for the reduction in J_{oe}. Simplified density of states calculations using small clusters of SiO_x lend qualitative support to this scenario; namely the gap in the density of states increases in a continuous manner as the oxygen content in SiO_x is increased (4). However, it is important to note that these clusters were constructed assuming a uniform and random distribution of oxygen throughout the film. While this may apply to films prepared at low temperatures (e.g. evaporation or sputtering), the CVD deposited SIPOS films used in these devices require a high temperature anneal in order to activate the dopant. A phase precipiation which results in a fine dispersion of silicon microcrystallites embedded in an oxygen rich matrix appears to be the result of such anneals (5). Such a heterogeneous structure would indicate that a model based on an effective bandgap and diffusion length may be oversimplified.

Experimental Results: Bipolar test structures and measurement techniques were refined to allow measurement of the emitter saturation current at these low levels; a sample Gummel plot showing the area related component from which J_{oe}, the emitter saturation current, was extracted is shown in Fig. 1. Devices with differing area/perimeter ratios were used in conjunction with the definition

$$I_{base} = Area * J_{area} + Perimeter * J_{peri}$$

to effect this separation. By utilizing various SIPOS emitter contact configurations, these measurements, after correcting to 300°K, allowed determination of which film parameters were relevant in determining the hole blocking action of the films.

The first set of experiments investigated the effect of varying the oxygen content on J_{oe}. These films were deposited in a hot wall APCVD reactor using nitrogen as the carrier gas. Varying γ, the ratio of nitrous oxide to silane in the deposition ambient, from $\gamma = 0$ (which should produce POLY) to $\gamma = 1.5$ (which should produce films comparable to ref. (3)) should display a monotonically decreasing J_{oe} as hole transport is increasingly impeded by the increasing bandgap in the bulk SIPOS. In fact for devices annealed at 900°C/13 min, there is very little dependence on γ as seen in Fig. 2, although increasing the anneal temperature to 1000°C adversly affected J_{oe}. That the γ=0 films produced such good results was surprising since POLY films of comparble thickness should yield a J_{oe} an order of magnitude larger. In fact it was discovered that these $\gamma = 0$ films

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incorporated significant (several atomic %) amounts of oxygen as indicated from electron microprobe and the fact that they etched, albeit slowly, in buffered HF. This insensitivity to bulk film properties implies that other mechanisms, in this case the formation of an interfacial oxide layer as a result of the annealing process (Fig. 3), may be primarily responsible for the reduced hole currents. This conclusion suggests that the mechanism of hole suppression is akin to that for polysilicon SIS contacts, and that the distinguishing feature of SIPOS may be its built-in source of oxygen which aids in the formation and/or maintainence of this interfacial layer.

In order to establish unambiguous results for a relatively oxygen free film, POLY films doped insitu in an RF heated cold wall APCVD reactor using a hydrogen carrier were used in the next set of emitter contacts; these films did not etch in BHF. Fig. 4 displays the resulting J_{oe} as a function of annealing temperature for emitter B which had a Gaussian (3×10^{19} surface concentration, 1 micron depth into 5×10^{16} background) emitter diffused prior to the POLY deposition and emitter C which relied solely on outdiffusion from the doped POLY to form the base-emitter junction. For both structures, devices were prepared with and without a chemically grown oxide (chemox) by dipping half of the wafer which underwent a full RCA clean in dilute HF. The value for emitter B with a conventional aluminum contact is shown for reference. Addition of POLY without the chemox does not greatly impact J_{oe} as would be expected since the heavily doped POLY acts essentially as an extension of the monocrystalline emitter. Addition of the chemox greatly decreases the J_{oe} as has been previously reported (6). "Prediffused" emitter B displays a baseline J_{oe} of 5×10^{-14} A/cm^2 due to recombination in the bulk of the emitter. To this is added a component due to outdiffusion from the heavily doped POLY which becomes increasingly significant for annealing temperatures above 900°C. This is apparent if one notes that the increase in J_{oe} for emitter B can be accounted for by the J_{oe} of emitter C at the same temperature. At 1000°C, this outdiffusion is severe enough to dominate the J_{oe} which accounted for the lack of difference between emitters B and C.

In Fig. 5, J_{oe} for a $\gamma = 0$ SIPOS film (which recall has several at% oxygen) without the chemox is shown. The behavior above 850°C strongly resembles the POLY case with chemox. Addition of the chemox to the SIPOS contact structure does not greatly affect the lowest values of J_{oe} attained. However, the increase in J_{oe} at higher temperatures is not as severe as for the devices in Fig. 4 and 5. Furthermore, devices annealed at 850°C, while displaying the same J_{oe} as the SIPOS devices without the chemox, also suffered from greatly increased series resistance.

Discussion: Emitter saturation currents of $1 - 2 \times 10^{-14}$ A/cm^2 have been attained for POLY with chemox and for both SIPOS contact structures. That there was little difference in J_{oe} between the SIPOS contacted emitters with and without the chemox would indicate that the interface between SIPOS and monocrystalline silicon is similar in both cases. Postulating the formation of a thin tunnelable interfacial oxide as a consequence of the high temperature annealing step is consistent with the observed similarities in J_{oe}. The smaller increase in J_{oe} for the SIPOS device with chemox can be explained by assuming that the chemox simply adds an additional thickness to the oxide layer resulting from the anneal step. This would act as a more robust diffusion barrier and would limit the extent of outdiffusion of dopants from the SIPOS thus reducing bulk recombination in the monocrystalline emitter region. This is also consistent with the increased series resistance which would arise from a thicker interfacial layer. The possibilty remains that a thin thermal oxide is growing during the thermal equilibration phase prior to deposition of the SIPOS films; although standard precautions were taken to minimze the presence of oxygen and water vapor in the deposition ambient, the apparatus currently available can not be used to rule out this possibility.

A key figure of merit which has not been discussed is the specific resistivity of the emitter contact structure. For the SIPOS films mentioned in ref. (3), a specific contact resistivity of 1×10^{-3} ohm-cm^2 would result for a 1000 angstrom thick film. This is far too high to permit use in scaled bipolar or in high concentration point contact solar cells. If the hole barrier mechanism operative in SIPOS contacts is indeed associated with the formation of interfacial layers, then there is no apriori need for such high oxygen concentrations in the bulk of the films with their attendant high resistivity. The focus, in this case, would shift to the kinetics of the annealing process and to the morphology of the near interface region, much as is the case with POLY SIS structures. For the $\gamma = 0$ SIPOS contacts, an upper limit to the specific resistivity can be set at 1×10^{-4} ohm-cm^2 from device Gummel plots; although the actual value is quite likely to be far below this, the presence of other parasitic resistances does not allow a more refined determination from the device data. The ability to directly measure the voltage drop at the interface is being incorporated into the next mask set.

References:

(1) D. Dong, E. Irene, et al "Preparation and Some Properties of CVD Si-rich SiO_2 and Si_3N_4 Films", J. Electrochemical Soc. 125(5), May 1978, p819

(2) H. Yamoto, N. Oh-uchi , et al "New Technology by the Use of Doped SIPOS Films", ECS Abstracts, #168, 1979

(3) T. Matsushita, "A Silicon Heterojunction Transistor," Appl. Phys. Lett., vol 35(7), p 549, 1979

(4) A. Bennet, L. Roth "Calculation of the Optical Properties of Amorphous SiO_x Materials" Phys. Rev. B 4(8), Oct. 15, 1971, p 2686

(5) M. Hamasaki, "Crystallographic Study of SIPOS Doped with Oxygen Atoms,"J. Appl. Phys. 49(7), p 3987, 1978

(6) B. Soerowirdjo, P. Ashburn, et al "The Influence of Surface Treatments on the Electrical Characteristics of Polysilicon Emitter Bipolar Transistors" Tech. Digest IEDM, 1982, p 668

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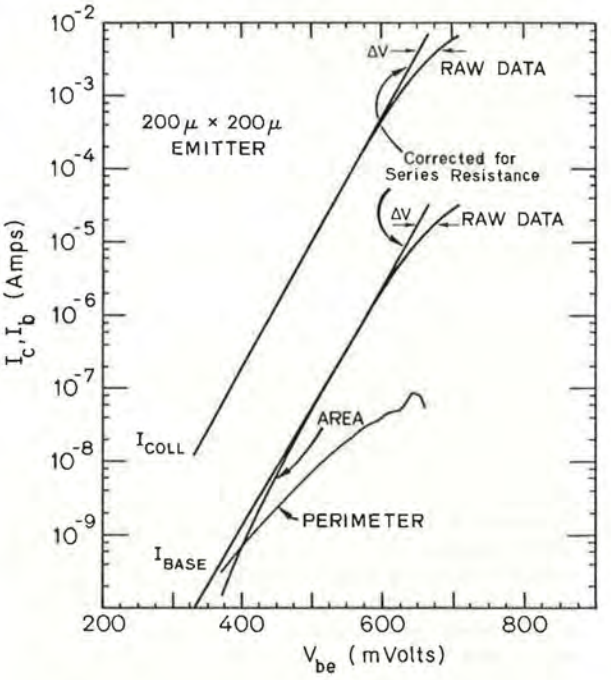


Fig. 1: Gummel plot of test bipolar structure showing area and perimeter related components.

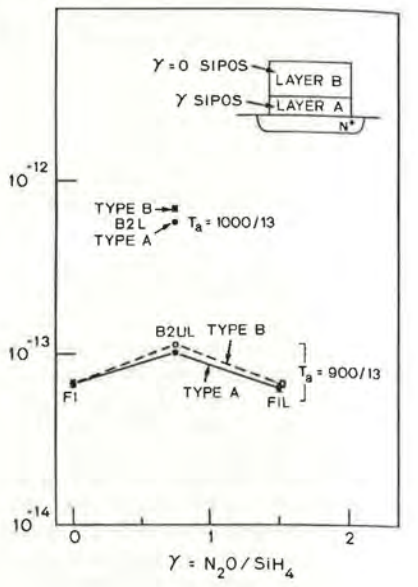


Fig.2: γ is the ratio of nitrous oxide to silane in the SIPOS deposition ambient, T_a is the anneal temperature (followed by a slash and anneal time in minutes). Layer B is a 2000 angstrom capping layer; layer A is the "active layer" ranging from 1000 to 1600 angstroms.

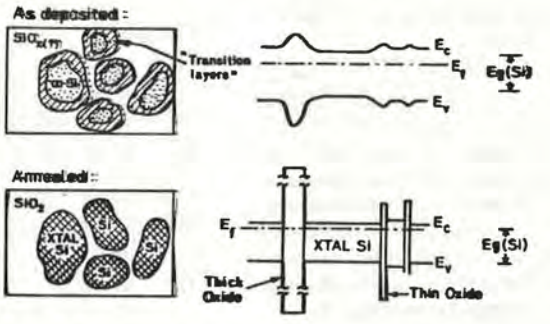


Fig. 3: (A) postulated structure of as-deposited SIPOS (B) and after annealing; the "oxide-like" regions become more SiO_2-like, accompanied by crystallization of the silicon crystallites.

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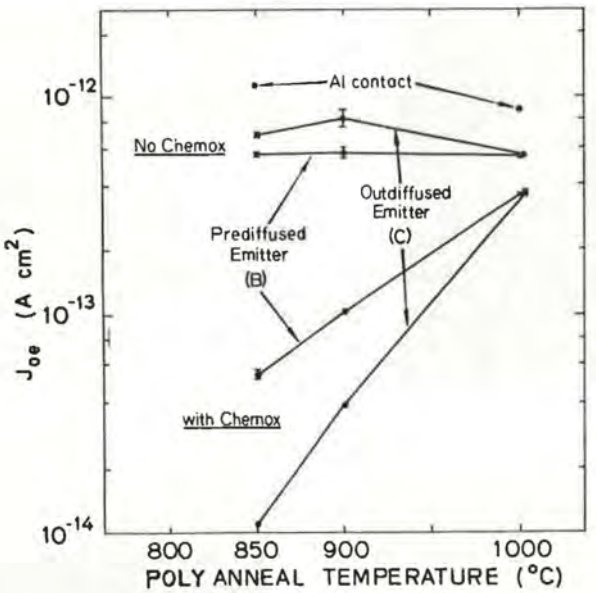


Fig. 4: emitter saturation current for POLY contacts with and without a chemically grown interfacial layer vs. anneal temperature. Thicknesses range from 3000-3600 angstroms. Note the large difference when the interfacial oxide is missing.

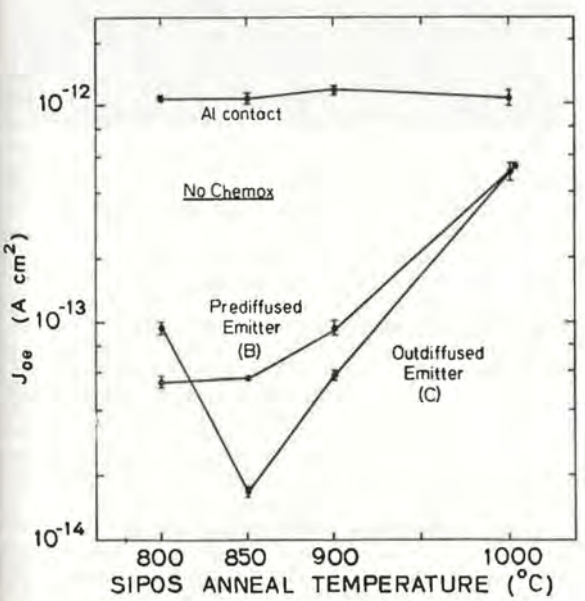


Fig. 5: emitter saturation current vs. anneal temperature for SIPOS contacts without a chemically grown interfacial oxide. The $\gamma = 0$ SIPOS layer is 3300 angstroms thick.

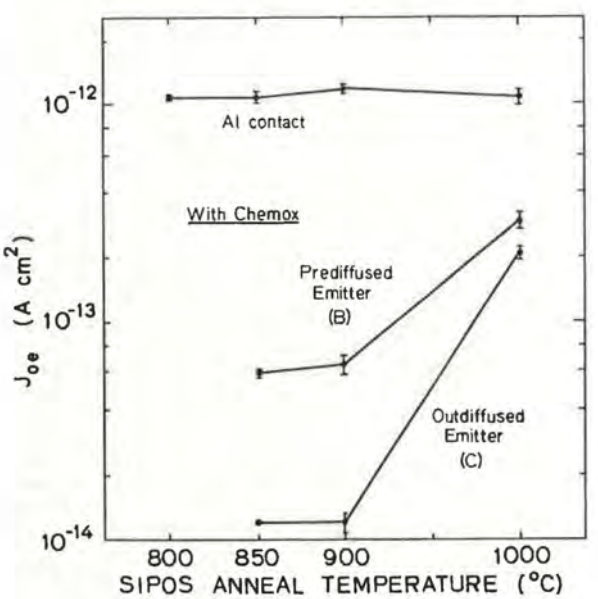
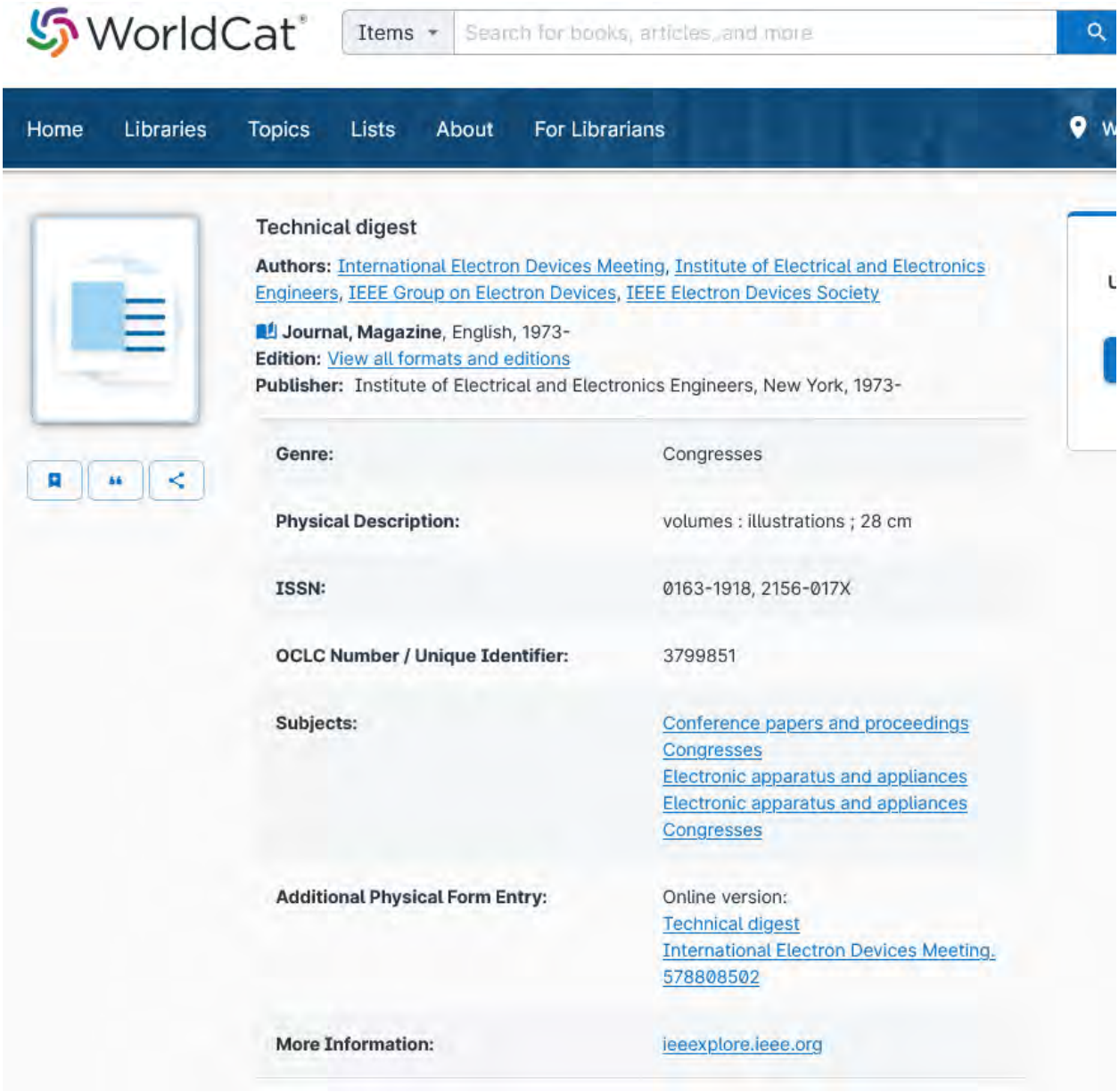


Fig. 6: emitter saturation current vs. anneal temperature for SIPOS contacts with a chemically grown interfacial oxide. The $\gamma = 0$ SIPOS layer is 3300 angstroms thick.

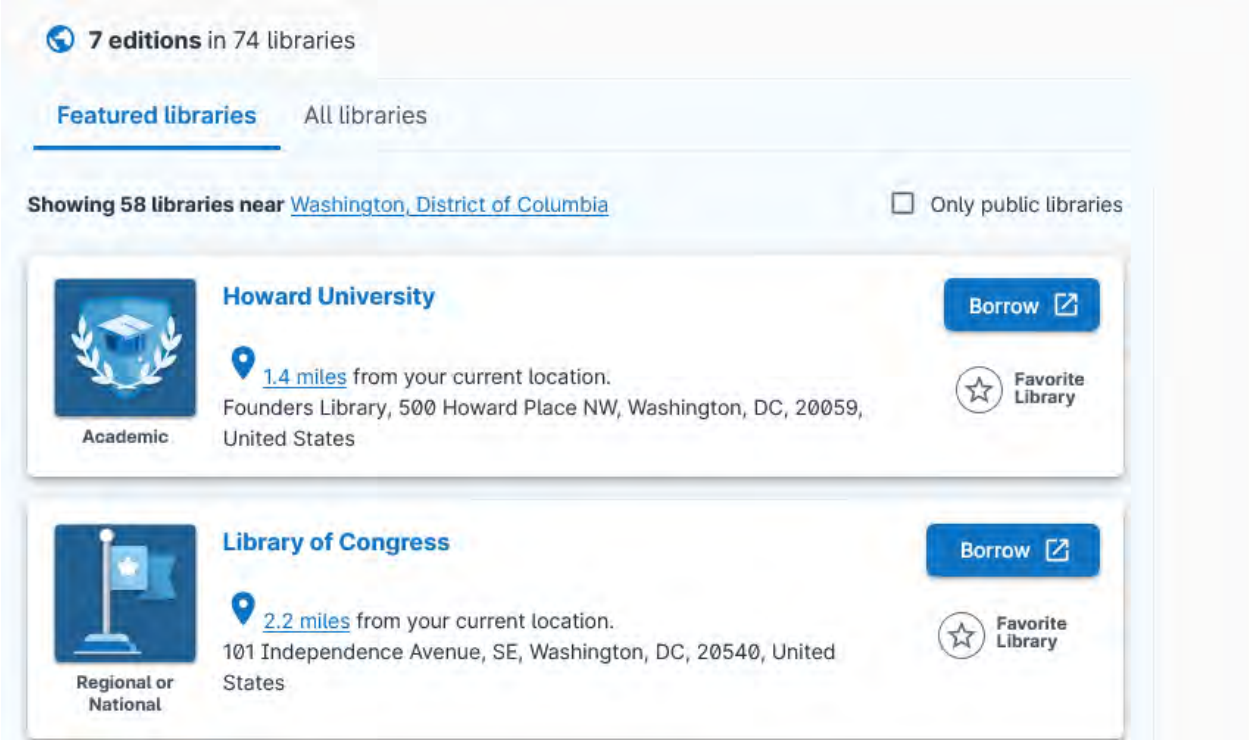
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Attachment F-4

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Attachment F-5

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Advances in crystalline silicon solar cell technology for industrial mass production

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Crystalline silicon photovoltaic (PV) cells are used in the largest quantity of all types of solar cells on the market, representing about 90% of the world total PV cell production in 2008. Crystalline silicon solar cells are also expected to have a primary role in the future PV market. This article reviews the current technologies used for the production and application of crystalline silicon PV cells. The highest energy conversion efficiency reported so far for research crystalline silicon PV cells is 25%. Standard industrial cells, however, remain limited to 15–18% with the exception of certain high-efficiency cells capable of efficiencies greater than 20%. High-efficiency research PV cells have advantages in performance but are often unsuitable for low-cost production due to their complex structures and the lengthy manufacturing processes required for fabrication. Various technologies for mono- and polycrystalline PV cells are compared and discussed with respect to the corresponding material technologies, such as silicon ingot and wafer production. High energy conversion efficiency and low processing cost can only be achieved simultaneously through the development of advanced production technologies and equipment, and some of the latest technologies that could lead to efficiencies of greater than 25% and commercially viable production costs are reviewed.

In 2008, the world annual production of photovoltaic (PV) cells reached more than 7.9 GW_p (W_p, peak power under standard test conditions) [1], and the average annual growth rate in PV cell production over the last decade has been more than 40%. Yet the electrical power generated by all PV systems around the world has been estimated to be less than 0.1% of the total world electricity generation [1]. Nevertheless, the strong growth in PV cell production is expected to continue for many years. Crystalline silicon PV cells, with over 60 years of development, have the longest production history and now account for the largest share of production, comprising up to 90% of all the solar cells produced in 2008 [1]. Silicon is safe for the environment and one of the most abundant resources on Earth, representing 26% of crustal material. The abundance and safety of silicon as a resource grants the silicon solar cell a prominent position among all the various kinds of solar cells in the PV industry. World annual PV cell production of 100 GW_p is expected to be achieved by around 2020, and the silicon PV cell is the most viable candidate to meet this demand from the point of view of suitability for large-volume production.

The crystalline silicon PV cell is one of many silicon-based semiconductor devices. The PV cell is essentially a diode with a semiconductor structure (Figure 1), and in the early years of solar cell production, many technologies for crystalline silicon cells were proposed on the basis of silicon semiconductor devices. The synergy of technologies and equipment developed for other silicon-based semiconductor devices, such as large-scale integrated circuits and the many different kinds of silicon semiconductor applications, with those developed for PV cells supported progress in both fields. Process technologies such as photolithography helped to increase energy conversion efficiency in solar cells, and mass-production technologies such as wire-saw slicing of silicon ingots developed for the PV industry were also readily applicable to other silicon-based semiconductor devices. However, the value of a PV cell per unit area is much lower than that for other silicon-based semiconductor devices. Production technologies such as silver-paste screen printing and firing for contact formation are therefore needed to lower the cost and increase the volume of production for crystalline silicon solar cells. To achieve parity with existing mains grid electricity prices, known as 'grid parity', lower material and process costs are as important as higher solar cell efficiencies. The realization

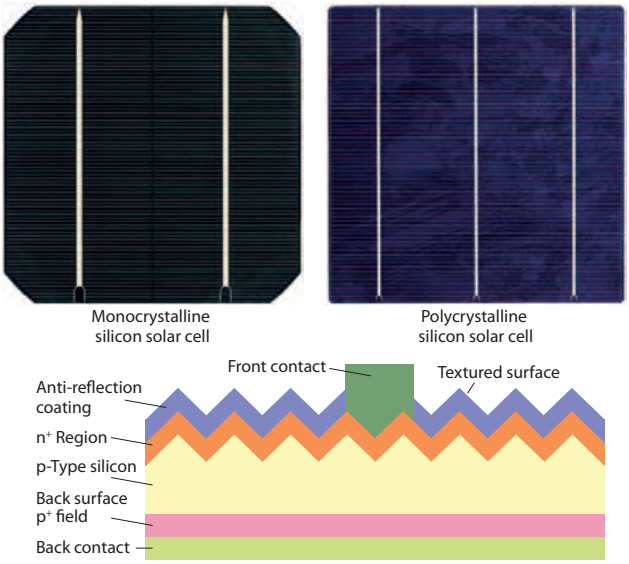


Figure 1. Typical mono- and polycrystalline silicon solar cells (upper), and simplified cross-section of a commercial monocrystalline silicon solar cell (lower) (© 2010 Sharp).

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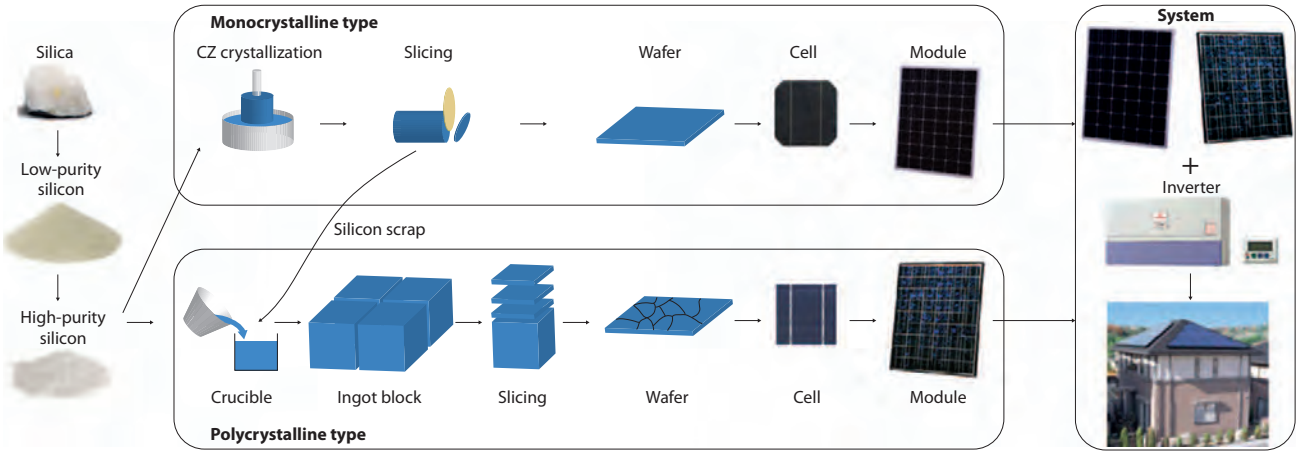


Figure 2. Production process for typical commercial crystalline silicon solar cells (© 2010 Sharp)

of high-efficiency solar cells with low process cost is currently the most important technical issue for solar cell manufacturers. Cutting the cost of producing expensive high-purity crystalline silicon substrates is one aspect of reducing the cost of silicon solar cell modules. This review covers the historical and recent technological advances in crystalline silicon solar cells from the perspective of industrial application.

Features of standard crystalline-silicon PV cells and modules

Crystalline silicon PV cells are the most popular solar cells on the market and also provide the highest energy conversion efficiencies of all commercial solar cells and modules. The structure of typical commercial crystalline-silicon PV cells is shown in Figure 1. Standard cells are produced using one of two different boron-doped p-type silicon substrates; monocrystalline and polycrystalline. The cells of each type are typically 125 mm (5 inches) or 156 mm (6 inches) square, respectively. Monocrystalline solar cells are produced from pseudo-square silicon wafer substrates cut from column ingots grown by the Czochralski (CZ) process (see Figure 2). Polycrystalline cells, on the other hand, are made from square silicon substrates cut from polycrystalline ingots grown in quartz crucibles. The front surface of the cell is covered with micrometer-sized pyramid structures (textured surface) to reduce reflection loss of incident light. An anti-reflection coating (ARC) of silicon nitride (SiN_x) or titanium oxide (TiO_x) is overlayed on the textured silicon surface to further reduce reflection loss. Crystalline silicon solar cells have highly phosphorous-doped n^+ (electron-producing) regions on the front surface of boron-doped p-type (electron-accepting) substrates to form p–n junctions. Back-surface p^+ field (BSF) regions are formed on the back surface of the silicon substrate to suppress recombination of minority carriers (photogenerated electrons). The BSF regions are usually formed by firing screen-printed aluminum paste in a belt furnace. The carriers (electrons) generated in the silicon bulk and diffusion layers are collected by silver contacts (electrodes) formed on the front and back silicon surfaces. The front contact consists of gridlines connected by a busbar to form a comb-shaped structure. The back contact is usually a series of silver stripes connected to the front bus bar of the adjacent cell via soldered copper interconnects. The contacts are usually formed by firing of screen-printed silver paste at the same time as firing for formation of the BSF regions. The front contact is similarly formed using screen-printed silver paste applied on top of the ARC layer. Contact between the front electrode and the n^+ region of the silicon substrate is achieved by firing such that the silver penetrates through the ARC layer. The screen-printed front silver contact prepared by firing to penetrate the ARC is one of the most important techniques for large-volume fabrication of modern standard crystalline silicon cells. Other techniques, such as using boron-doped BSF and nickel–copper plating contacts, are used by a small number of cell manufacturers. The efficiencies of typical commercial crystalline silicon solar cells with standard cell structures are in the range of 16–18% for monocrystalline substrates and 15–17% for polycrystalline substrates. The substrate thickness used in most standard crystalline cells is 160–240 μm. The solar cells are assembled into modules by soldering and laminating to a front glass panel using ethylene vinyl acetate as an encapsulant. The energy conversion efficiency of modules of standard solar cells is roughly 2% lower than the individual cell efficiency, falling in the range of 12–15%.

The sequence of crystalline silicon solar cell production, from raw materials to modules, is shown in Figure 2. The value chain for crystalline silicon solar cells and modules is longer than that for thin-film solar cells. There are generally three industries related to crystalline silicon solar cell and module production: metallurgical and chemical plants for raw material silicon production, monocrystalline and polycrystalline ingot fabrication and wafer fabrication by multi-wire saw, and solar cell and module production. The cost of PV production is roughly divided in half between solar cell module production and balance-of-system fabrication, which includes the inverter, cables and installation. The fabrication cost for solar cell modules includes the cost of the silicon substrate (50%), cell processing (20%) and module processing (30%). The cost share is therefore strongly affected by the market price for polysilicon feedstock, and reducing the cost of the silicon substrate remains one of the most important issues in the PV industry.

The industrial goal for PV power is to reduce the electricity generation cost to the equivalent of that for commercial grid electricity. The energy conversion efficiency of solar cells is another important issue because the efficiency influences the entire value-chain cost of the PV system, from material production to system installation. The solar cell efficiency is limited by the three loss mechanisms: photon losses due to surface reflection, silicon bulk transmission and back contact absorption; minority carrier (electrons in the p region and holes in the n region) loss due to recombination in the silicon bulk and at the surface; and heating joule loss due to series resistance in the gridlines and busbars, at the interface between the contact and silicon, and in the silicon bulk and diffusion region. In the design of solar cells and processes, these losses are minimized without lowering the productivity of the solar cells.

The electrical performance of a solar cell is determined by the short-circuit current (I_{sc}), open-circuit voltage (V_{oc}), current at the maximum power point (I_{mp}), voltage at the maximum power point (V_{mp}), maximum power (P_{max}), fill factor (FF) and energy conversion efficiency (η). In research and development, short-circuit current density (J_{sc}) is also used. An air mass 1.5 ($AM_{1.5}$) spectrum condition (1,000 W m^{-2}) is the standard test condition for terrestrial solar cells. The $AM_{1.5}$ condition is defined as 1.5 times the spectral absorbance of Earth's atmosphere;

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in contrast, the spectral absorbance for space is zero (air mass zero, AM_0). The solar energy under the $AM_{1.5}$ condition is used as the input energy for calculation of solar cell efficiency. The solar cell fill factor and efficiency are calculated using the following equations.

$$FF = \frac{P_{max}[W]}{I_{sc}[A] \times V_{oc}[V]}; (P_{max}[W] = I_{mp}[A] \times V_{mp}[V])$$
$$\eta\,[\%] = \frac{P_{max}[W] \times 100}{1{,}000\,[Wm^{-2}] \times \text{Cell area}\,[m^2]} \quad (1)$$

Efficiency improvements

Historical development

Bell Laboratory fabricated the first crystalline silicon solar cells in 1953, achieving 4.5% efficiency, followed in 1954 with devices with 6% efficiency [2,3]. In the ten years since the first demonstration, the efficiency of crystalline silicon cells was improved to around 15%, and were sufficiently efficient to be used as electrical power sources for spacecraft, special terrestrial applications such as lighthouses, and consumer products such as electronic calculators. The improvements in research-cell efficiencies achieved for various kinds of solar cells over the past 30 years are shown in Figure 3. Although crystalline silicon solar cell technologies are not yet as efficient as cells based on single-junction GaAs and multi-junction concentrators, they currently provide a good compromise between efficiency and cost.

The basic cell structure used in current industrial crystalline solar cells, which includes features such as a lightly doped n^+ layer (0.2–0.3 μm) for better blue-wavelength response, a BSF formed by a p/p^+ low/high junction on the rear side of the cell, a random pyramid-structured light-trapping surface, and an ARC optimized with respect to the refractive index of the glue used to adhere it, were developed for space and terrestrial use in the 1970s. The efficiency of monocrystalline cells for space use is in the range of 14–16% under '1 sun' AM_0 test conditions, equivalent to 15–17% at $AM_{1.5}$. These standard structures for crystalline silicon cells are still used in standard industrial crystalline cells, which offer efficiencies in the range of 14–17%.

The key technologies needed to realize efficiencies of higher than 20% were developed in the 1980s and '90s, and the latest high-efficiency crystalline silicon cells possess most of these features (Table 1).

Table 1. Key technologies for high-efficiency crystalline silicon solar cells

Minimizing photon loss
Front textured surface of random pyramid or inverted pyramid structures to reduce surface reflection loss
Single- or double-layer ARC to reduce surface reflection loss
Back-contact cell structure to reduce front contact shadow loss
Flat back surface by chemical etching of silicon to improve back reflectivity and reduce photon absorption
Back surface reflector consisted of a dielectric layer and high-reflectivity thin metal layer to reduce photon absorption
Minimizing carrier loss
Passivation of front electrode (partly in contact with highly doped silicon layer) to reduce carrier recombination under front electrode
Shallow-doped p–n junction with front surface dielectric passivation layer to reduce carrier recombination in the n^+-doped region and at the surface; heterojunction with thin amorphous layers on a crystalline silicon base in a heterojunction cell; front surface field and surface passivation for back contact in a back-junction cell
Locally p^+-doped back surface field and point contact structure to reduce carrier recombination in highly doped p^+ back region
Back surface passivation by a dielectric layer or heterojunction structure to reduce back surface recombination
Minimizing electrical loss
Fine gridline front contact to reduce series resistance of n^+-doped region
Selective emitter (deep and highly doped emitter under the contact) to reduce contact resistance of front contact with silicon surface
n-Type or p-type silicon substrates with minority carrier diffusion lengths longer than the base thickness

Monocrystalline solar cells

Representative examples of high-efficiency monocrystalline silicon PV cells are the passivated emitter rear localized (PERL) cell, the heterojunction with intrinsic thin layer (HIT) cell, and the back contact, back junction (BC-BJ) cell (Figure 4(a,b,c)). These PV cells feature many of the technologies that provide high efficiency in this type of PV cell. The PERL cell is a research PV cell with front and rear surface passivation layers, an inverted-pyramid light-trapping surface, a rear localized p^+ layer (BSF), a double-layer ARC and p-type float zone (FZ) monocrystalline silicon substrate. The bulk minority carrier lifetime in PERL cells is longer than 1 ms, and the best output parameters (V_{oc}, J_{sc}, FF and η) achieved for this type of cell are 706 mV, 42.7 mA cm^{-2}, 0.828 and 25.0% for a 4 cm^2 laboratory cell [4]. This cell approaches the limit of current technologies for the absorption of solar photons and the collection of carriers generated in the cell emitter and base. A PERL cell efficiency of 24.7% was reported almost ten years ago, and the record of 25.0% reported by researchers from the University of New South Wales (UNSW) in 2009 was obtained after re-measurement of the same cell using newer measurement techniques. The PERL cell has remained the most efficient type of monocrystalline-silicon PV cell for the past ten years [5], and has been the most popular laboratory structure of all the high-efficiency crystalline silicon PV cells. However, the full PERL design is not easy to apply to low-cost industrial production because of the necessity for multiple photolithography steps, similar to semiconductor devices with complex structures. Expensive silicon PV cells for space applications have a similar structure to the PERL cell [6]. The PLUTO cell developed for industrial use by SunTech Power has a simpler passivated emitter solar cell (PESC) design, which was also developed at the UNSW in 1985 [7], and provides efficiency of up to 19.2% in a 4 cm-square cell [8]. The PESC features front passivation, a selective emitter, and a plated front contact with fine gridlines.

The best output parameters reported for the HIT cell, which was developed for industrial use, are 729 mV, 39.5 mA cm^{-2}, 0.800 and 23.0% (V_{oc}, J_{sc}, FF and η) for a large 100.4 cm^2 cell [9]. This cell has a unique heterojunction structure consisting of very thin, amorphous

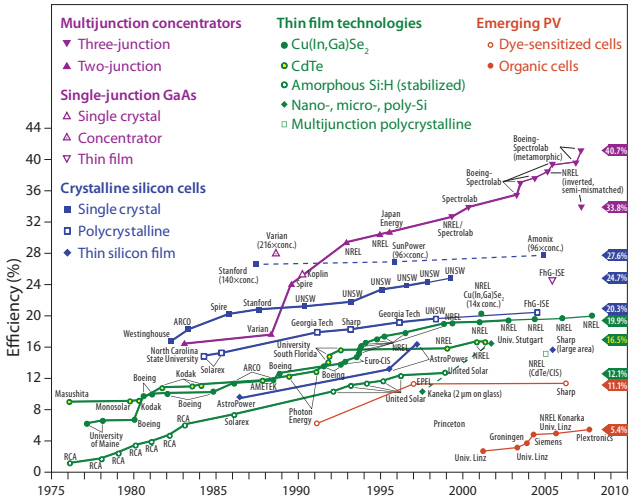


Figure 3. Best research solar cell efficiencies reported by NREL (© 2010 NREL)

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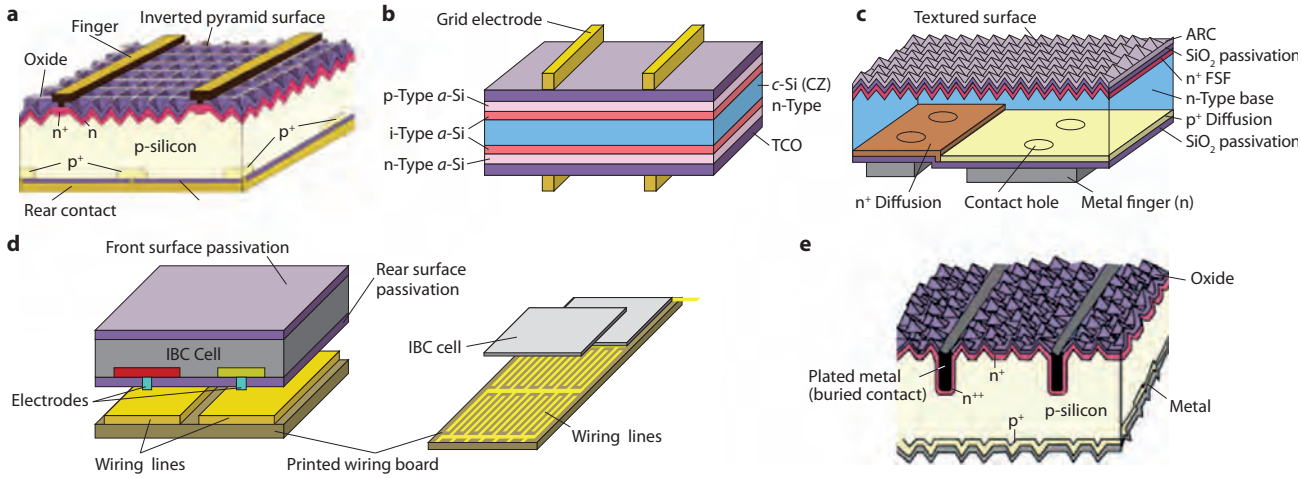


Figure 4. Schematics of various crystalline solar cell structures. (a) PERL. Adapted from Ref. 5 (© 1999 Wiley-VCH Verlag GmbH & Co. KGaA). (b) HIT. Adapted from Ref. 48 (© 2008 WIP Munich). (c) BC-BJ. Adapted from Ref. 49. (d) interdigitated back-contact (IBC) cell using surface mount technology. Adapted from Ref. 17 (© 1976 IEEE). (e) Buried-contact cell structure by BP Solar. Adapted from Ref. 40 (© 2008 IEEE). All figures reproduced with permission.

p- and n-doped layers and intrinsic amorphous layers on the front and rear surfaces of a CZ n-type monocrystalline-silicon substrate. This heterojunction structure improves V_{oc} considerably by the effects of the large energy bandgap of the front amorphous silicon layer and the excellent quality of the interface between the amorphous layer and the crystalline substrate. This cell has the additional advantage of a low temperature coefficient of about 0.30 % K^{-1} at P_{max} compare to about 0.45 % K^{-1} for standard industrial crystalline silicon PV cells. This cell has a transparent conductive oxide (TCO) ARC, which reduces the sheet resistivity of the front amorphous layers. The distinctly lower J_{sc} compared to other high-efficiency PV cells appears to be due to suppressed photocurrent collection by the front amorphous silicon layers and the bulk silicon by the effects of the lower transparency of the TCO layer compared to other ARCs and/or the lower internal quantum efficiency of the amorphous layers. The result is a weaker blue response and lower J_{sc}.

The BC-BJ cell has interdigitated n- and p-doped regions and n and p contacts on the back surface. The original BC-BJ cell, called the front surface field (FSF) cell or interdigitated back contact (IBC) cell, was fabricated and studied for space applications in the late 1970s [10,11]. The BC-BJ-structured point contact (PC) cell developed by Stanford University in the 1980s gave efficiencies of more than 20% from the outset [12]. BC-BJ cells were first fabricated for unmanned aircraft and solar race cars by SunPower in the 1990s. The cells were then extended to large-scale production for PV generation systems in the 2000s. The best conversion efficiency reported so far for a large-area industrial BC-BJ cell is 23.4% [13]. The BC-BJ cell has front and rear surface passivation layers, a random-pyramid light-trapping surface, FSF, interdigitated n- and p-doped regions on the back surface, n and p contact gridlines on n- and p-doped regions, a single-layer ARC and CZ n-type single-crystalline silicon substrate with a minority carrier lifetime of longer than 1 ms. Of all the crystalline silicon PV cell modules on the market at this time, only those based on BC-BJ cells provide the possibility of module efficiencies exceeding 20%. Several laboratories and manufactures are studying methods for improving the design and processing of BC-BJ cells [14,15]. BC-BJ cells have several advantages compared to the conventional front-contact cell structure: no gridline (sub-electrode) or busbar (main electrode) shading, a front surface with good passivation properties due to the absence of front electrodes, freedom in the design of back contacts (electrodes), and improved appearance with no front electrodes. They also provide advantages in module assembly, allowing the simultaneous interconnection of all cells on a flexible printed circuit (see Figure 4(d)). The low series resistance of interconnection formed by this type of surface-mount technology results in a high FF of 0.800, compared with around 0.75 for standard silicon PV cell modules [16,17].

Industrial cells

Monocrystalline solar cells

p-Type monocrystalline substrates sliced from boron-doped CZ ingots have been used for standard industrial PV cells for many years. In the early era of terrestrial PV cell production, small 2–5-inch-diameter CZ ingots were used, the small size and high cost of which obstructed cost reduction for monocrystalline cells. Much research and development has been devoted to reducing the production costs for CZ ingots and wafer processing over the past 20 years. CZ wafers with side lengths of 125 and 156 mm, sliced from 6- and 8-inch-diameter ingots, respectively, are now widely used for monocrystalline silicon PV cell fabrication. The fabrication of monocrystalline cells and modules using wafers of the same size as those used for polycrystalline cell production has improved the competitiveness of monocrystalline cells against their polycrystalline counterparts in terms of manufacturing cost per output watt. Monocrystalline cells represented 38% of all solar cells manufactured in 2008 [1].

There are large differences between the efficiencies of the best research crystalline silicon PV cells and the corresponding industrial cells. The efficiencies of standard industrial monocrystalline PV cells remain in the range of 16–18%, considerably lower than the 25% efficiency levels of the best research cells. Industrial cells are restricted by economic factors to simple cells that are suitable for high-speed, automated production using low-cost materials. Simple design features, such as front surface texturing and BSF similar, to those developed for terrestrial crystalline-silicon PV cells in the early 1980s are still adopted in most current industrial crystalline cells. To improve cell efficiencies, many cell manufactures are systematically attempting to introduce high-efficiency features, such as finer gridlines, selective emitters or more shallowly doped n^+ regions, into existing manufacturing processes. The BC-BJ cells and HIT cells have exceptionally high efficiencies for industrial monocrystalline PV cells, but have complex cell structures that require a much longer production process and more specialized equipment compared with the other industrial cells. As a result, it is difficult for these advanced cell types and modules to compete commercially in terms of production cost per output watt. There remains a dilemma in the balance between efficiency improvement and cost reduction for solar cells and modules using existing manufacturing technologies. Innovative and simple manufacturing technologies and equipment for the fabrication of high-efficiency solar cells are therefore needed in order to realize significant cost reductions for the production of crystalline silicon PV modules.

Another drawback of the monocrystalline cell technologies is that monocrystalline cells based on p-type CZ silicon substrates are susceptible to light-induced degradation (LID) caused by the recombination

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of reactive boron–oxygen complexes (B *s*–O 2*i*). Many studies have been undertaken in attempts to eliminate LID effects in monocrystalline-silicon PV cells, and permanent deactivation of the complex at high temperature (> 170 °C) has been reported [18]. Boron-doped magnetic-field CZ wafers and gallium-doped CZ wafers also show promise for eliminating LID effects in monocrystalline solar cells, and CZ-silicon cells based on phosphorous-doped n-type CZ wafers are also free of LID effects. The high-efficiency PV cells of SunPower and Sanyo are made using n-type CZ-silicon wafers.

Polycrystalline solar cells

Polycrystalline silicon ingots and wafers were developed as a means of reducing the production costs for silicon ingots, and have been investigated since the mid-1970s [19,20]. Modern polycrystalline furnaces are designed for maximum productivity, casting ingots of around 450 kg. Polycrystalline cells are currently the most widely produced cells, making up about 48% of world solar cell production in 2008 [1]. Standard polycrystalline industrial cells offer efficiencies of 15–17%, roughly 1% lower than for monocrystalline cells fabricated on the same production lines. The efficiencies of polycrystalline cell modules, however, are almost the same as those for monocrystalline cells (14%) due to the higher packing factor of the square polycrystalline cells; monocrystalline cells are fabricated from pseudo-square CZ wafers and have relatively poor packing factors.

The efficiencies of both monocrystalline and polycrystalline PV cells will be improved in the future through the introduction of high-efficiency structures. The difference in efficiency between monocrystalline and polycrystalline cells is expected to become larger with the introduction of such high-efficiency structures due to the difference in crystal quality (*i.e.* minority carrier lifetimes). The best of the current research polycrystalline silicon cells, a PERL cell developed by Fraunhofer ISE [21], provides an energy conversion efficiency of 20.3%. This PERL cell has a laser-fired contact back structure that gives a V_{oc} of as high as 664 mV. The efficiency of this polycrystalline cell, however, remains about 5% lower than that for the best of the research monocrystalline PERL cells, attributable mainly to the quality difference between mono- and polycrystalline substrates. Polycrystalline substrates are subject to higher rates of minority carrier recombination, both at active grain boundaries and within crystalline grains due to high dislocation and impurity densities in comparison with FZ or CZ monocrystalline substrates. A considerable amount of research and development has been conducted on improving the efficiencies of polycrystalline solar cells over many years, by both public and industrial laboratories, and recent high-efficiency polycrystalline silicon solar cells now have the features listed in Table 2. These features are generally the same as for recent monocrystalline solar cells.

Table 2. Key technologies for high-efficiency polycrystalline silicon solar cells

Minimizing photon loss
Front textured surface by acid etching (including honeycomb texturing) or reactive ion etching
Chemical polishing (etching) of back surface
Back surface reflector consisting of a dielectric layer and highly reflective thin metal layer
Minimizing carrier loss
Shallowly doped n^+ regions with SiN_x surface passivation layer
p-Type silicon substrates with minority carrier diffusion length longer than base thickness
Local BSF and point contacts, such as the laser fired contacts
Back surface passivation with SiO_2 and/or SiN_x layers
Minimizing electrical loss
Fine gridlines for front electrode by advanced screen printing techniques, such as stencil printing [46]
Selective emitter (deep, highly doped emitter beneath front electrodes)
Deposition of seed layers then copper plating for metallization instead of screen-printed silver paste

The honeycomb-structured polycrystalline solar cells demonstrated recently by Mitsubishi Electric exhibit efficiencies of over 19.3% and come in large 15 cm × 15 cm cells [22]. These polycrystalline cells have a distinct front honeycomb-textured surface to reduce light reflection, and the introduction of this front textured surface has resulted in a high J_{sc} of 37.5 mA cm^{-2} for cells with screen-printed and fired silver-paste electrodes. This cell also has the PERL structures of front surface passivation, rear surface passivation with local BSF, and a selective emitter for improved cell efficiency.

Approaches to reduce cell costs also include using thinner silicon wafers. High-efficiency (18.1%) polycrystalline silicon cells fabricated using 100 µm-thick wafers were reported by Sharp in 2009 [23]. The electrical performance of crystalline silicon PV cells with the standard back surface structure of an aluminum-alloyed BSF decreases as the substrate becomes thinner. High-efficiency polycrystalline cells with an SiN_x passivation layer and thin aluminum reflector on the back silicon surface display less of a performance degradation with decreasing substrate thickness for substrates of 100–180 µm in thickness. Cells with rear passivation and local BSF on 100 µm-thick substrates provide the additional advantage of less cell bowing compared with the standard aluminum alloyed BSF cells on substrates of the same thickness.

New types of back-contact polycrystalline cells, such as metal wrap through (MWT) cells and emitter wrap through (EWT) cells (Figure 5), have also been developed by institutes and companies such as ECN, Kyocera and Advent Solar [24–26]. BC-BJ cells without a front p–n junction require high-quality monocrystalline substrates with high minority carrier lifetimes. The WT back-contact cells, however, are suitable for use with polycrystalline substrate having relatively short minority carrier lifetimes (related to cell thickness). The front p–n junctions in these cells can collect most carriers generated in the region from the front n-doped layer to the back substrate surface. These back-contact cells have laser-drilled through-holes that can wrap through front n-electrodes and/or n-doped regions to the back surfaces. The MWT cells require only a relatively small number of through-holes to direct photogenerated electrons to the back surface through the metal electrodes and n-doped emitters, and produce higher collection photocurrents due to absence of a bus bar (main electrode) on the front surface as in conventional cells. A high J_{sc} of 37.3 mA cm^{-2} and an efficiency of 18.3% were reported for a recent MWT cell by Kyocera [26], and the module efficiency for MWT cell modules by ECN, 16.4%, is the highest reported to date [25].

The EWT cells have a larger number of close-spaced through-holes, which direct photogenerated electrons to the back surface solely through n-doped emitters. The EWT cells produce even higher photocurrents by eliminating the both busbar (main electrode) and gridline (sub-electrode) shading on the front surface. A high J_{sc} of 37.5 mA cm^{-2} and efficiency of 17.1% were reported recently for EWT cells by Q-Cells. The target for industrial polycrystalline PV cells is to realize average cell efficiencies of 17% in large-scale production [24].

Many methods have been investigated to improve the quality of

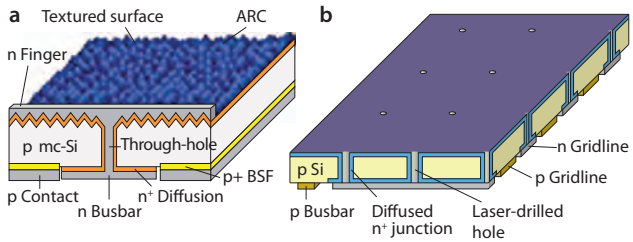


Figure 5. Schematics of back-contact solar cell structures. (a) MWT. Adapted from Ref. 26 (© 2008 WIP Munich). (b) EWT. Adapted from Ref. 25 (© 2008 IEEE). All figures reproduced with permission.

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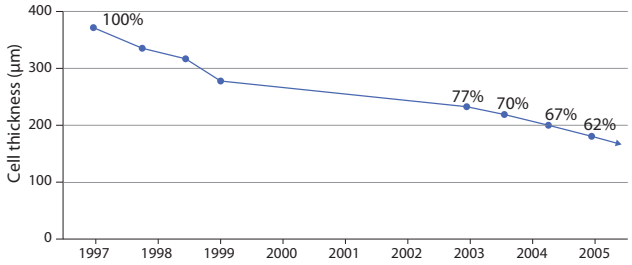


Figure 6. Reduction of silicon wafer thickness by Sharp (© 2010 Sharp)

polycrystalline substrates to match that of the more expensive CZ monocrystalline wafers. The dendritic casting method is one such approach that allows the grain orientation and size to be controlled, resulting in high-quality dendritic crystals with parallel twinning. Solar cells based on dendritic polycrystalline wafers show efficiencies of as high as 17%, comparable to the efficiencies provided by CZ monocrystalline cells using the same cell fabrication process [27].

Materials and processing

The raw, high-purity polysilicon material used for the fabrication of crystalline silicon solar cells is generally made by the Siemens method. The market price for raw silicon is affected by the demand–supply balance for solar cell and semiconductor fabrication, and can fluctuate markedly. In 2006–2008, for example, the cost of raw silicon as a proportion of total solar cell module cost jumped from 20–30% to more than 50% due to a market shortage of silicon. Reducing the cost of silicon in a cell module by reducing the substrate thickness is therefore an important aspect of achieving overall cost reductions for solar cell modules. Wire-saw wafer slicing is one of the key production technologies for industrial crystalline silicon PV cells, and improvements in wafer slicing technology have resulted in a reduction in raw wafer thickness from 370 μm to 180 μm since 1997 for Sharp industrial polycrystalline-silicon cells (Figure 6). To introduce wafers thinner than 150 μm, sophisticated manufacturing processes suitable for ultrathin wafers will be needed, and the processes will need to provide high processing speed and high manufacturing yield in each of the process steps of wafer slicing, cell fabrication and module assembly.

Several alternative growth methods have been proposed over the past four decades for the production of polycrystalline substrates directly from molten silicon, including edge-defined film-fed growth (EFG), string ribbon growth (SRG), and ribbon growth on substrate (RGS) [28–30]. These methods potentially make it possible to reduce the amount of silicon used in PV cell fabrication. The EFG and SRG methods are used on industrial production scales by SCHOTT Solar and Evergreen Solar, respectively [31]. These two methods have the advantages of low silicon consumption per W_p and high cell efficiencies in comparison with the RGS method. These methods afford inexpensive but slightly wavey polycrystalline substrates in comparison with the standard polycrystalline substrates. Recently manufactured cells based on direct-grown substrates have almost the same efficiencies as those of standard cast-silicon polycrystalline cells. However, the smaller EFG- and SRG-based cells, which are roughly half the size of standard industrial cells, incur higher cell and module processing costs. A crystallization on dipped substrate method, which can be used to produce standard-sized wafers (156 mm × 156 mm) directly from molten silicon in a crucible, was recently proposed by Sharp [32].

The front emitter layer of crystalline silicon PV cells is formed by phosphorus diffusion techniques in a quartz tube or belt furnace. Solid P_2O_5 or liquid $POCl_3$ is used as the phosphorus diffusion source. Phosphorous diffusion techniques the exploit gettering effects to reduce impurity densities in a silicon wafer and thereby improve minority carrier lifetime have been demonstrated to be effective provided diffusion is conducted under phosphorus supersaturation conditions (doping level above the solid solubility in silicon) [33–35].

The BSF layers in industrial cells are formed by alloying of screen-printed aluminum paste in a belt furnace. This process provides high productivity and relatively low process cost for BSF formation. Aluminum-paste alloying has the additional advantage of inducing wafer gettering effects in both polycrystalline and monocrystalline silicon PV cells similar to the phosphorus diffusion technologies [36,37]. Metal impurities, such as iron or copper, can be eliminated from bulk silicon by aluminum gettering effects, which can improve the minority carrier diffusion length.

The screen printing and firing of silver paste to make contact with the bulk silicon surface by penetrating the ARC is a well-established, simple and fast process for forming front and rear electrodes. It is also the most widely used and lowest-cost method for forming electrodes in industrial crystalline silicon PV cells. The front gridlines are designed so as to optimize the trade-off between shadow loss and series resistance. As an alternative to the screen-printed silver paste approach, plated electrodes of layered nickel, copper and silver have been developed by researchers at the UNSW for use in buried-contact (BC) cells [38,39]. The BC cell fabricated by BP Solar is shown in Figure 4(e) [40]. Crystalline silicon PV cells with plated electrodes have excellent electrical characteristics due to their low series resistance and fine gridlines, which result in a much smaller shadow area. However, plated electrodes, which are formed by a wet process, have not yet become as widely used as the screen-printed silver paste electrodes. The silver used as the electrode material in crystalline silicon cells will become a critical material resource when crystalline silicon solar cell production reaches the large volumes predicted in the future. Copper and aluminum have therefore been considered as substitutes for silver in silicon PV contacts.

Future views on crystalline silicon solar cells

Industrial solar cells module must reach a price level of \$1/W_p with a total system price level of \$2/W_p to reach grid parity, and to become competitive with coal or nuclear power generation will need to be mass produced at a total system cost of less than \$1/W_p. Achieving even a module price of \$1/W_p will require modules to be produced at a cost of less than 0.7\$/W_p. Although such low costs remain very challenging for modules based on crystalline silicon solar cells, cost reductions to such a level are considered to be possible based on the technologies presented in this review, and the cost reduction must be accomplished while public incentives for PV systems remain in effect. The annual production volume for all kinds of solar cells is expected to exceed 100 GW_p/year by around 2020. Crystalline silicon cell modules have a long history of proven field operation and offer high efficiencies while presenting fewer resource issues than many competing technologies. As such, crystalline silicon PV cells are expected to be strongly represented in the future solar cell market.

To reach these future price levels, new technologies as listed in Table 3 will be needed for crystalline silicon solar cells and modules. New technologies to break through the efficiency barrier of 25% for

Table 3. New technologies for high-efficiency crystalline silicon solar cells and modules

Novel technologies to break through efficiency barrier of 25%
Wafer slicing technologies and equipment for ultrathin (50 μm) wafers
Direct slicing technologies and equipment for ultrathin wafers without kerf loss [47]
Production technologies and equipment for solar cells and modules based on ultrathin wafers
High-quality polycrystalline ingot technologies providing performance comparable to monocrystalline cells
Low-cost contact-forming technologies and materials to replace screen-printed and fired silver paste
Low concentration (around 10×) and high efficiency module technologies to minimize total PV system cost

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crystalline silicon PV cells are being studied by many researchers and institutes around the world, but there have yet to be any practical improvements in cell efficiency. The peak theoretical efficiency in a crystalline silicon solar cell based on a single homojunction and a bulk silicon energy bandgap of 1.1 eV is 30% under 1 sun $AM_{1.5}$ illumination. To break through this ideal efficiency limit based on existing Schockley and Queisser solar cell theory, novel technologies based on quantum dot (QD) and quantum well structures have been proposed and studied by many researchers. Multi-junction designs have been attempted in many forms for improving solar cell efficiency beyond that of a single-junction cell. For example, a triple-junction solar cell with a silicon bottom cell is expected to give efficiencies of more than 40%. Researchers at the UNSW have also proposed a silicon-based tandem junction solar cell incorporating silicon QD technology [41]. An effective bandgap of up to 1.7 eV has been demonstrated for 2 nm-diameter silicon QDs embedded in SiO_2 [42]. Photon management, such as up- and down-conversion and plasmonic effects, are other potential approaches that could add extra efficiency based on existing high-efficiency silicon cells [43–45]. These technologies aim at shifting the photon energy of sunlight to match the sensitivity of the solar cell by adding special optical features (*e.g.* a fluorescent coating layer including rare-earth elements for up-and down-conversion) to the front and/or rear surface of the cells without modifying the structure of the solar cell itself.

These high-efficiency technologies, however, generally incur higher production costs compared to standard silicon cells. Cell and module manufacturing technologies that satisfy both high efficiency and low cost will be essential for industrial production in the near future. The impacts of novel technologies such as QDs and photon management will be interesting to watch as research and development on crystalline silicon solar cells continues.

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Author profile



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Advances in crystalline silicon solar cell technology for industrial mass production

Tatsuo Saga

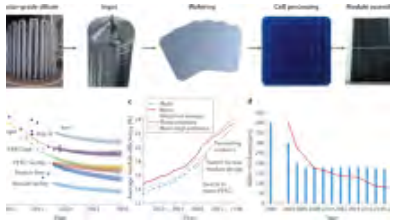
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Abstract

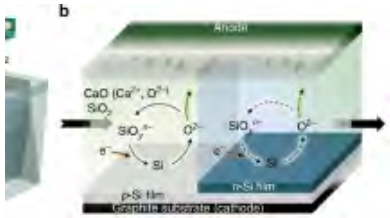
Crystalline silicon photovoltaic (PV) cells are used in the largest quantity of all types of solar cells on the market, representing about 90% of the world total PV cell production in 2008. Crystalline silicon solar cells are also expected to have a primary role in the future PV market. This article reviews the current technologies used for the production and application of crystalline silicon PV cells. The highest energy conversion efficiency reported so far for research crystalline silicon PV cells is 25%. Standard industrial cells, however, remain limited to 15–18% with the exception of certain high-efficiency cells capable of efficiencies greater than 20%. High-efficiency research PV cells have advantages in performance but are often unsuitable for low-cost production due to their complex structures and the lengthy manufacturing processes required for fabrication. Various technologies for mono- and polycrystalline PV cells are compared and discussed with respect to the corresponding material technologies, such as silicon ingot and wafer production. High energy conversion efficiency and low processing cost can only be achieved simultaneously through the development of advanced production technologies and equipment, and some of the latest technologies that could lead to efficiencies of greater than 25% and commercially viable production costs are reviewed.

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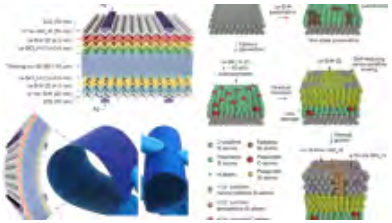
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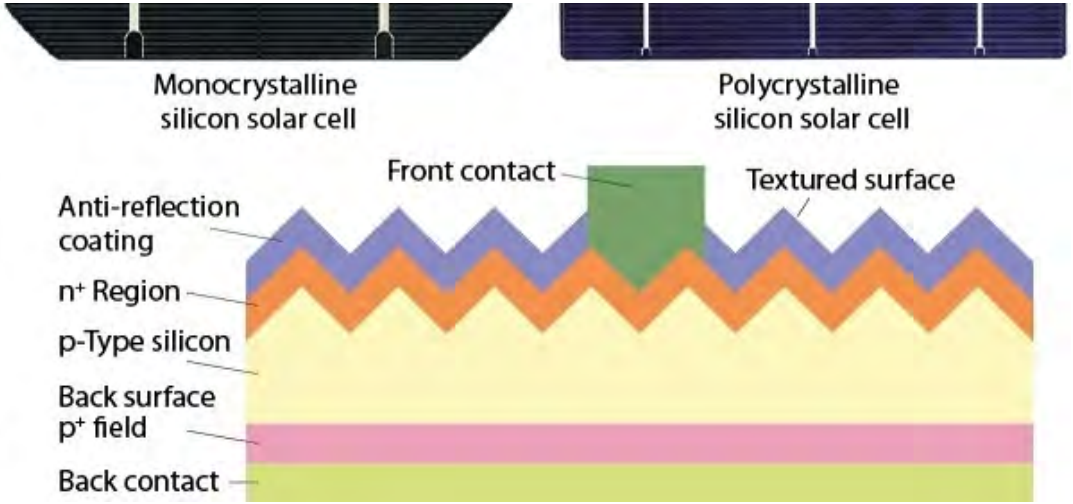
Main

In 2008, the world annual production of photovoltaic (PV) cells reached more than 7.9 GW_p (W_p, peak power under standard test conditions)[1], and the average annual growth rate in PV cell production over the last decade has been more than 40%. Yet the electrical power generated by all PV systems around the world has been estimated to be less than 0.1% of the total world electricity generation[1]. Nevertheless, the strong growth in PV cell production is expected to continue for many years. Crystalline silicon PV cells, with over 60 years of development, have the longest production history and now account for the largest share of production, comprising up to 90% of all the solar cells produced in 2008[1]. Silicon is safe for the environment and one of the most abundant resources on Earth, representing 26% of crustal material. The abundance and safety of silicon as a resource grants the silicon solar cell a prominent position among all the various kinds of solar cells in the PV industry. World annual PV cell production of 100 GW_p is expected to be achieved by around 2020, and the silicon PV cell is the most viable candidate to meet this demand from the point of view of suitability for large-volume production.

The crystalline silicon PV cell is one of many silicon-based semiconductor devices. The PV cell is essentially a diode with a semiconductor structure (Figure 1), and in the early years of solar cell production, many technologies for crystalline silicon cells were proposed on the basis of silicon semiconductor devices. The synergy of technologies and equipment developed for other silicon-based semiconductor devices, such as large-scale integrated circuits and the many different kinds of silicon semiconductor applications, with those developed for PV cells supported progress in both fields. Process technologies such as photolithography helped to increase energy conversion efficiency in solar cells, and mass-production technologies such as wire-saw slicing of silicon ingots developed for the PV industry were also readily applicable toother silicon-based semiconductor devices. However, the value of a PV cell per unit area is much lower than that for other silicon-based semiconductor devices. Production technologies such as silver-paste screen printing and firing for contact formation are therefore needed to lower the cost and increase the volume of production for crystalline silicon solar cells. To achieve parity with existing mains grid electricity prices, known as ‘grid parity’, lower material and process costs are as important as higher solar cell efficiencies. The realization of high-efficiency solar cells with low process cost is currently the most important technical issue for solar cell manufacturers. Cutting the cost of producing expensive high-purity crystalline silicon substrates is one aspect of reducing the cost of silicon solar cell modules. This review covers the historical and recent technological advances in crystalline silicon solar cells from the perspective of industrial application.

Figure 1





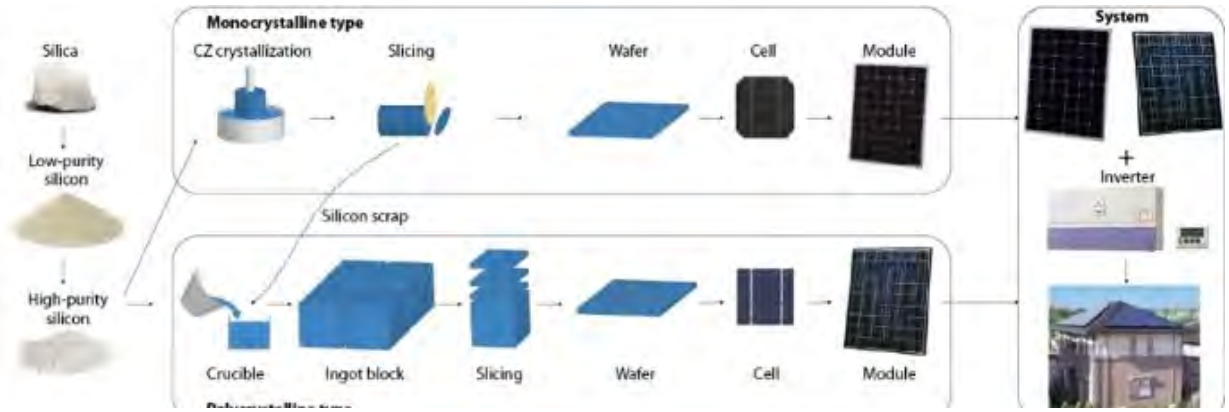
Typical mono- and polycrystalline silicon solar cells (upper), and simplified cross-section of a commercial monocrystalline silicon solar cell (lower) (© 2010 Sharp).

Features of standard crystalline-silicon PV cells and modules

Crystalline silicon PV cells are the most popular solar cells on the market and also provide the highest energy conversion efficiencies of all commercial solar cells and modules. The structure of typical commercial crystalline-silicon PV cells is shown in Figure 1. Standard cells are produced using one of two different boron-doped p-type silicon substrates; monocrystalline and polycrystalline. The cells of each type are typically 125 mm (5 inches) or 156 mm (6 inches) square, respectively. Monocrystalline solar cells are produced from pseudo-square silicon wafer substrates cut from column ingots grown by the Czochralski (CZ) process (see Figure 2). Polycrystalline cells, on the other hand, are made from square silicon substrates cut from polycrystalline ingots grown in quartz crucibles. The front surface of the cell is covered with micrometer-sized pyramid structures (textured surface) to reduce reflection loss of incident light. An anti-reflection coating (ARC) of silicon nitride (SiN_x) or titanium oxide (TiO_x) is overlayed on the textured silicon surface to further reduce reflection loss. Crystalline silicon solar cells have highly phosphorous-doped n_+ (electron-producing) regions on the front surface of boron-doped p-type (electron-accepting) substrates

to form p–n junctions. Back-surface p_+ field (BSF) regions are formed on the back surface of the silicon substrate to suppress recombination of minority carriers (photogenerated electrons). The BSF regions are usually formed by firing screen-printed aluminum paste in a belt furnace. The carriers (electrons) generated in the silicon bulk and diffusion layers are collected by silver contacts (electrodes) formed on the front and back silicon surfaces. The front contact consists of gridlines connected by a busbar to form a comb-shaped structure. The back contact is usually a series of silver stripes connected to the front bus bar of the adjacent cell via soldered copper interconnects. The contacts are usually formed by firing of screen-printed silver paste at the same time as firing for formation of the BSF regions. The front contact is similarly formed using screen-printed silver paste applied on top of the ARC layer. Contact between the front electrode and the n_+ region of the silicon substrate is achieved by firing such that the silver penetrates through the ARC layer. The screen-printed front silver contact prepared by firing to penetrate the ARC is one of the most important techniques for large-volume fabrication of modern standard crystalline silicon cells. Other techniques, such as using boron-doped BSF and nickel–copper plating contacts, are used by a small number of cell manufacturers. The efficiencies of typical commercial crystalline silicon solar cells with standard cell structures are in the range of 16–18% for monocrystalline substrates and 15–17% for polycrystalline substrates. The substrate thickness used in most standard crystalline cells is 160–240 μm. The solar cells are assembled into modules by soldering and laminating to a front glass panel using ethylene vinyl acetate as an encapsulant. The energy conversion efficiency of modules of standard solar cells is roughly 2% lower than the individual cell efficiency, falling in the range of 12–15%.

Figure 2





Production process for typical commercial crystalline silicon solar cells (© 2010 Sharp)

The sequence of crystalline silicon solar cell production, from raw materials to modules, is shown in Figure 2. The value chain for crystalline silicon solar cells and modules is longer than that for thin-film solar cells. There are generally three industries related to crystalline silicon solar cell and module production: metallurgical and chemical plants for raw material silicon production, monocrystalline and polycrystalline ingot fabrication and wafer fabrication by multi-wire saw, and solar cell and module production. The cost of PV production is roughly divided in half between solar cell module production and balance-of-system fabrication, which includes the inverter, cables and installation. The fabrication cost for solar cell modules includes the cost of the silicon substrate (50%), cell processing (20%) and module processing (30%). The cost share is therefore strongly affected by the market price for poly-silicon feedstock, and reducing the cost of the silicon substrate remains one of the most important issues in the PV industry.

The industrial goal for PV power is to reduce the electricity generation cost to the equivalent of that for commercial grid electricity. The energy conversion efficiency of solar cells is another important issue because the efficiency influences the entire value-chain cost of the PV system, from material production to system installation. The solar cell efficiency is limited by the three loss mechanisms: photon losses due to surface reflection, silicon bulk transmission and back contact absorption; minority carrier (electrons in the p region and holes in the n region) loss due to recombination in the silicon bulk and at the surface; and heating joule loss due to series resistance in the gridlines and busbars, at the interface between the contact and silicon, and in the silicon bulk and diffusion region. In the design of solar cells and processes, these losses are minimized without lowering the productivity of the solar cells.

The electrical performance of a solar cell is determined by the short-circuit current (I_{sc}), open-circuit voltage (V_{oc}), current at the maximum power point (I_{mp}), voltage at the maximum power point (V_{mp}), maximum power (P_{max}), fill factor (FF) and energy conversion efficiency (η). In research and development, short-circuit current density (J_{sc}) is also used. An air mass 1.5 ($AM_{1.5}$)

spectrum condition (1,000 W m_{-2}) is the standard test condition for terrestrial solar cells. The $AM_{1.5}$ condition is defined as 1.5 times the spectral absorbance of Earth's atmosphere; in contrast, the spectral absorbance for space is zero (air mass zero, AM_0). The solar energy under the $AM_{1.5}$ condition is used as the input energy for calculation of solar cell efficiency. The solar cell fill factor and efficiency are calculated using the following equations.

$$FF = \frac{P_{max}[W]}{I_{sc}[A] \times V_{oc}[V]}; (P_{max}[W] = I_{mp}[A] \times V_{mp}[V])$$

$$\eta\,[\%] = \frac{P_{max}[W] \times 100}{1,000\,[W m^{-2}] \times \text{Cell area}\,[m^2]}$$

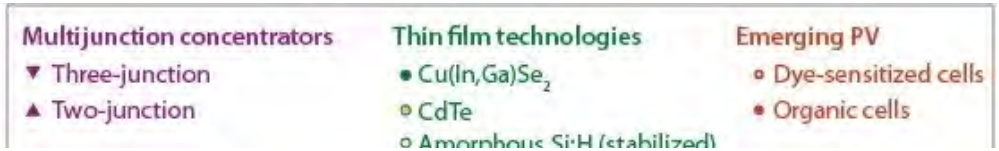
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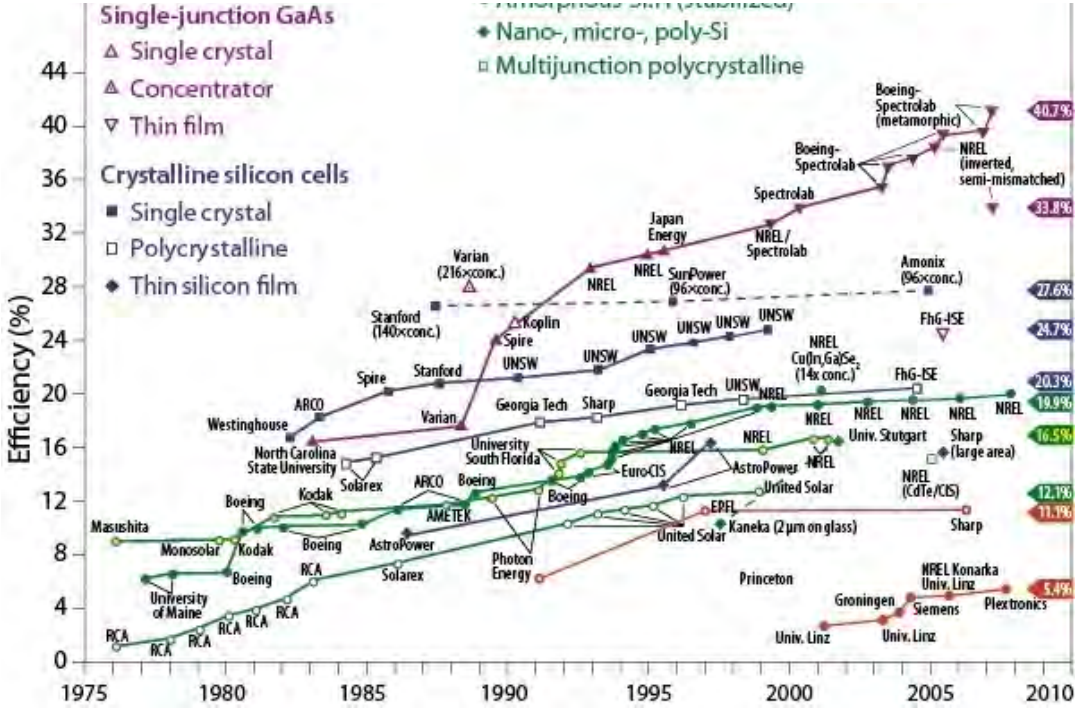
Efficiency improvements

Historical development

Bell Laboratory fabricated the first crystalline silicon solar cells in 1953, achieving 4.5% efficiency, followed in 1954 with devices with 6% efficiency [2,3]. In the ten years since the first demonstration, the efficiency of crystalline silicon cells was improved to around 15%, and were sufficiently efficient to be used as electrical power sources for spacecraft, special terrestrial applications such as lighthouses, and consumer products such as electronic calculators. The improvements in research-cell efficiencies achieved for various kinds of solar cells over the past 30 years are shown in Figure 3. Although crystalline silicon solar cell technologies are not yet as efficient as cells based on single-junction GaAs and multi-junction concentrators, they currently provide a good compromise between efficiency and cost.

Figure 3





Best research solar cell efficiencies reported by NREL (© 2010 NREL)

The basic cell structure used in current industrial crystalline solar cells, which includes features such as a lightly doped n_+ layer (0.2–0.3 µm) for better blue-wavelength response, a BSF formed by a p/p_+ low/high junction on the rear side of the cell, a random pyramid-structured light-trapping surface, and an ARC optimized with respect to the refractive index of the glue used to adhere it, were developed for space and terrestrial use in the 1970s. The efficiency of monocrystalline cells for space use is in the range of 14–16% under '1 sun' AM_0 test conditions, equivalent to 15–17% at $AM_{1.5}$. These standard structures for crystalline silicon cells are still used in standard industrial crystalline cells, which offer efficiencies in the range of 14–17%.

The key technologies needed to realize efficiencies of higher than 20% were developed in the 1980s and '90s, and the latest high-efficiency crystalline silicon cells possess most of these features (Table 1).

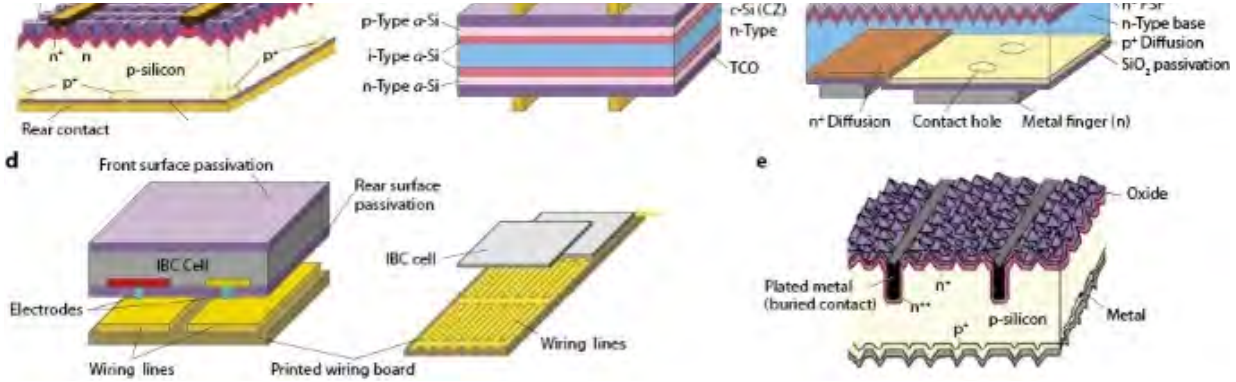
Table 1 Key technologies for high-efficiency crystalline silicon solar cells

Monocrystalline solar cells

Representative examples of high-efficiency monocrystalline silicon PV cells are the passivated emitter rear localized (PERL) cell, the heterojunction with intrinsic thin layer (HIT) cell, and the back contact, back junction (BC-BJ) cell (Figure 4(a,b,c)). These PV cells feature many of the technologies that provide high efficiency in this type of PV cell. The PERL cell is a research PV cell with front and rear surface passivation layers, an inverted-pyramid light-trapping surface, a rear localized p_+ layer (BSF), a double-layer ARC and p-type float zone (FZ) monocrystalline silicon substrate. The bulk minority carrier lifetime in PERL cells is longer than 1 ms, and the best output parameters (V_{oc}, J_{sc}, FF and η) achieved for this type of cell are 706 mV, 42.7 mA cm_{-2}, 0.828 and 25.0% for a 4 cm^2 laboratory cell[4]. This cell approaches the limit of current technologies for the absorption of solar photons and the collection of carriers generated in the cell emitter and base. A PERL cell efficiency of 24.7% was reported almost ten years ago, and the record of 25.0% reported by researchers from the University of New South Wales (UNSW) in 2009 was obtained after re-measurement of the same cell using newer measurement techniques. The PERL cell has remained the most efficient type of monocrystalline-silicon PV cell for the past ten years[5], and has been the most popular laboratory structure of all the high-efficiency crystalline silicon PV cells. However, the full PERL design is not easy to apply to low-cost industrial production because of the necessity for multiple photolithography steps, similar to semiconductor devices with complex structures. Expensive silicon PV cells for space applications have a similar structure to the PERL cell[6]. The PLUTO cell developed for industrial use by SunTech Power has a simpler passivated emitter solar cell (PESC) design, which was also developed at the UNSW in 1985[7], and provides efficiency of up to 19.2% in a 4 cm-square cell[8]. The PESC features front passivation, a selective emitter, and a plated front contact with fine gridlines.

Figure 4





Schematics of various crystalline solar cell structures. (a) PERL. Adapted from Ref. 5 (© 1999 Wiley-VCH Verlag GmbH & Co. KGaA). (b) HIT. Adapted from Ref. 48 (© 2008 WIP Munich). (c) BC-BJ. Adapted from Ref. 49. (d) interdigitated back-contact (IBC) cell using surface mount technology. Adapted from Ref. 17 (© 1976 IEEE). (e) Buried-contact cell structure by BP Solar. Adapted from Ref. 40 (© 2008 IEEE). All figures reproduced with permission.

The best output parameters reported for the HIT cell, which was developed for industrial use, are 729 mV, 39.5 mA cm_{-2}, 0.800 and 23.0% (V_{oc}, J_{sc}, FF and η) for a large 100.4 cm^2 cell[9]. This cell has a unique heterojunction structure consisting of very thin, amorphous p- and n-doped layers and intrinsic amorphous layers on the front and rear surfaces of a CZ n-type monocrystalline-silicon substrate. This heterojunction structure improves V_{oc} considerably by the effects of the large energy bandgap of the front amorphous silicon layer and the excellent quality of the interface between the amorphous layer and the crystalline substrate. This cell has the additional advantage of a low temperature coefficient of about 0.30 % K^{-1} at P_{max} compare to about 0.45 % K^{-1} for standard industrial crystalline silicon PV cells. This cell has a transparent conductive oxide (TCO) ARC, which reduces the sheet resistivity of the front amorphous layers. The distinctly lower J_{sc} compared to other high-efficiency PV cells appears to be due to suppressed photocurrent collection by the front amorphous silicon layers and the bulk silicon by the effects of the lower transparency of the TCO layer compared to other ARCs and/or the lower internal quantum efficiency of the amorphous layers. The result is a weaker blue response and lower J_{sc}.

The BC-BJ cell has interdigitated n- and p-doped regions and n and p contacts on the back surface. The original BC-BJ cell, called

the front surface field (FSF) cell or interdigitated back contact (IBC) cell, was fabricated and studied for space applications in the late 1970s [10,11]. The BC-BJ-structured point contact (PC) cell developed by Stanford University in the 1980s gave efficiencies of more than 20% from the outset[12]. BC-BJ cells were first fabricated for unmanned aircraft and solar race cars by SunPower in the 1990s. The cells were then extended to large-scale production for PV generation systems in the 2000s. The best conversion efficiency reported so far for a large-area industrial BC-BJ cell is 23.4%[13]. The BC-BJ cell has front and rear surface passivation layers, a random-pyramid light-trapping surface, FSF, interdigitated n- and p-doped regions on the back surface, n and p contact gridlines on n- and p-doped regions, a single-layer ARC and CZ n-type single-crystalline silicon substrate with a minority carrier lifetime of longer than 1 ms. Of all the crystalline silicon PV cell modules on the market at this time, only those based on BC-BJ cells provide the possibility of module efficiencies exceeding 20%. Several laboratories and manufactures are studying methods for improving the design and processing of BC-BJ cells [14,15]. BC-BJ cells have several advantages compared to the conventional front-contact cell structure: no gridline (sub-electrode) or busbar (main electrode) shading, a front surface with good passivation properties due to the absence of front electrodes, freedom in the design of back contacts (electrodes), and improved appearance with no front electrodes. They also provide advantages in module assembly, allowing the simultaneous interconnection of all cells on a flexible printed circuit (see Figure 4(d)). The low series resistance of interconnection formed by this type of surface-mount technology results in a high FF of 0.800, compared with around 0.75 for standard silicon PV cell modules [16,17].

Industrial cells

Monocrystalline solar cells

p-Type monocrystalline substrates sliced from boron-doped CZ ingots have been used for standard industrial PV cells for many years. In the early era of terrestrial PV cell production, small 2–5-inch-diameter CZ ingots were used, the small size and high cost of which obstructed cost reduction for monocrystalline cells. Much research and development has been devoted to reducing the production costs for CZ ingots and wafer processing over the past 20 years. CZ wafers with side lengths of 125 and 156 mm, sliced from 6- and 8-inch-diameter ingots, respectively, are now widely used for monocrystalline silicon PV cell fabrication. The

fabrication of monocrystalline cells and modules using wafers of the same size as those used for polycrystalline cell production has improved the competitiveness of monocrystalline cells against their polycrystalline counterparts in terms of manufacturing cost per output watt. Monocrystalline cells represented 38% of all solar cells manufactured in 2008[1].

There are large differences between the efficiencies of the best research crystalline silicon PV cells and the corresponding industrial cells. The efficiencies of standard industrial monocrystalline PV cells remain in the range of 16–18%, considerably lower than the 25% efficiency levels of the best research cells. Industrial cells are restricted by economic factors to simple cells that are suitable for high-speed, automated production using low-cost materials. Simple design features, such as front surface texturing and BSF similar, to those developed for terrestrial crystalline-silicon PV cells in the early 1980s are still adopted in most current industrial crystalline cells. To improve cell efficiencies, many cell manufactures are systematically attempting to introduce high-efficiency features, such as finer gridlines, selective emitters or more shallowly doped n_+ regions, into existing manufacturing processes. The BC-BJ cells and HIT cells have exceptionally high efficiencies for industrial monocrystalline PV cells, but have complex cell structures that require a much longer production process and more specialized equipment compared with the other industrial cells. As a result, it is difficult for these advanced cell types and modules to compete commercially in terms of production cost per output watt. There remains a dilemma in the balance between efficiency improvement and cost reduction for solar cells and modules using existing manufacturing technologies. Innovative and simple manufacturing technologies and equipment for the fabrication of high-efficiency solar cells are therefore needed in order to realize significant cost reductions for the production of crystalline silicon PV modules.

Another drawback of the monocrystalline cell technologies is that monocrystalline cells based on p-type CZ silicon substrates are susceptible to light-induced degradation (LID) caused by the recombination of reactive boron–oxygen complexes (B *s*–O 2*i*). Many studies have been undertaken in attempts to eliminate LID effects in monocrystalline-silicon PV cells, and permanent deactivation of the complex at high temperature (> 170 °C) has been reported[18]. Boron-doped magnetic-field CZ wafers and gallium-doped CZ wafers also show promise for eliminating LID effects in monocrystalline solar cells, and CZ-silicon cells based on phosphorous-doped n-type CZ wafers are also free of LID effects. The high-efficiency PV cells of SunPower and Sanyo are made using n-type CZ-silicon wafers.

Polycrystalline solar cells

Polycrystalline silicon ingots and wafers were developed as a means of reducing the production costs for silicon ingots, and have been investigated since the mid-1970s [19,20]. Modern polycrystalline furnaces are designed for maximum productivity, casting ingots of around 450 kg. Polycrystalline cells are currently the most widely produced cells, making up about 48% of world solar cell production in 2008[1]. Standard polycrystalline industrial cells offer efficiencies of 15–17%, roughly 1% lower than for monocrystalline cells fabricated on the same production lines. The efficiencies of polycrystalline cell modules, however, are almost the same as those for monocrystalline cells (14%) due to the higher packing factor of the square polycrystalline cells; monocrystalline cells are fabricated from pseudo-square CZ wafers and have relatively poor packing factors.

The efficiencies of both monocrystalline and polycrystalline PV cells will be improved in the future through the introduction of high-efficiency structures. The difference in efficiency between monocrystalline and polycrystalline cells is expected to become larger with the introduction of such high-efficiency structures due to the difference in crystal quality (*i.e.* minority carrier lifetimes). The best of the current research polycrystalline silicon cells, a PERL cell developed by Fraunhofer ISE[21], provides an energy conversion efficiency of 20.3%. This PERL cell has a laser-fired contact back structure that gives a V_{oc} of as high as 664 mV. The efficiency of this polycrystalline cell, however, remains about 5% lower than that for the best of the research monocrystalline PERL cells, attributable mainly to the quality difference between mono- and polycrystalline substrates. Polycrystalline substrates are subject to higher rates of minority carrier recombination, both at active grain boundaries and within crystalline grains due to high dislocation and impurity densities in comparison with FZ or CZ monocrystalline substrates. A considerable amount of research and development has been conducted on improving the efficiencies of polycrystalline solar cells over many years, by both public and industrial laboratories, and recent high-efficiency polycrystalline silicon solar cells now have the features listed in Table 2. These features are generally the same as for recent monocrystalline solar cells.

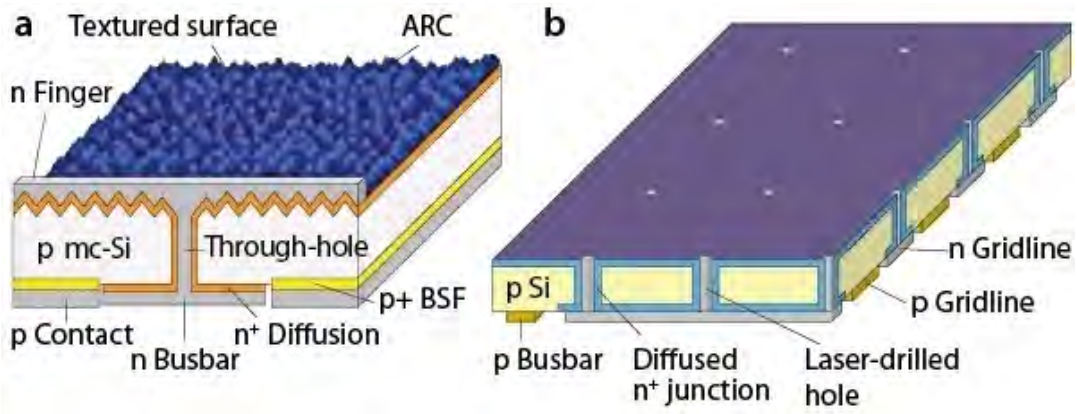
Table 2 Key technologies for high-efficiency polycrystalline silicon solar cells

The honeycomb-structured polycrystalline solar cells demonstrated recently by Mitsubishi Electric exhibit efficiencies of over 19.3% and come in large 15 cm × 15 cm cells[22]. These polycrystalline cells have a distinct front honeycomb-textured surface to reduce light reflection, and the introduction of this front textured surface has resulted in a high J_{sc} of 37.5 mA cm_{-2} for cells with screen-printed and fired silver-paste electrodes. This cell also has the PERL structures of front surface passivation, rear surface passivation with local BSF, and a selective emitter for improved cell efficiency.

Approaches to reduce cell costs also include using thinner silicon wafers. High-efficiency (18.1%) polycrystalline silicon cells fabricated using 100 µm-thick wafers were reported by Sharp in 2009[23]. The electrical performance of crystalline silicon PV cells with the standard back surface structure of an aluminum-alloyed BSF decreases as the substrate becomes thinner. High-efficiency polycrystalline cells with an SiN_x passivation layer and thin aluminum reflector on the back silicon surface display less of a performance degradation with decreasing substrate thickness for substrates of 100–180 µm in thickness. Cells with rear passivation and local BSF on 100 µm-thick substrates provide the additional advantage of less cell bowing compared with the standard aluminum alloyed BSF cells on substrates of the same thickness.

New types of back-contact polycrystalline cells, such as metal wrap through (MWT) cells and emitter wrap through (EWT) cells (Figure 5), have also been developed by institutes and companies such as ECN, Kyocera and Advent Solar [24–26]. BC-BJ cells without a front p–n junction require high-quality monocrystalline substrates with high minority carrier lifetimes. The WT back-contact cells, however, are suitable for use with polycrystalline substrate having relatively short minority carrier lifetimes (related to cell thickness). The front p–n junctions in these cells can collect most carriers generated in the region from the front n-doped layer to the back substrate surface. These back-contact cells have laser-drilled through-holes that can wrap through front n-electrodes and/or n-doped regions to the back surfaces. The MWT cells require only a relatively small number of through-holes to direct photogenerated electrons to the back surface through the metal electrodes and n-doped emitters, and produce higher collection photocurrents due to absence of a bus bar (main electrode) on the front surface as in conventional cells. A high J_{sc} of 37.3 mA cm_{-2} and an efficiency of 18.3% were reported for a recent MWT cell by Kyocera[26], and the module efficiency for MWT cell modules by ECN, 16.4%, is the highest reported to date[25].

Figure 5



Schematics of back-contact solar cell structures. (a) MWT. Adapted from Ref. 26 (© 2008 WIP Munich). (b) EWT. Adapted from Ref. 25 (© 2008 IEEE). All figures reproduced with permission.

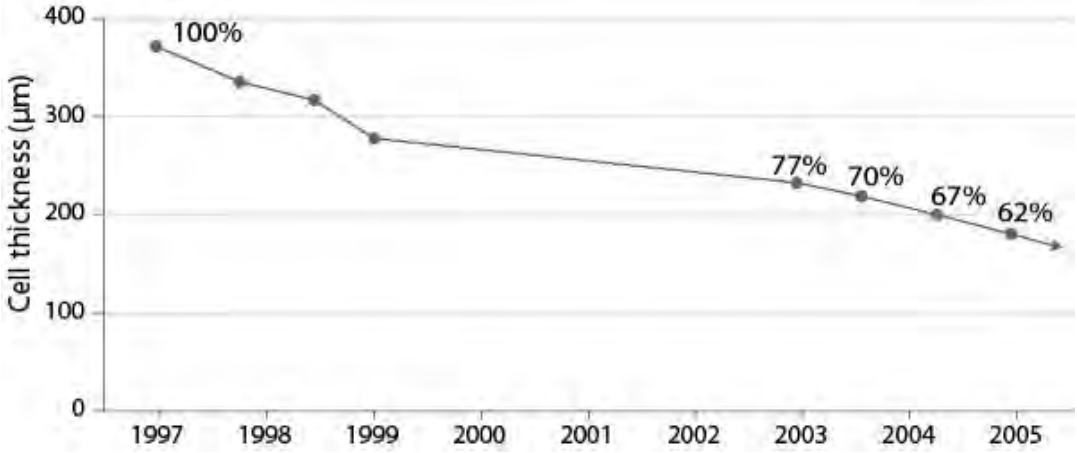
The EWT cells have a larger number of close-spaced through-holes, which direct photogenerated electrons to the back surface solely through n-doped emitters. The EWT cells produce even higher photocurrents by eliminating the both busbar (main electrode) and gridline (sub-electrode) shading on the front surface. A high J_{sc} of 37.5 mA cm_{-2} and efficiency of 17.1% were reported recently for EWT cells by Q-Cells. The target for industrial polycrystalline PV cells is to realize average cell efficiencies of 17% in large-scale production[24].

Many methods have been investigated to improve the quality of polycrystalline substrates to match that of the more expensive CZ monocrystalline wafers. The dendritic casting method is one such approach that allows the grain orientation and size to be controlled, resulting in high-quality dendritic crystals with parallel twinning. Solar cells based on dendritic polycrystalline wafers show efficiencies of as high as 17%, comparable to the efficiencies provided by CZ monocrystalline cells using the same cell fabrication process[27].

Materials and processing

The raw, high-purity polysilicon material used for the fabrication of crystalline silicon solar cells is generally made by the Siemens method. The market price for raw silicon is affected by the demand–supply balance for solar cell and semiconductor fabrication, and can fluctuate markedly. In 2006–2008, for example, the cost of raw silicon as a proportion of total solar cell module cost jumped from 20–30% to more than 50% due to a market shortage of silicon. Reducing the cost of silicon in a cell module by reducing the substrate thickness is therefore an important aspect of achieving overall cost reductions for solar cell modules. Wire-saw wafer slicing is one of the key production technologies for industrial crystalline silicon PV cells, and improvements in wafer slicing technology have resulted in a reduction in raw wafer thickness from 370 µm to 180 µm since 1997 for Sharp industrial polycrystalline-silicon cells (Figure 6). To introduce wafers thinner than 150 µm, sophisticated manufacturing processes suitable for ultrathin wafers will be needed, and the processes will need to provide high processing speed and high manufacturing yield in each of the process steps of wafer slicing, cell fabrication and module assembly.

Figure 6



Reduction of silicon wafer thickness by Sharp (© 2010 Sharp)

Several alternative growth methods have been proposed over the past four decades for the production of polycrystalline substrates directly from molten silicon, including edge-defined film-fed growth (EFG), string ribbon growth (SRG), and ribbon growth on substrate (RGS) [28–30]. These methods potentially make it possible to reduce the amount of silicon used in PV cell fabrication. The EFG and SRG methods are used on industrial production scales by SCHOTT Solar and Evergreen Solar, respectively[31]. These two methods have the advantages of low silicon consumption per W_p and high cell efficiencies in comparison with the RGS method. These methods afford inexpensive but slightly wavey polycrystalline substrates in comparison with the standard polycrystalline substrates. Recently manufactured cells based on direct-grown substrates have almost the same efficiencies as those of standard cast-silicon polycrystalline cells. However, the smaller EFG- and SRG-based cells, which are roughly half the size of standard industrial cells, incur higher cell and module processing costs. A crystallization on dipped substrate method, which can be used to produce standard-sized wafers (156 mm × 156 mm) directly from molten silicon in a crucible, was recently proposed by Sharp[32].

The front emitter layer of crystalline silicon PV cells is formed by phosphorus diffusion techniques in a quartz tube or belt furnace. Solid P_2O_5 or liquid $POCl_3$ is used as the phosphorus diffusion source. Phosphorous diffusion techniques the exploit gettering effects to reduce impurity densities in a silicon wafer and thereby improve minority carrier lifetime have been demonstrated to be effective provided diffusion is conducted under phosphorus supersaturation conditions (doping level above the solid solubility in silicon) [33–35].

The BSF layers in industrial cells are formed by alloying of screen-printed aluminum paste in a belt furnace. This process provides high productivity and relatively low process cost for BSF formation. Aluminum-paste alloying has the additional advantage of inducing wafer gettering effects in both polycrystalline and monocrystalline silicon PV cells similar to the phosphorus diffusion technologies [36,37]. Metal impurities, such as iron or copper, can be eliminated from bulk silicon by aluminum gettering effects, which can improve the minority carrier diffusion length.

The screen printing and firing of silver paste to make contact with the bulk silicon surface by penetrating the ARC is a well-established, simple and fast process for forming front and rear electrodes. It is also the most widely used and lowest-cost

method for forming electrodes in industrial crystalline silicon PV cells. The front gridlines are designed so as to optimize the trade-off between shadow loss and series resistance. As an alternative to the screen-printed silver paste approach, plated electrodes of layered nickel, copper and silver have been developed by researchers at the UNSW for use in buried-contact (BC) cells [38,39]. The BC cell fabricated by BP Solar is shown in Figure 4(e)[40]. Crystalline silicon PV cells with plated electrodes have excellent electrical characteristics due to their low series resistance and fine gridlines, which result in a much smaller shadow area. However, plated electrodes, which are formed by a wet process, have not yet become as widely used as the screen-printed silver paste electrodes. The silver used as the electrode material in crystalline silicon cells will become a critical material resource when crystalline silicon solar cell production reaches the large volumes predicted in the future. Copper and aluminum have therefore been considered as substitutes for silver in silicon PV contacts.

Future views on crystalline silicon solar cells

Industrial solar cells module must reach a price level of $\$1/W_p$ with a total system price level of $\$2/W_p$ to reach grid parity, and to become competitive with coal or nuclear power generation will need to be mass produced at a total system cost of less than $\$1/W_p$. Achieving even a module price of $\$1/W_p$ will require modules to be produced at a cost of less than $0.7\$/W_p$. Although such low costs remain very challenging for modules based on crystalline silicon solar cells, cost reductions to such a level are considered to be possible based on the technologies presented in this review, and the cost reduction must be accomplished while public incentives for PV systems remain in effect. The annual production volume for all kinds of solar cells is expected to exceed 100 GW_p/year by around 2020. Crystalline silicon cell modules have a long history of proven field operation and offer high efficiencies while presenting fewer resource issues than many competing technologies. As such, crystalline silicon PV cells are expected to be strongly represented in the future solar cell market.

To reach these future price levels, new technologies as listed in Table 3 will be needed for crystalline silicon solar cells and modules. New technologies to break through the efficiency barrier of 25% for crystalline silicon PV cells are being studied by many researchers and institutes around the world, but there have yet to be any practical improvements in cell efficiency. The

peak theoretical efficiency in a crystalline silicon solar cell based on a single homojunction and a bulk silicon energy bandgap of 1.1 eV is 30% under 1 sun $AM_{1.5}$ illumination. To break through this ideal efficiency limit based on existing Schockley and Queisser solar cell theory, novel technologies based on quantum dot (QD) and quantum well structures have been proposed and studied by many researchers. Multi-junction designs have been attempted in many forms for improving solar cell efficiency beyond that of a single-junction cell. For example, a triple-junction solar cell with a silicon bottom cell is expected to give efficiencies of more than 40%. Researchers at the UNSW have also proposed a silicon-based tandem junction solar cell incorporating silicon QD technology[41]. An effective bandgap of up to 1.7 eV has been demonstrated for 2 nm-diameter silicon QDs embedded in SiO_2[42]. Photon management, such as up- and down-conversion and plasmonic effects, are other potential approaches that could add extra efficiency based on existing high-efficiency silicon cells [43–45]. These technologies aim at shifting the photon energy of sunlight to match the sensitivity of the solar cell by adding special optical features (*e.g.* a fluorescent coating layer including rare-earth elements for up-and down-conversion) to the front and/or rear surface of the cells without modifying the structure of the solar cell itself.

Table 3 New technologies for high-efficiency crystalline silicon solar cells and modules

These high-efficiency technologies, however, generally incur higher production costs compared to standard silicon cells. Cell and module manufacturing technologies that satisfy both high efficiency and low cost will be essential for industrial production in the near future. The impacts of novel technologies such as QDs and photon management will be interesting to watch as research and development on crystalline silicon solar cells continues.

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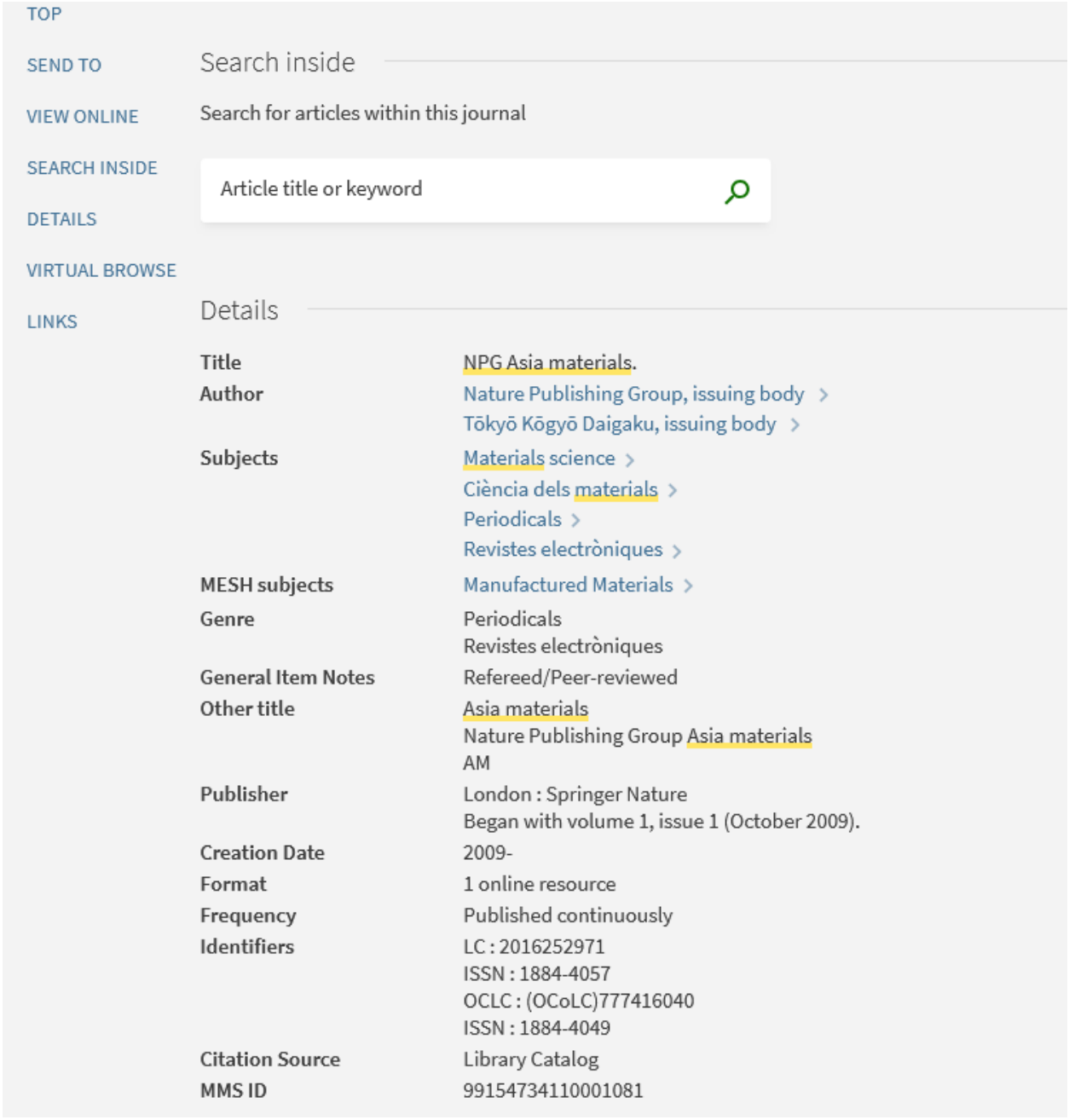
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Review paper: Toward highly efficient quantum-dot- and dye-sensitized solar cells

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ABSTRACT

Dye- and quantum-dot-sensitized solar cells have attracted tremendous attention as one of the potential low-cost alternatives for $p-n$ junction silicon solar cells. However, the conversion efficiencies of sensitized solar cells are still lower than those of silicon-based solar cells. Numerous research efforts have been made to enhance the sensitized solar cell efficiency over the past decades. Among the various attempts to improve the photovoltaic properties, the control of interface for reducing the charge recombination and the smart management of the light harvesting have proven to be most effective. Moreover, the $p-n$ junction structure can offer higher open-circuit voltage than the conventional n-type sensitized solar cell. In this review paper, recent developments in sensitized solar cells and the underlying mechanisms will be briefly introduced.

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1. Introduction

The vast uses of fossil fuels, causing environmental pollution and global warming, have led us to focus on the renewable energy sources for the future [1,2]. Among the renewable energy sources, solar cells have attracted a great interest as a solution to this situation [3–5]. To date, the silicon-based photovoltaic devices have power-conversion efficiencies over 20% [6]. However, the issues of high cost and environmentally-harmful waste in the processing technologies of silicon-based solar cells should be resolved [7].

Dye-sensitized solar cells (DSSCs) have been considered as one of the most promising photovoltaic technologies because they are generally made from inexpensive and nontoxic components, and can be designed in a diversity of colors and transparencies [8–11]. Since the pioneering work of Grätzel and O'Regan in 1991 [9], tremendous efforts have been made to improve the performance of DSSCs. However, the development of DSSCs has been sluggish over the last ten years, with the highest record of 12% ever reported [12]. To overcome the limited DSSCs efficiency, inorganic semiconductors have been considered as ideal next-generation sensitizers because of their bandgap tunability by controlling the quantum-dot size and high absorption coefficient (10^5–10^6/M cm) [13–16]. Moreover, quantum dots can generate more than two electrons from a single photon when they absorb light with higher energy than the bandgap of quantum dot (multiple-carrier generation) [17]. This may open up the possibility for exceeding the Schottky–Queisser limit. Nevertheless, the achieved conversion efficiencies of quantum-dot-sensitized solar cells (QDSCs) have been ~5% so far [18–21].

One of the main reasons for the efficiency deterioration in QDSC is the charge recombination, caused by porous nature of working electrode. In the conventional construction of sensitized solar cells, the charge recombination takes place dominantly at three possible interfaces: working electrode/electrolyte, quantum-dot-sensitizer/electrolyte, and transparent-conducting oxide (TCO)/electrolyte. Therefore, the control for these interfaces is the key issue for enhancing charge collection efficiencies. To reduce interfacial recombination, nanoscale coating with various materials on the surface of working electrode [22–33], quantum-dot semiconductor [34–38], and/or TCO [39–55] has been proven as an effective method. These nanoscale-passivation ideas have been effectively explored in the field of Li-ion batteries [56–84] and low-temperature fuel cells [85–98].

Another approach to improve efficiency of solar cell is light managements by utilizing light scatterers [99–105] and surface-plasmon resonances [106–111]. The scattering component modifies the photon paths, and extends the traveling distance of the incident light in the photoelectrodes, thereby enhancing the

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probability of photons being captured by the sensitizers. Metal nanoparticles can also contribute to the effective light absorption, both by field enhancement through the localized surface-plasmon resonance and by light scattering leading to prolonged optical-path lengths [112–115].

Meanwhile, *p*-type sensitized solar cell, which is the inverse mode of *n*-type counterpart, has attracted much attention as a component for the tandem DSSCs [116–120]. The combination of an *n*-type photoanode (TiO_2) with a *p*-type photocathode (NiO), in a tandem configuration can offer improved open-circuit voltage (V_{oc}). Generally, theoretical efficiency of tandem DSSCs is reported to be ~43%, well beyond that of single-junction DSSCs (~31%) [121–123].

This paper highlights recent progresses in sensitized solar cell in pursuit of the high conversion efficiency. Especially, this article focuses mainly on the nanoscale surface modification with various materials, light-harvesting management with scattering layer and surface-plasmon resonance, and tandem-sensitized solar cells.

2. Interface control for reducing charge recombination

2.1. Transparent-conducting-oxide/electrolyte interface

In DSSCs and QDSCs, the TiO_2 compact layer has been used to prevent the backward electron transfer from TCO to the electrolyte [41–47]. My group reported the correlations between photovoltaic properties and $TiCl_4$-treated compact-layer thickness in DSSCs system [41]. The physically-blocked FTO/electrolyte interface effectively prohibits injected electrons in FTO from recombining with the redox couple in electrolyte. As shown in Fig. 1, higher V_{oc} is obtained compared to the bare cell, and the short-circuit current (J_{sc}) is also increased. In particular, the 25 nm-deposited cell exhibits ~32% increase in power-conversion efficiency compared to the bare cell. In case of the thicker compact layer, however, the power-conversion efficiency is decreased. The trap states present in the thicker TiO_2 compact layer account for this phenomenon because these trap states tend to block the pathway of photoexcited electrons from the nanoporous TiO_2 layer to the FTO electrode [124,125].

The suppressed charge recombination at the FTO/electrolyte interface was analyzed by the open-circuit voltage decay, as shown in Fig. 2(a). The slow decay responses of the TiO_2 compact layer

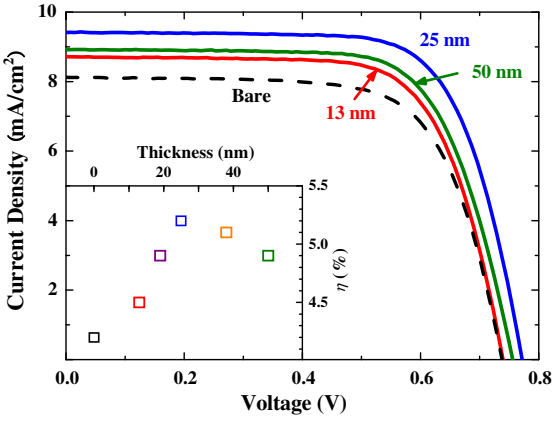


Fig. 1. Photocurrent–voltage curves of DSSCs with various TiO_2 compact-layer thicknesses. The inset shows power-conversion efficiency of DSSCs as a function of the compact-layer thickness. Reprinted with permission from B. Park et al. [41]. Copyright 2012, Elsevier.

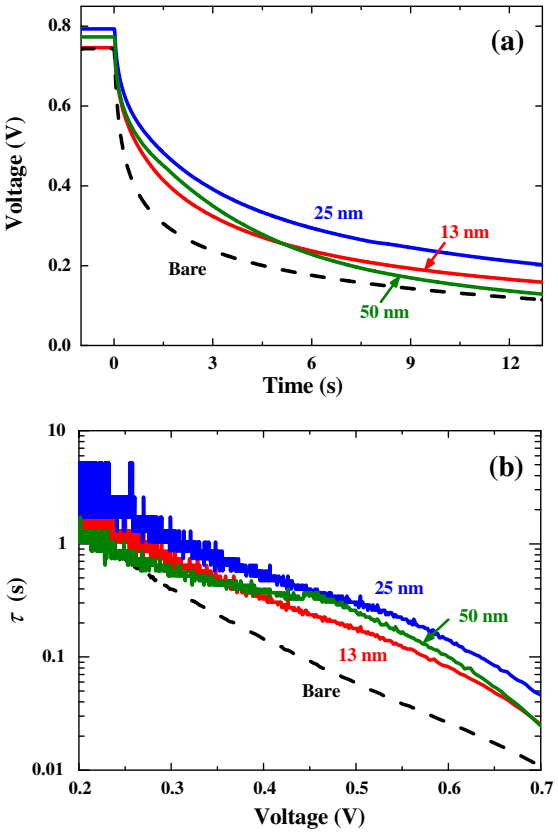


Fig. 2. (a) Experimental decay results of V_{oc} for the bare and compact-layer coated DSSCs. (b) Electron lifetimes as a function of voltage. Reprinted with permission from B. Park et al. [41]. Copyright 2012, Elsevier.

indicates that the recombination between electrons in the FTO and I_3^- in the electrolyte is drastically reduced by the TiO_2 compact layer. From the voltage decay curves, the electron-carrier lifetime (τ) can be calculated as a function of voltage [126,127], and the corresponding electron-carrier lifetime of DSSCs is shown in Fig. 2(b). At all voltages, electron-carrier lifetime of the 25 nm-deposited cell is approximately five times higher compared with the bare cell.

In the case of QDSCs system, the compact layer can also effectively reduce the backward reaction at the FTO/polysulfide-electrolyte interface. However, different from DSSCs system, asymmetric enhancement of incident photon-to-current conversion efficiency (IPCE) is observed for the thicker compact-layer cell (Fig. 3) [53]. In the case of DSSCs, an IPCE near the UV region is mainly affected by the absorption from TiO_2 electrode, because of higher molar absorption coefficient of TiO_2 than that of dye molecules (~10^4/M cm) [128]. In contrast, the CdS quantum dots have similar molar absorption coefficients (10^5–10^6/M cm), therefore, the values of the IPCE are represented by the sum of the CdS and TiO_2 responses in the UV region. As a result, the thicker compact-layer cell shows lower IPCE value below the ~390 nm region compared to the bare cell. Furthermore, the slopes of the IPCE spectra become steeper below the bandgap energy (middle region), since more trap states exist in the thicker compact layer meaning increased absorption near the conduction band. In the higher wavelength region, symmetric enhancement of the IPCE is observed because the absorption through the TiO_2 compact layer becomes negligible, and electron recombination at the FTO/

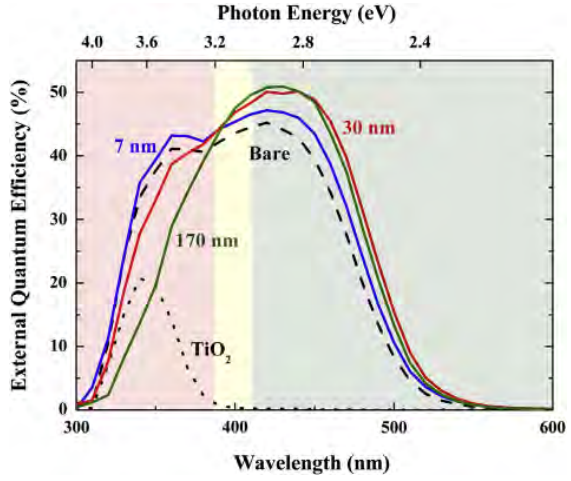


Fig. 3. Incident photon-to-current conversion efficiency (IPCE) spectra of QDSCs with various blocking-layer thicknesses. The IPCE of TiO_2 nanoparticles without CdS sensitizer is shown as a dotted line. Reprinted with permission from B. Park et al. [53]. Copyright 2011, Elsevier.

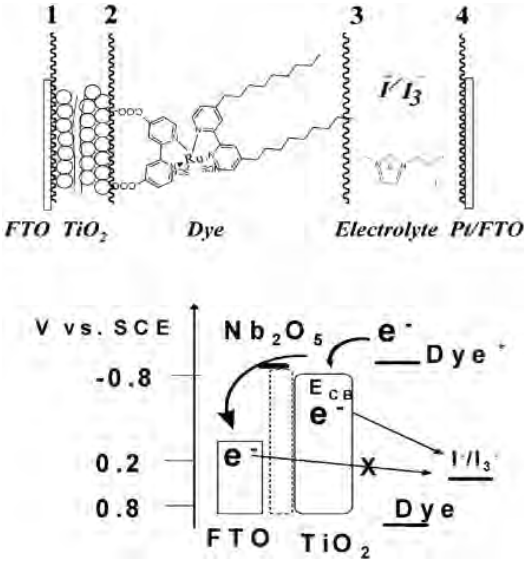


Fig. 5. Schematic views of interfaces in the DSSC device and the electron transfer of the FTO/Nb_2O_5/TiO_2 electrode. Reprinted with permission from S. Yanagida et al. [48]. Copyright 2007, Royal Society of Chemistry.

electrolyte interfaces is effectively suppressed. The thickness effects of TiO_2 compact layer in QDSCs are summarized in Fig. 4.

Another approach to minimize leakage electrons at TCO/electrolyte interface is to introduce potential-barrier layer such as Nb_2O_5, as shown in Fig. 5. Yanagida's group reported that nanoscale Nb_2O_5 layer worked as a remarkable blocking layer when deposited by rf magnetron sputtering [48]. Fig. 6 presents the *J–V* curve of the interface-optimized DSSCs by Nb_2O_5 blocking layer under AM 1.5 illumination. The metal oxide blocking layer can remarkably decrease the dark current (without illumination), resulting in higher V_{oc} and J_{sc} under AM 1.5 compared with the bare cell.

2.2. TiO_2-nanoparticle-electrode/electrolyte and quantum-dot-sensitizer/electrolyte interfaces

For the efficient operation of DSSCs and QDSCs, recombination pathways occurring at the TiO_2/sensitizer/electrolyte interface should also be minimized. The energy band structure at the TiO_2/dye-sensitizer interface is illustrated in Fig. 7 where charge separation processes take place in DSSCs. The generated electrons are able to recombine either with oxidized dye (path (3)) or redox couple (path (5)). In order to reduce these backward reactions, the passivation layer should have wide bandgap and conduction bandedge above that of TiO_2. At the same time, the surface charge of passivation layer is also important for the attachment of dye. Considering electrostatic interactions between dye and the passivation layer makes several metal oxides (e.g., ZnO, $CaCO_3$, MgO, and Al_2O_3) more charming, because they bear more positive surface charges than TiO_2, as shown in Fig. 8(a) [22–28].

The effect of Al_2O_3 coating layer thickness on the device performance was examined by varying the number of ALD cycles [27]. The high-resolution transmission electron microscope (HR-TEM) images of ALD samples after 20 and 40 cycles are shown in Fig. 9, respectively. These reveal the uniform shell formation around TiO_2 nanoparticles with a relatively-uniform alumina layer. With increasing number of Al_2O_3 coating cycles, a large increase in J_{sc}, V_{oc}, and the fill factor, thus enhancement in efficiency is observed up to 20 cycles (Fig. 10(a)). The increase in efficiency is likely to arise from an abundant adsorption of dye (Fig. 8(b)), and reduced carrier recombination at the TiO_2/dye/electrolyte interface.

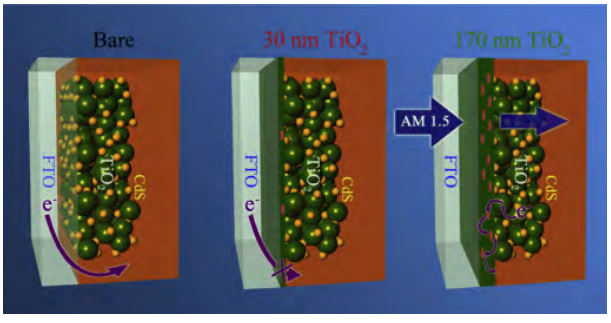


Fig. 4. Schematic figures of the TiO_2 blocking-layer effects on the performance of CdS-sensitized solar cells. Reprinted with permission from B. Park et al. [53]. Copyright 2011, Elsevier.

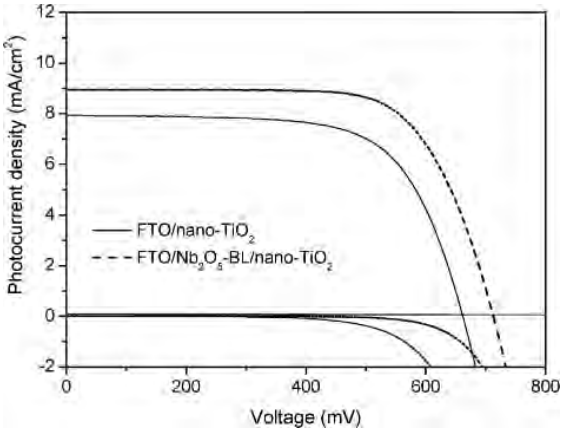


Fig. 6. *J–V* curves of cells employing Z-907 sensitized FTO/TiO_2 (solid line) and FTO/Nb_2O_5/TiO_2 electrodes (dashed line) under AM 1.5 illumination. Reprinted with permission from S. Yanagida et al. [48]. Copyright 2007, Royal Society of Chemistry.

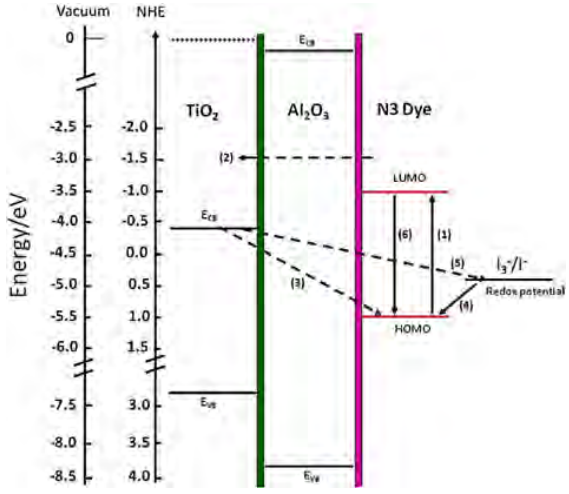


Fig. 7. Schematic diagram of band structure including interfacial charge-transfer processes occurring at TiO_2/dye/electrolyte interface in DSSCs. Reprinted with permission from S.-W. Rhee et al. [27]. Copyright 2010, Elsevier.

The improvement in photo-voltage is attributed to a reduction in dark current of the cells with Al_2O_3 layers, as shown in Fig. 10(b). The J_{sc} and V_{oc}, however, drop sharply as the coating thickness increases. This clearly indicates that the thickness of Al_2O_3 has

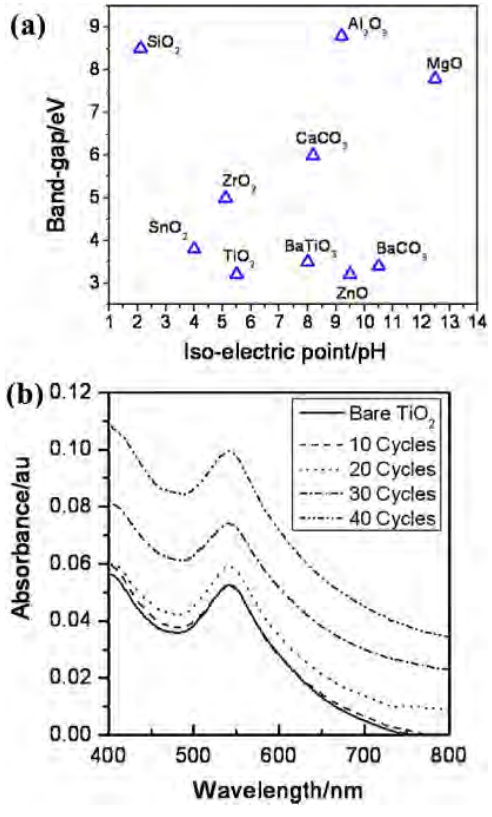


Fig. 8. (a) Graphical representation of isoelectric point and bandgap of various oxide materials. (b) Absorbance spectra of dye desorbed from bare and alumina-coated TiO_2 samples using 0.1 M NaOH. Alumina was deposited by ALD process with deposition cycles between 10 and 40. Reprinted with permission from S.-W. Rhee et al. [27]. Copyright 2010, Elsevier.

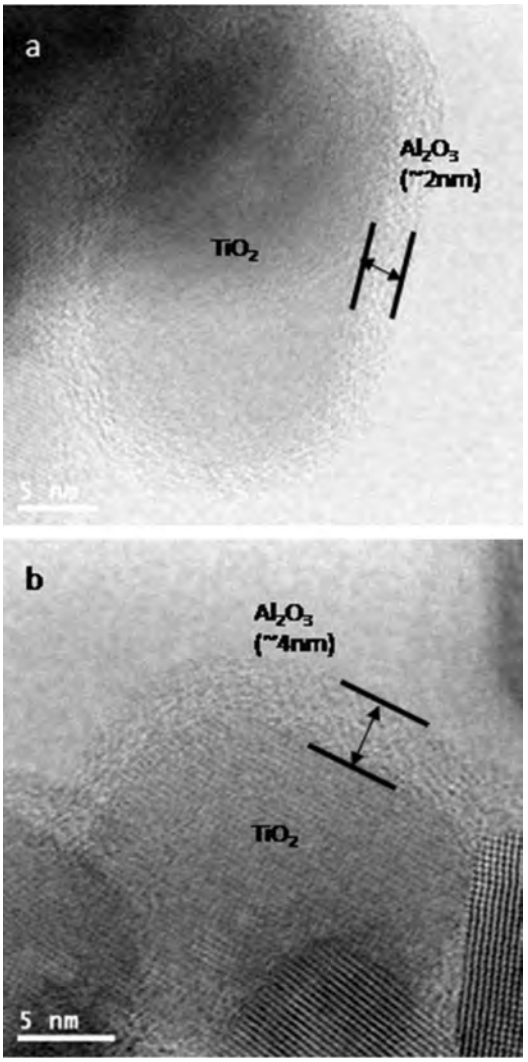


Fig. 9. High-resolution TEM images of TiO_2 porous layer covered with ALD alumina deposited with (a) 20 cycles and (b) 40 cycles. Reprinted with permission from S.-W. Rhee et al. [27]. Copyright 2010, Elsevier.

exceeded the tunneling thickness (~2 nm), and thereby leads to a decrease in device performance. Although the amount of dye adsorption is higher in the thicker Al_2O_3 layer (~4 nm), it results in the poor cell performance because the thick Al_2O_3-barrier blocks electron transport into TiO_2.

In case of the QDSCs system, surface modification of the TiO_2/electrolyte and quantum-dot/electrolyte interfaces is also crucial for high efficiency. My group reported the role of nanoscale TiO_2 passivation on the TiO_2-nanoparticle electrode for the performance of CdS–QDSCs [32]. As shown in Fig. 11, the optimized coating layer enhances the power-conversion efficiency by ~40% compared with the bare CdS-sensitized solar cell. The enhanced efficiency by TiO_2 passivation on the TiO_2 electrode is attributed to the reduction of charge recombination at the TiO_2/CdS/polysulfide-electrolyte interfaces by passivating the surface defects on the TiO_2-nanoparticle layer, as shown in Fig. 12. The effective suppression of recombination was confirmed by impedance analysis at the open-circuit voltage under AM 1.5 illumination (Fig. 13(a)). The charge-transfer resistance shows higher values with $TiCl_4$ treatment,

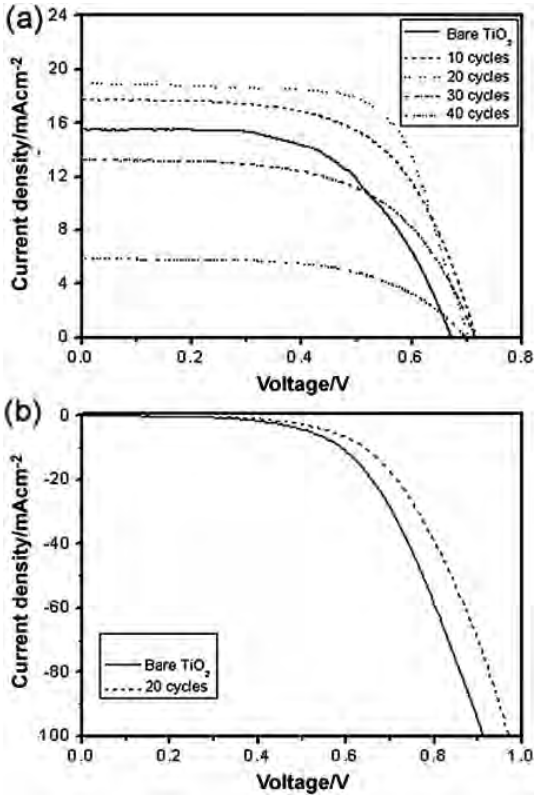


Fig. 10. (a) *J–V* characteristics of solar cell with bare and alumina-coated TiO_2 samples measured under one sun illumination. (b) *J–V* curves of bare TiO_2 and 20 cycles alumina-coated sample measured in dark. Reprinted with permission from S.-W. Rhee et al. [27]. Copyright 2010, Elsevier.

which means that the TiO_2-coating layer effectively suppresses charge transfer at the TiO_2/electrolyte interface.

As distinct from DSSCs, electrolyte diffusion is one of the factors to consider for the performance of QDSCs. This is because the diffusivity of polysulfide electrolyte without TiO_2 nanoparticles ($\sim 10^{-6}$ cm^2/s) is approximately 2 orders of magnitude lower than that of the iodide electrolyte typically used in DSSCs ($\sim 10^{-4}$ cm^2/s)

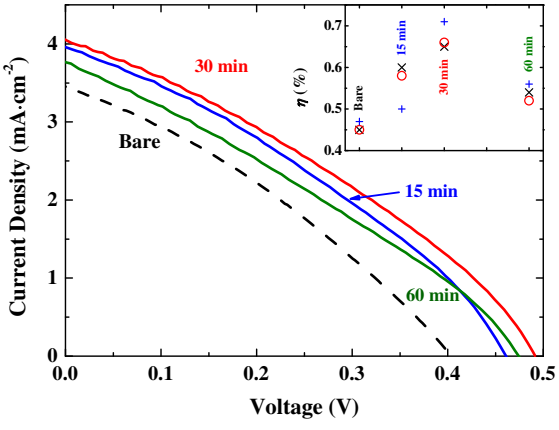


Fig. 11. Photocurrent–voltage curves of CdS quantum-dot-sensitized solar cells with various TiO_2-coating times. The inset shows power-conversion efficiency of QDSCs as a function of the coating time. Reprinted with permission from B. Park et al. [32]. Copyright 2012, Elsevier.

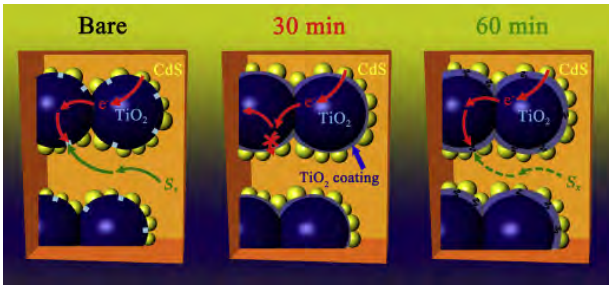


Fig. 12. Schematic figures of the $TiCl_4$-treatment effects on the performance of CdS-sensitized solar cells. Reprinted with permission from B. Park et al. [32]. Copyright 2012, Elsevier.

[129], and the size of quantum-dot sensitizer (2–6 nm) is larger than that of a dye molecule ($\sim$1 nm) [128]. From the impedance measured under dark condition [130,131], the diffusivity of electrolyte through the nanoporous TiO_2 electrode was obtained (Fig. 13(b)). The decrease in the diffusivity is associated with the increasing amount of TiO_2 on the nanoparticle electrode because the amount of layer scales with the TiO_2-passivation time. As a result, the pore size within TiO_2-nanoparticle film decreases and, therefore, the electrolyte diffusion through nanopores becomes inevitably difficult. This result is consistent with the increase of series resistance at V_{oc} for thicker TiO_2-coated cell (Fig. 11).

A great improvement in photocurrent and conversion efficiency was also reported for QDSCs when the CdS/CdSe-sensitized mesoporous TiO_2 electrode was passivated by ZnS. Lee et al. reported that ZnS layer coated on the TiO_2/CdS/CdSe photoelectrode showed enhanced photovoltaic performance (Fig. 14), due to the passivation of CdSe surface states from the photocorrosion [20]. It was furthermore argued that ZnS layer was able to inhibit the recombination of excited electron at the quantum-dot/electrolyte interface. It should be noted that in order to enhance chemical stability and photovoltaic in QDSCs, the use of nanoscale coatings on the quantum-dot sensitizer is also essential, and further research is necessary for better understanding of the interfacial charge-transport mechanisms.

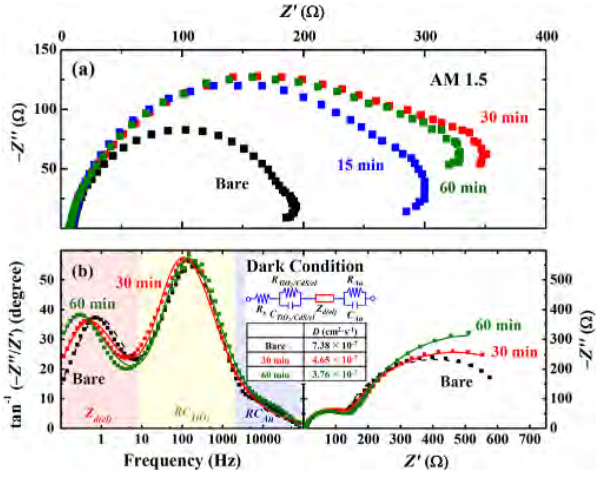


Fig. 13. (a) Electrochemical impedance spectra measured under AM 1.5 illumination, and (b) Bode and Nyquist plots measured under dark conditions with various TiO_2-passivation conditions at V_{oc}. Reprinted with permission from B. Park et al. [32]. Copyright 2012, Elsevier.

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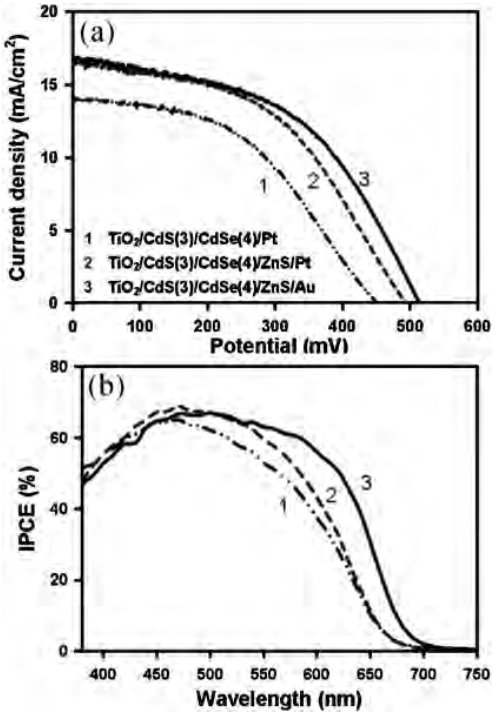


Fig. 14. (a) Effects of ZnS passivation layer and counter electrode on the *J*–*V* characteristics of the TiO_2/CdS/CdSe electrode. (b) Incident photon-to-current conversion efficiency spectra measured as a function of wavelength. Reproduced with permission from Y.-L. Lee and Y.-S. Lo [20]. Copyright 2009, Wiley-VCH.

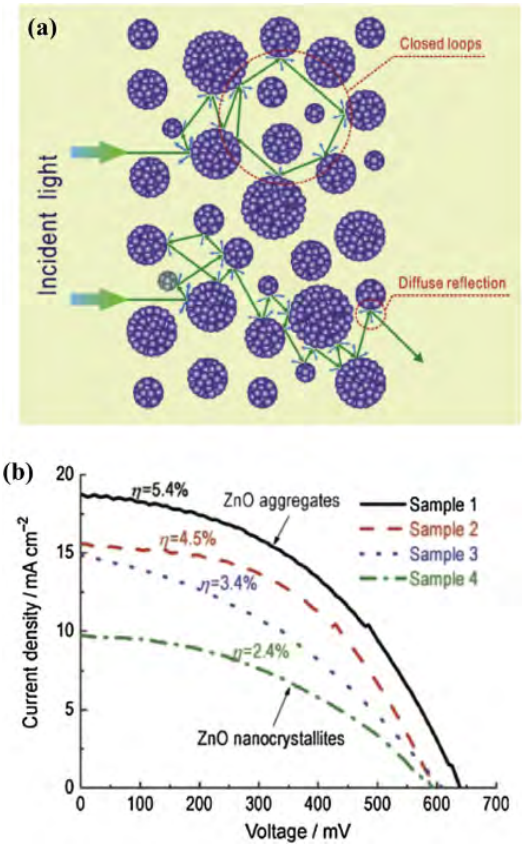


Fig. 15. (a) Schematic of light scattering and photon localization within a film consisting of submicrometer-sized aggregates. (b) Photovoltaic behavior of N_3-dye-adsorbed ZnO-film samples with differences in the degree of nanocrystallite aggregates. Reproduced with permission from G. Cao et al. [103]. Copyright 2009, Wiley-VCH.

3. Improving light-harvesting efficiency

3.1. Light-scattering effect

Optical effects generated by nanostructures provide opportunities for increasing the performance of sensitized solar cell. The light scattering is considered as another approach that can make an impact on the light-harvesting capability of the photoelectrode by utilizing optical enhancement effects. There have been many studies on enhancing the light-harvesting efficiency of photoelectrodes by adding submicrometer-scale particles as light scatterers, resulting in a significant advance in DSSCs. However, the introduction of large-sized particles into nanocrystalline films has unavoidable effect of lowering the internal surface area of the photoelectrode film [101].

Recently, submicrometer-sized polydisperse aggregates consisting of nanosized crystallites have been utilized for efficient scatterers [100–103], while the nanocrystallites provide the films with the necessary nanoporous structure and large surface area, as shown in Fig. 15(a). From the *J*–*V* curves in Fig. 15(b), the conversion efficiency of 5.4% is observed for submicrometer-sized polydisperse aggregates, whereas that of 2.4% is observed for ZnO nanoparticles without submicrometer-sized scatterers. This improved performance of DSSCs can be explained with the significantly extended traveling distance of light within the photoelectrode film.

However, the size of aggregates creates large voids between aggregates in photoelectrode (Fig. 16(a)), and these large voids may result in low connectivity for charge transfer and a decreased electron-diffusion length [132]. Thus, more charge recombination can occur, leading to reduced conversion efficiency. In this respect, Cao's group suggested the use of aggregate/nanoparticle mixtures, as shown in Fig. 16(b) [105]. They have systemically investigated the influences of the aggregate/nanoparticle ratio on the performance of DSSCs. The admixing of TiO_2 aggregates with nanoparticles exhibits an obvious improvement on the performance of DSSCs compared to both pure TiO_2 aggregates (5.35%) and pure TiO_2 nanoparticles (5.80%), as shown in Fig. 17. The TiO_2

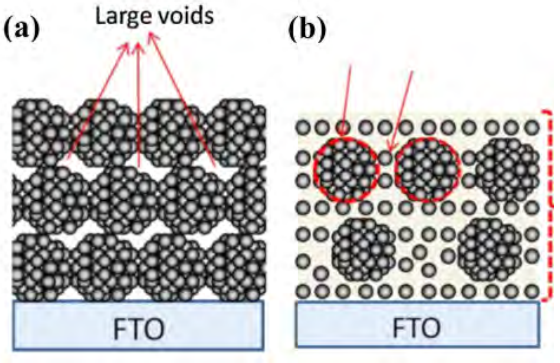


Fig. 16. (a) Films made of nanocrystallite aggregates for both high surface area and light scattering, and (b) with mixed nanoparticles and nanocrystallite aggregates for increased surface area and light scattering. Reprinted with permission from G. Cao et al. [105]. Copyright 2011, Elsevier.

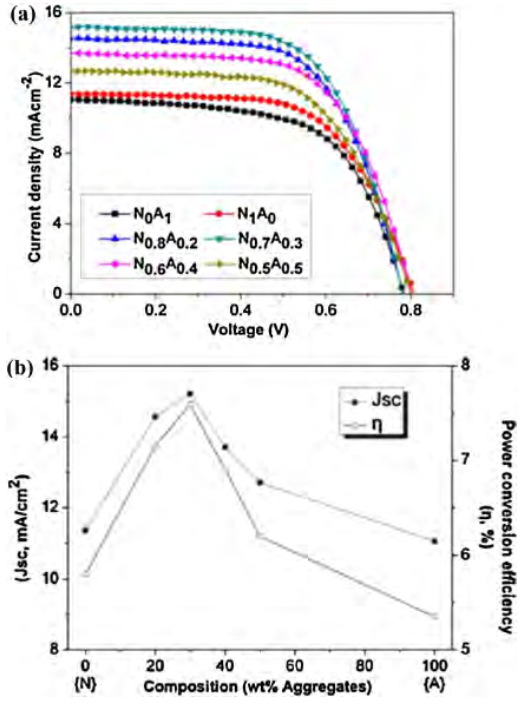


Fig. 17. (a) *J–V* curves of DSSCs with mixed photoelectrodes. (b) Comparison of the short-circuit current density and power-conversion efficiency as a function of TiO_2 nanoparticle (*N*) and aggregate (*A*) fraction. Reprinted with permission from G. Cao et al. [105]. Copyright 2011, Elsevier.

nanoparticles filling large voids among the aggregates lead to the increased amount of dye loading as well as the better connectivity for carrier transport.

3.2. Surface-plasmon resonance

The light-harvesting properties can also be amplified by employing surface-plasmon resonance. Surface plasmons are created when incident light excites oscillations of free electrons in metal nanoparticles, such as gold, aluminum, and silver. Hupp's group investigated the plasmon-enhanced absorption of the dyes by introducing silver nanoparticles [107]. Because the silver nanoparticles are corrosive in iodide electrolyte, they are conformably coated with a protective layer of TiO_2 by ALD (Fig. 18). From the IPCE measurement shown in Fig. 18(a), the cell with both dye and silver

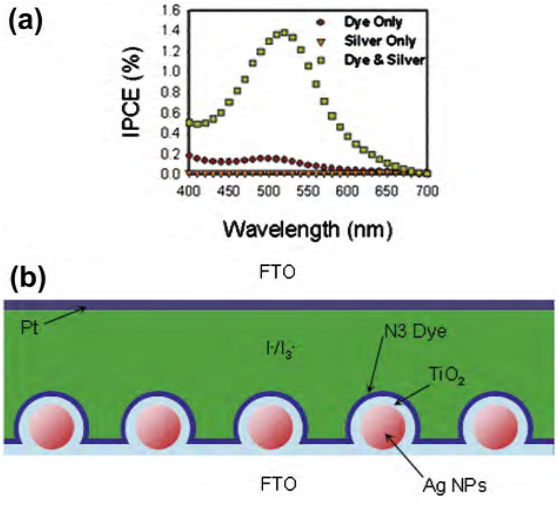


Fig. 18. (a) Incident photon-to-current conversion efficiency spectra of the DSSCs with silver nanoparticles and dye. (b) Configuration of solar cells containing silver nanoparticles and dye. From Ref. [107].

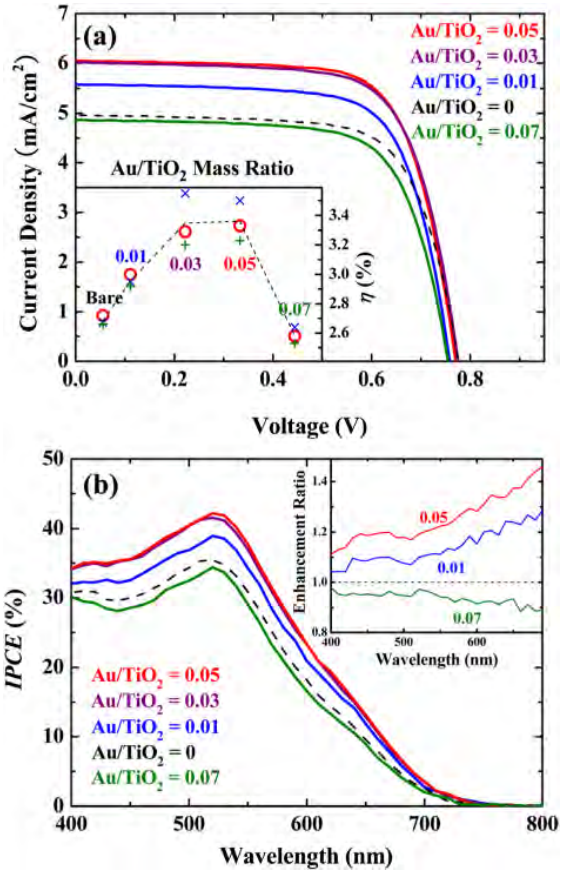


Fig. 19. (a) *J–V* characteristics of DSSCs at various Au/TiO_2 mass ratios. The inset shows the power-conversion efficiency of DSSCs with respect to the Au/TiO_2 mass ratio. (b) Incident photon-to-current conversion efficiency spectra of DSSCs at various Au/TiO_2 mass ratios. The IPCE enhancement ratios are also shown compared with the bare DSSC (Au/TiO_2 = 0) in the inset. Reprinted with permission from B. Park et al. [111]. Copyright 2011, American Institute of Physics.

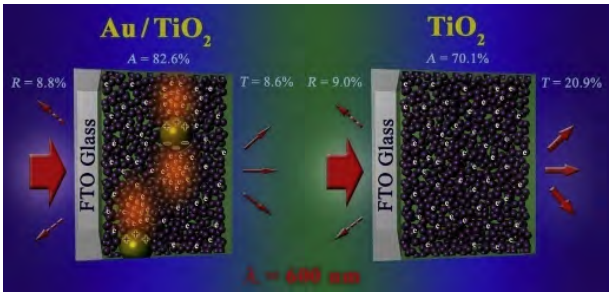


Fig. 20. Schematic figure representing the enhancement of Au/TiO_2-DSSC. Field enhancement near the Au nanoparticles is depicted as orange-color regions. Reprinted with permission from B. Park et al. [111]. Copyright 2011, American Institute of Physics.

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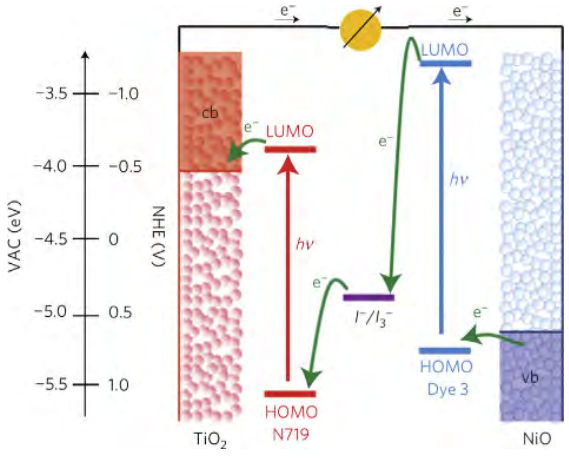


Fig. 21. Scheme for the electron-transfer processes occurring in the tandem-sensitized solar cell. Reprinted with permission from U. Bach et al. [116]. Copyright 2010, Nature Publishing Group.

nanoparticles exhibits higher IPCE peak value (~1.4%) compared to that made of the only dye (~0.2%) or only silver (~0%) samples. These results clearly confirm that spectra overlap between the dye and surface plasmon can give rise to an effective light absorption by the field-enhancement effect.

Recently, less-corrosive gold nanoparticles, as light-harvesting component, are incorporated to DSSCs system, and as a case study, the effects of 100-nm-diameter Au nanoparticles on the solar cell performance were investigated [111]. As shown in Fig. 19, the conversion efficiencies of Au/TiO_2 mixed cells are enhanced, which is mainly attributed to the increased current density. The IPCE enhancement ratio also reveals that the Au/TiO_2 mixed cell absorbs much more photons than the bare cell, particularly in the longer wavelength region (Fig. 19(b)). The electric field of incident light is strongly amplified by the oscillating surface charges in Au nanoparticles, yielding increased light absorption [133,134]. Therefore, more light can be absorbed by dye sensitizers, and more photocurrent can be generated in DSSCs, as shown in Fig. 20.

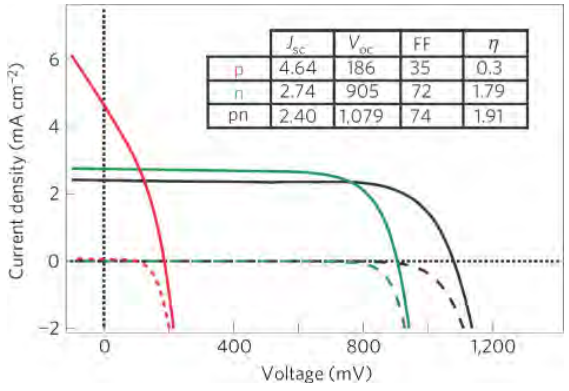


Fig. 22. *J–V* characteristics of a tandem solar cell (black) as well as *p*-type DSSCs (red) and *n*-type DSSCs (green) under illumination (solid lines) and in the dark (dashed lines). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.) Reprinted with permission from U. Bach et al. [116]. Copyright 2010, Nature Publishing Group.

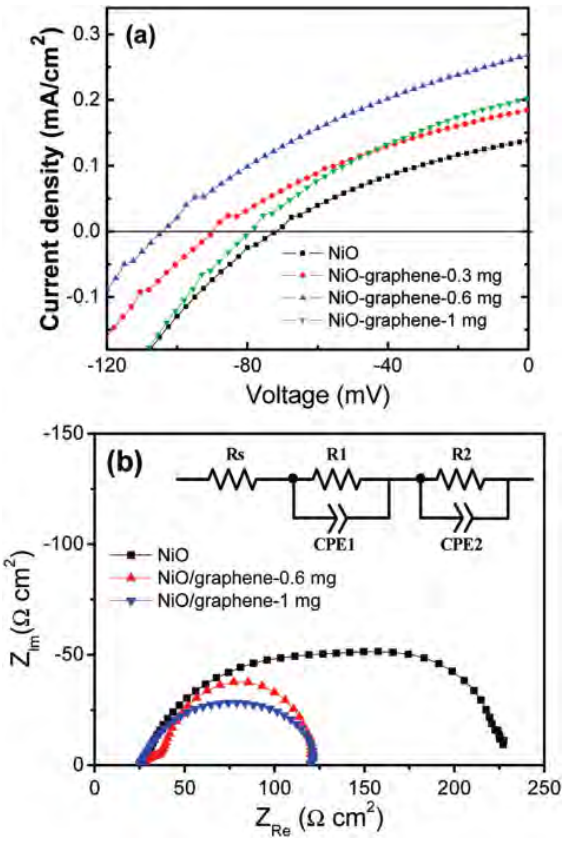


Fig. 23. (a) *J–V* characteristics of *p*-type DSSCs based on NiO and NiO/graphene composite films. (b) Nyquist plots of *p*-type DSSCs based on NiO and NiO/graphene composite electrodes. The inset displays the equivalent circuit of the devices. From Ref. [118].

4. *p*-type sensitized solar cell

4.1. *p–n* junction sensitized solar cell for high open-circuit voltage

Sensitized solar cell systems are generally composed of a nanoporous *n*-type semiconductors, such as TiO_2 and ZnO, coated with photosensitizers acting as an electron donor upon light excitation. In contrast, there is the limited number of studies on the sensitization of *p*-type semiconductors. The photoinjected hole transports into the valence band of the *p*-type semiconductor, of which the operating principle is just inverse scheme of the counterpart (*n*-type). The investigation of *p*-type sensitized solar cells is especially vital for the construction of tandem-sensitized solar cells (DSSCs and QDSCs). A scheme of tandem structure with the approximate energy levels is shown in Fig. 21. The tandem cell consists of a photoanode (*n*-type) and a photocathode (*p*-type) in a sandwich configuration with an intermediate electrolyte [116].

In tandem DSSCs, the maximum open-circuit voltage is determined by the difference between the conduction bandedge of the photoanode and the valence bandedge of the photocathode. The tandem (0.8 μm TiO_2 and 3.3 μm NiO) DSSC structure exhibits the V_{oc} of ~1.08 V, closely matching the sum of V_{oc} for *n*-type DSSC and *p*-type DSSC with similar short-circuit current to that of the *n*-type DSSC (Fig. 22). Therefore, the overall efficiency of tandem cell clearly exceeds that of the only *n*-type DSSC. However, the overall tandem efficiencies [116,121] are still considerably lower than those of conventional TiO_2-based DSSCs [9,10].

4.2. Modifications in p-type sensitized solar cell

The efficiencies of only *p*-type DSSCs are far below 0.5%, which limits the efficiency of tandem DSSCs drastically. Therefore, optimizing the power-conversion efficiency of *p*-type DSSCs is a key issue. As a photocathode, NiO has been widely adopted in that it is known as a large bandgap (3.5 eV) semiconductor with *p*-type nature as synthesized [135–137]. The main reason for the low efficiency in *p*-type DSSCs is that NiO has a low hole diffusivity ($\sim 10^{-8}$ cm^2/s), which may limit the diffusion length of the hole carriers resulting in the loss of photogenerated holes through recombination [138,139]. Several investigations to reduce fast charge recombination in NiO are currently underway as it is one of the major issues for increasing the performance of *p*-type DSSCs [118–120,123].

To improve the charge-transport properties, Yang et al. suggested the NiO/graphene nanocomposite film [118]. Then, the injected holes in the NiO photocathode can be transferred more rapidly through the graphene nanosheets. The enhanced hole transport by graphene gives rise to the improved J_{sc} and V_{oc}, as shown in Fig. 23(a). They analyzed the charge-transfer kinetics in the NiO/graphene nanocomposite films: the semicircle in the middle frequencies ($1–10^2$ Hz) of the Nyquist plot can be assigned to the hole-transport resistance in the nanoporous NiO electrode [140]. As shown in Fig. 23(b), the semicircles for the NiO/graphene electrodes are smaller than those of the bare NiO electrode, confirming that the carrier recombination of the composite-based *p*-type DSSCs is significantly suppressed due to the enhanced hole transport by the presence of conducting graphene.

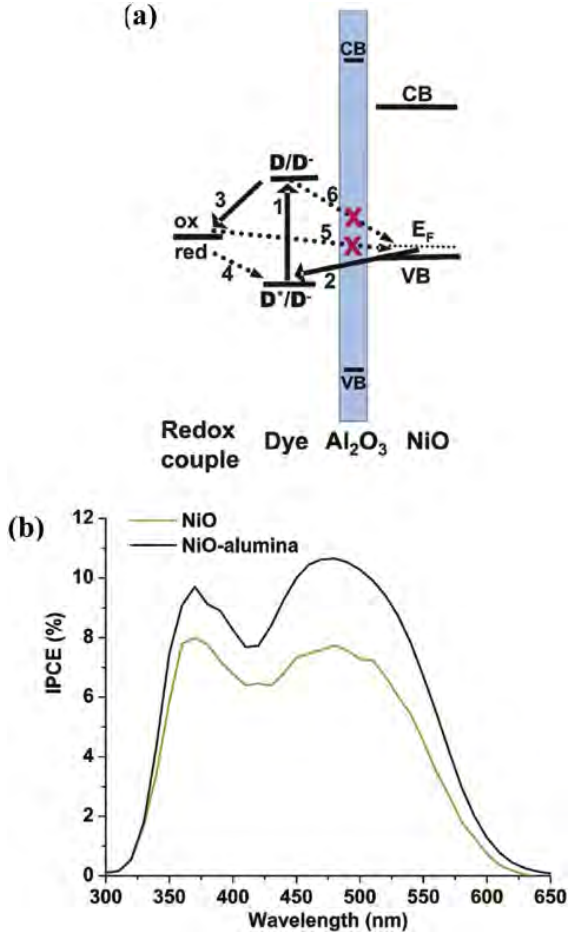


Fig. 24. (a) Schematic representation of the interfacial electron-transfer processes by the alumina-coating effect. (b) IPCE plots of *p*-type DSSCs fabricated from untreated NiO film and from a NiO film treated with 1 ALD cycle of alumina. From Ref. [120].

Another approach for reducing hole recombination is the surface modification of NiO electrode with a nanoscale blocking layer of a wide bandgap material (Fig. 24(a)). In this respect, Wu's group coated porous NiO electrodes with Al_2O_3 by ALD. Even though the amount of adsorbed dye on the NiO–Al_2O_3 film is slightly lower than that on the bare NiO film (different from the DSSCs system with Al_2O_3 coating), Al_2O_3-coated NiO cell exhibits higher collection efficiency of injected holes compared to the bare cell (Fig. 24(b)). This nanoscale Al_2O_3 layer has effectively reduced the hole recombination at the NiO/electrolyte interface.

5. Conclusions

This paper has mainly focused on the various approaches in pursuit of developing highly efficient sensitized solar cells, most of which are devoted to nanoscale surface passivation and tailoring desired nanostructures for light-harvesting efficiency. The basic tactics of enhanced photovoltaic properties rely on the reduced carrier recombination at the various interfaces, improved light absorption by photon management, and construction of tandem structures. It is obvious that exploiting intelligent nanoscience/nanotechnology to overcome these prohibitive issues will be the essential for the future work of quantum-dot- and dye-sensitized solar cells.

Acknowledgments

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Effect of air ambient on surface recombination and determination of diffusion length in silicon wafer using photocurrent generation method

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Abstract

An n^+–p–p^+ structure was formed by depositing a thin Al layer on one side and a semitransparent Pd layer on other side of a p–Si wafer, and the diffusion length L was determined from the slope of short circuit current density J_{sc} vs. illumination intensity P_{in} characteristics by illuminating the p^+ side with a laser light of wavelength $\lambda = 789$ nm, following the photocurrent generation method. The slope was found to decrease after the specimen was exposed to air for a few hours before the measurement. The present investigation revealed that the degradation of slope was owing to increase in surface recombination velocity S significantly, e.g. to 2800 cm/s for air exposure of 8 h, above its initial value 10 cm/s. This resulted from adsorption of moisture on Pd surface which decreases work function of Pd and lowers the accumulation potential barrier. The adsorbed water molecules could be removed from Pd surface by vacuum pumping and then S again became small and the slope regained its original value. The true value of L, smaller or larger than the wafer thickness, can be determined using single monochromatic illumination if S is known or has a negligibly small value, as in our case where the specimen was stored in vacuum. In our specimen we determined $L = 56$ μm when S was negligibly small. However, using the experimental slopes of J_{sc}–P_{in} curves at two monochromatic illuminations obtained by Sharma et al. we determined both S and L and found their values 1390 cm/s and 94 μm, respectively.
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Keywords: Thin Si wafer; Diffusion length; Surface recombination velocity; Induced n^+–p–p^+ structure

1. Introduction

The cost reduction has been and still remains the foremost necessity for terrestrial solar photovoltaics. This can be achieved either by an increase in solar cell efficiency or by a reduction in manufacturing cost of solar cells and PV modules. A highly effective approach for a cost reduction of c-Si solar cells is the better utilization of material by using thinner wafer, and therefore more wafers, per crystal length in manufacturing of solar modules. But, the performance of thin wafer based solar cells having p–n junction near the front surface and an ohmic contact at the back surface decreases with decreasing cell thickness. However, by creating a p–p^+ (or n–n^+) junction that gives a Back Surface Field (BSF) effect, a high and stable efficiency with decreasing cell thickness to a certain minimum is realizable (Münzer et al., 1999). In a Si solar cell the thickness d of its base region is primarily responsible for the absorption of useful solar radiations and the diffusion length L of photogenerated minority carriers in the base region is primarily responsible for generation of photocurrent. If d is large

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enough to absorb nearly all useful incident solar radiation on them and $d/L > 3$ then BSF is of no advantage to the cell.

As d/L decreases below 3 (either due to decrease in d or increase in L) the efficiency of BSF cells increases significantly, the improvements in the short circuit current density J_{sc} and the open circuit voltage V_{oc} are substantial if $d/L \ll 1$ (Singh and Jain, 1982). Therefore in order to benefit from BSF significantly a 300 μm thick cell will require Si wafer to have $L \gg 300$ μm. But the higher price of Si wafers capable of giving such large values of L in the cells make the solar photovoltaic production costly. Therefore, the practical way of reducing the d/L ratio is use thin Si wafers without decreasing J_{sc} generation capability of the cell. Fortunately despite the reduction in the wafer thickness from 300 μm to 100 μm or so nearly all the incident useful solar radiation can still be absorbed in Si by assorting to light trapping enhancement designs such as antireflection coating, front texture and back surface reflection, etc. (Singh et al., 1992). Then such a thin BSF cell, because of its improved collection efficiency with reduction in d/L, can give maximum possible J_{sc} value, enhanced V_{oc} and thereby a high efficiency (Singh and Jain, 1982; Singh et al., 1992). Polycrystalline Si solar cells of 18.1% efficiency have been fabricated using 100 μm thick wafers (Saga, 2010). The wafer thickness used in most crystalline Si solar cell in production is 160–240 μm (Saga, 2010). This shows that cells made using wafers of thickness as small as 160 μm have acceptably small breakage. SunPower Corporation manufactures high efficiency rear-contact solar cell with 21% efficiency on wafers of thickness <200 μm which have $d/L \ll 1$ (Mulliga et al., 2004). Hence, L measurement in the given Si wafers prior to fabrication of solar cells is very much necessary.

The existing methods, e.g. surface photovoltage method (Goodman, 1961; Moore, 1983; Schroder, 2001) and, spectral response methods (Stokes and Chu, 1977; Arora et al., 1980; Basu et al., 1994) require $d/L \approx 3$ for the measurement of L in the Si wafers, whereas generally $d/L < 2$ in Cz-Si or mc-Si wafers used in present manufacturing of commercial solar cells (Glunz, 2007; Cañizo et al., 2009). Therefore, surface photovoltage method and spectral response methods are not valid for the measurement of L in wafers used for present day Si solar cells. On the other hand, the back illumination photoresponse method (Jain et al., 1983; Sharma et al., 1986; Plá et al., 2000) can measure L in Si wafers easily with condition $d/L > 0.6$ and can be applied for measurement of L in the base region of bifacial Si solar cells or in virgin Si wafers using an n^+–p–p^+ (or p^+–n–n^+) induced junction structure. As shown by Sharma et al. (1986) in their photocurrent generation method (PCG), an induced n^+–p–p^+ structure can be formed on a p-Si wafer by depositing an Al layer on one side and a semitransparent Pd layer on the other side which form n^+ inversion and p^+ accumulation layers, respectively. On illumination with a monochromatic light from the p^+ back side, the photogenerated short circuit photo-current density J_{sc} of the n^+–p–p^+ structure increases linearly with the input intensity P_{in} of the incident light (Jain et al., 1983; Sharma et al., 1986). The slope of J_{sc}–P_{in} curve can be used to determine L. The higher the slope, the larger is the diffusion length. Sharma et al. (1986) had grown a thin SiO_x layer on the p-Si wafer by subjecting it to a heat treatment at 500 °C in dry oxygen before deposition of semitransparent Pd and Al layers on the wafer. Later Singh et al. (2005) applied this method to measure L in p-Si wafer without forming a SiO_x layer on the wafer surface prior to the deposition of Pd and Al layers. They found that the slope of J_{sc}–P_{in} curve decreased if the specimen was stored in air for a few hours. They determined substantially smaller values of L for prolonged storage of the specimen in air than in vacuum. As the diffusion length L is a bulk parameter of silicon, its decrease simply by exposing the n^+–p–p^+ structure to ambient air for a few hours at room temperature is unlikely.

In this paper we investigate the cause of the decrease in the slope of J_{sc}–P_{in} curve on exposure of the n^+–p–p^+ structure to air and present an analysis to determine the correct value of diffusion length L in the p-Si wafer and evaluate the surface recombination velocity S of minority carriers at the p–p^+ interface.

2. Theoretical details

Following Jain et al. (1983) and Sharma et al. (1986) we find that in an n^+–p–p^+ silicon solar cell structure, $d \gg d_p$ where d is the wafer thickness and d_p is the thickness of the p^+ (diffused emitter or the accumulation) layer. For such cases, the photo generated short circuit current density J_{sc} for illumination from the p^+ side is related with the intensity P_{in} of the incident light as (Jain et al., 1983).

$$J_{sc} = \frac{q\lambda(1-R_\lambda)LL_\lambda}{hc(L^2-L_\lambda^2)\cosh\left(\frac{d}{L}\right)}\left[e^{-\left(\frac{d_p}{L_\lambda}\right)}\left\{\frac{\beta+\frac{L}{L_\lambda}}{1+\beta\tanh\left(\frac{d}{L}\right)}\right\}\right]P_{in} \tag{1}$$

where $\beta = \frac{SL}{D_n}$, S is the recombination velocity of minority carriers (electrons) in the p base region at the p–p^+ interface, D_n is the diffusion coefficient of electrons, L is the diffusion length of electrons, L_λ is the absorption depth of the incident monochromatic light, R_λ is the reflectivity of the p^+ surface. Quantities q, h and c are the electronic charge, Planck's constant and velocity of light in free space respectively.

The $J_{sc}-P_{in}$ curve is a straight line and its slope $\xi = \frac{dJ_{sc}}{dP_{in}}$ can be expressed as

$$\xi = \xi_m f_s \operatorname{sech}\left(\frac{d}{L}\right) \tag{2}$$

$$\text{where } \xi_m = \frac{q\lambda(1-R_\lambda)}{hc} \tag{3}$$

and

$$f_s = \frac{LL_\lambda}{L^2 - L_\lambda^2}\left[e^{-\left(\frac{d_p}{L_\lambda}\right)}\left\{\frac{\beta + \frac{L}{L_\lambda}}{1 + \beta\tanh\left(\frac{d}{L}\right)}\right\}\right] \quad (4)$$

The value of ξ is obtained experimentally from the J_{sc}–P_{in} curve using monochromatic radiation of a given wavelength λ and ξ_m is determined from measurement of R_λ.

Eq. (2) has S and L as two unknown quantities. Hence S or L can be known from Eq. (2) with the knowledge of ξ, ξ_m, d, d_p, L_λ and D_n for the p^+–p–n^+ structure.

The conditions $L \gg L_\lambda$, $d_p \ll L_\lambda$ being valid, Eq. (4) becomes $f_s = \frac{1+\frac{SL_\lambda}{D_n}}{1+\frac{SL}{D_n}\tanh\left(\frac{d}{L}\right)}$ and then Eq. (2) is given as

$$\xi = \xi_m \frac{1 + \frac{SL_\lambda}{D_n}}{1 + \frac{SL}{D_n}\tanh\left(\frac{d}{L}\right)}\operatorname{sech}\left(\frac{d}{L}\right) \quad (5)$$

Also, then, S can be measured independently of L by carrying measurement of ξ and R_λ at two suitable monochromatic radiations of wavelengths λ_1 and λ_2 using the following relation.

$$S = \frac{D_n(L_{\lambda 2} - GL_{\lambda 1})}{L_{\lambda 1}L_{\lambda 2}(G-1)} \quad (6)$$

where $G = \frac{\xi_1}{\xi_2} \times \frac{\xi_{m2}}{\xi_{m1}} \times \frac{L_{\lambda 2}}{L_{\lambda 1}}$ and $L_{\lambda 2} > L_{\lambda 1}$.

Here ξ_1, $L_{\lambda 1}$ correspond to λ_1 and ξ_2, $L_{\lambda 2}$ correspond to λ_2.

Having obtained the value of S, we can compute L using Eq. (5). However, if S is so small that conditions $\beta \ll L/L_\lambda$, $\beta\tanh(d/L) \ll 1$ are also satisfied in addition to the condition $L \gg L_\lambda$, $d_p \ll L_\lambda$ then $f_s = 1$ and Eq. (6) gets simplified to as

$$L = \frac{d}{\cosh^{-1}\left(\frac{\xi_m}{\xi}\right)} \quad (7)$$

Eq. (7) is independent of S and has been applied earlier by Jain et al. (1983) and Sharma et al. (1986) to determine L in back illuminated solar cell and induced n^+–p–p^+ structures formed on p-Si wafers. In practice Eq. (7) is applicable so long as ξ is significantly smaller than ξ_m or in other words if $\cosh(d/L)$ is significantly greater than 1. As discussed by Jain et al. (1983) if $d/L = 0.6$ the $\cosh(d/L)$ is about 18.5% higher than 1 which will result in a measurably distinct value of ξ from ξ_m. Thus the method is easily applicable for $d/L \geqslant 0.6$.

In the following we shall show the application of Eqs. (2), (6), and (7) for determination of L. It may be pointed that the above analysis is valid even if only the space charge layer formed in the p-Si on the Al side consists of a p^- depletion layer instead of the n^+ layer. Henceforth, in this paper, we shall refer the space charge layer on the Al side as the n^+ inversion layer unless mentioned otherwise.

3. Experimental details

Four Cz-Si wafers, 50 mm diameter, ⟨1 0 0⟩ orientation, ~300 μm thickness, p type, B doped and of 1.0 Ω cm resistivity were chemically and mechanically polished. Thereafter an p^+ accumulation layer was created on one side of the wafer by depositing a semitransparent layer of Pd of thickness ~50 nm and an n^+ inversion layer on opposite side of the wafer by depositing an Al layer of thickness ~100 nm using thermal evaporation under vacuum. The wafer acquired a structure akin to p^+–p–n^+ and was capable of generating a photocurrent on illumination from the Pd side.

A circular area of 1.0 cm^2 on the Pd coated p^+ side of the structure was illuminated normally with a laser light of wavelength, 789 nm and the photo generated short circuit current density J_{sc} was measured for various intensities in 10–30 mW cm^{-2} range and was plotted against the input intensity P_{in} on a linear scale.

Each measurement of J_{sc}–P_{in} characteristics on the specimen was completed in <3 min at room temperature, 300 K, in air of 47% relative humidity after storing it for some hours under two different ambient conditions in the dark. First, the measurement was done immediately after the sample preparation and then repeated after 2 and 4 h of storage of the specimen in vacuum of the order 10^{-3} torr that was maintained using a rotary pump. Subsequently, the sample was stored in air for next 10 h. During this period, the measurement of J_{sc}–P_{in} characteristics was repeated after each 2 h of storage in air. After that the sample was stored again in vacuum for another 8 h and in this period J_{sc}–P_{in} measurements were repeated after each 2 h. The value of the reflectivity R_λ of the Pd coated surface was measured using a spectrophotometer SHIMADZU model UV 3101 PC after storing the specimens in vacuum for 1 h and in air for 10 h. The Fourier Transformed Infrared Spectroscopy (FTIR) measurements on the Pd coated side were done with FTIR spectrometer, Perkin Elmer Model BX, after storing the wafers in vacuum and in air for 10 h duration at room temperature to detect the presence of the adsorbed water.

4. Result and discussion

The experimental J_{sc} values obtained for a specimen S-1 after each measurement since the sample was first made (i.e. with the sample age 'y' in hours) are plotted against P_{in} of the incident laser light in Fig. 1.

Fig. 1a shows the experimental J_{sc}–P_{in} plots for aging of S-1 for $0 < y < 14$ h, during which it was stored first in vacuum for $0 < y < 4$ h and, then, in air for $4 < y < 14$ h, whereas, Fig. 1b shows the experimental J_{sc}–P_{in} plots for aging period $14 < y < 22$ h, during which it was stored in vacuum again after its storage in air since $y = 14$ h. The J_{sc}, P_{in} data of Fig. 1a and b were fitted into straight lines passing through the origin and their slopes were determined. These straight lines indicated that there was no significant deleterious effect of the series resistance of the structure if any on the measured J_{sc} value of the structure up to $P_{in} = 30$ mW/cm^2 used in this study.

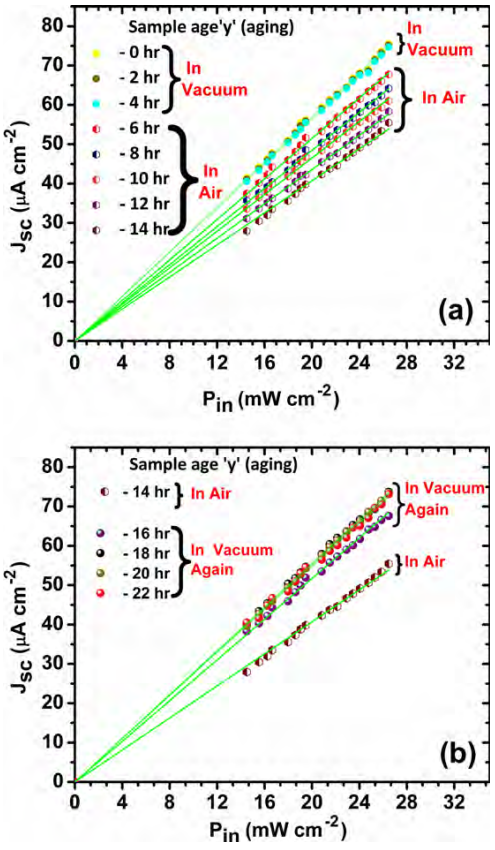


Fig. 1. $J_{sc}-P_{in}$ characteristics of S-1 at 300 K for illumination with laser radiation of 789 nm wavelength from p^+ side for (a) initial 4 h aging under vacuum and next 10 h aging under air ambient; (b) after 14 h aging under air ambient and for next 8 h aging under vacuum again.

It can be noted from Fig. 1a that the slope of the $J_{sc}-P_{in}$ curve of sample S-1 has not changed for storage in vacuum but has decreased significantly for storage in air. On the other hand, Fig. 1b shows that the slope of $J_{sc}-P_{in}$ curve of sample S-1 has improved with increase in duration of storage in vacuum from its value at $y = 14$ h for storage in air. Such an effect of storage in vacuum–air–vacuum was observed in all 4 wafers studied in this work. However, we shall present the details of our investigation for specimen S-1 only.

The values of the slopes ξ obtained from the $J_{sc}-P_{in}$ curves of Fig. 1a and b are listed in Table 1. The values of other parameters measured experimentally or taken from literature are $R_\lambda = 0.52$ and $L_\lambda = 10^{-3}$ cm corresponding to $\lambda = 789$ nm and $D_n = 25\ \mathrm{cm^2\ s^{-1}}$ corresponding to the resistivity $\rho = 1.0\ \Omega$ cm. Using the values of constants $q = 1.602 \times 10^{-19}$ C, $h = 6.626 \times 10^{-34}$ J s and $c = 3.0 \times 10^{10}$ cm/s and R_λ in Eq. (3) we obtained $\xi_m = 0.306$.

4.1. Application of Eq. (7)

The values of experimental slope ξ and the diffusion length L determined using Eq. (7) are plotted in Fig. 2 as a function of aging of S-1 in vacuum ($0 < y < 4$ h)–air ($4 < y < 14$ h)–vacuum ($14 < y < 22$ h). It is noted that ξ and L have the similar dependences on aging of S-1 in vacuum and air.

During initial aging for the period $0 < y < 4$ h in vacuum ξ is found to be constant but decreases with aging for the period $4 < y < 14$ h in air ambient and improved again for aging during $14 < y < 22$ h in vacuum to nearly regain its initial value. The value of L determined with corresponding ξ from the above values using Eq. (7) is found to be ~56 μm in the beginning and for subsequent aging in vacuum. It appears that the diffusion length L degraded to ~52.5 μm for aging of the sample for 10 h in air but improved to 55.5 μm again after storage in vacuum for 8 h.

Singh et al. (2005) had also found the decrease of the slope ξ of $J_{sc}-P_{in}$ curves of their induced n^+–p–p^+ structure specimen on storage in air ambient. They had determined L using the experimental values of ξ in Eq. (7) and found it decreasing with the aging of the sample in air. However, unlike the present case, they did not find any improvement in the slope on subsequent aging of their sample in a vacuum. Probably the quality of vacuum, not quantified in their case, may have been poorer than in the present study.

Since the diffusion length L of minority carriers in the p region of a silicon wafer is a bulk material property its reversible change by simply changing storage medium from vacuum to air and vice versa at room temperature under dark is quite unlikely. Therefore, we take the value of $L = 56$ μm determined for storage under vacuum as the true value of L for S-1. We shall also investigate the validity of Eq. (7), i.e. if S was indeed small enough to give $f_s = 1$ by estimating the values of S.

4.2. Estimation of S when L is known

If we take $L = 56$ μm as the true value of L then we can calculate the values of S and f_s from the measured value of ξ using combination of Eqs. (2) and (4). The values of S and f_s corresponding to the different values of ξ so determined using Eqs. (2) and (4) are listed in Table 1. It is noted that the value of S was small (~10 cm/s) for initial aging in vacuum but increased progressively with aging in air. S acquired a maximum value of 2800 cm/s for 10 h aging in air during the period $4 < y < 14$ h. Interestingly, S reduced again from 2800 cm/s to ~200 cm/s during $14 < y < 22$ h for second time aging in vacuum for 8 h. It may be mentioned that increase in S beyond 200 cm/s during aging in vacuum is attributed to exposure of S-1 to air for < 3 min during the $J_{sc}-P_{in}$ measurements. It may be pointed out that both $10 < S < 22$ cm/s achieved for initial aging in vacuum and $200 < S < 215$ cm/s after storing the specimen for last 6 h in vacuum the second time are low enough values of S to give f_s ~1 and thus permit application of Eq. (7) for determination of L correctly. However, the value of $S > 600$ cm/s attributed to the influence of aging in air during $6 < y < 16$ h is large and causes a decrease in f_s up to a

Table 1
Values of S and f_s for specimen S-1 determined using combination of Eqs. (2) and (4) when $L = 56$ μm and d = 300 μm, $D_n = 25\ cm^2s^{-1}$, $\lambda = 789$ nm, $R_\lambda = 0.52$, $L_\lambda = 10^{-3}$ cm.

Aging ambient	Specimen Age (h)	Slope ξ (mA/W)	S (cm/s)	$f_s < 1$	$1 - f_s$ (%)
Vacuum	0	2.880	10	0.9982248	0.2
	2	2.876	14	0.9968383	0.3
	4	2.868	22	0.9940655	0.6
Atmospheric Air	6	2.572	700	0.8914702	11.0
	8	2.423	1100	0.8398259	16.0
	10	2.320	1400	0.8041255	19.6
	12	2.182	2000	0.7562940	24.4
	14	2.034	2800	0.7049962	29.5
Vacuum	16	2.592	600	0.8984023	11.2
	18	2.784	200	0.9649506	3.5
	20	2.776	208	0.9621778	3.8
	22	2.768	215	0.9594049	4.0

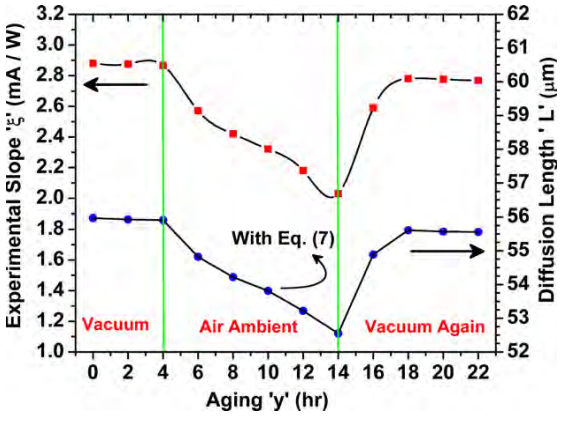


Fig. 2. Variations in the slope ξ of J_{sc}–P_{in} curve and in the diffusion length L as determined using Eq. (7) with the aging of specimen S-1 in vacuum–air–vacuum.

value substantially below 1 and thereby invalidates application of Eq. (7) for determination of L correctly.

4.3. Effect of air ambient on S

The ambient air contains nitrogen, oxygen, a significant amount of water vapor and some trace gases like CO_2. Some of these gases may be adsorbed at the Pd surface when the specimen is exposed to air. The adsorption may be expected to increase with prolong exposure of the specimen in air. Cao and Chen, 2007 have shown that the adsorption of N and O on Pd surfaces increases the work function of Pd but the adsorption of water has the opposite effect. They have shown that due the adsorption of water the work function of Pd decreases significantly even in the presence of N and O.

Fourier Transform Infra-Red Spectroscopy (FTIR) measurements were done on sample S-1 soon after taking

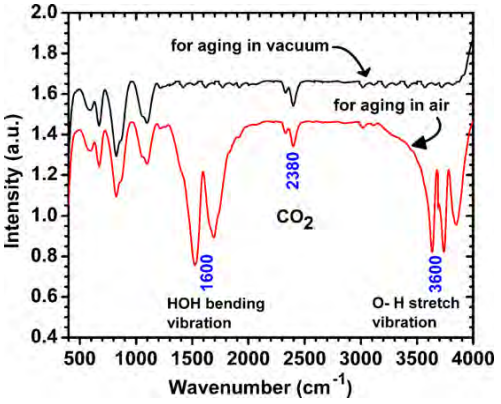


Fig. 3. FTIR spectra of Pd covered silicon wafer after taking it out from vacuum and after 10 h aging in air ambient.

it out of the vacuum chamber and, then, again after its aging in air for 10 h. The FTIR spectra shown in Fig. 3 presents a direct evidence for the presence of water vapor on the Pd coated surface of S-1 after aging in air ambient. The FTIR spectra shows water peaks (HOH bending vibration) at $\sim 1600\ cm^{-1}$ and (OH stretch vibration) at $\sim 3600\ cm^{-1}$ on Pd coated surface of S-1 for aging in air. No such peak was observed for aging under vacuum.

From Fig. 3, one may expect a decrease in the Pd work function Φ_{Pd} for aging of S-1 in air. Since the barrier height and the thickness of the p–p^+ accumulation layer depend on the difference in the work function Φ_{Pd} of Pd and the work function Φ_{Si} of p-Si, both the thickness and the barrier height of the accumulation layer will decrease with the decrease in the value of Φ_{Pd} as shown schematically in Fig. 4. For 1.0 Ω cm resistivity p-Si the value of $\Phi_{Si} = 5.0$ eV. Taking $\Phi_{Pd} = 5.25$ eV for Pd in vacuum the barrier height Ψ_{p-p+} of the p–p^+ interface potential barrier in vacuum can be expected to be ~0.25 V. The corresponding value of S can be computed using the Singh and Singh expression (Singh and Singh, 1990) as

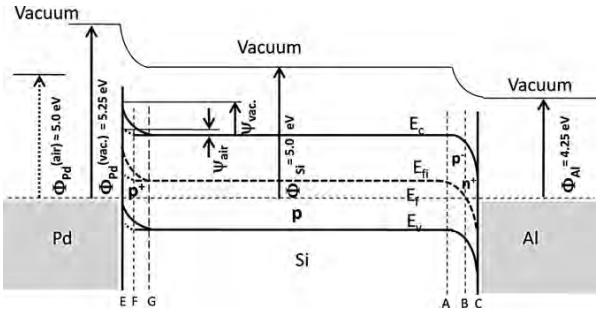


Fig. 4. A schematic energy band diagram for n^+–p–p^+ induced structure under thermal equilibrium for specimen S-1 stored in vacuum and the air ambient. EF and FG indicate the thickness of p^+ accumulation layer under air and vacuum respectively, AB is p^- depletion layer and BC is the n^+ inversion layer. $\Psi_{vac.}$ and Ψ_{air} stand for Ψ_{p-p+} for storage of S-1 in vacuum and air respectively.

Table 2
Measurement of S and L using data of Sharma et al. (1986). $L \gg L_\lambda$, $\exp(-d_p/L_\lambda) \approx 1$, and $D_n = 33.8\ \mathrm{cm^2 s^{-1}}$ for $\rho = 10\ \Omega\,\mathrm{cm}$ (Larin, 1968).

d (μm)	λ (nm)	R_λ (%)	L_λ (μm)	ξ (A/W)	ξ_m (A/W)	Sharma et al. ($f_s = 1$)	This work ($f_s = 0.8053$)	
						L (μm)	S (cm/s)	L (μm)
220	800	46	10	0.005	0.349	84	1390	94
	900	46	27	0.006	0.393	86		94

$$S = \frac{\pi}{4\tau_{n_E}}\sqrt{\frac{2kT \in \in_0}{q^2(N_a + n_E)}} \tag{8}$$

In above equation τ_{n_E} is the life time of minority carriers (electrons) at the surface of p-Si, ε is the dielectric constant of silicon and ε_0 is the permittivity of free space. $(N_a + n_E)$ stands for the majority carrier density $p_{\mathrm{Pd–Si}}$ in the accumulation layer at the Pd–Si interface, Hence,

$$p_{\mathrm{Pd\text{-}Si}} = N_a e^{\left(\frac{q\Psi_{\mathrm{p–p^+}}}{kT}\right)}$$

The value of $p_{\mathrm{Pd–Si}}$ will decrease with decrease in $\Psi_{\mathrm{p–p+}}$ owing to the decrease in Φ_{Pd} from its initial value. Assuming $\tau_{n_E} = 1 \times 10^{-9}$ s, S can be expected to increase from a value ~12 cm/s for $\Psi_{\mathrm{p–p^+}} = 0.25$ V for aging in vacuum to $S = 3780$ cm/s for $\Psi_{\mathrm{p–p^+}} \to 0$ V in air. This explains qualitatively the cause of increase in S for aging of S-1 in air as observed in the present study.

4.4. Measurement of both S and L

It has been discussed earlier that both S and L can be determined from the measurement of ξ at two wavelengths. To show this we use the published data of Sharma et al. (1986) for their measurement of ξ and other parameters for 800 nm and 900 nm wavelengths.

Table 2 gives a set of values of parameters such as R_λ, L_λ, ξ and ξ_m for two wavelengths 800 nm and 900 nm taken from Sharma et al. (1986). Eq. (6) was used for calculation of S with help of the above parameters in their induced n^+–p–p^+ structure formed on p-Si wafer. So, calculated value of S was used in Eq. (5) for determination of L. We have taken $D_n = 33.8\ \mathrm{cm^2\ s^{-1}}$ (Larin, 1968) for $\rho = 10\ \Omega\,\mathrm{cm}$ of p-Si wafer used in preparation of n^+–p–p^+ structure by Sharma et al. (1986). These values of S and L are also listed in Table 2.

Sharma et al. (1986) had applied Eq. (7) and had determined $L = 84$ μm and $L = 86$ μm corresponding to $\lambda_1 = 800$ nm and $\lambda_2 = 900$ nm, respectively. Table 2 shows that the value of S determined by us is 1390 cm/s and that of L is 94 μm. The difference between the values of L determined by Sharma et al. (1986) and in this work is due to the reason that Sharma et al. (1986) considered S negligible and hence $f_s \approx 1$. However, we found that S was 1390 cm/s which is a significant value leading to $f_s = 0.8053$. Therefore when only one monochromatic illumination is used the measurement of ξ should be done after storing the specimen under vacuum to ensure negligibly small value of S for determination of true value of L using Eq. (7). However, using two suitable monochromatic illuminations S can be evaluated by applying Eq. (6) and then L can be determined correctly using Eq. (5). Thus the use of two suitable monochromatic illuminations enables determination of true value of L with photocurrent generation method even for the storage of specimen in air or in general when S is not negligible.

5. Conclusion

A study has been done to see the effect of exposure of an induced n^+–p–p^+ structure to the atmospheric air for few hours on the slope of J_{sc}–P_{in} characteristics for illumination from the with p^+ side with a laser light of $\lambda = 789$ nm and to extract correct value of L from the slope. The slope of the J_{sc}–P_{in} curve is found to be nearly constant when measurements are done on the sample stored in vacuum and decreases when the sample is stored in atmospheric air for few hours. The slope improves to its nearly original value if the sample is stored again in vacuum for some hours. We have found that the decrease of the slope is owing to the increase in surface recombination velocity S at the p–p^+ surface which results from the adsorption of moisture on the Pd coated surface. The moisture decreases the work function of Pd. The moisture is removed when the vacuum is created and consequently S reduces again after storage in vacuum. S controls the value of f_s. For low values of S, $f_s \approx 1$ and, then, Eq. (7) is applicable for determining L from the slope obtained using single monochromatic illumination. Such small values of S to give $f_s \approx 1$ are ensured by storing the specimen in vacuum. In our specimen we determined $L = 56$ μm using Eq. (7) when S was negligibly small and hence $f_s \approx 1$. For larger values of S such that f_s is significantly smaller than 1, one can determine L using the Eqs. (2) and (5) if S is known. We have also shown that the both S and L can be determined with this method using Eq. (6) by measuring the slopes of J_{sc}–P_{in} curve for two suitable monochromatic radiations. Using the experimental slopes of J_{sc}–P_{in} curves at two monochromatic illuminations obtained by Sharma et al. we have been able to determine both S and L with values 1390 cm/s and 94 μm, respectively.

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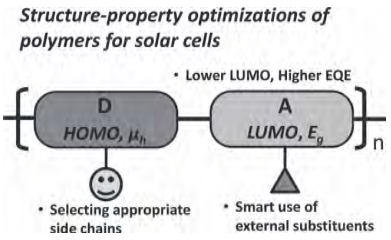
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Attachment G-6

Structure-Property Optimizations in Donor Polymers via Electronics, Substituents, and Side Chains Toward High Efficiency Solar Cells

Rycel L. Uy, Samuel C. Price, Wei You*

Many advances in organic photovoltaic efficiency are not yet fully understood and new insight into structure-property relationships is required to push this technology into broad commercial use. The aim of this article is not to comprehensively review recent work, but to provide commentary on recent successes and forecast where researchers should look to enhance the efficiency of photovoltaics. By lowering the LUMO level, utilizing electron-withdrawing substituents advantageously, and employing appropriate side chains on donor polymers, researchers can elucidate further aspects of polymer-PCBM interactions while ultimately developing materials that will push past 10% efficiency.



1. Introduction

Featuring significantly reduced cost on both materials and fabrication when compared with the market dominant crystalline Si solar cells, organic solar cells have been touted as a serious contender to lead the next generation of solar cells. Thus, the field of organic solar cells has attracted a tremendous amount of research activity. A simple search of the Web of Knowledge℠ using the key words "organic solar cells" returned over 8000 results! As shown in Figure 1a, the number of publications has been rapidly increasing in the past 10 years, in particular within the past 5 years (Figure 1b), which clearly indicates the rapid growth of this research field.

Among all "organic"-based solar cells, polymer solar cells, in particular polymer/fullerene-based bulk heterojunction (BHJ) solar cells,[1] are arguably one of the hottest research fields.[2,3] By blending the electron-donating semiconductor (DONOR, e.g., polymers) and an electron-accepting semiconductor (ACCEPTOR, e.g., fullerenes) in bulk, the BHJ offers some unique advantages and functions as follows (Figure 2). First, the light absorption by organic semiconductors only produces excitons (tightly bound electron-hole pairs), which need to travel to the DONOR–ACCEPTOR interface to separate into energy-carrying charges. However, these excitons usually have a very short lifespan and a similarly short diffusion distance (≈10 nm). Thus, the minimized travel distance to the DONOR–ACCEPTOR interface rendered by the BHJ configuration is beneficial for efficient exciton dissociation. Second, the BHJ maximizes the interfacial area between the DONOR and the ACCEPTOR, and allows one to employ films of thicknesses much larger (typically 100–200 nm) than the exciton diffusion length (≈10 nm). A thick film can absorb more photons, thus more excitons can split into usable charges. Finally, the interpenetrating network of the BHJ offers charge transport pathways to assist the charge collection at the electrodes.

Empowered by the synergistic efforts among chemists, physicists, and engineers, the power conversion efficiency of BHJ solar cells has been steadily increasing (Figure 3). From the materials' perspective, poly(phenylene vinylene)s (PPV) dominated the research field in the 1990s, such as poly[2-methoxy-5-(2′-ethylhexyloxy)-1,4-phenylenevinylene] (MEH–PPV) and (poly[2-methoxy-5-(3,7-dimethyloctyloxy)]-1,4-phenylenevinylene (MDMO–PPV). Through the application of chlorinated solvents to

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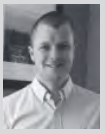
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tune the morphology of the active layer (i.e., the blend of polymer and fullerene derivatives), up to 3.3% power conversion efficiencies were achieved in PPV-based BHJ solar cells with $PC_{61}BM$ as the acceptor material ([6,6]-phenyl C_{61}-butyric acid methyl ester, a soluble version of the original C_{60}).[4,5] The next efficiency milestone was achieved by poly(3-hexylthiophene) (P3HT), which has been extensively studied since the early 2000s.[6–8] Again, the careful control of the morphology of the BHJ blend of P3HT:$PC_{61}BM$ ultimately resulted in ≈5% efficiency.[3,8–10] However, with relatively large band gaps, both PPVs and P3HT cannot absorb enough light, severely limiting further efficiency improvement. Therefore researchers have pursued novel polymers of lower band gaps, in order to harvest more light thereby potentially attaining higher efficiency. In the past few years, the field has witnessed the development of several new polymers, with a few achieving 7–8% efficiency in typical BHJ devices with fullerenes as the acceptor.[11–22] Very recently, a record high efficiency of over 10% was reportedly achieved by Mitsubishi.[23,24] All these accomplishments are a testament to the significant progress achieved by the organic photovoltaic (OPV) research community.

In response to the rapid growth of this exciting research area, a number of excellent reviews have been dedicated to the topic of polymer solar cells. These reviews have covered various aspects of this interdisciplinary research field, such as design of polymers,[26–28] device physics,[29,30] physical chemistry,[31,32] morphology control,[33–39] and stability/economics.[40,41] Rather than contributing another comprehensive review, we attempt to direct the readers' attention to the latest advances in the design of new polymeric materials for BHJ solar cells. We will focus on the outstanding issues in the molecular design of conjugated polymers that warrant further research activities, such as (1) lowering the lowest unoccupied molecular orbital (LUMO) energy level and enhancing the external quantum efficiency (EQE), as well as advantageously utilizing (2) electron-withdrawing substituents and (3) side chains. For each section, we will begin by discussing a few selected molecular systems, so as to introduce empirical guidelines for future design. We will then recommend additional research directions not yet fully explored. In doing so, we aim to further inspire creative molecular designs from the research community, in order to reach even higher efficiencies.



Rycel Uy earned her B.S. in Chemistry from the University of Nevada, Las Vegas in 2008. She is currently a Ph.D. candidate in Professor Wei You's group at the University of North Carolina at Chapel Hill, where she works on developing new polymer materials, particularly thienothiazole-based ones, for use in bulk heterojunction solar cells.



Sam Price earned his B.S. in Chemical Engineering from North Carolina State University in 2006, and received his Ph.D. in Chemistry in Prof. You's group in 2011 studying conjugated polymers. He is currently a postdoctoral researcher for the Army Research Lab at Aberdeen Proving Ground. His research interests focus on functional materials for energy and electronics applications.



Wei You was born in a small village outside of Chuzhou in Anhui Province of China, and grew up in Hefei, the provincial capital of Anhui. After receiving a B.S. degree in Polymer Chemistry from University of Science and Technology of China in 1999, he attended the graduate program of chemistry at the University of Chicago, where he obtained his Ph.D. in 2004 under the guidance of Professor Luping Yu. He then moved west and finished his postdoctoral training at Stanford University in 2006 with Professor Zhenan Bao. In July 2006, he joined the University of North Carolina at Chapel Hill as an Assistant Professor in Chemistry. Professor You's research interests focus on the development of novel multifunctional materials for a variety of applications, including organic solar cells, molecular electronics, and spintronics.

2. Lower LUMO Energy Level and Higher EQE

Excitons in organic semiconductors typically have a binding energy between 0.1–1.0 eV,[42,43] and thus photovoltaic cells employing organic semiconductors (typically *p*-type) require an additional semiconductor (typically $PC_{61}BM$ as the *n*-type) with a lower LUMO energy level to split these Frenkle excitons. However, even though conventional wisdom quotes a 0.3 eV driving force required to dissociate an exciton from a conjugated polymer, the vast majority of conjugated polymers developed in the past five years have a $LUMO_{polymer} - LUMO_{PCBM}$ gap (ΔE_{ED}) much greater than the 0.3 eV required. For example, regioregular P3HT has a measured ΔE_{ED} of 1.1 eV,[44] which gives a 0.8 eV excess energy that is wasted when the excited electron is transferred to PCBM (Figure 4).[45] Therefore the primary method for increasing the performance of the conjugated polymer is to decrease ΔE_{ED} to as close to 0.3 eV as possible.[46] This would help achieve both a small band gap and a low highest occupied molecular orbital (HOMO) energy level, in order to get both a high short-circuit current (J_{sc}) and a high open-circuit voltage (V_{oc}).

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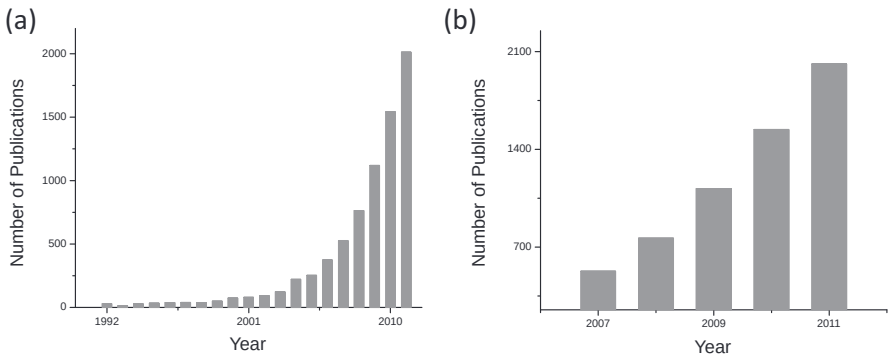


Figure 1. (a) Number of publications on organic solar cells since 1992. (b) Number of publications in the last 5 years.

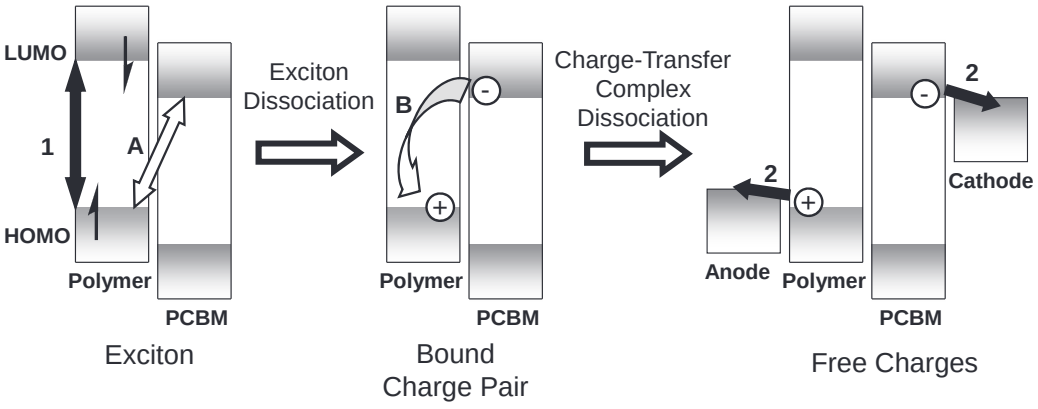


Figure 2. The process of exciton dissociation to charge separation. Parameters that affect the open circuit voltage (V_{oc}) are shown with white arrows and letters, parameters that affect the short circuit current (J_{sc}) are shown with black arrows and numbers.

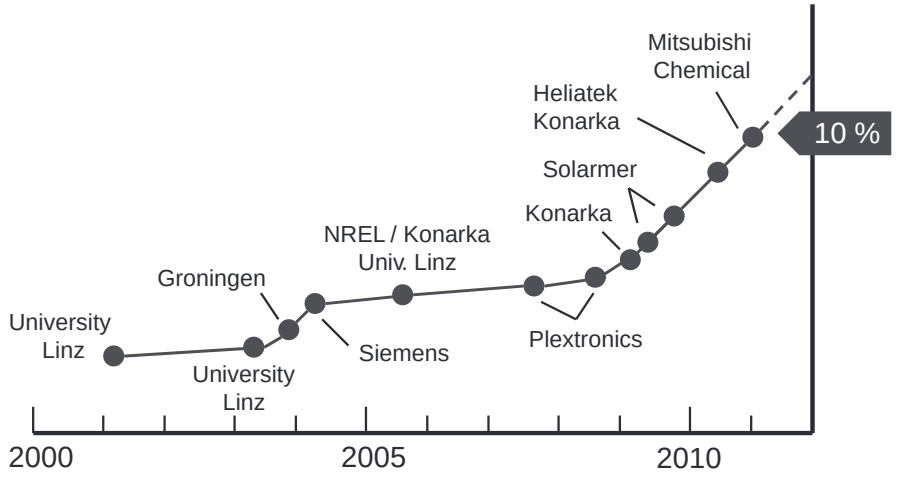


Figure 3. Selected power conversion efficiency results show significant progress. Adapted with permission[25]. Copyright 2010, Nature Publishing Group.

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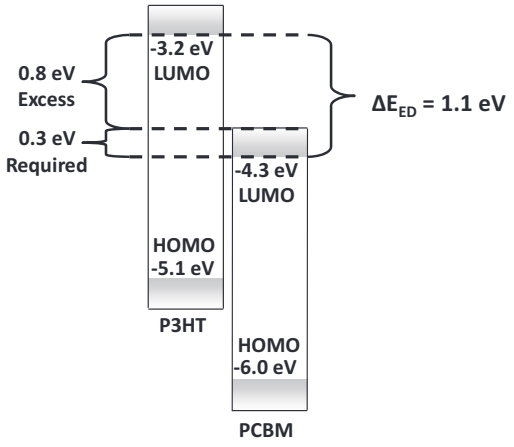


Figure 4. One of the key limitations of the P3HT:$PC_{61}BM$ system is the 1.1 eV $LUMO_{P3HT}$ - $LUMO_{PCBM}$ gap (ΔE_{ED}) where only 0.3 eV is required.

2.1. Current Status on the LUMO Level Engineering

Table 1 shows the top eight polymers which have achieved power conversion efficiencies above 7%, and the corresponding ΔE_{ED} of each polymer. The polymers with the lowest ΔE_{ED} of 0.4 eV are entries 3 and 4, employing the electron-deficient thieno[3,4-c]pyrrole-4,6-dione (TPD) monomer. TPD has been a very popular monomer recently in the literature, with three groups recently reporting polymer cells over 7% efficiency with this particular monomer unit,[17–20] among other high-performing ones.[47,48] The measured electrochemical LUMO for TPD materials is typically around –3.9 eV, which is the lowest electrochemical LUMO ever reported for a material with over 7% efficiency. Its widespread success is likely due to the low ΔE_{ED} for this class of materials. However, the EQE values for this family of polymers remain below 70%, therefore, additional work is required to optimize the other factors which govern photovoltaic performance that have allowed other materials with larger ΔE_{ED} values to reach EQE values greater than 70%.

2.2. Promising Electron-Deficient Structural Units

In order for BHJ photovoltaic cells to reach 10% or higher efficiency with $PC_{61}BM$, the LUMO of conjugated polymers must be reduced further still to at least –4.0 eV while maintaining a high EQE value. Therefore, in order to synthesize polymers with exceptionally low LUMO energy levels, new easily reduced aromatic moieties which can be readily included into conjugated polymers are required.

The most common method for synthesizing low-bandgap copolymers is the intramolecular charge transfer (ICT) approach,[49,50] in which the HOMO and LUMO energy levels are determined by different monomers, allowing the synthetic chemist to independently control both energy levels. The most widely investigated ICT LUMO reducing materials are based upon 2,1,3-benzothiadiazole (BT). One such material has reached IQE values of near 100% with a LUMO energy level of –3.6 eV.[15] Recent research has focused on designing aromatic moieties, which are more electron-deficient than BT, by either adding electron-withdrawing groups, pyridinal nitrogens, or additional electron-deficient rings to the benzothiadiazole core.

Pyridazine-based monomers are one promising yet unexplored family of electron-deficient heterocycles that have measured LUMO energy levels between –3.88 and –4.15 eV (Figure 5). Gendron and co-workers have led initial studies into these heterocycles as acceptors for conjugated polymers, showing significant results.[51] The key drawback for these reported materials is the low molecular weight, likely due to inhibition of the palladium catalytic cycle during polymerization. This drawback has kept performance below 1% efficiency for this class of materials. However, the promising LUMO level of these materials warrants further study into methods, which could deliver high-molecular-weight polymers based upon pyridazine electron acceptors (Table 2).

Monomers based upon indigo dye are another class of electron-deficient heterocycles which have the potential to provide low LUMO levels. Initial investigations by Reynolds and co-workers[53] have developed isoindigo as an electron-deficient moiety, yielding *p*-type chromophores with LUMO energy levels as low as –3.9 eV. When copolymerized in a typical ICT fashion through Stille coupling polycondensation, these systems yield power conversion efficiencies of over 4.0%. These initial results could likely be improved upon,[57–60] and indigo- and isoindigo-based systems are especially intriguing because of their ability to attach alkyl chains to the LUMO reducing unit.

2.3. The Issue of Low Absorption Coefficient

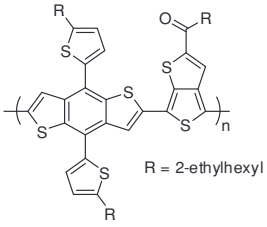
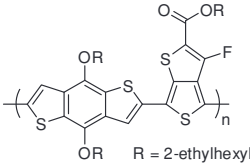
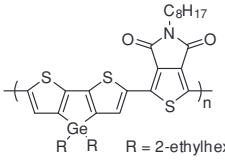
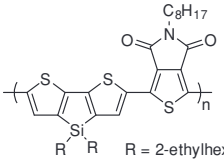
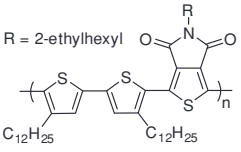
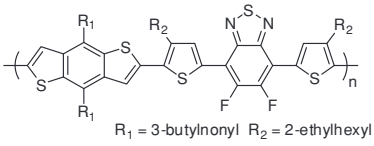
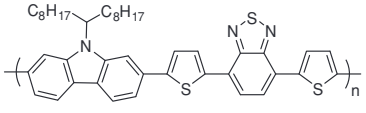
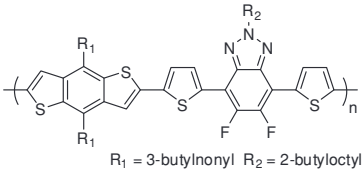
One major drawback of using exceptionally electron-deficient benzothiadiazoles and other electron-deficient acceptors for use in ICT copolymers is that the LUMO and HOMO are quite often located on different parts of the polymer, rather than delocalized along the polymer chain. This leads to relatively weak absorption coefficients, since excitation from the HOMO to the LUMO becomes quantum mechanically disallowed. An extreme example of this shortcoming is the case of polymers synthesized from cyclopenta[2,1-*b*:3,4-*b'*]dithiophen-4-one (CPD)[61] shown in Figure 6.

CPD-based systems such as the polymers and small molecules shown in Figure 7 exhibit exceptionally low LUMO levels, with malonitrile condensation derivatives such as (3) reaching LUMO levels below –4.2 eV. The CPD

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Table 1. Top eight polymer solar cells over 7% and their photovoltaic properties.

	Polymer Structure	Polymer Properties		References
1	 R = 2-ethylhexyl	$\eta = 7.6\%$ $\Delta E_{ED} = 1.1$ eV	HOMO = −5.1 eV LUMO = −3.3 eV $E_g = 1.6$ eV	[14]
2	 R = 2-ethylhexyl	$\eta = 7.4\%$ $(\eta = 8.4\%)$[13] $\Delta E_{ED} = 0.6$ eV	HOMO = −5.5 eV LUMO = −3.7 eV $E_g = 1.6$ eV	[11]
3	 R = 2-ethylhexyl	$\eta = 7.4\%$ $\Delta E_{ED} = 0.4$ eV	HOMO = −5.6 eV LUMO = −3.9 eV $E_g = 1.7$ eV	[17,18]
4	 R = 2-ethylhexyl	$\eta = 7.3\%$ $\Delta E_{ED} = 0.4$ eV	HOMO = −5.6 eV LUMO = −3.9 eV $E_g = 1.7$ eV	[20]
5	 R = 2-ethylhexyl	$\eta = 7.3\%$ $\Delta E_{ED} = 0.6$ eV	HOMO = −5.6 eV LUMO = −3.7 eV $E_g = 1.8$ eV	[19]
6	 R_1 = 3-butylnonyl R_2 = 2-ethylhexyl	$\eta = 7.2\%$ $\Delta E_{ED} = 0.7$ eV	HOMO = −5.8 eV LUMO = −3.6 eV $E_g = 1.7$ eV	[21]
7		$\eta = 7.2\%$ $\Delta E_{ED} = 0.7$ eV	HOMO = −5.5 eV LUMO = −3.6 eV $E_g = 1.9$ eV	[15,16]
8	 R_1 = 3-butylnonyl R_2 = 2-butyloctyl	$\eta = 7.1\%$ $\Delta E_{ED} = 0.9$ eV	HOMO = −5.7 eV LUMO = −3.4 eV $E_g = 2.0$ eV	[22]

[a]All HOMO/LUMO levels use Fc/Fc+ as −4.8 eV from vacuum. PCBM = −4.3 eV.

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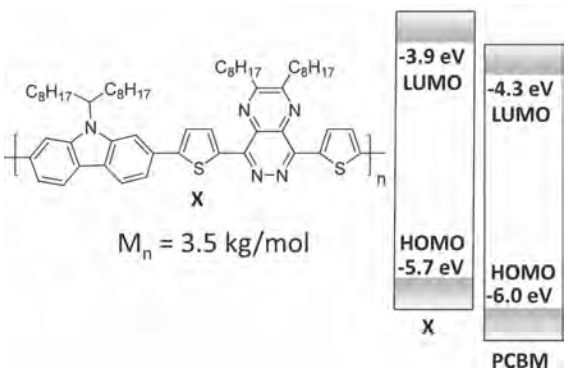
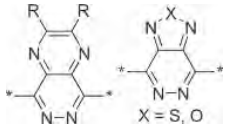
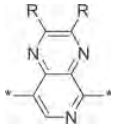
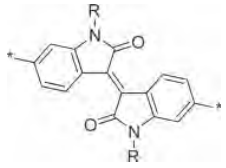
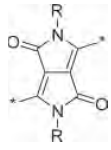


Figure 5. Pyridazine-based polymer with a near optimal LUMO.

monomer is so easily reduced because the unreduced form is a 13 electron ring system, one electron short of the 14 required to fulfill Hückel's rule. However, even though polymers and small molecules synthesized with CPD-based systems possess very low electrochemical band gaps, the optical absorption in the low energy portion of the spectrum is typically very poor.[62]

Similar poor absorption coefficients in the infrared portion of the absorption spectrum are seen in the case of benzo[1,2-*c*;4,5-*c*′] bis[1,2,5]thiadiazole-based copolymer systems as well, due to the same issues.[63,64] Therefore, when designing new acceptors for ICT polymers, emphasis

Table 2. Series of promising heterocycles, which have measured LUMO energy levels of −3.9 or lower that have not reached greater than 6% efficiency.

	LUMO reducing unit	LUMO range [ev]	References
1		−3.9 to − 4.2	[51]
2		−3.7 to − 4.0	[52]
3		−3.8 to − 3.9	[53]
4		−3.6 to − 3.9	[54–56]

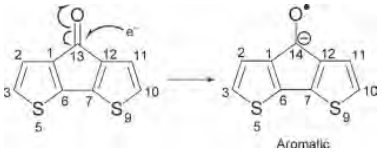


Figure 6. CPD monomer is an easily reduced, 13 electron species. Addition of 1 more electron causes the entire heterocyclic system to become aromatic because it has 14 electrons. The LUMO orbital resides almost exclusively on the carbonyl.

needs to be placed on delocalizing the LUMO along the polymer backbone, rather than localizing it on only a few atoms. Otherwise, low absorption coefficients will result.

Thus, while many successful electron-deficient monomers have been synthesized, there has still not been one comonomer, which allows for an optimal LUMO and EQE values above 70–80%. The next generation of LUMO-reducing monomers must be designed with optimal LUMOs, high absorption coefficients, and structures that promote fast charge extraction from the active layer to achieve maximum performance.

3. Influence of External Substituents

A growing trend has been to incorporate electron-withdrawing substituents into the polymer structure, which in many cases have led to dramatic enhancements in solar cell performance.[11,21,22,65] It has already been demonstrated that they can effectively lower the HOMO and LUMO levels.[66] However, researchers have yet to determine why these substituents, especially the fluorine atom, seem to have a good effect on the hole mobility, morphology, and charge dissociation of the polymer. The following section will categorize examples based on substituent location (on the electron-deficient acceptor moiety or the electron-rich donor moiety) and attempt to survey how photovoltaic properties are impacted.

3.1. Substitution on the Electron-Deficient Acceptor Moiety

Polymer backbones substituted with fluorines on the most electron-deficient unit have received widespread attention for their exceptional performance in solar cells. Three of the top polymers achieving over 7% efficiency contain the benzodithiophene (BnDT) unit copolymerized with a fluorinated acceptor moiety such as thienothiophene (TT),[11] benzotriazole (TAZ),[22] and benzothiadiazole (BT).[21] Table 3 lists the photovoltaic properties compared with their non-fluorinated counterparts, and as can be seen, fluorinating the acceptor moiety seems to lead to better photovoltaic properties all around.

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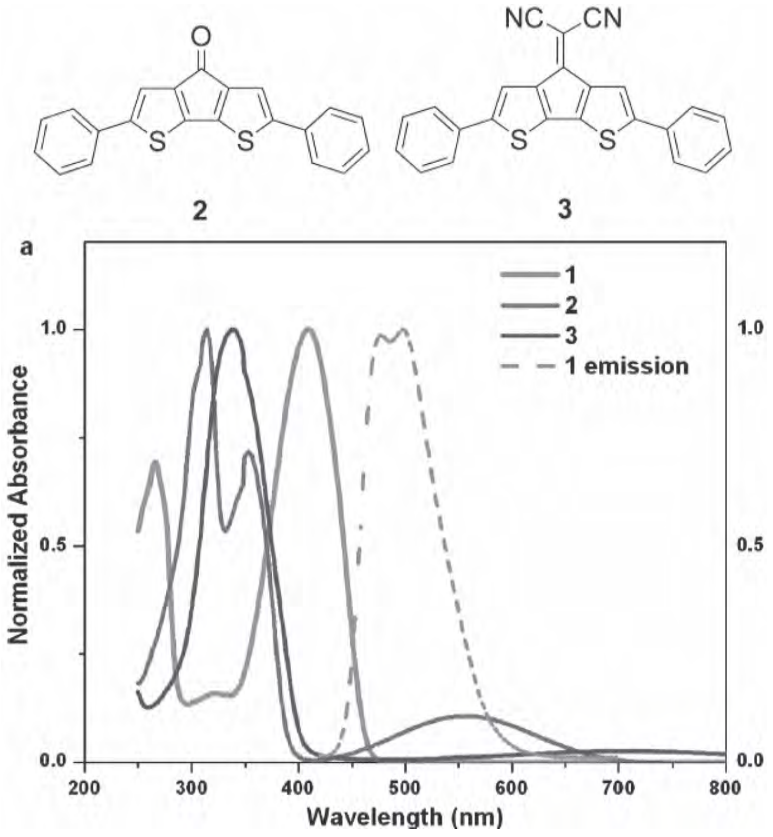


Figure 7. Molecules 2 and 3 have electrochemical band gaps of 2.1 and 1.7 eV, respectively, yet the absorption coefficients below 3.0 eV (413 nm) for these compounds are exceptionally poor. Adapted with permission.[62] Copyright 2011, American Chemical Society.

The PTB polymer series was the first to draw attention to incorporating fluorine into DONOR polymers and thus will be the main focus in this section because many studies have already been conducted on this series. Fluorine was originally introduced to the 3-position of the TT moiety as a second electron-withdrawing group (the first being the ester alkyl group) to further lower the HOMO level and therefore enhance V_{oc}.[65,68] Studies on PTB have shown that fluorine only lowers the HOMO level by –0.15 eV (PTB9 vs. PTB7) while the V_{oc} improves from only 0.60 to 0.74 V.[11,67]

In an attempt to further optimize the HOMO level of PTB polymers, attention was turned toward other electron-withdrawing substituents. Table 4 shows the various methods in which TT has been modified. Interestingly, when TT was substituted with only a ketone (entry 3), the HOMO level was brought down to –5.12 eV, indicating that a ketone has a comparable electronic impact on PTB as do an ester and fluorine combined.[69] When a ketone and fluorine were used in conjunction along with an alkyl chain on the BnDT unit (entry 4), the HOMO level significantly lowered to –5.34 eV.[70] However, further attempts to use the even more electron-withdrawing sulfonyl again yielded a HOMO level of only –5.12 eV (entry 5).[71] When Ikai and co-workers[72] employed phenyl ester pendants 4-fluorophenyl and 4-(trifluoromethyl)phenyl, deep HOMO levels of –5.39 eV and –5.60 eV were observed (entries 6 and 7). However, polymers exhibited rather low mobilities (2.8 10^{-5} and 1.4 10^{-5} $cm^2\ V^{-1}\ s^{-1}$, respectively), most likely due to the lack of a side chain on TT and the extremely bulky 2-octyldodecyloxy solubilizing chain that was needed on the BnDT unit.[72]

In an effort to remove reliance on external substituents, a nitrogen atom was introduced into TT (entry 8), thereby changing the unit to the more electron-deficient thienothiazole (TTz), which can also stabilize its quinoid form.[73] Initial results for PBnDT-TTz showed a higher efficiency of 2.5% compared with its direct TT analog, but the HOMO level of this TTz-based polymer was still not quite low enough. Just recently, Yu and co-workers[67] reported selenium-based derivatives of their PTB series. The resulting –5.05 eV HOMO level of PBSe1 (entry 9) was similarly high as its sulfur-based analog (entry 1).

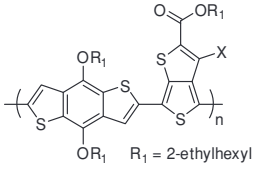
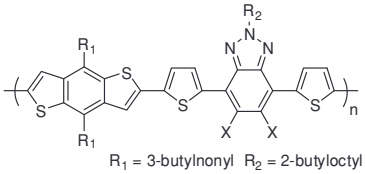
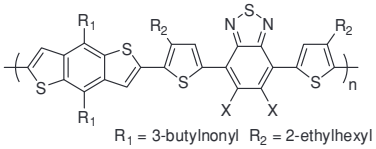
Of the various electron-withdrawing groups used, fluorine appears to be one of the most promising because it not only lowers the HOMO level but appears to improve morphology. PTB7, which achieved a previously record-breaking 7.4% efficiency,[11] has demonstrated a very favorable morphology. The "zig-zag" shape of PTB's backbone is credited with being responsible for its face-on orientation, which allows for maximal contact with the electrode.[74] Furthermore, a grazing incidence wide-angle X-ray scattering (GIWAXS) study proposes that within the active layer, a hierarchy exists ranging from PTB7 nanocrystallites > interpenetrating regions of polymer and fullerene > PCBM nanocrystallites (Figure 8).[75] The PTB7 crystalline aggregates are believed to be responsible for the high photocurrent observed because its crystallinity not only reduces charge transfer energy, but also is similar in size to exciton diffusion lengths (4–20 nm). Thus, when an exciton is generated within a PTB7 nanocrystallite, the process toward dissociating charges is greatly facilitated (inset of Figure 8). Whether or not this proposed morphology is inherent to PTB polymers or due to fluorine has yet to be determined. Thus, other

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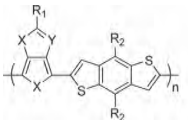
Table 3. Photovoltaic properties of high-performing fluorinated polymers and their nonfluorinated counterparts.

		X	η [%]	V_{oc} [V]	J_{sc} [mA/cm^{-2}]	*FF* [%]	μ_{hole} [cm^2 V^{-1} s^{-1}]	References
1	 R_1 = 2-ethylhexyl **PTB7** vs. **PTB9**	F	7.40	0.74	14.50	68.97	5.8 10^{-4}	[11]
		H	5.54	0.60	14.40	66.00	4.0 10^{-4}	[67]
2	 R_1 = 3-butylnonyl R_2 = 2-butyloctyl **PBnDT-FTAZ** vs. **PBnDT-HTAZ**	F	7.10	0.79	11.83	72.9	1.0 10^{-3}	[22]
		H	4.36	0.70	11.14	55.2	2.9 10^{-4}	
3	 R_1 = 3-butylnonyl R_2 = 2-ethylhexyl **PBnDT-DTffBT** vs. **PBnDT-DTBT**	F	7.2	0.91	12.91	61.2	8.3 10^{-5}	[21]
		H	5.0	0.87	10.03	57.3	3.8 10^{-5}	

fluorinated systems, especially their morphology, should be further investigated.

Similar improvements in morphology are observed in the benzothiadiazole and benzotriazole-based polymers, both of which were fabricated without the use of additives.[21,22] When compared with their nonfluorinated counterparts, the x-ray diffraction (XRD) data of PBnDT–DTffBT and PBnDT–FTAZ both show larger *d*-spacing values: 18.1 versus 17.7 Å for benzothiadiazole polymers and 18.7 versus 17.8 Å for benzotriazole polymers. It is likely that the repulsive nature of the fluorine atoms is keeping PCBM further away during electron-transfer

Table 4. Various methods of modifying thienothiophene and resulting photovoltaic properties.



C6,2 = 2-ethylhexyl
PhF = 4-fluorophenyl
$PhCF_3$ = 4-(trifluoromethyl)phenyl

OC6,2 = 2-ethylhexyloxy
C9,4 = 3-butylnonyl
OC12,8 = 2-octyldodecyloxy

	X	Y	R_1	R_2	HOMO [eV]	V_{oc} [V]	η [%]	References
1	S	C—H	Ester, C6,2	OC6,2	−5.00	0.60	5.54	[67]
2		C—F	Ester, C6,2	OC6,2	−5.15	0.74	7.40	[11]
3		C—H	Ketone, C6,2	OC6,2	−5.12	0.70	6.3	[69]
4		C—F	Ketone, C6,2	C9,4	−5.34	0.86	3.9	[70]
5		C—H	Sulfonyl, C6,2	OC6,2	−5.12	0.76	6.22	[71]
6		C—H	Phenyl ester, PhF	OC12,8	−5.39	–	–	[72]
7		C—H	Phenyl ester, $PhCF_3$	OC12,8	−5.60	–	–	[72]
8		N	Alkyl, C6,2	OC6,2	−5.06	0.69	2.5	[73]
9	Se	C—H	Ester, C6,2	OC6,2	−5.05	0.66	5.39	[67]

*Please see respective references for processing conditions and fullerene material used.

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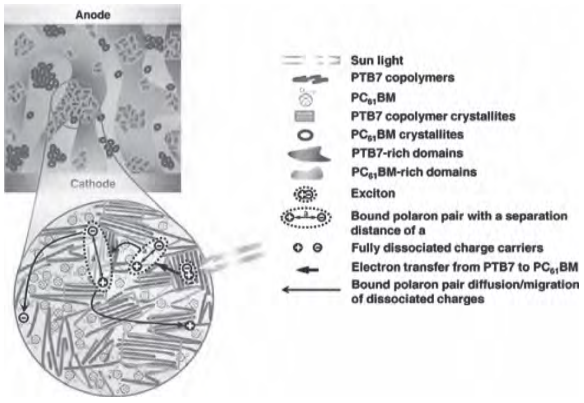
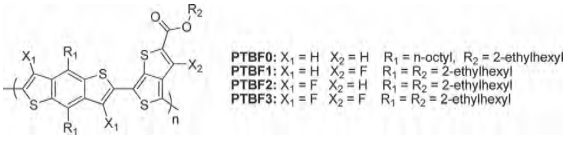


Figure 8. Diagrammatic hypothesis of the hierarchical nanomorphologies in the PTB7/PCBM active layer. Reproduced with permission.[75] Copyright 2011, American Chemical Society.

reactions, possibly enhancing electron-hole charge-transfer complex separation and slowing down processes such as charge recombination. However, additional studies beyond XRD are needed to accurately elucidate the behavior between fluorinated polymers with PCBM.

This then begs the question: is there a certain fluorine concentration that leads to optimum interactions with PCBM? Jen and co-workers[76] examined nonfluoro-, monofluoro-, and difluoro-substituted benzothiadiazole polymers PIDT–BT, PIDT–FBT, and PIDT–DFBT (Table 5). As expected, the HOMO energy levels lowered and V_{oc} increased with increasing fluorine concentration on the benzothiadiazole acceptor moiety. However, other properties such as J_{sc}, *FF* (fill factor), and hole mobility were roughly similar for all three polymers. Given that this is just one specific series, it would be interesting to see similar studies conducted on other systems. Such studies would gauge the influence of fluorine concentration on how polymers pack with fullerenes and the effect on charge recombination (geminate and bimolecular) to give further insight on charge transfer processes with PCBM.



Scheme 1. Chemical structures of PTBF polymer series.

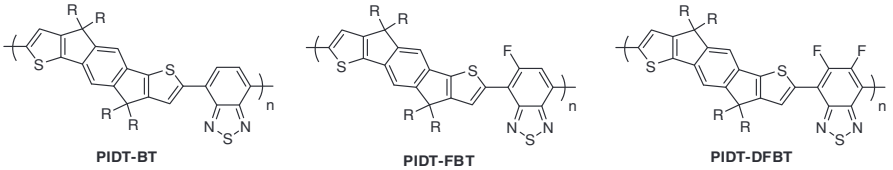
3.2. Substitution on the Electron-Rich Donor Moiety

Not all fluorine substitutions appear to be beneficial. When Yu and co-workers[77] fluorinated the BnDT donor moiety (Scheme 1), solar cells performed poorly compared with PTB7.[77] Similar to the previous strategy, fluorinating the BnDT unit was intended to fine-tune the HOMO level of PTB polymers. The resulting HOMO levels of PTBF2 and PTBF3 were indeed lowered by –0.26 and –0.33 eV, respectively. However, transmission electron micrographs (TEM) of the polymer–PCBM films for PTBF2 and PTBF3 revealed noncontinuous networks with large phase domains on the order of 50–200 nm (Figure 9), encouraging charge recombination and leading to dramatic decreases in V_{oc}, *FF*, and efficiency. In addition to the difficulty of synthesizing the fluorinated BnDT unit, PTBF2 and PTBF3 were observed to be unstable. The fluorines on BnDT pull electron density away from the TT moiety, concentrating it on the 4- and 6-positions of TT, making the polymer vulnerable to singlet oxygen attack.

3.3. Substituent Location

The improvement or decline in morphology of DONOR polymers is most likely related the location of the fluorine(s), more specifically which moiety is fluorinated. When the most electron-deficient unit is fluorinated (such as TT,[11,74] benzothiadiazole,[21] or benzotriazole),[22] the fluorines seem to keep PCBM at a distance creating

Table 5. Photovoltaic properties of PIDT-BT, PIDT-FBT, PIDT-DFBT.



Polymer	HOMO level [eV]	V_{oc} [V]	J_{sc} [mA/cm^{-2}]	*FF* [%]	μ_{hole} [cm^2 V^{-1} s^{-1}]	η [%]
PIDT-BT	–5.23	0.81	11.23	55	4.69 10^{-2}	5.02
PIDT-FBT	–5.38	0.86	11.23	56	3.38 10^{-2}	5.40
PIDT-DFBT	–5.48	0.92	10.87	51	2.88 10^{-3}	5.10

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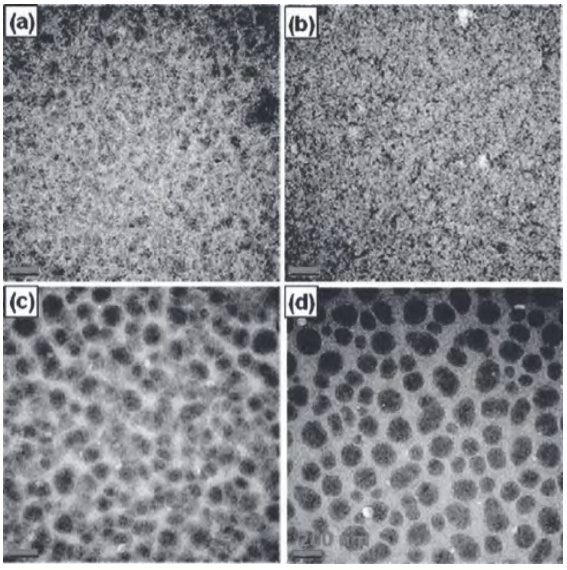


Figure 9. TEM images of polymer/$PC_{71}BM$ blend films prepared from dichlorobenzene solvent: PTBFo (a), PTBF1 (b), PTBF2 (c), and PTBF3 (d). Scale bar = 200 nm. Reproduced with permission.[77] Copyright 2011, American Chemical Society.

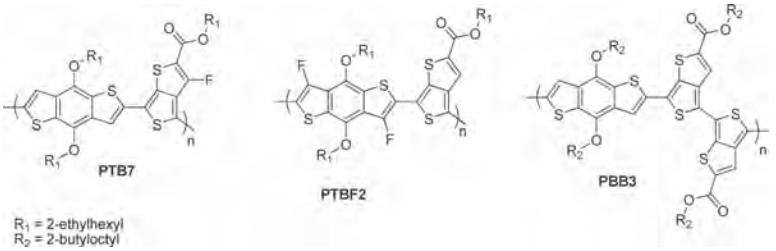
phase domains (≈10–20 nm) that favor charge separation. It is unclear if this is a property inherent to these specific polymer systems because this favorable polymer–PCBM interaction is not observed when the electron-rich unit (BnDT) is fluorinated.[77] From an electronic standpoint, this is in agreement with the weak donor-strong acceptor approach.[78] The "weak donor" should be kept electron-rich and the "strong acceptor" should be as electron-deficient as possible.

In addition, a recent report by the Yu group suggests that electron-withdrawing groups should be placed such that the resulting local dipole moments do not cancel each other out based on their study of PTBF2 and PBB3.[79] PTBF2 contains two opposing fluorines on the BnDT unit while PBB3 contains two adjacent TT units *trans* to another. In both cases, the internal dipole moment is greatly reduced according to calculations. Similar to PTB7, polymer PBB3 exhibits a good thin-film morphology, a high hole mobility, and even lower band gap (Table 6). Despite these favorable characteristics, PBB3 shows a comparatively low J_{sc} and thus efficiency of only 2.04%, suggesting that other factors need to be considered. Yu et al. propose that the minimized dipole moment in PTBF2 and PBB3 prevents the excited state from polarizing, leading to faster charge recombination and ultimately low power conversion efficiencies.

3.4. Recommendation

The influence of fluorine on hole mobility, morphology, and other photovoltaic properties has yet to be quantified or correlated. Yu and co-workers[65] suggest that there appears to be increased interaction between electron-rich aromatic rings and electron-deficient fluorinated aromatic rings. This is consistent with findings that fluorinated and nonfluorinated rings stack co-facially rather than in herringbone fashion as observed in traditional benzene rings.[80,81] Matsuo and co-workers[82] have recently demonstrated that Ar—F··Ar—H and CH··F interactions help facilitate face-to-face stacking in FPPT compared with that in PPT (Scheme 2 and Figure 10), which leads to a hole mobility two orders of magnitude greater in FPPT.[82] Although this study was done on small molecules for organic thin-film transistors, an analogous study in the context of DONOR polymers for solar cells would certainly be beneficial to further understand the interesting behavior of these fluorines. For example, would it be beneficial to have a 1:1 ratio of fluorinated to nonfluorinated rings? Would it be favorable for the donor and fluorinated acceptor

Table 6. Photovoltaic properties of PTB7, PTBF2, and PBB3.



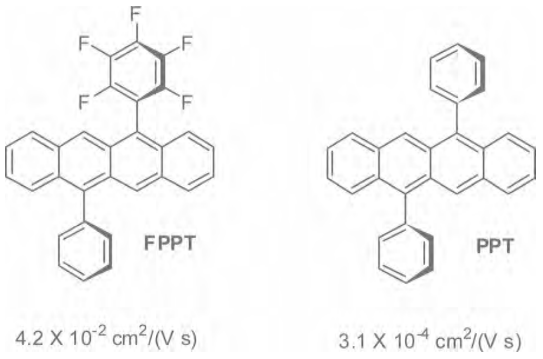
Polymer	HOMO [ev]	LUMO [eV]	E_g [eV]	V_{oc} [V]	J_{sc} [mA cm^{-2}]	FF [%]	μ_{hole} [cm^2 V^{-1} s^{-1}]	η [%]
PTB7	−5.15	−3.31	1.84	0.74	14.5	68.97	4.1 10^{-4}	7.40
PTBF2	−5.41	−3.60	1.81	0.68	11.1	42.2	1.8 10^{-4}	3.20
PBB3	−4.95	−3.28	1.67	0.63	6.37	51.0	1.1 10^{-4}	2.04

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Scheme 2. Chemical structures of FPPT and PPT and corresponding hole mobilities.

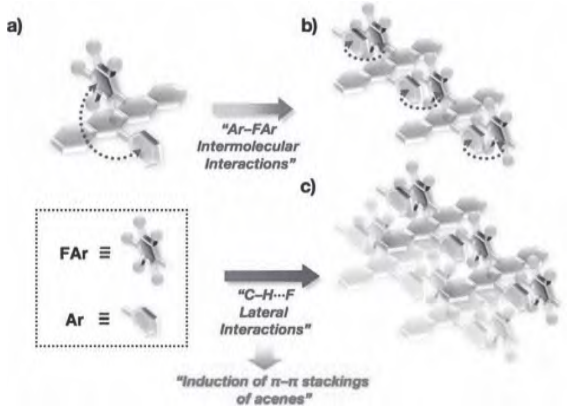


Figure 10. Molecular design and concept for the enhancement of π–π stacking between neighboring charge transporting units by the introduction of Ar and FAr substituents. Reproduced with permission.[82] Copyright 2011, American Chemical Society.

moieties to be similarly shaped? More studies focused on the physical chemistry and device physics of carefully crafted systems are needed to elucidate fluorinated polymer–PCBM interactions and how morphology, hole mobility, local dipole moments, and charge recombination are affected.

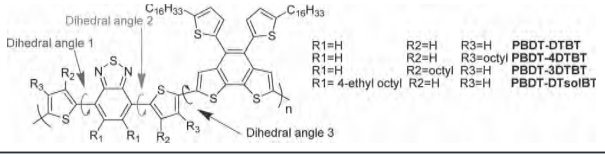
4. Side Chains: Beyond the Solubility

One of the main advantages that organic solar cells can boast over their inorganic counterparts is that they can be solution processed, and therefore much cheaper to produce. Thus, side chains are a necessary component to designing conjugated polymers. Recent studies have discovered that the function of these side chains is for more than just solubilizing purposes. The nature of side chains employed often dictates the solid-state morphology in the active layer, which in turn, influences intermolecular interactions such as polymer–polymer and polymer–PCBM, as well as charge transport.[48,83] Inspecting the top polymers over 7% (Table 1) reveals no clear pattern of the best combination of side chains and where on the backbone they should be anchored. The optimum combination of position and size is likely to be polymer specific and sometimes can only be determined after synthesizing an exhaustive library. Nevertheless, this section will attempt to survey key guidelines that have emerged as generally applicable, and shine a spotlight on less commonly employed chains by examining the following types: nonaromatic, aromatic, and end-group functionalized.

4.1. Nonaromatic Side Chains

The vast majority of DONOR polymers utilize simple alkyl or alkoxy side chains, and deciding where to position them on the polymer can profoundly affect performance. The PBDT–DTBT series demonstrates that the optimum location for side chains should cause the least steric disturbance to the planarity of the polymer backbone.[84,85] In this series, PBDT–4DTBT, which is alkylated at the four-position of the thienyl groups, exhibited the highest efficiency in its BHJ solar cells (Table 7). Similar to the control polymer

Table 7. Power conversion efficiencies, calculated dihedral angles, and polymerization results for PBDT–DTBT polymers. Reproduced with permission.[84] Copyright 2010, American Chemical Society.



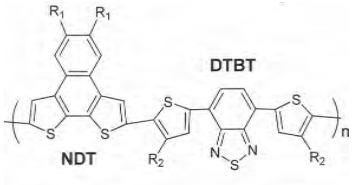
Polymer	η [%]	Dihedral angle 1 [°]	Dihedral angle 2 [°]	Dihedral angle 3 [°]	$\overline{M}_n$ [kg mol^{-1}]	$\overline{M}_w$ [kg mol^{-1}]
PBDT – DTBT	1.83	4.1	10.9	14.1	9	12
PBDT – 4DTBT	0.21	5.2	14.3	30.2	27	54
PBDT – 3DTBT	0.01	50.7	36.2	17.7	37	84
PBDT – DTsolBT	0.72	58	55.2	19.9	30	92

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Table 8. Photovoltaic properties of PNDT–DTBT polymers. Reproduced with permission.[86] Copyright 2010, American Chemical Society.



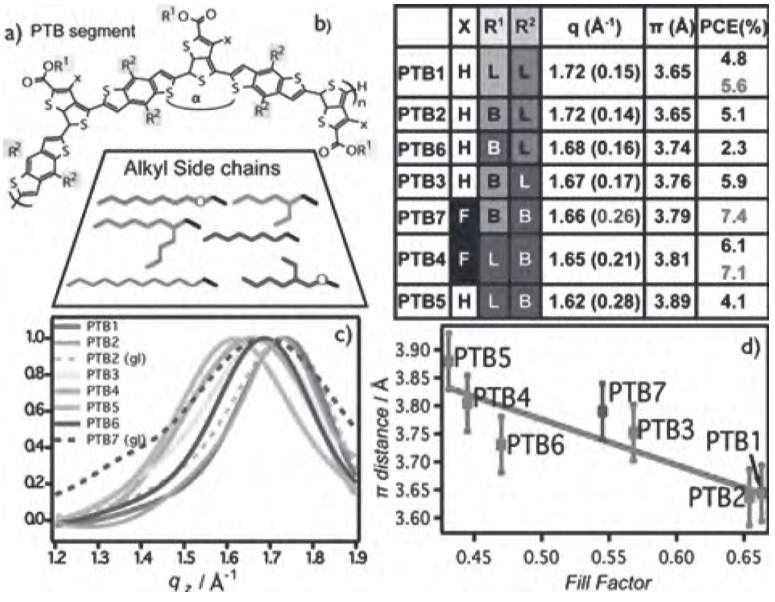
R1=2-hexyldecyl	R2=octyl	C10,6-C8
R1=2-hexyldecyl	R2=2-ethylhexyl	C10,6-C6,2
R1=octyl	R2=octyl	C8-C8
R1=octyl	R2=dodecyl	C8-C12
R1=octyl	R2=2-ethylhexyl	C8-C6,2
R1=2-ethylhexyl	R2=2-ethylhexyl	C6,2-C6,2

Polymer	V_{oc} [V]	J_{sc} [mA cm^{-2}]	*FF* [%]	η [%]
C10,6-C8	0.59	7.98	46.05	2.17
C10,6-C6,2	0.81	5.62	44.07	2.01
C8-C8	0.41	6.97	42.05	1.20
C8-C12	0.52	5.88	42.09	1.28
C8-C6,2	0.59	10.93	46.43	3.00
C6,2-C6,2	0.69	10.67	45.90	3.36

(nonalkylated PBDT–DTBT), PBDT–4DTBT maintains the most planar backbone as evidenced by its small calculated dihedral angles and low band gap. But unlike the control polymer, PBDT–4DTBT's solubilizing chains allow it to achieve a higher molecular weight and efficiency. Since many DONOR polymers contain thienyl groups, the design concepts established in this work can easily be applied to those systems as well as others. This study highlights the importance of strategically placing solubilizing chains such that there is no excessive twisting in the backbone and polymers can attain high molecular weight.

Upon deciding where to place the side chains, the next decision is what length (long or short) and shape (linear or branched) they should be, which can greatly impact properties such as J_{sc} and V_{oc}. You and co-authors[86] studied six polymers with an identical backbone (PNDT–DTBT) but with varying linear and branched side chains on both the NDT and DTBT units (Table 8).[86] Because of the identical backbone, the different side chain combinations represent the difference in π–π stacking between the aromatic cores. In general, a closer π-stacking distance reduces the energy barrier for intermolecular charge hopping while also minimizing charge trapping sites.[87] This systematic study on PNDT–DTBT polymers demonstrates that long and branched side chains weaken the intermolecular polymer interactions but also enhance V_{oc} (polymer C10,6-C6,2). On the other hand, short and straight side chains encourage polymer packing, increasing the J_{sc} at the expense of V_{oc} (polymer C8-C6,2). In order to mediate these opposing trends, it was found that short and branched side chains (polymer C6,2-C6,2) are the best compromise for attaining reasonably high V_{oc} and J_{sc}, leading to the optimum efficiency of 3.36% in this series.[86] A similar side chain study by Fréchet and co-workers[88] found that longer linear side chains can be used in place of branched chains for more soluble cores such as the furan-diketopyrrolopyrrole system.

Yu and co-workers[74] also found that linear versus branched chains affected polymer packing in the PTB polymers. As previously mentioned, PTB polymers intermolecularly stack in a face-on orientation. This favorable packing can be enhanced depending on whether or not the side chains are branched. GIWAXS results revealed that the BnDT unit is mostly responsible for controlling intermolecular π–π stacking interactions as it is composed of three fused aromatic units. Therefore, branched side chains on this unit increase the π–π stacking distance, decreasing *FF* and efficiency. For instance, the structures of PTB1 and PTB5 differ greatly by the chains on the BnDT unit (Figure 11). PTB1 containing a linear side chain exhibited a 3.65 Å π–π distance and 5.6% efficiency, whereas PTB5 containing a branched chain exhibited a larger 3.89 Å



	X	R^1	R^2	q (Å^{-1})	π (Å)	PCE(%)
PTB1	H	L	L	1.72 (0.15)	3.65	4.8 5.6
PTB2	H	B	L	1.72 (0.14)	3.65	5.1
PTB6	H	B	L	1.68 (0.16)	3.74	2.3
PTB3	H	B	L	1.67 (0.17)	3.76	5.9
PTB7	F	B	B	1.66 (0.26)	3.79	7.4
PTB4	F	L	B	1.65 (0.21)	3.81	6.1 7.1
PTB5	H	L	B	1.62 (0.28)	3.89	4.1

Figure 11. Photovoltaic properties and XRD values of PTB polymers. Reproduced with permission.[74]

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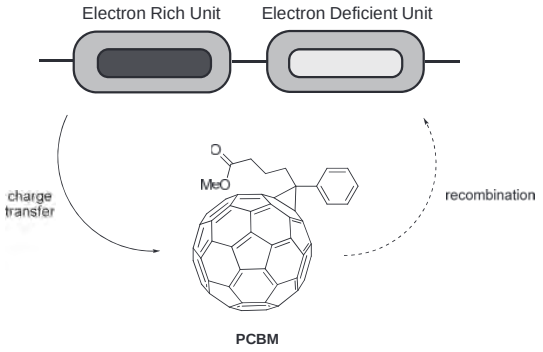
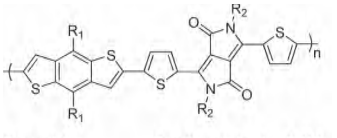


Figure 12. Possible interaction between polymer and PCBM, charger transfer, and recombination pathway are shown by arrows. Outer gray borders represent alkyl side chains. Reproduced with permission.[89] Copyright 2011 American Chemical Society.

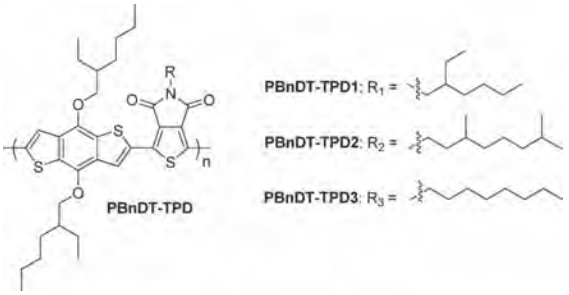
π–π distance and lower efficiency of 4.1%. In contrast, the side chain type on the TT unit does not appear to influence intermolecular π–π stacking, but most likely does so with PCBM interactions. For example, PTB1 and PTB2 contain the same chains on BnDT but linear or branched side chains, respectively, on the TT moiety, yet both exhibit the same 3.65 Å π–π spacing. In a similar side chain study on benzodithiophene and diketopyrrolopyrrole-based (BnDT–DPP) copolymers,[89] Li et al. proposed that the electron-rich BnDT should contain a linear side chain to possibly increase its contact with electron-poor PCBM and enhance charge transfer. Meanwhile the electron-deficient moiety DPP should contain bulky branched side chains to most likely repel PCBM and therefore prevent charge recombination (Figure 12). Thus, polymer O-HD was the front-runner in terms of photovoltaic performance (Table 9).

Despite these insightful studies on the type of side chains that should be used and where they should be anchored on the backbone of conjugated polymers, finding

Table 9. Photovoltaic properties of BnDT–DPP polymers. Reproduced with permission.[89] Copyright 2011, American Chemical Society.



Polymer	V_{oc} [V]	J_{sc} [mA cm^{-2}]	*FF* [%]	η [%]
O – HD	0.71	9.4	61	4.1
BO – BO	0.59	3.4	46	0.93
PU – O	0.62	5.2	43	1.4



Scheme 3. Structures of PBnDT–TPD polymers.

the optimum combination is still very much polymer specific and likely still an empirical process. For example, Fréchet and co-workers[48] investigated a series of copolymers (PBnDT–TPD) based on the BnDT and *N*-alkylthieno[3,4-c]-pyrrole-4,6-dione (TPD) (Scheme 3). According to grazing incidence X-ray scattering (GIXS) studies, PBnDT–TPD polymers may also pack face-on toward the substrate. However, unlike the TT in the previously mentioned PTB series, chain length on TPD moiety did in fact influence π–π stacking in the PBnDT–TPD series. The ethylhexyloxy chain on the BnDT was kept constant where R was varied on the TPD moiety. PBnDT–TPD1, which contained a short and branched ethylhexyl chain showed a larger π-stacking distance of 3.8 Å, whereas PBnDT–TPD2 and PBnDT–TPD3, which contained dimethyloctyl and octyl chains, respectively, showed a smaller *d*-spacing of 3.6 Å and lower efficiencies in their BHJ devices.

4.2. Aromatic Side Chains

Although much effort has gone into determining position, length, and branching of these solubilizing alkyl chains, the research field developing nonalkyl solubilizing chains, still remains under-explored. Aromatic side chains are particularly attractive because they can extend the conjugation of the polymer and therefore possibly promote hole mobility. Huo et al.[14,90] reported a series of PBDTTT polymers which compare alkylthienyl side chains against alkoxy chains (Table 10).[14,90] Both of the alkylthienyl-substituted polymers exhibited smaller band gaps, larger J_{sc} values, and higher efficiencies. The higher J_{sc} values were attributed to the higher hole mobilities of these polymers. These results indicate that although aromatic units as side chains may cause steric hindrance, this steric bulk can be advantageous if it extends conjugation and does not cause excessive repulsion between the polymer and PCBM.

4.3. End-Group Functionalized Side Chains

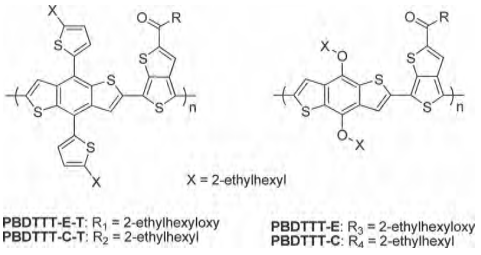
As charge separation occurs at the DONOR-ACCEPTOR interface, the physical interaction between the polymer

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Table 10. Photovoltaic properties of the PBDTTT polymer series. Reproduced with permission.[14]

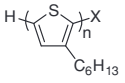


Polymer	V_{oc} [V]	J_{sc} [mA cm^{-2}]	*FF* [%]	η [%]	μ_{hole} [cm^2 V^{-1} s^{-1}]
PBDTTT-E	0.66	11.53	54.7	4.16	1.50 10^{-3}
PBDTTT-E-T	0.68	14.59	62.6	6.21	6.74 10^{-3}
PBDTTT-C	0.70	15.51	59.2	6.43	5.53 10^{-4}
PBDTTT-C-T	0.74	17.48	58.7	7.59	0.27

and PCBM has a significant impact on device performance. Kim et al.[91] have demonstrated that there is a correlation between end-group modification and the morphology of the active layer.[91] In their study, P3HT polymers end-capped with –Br, –OH, $-CH_2CH_3$, and $-CF_2CF_2CF_3$ were examined (Table 11). Of the four, P3HT–CH_3 and P3HT–CF_3 showed the highest efficiencies in BHJ devices and closest surface energies to PCBM. These well-matched surface energies resulted in a favorable balance between miscibility and phase separation between the polymer and PCBM, which ultimately led to better charge transport across the DONOR-ACCEPTOR interfaces. This suggests precedence that fluorinated polymers are morphologically compatible with PCBM.

So far there are a limited number of side chain end-modified polymer examples. However, the following squarine dyes and diketopyrrolopyrrole molecules (Scheme 4) have shown promising results. Bagnis et al.[92] compared two new alkyl- and alkyenyl-functionalized squarine dyes and found that both molecules had the same energy levels, band gap, and morphology.[92] However, the noncovalent alkenyl–phenyl interactions in Sqr. 2 resulted in a smaller stacking distance between the cores. This then translated into a higher mobility and higher J_{sc}. In a similar fashion, Bao and co-workers[93] reported that the siloxane-terminated solubilizing chains of diketopyrrolopyrrole-based molecule (PII2T-Si) for thin-film

Table 11. Photovoltaic parameters of end-functional-group modified P3HT. Adapted with permission.[91]

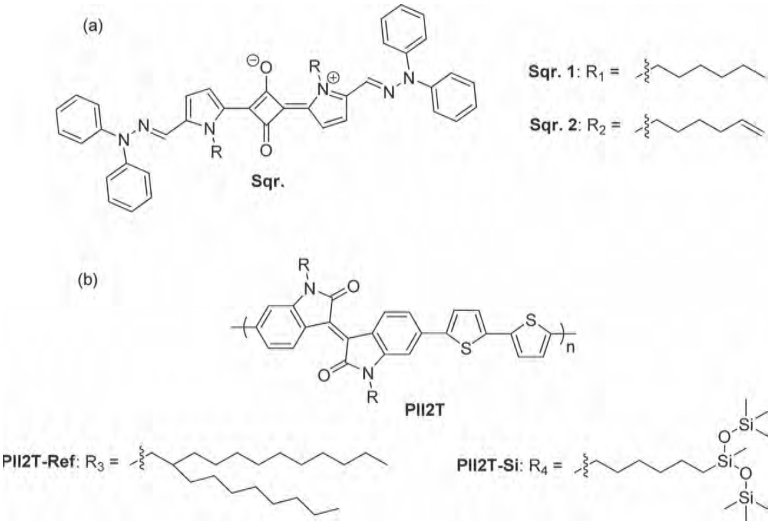


	V_{oc} [V]	J_{sc} [mA/cm^2]	*FF* [%]	η [%]	Surface energies [mJ /m^2]
P3HT-Br	0.59	9.89	0.55	3.2	39.2
P3HT-OH	0.58	7.65	0.46	2.1	40.3
P3HT-CH_3	0.60	10.69	0.61	4.0	35.1
P3HT-CF_3	0.60	10.89	0.69	4.5	34.3
PCBM	–	–	–	–	34.2

transistors decreased the π–π stacking between adjacent molecules and boosted the hole mobility. In light of these results, employing alkyenyl, siloxane, or end groups with similar effects are certainly synthetically feasible and could likely improve hole mobility.

4.4. Recommendation

Although deciding the appropriate side chains for specific polymers is an empirical process that will no doubt require the creation of libraries to discover the best combination, certain key guidelines have indeed emerged. The first is that the location of the side chains should be such that they cause the least amount of twisting along the backbone. The second is that in general, short and branched side chains seem to concurrently provide the optimal J_{sc} and V_{oc}. And finally, both aromatic and end-functionalized side chains have shown the potential



Scheme 4. Structures of (a) Sqr. and (b) PII2T derivatives.

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to enhance hole mobility through strengthening intermolecular polymer–polymer interactions. Thus, alkenyl-, siloxane-terminated, and alkylthienyl side chains should be further explored as well as many others. There are other important issues regarding side chains, which are beyond the scope of this discussion but nevertheless merit further consideration, including but not limited to side chain density[94] and fluorinated side chains for use as interfacial additive layers.[95]

5. Conclusions

Pushing the power conversion efficiency past 10% is certainly within the OPV community's reach, however doing so will require synergistic efforts from synthetic chemists to physicists to engineers to tackle current hurdles. The issues mentioned in this article are not meant to be an exhaustive laundry list, but rather a few key topics to inspire further studies. An emerging theme is the need for a better understanding of correlating structure–property relationships. Although much emphasis is often placed on lowering the HOMO level to increase V_{oc}, focusing on developing LUMO-reducing moieties would recover wasted energy during electron transfer to PCBM while enhancing V_{oc} and J_{sc} as well. Studies elucidating how PCBM interacts with the polymer are also especially vital. Various studies have implied that electron-poor PCBM should be kept near the electron-rich moiety of the polymer to enhance charge dissociation, whereas PCBM should be kept away from the electron-poor moiety to prevent charge recombination. These proposed models have yet to be proven or disproven; however, studies have demonstrated that both fluorine and side chain substituents can tune these interactions. If such structure–property relationships can be determined, this will greatly aid toward the movement of reaching 10% efficiency and beyond.

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Letter

Study on the edge isolation of industrial silicon solar cells with waterjet-guided laser

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Abstract

In this paper, we review the device physics to explain the necessity of edge isolation as well as the various common methods for performing this important step. In order to assess these processes, different aspects have to be taken into consideration and will be discussed. Finally, experimental results of edge isolation on commercial multicrystalline solar cells with waterjet-guided laser (wavelength 1064 nm) and conventional laser (wavelength 355 nm) are presented and discussed. From the experiments, we conclude that the waterjet-guided laser shows the potential to improve the laser scribing process in terms of pn junction damage and mechanical stability.
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Keywords: Edge isolation; Laser; Solar cells

1. Introduction

Unless the parasitic emitter diffusion wrapping around the wafer edge is removed, most industrial cells suffer from very low fill factors. This edge isolation process can be performed by different methods. Until a few years ago, plasma barrel etching was the standard process for edge isolation of solar cells. Since this batch process led to a strong disruption in the flow of the process due to stacking and unstacking of several hundreds of wafers, there was great interest in replacing this step by an appropriate inline process. One of the most successful new edge isolation processes is laser scribing. It is perfectly suitable for inline processing and the wafer needs not to be touched, which is an important requirement for the handling of thin wafers. In these systems, mostly solid-state lasers like Nd:YAG with short wavelengths (e.g., frequency tripled with $\lambda = 355\,\text{nm}$) are used. Even though the absorption of silicon in this wavelength range is very good and the pulses are quite short, the results are not always satisfying due to the recast of molten or evaporated silicon with respective mechanical stresses in the wafers or focusing problems with wafers of inhomogeneous thickness.

Therefore, alternatives to the conventional laser edge isolation have to be assessed if the commercial performance of the edge isolation step is to be further increased. An emerging new laser process that has the potential to overcome the problems of conventional lasers is the waterjet-guided laser [1,2] which has been studied experimentally in the present work.

An interesting option is the performance of edge isolation on the rear side of the cell because this prevents the damaging of the front side emitter where most of the photogeneration takes place. The difference between front and rear side edge isolation has been investigated experimentally as well as by DESSIS simulations.

1.1. Why do commercial solar cells need edge isolation?

Fig. 1 shows a sketch of a commercial screen-printed solar cell design. In the standard processing sequence, the entire wafer is phosphorous diffused. The contact to the p-type base is made by firing an Al containing paste that produces a local high doping of Al, thus overcompensating the shallow emitter diffusion. However, there is still a direct

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conductive path from the emitter on the front side to the rear p-contact. Therefore, a large portion of the photo-generated current can directly flow through the emitter to the back contact instead of flowing through the external circuit. This current path is modeled in the two-diode model of the solar cell as the parallel resistance R_p:

$$j(V) = j_{01}\left(\exp\frac{V - jR_s}{n_1 V_{th}} - 1\right) + j_{02}\left(\exp\frac{V - jR_s}{n_2 V_{th}} - 1\right) + \frac{V - jR_s}{R_p} - j_L.$$

In the this equation j_{01} and j_{02} represent the first and second diode saturation current densities; R_s and R_p are the series and parallel resistances, respectively; n_1 and n_2 denote the first and second diode ideality factors, respectively; $V_{th} = kT/q$ is the thermal voltage and j_L is the light-generated current density. In this model, the first diode accounts for emitter and bulk recombination with a recombination rate assumed to be proportional to the excess carrier density. This leads to an ideality factor of $n_1 = 1$. The second diode is associated with the recombination in the space–charge region that is assumed to be independent of the injection level, thus leading to $n_2 = 2$. The effect of increased j_{02} and R_p can be shown by model calculations for ideal solar cells in Fig. 2: for a fill factor potential above 84%, j_{02} must be less than 2×10^{-9} A/cm^2 and R_p must be greater than approximately 2000 Ω cm^2 if the respective parameters contribute solely to the fill factor loss. This increase in R_p is achieved by the edge isolation process that interrupts the parasitic current path as shown in Fig. 1.

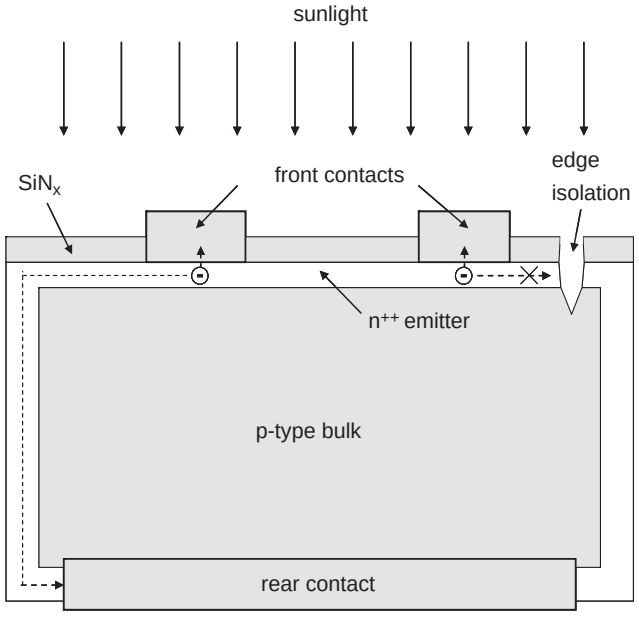


Fig. 1. Sketch of an industrial screen-printed solar cell. The emitter diffusion is present on the complete wafer surface and gets locally overcompensated by printing and firing an Al-containing metal paste as back contact. Without edge isolation, light-generated electrons can easily flow through the emitter region to the back contact which corresponds to a small series resistance in the two-diode model.

1.2. Common edge isolation methods

There are many different methods for performing edge isolation on silicon solar cells. These have been compared already by other authors [3–5]. The following processes are well known from the literature:

- plasma barrel etching [5],
- conventional laser grooving [5–7],
- dry etching [8],
- inline wet etching [3], and
- dispensing of etching pastes [9].

A general agreement exists that the interruption of the process flow associated with the plasma barrel etching is very disadvantageous. The laser and etching processes each have specific advantages and disadvantages. In this paper, laser and wet etching will not be compared in detail, despite the fact that both obtained an important market share, but it will be examined, whether the quality of the laser processing can be improved by guiding it in a thin waterjet.

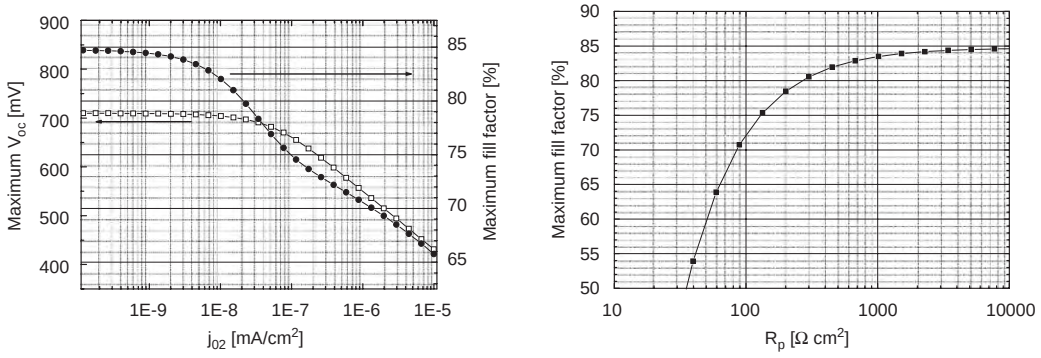


Fig. 2. Two-diode model calculations showing the fill factor and V_{oc} limitations imposed by j_{02} (left) and R_p (right). The respective assumptions were $n_1 = 1$, $n_2 = 2$, $j_L = 42$ mA/cm^2, $j_{01} = 5\,10^{-14}$ A/cm^2, $R_s = 0$ Ω cm^2, $R_p = 10^{10}$ Ω cm^2 (left) and $j_{02} = 10^{-18}$ A/cm^2 (right).

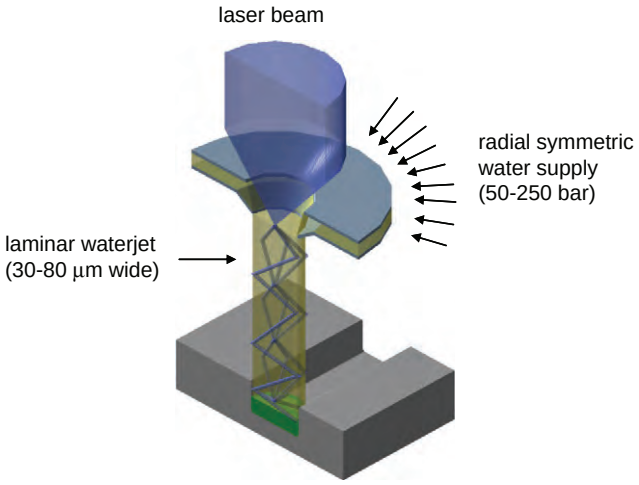


Fig. 3. Principle of the waterjet-guided laser. A hair-thin waterjet is generated in a flat nozzle with a glass window on top. A laser beam is focussed through this window into the waterjet thus allowing for guiding the laser beam just like in a liquid fiber.

1.3. Comparison of 'dry' and 'waterjet-guided' laser edge isolation

A sketch of the waterjet-guided laser is depicted in Fig. 3. A hair-thin waterjet (diameter down to 30 µm) is generated and the laser beam is focused into the jet through a transparent window on top of the water nozzle. The laser is guided via internal total reflection in the waterjet. This leads to a constant laser spot size independent of the distance between nozzle and wafer thus eliminating the need of refocusing if the wafer thickness changes. Additionally, the waterjet with its high flow velocity of up to 200 m/s can efficiently cool the groove after laser melting or evaporation and carry away the debris that generate unwanted recast in conventional laser processing. The waterjet-guided laser has already shown excellent performance in several microelectronic applications [10,11].

In order to assess whether the microstructuring quality of the waterjet-guided laser can also improve the edge isolation process for silicon solar cells, an experimental study with commercial solar cells was performed. Since the guidance of the laser in the waterjet increases the process complexity slightly compared to dry lasers, the edge isolation process must definitively be improved in terms of electrical and/or mechanical quality. If no other wet process follows the edge isolation, an additional drying step is necessary. However, there are also ideas how to reduce the effort for wafer drying considerably.

2. Experimental procedure

One hundred and twenty-five multicrystalline industrial solar cells of $156 \times 156\,mm^2$ size were purchased of which 95 were not yet edge isolated. Preliminary tests on 15 cells were performed to optimize the laser parameters for the waterjet-guided laser. The main focus was to achieve comparable groove depths with different parameters and to determine the minimum depth to ensure electrical isolation of the cells. The chosen laser parameter variations that have been used to isolate 70 solar cells (at 300 µm distance from the edge) are summarized in Table 1. Those yielded different cutting depths with different scanning speeds and pulse frequencies and have been applied to front and rear side. The pulse overlap was chosen to be close to or above 80% according to the results of Emanuel et al. [6]. It should be noted that due to technical problems, only straight lines have been grooved with the waterjet-guided laser, leaving the beveled corners without isolation. This would of course be possible with a commercial system with optimized laser and motion control.

As a first reference, a laser edge isolation process with a dry laser ($\lambda = 355\,nm$) with flying optics was applied to 10 cells while the distance of the groove to the edge was 250 µm. The exact parameters of the manufacturer's laser edge isolation, which were used as a second reference, are not known but the measured groove depth was about 10 µm, comparable to our UV dry laser process.

The dark and illuminated *IV* curves have been measured before and after edge isolation. Additionally, dark thermography maps with forward and reverse voltage [12] were recorded for cells with typical performance to detect ohmic and non-ohmic edge shunts. To exclude the influence of the series resistance losses, Suns-V_{oc} measurements [13] were performed for these cells as well. Finally, microscope observations (light microscope and SEM) as well as four line-breaking tests [14] have been performed which tests especially the mechanical quality of the wafer edges.

3. Results

3.1. IV curves measurements

In Table 2, the illuminated *IV* parameters are shown for the different processes. It can be seen that the waterjet-guided laser can reach results comparable to the dry lasers. This was accomplished with nearly industrial scanning speeds of 250 mm/s that could be further increased to about 500–600 mm/s by faster wafer stages. Only for the 5-µm-deep grooves (variants 3, 4, 7, 8), a low fill factor is observed. For the variants with fill factors above 70%, values of R_p between 2 and $7\,k\Omega\,cm^2$ could be fitted.

This is a very positive result since the waterjet-guided laser system used in the process suffered from the following three drawbacks compared to the dry lasers:

(1) An IR laser source was used that decreases the absorption coefficient in silicon by five orders of magnitude compared to the UV wavelength. Therefore the heat-affected zone is considerably larger.
(2) The beveled corners of the cells were not isolated due to technical problems.
(3) A 100-µm nozzle was used, generating a groove width of about 80 µm that corresponds to two to three times

Table 1
Parameter variation for edge isolation with waterjet-guided laser

Variant no.	Laser power (W)	Pulse repetition rate (kHz)	Scanning speed (mm/s)	Pulse overlap (%)	Structured surface	Laser groove depth (μm)
1	40.4	13	250	77	Front side	20
2	40.4	13	250	77	Rear side	20
3	22.8	13	250	77	Front side	5
4	22.8	13	250	77	Rear side	5
5	45.2	20	250	85	Front side	20
6	45.2	20	250	85	Rear side	20
7	23.9	20	250	85	Front side	5
8	23.9	20	250	85	Rear side	5
9	40.4	13	100	90	Front side	40
10	45.2	20	100	94	Front side	45

A fiber-coupled Spectron Nd:YAG laser system with pulse length in the order of several hundreds of ns was used for the study. The water pressure was set to 100 bar and a nozzle with 100-μm diameter was used. Since the laser power was measured after the fiber, the optical losses in the waterjet and the coupling unit are not taken into account.

Table 2
Effect on fill factor, j_{sc} and efficiency of industrial multicrystalline solar cells of $156 \times 156\,mm^2$ size after different edge isolation processes compared to the solar cells without edge isolation

Variant no.	Average fill factor, FF	Average fill factor improvement, ΔFF ($\%_{rel}$)	S.D. of ΔFF (%)	Average J_{sc} (mA/cm^2)	Average efficiency improvement ($\%_{rel}$)	No. of measured solar cells
1	0.751	+20.0	1.6	31.5	+22.0	7
2	0.747	+19.4	1.2	31.8	+23.3	7
3	0.688	+10.1	1.5	31.6	+11.4	7
4	0.678	+8.5	1.4	31.4	+9.8	7
5	0.760	+22.1	1.4	31.5	+24.0	7
6	0.744	+18.5	1.1	32.5	+21.8	7
7	0.672	+6.8	1.2	32.1	+7.2	7
8	0.652	+3.7	0.8	32.0	+4.4	7
9	0.751	+19.7	2.0	32.0	+22.1	7
10	0.748	+19.2	1.3	32.2	+21.3	7
Dry UV laser	0.750	+19.8	1.6	31.9	+22.3	10
Industry reference	0.755			31.8		30

FF, ΔFF, J_{sc} and efficiency are average values. Variants 1–10 are the waterjet-guided laser processes described in detail in Table 1.

the groove width of the dry lasers. The front side areas outside the laser grooves as well as the laser-scribed areas have much lower quantum efficiencies than the rest of the solar cell. This is due to the laser damage and leads to a reduction in j_{sc} and V_{oc}.[1]

This fact gives rise to an optimistic outlook for experiments with waterjet-guided UV lasers that allows round corner isolation grooves and uses, e.g., 40-μm nozzles.

Interestingly, the dark *IV* curves of all the cells isolated by the waterjet-guided laser showed a nearly perfect fit to the two-diode model with $n_1 = 1$ and $n_2 = 2$ while the cells isolated by the dry lasers could only be fitted with $n_2 = 2.8$ (average of 30 cells). This indicates that the removal of the molten silicon by the waterjet decreases the damage in the pn junction region.

3.2. Rear side edge isolation quality

It was also possible to perform rear side edge isolation for the studied cells. Schneiderlöchner reported in Ref. [15] the results for dry laser edge isolation experiments on solar cells from different manufacturers. Since the rear side isolation was equivalent to the front side isolation for only one material, he conjectured that edge defects, possibly from the brick cutting process, were not completely removed from the wafer edges for the material that did not allow rear side isolation.

To elucidate this problem, we performed 2D DESSIS simulations for a high-efficiency solar cell structure. In the

[1]To observe this small effect clearly experimentally, larger amounts of cells have to be tested.

first case, the emitter wraps around the edge but does not reach the back contact (this represents an ideal rear side isolation). In the second case, the emitter is interrupted on the front side by a 50-μm wide, passivated gap at 10 μm distance from the edge (this is nearly an ideal front side isolation). The simulated illuminated cell parameters are shown in Table 3. Obviously, no edge defects are necessary to reduce the fill factor for the rear side isolation. This is simply done by the edge emitter that has a much lower injection level than the front emitter and is connected in parallel to the front emitter. V_{oc} is decreased by 10 mV and the fill factor is reduced by 2.5%$_{abs}$ compared to the front side isolation due to the higher recombination in this 'dark' emitter. More details about this issue will be published elsewhere.

However, in the DESSIS simulation, a current gain of more than 4% is assumed for the rear side isolation. In large industrial cells, this will not be realized. When the laser groove can be restricted to the area at a maximum distance of 300 (150) μm from the 156-mm-long cell edge, the 'blinded' area fraction is only 0.8 (0.4)%. A current gain in this order of magnitude does not compensate for the fill factor and V_{oc} loss, so isolating from the front side seems to be the better process.

This is also true for our study: comparing the mean performance parameters of the cells with 20-μm deep grooves (variants 1, 2, 5, 6 in Table 1), the cells isolated from the front side show nearly identical V_{oc} (1.4 mV less), lower j_{sc} (0.7 mA/cm^2 less) and higher fill factors (1.2%$_{abs}$) than those isolated from the rear side. This leads to an increase in efficiency by 23.0%$_{rel}$ via front side edge isolation compared to 22.6%$_{rel}$ via rear side edge isolation.

Table 3
2D DESSIS simulation results for ideal front or rear side edge isolation for a high-efficiency solar cell structure

Edge isolation type	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
From front side	657	37.15	82.7	20.19
From rear side	647	38.80	80.2	20.24

3.3. Thermography maps

In Fig. 4, thermography maps at V_{oc} conditions are shown for the industrial reference, the waterjet-guided laser (variant 1 in Table 1) and the dry UV laser reference. It is to be noted that the edge areas between the busbars are obscured in the measurement setup so that no shunts are visible. Comparing the maps with the reverse bias measurements (not shown here) reveals that the right edge on the picture shows areas with ohmic shunting behavior for the dry laser processes while the other edges exhibit mostly diode-type behavior. The thermography maps of the cells isolated by the waterjet-guided laser show less recombination activity and a more homogeneous edge contrast compared to those from the cells scribed by the dry lasers. The homogeneous edge contrast indicates that the process fluctuations are less than for the other two laser scribing processes. Only the four unisolated corners are well visible in the map of the waterjet-guided laser. The shunts in the middle of two of the cells were introduced by problems with the contact probes in the *IV* measurements.

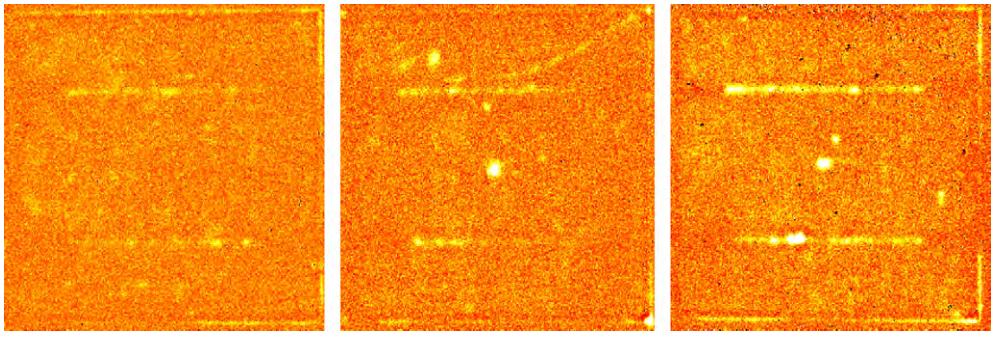


Fig. 4. Dark thermography maps at V_{oc} conditions of industrial solar cells of 156 × 156 mm^2 size. Left: reference industrial laser edge isolation, middle: edge isolation with waterjet-guided laser (variant 2, cf. Table 1), right: dry UV laser edge isolation.

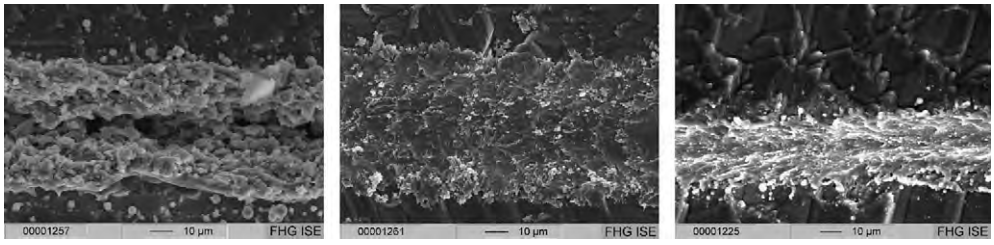


Fig. 5. SEM pictures of laser grooves from different laser processes. Left: reference industrial laser process, middle: waterjet-guided laser (variant 6, cf. Table 1), right: dry UV laser.

These do definitively influence the fill factor but since all measured cells had the same thickness, this mechanical damage must statistically be present on all cells independent of the edge isolation method. Therefore, we expect a decrease in the mean values of the fill factor and efficiency but not an influence of the trend of the mean values.

3.4. Suns-V_{oc} measurements

From Suns-V_{oc} measurements on one typical cell of the reference processes, as well as the variants 1 and 6 from Table 1, it was concluded that the absolute fill factor loss due to series resistances was about 5% for all cells. The pseudo fill factors were in the range between 81.3% and 82.0% indicating that no serious recombination problem in the space–charge region existed and there was also no pronounced shunting. Therefore, all laser methods generated satisfying isolation results from the electrical point of view.

3.5. Breakage tests and SEM investigation

Another important aspect for the edge isolation process is the mechanical stability of the cells. If significant cracks are introduced in this process step, the wafer has already undergone the complete solar cell process and a breakage in the next steps is the most costly scenario for the cell manufacturer. Additionally, cracks can significantly increase the risk of cell breakage in the module laminating process which can lead to complete module failure. Therefore, the assessment of the mechanical quality of the edge isolation is as important as the study of the electrical performance. In Refs. [16,17], the superior performance of waterjet-guided lasers by reducing the mechanical defects in laser grooving compared to dry lasers was shown.

Analyzing the SEM pictures in Fig. 5, it could be expected that the mechanical properties of the solar cells change with the different edge isolation methods. It was observed that the quality of the dry laser methods was very inhomogeneous over the complete wafer edge, most probably due to wafer thickness variations and associated focusing problems. Therefore, it was quite difficult to depict a representative area. On the other hand, the waterjet-guided laser shows a very homogeneous groove over the entire wafer edge. Less molten and resolidified silicon can be seen in comparison to the dry lasers. This shows that the molten silicon is carried away by the waterjet instead of being redeposited on the cell.

To evaluate quantitatively if the different appearances of the grooves leads to different mechanical stabilities, we performed four line-bending tests of all cells as described in Ref. [14]. The breakage force with its standard deviation has been recorded and summarized in Table 4. For statistical relevance, the number of broken solar cells is not sufficient, so only a first trend can be derived from the experiments. The dry UV laser shows a comparable breakage force to the industrial reference, while the measured values for the waterjet-guided laser scatter largely. This might be due to the small amount of samples available (seven for each variant compared to 30 samples of the industry reference). Thus, it is difficult to suppress the influence of varying mechanical bulk quality of the cells. But from our studies on wafers [16,17] and the fact that we measured significantly higher breakage forces on some cells, it seems possible to achieve consistently higher breakage forces with further optimization of the waterjet-guided laser edge isolation. To prove this hypothesis, a larger study with more samples and an optimized waterjet-guided laser system is necessary.

Table 4
Breakage forces and respective S.D. of solar cells with edge isolations by different methods

Edge isolation method	Range of breakage force (S.D.) (N)	No. of cells tested
Industrial laser reference	8.8 (4.4)	30
UV dry laser	8.4 (3.3)	10
Waterjet-guided laser	5.0–11.6 (3.6–5.2)	70 (7 for each variant)

4. Conclusion

In this paper, we have investigated the effect of guiding a laser beam in a waterjet on the performance of the edge isolation process for industrial multicrystalline silicon solar cells. The experimental study with over 100 solar cells has demonstrated successful edge isolation by waterjet-guided laser. Even with the drawbacks of an IR laser instead of UV, the lack of isolation of the cell's beveled corners and a two to three times larger laser groove, the performance of the reference processes could be obtained. In addition, better second ideality factors have been measured and the groove quality was much more homogeneous than for the dry laser processes.

It can be expected that the edge isolation could be improved further in terms of electrical and mechanical properties by using shorter wavelengths and smaller nozzles. This outlook makes the waterjet-guided laser an interesting option for solar cell microstructuring, not only for edge isolation purposes.

Acknowledgments

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Letter

Study on the edge isolation of industrial silicon solar cells with waterjet-guided laser

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Abstract

In this paper, we review the device physics to explain the necessity of edge isolation as well as the various common methods for performing this important step. In order to assess these processes, different aspects have to be taken into consideration and will be discussed. Finally, experimental results of edge isolation on commercial multicrystalline solar cells with waterjet-guided laser (wavelength 1064 nm) and conventional laser (wavelength 355 nm) are presented and discussed. From the experiments, we conclude that the waterjet-guided laser shows the potential to improve the laser scribing process in terms of pn junction damage and mechanical stability.
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Keywords: Edge isolation; Laser; Solar cells

1. Introduction

Unless the parasitic emitter diffusion wrapping around the wafer edge is removed, most industrial cells suffer from very low fill factors. This edge isolation process can be performed by different methods. Until a few years ago, plasma barrel etching was the standard process for edge isolation of solar cells. Since this batch process led to a strong disruption in the flow of the process due to stacking and unstacking of several hundreds of wafers, there was great interest in replacing this step by an appropriate inline process. One of the most successful new edge isolation processes is laser scribing. It is perfectly suitable for inline processing and the wafer needs not to be touched, which is an important requirement for the handling of thin wafers. In these systems, mostly solid-state lasers like Nd:YAG with short wavelengths (e.g., frequency tripled with $\lambda = 355$ nm) are used. Even though the absorption of silicon in this wavelength range is very good and the pulses are quite short, the results are not always satisfying due to the recast of molten or evaporated silicon with respective mechanical stresses in the wafers or focusing problems with wafers of inhomogeneous thickness.

Therefore, alternatives to the conventional laser edge isolation have to be assessed if the commercial performance of the edge isolation step is to be further increased. An emerging new laser process that has the potential to overcome the problems of conventional lasers is the waterjet-guided laser [1,2] which has been studied experimentally in the present work.

An interesting option is the performance of edge isolation on the rear side of the cell because this prevents the damaging of the front side emitter where most of the photogeneration takes place. The difference between front and rear side edge isolation has been investigated experimentally as well as by DESSIS simulations.

1.1. Why do commercial solar cells need edge isolation?

Fig. 1 shows a sketch of a commercial screen-printed solar cell design. In the standard processing sequence, the entire wafer is phosphorous diffused. The contact to the p-type base is made by firing an Al containing paste that produces a local high doping of Al, thus overcompensating the shallow emitter diffusion. However, there is still a direct

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conductive path from the emitter on the front side to the rear p-contact. Therefore, a large portion of the photo-generated current can directly flow through the emitter to the back contact instead of flowing through the external circuit. This current path is modeled in the two-diode model of the solar cell as the parallel resistance R_p:

$$j(V) = j_{01}\left(\exp\frac{V - jR_s}{n_1 V_{th}} - 1\right) + j_{02}\left(\exp\frac{V - jR_s}{n_2 V_{th}} - 1\right) + \frac{V - jR_s}{R_p} - j_L.$$

In the this equation j_{01} and j_{02} represent the first and second diode saturation current densities; R_s and R_p are the series and parallel resistances, respectively; n_1 and n_2 denote the first and second diode ideality factors, respectively; $V_{th} = kT/q$ is the thermal voltage and j_L is the light-generated current density. In this model, the first diode accounts for emitter and bulk recombination with a recombination rate assumed to be proportional to the excess carrier density. This leads to an ideality factor of $n_1 = 1$. The second diode is associated with the recombination in the space–charge region that is assumed to be independent of the injection level, thus leading to $n_2 = 2$. The effect of increased j_{02} and R_p can be shown by model calculations for ideal solar cells in Fig. 2: for a fill factor potential above 84%, j_{02} must be less than 2×10^{-9} A/cm^2 and R_p must be greater than approximately 2000 Ω cm^2 if the respective parameters contribute solely to the fill factor loss. This increase in R_p is achieved by the edge isolation process that interrupts the parasitic current path as shown in Fig. 1.

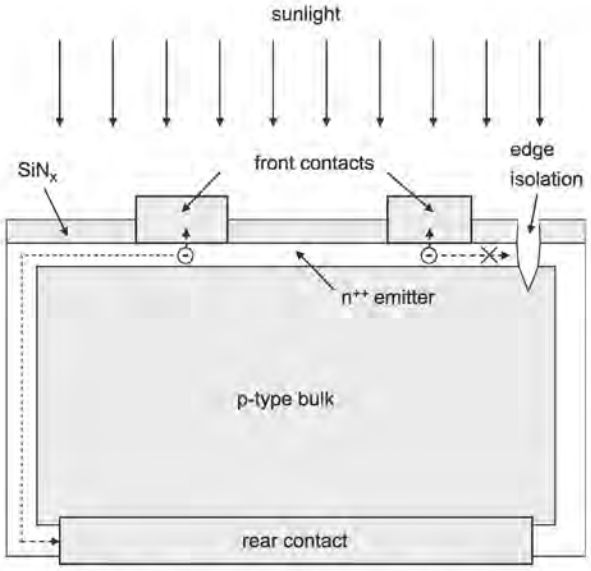


Fig. 1. Sketch of an industrial screen-printed solar cell. The emitter diffusion is present on the complete wafer surface and gets locally overcompensated by printing and firing an Al-containing metal paste as back contact. Without edge isolation, light-generated electrons can easily flow through the emitter region to the back contact which corresponds to a small series resistance in the two-diode model.

1.2. Common edge isolation methods

There are many different methods for performing edge isolation on silicon solar cells. These have been compared already by other authors [3–5]. The following processes are well known from the literature:

- plasma barrel etching [5],
- conventional laser grooving [5–7],
- dry etching [8],
- inline wet etching [3], and
- dispensing of etching pastes [9].

A general agreement exists that the interruption of the process flow associated with the plasma barrel etching is very disadvantageous. The laser and etching processes each have specific advantages and disadvantages. In this paper, laser and wet etching will not be compared in detail, despite the fact that both obtained an important market share, but it will be examined, whether the quality of the laser processing can be improved by guiding it in a thin waterjet.

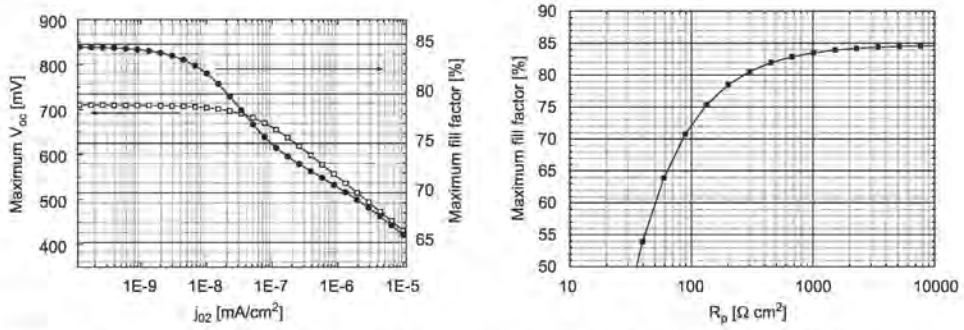


Fig. 2. Two-diode model calculations showing the fill factor and V_{oc} limitations imposed by j_{02} (left) and R_p (right). The respective assumptions were $n_1 = 1$, $n_2 = 2$, $j_L = 42$ mA/cm^2, $j_{01} = 5\,10^{-14}$ A/cm^2, $R_s = 0\,\Omega\,\text{cm}^2$, $R_p = 10^{10}\,\Omega\,\text{cm}^2$ (left) and $j_{02} = 10^{-18}$ A/cm^2 (right).

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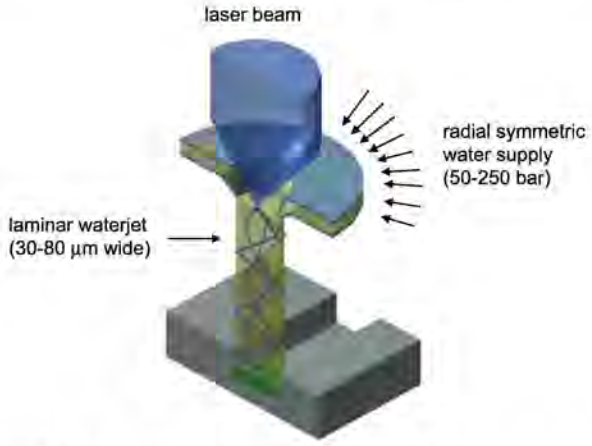


Fig. 3. Principle of the waterjet-guided laser. A hair-thin waterjet is generated in a flat nozzle with a glass window on top. A laser beam is focussed through this window into the waterjet thus allowing for guiding the laser beam just like in a liquid fiber.

1.3. Comparison of 'dry' and 'waterjet-guided' laser edge isolation

A sketch of the waterjet-guided laser is depicted in Fig. 3. A hair-thin waterjet (diameter down to 30 µm) is generated and the laser beam is focused into the jet through a transparent window on top of the water nozzle. The laser is guided via internal total reflection in the waterjet. This leads to a constant laser spot size independent of the distance between nozzle and wafer thus eliminating the need of refocusing if the wafer thickness changes. Additionally, the waterjet with its high flow velocity of up to 200 m/s can efficiently cool the groove after laser melting or evaporation and carry away the debris that generate unwanted recast in conventional laser processing. The waterjet-guided laser has already shown excellent performance in several microelectronic applications [10,11].

In order to assess whether the microstructuring quality of the waterjet-guided laser can also improve the edge isolation process for silicon solar cells, an experimental study with commercial solar cells was performed. Since the guidance of the laser in the waterjet increases the process complexity slightly compared to dry lasers, the edge isolation process must definitively be improved in terms of electrical and/or mechanical quality. If no other wet process follows the edge isolation, an additional drying step is necessary. However, there are also ideas how to reduce the effort for wafer drying considerably.

2. Experimental procedure

One hundred and twenty-five multicrystalline industrial solar cells of $156 \times 156\,mm^2$ size were purchased of which 95 were not yet edge isolated. Preliminary tests on 15 cells were performed to optimize the laser parameters for the waterjet-guided laser. The main focus was to achieve comparable groove depths with different parameters and to determine the minimum depth to ensure electrical isolation of the cells. The chosen laser parameter variations that have been used to isolate 70 solar cells (at 300 µm distance from the edge) are summarized in Table 1. Those yielded different cutting depths with different scanning speeds and pulse frequencies and have been applied to front and rear side. The pulse overlap was chosen to be close to or above 80% according to the results of Emanuel et al. [6]. It should be noted that due to technical problems, only straight lines have been grooved with the waterjet-guided laser, leaving the beveled corners without isolation. This would of course be possible with a commercial system with optimized laser and motion control.

As a first reference, a laser edge isolation process with a dry laser ($\lambda = 355\,nm$) with flying optics was applied to 10 cells while the distance of the groove to the edge was 250 µm. The exact parameters of the manufacturer's laser edge isolation, which were used as a second reference, are not known but the measured groove depth was about 10 µm, comparable to our UV dry laser process.

The dark and illuminated *IV* curves have been measured before and after edge isolation. Additionally, dark thermography maps with forward and reverse voltage [12] were recorded for cells with typical performance to detect ohmic and non-ohmic edge shunts. To exclude the influence of the series resistance losses, Suns-V_{oc} measurements [13] were performed for these cells as well. Finally, microscope observations (light microscope and SEM) as well as four line-breaking tests [14] have been performed which tests especially the mechanical quality of the wafer edges.

3. Results

3.1. IV curves measurements

In Table 2, the illuminated *IV* parameters are shown for the different processes. It can be seen that the waterjet-guided laser can reach results comparable to the dry lasers. This was accomplished with nearly industrial scanning speeds of 250 mm/s that could be further increased to about 500–600 mm/s by faster wafer stages. Only for the 5-µm-deep grooves (variants 3, 4, 7, 8), a low fill factor is observed. For the variants with fill factors above 70%, values of R_p between 2 and 7 $k\Omega\,cm^2$ could be fitted.

This is a very positive result since the waterjet-guided laser system used in the process suffered from the following three drawbacks compared to the dry lasers:

(1) An IR laser source was used that decreases the absorption coefficient in silicon by five orders of magnitude compared to the UV wavelength. Therefore the heat-affected zone is considerably larger.
(2) The beveled corners of the cells were not isolated due to technical problems.
(3) A 100-µm nozzle was used, generating a groove width of about 80 µm that corresponds to two to three times

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Table 1
Parameter variation for edge isolation with waterjet-guided laser

Variant no.	Laser power (W)	Pulse repetition rate (kHz)	Scanning speed (mm/s)	Pulse overlap (%)	Structured surface	Laser groove depth (μm)
1	40.4	13	250	77	Front side	20
2	40.4	13	250	77	Rear side	20
3	22.8	13	250	77	Front side	5
4	22.8	13	250	77	Rear side	5
5	45.2	20	250	85	Front side	20
6	45.2	20	250	85	Rear side	20
7	23.9	20	250	85	Front side	5
8	23.9	20	250	85	Rear side	5
9	40.4	13	100	90	Front side	40
10	45.2	20	100	94	Front side	45

A fiber-coupled Spectron Nd:YAG laser system with pulse length in the order of several hundreds of ns was used for the study. The water pressure was set to 100 bar and a nozzle with 100-μm diameter was used. Since the laser power was measured after the fiber, the optical losses in the waterjet and the coupling unit are not taken into account.

Table 2
Effect on fill factor, j_{sc} and efficiency of industrial multicrystalline solar cells of $156 \times 156\,mm^2$ size after different edge isolation processes compared to the solar cells without edge isolation

Variant no.	Average fill factor, FF	Average fill factor improvement, ΔFF ($\%_{rel}$)	S.D. of ΔFF (%)	Average J_{sc} (mA/cm^2)	Average efficiency improvement ($\%_{rel}$)	No. of measured solar cells
1	0.751	+20.0	1.6	31.5	+22.0	7
2	0.747	+19.4	1.2	31.8	+23.3	7
3	0.688	+10.1	1.5	31.6	+11.4	7
4	0.678	+8.5	1.4	31.4	+9.8	7
5	0.760	+22.1	1.4	31.5	+24.0	7
6	0.744	+18.5	1.1	32.5	+21.8	7
7	0.672	+6.8	1.2	32.1	+7.2	7
8	0.652	+3.7	0.8	32.0	+4.4	7
9	0.751	+19.7	2.0	32.0	+22.1	7
10	0.748	+19.2	1.3	32.2	+21.3	7
Dry UV laser	0.750	+19.8	1.6	31.9	+22.3	10
Industry reference	0.755			31.8		30

FF, ΔFF, J_{sc} and efficiency are average values. Variants 1–10 are the waterjet-guided laser processes described in detail in Table 1.

the groove width of the dry lasers. The front side areas outside the laser grooves as well as the laser-scribed areas have much lower quantum efficiencies than the rest of the solar cell. This is due to the laser damage and leads to a reduction in j_{sc} and V_{oc}.[1]

This fact gives rise to an optimistic outlook for experiments with waterjet-guided UV lasers that allows round corner isolation grooves and uses, e.g., 40-μm nozzles.

Interestingly, the dark *IV* curves of all the cells isolated by the waterjet-guided laser showed a nearly perfect fit to the two-diode model with $n_1 = 1$ and $n_2 = 2$ while the cells isolated by the dry lasers could only be fitted with $n_2 = 2.8$ (average of 30 cells). This indicates that the removal of the molten silicon by the waterjet decreases the damage in the pn junction region.

3.2. Rear side edge isolation quality

It was also possible to perform rear side edge isolation for the studied cells. Schneiderlöchner reported in Ref. [15] the results for dry laser edge isolation experiments on solar cells from different manufacturers. Since the rear side isolation was equivalent to the front side isolation for only one material, he conjectured that edge defects, possibly from the brick cutting process, were not completely removed from the wafer edges for the material that did not allow rear side isolation.

To elucidate this problem, we performed 2D DESSIS simulations for a high-efficiency solar cell structure. In the

[1]To observe this small effect clearly experimentally, larger amounts of cells have to be tested.

first case, the emitter wraps around the edge but does not reach the back contact (this represents an ideal rear side isolation). In the second case, the emitter is interrupted on the front side by a 50-μm wide, passivated gap at 10 μm distance from the edge (this is nearly an ideal front side isolation). The simulated illuminated cell parameters are shown in Table 3. Obviously, no edge defects are necessary to reduce the fill factor for the rear side isolation. This is simply done by the edge emitter that has a much lower injection level than the front emitter and is connected in parallel to the front emitter. V_{oc} is decreased by 10 mV and the fill factor is reduced by $2.5\%_{abs}$ compared to the front side isolation due to the higher recombination in this 'dark' emitter. More details about this issue will be published elsewhere.

However, in the DESSIS simulation, a current gain of more than 4% is assumed for the rear side isolation. In large industrial cells, this will not be realized. When the laser groove can be restricted to the area at a maximum distance of 300 (150) μm from the 156-mm-long cell edge, the 'blinded' area fraction is only 0.8 (0.4)%. A current gain in this order of magnitude does not compensate for the fill factor and V_{oc} loss, so isolating from the front side seems to be the better process.

This is also true for our study: comparing the mean performance parameters of the cells with 20-μm deep grooves (variants 1, 2, 5, 6 in Table 1), the cells isolated from the front side show nearly identical V_{oc} (1.4 mV less), lower j_{sc} (0.7 mA/cm^2 less) and higher fill factors ($1.2\%_{abs}$) than those isolated from the rear side. This leads to an increase in efficiency by $23.0\%_{rel}$ via front side edge isolation compared to $22.6\%_{rel}$ via rear side edge isolation.

Table 3
2D DESSIS simulation results for ideal front or rear side edge isolation for a high-efficiency solar cell structure

Edge isolation type	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	η (%)
From front side	657	37.15	82.7	20.19
From rear side	647	38.80	80.2	20.24

3.3. Thermography maps

In Fig. 4, thermography maps at V_{oc} conditions are shown for the industrial reference, the waterjet-guided laser (variant 1 in Table 1) and the dry UV laser reference. It is to be noted that the edge areas between the busbars are obscured in the measurement setup so that no shunts are visible. Comparing the maps with the reverse bias measurements (not shown here) reveals that the right edge on the picture shows areas with ohmic shunting behavior for the dry laser processes while the other edges exhibit mostly diode-type behavior. The thermography maps of the cells isolated by the waterjet-guided laser show less recombination activity and a more homogeneous edge contrast compared to those from the cells scribed by the dry lasers. The homogeneous edge contrast indicates that the process fluctuations are less than for the other two laser scribing processes. Only the four unisolated corners are well visible in the map of the waterjet-guided laser. The shunts in the middle of two of the cells were introduced by problems with the contact probes in the *IV* measurements.

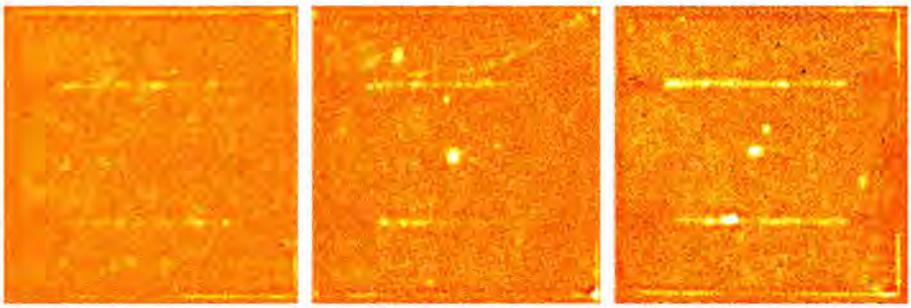


Fig. 4. Dark thermography maps at V_{oc} conditions of industrial solar cells of 156 × 156 mm^2 size. Left: reference industrial laser edge isolation, middle: edge isolation with waterjet-guided laser (variant 2, cf. Table 1), right: dry UV laser edge isolation.

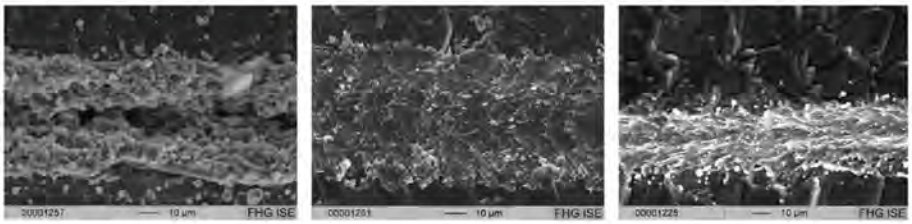


Fig. 5. SEM pictures of laser grooves from different laser processes. Left: reference industrial laser process, middle: waterjet-guided laser (variant 6, cf. Table 1), right: dry UV laser.

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These do definitively influence the fill factor but since all measured cells had the same thickness, this mechanical damage must statistically be present on all cells independent of the edge isolation method. Therefore, we expect a decrease in the mean values of the fill factor and efficiency but not an influence of the trend of the mean values.

3.4. Suns-V_{oc} measurements

From Suns-V_{oc} measurements on one typical cell of the reference processes, as well as the variants 1 and 6 from Table 1, it was concluded that the absolute fill factor loss due to series resistances was about 5% for all cells. The pseudo fill factors were in the range between 81.3% and 82.0% indicating that no serious recombination problem in the space–charge region existed and there was also no pronounced shunting. Therefore, all laser methods generated satisfying isolation results from the electrical point of view.

3.5. Breakage tests and SEM investigation

Another important aspect for the edge isolation process is the mechanical stability of the cells. If significant cracks are introduced in this process step, the wafer has already undergone the complete solar cell process and a breakage in the next steps is the most costly scenario for the cell manufacturer. Additionally, cracks can significantly increase the risk of cell breakage in the module laminating process which can lead to complete module failure. Therefore, the assessment of the mechanical quality of the edge isolation is as important as the study of the electrical performance. In Refs. [16,17], the superior performance of waterjet-guided lasers by reducing the mechanical defects in laser grooving compared to dry lasers was shown.

Analyzing the SEM pictures in Fig. 5, it could be expected that the mechanical properties of the solar cells change with the different edge isolation methods. It was observed that the quality of the dry laser methods was very inhomogeneous over the complete wafer edge, most probably due to wafer thickness variations and associated focusing problems. Therefore, it was quite difficult to depict a representative area. On the other hand, the waterjet-guided laser shows a very homogeneous groove over the entire wafer edge. Less molten and resolidified silicon can be seen in comparison to the dry lasers. This shows that the molten silicon is carried away by the waterjet instead of being redeposited on the cell.

To evaluate quantitatively if the different appearances of the grooves leads to different mechanical stabilities, we performed four line-bending tests of all cells as described in Ref. [14]. The breakage force with its standard deviation has been recorded and summarized in Table 4. For statistical relevance, the number of broken solar cells is not sufficient, so only a first trend can be derived from the experiments. The dry UV laser shows a comparable breakage force to the industrial reference, while the measured values for the waterjet-guided laser scatter largely. This might be due to the small amount of samples available (seven for each variant compared to 30 samples of the industry reference). Thus, it is difficult to suppress the influence of varying mechanical bulk quality of the cells. But from our studies on wafers [16,17] and the fact that we measured significantly higher breakage forces on some cells, it seems possible to achieve consistently higher breakage forces with further optimization of the waterjet-guided laser edge isolation. To prove this hypothesis, a larger study with more samples and an optimized waterjet-guided laser system is necessary.

Table 4
Breakage forces and respective S.D. of solar cells with edge isolations by different methods

Edge isolation method	Range of breakage force (S.D.) (N)	No. of cells tested
Industrial laser reference	8.8 (4.4)	30
UV dry laser	8.4 (3.3)	10
Waterjet-guided laser	5.0–11.6 (3.6–5.2)	70 (7 for each variant)

4. Conclusion

In this paper, we have investigated the effect of guiding a laser beam in a waterjet on the performance of the edge isolation process for industrial multicrystalline silicon solar cells. The experimental study with over 100 solar cells has demonstrated successful edge isolation by waterjet-guided laser. Even with the drawbacks of an IR laser instead of UV, the lack of isolation of the cell's beveled corners and a two to three times larger laser groove, the performance of the reference processes could be obtained. In addition, better second ideality factors have been measured and the groove quality was much more homogeneous than for the dry laser processes.

It can be expected that the edge isolation could be improved further in terms of electrical and mechanical properties by using shorter wavelengths and smaller nozzles. This outlook makes the waterjet-guided laser an interesting option for solar cell microstructuring, not only for edge isolation purposes.

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Attachment H-3

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Multi-objective optimization of laser scribing for the isolation process of solar cell wafers using grey relational analysis

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Abstract- **A novel method is presented for optimizing laser scribing of solar cell wafers for the isolation process. Multiple performance characteristics are optimized using grey relational analysis (GRA). Laser scribing technology is a useful solution for solar cell isolation processes. Solar energy is available worldwide and useful to everybody. Most solar cell technology is currently based on silicon wafer technology. Two important targets for this solar cell industry are high effective rates of energy transfer and low manufacturing costs. The isolation process for solar cell silicon wafer processing using laser scribing technology needs a high quality process to obtain a good surface profie. This study uses a Q-switched diode-pumped solid-state laser (DPSSL) to perform the scribing. Results are characterized using three parameters, including two laser operation parameters (laser average power and Q-switching frequency), and one laser scanning parameter (laser scribing speed for manufacturing throughput). These parameters are optimized based on multiple performance characteristics. Some characteristics of the scribing isolation process using laser technology for solar cell wafers are verified. The characteristics of interest are the minimum width of the average scribing groove for edge isolation on wafer substrates and the maximum depth of the average groove. Nine experiments were conducted using GRA to optimize the values for laser scribing parameters in order to generate various quality characteristics. Analysis of the grey relational grade indicates parameter significance and the optimal parameter combination for the laser scribing process is identified. The measured analytical results using the optimal parameters confirm that laser scribing technology can be effectively applied to isolate the edge of solar cell wafers.**

Keywords: Laser scribing, solar cell wafer, grey relational analysis, diode-pumped solid-state laser

I. INTRODUCTION

The most important objective for the photo voltaic (PV) market is to reduce the ratio of manufacturing cost to power output, thus becoming a more competitive energy source. Solar cell silicon wafer technology remains the dominant technology for most PV production. Solar cell wafers have become more and more popular for use in many new or remodeled buildings and have been developed for new green power generator stations. The laser technology applied to PV applications has a good chance to simplify the process and integrate nicely into in-line tools with a small footprint. A large number of new applications include edge isolation, ID marking, defect and shunt repairing and back-contact deposition. Lasers will continue to find and be developed for new applications in the fast growing PV industry.

In the standard processing sequence, the entire wafer is phosphorous diffused resulting in a direct conductive path from the emitter on the front side to the rear p-contact. A large portion of the photo-generated current can directly flow through the emitter to the back contact instead of flowing through the external circuit. So, a process isolating the front and rear surfaces of the wafer is very important for the solar cell wafer to achieve high efficiency. Kray *et al.* [1] demonstrated one of the most successful new edge isolation processes using laser scribing. It is perfectly suited for inline processing and the wafer need not be mechanically contacted, which is an important requirement for the handling of thin wafers. Buzas and Geretovszky [2] presented that while the efficiency of a cell depends solely on the quality of its layers, the module efficiency of an entire solar panel depends strongly on the quality of cell interconnections, as well. Laser micromachining is believed to be a good compromise between these two extremes offering a potential in making high quality scribes at an affordable price under optimized conditions.

Booth [3] described the high speed laser scribing of polycrystalline silicon wafers for use in solar cells which has recently become a proven industrial manufacturing process. In semiconductor scribing, quality is assessed by comparing legibility characteristics such as width, depth, and micro-cracks. Molpeceres *et al.* [4] presented that material ablation with minimum debris and a small heat affected zone is difficult to achieve, but it reduces costs and improves device efficiency. Dobrzanski *et al.* [5] depicted that there are many factors influencing the interaction between the laser beam and the treated surface. On one hand, it depends on the material

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properties, such as absorption coefficient, thermal diffusivity, thermal expansion coefficient, and melting and evaporation points. On the other hand, laser parameters, such as power, wavelength, pulse duration, repetition frequency, and beam translation, influence the results of laser treatment. Raciukaitis *et al.* [6] demonstrated that the use of laser fluencies close to the ablation threshold makes it possible to minimize recast ridge formation and surface contamination during the process. Yamamoto *et al.* [7] presented that the crack depth in laser scribing depends on the surface tensile stress in the cooling area and the compressive stress field immediately under that area. But controlling crack progress by thermal stress is difficult, since it is influenced by substrate size or a cut position such as a center of a substrate and an end.

When the laser fluence is only slightly higher than the ablation threshold, an engraved path can be scribed with line-width similar to the beam size derived from laser focus theory. These results meet the requirement of precise micromachining with a desired stability and reproducibility as described by Venkatakrishnan *et al.* [8]. The scribing depth needs to be smooth in order to remove silicon material to a suitable depth with only light cracking damage for the wafer and the edges to be free of molted material without serious hillocks.

Fig.1 (A) depicts the isolation of the solar cell wafer, and Fig.1 (B) shows the 3D surface profile for a scribing groove after the laser isolation process. This laser scribing process is required to obtain the performance characteristics as Fig.1 (C) describes, including minimal average width of groove path and maximal average depth of groove. The study uses an effective analysis tool, called grey relational analysis (GRA), which is utilized to optimize laser scribing parameters with multiple performance characteristics using finite experiment results and to optimize the factor level condition.

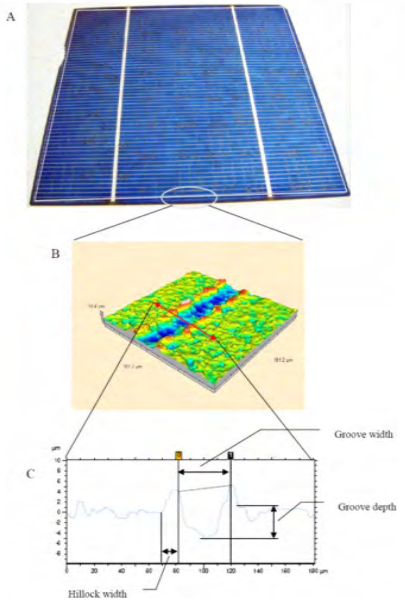


Fig.1 Laser scribing isolation on solar cell wafer. (A) Top view of a solar cell wafer; (B) side view; (C) schematic representation of multi-performance response.

Grey relational theory can solve both unclear problems and those involving incomplete data, can compensate for the shortcomings of statistical regression, and can effectively analyze relationships between sequences in situations involving limited data. Grey relational theory is highly appropriate for numerous pragmatic problems that occur in industrial strategic decision making. This work presents a novel laser scribing technology for solar cell isolation processes based on silicon substrate wafers. GRA can assess the grey relation grade for each control factor and determine the relative contribution of various parameters, even in situations in which probability cannot be defined or available data are limited.

GRA was first proposed by Deng [9] in 1982 to deal with poor, incomplete, and uncertain systems. As implied by its name, GRA can effectively recommend a method that optimizes complex inter-relationships, and has been applied broadly to assess the performance of complex projects involving situations where available information is limited as presented by Pan *et al.* [10]. The GRA method can process numerous attributes with different value types, physical measurement units, and score attributes, including attributes with limited accuracy and reliability. Notably, GRA can be applied to multi-parameter evaluation problems with multiple objectives.

II. Laser Scribing System

Fig. 2 illustrates the configuration of a Q-switched diode-pumped solid-state laser (DPSSL) scribing system for the solar cell isolation process, which includes a laser source with a Q-switch, a beam expander, a beam delivery optical scanning module, a focusing scan lens, an edge path vision process, a height adjusting handler, and a CNC controller for laser controlling and a motion system. The main benefits of the technique are to create a scribing groove with the smallest width, smoothest curve, and most sufficient isolation depth. This scribing process with vaporization and chemical degradation can generate a smooth groove quality with a good surface. Experimental results for nine groups of samples following laser scribing were assessed in terms of performance (Fig. 1 (C)), including first,, the minimum average width of the grooves of the wafer edge, which were typically larger than the 1064 nm laser spot size (20 ~ 40 μm) , and second, the maximum depth of the groove with the 1064 nm DPSSL at less than 10 watts, which was typically less than the expected (10~ 30 μm), due to the use of an economical laser system for cost consideration. The characteristics of the laser scribing surface were measured using a white light interference microscope.

Although there are many parameters that relate to the laser source, beam shaping, focusing module, and machine handler, in this paper, many of these parameters were fixed, including, the focusing length of the scan lens for a 6" wafer size, the Z

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height for suitable laser reaction on the wafer surface, and the beam spot size. Giacomo and Pascale [11] presented that the focus of laser should be placed a few millimeters distance away from the target so that an air spark is generated close to the target. In this way, it is not necessary to expose the target surface to a high energy laser pulse to get a laser induced plasma (LIP). Rozman *et al.* [12] demonstrated the formation of a laser-induced plasma plume appropriate for characterization and optimization of laser material processing, which is of great theoretical and practical importance. This study fixed the focus position to obtain a suitable reaction on the surface after testing several different distances.

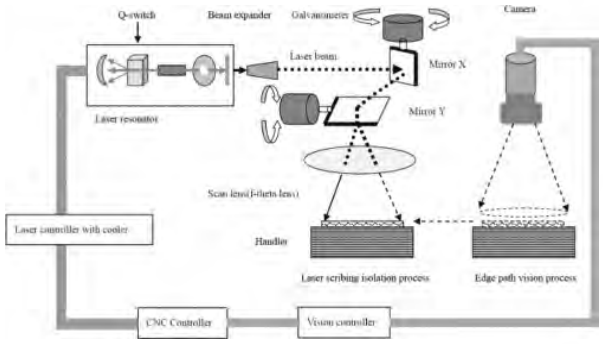


Fig. 2 Configuration of the laser scribing system for solar cell wafers.

Shanjin and Yang [13], Li *et al.* [14], Li *et al.* [15], and Caydas and Hascalik [16] presented that the average laser power has a marked influence on laser application. Dobrzanski [17] demonstrated that the higher the order of transverse mode, the lower the depth of the groove. Therefore, from a practical point of view, it is important to keep a balance between the order of the transverse mode and the corresponding effective power of the laser beam. Compaan [18] noted high-speed scribing is a major goal. Clearly this is a function of the laser power, but also of the energy efficiency of vaporization. The vaporization depth as a function of pulse energy is used to identify the energy density needed to optimize the scribing rate. Shanjin and Yang [13], Li *et al.* [14], and Dubey and Yadava [19] demonstrated Q-switching frequency has an influence on the laser application.

Table 1 summarizes the experimental conditions and level settings. There are three main parameters discussed in this process for good optimization of laser scribing, including laser average power P_{av} as shown in Eq. (1), laser scribing speed, and Q-switching frequency which is related to the quality factor Q as described by Kuhn [20] in Eq. (2),

$$P_{av} = Jf_p \tag{1}$$

where J is average pulse energy (Joules) and f_p is the pulse repetition rate (Hz).

$$Q = \frac{\upsilon_0}{\Delta\upsilon} \tag{2}$$

where υ_0 is the resonant frequency (Hz) of the cavity, $\Delta\upsilon$ is the frequency linewidth at full-width half-maximum.

Symbol A is the laser average power, and is adjusted to a certain value for the different setting levels after the Q-switching frequency is set. This study assigned the value of 85% to level 1, 93% to level 2, and 100% to level 3, at a maximum of 10 watts.

Symbol B is the laser scribing speed which the manufacturing process requires to be over 400 mm/s. So this study assigned the value of 400 mm/s to level 1, 600 mm/s to level 2, and 800 mm/s to level 3.

Symbol C is the Q-switching frequency. This study assigned the value of 15 kHz to level 1, 30 kHz to level 2, and 45 kHz to level 3.

The degree of overlap of individual laser pulses can be calculated from equation (3) as Kaldos et al. [21] presented, the overlap rate for laser beams on the scribing path by considering the Q-switching frequency.

$$U_d = [1 - \frac{V_S}{f_p D}] \times 100\% \tag{3}$$

Where U_d is the degree of overlap (%), V_s is the speed (mms^{-1}), f_p is the repetition rate (kHz), and D is the laser spot diameter (μm).

This study examines three input parameters to obtain multiple quality characteristics. These parameters are considered in laser scribing for isolation of solar cell wafer, involved vaporization and chemical degradation mechanisms during micro-machining. This paper conducted nine scribing experiment to assess the significance of these factors using GRA of multiple quality characteristics, and determine the optimal parameter settings, including the width, and depth of grooves.

Table 1
Laser scribing factors and their levels.

Symbol	Scribing factor	Level 1	Level 2	Level 3
A	Laser average power rate (% of 10W)	85	93	100
B	Laser scribing speed (mm/s)	400	600	800
C	Q-switching frequency (kHz)	15	30	45

III. GREY RELATIONAL ANALYSIS

It is obvious that GRA utilizes mathematical methods when analyzing correlations between series comprising a grey relational system, and thereby determines the difference in contribution between a reference series and each compared series. The compared series are alternative vectors created from sets based on attribute characteristics, which are the larger-the-better and the smaller-the-better, or optimization of specific

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values between the maximum and minimum values of an attribute. Applying a GRA algorithm can rank different alternatives by determining their grey relational grades. The grey relational grades of different series can be used to rank various alternatives, where higher values indicate superior alternatives as Lu and Wevers [22] described.

A. Data pre-processing

Data pre-processing is the first step in the procedure for using GRA. Data pre-processing involves transforming an original sequence into a comparable sequence. Experimental results are thus normalized in a range of 0–1. Eq. (4) shows the calculations for the larger-the-better case, Eq. (5) shows those for the smaller-the-better case, and Eq. (6) shows those for the case in which a definite target value must be achieved as You *et al.* [23] depicted,

$$x_i^*(k)=\frac{x_i^{(0)}(k)-\min_{all(i)} x_i^{(0)}(k)}{\max_{all(i)} x_i^{(0)}(k)-\min_{all(i)} x_i^{(0)}(k)} \tag{4}$$

$$x_i^*(k)=\frac{\max_{all(i)} x_i^{(0)}(k)-x_i^{(0)}(k)}{\max_{all(i)} x_i^{(0)}(k)-\min_{all(i)} x_i^{(0)}(k)} \tag{5}$$

$$x_i^*(k)=1-\frac{\left|x_i^{(0)}(k)-OB\right|}{\max_{all(i)}\{O_1,O_2\}} \tag{6}$$

where $x_i^*(k)$ is the i th grey datum following grey generation for experiment k, $x_i^{(0)}(k)$ is the original i th quality datum of experiment k, $\max_{all(i)} x_i^{(0)}(k)$ is the maximum value in original sequence, $\min_{all(i)} x_i^{(0)}(k)$ is the minimum value in the original sequence, OB is the target value, $O_1=\max_{all(i)} x_i^{(0)}(k)-OB$, and $O_2=OB-\min_{all(i)} x_i^{(0)}(k)$.

In this investigation, the smaller-the-better case is selected for the quality characteristic of groove width, and the larger-the-better case is selected for the quality characteristic of groove depth. This study conducted nine experiments in which solar cell wafers were scribed using different parameters. Table 1 lists the control factors and their levels, Table 2 describes the parameter combination of the nine experiments and the values of multiple quality characteristics. Figure 1 (C) shows the multiple performance characteristics for laser scribing solar cell wafers. Pre-processing results were obtained using Eq. (4-5) for the trends of both quality characteristics to normalize sequences of each performance characteristic and derive quantitative indices for subsequent analysis.

B. Grey relational coefficient and grey relational grade

Following data pre-processing, a grey relational coefficient is calculated to express the relationship between an ideal and an actual normalized experimental result. Initially, the deviation sequence of the reference sequence is calculated using Eq. (7). The grey relational coefficients were obtained to integrate the values obtained from Eq. (8) and Eq. (9) into Eq. (10),

$$\Delta_{oi}(k)=\left\|x_0^*(k)-x_i^*(k)\right\| \tag{7}$$

$$\Delta_{\max}=\max_{\forall j\in i}\max_{\forall k}\left\|x_0^*(k)-x_j^*(k)\right\| \tag{8}$$

$$\Delta_{\min}=\min_{\forall j\in i}\min_{\forall k}\left\|x_0^*(k)-x_j^*(k)\right\| \tag{9}$$

$$\xi_i(k)=\frac{\Delta_{\min}+\xi\cdot\Delta_{\max}}{\Delta_{0i}(k)+\xi\cdot\Delta_{\max}} \tag{10}$$

where $\Delta_{0i}(k)$ is the deviation sequence of the reference sequence $x_0^*(k)$, $x_i^*(k)$ is the comparability sequence, and ξ is the distinguishing or identification coefficient ($\xi\in[0,1]$).

The calculated grey coefficient is employed by choosing $\xi=0.5$, which is generally adopted in most studies. Following acquisition of the grey relational coefficient, Eq. (11) is used to derive the grey relational grade γ_i by taking the average of the grey relational coefficients and applying the same weight to both qualities under investigation. Additionally, the grey relational ordinal was obtained,,

$$\gamma_i=\frac{1}{n}\sum_{k=1}^{n}\xi_i(k) \tag{11}$$

where γ_i is the i th grey relational grade of each experiment obtained by taking the average of the grey relational coefficients and n is the quality number.

The grey relational grade, as depicted in Table 3, shows the important relationships among the sequences and indicates their degree of influence.

Table 2
Experimental results of control factors and multiple performance data.

Experiment no.	A	B	C	Groove width (μ m)	Groove depth (μ m)
Reference value				20	10
1	1	1	1	57.12	7.92
2	1	2	2	49.79	9.47
3	1	3	3	40.49	6.75
4	2	1	2	42.67	9.19
5	2	2	3	40.05	4.85
6	2	3	1	53.94	2.44
7	3	1	3	50.46	5.12
8	3	2	1	42.65	5.14
9	3	3	2	49.59	4.52

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Table 3
Calculated grey relational coefficients and grey relational grades.

Experiment no.	Grey relational coefficient		Grey relational grade	Orders
	Groove width (μ m)	Groove depth (μ m)		
1	0.3801	0.7355	0.5578	4
2	0.4377	1.0000	0.7189	2
3	0.5419	0.6131	0.5775	3
4	0.5133	0.9391	0.7262	1
5	0.5481	0.4826	0.5154	5
6	0.4031	0.3801	0.3916	9
7	0.4317	0.4977	0.4647	7
8	0.5135	0.4988	0.5062	6
9	0.4395	0.4654	0.4525	8

* Identification coefficient $\zeta = 0.5$
* Weight ratio $\beta_1 = 0.5$, $\beta_2 = 0.5$

IV. Experimental Results and Discussion

This study focusses on multiple characteristics of surface quality after the isolation process. The width, and depth of the grooves were measured using 3D profiling.

To determine the performance of the proposed laser scribing technology applied to the isolation process of solar cell wafers, GRA is applied to determine the optimal factor level conditions. Table 2 lists the performance characteristics of the average scribing width of grooves and the average scribing depth of grooves with different laser scribing parameters. Both the smaller-the-better case for the groove width and the larger-the-better case for the groove depth are desirable in terms of quality characteristics. In total, nine experiments were conducted to identify the three important input control parameters and to normalize the data of the two quality characteristics. Notably, GRA mathematical conversion enables limited experiments to obtain comparable coefficients and grades. The grey relational grade can be used to determine the optimal combination of control factors and to determine the effective contribution of each experimental factor.

According to the GRA results (Table 3), the laser scribing parameter setting from the fourth experiment has the highest grey relational grade. In terms of grey relational grades, the fourth experiment was followed by the second experiment, third experiment, first experiment, fifth experiment, eighth experiment, seventh experiment, ninth experiment, and finally the sixth experiment. Table 3 indicates that the best multiple performance characteristics were obtained with the combination of A2B1C2 for the nine experiments presented in Table 2.

The grey relational grade for each factor level was derived from the factor levels (Table 2), which are related to the grey relational grades (Table 3). The grey relational grade of each factor level is calculated as the average for the same level in each column; the grey relational grades are shown in intersecting rows.

Table 4 lists the average grey relational grade for each factor level and its grey relational grade. Since grey relational grades represent the correlation between the reference and comparable sequences, a large grey relational grade means the comparability sequence is closely correlated with the reference sequence. This investigation selects the level that provides the largest average response. Furthermore, these laser parameters with their levels A1, B1, and C2 list the highest grey relational grade for factors A, B, and C, respectively. Thus, A1B1C2 comprises the optimal parameter combination for the laser scribing process. This optimal parameter combination is a laser average power of 85% of 10 W, a laser scribing speed of 400 mm/s, and a Q-switching frequency of 30 kHz.

The grey relational grade shows the influence of factors with their levels for each scribing parameter and illustrates the variable response for the three different levels. Table 4 lists the difference between the maximum and minimum values of the grey relational grade for each factor, which indicates that as the difference increases, the effect of laser scribing factor on the performance characteristics also increases. This difference can be defined as the effect contribution of control factors, which follow the order of C, A, and B. This order demonstrates that the first effect value of 0.1473 is the Q-switching frequency, which has a little stronger effect than other laser scribing factors; the second effect value of 0.1436 is the laser average power; and the third effect value of 0.1090 is the laser scribing speed.

Table 4
Response table for the grey relational grade.

Cutting factors	Average grey relational grade by factor level			
	Level 1	Level 2	Level 3	Max.-Min.
A	**0.6181***	0.5444	0.4745	0.1436
B	**0.5829***	0.5802	0.4739	0.1090
C	0.4852	**0.6325***	0.5192	0.1473

* Optimal level.

To verify the optimal laser scribing parameters, one additional experiment (Table 5) was conducted to confirm the influences of the optimal combination of control factors and their levels on the performance characteristics. Fig. 3(a) indicated the 3D profiling of the optimal combination in experiment 4. Fig. 3(b) demonstrated the 3D profiling of the optimal combination in the confirmation experiment from Table 3, The average groove width was 41.15 μm and the average groove depth was 10.20 μm. Compared with the optimal combination in experiment 4, which derived the highest grey relational grade, the average groove width is 42.67 μm and the average groove depth is 9.19 μm. This phenomenon accounts for the improvement in average groove width from 42.67 to 41.15 μm (a reduction of 1.52 μm for the smaller-the-better), and the improvement in average groove depth from 9.19 to 10.20 μm (an addition of 1.01 μm for the larger-the-better). In this study, the application of GRA was successful and improved the quality characteristics of laser scribing for the isolation process for solar cell wafers.

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Table 5

Results of confirmation experiments

Laser beam scribing parameters (A1B1C2)	Sample
A laser average power (% of 10 Watt)	85
B laser scribing speed(mm/s)	400
C Q-switch frequency (kHz)	30
Performance characteristics of confirmation experiments	
The average groove width (μm)	41.15
The average groove depth (μm)	10.20

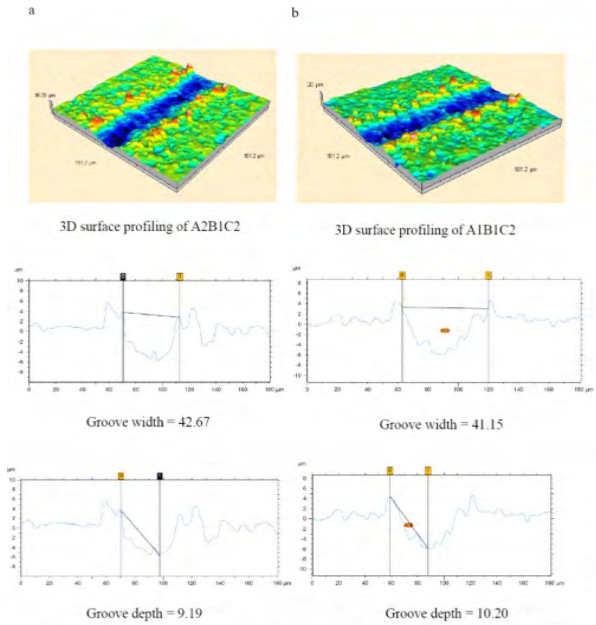


Fig. 3 Comparisons of the measured surface profiling. (a) Experiment 4 for order 1: A2B1C2; (b) confirmation experiment for optimal combination: A1B1C2.

V. CONCLUSIONS

The laser ablation for the isolation process on a solar cell wafer substrate was investigated on the basis of surface morphology observations. This work presented a novel laser scribing procedure for the isolation process of solar cell wafers based on average groove width, and groove depth. For the analytical data generated by the nine experiments using three laser control factors, GRA obtained the grade distribution and verified the laser scribing parameters that demonstrated optimal performance characteristics. By employing GRA, the contribution of each factor was weighted according to its importance. One additional experiment using the optimal parameters was also performed to confirm the effects of different parameters. The optimal laser scribing parameters were obtained successfully.

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Optical properties of silicon light trapping structures for photovoltaics

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ABSTRACT

Light trapping structures in photovoltaics are essential to suppress reflection losses and increase conversion efficiency. For wafer silicon (Si) solar cells, this is commonly achieved by chemical texturing and the application of an antireflection coating. Such surfaces still show significant reflection losses that are ~10%. Hence, for further reduction in reflection, new methods for light trapping need to be explored, which are effective for a broad solar spectral and angular range. In this paper, we explore an ultrafast laser texturing method that successfully reduces the reflection below 5% over a broad spectral and angular range and more importantly, is applicable to crystalline, multi-crystalline, thin film silicon and other materials. The optical properties of ultrafast laser textured silicon surfaces produced in a sulfur hexafluoride (SF_6) gas ambient are evaluated by total reflection including scattering as a function of wavelength and angle of incidence. The optical results are further compared with other texturing schemes. This study also investigates the silicon bandgap modification induced by ultrafast texturing method. Finally, a comparison is made for the photovoltaic parameters of solar cells made of ultrafast laser textured surfaces, chemically textured surfaces, porous silicon surfaces, and etched silicon surfaces that result in nanowires for light trapping to understand impact of surface texturing on photovoltaic device performance.

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1. Introduction

For photovoltaic applications, near zero reflection over a broad spectral and angular range is desired to increase conversion efficiency. Surface texturing greatly enhances the optical path length of the incident light and reduces surface reflection and has become indispensable for solar cells. For silicon solar cells, surface texturing is conventionally obtained by chemical (anisotropic and isotropic) etching [1,2]. Chemical etching techniques produce randomly distributed structures on the silicon surface. Antireflection coatings (ARC) like titanium dioxide, silicon nitride (SiN_x), etc. are used for further reduction of reflection. Even with ARC, chemically textured surfaces still show reflection losses of about 5–10% [3–5]. Furthermore, these techniques are inapplicable to thin film silicon solar cells and are less effective for multi-crystalline silicon wafers, which are more widely used. Hence, it becomes essential to explore new surfaces texturing methods that are suitable to next-generation ultrathin ($<100\,\mu m$) wafers (crystalline and multi-crystalline) and thin film ($<5\,\mu m$) silicon solar cells. Density graded (porous) silicon surfaces, silicon nanowires, nanoholes, laser texturing and plasmonics for thin films are some of the promising alternatives that have been recently reported [6–15] out of which laser-induced surface texturing is fast emerging to be an attractive alternative. Currently, laser processing plays an important role in photovoltaic manufacturing [16–22] and is showing immense potential for new applications like doping, back fired contacts, etc. [23–33], which is a great motivation to explore laser surface texturing.

Laser surface texturing has been achieved using lasers with pulse widths in the nanosecond and femtosecond regime [11,34,35]. Depending on the pulse width, wavelength and laser fluence, surface texturing is obtained either by (a) ablation-induced surface grooving [10,34] or (b) laser-induced self-assembled semi-periodic light trapping structures [29,36–38]. The ablation-induced surface grooving technique creates 50 μm deep craters to reduce reflection losses with significant material lost during etching of the laser-damaged region. Short wavelength ($\lambda=248$ and 532 nm) nanosecond laser irradiation can create self-assembled conical pillars that very effectively trap light, but the height of these pillars are over 20 μm. This makes the process unsuitable for next-generation ultrathin wafers, where the texture size approaches the thickness of the wafer. Ultrafast (fs and ps) lasers on the other hand are able to create similar conical structures that are about 3–10 μm high with similar light trapping properties [39–41]. The high density or decreased periodicity of these structures relaxes the pillar height thus providing excellent light trapping. The other advantage of ultrafast laser (femtosecond pulses) over pulsed (nanosecond pulses) laser processing is that the heat-affected zone and laser-induced damage can be greatly minimized [40]. Hence, ultrafast laser processing is seen to be a very promising technology for surface texturing.

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In this paper, we report results of total integrated light scattering (TIS), which is inclusive of reflection, scattering and transmission, as a function of angle and wavelength for femtosecond laser textured silicon surfaces prepared in a SF_6 gas ambient. We further compare it with graded density porous surfaces and chemically textured surfaces, which are very effective light trapping schemes. Through this optical study, we also investigated the role of sulfur incorporation in silicon during the ultrafast laser texturing process, which creates an intermediate band within the silicon bandgap. Lastly, we compare the photovoltaic device parameters of ultrafast laser textured silicon solar cells fabricated in our laboratory and compare it with other texturing schemes discussed in the literature to fully understand the implications of surface texturing on photovoltaic device performance. The goal of this work is to study the optical properties of femtosecond laser-induced light trapping structures, its control and highlight its role as an alternative method for texturing of single crystal silicon, multi-crystalline silicon and thin film silicon for photovoltaics applications.

2. Experimental

Ultrafast laser texturing is achieved by exposing float zone (FZ) Si (1 0 0) wafers of thickness 280 μm and resistivity of 1 Ω cm to a train of femtosecond (130 fs) pulses from a Spectra Physics Ti–sapphire laser system (1 mJ pulse energy; frequency 1 kHz) having a wavelength of 800 nm. The experiments are carried out in 800 mbar pressure of SF_6 gas. Large area texturing is obtained by scanning the sample under the laser beam using a computer controlled precision *x*–*y* stage. Samples with different texture heights are prepared by varying the average number of laser pulses impinging on the silicon surface. The average numbers of laser pulses are controlled by varying the velocity at which the samples are scanned under the laser beam. Further details describing the processing of the samples is described in Ref [35]. One of the ultrafast laser textured silicon samples also undergoes a thermal annealing step in the presence of oxygen at 1100 °C for 7 h. Next, chemically textured (CT) silicon surfaces are obtained by anisotropic etching in a mixture of sodium hydroxide, isopropyl alcohol and de-ionized water [42]. After chemical texturing, 70 nm of silicon nitride is deposited using a plasma enhanced chemical vapor deposition (PECVD) system to serve as an antireflection coating. Lastly, density graded porous silicon surfaces (PS) are obtained by a technique described in reference [8] investigated for photovoltaic applications. This is very similar to the nanoporous surfaces reported by NREL [43]. The morphology of the textured surfaces is investigated using a Zeiss SUPRA 40 scanning electron microscope.

Total integrating scattering (sum of specular reflection, scattering and transmission) values are obtained using a 6 in. integrating sphere (Model#RTC-060-SF from Labsphere Inc.) with spectraflect coating. Individual lasers of different wavelengths (405–1550 nm) are used as the light sources. The textured samples are mounted in the center of the sphere using a jaw and clip type center mount holder. This enables the measurement of total integrated scattering as a function of angle. Total integrated scattering is calculated by measuring the signal from the sample and normalizing it with a calibrated reflectance standard. Next, angular scattering measurements are made by having the incident light normal to the textured surface and detecting the scattered light at different detection angles (θ_d) with respect to the normal. A silicon detector (model#818-SL) and a germanium detector (model#818-IR-L) with a power meter (model#1830-C), all from Newport Corp., are used to measure the incident and reflected powers. Specular reflection and transmission are measured using a Film Metrics reflectometer and an absorption spectrophotometer (Perkin Elmer Lambda EZ201).

Lastly, solar cells (active area = 1 cm^2) on ultrafast laser textured FZ-silicon surfaces are fabricated to assess the performance of texturing method. These results are then compared with solar cells having different texturing schemes found in the literature. Ultrafast laser textured silicon solar cell fabrication steps include, (a) laser damage removal by chemical etching, (b) thermal defect annealing at 1050 °C for 60 min, (c) emitter doping by the spin on doping method, (d) surface passivation with 10 thermal oxide and 70 nm PECVD silicon nitride, (e) formation of a back surface field and contact using a Ferro 53-038 aluminum paste, (f) photolithography for front electrode patterning (g) e-beam evaporation of Ti (100 nm)/Pd (50 nm)/Ag (1000 nm) followed by 3 μm Ag electroplating and (h) forming gas annealing at 400 °C for 20 min. Devices are characterized for total efficiency and quantum efficiency. Further details on the device fabrication steps and characterization can be found in Ref. [38,44].

3. Results and discussion

Fig. 1 shows the scanning electron microscope images of the three types of textured surfaces used in this work.

Fig. 2 shows the total integrated scattering (TIS), which includes reflection, scattering and transmission measurements as a function of angle for different wavelengths for ultrafast laser textured silicon. These measurements are further compared with chemically textured silicon having SiN_x as ARC and for a porous silicon surface. Fig. 2 also includes an ultrafast laser textured silicon sample that is thermally annealed in a dry oxygen environment at 1100 °C for a period of 7 h in a tube furnace. The thickness of the resulting thermal oxide on a planar control surface is measured to be ~250 nm.

The comparison of these four types of textured structures is indeed very interesting because the mechanism of light trapping for each one is different. Light trapping for the ultrafast laser textured surface and the conventional chemically textured surface is governed by multiple reflections [45]. Ultrafast laser textured silicon surfaces processed in SF_6 gas ambient have about 1 at% of sulfur incorporated in the silicon surface. Such a high concentration of sulfur in silicon creates an intermediate band within the bandgap of silicon. This enables silicon to absorb photons with energies smaller than its bandgap. This means that light absorption for the ultrafast laser textured silicon occurs by multiple light reflections and sulfur mediated absorption. For the porous silicon case, light trapping is obtained by the gradual modulation of the effective refractive index that tends to be close to unity as suggested by Refs. [7,46].

As seen in Fig. 2, the porous silicon surface is the most effective medium to reduce reflection. It is also seen that the porous silicon surface has little or no angular dependence as seen in Fig. 2(a)–(d). However, we can clearly see a weak angular dependence for all other textured surfaces. It is also apparent that the chemically textured surface with ARC displays an angular dependence that is similar to the laser textured sample. We have also carried out Monte Carlo based ray tracing (TracePro from Lambda Research Corp.) to simulate the optical characteristics of thermally annealed ultrafast laser textured silicon surfaces. The simulation results are included in Fig. 2(b). It can be seen that the simulation results closely match the experimentally measured values. The small deviation of the simulated results from the experimental values can be attributed to surface roughness, feature size variation, etc. in our samples, which have not been included in the simulations. Thus, it is clear that light trapping in the ultrafast

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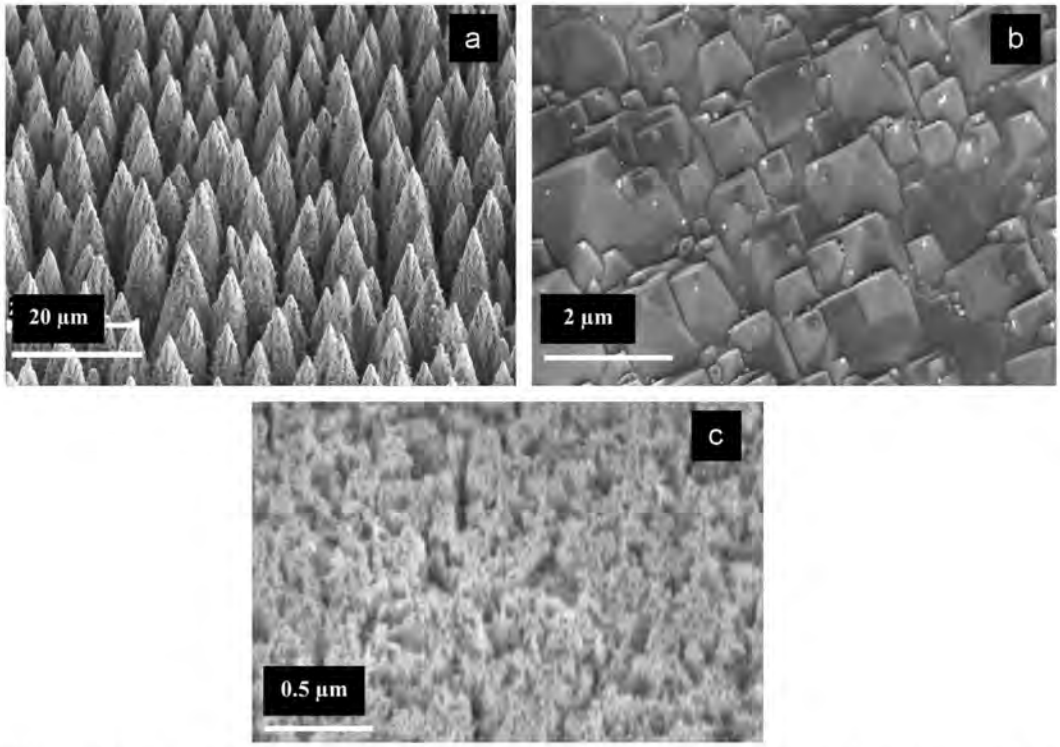


Fig. 1. SEM images of (a) ultrafast laser textured silicon surface in SF_6 gas ambient, (b) chemically textured silicon surface and (c) porous silicon surface.

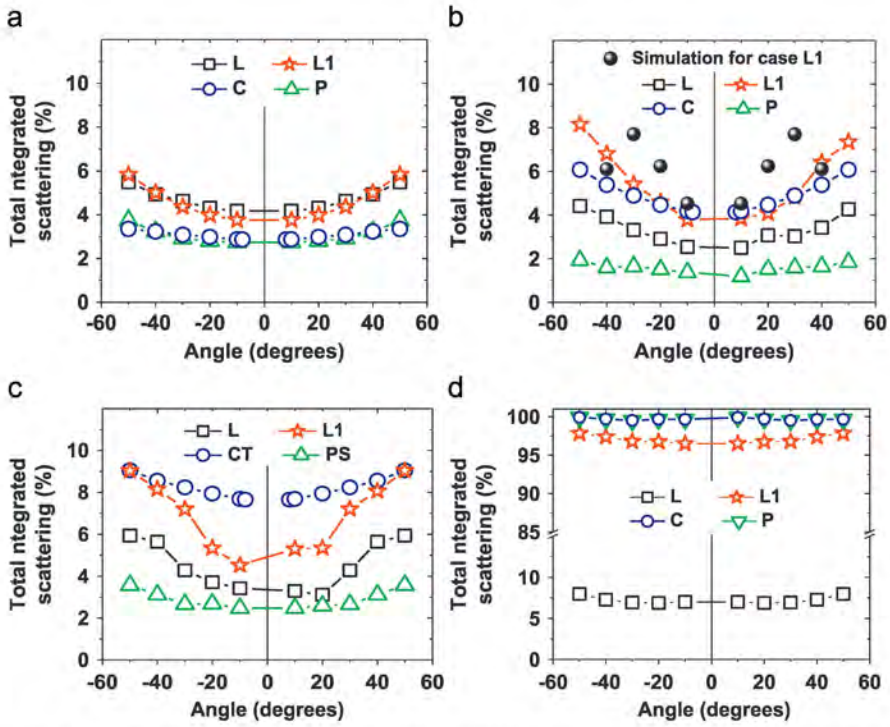


Fig. 2. Total integrated scattering (TIS) as a function of angle for wavelengths (a) 405, (b) 633, (c) 980 and (d) 1550 nm. The different types of textured surfaces included are ultrafast laser textured silicon (L), ultrafast laser textured silicon that has been annealed (L1), chemically textured silicon with SiN_x (C) and porous silicon surface (P). Simulated values for case L1 are also included in (b).

laser textured silicon surfaces occurs mainly due to multiple light reflections. It is also interesting to note that in Fig. 2(d), the ultrafast laser textured surface only scatters about 7% at a wavelength of 1550 nm. This fact can be attributed to the modification of the silicon bandgap as mentioned earlier in this section. Similar behavior is also observed (not shown) for a wavelength of 1310 nm. However, the most striking attribute in Fig. 2(d) is that the total integrated scattering for the thermally annealed ultrafast laser textured sample is close to 100%. This implies that the sample no longer absorbs photons with energies less that its bandgap. The light scattered from the textured surface and light transmission through the sample accounts for the ~100% of the incident light. This confirms the fact that prolonged thermal annealing is able to recover the original absorption properties of silicon. Crouch et al. [47] reported that thermal annealing at 600 °C for 30 min reduces the net absorption to about 14%. As expected, porous silicon and chemically textured samples also display no absorption as seen in Fig. 2(d). Next, we plot the total integrated scattering as a function of wavelength for all the samples at an incidence angle of 8° and data are shown in Fig. 3. Fig. 3 also includes the reflection curve for the chemically textured surface without SiN_x.

From Fig. 3 we can clearly see that density graded porous silicon sample exhibits the lowest reflection. The L, L1 and C samples all show refection that is below 10%. Monte Carlo simulation results of total integrated scattering for the sample L1 is also included, which agrees reasonably well with the experimental values. We have also seen that the reflection of ultrafast laser textured sample reduces below 1% with the deposition of SiN_x as the antireflection coating.

One should note that the presence of SF_6 gas ambient during the ultrafast laser texturing process is not necessary. Similar structures have been obtained when the texturing process has been carried out in different ambients like vacuum, air, nitrogen gas and hydrochloric gas which means that problems like sulfur incorporation and use of a green house gas like SF_6 can be avoided [35,48].

This ultrafast laser process-induced light trapping structures are highly reproducible, controllable and provide excellent surface coverage unlike chemically textured surfaces. The ultrafast laser texturing process can be controlled by varying the laser

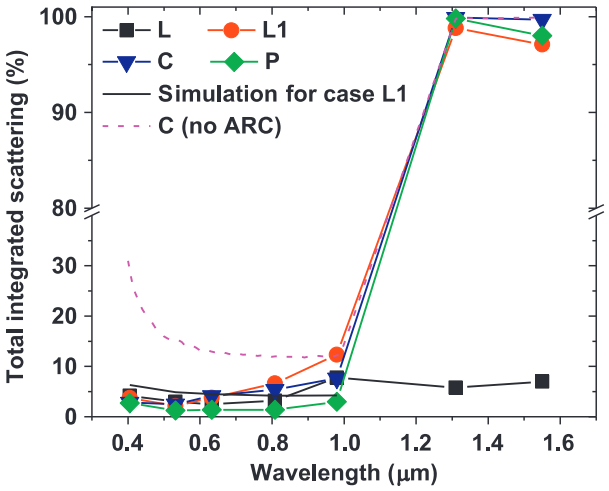


Fig. 3. Total integrated scattering as a function of wavelength at an incidence angle θ_i of 8° for ultrafast laser textured silicon (L), ultrafast laser textured silicon that has been annealed (L1), chemically textured silicon with SiN_x (C) and porous silicon surface (P).

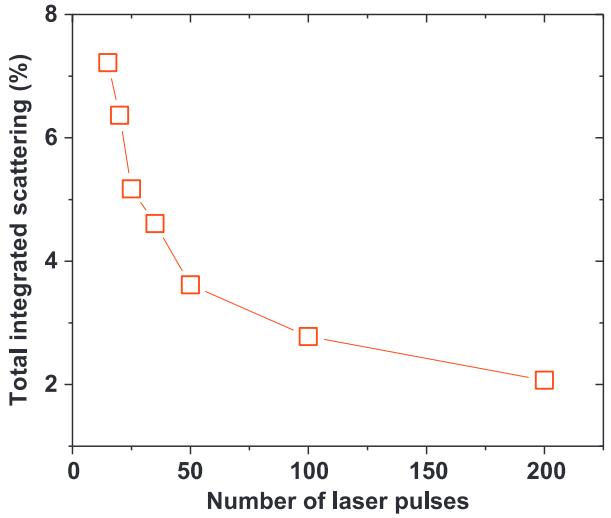


Fig. 4. Total integrated scattering as a function number of laser pulses for ultrafast laser textured silicon. Angle of incidence is 8° and wavelength of incident light is 633 nm.

fluence or the average number of impinging laser pulses. This enables the control of the surface texture morphology and hence total integrated scattering. The resulting morphology can be varied from sub-micron ripples to tall conical pillars that are several microns in height. Fig. 4 shows the total integrated scattering at $\lambda = 633$ nm for different number of pulses.

It is clear from Fig. 4 that the total integrated scattering decreases as the number of laser pulses impinging the silicon surface increases. Higher number of laser pulses implies a higher ablation, which leads to taller pillars with smaller cone angles. Another noteworthy point is that the reflection abruptly drops to 7% for 15 laser pulses where the surface is covered with ripples rather than tall conical structures. This regime is particularly important for thin film silicon solar cell applications where ultrafast laser processing can be used for simultaneous crystallization and surface texturing as demonstrated by Nayak and Gupta [49].

For further optical characterization, we measure the specular reflection (R) and transmission (T). This enables us to calculate the total absorption (A) for different types of textured surfaces using $A = 1 - (R + T + \text{TIS})$. The results are summarized in Table 1.

From Table 1 it is clear that specular reflection and transmission for all textured samples have been suppressed below 0.1% indicating a highly scattering surface. For all the textured surfaces, we also see that the total absorption in silicon is ~95% over the spectral range. As expected, the absorption for annealed ultrafast laser textured silicon, porous silicon surface and chemically textured silicon with ARC is 0%.

We further characterize the ultrafast laser textured surfaces by its angular scattering properties. The experimental setup is shown in Fig. 5(a) where the scattering as a function of detection angle is measured for normal light incidence. Here, scattering is defined as the ratio of the detected light power to the incident light power. The two types of samples characterized are the ultrafast laser textured silicon and ultrafast laser textured silicon that has been annealed. As discussed earlier, the intermediate band effect in ultrafast laser textured silicon is eliminated on thermal annealing and photons with energies lower than the bandgap of silicon are no longer absorbed. This prompted us to check the scattering properties of the annealed ultrafast laser textured silicon at $\lambda = 1310$ nm for two

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different configurations C1 and C2. For the C1 case, light is incident on the textured surface and for the C2 case, light is incident on the opposite polished surface. For both configurations, backward and forward scatterings are measured. The scattering characteristics for the both samples are shown in Fig. 5(b)

It is clear from Fig. 5(b) that for both configurations, scattering values are nearly the same with a small peak for the forward (transmitted) scattering only. As expected this peak is lower for the case where the light is incident on the polished surface as opposed to light incident on the textured surface thus confirming the scattering nature of the ultrafast laser textured surface. It is also clear from Fig. 5(b) that the angular dependence for ultrafast laser textured silicon surface is lower than for its annealed counterpart.

Until now we have discussed in detail the optical properties of light trapping structures for application in silicon solar cells. Although the discussed textured surfaces provide excellent light trapping, it is very essential to understand the impact these surfaces have on the photovoltaics conversion performance. Therefore, we fabricated silicon solar cells on laser textured silicon surfaces and compared the total and quantum efficiency with solar cells made with other texturing techniques that were discussed in the previous section. The silicon nanowire (Si nw) technique has also been included, which is similar to the porous silicon surface. The height of nanowires here are about 3–4 μm compared to the 300 nm tall nanowires for the porous silicon case. The photovoltaic device parameters for the four different types of solar cells are summarized in Table 2. All the devices in Table 2 have similar emitter doping concentrations, surface passivation layers and alloyed aluminum back surface field to ensure a fair comparison.

The device with a chemically textured surface and SiN_x as the ARC is used to benchmark solar cells with other surface texturing schemes. It is evident from Table 1 that the ultrafast laser texturing scheme results in the highest short-circuit current density of 39.2 mA/cm^2 and is a clear indication of superior light trapping. However, the device displays a conversion efficiency of over 14% due to a lower open-circuit voltage. We believe that proper optimization of surface dopant concentration, removal of laser-induced defects and a better surface passivation layer will improve the V_{oc}. The silicon nanowire scheme also shows a very promising current density value with a conversion efficiency of 13.7%. The porous silicon solar cell reported by NREL shows the best conversion efficiency of around 16.8% and a short-circuit current density of 34.1 mA/cm^2. The question now arises as to why there is a significant variation in the short-circuit current density among the different surface texturing schemes even though all of them have reflection losses below 5–6%. Hence, in order to gain a further insight on the impact of surface texturing

Table 1
Summary of the optical properties of different types of textured surfaces used in this work.

Sample	Wavelength (nm)	Reflection (%)	Transmission (%)	TIS (%)	Absorption (%)
Double side polished Si	405	47.81	0	-	52.19
	633	34.77	0	-	65.23
	980	31.76	1.13	-	67.11
	1550	46.78	52.61	-	0
Ultrafast laser textured Si	405	< 0.1	< 0.1	4.1	95.7
	633	< 0.1	< 0.1	2.5	97.3
	980	< 0.1	< 0.1	7.8	92
	1550	< 0.1	< 0.1	7	92.8
Annealed ultrafast laser textured Si	405	< 0.1	< 0.1	3.7	96.1
	633	< 0.1	< 0.1	3.8	96
	980	< 0.1	< 0.1	12.3	87.5
	1550	< 0.1	< 1	97.8	~0
Porous Si	405	< 0.1	< 0.1	2.7	97.1
	633	< 0.1	< 0.1	1.36	98.44
	980	< 0.1	< 0.1	3.9	95.9
Chemically textured Si with SiN_x	405	< 0.1	< 0.1	2.8	97
	633	< 0.1	< 0.1	4.13	95.67
	980	< 0.1	< 0.1	7.6	92.2

Table 2
Device parameters of silicon solar cells fabricated on ultrafast laser textured surface and compared with various other texturing techniques.

Surface texturing type	V_{oc} (mV)	I_{sc} (mA/cm^2)	FF (%)	Efficiency (%)	Reference
Ultrafast laser texturing	507	39.2	72	14.12	This work
Porous Si surface	612	34.1	80	16.8	[50]
Chemically textured + SiN_x	632	35.2	81.2	18	[51]
Si nanowire	544	37	68	13.7	[14]

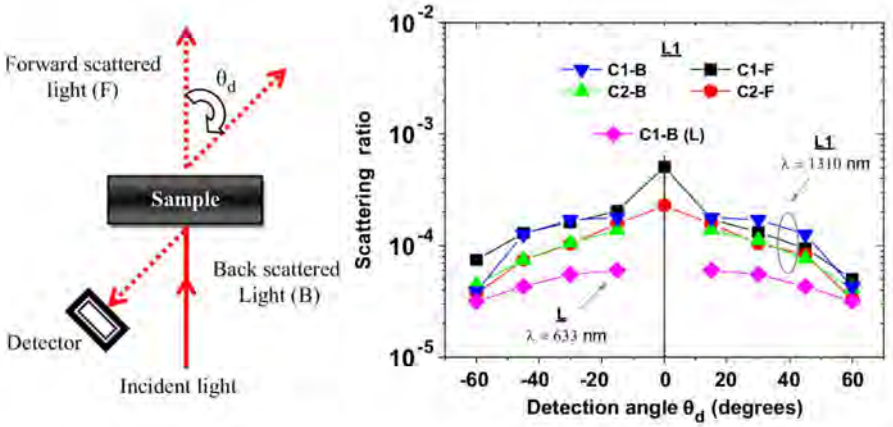


Fig. 5. (a) Experimental setup used to characterize light scattering for the ultrafast laser textured surface and (b) scattering as a function of detection angle for the ultrafast laser textured silicon (L) and annealed ultrafast laser textured silicon (L1) surfaces. L1 sample has been characterized by forward (F) as well as backward scatterings (B) at a wavelength of 1310 nm. The C1-B curve represents the backward scattering ratio and C1-F refers to forward scattering ratio for the configuration where light is normally incident on the textured surface. The C2-B curve represents the backward scattering ratio and C2-F refers to forward scattering ratio for the configuration where light is normally incident on the polished surface. The ultrafast laser textured silicon, C1-B (L), surface is only characterized for backward scattering for a wavelength of 633 nm.

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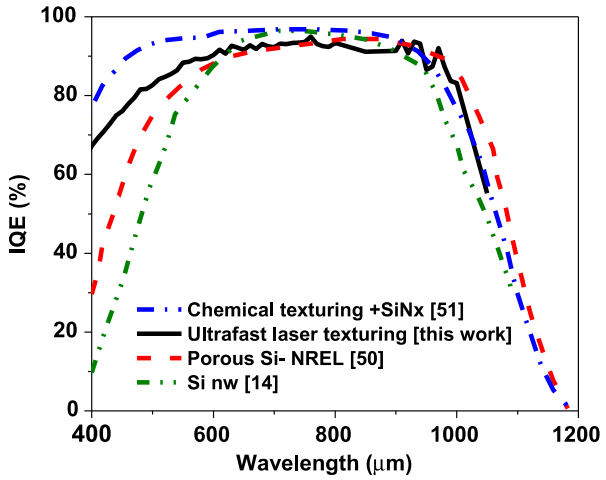


Fig. 6. Internal quantum efficiency of solar cells fabricated with different texturing schemes.

on performance of solar cells, we compare the internal quantum efficiencies (IQE) of devices with different types of textured surfaces and the results are shown in Fig. 6.

From Fig. 6 it is evident that the chemically textured device displays the best IQE, which is again the benchmark. However a very interesting trend in the short wavelength (400–600 nm) response among various techniques emerges. It should be noted that the porous silicon and silicon nanowire schemes have wires that are ~300 nm and 3–4 μm tall, respectively. Clearly, the short wavelength response for the ultrafast laser textured device is significantly better than the devices with porous silicon and silicon nw schemes. The authors attributed this poor short wavelength response of porous silicon surfaces to an extremely high surface recombination velocity and higher auger recombination due to the conversion of the 300 nm wires to n^+ type [50]. This can be used to explain the increased short wavelength losses for the Si nw device because of increase in height of the nanowires and surface area. However, for the ultrafast laser textured device, the problem of conversion of the surface features to n^+ type is avoided as the feature sizes are in the order of several microns similar to the chemically textured pyramids with conformal doping. However, an excellent passivation scheme is needed to passivate the large surface area induced by the ultrafast laser texturing method. The variation in long wavelength response for the different surface texturing schemes in Fig. 6 is negligible. This is evident that the surface texturing methods do not impact the long wavelength response and are in line with the chemically textured benchmark data. An improvement can however be seen if a rear passivated back electrode structure replaces the full area back surface field. Thus, the variation in the short-circuit current densities and open-circuit voltage can be partially explained by the examination of IQE response.

4. Conclusion

We demonstrate a method for surface texturing of silicon using an ultrafast laser processing method that produces self-assembled conical pillars with high uniformity, reproducibility and is applicable to crystalline, multi-crystalline and thin film silicon. The optical properties of such an ultrafast laser textured silicon surface are investigated in detail and compared with other texturing methods. Through experimental measurements and Monte Carlo simulations of ultrafast laser textured silicon surface, it can be concluded that (a) the mechanism of light trapping occurs mainly through multiple reflections, (b) surfaces appear black to the naked eye with a reflection of few percent over a wide spectral and angular range, (c) the losses are primarily due to scattering with negligible ($<0.1\%$) specular reflection and (d) reduction in long wavelength ($\lambda=1310$ and 1550 nm) absorption due to sulfur incorporation in ultrafast laser textured silicon surfaces. Lastly, the impact different texturing methods has on photovoltaic performance is investigated. From the short-circuit current density and internal quantum efficiency, it can be concluded that the ultrafast laser texturing has the least impact on fabricated solar cells with short-circuit current densities over 39 mA/cm^2 making it an ideal alternative to create light trapping structures for silicon photovoltaics.

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Analysis of multi-crystalline silicon solar cells at low illumination levels using a modified two-diode model

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ABSTRACT

Current–voltage characteristics of multi-crystalline silicon solar cells measured under several low illumination levels are analyzed. The fitting analysis is conducted using a modified two-diode equivalent circuit accounting for an additional ohmic series resistance in the vicinity of grain boundaries and allowing for variable diode ideality factors. Apart from the shunt resistance—a key factor at very low illumination levels—the model indicates two other current transport mechanisms at low illumination levels, both related to recombination, but each of them can be allocated to a different region in the cell: (1) recombination in the crystalline region and (2) recombination at grain boundaries. The role played by each mechanism is studied depending on illumination level.

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1. Introduction

Multi-crystalline silicon solar cells constitute one of the main solar cell branches on the PV market; still, there is room for enhancing the efficiency of these cells in comparison with mono-crystalline ones. Losses in multi-crystalline cells are often put in relation with grain boundaries, where recombination is likely to take place. Therefore, current transport in these cells is better described through a model that takes the effect of grain boundaries into consideration. Increasingly, the one-diode model usually applied to analyze *I–V* characteristics of multi-crystalline silicon solar cells is making way for different forms of the two-diode model [1–4], especially at low illumination levels [2]. This is the case when solar cells are utilized for indoor applications. Some groups even proposed a 3-diode equivalent circuit, accounting for a large leakage current through periphery [5].

Having decided in favor of a two-diode model, it is important to identify the current transport mechanism of each diode and its domain of action in the cell. Most groups proposing two-diode models for describing current transport in multi-crystalline silicon solar cells use constant diode ideality factors $n_1=1$ and $n_2=2$ [4–8]. This would mean that the first mechanism is an ideal diffusion one and the second mechanism is recombination at defects with an energy level exactly equal to the intrinsic Fermi level (i.e. with an activation energy exactly equal to half the energy gap of the absorber). Although the assumption of constant diode ideality factors would simplify the fitting analysis by reducing the number of fitting parameters, it represents a strong restriction of the possible current transport mechanisms that may result from the analysis and of the possible activation energies of the transport mechanisms.

On the other hand and in order to identify the contribution of each mechanism to the whole cell performance, a method was presented recently [9], which calculates the fraction of photo-current needed to compensate for the loss current of each mechanism under open circuit condition. The so calculated compensation current in each branch of the equivalent circuit is a measure of the role played by the corresponding mechanism in limiting cell performance.

In this paper, a modified two-diode model is presented that accounts for an additional ohmic series resistance in the vicinity of grain boundaries and assumes variable diode ideality factors—representing the reality more accurately. The application of the model is carried out on *I–V* characteristics of multi-crystalline silicon solar cells at room temperature and under various low illumination levels. Furthermore, the compensation current in each branch of the equivalent circuit is deduced depending on illumination level.

2. The model

Our model is a modified two-diode equivalent circuit (see Fig. 1) based on the following assumptions:

- The cell consists of two different regions with different current transport mechanisms: the crystalline region and the grain

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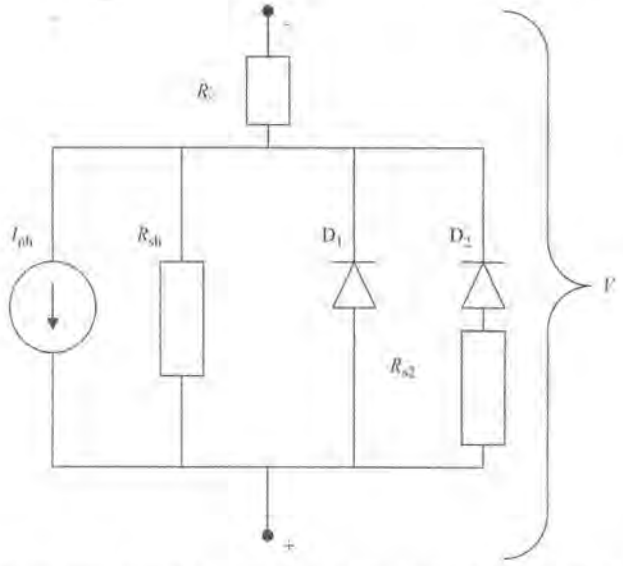


Fig. 1. Modified two-diode equivalent circuit used in this study for analyzing the multi-crystalline silicon solar cell.

boundary region, accounted by the two parallel diodes D_1 and D_2 in the equivalent circuit, respectively.

- The grain boundary region exhibits an additional series resistance since the resistivity in the vicinity of grain boundaries is higher than that within the crystallites [10]. This is accounted for by R_{s2}, which is connected to D_2 in Fig. 1.
- A shunt resistance R_{sh} is connected in parallel to both diodes D_1 and D_2. Furthermore, a series resistance R_s is connected to all three branches.
- The equations describing current transport through the cell contain variable diode ideality factors, so that the restriction of current transport mechanisms mentioned above is lifted.

In accordance with this equivalent circuit, the total current that flows through the cell can be written as follows:

$$I(V) = I_1(V) + I_2(V) + \frac{[V - I(V)R_s]}{R_{sh}} + I_{ph} \quad (1)$$

Here R_s is the series resistance, R_{sh} the shunt resistance and I_{ph} the photo-current. The quantities $I_1(V)$ and $I_2(V)$ represent currents that flow through diode D_1 and diode D_2, respectively, and can be written as

$$I_1(V) = I_{01}\left\{\exp\left[\frac{q[V - I(V)R_s]}{n_1 kT}\right] - 1\right\} \quad (2)$$

$$I_2(V) = I_{02}\left\{\exp\left[\frac{q[V - I(V)R_s - I_2(V)R_{s2}]}{n_2 kT}\right] - 1\right\} \quad (3)$$

where I_{01} and I_{02} are the saturation currents, n_1 and n_2 the diode ideality factors, q is the electron charge, k the Boltzmann constant, T the absolute temperature and R_{s2} is an additional series resistance connected to D_2.

3. Experimental

The analyzed cell was a 7.7 cm^2 partition of a cell denoted Q6-1380 (not encapsulated), which was thankfully provided by Q-Cells AG, Germany. Table 1 summarizes the cell properties taken from its data sheet. Current–voltage characteristics of the analyzed cell were measured at room temperature and investigated under several low illumination levels. Measurements were performed using a Keithley 238 Source Measure Unit (SMU) through a four-point connection. Halogen lamps were used for illumination, whereas a silicon calibration cell was used to set the illumination level. The illumination level was varied between 0 mW/cm^2 (dark) and 20 mW/cm^2. Fig. 2 presents the illumination level dependent I–V characteristics performed at room temperature.

Table 1
Data of the cell Q6-1380 provided by Q-Cells AG, Germany. The analyzed cell was a 7.7 cm^2 partition of this cell.

Product	Multi-crystalline silicon solar cell
Format	150 × 150 mm^2 ± 1 mm
Thickness	300 μm ± 40 μm
Front (−)	2 mm bus bars (silver), blue anti-reflection coating (silicon nitride)
Back (+)	5 mm wide soldering pads (silver/aluminum), back surface field (aluminum)

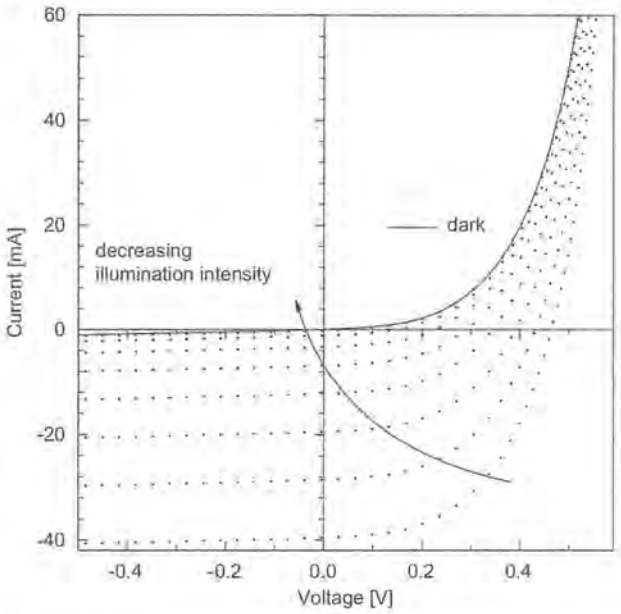


Fig. 2. Illumination-level-dependent current–voltage characteristics for the analyzed solar cell performed at room temperature.

4. Analysis and discussion

Current–voltage fitting characteristics of a multi-crystalline silicon solar cell were analyzed using the model presented above. The fitting method used was a least squares method. The need for a two-diode model for describing this cell is demonstrated through a comparison between the fitting results of its dark I–V curve, first with an one-diode model (deleting the branch of D_2 and R_{s2} in Fig. 1), and then with the two-diode model proposed above (Fig. 1). Table 2 shows the fitting parameters in each case, where it is clear that the two-diode fit gives a better χ^2 value than the one-diode fit by two orders of magnitude. Furthermore, Fig. 3 presents a comparison between the two fits, showing the need for the two-diode fit especially in the voltage region between 0.2 and 0.5 V.

Table 3 summarizes the parameters obtained by analyzing the I–V characteristics measured at room temperature under several illumination levels.

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Table 2
Comparison between the parameters obtained from fitting the measured dark *I–V* characteristic of the studied cell using first a one-diode model, and then the two-diode model proposed.

	R_{sh} (Ω)	R_{s2} (Ω)	R_s (Ω)	n_2	I_{02} (A)	n_1	I_{01} (A)	χ^2 (A^2)
One-diode model	569.6		0.0413			3.236	1.243E−4	2.83E−4
Two-diode model	568.3	1.6425	0.1645	2.949	1.491E−4	1.411	1.117E−8	6.23E−7

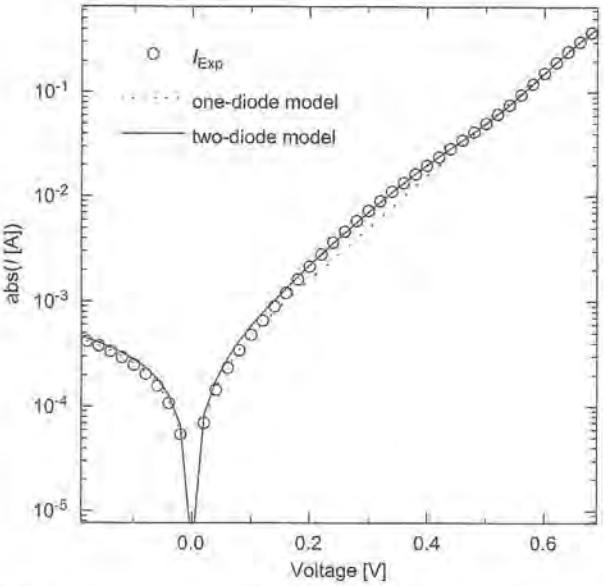


Fig. 3. Comparison between two fits of the dark *I–V* characteristic using first a one-diode model, and then the two-diode model proposed. The discrepancy is largest in the range between 0.2 and 0.5 V.

Since the model allocates D_1 to the crystalline region and D_2 (with the additional series resistance R_{s2}) to the grain boundary region, it is obvious that parameter set (I_{01}, n_1) describes current transport in the crystalline region, while parameter set (I_{02}, n_2) characterizes current passing along grain boundaries. In the following, a closer investigation of the obtained ideality factor values is presented.

In the literature, a value of n between 1 and 2 is often interpreted in terms of the Shockley–Read–Hall (SRH) model [11,12]. According to this model, the diode ideality factor should be equal to 2 if recombination in the space charge region (SCR) takes place via a single trap level in the middle of the absorber band gap; however, for an exponential distribution of trap states in the SCR and depending on the doping concentrations and energetic and spatial distribution of the recombination centers, the value of n may vary between 1 and 2 [13–15]. Another possible interpretation for diode ideality factor values between 1 and 2 is that current is dominated by a combination between recombination in the SCR and recombination in the (neutral or quasi-neutral) bulk [16]. In many cases, describing the cell with a single diode model reveals a diode ideality factor between 1 and 2 (interpreted as a combination of both diffusion as well as recombination in the SCR at the same time [17]); however, describing the same cell with the double-diode model would reveal the standard values of $n_1=1$ and $n_2=2$, which is then interpreted as diffusion for the first diode and recombination for the second [4]. In this paper, the values of n_1 (for diode D_1) lie between $n_1=1.36$ and $n_1=1.41$. This indicates that current transport in the crystalline region of the studied cell is controlled either by recombination in the SCR at an exponential distribution of trap states in the absorber band gap or by recombination in both SCR and bulk (quasi-neutral region) or by both diffusion as well as recombination in the SCR. The term "recombination in the crystalline region" (as opposed to the grain boundary region) is found suitable for describing these possibilities here.

A diode ideality factor greater than 2, although rarely presented for laboratory crystalline silicon cells, is often observed for industrial cells [18]. Generally, such relatively large diode ideality factors are observed in hetero-junction devices (e.g. solar cells based on chalcopyrite compounds); these factors are thought to result from recombination at a high density of defect states, either directly [19–21] or assisted by tunneling [22–24]. In polycrystalline silicon, high density of electrically active defect states is likely to be found at grain boundaries [25,26]. In this paper, the values of n_2 (for diode D_2) lie between $n_2=2.95$ and $n_2=3.1$. This indicates that current transport in the grain boundary region of the studied cell is controlled by recombination at a high density of defect states in this region.

Furthermore, Table 3 clearly shows that illumination of the cell does not lead to large changes in diode parameters (with the exception of the photo-current I_{ph}). This is in line with the relatively ideal behavior of silicon solar cells concerning their stability under illumination. Nevertheless, there is a slight decrease in the parameters of D_1 (I_{01}, n_1), which could be attributed to a deactivation of recombination defects in the gap by light irradiance through the higher quasi-Fermi level under light. This slight decrease in diode parameters was also found for some thin film $Cu(In,Ga)Se_2$ cells [27]. On the other hand, there is a slight increase in the parameters of D_2 (I_{02}, n_2) with increasing illumination level, which could be attributed to an increase in number of effective grain boundary recombination defects in a similar manner to interface recombination presented earlier [19]. It is worth mentioning that the change in diode parameters of D_2 (I_{02}, n_2) due to illumination is far less than the change found for the $CuGaSe_2$ cell presented in Refs. [20,22]. Moreover, values of R_{s2} are approximately an order of magnitude higher than those of R_s, in line with the higher resistivity at grain boundaries [10].

Furthermore, the method presented in Ref. [9] is used to calculate the fraction of photo-current needed to compensate for the loss current of each mechanism under open circuit condition. Fig. 4 shows the equivalent circuit for the cell under open circuit condition, where I_{c1}, I_{c2} and I_{c3} are the compensation currents in the three branches, whose sum equals the cell photo-current (I_{ph} in Fig. 1).

Table 4 summarizes the calculated compensation currents I_{c1}, I_{c2} and I_{c3} for the three branches in Fig. 4 depending on illumination level. The last column in Table 4 contains the value of the ratio of recombination current to cell photo-current $r=I_{c2}/I_{ph}$. This parameter is practically the same as the parameter denoted also as r in Ref. [4]. There, it represented the ratio of recombination area to the whole cell area and was considered a fitting parameter. It is worth mentioning that applying the separation method presented in Ref. [9] would lead to a reduction in the number of fitting parameters by one without losing any information.

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Table 3
Diode parameters of the analyzed multi-crystalline silicon solar cell determined for different illumination levels using Eq. (1). The quantities I_{ill}, I_{ph}, n_1, n_2, I_{01}, I_{02}, R_s and R_{sh} represent illumination level, photo-current, diode ideality factors of D_1 and D_2, saturation currents of D_1 and D_2, series resistance and shunt resistance, respectively. R_{s2} is an additional series resistance connected to D_2.

I_{ill} (mW/cm^2)	R_{sh} (Ω)	R_{s2} (Ω)	R_s (Ω)	n_2	I_{02} (A)	n_1	I_{01} (A)	I_{ph} (A)
20	471.9	1.386	0.173	3.096	1.866E−4	1.361	6.473E−9	3.949E−2
14.5	510.6	1.462	0.170	3.065	1.806E−4	1.376	7.695−9	2.859E−2
9.84	481.8	1.493	0.168	3.034	1.716E−4	1.384	8.370E−9	1.942E−2
6.20	500.5	1.582	0.167	2.999	1.660E−4	1.395	9.479E−9	1.225E−2
3.47	501.6	1.603	0.167	2.975	1.592E−4	1.340	9.879E−9	6.844E−3
1.66	516.4	1.626	0.166	2.968	1.572E−4	1.405	1.049E−8	3.283E−3
0.58	530.5	1.643	0.166	2.958	1.540E−4	1.409	1.090E−8	1.144E−3
0.10	543.5	1.652	0.166	2.949	1.512E−4	1.410	1.107E−8	2.045E−4
0 (dark)	568.3	1.643	0.165	2.949	1.491E−4	1.411	1.117E−8	0

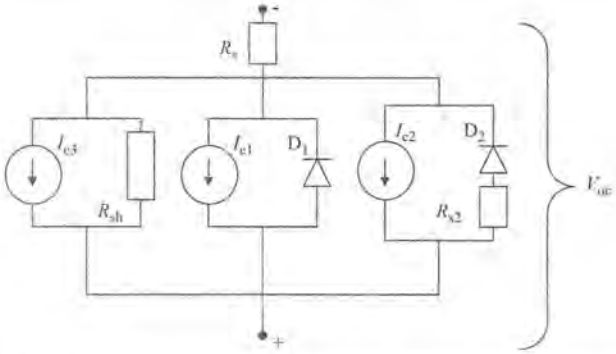


Fig. 4. Modified two-diode equivalent circuit under open circuit condition. I_{c1}, I_{c2} and I_{c3} are the compensation currents in the three branches, whose sum equals the cell photo-current (I_{ph} in Fig. 1).

Table 4
Calculated compensation currents I_{c1}, I_{c2} and I_{c3} for the three branches in Fig. 4 depending on illumination level I_{ill}. The quantity I_{ph} is cell photo-current and r is the recombination current ratio.

I_{ill} (mW/cm^2)	I_{ph} (A)	I_{c1} (A)	I_{c2} (A)	I_{c3} (A)	$r=I_{c2}/I_{ph}$
20	3.949E−2	3.67E−3	3.47E−2	9.96E−4	0.88
14.5	2.859E−2	1.62E−3	2.64E−2	8.48E−4	0.92
9.84	1.942E−2	5.38E−4	1.82E−2	8.20E−4	0.94
6.20	1.225E−2	1.34E−4	1.14E−2	6.85E−4	0.93
3.47	6.844E−3	5.39E−5	6.22E−3	5.88E−4	0.91
1.66	3.283E−3	4.20E−6	2.83E−3	4.31E−4	0.86
0.58	1.144E−3	6.91E−7	8.70E−4	2.65E−4	0.76
0.10	2.045E−4	6.40E−8	1.05E−4	8.10E−5	0.51

For a better illustration, the three compensation currents I_{c1}, I_{c2} and I_{c3} are presented in Fig. 5 versus cell photo-current. It is readily seen in this figure that while I_{c2} remains of the same order of magnitude as I_{ph} over the range of 3 decades, I_{c1} goes through 5 orders of magnitude and remains always below I_{c2} in that range. The value of I_{c3} indicates the beginning of a saturation behavior, and even a linear fit of I_{c3} shows that at standard illumination level only a small fraction of I_{ph} is needed to compensate for the cell shunt current. On the other hand, extrapolating the behavior of I_{c1} and I_{c2} to standard illumination level (as seen in Fig. 5) would result in I_{c1} and I_{c2} being of the same order of magnitude. This would be in accordance with what was found in Ref. [4], namely, the value of r between 0.35 and 0.74, meaning that diffusion current and recombination current are of the same order of magnitude. From Table 4, it is also clear that at very low illumination levels the main competition to compensate for the generated photo-current is between recombination current in the

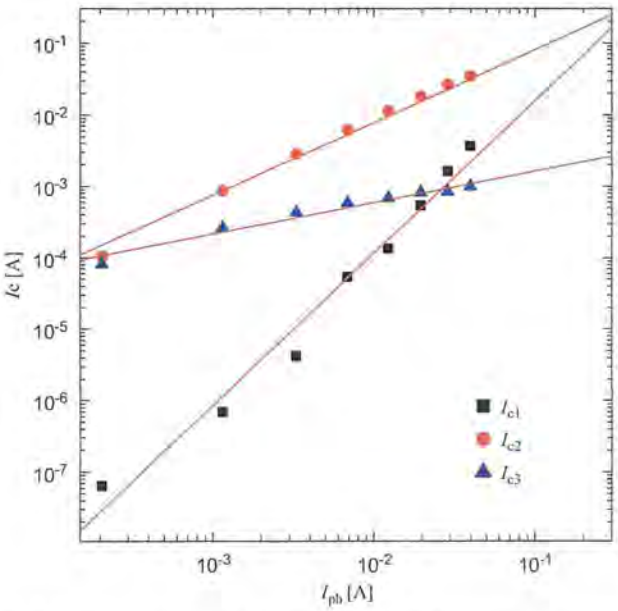


Fig. 5. Compensation currents I_{c1}, I_{c2} and I_{c3} versus cell photo-current I_{ph}. Linear best fits are also drawn for all three curves. At standard illumination level (at which $I_{ph} \approx 0.2$ A for the studied cell) I_{c3} remains relatively small, while I_{c1} and I_{c2} become of the same order of magnitude.

grain boundary region and shunt current, while at higher levels the competition is mainly between recombination at grain boundaries and recombination within crystallites.

From the parameters (I_0 and n) of each diode, it can be stated that diode D_1 is more favorable to good cell performance than diode D_2. Assigning the first mechanism to the crystalline region and the second one to the grain boundary region makes it straightforwardly understandable that an enlargement of crystallite size will directly enhance cell performance [28].

5. Conclusion

A modified two-diode equivalent circuit accounting for an additional ohmic series resistance in the vicinity of grain boundaries was proposed in order to accurately describe current–voltage characteristics of multi-crystalline silicon solar cells, especially under low illumination levels. The model allows for variable ideality factors, resulting in a more precise insight into current transport mechanisms. Two mechanisms were found to dominate current transport at low illumination levels: recombination in the crystalline region and recombination at

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grain boundaries. At very low illumination levels, the main competition to compensate for the generated photo-current is between shunt current and recombination current in the grain boundary region. Furthermore, the clear assignment of one branch of the equivalent circuit to the grain boundary region enables the evaluation of the influence of grain boundaries on solar cell performance.

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Novel method for preparation of interdigitated back contacted a-Si:H/c-Si heterojunction solar cells

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NOVEL METHODE FOR PREPARATION OF INTERDIGITATED BACK CONTACTED a-Si:H/c-Si HETEROJUNCTION SOLAR CELLS

Maximilian Scherff
Q-Cells SE, Sonnenallee 17-21, 06766 Bitterfeld-Wolfen OT Thalheim, Germany m.scherff@q-cells.com

ABSTRACT: We present a **novel method for structuring** Emitter and BSF areas **of interdigitated back contacted silicon heterojunction solar cells** (IBC-HJ). The **method combines** the **benefits of in-line capability** with **vacuum processes only**, **reusable masks**, **self alignment** and furthermore an easy and **extreme safe wafer handling**. It is based on plasma etching of passivation layers and a following layer deposition procedure via openings in a **mechanical masking**. The exceptional way how the reusable masks are attached to the sample provides accurate masking over large area. By overlaying two masks the wafer can remain underneath the lower masking, which also works as a sample holder during all the structuring steps while, if necessary, the upper mask is exchanged for each particular process step. This provides an **extreme safe wafer handling** along all the IBC-HJ specific process steps, highly recommended **for very thin wafers**. This allows processing the different layers (e.g. emitter, BSF, TCO, metal) structures without the need to touch the wafer after each step. Furthermore a **mechanical self aligning** of the mask-stacks can be applied in mass production. First test structures are shown and cost estimation for IBC-HJ solar cells is presented.
Keywords: heterojunction, IBC, a-Si/c-Si

1 Introduction

IBC-HJ solar cells have a very high efficiency potential of more than 24% on p-type [1]. and more than 25% on n-type, respectively [2]. They combine the most efficient silicon solar cell technologies available on the market, namely the interdigitated back contacted back junction solar cell known from SUNPOWER and the HIT solar cell from SANYO. The IBC-HJ cell structure consists of a contactless and well passivated front side with any kind of light capturing features. On the back side the highly diffused emitter and BSF areas are substituted by the amorphous/crystalline silicon (*a*-Si:H/*c*-Si) heterojunction contact structures (figure 1), which are deposited at temperatures of less than 200°C. These *a*-Si:H/*c*-Si structures are very low recombinative and cause the very high voltages potential of these kind of cell. During the last years a rapid efficiency increase with an actual maximum of 20,2% [3] and 22,2% [10] is observed. Different approaches how to structure the emitter and base contacts of silicon heterojunction (HJ) contact patterns on the cell rear side are known: a) with photolithography like in [1] or like in the RECASH or PRECASH method [5], b) with screen printing a resist plus etching steps [6], c) by putting a hard mask on the sample like in the BEHIND procedure [7], or by using a hard mask in small distance to the sample [8].

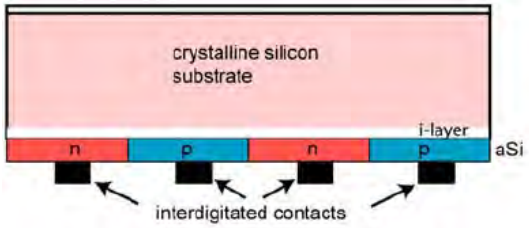


Figure 1: Side cut of a common IBC-HJ solar cell [4].

The first two production methods (a, b) suffer from the unpleasant procedures like depositing and hardening plus in the case of photolithography illuminating and developing a resist, as well as etching of the uncovered areas and wet chemically removing the resist. All these steps are associated to unfortunate handling steps and switching between in-line and batch procedures. This kind of processing is expensive and rather uncomfortable for very thin substrates (e.g. 100µm thickness). Furthermore, wet chemical residuals have to be carefully removed from the wafer surface since they would be located in the very sensitive space charge region of the heterojunction contacts and would strongly reduce the performance of the final device. All these aspects are cost effective.

The BEHIND concept benefits from the cheap and reusable mask as well as form the high V_{OC} potential (695mV) due to the full area emitter deposition in the beginning of the procedure [5]. On the other hand it suffers from accurate mask adjustment after the first structuring step. Furthermore in mass production a hard mask tends to mechanically damage the thin underlying passivation or heterojunction layers due to local mechanical contact. Also problems can appear due to plasma penetration below the mask if the sample or the mask is not flat or deformed by continuous use. Later on in figure 5 a comparable process flow (BEHIND-like) is presented, which uses the stacked masks and the novel method with foils.

The mentioned problem of plasma penetration below the mask turns up extremely by keeping the mask in small distance to the sample like presented in [8]. The effect is very sensitive to the applied distance and does not allow exact structuring as penetration of the plasma below the mask appears everywhere and is detrimental to the cell performance.

2 Cell processing using the novel method:

The new approach combines the benefits of in-line capability with vacuum processes only, reusable masks, self alignment plus easy and save wafer handling. It is based on a plasma etching and layer deposition procedure via openings in stacks of mechanical masks. The procedure how the reusable masks are attached to the sample provides accurate masking over large areas. By using this thin films instead of thick hard masks surface damage is avoided, especially if the film is soft or a soft coat is applied. Furthermore plasma penetration below the mask, due to incomplete proximity of the mask to the wafer, is avoided. This proximity is achieved by using a non-planar holder with a curved surface, on which the

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cell precursor is bended by pressing the tensed mask onto it.

In the following three different kinds of samples and an exemplary process flow are presented. First *a*-Si:H structures which were deposited and etched via one mask. Then transparent conductive oxide (TCO) layers are deposited via this mask. Afterwards an exemplary process flow is presented and finally a structure is shown, which uses a stack of masks, where the upper masks are exchanged for emitter and BSF structures, respectively.

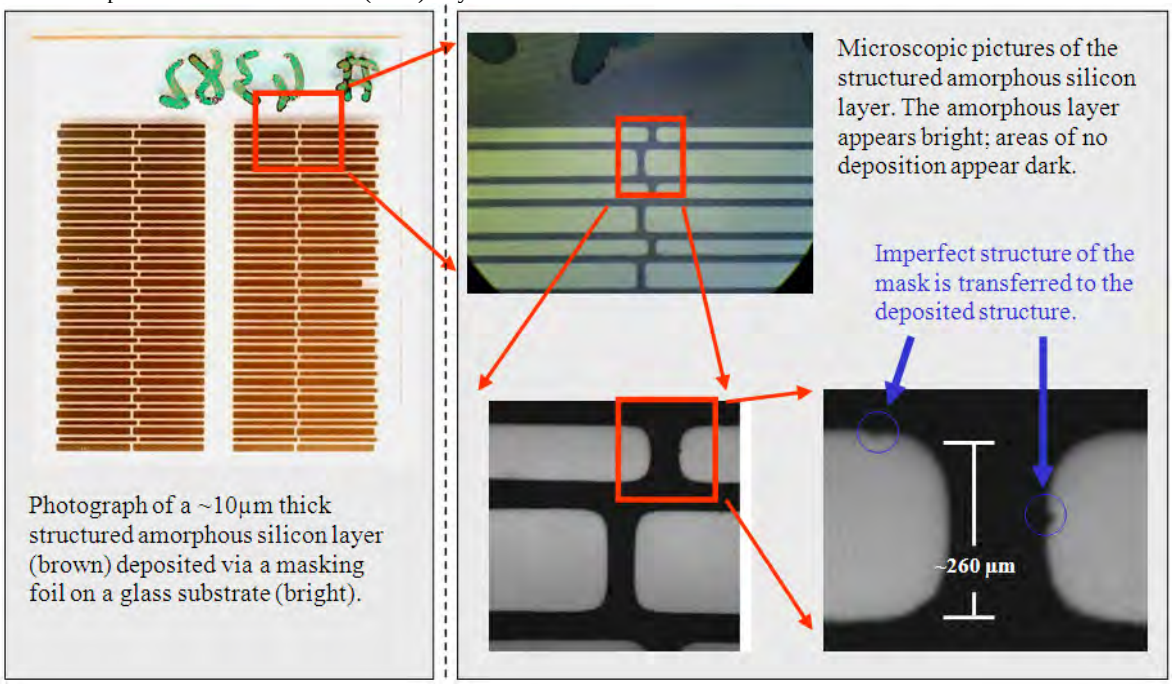


Figure 2: Structured *a*-Si:H layer deposited through a flexible mask according to the novel method.

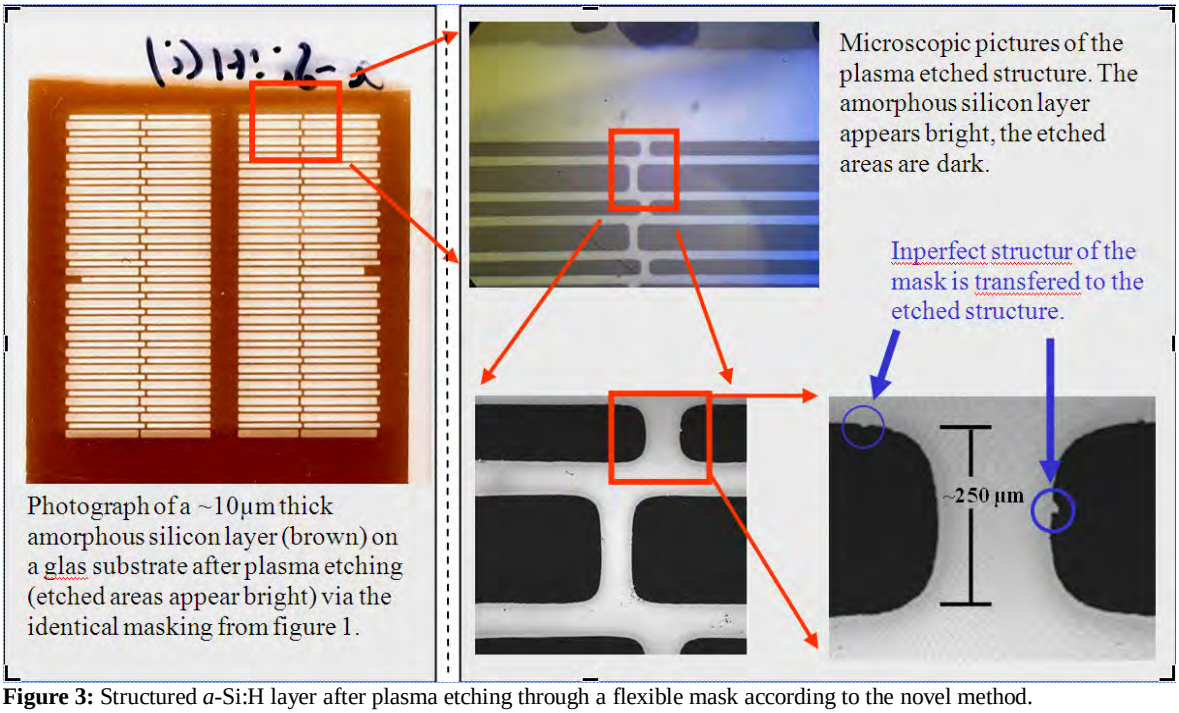


Figure 3: Structured *a*-Si:H layer after plasma etching through a flexible mask according to the novel method.

2.1 Test sample using one mask

As test sample a ~10µm thick amorphous silicon layers is shown, which was deposited through openings in a flexible mask onto a glass substrate according to the novel method (in figure 2). The *a*-Si:H was deposited in a standard parallel plate PECVD setup at an excitation frequency of 13.56MHz. Due to the absorption of the *a*-Si:H in the wavelength range up to 600nm the layer appears brown. Even very thin layers are easily visible. The abrupt borderline is visible, which even properly transfers imperfections of the mask openings to the deposited layer structure (lower right picture in figure 2).

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Furthermore no parasitic deposition can be observed all over the sample area. Please note that the thickness of the used amorphous layers is three orders of magnitude thicker than used in a-Si:H/c-Si structures.

In figure 3 first a ~10µm thick full area amorphous silicon layer was deposited on a glass. Afterwards plasma etching was applied through openings of the identical flexible mask used above. Once more one can see the abrupt borderline which perfectly transfers the imperfections of the mask openings to the etched layer structure (lower right picture in figure 2). No parasitic etching is observed all over the sample area.

The width of the deposited and etched test structures are ~250µm and ~450µm with a pitch of 1mm. These dimensions are more than adequate for IBC solar cells.

To have an idea of the steepness of the edges at the borderline of the prepared structures two 3D scans were prepared with a confocal microscope. As shown in figure 4 (left) the shape of the plasma etched step is perfectly perpendicular with no any rounding of the edge neither under etching of the mask. Furthermore the deposited *a*-Si:H layer (right) shows a well defined structure with slightly rounded edges.

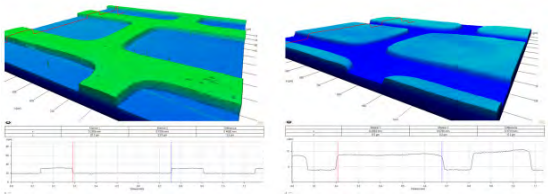


Figure 4: Topographies of the structured deposited *a*-Si:H layers shown in figure 1 (right) and etched *a*-Si:H layer after plasma etching from figure 2 (left) prepared by a confocal microscope.

2.2 TCO deposited via the mask

Usually the thin silicon layers of a-Si:H/c-Si HJ structures are covered with TCO to provide an anti reflection coating, and low ohmic contacts to the metallization, for light confinement, and to increase the lateral conductivity of the layer stack. In figure 4 80nm of indium tin oxide (standard used TCO) was deposited through the flexible mask onto a silicon wafer. Once more the shape of the mask is well defined and no any parasitic deposition occurs.

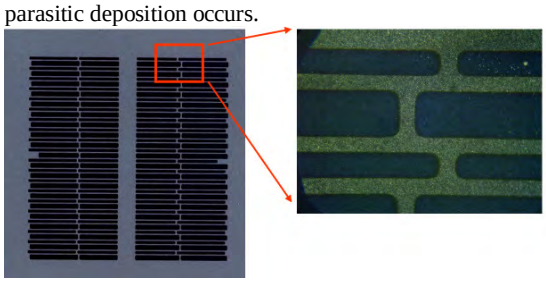


Figure 4: Photograph (left) and microscopic picture (right) of a ~80nm thick structured indium tin oxid (ITO) layer (dark/blue) deposited via a masking foil on a silicon wafer (grey).

2.3 Novel method using two stacked masks

By overlaying two masks the wafer can remain underneath the lower mask (blue mask in figure 5), which provides all the openings used in the two different upper masks (grey and brown in figure 5). During the complete process flow the upper masks are exchanged while the lower mask stays unmoved. In this example (figure 5) a BEHIND-like process flow is used in which two upper masks, for producing the BSF layer and the TCO, are involved. This technique allows processing the different structures without the need to touch the wafer after each step and consequently provides an extreme save wafer handling during all IBC-HJ specific process steps, what is highly recommended for very thin substrates of future technologies. Please note, that with the BEHIND process 695mV and high parallel resistances were archived.

2.4 Cell precursor with dielectric rear side

One sample prepared with this technology but with a different process flow to figure 5 is shown in figure 6. An oxidized (100nm) wafer was covered by two stacked masks, then local areas were opened and the first HJ layer stack was deposited (e.g. the emitter). Afterwards the upper mask was exchanged and the second HJ layer stack

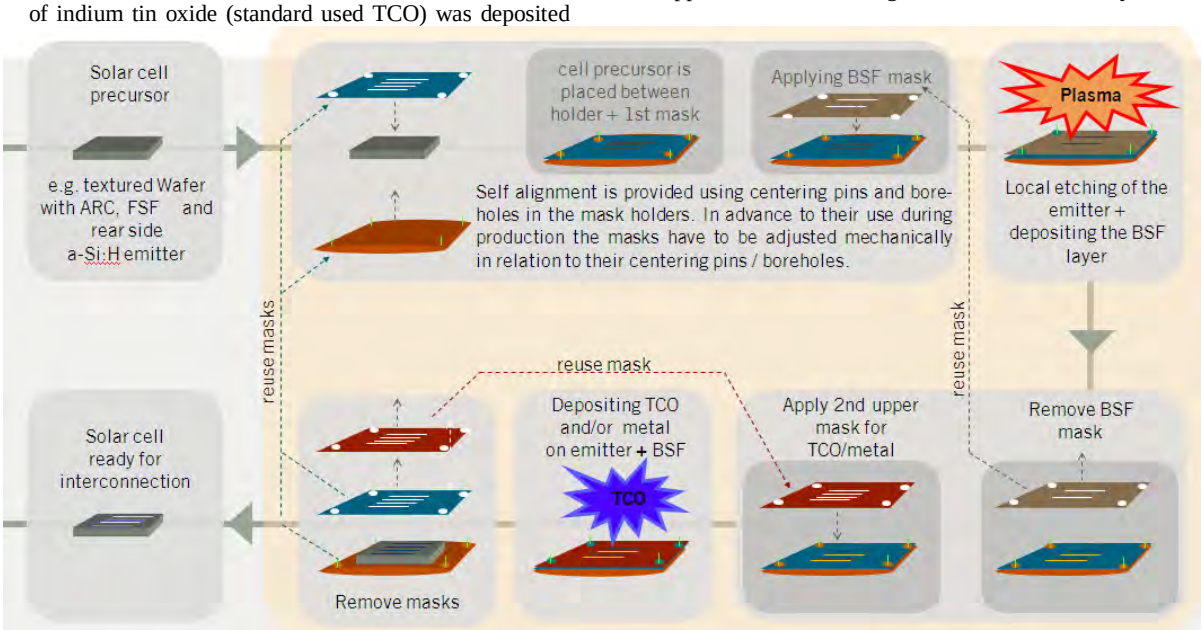


Figure 5: Example of one possible process flow using a BEHIND-like [5] procedure to prepare the structured *a*-Si:H layers.

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(e.g. the BSF) was deposited into the prior plasma etched openings. A well defined IBC structure is produced, which congruence is sufficient for this kind of cell type anyway.

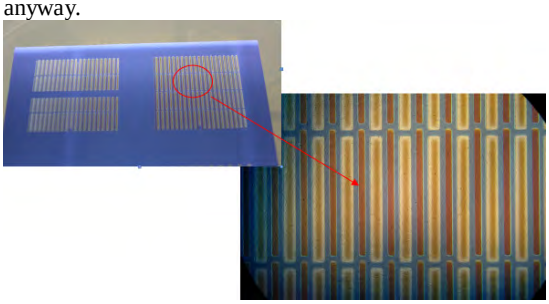


Figure 6: Photograph (left) and microscopic picture (right) of an oxidized silicon wafer after separate plasma etching the oxide and subsequent depositing of amorphous layers. Two stacked masks were used.

2.5 Self alignments of stacked masks

The processing procedure can be provided with a self aligning of the mask-stacks in mass production. Thus during the process flow the lower mask keeps it position relatively to the sample, only the position of the upper mask relative to the lower mask have to be adjusted.

This adjustment can be applied mechanically by using centering pins and boreholes in the mask holders (frame which holds the flexible mask). In advance to their use during the production process the masks have to be adjusted mechanically in relation to their centering pins and boreholes, respectively. In the production process the masks are adjusted automatically when they are put on the centering pins. This procedure provides sufficient accuracy.

3 Process cost estimation

The cost estimation for the specific process steps of the novel method is based on a multiple 100MW mass production for 6" wafers and a depreciation time for equipment of 5 years as well as for building and infrastructure etc. of 10 years.

The costs are calculated by using a Cost of Ownership (CoO) tool which has been developed at Q-Cells and is originally used for comparing process equipment of different suppliers for the same process step. It is a Windows-Excel based calculation which considers not only the equipment investment but also all aspects of a later date usage. Labor and maintenance costs are involved as well as operation materials and consumables. One result of the calculation is the overall equipment efficiency since the tool determines the net capacity of the equipment. This net capacity has a relevant influence on the wafer costs. As result the specific costs per wafer for a certain process step and equipment are obtained.

The exemplary CoO estimation is based on the process flow of figure 6 and starts with n-type silicon cell precursor with optical and electrical optimized front side (e.g. front surface field, front side silicon surface passivation, anti reflective coating). The deposition of the amorphous silicon emitter on the back side including an adequate wet chemical cleaning step previous to the layer depositions is calculated to 10,6 ct per 6" wafer (wa). The structured plasma etching followed by the HJ-BSF deposition is 14,4 ct/wa (figure 8) and the final TCO and/or metal deposition (in sum ~75nm) is estimated to 10,9 ct/wa. All this costs are distributed like presented in figure 9. The cost drivers are the estimated invest and the estimated reduced throughput due to prolonged vacuum pump down. In sum the process cost for the complete procedure excluding cost for preparing the precursor is 36,3 ct/wafer. As the cells bear of highly conductive metallisation the current collection should be shifted to the cell interconnection level e.g. like described in Patent DE 102008043833 A1.

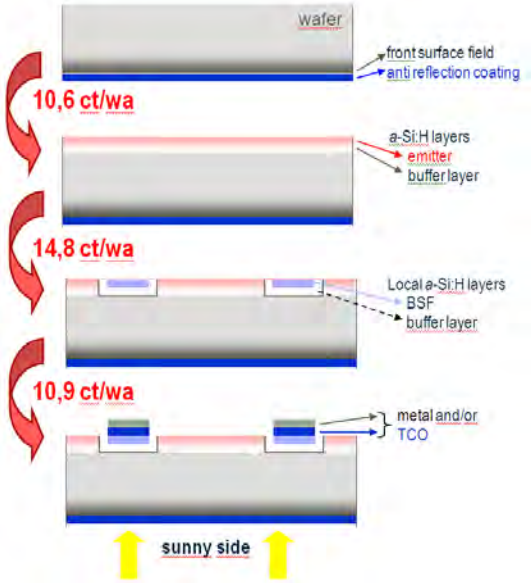


Figure 8: Estimated cost per wafer for IBC-HJ solar cells produced according to the flow of figure 5.

The CoO is based on equipment cost of 2009, is calculated for a first pilot production line and excludes further cost reduction potentials. Furthermore the net capacity can be improved. Due to this the expected process cost will be significantly lower.

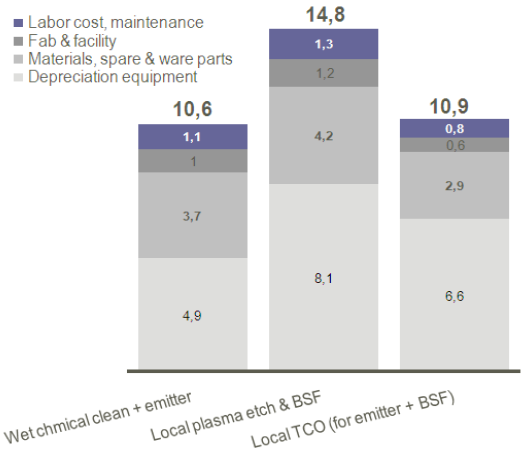


Figure 9: Cost distribution for the process flow of figure 5 excluding cost for preparing the cell precursor.

4 Conclusion

A new technique for preparing IBC-HJ solar cells is presented. Instead of lithographical processes it works with reusable masks or stacks of masks. These are softly

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attached to the sample surface in an exceptional way, which guarantees a dense proximity over large areas. By using stacks of masks an extreme save wafer handling for very thin wafers without touching the samples after each step is guaranteed and easy mechanical self aligning can be provided. The cell process cost are estimated to 36,3 ct/wa for the specific processes.
This technology is subject of the international patent family [10]. Q-Cells offer non-exclusive licenses to potentially interested companies. For more information please contact:
r.paugstadt@q-cells.com (licening),
m.scherff@q-cells.com (tecnical information)

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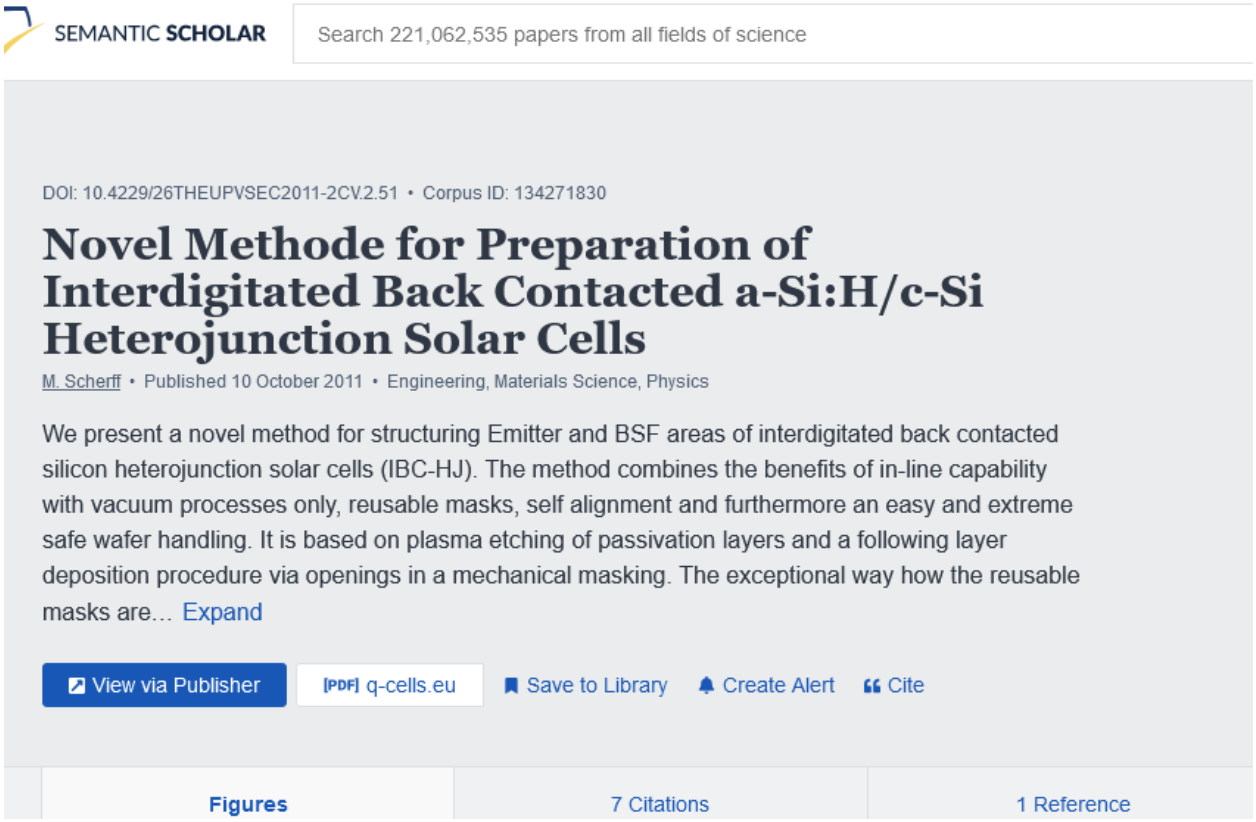
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Attachment I-2

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Attachment I-3

NOVEL METHODE FOR PREPARATION OF INTERDIGITATED BACK CONTACTED a-Si:H/c-Si HETEROJUNCTION SOLAR CELLS

Maximilian Scherff
Q-Cells SE, Sonnenallee 17-21, 06766 Bitterfeld-Wolfen OT Thalheim, Germany m.scherff@q-cells.com

ABSTRACT: We present a **novel method for structuring** Emitter and BSF areas **of interdigitated back contacted silicon heterojunction solar cells** (IBC-HJ). The **method combines** the **benefits of in-line capability** with **vacuum processes only**, **reusable masks**, **self alignment** and furthermore an easy and **extreme safe wafer handling**. It is based on plasma etching of passivation layers and a following layer deposition procedure via openings in a **mechanical masking**. The exceptional way how the reusable masks are attached to the sample provides accurate masking over large area. By overlaying two masks the wafer can remain underneath the lower masking, which also works as a sample holder during all the structuring steps while, if necessary, the upper mask is exchanged for each particular process step. This provides an **extreme safe wafer handling** along all the IBC-HJ specific process steps, highly recommended **for very thin wafers**. This allows processing the different layers (e.g. emitter, BSF, TCO, metal) structures without the need to touch the wafer after each step. Furthermore a **mechanical self aligning** of the mask-stacks can be applied in mass production. First test structures are shown and cost estimation for IBC-HJ solar cells is presented.
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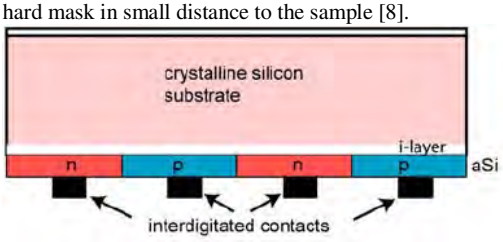


Figure 1: Side cut of a common IBC-HJ solar cell [4].

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cell precursor is bended by pressing the tensed mask onto it.

In the following three different kinds of samples and an exemplary process flow are presented. First *a*-Si:H structures which were deposited and etched via one mask. Then transparent conductive oxide (TCO) layers are deposited via this mask. Afterwards an exemplary process flow is presented and finally a structure is shown, which uses a stack of masks, where the upper masks are exchanged for emitter and BSF structures, respectively.

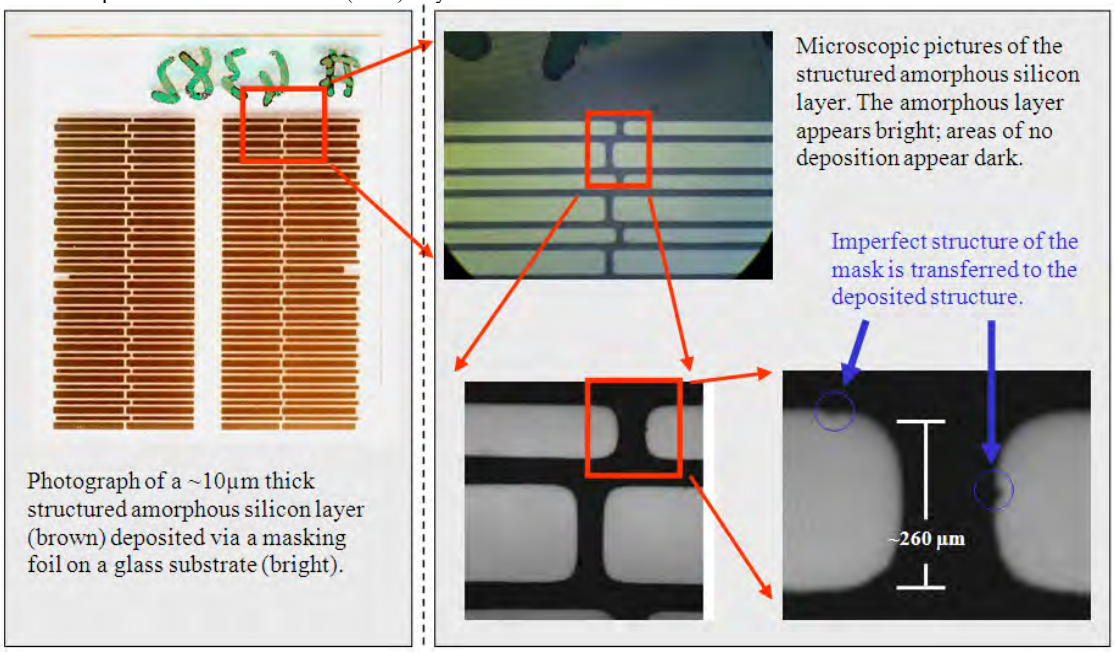


Figure 2: Structured *a*-Si:H layer deposited through a flexible mask according to the novel method.

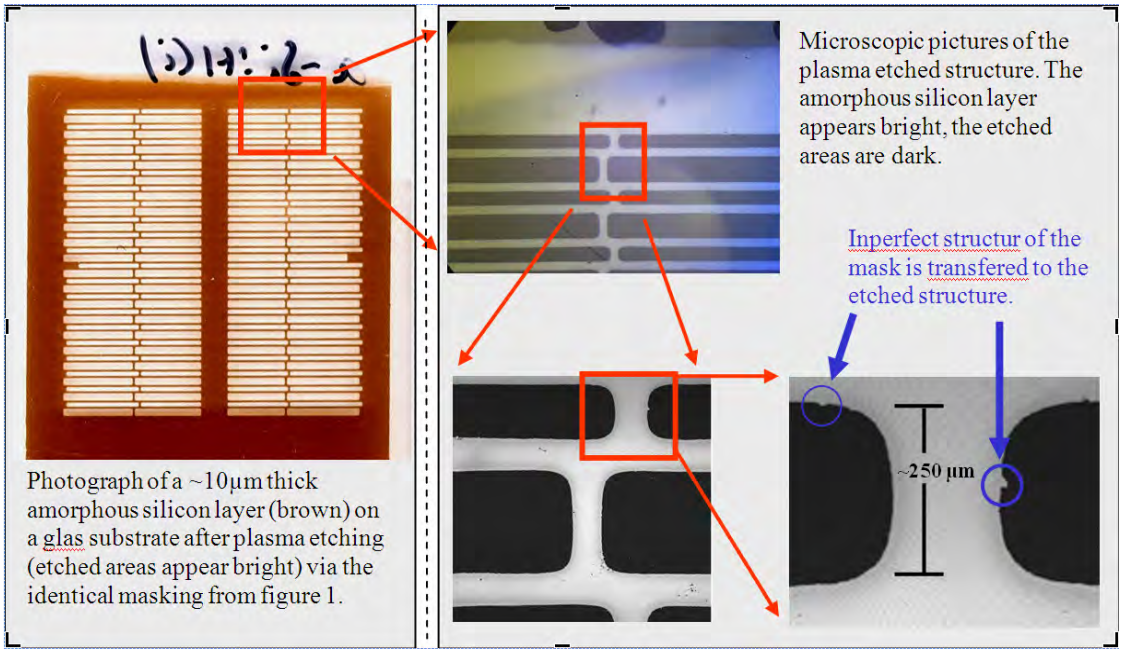


Figure 3: Structured *a*-Si:H layer after plasma etching through a flexible mask according to the novel method.

2.1 Test sample using one mask

As test sample a ~10µm thick amorphous silicon layers is shown, which was deposited through openings in a flexible mask onto a glass substrate according to the novel method (in figure 2). The *a*-Si:H was deposited in a standard parallel plate PECVD setup at an excitation frequency of 13.56MHz. Due to the absorption of the *a*-Si:H in the wavelength range up to 600nm the layer appears brown. Even very thin layers are easily visible. The abrupt borderline is visible, which even properly transfers imperfections of the mask openings to the deposited layer structure (lower right picture in figure 2).

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Furthermore no parasitic deposition can be observed all over the sample area. Please note that the thickness of the used amorphous layers is three orders of magnitude thicker than used in a-Si:H/c-Si structures.

In figure 3 first a ~10µm thick full area amorphous silicon layer was deposited on a glass. Afterwards plasma etching was applied through openings of the identical flexible mask used above. Once more one can see the abrupt borderline which perfectly transfers the imperfections of the mask openings to the etched layer structure (lower right picture in figure 2). No parasitic etching is observed all over the sample area.

The width of the deposited and etched test structures are ~250µm and ~450µm with a pitch of 1mm. These dimensions are more than adequate for IBC solar cells.

To have an idea of the steepness of the edges at the borderline of the prepared structures two 3D scans were prepared with a confocal microscope. As shown in figure 4 (left) the shape of the plasma etched step is perfectly perpendicular with no any rounding of the edge neither under etching of the mask. Furthermore the deposited *a*-Si:H layer (right) shows a well defined structure with slightly rounded edges.

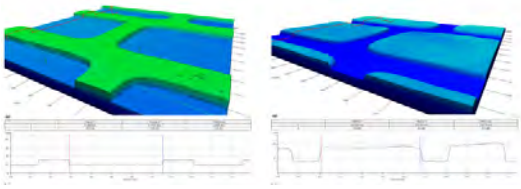


Figure 4: Topographies of the structured deposited *a*-Si:H layers shown in figure 1 (right) and etched *a*-Si:H layer after plasma etching from figure 2 (left) prepared by a confocal microscope.

2.2 TCO deposited via the mask

Usually the thin silicon layers of a-Si:H/c-Si HJ structures are covered with TCO to provide an anti reflection coating, and low ohmic contacts to the metallization, for light confinement, and to increase the lateral conductivity of the layer stack. In figure 4 80nm of indium tin oxide (standard used TCO) was deposited through the flexible mask onto a silicon wafer. Once more the shape of the mask is well defined and no any parasitic deposition occurs.

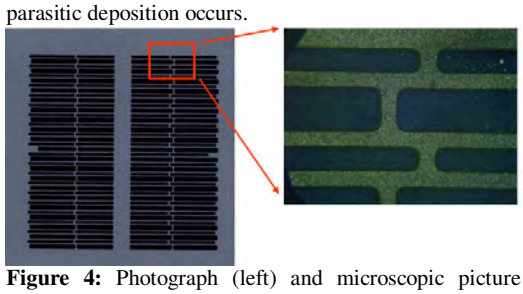


Figure 4: Photograph (left) and microscopic picture (right) of a ~80nm thick structured indium tin oxid (ITO) layer (dark/blue) deposited via a masking foil on a silicon wafer (grey).

2.3 Novel method using two stacked masks

By overlaying two masks the wafer can remain underneath the lower mask (blue mask in figure 5), which provides all the openings used in the two different upper masks (grey and brown in figure 5). During the complete process flow the upper masks are exchanged while the lower mask stays unmoved. In this example (figure 5) a BEHIND-like process flow is used in which two upper masks, for producing the BSF layer and the TCO, are involved. This technique allows processing the different structures without the need to touch the wafer after each step and consequently provides an extreme save wafer handling during all IBC-HJ specific process steps, what is highly recommended for very thin substrates of future technologies. Please note, that with the BEHIND process 695mV and high parallel resistances were archived.

2.4 Cell precursor with dielectric rear side

One sample prepared with this technology but with a different process flow to figure 5 is shown in figure 6. An oxidized (100nm) wafer was covered by two stacked masks, then local areas were opened and the first HJ layer stack was deposited (e.g. the emitter). Afterwards the upper mask was exchanged and the second HJ layer stack

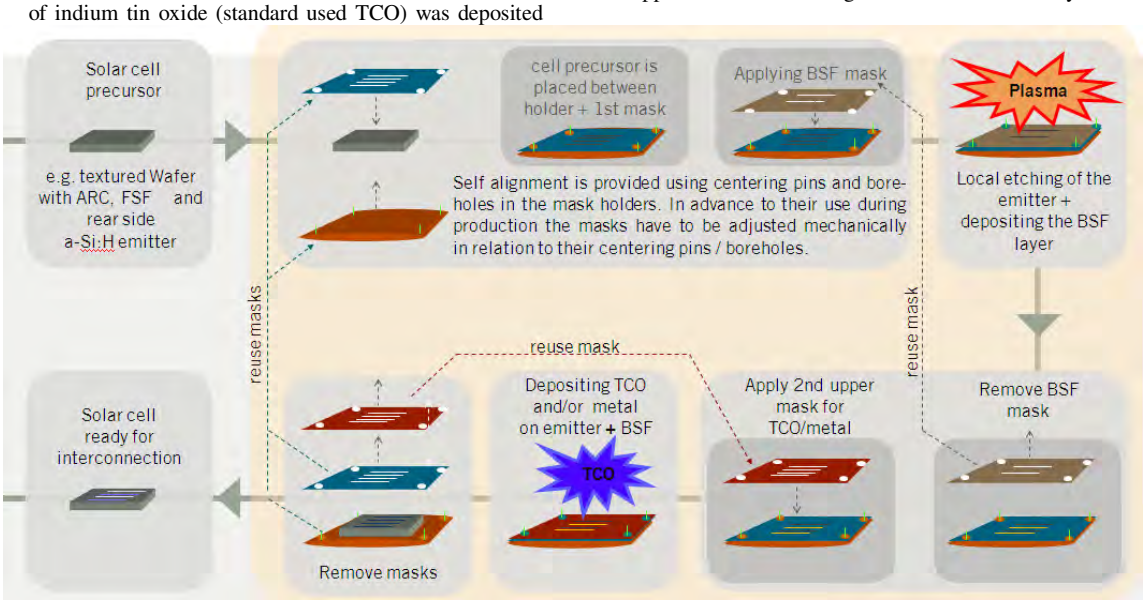


Figure 5: Example of one possible process flow using a BEHIND-like [5] procedure to prepare the structured *a*-Si:H layers.

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(e.g. the BSF) was deposited into the prior plasma etched openings. A well defined IBC structure is produced, which congruence is sufficient for this kind of cell type anyway.

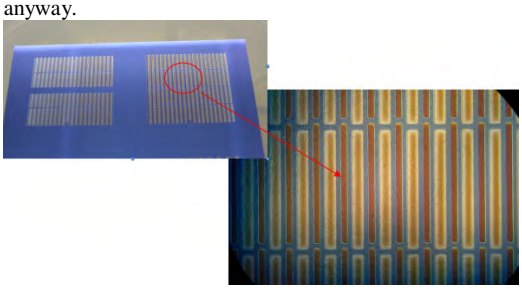


Figure 6: Photograph (left) and microscopic picture (right) of an oxidized silicon wafer after separate plasma etching the oxide and subsequent depositing of amorphous layers. Two stacked masks were used.

2.5 Self alignments of stacked masks

The processing procedure can be provided with a self aligning of the mask-stacks in mass production. Thus during the process flow the lower mask keeps it position relatively to the sample, only the position of the upper mask relative to the lower mask have to be adjusted.

This adjustment can be applied mechanically by using centering pins and boreholes in the mask holders (frame which holds the flexible mask). In advance to their use during the production process the masks have to be adjusted mechanically in relation to their centering pins and boreholes, respectively. In the production process the masks are adjusted automatically when they are put on the centering pins. This procedure provides sufficient accuracy.

3 Process cost estimation

The cost estimation for the specific process steps of the novel method is based on a multiple 100MW mass production for 6" wafers and a depreciation time for equipment of 5 years as well as for building and infrastructure etc. of 10 years.

The costs are calculated by using a Cost of Ownership (CoO) tool which has been developed at Q-Cells and is originally used for comparing process equipment of different suppliers for the same process step. It is a Windows-Excel based calculation which considers not only the equipment investment but also all aspects of a later date usage. Labor and maintenance costs are involved as well as operation materials and consumables. One result of the calculation is the overall equipment efficiency since the tool determines the net capacity of the equipment. This net capacity has a relevant influence on the wafer costs. As result the specific costs per wafer for a certain process step and equipment are obtained.

The exemplary CoO estimation is based on the process flow of figure 6 and starts with n-type silicon cell precursor with optical and electrical optimized front side (e.g. front surface field, front side silicon surface passivation, anti reflective coating). The deposition of the amorphous silicon emitter on the back side including an adequate wet chemical cleaning step previous to the layer depositions is calculated to 10,6 ct per 6" wafer (wa). The structured plasma etching followed by the HJ-BSF deposition is 14,4 ct/wa (figure 8) and the final TCO and/or metal deposition (in sum ~75nm) is estimated to 10,9 ct/wa. All this costs are distributed like presented in figure 9. The cost drivers are the estimated invest and the estimated reduced throughput due to prolonged vacuum pump down. In sum the process cost for the complete procedure excluding cost for preparing the precursor is 36,3 ct/wafer. As the cells bear of highly conductive metallisation the current collection should be shifted to the cell interconnection level e.g. like described in Patent DE 102008043833 A1.

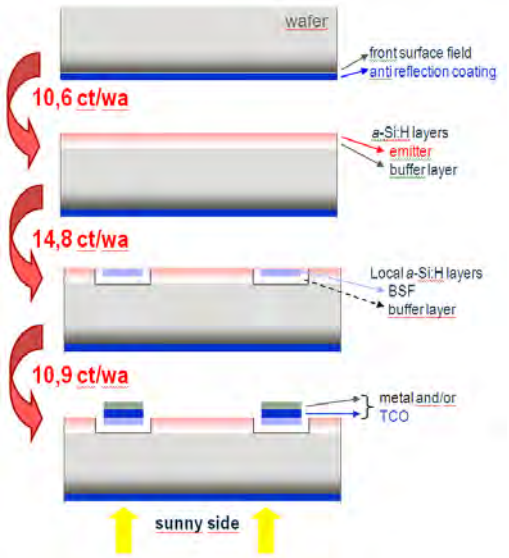


Figure 8: Estimated cost per wafer for IBC-HJ solar cells produced according to the flow of figure 5.

The CoO is based on equipment cost of 2009, is calculated for a first pilot production line and excludes further cost reduction potentials. Furthermore the net capacity can be improved. Due to this the expected process cost will be significantly lower.

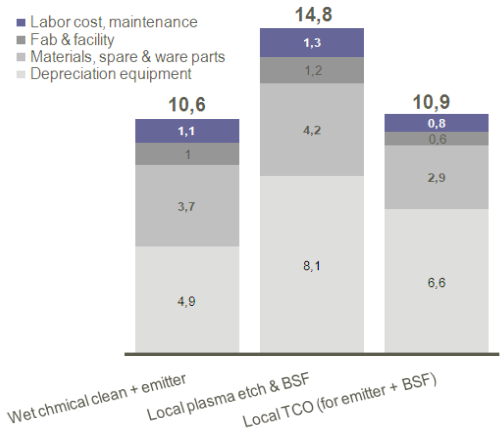


Figure 9: Cost distribution for the process flow of figure 5 excluding cost for preparing the cell precursor.

4 Conclusion

A new technique for preparing IBC-HJ solar cells is presented. Instead of lithographical processes it works with reusable masks or stacks of masks. These are softly

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attached to the sample surface in an exceptional way, which guarantees a dense proximity over large areas. By using stacks of masks an extreme save wafer handling for very thin wafers without touching the samples after each step is guaranteed and easy mechanical self aligning can be provided. The cell process cost are estimated to 36,3 ct/wa for the specific processes.
This technology is subject of the international patent family [10]. Q-Cells offer non-exclusive licenses to potentially interested companies. For more information please contact:
r.paugstadt@q-cells.com (licening),
m.scherff@q-cells.com (tecnical information)

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[10] DE10200604261B4, EP000002062300A2, JP002010503222A, WO002008040273A3, US000007943416B2.

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Attachment I-4

NOVEL METHODE FOR PREPARATION OF INTERDIGITATED BACK CONTACTED a-Si:H/c-Si HETEROJUNCTION SOLAR CELLS

Maximilian Scherff
Q-Cells SE, Sonnenallee 17-21, 06766 Bitterfeld-Wolfen OT Thalheim, Germany m.scherff@q-cells.com

ABSTRACT: We present a **novel method for structuring** Emitter and BSF areas **of interdigitated back contacted silicon heterojunction solar cells** (IBC-HJ). The **method combines** the **benefits of in-line capability** with **vacuum processes only**, **reusable masks**, **self alignment** and furthermore an easy and **extreme safe wafer handling**. It is based on plasma etching of passivation layers and a following layer deposition procedure via openings in a **mechanical masking**. The exceptional way how the reusable masks are attached to the sample provides accurate masking over large area. By overlaying two masks the wafer can remain underneath the lower masking, which also works as a sample holder during all the structuring steps while, if necessary, the upper mask is exchanged for each particular process step. This provides an **extreme safe wafer handling** along all the IBC-HJ specific process steps, highly recommended **for very thin wafers**. This allows processing the different layers (e.g. emitter, BSF, TCO, metal) structures without the need to touch the wafer after each step. Furthermore a **mechanical self aligning** of the mask-stacks can be applied in mass production. First test structures are shown and cost estimation for IBC-HJ solar cells is presented.
Keywords: heterojunction, IBC, a-Si/c-Si

1 Introduction

IBC-HJ solar cells have a very high efficiency potential of more than 24% on p-type [1]. and more than 25% on n-type, respectively [2]. They combine the most efficient silicon solar cell technologies available on the market, namely the interdigitated back contacted back junction solar cell known from SUNPOWER and the HIT solar cell from SANYO. The IBC-HJ cell structure consists of a contactless and well passivated front side with any kind of light capturing features. On the back side the highly diffused emitter and BSF areas are substituted by the amorphous/crystalline silicon (*a*-Si:H/*c*-Si) heterojunction contact structures (figure 1), which are deposited at temperatures of less than 200°C. These *a*-Si:H/*c*-Si structures are very low recombinative and cause the very high voltages potential of these kind of cell. During the last years a rapid efficiency increase with an actual maximum of 20,2% [3] and 22,2% [10] is observed. Different approaches how to structure the emitter and base contacts of silicon heterojunction (HJ) contact patterns on the cell rear side are known: a) with photolithography like in [1] or like in the RECASH or PRECASH method [5], b) with screen printing a resist plus etching steps [6], c) by putting a hard mask on the sample like in the BEHIND procedure [7], or by using a hard mask in small distance to the sample [8].

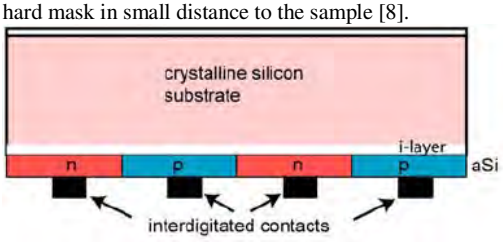


Figure 1: Side cut of a common IBC-HJ solar cell [4].

The first two production methods (a, b) suffer from the unpleasant procedures like depositing and hardening plus in the case of photolithography illuminating and developing a resist, as well as etching of the uncovered areas and wet chemically removing the resist. All these steps are associated to unfortunate handling steps and switching between in-line and batch procedures. This kind of processing is expensive and rather uncomfortable for very thin substrates (e.g. 100µm thickness). Furthermore, wet chemical residuals have to be carefully removed from the wafer surface since they would be located in the very sensitive space charge region of the heterojunction contacts and would strongly reduce the performance of the final device. All these aspects are cost effective.

The BEHIND concept benefits from the cheap and reusable mask as well as form the high V_{OC} potential (695mV) due to the full area emitter deposition in the beginning of the procedure [5]. On the other hand it suffers from accurate mask adjustment after the first structuring step. Furthermore in mass production a hard mask tends to mechanically damage the thin underlying passivation or heterojunction layers due to local mechanical contact. Also problems can appear due to plasma penetration below the mask if the sample or the mask is not flat or deformed by continuous use. Later on in figure 5 a comparable process flow (BEHIND-like) is presented, which uses the stacked masks and the novel method with foils.

The mentioned problem of plasma penetration below the mask turns up extremely by keeping the mask in small distance to the sample like presented in [8]. The effect is very sensitive to the applied distance and does not allow exact structuring as penetration of the plasma below the mask appears everywhere and is detrimental to the cell performance.

2 Cell processing using the novel method:

The new approach combines the benefits of in-line capability with vacuum processes only, reusable masks, self alignment plus easy and save wafer handling. It is based on a plasma etching and layer deposition procedure via openings in stacks of mechanical masks. The procedure how the reusable masks are attached to the sample provides accurate masking over large areas. By using this thin films instead of thick hard masks surface damage is avoided, especially if the film is soft or a soft coat is applied. Furthermore plasma penetration below the mask, due to incomplete proximity of the mask to the wafer, is avoided. This proximity is achieved by using a non-planar holder with a curved surface, on which the

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cell precursor is bended by pressing the tensed mask onto it.

In the following three different kinds of samples and an exemplary process flow are presented. First *a*-Si:H structures which were deposited and etched via one mask. Then transparent conductive oxide (TCO) layers are deposited via this mask. Afterwards an exemplary process flow is presented and finally a structure is shown, which uses a stack of masks, where the upper masks are exchanged for emitter and BSF structures, respectively.

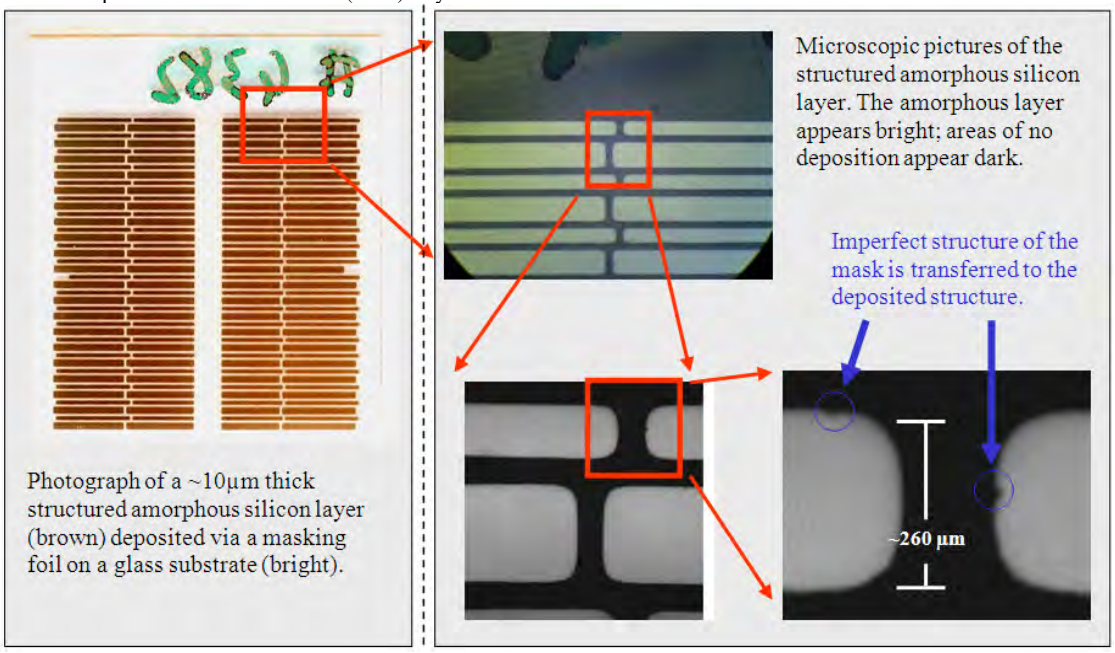


Figure 2: Structured *a*-Si:H layer deposited through a flexible mask according to the novel method.

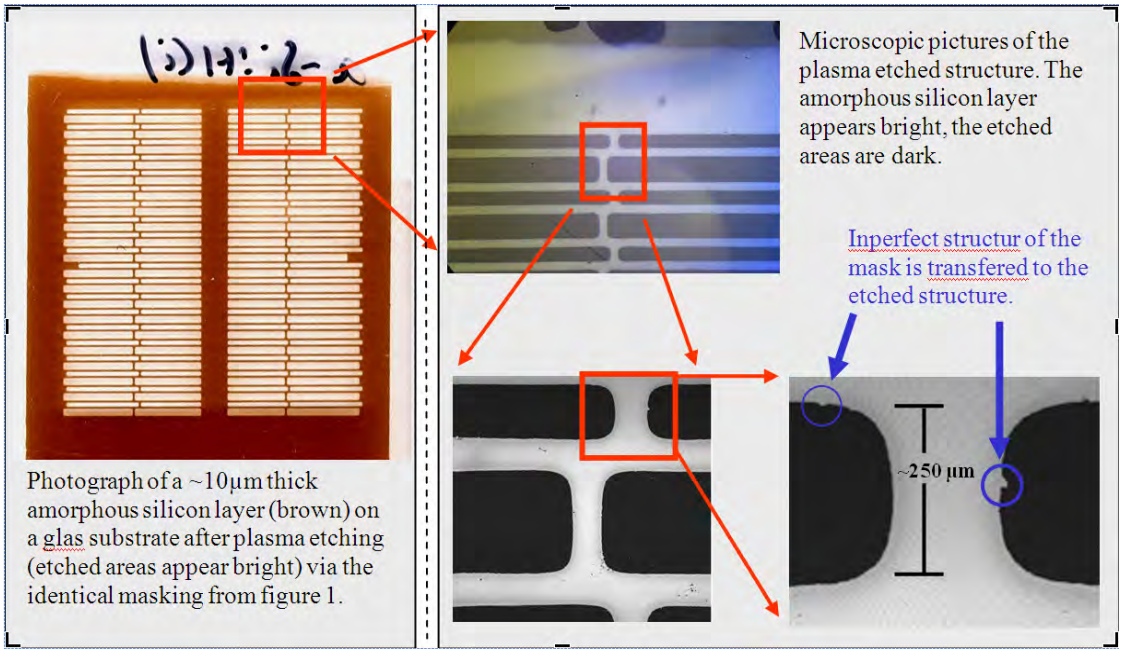


Figure 3: Structured *a*-Si:H layer after plasma etching through a flexible mask according to the novel method.

2.1 Test sample using one mask

As test sample a ~10µm thick amorphous silicon layers is shown, which was deposited through openings in a flexible mask onto a glass substrate according to the novel method (in figure 2). The *a*-Si:H was deposited in a standard parallel plate PECVD setup at an excitation frequency of 13.56MHz. Due to the absorption of the *a*-Si:H in the wavelength range up to 600nm the layer appears brown. Even very thin layers are easily visible. The abrupt borderline is visible, which even properly transfers imperfections of the mask openings to the deposited layer structure (lower right picture in figure 2).

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Furthermore no parasitic deposition can be observed all over the sample area. Please note that the thickness of the used amorphous layers is three orders of magnitude thicker than used in a-Si:H/c-Si structures.

In figure 3 first a ~10µm thick full area amorphous silicon layer was deposited on a glass. Afterwards plasma etching was applied through openings of the identical flexible mask used above. Once more one can see the abrupt borderline which perfectly transfers the imperfections of the mask openings to the etched layer structure (lower right picture in figure 2). No parasitic etching is observed all over the sample area.

The width of the deposited and etched test structures are ~250µm and ~450µm with a pitch of 1mm. These dimensions are more than adequate for IBC solar cells.

To have an idea of the steepness of the edges at the borderline of the prepared structures two 3D scans were prepared with a confocal microscope. As shown in figure 4 (left) the shape of the plasma etched step is perfectly perpendicular with no any rounding of the edge neither under etching of the mask. Furthermore the deposited *a*-Si:H layer (right) shows a well defined structure with slightly rounded edges.

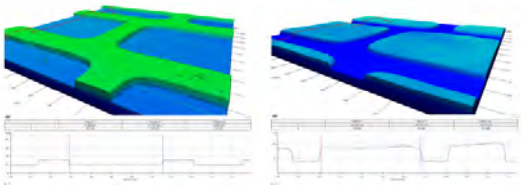


Figure 4: Topographies of the structured deposited *a*-Si:H layers shown in figure 1 (right) and etched *a*-Si:H layer after plasma etching from figure 2 (left) prepared by a confocal microscope.

2.2 TCO deposited via the mask

Usually the thin silicon layers of a-Si:H/c-Si HJ structures are covered with TCO to provide an anti reflection coating, and low ohmic contacts to the metallization, for light confinement, and to increase the lateral conductivity of the layer stack. In figure 4 80nm of indium tin oxide (standard used TCO) was deposited through the flexible mask onto a silicon wafer. Once more the shape of the mask is well defined and no any parasitic deposition occurs.

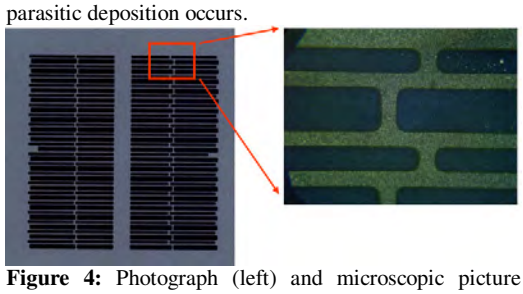


Figure 4: Photograph (left) and microscopic picture (right) of a ~80nm thick structured indium tin oxid (ITO) layer (dark/blue) deposited via a masking foil on a silicon wafer (grey).

2.3 Novel method using two stacked masks

By overlaying two masks the wafer can remain underneath the lower mask (blue mask in figure 5), which provides all the openings used in the two different upper masks (grey and brown in figure 5). During the complete process flow the upper masks are exchanged while the lower mask stays unmoved. In this example (figure 5) a BEHIND-like process flow is used in which two upper masks, for producing the BSF layer and the TCO, are involved. This technique allows processing the different structures without the need to touch the wafer after each step and consequently provides an extreme save wafer handling during all IBC-HJ specific process steps, what is highly recommended for very thin substrates of future technologies. Please note, that with the BEHIND process 695mV and high parallel resistances were archived.

2.4 Cell precursor with dielectric rear side

One sample prepared with this technology but with a different process flow to figure 5 is shown in figure 6. An oxidized (100nm) wafer was covered by two stacked masks, then local areas were opened and the first HJ layer stack was deposited (e.g. the emitter). Afterwards the upper mask was exchanged and the second HJ layer stack

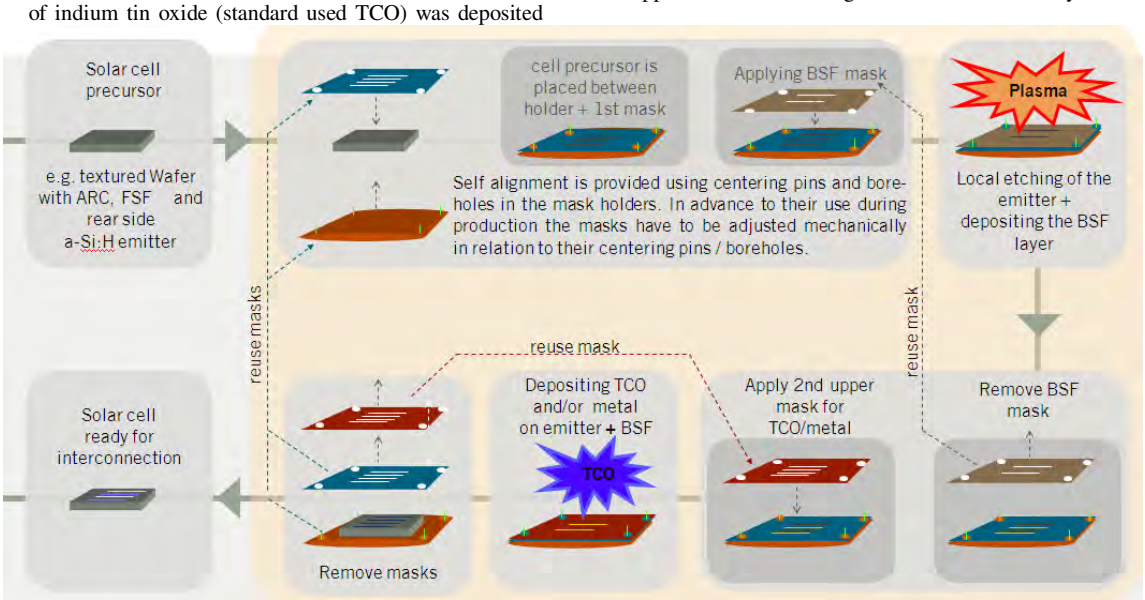


Figure 5: Example of one possible process flow using a BEHIND-like [5] procedure to prepare the structured *a*-Si:H layers.

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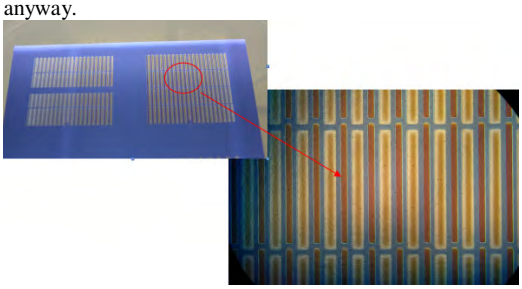


Figure 6: Photograph (left) and microscopic picture (right) of an oxidized silicon wafer after separate plasma etching the oxide and subsequent depositing of amorphous layers. Two stacked masks were used.

2.5 Self alignments of stacked masks

The processing procedure can be provided with a self aligning of the mask-stacks in mass production. Thus during the process flow the lower mask keeps it position relatively to the sample, only the position of the upper mask relative to the lower mask have to be adjusted.

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The exemplary CoO estimation is based on the process flow of figure 6 and starts with n-type silicon cell precursor with optical and electrical optimized front side (e.g. front surface field, front side silicon surface passivation, anti reflective coating). The deposition of the amorphous silicon emitter on the back side including an adequate wet chemical cleaning step previous to the layer depositions is calculated to 10,6 ct per 6" wafer (wa). The structured plasma etching followed by the HJ-BSF deposition is 14,4 ct/wa (figure 8) and the final TCO and/or metal deposition (in sum ~75nm) is estimated to 10,9 ct/wa. All this costs are distributed like presented in figure 9. The cost drivers are the estimated invest and the estimated reduced throughput due to prolonged vacuum pump down. In sum the process cost for the complete procedure excluding cost for preparing the precursor is 36,3 ct/wafer. As the cells bear of highly conductive metallisation the current collection should be shifted to the cell interconnection level e.g. like described in Patent DE 102008043833 A1.

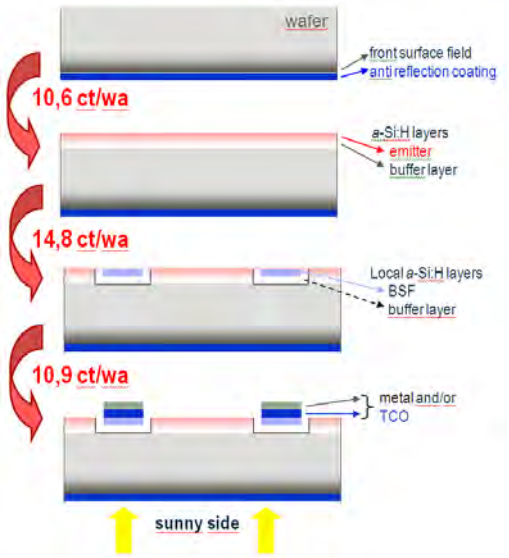


Figure 8: Estimated cost per wafer for IBC-HJ solar cells produced according to the flow of figure 5.

The CoO is based on equipment cost of 2009, is calculated for a first pilot production line and excludes further cost reduction potentials. Furthermore the net capacity can be improved. Due to this the expected process cost will be significantly lower.

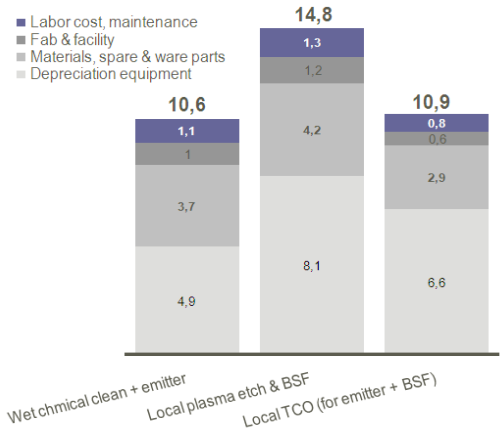


Figure 9: Cost distribution for the process flow of figure 5 excluding cost for preparing the cell precursor.

4 Conclusion

A new technique for preparing IBC-HJ solar cells is presented. Instead of lithographical processes it works with reusable masks or stacks of masks. These are softly

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attached to the sample surface in an exceptional way, which guarantees a dense proximity over large areas. By using stacks of masks an extreme save wafer handling for very thin wafers without touching the samples after each step is guaranteed and easy mechanical self aligning can be provided. The cell process cost are estimated to 36,3 ct/wa for the specific processes.
This technology is subject of the international patent family [10]. Q-Cells offer non-exclusive licenses to potentially interested companies. For more information please contact:
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Attachment I-5

Heterojunction Interdigitated Back-Contact Solar Cells Fabricated on Wafer Bonded to Glass

Stefano N. Granata, Monica Aleman, Twan Bearda, Jonathan Govaerts, Mariella Brizzi, Yaser Abdulraheem, Ivan Gordon, Jef Poortmans, and Robert Mertens

***Abstract*—Future wafer-based silicon solar cells will be fabricated on thin ($<$140 μm) wafers. However, technologies to handle thin wafers during cell processing are not yet available for industry. In this paper, a flow to handle thin wafers during rear side cell processing is developed and demonstrated on 4-in 200 μm-thick wafers. The flow involves bonding the wafers to glass after front-side processing followed by a low-temperature p-n heterojunction formation on the rear side. 2.5 $\times$ 2.5 cm^2 amorphous/crystalline silicon heterojunction interdigitated back-contact solar cells are fabricated by use of lithography while bonded to glass, and they show an efficiency of up to 17.7%. Shunts, infrared light absorption, and rear side interface passivation are identified as the main efficiency losses. Dedicated experiments suggest that the passivation losses are related to the degradation of the adhesive during wafer cleaning. Hence, methods to improve the compatibility of the adhesive with the cleaning process are discussed.**

***Index Terms*—Heterojunction silicon solar cells, interdigitated-back-contact (i-BC), superstrate processing.**

I. Introduction

THE silicon wafer-based photovoltaic roadmap shows future trends toward the fabrication of kerf-free solar cells using wafers thinner than 140 μm. Thin wafers are more fragile than standard $\sim$200-μm-thick wafers. For this reason, their handling has been identified as a major issue for industrial cell processing; thin wafers can easily break, and the production yield may be affected [1].

A method to overcome the issue of wafer breakage is to mechanically support the thin wafer during processing, for example, with a wafer carrier. The literature reveals examples of solar devices that are fabricated on thin wafers, while they are bonded to different carriers throughout solar cell processing. This is the case of the HySi concept proposed by ISFH [2], the i^2-module concept proposed by IMEC [3], the XIS concept proposed by ECN [4], and other similar industrial prototypes [5]–[7]. The devices that are suggested in these concepts are fabricated according to the following flow. Beginning with thick silicon wafer, a few micrometers at the top of the material are porosified by means of electrochemical etching. This porous silicon layer is used as a seed for the epitaxial growth of a thin silicon foil. After epitaxial growth, the accessible side of the thin foil is partially processed into a solar cell. The foil is transferred to a second permanent substrate, e.g., the module glass, and detached from the parent substrate at the depth of the porous layer. The other side of the foil is now accessible and the process steps necessary to complete the solar cell are performed on the accessible side. As such, the foils are processed into solar cells while being mechanically supported during the majority of the process steps; this way, most handling issues are solved. Furthermore, several foils can be bonded to the same module glass and part of the processing can be realized at module level (module-level processing) [2], [8]–[11]. This way, the module throughput can be significantly increased and, if the process after bonding is maintained simple, the production cost is decreased.

After bonding, the mechanical carriers and the adhesive that are used for bonding introduce constraints in the experimental window of module-level processing. For instance, in the i^2-module, a silicone adhesive is used to bond the front-processed thin foil to the module glass and an interdigitated back-contact (i-BC) solar cell is fabricated on the rear side of the bonded foil. The silicone adhesive limits the processing temperatures of the bonded foil to 300 °C [12]. Hence, high-temperature processes have to be either performed prior to bonding or replaced by low-temperature processes. This constraint introduces a problem for the emitter formation and surface passivation of the back contact solar cell. Conventionally, the emitter of the cell is formed through diffusion of dopants into the wafers at temperatures above 900 °C [13]. The surface is passivated either by a thermal oxide grown during diffusion or by dielectric deposition and forming gas annealing at a temperature above 400 °C [14]. These conventional methods are not compatible with the i^2-module, since the emitter is located at the rear side of the wafer and this area is only accessible to process after bonding and detachment. Nevertheless, several other solutions are available to form the i^2-module emitter: some examples are emitter epitaxial growth [3], laser doping [15], or amorphous silicon a-Si:H deposition [16]. Among these, a-Si:H deposition has the additional advantage to provide excellent

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surface passivation at temperatures below 300 °C [17]. Furthermore, a-Si:H/c-Si heterojunction solar cells (HJ) can reach state-of-the-art efficiencies up to 24.7% for double side contact cells [18] and 23.4% for back contact solar cells [16]. For these two reasons, i.e., low temperature emitter formation and excellent surface passivation, the a-Si:H /c-Si HJ technology is a good candidate for the development of the i^2-module.

In this paper, the a-Si:H /c-Si HJ technology is implemented in the fabrication and passivation of emitters for i^2-module demonstrator cells and replaces the conventional high-temperature methods used in the previous trial [19]. The demonstrator cells are fabricated on 200-μm-thick wafers bonded to glass. Only low-temperature ($\leq$230 °C) rear-side processes are used, these being compatible with the presence of silicone adhesive [20]. The main losses of the HJ i-BC cells are identified, and the ones related to the issues of processing on glass are discussed in detail.

II. Device Process

The wafers that are used are 4-in round n-type float-zone with a resistivity of 1–3 Ω·cm and a thickness of 180 μm. The ingot minority carrier lifetime is 2 ms, as indicated by the wafer supplier.

First, the wafers are thermally oxidized. The front oxide is removed by vapor HF and the wafers are single-side textured in a TMAH-based solution. A phosphorus-doped layer is diffused by $POCl_3$, resulting in a front-surface field (FSF) with a sheet resistance R_{sheet} of approximately 300 Ω/sq. A thin oxide layer is used for the front passivation of the n^+ region and an antireflection coating based on a SiN_x PECVD layer is deposited on the front side. This process leads to an FSF saturation current density $J_{o,\mathrm{FSF}}$ of approximately 20 fA/cm^2. [13]. Up to this point, the wafers are free standing. In the i^2-module configuration, the thin Si foils would still be attached to the parent substrate, allowing high temperature processes [11].

The wafers are then bonded to a 10 × 10 cm^2 quartz superstrate. A layer of 100 μm of Dow Corning PV6100 silicone [12] is screen printed on the glass on an area smaller than the wafer with an offset of 5 mm from the wafer edge. This offset is chosen to avoid the direct exposure of the silicone during subsequent steps, which could have an influence on the cell performance [20]. This layer is cured at 100 °C for 5 min under vacuum prior to wafer bonding. The wafers are manually bonded on the glass and the wafer/silicone/glass stack is cured at a temperature of 200 °C for 1 h in a vacuum. This additional curing is performed to avoid silicone contamination of the plasma chamber during PECVD deposition [9], [21]. The samples are then left in the vacuum overnight in order to remove air bubbles that are created during the manual bonding. As such, the process produces a homogenous front side reflectance of 5.4% at 700 nm, as measured on finished cells.

After bonding, the samples are cleaned. The cleaning process involves thermal oxide stripping by buffered HF (1:2 in water, 25 °C, 7 min) and silicon removal by hot TMAH (1:4 in water, 75 °C, 8 min) and an HF:HNO_3 mixture (1:80, 25 °C, 6 min). The chemical sequence replaces the standard H_2O_2:H_2SO_4/HF cleaning sequence, which is not compatible with the silicone adhesive [19]. Finally, the rear surface is chemically oxidized in a H_2O:HCl:H_2O_2 solution (5:1:1, 25 °C, 20 min) to protect it from atmospheric contamination. The remaining steps are performed on the rear side of the bonded sample. The sample is dipped into HF (1:100, 25 °C, 1 min′) and an a-Si:H emitter is deposited by PECVD on the back surface of the wafer. The emitter is a stack of 3 ± 1 nm of a-Si:H(i) followed by an H_2 plasma [22] and 22 ± 1 nm of a-Si:H(p^+). The process conditions for these layers are detailed in Table I. The a-Si:H(i/p^+) stack gives a saturation current density in the order of 50 fA/cm^2.

TABLE I
Process Parameters for the Different Layers Deposited by PECVD

Layer	Temperature [°C]	Pressure [Torr]	Power [mW/cm^2]
a-Si:H (i)	200	1.7	45
a-Si:H (p^+)	160	0.7	23
a-Si:H (n^+)	160	0.7	45
SiO_x	225	1	82
SiN_x	230	1.2	66

A SiO_x/SiN_x PECVD mask is deposited on top of the a-Si:H(i/p^+) layer for protection during further process steps. The process conditions for these layers are also reported in Table I. After mask deposition, the sample lifetime is maintained: no degradation of the a-Si:H/cSi interface is suspected, conversely to what is sometimes reported for SiO_x/cSi or SiN_x/cSi interface [23]. Lithography is performed on the a-Si:H(i/p^+)/SiO_x/SiN_x layer to pattern 2.5 × 2.5 cm^2 cells (5 per wafer). First, the SiO_x/SiN_x stack is etched in buffered HF (1:2, 25 °C, 5 min′) and then the a-Si:H(i/p^+) is etched in a BHF:HNO_3:H_20 mixture (1:40:16, 25 °C, 6 min). This last step etches the a-Si:H(i/p^+) emitter and approximately 850 nm of the c-Si wafer. Subsequently, a blanket back surface field BSF layer is deposited on the patterned wafer. This is a stack of 6 ± 1 nm of a-Si:H(i) followed by an H_2 plasma [22] layer and a 28 ± 1 nm of a-Si:H(n). All process conditions are reported in Table I. The a-Si:H(i/n^+) layers give saturation current density in the order of 10 fA/cm^{-2} as measured on symmetric test structures prior to device integration. The BSF layer is patterned by photolithography and etched in TMAH (1:100 in water, 25 °C, 5 min′), with the a-Si:H(i/p^+) layer that is protected by the SiO_x/SiN_x mask. Then, the resist is removed and the remaining SiO_x/SiN_x mask is etched in buffered HF. The design for the fingers pitch is taken from [24], and no gap between emitter and BSF a-Si:H fingers is present.

At this stage of the process, some cells undergo backside indium tin oxide (ITO) deposition (in the following named split HJ ITO), while the others are directly metalized (split HJ). 80 nm of ITO are deposited on the full area of the split HJ ITO by PVD with a power density of 0.32 W/cm^2 and a O_2 partial pressure of 1.5%. The layers are annealed for 1 h at 200 °C. The resulting ITO has a resistivity of 5 × 10^{-4} Ω·cm and 3.5 × 10^{-4} Ω·cm before and after annealing, respectively. The ITO is lithographically patterned and etched in HCl (5:8, 25 °C, 35 min). A layer of TiW/Ag of 20/1800 nm is thermally evaporated on both splits and patterned on an area smaller than the a-Si:H fingers by liftoff. TiW is used to improve adhesion between silicon and

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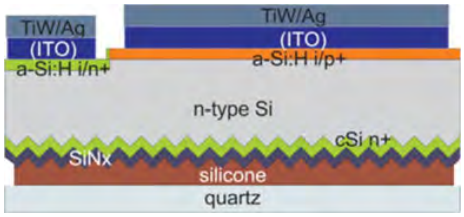


Fig. 1. Scheme of the devices obtained with the designed flow. The ITO layer is only present in the HJ ITO split, and the cell dimension is 2.5 × 2.5 cm^2.

TABLE II
2.5 × 2.5 cm^2 CELLS PERFORMANCE FOR THE HJ, HJ ITO, AND HYBRID

	Split (n. of cells)	J_{sc} [mA.cm^{-2}]	V_{oc} [mV]	FF [%]	Eff [%]
Average	HJ (5)	34.8±1.4	641±17	71.6±3.8	16.0±1.5
	HJ ITO (10)	35.8±0.9	648±6	72.5±2.9	16.8±0.9
Best Cells	HJ (1)	35.9	656	75.0	17.7
	HJ ITO (1)	36.4	654	73.8	17.6
	Hybrid [19]	37.8	650	74.7	18.4

Ag [25], and it is not removed in the HJ ITO split in order to relate the differences between the backside reflectance of the HJ and the HJ ITO device to the ITO uniquely. The geometries of the ITO and TiW/Ag patterns are identical. Final contact annealing is performed for 20 min at 165 °C under atmospheric pressure. Fig. 1 shows the scheme of the obtained cells.

The IV characteristics of all cells are measured with an illuminated area of 2 × 2 cm^2 at different illumination levels ranging from dark to 1 sun, and the values of R_{series} and R_{shunt} are extracted [26]. The internal quantum efficiencies (IQEs) of the best cells of each split are extracted from measurements of spectral response and reflectance. The saturation current density J_{01}, the ideality factor n, and the pseudo fill factor pFF of the best cells are measured by suns-V_{oc} [27]. The two-diode model is fitted with dark IV curves to extract the values of J_{02} and reconfirm the values of J_{01}, R_{shunt}, and R_{series}. The J_0 at the wafer interfaces with the emitter; the FSF and the BSF are measured on freestanding monitor wafers. The monitor wafers have symmetric structures and undergo the same process as the device wafers, except for bonding and metallization, which are not performed on the monitor samples. However, neither bonding nor thermal evaporation should degrade the passivation [20], [28].

III. RESULTS

A. Cell Characterization

Table II reports the cell parameters that are measured on both splits (HJ and HJ ITO), with the best cell for each split also included. The best results of the previous i^2-module demonstrator cells are also reported for reference and named Hybrid [19]. The main difference between the previous and the present attempt is the emitter formation and its passivation. In [19], the emitter is diffused and passivated by PECVD-deposited SiO_x. Both processes are performed prior to bonding at temperatures above 300 °C. In the HJ and HJ ITO, the emitter and the passivation

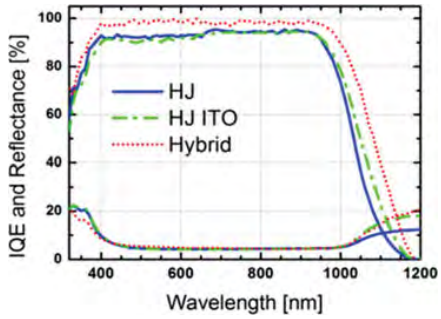


Fig. 2. Reflectance and IQE of the best cells of each split. For comparison, the IQE and reflectance of the Hybrid cells are also reported [19].

are realized with a PECVD-deposited a-Si:H i/p$^+$ layer on the bonded wafer.

The 95% confidence intervals for the efficiency of each split are: 14.7–17.3, 16.2–17.3, and 16.3–17.3 for the HJ, the HJ ITO, and the Hybrid, respectively. The cells have similar efficiency, regardless of their position on the wafers. The efficiencies of the HJ, HJ ITO, and Hybrid are comparable, but their performances are lower than the ones of state-of-the-art HJ i-BC cells [16].

The IQE of the best cells is extracted to evaluate the optical losses in the devices [29]. Fig. 2 shows the reflectance and the IQE of the best cells for both splits, together with the values for the Hybrid device [19].

The reflectivity in the short wavelengths (300–400 nm) is around 20% and comparable with that of the Hybrid cells. This value is much lower compared with freestanding cells that are processed with an identical ARC [13], and this difference is because of the presence of the silicone and glass [19]. The low reflectance indicates the excellent refractive index matching of the silicone with wafer and glass that avoids optical losses during cell encapsulation. The IQE in the short wavelengths is below 80% for both splits, which indicates poor carrier collection at the front side of the wafers. Similar results are also reported in other cell structures that are processed with the same front side, independently whether these are bonded [19] or not [13]. Hence, the poor collection is not related to the process sequence of the bonded wafers, and for this reason, it is not discussed further in this paper.

The reflectance in the medium wavelength range (400–1000 nm) is comparable for HJ and HJ ITO. However, the IQE of the HJ and HJ ITO is lower compared with the Hybrid device. This cannot be attributed to bulk lifetime, since the value of 2 ms leads to a diffusion length above 1.5 mm, which is more than three times the thickness of the cell. The reason for the loss in J_{sc} is the shunts between the emitter and the BSF region. This shunt is because of the absence of insulation gap between the a-Si:H(i/p$^+$) and a-Si:H(i/n$^+$), which is not the case for the thermal oxide in the Hybrid cells [19]. R_{shunt} values that are extracted from *I–V* measurements are in the order of 1–1.3 × 10^3 Ω·cm^2 for the HJ and HJ ITO splits, while the Hybrid concepts reports values above 2 × 10^4 Ω·cm^2 [19]. Electrical shading [30] is not considered in the analysis since the HJ and the Hybrid structures are fabricated with the same

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TABLE III
J_0 EXTRACTED AT 10^{16} cm^{-3} AT DIFFERENT INTERFACES

Best Cell	HJ	HJ ITO
Front	20 fA/cm^2	20 fA/cm^2
Emitter	115 fA/cm^2	123 fA/cm^2
BSF	200 fA/cm^2	210 fA/cm^2

geometry and the decrease in IQE in the medium wavelength range is only present in the HJ and HJ ITO. To avoid shunts, a different cell geometry is needed for the HJ cells, which foresee an insulation gap between the two fingers [31]. However, this loss is not related to the processing of bonded wafers, and for this reason, it is not further discussed in this paper.

The reflectance in the high wavelength range (1000–1200 nm) is poor, and this results in significant parasitic absorption in the back side metal and low IQE for the long wavelengths [32]. The presence of ITO slightly improves the infrared reflectivity, which in turns leads to a slightly better IQE. The difference between the integrated spectral currents of the HJ and the HJ ITO cell of Fig. 2 is $\sim$0.6 mA/cm^2, which is in line with the higher $J_{\rm sc}$ reported for the HJ ITO compared with HJ.

$R_{\rm series}$ values of the best cells of each split are determined by the Bowden method [26] in order to evaluate the influence of the ITO on the a-Si:H contact. The $R_{\rm series}$ of the HJ split is 0.34 Ω/cm^2 and lower than the one of the HJ ITO split, which is 0.52 Ω/cm^2. The difference in $R_{\rm series}$ may arise from a difference in contact resistances $R_{\rm contact}$. The lateral conduction of carriers is similar in the two splits because of the identical contacting scheme and the use of the same bulk wafer material. The values of $R_{\rm series}$ suggests that a-Si:H/TiW gives a lower resistive contact than a-Si:H/ITO. However, TLM structures that are fabricated both on p- and n-type contacts exhibit nonreproducible behavior and could not confirm this hypothesis.

The ideal fill factor FF$_0$ is calculated theoretically [33] and gives values of 83.8% for both splits. pFF and n are 78.7% and 1.28, respectively, for HJ and 78.5% and 1.29 for HJ ITO. The difference between FF$_0$ and pFF is similar for both splits and larger than the pFF – FF difference; the main FF losses are caused by recombination and shunts, which equally affect both structures.

High recombination losses are also indicated by the values of $V_{\rm oc}$, J_{01}, and J_{02}. $V_{\rm oc}$ is approximately 80 mV lower compared with state-of-the-art cells ($V_{\rm oc}$ of $\sim$740 mV). The total J_{01} of the best cells are 160 fA/cm^2 (HJ) and 170 fA/cm^2 (HJ ITO). These values are slightly better than for the Hybrid cell (3×10^{-13} A/cm^2 [19]) but still much higher than state-of-the-art heterojunction cells (10^{-15} A/cm^2 [16]). J_{02} is approximately 80–90 nA/cm^2 and similar for HJ, HJ ITO, and Hybrid.

The passivation at the different interfaces of the device is evaluated by QSSPC on freestanding monitor wafers. The J_0 for the front side and for the heterojunctions (emitter and BSF) are extracted considering an ideality factor equal to 1 and 1.28, respectively. J_0 values at 10^{16} cm^{-3} are extracted from QSSPC measurements and reported in Table III, showing that the majority of the recombination occurs at the backside of the wafer. The J_0 at the different interfaces are averaged according to the cell geometry and correlate well (difference below 2% relative) with the J_{01} values measured by suns-$V_{\rm oc}$.

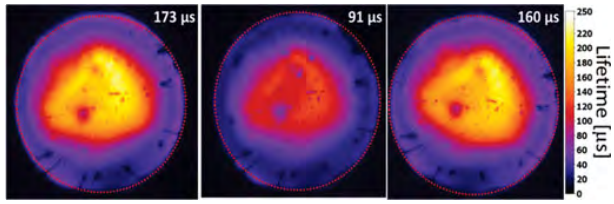


Fig. 3. PL pictures of monitor wafers for the evaluation of the a-Si:H passivation. The measurements are taken after: a-Si:H(i/p$^+$) passivation (left); ITO deposition and etching (middle); 1 h annealing at 200 °C (right). The lifetimes measured at an injection level of 10^{15} cm^{-3} are indicated.

However, the J_0 at the a-Si:H/c-Si interface of monitor wafers are higher compared with the J_0 values mentioned in Section II, which were obtained on tests performed prior to device integration. The difference between the passivation obtained on monitor and device wafers and the value mentioned in Section II suggests that this issue is not caused by the a-Si:H layers, as such, but related to the process sequence of the bonded devices. Hence, the influences of critical process steps for a-Si:H passivation, i.e., the postbonding cleaning sequence prior to a-Si:H deposition [34] and the damage due to the ITO [35] are investigated in detail.

B. *Influence of the Indium Tin Oxide*

The influence of the ITO PVD deposition on the passivation is monitored during the process sequence. Fig. 3 shows the wafer after 1) a-Si:H(i/p$^+$) passivation, 2) ITO deposition and etching, and 3) 1 h of annealing at 200 °C.

The PL pictures of Fig. 3 show a decrease in lifetime after ITO deposition, confirming previously reported results [19], [28]. This drop is almost fully recovered (>90%) by wafer annealing, as reported in the literature [35]. A similar trend has also been observed for a-Si:H(i/n$^+$) layers (not shown). Hence, the impact of the ITO deposition is almost completely recovered after the annealing step.

The influence of the annealing on the absorption of the ITO layer is also studied. Reflectance and transmission of dedicated freestanding samples of cSi(n)/aSi(i/p$^+$)/ITO(80 nm) textured on the front and polished on the rear have been measured in the range 900–1400 cm^{-1} (see Fig. 4). After annealing, both the reflectance and the transmission in the infrared region decrease, i.e., the absorbance increases. The absorbance of the ITO at 1200 cm^{-1} is 26% and 55% before and after annealing, respectively. The increased absorption is caused by the thermal activation of free carriers during the annealing step [36]. Subsequently, the annealing step minimizes the improvement related to the presence of an optical spacer between the aSi:H(i/p$^+$) and the metal [32], and the IQE remains poor for the HJ ITO split as well. No influence of the annealing performed after contact deposition is seen.

Hence, the annealing that is performed after ITO deposition is beneficial for passivation but is detrimental for carrier collection at long wavelength. The compromise between these two effects

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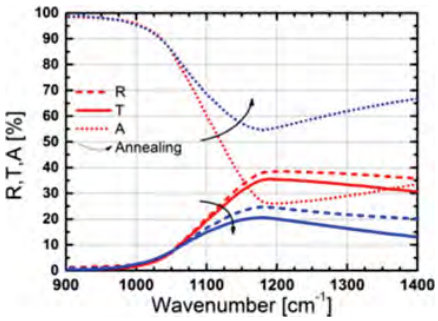


Fig. 4. Infrared carrier reflectance, transmittance, and absorbance of the sample cSi(n)/aSi(i/p$^+$)/ITO (80 nm) before and after annealing at 200 °C for 1 h.



Fig. 5. Silicone degradation after dip in HF: HNO_3 mixture. The red dotted line indicates approximately the perimeter of the silicone area before dip.

can be solved with different options. For instance, the carrier density can be minimized during deposition by increasing O_2 partial pressure [36]. The corresponding increase in resistivity may not necessarily limit the cell performance, since the lateral conduction occurs in the metal and the ITO is mainly used as an optical spacer. Another way to solve the compromise is to reduce the passivation damage by lowering the ITO deposition power density [37].

With the careful tuning of these two parameters during deposition, i.e., O_2 partial pressure and power density; the postdeposition annealing may be performed at lower temperature/shorter time and limit the thermal activation of carriers in the ITO, while still recovering the passivation damage.

C. *Influence of Surface Cleaning*

The impact of the postbonding cleaning on the silicone has been investigated. Previous results [19] show that the HF:HNO_3 mixtures are as efficient as H_2SO_4:H_2O_2 mixtures in the removal of surface contamination for bonded wafers. However, the effects of HF:HNO_3 on silicone are not detailed. Tests are performed on bare wafers bonded to glass. The wafer, silicone, and glass areas are 5×5 cm^2, 6×6 cm^2, and 12.5×12.5 cm^2, respectively (see Fig. 5). The silicone area is bigger than the one of the wafer, in order to directly expose the silicone to the chemical solution and maximize the impact of the possible reaction. The bonded samples followed the same bonding and curing process of the devices. The silicone directly exposed to the solution is degraded after immersion in HF:HNO_3 (1:80 25 °C, 6 min, Fig. 5), and similar effects are obtained at different concentrations (not shown). Similar tests are performed with the TMAH solution, but no degradation is observed.

TABLE IV
SILICONE AND WAFER APPEARANCE AFTER 10 min CLEANING IN DIFFERENT SOLUTIONS

	Composition	T [°C]	Silicone Appearance	Wafer Appearance
SC1	NH_4OH:H_2O_2:H_2O	~70	DEGRADED	HYDROPHOBIC
	1:1:5	25	NO CHANGES	HYDROPHILLIC
SC2	H_2O_2:HCL:H_2O	~70	DEGRADED	HYDROPHOBIC
	1:1:6	25	NO CHANGES	HYDROPHILLIC
HF	(2:100 IN WATER)	25	NO CHANGES	HYDROPHOBIC

In the cell process flow, the HF:HNO_3 degradation is not visible by optical methods and this may depend on the limited interaction between the chemistry and the silicone shielded under the wafer. However, the silicone degradation and the release of molecules in the solution during the HF:HNO_3 etching cannot be excluded. The molecules that are released in the solution may compromise the cleanness of the wafer surface and later in the process cause poor a-Si:H passivation. This may be the reason for the reported high a-Si:H J_0 recorded during device integration. The monitor wafers also report the same degradation since they are processed in the same chemical solution as the bonded wafers.

As such, the HF:HNO_3 and H_2SO_4:H_2O_2 mixtures cannot be used to clean wafers bonded with silicones. Hence, similar tests are performed to check the compatibility of the silicone with the standard cleaning (SC) sequence [38], which could replace both HF:HNO_3 and H_2SO_4:H_2O_2 mixtures. Results are reported in Table IV.

SC sequence that is performed at a temperature of 70 °C cannot be used to clean the rear surface of the wafer bonded to glass, since the silicone is degraded during the oxidation step. This degradation affects the wafer surface. The wafer surface appears hydrophobic instead of hydrophilic, as expected from a chemically oxidized surface. The hydrophobicity of the surface may be related to the presence of organic molecules released during the degradation of the silicone. The same SC sequence that is performed at room temperature (RT) eliminates the visual degradation of the silicone and the hydrophilicity of the wafer surface is recovered. In this case, no organic contamination is expected.

Hence, the impact of the oxidation step on the silicone decreases with the temperature. J_0 measurements on bonded wafer cleaned with RT SC and passivated with a-Si:H needs to be performed in order to state the possibility of implementing RT SC in the current process flow.

Furthermore, the results of Table IV, together with the ones reported previously [19], show that the silicone is compatible with few type of chemicals that are used in solar cell wet processing. For these reasons, the process flow that is described in Section II needs to be simplified in order to limit the wet processing of bonded wafer, i.e., the steps of surface cleaning and patterning. For instance, a full SC sequence may be replaced by optimized HF:HCl solutions [39], while the interdigitated pattern may be created by means of single-side dry processes such as the use of mechanical masks during deposition [40] or

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screen printing [41]. The implementation of dry methods in the process flow may also have the additional advantage to avoid lithography and decrease the production cost.

IV. Summary

A process flow for the rear side processing of heterojunction back contact solar cells bonded to glass is developed. In this flow, the steps of surface cleaning, emitter and BSF formation, and metallization are realized with low temperature processes ($\leq$230 °C), while the wafer is bonded to glass in a superstrate configuration. Following the developed flow, solar cells of two types were achieved: heterojunction with a-Si:H/metal contact (HJ) and heterojunction with an a-Si:H/ITO/metal contact (HJ ITO). The cells show similar efficiencies around 16%, with maximal values of 17.6% (HJ) and 17.7% (HJ ITO). The differences between HJ and HJ ITO are mainly the infrared reflectivity (higher in the HJ ITO case) and the series resistance (lower in the HJ case). Both types of cells suffer from shunts, low-infrared carrier collection, and high recombination at the emitter and the BSF interfaces. The losses that are related to the processing on glass, i.e., recombination at the emitter and the BSF interfaces, are discussed. The recombination losses are caused by cleaning issues of bonded wafers prior to a-Si:H deposition: the silicone is degraded during the HF:HNO_3 step, presumably contaminating the wafer surface. For this reason, SC sequences have been tested as a replacement of HF:HNO_3 mixtures, showing no silicone degradation if the cleaning is performed at RT. Furthermore, the reduction of wet processing steps after bonding is foreseen in order to avoid silicone degradation and decrease the production cost.

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