Attachment I-6

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BROADER PERSPECTIVES

The energy payback time of advanced crystalline silicon PV modules in 2020: a prospective study

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ABSTRACT

The photovoltaic (PV) market is experiencing vigorous growth, whereas prices are dropping rapidly. This growth has in large part been possible through public support, deserved for its promise to produce electricity at a low cost to the environment. It is therefore important to monitor and minimize environmental impacts associated with PV technologies. In this work, we forecast the environmental performance of crystalline silicon technologies in 2020, the year in which electricity from PV is anticipated to be competitive with wholesale electricity costs all across Europe. Our forecasts are based on technological scenario development and a prospective life cycle assessment with a thorough uncertainty and sensitivity analysis. We estimate that the energy payback time at an in-plane irradiation of 1700 kWh/(m^2 year) of crystalline silicon modules can be reduced to below 0.5 years by 2020, which is less than half of the current energy payback time. Copyright © 2013 John Wiley & Sons, Ltd.

KEYWORDS

energy payback time; life cycle assessment; roadmap; crystalline silicon PV; prospective

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1. INTRODUCTION

The photovoltaic (PV) market has experienced double digit growth in the past decade and has now reached a global capacity of approximately 67 GW [1]. The year-on-year growth of newly installed capacity was 67% from 2010 to 2011, greatly exceeding the International Energy Agency's (IEA) annual growth rate projection of 17% for this decade from 2009 [2,3].

Average European electricity generation costs from PV modules today are 0.20 €/kWh [4], which is competitive with the retail electricity prices in some European countries. However, to fully penetrate the market, the cost of PV electricity has to be driven down further, to the wholesale electricity cost of ~0.08 €/kWh in most European countries [5]. Module production costs have historically been reduced by increases in plant production capacity, increases in module efficiency, reduced cost of silicon feedstock, and reduced silicon consumption per watt-peak (W_p) [6–8]. In recent years, there have been a number of roadmapping exercises that outline paths toward low-cost crystalline silicon modules [2,9–15], which basically emphasize these approaches. With ongoing cost reductions of PV modules and rising wholesale electricity costs, it is expected that utility-scale grid parity will be reached by 2014 in south Italy and by 2020 throughout Europe [4].

The fast growth of the PV markets is largely based on their promise to produce abundant electricity at a low cost to the environment. It is therefore important to monitor and report indicators of the environmental performance of PV technologies, such as the energy payback time (EPBT), the time in which an operating PV system produces the energy required to manufacture it. EPBTs are determined through life cycle assessments (LCAs) of the PV systems' cradle-to-grave life cycles. The most recent reported EPBT values are 1.5 and 1.3 years for monocrystalline and multicrystalline silicon PV systems, produced in Germany and

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located in southern Europe [16]. Note that it is important to distinguish between "modules" and "systems", as the former does not include production of the balance of system (BOS) components and installation. The European Photovoltaic Technology Platform stresses that any negative environmental impact associated with PV systems must be minimized, implying reduction of emissions, recycling of materials, and reduction of EPBTs [15]. Their system EPBT target for 2020 is 0.6 years, and a long-term target is 0.3 years [17]. The IEA targets are 0.9 years for 2020 and 0.7 years for 2030 [2,17].

In this paper, we forecast the 2020 EPBTs for crystalline silicon modules. To do so, we developed three prospective module types, based on the aforementioned roadmaps. These scenarios are then modeled in a prospective LCA to calculate the EPBT and energy return on energy investment (EROI). The roadmapping exercise is discussed in Section 2, the LCA methodology in Section 3, and the uncertainty analysis in Section 4. The results are presented in Section 5 and discussed in Section 6.

2. TECHNOLOGY ROADMAPPING

In this section, we will present a short overview of technological improvements that are proposed to drive down production costs per Wp, drawing from the existing roadmapping exercises [10–13].

2.1. Feedstock and ingot growth

Today, almost all commercially available modules are made from polysilicon from the Siemens process, which is converted into crystalline ingots through either Czochralski (Cz) crystal growth (for monocrystalline silicon) or directional solidification (DS) (for multicrystalline silicon). As polysilicon accounts for almost 25% of the total module production cost today [10], some facilities try to reduce cost by process integration with material and energy recycling routes [16]. Additionally, the high cost has triggered development of alternatives to the traditional Siemens route (e.g., the fluidized bed reactor process [18]) and even abandonment of poly-Si altogether, as with upgraded metallurgical grade silicon (UMG-Si) [19]. Multi-Si cell efficiencies achieved on alternative Si feedstocks such as UMG-Si have been demonstrated to be comparable with those of multi-Si cells from standard feedstock in selected cases [19,20].

Ingot sizes will increase (most notably for the DS technique), which increases the throughput and yield of good quality silicon. Another interesting development is quasi-mono silicon, a crossover between both crystallization techniques [21]. Here, the DS method is modified so that the crystal growth is seeded by a monocrystalline layer at the bottom of the melt. This produces large ingots with a central monocrystalline region, surrounded by multicrystalline edges. This approach has several benefits to regular DS ingots: as the material is quasi-mono, the lack of grain boundaries could result in higher efficiencies. In fact, because of the lack of grain boundaries in central regions of the ingot, the segregation of impurities is more effective. This further encourages the use of UMG feedstock without compromising efficiency loss [10].

2.2. Wafering

To reduce the required amount of polysilicon, the wafer thickness is continuously reduced, from 500 μm in 1979 [22] to an average of 180 μm today [13]. The kerf loss, the silicon loss due to sawing, has decreased as well, to about 150 μm per wafer today. With further advances in the multi-wire slurry saw (MWSS) process, it is expected that 120 μm wafers with 120 μm kerf loss are achievable by 2020 [13], which already reduces silicon consumption by 27% if breakage does not increase and efficiencies can be maintained.

Aside from the kerf loss, the MWSS process has other drawbacks: wafer contamination, thickness variation across the wafer, high breakage, and high material consumption. To address those drawbacks, alternative wafering methods were proposed, most notably a wire sawing process using a fixed diamond abrasive on the wire (fixed abrasive sawing) [23]. Most machines on the market today are adaptable for diamond wires, and implementing them will increase the throughput by a factor of 2–3. In addition, the kerf is commercially recyclable as opposed to kerf from the slurry-based process [24], and wire consumption per wafer is much lower. However, the cost of the wire is much higher, and this so far stands in the way of significant market penetration, but wire costs have been decreasing by 30% per year [23].

To do away with the kerf loss altogether, kerfless cutting methods have been developed, such as the ribbon silicon [25], electrochemical cutting [26], laser wafer cutting [27], stress-induced lift-off [28], and light ion implantation [29]. Of these methods, ribbon silicon is the oldest, but it has difficulties maintaining or increasing market share [25]. Light ion implantation is commercially available, originally through Silicon Genesis (their PolyMax process [29]) but more recently also through Twin Creeks (the Hyperion [30]). It uses proton implantation to create a weak layer at a controlled depth in the silicon brick, after which the wafer is separated by cleaving. This process allows for wafers with a thickness between 20 and 150 μm, and even the thinner wafers have excellent mechanical strength [29]. A drawback is the considerable energy required for the high-vacuum hydrogen implantation process.

In the past, wafer sizes have also increased to reduce production costs. Larger $210 \times 210\,\mathrm{mm}^2$ wafers are expected to be introduced in 2017, but the current $156 \times 156\,\mathrm{mm}^2$ size will be the norm until at least 2020 [13], because larger and thinner wafers will be too brittle to handle with current processing techniques. In fact, thinner wafers already put considerable constraints on cell design and processing, as, for instance, front-to-rear interconnection, soldering, and high-temperature

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processing will result in high yield losses for currently used processes and module architectures.

2.3. Cell processing

Surface recombination becomes more important as the wafer thickness decreases, so very high quality passivation schemes are needed. Because the aluminum back surface field does not passivate well enough and the contact area has to be reduced, a transition to rear-side dielectric passivation is required. Excellent results have recently been achieved on thermal SiO_2/plasma-enhanced chemical vapor deposition SiN_x stacks [31], but thermal growth of SiO_2 might be less favorable for very thin wafers. A relatively new low-temperature approach to high-quality passivation is atomic layer deposition of Al_2O_3 [32], with recombination velocities as low as 2 cm/s on n-type float-zone wafers [33]. Another effective low-temperature approach is to use amorphous silicon (a-Si), as in a-Si : H/crystalline silicon heterojunction (HIT) cells [34]. The HIT and effective passivation increase the open circuit voltage significantly: an efficiency of 23.7% has already been achieved on a 98-μm-thick wafer [35]. As the patent on HIT technology has expired, it can be expected that by 2020, other manufacturers will also make use of this approach.

Because front-to-rear interconnection and soldering of interconnects will induce too much stress on thin wafers, the International Technology Roadmap for Photovoltaics (ITRPV) roadmap expects 35% of all cells to be rear contact by 2020 [13]. There are three main approaches to rear-contact cells [36]: metal wrap-through (MWT), emitter wrap-through (EWT), and back-junction (BJ). In the first two approaches, the emitter is still at the front of the device, but holes are laser drilled through the wafer that transports carriers to the rear, either through the metal contacts (MWT) or the emitter (EWT). The main difference between MWT and EWT is thus that the MWT still has grid lines (but no bus bars) on the front surface. In a BJ cell, the emitter is located at the rear surface, typically in an interdigitated fashion with the back surface field (BSF). A BJ has the benefit that the contacts can cover almost the whole rear side of the cell, greatly reducing series resistance [37]. All three approaches reduce contact shading, although this is especially true for the EWT and BJ types. So far, large-area efficiencies of 24.2% have been reached on BJ solar cells [38] and over 20% on MWT cells [39]. An interdigitated back contact silicon (IBC) HIT cell (IBC-HIT) has been reported at an efficiency of 20.2% [40], but simulations show that 26% conversion efficiency is achievable [41].

Traditional screen printing is reaching its limits too. It is a "hard contact" technique, which creates yield issues on thin wafers. Furthermore, the aspect ratio of fingers is rather low, resulting in either large contact areas (which are high surface recombination areas) or small contacts with high resistance. Finally, the cost of silver in the metallization paste is becoming quite high, at 6–14 ¢ per Wp today [42]. All in all, this implies a move away from silver screen printing in the coming years. A first step may be the introduction of stencil printing, providing higher aspect ratios than screen printing, but the preferred option on the somewhat longer term seems to be plating of copper contacts [42].

Reducing the wafer thickness relaxes the demands on the bulk diffusion length for efficient carrier collection but at the same time reduces the amount of light absorbed if no additional light trapping measures are taken. Random pyramidal textures are shown to perform quite well even at 50 μm wafer thickness, with demonstrated efficiencies of over 19% [43]. Such thin cells with inverted pyramidal textures have even shown efficiencies of up to 21.5% [44,45] and could be further improved with BJ schemes and better passivation. Below 40 μm, the absorption starts dropping rapidly, and for very thin wafers, dielectric [46,47] or plasmonic resonators [3,48] may be required for high efficiencies.

2.4. Encapsulation

The encapsulation step is responsible for most material and labor costs: it accounts for 30–40% of the total costs per Wp [9,10]. Hence, there is much to gain by cutting down on material consumption and through automation and increasing throughput.

Front-to-rear interconnection through stringing and soldering is responsible for a large fraction of the yield losses today, and with decreasing wafer thickness, this may get worse. As back-contact cells require an interdigitated conductive pattern on the back sheet, these interconnection yield losses can be prevented. Späth *et al*. have already developed a fully automated high-throughput module assembly line that drastically reduced cell breakage, even on 130-μm wafers [49]. Because for BJ cells most processing is on the back of the cell, it is possible to attach the wafers to a glass superstrate after processing of the front [50]. This then allows for monolithic processing of the cells, which increases the yield of very thin wafers during cell processing.

Another approach is to eliminate foil lamination all together [51]. Modules are sealed in double glazing at room temperature. An automated module assembly line based on this process, which also eliminates soldering, was first offered by Apollon Solar [52] and produced a module every 2 min. More recently, Bystronic Glass introduced a system that reportedly can produce a module every 45 s [53] (but with soldering). These throughputs are incredibly high compared with conventional module encapsulation processes, while material consumption is reduced and recycling becomes easier.

2.5. Technological scenarios

On the basis of the developments described in the previous subsections, we have defined three modules, as shown in Table I and Figure 1. Module 1a is a very high efficiency scenario based on 120-μm-thick $156 \times 156\,mm^2$ MWSS wafers and an IBC-HIT design with dielectric stack passivation, random pyramidal texture on the front surface, and plated copper contacts. As shown in Table I, high cell and module yield are assumed because of advances

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Table I. Description of the three technological scenarios under investigation.

Process step	Module 1a	Module 1b	Module 2
Feedstock	Poly-Si		UMG-Si
Crystallization	Czochralski ingot growth		Seeded DS
Ingot yield (%)	95	95	95
Good Si out/Si in (%)	85	85	85
Wafering	MWSS	Ion implantation	MWSS
Wafer thickness	120	40	120
Kerf loss	120	0	120
Yield (%)	90	98	90
Cell processing	IBC-HIT design, random pyramidal texture, plated copper contacts.		Metal wrap-through design, random texture, front and rear passivation, plated copper contacts.
Yield (%)	99	99.5	99
Efficiency (%)	23.5	22.5	20
Module assembly	Frameless encapsulation without lamination foil [51], with all-rear low-stress interconnection and high packing density.		
Yield (%)	99.5	99.5	99.5
Efficiency (%)	22	21	19

UMG-Si, upgraded metallurgical grade silicon; DS, directional solidification; MWSS, multiwire slurry saw; IBC-HIT, interdigitated back contact silicon heterojunction.

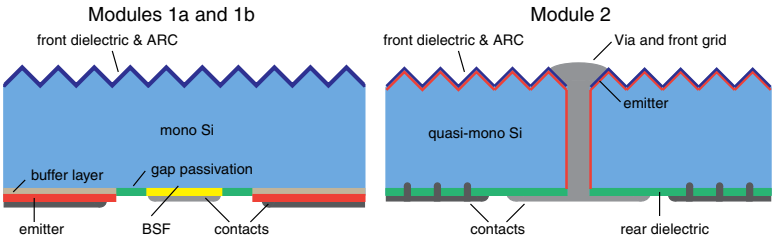

Figure 1. Schematic structure of the three modules. Modules 1a and 1b only differ in the wafer thickness, 100 and 40 μm, respectively. Both are interdigitated back contact heterojunction cells with plated copper contacts. Module 2 is a metal wrap-through cell based on quasi-mono wafers with plated copper contacts. The schematics of modules 1a/b are based on [40] and of 2 on [39]. BSF, back surface field.

expected in monolithic cell processing and module assembly [13], whereas ingot and wafer yields are assumed to be the same as today. Because efficiencies of 23.7% have already been achieved on 100-μm-thick front contacted HIT cells [35], but results on IBC-HIT are not quite that high yet, we estimate the efficiency to be 23.5%. Because of high packing densities and antireflection coated glass, we estimated the difference between cell and total area module efficiencies to be 1.5% absolute, down from 2.5 to 3% for today's high-efficiency modules.

Module 1b is a slight modification of 1a: Wafering is now carried out through light ion implantation, as in Silicon Genesis' PolyMax process [29]. Wafers from this process are stronger mechanically, which is why we have assumed higher yields. Furthermore, the wafers are much thinner, at 40 μm, which comes at an efficiency penalty of at most 1% absolute [45].

Module 2 is a low-cost alternative based on UMG-Si feedstock and $156 \times 156\,\mathrm{mm}^2$ quasi-monocrystalline wafers. Because of the poorer quality material, we chose an MWT cell design, with random texturing on the front, front/rear passivation, and plated contacts. The efficiency for this cell is 20%, based on promising UMG-Si and MWT results and ITRPV projections [13]. Because these wafers are square, we took the efficiency loss between cell and total module at 1% absolute, even lower than in modules 1a and b.

All modules are encapsulated in a double glazing type of process, without lamination foil or curing [51]. This is a high-throughput process that is symbolic of new module

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assembly techniques, but as with the cell designs, there is large uncertainty on whether this is the direction the market will go. We will therefore discuss other possibilities of cell design and encapsulation in the discussion (Section 6.2).

3. PROSPECTIVE LCA

To obtain an idea of the environmental impacts of these modules, we performed a prospective LCA. LCA is a methodological tool to evaluate a product's environmental impact over its life cycle, from primary resource extraction (cradle) to disposal (grave) or recycling. For PV energy, a guideline is provided by IEA PVPS task 12 [54], and a general guideline can be found in Reference [55]. An LCA is typically performed in four stages: (i) scope definition, (ii) life cycle inventory analysis, (iii) impact assessment, and (iv) interpretation. We used SimaPro 7.3.2 as the software tool to perform the inventory analysis and impact assessment [56].

The functional unit is one m^2 module area of the three modules introduced in the previous section, and the system boundaries are shown in Figure 2. Our prospective analysis focuses only on the cradle-to-gate stages of the modules, excluding the BOS and end-of-life stage. However, to make comparisons with system EPBT targets, we accounted for the BOS assuming static scenarios in the discussion.

3.1. Data collection, modeling, and inventory analysis

The life cycle inventory analysis is performed using the Ecoinvent database (version 2.2) (Ecoinvent Centre, St. Gallen, Switzerland) [57] for material and energy inputs. For electricity inputs, we used the continental European electricity mix, which has a conversion efficiency of 0.315. The primary energy requirement is calculated using the cumulative energy demand (CED) (v. 1.08) method [58] in units of MJp.

In the inventory, we have used as much original data as possible. As shown in Table II, we used new data from four different companies and complemented that with data published in literature and from the Ecoinvent database. In two cases, the HIT formation step and conductive patterning of the back sheet, data were unavailable and modeling was required.

For the HIT formation, we used general data on Oerlikon's KAI-1200 a-Si plasma-enhanced chemical vapor deposition chamber [59] (Table III), which can deposit the a-Si layer on 40 1.43 m^2 modules per hour, in two batches of 20 modules. With a deposition speed of 0.3 nm/s and an a-Si : H layer of 300 nm, it follows that the KAI-1200 requires 800 s of loading, unloading, and starting up per batch.

We modeled a device structure as described in [18], with a 5-nm intrinsic buffer layer under the emitter. The process flow is based on [60]: the starting point is a wafer with a passivation layer, which is to be etched away in the regions where the emitter and BSF are deposited. Then, an additional mask is put in place for deposition of the intrinsic layer and emitter, after which the mask is changed for deposition of the BSF. We have assumed that each mask change requires half the time it takes to fully load or unload the chambers. Because vacuum and heater equipment are responsible for most of the power consumption, and are always on, we use the average power consumption for each process step.

The deposition and patterning of a conductive layer on the back sheet were modeled as follows: (i) vapor deposition of a thin metal layer on a glass sheet, (ii) copper plating of that thin metal layer, (iii) screen printing of an etch-resist resin in an interdigitated pattern on the metal layer, (iv) etching, and (v) washing. The vapor deposition process data were obtained from the Ecoinvent database, whereas the other steps are taken from cell processing steps (Table II).

3.2. Impact assessment

We have chosen to calculate the embodied energy, or CED for the production of one m^2 of module, which we will present as such. Additionally, we will present the EPBT, defined as the ratio of the CED over the primary energy that the PV system prevents from being consumed on the grid to which it is connected:

$$EPBT = \frac{E_{\mathrm{CED}}}{G\eta_{\mathrm{conv}}PR}\eta_{\mathrm{grid}} \quad (1)$$

where E_{CED} is the CED required for the production of 1 m^2 of module, η_{grid} is the conversion efficiency of the grid in which the PV system is installed (0.315), G is the annual insolation for southern Europe (1700 kWh/(m^2*yr), η_{conv} is the PV module conversion efficiency, and PR is the system performance ratio. Following the IEA PVPS guideline [54], we assumed a PR of 0.75 for rooftop residential systems, but we will discuss how higher PRs affect the EPBT in the discussion.

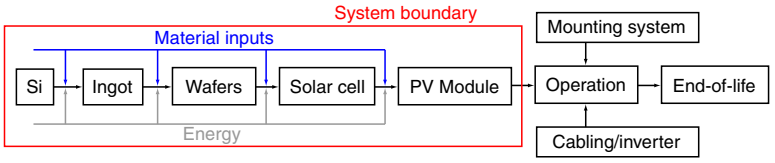

Figure 2. System boundaries used in the inventory analysis.

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Table II. Primary energy data values and sources.

Process step	Key inputs	Value	Source (year)
Feedstock	Poly-Si, Siemens process (Wacker, Germany)	545 MJp/kg	Wetzel, Feuerstein [16] (2011)
	UMG-Si (Elkem Solar, Norway)	322 MJp/kg	De Wild-Scholten, MJ [62] (2008)
Crystallization	CZ-Si electricity use	85.6 kWh/kg Cz-Si	Ecoinvent [63] (2007)
	Quasi-mono Si electricity use	19.3 kWh/kg quasi-mono Si	Multi-Si from Ecoinvent [63] (2007)
	Other		Ecoinvent [63] (2007)
Wafering (MWSS)	Electricity (including cooling), wire, and slurry consumption	Confidential	Applied Materials [64] (2012)
	Other		Ecoinvent [63] (2007)
Wafering (ion implantation)	Electricity requirement for total process	51.4 kWh/m^2	SiGen [65] (2012)
Cell processing	Plating of contacts	Confidential	Meco [66] (2012)
	IBC-HIT deposition	44.5 MJp/m^2	Modeled based on Photon International [59] (2011)
	Various process steps		Photon International [67] (2009)
Encapsulation	Solar glass (front 3.0 mm, rear 2.8 mm)	14.6 kg/m^2	ITRPV [13] (2012)
	Conductive back sheet (without glass)	66.7 MJp/m^2	Modeled based on Ecoinvent [57] (2007) and Meco [66] (2012)
	Other		Apollon Solar [68] (2010)

UMG-Si, upgraded metallurgical grade silicon; MWSS, multiwire slurry saw; IBC-HIT, interdigitated back contact silicon heterojunction.

The EPBT is a widely used measure to indicate the energy performance of PV. It is attractive for a number of reasons: it relates the somewhat abstract CED to the module performance and it is a proxy for environmental performance. Furthermore, less data is required than for the calculation of emissions per kWh. On the other hand, it has drawbacks too: it does not take into account the PV module lifetime, it is inherently linked to the system in which the PV system is installed (through the grid conversion efficiency [61]), and it does not compare easily with other sources of electricity. An alternative metric that accounts for the life expectancy of the system is the EROI, defined as [70]:

$$EROI = \frac{E_{\text{out}}}{E_{\text{inv}}} = \frac{E_{\text{out}}}{E_{\text{ED}} + E_{\text{PP}}} \tag{2}$$

where E_{out} is the net electricity output over the product's lifetime, E_{inv} is the total invested primary energy required to produce that electricity, that is, the sum of the primary energy required for the production of the product (E_{PP}) and energy for the supply chain of the feedstock to produce the electricity (E_{ED}). Note that the EROI as defined here equals the life expectancy of the PV system multiplied by the grid efficiency and divided by the EPBT.

After the impact assessment, we move on to the next, and final, stage of the LCA: interpretation. Because of the prospective nature of this study, a thorough uncertainty analysis is required.

4. UNCERTAINTY ANALYSIS

We can distinguish between various sources of uncertainty in LCA [71]. First and foremost, there is parameter uncertainty: Parameters can be hard to measure precisely or precise values might be unavailable, and they might be inherently variable. Then, there is scenario uncertainty, which is related to the normative choices made in constructing scenarios. The last source is modeling uncertainty, which comes from the structure of the model.

Because of the prospective nature of this study, parameter and scenario uncertainty are most significant: Data are subject to change in the coming years, and the scenarios that we have developed may not represent the actual situation in 2020. Our approach to deal with these uncertainties is discussed as follows.

4.1. Parameter uncertainty

A prospective LCA study has two major data quality issues: data representativeness (e.g., scaling up from laboratory scale or temporal fluctuations in primary energy requirements for material inputs) and data availability (e.g., confidential or nonexistent data, which therefore have to be modeled). The challenge is to quantify these

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Table III. Modeling of interdigitated back contact silicon heterojunction deposition.

Process parameters	Value	Source
a-Si deposition rate	0.3 nm/s	Photon International [59]
Average power consumption	280 kW	Photon International [59]
Loading or unloading	400 s/batch	See Section 3.1
Changing masks	200 s/batch	Own estimate
Total process time	1433 s/batch	Own estimate
Energy and material consumption		
Electricity	3.9 kWh/m^2	Own model, Photon International [59]
SiH_4	0.97 g/m^2	Van der Meulen, R, and Alsema, EA [69]
H_2	1.45 g/m^2	
O_2	0.16 g/m^2	
NF_3	0.11 g/m^2	

uncertainties in a transparent manner, for which the most common approach is to use a pedigree matrix approach, as in the Ecoinvent database [72]. Here, the assumption is made that all inputs are accurately described by a log-normal distribution. The variance of this distribution is a measure of the uncertainty of the input and is found using a pedigree matrix with data quality indicators [72,73]. There are five data characteristics on which this variance is based: (i) data reliability, (ii) data completeness, (iii) temporal correlation, (iv) geographic correlation, and (v) further technical correlation. Each characteristic is divided into five quality levels, ranging from good to poor. On the basis of expert judgment, the indicator scores then give the variance of the input value. In Table IV, we show the pedigree matrix for the two most important characteristics in prospective studies (temporal and technological correlation).

A useful measure of the uncertainty of an input is the 95% confidence interval: a range in which the true value will lie with 95% certainty. The confidence interval is related to the input variance and is thus calculated on the basis of the pedigree matrix, as outlined in [72]. For example, the electricity use for production of Cz-Si comes from the Ecoinvent database. The input value of 85.6 kWh/kg is based on verified measurements (score 1 on reliability) but comes from only one site relevant for the market (score 4 on completeness). It is valid for the year 2007 (temporal score 4), comes from an area with similar production conditions (geographical score 3), and is representative for enterprises, processes, and materials under study (technological score 1). Following the procedure outlined in [72], the 95% confidence interval of the electricity requirement for a kilogram of Cz-Si in 2020 then ranges from 69.7 to 105 kWh/kg Cz-Si. It should be noted, however, that the electricity requirement is more likely to move toward the lower bound because of technological improvements.

Using the same procedure, we have calculated the variances of all inputs and then propagated these using Monte Carlo analysis [74] to find the 95% confidence interval of the CED, EPBT, and EROI for each module.

4.2. Scenario uncertainty

The technological scenarios and performance forecasts that we have made are subject to uncertainty too. For instance, cell and module efficiencies might be higher or lower than we predicted, so we will present the EPBT and EROI results on an efficiency interval. We have based our yield assumptions on the values reported in the ITRPV roadmap [13], which are based on expert judgment. We address the yield uncertainty through parameter uncertainty, as described in the previous subsection: industrial expert estimates receive a data quality indicator score of 4 for reliability. Together with the other indicator scores, one can find the variance and 95% confidence interval of the yield assumptions, as outlined in [72]. For example, the yield during cell processing is reported to be 99% by 2020. This means that for 1 m^2 of cells, 1.01 m^2 of wafers is required, but the 95% confidence interval lies between 1.008 and 1.012 m^2. The uncertainty on process yields is then propagated just as the other parameter uncertainties.

Table IV. Excerpt of the pedigree matrix [72], adjusted to have 2020 as the database base year.

Indicator score	1 (Good)	2	3	4	5 (Poor)
Temporal correlation	—	—	Data from 2010 or later.	Data from 2005 or later.	Data from before 2005.
Further technical correlation	Data from enterprises, processes, and materials under study.	Data from processes and materials under study but different enterprises.	Data from processes and materials under study but from different technology.	Data on related processes or materials.	Data on related processes on laboratory scale or from different technology.

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Finally, crystalline silicon PV modules might be produced by processes in 2020 that are unknown today or that we did not account for in our scenarios: we address these possibilities in Section 6.2.

5. RESULTS

On the basis of the life cycle inventory, we calculated the cradle-to-gate (factory) primary energy consumption for production of the three modules, including the 95% confidence interval, as shown in Figure 3(a) (in primary energy requirement per m^2 of module). To put these values into context: the most recent LCA results for multicrystalline and monocrystalline silicon PV modules are 2150 and 2750 MJp/m^2, respectively [16], so the CED of modules 1a, 1b, and 2 are only 74% (2030/2750), 55% (1500/2750), and 62% (1330/2150) of the corresponding CEDs today.

The CED of module 1a is considerably higher than that of modules 1b and 2. The breakdown in Figure 3(b) shows that this is almost solely due to the relatively high consumption of monocrystalline silicon. Moving toward a kerfless cutting method drastically reduces silicon consumption, by a factor of five, but at the same time, the wafering energy is increased because of the energy intensive ion implantation process. Modules 1a and 2 require the same amount of feedstock, but the UMG-Si feedstock and seeded DS reduce the primary energy requirement for this step by almost a factor of three (although this comes at an efficiency penalty). Because we only investigated a double glazing-like encapsulation process, all modules have the same encapsulation energy.

The breakdown for the aforementioned recent LCA results on monocrystalline silicon modules into poly-Si, ingot growth and wafering, cell processing, and encapsulation is approximately 500, 1260, 390, and 600 MJp/m^2 (or 18%, 46%, 14%, and 22%), respectively [16]. Comparing this with the breakdown shown in Figure 3(b), we see that in module 1a, modest reductions have been achieved in feedstock, crystallization and wafering (owing to thinner wafers), and encapsulation. The cell processing energy requirement has not changed much, most likely because low-temperature processing has offset increases due to the increased overall process complexity. As mentioned before, poly-Si consumption is drastically reduced in module 1b, and module 2 uses low-energy feedstock. Because module 2 is based on quasi-mono wafers, the energy requirement here is reduced further (the corresponding energy requirement for ingot growth and wafering in 2011 in a multi-Si module was ~670 MJ_p/m^2 [16]).

The confidence intervals are quite large: [1560, 2660], [1110, 2010], and [1060, 1650] MJp/m^2 for modules 1a, 1b, and 2 respectively (Figure 2(a)). This is mainly due to the temporal uncertainty: About half (or even 63% for module 1a) of the primary energy requirement comes from poly-Si feedstock, ingot growth, and wafering, and these production steps have a large potential for reduction in energy intensity by scaling up. We therefore expect the actual CED to decrease toward the lower bound rather than increase.

We also calculated the EPBTs for these modules (Figure 4(a)). The mean payback time of module 1a is just over 0.6 years, whereas 1b and 2 have an EPBT just below than 0.5 years. As is common today, there is a gap between multi-Si and mono-Si for traditional wafers, but by using thin, kerfless cut wafers, this gap closes. The most recent module EPBT values are 1.3 for mono-Si and 1.1 for multi-Si [16], so a reduction in the EPBT of over a factor two is feasible by 2020—or even more if we take into account the potential to move toward the lower bound of the confidence interval. Aside from the reduction in CED of the three modules, the considerable increase in module efficiency is an important factor in the EPBT reductions.

In Figure 4(b), we show the EROI of produced electricity for a lifetime of 35 years [15]. It is by using the same data as for the comparison of CED [16], but with a lifetime of 30 years, that the EROI for multi-Si and mono-Si PV

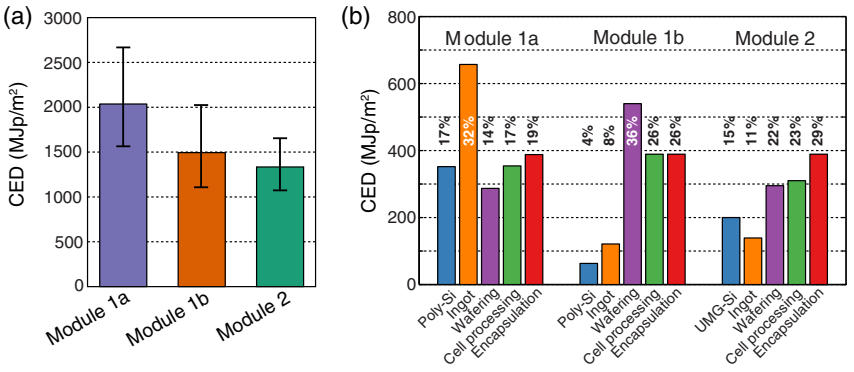

Figure 3. (a) Cumulative energy demand (CED) per m^2 and (b) Breakdown into feedstock, ingot, wafering, cell processing, and encapsulation steps. The percentage shows the contribution of each process step to the total CED. UMG-Si, upgraded metallurgical grade silicon.

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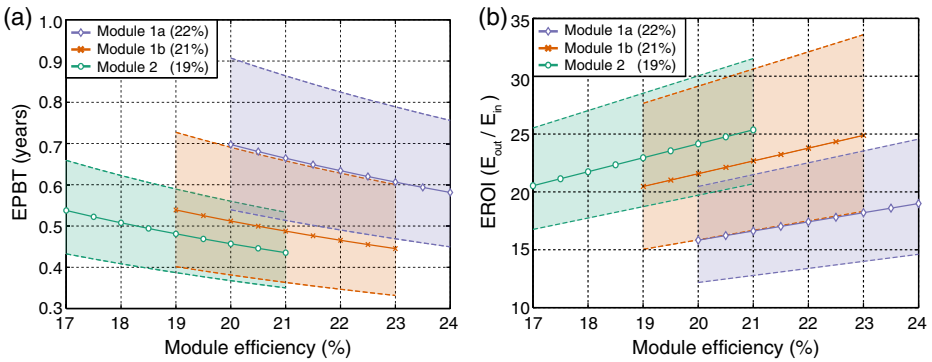

Figure 4. (a) Module energy payback time (EPBT) over efficiency range (with the estimated efficiency given in the legend), where the solid line is the mean, and the shaded area gives the 95% confidence interval. (b) Module energy return on energy investment (EROI) over efficiency range. We assumed a life expectancy of 35 years and an insolation of 1700 kWh/(m^2*year).

modules from 2011 is 8.8 and 7.5, respectively, so the EROI of crystalline silicon PV modules will increase dramatically in the coming years.

6. DISCUSSION

As we mentioned before, prospective LCA studies are subject to parameter and scenario uncertainties. We will discuss those uncertainties in the next two subsections and then conclude this section with a brief discussion of the BOS components.

6.1. Parameter sensitivity

In addition to the uncertainty analysis that we included in our results, it is important to check if our results are overly sensitive for certain input parameters. As we mentioned in Section 3.2, the PR is one of these parameters: currently taken at 0.75, it might well be underestimated significantly and values of 0.9 are feasible [75]. If the PR were to increase to 0.80, 0.85, or 0.90, this would further reduce the EPBT of the modules by 6%, 12%, or 17%, respectively. With a PR of 90%, the lowest EPBT would be 0.4 years (for module 2).

To check for sensitive inputs in the LCI, we calculated how much the module's CED would change if the input value were to move to the upper bound of the 95% confidence interval. The top three inputs to which the results are most sensitive are shown in Table V. For example, with 7%, the electricity requirement for Cz ingot growth is the most sensitive input for module 1a. This means that if the electricity requirement were to increase to the upper bound of the input's 95% confidence interval by 2020, the total CED of module 1a would increase by 7%. In other words, regarding the Cz electricity requirement, we are 95% sure that module 1a's CED lies within an interval of approximately ±7%.

In this section, we will explicitly deal with the kerfless cutting energy and the Cz crystal growth electricity consumption. Note that the process steps that we modeled have high uncertainty but account for only a small share of the total primary energy demand, and therefore, the final CED can be considered insensitive to these inputs.

Although we have first-hand data from Silicon Genesis on the energy requirement for ion implantation wafering, it is a new technology. Pilot production is running since 2009 but not yet at full capacity [29], and the energy requirement per wafer might therefore be subject to considerable change in the future. In Figure 5(a), we show the 95% confidence interval of the ion implantation wafering electricity requirement for 50 μm wafers, but variation over this interval only results in a 5% decrease at the lower bound or a 6% increase at the upper bound of the CED and EPBT. The energy intensity usually decreases as a technology matures, so we expect that changes will be for the better.

Module 1a is particularly sensitive to the electricity requirement for Cz crystal growth: the input share is large (almost 30%), the data are old (published in 2007), and the data already had a relatively high uncertainty to start with. Over the confidence interval for Cz-Si electricity consumption, the CED and EPBT of module 1a range from 94% on the lower bound to 107% on the upper bound

Table V. The top three most sensitive inputs for the three modules, with the influence on the total CED that the inputs have if they shift to the upper bound of their 95% confidence interval.

	Module 1a	Module 1b	Module 2
1	Cz electricity requirement (7%)	Wafering electricity demand (6%)	Solar glass (4%)
2	Poly-Si feedstock (5%)	Solar glass (3%)	UMG-Si feedstock (4%)
3	Solar glass (3%)	ARC deposition (3%)	DS electricity requirement (3%)

CED, cumulative energy demand; UMG-Si, upgraded metallurgical grade silicon; DS, directional solidification; ARC, antireflection coating.

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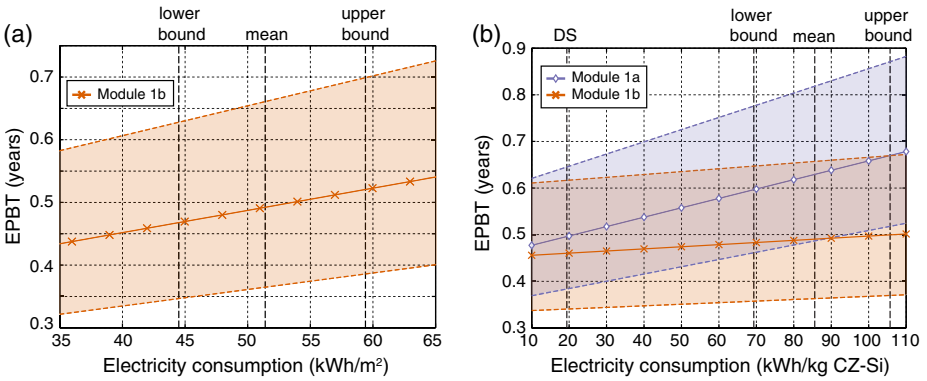

Figure 5. (a) Sensitivity analysis for ion implantation wafering energy requirement for module 1b and (b) sensitivity analysis for modules 1a and 1b on the electricity requirement for Cz crystal pulling. The vertical dashed lines show the lower and upper bounds of the 95% confidence interval, and the mean value, which is used in our inventory. In (b), the vertical dashed line marked "DS" signifies the energy consumption for directional solidification.

compared with the mean. Figure 5(b) shows the impact of the electricity requirement per kilogram Cz-Si on the EPBT of modules 1a and 1b. It is quite clear that the impact on module 1b is modest, because the input share for that module is just 7%. The dashed line on the left in Figure 4(b) shows the electricity requirement per kilogram Si for DS, which is lower than 20 kWh/kg. We show this because it is representative for quasi-mono feedstock, which according to the ITRPV will have a market share of almost 50% in 2020 [13]. If quasi-mono ingots can replace Cz ingots, this will result in a substantial reduction in the EPBT of module 1a: over 22%. Even if the use of quasi-mono ingots comes at an efficiency penalty, the reduction in electricity requirement will be beneficial. It must be noted, however, that BJ solar cells require very high carrier lifetimes, and at this point, it is uncertain whether such demands can be met on quasi-mono wafers. This is why, in the ITRPV roadmap, quasi-mono is projected to replace multi-Si wafers (and hence is used in module 2), whereas the mono-Si share remains practically constant.

To conclude, the primary energy requirement for the production of electricity is a very sensitive parameter, as other authors have pointed out [61,76]. In this study, we used the average continental European grid electricity mix, which has an efficiency of 31.5%. However, the grid efficiency varies between countries and changes over time. For example, if PV reaches a 20% penetration of the grid, the grid efficiency will increase to roughly 41% [61]. As Figure 6(a) shows, this increases the EPBT because less primary energy consumption is prevented by displacing grid mix electricity with electricity from a PV module. On the other hand, it also reduces the primary energy requirement for module production, which causes the EROI to increase, as shown in Figure 6(b). For these figures, we have assumed that the poly-Si feedstock is not produced with grid electricity but with on-site power generation, and hence that share of the CED is not affected by a change in grid efficiency. In reality, poly-Si is often produced using power from a mix of gas and steam turbines, hydro, and the grid. It is noted that if poly-Si production in the future increasingly uses coal-based electricity, EPBTs and emissions will worsen.

6.2. Scenario uncertainty

Sources of scenario uncertainty include diamond wire sawing, encapsulation methods, double-sided contact cells, and passivation methods. Starting from the latter, Al_2O_3 is a promising candidate for high-quality passivation, but lacking data, we used data for SiN_x passivation. Even though SiN_x passivation does not reduce the surface recombination velocities enough for high efficiencies, the energy this deposition process requires will be similar to (or higher than) Al_2O_3 deposition, and any difference will not significantly influence the final results because the input share is low.

Although we only investigated rear-contact modules, the ITRPV expects 65% of the market share to still be double-sided contact modules in 2020 [13]. This will primarily result in lower packing densities, as efficiencies of 23.7% have already been shown on double-sided HIT cells and module 2 already has a contact grid on the front, so the efficiency penalty from the additional bus bars is small.

There are two sources of scenario uncertainty that we believe could significantly impact the outcome. The first is fixed abrasive sawing with diamond-particle-coated wires. According to the ITRPV, by 2020, 100% of mono-Si and 80% of multi-Si wafers will be sawn with diamond-coated wires, thus almost completely replacing slurry-based wire sawing [13]. Using diamond-particle-coated wires results in higher throughput, lower sawing energy consumption, kerf width reduction, kerf recycling, and lower wire consumption. With data from NorSun [77] and Garbo [78], we have calculated that this results in a 29% reduction in the primary energy requirement per

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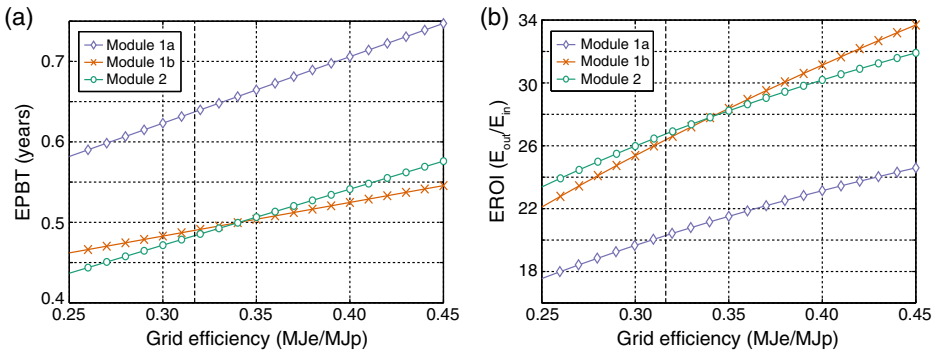

Figure 6. The influence of the grid efficiency, the produced electricity (MJe) per consumed primary energy (MJp), on (a) the module energy payback time (EPBT) and (b) the module energy return on energy investment (EROI) of the three technological scenarios. The vertical dashed line shows the European electricity mix grid efficiency used in this study.

120-μm-thick monocrystalline wafer or to an *EPBT* of 0.5 years for module 1a. Unfortunately, no diamond-wire producer was willing to share data with us because of their highly competitive business environment, so we could not include a diamond-wire cutting scenario in our study.

The second source of significant scenario uncertainty is the encapsulation method. We used a high-throughput encapsulation process that does not require foil lamination, but it may very well be that, for instance, an interdigitated interconnection scheme can only successfully be integrated on foil. From [16], we calculated that the additional primary energy requirement for the conventional encapsulation method with only one glass sheet, but with EVA, Tedlar, and curing is about 190 MJ_p/m^2. This would increase the EPBT of modules 1a, 1b, and 2 by 9%, 13%, and 15%, respectively.

6.3. Balance of system

Although the BOS lies outside of the scope of this investigation, it is a crucial part of any PV energy system, and we will therefore briefly discuss its impacts on our results. One can distinguish between two common types of grid-connected PV systems: building-integrated systems (e.g., rooftop panels) and ground-based systems (e.g., large-scale centralized power plants). In Table VI, we show the EPBT and EROI for both types of system, calculated with data from [79]. The rooftop system consists of a 2.5-kW inverter and a Schletter mounting system. The PV plant uses average mounting structure data from market surveys and inverter data based on a 4.6-MWp plant in Tucson, USA. For the large-scale PV plant, a *PR* of 0.80 is used [56]. An extensive discussion of the EROI of PV systems in relation to other sources of electricity is given in [70].

To reduce costs associated with the BOS, the EUPVTP has identified some research priorities [15]. For the EPBT, the most relevant goals are an increase in the inverter lifetime (of over 30 years by 2025 compared with 15 years now) and low-cost support structures, cabling and electrical connections. As Table VI shows, the inverter accounts for a considerable share of the CED of rooftop systems, and even a modest increase in the inverter lifetime would therefore significantly decrease the system EPBT. The inverter is less important in the case of large-scale PV plants, where the support structure dominates the CED.

7. CONCLUSION

In this work, we presented a prospective life cycle analysis of crystalline silicon PV technologies in the year 2020. To do so, we developed three technological scenarios (two based on monocrystalline silicon and one based on

Table VI. The primary energy consumption of the BOS components for two types of PV systems and the EPBT and EROI on a system level.

	Rooftop			Grount-mount PV plant		
Module	1a	1b	2	1a	1b	2
Structure, cabling (MJ/m^2)	225	225	225	645	645	645
Inverter (MJ/m^2)	704	675	614	254	243	222
Total (MJ/m^2)	929	900	839	899	888	867
EPBT (years)	0.9	0.7	0.7	0.8	0.7	0.7
EROI (E_{out}/E_{in})	13	15	15	14	16	16

BOS, balance of system; PV, photovoltaic; *EPBT*, energy payback time; *EROI*, energy return on energy investment.
Data comes from [78].

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quasi-monocrystalline silicon), building on various existing roadmaps. To summarize, increasing the cell efficiency is (after scaling up) the most important lever to reduce energy demand and costs. By using high-quality passivation and BJs, higher efficiencies can be achieved while simultaneously reducing the wafer thickness, which reduces the embodied energy even further. However, thinner wafers also require novel cell processing and encapsulation schemes, which we accounted for. We forecast that the EPBT of crystalline silicon modules can be reduced to 0.5 years or less (below 0.7 years when including BOS). This confirms that the European Photovoltaic Technology Platform's target of 0.6 years at the system level may be too ambitious, but the IEA target of 0.9 year will be met. The EROI of PV modules is expected to increase further by a factor two to three in the coming years.

This is a prospective LCA, subject to technological improvements taking place, and as such, it carries a considerable degree of uncertainty. To address parameter uncertainty, we present results with a 95% confidence interval, but scenario uncertainty remains: crystalline silicon modules in 2020 may be based on technologies or production methods that we did not include in our scenarios, such as diamond-particle-coated wire sawing for wafering. Because the general tendency of maturing technologies is to become less energy and material intensive and we have used data that are representative of, at best, the situation today, our forecasts can be considered conservative.

Finally, it is important to note that these results cannot easily be compared with other PV technologies, because they too can change over time. Nonetheless, these results show that there is considerable potential to reduce the environmental impact of crystalline silicon PVs while reducing production costs.

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Attachment I-7

Back-Contacted Silicon Heterojunction Solar Cells With Efficiency >21%

Andrea Tomasi, Bertrand Paviet-Salomon, Damien Lachenal, Silvia Martin de Nicolas, Antoine Descoeudres, Jonas Geissbühler, Stefaan De Wolf, and Christophe Ballif

***Abstract*—We report on the fabrication of back-contacted silicon heterojunction solar cells with conversion efficiencies above 21%. Our process technology relies solely on simple and size-scalable patterning methods, with no high-temperature steps. Using *in situ* shadow masks, doped hydrogenated amorphous silicon layers are patterned into two interdigitated combs. Transparent conductive oxide and metal layers, forming the back electrodes, are patterned by hot melt inkjet printing. With this process, we obtain high short-circuit current densities close to 40 mA/cm^2 and open-circuit voltages exceeding 720 mV, leading to a conversion efficiency of 21.5%. However, moderate fill factor values limit our current device efficiencies. Unhindered carrier transport through both heterocontact layer stacks, as well as higher passivation quality over the minority carrier-injection range relevant for solar cell operation, are identified as key factors for improved fill factor values and device performance.**

***Index Terms*—Amorphous silicon, crystalline silicon (c-Si), heterojunctions, photovoltaic cells, solar cells.**

I. Introduction

SILICON heterojunction (SHJ) technology is of high interest for application in solar cells; it combines the use of crystalline silicon (c-Si) wafers as optically active absorbers with thin-film silicon deposition technology for device fabrication [1]. The excellent c-Si surface passivation properties of hydrogenated amorphous silicon (a-Si:H) enable high open-circuit voltages $(V_{\rm oc})$ over 700 mV, as well as excellent low temperature coefficients in finished devices. The promise of this technology was recently further substantiated by Panasonic, Osaka, Japan, which reported conversion efficiencies as high as 24.7%, within the highest ever reached for c-Si-based solar cells of practical size to date [2]. The high level of surface passivation and the fact that SHJ device fabrication avoids any high-temperature processes makes this technology also, particularly, suited for thin wafers [3].

The fill factor (*FF*) and short-circuit current density $(J_{\rm sc})$ values of SHJ devices are comparable with those of typical homojunction devices. Despite the fact that tunneling may play an important role in carrier transport, the *FF* in SHJ devices has been empirically shown not to suffer from any significant fundamental limitation [2], compared with best homojunction technologies as passivated emitter, rear locally diffused [4] and back-contacted [5] solar cells. However, standard two-side contacted front-emitter silicon heterojunction (Std-SHJ) solar cells are limited by parasitic absorption of light, either in the a-Si:H films or the transparent conductive oxide (TCO). These $J_{\rm sc}$ losses are linked to the short-wavelength response of SHJ devices [6]. In the long-wavelength part of the spectrum, well-engineered SHJ devices can outperform the best reported homojunction solar cells [7].

A straightforward step toward higher $J_{\rm sc}$ values and higher conversion efficiencies in SHJ devices consists of the back-contacted architecture, featuring both electron and hole collection contacts at the rear of the solar cell. This cell concept—which is industrially proven by SunPower, Union City, CA, USA, in the case of homojunction devices with conversion efficiencies of up to 24.2% [5]—has the advantage of eliminating front-electrode shadowing. Moreover, in the case of SHJ devices, it brings additional benefits by minimizing or even eliminating parasitic absorption. In back-contacted SHJ solar cells, a front TCO layer is no longer required and the front a-Si:H layers can be tuned, irrespective of their carrier transport properties, solely in regard to their transparency and passivation properties. Actually, substitution of the complete TCO/a-Si:H stack with wider bandgap passivating dielectrics for improved transparency becomes possible.

The potential of back-contacted architectures using SHJ contacts was recently convincingly pointed out by Panasonic, Osaka, Japan, reporting the world's highest energy conversion efficiency of 25.6% for c-Si-based solar cells under 1-sun illumination [8]. This record device exhibits an area of 143.7 cm^2 and demonstrates, in addition to the enormous potentiality of the technology, its scalability to devices of practical size. Based on this new exciting result, back-contacted SHJ is arguably the ultimate device architecture for single-junction silicon wafer-based solar cells. Similarly, another impressive result was recently

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reported by Sharp, Japan; its so-called rear heterojunction emitter plus antireflective passivation layers concept, using interdigitated back contacts, yielded a conversion efficiency of 24.7%, on a cell area <4 cm^2 [9]. Furthermore, a conversion efficiency of 20.5%, on a cell area of 221 cm^2, was reached by LG, Korea [10], again by means of an interdigitated back-contacted silicon heterojunction (IBC-SHJ) device. Always in the field of IBC-SHJ devices, Helmholtz-Zentrum Berlin, Germany, has reported a conversion efficiency of 20.2% [11], whereas several other groups have presented solar cells with conversion efficiencies in the range of 15–20% [12]–[15]. Back-contacted SHJ devices using alternative contacting schemes have been reported as well [16]–[18]. In this case, a maximum conversion efficiency of 17.1% [19], with a rear point-contact scheme, has been shown. It is worth mentioning that the use of *in situ* shadow masks to structure a-Si:H layers in back-contacted SHJ, as proposed in this study, is an approach previously demonstrated; however, so far, only relatively modest device performances were achieved [20]–[23].

The implementation of all back-contact architectures typically adds complexity to the overall fabrication process; indeed, it requires adequate patterning technologies and accurate alignment techniques. In this study, we aimed for the fabrication of high-efficiency IBC-SHJ devices via simple processing technologies and a minimal number of processing steps, comparable with those required for the fabrication of Std-SHJ devices. In the first part of this paper, we describe the cell design and the proposed fabrication technology. In the second part, we analyze the solar cell results that are achieved so far, as well as the factors limiting current solar cell efficiencies.

II. Experimental Details

A. Solar Cell Design and Fabrication Process

In this paper, IBC-SHJ solar cells with 9-cm^2 active cell area were fabricated on 250-μm-thick, n-type, 4-in float-zone (FZ) wafers, with a nominal resistivity of 3 Ω·cm.

Wafer texturing was performed in a potassium hydroxide solution. Following wet-chemical cleaning of the surfaces and a short dip in a diluted hydrofluoric solution, an intrinsic a-Si:H layer and a thin intrinsic/n-type a-Si:H layer stack were deposited on the backside and on the front side of the wafer, respectively. The n- and p-type a-Si:H combs on the backside, needed for, respectively, electron and hole collection, were fabricated via *in situ* shadow masks. All a-Si:H layers were deposited by plasma-enhanced chemical vapor deposition (PECVD); details can be found elsewhere [24]. For the back electrodes, a thick TCO/metal stack was deposited on the full back surface of the cell precursor via physical vapor deposition (PVD). For an antireflection coating on the front side, a hydrogenated amorphous silicon nitride (a-SiN:H) layer was deposited by PECVD at sufficiently low temperature (<200 °C) to avoid annealing-induced degradation of the a-Si:H layers [25]. The TCO/metal stack was then patterned into two interdigitated combs by hot melt inkjet printing of an etch resist that was well aligned with the p- and n-type regions underneath, followed by wet etching of the exposed areas. A final curing step, at a temperature below 200 °C, was performed in a belt furnace. The resulting cell architecture is represented in Fig. 1.

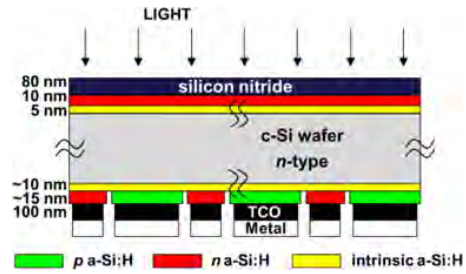

Fig. 1. Schematic of IBC-SHJ solar cell architecture.

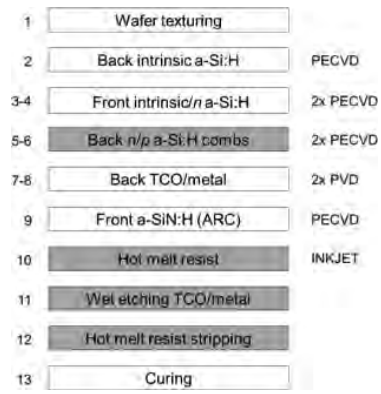

Fig. 2. Proposed IBC-SHJ process flow (patterning steps are highlighted with a gray background).

The overall cell fabrication process relies in total on six PECVD and two PVD steps, some of these without vacuum break, in the same reactor. Counting wafer texturing, hot melt inkjet printing, TCO/metal etching, hot melt stripping, and curing, we end up with only 13 processing steps for our IBC-SHJ processing sequence, to be compared with a total of ten steps required for typical Std-SHJ devices (wafer texturing, four PECVD, and three PVD layers plus metal-paste printing and curing). In Fig. 2, we show the overall process flow of our IBC-SHJ devices.

B. Patterning Techniques and Alignment Methodologies

The IBC-SHJ architecture requires patterning of the back n- and p-type a-Si:H layers and of the back TCO/metal stack. The patterning of the doped a-Si:H PECVD layers is critical due to the high-purity requirements of wafer surfaces during PECVD passivation processes and the need to strictly preserve the high quality of the intrinsic/p-type a-Si:H and intrinsic/n-type a-Si:H interfaces [26]. For patterning the doped a-Si:H PECVD layers, we laser cut masks from c-Si wafers. Alignment between the mask and substrate in the PECVD deposition chamber was achieved by means of an especially designed substrate holder and metal pins. The deposition rate of a-Si:H through 1-mm- (n-type a-Si:H) and 1.4-mm-wide (p-type a-Si:H) mask slits was found to be, respectively, 52% and 12% lower,

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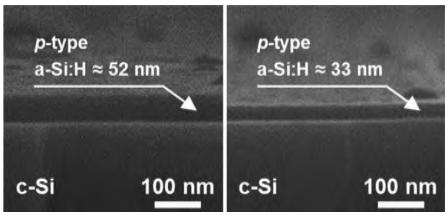

Fig. 3. SEM cross sections of a thick p-type a-Si:H layer on a polished silicon wafer, patterned via *in situ* masking, close to the center (left image) and edge (right image) of the deposited feature, respectively. The deposition rate through a 1.4-mm-wide mask slit is reduced by 12% compared with a full-area PECVD a-Si:H deposition.

compared with full-area PECVD a-Si:H deposition. The reduction of the a-Si:H deposition rate through a mask slit was confirmed by both ellipsometry and scanning electron microscope (SEM) cross-sectional observations. Moreover, SEM micrographs of a thick p-type a-Si:H layer, deposited on a polished silicon wafer through an *in situ* shadow mask, reveal tapering of the a-Si:H layer thickness toward the edge of the deposited feature (see Fig. 3). For patterning the TCO/metal stack, we used hot melt inkjet printing combined with wet etching, as already mentioned. Features as small as 50 μm can be easily achieved via hot melt inkjet printing, enabling the fabrication of IBC electrodes [27]. In our case, the alignment of the hot melt inkjet print over the patterned doped a-Si:H layers was achieved by fiducials laser-marked on the wafer.

We estimate an overall accuracy of ± 15 μm for the positioning of the TCO/metal combs over the mask-patterned a-Si:H layers. The main error sources are linked to laser distortion in marking and mask fabrication, and mask positioning during PECVD processes. In designing the hot melt inkjet etch resist, underetching effects were also considered for accurate patterning. To account for these positioning errors, the width of the TCO/metal comb fingers in our cells is kept narrower than that one of the doped a-Si:H comb fingers underneath. From optical microscopy images, we can evaluate that the TCO/metal electrodes cover the p- and n-type a-Si:H layers by $\sim$89% and $\sim$85%, respectively. However, these coverage fraction values, with respect to those reported in [21] and [28], are underestimated. The very edges of the doped a-Si:H comb fingers are indeed electronically inactive due to the observed thickness tapering effects. The alignment quality can be assessed from Fig. 4, where both a p-type a-Si:H layer and a TCO/metal electrode are visible, whereas an n-type a-Si:H layer is weakly visible.

III. Results and Discussion

A. Interdigitated Back-Contacted Silicon Heterojunction Solar Cell Results

The 1-sun current–voltage (I–V) characteristics of our IBC-SHJ solar cells were measured in-house under AM-1.5G at a temperature of 25 °C. The designated cell area of 9 cm^2 was defined by a shadow mask, excluding the busbar region at the rear. For the following discussion (see Sections III-A and B), we chose a representative 9-cm^2 IBC-SHJ device for which the

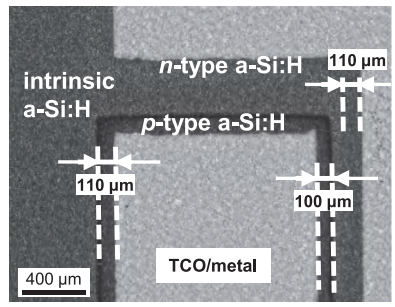

Fig. 4. Alignment quality of doped a-Si:H layers and TCO/metal electrode for use in our IBC-SHJ solar cells. In the area between the doped a-Si:H layers, the textured silicon surface is covered only by an intrinsic a-Si:H layer.

TABLE I
Electrical Parameters and FF Losses of IBC-SHJ (see Sections III-A and B), Best IBC-SHJ (see Sections III-C), and Best Std-SHJ Devices

Parameter	IBC-SHJ (Sections III.A and III.B)	Best Std-SHJ [29]	Best IBC-SHJ (Section III.C)
V_{oc} (V)	0.726	0.727	0.724
J_{sc} (mA/cm^2)	39.5	38.9	39.9
Eff (%)	20.9	22.1	21.5
FF (%)	73.0	78.4	74.5
R^N_{series} (Ω·cm^2)	2.1	1.1	1.3
ΔFF_R_{series} (%)	10.4	5.2	6.6
$\Delta FF_J(n\neq 1)$ (%)	1.6	1.4	3.8

a-Si:H layers, apart from the deposition time, were deposited with the same plasma conditions as in our best certified 4-cm^2 Std-SHJ device [29]. The chosen IBC-SHJ device shows a conversion efficiency of 20.9%, a $V_{\rm oc}$ of 726 mV, and a $J_{\rm sc}$ of 39.5 mA/cm^2. We compare these parameters with those of our best certified Std-SHJ device (see Table I). The achieved $V_{\rm oc}$ of 726 mV is only 1 mV lower than that of our best Std-SHJ device, demonstrating the compatibility of our IBC processing sequence with high-quality a-Si:H passivation layers. The measured $J_{\rm sc}$ of 39.5 mA/cm^2 is 0.6 mA/cm^2 higher than the $J_{\rm sc}$ of our silver-printed best certified Std-SHJ device. Conversely, the IBC-SHJ device FF is 73.0%, which is significantly lower than any typical high-performance Std-SHJ device. Based on spectral response and light-beam-induced current measurements, we link the still relatively modest $J_{\rm sc}$ gain in our IBC-SHJ devices (versus our best Std-SHJ device) to not fully minimized parasitic absorption losses (both in the short- and long-wavelength parts of the spectrum), rather than to electrical shading effects [30], [31]. Further details on this topic will be the subject of future research.

B. Fill-Factor Losses: Interdigitated Back-Contacted Silicon Heterojunction and Best Standard Two-Side Contacted Front-Emitter Silicon Heterojunction Solar Cells

Deviation of the FF of a solar cell from its ideal value is generally the result of loss mechanisms related to charge–carrier

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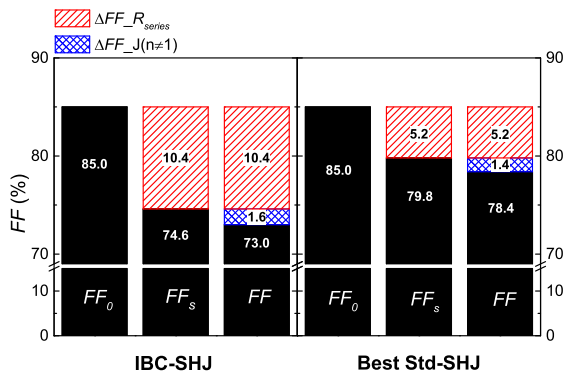

Fig. 5. Charge–carrier transport and recombination influences on solar cell *FF*: Ideal *FF* (FF_0), series-resistance-affected *FF* (FF_s), and measured *FF* (from illuminated *I–V* measurements) of our IBC-SHJ and best Std-SHJ devices [29].

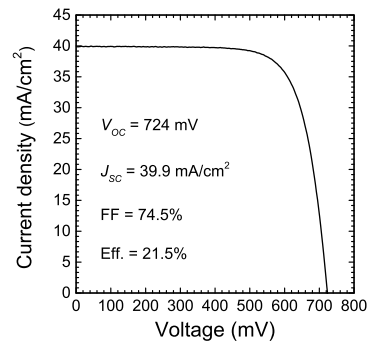

Fig. 6. *I–V* characteristic of the best 9-cm^2 IBC-SHJ device.

transport, as well as carrier recombination processes. Quantitative analysis of such *FF* losses is complex, and carrier-injection-level-dependent effects of these mechanisms can further complicate this type of study. In the following analysis, we calculate *FF* resistance losses using the measured series-resistance (R_{series}) and shunt-resistance (R_{sh}) values and estimate and compare the amount of *FF* recombination losses in both IBC- and best Std-SHJ devices. Resistance values normalized to the designated cell area are indicated with the superscript N.

The normalized series resistance associated with our IBC-SHJ solar cell, extracted from the comparison of 1-sun *I–V* and dark *I–V* curves [32], equals $R_{\mathrm{series}}^{N,\mathrm{IBC}} = 2.1\ \Omega{\cdot}\mathrm{cm}^2$. This value is significantly higher than what we find for our best Std-SHJ solar cell: $R_{\mathrm{series}}^{N,\mathrm{FJ}} = 1.1\ \Omega{\cdot}\mathrm{cm}^2$. The *FF* losses associated with these extracted series-resistance values ($\Delta FF_R_{\mathrm{series}}$) can be calculated from the difference between the ideal *FF* (FF_0) and the series-resistance-affected *FF* (FF_s), using the semiempirical expressions reported by Green (see Fig. 5) [33]: $FF_0 = \frac{v_{\mathrm{oc}} - \ln(v_{\mathrm{oc}}+0.72)}{v_{\mathrm{oc}}+1}$ and $FF_{\mathrm{s}} = FF_0\,(1 - 1.1r_s) + \frac{r_s^2}{5.4}$. In these expressions, v_{OC} and r_s are defined as $v_{\mathrm{oc}} = \frac{V_{\mathrm{oc}}}{nKT/q}$ and $r_s = \frac{R_{\mathrm{series}}}{V_{\mathrm{oc}}/I_{\mathrm{sc}}}$, respectively. FF_0 can be regarded as the *FF* of a diode *I–V* curve, of diode ideality factor n, offset by a value equal to the photogenerated current, and intersecting the abscissa $I = 0$ A at a voltage equal to V_{oc}. This function scales with increasing V_{oc} values, and for given temperature and n values, it depends only on V_{oc}. Practically, for a solar cell with a given V_{oc}, FF_0 represents the highest theoretically possible *FF*, assuming only the presence of recombination mechanisms with an ideality factor n, where R_{series} equals zero and R_{sh} is infinitely large. In Table I, we report the values of $\Delta FF_R_{\mathrm{series}}$, calculated assuming $n = 1$. From this, we conclude that the *FF* of our best IBC-SHJ device suffers from increased series-resistance losses. Indeed, in the case of our IBC-SHJ solar cell, $\Delta FF_R_{\mathrm{series}}$ is twice that of the best Std-SHJ solar cell.

The R_{sh} values were extracted from the slope of a linear fit to the dark *I–V* characteristic in the range (0, −100) mV. For the IBC- and best Std-SHJ solar cells, normalized R_{sh} equals, respectively, $R_{\mathrm{sh}}^{N,\mathrm{IBC}} = 0.5 \times 10^5\ \Omega{\cdot}\mathrm{cm}^2$ and $R_{\mathrm{sh}}^{N,\mathrm{FJ}} = 1.7 \times 10^5\ \Omega{\cdot}\mathrm{cm}^2$. Similar to the case of $\Delta FF_R_{\mathrm{series}}$, we can estimate the magnitude of *FF* losses associated with R_{sh}, by taking the difference between FF_s and series- and shunt-resistance-affected *FF* [33]. We find that shunt-related effects on the overall *FF* are negligible for both of our IBC-SHJ and best Std-SHJ solar cells (in either architecture, <0.1% absolute). This underlines the quality of our patterning methods, resulting in no additional shunting of our IBC-SHJ cells.

Following an approach similar to [34], by considering the difference between FF_s and measured *FF* (from illuminated *I–V* measurements), we can estimate the magnitude of *FF* losses due to recombination currents following ideality factors n different from 1: $\Delta FF_J(n \neq 1) = FF_s - FF$ (see Fig. 5). ΔFF_J $(n \neq 1)$ in the case of our IBC-SHJ device appears to be almost equal to the case of the best Std-SHJ device, demonstrating that *FF* recombination losses in IBC-SHJ cells can be as low as in Std-SHJ devices.

C. Best Interdigitated Back-Contacted Silicon Heterojunction Solar Cell Results and Discussion

The 1-sun *I–V* characteristic of our best 9-cm^2 IBC-SHJ solar cell is given in Fig. 6. This best solar cell belongs to an entire class of devices fabricated with a-Si:H layers, different from the case of the best certified Std-SHJ solar cell, in which the plasma conditions were specifically tuned for improved carrier transport at the two heterocontacts. It shows a conversion efficiency of 21.5%, a V_{oc} of 724 mV, and a J_{sc} of 39.9 mA/cm^2. *FF* reaches a moderate value of 74.5%. Interestingly, the *FF* loss analysis performed in the previous section provides different outcomes in this case. For this device, it results in $R_{\mathrm{series}}^{N,\mathrm{IBC}} = 1.3\ \Omega{\cdot}\mathrm{cm}^2$ and $\Delta FF_R_{\mathrm{series}} = 6.6\%$. Thus, series-resistance losses are only slightly higher than for the best Std-SHJ device. However, $\Delta FF_J(n \neq 1)$ is large in this case, accounting for 3.8% absolute *FF* losses (see Table I). The increased value of $\Delta FF_J(n \neq 1)$ can be clearly linked with a lack of passivation in the carrier carrier-injection range $<3 \times 10^{15}$ cm^{-3}. By calculating the implied *FF* value from the injection-level-dependent lifetime data of the best IBC-SHJ precursor (as described in [29]), after the deposition of all intrinsic and doped a-Si:H layers, we extract a value that is around 2% lower than for typical Std-SHJ precursors. Importantly, this lack of

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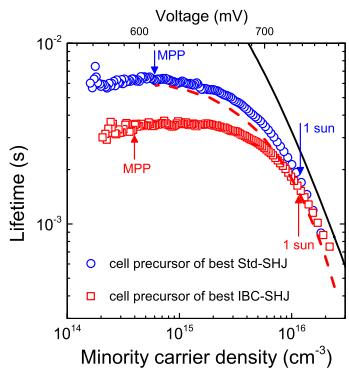

Fig. 7. Minority carrier effective lifetimes of the best IBC- and best Std-SHJ solar cell precursors after deposition of all intrinsic and doped a-Si:H layers (no other contacting layers are present). Implied voltages, calculated according to [36] and assuming a wafer resistivity of 3 Ω·cm ($N_D = 1.4 \times 10^{15}\,\mathrm{cm}^{-3}$), are reported on the top axis. The injection levels corresponding to 1-sun illumination and the MPP of finished devices are marked by solid arrows. The combined Auger and radiative limit is indicated by the solid line [37]. High minority carrier effective lifetime curves were also achieved for IBC-SHJ precursors; the dashed red line shows the lifetime curve associated with the solar cell precursor of the IBC-SHJ device analyzed in Sections III-A and B.

passivation is not intrinsically linked to the IBC-SHJ process flow or device architecture, as we also fabricated IBC-SHJ cell precursors with excellent passivation over the complete injection range (see Fig. 7), yielding implied *FF* values as those of typical Std-SHJ cell precursors. This is the case for the cell precursor of the IBC-SHJ solar cell presented in Sections III-A and B; however, with the type of layers used in this cell, $\Delta FF_R_{\mathrm{series}}$ was larger, compared with that of the class of IBC-SHJ devices presented in this section, and thus, final cell *FF* values over 74.5% have yet to be achieved. These findings suggest that passivation and carrier transport properties of a-Si:H layer contact stacks are entangled, and their independent optimization is not trivial.

Our IBC-SHJ devices reach conversion efficiencies of over 21%, using the described simple processes. This is on par with the best published back-contacted SHJ devices [10], [11], [35], excluding the outstanding results of Panasonic [8] and Sharp [9], of which precise details about the fabrication complexity are undisclosed.

For the sake of completeness, we briefly remark on the care to be taken when performing the proposed *FF* loss analysis. When very high-quality passivation is achieved, recombination during the solar cell operation is driven mainly by radiative and Auger recombination, with the latter dominant. To account for this in the calculation of the ideal FF_0, the ideality factor should be set, in principle, to $n = 2/3$ [38], yielding an increased ideal FF_0 value. This increases the upper limit for the *FF*, but leaves the conclusions about the relative importance of resistance and recombination losses in our IBC-SHJ devices unchanged. Additionally, in back-contacted solar cells, effects linked to the 2-D character of such devices and to locally different carrier injection levels must not be underestimated. At the back side of these devices, indeed, several interfaces are present, with different recombination behavior, and even current crowding effects toward the heterocontacts can be envisaged. Despite this, in the case of our IBC-SHJ devices, we deal with "well-behaved" diodes with dark *I–V* characteristics that can be easily fitted with a classical two-diode model [39] and for which the described analysis is valid (data not shown).

D. Series-Resistance Components in Interdigitated Back-Contacted Silicon Heterojunction Solar Cells

In the previous sections, we concluded that series-resistance losses are an important limiting factor for the *FF* of IBC-SHJ devices. Here, we analyze in detail the main different components contributing to the device total series resistance. In general, these can be divided into three classes:

1) base resistance (R_{base}) of the wafer;
2) finger (R_{finger}) and busbar (R_{bb}) grid resistances;
3) heterocontact resistances (R_{contact}).

R_{base} is linked to charge–carrier lateral transport in the bulk of the wafer between the two comb electrodes. R_{finger} and R_{bb} are associated with electrical conduction into the TCO/metal back contact; $(R_{\mathrm{finger}})_p$ and $(R_{\mathrm{bb}})_p$ refer to the emitter comb; and $(R_{\mathrm{finger}})_n$ and $(R_{\mathrm{bb}})_n$ refer to the base comb. $(R_{\mathrm{contact}})_p$ and $(R_{\mathrm{contact}})_n$ are linked, respectively, to transport through the emitter heterocontact (n-type c-Si/intrinsic a-Si:H/p-type a-Si:H/TCO) and through the base heterocontact (n-type c-Si/intrinsic a-Si:H/n-type a-Si:H/TCO). Note that both stacks feature several interfaces each possibly affecting R_{contact} and, consequently, R_{series}.

The several orders of magnitude difference between metal and TCO layer resistivity cause the latter to act in principle as a buffer layer for *transverse* carrier extraction. However, as a result of typical TCO resistivity (1–2 × 10^{-3} Ω·cm), TCO thickness (≤100 nm), and TCO/metal specific contact resistivity (<1 × 10^{-3} Ω·cm^2), series-resistance contributions linked with transport through the TCO layer to the metal layer, perpendicular to the wafer, are negligible (<1 × 10^{-2} Ω·cm^2). Due to the difference in metal and TCO layer resistivity, the TCO does not contribute to *lateral* carrier conduction into the back contact. The R_{finger} and R_{bb} values can, thus, be considered as merely metal line resistances. The typical values indicated above are those of the layers employed in our IBC-SHJ devices; TCO resistivity was measured by Hall effect measurements, TCO thickness using a stylus profiler, and TCO/metal specific contact resistivity by means of the transfer length method [40].

The precise derivation of the series-resistance components specific to our IBC-SHJ solar cell design is given in the Appendix. The normalized cell series resistance (R^N_{series}) equals

$$R^N_{\mathrm{series}} = R^N_{\mathrm{base}} + \left(R^N_{\mathrm{finger}} + R^N_{\mathrm{bb}} + R^N_{\mathrm{contact}}\right)_n + \left(R^N_{\mathrm{finger}} + R^N_{\mathrm{bb}} + R^N_{\mathrm{contact}}\right)_p. \quad (1)$$

Based on (1), we now evaluate the magnitude of the different series-resistance components and their associated *FF* losses. For this, we take experimental values from our IBC-SHJ solar cells for the wafer and TCO/metal stack properties, back-contact geometry, and minority carrier injection level at the maximum power point (MPP).

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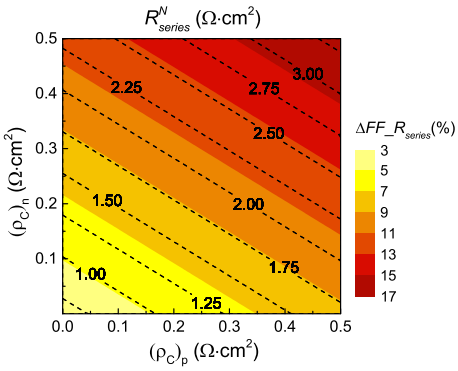

Fig. 8. Normalized series resistance $(R^N_{\rm series}\ (\Omega\cdot{\rm cm}^2))$ of IBC-SHJ devices and associated absolute *FF* loss [$\Delta FF_R_{\rm series}$ (%)] as a function of heterocontact specific contact resistivity. Dashed contour lines delimitate regions of $R^N_{\rm series}$ values, whereas the color map is used to represent $\Delta FF_R_{\rm series}$ values.

We find that transport losses at the heterocontacts have a preponderant role in the determination of the total device $R^N_{\rm series}$ and the associated $\Delta FF_R_{\rm series}$ In a range of specific contact resistivity values 0.1–0.5 $\Omega\cdot{\rm cm}^2$, for both emitter $((\rho_{\rm c})_{\rm p})$ and base $((\rho_{\rm c})_{\rm n})$ heterocontacts, the *FF* loss associated with only the contact resistance component goes from a minimum of 2.7% absolute to a value of 13.8% absolute, which are indeed significant losses. The range 0.1–0.5 $\Omega\cdot{\rm cm}^2$ covers most of the values reported in the literature for the specific contact resistivity of the heterocontacts [10], [41], [42]. On the other hand, the *FF* loss associated with lateral conduction in the base accounts for 1.6% absolute, and the overall *FF* loss associated with the different grid resistance components is 1.7% absolute. In Fig. 8, we give calculated values of $R^N_{\rm series}$, and of the associated total $\Delta FF_R_{\rm series}$, as a function of the specific contact resistivity values of both stacks. Fig. 8 shows how contact resistance can have an important detrimental influence on the final device *FF* value.

FF losses associated with heterocontact transport properties can be at least partially ascribed to the TCO/a-Si:H interface [10], [43]–[46]. Our experimental work with IBC-SHJ confirms the importance of this interface with respect to series-resistance losses; changes in the TCO layer composition have shown a relevant impact on total series resistance and *FF* of final devices (data not shown), as have changes in the deposition conditions of the doped a-Si:H layers. However, characterization of the detailed heterocontact transport properties is complex, and we believe that additional efforts in this regard are needed. Increased insights into the transport mechanisms at the heterocontacts would help further optimization.

E. Interdigitated Back-Contacted Silicon Heterojunction Fill Factor Limiting Factors

Basic modeling of the different series-resistance components in IBC-SHJ devices and analysis of *FF* losses in IBC-SHJ devices demonstrate that series resistance can limit final cell *FF* values.

For IBC devices, a front-diffused layer may help to achieve high *FF* either by improving front-surface recombination behavior [47] or enhancing lateral transport and reducing $R_{\rm base}$ component [48]. However, the latter depends on the wafer injection level under solar cell working conditions. Assuming typical passivation quality of a-Si:H films (high injection level under solar cell working conditions, i.e., MPP) and a suitable pitch for the back-contact geometry, we think that such front-diffused layers can be avoided in IBC-SHJ devices without incurring large lateral transport losses.

The level of transport optimization at the two heterocontacts in IBC-SHJ devices assumes an increased relevance compared with typical Std-SHJ devices. This augmented relevance comes from a minor degree of freedom in the optimization of the two contact stacks and an overall reduced contact area. In the proposed processing sequence, TCO is deposited by a unique deposition process, and thus, it cannot be optimized independently for each single heterocontact, unless an increased amount of processing steps can be accepted. The same occurs for the back intrinsic a-Si:H layer. Next, the overall area occupied by the heterocontacts is reduced to less than half with respect to any typical two-side-contacted SHJ solar cell. This significantly increases the current densities through the heterocontacts; for our back-contact geometry, current densities of 80 mA/cm^2 and of 130 mA/cm^2, for the emitter and base heterocontacts, respectively, must be collected, compared with about 40 mA/cm^2 for typical Std-SHJ cells. The type of a-Si:H layers that led to our best IBC-SHJ device demonstrates that these *FF* transport losses can be minimized. However, this was achieved at the expense of increased *FF* recombination losses. Efforts to resolve these problems will also benefit Std-SHJ devices.

These conclusions on the importance of electrical contact optimization are limited to back-contacted SHJ devices; in the case of typical back-contacted homojunction devices, specific contact resistivity values are significantly lower and the contact area must be limited to openings through dielectric passivation layers [49]–[54] to allow for high-$V_{\rm oc}$ devices. Interestingly, in both cases, we eventually face a tradeoff between recombination and transport losses.

IV. Conclusion

Back-contacted SHJ devices, using interdigitated back contacts, with conversion efficiencies of up to 21.5% have been fabricated by a simple processing sequence and size-scalable techniques. The added complexity typically associated with IBC process flows has been minimized. *In situ* masking of a-Si:H layers has been demonstrated to be a viable patterning method for high-efficiency devices. $J_{\rm sc}$ values have been shown to benefit from the back-contacted architecture, and $V_{\rm oc}$ values have been shown not to suffer from the additional processing required by the proposed fabrication methodology. Moderate *FF* values remain the main limiting factor for higher device efficiencies. *FF* losses related to transport and recombination currents have been studied in our IBC-SHJ devices and compared with our best Std-SHJ device. Based on this analysis, higher device *FF* and efficiencies are possible, using the proposed processing solution,

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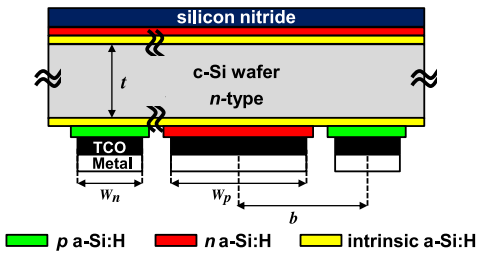

Fig. 9. Geometry of the back contact. Side view.

via further optimization of transport at the two heterocontacts and high-quality a-Si:H passivation layers.

APPENDIX

The interdigitated back contact consists of two combs, each with n fingers of length a and width w, which half-pitch is indicated with the parameter b. In the following text, when present, subscripts n and p specify, respectively, the n-type and the p-type comb (see Fig. 9). The designated cell area [see (3)–(5)] is indicated with the parameter A_d.

Equation (2) for the normalized series-resistance base component is taken from [55] and reformulated according to our specific device architecture. For substrate, we assume an n-type wafer of thickness t, resistivity ρ_w, and with a donor-dopant density equal to N_D. The solar cell injection level at MPP (Δp) is calculated from V_{mpp} of the resistance-free *I–V* curve, measured by suns-V_{oc}, according to [36]

$$R^N_{\mathrm{base}} \cong \frac{\rho_w N_D}{(N_D + \Delta p)} \left(\frac{b \cdot (b - w_n/2 - w_p/2)}{t} + \frac{b \cdot w_p/2}{3t} \right). \tag{2}$$

The expressions for the normalized metal grid series-resistance component [see (3) and (4)] of each comb are derived, as reported in [56]. The TCO/metal stack is a unique conduction medium, whose sheet resistance equals the measured value $R^{\mathrm{metal/TCO}}_{\mathrm{sheet}} = 0.02\Omega/\square$. The prefactor in (4) accounts for three current-extraction points along each busbar (of width $w\prime$), as in our measurement setup

$$R^N_{\mathrm{finger}} = \frac{4}{3} a^3 b^2 n \left(\frac{R^{\mathrm{metal/TCO}}_{\mathrm{sheet}}}{w} \right) \cdot \frac{1}{A_d} \tag{3}$$

$$R^N_{\mathrm{bb}} = \frac{2}{27} a^2 n^3 b^3 \left(\frac{R^{\mathrm{metal/TCO}}_{\mathrm{sheet}}}{w'} \right) \cdot \frac{1}{A_d}. \tag{4}$$

The normalized resistance components associated with the heterocontacts are calculated according to (5). Modifying (5) to account for carrier collection below the contacts over a region wide as the transfer length $L_{t(c)}$, the conclusions from Section III-D remain unchanged

$$\left(R^N_{\mathrm{contact}}\right)_p = \frac{(\rho_C)_p}{w_p n a} \cdot A_d \quad \left(R^N_{\mathrm{contact}}\right)_n = \frac{(\rho_C)_n}{w_n n a} \cdot A_d. \tag{5}$$

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Tri-layer antireflection coatings ($SiO_2/SiO_2–TiO_2/TiO_2$) for silicon solar cells using a sol–gel technique

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Abstract

Antireflection coatings (ARCs) have become one of the key issues for mass production of Si solar cells. They are generally performed by vacuum processes such as thermal evaporation, reactive sputtering, and plasma-enhanced chemical vapor deposition. In this work, a sol–gel method has been demonstrated to prepare the ARCs for the non-textured monocrystalline Si solar cells. The spin-coated TiO_2 single-layer, SiO_2/TiO_2 double-layer and $SiO_2/SiO_2–TiO_2/TiO_2$ triple-layer ARCs were deposited on the Si solar cells and they showed good uniformity in thickness. The measured average optical reflectance (400–1000 nm) was about 9.3, 6.2 and 3.2% for the single-layer, double-layer and triple-layer ARCs, respectively. Good correlation between theoretical and experimental data was obtained. Under a triple-layer ARC condition, a 39% improvement in the efficiency of the monocrystalline Si solar cell was achieved. These indicate that the sol–gel ARC process has high potential for low-cost solar cell fabrication.
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Keywords: silicon; antireflection coating; sol–gel; TiO_2; SiO_2; solar cell

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1. Introduction

Antireflection coatings (ARCs) are widely used in various applications such as display panels, solar cells and optical lenses [1–3]. Thin-film ARCs can greatly reduce the optical loss in multi-element lenses by making use of phase changes and the dependence of the reflectivity on refraction index. A thin, dielectric film or several such films were applied to an optical surface to reduce its reflectance and thereby increase its transmittance. A single-layer ARC can be non-reflective only at one wavelength, usually at the middle of the visible region. Multiple layers are more effective over the entire visible spectrum. Several transparent and high refractive-index material films have already been applied to ARC techniques, e.g. SiO ($n = 1.8$–1.9), SiO_2 ($n = 1.44$), Si_3N_4 ($n = 1.9$), TiO_2 ($n = 2.3$), Al_2O_3 ($n = 1.86$), Ta_2O_5 ($n = 2.26$), SiO_2–TiO_2 ($n = 1.8$–1.96) and ZnS [4–9]. Optical coatings are generally performed by vacuum processes such as thermal evaporation, reactive sputtering, and plasma-enhanced chemical vapor deposition (PECVD). All these methods are capable of producing films with uniform thickness and good optical properties. However, the conventional vacuum deposition processes are expensive and unsuitable for continuous mass production techniques in low-cost solar cells. Recently, high refractive-index and high-transparency Si_3N_4 or TiO_2 single layer and SiO_2/TiO_2 double-layer have been developed and applied in solar cell ARCs process. These favorite films are prepared by PECVD and this results in reflectance below 10% [10–12].

Recently, ARCs have become one of the key issues for mass production of mono- and multi-crystalline Si solar cells. The sol–gel technique offers a simple and low-cost process to prepare the high-quality thin films [13,14]. In this work, the TiO_2 single-layer, SiO_2/TiO_2 double-layer and SiO_2/SiO_2–TiO_2/TiO_2 triple-layer ARCs on monocrystalline Si solar cells were prepared by a sol–gel spin-coating technique. To achieve minimum reflection of a normal incident wave of a single wavelength, the antireflection coating may consist of a single layer, which must possess (a) a refractive index equal to the square root of the refractive indices of the materials bounding the coating, and (b) a thickness equal to one-quarter of the wavelength (i.e., the wavelength within the material of which the coating consists). However, if one wants to achieve minimum reflection of multiple wavelengths, additional layers must be added. Kern and Tracy have observed an increase of 44% in the cell efficiency after spraying TiO_2 single-layer ARC [15]. Green et al. have used MgF_2/ZnS double-layer ARCs on Si cells with 19.1% efficiency [16]. In this paper, we present the results of calculations and experiments obtained by sol–gel method of single-layer, double-layer and triple-layer ARCs on polished silicon substrates. For an optimum ARCs design, the refractive index and thickness of each layer must be controllable to achieve the best performance along the desired spectrum. Details of the fabrication process and efficiency improvement will be described.

2. Experimental details

2.1. Sol–gel and spin coating process

The flow chart of the ARC synthesis process was performed using a sol–gel process as shown in Fig. 1. A clear solution is prepared by reacting metal alkoxide with a mixture of critical amount of water and/or acid in an alcohol diluted medium, and the SiO_2, SiO_2–TiO_2 and TiO_2 coatings were spin coated on the Si substrate from the above-said

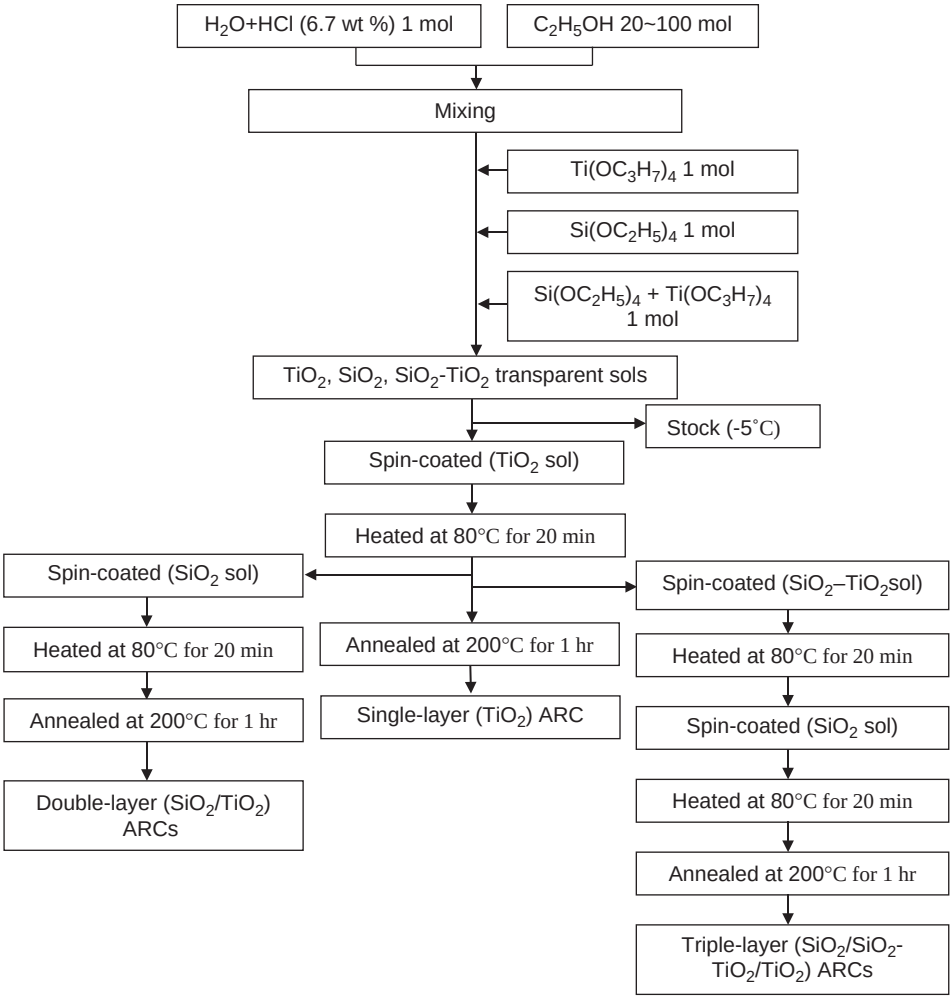

Fig. 1. Flow chart of sol–gel process for TiO_2 single-layer, SiO_2/TiO_2 double-layer and SiO_2/SiO_2–TiO_2/TiO_2 triple-layer antireflection coatings.

solution at 2000–6000 r.p.m for 30 s. The desired film thickness can be adjusted by the spin speed. Each film was pre-baked at 80°C for 20 min and then post baked at 200°C for 1 h in atmosphere. Table 1 tabulated the sol–gel parameters and deposition results of the SiO_2, SiO_2–TiO_2 and TiO_2 films. After spin coating and post-baking processes, the refractive index, thickness and reflectance of the film were measured using an n&k analyzer (model: 1280, N&K Tech. Inc.).

2.2. Design of single-layer, double-layer and triple-layer ARCs

In some applications, zero reflectance is needed at a single wavelength or throughout a narrow spectrum band. The optimum thickness and refractive index with a minimum

Table 1
Sol–gel parameters and deposition results of the SiO_2, SiO_2-TiO_2 and TiO_2 films

	$Ti(OC_3H_9)_4$:$Si(OC_2H_5)_4$:C_2H_5OH (mol)	Spin rate (r.p.m)	Thickness (nm)	Refractive index ($\lambda = 500$ nm)
TiO_2	1:0:60	2000–6000	64–33	2.26
SiO_2	0:1:80		93–54	1.45
SiO_2–TiO_2	1:1:80		76–42	1.78

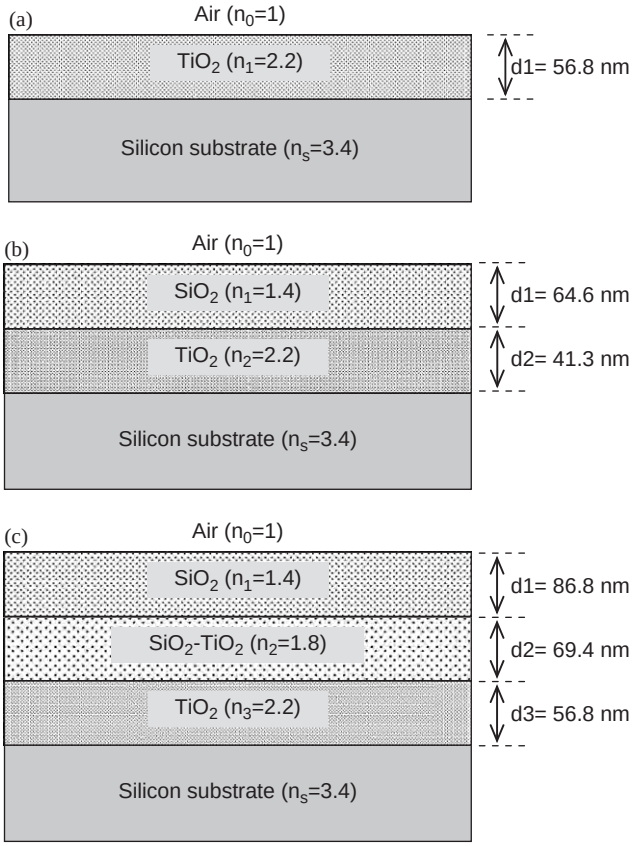

Fig. 2. Design diagram of antireflection coatings with (a) TiO_2 single layer, (b) SiO_2/TiO_2 double layers and (c) SiO_2/SiO_2–TiO_2/TiO_2 triple layers.

reflectance for a single-layer ARC can be deduced from

$$\lambda_0 = 4n_1 \times d_1, \tag{1}$$

where λ_0 is the midrange wavelength of 550 nm, n_1 and d_1 are the refractive index and layer thickness, respectively. A schematic diagram of this case is shown in Fig. 2(a).

For the double-layer ARC design, the low–high index on the Si substrate (i.e., the outer layer has the low refractive index and inner layer has high refractive index) is used.

Fig. 2(b) shows a typical double-layer ARC structure, where n_0, n_s, n_1 and n_2 correspond to the refractive index of air, substrate, outer and inner layers, respectively. Moreover, d_1 and d_2 represent the thickness of the outer and inner layers, respectively. Each layer must meet Eqs. (2) and (3) in order to achieve a zero reflectance [17],

$$\frac{n_2 d_2}{\lambda_0} = \frac{1}{2\pi}\tan^{-1}\left\{\pm\left[\frac{(n_s - n_0)(n_0 n_s - n_1^2)n_2^2}{(n_1^2 n_s - n_0 n_2^2)(n_2^2 - n_0 n_s)}\right]^{1/2}\right\}, \tag{2}$$

$$\frac{n_1 d_1}{\lambda_0} = \frac{1}{2\pi}\tan^{-1}\left\{\pm\left[\frac{(n_s - n_0)(n_0 n_s - n_2^2)n_1^2}{(n_1^2 n_s - n_0 n_2^2)(n_1^2 - n_0 n_s)}\right]^{1/2}\right\}. \tag{3}$$

The design of triple-layer ARC on Si can be optimized using Eqs. (4–6) when the optimum refractive index and thickness of each layer in the stack is calculated,

$$\lambda_0 = 4n_1 \times d_1, \tag{4}$$

$$\lambda_0 = 4n_2 \times d_2, \tag{5}$$

$$\lambda_0 = 4n_3 \times d_3, \tag{6}$$

where n_2 is the refractive index of the medium layer. The refractive index decreases from the high value (n_s) to the low value ($n_0 = 1$) in the order: $n_0 < n_1 < n_2 < n_3 < n_s$. Here each layer thickness is equal to one-quarter the wavelength in question and the multiple internal reflection of light is not been considered in these calculations. The principle of this type of ARC has been illustrated using the vector methods previously [18–20]. For a triple-layer AR stack, Fig. 2(c), shows the optimum refractive index and the thickness of each layer. A film with any medium refractive index between 1.4 and 2.4 (for 500 nm) can be obtained by mixing the starting SiO_2 and TiO_2 sol in different proportions. Using materials deposited by the sol–gel process [SiO_2 ($n = 1.4$), SiO_2–TiO_2 ($n = 1.8$) and TiO_2 ($n = 2.3$)], a triple-layer ARC on Si can be formed with minimum optical reflection.

2.3. Solar cell performance

Solar cells were fabricated using a 1–10 Ω cm boron-doped monocrystalline Si wafer ($2 \times 2\,cm^2$ area, 300 μm thick and one side polished). The emitter region was realized by thermal diffusion of phosphorous atoms in a quartz tube furnace at 850°C. The Al back contact was deposited by evaporation and then annealed at 800°C in order to form both effective back surface field and back contact. The TiO_2 single-layer, SiO_2/TiO_2 double-layer and SiO_2/SiO_2–TiO_2/TiO_2 triple-layer ARCs were deposited on the front of solar cells using a spin-coating technique. A front Al contact was deposited through a metallic mask (grid-type collecting electrode) and then thermal annealed at 700°C for 30 min.This grid-type correcting electrode reduces about 15% the effective illuminated area of the cell. Current density versus voltage measurements were taken under AM1.5 ($80\,mW/cm^2$) white light from a dual beam solar simulator.

3. Results and discussion

The thicknesses of the TiO_2, SiO_2–TiO_2 and SiO_2 films as functions of the spin rate are shown in Fig. 3. It was found that the film thickness decreased when the spin rate increased. Each TiO_2, SiO_2–TiO_2 or SiO_2 film thickness can be controlled by changing the spin rate or the alcohol concentration in the sol–gel solution. Fig. 4 shows the absorbance spectra and refractive indices of the deposited films as a function of wavelength. The refractive index of the SiO_2, SiO_2–TiO_2 and TiO_2 film was determined to be 1.45, 1.78 and

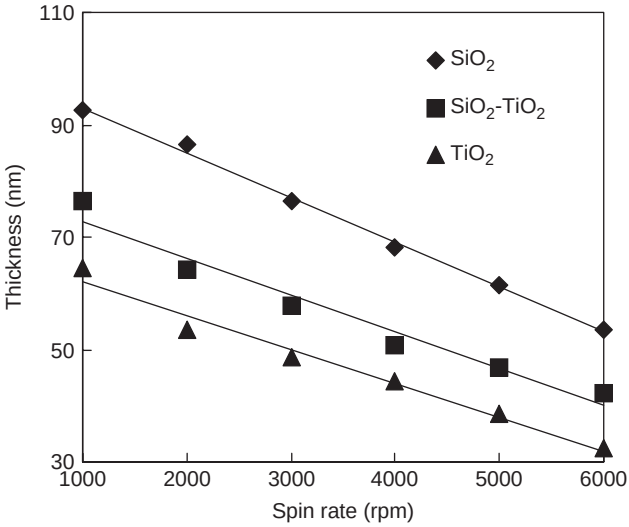

Fig. 3. Variations of SiO_2, SiO_2–TiO_2 and TiO_2 film thickness as a function ofspin rate.

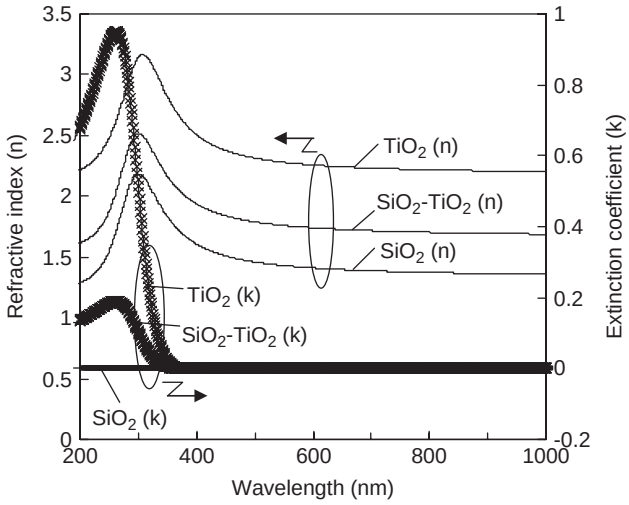

Fig. 4. Variations of extinction coefficients (k) and refractive index (n) of SiO_2, SiO_2–TiO_2 and TiO_2 films.

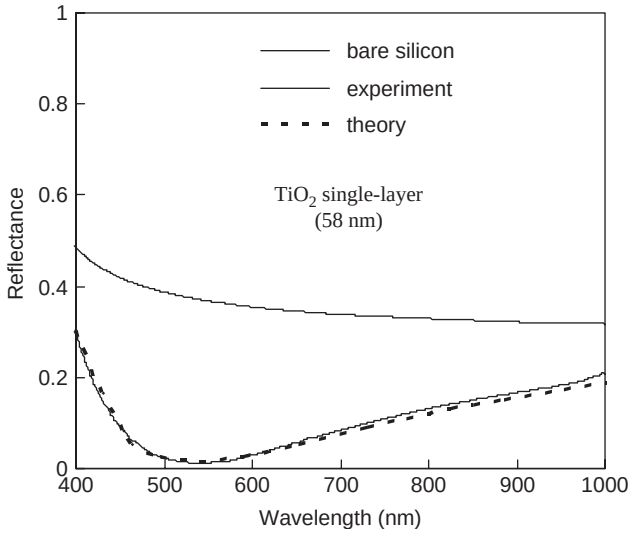

Fig. 5. Experimental and calculated reflectance data as a function of wavelength for TiO_2 single-layer ARC on Si substrate.

2.26 (for wavelength at 500 nm), respectively. It was found that the extinction coefficients (k) of each film after the annealing process almost approached to zero between 400 and 1000 nm.Furthermore, the absorbance point of the SiO_2–TiO_2 and TiO_2 films is located at a wavelength of 340 nm.These indicate that the sol–gel deposited SiO_2 and TiO_2 films can be used as ARCs for Si solar cells [21,22].

Fig. 5 shows the measured and calculated reflectance spectra of the TiO_2 single-layer ARC on non-textured Si substrates. It is well known that bare silicon has a high-refractive index, which leads to a solar-averaged reflectance of about 37%. The large reflection loss can be reduced significantly via a suitable ARC. A minimum value of reflectance $R(\lambda) = 0.5\%$ can be obtained at 536 nm.The average reflectance of approximately 9.3% between 400 and 1000 nm was obtained by the TiO_2 single-layer ARC on the non-textured Si substrate. The curves in Fig. 5 showed good agreement between the theoretical and experimental results for the reflectance data. The measured and calculated reflectance spectra of the optimized double-layer ARC are shown in Fig. 6. The reflectance $R(\lambda)$ is lower than 5% in the wavelength between 550 and 900 nm, which maximizes the absorption of the incident photons and increases the photo-generated current. The SiO_2/TiO_2 double-layer ARC results in a minimum reflectance of 1% at 690 nm with an average reflectance of approximately 6.2% between 400 and 1000 nm.That is, the Si absorbance increases by approximately 49.8%. Good correlation is also obtained between the theoretical and experimental results.

The experimental and theoretical reflectance data versus wavelength of the optimum triple-layer ARC structure are presented in Fig. 7. Here the theoretical SiO_2/SiO_2–TiO_2/TiO_2 triple-layer ARC on Si was calculated under normal optical incidence. The effective reflectance can reach 3.2% over 400–1000 nm range, indicating an increase in the absorption of the bare Si by approximately 54.6%. The difference in the short wavelength region is probably due to the dispersion of the refractive index in the wavelength region.

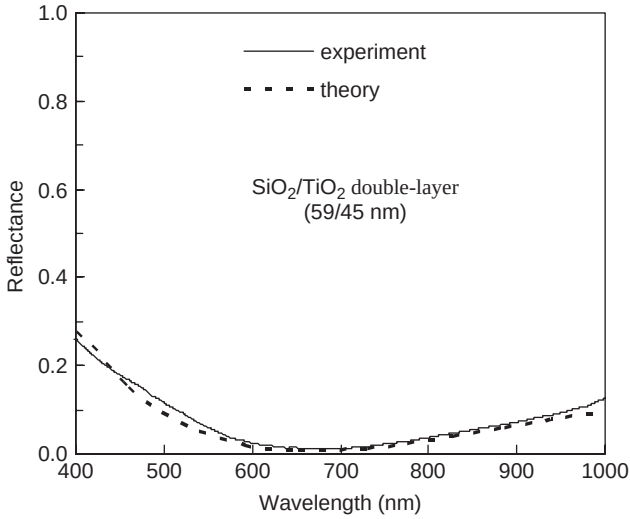

Fig. 6. Experimental and calculated reflectance data as a function of wavelength for SiO_2/TiO_2 double-layer ARCs on Si substrate.

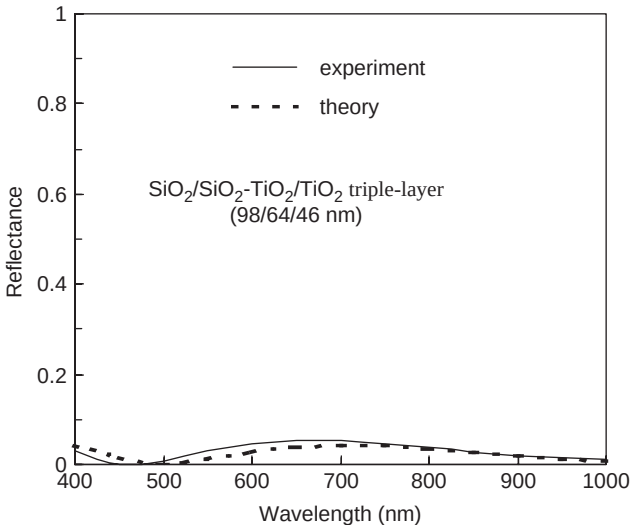

Fig. 7. Experimental and calculated reflectance data as a function of wavelength for SiO_2/SiO_2–TiO_2/TiO_2 triple-layer ARCs on Si substrate.

Finally, the current–voltage characteristics of the solar cell devices with sol–gel ARCs are shown in Fig. 8. Significant improvement of the short circuit current after ARCs was observed. However, the open-circuit voltage and the fill factor were not affected by the ARCs in these measurements. It is found that the current–voltage characteristic with a triple-layer ARC is better than that with double- or single-layer ARCs. Table 2 shows the device performance of the Si solar cells with various ARC structures. The performance of

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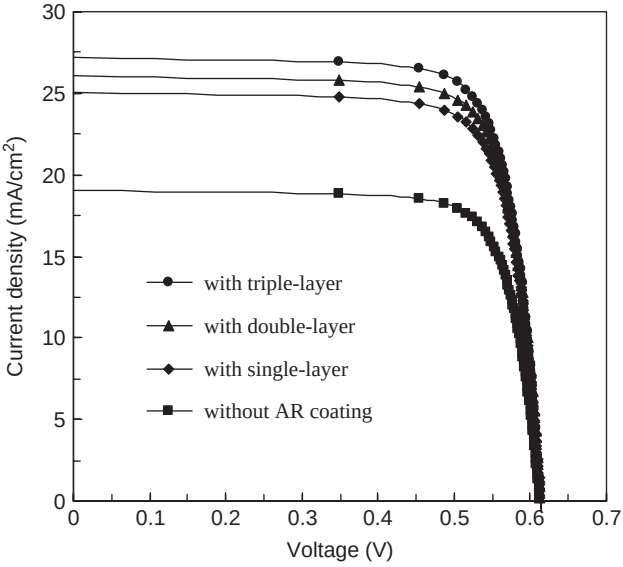

Fig. 8. Current density versus voltage characteristics of Si solar cells with triple-layer (●), double-layer (▲), single-layer (◆) and without ARCs (■).

Table 2
Characterization of Si solar cells with various antireflection coatings

Solar cell	Jsc (mA/cm^2)	Voc (V)	Fill factor (%)	Efficiency (%)
Bare silicon	16.2	0.61	76.4	11.36
Single-layer TiO_2	24.8	0.61	76.6	14.49
Double-layer SiO_2/TiO_2	25.8	0.61	76.2	14.99
Triple-layer SiO_2/SiO_2–TiO_2/TiO_2	27.1	0.61	76.7	15.85

bare Si solar cell without any ARC has an efficiency of 11.36%. The Si solar cells with triple-, double- and single-layer ARC show an increase of efficiency of about 39, 32 and 27%, respectively. That is, the efficiency of the Si solar cell with a triple-layer ARC can increase to 15.85% in the present work by utilizing a sol–gel technique.

4. Conclusions

This work presents a comprehensive experimental study with the aim to prepare high-quality single-, double- and triple-layer ARCs on Si solar cells using a sol–gel process. The effective refractive index and thickness of the films can be easily adjusted via the concentration of the sols, spin rate and annealed temperature. The reflectance of TiO_2 single-layer, SiO_2/TiO_2 double-layer and SiO_2/SiO_2–TiO_2/TiO_2 triple-layer ARCs was determined to be 9.3, 6.2 and 3.2%, respectively. The optical performance of the sol–gel-deposited ARC can be compared with that of the conventional ARC using more expensive vacuum processes such as PECVD or sputtering. A 39% enhancement in conversion

efficiency was obtained in the monocrystalline Si solar cell with a triple-layer ARC. In the future, using a combination of spin coating and rapid thermal annealing processes, the sol–gel ARCs could have high potential for continuous mass production of Si solar cells at a fraction of the cost.

Acknowledgments

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Tri-layer antireflection coatings (SiO_2/SiO_2–TiO_2/TiO_2) for silicon solar cells using a sol–gel technique

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Abstract

Antireflection coatings (ARCs) have become one of the key issues for mass production of Si solar cells. They are generally performed by vacuum processes such as thermal evaporation, reactive sputtering, and plasma-enhanced chemical vapor deposition. In this work, a sol–gel method has been demonstrated to prepare the ARCs for the non-textured monocrystalline Si solar cells. The spin-coated TiO_2 single-layer, SiO_2/TiO_2 double-layer and SiO_2/SiO_2–TiO_2/TiO_2 triple-layer ARCs were deposited on the Si solar cells and they showed good uniformity in thickness. The measured average optical reflectance (400–1000 nm) was about 9.3, 6.2 and 3.2% for the single-layer, double-layer and triple-layer ARCs, respectively. Good correlation between theoretical and experimental data was obtained. Under a triple-layer ARC condition, a 39% improvement in the efficiency of the monocrystalline Si solar cell was achieved. These indicate that the sol–gel ARC process has high potential for low-cost solar cell fabrication.
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Keywords: silicon; antireflection coating; sol–gel; TiO_2; SiO_2; solar cell

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1. Introduction

Antireflection coatings (ARCs) are widely used in various applications such as display panels, solar cells and optical lenses [1–3]. Thin-film ARCs can greatly reduce the optical loss in multi-element lenses by making use of phase changes and the dependence of the reflectivity on refraction index. A thin, dielectric film or several such films were applied to an optical surface to reduce its reflectance and thereby increase its transmittance. A single-layer ARC can be non-reflective only at one wavelength, usually at the middle of the visible region. Multiple layers are more effective over the entire visible spectrum. Several transparent and high refractive-index material films have already been applied to ARC techniques, e.g. SiO ($n = 1.8$–1.9), SiO_2 ($n = 1.44$), Si_3N_4 ($n = 1.9$), TiO_2 ($n = 2.3$), Al_2O_3 ($n = 1.86$), Ta_2O_5 ($n = 2.26$), SiO_2–TiO_2 ($n = 1.8$–1.96) and ZnS [4–9]. Optical coatings are generally performed by vacuum processes such as thermal evaporation, reactive sputtering, and plasma-enhanced chemical vapor deposition (PECVD). All these methods are capable of producing films with uniform thickness and good optical properties. However, the conventional vacuum deposition processes are expensive and unsuitable for continuous mass production techniques in low-cost solar cells. Recently, high refractive-index and high-transparency Si_3N_4 or TiO_2 single layer and SiO_2/TiO_2 double-layer have been developed and applied in solar cell ARCs process. These favorite films are prepared by PECVD and this results in reflectance below 10% [10–12].

Recently, ARCs have become one of the key issues for mass production of mono- and multi-crystalline Si solar cells. The sol–gel technique offers a simple and low-cost process to prepare the high-quality thin films [13,14]. In this work, the TiO_2 single-layer, SiO_2/TiO_2 double-layer and SiO_2/SiO_2–TiO_2/TiO_2 triple-layer ARCs on monocrystalline Si solar cells were prepared by a sol–gel spin-coating technique. To achieve minimum reflection of a normal incident wave of a single wavelength, the antireflection coating may consist of a single layer, which must possess (a) a refractive index equal to the square root of the refractive indices of the materials bounding the coating, and (b) a thickness equal to one-quarter of the wavelength (i.e., the wavelength within the material of which the coating consists). However, if one wants to achieve minimum reflection of multiple wavelengths, additional layers must be added. Kern and Tracy have observed an increase of 44% in the cell efficiency after spraying TiO_2 single-layer ARC [15]. Green et al. have used MgF_2/ZnS double-layer ARCs on Si cells with 19.1% efficiency [16]. In this paper, we present the results of calculations and experiments obtained by sol–gel method of single-layer, double-layer and triple-layer ARCs on polished silicon substrates. For an optimum ARCs design, the refractive index and thickness of each layer must be controllable to achieve the best performance along the desired spectrum. Details of the fabrication process and efficiency improvement will be described.

2. Experimental details

2.1. Sol–gel and spin coating process

The flow chart of the ARC synthesis process was performed using a sol–gel process as shown in Fig. 1. A clear solution is prepared by reacting metal alkoxide with a mixture of critical amount of water and/or acid in an alcohol diluted medium, and the SiO_2, SiO_2–TiO_2 and TiO_2 coatings were spin coated on the Si substrate from the above-said

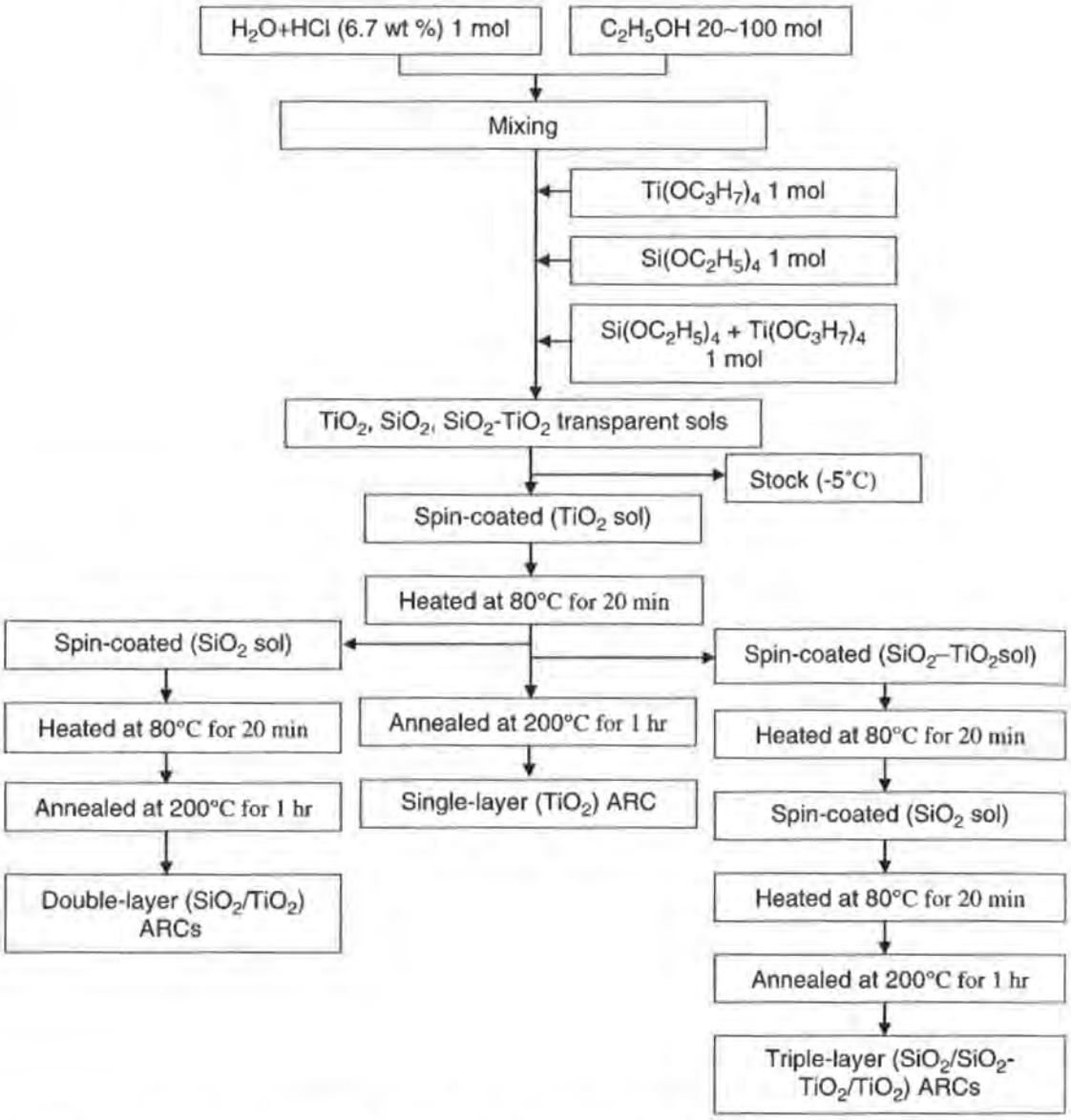

Fig. 1. Flow chart of sol–gel process for TiO_2 single-layer, SiO_2/TiO_2 double-layer and SiO_2/SiO_2–TiO_2/TiO_2 triple-layer antireflection coatings.

solution at 2000–6000 r.p.m for 30 s. The desired film thickness can be adjusted by the spin speed. Each film was pre-baked at 80°C for 20 min and then post baked at 200°C for 1 h in atmosphere. Table 1 tabulated the sol–gel parameters and deposition results of the SiO_2, SiO_2–TiO_2 and TiO_2 films. After spin coating and post-baking processes, the refractive index, thickness and reflectance of the film were measured using an n&k analyzer (model: 1280, N&K Tech. Inc.).

2.2. Design of single-layer, double-layer and triple-layer ARCs

In some applications, zero reflectance is needed at a single wavelength or throughout a narrow spectrum band. The optimum thickness and refractive index with a minimum

Table 1
Sol–gel parameters and deposition results of the SiO_2, SiO_2-TiO_2 and TiO_2 films

	$Ti(OC_3H_9)_4$:$Si(OC_2H_5)_4$:C_2H_5OH (mol)	Spin rate (r.p.m)	Thickness (nm)	Refractive index ($\lambda = 500$ nm)
TiO_2	1:0:60	2000–6000	64–33	2.26
SiO_2	0:1:80		93–54	1.45
SiO_2–TiO_2	1:1:80		76–42	1.78

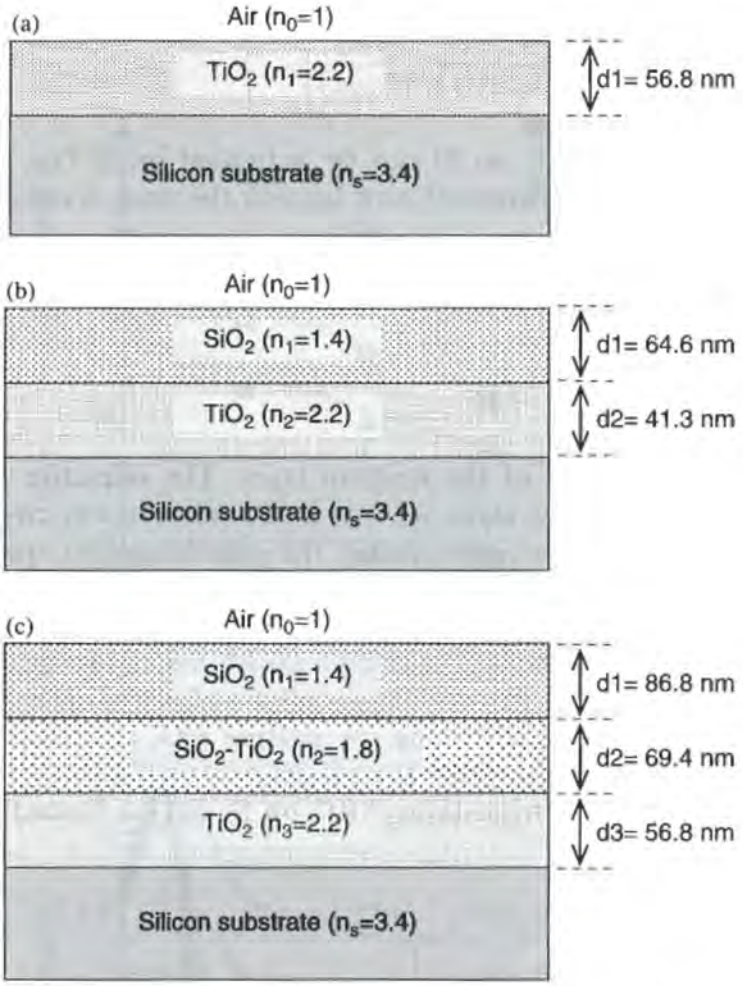

Fig. 2. Design diagram of antireflection coatings with (a) TiO_2 single layer, (b) SiO_2/TiO_2 double layers and (c) SiO_2/SiO_2–TiO_2/TiO_2 triple layers.

reflectance for a single-layer ARC can be deduced from

$$\lambda_0 = 4n_1 \times d_1, \tag{1}$$

where λ_0 is the midrange wavelength of 550 nm, n_1 and d_1 are the refractive index and layer thickness, respectively. A schematic diagram of this case is shown in Fig. 2(a).

For the double-layer ARC design, the low–high index on the Si substrate (i.e., the outer layer has the low refractive index and inner layer has high refractive index) is used.

Fig. 2(b) shows a typical double-layer ARC structure, where n_0, n_s, n_1 and n_2 correspond to the refractive index of air, substrate, outer and inner layers, respectively. Moreover, d_1 and d_2 represent the thickness of the outer and inner layers, respectively. Each layer must meet Eqs. (2) and (3) in order to achieve a zero reflectance [17],

$$\frac{n_2 d_2}{\lambda_0} = \frac{1}{2\pi}\tan^{-1}\left\{\pm\left[\frac{(n_s - n_0)(n_0 n_s - n_1^2)n_2^2}{(n_1^2 n_s - n_0 n_2^2)(n_2^2 - n_0 n_s)}\right]^{1/2}\right\}. \tag{2}$$

$$\frac{n_1 d_1}{\lambda_0} = \frac{1}{2\pi}\tan^{-1}\left\{\pm\left[\frac{(n_s - n_0)(n_0 n_s - n_2^2)n_1^2}{(n_1^2 n_s - n_0 n_2^2)(n_1^2 - n_0 n_s)}\right]^{1/2}\right\}. \tag{3}$$

The design of triple-layer ARC on Si can be optimized using Eqs. (4–6) when the optimum refractive index and thickness of each layer in the stack is calculated,

$$\lambda_0 = 4n_1 \times d_1, \tag{4}$$

$$\lambda_0 = 4n_2 \times d_2, \tag{5}$$

$$\lambda_0 = 4n_3 \times d_3, \tag{6}$$

where n_2 is the refractive index of the medium layer. The refractive index decreases from the high value (n_s) to the low value ($n_0 = 1$) in the order: $n_0 < n_1 < n_2 < n_3 < n_s$. Here each layer thickness is equal to one-quarter the wavelength in question and the multiple internal reflection of light is not been considered in these calculations. The principle of this type of ARC has been illustrated using the vector methods previously [18–20]. For a triple-layer AR stack, Fig. 2(c), shows the optimum refractive index and the thickness of each layer. A film with any medium refractive index between 1.4 and 2.4 (for 500 nm) can be obtained by mixing the starting SiO_2 and TiO_2 sol in different proportions. Using materials deposited by the sol–gel process [SiO_2 ($n = 1.4$), SiO_2–TiO_2 ($n = 1.8$) and TiO_2 ($n = 2.3$)], a triple-layer ARC on Si can be formed with minimum optical reflection.

2.3. Solar cell performance

Solar cells were fabricated using a 1–10 Ω cm boron-doped monocrystalline Si wafer ($2 \times 2\,cm^2$ area, 300 μm thick and one side polished). The emitter region was realized by thermal diffusion of phosphorous atoms in a quartz tube furnace at 850°C. The Al back contact was deposited by evaporation and then annealed at 800°C in order to form both effective back surface field and back contact. The TiO_2 single-layer, SiO_2/TiO_2 double-layer and SiO_2/SiO_2–TiO_2/TiO_2 triple-layer ARCs were deposited on the front of solar cells using a spin-coating technique. A front Al contact was deposited through a metallic mask (grid-type collecting electrode) and then thermal annealed at 700°C for 30 min.This grid-type correcting electrode reduces about 15% the effective illuminated area of the cell. Current density versus voltage measurements were taken under AM1.5 ($80\,mW/cm^2$) white light from a dual beam solar simulator.

3. Results and discussion

The thicknesses of the TiO_2, SiO_2–TiO_2 and SiO_2 films as functions of the spin rate are shown in Fig. 3. It was found that the film thickness decreased when the spin rate increased. Each TiO_2, SiO_2–TiO_2 or SiO_2 film thickness can be controlled by changing the spin rate or the alcohol concentration in the sol–gel solution. Fig. 4 shows the absorbance spectra and refractive indices of the deposited films as a function of wavelength. The refractive index of the SiO_2, SiO_2–TiO_2 and TiO_2 film was determined to be 1.45, 1.78 and

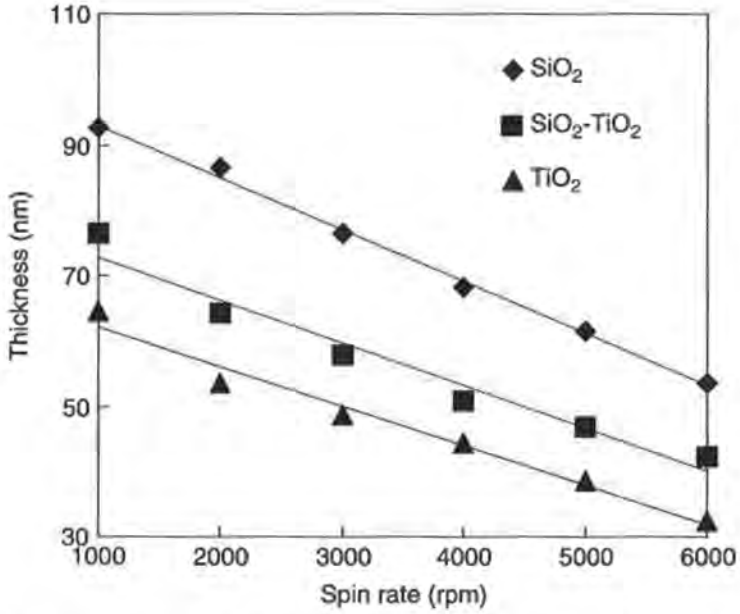

Fig. 3. Variations of SiO_2, SiO_2–TiO_2 and TiO_2 film thickness as a function ofspin rate.

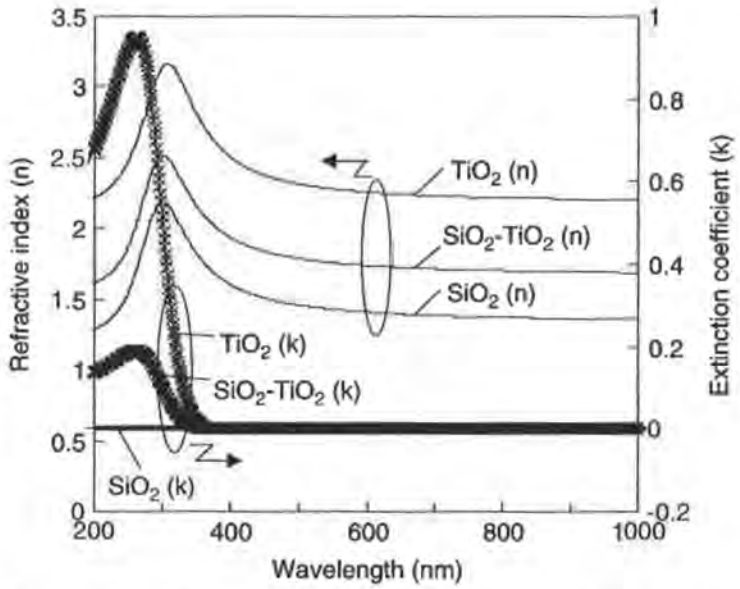

Fig. 4. Variations of extinction coefficients (k) and refractive index (n) of SiO_2, SiO_2–TiO_2 and TiO_2 films.

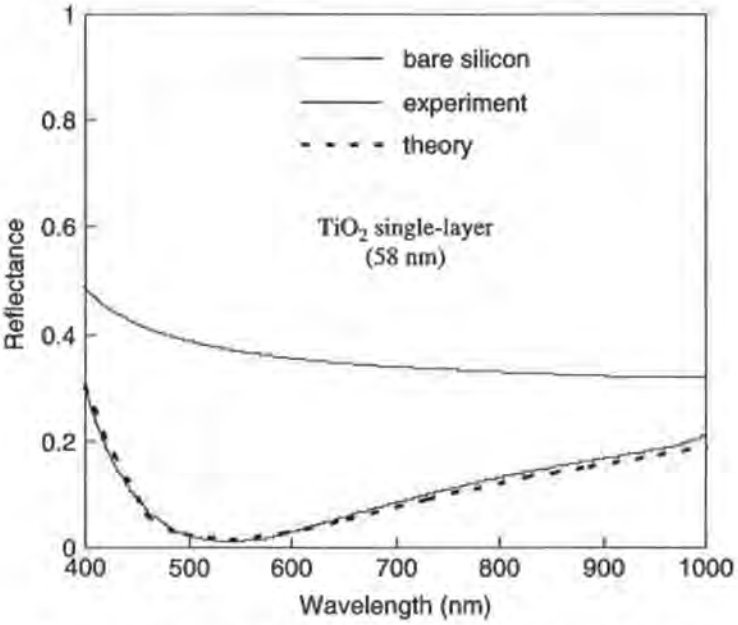

Fig. 5. Experimental and calculated reflectance data as a function of wavelength for TiO_2 single-layer ARC on Si substrate.

2.26 (for wavelength at 500 nm), respectively. It was found that the extinction coefficients (k) of each film after the annealing process almost approached to zero between 400 and 1000 nm.Furthermore, the absorbance point of the SiO_2–TiO_2 and TiO_2 films is located at a wavelength of 340 nm.These indicate that the sol–gel deposited SiO_2 and TiO_2 films can be used as ARCs for Si solar cells [21,22].

Fig. 5 shows the measured and calculated reflectance spectra of the TiO_2 single-layer ARC on non-textured Si substrates. It is well known that bare silicon has a high-refractive index, which leads to a solar-averaged reflectance of about 37%. The large reflection loss can be reduced significantly via a suitable ARC. A minimum value of reflectance $R(\lambda) = 0.5\%$ can be obtained at 536 nm.The average reflectance of approximately 9.3% between 400 and 1000 nm was obtained by the TiO_2 single-layer ARC on the non-textured Si substrate. The curves in Fig. 5 showed good agreement between the theoretical and experimental results for the reflectance data. The measured and calculated reflectance spectra of the optimized double-layer ARC are shown in Fig. 6. The reflectance $R(\lambda)$ is lower than 5% in the wavelength between 550 and 900 nm, which maximizes the absorption of the incident photons and increases the photo-generated current. The SiO_2/TiO_2 double-layer ARC results in a minimum reflectance of 1% at 690 nm with an average reflectance of approximately 6.2% between 400 and 1000 nm.That is, the Si absorbance increases by approximately 49.8%. Good correlation is also obtained between the theoretical and experimental results.

The experimental and theoretical reflectance data versus wavelength of the optimum triple-layer ARC structure are presented in Fig. 7. Here the theoretical SiO_2/SiO_2–TiO_2/TiO_2 triple-layer ARC on Si was calculated under normal optical incidence. The effective reflectance can reach 3.2% over 400–1000 nm range, indicating an increase in the absorption of the bare Si by approximately 54.6%. The difference in the short wavelength region is probably due to the dispersion of the refractive index in the wavelength region.

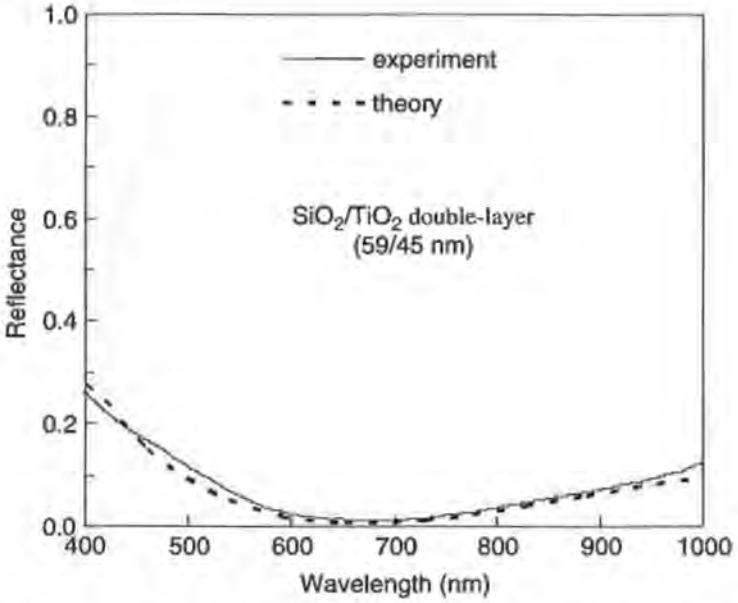

Fig. 6. Experimental and calculated reflectance data as a function of wavelength for SiO_2/TiO_2 double-layer ARCs on Si substrate.

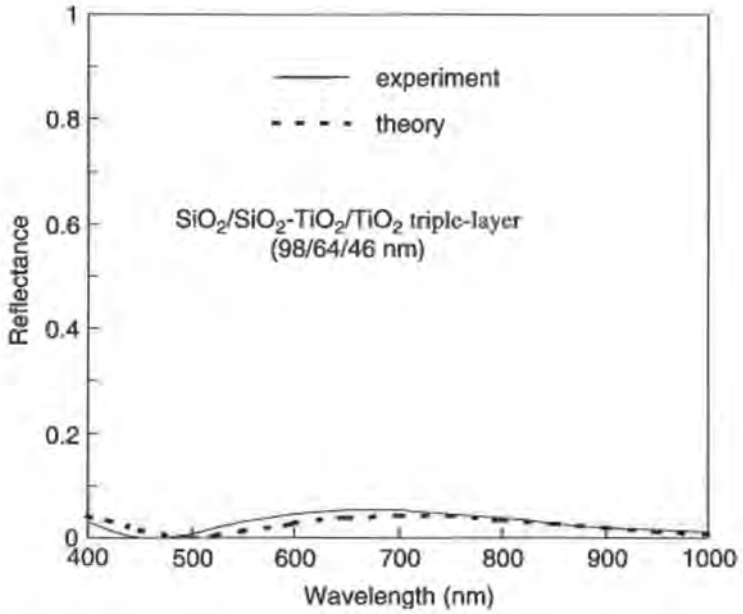

Fig. 7. Experimental and calculated reflectance data as a function of wavelength for SiO_2/SiO_2–TiO_2/TiO_2 triple-layer ARCs on Si substrate.

Finally, the current–voltage characteristics of the solar cell devices with sol–gel ARCs are shown in Fig. 8. Significant improvement of the short circuit current after ARCs was observed. However, the open-circuit voltage and the fill factor were not affected by the ARCs in these measurements. It is found that the current–voltage characteristic with a triple-layer ARC is better than that with double- or single-layer ARCs. Table 2 shows the device performance of the Si solar cells with various ARC structures. The performance of

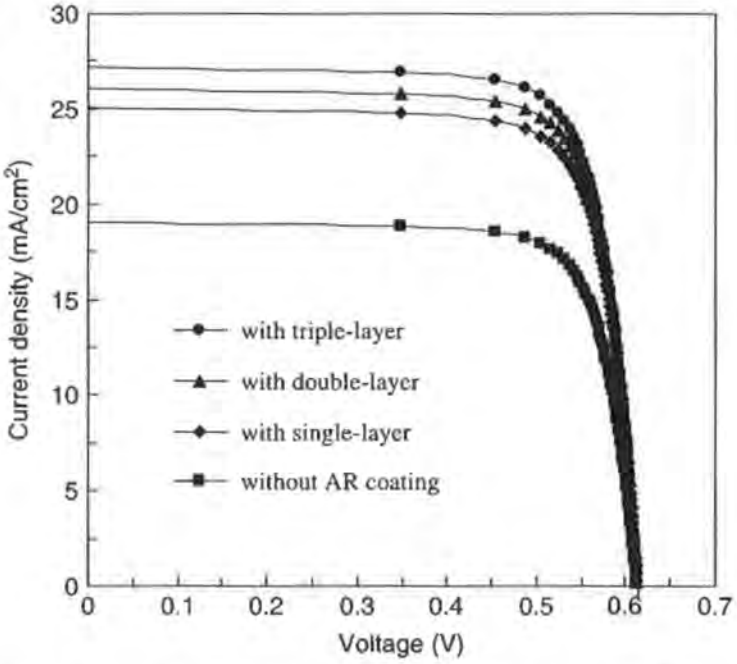

Fig. 8. Current density versus voltage characteristics of Si solar cells with triple-layer (●), double-layer (▲), single-layer (◆) and without ARCs (■).

Table 2
Characterization of Si solar cells with various antireflection coatings

Solar cell	Jsc (mA/cm^2)	Voc (V)	Fill factor (%)	Efficiency (%)
Bare silicon	16.2	0.61	76.4	11.36
Single-layer TiO_2	24.8	0.61	76.6	14.49
Double-layer SiO_2/TiO_2	25.8	0.61	76.2	14.99
Triple-layer SiO_2/SiO_2–TiO_2/TiO_2	27.1	0.61	76.7	15.85

bare Si solar cell without any ARC has an efficiency of 11.36%. The Si solar cells with triple-, double- and single-layer ARC show an increase of efficiency of about 39, 32 and 27%, respectively. That is, the efficiency of the Si solar cell with a triple-layer ARC can increase to 15.85% in the present work by utilizing a sol–gel technique.

4. Conclusions

This work presents a comprehensive experimental study with the aim to prepare high-quality single-, double- and triple-layer ARCs on Si solar cells using a sol–gel process. The effective refractive index and thickness of the films can be easily adjusted via the concentration of the sols, spin rate and annealed temperature. The reflectance of TiO_2 single-layer, SiO_2/TiO_2 double-layer and SiO_2/SiO_2–TiO_2/TiO_2 triple-layer ARCs was determined to be 9.3, 6.2 and 3.2%, respectively. The optical performance of the sol–gel-deposited ARC can be compared with that of the conventional ARC using more expensive vacuum processes such as PECVD or sputtering. A 39% enhancement in conversion

efficiency was obtained in the monocrystalline Si solar cell with a triple-layer ARC. In the future, using a combination of spin coating and rapid thermal annealing processes, the sol–gel ARCs could have high potential for continuous mass production of Si solar cells at a fraction of the cost.

Acknowledgments

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Tri-layer antireflection coatings ($SiO_2/SiO_2–TiO_2/TiO_2$) for silicon solar cells using a sol–gel technique

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Abstract

Antireflection coatings (ARCs) have become one of the key issues for mass production of Si solar cells. They are generally performed by vacuum processes such as thermal evaporation, reactive sputtering, and plasma-enhanced chemical vapor deposition. In this work, a sol–gel method has been demonstrated to prepare the ARCs for the non-textured monocrystalline Si solar cells. The spin-coated TiO_2 single-layer, SiO_2/TiO_2 double-layer and $SiO_2/SiO_2–TiO_2/TiO_2$ triple-layer ARCs were deposited on the Si solar cells and they showed good uniformity in thickness. The measured average optical reflectance (400–1000 nm) was about 9.3, 6.2 and 3.2% for the single-layer, double-layer and triple-layer ARCs, respectively. Good correlation between theoretical and experimental data was obtained. Under a triple-layer ARC condition, a 39% improvement in the efficiency of the monocrystalline Si solar cell was achieved. These indicate that the sol–gel ARC process has high potential for low-cost solar cell fabrication.
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Keywords: silicon; antireflection coating; sol–gel; TiO_2; SiO_2; solar cell

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1. Introduction

Antireflection coatings (ARCs) are widely used in various applications such as display panels, solar cells and optical lenses [1–3]. Thin-film ARCs can greatly reduce the optical loss in multi-element lenses by making use of phase changes and the dependence of the reflectivity on refraction index. A thin, dielectric film or several such films were applied to an optical surface to reduce its reflectance and thereby increase its transmittance. A single-layer ARC can be non-reflective only at one wavelength, usually at the middle of the visible region. Multiple layers are more effective over the entire visible spectrum. Several transparent and high refractive-index material films have already been applied to ARC techniques, e.g. SiO ($n = 1.8$–1.9), SiO_2 ($n = 1.44$), Si_3N_4 ($n = 1.9$), TiO_2 ($n = 2.3$), Al_2O_3 ($n = 1.86$), Ta_2O_5 ($n = 2.26$), SiO_2–TiO_2 ($n = 1.8$–1.96) and ZnS [4–9]. Optical coatings are generally performed by vacuum processes such as thermal evaporation, reactive sputtering, and plasma-enhanced chemical vapor deposition (PECVD). All these methods are capable of producing films with uniform thickness and good optical properties. However, the conventional vacuum deposition processes are expensive and unsuitable for continuous mass production techniques in low-cost solar cells. Recently, high refractive-index and high-transparency Si_3N_4 or TiO_2 single layer and SiO_2/TiO_2 double-layer have been developed and applied in solar cell ARCs process. These favorite films are prepared by PECVD and this results in reflectance below 10% [10–12].

Recently, ARCs have become one of the key issues for mass production of mono- and multi-crystalline Si solar cells. The sol–gel technique offers a simple and low-cost process to prepare the high-quality thin films [13,14]. In this work, the TiO_2 single-layer, SiO_2/TiO_2 double-layer and SiO_2/SiO_2–TiO_2/TiO_2 triple-layer ARCs on monocrystalline Si solar cells were prepared by a sol–gel spin-coating technique. To achieve minimum reflection of a normal incident wave of a single wavelength, the antireflection coating may consist of a single layer, which must possess (a) a refractive index equal to the square root of the refractive indices of the materials bounding the coating, and (b) a thickness equal to one-quarter of the wavelength (i.e., the wavelength within the material of which the coating consists). However, if one wants to achieve minimum reflection of multiple wavelengths, additional layers must be added. Kern and Tracy have observed an increase of 44% in the cell efficiency after spraying TiO_2 single-layer ARC [15]. Green et al. have used MgF_2/ZnS double-layer ARCs on Si cells with 19.1% efficiency [16]. In this paper, we present the results of calculations and experiments obtained by sol–gel method of single-layer, double-layer and triple-layer ARCs on polished silicon substrates. For an optimum ARCs design, the refractive index and thickness of each layer must be controllable to achieve the best performance along the desired spectrum. Details of the fabrication process and efficiency improvement will be described.

2. Experimental details

2.1. Sol–gel and spin coating process

The flow chart of the ARC synthesis process was performed using a sol–gel process as shown in Fig. 1. A clear solution is prepared by reacting metal alkoxide with a mixture of critical amount of water and/or acid in an alcohol diluted medium, and the SiO_2, SiO_2–TiO_2 and TiO_2 coatings were spin coated on the Si substrate from the above-said

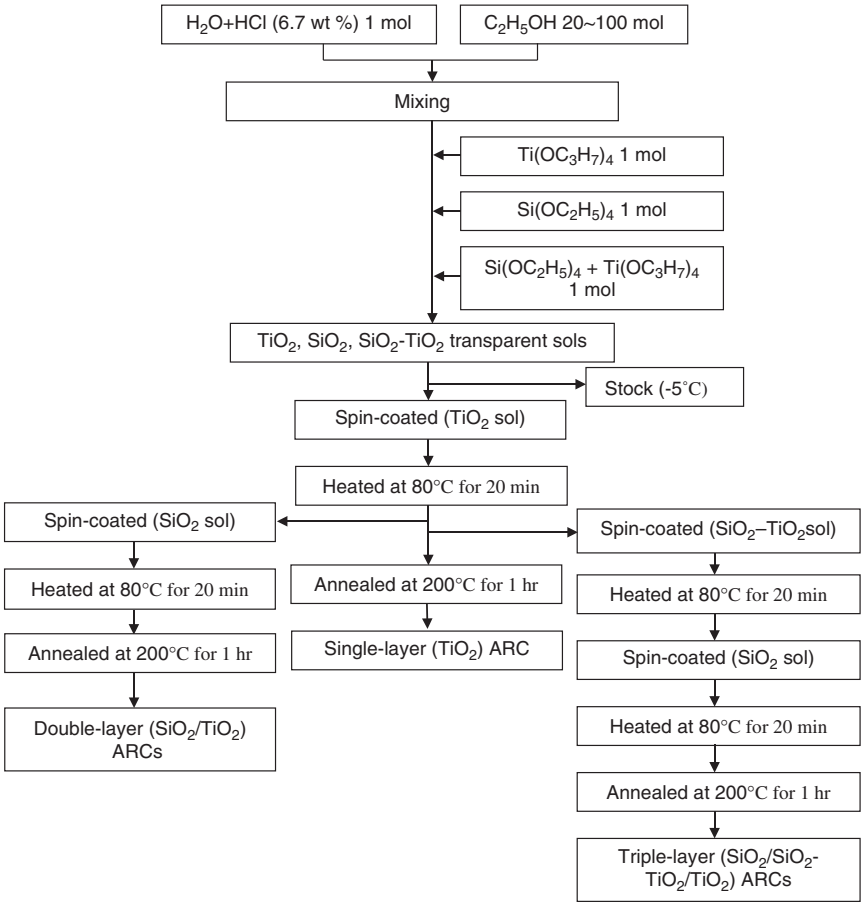

Fig. 1. Flow chart of sol–gel process for TiO_2 single-layer, SiO_2/TiO_2 double-layer and SiO_2/SiO_2–TiO_2/TiO_2 triple-layer antireflection coatings.

solution at 2000–6000 r.p.m for 30 s. The desired film thickness can be adjusted by the spin speed. Each film was pre-baked at 80°C for 20 min and then post baked at 200°C for 1 h in atmosphere. Table 1 tabulated the sol–gel parameters and deposition results of the SiO_2, SiO_2–TiO_2 and TiO_2 films. After spin coating and post-baking processes, the refractive index, thickness and reflectance of the film were measured using an n&k analyzer (model: 1280, N&K Tech. Inc.).

2.2. Design of single-layer, double-layer and triple-layer ARCs

In some applications, zero reflectance is needed at a single wavelength or throughout a narrow spectrum band. The optimum thickness and refractive index with a minimum

Table 1
Sol–gel parameters and deposition results of the SiO_2, SiO_2-TiO_2 and TiO_2 films

	$Ti(OC_3H_9)_4$:$Si(OC_2H_5)_4$:C_2H_5OH (mol)	Spin rate (r.p.m)	Thickness (nm)	Refractive index ($\lambda = 500$ nm)
TiO_2	1:0:60	2000–6000	64–33	2.26
SiO_2	0:1:80		93–54	1.45
SiO_2–TiO_2	1:1:80		76–42	1.78

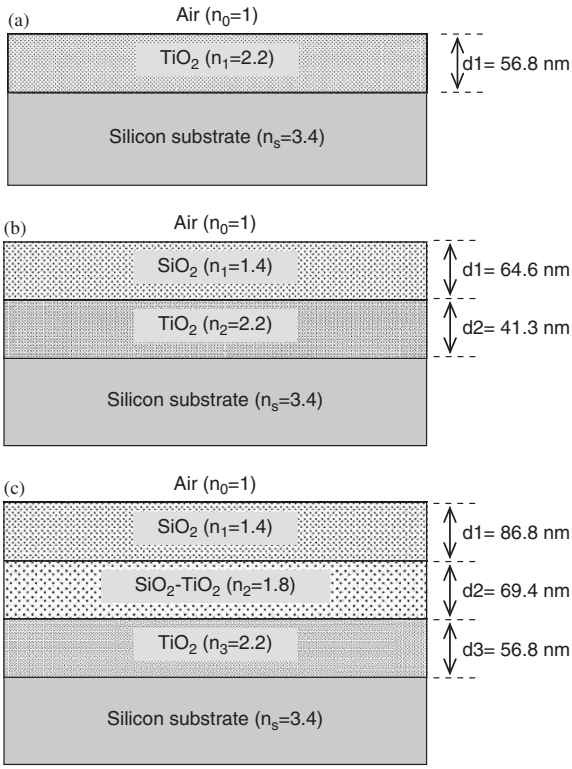

Fig. 2. Design diagram of antireflection coatings with (a) TiO_2 single layer, (b) SiO_2/TiO_2 double layers and (c) SiO_2/SiO_2–TiO_2/TiO_2 triple layers.

reflectance for a single-layer ARC can be deduced from

$$\lambda_0 = 4n_1 \times d_1, \tag{1}$$

where λ_0 is the midrange wavelength of 550 nm, n_1 and d_1 are the refractive index and layer thickness, respectively. A schematic diagram of this case is shown in Fig. 2(a).

For the double-layer ARC design, the low–high index on the Si substrate (i.e., the outer layer has the low refractive index and inner layer has high refractive index) is used.

Fig. 2(b) shows a typical double-layer ARC structure, where n_0, n_s, n_1 and n_2 correspond to the refractive index of air, substrate, outer and inner layers, respectively. Moreover, d_1 and d_2 represent the thickness of the outer and inner layers, respectively. Each layer must meet Eqs. (2) and (3) in order to achieve a zero reflectance [17],

$$\frac{n_2 d_2}{\lambda_0} = \frac{1}{2\pi}\tan^{-1}\left\{\pm\left[\frac{(n_s - n_0)(n_0 n_s - n_1^2)n_2^2}{(n_1^2 n_s - n_0 n_2^2)(n_2^2 - n_0 n_s)}\right]^{1/2}\right\}, \tag{2}$$

$$\frac{n_1 d_1}{\lambda_0} = \frac{1}{2\pi}\tan^{-1}\left\{\pm\left[\frac{(n_s - n_0)(n_0 n_s - n_2^2)n_1^2}{(n_1^2 n_s - n_0 n_2^2)(n_1^2 - n_0 n_s)}\right]^{1/2}\right\}. \tag{3}$$

The design of triple-layer ARC on Si can be optimized using Eqs. (4–6) when the optimum refractive index and thickness of each layer in the stack is calculated,

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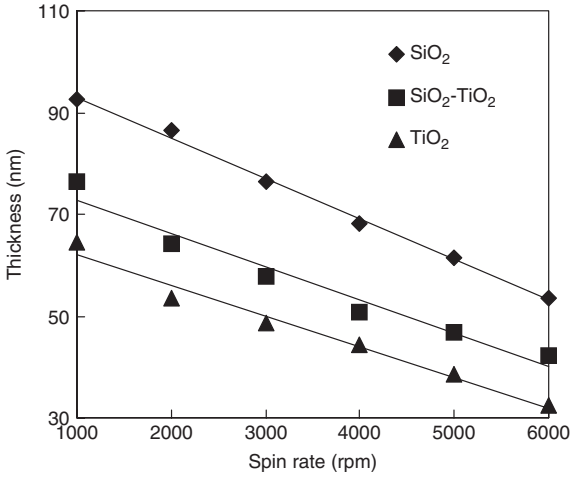
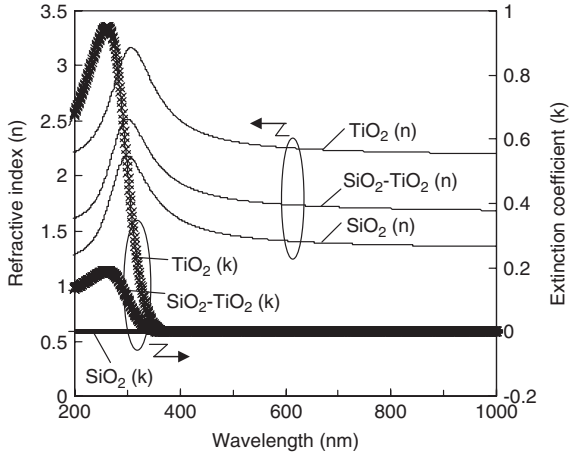


Fig. 3. Variations of SiO_2, SiO_2–TiO_2 and TiO_2 film thickness as a function ofspin rate.



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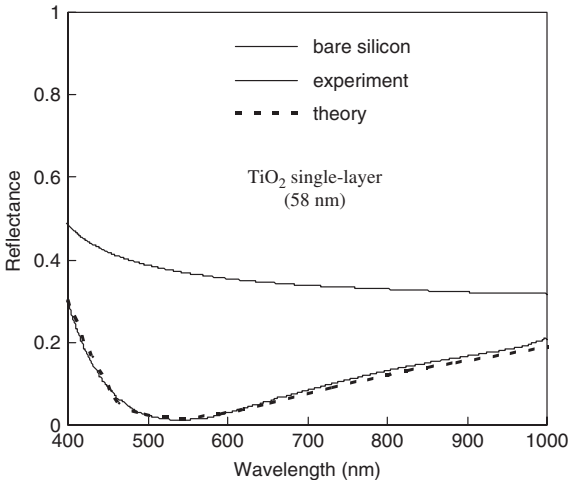

Fig. 5. Experimental and calculated reflectance data as a function of wavelength for TiO_2 single-layer ARC on Si substrate.

2.26 (for wavelength at 500 nm), respectively. It was found that the extinction coefficients (k) of each film after the annealing process almost approached to zero between 400 and 1000 nm.Furthermore, the absorbance point of the SiO_2–TiO_2 and TiO_2 films is located at a wavelength of 340 nm.These indicate that the sol–gel deposited SiO_2 and TiO_2 films can be used as ARCs for Si solar cells [21,22].

Fig. 5 shows the measured and calculated reflectance spectra of the TiO_2 single-layer ARC on non-textured Si substrates. It is well known that bare silicon has a high-refractive index, which leads to a solar-averaged reflectance of about 37%. The large reflection loss can be reduced significantly via a suitable ARC. A minimum value of reflectance $R(\lambda) = 0.5\%$ can be obtained at 536 nm.The average reflectance of approximately 9.3% between 400 and 1000 nm was obtained by the TiO_2 single-layer ARC on the non-textured Si substrate. The curves in Fig. 5 showed good agreement between the theoretical and experimental results for the reflectance data. The measured and calculated reflectance spectra of the optimized double-layer ARC are shown in Fig. 6. The reflectance R(λ) is lower than 5% in the wavelength between 550 and 900 nm, which maximizes the absorption of the incident photons and increases the photo-generated current. The SiO_2/TiO_2 double-layer ARC results in a minimum reflectance of 1% at 690 nm with an average reflectance of approximately 6.2% between 400 and 1000 nm.That is, the Si absorbance increases by approximately 49.8%. Good correlation is also obtained between the theoretical and experimental results.

The experimental and theoretical reflectance data versus wavelength of the optimum triple-layer ARC structure are presented in Fig. 7. Here the theoretical SiO_2/SiO_2–TiO_2/TiO_2 triple-layer ARC on Si was calculated under normal optical incidence. The effective reflectance can reach 3.2% over 400–1000 nm range, indicating an increase in the absorption of the bare Si by approximately 54.6%. The difference in the short wavelength region is probably due to the dispersion of the refractive index in the wavelength region.

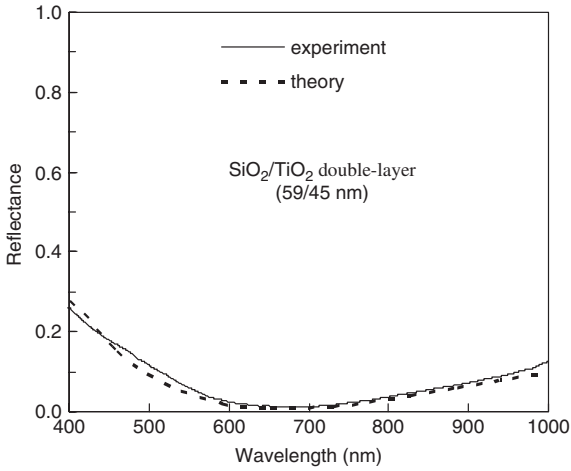

Fig. 6. Experimental and calculated reflectance data as a function of wavelength for SiO_2/TiO_2 double-layer ARCs on Si substrate.

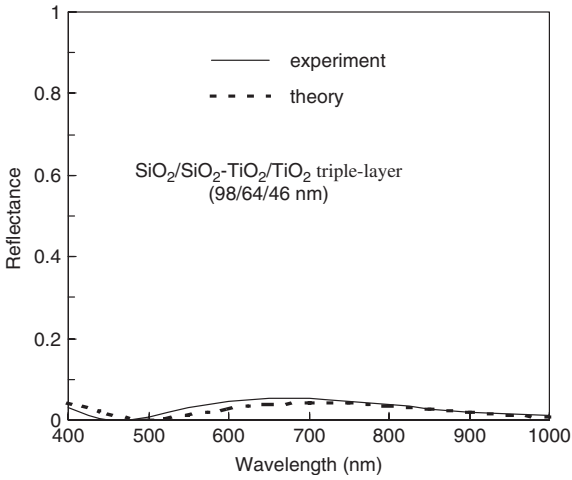

Fig. 7. Experimental and calculated reflectance data as a function of wavelength for SiO_2/SiO_2–TiO_2/TiO_2 triple-layer ARCs on Si substrate.

Finally, the current–voltage characteristics of the solar cell devices with sol–gel ARCs are shown in Fig. 8. Significant improvement of the short circuit current after ARCs was observed. However, the open-circuit voltage and the fill factor were not affected by the ARCs in these measurements. It is found that the current–voltage characteristic with a triple-layer ARC is better than that with double- or single-layer ARCs. Table 2 shows the device performance of the Si solar cells with various ARC structures. The performance of

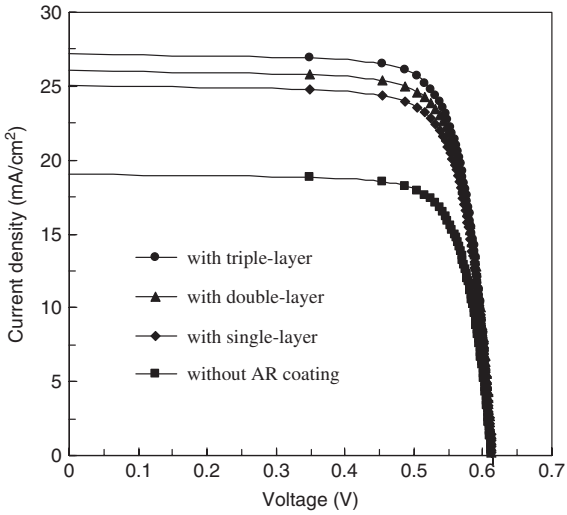

Fig. 8. Current density versus voltage characteristics of Si solar cells with triple-layer (●), double-layer (▲), single-layer (◆) and without ARCs (■).

Table 2
Characterization of Si solar cells with various antireflection coatings

Solar cell	Jsc (mA/cm^2)	Voc (V)	Fill factor (%)	Efficiency (%)
Bare silicon	16.2	0.61	76.4	11.36
Single-layer TiO_2	24.8	0.61	76.6	14.49
Double-layer SiO_2/TiO_2	25.8	0.61	76.2	14.99
Triple-layer SiO_2/SiO_2–TiO_2/TiO_2	27.1	0.61	76.7	15.85

bare Si solar cell without any ARC has an efficiency of 11.36%. The Si solar cells with triple-, double- and single-layer ARC show an increase of efficiency of about 39, 32 and 27%, respectively. That is, the efficiency of the Si solar cell with a triple-layer ARC can increase to 15.85% in the present work by utilizing a sol–gel technique.

4. Conclusions

This work presents a comprehensive experimental study with the aim to prepare high-quality single-, double- and triple-layer ARCs on Si solar cells using a sol–gel process. The effective refractive index and thickness of the films can be easily adjusted via the concentration of the sols, spin rate and annealed temperature. The reflectance of TiO_2 single-layer, SiO_2/TiO_2 double-layer and SiO_2/SiO_2–TiO_2/TiO_2 triple-layer ARCs was determined to be 9.3, 6.2 and 3.2%, respectively. The optical performance of the sol–gel-deposited ARC can be compared with that of the conventional ARC using more expensive vacuum processes such as PECVD or sputtering. A 39% enhancement in conversion

efficiency was obtained in the monocrystalline Si solar cell with a triple-layer ARC. In the future, using a combination of spin coating and rapid thermal annealing processes, the sol–gel ARCs could have high potential for continuous mass production of Si solar cells at a fraction of the cost.

Acknowledgments

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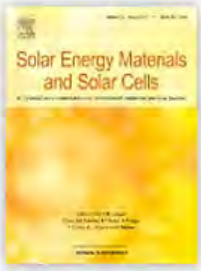

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Attachment K-1

Progress in Surface Passivation of Heavily Doped n-Type and p-Type Silicon by Plasma-Deposited AlO_x/SiN_x Dielectric Stacks

Shubham Duttagupta, Fa-Jun Ma, Serena Fen Lin, Thomas Mueller, Armin G. Aberle, and Bram Hoex

***Abstract*—We report an outstanding level of surface passivation for both n^+ and p^+ silicon by AlO_x/SiN_x dielectric stacks deposited in an inline plasma-enhanced chemical vapor deposition (PECVD) reactor for a wide range of sheet resistances. Extremely low emitter saturation current densities (J_{0e}) of 12 and 200 fA/cm^2 are obtained on 165 and 25 Ω/sq n^+ emitters, respectively, and 8 and 45 fA/cm^2 on 170 and 30 Ω/sq p^+ emitters, respectively. Using contactless corona–voltage measurements and device simulations, we demonstrate that the surface passivation mechanism on both n^+ and p^+ silicon is primarily due to a relatively low interface defect density of $<10^{11}$ eV^{-1}cm^{-2} in combination with a moderate fixed negative charge density of (1–2) $\times$ 10^{12} cm^{-2}. From advanced modeling, the fundamental surface recombination velocity parameter is shown to be in the order of 10^4 cm/s for PECVD AlO_x/SiN_x passivated heavily doped n^+ and p^+ silicon surfaces.**

***Index Terms*—Aluminum oxide/silicon nitride (AlO_x/SiN_x) stacks, boron-doped emitters, crystalline silicon, phosphorus-doped emitters, plasma-enhanced chemical vapor deposition (PECVD), surface passivation.**

I. Introduction

In recent years, amorphous aluminum oxide (AlO_x) has received tremendous interest from the photovoltaic community for its application as a surface passivation film for crystalline silicon wafer solar cells. AlO_x films provide excellent surface passivation on lightly doped n-type and p-type silicon as well as on heavy doped p^+ silicon [1]–[5]. In addition to a low interface defect density ($\sim 10^{11}$ eV^{-1}cm^{-2}), a distinguished property of AlO_x is the presence of a high negative charge density (10^{12}–10^{13} cm^{-2}, in units of elementary charges) in the film. This is especially beneficial on p-type c-Si surfaces as the minority carriers (electrons) are effectively shielded from the c-Si surface. Because of its excellent surface passivation properties on p-type surfaces, AlO_x has mainly been considered for the application in p-type passivated emitter and rear cell cells, p-type aluminum local back-surface field (Al-LBSF) cells, and n-type passivated emitter and rear locally diffused cells [6], [7].

Excellent passivation of heavily doped n^+ and p^+ silicon surfaces is very important for high-efficiency Si wafer solar cells. Some solar cell structures, such as interdigitated back-contact (IBC) solar cells, require simultaneous passivation of both dopant polarities [8], [9]. For this application, preferentially a suitable dielectric is needed that can passivate both n^+ and p^+ silicon surfaces simultaneously. Thick ($\sim$100 nm) thermal silicon oxide (SiO_2) films or stacks consisting of a thin (5–30 nm) SiO_2 film capped by a 50–100-nm-thick silicon nitride (SiN_x) film are often used due to their ability to passivate both n^+ and p^+ silicon surfaces [8]–[12]. However, low-temperature ($<$400 °C) surface passivation is typically preferred for the fabrication of industrial high-efficiency silicon wafer solar cells, due to its potential cost effectiveness, lower thermal budget, and the possibility for inline processing. Recently, Mihailetchi *et al*. reported excellent results for p^+ surfaces passivated by a stack consisting of an ultrathin oxide grown by hot HNO_3 and then capped with a SiN_x film [13]. Although no specific results are available in regards to its capability of passivating n^+ silicon surfaces, it can be considered a good method for passivating both n^+ and p^+ silicon surfaces simultaneously as these layers have already been used for large-area screen-printed IBC solar cells showing good efficiencies [14]–[17]. However, it should be noted that these devices showed moderate implied V_{oc} (iV_{oc}) in the range of 660–680 mV and also resulted in moderate solar cell open-circuit voltages of $V_{oc} < 650$ mV [14]–[17]. It is also suggested in these publications that an optimized dielectric is still needed that can passivate both n^+ and p^+ silicon surfaces simultaneously in order to achieve higher open-circuit voltage, and therefore, higher solar cell efficiency.

AlO_x films provide excellent surface passivation on p^+ silicon for an arbitrary sheet resistance [2], [18], [19]. Recently it has been shown that n^+-doped Si in a certain sheet resistance range can also be passivated by Al_2O_3 films grown by plasma-assisted and O_3-based atomic layer deposition (ALD), however, the results are not yet competitive [20], [21]. In addition, PA-ALD is not yet an industrially feasible technique. Thus, it is of great interest to investigate if negatively charged AlO_x films deposited by the industrial PECVD can provide excellent passivation on both n^+ and p^+ silicon surfaces.

In this study, we demonstrate that PECVD AlO_x/SiN_x dielectric stacks can provide excellent passivation on both heavily doped n^+ and p^+ silicon surfaces that are relevant for the industrial solar cell application. These results are primarily explained

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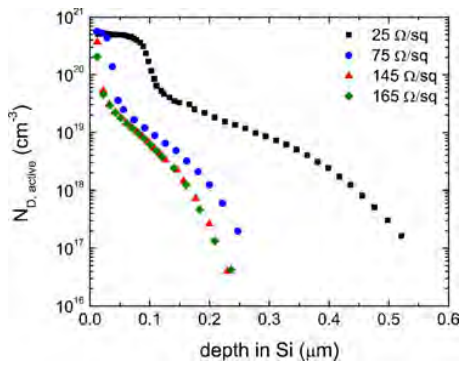

Fig. 1. Phosphorus dopant profile of n^+pn^+ samples measured by ECV profiling. The sheet resistance values determined by four-point probe measurements are shown in the graph.

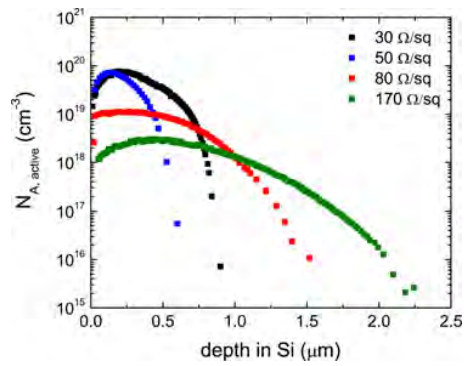

Fig. 2. Boron dopant profile of p^+np^+ samples measured by ECV profiling. The sheet resistance values determined by four-point probe measurements are shown in the graph.

by a low midgap interface defect density of $<10^{11}$ eV^{-1}cm^{-2}, which is beneficial for both n^+ and p^+ silicon surfaces. The stacks developed in this study feature a relatively moderate fixed negative charge density of (1–2) $\times$ 10^{12} cm^{-2}, as determined by contactless corona–voltage (*C–V*) experiments. Based on device simulations, we show that moderate fixed charge densities in the range of -10^{12} cm^{-2}–10^{12} cm^{-2} do not significantly affect the emitter saturation current density of typical industrial n^+ diffusions. Thus, the passivation is mainly ruled by the excellent electronic quality of the interface or low interface defect density.

II. Experimental Details

Symmetrical n^+pn^+ carrier lifetime structures were fabricated using an industrial $POCl_3$ diffusion process. The sheet resistance of the n^+ emitter was varied by changing the temperature and time of the $POCl_3$ diffusion. The phosphorus dopant profiles of the n^+pn^+ samples used in this study were measured with the electrochemical voltage (ECV) method, as shown in Fig. 1. The p-type Si wafers were monocrystalline (Cz method, boron-doped, 5–8 Ωcm), about 150 μm thick, pseudosquare (125 mm $\times$ 125 mm), and with a (100) surface orientation.

The p^+np^+ structures were fabricated by an industrial BBr_3 diffusion process. The p^+ emitter sheet resistance was varied by varying the process conditions during the BBr_3 diffusion and by a postdiffusion oxidation, as explained in detail elsewhere [18]. The boron dopant profiles of the p^+np^+ samples used in this study were measured by the ECV method, as shown in Fig. 2. The n-type Si wafers were monocrystalline (Cz, phosphorus-doped, 6–8 Ωcm), about 150 μm thick, pseudosquare (125 mm $\times$ 125 mm), and with a (100) surface orientation. After the diffusion process, the phosphorus or borosilicate glass layers were removed by dipping in HF solution, followed by rinsing in deionised water.

Prior to the deposition of the PECVD dielectric films, the samples were cleaned using the Radio Corporation of America (RCA) clean with a final HF dip followed by water rinsing and drying to ensure an H-terminated surface. The sheet resistance of the p^+ and n^+ diffusions was unaffected by the predeposition cleaning as confirmed by four-point probe measurements. The n^+pn^+ and p^+np^+ samples with various sheet resistances were coated on both sides with 30-nm AlO_x capped with 70-nm SiN_x, using an industrial inline microwave-powered remote PECVD reactor (SiNA-XS, Roth & Rau, Germany). We emphasize that all samples (n^+pn^+ and p^+np^+) were processed without any change in the PECVD process conditions. The deposition conditions are summarized in Table I.

After the PECVD processes, the samples received an activation anneal in an industrial fast firing furnace (Ultraflex, Despatch, USA) for a few seconds at a set peak temperature of $>$800 °C, similar to the cofiring step applied to the screen-printed metallization of industrial silicon wafer solar cells. The effective minority carrier lifetime $(\tau_{\rm eff})$ of the lifetime samples was measured using a contactless flash-based photoconductance decay tester (WCT-120, Sinton Instruments), in both the quasi-steady-state and the transient mode [22]. From the $\tau_{\rm eff}$ measurement, the emitter saturation current density (J_{0e}) per side of the n^+pn^+ and p^+np^+ samples was extracted from the slope of the Auger-corrected inverse lifetime versus injection level curve under high-injection conditions ($\Delta n \sim 10^{15}$ to 10^{16} cm^{-3} in our case), using the relation proposed by Kane and Swanson [23];

$$\frac{1}{\tau_{\rm eff}} - \frac{1}{\tau_{\rm Auger}} = \frac{1}{\tau_{\rm SRH}} + 2\frac{J_{0e}\left(N_d + \Delta n\right)}{q n_i^2 W} \qquad (1)$$

where $\tau_{\rm Auger}$ and $\tau_{\rm SRH}$ are the Auger lifetime and the Shockley–Read–Hall lifetime in the bulk of the sample [24], respectively, N_d and Δn are the doping concentration and the excess carrier concentration (or "injection level") in the bulk of the sample, q is the elementary charge, n_i is the intrinsic carrier concentration (8.6 $\times$ 10^9 cm^{-3} at 298 K) [25], and W is the thickness of the sample. In addition, contactless *C–V* measurements (PV-2000, Semilab SDI Inc., USA) were carried out to extract the fixed charge density (Q_f) and the interface defect density $(D_{\rm it})$ of the dielectric films on undiffused Si samples. The details of the measurement system and extraction procedure of Q_f and $D_{\rm it}$ are explained elsewhere [26]–[29].

III. Results and Discussion

Fig. 3 shows the measured injection level dependence of the Auger-corrected inverse effective carrier lifetime of industrially fired n^+pn^+ samples passivated on both sides by a PECVD AlO_x/SiN_x dielectric stack. The results cover a wide range of industry relevant sheet resistances (25–165 Ω/sq).

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TABLE I
EXPERIMENTAL DETAILS USED FOR THE DEPOSITION OF THE DIELECTRIC FILMS IN THIS STUDY

Dielectric	Process gas	Deposition temperature (°C)	Reactor pressure (mbar)	Plasma power (W)
AlO_x	$Al(CH_3)_3 + N_2O + Ar$	450	0.10	1500
SiN_x	$SiH_4 + NH_3$	200	0.20	3000

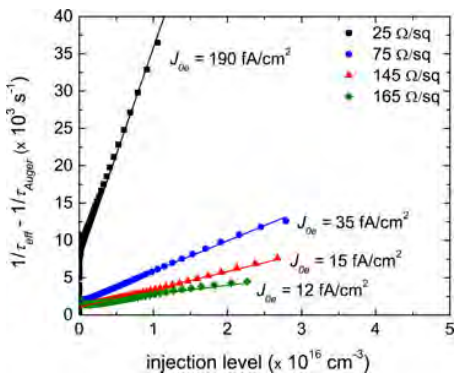

Fig. 3. Measured injection level dependence of the Auger-corrected inverse effective lifetime of industrially fired n^+pn^+ samples symmetrically passivated by PECVD AlO_x/SiN_x dielectric stacks (symbols). The sheet resistance of the n^+ emitters determined by four point probe measurements is shown in the legend. The J_{0e} values obtained from the straight-line fits (solid lines) are also shown.

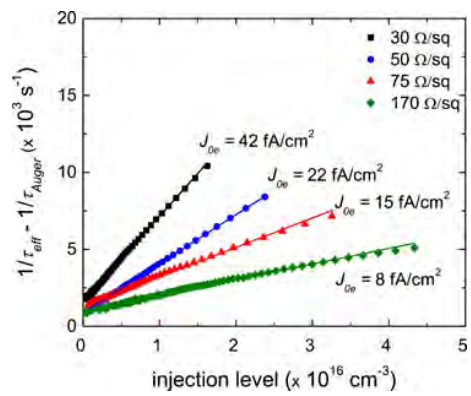

Fig. 4. Measured injection level dependence of the Auger-corrected inverse effective lifetime of industrially fired p^+np^+ samples symmetrically passivated by PECVD AlO_x/SiN_x dielectric stacks (symbols). The sheet resistance of the p^+ emitters determined by four point probe measurements is shown in the legend. The J_{0e} values obtained from the straight-line fits (solid lines) are also shown.

It is emphasized that we observe a linear relationship for all lifetime samples, allowing the extraction of J_{0e} values using (1). This was not always the case in the work of Hoex *et al.*, where it was mentioned that the relationship was not linear for 100–200 Ω/sq n^+ emitters passivated by PA-ALD Al_2O_3 [20]. This was attributed to the very high negative fixed charge density (up to 10^{13} cm^{-2}) of PA-ALD Al_2O_3 films, which strongly increased the minority carrier (hole) density at the n^+ surface in their work, and thereby, caused an injection level dependent J_{0e}. In this study, we show an excellent level of surface passivation with extremely low J_{0e} values of 12 fA/cm^2 for 165 Ω/sq planar n^+ emitters passivated by PECVD AlO_x/SiN_x dielectric stacks after an industrial firing process. As a matter of fact, the J_{0e} values obtained in this study are similar to, or even better than, the best values reported in the literature for n^+ emitters passivated by PECVD SiN_x [30]. These results are also significantly better than those obtained for n^+ emitters passivated by Al_2O_3 grown by ALD techniques reported so far [20], [21].

Identical PECVD stacks were also used to passivate p^+ emitters. Fig. 4 shows the measured injection level dependence of the Auger-corrected inverse effective carrier lifetimes of industrially fired p^+np^+ samples passivated on both sides with an AlO_x/SiN_x dielectric stack. The lifetime samples show a clear linear relationship, indicating again that (1) can be used to extract the J_{0e} value of this emitter. An extremely low J_{0e} value of 8 fA/cm^2 was obtained for a 170-Ω/sq emitter, which is comparable with the values obtained for p^+ emitters passivated by Al_2O_3 films grown by the PA-ALD [2]. It should be noted that in our earlier work, p^+np^+ samples were passivated on both sides with an AlO_x/SiN_x dielectric stack deposited under slightly different processing conditions [18]. In this study, both n^+pn^+ and p^+np^+ samples were processed simultaneously with 100 °C higher deposition temperature for AlO_x and ∼100 °C lower deposition temperature for capping SiN_x layer. This resulted in better interface quality and more importantly, a reduced fixed charge density. These stacks also provide excellent results on p^+ Si surfaces for a wide range of sheet resistance with similar J_{0e} values as reported earlier [18].

Table II summarizes the experimentally measured effective lifetime (τ_{eff} at $\Delta n = 10^{15}$ cm^{-3}), emitter saturation current density (J_{0e}), and implied V_{oc} (iV_{oc}) for n^+pn^+ and p^+np^+ samples symmetrically passivated by an industrially fired AlO_x/SiN_x dielectric stack. Note that effective lifetime and implied V_{oc} also depends on factors such as bulk doping level and bulk effective minority carrier lifetime of the used silicon wafer and the optical properties of the passivation coating, hence, care must be taken when comparing experimental values between different experiments. $V_{\text{oc,limit}}$ represents the one-Sun open-circuit voltage limit of a solar cell at 25 °C calculated from the experimentally measured J_{0e} and assuming a short-circuit current density (J_{sc}) of 40 mA/cm^2 with an ideal diode law ($n = 1$) by [22], [31]:

$$V_{\text{oc,limit}} = n\frac{kT}{q}\ln\left(\frac{J_{\text{sc}}}{J_{0e}} + 1\right) \tag{2}$$

where n is the diode ideality factor, which is considered one in this calculation. kT/q is 25.9 mV at 25 °C with k, T, q being the Boltzmann constant, absolute temperature in Kelvin and the elementary charge, respectively.

Fig. 5 shows the experimentally obtained J_{0e} values for n^+ and p^+ emitters passivated by industrially fired PECVD

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TABLE II
EXPERIMENTALLY DETERMINED EFFECTIVE LIFETIME ($\tau_{\rm eff}$) AT $\Delta n = 10^{15}$ cm^{-3}, SATURATION CURRENT DENSITY (J_{0e}) PER SIDE AND IMPLIED $V_{\rm oc}$ ($iV_{\rm oc}$) FOR n^+pn^+ AND p^+np^+ SAMPLES SYMMETRICALLY PASSIVATED BY AN AlO_x/SiN_x STACK

	Sheet resistance for phosphorus-diffused n^+ surface on p-type Si (Ω/sq.)				Sheet resistance for boron-diffused p^+ surface on n-type Si (Ω/sq.)			
	25	**75**	**145**	**165**	**30**	**50**	**80**	**170**
τ_{eff} **(µs)**	94	465	770	700	484	841	700	930
J_{0e} **(fA/cm²)**	190	35	15	12	45	22	15	8
iV_{oc} **(mV)**	640	688	706	703	670	690	700	712
$V_{oc,\,limit}$ **(mV)**	670	713	735	741	707	725	735	751

The $V_{\rm oc,limit}$ was calculated by (2) using the measured J_{0e} values.

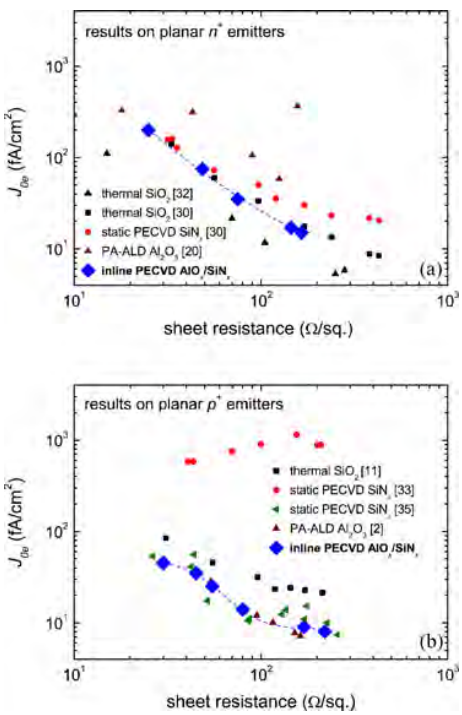

Fig. 5. Experimentally obtained J_{0e} values (diamonds in this work) for (a) n^+ emitters and (b) p^+ emitters passivated by industrially fired PECVD AlO_x/SiN_x stacks (the dotted lines are guides to the eye). Each of our J_{0e} values is the average result of a batch of 10 samples. Also shown, for comparison, are state-of-the-art J_{0e} values reported in the literature for planar n^+ and p^+ emitters passivated by thermal SiO_2, PECVD SiN_x, and ALD-grown Al_2O_3.

AlO_x/SiN_x stacks. For comparison, the best published results from the literature are included as well. It should be noted that the preparation of the n^+ and p^+ emitters in the various studies were different and most likely resulted in different dopant profiles for a comparable sheet resistance. This potentially affects the Auger recombination losses in these emitters. However, the general trend can be used for comparison. It is evident from Fig. 5 that thermal SiO_2 is a good candidate for both dopant polarities, showing excellent surface passivation of n^+ emitters and a decent surface passivation for p^+ emitters after either *alneal* (aluminum-annealing) or forming gas anneal (FGA) [11], [30], [32]. PECVD SiN_x provides excellent passivation of n^+ emitters after FGA [30]. Generally, these SiN_x films provide a compromised level of surface passivation on p^+ emitters [11], [33]. Only limited reports are available were PECVD SiN_x provides a good level of surface passivation on p^+ emitters, however, the underlying mechanism is not yet properly understood [34], [35]. Similarly PA-ALD Al_2O_3 films provide only a moderate passivation on n^+ emitters [see Fig. 5(a)], however, p^+ surfaces with an arbitrary sheet resistance can be well passivated with PA-ALD Al_2O_3 films [2], [20]. Based on the experimental results presented in this study, it is clear that our industrially fired PECVD AlO_x/SiN_x stacks provide an excellent level of surface passivation on both n^+ and p^+ emitters, for the entire investigated sheet resistance range. Hence, our work demonstrates that these PECVD AlO_x/SiN_x stacks can be used to simultaneously passivate all c-Si surfaces that are of relevance in today's PV industry.

To obtain more insight into the interface properties such as fixed charge density (Q_f) and interface defect density (D_{it}) of our industrially fired AlO_x/SiN_x stacks, contactless *C–V* measurements were performed on undiffused Si samples. These measurements revealed that the industrially fired AlO_x/SiN_x dielectric stacks on c-Si used in this study have a comparatively low midgap interface defect density of $<10^{11}$ eV^{-1}cm^{-2} in combination with a moderate negative fixed charge density in the range of (1–2) $\times$ 10^{12} cm^{-2}. Note that the fixed charge density in the dielectric stack is highly dependent on the deposition conditions and the postdeposition treatments used, as will be reported in detail in a separate study.

Understanding the surface passivation of p^+ Si surfaces by negatively charged dielectrics is relatively straightforward. A low interface defect density provides excellent chemical passivation. In addition, the negative fixed charge density reduces the minority carrier concentration at p^+ Si surfaces (for the B surface concentrations investigated in this study) providing field-effect passivation. Understanding the passivation of n^+ Si surfaces by negatively charged dielectrics is, however, not straightforward. For this purpose, we used advanced computer modeling (TCAD, Sentaurus) to study the role of field-effect passivation for heavily doped n^+ surfaces. In these simulations, we take both the fundamental hole surface recombination

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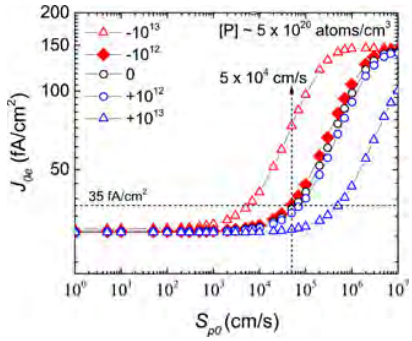

Fig. 6. Simulated J_{0e} as a function of the S_{p0} at the c-Si/dielectric interface for high (10^{13} cm^{-2}) and moderate (10^{12} cm^{-2}) fixed charge densities of both polarities in the dielectric film. A symmetrical n$^+$pn$^+$ sample was used with a 75-Ω/sq diffusion per side (the experimental measured diffusion profile from Fig. 1 was used in the simulation).

velocity parameter (S_{p0}) and the interface fixed charge (Q_f) into account, similar to the approach presented by Girish *et al.* [36] and Aberle *et al.* [37], and furthermore, using the physical models from [38] and [39], S_{p0} is the surface recombination velocity parameter for holes assuming flat band conditions and can be expressed by

$$S_{p0} \equiv \nu_{\rm th}\sigma_p N_{\rm st} \tag{3}$$

where $v_{\rm th}$ is the thermal velocity, σ_p is the capture cross-section for holes, and $N_{\rm st}$ is the number of surface states per unit area [40]. Using the measured n$^+$ dopant profile of the 75 Ω/sq diffusion from Fig. 1, J_{0e} versus S_{n0} curves for various fixed charge densities were determined. The results are shown in Fig. 6. From Fig. 6, it is clear that positive fixed charge densities are beneficial for the passivation of the 75-Ω/sq n$^+$ Si diffusion, resulting in significantly lower J_{0e} values for similar S_{p0} values. On the other side, a very high negative fixed charge density of 10^{13} cm^{-2} is found to be detrimental and results in higher J_{oe} values, in good agreement with the experimental results reported by Hoex *et al.* for n$^+$ Si passivated by Al_2O_3 films grown by the PA-ALD [20].

For moderate fixed interface charge densities in the range of -10^{12} cm^{-2} to $+10^{12}$ cm^{-2}, it can be seen that the fixed charge is hardly affecting the J_{0e} over the whole investigated S_{p0} range, and hence, the passivation is predominantly ruled by chemical passivation in this case. It should be noted that a similar trend (effect of fixed charge) was observed on other n$^+$ diffusions used in this study; however, the fixed charge range will depend on the surface dopant concentration. The results in Fig. 6 also allow us to extract the S_{p0} value at the interface between the c-Si wafer and the AlO_x/SiN_x stack. Taking the measured J_{0e} value of 35 fA/cm^2 and the measured Q_f of -10^{12} cm^{-2}, we can see that this results in a S_{p0} value of $\sim 5 \times 10^4$ cm/s. This value is in the similar order to the S_{n0} (electron surface recombination velocity parameter) value obtained by our PECVD AlO_x/SiN_x stack on heavily doped p$^+$ Si surfaces, which is in the range of 10^4 cm/s [41]. We observe that the S_{p0} value obtained in this study is slightly better than the S_{p0} reported by Altermatt *et al.* ($> 10^5$ cm/s) for n$^+$ Si having a surface dopant density of $\sim 2 \times 10^{20}$ atoms/cm^3 passivated by FGA thermal SiO_2 [39]. Hence, these results indicate that heavily doped n$^+$ Si surfaces can be passivated as effectively as heavily doped p$^+$ Si surfaces using a negatively charged PECVD AlO_x/SiN_x stack.

IV. Conclusion

In conclusion, we have shown that both n$^+$-type and p$^+$-type c-Si surfaces in a very wide sheet resistance range are well passivated by an industrially fired PECVD AlO_x/SiN_x dielectric stack. This is an important step forward in surface passivation with AlO_x/SiN_x dielectric stacks, as some high-efficiency c-Si solar cell designs (for example, all back-contact and bifacial Si solar cells) require passivation of both dopant polarities. Based on contactless *C–V* measurements and device simulations, we show that a negatively-charged AlO_x/SiN_x stack with lower charge density can provide excellent passivation on both n$^+$-type and p$^+$-type c-Si surfaces, provided the interface defect density remains low. In combination with the excellent results obtained on undiffused c-Si surfaces, our work demonstrates that all c-Si surfaces of relevance in today's PV industry can be well passivated by a firing stable, low-temperature deposited, and industrially feasible dielectric stack.

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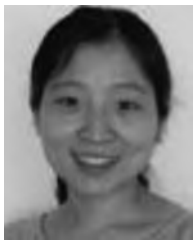

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Progress in Surface Passivation of Heavily Doped n-Type and p-Type Silicon by Plasma-Deposited AlO_x/SiN_x Dielectric Stacks

Shubham Duttagupta, Fa-Jun Ma, Serena Fen Lin, Thomas Mueller, Armin G. Aberle, and Bram Hoex

Abstract—**We report an outstanding level of surface passivation for both n^+ and p^+ silicon by AlO_x/SiN_x dielectric stacks deposited in an inline plasma-enhanced chemical vapor deposition (PECVD) reactor for a wide range of sheet resistances. Extremely low emitter saturation current densities (J_{0e}) of 12 and 200 fA/cm^2 are obtained on 165 and 25 Ω/sq n^+ emitters, respectively, and 8 and 45 fA/cm^2 on 170 and 30 Ω/sq p^+ emitters, respectively. Using contactless corona–voltage measurements and device simulations, we demonstrate that the surface passivation mechanism on both n^+ and p^+ silicon is primarily due to a relatively low interface defect density of $<10^{11}$ eV^{-1}cm^{-2} in combination with a moderate fixed negative charge density of (1–2) × 10^{12} cm^{-2}. From advanced modeling, the fundamental surface recombination velocity parameter is shown to be in the order of 10^4 cm/s for PECVD AlO_x/SiN_x passivated heavily doped n^+ and p^+ silicon surfaces.**

Index Terms—**Aluminum oxide/silicon nitride (AlO_x/SiN_x) stacks, boron-doped emitters, crystalline silicon, phosphorus-doped emitters, plasma-enhanced chemical vapor deposition (PECVD), surface passivation.**

I. Introduction

In recent years, amorphous aluminum oxide (AlO_x) has received tremendous interest from the photovoltaic community for its application as a surface passivation film for crystalline silicon wafer solar cells. AlO_x films provide excellent surface passivation on lightly doped n-type and p-type silicon as well as on heavy doped p^+ silicon [1]–[5]. In addition to a low interface defect density ($\sim 10^{11}$ eV^{-1}cm^{-2}), a distinguished property of AlO_x is the presence of a high negative charge density (10^{12}–10^{13} cm^{-2}, in units of elementary charges) in the film. This is especially beneficial on p-type c-Si surfaces as the minority carriers (electrons) are effectively shielded from the *c*-Si surface. Because of its excellent surface passivation properties on p-type surfaces, AlO_x has mainly been considered for the application in p-type passivated emitter and rear cell cells, p-type aluminum local back-surface field (Al-LBSF) cells, and n-type passivated emitter and rear locally diffused cells [6], [7].

Excellent passivation of heavily doped n^+ and p^+ silicon surfaces is very important for high-efficiency Si wafer solar cells. Some solar cell structures, such as interdigitated back-contact (IBC) solar cells, require simultaneous passivation of both dopant polarities [8], [9]. For this application, preferentially a suitable dielectric is needed that can passivate both n^+ and p^+ silicon surfaces simultaneously. Thick ($\sim$100 nm) thermal silicon oxide (SiO_2) films or stacks consisting of a thin (5–30 nm) SiO_2 film capped by a 50–100-nm-thick silicon nitride (SiN_x) film are often used due to their ability to passivate both n^+ and p^+ silicon surfaces [8]–[12]. However, low-temperature (<400 °C) surface passivation is typically preferred for the fabrication of industrial high-efficiency silicon wafer solar cells, due to its potential cost effectiveness, lower thermal budget, and the possibility for inline processing. Recently, Mihailetchi *et al.* reported excellent results for p^+ surfaces passivated by a stack consisting of an ultrathin oxide grown by hot HNO_3 and then capped with a SiN_x film [13]. Although no specific results are available in regards to its capability of passivating n^+ silicon surfaces, it can be considered a good method for passivating both n^+ and p^+ silicon surfaces simultaneously as these layers have already been used for large-area screen-printed IBC solar cells showing good efficiencies [14]–[17]. However, it should be noted that these devices showed moderate implied V_{oc} (iV_{oc}) in the range of 660–680 mV and also resulted in moderate solar cell open-circuit voltages of $V_{oc} < 650$ mV [14]–[17]. It is also suggested in these publications that an optimized dielectric is still needed that can passivate both n^+ and p^+ silicon surfaces simultaneously in order to achieve higher open-circuit voltage, and therefore, higher solar cell efficiency.

AlO_x films provide excellent surface passivation on p^+ silicon for an arbitrary sheet resistance [2], [18], [19]. Recently it has been shown that n^+-doped Si in a certain sheet resistance range can also be passivated by Al_2O_3 films grown by plasma-assisted and O_3-based atomic layer deposition (ALD), however, the results are not yet competitive [20], [21]. In addition, PA-ALD is not yet an industrially feasible technique. Thus, it is of great interest to investigate if negatively charged AlO_x films deposited by the industrial PECVD can provide excellent passivation on both n^+ and p^+ silicon surfaces.

In this study, we demonstrate that PECVD AlO_x/SiN_x dielectric stacks can provide excellent passivation on both heavily doped n^+ and p^+ silicon surfaces that are relevant for the industrial solar cell application. These results are primarily explained

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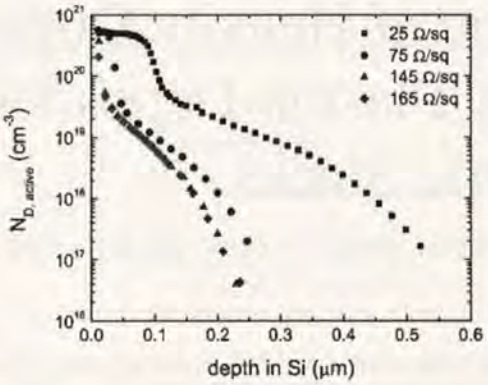

Fig. 1. Phosphorus dopant profile of n^+pn^+ samples measured by ECV profiling. The sheet resistance values determined by four-point probe measurements are shown in the graph.

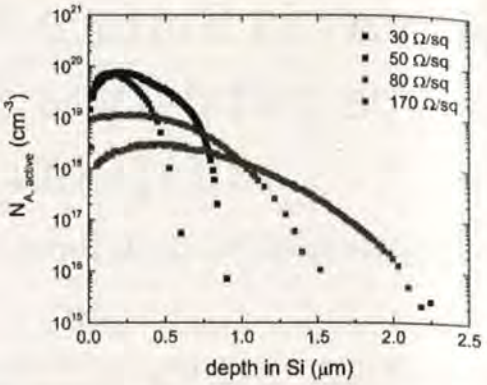

Fig. 2. Boron dopant profile of p^+np^+ samples measured by ECV profiling. The sheet resistance values determined by four-point probe measurements are shown in the graph.

by a low midgap interface defect density of $<10^{11}$ eV^{-1}cm^{-2}, which is beneficial for both n^+ and p^+ silicon surfaces. The stacks developed in this study feature a relatively moderate fixed negative charge density of (1–2) $\times 10^{12}$ cm^{-2}, as determined by contactless corona–voltage (C–V) experiments. Based on device simulations, we show that moderate fixed charge densities in the range of -10^{12} cm^{-2}–10^{12} cm^{-2} do not significantly affect the emitter saturation current density of typical industrial n^+ diffusions. Thus, the passivation is mainly ruled by the excellent electronic quality of the interface or low interface defect density.

II. Experimental Details

Symmetrical n^+pn^+ carrier lifetime structures were fabricated using an industrial $POCl_3$ diffusion process. The sheet resistance of the n^+ emitter was varied by changing the temperature and time of the $POCl_3$ diffusion. The phosphorus dopant profiles of the n^+pn^+ samples used in this study were measured with the electrochemical voltage (ECV) method, as shown in Fig. 1. The p-type Si wafers were monocrystalline (Cz method, boron-doped, 5–8 Ωcm), about 150 μm thick, pseudosquare (125 mm × 125 mm), and with a (100) surface orientation.

The p^+np^+ structures were fabricated by an industrial BBr_3 diffusion process. The p^+ emitter sheet resistance was varied by varying the process conditions during the BBr_3 diffusion and by a postdiffusion oxidation, as explained in detail elsewhere [18]. The boron dopant profiles of the p^+np^+ samples used in this study were measured by the ECV method, as shown in Fig. 2. The n-type Si wafers were monocrystalline (Cz, phosphorus-doped, 6–8 Ωcm), about 150 μm thick, pseudosquare (125 mm × 125 mm), and with a (100) surface orientation. After the diffusion process, the phosphorus or borosilicate glass layers were removed by dipping in HF solution, followed by rinsing in deionised water.

Prior to the deposition of the PECVD dielectric films, the samples were cleaned using the Radio Corporation of America (RCA) clean with a final HF dip followed by water rinsing and drying to ensure an H-terminated surface. The sheet resistance of the p^+ and n^+ diffusions was unaffected by the predeposition cleaning as confirmed by four-point probe measurements. The n^+pn^+ and p^+np^+ samples with various sheet resistances were coated on both sides with 30-nm AlO_x capped with 70-nm SiN_x, using an industrial inline microwave-powered remote PECVD reactor (SiNA-XS, Roth & Rau, Germany). We emphasize that all samples (n^+pn^+ and p^+np^+) were processed without any change in the PECVD process conditions. The deposition conditions are summarized in Table I.

After the PECVD processes, the samples received an activation anneal in an industrial fast firing furnace (Ultraflex, Despatch, USA) for a few seconds at a set peak temperature of >800 °C, similar to the cofiring step applied to the screen-printed metallization of industrial silicon wafer solar cells. The effective minority carrier lifetime (τ_{eff}) of the lifetime samples was measured using a contactless flash-based photoconductance decay tester (WCT-120, Sinton Instruments), in both the quasi-steady-state and the transient mode [22]. From the τ_{eff} measurement, the emitter saturation current density (J_{0e}) per side of the n^+pn^+ and p^+np^+ samples was extracted from the slope of the Auger-corrected inverse lifetime versus injection level curve under high-injection conditions ($\Delta n \sim 10^{15}$ to 10^{16} cm^{-3} in our case), using the relation proposed by Kane and Swanson [23];

$$\frac{1}{\tau_{\text{eff}}} - \frac{1}{\tau_{\text{Auger}}} = \frac{1}{\tau_{\text{SRH}}} + 2\frac{J_{0e}\,(N_d + \Delta n)}{q n_i^2 W} \qquad (1)$$

where τ_{Auger} and τ_{SRH} are the Auger lifetime and the Shockley–Read–Hall lifetime in the bulk of the sample [24], respectively, N_d and Δn are the doping concentration and the excess carrier concentration (or "injection level") in the bulk of the sample, q is the elementary charge, n_i is the intrinsic carrier concentration (8.6×10^9 cm^{-3} at 298 K) [25], and W is the thickness of the sample. In addition, contactless C–V measurements (PV-2000, Semilab SDI Inc., USA) were carried out to extract the fixed charge density (Q_f) and the interface defect density (D_{it}) of the dielectric films on undiffused Si samples. The details of the measurement system and extraction procedure of Q_f and D_{it} are explained elsewhere [26]–[29].

III. Results and Discussion

Fig. 3 shows the measured injection level dependence of the Auger-corrected inverse effective carrier lifetime of industrially fired n^+pn^+ samples passivated on both sides by a PECVD AlO_x/SiN_x dielectric stack. The results cover a wide range of industry relevant sheet resistances (25–165 Ω/sq).

TABLE I
EXPERIMENTAL DETAILS USED FOR THE DEPOSITION OF THE DIELECTRIC FILMS IN THIS STUDY

Dielectric	Process gas	Deposition temperature (°C)	Reactor pressure (mbar)	Plasma power (W)
AlO_x	$Al(CH_3)_3 + N_2O + Ar$	450	0.10	1500
SiN_x	$SiH_4 + NH_3$	200	0.20	3000

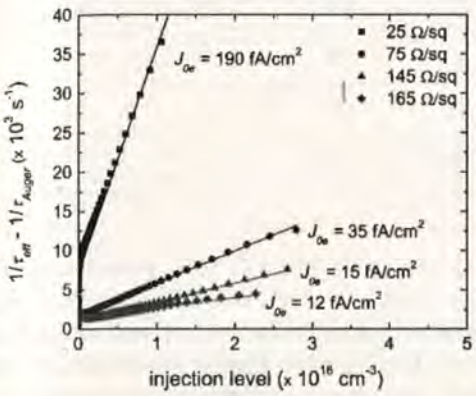

Fig. 3. Measured injection level dependence of the Auger-corrected inverse effective lifetime of industrially fired n^+pn^+ samples symmetrically passivated by PECVD AlO_x/SiN_x dielectric stacks (symbols). The sheet resistance of the n^+ emitters determined by four point probe measurements is shown in the legend. The J_{0e} values obtained from the straight-line fits (solid lines) are also shown.

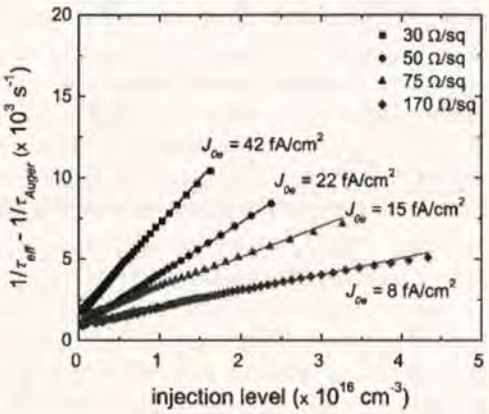

Fig. 4. Measured injection level dependence of the Auger-corrected inverse effective lifetime of industrially fired p^+np^+ samples symmetrically passivated by PECVD AlO_x/SiN_x dielectric stacks (symbols). The sheet resistance of the p^+ emitters determined by four point probe measurements is shown in the legend. The J_{0e} values obtained from the straight-line fits (solid lines) are also shown.

It is emphasized that we observe a linear relationship for all lifetime samples, allowing the extraction of J_{0e} values using (1). This was not always the case in the work of Hoex *et al.*, where it was mentioned that the relationship was not linear for 100–200 Ω/sq n^+ emitters passivated by PA-ALD Al_2O_3 [20]. This was attributed to the very high negative fixed charge density (up to 10^{13} cm^{-2}) of PA-ALD Al_2O_3 films, which strongly increased the minority carrier (hole) density at the n^+ surface in their work, and thereby, caused an injection level dependent J_{0e}. In this study, we show an excellent level of surface passivation with extremely low J_{0e} values of 12 fA/cm² for 165 Ω/sq planar n^+ emitters passivated by PECVD AlO_x/SiN_x dielectric stacks after an industrial firing process. As a matter of fact, the J_{0e} values obtained in this study are similar to, or even better than, the best values reported in the literature for n^+ emitters passivated by PECVD SiN_x [30]. These results are also significantly better than those obtained for n^+ emitters passivated by Al_2O_3 grown by ALD techniques reported so far [20], [21].

Identical PECVD stacks were also used to passivate p^+ emitters. Fig. 4 shows the measured injection level dependence of the Auger-corrected inverse effective carrier lifetimes of industrially fired p^+np^+ samples passivated on both sides with an AlO_x/SiN_x dielectric stack. The lifetime samples show a clear linear relationship, indicating again that (1) can be used to extract the J_{0e} value of this emitter. An extremely low J_{0e} value of 8 fA/cm² was obtained for a 170-Ω/sq emitter, which is comparable with the values obtained for p^+ emitters passivated by Al_2O_3 films grown by the PA-ALD [2]. It should be noted that in our earlier work, p^+np^+ samples were passivated on both sides with an AlO_x/SiN_x dielectric stack deposited under slightly different processing conditions [18]. In this study, both n^+pn^+ and p^+np^+ samples were processed simultaneously with 100 °C higher deposition temperature for AlO_x and ~100 °C lower deposition temperature for capping SiN_x layer. This resulted in better interface quality and more importantly, a reduced fixed charge density. These stacks also provide excellent results on p^+ Si surfaces for a wide range of sheet resistance with similar J_{0e} values as reported earlier [18].

Table II summarizes the experimentally measured effective lifetime (τ_{eff} at $\Delta n = 10^{15}$ cm^{-3}), emitter saturation current density (J_{0e}), and implied V_{oc} (iV_{oc}) for n^+pn^+ and p^+np^+ samples symmetrically passivated by an industrially fired AlO_x/SiN_x dielectric stack. Note that effective lifetime and implied V_{oc} also depends on factors such as bulk doping level and bulk effective minority carrier lifetime of the used silicon wafer and the optical properties of the passivation coating, hence, care must be taken when comparing experimental values between different experiments. $V_{oc,limit}$ represents the one-Sun open-circuit voltage limit of a solar cell at 25 °C calculated from the experimentally measured J_{0e} and assuming a short-circuit current density (J_{sc}) of 40 mA/cm² with an ideal diode law ($n = 1$) by [22], [31]:

$$V_{oc,limit} = n\frac{kT}{q}\ln\left(\frac{J_{sc}}{J_{0e}} + 1\right) \quad (2)$$

where n is the diode ideality factor, which is considered one in this calculation. kT/q is 25.9 mV at 25 °C with k, T, q being the Boltzmann constant, absolute temperature in Kelvin and the elementary charge, respectively.

Fig. 5 shows the experimentally obtained J_{0e} values for n^+ and p^+ emitters passivated by industrially fired PECVD

TABLE II
EXPERIMENTALLY DETERMINED EFFECTIVE LIFETIME (τ_{eff}) AT $\Delta n = 10^{15}$ cm^{-3}, SATURATION CURRENT DENSITY (J_{0e}) PER SIDE AND IMPLIED V_{oc} (iV_{oc}) FOR n^+pn^+ AND p^+np^+ SAMPLES SYMMETRICALLY PASSIVATED BY AN AlO_x/SiN_x STACK

	Sheet resistance for phosphorus-diffused n^+ surface on p-type Si (Ω/sq.)				Sheet resistance for boron-diffused p^+ surface on n-type Si (Ω/sq.)			
	25	**75**	**145**	**165**	**30**	**50**	**80**	**170**
τ_{eff} (µs)	94	465	770	700	484	841	700	930
J_{0e} (fA/cm^2)	190	35	15	12	45	22	15	8
iV_{oc} (mV)	640	688	706	703	670	690	700	712
$V_{oc,limit}$ (mV)	670	713	735	741	707	725	735	751

The $V_{oc,limit}$ was calculated by (2) using the measured J_{0e} values.

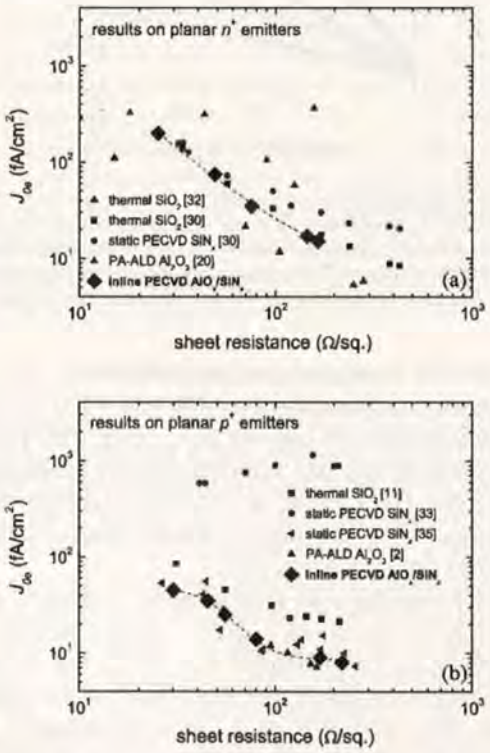

Fig. 5. Experimentally obtained J_{0e} values (diamonds in this work) for (a) n^+ emitters and (b) p^+ emitters passivated by industrially fired PECVD AlO_x/SiN_x stacks (the dotted lines are guides to the eye). Each of our J_{0e} values is the average result of a batch of 10 samples. Also shown, for comparison, are state-of-the-art J_{0e} values reported in the literature for planar n^+ and p^+ emitters passivated by thermal SiO_2, PECVD SiN_x, and ALD-grown Al_2O_3.

AlO_x/SiN_x stacks. For comparison, the best published results from the literature are included as well. It should be noted that the preparation of the n^+ and p^+ emitters in the various studies were different and most likely resulted in different dopant profiles for a comparable sheet resistance. This potentially affects the Auger recombination losses in these emitters. However, the general trend can be used for comparison. It is evident from Fig. 5 that thermal SiO_2 is a good candidate for both dopant polarities, showing excellent surface passivation of n^+ emitters and a decent surface passivation for p^+ emitters after either *alneal* (aluminum-annealing) or forming gas anneal (FGA) [11], [30], [32]. PECVD SiN_x provides excellent passivation of n^+ emitters after FGA [30]. Generally, these SiN_x films provide a compromised level of surface passivation on p^+ emitters [11], [33]. Only limited reports are available were PECVD SiN_x provides a good level of surface passivation on p^+ emitters, however, the underlying mechanism is not yet properly understood [34], [35]. Similarly PA-ALD Al_2O_3 films provide only a moderate passivation on n^+ emitters [see Fig. 5(a)], however, p^+ surfaces with an arbitrary sheet resistance can be well passivated with PA-ALD Al_2O_3 films [2], [20]. Based on the experimental results presented in this study, it is clear that our industrially fired PECVD AlO_x/SiN_x stacks provide an excellent level of surface passivation on both n^+ and p^+ emitters, for the entire investigated sheet resistance range. Hence, our work demonstrates that these PECVD AlO_x/SiN_x stacks can be used to simultaneously passivate all c-Si surfaces that are of relevance in today's PV industry.

To obtain more insight into the interface properties such as fixed charge density (Q_f) and interface defect density (D_{it}) of our industrially fired AlO_x/SiN_x stacks, contactless C–V measurements were performed on undiffused Si samples. These measurements revealed that the industrially fired AlO_x/SiN_x dielectric stacks on c-Si used in this study have a comparatively low midgap interface defect density of $<10^{11}$ eV^{-1}cm^{-2} in combination with a moderate negative fixed charge density in the range of (1–2) $\times$ 10^{12} cm^{-2}. Note that the fixed charge density in the dielectric stack is highly dependent on the deposition conditions and the postdeposition treatments used, as will be reported in detail in a separate study.

Understanding the surface passivation of p^+ Si surfaces by negatively charged dielectrics is relatively straightforward. A low interface defect density provides excellent chemical passivation. In addition, the negative fixed charge density reduces the minority carrier concentration at p^+ Si surfaces (for the B surface concentrations investigated in this study) providing field-effect passivation. Understanding the passivation of n^+ Si surfaces by negatively charged dielectrics is, however, not straightforward. For this purpose, we used advanced computer modeling (TCAD, Sentaurus) to study the role of field-effect passivation for heavily doped n^+ surfaces. In these simulations, we take both the fundamental hole surface recombination

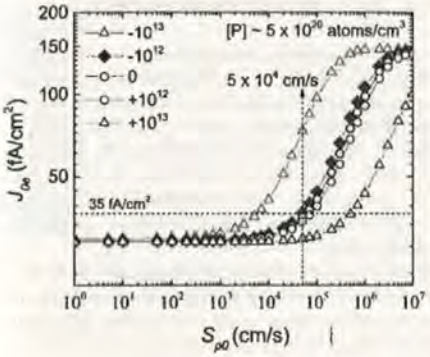

Fig. 6. Simulated J_{0e} as a function of the S_{p0} at the c-Si/dielectric interface for high (10^{13} cm^{-2}) and moderate (10^{12} cm^{-2}) fixed charge densities of both polarities in the dielectric film. A symmetrical n^+pn^+ sample was used with a 75-Ω/sq diffusion per side (the experimental measured diffusion profile from Fig. 1 was used in the simulation).

velocity parameter (S_{p0}) and the interface fixed charge (Q_f) into account, similar to the approach presented by Girish *et al.* [36] and Aberle *et al.* [37], and furthermore, using the physical models from [38] and [39], S_{p0} is the surface recombination velocity parameter for holes assuming flat band conditions and can be expressed by

$$S_{p0} \equiv \nu_{\rm th}\sigma_p N_{\rm st} \tag{3}$$

where $v_{\rm th}$ is the thermal velocity, σ_p is the capture cross-section for holes, and $N_{\rm st}$ is the number of surface states per unit area [40]. Using the measured n^+ dopant profile of the 75 Ω/sq diffusion from Fig. 1, J_{0e} versus S_{n0} curves for various fixed charge densities were determined. The results are shown in Fig. 6. From Fig. 6, it is clear that positive fixed charge densities are beneficial for the passivation of the 75-Ω/sq n^+ Si diffusion, resulting in significantly lower J_{0e} values for similar S_{p0} values. On the other side, a very high negative fixed charge density of 10^{13} cm^{-2} is found to be detrimental and results in higher J_{oe} values, in good agreement with the experimental results reported by Hoex *et al.* for n^+ Si passivated by Al_2O_3 films grown by the PA-ALD [20].

For moderate fixed interface charge densities in the range of -10^{12} cm^{-2} to $+10^{12}$ cm^{-2}, it can be seen that the fixed charge is hardly affecting the J_{0e} over the whole investigated S_{p0} range, and hence, the passivation is predominantly ruled by chemical passivation in this case. It should be noted that a similar trend (effect of fixed charge) was observed on other n^+ diffusions used in this study; however, the fixed charge range will depend on the surface dopant concentration. The results in Fig. 6 also allow us to extract the S_{p0} value at the interface between the c-Si wafer and the AlO_x/SiN_x stack. Taking the measured J_{0e} value of 35 fA/cm^2 and the measured Q_f of -10^{12} cm^{-2}, we can see that this results in a S_{p0} value of $\sim 5 \times 10^4$ cm/s. This value is in the similar order to the S_{n0} (electron surface recombination velocity parameter) value obtained by our PECVD AlO_x/SiN_x stack on heavily doped p^+ Si surfaces, which is in the range of 10^4 cm/s [41]. We observe that the S_{p0} value obtained in this study is slightly better than the S_{p0} reported by Altermatt *et al.* ($> 10^5$ cm/s) for n^+ Si having a surface dopant density of $\sim 2 \times 10^{20}$ atoms/cm^3 passivated by FGA thermal SiO_2 [39]. Hence, these results indicate that heavily doped n^+ Si surfaces can be passivated as effectively as heavily doped p^+ Si surfaces using a negatively charged PECVD AlO_x/SiN_x stack.

IV. Conclusion

In conclusion, we have shown that both n^+-type and p^+-type c-Si surfaces in a very wide sheet resistance range are well passivated by an industrially fired PECVD AlO_x/SiN_x dielectric stack. This is an important step forward in surface passivation with AlO_x/SiN_x dielectric stacks, as some high-efficiency c-Si solar cell designs (for example, all back-contact and bifacial Si solar cells) require passivation of both dopant polarities. Based on contactless *C–V* measurements and device simulations, we show that a negatively-charged AlO_x/SiN_x stack with lower charge density can provide excellent passivation on both n^+-type and p^+-type c-Si surfaces, provided the interface defect density remains low. In combination with the excellent results obtained on undiffused c-Si surfaces, our work demonstrates that all c-Si surfaces of relevance in today's PV industry can be well passivated by a firing stable, low-temperature deposited, and industrially feasible dielectric stack.

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Attachment K-3

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Progress in Surface Passivation of Heavily Doped n-Type and p-Type Silicon by Plasma-Deposited AlO_x/SiN_x Dielectric Stacks

Shubham Duttagupta, Fa-Jun Ma, Serena Fen Lin, Thomas Mueller, Armin G. Aberle, and Bram Hoex

***Abstract*—We report an outstanding level of surface passivation for both n^+ and p^+ silicon by AlO_x/SiN_x dielectric stacks deposited in an inline plasma-enhanced chemical vapor deposition (PECVD) reactor for a wide range of sheet resistances. Extremely low emitter saturation current densities (J_{0e}) of 12 and 200 fA/cm^2 are obtained on 165 and 25 Ω/sq n^+ emitters, respectively, and 8 and 45 fA/cm^2 on 170 and 30 Ω/sq p^+ emitters, respectively. Using contactless corona–voltage measurements and device simulations, we demonstrate that the surface passivation mechanism on both n^+ and p^+ silicon is primarily due to a relatively low interface defect density of $<10^{11}$ eV^{-1}cm^{-2} in combination with a moderate fixed negative charge density of (1–2) × 10^{12} cm^{-2}. From advanced modeling, the fundamental surface recombination velocity parameter is shown to be in the order of 10^4 cm/s for PECVD AlO_x/SiN_x passivated heavily doped n^+ and p^+ silicon surfaces.**

***Index Terms*—Aluminum oxide/silicon nitride (AlO_x/SiN_x) stacks, boron-doped emitters, crystalline silicon, phosphorus-doped emitters, plasma-enhanced chemical vapor deposition (PECVD), surface passivation.**

I. Introduction

In recent years, amorphous aluminum oxide (AlO_x) has received tremendous interest from the photovoltaic community for its application as a surface passivation film for crystalline silicon wafer solar cells. AlO_x films provide excellent surface passivation on lightly doped n-type and p-type silicon as well as on heavy doped p^+ silicon [1]–[5]. In addition to a low interface defect density (~10^{11} eV^{-1}cm^{-2}), a distinguished property of AlO_x is the presence of a high negative charge density (10^{12}–10^{13} cm^{-2}, in units of elementary charges) in the film. This is especially beneficial on p-type c-Si surfaces as the minority carriers (electrons) are effectively shielded from the *c*-Si surface. Because of its excellent surface passivation properties on p-type surfaces, AlO_x has mainly been considered for the application in p-type passivated emitter and rear cell cells, p-type aluminum local back-surface field (Al-LBSF) cells, and n-type passivated emitter and rear locally diffused cells [6], [7].

Excellent passivation of heavily doped n^+ and p^+ silicon surfaces is very important for high-efficiency Si wafer solar cells. Some solar cell structures, such as interdigitated back-contact (IBC) solar cells, require simultaneous passivation of both dopant polarities [8], [9]. For this application, preferentially a suitable dielectric is needed that can passivate both n^+ and p^+ silicon surfaces simultaneously. Thick (~100 nm) thermal silicon oxide (SiO_2) films or stacks consisting of a thin (5–30 nm) SiO_2 film capped by a 50–100-nm-thick silicon nitride (SiN_x) film are often used due to their ability to passivate both n^+ and p^+ silicon surfaces [8]–[12]. However, low-temperature (<400 °C) surface passivation is typically preferred for the fabrication of industrial high-efficiency silicon wafer solar cells, due to its potential cost effectiveness, lower thermal budget, and the possibility for inline processing. Recently, Mihailetchi *et al.* reported excellent results for p^+ surfaces passivated by a stack consisting of an ultrathin oxide grown by hot HNO_3 and then capped with a SiN_x film [13]. Although no specific results are available in regards to its capability of passivating n^+ silicon surfaces, it can be considered a good method for passivating both n^+ and p^+ silicon surfaces simultaneously as these layers have already been used for large-area screen-printed IBC solar cells showing good efficiencies [14]–[17]. However, it should be noted that these devices showed moderate implied V_{oc} (iV_{oc}) in the range of 660–680 mV and also resulted in moderate solar cell open-circuit voltages of $V_{oc} < 650$ mV [14]–[17]. It is also suggested in these publications that an optimized dielectric is still needed that can passivate both n^+ and p^+ silicon surfaces simultaneously in order to achieve higher open-circuit voltage, and therefore, higher solar cell efficiency.

AlO_x films provide excellent surface passivation on p^+ silicon for an arbitrary sheet resistance [2], [18], [19]. Recently it has been shown that n^+-doped Si in a certain sheet resistance range can also be passivated by Al_2O_3 films grown by plasma-assisted and O_3-based atomic layer deposition (ALD), however, the results are not yet competitive [20], [21]. In addition, PA-ALD is not yet an industrially feasible technique. Thus, it is of great interest to investigate if negatively charged AlO_x films deposited by the industrial PECVD can provide excellent passivation on both n^+ and p^+ silicon surfaces.

In this study, we demonstrate that PECVD AlO_x/SiN_x dielectric stacks can provide excellent passivation on both heavily doped n^+ and p^+ silicon surfaces that are relevant for the industrial solar cell application. These results are primarily explained

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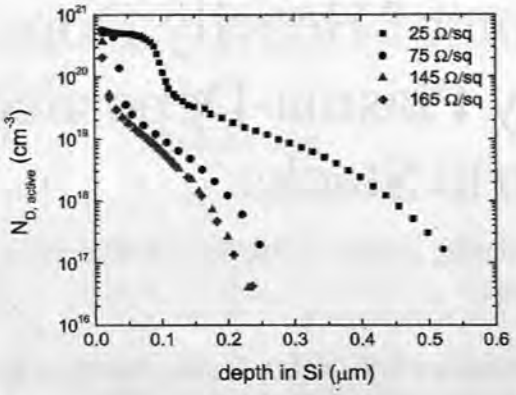

Fig. 1. Phosphorus dopant profile of n^+pn^+ samples measured by ECV profiling. The sheet resistance values determined by four-point probe measurements are shown in the graph.

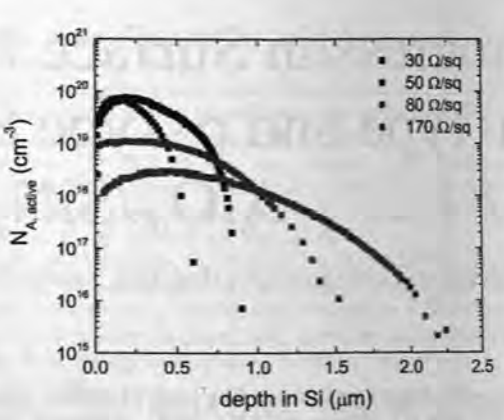

Fig. 2. Boron dopant profile of p^+np^+ samples measured by ECV profiling. The sheet resistance values determined by four-point probe measurements are shown in the graph.

by a low midgap interface defect density of $<10^{11}$ eV^{-1}cm^{-2}, which is beneficial for both n^+ and p^+ silicon surfaces. The stacks developed in this study feature a relatively moderate fixed negative charge density of (1–2) $\times$ 10^{12} cm^{-2}, as determined by contactless corona–voltage (*C–V*) experiments. Based on device simulations, we show that moderate fixed charge densities in the range of -10^{12} cm^{-2}–10^{12} cm^{-2} do not significantly affect the emitter saturation current density of typical industrial n^+ diffusions. Thus, the passivation is mainly ruled by the excellent electronic quality of the interface or low interface defect density.

II. Experimental Details

Symmetrical n^+pn^+ carrier lifetime structures were fabricated using an industrial $POCl_3$ diffusion process. The sheet resistance of the n^+ emitter was varied by changing the temperature and time of the $POCl_3$ diffusion. The phosphorus dopant profiles of the n^+pn^+ samples used in this study were measured with the electrochemical voltage (ECV) method, as shown in Fig. 1. The p-type Si wafers were monocrystalline (Cz method, boron-doped, 5–8 Ωcm), about 150 μm thick, pseudosquare (125 mm × 125 mm), and with a (100) surface orientation.

The p^+np^+ structures were fabricated by an industrial BBr_3 diffusion process. The p^+ emitter sheet resistance was varied by varying the process conditions during the BBr_3 diffusion and by a postdiffusion oxidation, as explained in detail elsewhere [18]. The boron dopant profiles of the p^+np^+ samples used in this study were measured by the ECV method, as shown in Fig. 2. The n-type Si wafers were monocrystalline (Cz, phosphorus-doped, 6–8 Ωcm), about 150 μm thick, pseudosquare (125 mm × 125 mm), and with a (100) surface orientation. After the diffusion process, the phosphorus or borosilicate glass layers were removed by dipping in HF solution, followed by rinsing in deionised water.

Prior to the deposition of the PECVD dielectric films, the samples were cleaned using the Radio Corporation of America (RCA) clean with a final HF dip followed by water rinsing and drying to ensure an H-terminated surface. The sheet resistance of the p^+ and n^+ diffusions was unaffected by the predeposition cleaning as confirmed by four-point probe measurements. The n^+pn^+ and p^+np^+ samples with various sheet resistances were coated on both sides with 30-nm AlO_x capped with 70-nm SiN_x, using an industrial inline microwave-powered remote PECVD reactor (SiNA-XS, Roth & Rau, Germany). We emphasize that all samples (n^+pn^+ and p^+np^+) were processed without any change in the PECVD process conditions. The deposition conditions are summarized in Table I.

After the PECVD processes, the samples received an activation anneal in an industrial fast firing furnace (Ultraflex, Despatch, USA) for a few seconds at a set peak temperature of >800 °C, similar to the cofiring step applied to the screen-printed metallization of industrial silicon wafer solar cells. The effective minority carrier lifetime (τ_{eff}) of the lifetime samples was measured using a contactless flash-based photoconductance decay tester (WCT-120, Sinton Instruments), in both the quasi-steady-state and the transient mode [22]. From the τ_{eff} measurement, the emitter saturation current density (J_{0e}) per side of the n^+pn^+ and p^+np^+ samples was extracted from the slope of the Auger-corrected inverse lifetime versus injection level curve under high-injection conditions ($\Delta n \sim 10^{15}$ to 10^{16} cm^{-3} in our case), using the relation proposed by Kane and Swanson [23];

$$\frac{1}{\tau_{\text{eff}}} - \frac{1}{\tau_{\text{Auger}}} = \frac{1}{\tau_{\text{SRH}}} + 2\frac{J_{0e}\,(N_d + \Delta n)}{q n_i^2 W} \qquad (1)$$

where τ_{Auger} and τ_{SRH} are the Auger lifetime and the Shockley–Read–Hall lifetime in the bulk of the sample [24], respectively, N_d and Δn are the doping concentration and the excess carrier concentration (or "injection level") in the bulk of the sample, q is the elementary charge, n_i is the intrinsic carrier concentration (8.6×10^9 cm^{-3} at 298 K) [25], and W is the thickness of the sample. In addition, contactless *C–V* measurements (PV-2000, Semilab SDI Inc., USA) were carried out to extract the fixed charge density (Q_f) and the interface defect density (D_{it}) of the dielectric films on undiffused Si samples. The details of the measurement system and extraction procedure of Q_f and D_{it} are explained elsewhere [26]–[29].

III. Results and Discussion

Fig. 3 shows the measured injection level dependence of the Auger-corrected inverse effective carrier lifetime of industrially fired n^+pn^+ samples passivated on both sides by a PECVD AlO_x/SiN_x dielectric stack. The results cover a wide range of industry relevant sheet resistances (25–165 Ω/sq).

TABLE I
EXPERIMENTAL DETAILS USED FOR THE DEPOSITION OF THE DIELECTRIC FILMS IN THIS STUDY

Dielectric	Process gas	Deposition temperature (°C)	Reactor pressure (mbar)	Plasma power (W)
AlO_x	$Al(CH_3)_3 + N_2O + Ar$	450	0.10	1500
SiN_x	$SiH_4 + NH_3$	200	0.20	3000

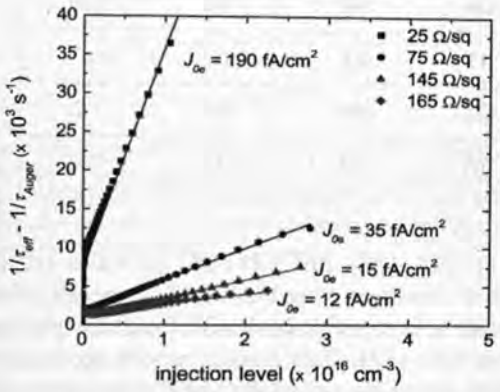

Fig. 3. Measured injection level dependence of the Auger-corrected inverse effective lifetime of industrially fired n^+pn^+ samples symmetrically passivated by PECVD AlO_x/SiN_x dielectric stacks (symbols). The sheet resistance of the n^+ emitters determined by four point probe measurements is shown in the legend. The J_{0e} values obtained from the straight-line fits (solid lines) are also shown.

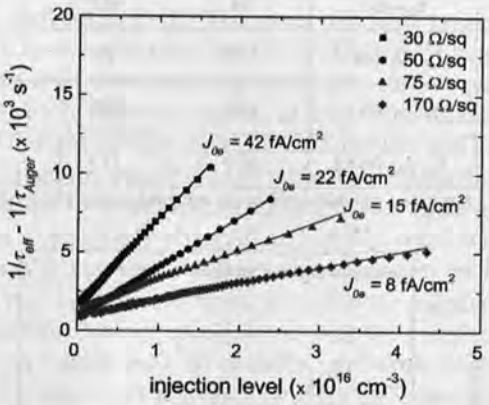

Fig. 4. Measured injection level dependence of the Auger-corrected inverse effective lifetime of industrially fired p^+np^+ samples symmetrically passivated by PECVD AlO_x/SiN_x dielectric stacks (symbols). The sheet resistance of the p^+ emitters determined by four point probe measurements is shown in the legend. The J_{0e} values obtained from the straight-line fits (solid lines) are also shown.

It is emphasized that we observe a linear relationship for all lifetime samples, allowing the extraction of J_{0e} values using (1). This was not always the case in the work of Hoex *et al.*, where it was mentioned that the relationship was not linear for 100–200 Ω/sq n^+ emitters passivated by PA-ALD Al_2O_3 [20]. This was attributed to the very high negative fixed charge density (up to 10^{13} cm^{-2}) of PA-ALD Al_2O_3 films, which strongly increased the minority carrier (hole) density at the n^+ surface in their work, and thereby, caused an injection level dependent J_{0e}. In this study, we show an excellent level of surface passivation with extremely low J_{0e} values of 12 fA/cm^2 for 165 Ω/sq planar n^+ emitters passivated by PECVD AlO_x/SiN_x dielectric stacks after an industrial firing process. As a matter of fact, the J_{0e} values obtained in this study are similar to, or even better than, the best values reported in the literature for n^+ emitters passivated by PECVD SiN_x [30]. These results are also significantly better than those obtained for n^+ emitters passivated by Al_2O_3 grown by ALD techniques reported so far [20], [21].

Identical PECVD stacks were also used to passivate p^+ emitters. Fig. 4 shows the measured injection level dependence of the Auger-corrected inverse effective carrier lifetimes of industrially fired p^+np^+ samples passivated on both sides with an AlO_x/SiN_x dielectric stack. The lifetime samples show a clear linear relationship, indicating again that (1) can be used to extract the J_{0e} value of this emitter. An extremely low J_{0e} value of 8 fA/cm^2 was obtained for a 170-Ω/sq emitter, which is comparable with the values obtained for p^+ emitters passivated by Al_2O_3 films grown by the PA-ALD [2]. It should be noted that in our earlier work, p^+np^+ samples were passivated on both sides with an AlO_x/SiN_x dielectric stack deposited under slightly different processing conditions [18]. In this study, both n^+pn^+ and p^+np^+ samples were processed simultaneously with 100 °C higher deposition temperature for AlO_x and ~100 °C lower deposition temperature for capping SiN_x layer. This resulted in better interface quality and more importantly, a reduced fixed charge density. These stacks also provide excellent results on p^+ Si surfaces for a wide range of sheet resistance with similar J_{0e} values as reported earlier [18].

Table II summarizes the experimentally measured effective lifetime (τ_{eff} at $\Delta n = 10^{15}$ cm^{-3}), emitter saturation current density (J_{0e}), and implied V_{oc} (iV_{oc}) for n^+pn^+ and p^+np^+ samples symmetrically passivated by an industrially fired AlO_x/SiN_x dielectric stack. Note that effective lifetime and implied V_{oc} also depends on factors such as bulk doping level and bulk effective minority carrier lifetime of the used silicon wafer and the optical properties of the passivation coating, hence, care must be taken when comparing experimental values between different experiments. $V_{\text{oc,limit}}$ represents the one-Sun open-circuit voltage limit of a solar cell at 25 °C calculated from the experimentally measured J_{0e} and assuming a short-circuit current density (J_{sc}) of 40 mA/cm^2 with an ideal diode law ($n = 1$) by [22], [31]:

$$V_{\text{oc,limit}} = n\frac{kT}{q}\ln\left(\frac{J_{\text{sc}}}{J_{0e}} + 1\right) \tag{2}$$

where n is the diode ideality factor, which is considered one in this calculation. kT/q is 25.9 mV at 25 °C with k, T, q being the Boltzmann constant, absolute temperature in Kelvin and the elementary charge, respectively.

Fig. 5 shows the experimentally obtained J_{0e} values for n^+ and p^+ emitters passivated by industrially fired PECVD

TABLE II
EXPERIMENTALLY DETERMINED EFFECTIVE LIFETIME (τ_{eff}) AT $\Delta n = 10^{15}$ cm^{-3}, SATURATION CURRENT DENSITY (J_{0e}) PER SIDE AND IMPLIED V_{oc} (iV_{oc}) FOR n^+pn^+ AND p^+np^+ SAMPLES SYMMETRICALLY PASSIVATED BY AN AlO_x/SiN_x STACK

	Sheet resistance for phosphorus-diffused n^+ surface on p-type Si (Ω/sq.)				Sheet resistance for boron-diffused p^+ surface on n-type Si (Ω/sq.)			
	25	**75**	**145**	**165**	**30**	**50**	**80**	**170**
τ_{eff} (μs)	94	465	770	700	484	841	700	930
J_{0e} (fA/cm^2)	190	35	15	12	45	22	15	8
iV_{oc} (mV)	640	688	706	703	670	690	700	712
$V_{oc,\,limit}$ (mV)	670	713	735	741	707	725	735	751

The $V_{oc,limit}$ was calculated by (2) using the measured J_{0e} values.

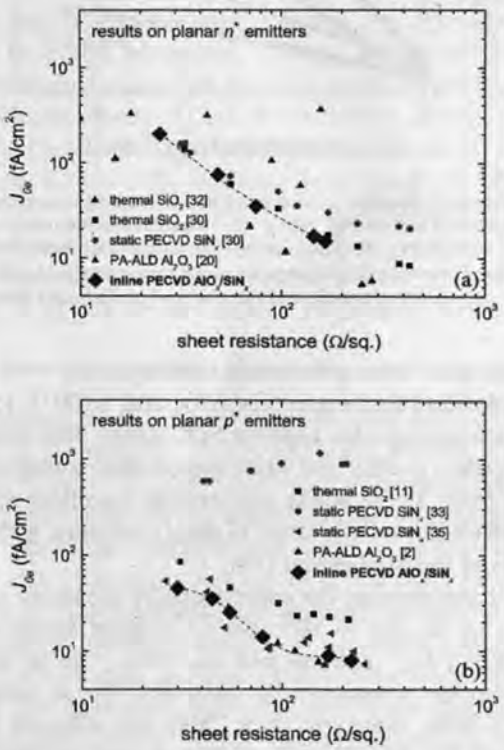

Fig. 5. Experimentally obtained J_{0e} values (diamonds in this work) for (a) n^+ emitters and (b) p^+ emitters passivated by industrially fired PECVD AlO_x/SiN_x stacks (the dotted lines are guides to the eye). Each of our J_{0e} values is the average result of a batch of 10 samples. Also shown, for comparison, are state-of-the-art J_{0e} values reported in the literature for planar n^+ and p^+ emitters passivated by thermal SiO_2, PECVD SiN_x, and ALD-grown Al_2O_3.

AlO_x/SiN_x stacks. For comparison, the best published results from the literature are included as well. It should be noted that the preparation of the n^+ and p^+ emitters in the various studies were different and most likely resulted in different dopant profiles for a comparable sheet resistance. This potentially affects the Auger recombination losses in these emitters. However, the general trend can be used for comparison. It is evident from Fig. 5 that thermal SiO_2 is a good candidate for both dopant polarities, showing excellent surface passivation of n^+ emitters and a decent surface passivation for p^+ emitters after either *alneal* (aluminum-annealing) or forming gas anneal (FGA) [11], [30], [32]. PECVD SiN_x provides excellent passivation of n^+ emitters after FGA [30]. Generally, these SiN_x films provide a compromised level of surface passivation on p^+ emitters [11], [33]. Only limited reports are available were PECVD SiN_x provides a good level of surface passivation on p^+ emitters, however, the underlying mechanism is not yet properly understood [34], [35]. Similarly PA-ALD Al_2O_3 films provide only a moderate passivation on n^+ emitters [see Fig. 5(a)], however, p^+ surfaces with an arbitrary sheet resistance can be well passivated with PA-ALD Al_2O_3 films [2], [20]. Based on the experimental results presented in this study, it is clear that our industrially fired PECVD AlO_x/SiN_x stacks provide an excellent level of surface passivation on both n^+ and p^+ emitters, for the entire investigated sheet resistance range. Hence, our work demonstrates that these PECVD AlO_x/SiN_x stacks can be used to simultaneously passivate all c-Si surfaces that are of relevance in today's PV industry.

To obtain more insight into the interface properties such as fixed charge density (Q_f) and interface defect density (D_{it}) of our industrially fired AlO_x/SiN_x stacks, contactless C–V measurements were performed on undiffused Si samples. These measurements revealed that the industrially fired AlO_x/SiN_x dielectric stacks on c-Si used in this study have a comparatively low midgap interface defect density of $<10^{11}$ eV^{-1}cm^{-2} in combination with a moderate negative fixed charge density in the range of (1–2) $\times 10^{12}$ cm^{-2}. Note that the fixed charge density in the dielectric stack is highly dependent on the deposition conditions and the postdeposition treatments used, as will be reported in detail in a separate study.

Understanding the surface passivation of p^+ Si surfaces by negatively charged dielectrics is relatively straightforward. A low interface defect density provides excellent chemical passivation. In addition, the negative fixed charge density reduces the minority carrier concentration at p^+ Si surfaces (for the B surface concentrations investigated in this study) providing field-effect passivation. Understanding the passivation of n^+ Si surfaces by negatively charged dielectrics is, however, not straightforward. For this purpose, we used advanced computer modeling (TCAD, Sentaurus) to study the role of field-effect passivation for heavily doped n^+ surfaces. In these simulations, we take both the fundamental hole surface recombination

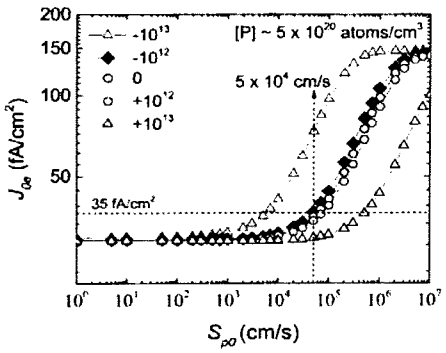

Fig. 6. Simulated J_{0e} as a function of the S_{p0} at the c-Si/dielectric interface for high (10^{13} cm^{-2}) and moderate (10^{12} cm^{-2}) fixed charge densities of both polarities in the dielectric film. A symmetrical n^+pn^+ sample was used with a 75-Ω/sq diffusion per side (the experimental measured diffusion profile from Fig. 1 was used in the simulation).

velocity parameter (S_{p0}) and the interface fixed charge (Q_f) into account, similar to the approach presented by Girish *et al.* [36] and Aberle *et al.* [37], and furthermore, using the physical models from [38] and [39], S_{p0} is the surface recombination velocity parameter for holes assuming flat band conditions and can be expressed by

$$S_{p0} \equiv \nu_{\rm th}\sigma_p N_{\rm st} \tag{3}$$

where $v_{\rm th}$ is the thermal velocity, σ_p is the capture cross-section for holes, and $N_{\rm st}$ is the number of surface states per unit area [40]. Using the measured n^+ dopant profile of the 75 Ω/sq diffusion from Fig. 1, J_{0e} versus S_{n0} curves for various fixed charge densities were determined. The results are shown in Fig. 6. From Fig. 6, it is clear that positive fixed charge densities are beneficial for the passivation of the 75-Ω/sq n^+ Si diffusion, resulting in significantly lower J_{0e} values for similar S_{p0} values. On the other side, a very high negative fixed charge density of 10^{13} cm^{-2} is found to be detrimental and results in higher J_{oe} values, in good agreement with the experimental results reported by Hoex *et al.* for n^+ Si passivated by Al_2O_3 films grown by the PA-ALD [20].

For moderate fixed interface charge densities in the range of -10^{12} cm^{-2} to $+10^{12}$ cm^{-2}, it can be seen that the fixed charge is hardly affecting the J_{0e} over the whole investigated S_{p0} range, and hence, the passivation is predominantly ruled by chemical passivation in this case. It should be noted that a similar trend (effect of fixed charge) was observed on other n^+ diffusions used in this study; however, the fixed charge range will depend on the surface dopant concentration. The results in Fig. 6 also allow us to extract the S_{p0} value at the interface between the c-Si wafer and the AlO_x/SiN_x stack. Taking the measured J_{0e} value of 35 fA/cm^2 and the measured Q_f of -10^{12} cm^{-2}, we can see that this results in a S_{p0} value of $\sim 5 \times 10^4$ cm/s. This value is in the similar order to the S_{n0} (electron surface recombination velocity parameter) value obtained by our PECVD AlO_x/SiN_x stack on heavily doped p^+ Si surfaces, which is in the range of 10^4 cm/s [41]. We observe that the S_{p0} value obtained in this study is slightly better than the S_{p0} reported by Altermatt *et al.* ($> 10^5$ cm/s) for n^+ Si having a surface dopant density of $\sim 2 \times 10^{20}$ atoms/cm^3 passivated by FGA thermal SiO_2 [39]. Hence, these results indicate that heavily doped n^+ Si surfaces can be passivated as effectively as heavily doped p^+ Si surfaces using a negatively charged PECVD AlO_x/SiN_x stack.

IV. Conclusion

In conclusion, we have shown that both n^+-type and p^+-type c-Si surfaces in a very wide sheet resistance range are well passivated by an industrially fired PECVD AlO_x/SiN_x dielectric stack. This is an important step forward in surface passivation with AlO_x/SiN_x dielectric stacks, as some high-efficiency c-Si solar cell designs (for example, all back-contact and bifacial Si solar cells) require passivation of both dopant polarities. Based on contactless *C–V* measurements and device simulations, we show that a negatively-charged AlO_x/SiN_x stack with lower charge density can provide excellent passivation on both n^+-type and p^+-type c-Si surfaces, provided the interface defect density remains low. In combination with the excellent results obtained on undiffused c-Si surfaces, our work demonstrates that all c-Si surfaces of relevance in today's PV industry can be well passivated by a firing stable, low-temperature deposited, and industrially feasible dielectric stack.

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Attachment K-4

Progress in Surface Passivation of Heavily Doped n-Type and p-Type Silicon by Plasma-Deposited AlO_x/SiN_x Dielectric Stacks

Shubham Duttagupta, Fa-Jun Ma, Serena Fen Lin, Thomas Mueller, Armin G. Aberle, and Bram Hoex

***Abstract*—We report an outstanding level of surface passivation for both n^+ and p^+ silicon by AlO_x/SiN_x dielectric stacks deposited in an inline plasma-enhanced chemical vapor deposition (PECVD) reactor for a wide range of sheet resistances. Extremely low emitter saturation current densities (J_{0e}) of 12 and 200 fA/cm^2 are obtained on 165 and 25 Ω/sq n^+ emitters, respectively, and 8 and 45 fA/cm^2 on 170 and 30 Ω/sq p^+ emitters, respectively. Using contactless corona–voltage measurements and device simulations, we demonstrate that the surface passivation mechanism on both n^+ and p^+ silicon is primarily due to a relatively low interface defect density of $<10^{11}$ eV^{-1}cm^{-2} in combination with a moderate fixed negative charge density of (1–2) $\times$ 10^{12} cm^{-2}. From advanced modeling, the fundamental surface recombination velocity parameter is shown to be in the order of 10^4 cm/s for PECVD AlO_x/SiN_x passivated heavily doped n^+ and p^+ silicon surfaces.**

***Index Terms*—Aluminum oxide/silicon nitride (AlO_x/SiN_x) stacks, boron-doped emitters, crystalline silicon, phosphorus-doped emitters, plasma-enhanced chemical vapor deposition (PECVD), surface passivation.**

I. Introduction

In recent years, amorphous aluminum oxide (AlO_x) has received tremendous interest from the photovoltaic community for its application as a surface passivation film for crystalline silicon wafer solar cells. AlO_x films provide excellent surface passivation on lightly doped n-type and p-type silicon as well as on heavy doped p^+ silicon [1]–[5]. In addition to a low interface defect density ($\sim 10^{11}$ eV^{-1}cm^{-2}), a distinguished property of AlO_x is the presence of a high negative charge density (10^{12}–10^{13} cm^{-2}, in units of elementary charges) in the film. This is especially beneficial on p-type c-Si surfaces as the minority carriers (electrons) are effectively shielded from the *c*-Si surface. Because of its excellent surface passivation properties on p-type surfaces, AlO_x has mainly been considered for the application in p-type passivated emitter and rear cell cells, p-type aluminum local back-surface field (Al-LBSF) cells, and n-type passivated emitter and rear locally diffused cells [6], [7].

Excellent passivation of heavily doped n^+ and p^+ silicon surfaces is very important for high-efficiency Si wafer solar cells. Some solar cell structures, such as interdigitated back-contact (IBC) solar cells, require simultaneous passivation of both dopant polarities [8], [9]. For this application, preferentially a suitable dielectric is needed that can passivate both n^+ and p^+ silicon surfaces simultaneously. Thick ($\sim$100 nm) thermal silicon oxide (SiO_2) films or stacks consisting of a thin (5–30 nm) SiO_2 film capped by a 50–100-nm-thick silicon nitride (SiN_x) film are often used due to their ability to passivate both n^+ and p^+ silicon surfaces [8]–[12]. However, low-temperature ($<$400 °C) surface passivation is typically preferred for the fabrication of industrial high-efficiency silicon wafer solar cells, due to its potential cost effectiveness, lower thermal budget, and the possibility for inline processing. Recently, Mihailetchi *et al.* reported excellent results for p^+ surfaces passivated by a stack consisting of an ultrathin oxide grown by hot HNO_3 and then capped with a SiN_x film [13]. Although no specific results are available in regards to its capability of passivating n^+ silicon surfaces, it can be considered a good method for passivating both n^+ and p^+ silicon surfaces simultaneously as these layers have already been used for large-area screen-printed IBC solar cells showing good efficiencies [14]–[17]. However, it should be noted that these devices showed moderate implied V_{oc} (iV_{oc}) in the range of 660–680 mV and also resulted in moderate solar cell open-circuit voltages of $V_{oc} < 650$ mV [14]–[17]. It is also suggested in these publications that an optimized dielectric is still needed that can passivate both n^+ and p^+ silicon surfaces simultaneously in order to achieve higher open-circuit voltage, and therefore, higher solar cell efficiency.

AlO_x films provide excellent surface passivation on p^+ silicon for an arbitrary sheet resistance [2], [18], [19]. Recently it has been shown that n^+-doped Si in a certain sheet resistance range can also be passivated by Al_2O_3 films grown by plasma-assisted and O_3-based atomic layer deposition (ALD), however, the results are not yet competitive [20], [21]. In addition, PA-ALD is not yet an industrially feasible technique. Thus, it is of great interest to investigate if negatively charged AlO_x films deposited by the industrial PECVD can provide excellent passivation on both n^+ and p^+ silicon surfaces.

In this study, we demonstrate that PECVD AlO_x/SiN_x dielectric stacks can provide excellent passivation on both heavily doped n^+ and p^+ silicon surfaces that are relevant for the industrial solar cell application. These results are primarily explained

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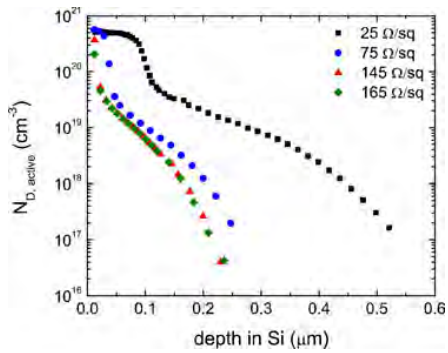

Fig. 1. Phosphorus dopant profile of n^+pn^+ samples measured by ECV profiling. The sheet resistance values determined by four-point probe measurements are shown in the graph.

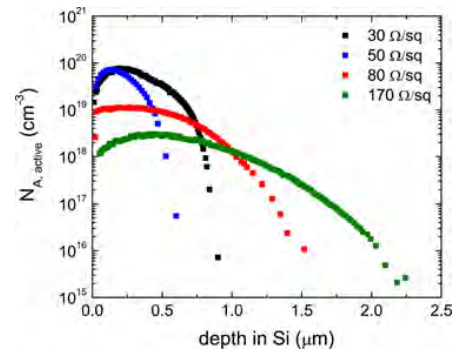

Fig. 2. Boron dopant profile of p^+np^+ samples measured by ECV profiling. The sheet resistance values determined by four-point probe measurements are shown in the graph.

by a low midgap interface defect density of $<10^{11}$ eV^{-1}cm^{-2}, which is beneficial for both n^+ and p^+ silicon surfaces. The stacks developed in this study feature a relatively moderate fixed negative charge density of (1–2) $\times$ 10^{12} cm^{-2}, as determined by contactless corona–voltage (*C–V*) experiments. Based on device simulations, we show that moderate fixed charge densities in the range of -10^{12} cm^{-2}–10^{12} cm^{-2} do not significantly affect the emitter saturation current density of typical industrial n^+ diffusions. Thus, the passivation is mainly ruled by the excellent electronic quality of the interface or low interface defect density.

II. Experimental Details

Symmetrical n^+pn^+ carrier lifetime structures were fabricated using an industrial $POCl_3$ diffusion process. The sheet resistance of the n^+ emitter was varied by changing the temperature and time of the $POCl_3$ diffusion. The phosphorus dopant profiles of the n^+pn^+ samples used in this study were measured with the electrochemical voltage (ECV) method, as shown in Fig. 1. The p-type Si wafers were monocrystalline (Cz method, boron-doped, 5–8 Ωcm), about 150 μm thick, pseudosquare (125 mm × 125 mm), and with a (100) surface orientation.

The p^+np^+ structures were fabricated by an industrial BBr_3 diffusion process. The p^+ emitter sheet resistance was varied by varying the process conditions during the BBr_3 diffusion and by a postdiffusion oxidation, as explained in detail elsewhere [18]. The boron dopant profiles of the p^+np^+ samples used in this study were measured by the ECV method, as shown in Fig. 2. The n-type Si wafers were monocrystalline (Cz, phosphorus-doped, 6–8 Ωcm), about 150 μm thick, pseudosquare (125 mm × 125 mm), and with a (100) surface orientation. After the diffusion process, the phosphorus or borosilicate glass layers were removed by dipping in HF solution, followed by rinsing in deionised water.

Prior to the deposition of the PECVD dielectric films, the samples were cleaned using the Radio Corporation of America (RCA) clean with a final HF dip followed by water rinsing and drying to ensure an H-terminated surface. The sheet resistance of the p^+ and n^+ diffusions was unaffected by the predeposition cleaning as confirmed by four-point probe measurements. The n^+pn^+ and p^+np^+ samples with various sheet resistances were coated on both sides with 30-nm AlO_x capped with 70-nm SiN_x, using an industrial inline microwave-powered remote PECVD reactor (SiNA-XS, Roth & Rau, Germany). We emphasize that all samples (n^+pn^+ and p^+np^+) were processed without any change in the PECVD process conditions. The deposition conditions are summarized in Table I.

After the PECVD processes, the samples received an activation anneal in an industrial fast firing furnace (Ultraflex, Despatch, USA) for a few seconds at a set peak temperature of >800 °C, similar to the cofiring step applied to the screen-printed metallization of industrial silicon wafer solar cells. The effective minority carrier lifetime ($\tau_{\rm eff}$) of the lifetime samples was measured using a contactless flash-based photoconductance decay tester (WCT-120, Sinton Instruments), in both the quasi-steady-state and the transient mode [22]. From the $\tau_{\rm eff}$ measurement, the emitter saturation current density (J_{0e}) per side of the n^+pn^+ and p^+np^+ samples was extracted from the slope of the Auger-corrected inverse lifetime versus injection level curve under high-injection conditions ($\Delta n \sim 10^{15}$ to 10^{16} cm^{-3} in our case), using the relation proposed by Kane and Swanson [23];

$$\frac{1}{\tau_{\rm eff}} - \frac{1}{\tau_{\rm Auger}} = \frac{1}{\tau_{\rm SRH}} + 2\frac{J_{0e}\,(N_d + \Delta n)}{q n_i^2 W} \qquad (1)$$

where $\tau_{\rm Auger}$ and $\tau_{\rm SRH}$ are the Auger lifetime and the Shockley–Read–Hall lifetime in the bulk of the sample [24], respectively, N_d and Δn are the doping concentration and the excess carrier concentration (or "injection level") in the bulk of the sample, q is the elementary charge, n_i is the intrinsic carrier concentration (8.6 × 10^9 cm^{-3} at 298 K) [25], and W is the thickness of the sample. In addition, contactless *C–V* measurements (PV-2000, Semilab SDI Inc., USA) were carried out to extract the fixed charge density (Q_f) and the interface defect density ($D_{\rm it}$) of the dielectric films on undiffused Si samples. The details of the measurement system and extraction procedure of Q_f and $D_{\rm it}$ are explained elsewhere [26]–[29].

III. Results and Discussion

Fig. 3 shows the measured injection level dependence of the Auger-corrected inverse effective carrier lifetime of industrially fired n^+pn^+ samples passivated on both sides by a PECVD AlO_x/SiN_x dielectric stack. The results cover a wide range of industry relevant sheet resistances (25–165 Ω/sq).

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TABLE I
EXPERIMENTAL DETAILS USED FOR THE DEPOSITION OF THE DIELECTRIC FILMS IN THIS STUDY

Dielectric	Process gas	Deposition temperature (°C)	Reactor pressure (mbar)	Plasma power (W)
AlO_x	$Al(CH_3)_3 + N_2O + Ar$	450	0.10	1500
SiN_x	$SiH_4 + NH_3$	200	0.20	3000

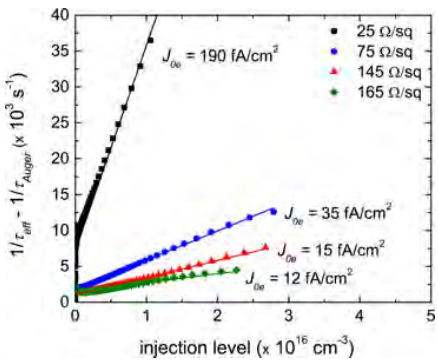

Fig. 3. Measured injection level dependence of the Auger-corrected inverse effective lifetime of industrially fired n^+pn^+ samples symmetrically passivated by PECVD AlO_x/SiN_x dielectric stacks (symbols). The sheet resistance of the n^+ emitters determined by four point probe measurements is shown in the legend. The J_{0e} values obtained from the straight-line fits (solid lines) are also shown.

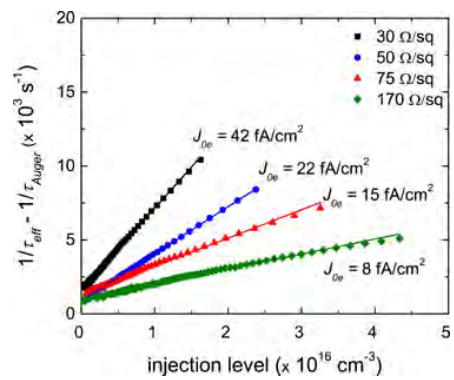

Fig. 4. Measured injection level dependence of the Auger-corrected inverse effective lifetime of industrially fired p^+np^+ samples symmetrically passivated by PECVD AlO_x/SiN_x dielectric stacks (symbols). The sheet resistance of the p^+ emitters determined by four point probe measurements is shown in the legend. The J_{0e} values obtained from the straight-line fits (solid lines) are also shown.

It is emphasized that we observe a linear relationship for all lifetime samples, allowing the extraction of J_{0e} values using (1). This was not always the case in the work of Hoex *et al.*, where it was mentioned that the relationship was not linear for 100–200 Ω/sq n^+ emitters passivated by PA-ALD Al_2O_3 [20]. This was attributed to the very high negative fixed charge density (up to 10^{13} cm^{-2}) of PA-ALD Al_2O_3 films, which strongly increased the minority carrier (hole) density at the n^+ surface in their work, and thereby, caused an injection level dependent J_{0e}. In this study, we show an excellent level of surface passivation with extremely low J_{0e} values of 12 fA/cm^2 for 165 Ω/sq planar n^+ emitters passivated by PECVD AlO_x/SiN_x dielectric stacks after an industrial firing process. As a matter of fact, the J_{0e} values obtained in this study are similar to, or even better than, the best values reported in the literature for n^+ emitters passivated by PECVD SiN_x [30]. These results are also significantly better than those obtained for n^+ emitters passivated by Al_2O_3 grown by ALD techniques reported so far [20], [21].

Identical PECVD stacks were also used to passivate p^+ emitters. Fig. 4 shows the measured injection level dependence of the Auger-corrected inverse effective carrier lifetimes of industrially fired p^+np^+ samples passivated on both sides with an AlO_x/SiN_x dielectric stack. The lifetime samples show a clear linear relationship, indicating again that (1) can be used to extract the J_{0e} value of this emitter. An extremely low J_{0e} value of 8 fA/cm^2 was obtained for a 170-Ω/sq emitter, which is comparable with the values obtained for p^+ emitters passivated by Al_2O_3 films grown by the PA-ALD [2]. It should be noted that in our earlier work, p^+np^+ samples were passivated on both sides with an AlO_x/SiN_x dielectric stack deposited under slightly different processing conditions [18]. In this study, both n^+pn^+ and p^+np^+ samples were processed simultaneously with 100 °C higher deposition temperature for AlO_x and ∼100 °C lower deposition temperature for capping SiN_x layer. This resulted in better interface quality and more importantly, a reduced fixed charge density. These stacks also provide excellent results on p^+ Si surfaces for a wide range of sheet resistance with similar J_{0e} values as reported earlier [18].

Table II summarizes the experimentally measured effective lifetime ($\tau_{\rm eff}$ at $\Delta n = 10^{15}$ cm^{-3}), emitter saturation current density (J_{0e}), and implied $V_{\rm oc}$ ($iV_{\rm oc}$) for n^+pn^+ and p^+np^+ samples symmetrically passivated by an industrially fired AlO_x/SiN_x dielectric stack. Note that effective lifetime and implied $V_{\rm oc}$ also depends on factors such as bulk doping level and bulk effective minority carrier lifetime of the used silicon wafer and the optical properties of the passivation coating, hence, care must be taken when comparing experimental values between different experiments. $V_{\rm oc,limit}$ represents the one-Sun open-circuit voltage limit of a solar cell at 25 °C calculated from the experimentally measured J_{0e} and assuming a short-circuit current density ($J_{\rm sc}$) of 40 mA/cm^2 with an ideal diode law ($n = 1$) by [22], [31]:

$$V_{\rm oc,limit} = n\frac{kT}{q}\ln\left(\frac{J_{\rm sc}}{J_{0e}} + 1\right) \tag{2}$$

where n is the diode ideality factor, which is considered one in this calculation. kT/q is 25.9 mV at 25 °C with k, T, q being the Boltzmann constant, absolute temperature in Kelvin and the elementary charge, respectively.

Fig. 5 shows the experimentally obtained J_{0e} values for n^+ and p^+ emitters passivated by industrially fired PECVD

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TABLE II
EXPERIMENTALLY DETERMINED EFFECTIVE LIFETIME ($\tau_{\rm eff}$) AT $\Delta n = 10^{15}$ cm^{-3}, SATURATION CURRENT DENSITY (J_{0e}) PER SIDE AND IMPLIED $V_{\rm oc}$ ($iV_{\rm oc}$) FOR n^+pn^+ AND p^+np^+ SAMPLES SYMMETRICALLY PASSIVATED BY AN AlO_x/SiN_x STACK

	Sheet resistance for phosphorus-diffused n^+ surface on p-type Si (Ω/sq.)				Sheet resistance for boron-diffused p^+ surface on n-type Si (Ω/sq.)			
	25	**75**	**145**	**165**	**30**	**50**	**80**	**170**
τ_{eff} (µs)	94	465	770	700	484	841	700	930
J_{0e} (fA/cm^2)	190	35	15	12	45	22	15	8
iV_{oc} (mV)	640	688	706	703	670	690	700	712
$V_{oc,\,limit}$ (mV)	670	713	735	741	707	725	735	751

The $V_{oc,limit}$ was calculated by (2) using the measured J_{0e} values.

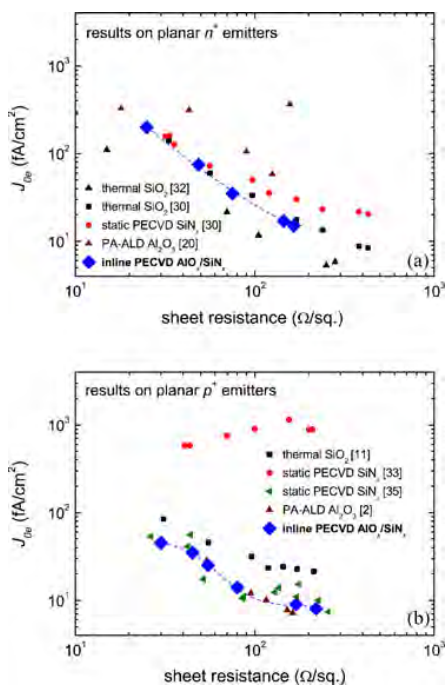

Fig. 5. Experimentally obtained J_{0e} values (diamonds in this work) for (a) n^+ emitters and (b) p^+ emitters passivated by industrially fired PECVD AlO_x/SiN_x stacks (the dotted lines are guides to the eye). Each of our J_{0e} values is the average result of a batch of 10 samples. Also shown, for comparison, are state-of-the-art J_{0e} values reported in the literature for planar n^+ and p^+ emitters passivated by thermal SiO_2, PECVD SiN_x, and ALD-grown Al_2O_3.

AlO_x/SiN_x stacks. For comparison, the best published results from the literature are included as well. It should be noted that the preparation of the n^+ and p^+ emitters in the various studies were different and most likely resulted in different dopant profiles for a comparable sheet resistance. This potentially affects the Auger recombination losses in these emitters. However, the general trend can be used for comparison. It is evident from Fig. 5 that thermal SiO_2 is a good candidate for both dopant polarities, showing excellent surface passivation of n^+ emitters and a decent surface passivation for p^+ emitters after either *alneal* (aluminum-annealing) or forming gas anneal (FGA) [11], [30], [32]. PECVD SiN_x provides excellent passivation of n^+ emitters after FGA [30]. Generally, these SiN_x films provide a compromised level of surface passivation on p^+ emitters [11], [33]. Only limited reports are available were PECVD SiN_x provides a good level of surface passivation on p^+ emitters, however, the underlying mechanism is not yet properly understood [34], [35]. Similarly PA-ALD Al_2O_3 films provide only a moderate passivation on n^+ emitters [see Fig. 5(a)], however, p^+ surfaces with an arbitrary sheet resistance can be well passivated with PA-ALD Al_2O_3 films [2], [20]. Based on the experimental results presented in this study, it is clear that our industrially fired PECVD AlO_x/SiN_x stacks provide an excellent level of surface passivation on both n^+ and p^+ emitters, for the entire investigated sheet resistance range. Hence, our work demonstrates that these PECVD AlO_x/SiN_x stacks can be used to simultaneously passivate all c-Si surfaces that are of relevance in today's PV industry.

To obtain more insight into the interface properties such as fixed charge density (Q_f) and interface defect density (D_{it}) of our industrially fired AlO_x/SiN_x stacks, contactless *C–V* measurements were performed on undiffused Si samples. These measurements revealed that the industrially fired AlO_x/SiN_x dielectric stacks on c-Si used in this study have a comparatively low midgap interface defect density of $<10^{11}$ eV^{-1}cm^{-2} in combination with a moderate negative fixed charge density in the range of (1–2) $\times$ 10^{12} cm^{-2}. Note that the fixed charge density in the dielectric stack is highly dependent on the deposition conditions and the postdeposition treatments used, as will be reported in detail in a separate study.

Understanding the surface passivation of p^+ Si surfaces by negatively charged dielectrics is relatively straightforward. A low interface defect density provides excellent chemical passivation. In addition, the negative fixed charge density reduces the minority carrier concentration at p^+ Si surfaces (for the B surface concentrations investigated in this study) providing field-effect passivation. Understanding the passivation of n^+ Si surfaces by negatively charged dielectrics is, however, not straightforward. For this purpose, we used advanced computer modeling (TCAD, Sentaurus) to study the role of field-effect passivation for heavily doped n^+ surfaces. In these simulations, we take both the fundamental hole surface recombination

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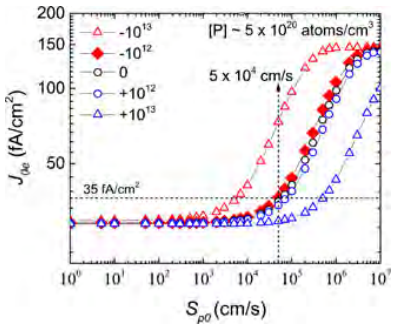

Fig. 6. Simulated J_{0e} as a function of the S_{p0} at the c-Si/dielectric interface for high (10^{13} cm^{-2}) and moderate (10^{12} cm^{-2}) fixed charge densities of both polarities in the dielectric film. A symmetrical n$^+$pn$^+$ sample was used with a 75-Ω/sq diffusion per side (the experimental measured diffusion profile from Fig. 1 was used in the simulation).

velocity parameter (S_{p0}) and the interface fixed charge (Q_f) into account, similar to the approach presented by Girish *et al.* [36] and Aberle *et al.* [37], and furthermore, using the physical models from [38] and [39], S_{p0} is the surface recombination velocity parameter for holes assuming flat band conditions and can be expressed by

$$S_{p0} \equiv \nu_{\rm th}\sigma_p N_{\rm st} \tag{3}$$

where $v_{\rm th}$ is the thermal velocity, σ_p is the capture cross-section for holes, and $N_{\rm st}$ is the number of surface states per unit area [40]. Using the measured n$^+$ dopant profile of the 75 Ω/sq diffusion from Fig. 1, J_{0e} versus S_{n0} curves for various fixed charge densities were determined. The results are shown in Fig. 6. From Fig. 6, it is clear that positive fixed charge densities are beneficial for the passivation of the 75-Ω/sq n$^+$ Si diffusion, resulting in significantly lower J_{0e} values for similar S_{p0} values. On the other side, a very high negative fixed charge density of 10^{13} cm^{-2} is found to be detrimental and results in higher J_{oe} values, in good agreement with the experimental results reported by Hoex *et al.* for n$^+$ Si passivated by Al_2O_3 films grown by the PA-ALD [20].

For moderate fixed interface charge densities in the range of -10^{12} cm^{-2} to $+10^{12}$ cm^{-2}, it can be seen that the fixed charge is hardly affecting the J_{0e} over the whole investigated S_{p0} range, and hence, the passivation is predominantly ruled by chemical passivation in this case. It should be noted that a similar trend (effect of fixed charge) was observed on other n$^+$ diffusions used in this study; however, the fixed charge range will depend on the surface dopant concentration. The results in Fig. 6 also allow us to extract the S_{p0} value at the interface between the c-Si wafer and the AlO_x/SiN_x stack. Taking the measured J_{0e} value of 35 fA/cm^2 and the measured Q_f of -10^{12} cm^{-2}, we can see that this results in a S_{p0} value of $\sim 5 \times 10^4$ cm/s. This value is in the similar order to the S_{n0} (electron surface recombination velocity parameter) value obtained by our PECVD AlO_x/SiN_x stack on heavily doped p$^+$ Si surfaces, which is in the range of 10^4 cm/s [41]. We observe that the S_{p0} value obtained in this study is slightly better than the S_{p0} reported by Altermatt *et al.* ($> 10^5$ cm/s) for n$^+$ Si having a surface dopant density of $\sim 2 \times 10^{20}$ atoms/cm^3 passivated by FGA thermal SiO_2 [39]. Hence, these results indicate that heavily doped n$^+$ Si surfaces can be passivated as effectively as heavily doped p$^+$ Si surfaces using a negatively charged PECVD AlO_x/SiN_x stack.

IV. Conclusion

In conclusion, we have shown that both n$^+$-type and p$^+$-type c-Si surfaces in a very wide sheet resistance range are well passivated by an industrially fired PECVD AlO_x/SiN_x dielectric stack. This is an important step forward in surface passivation with AlO_x/SiN_x dielectric stacks, as some high-efficiency c-Si solar cell designs (for example, all back-contact and bifacial Si solar cells) require passivation of both dopant polarities. Based on contactless *C–V* measurements and device simulations, we show that a negatively-charged AlO_x/SiN_x stack with lower charge density can provide excellent passivation on both n$^+$-type and p$^+$-type c-Si surfaces, provided the interface defect density remains low. In combination with the excellent results obtained on undiffused c-Si surfaces, our work demonstrates that all c-Si surfaces of relevance in today's PV industry can be well passivated by a firing stable, low-temperature deposited, and industrially feasible dielectric stack.

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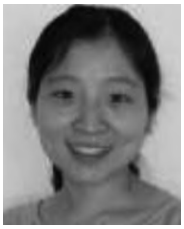

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HIGH-EFFICIENCY RISE-IBC SOLAR CELLS: INFLUENCE OF REAR SIDE-PASSIVATION ON PN-JUNCTION MEANDER RECOMBINATION

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ABSTRACT: We investigate the influence of the rear side passivation scheme in our *n*-type RISE-IBC (Rear Interdigitated Single Evaporation - Interdigitated Backjunction Cell) solar cells. We compare selective rear-side passivation, i.e. the passivation of the n^+ doped back surface field with thermally grown SiO_2 and the passivation of the p^+ doped emitter with PA-ALD (plasma-assisted atomic layer deposition) Al_2O_3, with full-area Al_2O_3 rear-side passivation of both polarities. We show evidence that the choice of rear-side passivation strongly influences the strength of the recombination where the *pn*-junction meander surfaces at the rear of the solar cell. While selective rear-side passivation yields on average 7 mV higher open circuit voltages, the surface recombination at the *pn*-junction is significant for this passivation scheme, implying lower pseudo fill factors. The highest energy conversion efficiency of 23.1% is achieved with selective rear-side passivation. The RISE-IBC solar cells of this study do not have a diffused front-surface field (FSF), but instead rely solely on SiN_x passivation of the textured front side. Nevertheless, very high fill factor values > 82% are obtained. Lateral conductivity of the FSF is obviously not necessarily needed for achieving high fill factors, particularly not for the low-resistivity (< 2 Ω.cm) *n*-type Cz Si wafers used in this study.

Keywords: High-efficiency, Passivation, Back Contact, SiO, Al_2O_3, c-Si

1 INTRODUCTION

IBC (Interdigitated Backjunction Cell) solar cells have proven to be a suitable cell architecture for commercially producing high-efficiency solar cells [1,2]. The process complexity implied by the necessity to form patterned doped regions on the cell rear side can be significantly reduced by using "enabling techniques", e.g. in-situ patterned ion implantation [3,4]. On the other hand, excellent IBC cell results have been demonstrated by various institutes [5,6] on small area cells fabricated with laboratory (lab)-type processes. Those lab-type processes are usually lacking of an enabling technology, thus implying a large number of process steps. The RISE (Rear Interdigitated Single Evaporation) - IBC process developed at ISFH [7-9] uses laser structuring instead of photolithography, but still implies a rather high number of process steps. We therefore also consider the RISE process as rather lab- than industrial-type. There are different applications of lab-type IBC processes: (*i*) as an internal research platform, e.g. for the evaluation of innovative module interconnection schemes [10] or the evaluation of the efficiency potential of promising kerfless technologies [9], (*ii*) as an evaluation platform for wafer material and single process steps of external partners, and (*iii*) for principle studies of effects also relevant for industrial IBC cells [5].

In this paper, we evaluate on the one hand the performance of the $POCl_3$-diffusion process of Hanwha Solar America (HSA) R&D facility, alongside with the *n*-type Cz Si wafers that are accessible to HSA (application (*ii*)). For this purpose we use these wafers and HSA's $POCl_3$-diffusion for performing ISFH's RISE-IBC solar cell process and compare the performance to RISE-IBC solar cells where all of the processes have been performed at ISFH. On the other hand, and more fundamentally, we investigate in this paper the effect of rear side passivation (application (*iii*)): A passivation layer deposited full-area on the rear-side of an IBC cell has to passivate both polarities, i.e., the p^+ doped emitter and the n^+ doped BSF (Back Surface Field). While Al_2O_3 is known to yield excellent passivation quality on p^+ doped surfaces [11,12], the passivation quality on n^+ doped surfaces seems to depend on the Al_2O_3 deposition method. While excellent results have been reported recently for PE-CVD (Plasma Enhanced Chemical Vapor Deposition) - deposited Al_2O_3 [13], PA-ALD (Plasma Assisted Atomic Layer Deposition) - deposited Al_2O_3 seems to provide a rather poor passivation on n^+ doped surfaces [14]. It should therefore be beneficial to apply a "selective" rear-side passivation, i.e., to passivate only the boron emitter with Al_2O_3 while well-passivating the phosphorous doped BSF with thermally grown SiO_2 [15]. In this paper, we compare selective rear-side passivation to full-area passivation of the rear-side with PA-ALD-deposited Al_2O_3.

2 EXPERIMENTALS

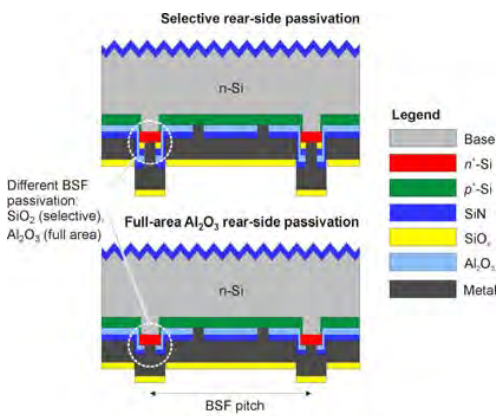

Figure 1: Illustration of the *n*-type RISE IBC structure for the two different rear-side passivation schemes investigated.

The primary features of the RISE process are described in detail in previous publications [7-9], where we have realized a cell structure similar to that of Sinton *et al.* [16], except that the RISE cell consists of a laser-based lithography-free self aligned process for rear side

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semiconductor structuring and metallization. The schematic cross sections of the solar cells of this investigation are shown in Figure 1.

We compared two different wafer materials: 2 Ωcm *n*-type Cz received from Hanwha Solar America, and material in stock at ISFH, in this case 1.4 Ωcm *n*-type Cz. For the 2 Ωcm HSA material, the phosphorus diffusion was performed either at HSA or at ISFH. All other process steps of the solar cells of these groups were performed at ISFH. The solar cells made from the 1.4 Ωcm wafers were completely processed at ISFH.

We processed 25 small area cells (20x20) mm² on full (156x156) mm² pseudosquare *n*-type Cz wafers. On each wafer, we applied four variations of the device geometry and report here about the performance of two pitches: 2300 µm and 1150 µm BSF pitch, both with emitter/BSF finger width ratio 18/5. We adjusted the distance of the laser contact openings [7,17] in order to ensure that solar cells of both pitches also have the same contact area fraction.

We also prepared reference samples for monitoring of each process step by measuring emitter saturation currents and doping profiles. The reference samples feature on both sides on the full area the respective cell area preparation, i.e. emitter or BSF diffusion, or textured front side passivation. To evaluate the recombination of these cell regions we let the reference samples undergo the full cell processing sequence. The saturation current densities determined on the reference samples are listed in Tab. 1. For the phosphorous doped BSF, the J_{0e} values for Al_2O_3 passivation comparable to those reported by Hoex *et al.* [14]. From the area-weighted J_{0e} values for the BSF, one expects a V_{oc} difference of ~ 6 mV between the selective and the full-area rear-side passivation scheme.

	R_{sheet} [Ω/□]	J_{0e} **Al_2O_3** pass. [fA/cm²]	J_{0e} **SiO_2** pass. [fA/cm²]
Phosphorous BSF, HSA $POCl_3$ diffusion	53	215 ± 30	83 ± 10
Phosphorous BSF, ISFH $POCl_3$ diffusion	31	145 ± 20	95 ± 10
Boron emitter	61	20 ± 3	-

Table 1: Saturation current densities, determined by QSSPC [18] on reference samples.

3 CELL RESULTS

The main *IV*-curve quantities, as determined in-house under standard test conditions, are shown in Fig. 2. For all quantities, one should remark that no significant differences between the three groups - 2Ωcm HSA material, phosphorous diffusion performed either at HSA or ISFH and 1.4 Ωcm HSA material, ISFH $POCl_3$ diffusion - are resolvable. The HSA material (the HSA $POCl_3$ diffusion) is performing as excellent as the ISFH reference material (the ISFH $POCl_3$ diffusion). For more details on the comparison of the different groups, the reader should refer to Ref. [19].

For the open circuit voltage V_{oc}, the constant emitter area fraction and the constant metalized area fraction imply comparable values for both BSF pitches. The cells with selective rear-side passivation exhibit on average ~7 mV higher V_{oc} values than the cells with full-area Al_2O_3 passivation, in agreement with the expectation from the area-weighted J_{0e}-values of the reference samples (Sec. 2).

No clear influence of the rear-side passivation scheme can be resolved in the short-circuit current density (J_{sc}) values. By contrast, the BSF pitch clearly influences J_{sc}: for 1150 µm pitch, J_{sc} is ~0.4 mA/cm² higher than for 2300 µm pitch. This observation can be explained by the so-called "electrical shading"-effect [20], which describes the reduced minority carrier collection efficiency implied by extended BSF regions.

For the fill factor (*FF*), a smaller BSF pitch is clearly beneficial. Lateral transport losses implied by the rather long majority carrier paths in case of the 2300µm BSF pitch are a plausible explanation for this observation.

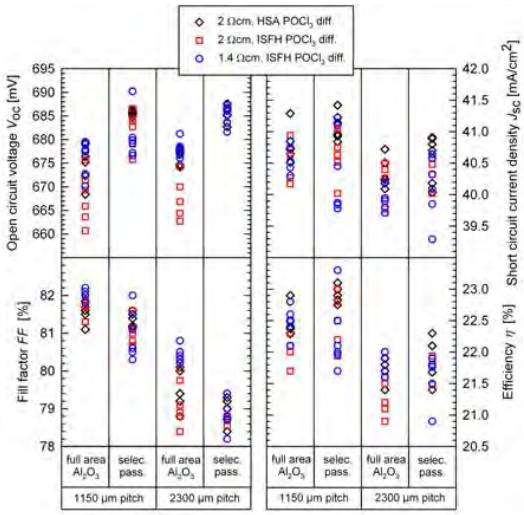

Figure 2: Main *IV*-quantities for BSF-pitches of 1150µm and 2300µm and for the two passivation schemes (in-house measurement, designated area of 3.97cm²).

Nevertheless, the absolute *FF* values up to more than 82% are very high, especially in face of the absence of a diffused front-surface field. Obviously, the additional lateral conductivity provided by a FSF is not necessarily required, particularly not for the low-resistivity (≤2 Ω.cm) *n*-type Cz Si wafers used in this study. This observation poses experimental support of the simulation-based prediction of Ohrdes *et al.* [21]. The most puzzling observations is the dependency of the fill factor on the rear-side passivation scheme. For both BSF pitches investigated, the absolute *FF* values for full area Al_2O_3 rear-side passivation are ~0.5% higher than for selective rear-side passivation. This effect is further discussed in Sec. 4.

Due to higher J_{sc} and *FF*, the efficiency is highest for the cells with 1150µm pitch. Several cells from different groups are measured in-house with efficiencies >23%. The expected benefit of the selective rear-side passivation is not obvious from the measured efficiency values. The counteracting dependency of V_{oc} and *FF* on the rear-side passivation scheme implies only slightly higher average efficiencies for the cells with selective rear-side passivation.

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The cell measured in-house with the highest efficiency - 1150µm pitch, selective rear-side passivation, 1.4Ωcm material, ISFH $POCl_3$ diffusion - was sent to F-ISE CalLab for independent confirmation. Table 2 compares the confirmed *IV*-curve quantities to the in-house measurements. Within the range of uncertainty, all quantities are in good agreement. We thus conclude that the same accounts for the other data shown in Fig. 2.

	In-house data	F-ISE CalLab data
Short circuit current density J_{sc}	41.2 mA/cm^2	41.3±1mA/cm^2
Open circuit voltage V_{oc}	690.2 mV	686.2±3.4 mV
Fill factor *FF*	82 %	81.59±0.82 %
Efficiency	23.3 %	23.12±0.7 %

Table 2: Best cell: comparison of the in-house measured *IV*-quantities with the values independently confirmed by F-ISE CalLab.

4 PSEUDO FILL FACTOR ANALYSIS

The puzzling dependency of the *FF* on the rear-side passivation scheme requires more discussion. In order to exclude any difference induced by series resistance, we determined the pseudo fill factor (*pFF*) from suns-V_{oc} measurements (Fig. 3).

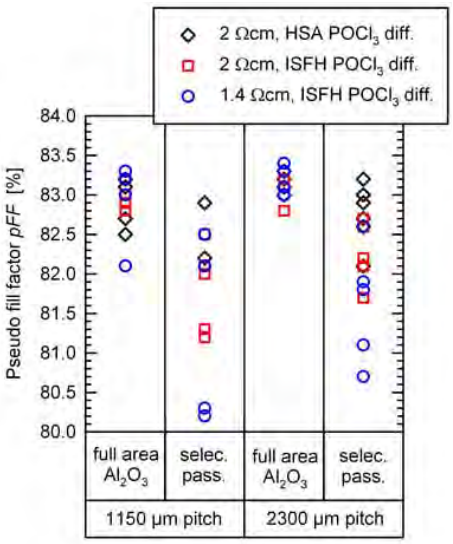

Figure 3: Pseudo fill factor values, determined by suns-V_{oc} measurements.

Also for the *pFF*, significantly higher values are obtained in case of full-area Al_2O_3 rear-side passivation. Obviously, the different rear-side passivation schemes imply a different recombination behavior. The highest *pFF* values are obtained for the cells with 2300µm BSF pitch and full-area Al_2O_3 rear-side passivation. For the cells with selective rear-side passivation, the *pFF* values seem to be higher for the larger BSF pitch.

In order to analyze the recombination behavior of the cells with selective rear-side passivation, we compare the suns-V_{oc} curve of the complete cell with the area-weighted suns-$V_{oc,impl.}$ curves measured on the reference samples (Fig. 4). The representative cell chosen for this analysis has a BSF pitch of 2300µm and a rather low *pFF*

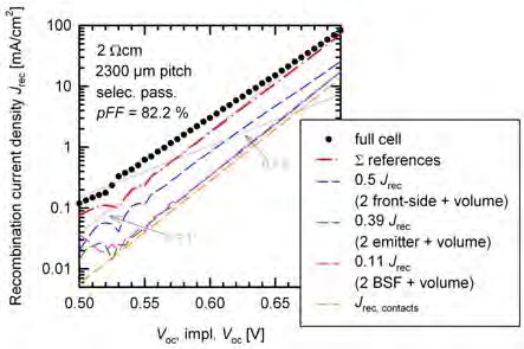

Figure 4: (Symbols) recombination current density of a representative cell with selective rear-side passivation and 2300µm BSF pitch (2Ωcm, ISFH $POCl_3$ diffusion), determined by suns-V_{oc} measurements. The dashed lines represent the area-weighted recombination currents of the references samples, determined by suns-$V_{oc,impl.}$ measurements.

of 82.2%. In the voltage regime investigated, the recombination current density of the complete cell (symbols) can neither be well described by an ideality factor of n=1 nor by an ideality factor of n=2 (solid lines). The suns-$V_{oc,impl.}$ curves from the reference samples (dashed lines) are scaled by the half of the area fraction of the respective region. The factor 0.5 arises from the fact that the references are symmetrical samples, featuring either two textured sides with SiN_x passivation (front side reference) or two sides with passivated boron emitter or phosphorous BSF region. The injection-level dependent bulk recombination is also included in the suns-$V_{oc,impl.}$ curves of the reference samples and thus scaled accordingly. Since the recombination at the metal contacts is more difficult to determine, we calculated this contribution by assuming an ideality factor n=1 and $J_{0e,met}$ values as reported in Ref. [18] (600 fA/cm^2 for the 60 Ω/□ boron emitter and 500 fA/cm^2 for the 30 Ω/□ phosphorous BSF). One should remark that an error in the $J_{0e,met}$ values is of minor effect for the total recombination due to the small metalized area fraction (3.7 % in total). The illumination levels are scaled by the short current density of the cell. The sum of all references (dash-dotted line) poorly describes the recombination current of the complete cell. Obviously, there is an additional recombination path present in the cell. The most plausible origin for this additional recombination is recombination at the *pn*-junctions. In the following, we therefore denote this recombination current density by $J_{rec,pn}$. Since the choice of rear-side passivation strongly influences the strength of $J_{rec,pn}$, this recombination seems to occur where the *pn*-junction meander surfaces at the cell rear side [22].

Since the cells with finger pitch 1150 µm and 2300 µm have the same emitter/BSF area coverage fraction and the same contact opening fraction but a different *pn*-junction meander length, subtracting the suns-V_{oc} curve of the 2300 µm pitch cell from that of the 1150 µm pitch cell should give a fingerprint of the recombination at the *pn*-junction meander. In fact, if we assume that the

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recombination at this meander is microscopically identical for both cell types, this subtraction should yield exactly the *pn*-junction meander recombination $J_{rec,pn}$ of the 2300 µm pitch cell. This is shown in Fig.5.

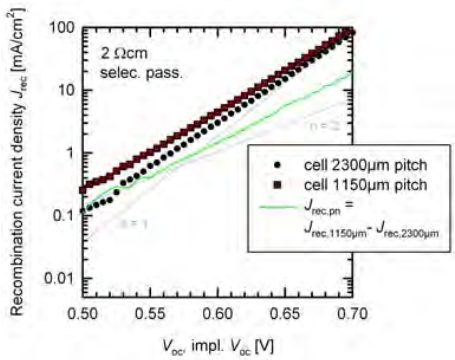

Figure 5: Recombination current densities of two representative cells with 1150µm and 2300µm BSF pitch (selective rear-side pass., 2Ωcm, ISFH $POCl_3$ diffusion). The solid line corresponds to the difference between the recombination current densities.

The ideality factor of $J_{rec,pn}$ is ~1.5. For full-area Al_2O_3 passivation, the recombination current density for cells with a pitch of 1150µm is not significantly larger than for cells with a pitch of 2300µm, implying very low $J_{rec,pn}$ values (not shown).
Adding $J_{rec,pn}$ to the area-weighted recombination currents densities for the emitter, BSF, contacts, front-side and bulk, the total recombination of the full cell can be well reproduced (Fig. 6). This excellent agreement supports the hypothesis that the missing additional recombination mechanism visible in Fig. 4 is indeed correlated with the recombination at the *pn*-junction meander.

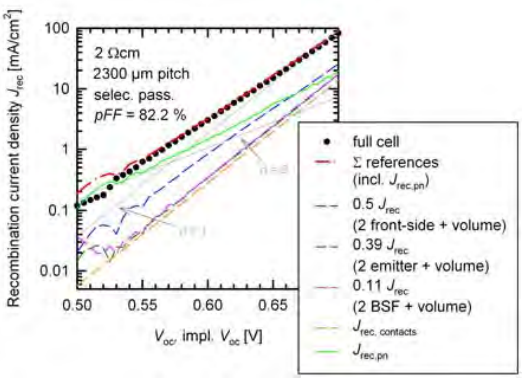

Figure 6: Comparison of the recombination current density for the 2300µm pitch cell (symbols) with the sum (dash-dotted line) of all references (dashed lines) and the *pn*-junction meander recombination $J_{rec,pn}$ (solid line).

5 CONCLUSIONS

We investigate the influence of the rear side passivation scheme in our *n*-type RISE-IBC solar cells. We compare selective rear-side passivation, i.e. the passivation of the n^+ doped BSF with thermally grown SiO_2 and the passivation of the p^+ doped emitter with Al_2O_3, with full-area Al_2O_3 rear-side passivation of both polarities.
While the highest open circuit voltages are achieved with selective rear-side passivation, the corresponding pseudo fill factor is found to be significantly lower than with full-area Al_2O_3 passivation. Nevertheless, the highest efficiency obtained in this study is measured to 23.1% on a cell with selective rear-side passivation.
The puzzling recombination behavior of the cells with selective rear-side passivation cannot be described by the sum of all area-weighted recombination currents of the front-side, emitter, BSF, contacts and volume determined on reference samples. An additional recombination path is obviously present in the full cells. We attribute this additional recombination to surface recombination at the *pn*-junction at the rear side of the solar cell. We quantify this recombination current density $J_{rec,pn}$ by subtracting the suns-V_{oc} curves of cells with different *pn*-junction meander length. Adding $J_{rec,pn}$ to the area-weighted recombination currents densities for the emitter, BSF, contacts, front-side and bulk, the total recombination of the full cell can be well reproduced.
At present, the microscopic origin for the significant surface recombination at the *pn*-junction in case of selective rear-side passivation is not clear and requires further investigations. Nevertheless, we conclude that a proper surface passivation of the *pn*-junction is crucial to achieve high pseudo fill factors in IBC cells.

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Ion implantation for all-alumina IBC solar cells with floating emitter

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Abstract

Interdigitated back contact (IBC) solar cells have a high efficiency potential. However, the fabrication of this cell structure is quite complex. Ion implantation for structured doping together with batch reactors for front and rear side passivation with Al_2O_3 could help to reduce the fabrication effort. Since Al_2O_3 gives a very good passivation on *p*-doped surfaces, we investigate *n*-type IBC solar cells with a low-dose ion-implanted front floating emitter (FFE) which we compare to a low-dose ion implanted front surface field (FSF) passivated by SiO_2. We measured saturation current densities (J_0) between 10 and 15 fA/cm^2 for the SiO_2 passivated FSF and down to 5 fA/cm^2 for the Al_2O_3 passivated FFE on textured samples. The FFE has been successfully applied to fully implanted IBC cells ($\eta = 21.8$ %). Cells with FSF degraded strongly under UV-illumination due to the instable SiO_2 passivation on the front side while the FFE cells with Al_2O_3 passivation were much less affected. IV measurements under low level illumination revealed a linear performance down to 0.01 suns for both, FSF and FFE.

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Keywords: ion implantation; IBC solar cells; floating emitter

1. Introduction

Interdigitated back contact (IBC) solar cells have a high efficiency potential as there are no metal contacts on the front side resulting in a maximum absorption of the incident light. Having both, *n*- and *p*-contacts, on the back side necessitates a structured doping which makes the fabrication of this cell concept quite complex. It has been shown

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that selective doping structures can be easily formed by ion implantation using shadow masks [1]. This process could help to reduce the fabrication complexity of IBC solar cells significantly. As the IBC solar cell relies on a perfect passivation on the front side, the formation of a very lowly doped FSF or FFE which allows for a low recombination would be quite beneficial for this type of cell. Such type of profiles can easily be realized by ion implantation. Another possibility to get to a cost effective production is the passivation of both sides in a single process step using large scale ALD batch reactors. Al_2O_3 is an excellent passivation of (implanted) boron-doped profiles [2] and, recently, it has been shown that it is also possible to achieve a good passivation of heavily phosphorus-doped profiles applying suitable process parameters [3].

An all-alumina passivated IBC cell on *n*-type material can be realized by applying a boron-doped floating emitter on the front side. This concept could benefit from the stable passivation provided by the Al_2O_3 passivation [4]. It is known that the passivation quality of SiO_2 degrades under UV-illumination [5, 6]. Gruenbaum *et al*. found an increased surface recombination velocity after UV-illumination, most probably due to an increased defect density at the Si/SiO_2 interface [5]. Since alumina passivation is mainly based on the electrical shielding of electrons by the huge amount of fixed negative charges, a much weaker influence of UV-illumination on the passivation quality is expected [4]. A front floating emitter (FFE) formed with a $POCl_3$ diffusion on *p*-type material and passivated with a SiO_2/SiN_x layer stack was already investigated by Granek *et al*. [7]. They found a poor cell performance compared to samples with a conventional front surface field (FSF) on *n*-type material at low illumination intensities which was explained by a defect related shunt resistance across the floating junction. It is still unclear whether this effect influences a boron-doped front floating emitter in *n*-type IBC solar cells to the same extent as phosphorus-doped front floating emitter in *p*-type IBC-solar cells.

In this study processes for the formation of doping profiles suitable for all-alumina *n*-type IBC solar cells are presented. We evaluate different processing parameters and those resulting in the most promising profiles are applied for the fabrication of small area solar cells. IBC solar cells featuring an alumina passivated floating emitter and reference cells with a FSF passivated by a SiO_2/SiN_x stack were fabricated. We compared the cell performance of FSF and FFE cells under low level illumination and the degradation due to UV-illumination.

2. Experimental

Symmetrical lifetime samples were prepared on 10 Ω cm *n*-type FZ silicon. They first received an RCA clean followed by a boron or a phosphorus implantation (Varian VIISta HC) on both sides with doses between 1e13 and 3e15 cm^{-2}. Then all samples received an SC2 clean before the annealing in a tube furnace. For this process a peak time of 80 min at 1050 °C in a non-oxidizing atmosphere has been applied. For the passivation, the samples were either dipped in HF (1 % HF) and received an alumina passivation (plasma assisted atomic layer deposition, PA-ALD) or entered the furnace again to grow a 10 nm thermal oxide which then was capped by a PECVD silicon nitride. Finally, the Al_2O_3 and SiO_2/SiN_x passivation was activated or improved by a forming gas anneal for 25 min at 425 °C, respectively.

For the fabrication of small area IBC solar cells we used 1 Ω cm *n*-type FZ silicon. The samples received an RCA clean and random pyramids were etched on the front side (only in active cell area). Ion implantation was used to form the doped regions: floating emitter (FE) on the textured front side (1e14 cm^{-2} boron), emitter (1.5e15 cm^{-2} boron) and back surface field (BSF) (3e15 cm^{-2} phosphorus) on the planar back side. The masking of the local implantations was done by photoresists. All implanted regions were co-annealed in a tube furnace for 80 min at 1050 °C in a non-oxidizing atmosphere and passivated by PA-ALD Al_2O_3. The front side was capped by a PECVD nitride and the back side by a PECVD silicon oxide. Aluminum was evaporated on the back side (10 µm thickness) and structured in a wet chemical etch solution with a photoresist mask. Finally, the finished cells were annealed on a hotplate for 5 min at 340 °C to activate the passivation and improve the electrical contact. Samples with front surface field (FSF) were processed identically but received an implantation of phosphorus instead of boron on the front side and 10 nm thermal oxide (etched on back side afterwards) instead of Al_2O_3.

QSSPC measurements were done with a WCT120 tester. The sheet resistance was determined with a four point probe measurement tool. The doping profiles were measured by electrochemical capacitance-voltage (ECV) profiling. IV curves were measured in house under calibrated standard conditions. Degradation experiments were executed with a sun tester at 500 W/m^2.

3. Results

3.1. Doping profiles & lifetimes

Figure 1 shows ECV profiles measured after ion implantation of boron or phosphorus and furnace annealing. With the ion implanter used in this study it is possible to run perfectly controlled and uniform processes with doses down to 1e13 ions/cm^2 resulting in extremely weak doping profiles with peak doping concentrations in the range of 1e17 to 2e18 cm^{-3}. The sheet resistance (R_{Sheet}) of the implanted FFE and FSF samples is in the range of several hundred (1e14 cm^{-2} dose) to thousands (1e13 cm^{-2} dose) Ohm per square (see Table 1).

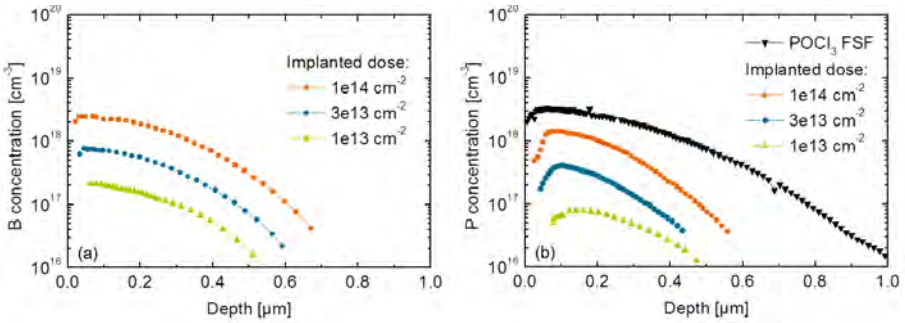

Fig. 1. ECV profiles measured on planar samples after ion implantation and annealing for 80 min at 1050 °C. (a) Low dose boron implantations for a floating emitter; (b) low dose phosphorus implantations for a front surface field. A conventional $POCl_3$-diffused FSF used in Ref [8] is shown for comparison.

The diffusivity of boron and phosphorus during the furnace anneal is quite similar. Profile depths are in the range of 0.5 to 0.7 µm with boron diffusing a little bit deeper. Since the phosphorus profiles are intended for a front surface field passivated by a SiO_2/SiN_x stack, a ~10 nm thick thermal oxide was grown after the annealing. This is done at a much lower temperature and has only a minor influence on the resulting profile, except for the depletion of phosphorus close to the surface.

QSSPC measurements reveal that the saturation current is very low for low dose boron implants passivated with Al_2O_3. According to the intended application on the front side of a solar cell, textured samples with random pyramids on both sides have been used for lifetime studies. Saturation current densities (J_0) down to 5 fA/cm^2 have been achieved (see Table 1). For the boron implanted samples there is a slight trend showing an increase in J_0 for higher boron doses. This is because Auger recombination and the surface recombination velocity usually increase with higher doping concentrations (see Ref [9] for Al_2O_3). Both effects lead to a higher recombination rate resulting in a higher saturation current. The results of phosphorus implanted samples with SiO_2/SiN_x passivation are also very promising. As can be seen in Table 1, J_0 is between 10 and 15 fA/cm^2, significantly below the 20 to 25 fA/cm^2 measured for the conventional $POCl_3$-diffused FSF profile from Fig. 1b. There is no correlation between phosphorus dose and saturation current. This must be due to the passivation and we assume that the surface recombination velocity, dominating the overall recombination, is weakly influenced by the phosphorus surface concentration for SiO_2 on lowly doped *n*-type silicon as it was already simulated by Altermatt *et al*. [10].

Table 1. Characteristics of the investigated profiles (best values achieved so far). Sheet resistance was measured by 4 point probe on planar reference samples. J_0 was extracted from QSSPC measurements (textured samples for FSF & FFE and planar samples for emitter and BSF) using the high injection method [11].

Sample type	Species	Implanted dose [cm^{-2}]	R_{Sheet} [Ω/sq]	J_0 [fA/cm^2]	Passivation
Floating emitter (FFE)	Boron	1e13	3900	5	Al_2O_3
		3e13	1500	6	
		1e14	650	7	
Front surface field (FSF)	Phosphorus	1e13	2200	12	SiO_2/SiN_x
		3e13	880	15	
		1e14	440	10	
Emitter	Boron	7e14	147	9	Al_2O_3
		1e15	108	22	
		1.5e15	73	24	
Back surface field (BSF)	Phosphorus	3e15	39	370	Al_2O_3

With boron implantation in the range of 1e15 cm^{-2}, an emitter suitable for IBC solar cells can be formed (see Fig. 2a). For the anneal with a high thermal budget applied in this study, the profile depth is around 1 µm with a peak concentration between 1e19 and 3e19 cm^{-3}. The sheet resistance (R_{Sheet}) can be easily adjusted in the range of 70 to 150 Ω/sq by varying the implanted dose with only small changes of the doping profile. Together with an Al_2O_3 passivation we found good electrical properties, i.e. low saturation currents (see Table 1). J_0 increases with increasing boron dose, but stays below 30 fA/cm^2, even for the highest dose applied (1.5e15 cm^{-2}).

For the formation of the phosphorus-doped BSF we investigated a large variety of implanted doses resulting in profiles with sheet resistance ranging from 39 to 240 Ω/sq. Unfortunately, we found a strong injection dependent lifetime for phosphorus surface concentrations around 1e19 cm^{-3} (here, profiles implanted with a dose of 3e14 to 1.5e15 cm^{-2}) which makes it impossible to use the high injection method [11] for the extraction of J_0 from the lifetime curves. This is most probably due to the fixed negative charge in the Al_2O_3 passivation, inappropriate for *n*-doped surfaces [12]. We assume that an injection dependent lifetime will have a negative effect on the fill factor (*FF*) of the solar cell. For the highest phosphorus dose of 3e15 cm^{-3}, the high injection method works, giving J_0 of 370 fA/cm^2. The implied fill factor (*iFF*) extracted from the QSSPC measurement is ~84 % indicating that there are no unusual injection dependent recombination paths. So the *n*-doping seems to dominate over the fixed charges in the passivation. The saturation current of the BSF is quite high, but since the area fraction of the BSF is only around 10 % in the IBC solar cells, the J_0 contribution to the whole solar cell is roughly 37 fA/cm^2.

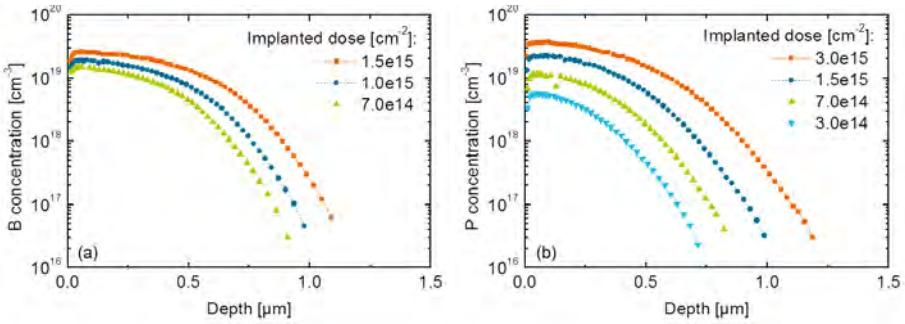

Fig. 2. ECV profiles measured on planar samples after ion implantation and annealing for 80 min at 1050 °C. (a) High dose boron implantations for the emitter; (b) phosphorus implantations for the back surface field.

3.2. IBC solar cells

From the investigations on symmetrical lifetime samples we identified useful parameters to fabricate small area IBC solar cells with an industrial contact pitch of 2.1 mm. The structure is schematically shown in Figure 3a. We choose an implantation dose of 1e14 cm^{-2} for front floating emitter (FFE) and front surface field (FSF) because for this process we expect the best process stability and J_0 appeared to be very similar for the dose variation investigated in the previous section. 2D simulations of the IBC cell with the data from section 3.1 using COMSOL Multiphysics® predict a better fill factor (*FF*) for a boron emitter with lower sheet resistance at costs of the open-circuit voltage (V_{OC}). Since the influence on *FF* is dominant and the overall efficiency should be higher with a stronger boron doping, we applied a boron dose of 1.5e15 cm^{-2} to obtain the emitter with 73 Ω/sq in the solar cell process. The phosphorus BSF was implanted with a dose of 3e15 cm^{-2} (resulting in 39 Ω/sq) to achieve a strong *n*-doping that shows no unusual injection dependent lifetime when being passivated with Al_2O_3.

The best solar cell with a boron doped front floating emitter has a conversion efficiency of 21.8 % (see Fig. 3b). With a V_{OC} of 675 mV, the cell is far below of what would be expected from the J_0 values measured on lifetime samples. Process references showed that the temperature step applied to the finished cells was not sufficient and the passivation could not be fully activated. Unfortunately, aluminum spikes through the emitter lead to a shunt of the pn junction when the cells were tempered at more than 340 °C. A much higher V_{OC} and cell efficiency should be achievable by activating the passivation prior to the metallization.

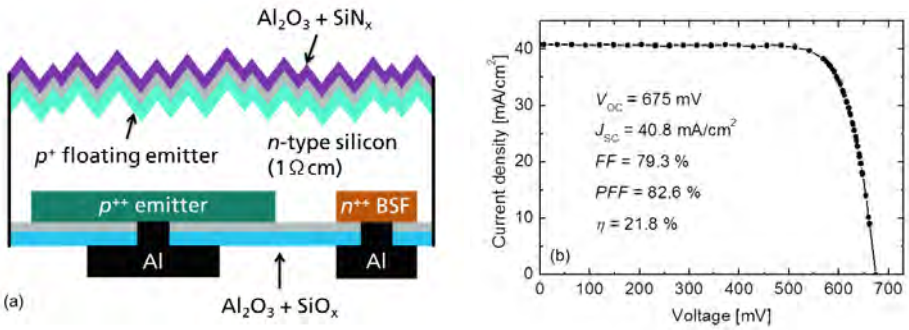

Fig. 3. (a) Cross-sectional sketch of the fabricated IBC solar cells; (b) IV data of the best cell measured in-house. Active cell area is 2 x 2 mm^2, thickness is 200 µm, pitch is 2.1 mm.

Degradation experiments were performed in a sun tester with IBC solar cells featuring a front surface field (FSF) passivated by a SiO_2/SiN_x stack or a front floating emitter (FFE) passivated by an Al_2O_3/SiN_x stack. The measurement of IV-data after 36 h exposure to UV-light shows that the cell with FSF degrades strongly, i.e. the current drops to half of its initial value reducing the efficiency from 20.9 to 9.6 % (see Table 2). The cell with FFE is much more stable, but is still losing ~1 % absolute in efficiency. The effect of degradation under UV-illumination has been observed on symmetrical lifetime samples, too. For the FSF, the effective lifetime at a minority carrier density of 1e15 cm^{-3} dropped by 50 to 85 % while the FFE samples remained at an almost constant lifetime level and lost only 2 to 12 %.

It is known that the SiO_2 passivation degrades under UV-illumination [5] and Granek *et al*. observed a similar strong degradation of IBC cells but only for cells without front surface field [6]. Note that the overall degradation for the FSF samples shown here is stronger than what has been observed by Granek *et al*., but this might be due to the fact that we used a ~1.5 times higher UV-illumination intensity. The degradation of the cells investigated by Granek *et al*. was efficiently suppressed by using a quite strong doping on the front side (FSF with ~150 Ω/sq) and

explained by the weaker dependence on the surface recombination velocity in case of a FSF underneath the passivation [6]. Hence, we conclude that a weaker FSF which can be formed by ion-implantation as shown in this study in fact enables lower J_0 values but becomes more sensitive to the surface passivation quality, especially under UV-illumination.

Table 2. Degradation of IBC solar cells under UV-illumination in a sun tester for 36 h at 500 W/m^2.

Front side	State	V_{OC} [mV]	J_{SC} [mA/cm^2]	FF [%]	η [%]
Front surface field (FSF)	before UV exposure	672	39.2	79.6	20.9
	after UV exposure	612	19.8	79.3	9.6
Floating emitter (FE)	before UV exposure	673	39.9	77.3	20.7
	after UV exposure	668	38.2	76.7	19.6

To investigate the cell performance under low level illumination, we measured IV-data with optical filters placed above the solar cells prior to the degradation experiment described above. The resulting illumination intensities were determined by measuring the current of a calibrated reference cell. Those optical filters might have some influence on the spectrum of the incident light, but since we compare two similar cells, this should be of minor importance. In Figure 4 the short-circuit current and open-circuit voltage are plotted against the illumination intensity for a FSF and FFE cell. In both cases the short-circuit current (J_{SC}) shows a similar dependence on the amount of incoming photons that can be well described by a linear fit. Neglecting series and parallel resistances, the one-diode equation evaluated at open-circuit conditions

$$J_{SC} = J_0 \times \left(\exp\left(\frac{V_{OC} \cdot q}{n \cdot k_B \cdot T} \right) - 1 \right) \tag{1}$$

with elementary charge q, ideality factor n, Botzmann constant k_B and temperature T implies a logarithmic dependence of V_{OC} on J_{SC}. The logarithmical fit to the measured V_{OC} values in Fig. 4b is a quite good indication that the solar cell performance under low level injection is ideal down to at least 0.01 suns. FSF and FFE show a very similar behavior, not only in J_{SC} and V_{OC} but in FF and efficiency as well (not shown here). This is in contradiction with a former publication where p-type IBC cells with a front floating emitter were investigated [7]. Granek *et al.* found a pronounced non-linearity for illumination intensities lower than 0.5 suns and explained this effect by an internal shunt element across the floating junction. It is still unclear whether this effect is present in the n-type IBC solar cells fabricated with ion implantation, but if so, it must be much weaker because it is not visible in the IV data down to 0.01 suns shown here.

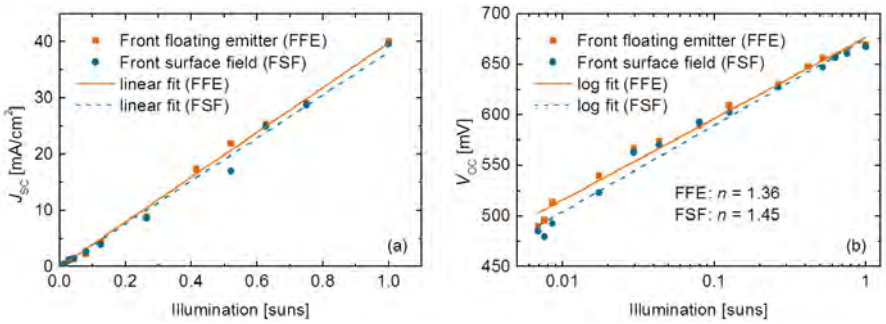

Fig. 4. Comparison of front surface field (FSF) and front floating emitter (FFE) under low level illumination (a) Short-circuit current (J_{SC}) with linear fit; (b) Open-circuit voltage (V_{OC}) with logarithmic fit corresponding to the one-diode equation.

4. Conclusion

Ion implantation is suitable to form lowly doped regions acting as front surface field (FSF) or front floating emitter (FFE) in *n*-type IBC solar cells. Very low saturation current densities (J_0) in the range of 10 to 15 fA/cm^2 have been achieved for textured FSF samples passivated with a SiO_2/SiN_x stack. These weak profiles strongly depend on the surface recombination velocity and therefore suffer from UV-illumination degrading the SiO_2 passivation quality. For textured FFE samples, J_0 values down to 5 fA/cm^2 were measured with an Al_2O_3 passivation. This configuration turned out to be quite stable against UV-irradiation. The sheet resistance of boron emitter and phosphorus BSF can be easily adjusted by the implanted dose. Al_2O_3 passivation works well on the boron doped emitter, but for the phosphorus BSF it was found that a surface concentration higher than 3e19 cm^{-3} is necessary to from a suitable BSF and avoid a weird injection dependence of the effective lifetime.

Fully ion implanted and co-annealed IBC solar cells with an Al_2O_3 passivation on both sides featuring a weakly boron doped front floating emitter (FFE) were successfully fabricated ($\eta = 21.8$ %). It is known that the SiO_2/Si surface recombination velocity increases under UV-illumination [5]. This degradation effect has been identified at lifetime and cell level because the FSF doping used in this study is very weak and therefore very sensitive to the surface passivation. The efficiency of FSF cells dropped dramatically by more than 50% while the FFE cells lost only about 1 % absolute. IV measurements at different illumination intensities revealed a linear dependence of J_{SC} on the injection level for both, FSF and FFE cells. For illumination intensities down to 0.01 suns, no significant influence of an internal shunt element across the floating junction [7] on the IV data was observed.

Acknowledgements

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Attachment K-11

INFLUENCE OF REAR-SIDE PASSIVATION ON SOLAR CELL PERFORMANCE OF BOSCO SOLAR CELLS

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ABSTRACT: The recently introduced BOSCO ("Both Sides Collecting and Contacted") solar cell exhibits emitter regions on front and rear side, which are interconnected by diffused vias. This allows double-sided collection of carriers in the base and bifacial operation while supporting standard module interconnection technology. Since the BOSCO cell's rear side exhibits *p*-doped as well as highly n^+-doped surfaces the dielectric used as rear-side passivation needs to be suitable to passivate both polarities. This work compares the passivation of the BOSCO cell's rear side by a PECVD aluminium oxide (AlO_x) and a thermally grown silicon oxide (SiO_2). A difference in efficiency of up to $\Delta\eta = 0.5\ \%_{abs}$ occurs between BOSCO cells with AlO_x and SiO_2 passivation, with the AlO_x passivated solar cells achieving better cell performance. The difference in efficiency is dominated by a loss in fill factor of up to $\Delta FF = 1.6\ \%_{abs}$ for cells with SiO_2 passivation compared to AlO_x passivated cells. An investigation of the suns-V_{oc} characteristics shows that this loss is mainly caused by increased recombination at lower injection, which strongly affects the pseudo fill factor. This work shows that the choice of rear-side passivation is essential to optimize the performance of BOSCO solar cells.

Keywords: BOSCO, bifacial, passivation, double-sided collection, multicrystalline silicon

1 INTRODUCTION

The BOSCO ("*Bo*th *S*ides *CO*llecting and *CO*ntacted") solar cell [1, 2] features a double-sided emitter and a grid on both sides as sketched in Fig. 1. The front- and rear-side emitter areas are interconnected by diffused vias. For the rear-side contact grid the emitter is disconnected. The double-sided emitter allows carrier collection on either side and, therefore, supports the use of lower diffusion length material such as multicrystalline silicon (mc-Si) [2]. Furthermore, the layout of the front- and rear-side grid allows for bifacial application while supporting standard module interconnection technology. Compared to Al-BSF cells a significant advantage in monofacial efficiencies has been demonstrated [2, 3]. Furthermore, it has been shown that the BOSCO cell concept is a promising candidate to enable bifacial application also for low-to-medium diffusion length material such as mc-Si [2, 3]. A principle process flow of the BOSCO cell concept with a complexity similar to a typical PERC processing route has been introduced [3]. Due to the interdigitated structure of the rear-side emitter and base regions, the passivation layer deposited on the rear side has to passivate both a *p*-type and a highly-doped n^+-type surface. Thin thermal silicon oxide (SiO_2) films capped with silicon nitride have been shown to achieve low surface recombination velocities on the rear side of *p*-type PERC cells [4], simultaneously achieving low front-side n^+-type emitter recombination [4]. Therefore, SiO_2 seems to be a promising candidate for the passivation of BOSCO cells, where *p*-type and highly doped n^+-type surfaces need to be passivated by the same layer. Aluminium oxide (AlO_x) deposited by plasma-enhanced chemical vapour deposition (PECVD) is known to be well-suited for the passivation of *p*-type doped silicon [5], due to a low interface defect density and fixed negative charges at the interface. Furthermore, PECVD AlO_x has been reported to yield good passivation quality on n^+-emitters [6].

In this work, we compare thin thermally grown SiO_2 and PECVD AlO_x for the use as rear-side passivation of BOSCO cells.

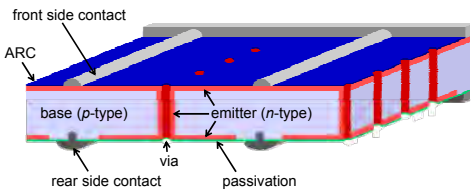

Figure 1 Sketch of the BOSCO cell structure. Illustration is taken from Ref. [2]

2 EXPERIMENTAL

For this work, BOSCO cells processed on 15.6×15.6 cm^2 block-cast mc-Si wafers with varying base resistivity and purity are investigated. The investigated materials include upgraded metallurgical-grade (UMG) Si with a feedstock purity of 5N (i.e., 99.999 % pure silicon) as well as electronic-grade (EG) Si with a purity of 9N.

Fig. 2 depicts the process flow for the BOSCO cells with a variation of the rear-side passivation layer. The key properties of the BOSCO process are described in Ref. [3]. Prior to surface texturing, vias are drilled using an IR laser. After a rear side polish, which may not be needed once the BOSCO process is optimized for bifacial illumination, a diffusion barrier is deposited in order to

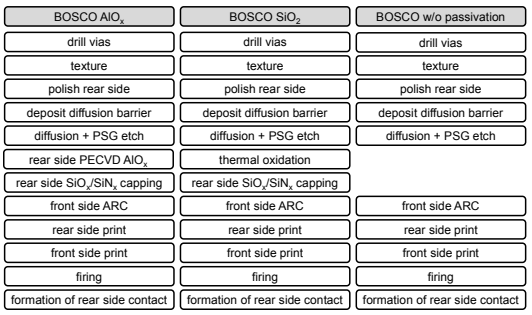

Figure 2 Principle process flow for the production of BOSCO solar cells with a variation of the passivation schemes.

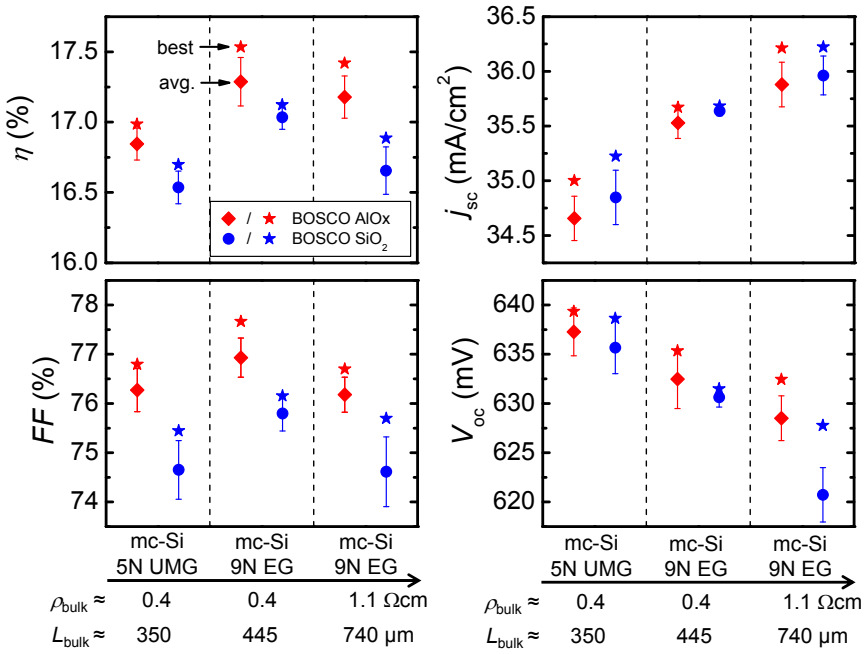

Figure 3 Illuminated *I-V* parameters for front-side illumination of the processed BOSCO cells with AlO_x and SiO_2 rear-side passivation. The cells have been measured on a non-reflecting chuck. Cell areas are A_{cell} = 15.6 × 15.6 cm^2.

obtain the structured emitter on the rear side. In this experiment, the diffusion barrier is formed by a PECVD silicon oxide (SiO_x) with a screen-printed etch resist lacquer and subsequent wet chemical oxide etch-off and stripping of the lacquer. After the diffusion, the diffusion barrier is removed in the PSG etch. The rear-side passivation has been varied between

(i) PECVD AlO_x,
(ii) thermally grown SiO_2 and
(iii) no rear-side passivation at all.

The thin SiO_2 film is thermally grown during an oxidation process at a plateau temperature of 800°C in an inline walking string furnace [7]. Note that for this group the front-side emitter is passivated with SiO_2 as well. Both passivation layers, the AlO_x and the SiO_2, are stacked with a capping layer consisting of a PECVD SiO_x and a PECVD silicon nitride (SiN_x). On the front side, a PECVD SiN_x is deposited as an anti-reflective coating (ARC). For the cells passivated with SiO_2, the thickness of the ARC is adapted considering the thin SiO_2 layer which is deposited on the front side as well. After screen printing of the rear and front side and subsequent firing, the rear-side contact is formed with laser-fired contacts (LFC) [8, 9].

3 IMPACT ON CELL PERFORMANCE

3.1 *I-V* parameters

Illuminated *I-V* parameters have been measured under front-side illumination on a non-reflecting chuck. The results for the passivated cells are shown in Fig. 3, the results for cells without passivation will be discussed later within the fill factor analysis. On all materials, cells with AlO_x passivation yield higher efficiencies than cells passivated with SiO_2. The difference in-between both groups is $\Delta\eta$ = 0.3 to 0.5 $\%_{abs}$ or $\Delta\eta$ = 1.5 to 2.1 $\%_{rel}$, respectively. For the UMG Si cells with AlO_x passivation, the open-circuit voltage is increased by ΔV_{oc} = 0.3 $\%_{rel}$ and the short-circuit current density is reduced by Δj_{sc} = -0.6 $\%_{rel}$, while the fill factor is increased by ΔFF = 1.8 $\%_{rel}$ compared to cells with SiO_2 passivation. For the EG Si materials, the fill factor is increased by ΔFF = 1.5 $\%_{rel}$ for the low resistivity and by ΔFF = 3.0 $\%_{rel}$ for the high base resistivity material, respectively, both representing the dominant difference in the *I-V*-parameters between AlO_x and SiO_2 passivated cells. Therefore, the lower efficiency of the cells with SiO_2 passivation compared with AlO_x passivation can mainly be attributed to losses in fill factor for all materials.

3.2 Fill factor and suns-V_{oc} analysis

In order to investigate the differences of the groups in fill factor in more detail, the pseudo fill factor and the fill factor differences between the pseudo fill factor and the ideal fill factor FF_0 will be investigated. Series resistances are assumed to be lumped in this analysis so that the *pFF* can be considered to be free from losses due to series resistances [10]. The ideal fill factor is calculated from the ideal *I-V*-curve and is therefore free from losses due to series resistance and recombination in the space charge region [10, 11]. Hence, the fill factor difference FF_0-*pFF* quantifies fill factor losses due to recombination in the space charge region and low shunt resistances [10].

Fig. 4 shows the pseudo fill factor and the fill factor difference FF_0-*pFF* of BOSCO cells with AlO_x and SiO_2 passivation, respectively, and BOSCO cells without any rear-side passivation. On all materials, cells with AlO_x passivation yield the highest *pFF* and the lowest values

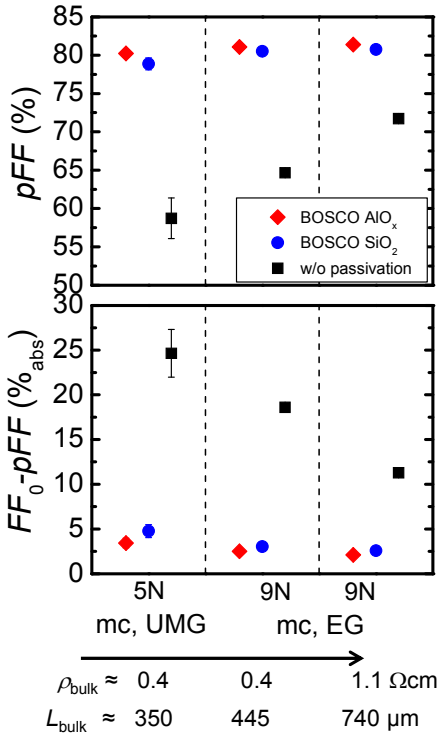

Figure 4 Pseudo fill factor and fill factor difference between ideal fill factor and pseudo fill factor for all materials and cells with AlO_x, SiO_2 and without passivation.

for FF_0-pFF. The difference in pseudo fill factor to cells with SiO_2 passivation is $\Delta pFF = 0.6\ \%_{abs}$ for the EG Si materials and $\Delta pFF = 1.4\ \%_{abs}$ for the UMG Si material. Therefore, the fill factor difference FF_0-pFF of the cells with AlO_x passivation is decreased by $\Delta(FF_0\text{-}pFF) = 0.5$ and $1.3\ \%_{abs}$ for the EG Si and the UMG-Si, respectively, compared to the cells with SiO_2 passivation. For the cells without passivation the pFF is drastically decreased to $pFF = 71.7\ \%$ for the high resistivity and $pFF = 64.7\ \%$ for the low resistivity EG-Si, respectively, and $pFF = 58.7\ \%$ for the UMG-Si material. In this case, the pFF is affected by very low shunt resistances of $R_p < 200\ \Omega cm^2$ which are observed on all materials for cells without rear-side passivation.

To analyze the influence of the passivation on pFF in more detail, suns-V_{oc} characteristics [12] of the cells passivated with AlO_x and SiO_2 and the cells without passivation are compared. In Fig. 5 suns-V_{oc} characteristics of a representative BOSCO cell for each material passivated with AlO_x, SiO_2 and no passivation are shown. For illumination levels below $E = 0.1$ suns, the open-circuit voltage for cells passivated with SiO_2 drops more strongly than for cells with AlO_x passivation. Hence, the recombination for low illumination levels is higher for cells with SiO_2 passivation than for cells with AlO_x passivation. In case of the cells without passivation, the recombination is even higher, leading to a strong drop in V_{oc} at illumination intensities below $E \approx 0.3$ suns.A possible explanation for this behavior might be re-injection of electrons at the rear-side *pn*-junction, that causes an enhanced sensitivity of cell performance to the

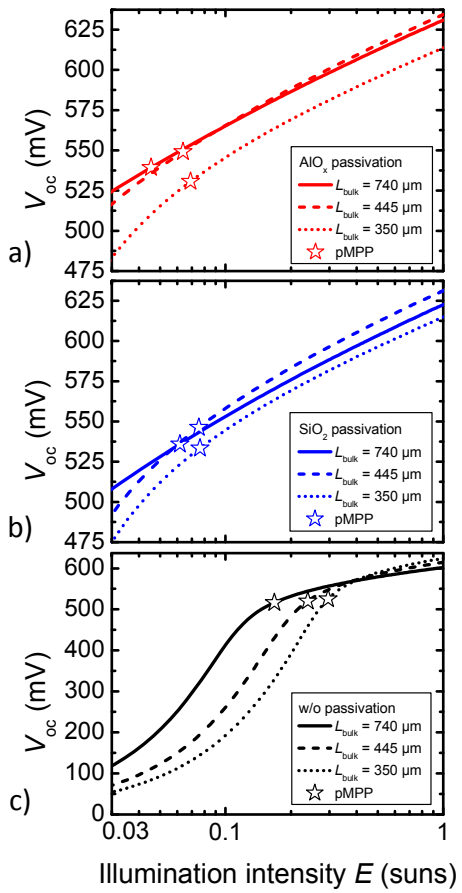

Figure 5 Suns-V_{oc} curves of BOSCO cells with a) AlO_x passivation b) SiO_2 c) without passivation.

passivation quality of the rear-side passivation. Further investigations are on-going.

4 CONCLUSION

Solar cell results on mc-Si materials with an AlO_x and a SiO_2 passivation on the rear side have been presented. The cells passivated with AlO_x exhibit the highest efficiencies with a difference in efficiency of $\Delta\eta = 0.3$ to $0.5\ \%_{abs}$ compared to cells with SiO_2 passivation. The difference in efficiency is mainly attributed to a loss in fill factor. An in-depth analysis of the pseudo fill factor via discussion of the suns-V_{oc} characteristics shows that the pseudo fill factor of the cells with SiO_2 passivation is strongly affected by an inferior passivation quality, due to increased recombination in the cell at low illuminations levels. Therefore, we identify AlO_x as the superior passivation for the BOSCO cell concept.

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Novel Low Pressure Sputtering Source and Improved Vacuum Deposition of Small Patterned Features Using Precision Shadow Masks

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ABSTRACT

A novel low-pressure sputtering source (LPSS) has been successfully used to deposit crisp, well-defined 10-µm-and-larger features using precision shadow masks. The LPSS operates at low pressure yielding viable deposition rates and low thermal exposure of the mask and allows sputter deposition from both the top and bottom cathode surfaces. The LPSS design has been scaled to a large area 6" × 32" source that enables efficient additive manufacturing of embedded electronic devices, circuits, and systems using precision shadow masks.

INTRODUCTION: A NOVEL SPUTTERING SOURCE TECHNOLOGY

This paper reports on the collaborative work of Advantech U.S., Inc., and the Kurt J. Lesker Company on a novel thin-film deposition technology for embedded electronic components and circuits. The novel low-pressure sputtering source (LPSS) is suitable for deposition of fine-pattern thin films using precision shadow masks.

TODAY'S SHADOW MASK TECHNOLOGY

Deposition of thin films through precision shadow masks bridges a highly desired feature size range for electronic devices and components. The traditional integrated circuit (IC) manufacturing industry typically patterns device features from 1 µm down into the nanometer range. The printed circuit board (PCB) industry works with feature sizes from 50 µm (2 mils = 0.002") to hundreds of millimeters.

Both the IC and PCB industries use photolithography – on different length scales – and subtractive processing steps to pattern their substrates.

In contrast, the evaporative printing process developed by Advantech enables complete additive manufacturing of electronic devices and circuits with feature sizes and spacing between 5µm and several cm, bridging the feature size gap between the IC and the PCB manufacturing industries (Figure 1). Fine line interconnects, interposers, vias, passive embedded devices such as resistors, parallel plate capacitors, gap filters, inductors, antennas, and so on, as well as MOSFETs, logic gates, and active matrix display backplanes have been built with this technique. The process uses an in-line multi-chamber vacuum deposition system. No wet chemical process steps are required in the device deposition or patterning operations. The evaporation printing process deposits thin films with near-bulk material properties and performance using physical vapor deposition on a wide variety of substrates – display-grade rigid or flexible glass, advanced circuit board substrates, plastic or metal foils. The resulting devices, circuits, and board layers can be used directly in traditional PCB lamination, bonding, or solder processes.

THIN FILM DEPOSITION THROUGH SHADOW MASKS

Figure 2 depicts the arrangement for physical vapor deposition (PVD) of patterned thin films through a shadow mask in a vacuum deposition system.

The thin film material originates at the source and is turned into a vapor flux using a thermal evaporator, an e-beam evaporator, or a sputter source inside a vacuum chamber. The substrate opposes the material source at a distance T above the source. A shadow mask is placed parallel to the substrate facing the materials source, aligned to the substrate, and brought into close contact with the substrate.

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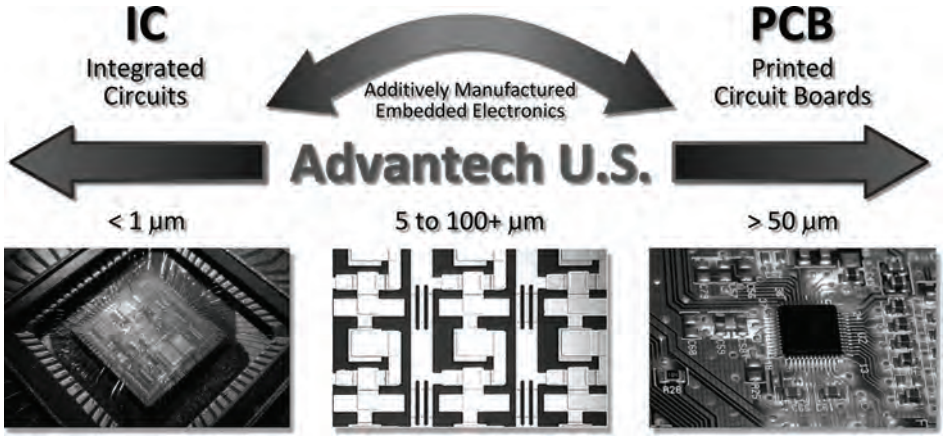

Figure 1. Bridging The Gap – Typical feature sizes in integrated circuit manufacturing, evaporation printing, and printed circuit board technology.

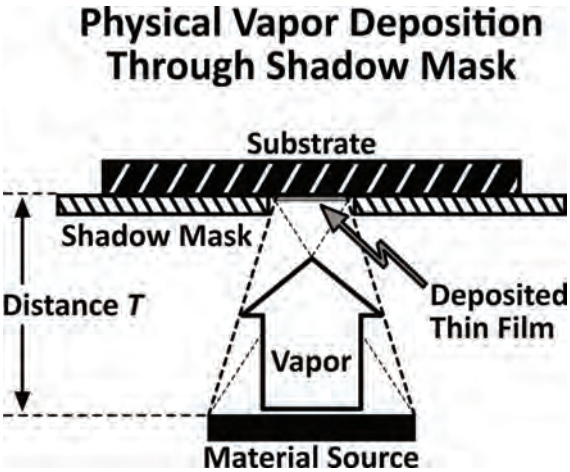

Figure 2. Physical vapor deposition (PVD) through a shadow mask in line-of-sight conditions.

Precision shadow masks, also referred to as "Fine Metal Masks (FMM)," are made from a thin foil such as nickel or stainless steel. Typical foil thickness ranges from 10 to 25 µm. Small openings or apertures are created through chemical or laser etching. For highest resolution the foil is made by an electroforming process. The aperture pattern is first produced using a photoresist exposure process, where resist is left on the forming mandrel in any area that forms an aperture. Aperture dimensions of 10 µm and less have been produced reliably using this method. (Figure 3).

The shadow masks are mounted on rigid mask frames designed for the automated mask storage, handling, and alignment system. Positional accuracy of the shadow mask is verified prior to and during the mounting process using a vision measurement machine (VMM).

In the deposition process the mask is first placed between the evaporation source and the substrate. Advantech uses a high precision alignment system to align the mask to fiducial marker patterns on the substrate and places the mask within 1 µm of its desired position. This allows the use of multiple masks to create complex patterns and/or deposit different materials to build complete electronic circuits.

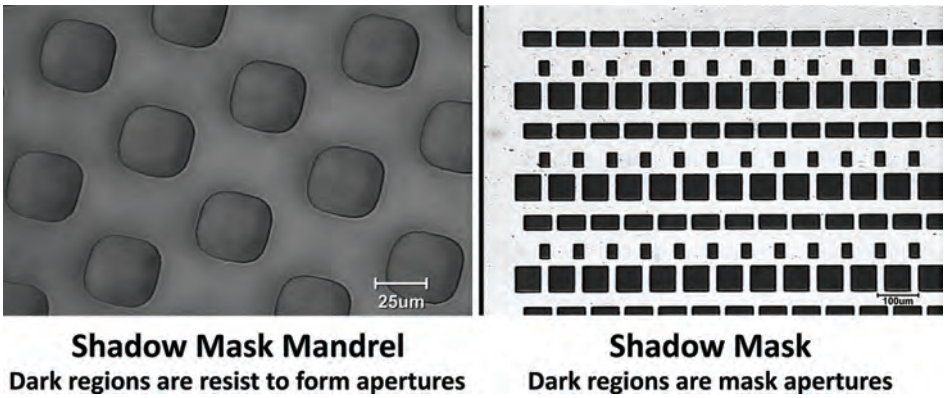

Figure 3. Shadow mask mandrel (left) and electroformed nickel shadow mask (right).

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After alignment the mask is brought into direct contact with the substrate to avoid any shadowing effect (also described as overspray). When magnetic materials are used for the mask, such as nickel foil, a magnet behind the substrate can enhance the contact between mask and substrate.

The desired material is then deposited onto the substrate/mask combination. After the deposition process is completed and the mask is removed the desired pattern remains on the substrate.

SHADOW MASKS LIMITATIONS: THERMAL EXPANSION

A critical factor determining the geometrical precision of the deposited thin film pattern is the position accuracy of the shadow mask relative to the substrate during the duration of the deposition process. In particular, heat imposed by the material source on the shadow mask and substrate can result in poor quality of the deposited features.

The shadow mask material is subject to thermal expansion when exposed to heat from the deposition source. Absolute positions of the aperture patterns relative to the substrate will deviate from the desired deposition locations due to thermal expansion of the mask material and mask frame. Positions of apertures relative to each other on the mask are likewise affected by thermal expansion and the method of mounting the shadow mask on the frame, as well as the method of mounting the mask and frame relative to the substrate. Similarly, the substrate experiences thermal expansion by heating imposed by the material source. These thermal mask expansion effects result in a positional offset of the deposition pattern from the desired deposition position, often compromising the device's functionality.

Besides dimensional instability thermal expansion can also lead to buckling and unintended separation between mask and substrate. Any separation between mask and substrate leads to shadow deposits or overspray, as illustrated in Figure 4.

Thermal management therefore is essential to prevent any of the aforementioned shortcomings. Pre-stressing the mask, for example, allows for some compensation of heat-up, as does proper timing of the deposition sequence.

REQUIREMENTS FOR HIGH DEFINITION OF FINE FEATURES

PVD occurs in a vacuum vessel that is typically evacuated to a base pressure low enough to enable vapor species transport with a mean free path λ exceeding the source/substrate distance T > λ. Under such conditions, the vapor path between the source and the substrate approximates line-of-sight conditions, indicated by the dashed lines in Figure 4. For a base pressure of 1×10^{-3} Pa the mean free path is approximately 50 m, significantly larger than the source/substrate distance *T*.

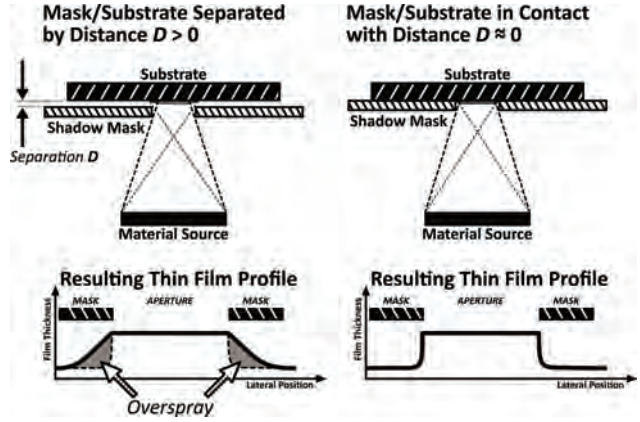

Figure 4. Thin film height profile for deposition with shadow mask separated by distance *D* from substrate (left) and shadow mask in close contact with substrate (right).

Generally, physical vapor deposition (PVD) by evaporation is suitable for producing sharp, well-defined features in thin films deposited through ideal shadow masks. This is the case in particular if the source resembles a point source such as thermal or e-beam evaporator at an appropriate distance from the mask/substrate arrangement and the base pressure can be held below 1×10^{-2} Pa.

A difficulty for evaporation processes lies in the limitation of size for the source as well as the selection of materials that can be evaporated from either thermal or e-beam sources. Some refractory metals, for example, require fairly high evaporation temperatures. The undesired side effect of evaporation at such high temperatures is the heat transfer generated by radiation.

SPUTTER DEPOSITION THROUGH SHADOW MASK

Sputtering offers an enhanced selection of materials that can be vacuum deposited as thin films on many types of substrates. Traditional sputter deposition, however, requires a chamber pressure of 1 to 10 Pa or even higher. In this pressure range the mean free path of sputter species is reduced to 0.05 m and less. For shadow mask deposition, however, it is impossible to place a sputter source this close to the mask

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to achieve more or less line-of-sight deposition and creation of sharp and defined features. The close proximity results in a coupling of the sputter plasma into the metal mask, and the electron current into the mask creates an unacceptable heat load in the mask, resulting in the aforementioned problems.

Increasing the distance between sputter source and mask and the reduced mean free path in this pressure regime results in frequent gas phase collisions of the sputtered vapor and the ambient gas molecules, and this creates non-line-of-sight deposition conditions. Patterns deposited by conventional sputtering through a shadow mask are broadened and blurred compared to evaporative physical vapor deposition (Figure 5).

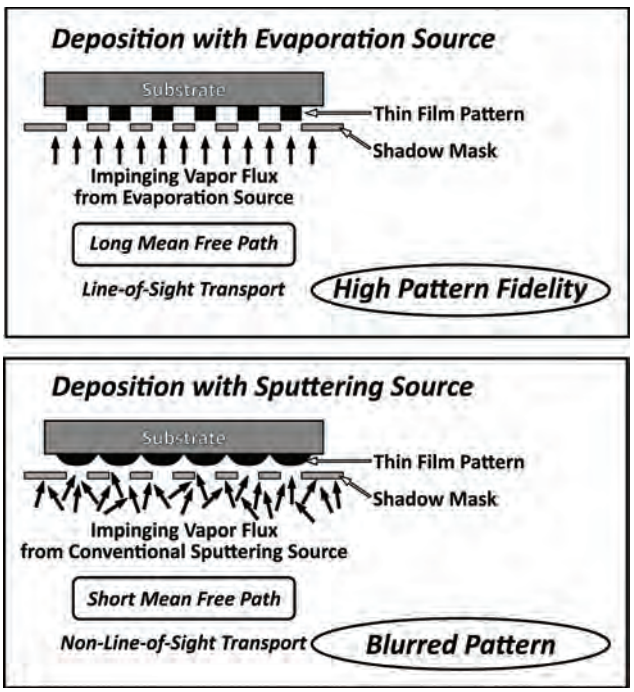

Figure 5. Evaporation (top) and conventional sputter deposition (bottom) through shadow mask and resulting feature height profiles.

RESULTS: LOW-PRESSURE SPUTTERING SOURCE

Advantech U.S., Inc., employed a novel low-pressure sputtering source (LPSS) developed by the Kurt J. Lesker Company that sustains stable operation at a pressure as low as 0.01 Pa (7.5×10^{-5} Torr).

The low pressure operation results in an increase of the mean free path to about 0.5 m, which allows sufficient separation between mask and sputter source to prevent coupling of plasma into the metal mask.

Figure 6 shows a top view and side view of the first-generation prototype of the LPSS. The horizontally mounted aluminum (AL) cathode body holds three integrated rod magnets and water cooling lines. The magnetic field lines wrap around the entire cathode body, creating an electron race track around the entire source. The LPSS source sputters material from both the top and bottom surfaces, consuming the cathode body.

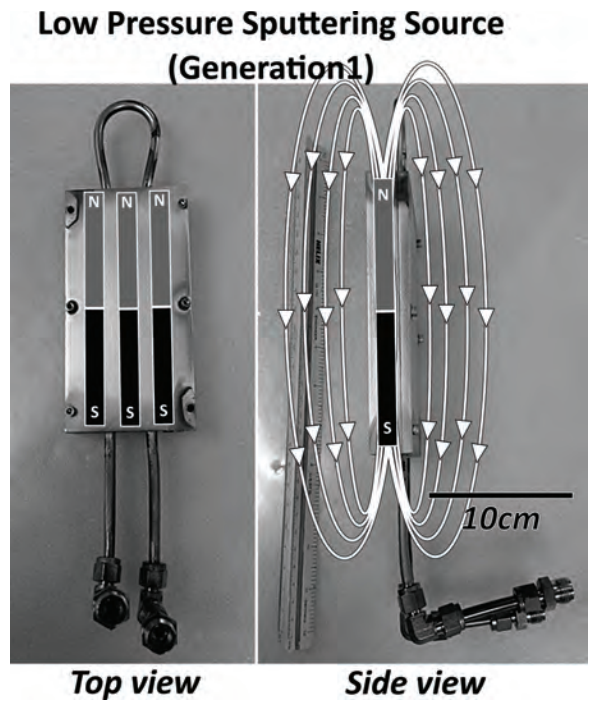

Figure 6. Low-pressure sputtering source Gen 1 prototype 8.9 cm × 19 cm (3.5″ × 7.5″) with magnet arrangement.

Figure 7 shows the voltage over pressure curve of a conventional magnetron sputtering source (triangle symbols on dashed curve) compared to the LPSS (circle symbols on

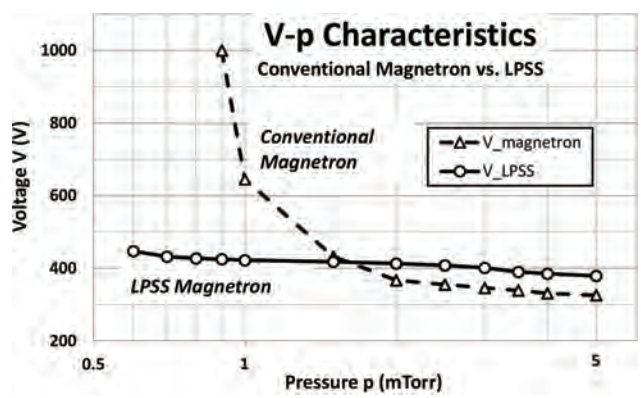

Figure 7. Voltage-pressure curves for conventional (dashed lines) and LPSS sputtering source (solid lines). The LPPS exhibits stable operation pressures below 12 Pa (1 mTorr) similar to cylindrical post magnetron sources [1]

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solid curve).Transport rates achieved with the LPSS are comparable to conventional sputtering sources. The LPSS achieves power densities that exceed those of conventional sputtering sources by one or two orders of magnitude. The original Gen 1 LPSS prototype was sized 8.9 cm × 19 cm (3.5" × 7.5") (Figure 6), the second-generation LPSS features 15.2 cm × 40.6 cm (6" × 16") and 15.2 cm × 81.3 cm (6" × 32") cathodes for large area deposition (Figure 8). The Gen 2 LPSS cathodes are mounted on a linear scanning stage to accommodate deposition on substrates as large as 61 cm × 91 cm (24" × 36").

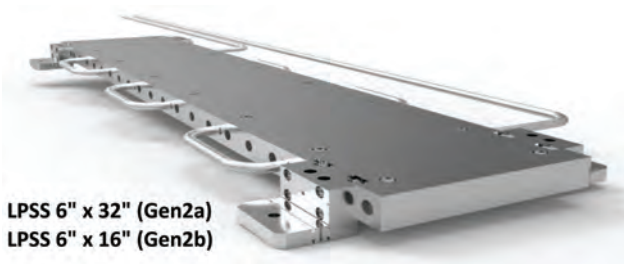

Figure 8. Second-generation large-area low-pressure sputtering source (LPSS) with 40.6 cm (16″) and 81.3 cm (32″) (shown) length.

MASKED THIN FILM DEPOSITION RESULTS USING NOVEL LOW-PRESSURE SPUTTERING SOURCE

Figure 9 shows the height profiles (lower graph) of 100-µm-wide features deposited through the same 20-µm-thick shadow mask using a conventional magnetron sputtering source (solid grey profile) and the Gen 1 LPSS in stationary mode (dashed black profile), both with 15.2 cm (6") target-substrate distance. The two upper images in Figure 9 are shadow masks with 60-µm and 70-µm features. LPSS deposition of the 800-Å-thick film from an aluminum target occurred at a chamber base pressure of 1×10^{-3} Pa and sputter pressure of 0.28 Pa under 2.5 sccm Ar flow with a DC power of 37 W at 467 V with a 15 min deposition duration. The LPSS-sputtered features replicate the mask aperture dimensions, whereas the features deposited with the conventional magnetron source exhibit a rounded profile that does not entirely fill the width of the 100-µm-wide shadow mask aperture.

Figure 10 shows a pattern of 10-µm-wide features deposited through a shadow mask with the 40.6 cm (16") Gen 2 LPSS source at 16.5 cm (6.5") target-substrate distance. The height profile of the features are crisp and well defined. It is worth noting that the profile was acquired with a 12.5-µm stylus which created to the rounded top edge shape.

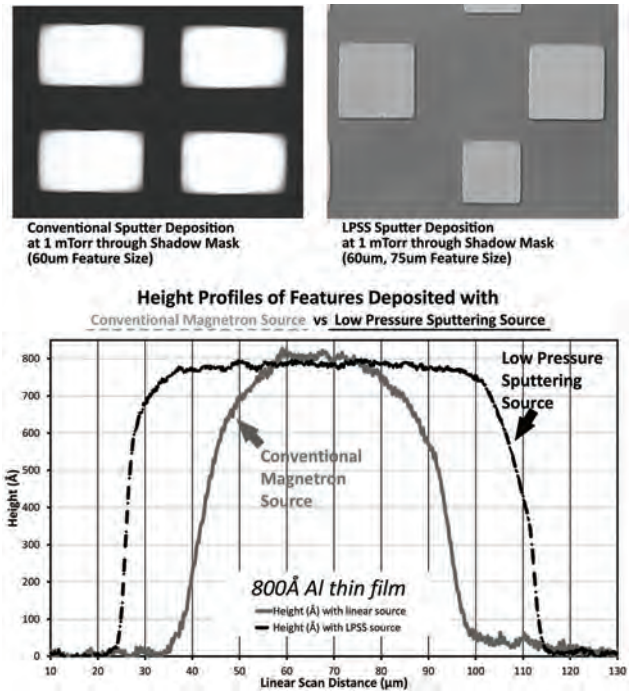

Figure 9. Shown in the lower graph is a comparison of 100-µm features and their height profiles deposited by two different sources. One profile was deposited with a conventional sputtering source (grey solid line); the other profile was deposited by the Gen 1 LPSS (black dashed line). The LPSS deposition shows a sharper, more well-defined deposited feature as compared to conventional sputtering The upper images in this figure are of 60 µm, 70 µm feature shadow masks.

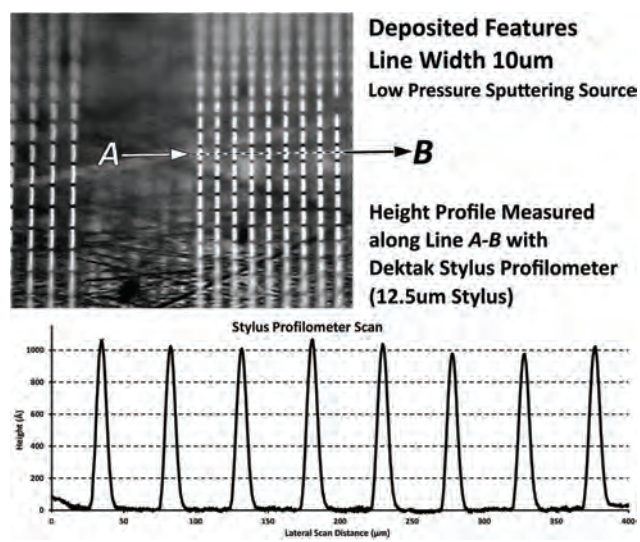

Figure 10. Height profile of 10 µm features deposited with LPSS through a shadow mask. The top image shows the deposited pattern. The bottom graph shows the surface profilometer scan from A to B, using a 12.5 µm stylis. The LPSS deposition yields sharp, well-defined features.

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CONCLUSIONS

The novel low-pressure sputtering source (LPSS) has been successfully used to deposit crisp, well-defined 10-µm-and-larger features using precision shadow masks. The LPSS operates at low pressure yielding viable deposition rates and low thermal exposure of the mask and allows sputter deposition from both the top and bottom surfaces.

The 17.8 cm (7") LPSS prototype was scaled to 40.6 cm (16") and 81.3 cm (32") and succeeded in low pressure operation and deposition of sharp, well-defined features in stationary and scanning conditions. To date, aluminum, copper, and several refractory metals have been successfully deposited with the LPSS sources.

A patent application has been filed, and a production-ready cathode design is being evaluated while the source material portfolio is expanded.

The cost- and process-efficient LPSS technology opens new avenues for the additive manufacture of embedded electronic devices, circuits, and systems patterned by shadow masks, using advanced thin film materials.

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ABSTRACT

A novel low-pressure sputtering source (LPSS) has been successfully used to deposit crisp, well-defined 10-µm-and-larger features using precision shadow masks. The LPSS operates at low pressure yielding viable deposition rates and low thermal exposure of the mask and allows sputter deposition from both the top and bottom cathode surfaces. The LPSS design has been scaled to a large area 6" × 32" source that enables efficient additive manufacturing of embedded electronic devices, circuits, and systems using precision shadow masks.

INTRODUCTION: A NOVEL SPUTTERING SOURCE TECHNOLOGY

This paper reports on the collaborative work of Advantech U.S., Inc., and the Kurt J. Lesker Company on a novel thin-film deposition technology for embedded electronic components and circuits. The novel low-pressure sputtering source (LPSS) is suitable for deposition of fine-pattern thin films using precision shadow masks.

TODAY'S SHADOW MASK TECHNOLOGY

Deposition of thin films through precision shadow masks bridges a highly desired feature size range for electronic devices and components. The traditional integrated circuit (IC) manufacturing industry typically patterns device features from 1 µm down into the nanometer range. The printed circuit board (PCB) industry works with feature sizes from 50 µm (2 mils = 0.002") to hundreds of millimeters.

Both the IC and PCB industries use photolithography – on different length scales – and subtractive processing steps to pattern their substrates.

In contrast, the evaporative printing process developed by Advantech enables complete additive manufacturing of electronic devices and circuits with feature sizes and spacing between 5µm and several cm, bridging the feature size gap between the IC and the PCB manufacturing industries (Figure 1). Fine line interconnects, interposers, vias, passive embedded devices such as resistors, parallel plate capacitors, gap filters, inductors, antennas, and so on, as well as MOSFETs, logic gates, and active matrix display backplanes have been built with this technique. The process uses an in-line multi-chamber vacuum deposition system. No wet chemical process steps are required in the device deposition or patterning operations. The evaporation printing process deposits thin films with near-bulk material properties and performance using physical vapor deposition on a wide variety of substrates – display-grade rigid or flexible glass, advanced circuit board substrates, plastic or metal foils. The resulting devices, circuits, and board layers can be used directly in traditional PCB lamination, bonding, or solder processes.

THIN FILM DEPOSITION THROUGH SHADOW MASKS

Figure 2 depicts the arrangement for physical vapor deposition (PVD) of patterned thin films through a shadow mask in a vacuum deposition system.

The thin film material originates at the source and is turned into a vapor flux using a thermal evaporator, an e-beam evaporator, or a sputter source inside a vacuum chamber. The substrate opposes the material source at a distance *T* above the source. A shadow mask is placed parallel to the substrate facing the materials source, aligned to the substrate, and brought into close contact with the substrate.

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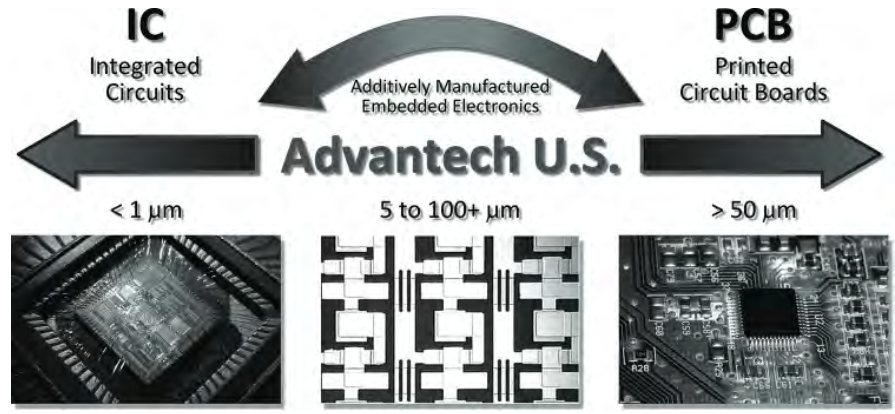

Figure 1. Bridging The Gap – Typical feature sizes in integrated circuit manufacturing, evaporation printing, and printed circuit board technology.

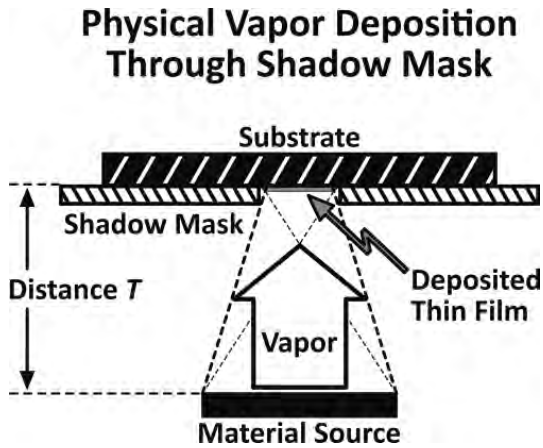

Figure 2. Physical vapor deposition (PVD) through a shadow mask in line-of-sight conditions.

Precision shadow masks, also referred to as "Fine Metal Masks (FMM)," are made from a thin foil such as nickel or stainless steel. Typical foil thickness ranges from 10 to 25 µm. Small openings or apertures are created through chemical or laser etching. For highest resolution the foil is made by an electroforming process. The aperture pattern is first produced using a photoresist exposure process, where resist is left on the forming mandrel in any area that forms an aperture. Aperture dimensions of 10 µm and less have been produced reliably using this method. (Figure 3).

The shadow masks are mounted on rigid mask frames designed for the automated mask storage, handling, and alignment system. Positional accuracy of the shadow mask is verified prior to and during the mounting process using a vision measurement machine (VMM).

In the deposition process the mask is first placed between the evaporation source and the substrate. Advantech uses a high precision alignment system to align the mask to fiducial marker patterns on the substrate and places the mask within 1 µm of its desired position. This allows the use of multiple masks to create complex patterns and/or deposit different materials to build complete electronic circuits.

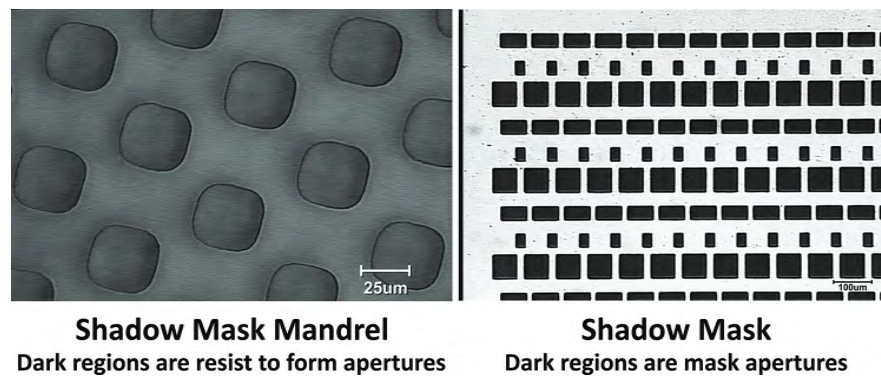

Figure 3. Shadow mask mandrel (left) and electroformed nickel shadow mask (right).

After alignment the mask is brought into direct contact with the substrate to avoid any shadowing effect (also described as overspray). When magnetic materials are used for the mask, such as nickel foil, a magnet behind the substrate can enhance the contact between mask and substrate.

The desired material is then deposited onto the substrate/mask combination. After the deposition process is completed and the mask is removed the desired pattern remains on the substrate.

SHADOW MASKS LIMITATIONS: THERMAL EXPANSION

A critical factor determining the geometrical precision of the deposited thin film pattern is the position accuracy of the shadow mask relative to the substrate during the duration of the deposition process. In particular, heat imposed by the material source on the shadow mask and substrate can result in poor quality of the deposited features.

The shadow mask material is subject to thermal expansion when exposed to heat from the deposition source. Absolute positions of the aperture patterns relative to the substrate will deviate from the desired deposition locations due to thermal expansion of the mask material and mask frame. Positions of apertures relative to each other on the mask are likewise affected by thermal expansion and the method of mounting the shadow mask on the frame, as well as the method of mounting the mask and frame relative to the substrate. Similarly, the substrate experiences thermal expansion by heating imposed by the material source. These thermal mask expansion effects result in a positional offset of the deposition pattern from the desired deposition position, often compromising the device's functionality.

Besides dimensional instability thermal expansion can also lead to buckling and unintended separation between mask and substrate. Any separation between mask and substrate leads to shadow deposits or overspray, as illustrated in Figure 4.

Thermal management therefore is essential to prevent any of the aforementioned shortcomings. Pre-stressing the mask, for example, allows for some compensation of heat-up, as does proper timing of the deposition sequence.

REQUIREMENTS FOR HIGH DEFINITION OF FINE FEATURES

PVD occurs in a vacuum vessel that is typically evacuated to a base pressure low enough to enable vapor species transport with a mean free path λ exceeding the source/substrate distance T > λ. Under such conditions, the vapor path between the source and the substrate approximates line-of-sight conditions, indicated by the dashed lines in Figure 4. For a base pressure of 1×10^{-3} Pa the mean free path is approximately 50 m, significantly larger than the source/substrate distance *T*.

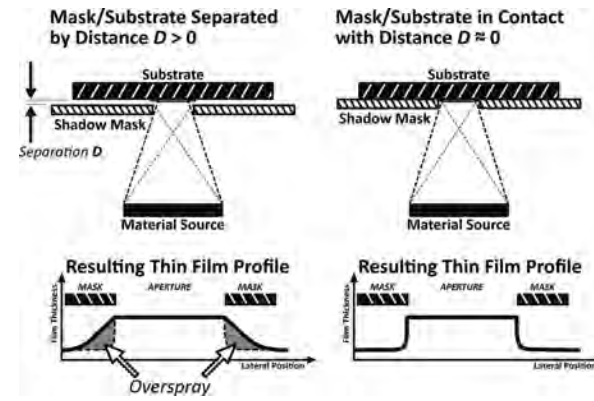

Figure 4. Thin film height profile for deposition with shadow mask separated by distance *D* from substrate (left) and shadow mask in close contact with substrate (right).

Generally, physical vapor deposition (PVD) by evaporation is suitable for producing sharp, well-defined features in thin films deposited through ideal shadow masks. This is the case in particular if the source resembles a point source such as thermal or e-beam evaporator at an appropriate distance from the mask/substrate arrangement and the base pressure can be held below 1×10^{-2} Pa.

A difficulty for evaporation processes lies in the limitation of size for the source as well as the selection of materials that can be evaporated from either thermal or e-beam sources. Some refractory metals, for example, require fairly high evaporation temperatures. The undesired side effect of evaporation at such high temperatures is the heat transfer generated by radiation.

SPUTTER DEPOSITION THROUGH SHADOW MASK

Sputtering offers an enhanced selection of materials that can be vacuum deposited as thin films on many types of substrates. Traditional sputter deposition, however, requires a chamber pressure of 1 to 10 Pa or even higher. In this pressure range the mean free path of sputter species is reduced to 0.05 m and less. For shadow mask deposition, however, it is impossible to place a sputter source this close to the mask

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to achieve more or less line-of-sight deposition and creation of sharp and defined features. The close proximity results in a coupling of the sputter plasma into the metal mask, and the electron current into the mask creates an unacceptable heat load in the mask, resulting in the aforementioned problems.

Increasing the distance between sputter source and mask and the reduced mean free path in this pressure regime results in frequent gas phase collisions of the sputtered vapor and the ambient gas molecules, and this creates non-line-of-sight deposition conditions. Patterns deposited by conventional sputtering through a shadow mask are broadened and blurred compared to evaporative physical vapor deposition (Figure 5).

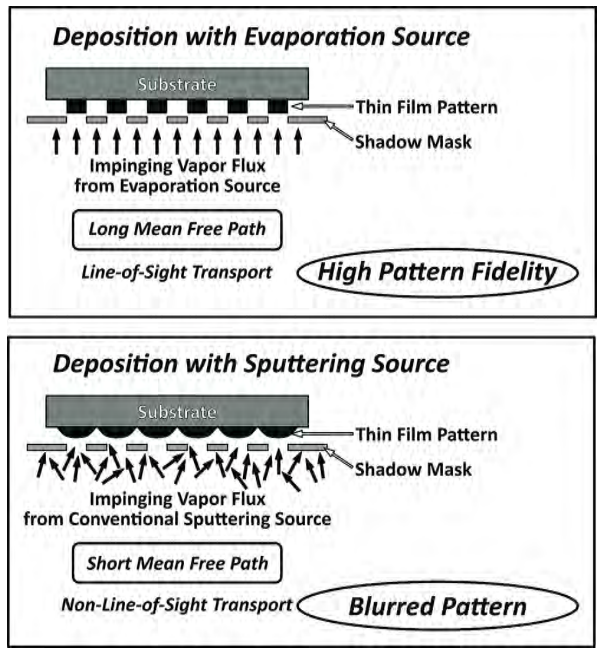

Figure 5. Evaporation (top) and conventional sputter deposition (bottom) through shadow mask and resulting feature height profiles.

RESULTS: LOW-PRESSURE SPUTTERING SOURCE

Advantech U.S., Inc., employed a novel low-pressure sputtering source (LPSS) developed by the Kurt J. Lesker Company that sustains stable operation at a pressure as low as 0.01 Pa (7.5×10^{-5} Torr).

The low pressure operation results in an increase of the mean free path to about 0.5 m, which allows sufficient separation between mask and sputter source to prevent coupling of plasma into the metal mask.

Figure 6 shows a top view and side view of the first-generation prototype of the LPSS. The horizontally mounted aluminum (AL) cathode body holds three integrated rod magnets and water cooling lines. The magnetic field lines wrap around the entire cathode body, creating an electron race track around the entire source. The LPSS source sputters material from both the top and bottom surfaces, consuming the cathode body.

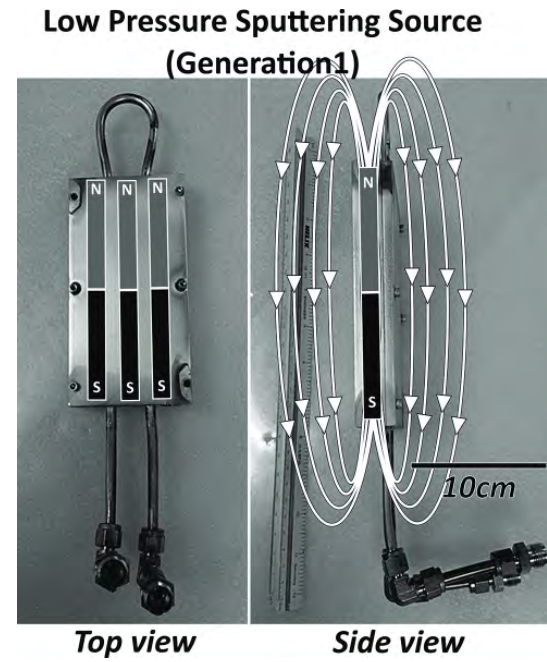

Figure 6. Low-pressure sputtering source Gen 1 prototype 8.9 cm × 19 cm (3.5″ × 7.5″) with magnet arrangement.

Figure 7 shows the voltage over pressure curve of a conventional magnetron sputtering source (triangle symbols on dashed curve) compared to the LPSS (circle symbols on

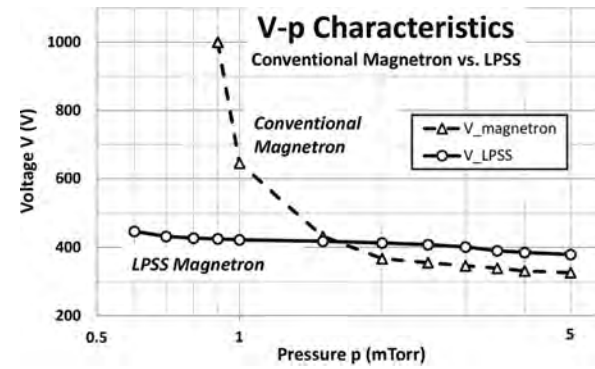

Figure 7. Voltage-pressure curves for conventional (dashed lines) and LPSS sputtering source (solid lines). The LPPS exhibits stable operation pressures below 12 Pa (1 mTorr) similar to cylindrical post magnetron sources [1]

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solid curve).Transport rates achieved with the LPSS are comparable to conventional sputtering sources. The LPSS achieves power densities that exceed those of conventional sputtering sources by one or two orders of magnitude. The original Gen 1 LPSS prototype was sized 8.9 cm × 19 cm (3.5” × 7.5") (Figure 6), the second-generation LPSS features 15.2 cm × 40.6 cm (6" × 16") and 15.2 cm × 81.3 cm (6" × 32") cathodes for large area deposition (Figure 8). The Gen 2 LPSS cathodes are mounted on a linear scanning stage to accommodate deposition on substrates as large as 61 cm × 91 cm (24" × 36").

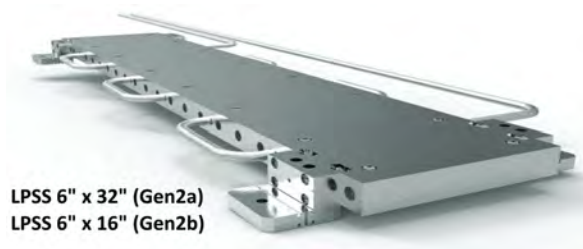

Figure 8. Second-generation large-area low-pressure sputtering source (LPSS) with 40.6 cm (16″) and 81.3 cm (32″) (shown) length.

MASKED THIN FILM DEPOSITION RESULTS USING NOVEL LOW-PRESSURE SPUTTERING SOURCE

Figure 9 shows the height profiles (lower graph) of 100-µm-wide features deposited through the same 20-µm-thick shadow mask using a conventional magnetron sputtering source (solid grey profile) and the Gen 1 LPSS in stationary mode (dashed black profile), both with 15.2 cm (6") target-substrate distance. The two upper images in Figure 9 are shadow masks with 60-µm and 70-µm features. LPSS deposition of the 800-Å-thick film from an aluminum target occurred at a chamber base pressure of 1×10^{-3} Pa and sputter pressure of 0.28 Pa under 2.5 sccm Ar flow with a DC power of 37 W at 467 V with a 15 min deposition duration. The LPSS-sputtered features replicate the mask aperture dimensions, whereas the features deposited with the conventional magnetron source exhibit a rounded profile that does not entirely fill the width of the 100-µm-wide shadow mask aperture.

Figure 10 shows a pattern of 10-µm-wide features deposited through a shadow mask with the 40.6 cm (16") Gen 2 LPSS source at 16.5 cm (6.5") target-substrate distance. The height profile of the features are crisp and well defined. It is worth noting that the profile was acquired with a 12.5-µm stylus which created to the rounded top edge shape.

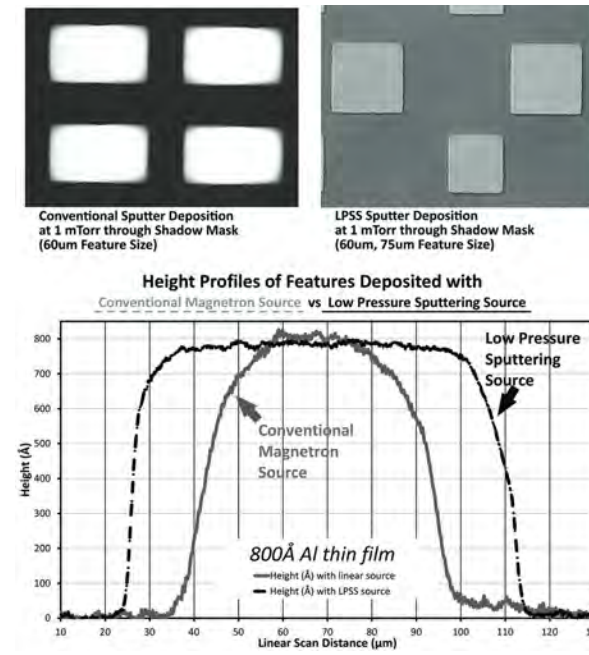

Figure 9. Shown in the lower graph is a comparison of 100-µm features and their height profiles deposited by two different sources. One profile was deposited with a conventional sputtering source (grey solid line); the other profile was deposited by the Gen 1 LPSS (black dashed line). The LPSS deposition shows a sharper, more well-defined deposited feature as compared to conventional sputtering The upper images in this figure are of 60 µm, 70 µm feature shadow masks.

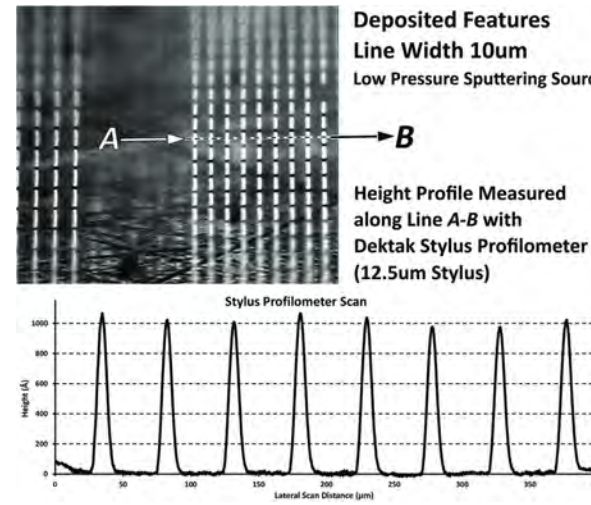

Figure 10. Height profile of 10 µm features deposited with LPSS through a shadow mask. The top image shows the deposited pattern. The bottom graph shows the surface profilometer scan from A to B, using a 12.5 µm stylis. The LPSS deposition yields sharp, well-defined features.

CONCLUSIONS

The novel low-pressure sputtering source (LPSS) has been successfully used to deposit crisp, well-defined 10-µm-and-larger features using precision shadow masks. The LPSS operates at low pressure yielding viable deposition rates and low thermal exposure of the mask and allows sputter deposition from both the top and bottom surfaces.

The 17.8 cm (7") LPSS prototype was scaled to 40.6 cm (16") and 81.3 cm (32") and succeeded in low pressure operation and deposition of sharp, well-defined features in stationary and scanning conditions. To date, aluminum, copper, and several refractory metals have been successfully deposited with the LPSS sources.

A patent application has been filed, and a production-ready cathode design is being evaluated while the source material portfolio is expanded.

The cost- and process-efficient LPSS technology opens new avenues for the additive manufacture of embedded electronic devices, circuits, and systems patterned by shadow masks, using advanced thin film materials.

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https://doi.org/10.1016/c2009-0-22311-7

FOR MORE INFORMATION:

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Attachment L-3

Screen capture created by J L Mullins from Knovel website on September 26, 2024 at URL: https://app.knovel.com/kn/resources/kpATCPMII5/toc?toc-within=Novel+low+presssure+sputtering+and+improved+vacuum+deposition+of+small+patterned+features+using+precision+shadow+masks

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13. Novel Low Pressure Sputtering Source and Improved Vacuum Deposition of Small Patterned Features Using Precision Shadow Masks

13.6 Sputter Deposition through Shadow Mask

... SPUTTER DEPOSITION THROUGH SHADOW MASK Sputtering offers an enhanced selection of materials that can be vacuum deposited as thin films on many types of substrates. Traditional sputter deposition, however, requires a chamber pressure of 1 to 10 Pa or even higher. In this pressure range the mean free path of sputter species is reduced to 0.05 m and less. For shadow mask deposition, however ...

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13.2 Today's Shadow Mask Technology

... 95 59th Annual Technical Conference Proceedings ©2016 Society of Vacuum Coaters Indianapolis, Indiana, May 9–13, 2016 All rights reserved• ISSN 07375921 https://doi•org/10•14332/svc16•proc•0036 www•svc•org Novel Low Pressure Sputtering Source and Improved Vacuum Deposition of Small Patterned Features Using Precision Shadow Masks Wolfgang Decker1, Rob Belan2, Volker D• Heydemann1, Sean Armstrong2 ...

13. Novel Low Pressure Sputtering Source and Improved Vacuum Deposition of Small Patterned Features Using Precision Shadow Masks

13.3 Thin Film Deposition through Shadow Masks

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Position-selective growth of carbon nanotubes on Ni catalysts/Mo underlayers by thermal chemical vapor deposition

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Position-selective growth of carbon nanotubes (CNTs) and vertically aligned CNTs (VACNTs) on patterned metal were prepared using thermal chemical vapor deposition (TCVD) and direct current (DC) plasma-enhanced chemical vapor deposition. We propose a new position-controlling method of CNTs by controlling not only the position of Ni as a catalyst, but also the morphology of Mo as an underlayer for the catalysts. Selective growth of CNTs was achieved at the edges of the patterned metal using TCVD. The minimum width of selectively grown CNTs, approximately 2.6 μm, was approximately one-eightieth that of the patterned metal, 200 μm. The VACNTs were synthesized using the PECVD method, but the VACNTs grew throughout the patterned metal. A position-controlled method of CNT growth was demonstrated in optimum conditions of the TCVD.

I. INTRODUCTION

Carbon nanotubes (CNTs) have been studied intensively because of their many featured characteristics such as high electric conductivity,[1] high permissible current density,[2] and high mechanical strength in spite of their high flexibility.[3] These characteristics are beneficial in preparing various nanostructures for use in scanning-probe microscopy tips,[4–6] field emitters,[7–9] and so on. To prepare such nanoscaled CNT devices, the controlling position and direction of CNTs is necessary. CNTs grow selectively from catalyst particles using chemical vapor deposition (CVD).[10] The growth direction of CNTs is controlled by applying an electric field during CVD growth.[11]

Position-selective growth of CNTs is possible by virtue of two characteristics: CNTs grow selectively from fine particle catalysts, and, we can control the synthesis of the fine particle catalysts by noticing wettability between metal interfaces. Wettability of metal interface is high. Therefore, it is difficult to form fine particles as overlayers on smooth underlayers. Overlayered metals form fine particles when the surfaces of underlayers are rough. In this article, we propose a new position-controlled method of CNT growth by controlling not only the catalysts' position, but also surface morphology of metal underlayers. We tried to prepare position-selective growth of CNTs and vertically aligned CNTs (VACNTs) on patterned metal electrodes to realize a novel electronic measuring nanoprobe.

II. EXPERIMENTAL

Patterned metals of Ni catalysts and Mo underlayers were deposited on quartz substrates through a metal mask (thickness of 30 μm, pattern width of 200 μm, and gap of 100 μm) using radio frequency (RF) magnetron sputtering. The chamber background pressure was 3.0×10^{-3} Pa, and the pressure during deposition was fixed at 2.0 Pa by feeding Ar gas. Growth conditions were 120 °C of substrate temperature, 50 W of sputtering power, and 1 min of sputtering time for Mo underlayers, and 70 °C, 20 W, and 1 min for Ni catalysts. The films' deposition rates were 10 nm/min^{-1} for Mo and 1 nm/min^{-1} for Ni. To control incident angles of sputtered atoms, aligned fins were installed during deposition. A schematic configuration of the fins and the metal mask is shown in Fig. 1.

The CNTs were grown using thermal chemical vapor deposition (TCVD) and direct current (DC) plasma-enhanced (PE) CVD methods. The CVD equipment reactor tube was heated to 600 °C. The background pressure was 0.1 Pa. The flow of H_2:Ar (10:200 ccm) was introduced into the reactor tube during heating. In the case of a TCVD method, a gas mixture of ethylene C_2H_4:H_2:Ar (20:10:200 ccm) was introduced into the reactor tube for 30 min for CNT growth. The total pressure was maintained at 100 kPa. In the case of the PECVD method, the CNT growth was performed by inducing a

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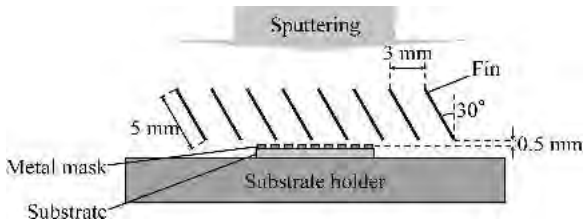

FIG. 1. Schematic configuration of the fins and the metal mask.

DC glow discharge and feeding a gas mixture of C_2H_4:H_2:Ar (5:50:50 ccm). The total pressure was maintained at 2 kPa. The DC plasma was produced by applying a bias voltage of −250 V between a substrate holder and grounded anodes, which were separated from the substrates by approximately 5 mm.

The patterned metals' respective morphologies were investigated using atomic force microscopy (AFM, NanoNavi Station; SII Nanotechnology, Inc., Tokyo, Japan). The CNTs' structures were observed using a field emission scanning electron microscope (SEM; S-4500; Hitachi Ltd., Tokyo, Japan) operated at 15 kV and a field emission transmission electron microscope (TEM; HF-2000; Hitachi Ltd.) operated at 200 kV.

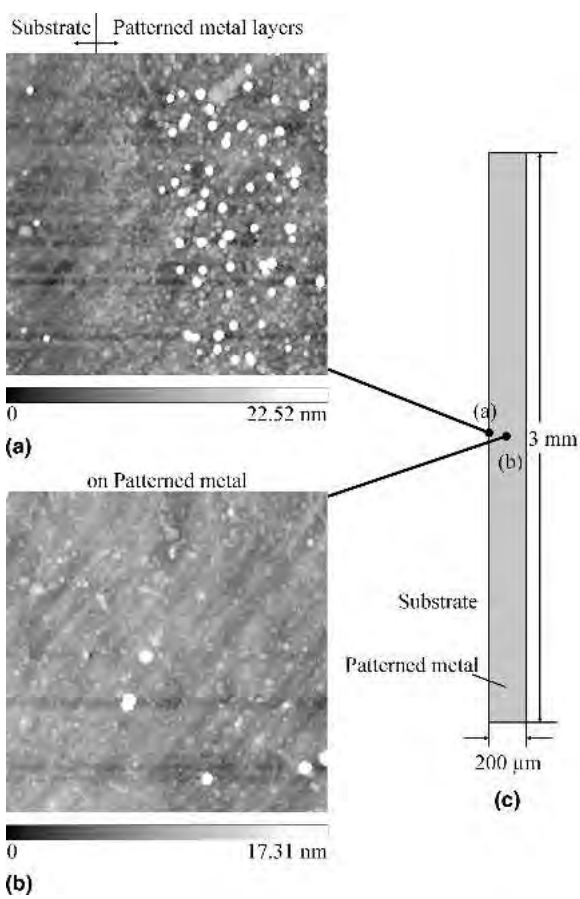

FIG. 2. (a) and (b) AFM images (5×5 μm^2) of patterned metal layers. (c) The scanning area of the AFM images. (a) The edge boundary of patterned metal layers. The left of the AFM image shows the substrate surfaces; the right shows the patterned metal layers. (b) The middle areas of the patterned metal.

III. RESULTS AND DISCUSSION

Figure 2 shows AFM images (5×5 μm^2) of the patterned metal layers immediately before CNT growth. Figures 2(a) and 2(b), respectively, show the edge boundary of patterned metal layers and the middle areas of the patterned metal. Figure 2(c) shows scanned areas of Figs. 2(a) and 2(b). The left of Fig. 2(a) shows the substrate surfaces; the right shows the patterned metal layers. At the pattern edges, large Ni particles with an approximate 30-nm height were observed on small Mo particles with an approximate 3-nm height. At the middle areas of the pattern [Fig. 2(b)], only a few particles were observed on smooth surfaces. Figure 3 shows SEM images of the edge boundary of the patterned metal layers after TCVD deposition at varying thickness of the Mo

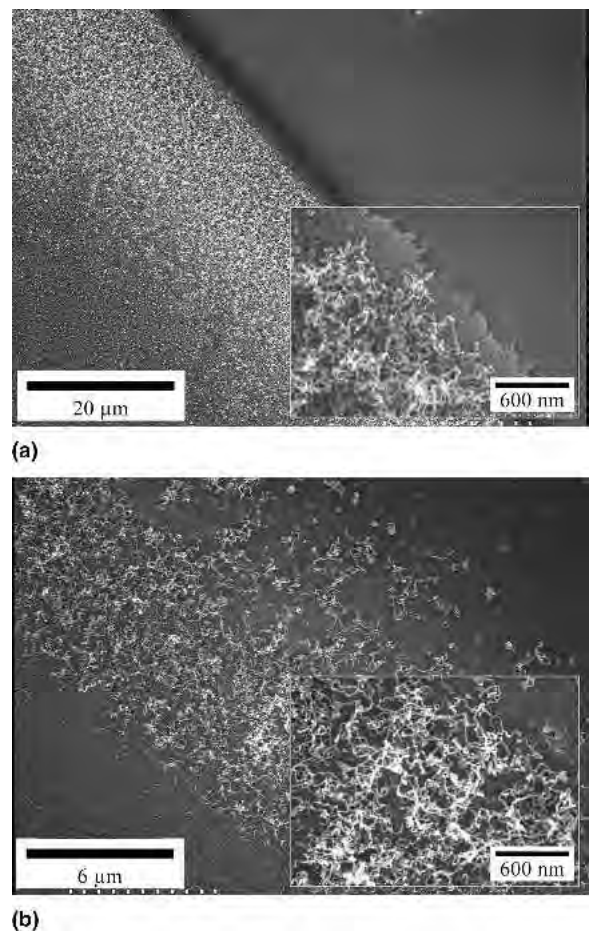

FIG. 3. SEM images of patterned metal layer boundary edges after TCVD while varying the Mo underlayer thickness. The Mo layers were (a) 10 nm and (b) 30 nm thick. The upper-right of the image shows the substrate surfaces; the lower-left shows the patterned metal layers. The CNTs grew in the narrow region that appears as the white contrast. The W_{CNT} was approximately (a) 30 μm and (b) 6.3 μm. The insets are magnified images.

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underlayer. Thickness of the Mo layers was 10 nm [Fig. 3(a)] and 30 nm [Fig. 3(b)]. The upper-right of the image shows the substrate surfaces; the lower-left shows the patterned metal layers. The CNTs, with an approximate 30-nm diameter, grew selectively immediately inside from the pattern edges that appear in the image as the white contrast. However, CNTs did not grow on the middle areas of the pattern. By increasing the Mo thickness from 10 nm [Fig. 3(a)] to 30 nm [Fig. 3(b)], the widths of selectively grown CNTs (W_{CNT}) decreased respectively from 30 μm [Fig. 3(a)] to 6.3 μm [Fig. 3(b)]. The CNT diameter was similar to that of the Ni particle, as observed using AFM. At the pattern edges, many small Mo particles were observed under the CNTs.

The position-selective growth of CNTs at the pattern edges was achieved because CNTs grow only from fine particle catalysts. Delzeit et al.[12] reported that no CNT was grown with 0.1–1.0 nm Fe on smooth, clean Si substrates. The CNTs grew by the addition of an Ir underlayer to increase the surface roughness and to provide more active nucleation sites. On the smooth surface of Mo underlayers, it is difficult for Ni catalysts to become fine particles because of the high wettability. The rough morphology of Mo underlayers provides active nucleation sites for Ni catalysts. The rough morphology was apparent in very thin regions of Mo because of a "shadow effect" of the sputtering method. A schematic shadow effect is illustrated in Fig. 4. Sputtered atoms arrive at substrates with various incident angles because of scattering by atmospheric gasses. Then the pattern edges thin down by deposition of particles shaded from the mask pattern. The rough regions of thicker Mo underlayers became narrow. Therefore, the W_{CNT} decreased by increasing Mo thickness.

Figure 5 shows SEM images of the pattern boundary after TCVD at varying sputtering pressures of metal layers. The W_{CNT} was decreased from 230 to 6.4 μm by reducing sputtering pressure from 4.0 to 1.2 Pa.

The shady region by metal mask is decreased by reducing sputtering pressure because incident angle variations of sputtered atoms are decreased. Therefore, by reducing sputtering pressure, the metal pattern edge was sharpened and W_{CNT} was reduced.

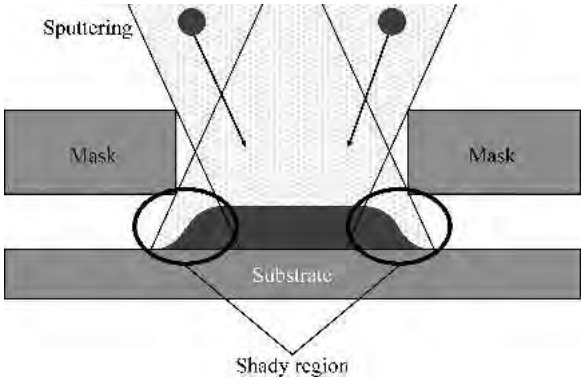

FIG. 4. Schematic of the "shadow effect" that appeared through the mask pattern. The pattern edges thin down because of deposition of shaded sputtered atoms under the mask edges (indicated by the oval).

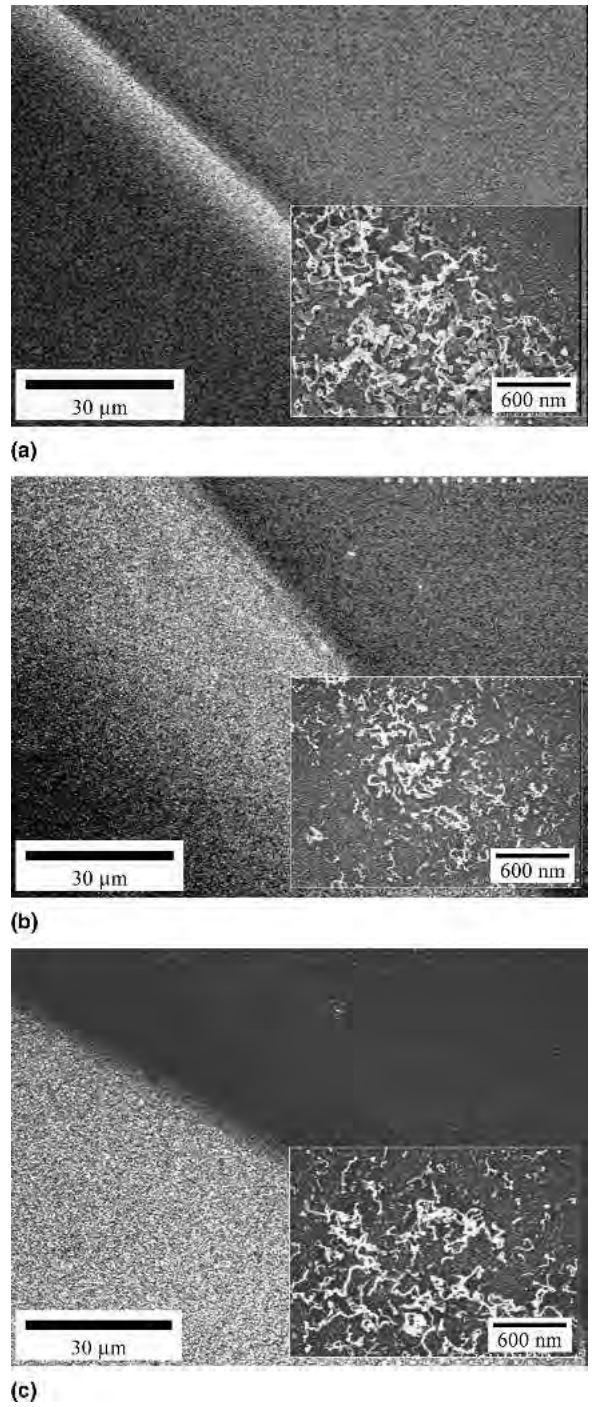

FIG. 5. SEM images of the edge boundary of patterned metal layers after TCVD at varying sputtering pressure of metal layers. The sputtering pressure of the metal layers was (a) 1.2 Pa, (b) 2.0 Pa, and (c) 4.0 Pa. The upper-right at the image is the substrate, the lower-left of the image is the metal pattern. The CNTs grew at narrow region where the contrast of the SEM image is white. The W_{CNT} was (a) 6.4 μm, (b) 26 μm, and (c) 230 μm. The inset shows magnified images.

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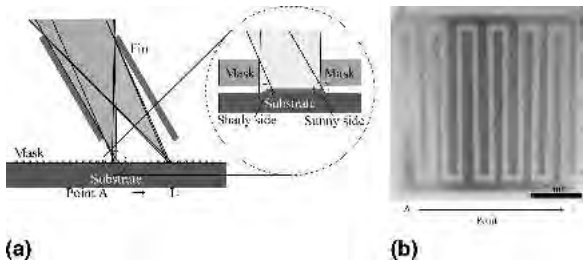

FIG. 6. (a) Schematic configuration of the aligned fins and the mask. (b) An optical microscopy image of a specimen prepared by installing the fins.

The aligned fins were installed during deposition to control incident angles of sputtered atoms. A schematic configuration of the fins and the metal mask is depicted in Fig. 6(a). The optical microscopy image of the patterned metal, which was sputtered through the fins, is shown in Fig. 6(b). The pattern contrast was not uniform because the metal pattern thickness was not uniform. For that reason, various metal pattern thicknesses can be evaluated simultaneously on this sample. Figure 7 shows typical SEM images of the pattern boundary after TCVD by installing the fins during Mo deposition. Figures 7(a) and 7(b), respectively, show the results on the edges of point D, and Figs. 7(c) and 7(d) show the results on the edges of point K. The images in Figs. 7(a) and 7(c) depict the "shady side"; the upper-right of the image shows the metal pattern. Images in Figs. 7(b) and 7(d) portray the "sunny side"; the lower-left of the image shows the metal pattern. The CNTs grew in the narrow region that appears as the white contrast. The W_{CNT} was (a) 17 μm, (b) 2.6 μm, (c) 29 μm, and (d) 19 μm. The W_{CNT} for every pattern is summarized in Fig. 8. The gray belts correspond to metal mask patterns and white belts correspond to the pattern gaps. The results show that the W_{CNT} was narrower on the "sunny side" than on the "shady side." In addition, the W_{CNT} depended on the position of the pattern. The minimum W_{CNT} was 2.6 μm. This width was approximately one-eightieth of the pattern width.

At pressures of 2.0 Pa, the sputtering condition of the mean free path of sputtered atoms was approximately 6 mm, which was slightly longer than the fin length of 5 mm. The sputtered atoms travel straight through vacancies of the fins. The incident angles of sputtered atoms were limited by the fins. The incident angle distributions were calculated. The width between the maximum and the minimum distance of the shaded area was determined as an effective width considering the shadow effect (W_{SE}). The solid lines in Fig. 8 show the W_{SE}. The gap between the mask and the substrate was fixed as about 5 μm. In calculation results, the W_{SE} was uniform between Points C and I. The respective W_{SE} of sunny and shady sides were 3 and 22 μm. The W_{SE} and W_{CNT} of

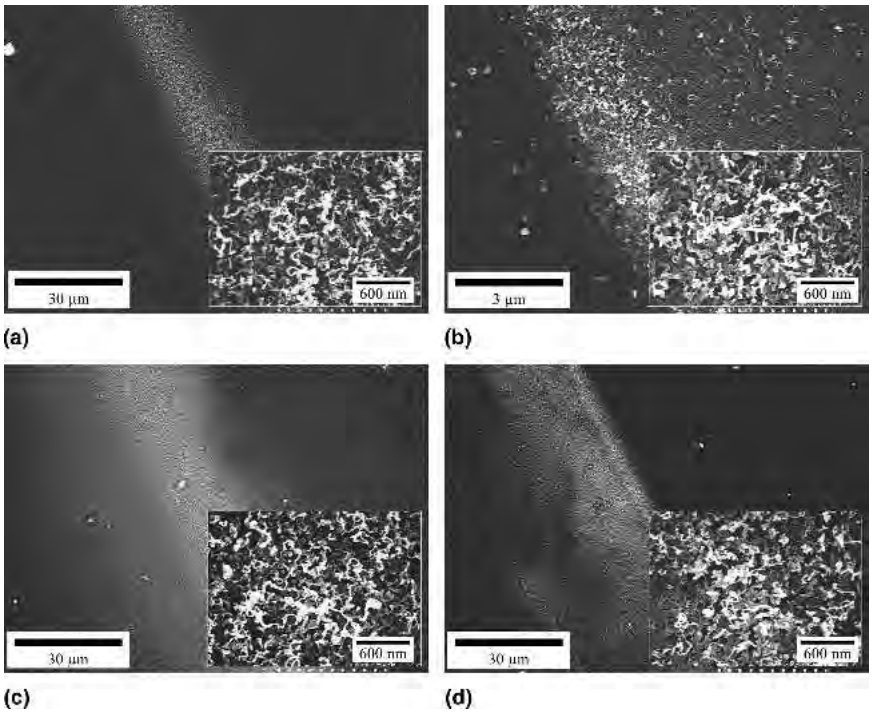

FIG. 7. Typical SEM images of the pattern boundary after TCVD by installing the fins: (a) and (b) results on the edges of point D; (c) and (d) results on point K. The images of (a) and (c) are the "shady side" and the upper-right of the image is the metal pattern. The images of (b) and (d) are the "sunny side" and the lower-left of the image is the metal pattern. The CNTs grew in the narrow region that appears as the white contrast area. The W_{CNT} was (a) 17 μm, (b) 2.6 μm, (c) 29 μm, and (d) 19 μm. The insets show magnified images.

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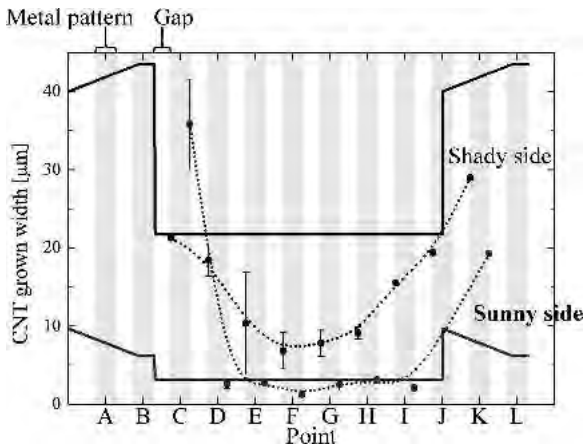

FIG. 8. The W_{CNT} observed at each point in every pattern prepared. The gray belts correspond to the metal mask patterns; white belts correspond to the pattern gaps. The solid lines show the effective width, W_{SE}.

sunny sides were narrower than those of shady sides because the number of atoms that originate from shaded directions under the edges of the mask is reduced by the fins. The W_{CNT} of shady sides depended on the position of the patterns, whereas the calculated W_{SE} was uniform between Point C and I. Figure 6(b) shows that this uniformity was attributable to the nonuniform thickness of the metal pattern. By increasing the thickness of the metal patterns, the W_{CNT} decreased, as discussed above. The thickness distribution resulted from installation of the fins. The W_{SE} and the W_{CNT} increased just under the tail of fins (Points A, B, J, K, and L) because of increased incident angles. The sputtered atoms were deposited through the left and right sides of the fin. Because the W_{SE} contains not only thin and rough regions, but also thick and smooth regions, the W_{SE} was larger than the W_{CNT}.

An electric field was applied during CVD to obtain VACNTs. Figure 9 shows SEM images of CNTs grown using TCVD only, applying a bias without a glow discharge [Fig. 9(a)], and PECVD with a glow discharge accompanying the discharge current [Fig. 9(b)]. The CNTs with an approximate 15-nm diameter grew in various, apparently random, directions using the TCVD method. The CNTs grew selectively near the boundary of the metal pattern. Effects of the applied bias during TCVD were not observed. In the case of PECVD method, CNTs with an approximate 25-nm diameter grew perpendicular to the surfaces. The VACNTs were observed throughout the pattern. Figure 10 shows a TEM image of CNTs grown using PECVD. The hollow center and graphitic sidewalls were observed. In this case, the number of walls was 25, and the CNT internal and external diameters were approximately 4.6 and 26 nm, respectively.

The VACNTs were achieved only through the use of

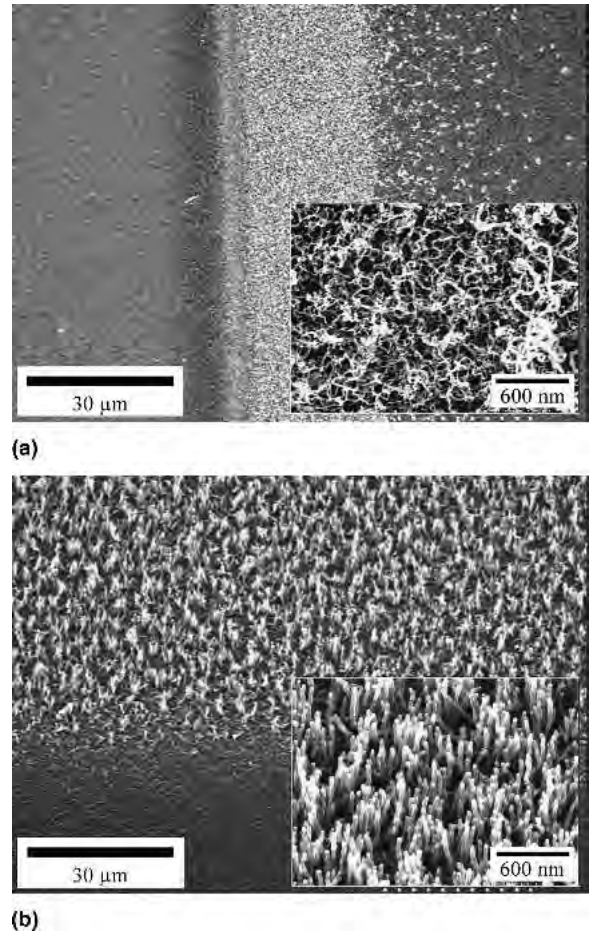

FIG. 9. SEM images of CNTs grown using TCVD only (a) applying bias without a discharge and (b) PECVD with a glow discharge. An applied bias voltage was −300 V [(a) discharge current of approximately 0.005 A]; and −250 V [(b) discharge current of approximately 0.3 A]. Images of (b) were taken at a 45° tilt angle. The inset shows magnified images.

PECVD method. The voltage drop takes place mostly in the cathode dark space when a glow discharge is induced. The thickness of the cathode dark space was estimated using the Child-Langmuir law. The estimated thickness of the cathode dark space was 0.21 mm. Then, the electric field induced above the substrates was approximately 1.2 kV/mm^{-1}. The cathode dark space thickness was estimated in the case of TCVD also. The estimated cathode dark space thickness was 60 mm, which was larger than the distance separating the cathode and anode. Therefore, the electric field might be uniform in the space between the cathode and the anode. The electric field above the substrates was approximately 60 V/mm^{-1}. The electric field applied in the case of PECVD was approximately 20 times larger than that in TCVD. The CNTs grew throughout the pattern by PECVD, whereas selective growth was observed using TCVD. This result suggests that the Ni catalysts were changed into fine particles by bombardment of ions accelerated in a large electric field.

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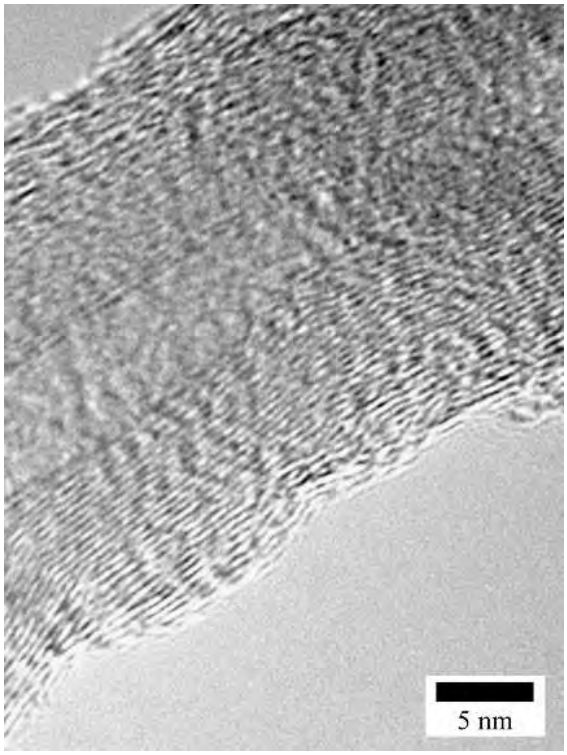

FIG. 10. Typical TEM image of CNTs grown using PECVD.

Results showed that CNTs were able to grow even on the smooth metal patterns.

IV. CONCLUSIONS

We prepared CNTs and VACNTs grown selectively on patterned metal. The selectively grown CNTs were observed at the edges of the patterned metal using TCVD. By controlling not only the catalyst position, but also the surface morphology of their underlayers, the width of selectively grown CNTs was minimized to approximately 2.6 μm. That width was approximately one-eightieth that of the patterned metal, which was 200 μm. To prepare VACNTs, DC-negative bias voltage was applied to the substrates. The VACNTs were synthesized when the glow discharge took place in the PECVD. The VACNTs grew all over the patterned metal. Selective growth of CNTs was achieved in optimum conditions of the TCVD by controlling the morphology of the Mo underlayers for Ni catalysts.

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2911–2915	**Raman studies of optical phonons in vertical cadmium sulfide nanorod arrays**	Dongjuan Xi, Jianzhong Li, Qibing Pei, Bin Chen
2916–2921	**Nanofabrication of top-gated carbon nanotube-based transistors: Probing electron-electron interactions in one-dimensional systems**	J.A. Sulpizio, Z.Z. Bandić, D. Goldhaber-Gordon
2922–2926	**Bonding strength of a carbon nanofiber array to its substrate**	Yi Zhang, Ephraim Suhir, Yuan Xu, Claire Gu
2927–2935	**Electronic structure of free-standing InP and InAs nanowires**	B. Lassen, M. Willatzen, R. Melnik, L.C. Lew Yan Voon
2936–2940	**Solid-state growth of nickel silicide nanowire by the metal-induced growth method**	Joondong Kim, Jong-Uk Bae, Wayne A. Anderson, Hyun-Mi Kim, Ki-Bum Kim
2941–2947	**Synthesis, characterization, and photocatalytic properties of pyrochlore $Bi_2Ti_2O_7$ nanotubes**	Hongjun Zhou, Tae-Jin Park, Stanislaus S. Wong
2948–2954	**Effective Young's modulus of carbon nanofiber array**	Yi Zhang, Ephraim Suhir, Yuan Xu
2955–2962	**Synthesis, structure, and magnetic properties of iron-oxide nanowires**	Matej Pregelj, Polona Umek, Boštjan Drolc, Boštjan Jančar, Zvonko Jagličič, Robert Dominko, Denis Arčon

Position-selective growth of carbon nanotubes on Ni catalysts/Mo underlayers by thermal chemical vapor deposition

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Position-selective growth of carbon nanotubes (CNTs) and vertically aligned CNTs (VACNTs) on patterned metal were prepared using thermal chemical vapor deposition (TCVD) and direct current (DC) plasma-enhanced chemical vapor deposition. We propose a new position-controlling method of CNTs by controlling not only the position of Ni as a catalyst, but also the morphology of Mo as an underlayer for the catalysts. Selective growth of CNTs was achieved at the edges of the patterned metal using TCVD. The minimum width of selectively grown CNTs, approximately 2.6 μm, was approximately one-eightieth that of the patterned metal, 200 μm. The VACNTs were synthesized using the PECVD method, but the VACNTs grew throughout the patterned metal. A position-controlled method of CNT growth was demonstrated in optimum conditions of the TCVD.

I. INTRODUCTION

Carbon nanotubes (CNTs) have been studied intensively because of their many featured characteristics such as high electric conductivity,[1] high permissible current density,[2] and high mechanical strength in spite of their high flexibility.[3] These characteristics are beneficial in preparing various nanostructures for use in scanning-probe microscopy tips,[4–6] field emitters,[7–9] and so on. To prepare such nanoscaled CNT devices, the controlling position and direction of CNTs is necessary. CNTs grow selectively from catalyst particles using chemical vapor deposition (CVD).[10] The growth direction of CNTs is controlled by applying an electric field during CVD growth.[11]

Position-selective growth of CNTs is possible by virtue of two characteristics: CNTs grow selectively from fine particle catalysts, and, we can control the synthesis of the fine particle catalysts by noticing wettability between metal interfaces. Wettability of metal interface is high. Therefore, it is difficult to form fine particles as overlayers on smooth underlayers. Overlayered metals form fine particles when the surfaces of underlayers are rough. In this article, we propose a new position-controlled method of CNT growth by controlling not only the catalysts' position, but also surface morphology of metal underlayers. We tried to prepare position-selective growth of CNTs and vertically aligned CNTs (VACNTs) on patterned metal electrodes to realize a novel electronic measuring nanoprobe.

II. EXPERIMENTAL

Patterned metals of Ni catalysts and Mo underlayers were deposited on quartz substrates through a metal mask (thickness of 30 μm, pattern width of 200 μm, and gap of 100 μm) using radio frequency (RF) magnetron sputtering. The chamber background pressure was 3.0×10^{-3} Pa, and the pressure during deposition was fixed at 2.0 Pa by feeding Ar gas. Growth conditions were 120 °C of substrate temperature, 50 W of sputtering power, and 1 min of sputtering time for Mo underlayers, and 70 °C, 20 W, and 1 min for Ni catalysts. The films' deposition rates were 10 nm/min^{-1} for Mo and 1 nm/min^{-1} for Ni. To control incident angles of sputtered atoms, aligned fins were installed during deposition. A schematic configuration of the fins and the metal mask is shown in Fig. 1.

The CNTs were grown using thermal chemical vapor deposition (TCVD) and direct current (DC) plasma-enhanced (PE) CVD methods. The CVD equipment reactor tube was heated to 600 °C. The background pressure was 0.1 Pa. The flow of H_2:Ar (10:200 ccm) was introduced into the reactor tube during heating. In the case of a TCVD method, a gas mixture of ethylene C_2H_4:H_2:Ar (20:10:200 ccm) was introduced into the reactor tube for 30 min for CNT growth. The total pressure was maintained at 100 kPa. In the case of the PECVD method, the CNT growth was performed by inducing a

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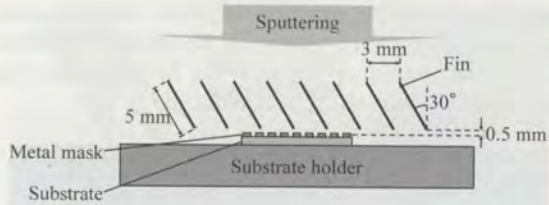

FIG. 1. Schematic configuration of the fins and the metal mask.

DC glow discharge and feeding a gas mixture of C_2H_4:H_2:Ar (5:50:50 ccm). The total pressure was maintained at 2 kPa. The DC plasma was produced by applying a bias voltage of −250 V between a substrate holder and grounded anodes, which were separated from the substrates by approximately 5 mm.

The patterned metals' respective morphologies were investigated using atomic force microscopy (AFM, NanoNavi Station; SII Nanotechnology, Inc., Tokyo, Japan). The CNTs' structures were observed using a field emission scanning electron microscope (SEM; S-4500; Hitachi Ltd., Tokyo, Japan) operated at 15 kV and a field emission transmission electron microscope (TEM; HF-2000; Hitachi Ltd.) operated at 200 kV.

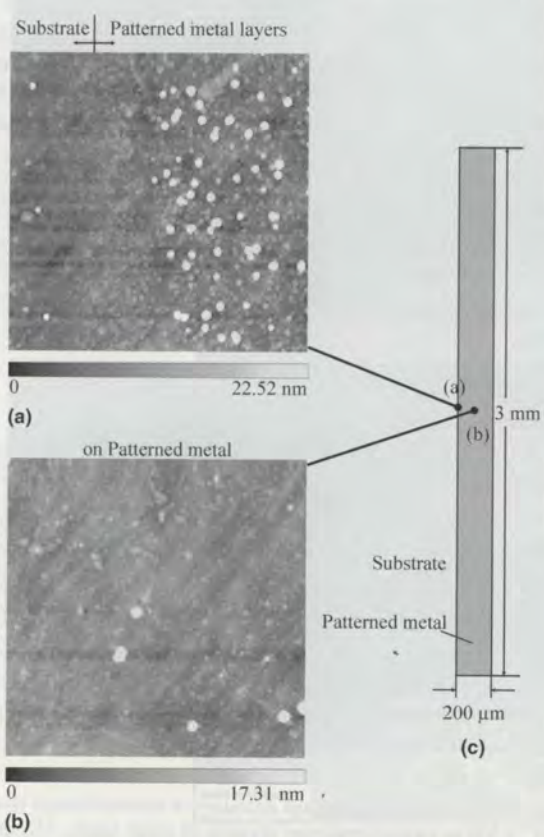

FIG. 2. (a) and (b) AFM images (5×5 μm^2) of patterned metal layers. (c) The scanning area of the AFM images. (a) The edge boundary of patterned metal layers. The left of the AFM image shows the substrate surfaces; the right shows the patterned metal layers. (b) The middle areas of the patterned metal.

III. RESULTS AND DISCUSSION

Figure 2 shows AFM images (5×5 μm^2) of the patterned metal layers immediately before CNT growth. Figures 2(a) and 2(b), respectively, show the edge boundary of patterned metal layers and the middle areas of the patterned metal. Figure 2(c) shows scanned areas of Figs. 2(a) and 2(b). The left of Fig. 2(a) shows the substrate surfaces; the right shows the patterned metal layers. At the pattern edges, large Ni particles with an approximate 30-nm height were observed on small Mo particles with an approximate 3-nm height. At the middle areas of the pattern [Fig. 2(b)], only a few particles were observed on smooth surfaces. Figure 3 shows SEM images of the edge boundary of the patterned metal layers after TCVD deposition at varying thickness of the Mo

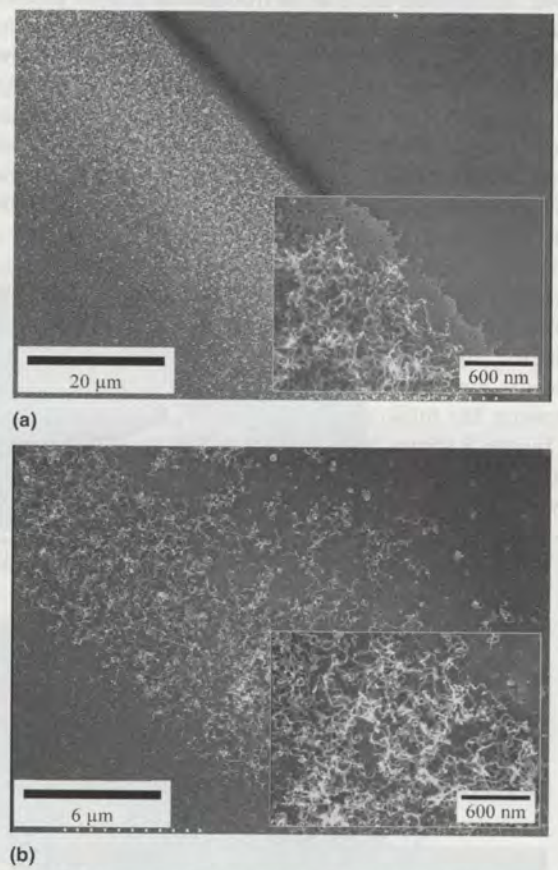

FIG. 3. SEM images of patterned metal layer boundary edges after TCVD while varying the Mo underlayer thickness. The Mo layers were (a) 10 nm and (b) 30 nm thick. The upper-right of the image shows the substrate surfaces; the lower-left shows the patterned metal layers. The CNTs grew in the narrow region that appears as the white contrast. The W_{CNT} was approximately (a) 30 μm and (b) 6.3 μm. The insets are magnified images.

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underlayer. Thickness of the Mo layers was 10 nm [Fig. 3(a)] and 30 nm [Fig. 3(b)]. The upper-right of the image shows the substrate surfaces; the lower-left shows the patterned metal layers. The CNTs, with an approximate 30-nm diameter, grew selectively immediately inside from the pattern edges that appear in the image as the white contrast. However, CNTs did not grow on the middle areas of the pattern. By increasing the Mo thickness from 10 nm [Fig. 3(a)] to 30 nm [Fig. 3(b)], the widths of selectively grown CNTs (W_{CNT}) decreased respectively from 30 μm [Fig. 3(a)] to 6.3 μm [Fig. 3(b)]. The CNT diameter was similar to that of the Ni particle, as observed using AFM. At the pattern edges, many small Mo particles were observed under the CNTs.

The position-selective growth of CNTs at the pattern edges was achieved because CNTs grow only from fine particle catalysts. Delzeit et al.[12] reported that no CNT was grown with 0.1–1.0 nm Fe on smooth, clean Si substrates. The CNTs grew by the addition of an Ir underlayer to increase the surface roughness and to provide more active nucleation sites. On the smooth surface of Mo underlayers, it is difficult for Ni catalysts to become fine particles because of the high wettability. The rough morphology of Mo underlayers provides active nucleation sites for Ni catalysts. The rough morphology was apparent in very thin regions of Mo because of a "shadow effect" of the sputtering method. A schematic shadow effect is illustrated in Fig. 4. Sputtered atoms arrive at substrates with various incident angles because of scattering by atmospheric gasses. Then the pattern edges thin down by deposition of particles shaded from the mask pattern. The rough regions of thicker Mo underlayers became narrow. Therefore, the W_{CNT} decreased by increasing Mo thickness.

Figure 5 shows SEM images of the pattern boundary after TCVD at varying sputtering pressures of metal layers. The W_{CNT} was decreased from 230 to 6.4 μm by reducing sputtering pressure from 4.0 to 1.2 Pa.

The shady region by metal mask is decreased by reducing sputtering pressure because incident angle variations of sputtered atoms are decreased. Therefore, by reducing sputtering pressure, the metal pattern edge was sharpened and W_{CNT} was reduced.

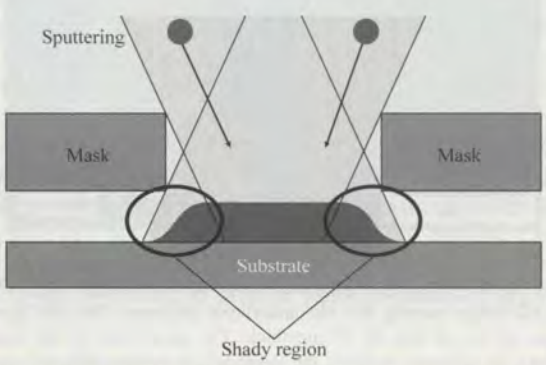

FIG. 4. Schematic of the "shadow effect" that appeared through the mask pattern. The pattern edges thin down because of deposition of shaded sputtered atoms under the mask edges (indicated by the oval).

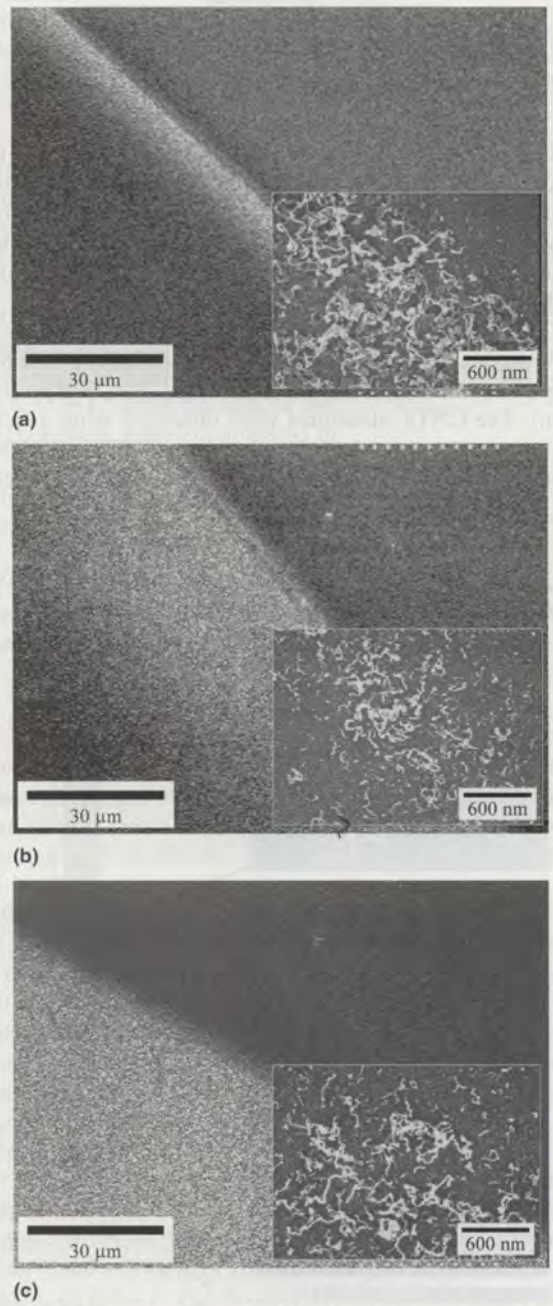

FIG. 5. SEM images of the edge boundary of patterned metal layers after TCVD at varying sputtering pressure of metal layers. The sputtering pressure of the metal layers was (a) 1.2 Pa, (b) 2.0 Pa, and (c) 4.0 Pa. The upper-right at the image is the substrate, the lower-left of the image is the metal pattern. The CNTs grew at narrow region where the contrast of the SEM image is white. The W_{CNT} was (a) 6.4 μm, (b) 26 μm, and (c) 230 μm. The inset shows magnified images.

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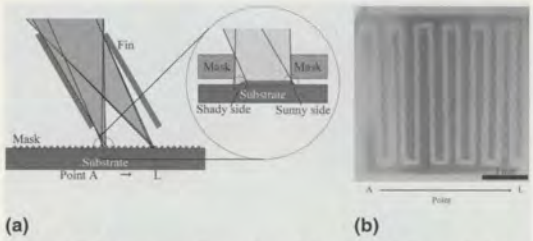

FIG. 6. (a) Schematic configuration of the aligned fins and the mask. (b) An optical microscopy image of a specimen prepared by installing the fins.

The aligned fins were installed during deposition to control incident angles of sputtered atoms. A schematic configuration of the fins and the metal mask is depicted in Fig. 6(a). The optical microscopy image of the patterned metal, which was sputtered through the fins, is shown in Fig. 6(b). The pattern contrast was not uniform because the metal pattern thickness was not uniform. For that reason, various metal pattern thicknesses can be evaluated simultaneously on this sample. Figure 7 shows typical SEM images of the pattern boundary after TCVD by installing the fins during Mo deposition. Figures 7(a) and 7(b), respectively, show the results on the edges of point D, and Figs. 7(c) and 7(d) show the results on the edges of point K. The images in Figs. 7(a) and 7(c) depict the "shady side"; the upper-right of the image shows the metal pattern. Images in Figs. 7(b) and 7(d) portray the "sunny side"; the lower-left of the image shows the metal pattern. The CNTs grew in the narrow region that appears as the white contrast. The W_{CNT} was (a) 17 μm, (b) 2.6 μm, (c) 29 μm, and (d) 19 μm. The W_{CNT} for every pattern is summarized in Fig. 8. The gray belts correspond to metal mask patterns and white belts correspond to the pattern gaps. The results show that the W_{CNT} was narrower on the "sunny side" than on the "shady side." In addition, the W_{CNT} depended on the position of the pattern. The minimum W_{CNT} was 2.6 μm. This width was approximately one-eightieth of the pattern width.

At pressures of 2.0 Pa, the sputtering condition of the mean free path of sputtered atoms was approximately 6 mm, which was slightly longer than the fin length of 5 mm. The sputtered atoms travel straight through vacancies of the fins. The incident angles of sputtered atoms were limited by the fins. The incident angle distributions were calculated. The width between the maximum and the minimum distance of the shaded area was determined as an effective width considering the shadow effect (W_{SE}). The solid lines in Fig. 8 show the W_{SE}. The gap between the mask and the substrate was fixed as about 5 μm. In calculation results, the W_{SE} was uniform between Points C and I. The respective W_{SE} of sunny and shady sides were 3 and 22 μm. The W_{SE} and W_{CNT} of

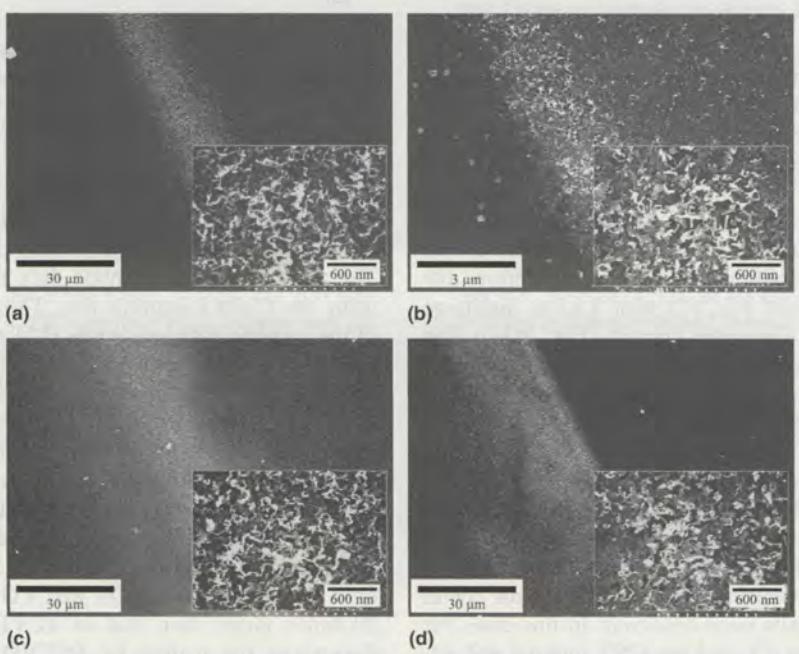

FIG. 7. Typical SEM images of the pattern boundary after TCVD by installing the fins: (a) and (b) results on the edges of point D; (c) and (d) results on point K. The images of (a) and (c) are the "shady side" and the upper-right of the image is the metal pattern. The images of (b) and (d) are the "sunny side" and the lower-left of the image is the metal pattern. The CNTs grew in the narrow region that appears as the white contrast area. The W_{CNT} was (a) 17 μm, (b) 2.6 μm, (c) 29 μm, and (d) 19 μm. The insets show magnified images.

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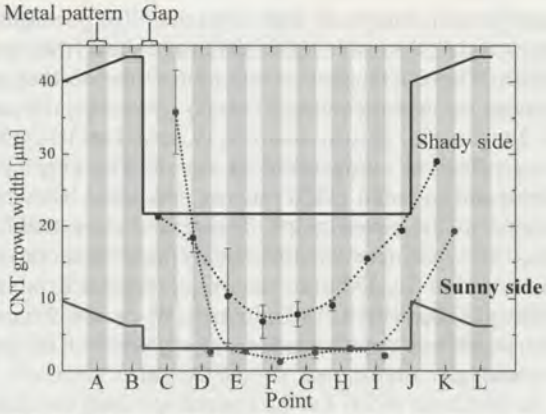

FIG. 8. The W_{CNT} observed at each point in every pattern prepared. The gray belts correspond to the metal mask patterns; white belts correspond to the pattern gaps. The solid lines show the effective width, W_{SE}.

sunny sides were narrower than those of shady sides because the number of atoms that originate from shaded directions under the edges of the mask is reduced by the fins. The W_{CNT} of shady sides depended on the position of the patterns, whereas the calculated W_{SE} was uniform between Point C and I. Figure 6(b) shows that this uniformity was attributable to the nonuniform thickness of the metal pattern. By increasing the thickness of the metal patterns, the W_{CNT} decreased, as discussed above. The thickness distribution resulted from installation of the fins. The W_{SE} and the W_{CNT} increased just under the tail of fins (Points A, B, J, K, and L) because of increased incident angles. The sputtered atoms were deposited through the left and right sides of the fin. Because the W_{SE} contains not only thin and rough regions, but also thick and smooth regions, the W_{SE} was larger than the W_{CNT}.

An electric field was applied during CVD to obtain VACNTs. Figure 9 shows SEM images of CNTs grown using TCVD only, applying a bias without a glow discharge [Fig. 9(a)], and PECVD with a glow discharge accompanying the discharge current [Fig. 9(b)]. The CNTs with an approximate 15-nm diameter grew in various, apparently random, directions using the TCVD method. The CNTs grew selectively near the boundary of the metal pattern. Effects of the applied bias during TCVD were not observed. In the case of PECVD method, CNTs with an approximate 25-nm diameter grew perpendicular to the surfaces. The VACNTs were observed throughout the pattern. Figure 10 shows a TEM image of CNTs grown using PECVD. The hollow center and graphitic sidewalls were observed. In this case, the number of walls was 25, and the CNT internal and external diameters were approximately 4.6 and 26 nm, respectively.

The VACNTs were achieved only through the use of

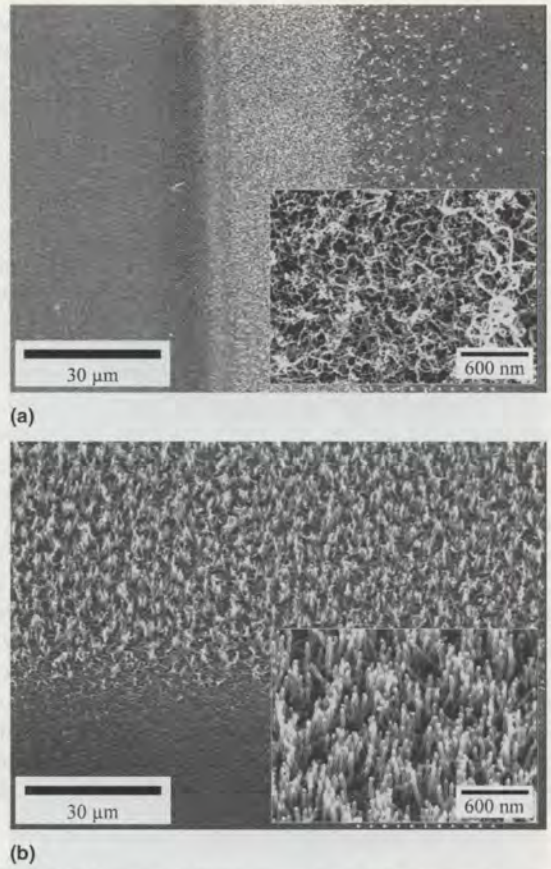

FIG. 9. SEM images of CNTs grown using TCVD only (a) applying bias without a discharge and (b) PECVD with a glow discharge. An applied bias voltage was −300 V [(a) discharge current of approximately 0.005 A]; and −250 V [(b) discharge current of approximately 0.3 A]. Images of (b) were taken at a 45° tilt angle. The inset shows magnified images.

PECVD method. The voltage drop takes place mostly in the cathode dark space when a glow discharge is induced. The thickness of the cathode dark space was estimated using the Child-Langmuir law. The estimated thickness of the cathode dark space was 0.21 mm. Then, the electric field induced above the substrates was approximately 1.2 kV/mm^{-1}. The cathode dark space thickness was estimated in the case of TCVD also. The estimated cathode dark space thickness was 60 mm, which was larger than the distance separating the cathode and anode. Therefore, the electric field might be uniform in the space between the cathode and the anode. The electric field above the substrates was approximately 60 V/mm^{-1}. The electric field applied in the case of PECVD was approximately 20 times larger than that in TCVD. The CNTs grew throughout the pattern by PECVD, whereas selective growth was observed using TCVD. This result suggests that the Ni catalysts were changed into fine particles by bombardment of ions accelerated in a large electric field.

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FIG. 10. Typical TEM image of CNTs grown using PECVD.

Results showed that CNTs were able to grow even on the smooth metal patterns.

IV. CONCLUSIONS

We prepared CNTs and VACNTs grown selectively on patterned metal. The selectively grown CNTs were observed at the edges of the patterned metal using TCVD. By controlling not only the catalyst position, but also the surface morphology of their underlayers, the width of selectively grown CNTs was minimized to approximately 2.6 μm. That width was approximately one-eightieth that of the patterned metal, which was 200 μm. To prepare VACNTs, DC-negative bias voltage was applied to the substrates. The VACNTs were synthesized when the glow discharge took place in the PECVD. The VACNTs grew all over the patterned metal. Selective growth of CNTs was achieved in optimum conditions of the TCVD by controlling the morphology of the Mo underlayers for Ni catalysts.

ACKNOWLEDGMENTS

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Attachment M-3

Position-selective growth of carbon nanotubes on Ni catalysts/Mo underlayers by thermal chemical vapor deposition

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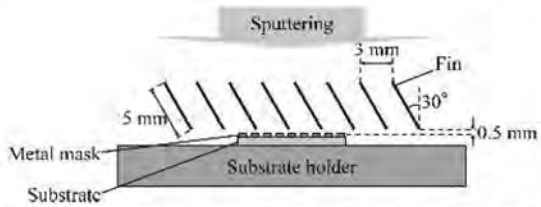

FIG. 1. Schematic configuration of the fins and the metal mask.

DC glow discharge and feeding a gas mixture of C_2H_4:H_2:Ar (5:50:50 ccm). The total pressure was maintained at 2 kPa. The DC plasma was produced by applying a bias voltage of −250 V between a substrate holder and grounded anodes, which were separated from the substrates by approximately 5 mm.

The patterned metals' respective morphologies were investigated using atomic force microscopy (AFM, NanoNavi Station; SII Nanotechnology, Inc., Tokyo, Japan). The CNTs' structures were observed using a field emission scanning electron microscope (SEM; S-4500; Hitachi Ltd., Tokyo, Japan) operated at 15 kV and a field emission transmission electron microscope (TEM; HF-2000; Hitachi Ltd.) operated at 200 kV.

III. RESULTS AND DISCUSSION

Figure 2 shows AFM images (5×5 μm^2) of the patterned metal layers immediately before CNT growth. Figures 2(a) and 2(b), respectively, show the edge boundary of patterned metal layers and the middle areas of the patterned metal. Figure 2(c) shows scanned areas of Figs. 2(a) and 2(b). The left of Fig. 2(a) shows the substrate surfaces; the right shows the patterned metal layers. At the pattern edges, large Ni particles with an approximate 30-nm height were observed on small Mo particles with an approximate 3-nm height. At the middle areas of the pattern [Fig. 2(b)], only a few particles were observed on smooth surfaces. Figure 3 shows SEM images of the edge boundary of the patterned metal layers after TCVD deposition at varying thickness of the Mo

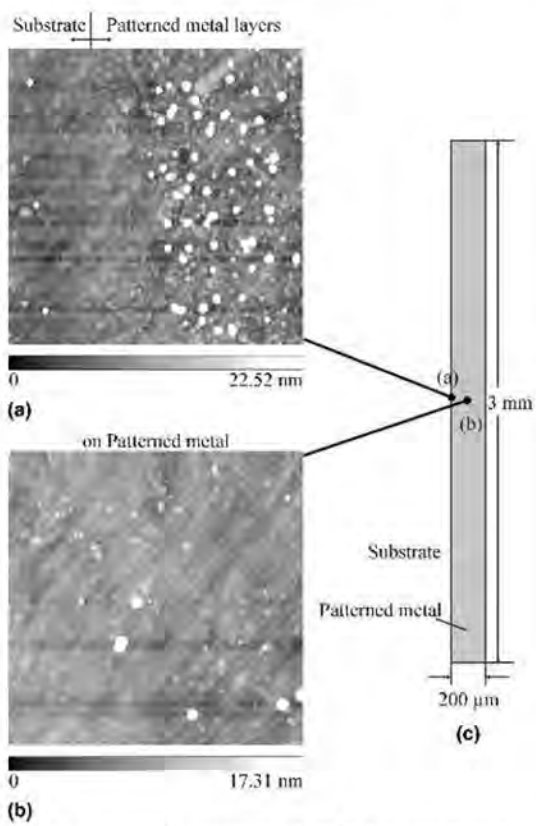

FIG. 2. (a) and (b) AFM images (5×5 μm^2) of patterned metal layers. (c) The scanning area of the AFM images. (a) The edge boundary of patterned metal layers. The left of the AFM image shows the substrate surfaces; the right shows the patterned metal layers. (b) The middle areas of the patterned metal.

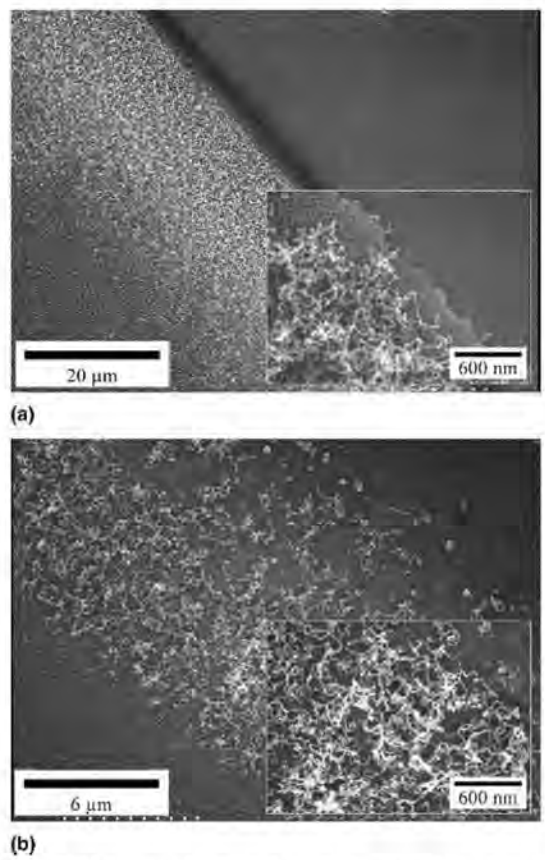

FIG. 3. SEM images of patterned metal layer boundary edges after TCVD while varying the Mo underlayer thickness. The Mo layers were (a) 10 nm and (b) 30 nm thick. The upper-right of the image shows the substrate surfaces; the lower-left shows the patterned metal layers. The CNTs grew in the narrow region that appears as the white contrast. The W_{CNT} was approximately (a) 30 μm and (b) 6.3 μm. The insets are magnified images.

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underlayer. Thickness of the Mo layers was 10 nm [Fig. 3(a)] and 30 nm [Fig. 3(b)]. The upper-right of the image shows the substrate surfaces; the lower-left shows the patterned metal layers. The CNTs, with an approximate 30-nm diameter, grew selectively immediately inside from the pattern edges that appear in the image as the white contrast. However, CNTs did not grow on the middle areas of the pattern. By increasing the Mo thickness from 10 nm [Fig. 3(a)] to 30 nm [Fig. 3(b)], the widths of selectively grown CNTs (W_{CNT}) decreased respectively from 30 μm [Fig. 3(a)] to 6.3 μm [Fig. 3(b)]. The CNT diameter was similar to that of the Ni particle, as observed using AFM. At the pattern edges, many small Mo particles were observed under the CNTs.

The position-selective growth of CNTs at the pattern edges was achieved because CNTs grow only from fine particle catalysts. Delzeit et al.[12] reported that no CNT was grown with 0.1–1.0 nm Fe on smooth, clean Si substrates. The CNTs grew by the addition of an Ir underlayer to increase the surface roughness and to provide more active nucleation sites. On the smooth surface of Mo underlayers, it is difficult for Ni catalysts to become fine particles because of the high wettability. The rough morphology of Mo underlayers provides active nucleation sites for Ni catalysts. The rough morphology was apparent in very thin regions of Mo because of a "shadow effect" of the sputtering method. A schematic shadow effect is illustrated in Fig. 4. Sputtered atoms arrive at substrates with various incident angles because of scattering by atmospheric gasses. Then the pattern edges thin down by deposition of particles shaded from the mask pattern. The rough regions of thicker Mo underlayers became narrow. Therefore, the W_{CNT} decreased by increasing Mo thickness.

Figure 5 shows SEM images of the pattern boundary after TCVD at varying sputtering pressures of metal layers. The W_{CNT} was decreased from 230 to 6.4 μm by reducing sputtering pressure from 4.0 to 1.2 Pa.

The shady region by metal mask is decreased by reducing sputtering pressure because incident angle variations of sputtered atoms are decreased. Therefore, by reducing sputtering pressure, the metal pattern edge was sharpened and W_{CNT} was reduced.

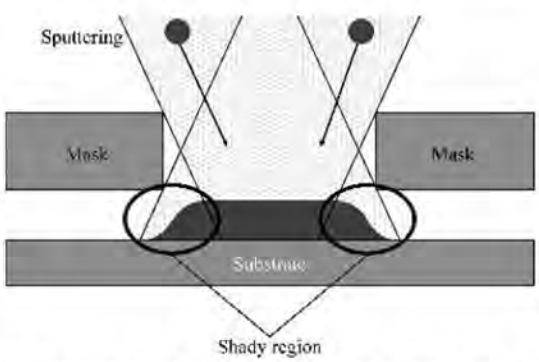

FIG. 4. Schematic of the "shadow effect" that appeared through the mask pattern. The pattern edges thin down because of deposition of shaded sputtered atoms under the mask edges (indicated by the oval).

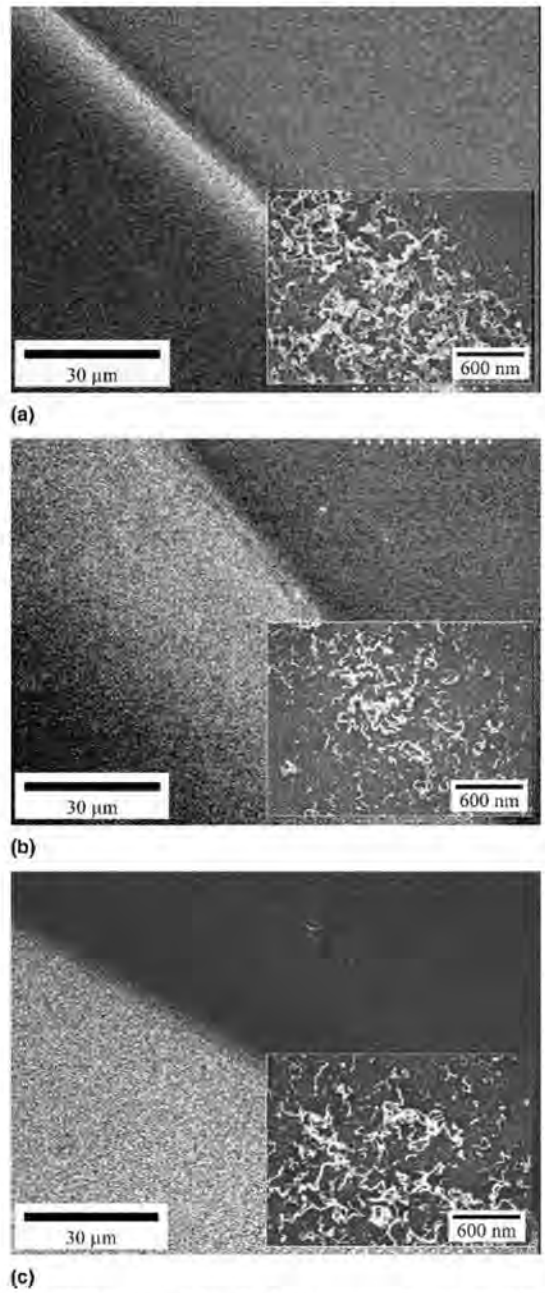

FIG. 5. SEM images of the edge boundary of patterned metal layers after TCVD at varying sputtering pressure of metal layers. The sputtering pressure of the metal layers was (a) 1.2 Pa, (b) 2.0 Pa, and (c) 4.0 Pa. The upper-right at the image is the substrate, the lower-left of the image is the metal pattern. The CNTs grew at narrow region where the contrast of the SEM image is white. The W_{CNT} was (a) 6.4 μm, (b) 26 μm, and (c) 230 μm. The inset shows magnified images.

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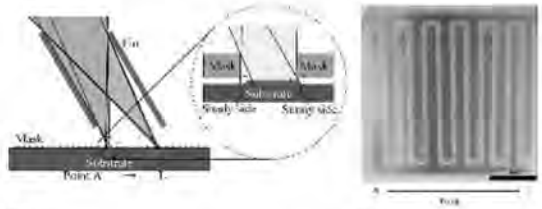
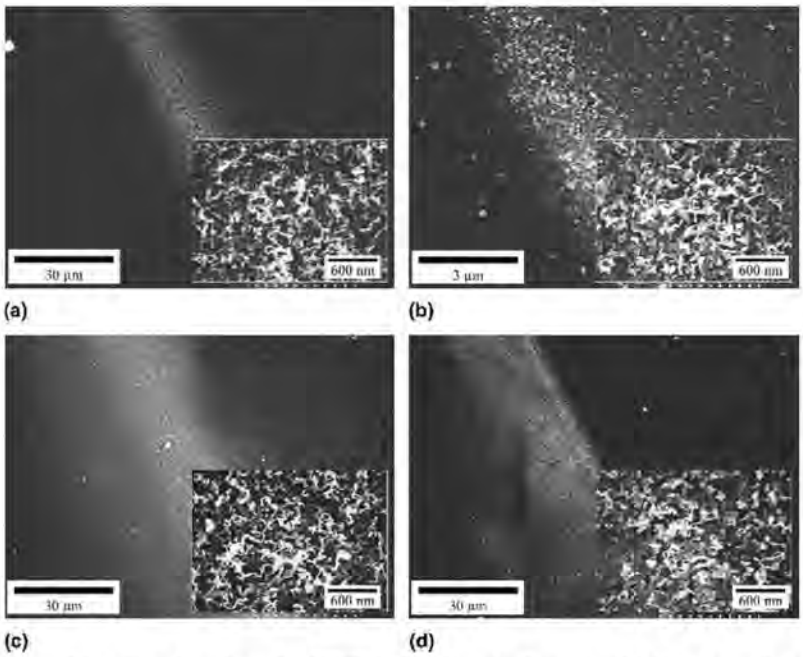


(a) (b)

FIG. 6. (a) Schematic configuration of the aligned fins and the mask. (b) An optical microscopy image of a specimen prepared by installing the fins.

The aligned fins were installed during deposition to control incident angles of sputtered atoms. A schematic configuration of the fins and the metal mask is depicted in Fig. 6(a). The optical microscopy image of the patterned metal, which was sputtered through the fins, is shown in Fig. 6(b). The pattern contrast was not uniform because the metal pattern thickness was not uniform. For that reason, various metal pattern thicknesses can be evaluated simultaneously on this sample. Figure 7 shows typical SEM images of the pattern boundary after TCVD by installing the fins during Mo deposition. Figures 7(a) and 7(b), respectively, show the results on the edges of point D, and Figs. 7(c) and 7(d) show the results on the edges of point K. The images in Figs. 7(a) and 7(c) depict the "shady side"; the upper-right of the image shows the metal pattern. Images in Figs. 7(b) and 7(d) portray the "sunny side"; the lower-left of the image shows the metal pattern. The CNTs grew in the narrow region that appears as the white contrast. The W_{CNT} was (a) 17 μm, (b) 2.6 μm, (c) 29 μm, and (d) 19 μm. The W_{CNT} for every pattern is summarized in Fig. 8. The gray belts correspond to metal mask patterns and white belts correspond to the pattern gaps. The results show that the W_{CNT} was narrower on the "sunny side" than on the "shady side." In addition, the W_{CNT} depended on the position of the pattern. The minimum W_{CNT} was 2.6 μm. This width was approximately one-eightieth of the pattern width.

At pressures of 2.0 Pa, the sputtering condition of the mean free path of sputtered atoms was approximately 6 mm, which was slightly longer than the fin length of 5 mm. The sputtered atoms travel straight through vacancies of the fins. The incident angles of sputtered atoms were limited by the fins. The incident angle distributions were calculated. The width between the maximum and the minimum distance of the shaded area was determined as an effective width considering the shadow effect (W_{SE}). The solid lines in Fig. 8 show the W_{SE}. The gap between the mask and the substrate was fixed as about 5 μm. In calculation results, the W_{SE} was uniform between Points C and I. The respective W_{SE} of sunny and shady sides were 3 and 22 μm. The W_{SE} and W_{CNT} of



(a) (b) (c) (d)

FIG. 7. Typical SEM images of the pattern boundary after TCVD by installing the fins: (a) and (b) results on the edges of point D; (c) and (d) results on point K. The images of (a) and (c) are the "shady side" and the upper-right of the image is the metal pattern. The images of (b) and (d) are the "sunny side" and the lower-left of the image is the metal pattern. The CNTs grew in the narrow region that appears as the white contrast area. The W_{CNT} was (a) 17 μm, (b) 2.6 μm, (c) 29 μm, and (d) 19 μm. The insets show magnified images.

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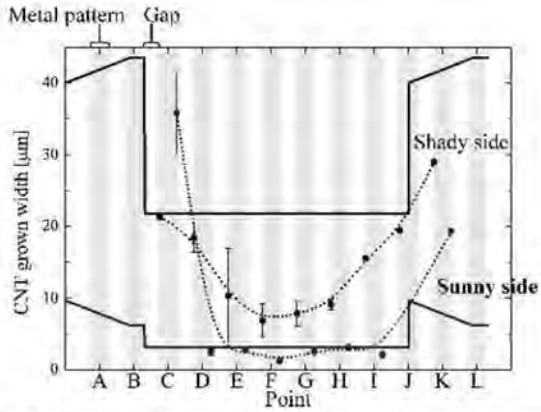

FIG. 8. The W_{CNT} observed at each point in every pattern prepared. The gray belts correspond to the metal mask patterns; white belts correspond to the pattern gaps. The solid lines show the effective width, W_{SE}.

sunny sides were narrower than those of shady sides because the number of atoms that originate from shaded directions under the edges of the mask is reduced by the fins. The W_{CNT} of shady sides depended on the position of the patterns, whereas the calculated W_{SE} was uniform between Point C and I. Figure 6(b) shows that this uniformity was attributable to the nonuniform thickness of the metal pattern. By increasing the thickness of the metal patterns, the W_{CNT} decreased, as discussed above. The thickness distribution resulted from installation of the fins. The W_{SE} and the W_{CNT} increased just under the tail of fins (Points A, B, J, K, and L) because of increased incident angles. The sputtered atoms were deposited through the left and right sides of the fin. Because the W_{SE} contains not only thin and rough regions, but also thick and smooth regions, the W_{SE} was larger than the W_{CNT}.

An electric field was applied during CVD to obtain VACNTs. Figure 9 shows SEM images of CNTs grown using TCVD only, applying a bias without a glow discharge [Fig. 9(a)], and PECVD with a glow discharge accompanying the discharge current [Fig. 9(b)]. The CNTs with an approximate 15-nm diameter grew in various, apparently random, directions using the TCVD method. The CNTs grew selectively near the boundary of the metal pattern. Effects of the applied bias during TCVD were not observed. In the case of PECVD method, CNTs with an approximate 25-nm diameter grew perpendicular to the surfaces. The VACNTs were observed throughout the pattern. Figure 10 shows a TEM image of CNTs grown using PECVD. The hollow center and graphitic sidewalls were observed. In this case, the number of walls was 25, and the CNT internal and external diameters were approximately 4.6 and 26 nm, respectively.

The VACNTs were achieved only through the use of

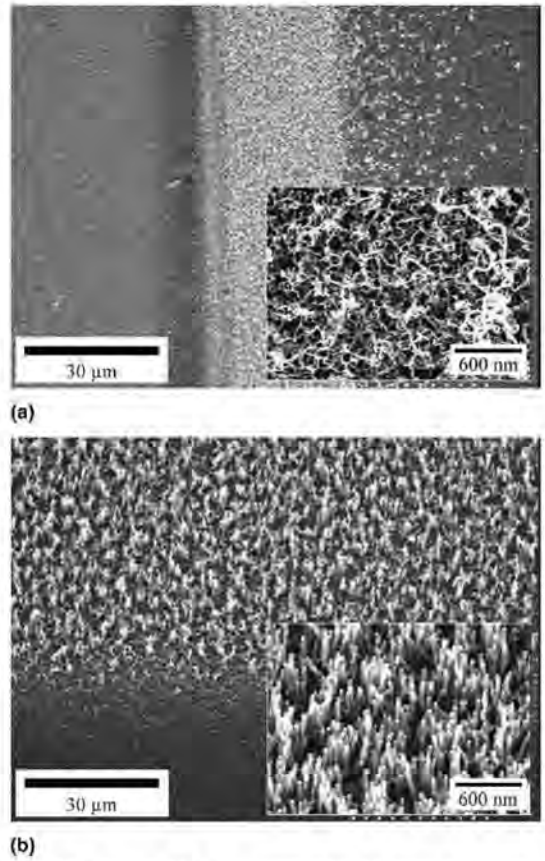

FIG. 9. SEM images of CNTs grown using TCVD only (a) applying bias without a discharge and (b) PECVD with a glow discharge. An applied bias voltage was −300 V [(a) discharge current of approximately 0.005 A]; and −250 V [(b) discharge current of approximately 0.3 A]. Images of (b) were taken at a 45° tilt angle. The inset shows magnified images.

PECVD method. The voltage drop takes place mostly in the cathode dark space when a glow discharge is induced. The thickness of the cathode dark space was estimated using the Child-Langmuir law. The estimated thickness of the cathode dark space was 0.21 mm. Then, the electric field induced above the substrates was approximately 1.2 kV/mm^{-1}. The cathode dark space thickness was estimated in the case of TCVD also. The estimated cathode dark space thickness was 60 mm, which was larger than the distance separating the cathode and anode. Therefore, the electric field might be uniform in the space between the cathode and the anode. The electric field above the substrates was approximately 60 V/mm^{-1}. The electric field applied in the case of PECVD was approximately 20 times larger than that in TCVD. The CNTs grew throughout the pattern by PECVD, whereas selective growth was observed using TCVD. This result suggests that the Ni catalysts were changed into fine particles by bombardment of ions accelerated in a large electric field.

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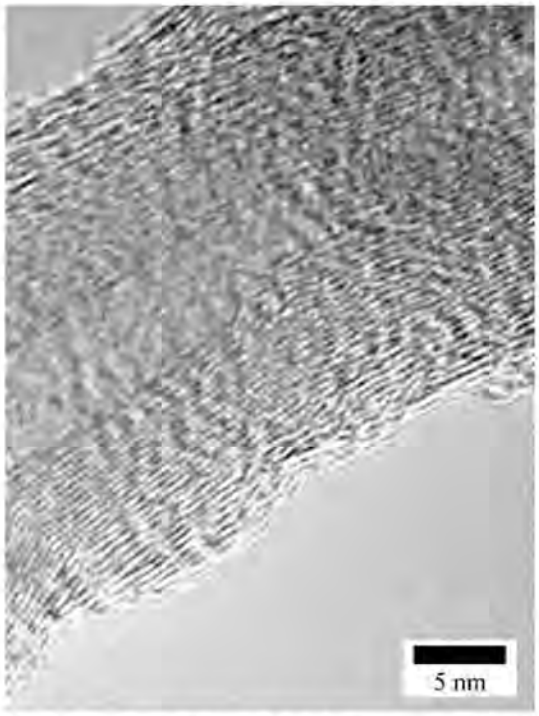

FIG. 10. Typical TEM image of CNTs grown using PECVD.

Results showed that CNTs were able to grow even on the smooth metal patterns.

IV. CONCLUSIONS

We prepared CNTs and VACNTs grown selectively on patterned metal. The selectively grown CNTs were observed at the edges of the patterned metal using TCVD. By controlling not only the catalyst position, but also the surface morphology of their underlayers, the width of selectively grown CNTs was minimized to approximately 2.6 μm. That width was approximately one-eightieth that of the patterned metal, which was 200 μm. To prepare VACNTs, DC-negative bias voltage was applied to the substrates. The VACNTs were synthesized when the glow discharge took place in the PECVD. The VACNTs grew all over the patterned metal. Selective growth of CNTs was achieved in optimum conditions of the TCVD by controlling the morphology of the Mo underlayers for Ni catalysts.

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