

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
31 October 2002 (31.10.2002)

PCT

(10) International Publication Number
WO 02/087294 A1

(51) International Patent Classification⁷: **H05K 1/00**, 3/00

(21) International Application Number: PCT/SG02/00050

(22) International Filing Date: 28 March 2002 (28.03.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
200102200-3 19 April 2001 (19.04.2001) SG

(71) Applicant (*for all designated States except US*): **GUL TECHNOLOGIES SINGAPORE LTD.** [SG/SG]; 149-A Gul Circle, Singapore 629606 (SG).

(72) Inventor; and

(75) Inventor/Applicant (*for US only*): **CHUA, Ah, Lim** [SG/SG]; BLK 326, #04-1348 Yishun Ring Road, Singapore 760326 (SG).

(74) Agent: **LAWRENCE Y D HO & ASSOCIATES PTE LTD**; 30 Bideford Road, #07-01, Thongsia Building, Singapore 229922 (SG).

(81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: A METHOD FOR FORMING A PRINTED CIRCUIT BOARD AND A PRINTED CIRCUIT BOARD FORMED THEREBY

(57) Abstract: Upper, inner and lower sections (182, 180 and 184) of a PCB (100) are formed with each section having a substrate (140, 150 and 160) having patterned layers of metallization (105 and 110, 115 and 120, and 125 and 130), respectively. Some of the patterned layers of metallization (110, 115, 120, and 125) have thicker portions (171, 173) and part (188) of portion (186), and thinner portions (172, 174, 187, 190, 191, 192 and 193). The resultant thinner portion (175 and 194) in the prepreg layers (145 and 155) with the respective thicker portions of metallization provide decoupling capacitors, while the resultant thicker portions (196 and 198), for example, provide a lower capacitance for improved trace impedance for the signal traces (191 and 192).



WO 02/087294 A1

A METHOD FOR FORMING A PRINTED CIRCUIT BOARD AND A PRINTED CIRCUIT BOARD FORMED THEREBY

Field of the Invention

5

The present invention relates to a printed circuit board which reduces electromagnetic interference, and more particularly to a printed circuit board incorporating distributed capacitance therein.

10

Background of the Invention

Printed circuit boards (PCBS) are commonly used to provide a mechanical structure on which discrete electronic components, such as integrated circuits, resistors, capacitors and the like, are mounted and interconnected. The interconnections in a PCB are provided by layers of patterned traces of metal, typically copper, on and in the PCB. To meet more compact requirements, multi-layered PCBS with multiple layers of patterned metal traces are used. Such PCBS comprise alternate layers of insulation and patterned metal traces, with interconnections between the patterned metal traces through the layers of insulation by vertical vias or plated through holes. Typically, in a four layer PCB i.e. one having four patterned layers of metal traces, the two inner most layers provide a common electrical power plane and a common electrical ground plane, respectively, for all the circuitry on the PCB.

25 The operation of circuitry on a multi-layered PCB, especially where there signals at high frequencies of around 50 megahertz or more, causes voltage fluctuations between the power and ground planes. Such fluctuations, often referred to as electromagnetic interference (EMI) or noise, is undesirable. The common ground and common power planes in a multi-layered PCB have a capacitance value which helps to reduce EMI, however for most applications a larger capacitance is required to

30

further reduce the EMI to meet EMI standards set by state regulatory bodies.

A method of controlling EMI is to decouple the power and ground planes by inserting discrete capacitors at various locations on a PCB, particularly at locations where the power and ground planes couple to power input terminals of an integrated circuit mounted on the PCB. A disadvantage of this method is that discrete capacitors consume scarce real estate on the PCB, and in addition, at high frequencies, discrete capacitors become less efficient in providing effective decoupling.

Another relatively new method of controlling EMI is disclosed in US patent 5,079,069 assigned to Zycon Corporation, which provides a capacitive PCB that includes a capacitor laminate having a high capacitance value between the power and ground planes. The capacitor laminate extends through out the PCB, including locations with signal traces. The high capacitance of the capacitor laminate provides effective decoupling of EMI, however, a disadvantage of this method is that the high capacitance value of the capacitor laminate reduces the trace impedance of the signal traces.

This is because the capacitance of the capacitor laminate is inversely proportional to the thickness of the laminate, while signal trace impedance is directly proportional to the thickness of the laminate. Consequently, the high capacitance of the capacitor laminate has a relatively small thickness to provide improved decoupling, but at the same time the small thickness of the capacitor laminate reduces the impedance of the signal traces to below desired impedance values.

The signal trace impedance is inversely proportional to the width of the trace, hence a common method of increasing the signal trace impedance to desired values when using the capacitor laminate is to reduce the width of the signal trace. Therefore, while using the capacitor laminate improves decoupling in a PCB, there is presently a consequent need to reduce the width of signal traces on the PCB to ensure the signal traces have the desired trace impedance values. The

resultant difficulty then when using the capacitor laminate in a PCB is fabricating the relatively narrow traces that are required.

Brief Summary of the Invention

5

The present invention seeks to provide a method for forming a printed circuit board and a printed circuit board formed thereby, which overcomes or at least reduces the abovementioned problems of the prior art.

10 Accordingly, in one aspect, the present invention provides a multi-layered substrate comprising:

 a dielectric layer having a substantially uniform dielectric constant, the dielectric layer having a first surface and a second surface, and the dielectric layer having thicker portions and thinner portions between the first and second surfaces;

15 a first conductive layer on the first surface of the dielectric layer; and

 a second layer comprising a plurality of conductive pieces on the second surface of the dielectric layer,

20 wherein a first of the plurality of conductive pieces, one of the thicker portions of the dielectric layer, and the first conductive layer form a first capacitor, and

 wherein a second of the plurality of conductive pieces, one of the thinner portions of the dielectric layer, and the first conductive layer
25 form a second capacitor.

In another aspect, the present invention provides a printed circuit board comprising:

 at least one dielectric layer having at least a first portion with a first thickness and having at least a second portion with a second
30 thickness, wherein the second thickness is different from the first thickness;

at least a first pair of metallization layers having the at least the first portion therebetween forming a first capacitor with a first value.

at least a second pair of metallization layers having the at least the second portion therebetween forming a second capacitor with a
5 second value different from the first value.

In yet another aspect, the present invention provides a substrate comprising:

a layer of dielectric material having a first surface and a second surface, wherein the second surface is opposite the first surface; and

10 a plurality of conductive portions comprising:

at least a first pair of the plurality of conductive portions,
wherein one of the first pair of the plurality of
conductive portions being disposed in the layer of dielectric material
proximal to the first surface, wherein at least part of the one of the first
15 pair of the plurality of conductive portions extending from the first
surface towards the second surface, and

wherein the other one of the first pair of the plurality
of conductive portions being disposed proximal to the second surface
and being spaced apart from the at least part of the one of the first pair
20 of the plurality of conductive portions by a first distance; and

at least a second pair of the plurality of conductive
portions,

wherein one of the second pair of the plurality of
conductive portions being disposed in the layer of dielectric material
proximal to the first surface, wherein at least part of the one of the
25 second pair of the plurality of conductive portions extending from the
first surface towards the second surface, and

wherein the other one of the second pair of
conductive portions being disposed proximal to the second surface and
30 being spaced apart from the at least part of the one of the second pair of
conductive portions by a second distance, wherein the first distance is
greater than the second distance.

In still another aspect, the present invention provides a method for forming a multi-layered substrate comprising:

- a) forming a plurality of sections, each of the plurality of sections comprising at least one substrate layer and at least one patterned layer of metallization, wherein the patterned layer of metallization has thicker portions and thinner portions;
- b) stacking the plurality of sections with intervening layers of dielectric material;
- c) forming the stack of the plurality of sections and the intervening layers of dielectric material into the multi-layered substrate.

Brief Description of the Drawings

An embodiment of the present invention will now be fully described, by way of example, with reference to the drawings of which:

FIG. 1 shows a cross-sectional view of a printed circuit board in accordance with the present invention;

FIG. 2 shows a flowchart detailing a process for fabricating the PCB in FIG. 1;

FIG. 3 shows a cross-sectional view of an arrangement of the sections the PCB in FIG. 1 in accordance with the process in FIG. 2;

FIG. 4 shows a flowchart detailing a generic process for fabricating the sections of the PCB in FIG. 1;

FIG. 5 shows a flowchart detailing a particular process for fabricating the sections of the PCB in FIG. 1;

FIGS. 6A-C show cross-sectional views of the formation of an inner section of the PCB in FIG. 1 in accordance with the process in FIG. 5;

FIG. 7A-C show cross-sectional views of the formation of an upper section of the PCB in FIG. 1 in accordance with the process in FIG. 5;

FIGS. 8A-B show cross-sectional views of the formation of a lower section of the PCB in FIG. 1 in accordance with the process in FIG. 5;

FIG. 9 shows a flow chart detailing a process for fabricating sections of the PCB in FIG. 1;

FIGS. 10A-C shows cross-sectional views of the formation of the inner section of the PCB in FIG. 1 in accordance with the process in
5 FIG. 9;

FIGS. 11A-C shows cross-sectional views of the formation of the inner section of the PCB in FIG. 1 in accordance with the process in
FIG. 9;

FIG. 12 shows a flowchart detailing another process for fabricating
10 the PCB in FIG. 1; and

FIG. 13 shows cross-sectional views of the formation of the PCB in FIG. 1 in accordance with the process in FIG. 12.

Detail Description of the Drawings

15

The present invention, as described below, provides a dielectric layer in the PCB having varying thickness. Thinner portions of the dielectric layer form decoupling capacitors having a higher capacitance, and thicker portions form capacitors with lower capacitance for trace
20 impedance values within a desired range. This separates the conflicting requirements of decoupling and trace impedance on the dielectric layer in a PCB making each less dependent on the other. Portions of metallization on power and ground planes are made thicker with portions of the dielectric layer between the portions of metallization
25 being made thinner, to produce a higher capacitance for decoupling. Portions of metallization on the ground plane that are aligned with signal traces on a PCB are made thinner resulting in a thicker portion of the dielectric layer between the traces and the ground plane to produce a lower capacitance, advantageously allowing the traces to be
30 made wider without adversely affecting the trace impedance.

In FIG. 1, a six layered printed circuit board (PCB) 100 has six layers of metallization 105, 110, 115, 120, 125 and 130, and five

intervening layers of electrically non-conductive material or insulation 140, 145, 150, 155 and 160. The layers of metallization 105, 110, 115, 120, 125 and 130 are typically made of copper.

The patterned copper layer 105 provides copper interconnections
5 or traces between the components that are mounted on the upper surface of the PCB 100, and is often referred to as the signal layer. Below the copper layer 105 is the layer 140 that is made of electrically insulating materials typically used in the fabrication of PCBs. These materials include epoxy glass FR4, ceramic, and polyimide. The layer
10 140 insulates the copper layer 105 from the next copper layer 110. The layer 110 is a patterned copper layer which provides the common electrical power plane having connections to electrical power. In addition, the layer 110 can provide interconnections in the form of traces for signals. For example, the layer 110 comprises thicker
15 portions 171 that provide power, and thinner portions 172 that are signal traces.

The layer 145 is made of prepreg, such as FR4, Ceramic, Liquid Epoxy & Polyimide, from Nelco, Dupont, Taiyo & Gore with a dielectric constant of 2.5~10.0.

20 The next patterned copper layer 115 has thicker portions 173 and thinner portions 174, and is often referred to as the ground plane as it forms a common electrical ground in the PCB 100. The layer 115 can for example include the thinner portions 174 providing signal traces. The portions 171, associated portions 173, of the patterned copper
25 layers, and portions 175 of the prepreg of layer 145 between the portions 171 and 173, advantageously form distributed decoupling capacitance between the power plane 110 and the ground plane 115.

The layer 150 is a substrate made of electrically insulating material, and may be of similar material to that of the layer 140. The
30 layer 150 together with the patterned copper layers 115 and 120 above and below the layer 150, form an inner section 180 of the PCB 100. Similarly, the layer of insulation 140, the patterned copper layer 105

and the patterned copper layer 110 form an upper section 182, and the layer of insulation 160, the patterned copper layer 130, and the patterned copper layer 125 form a lower section 184, of the PCB 100.

It will be appreciated that the upper and lower sections 182 and 184 are similar in constitution and function. In the lower section 184, the layer 130 is the outer plane, the layer 125 is the power plane and the layer 120 the ground plane.

With reference to the inner section 180, a portion 186 of the patterned copper layer 120 is a part of the ground plane which has a thicker part 188 and a thinner part 189. The thicker part 188 together with an associated portion 190 of the patterned copper layer 125, and a portion 194 of the prepreg layer 155, form decoupling capacitance. The thinner part 189 with associated portions 191 and 192 of the patterned copper layer 125 and portions 196 and 198 of the prepreg layer 155 form a lower capacitance, that results in trace impedance of traces 191 and 192 being within a desired impedance range.

Hence, the relatively smaller thickness of the portion 194 of the prepreg layer 155 between the thicker part 188 and the portion 190 advantageously ensures that the resultant high capacitance between the thicker part 188 and the portion 190 provides decoupling between the ground plane 120 and the power plane 125. In addition, the relatively larger thickness of portions 196 and 198 of the prepreg layer 155 between the thinner part 189 and the traces 191 and 192 produces relatively lower capacitance, advantageously allowing the traces 191 and 192 to be fabricated having relatively larger trace widths but with trace impedances within the desired trace impedance range.

With additional reference to FIG. 2 a process 200 for fabricating the PCB 100 starts 205 with three steps 210, 215 and 220 that are shown being performed concurrently, but can also be performed sequentially. The steps form 210, 215 and 220 form the upper 182, inner 180 and lower 184 sections, of the PCB 100, respectively. Forming 210, 215 and 220 the sections 182, 180 and 184 involves processes that

form the patterned layers of copper 105, 110, 115, 120, 125 and 130 on the substrate layers 140, 150 and 160, respectively.

On the inner section 180 the copper layers 115 and 120 are formed on the substrate layer 150, and on both the upper and lower sections 182 and 184, the copper layers 105 and 110, and 125 and 130, are formed on the substrate layers 140 and 160. In addition, forming the patterned layers of copper 105, 110, 115, 120, 125 and 130 includes forming the patterned layers of copper 110, 115, 120 and 125 with the thinner portions 172, 174, 187, 190, 191, 192, 193 and the part 189, and the thicker portions 171, 173 and the part 188. The process of forming the individual sections will be described in more detail later.

Next, with additional reference to FIG. 3, the three sections 182, 180 and 184 are arranged 225 in a stack 300 with the two alternate layers of prepreg 305 and 310, and with the necessary alignment between the patterned layers of copper on the three sections 182, 180 and 184. Subsequently, the stack 300 of the sections 182, 180 and 184 and the layers of prepreg 305 and 310, is compressed under pressure 230, and the whole assembly is heated 230 to produce the PCB 100, ending 240 the process 200.

With further reference now to FIG. 4, a generic process 400 of forming any one of the sections 182, 180 and 184 starts 405 with providing 410 a substrate. The substrate may be a bare substrate or a laminate comprising an insulating core sandwiched between two layers of copper.

A first layer of metallization is then formed 415 on the substrate in accordance with a first predetermined pattern. When the substrate is a bare substrate, then a process of imaging using photolithography followed by electro-deposition can be used to form the first layer of copper. Alternatively, when the substrate is a laminate, a photolithographic process followed by an etching process is used to form the first layer of metallization. The photolithography, electro-

deposition and etching processes would be understood to one skilled in the art and will not be elaborated herein.

Subsequently, a second layer of metallization is formed 420 in accordance with a second predetermined pattern, over the substrate and the first layer of metallization. Whether the first layer of metallization was formed by the deposition or the etching processes, the second layer of metallization is formed by the photolithography and the electro-deposition processes. The process 400 then ends 425.

With the process 400, the first layer of metallization is formed with a predetermined thickness, and the second layer of metallization is formed on portions of the first layer of metallization in accordance with the first and second predetermined patterns. In this way, selected portions of the resulting layers of metallization have a larger thickness relative to other non-selected portions.

With due regard to the practical constraints of materials that are available from material suppliers, and the processes commonly employed in PCB manufacturing facilities, an alternative process for fabricating the sections 182, 180 and 184, now follows.

Referring now to FIGS. 5, 6A-C, 7A-C, 8A-B, a process 500 for making the inner, upper and lower sections 182, 180 and 184 starts 505 with providing a laminate 600, 700 and 800 which have a middle layer of insulation 150, 140, and 160, sandwiched between two layers of unpatterned copper layers, 605 and 610, 105 and 705, and 805 and 130, respectively. This is followed by photolithographic imaging and etching 515 to form one or both of the layers of copper on the substrate, in accordance with a first predetermined pattern. Of course, the first predetermined pattern of copper has a first uniform thickness which is equal to the original thickness of the copper layers. The photolithographic and etching processes simply removes the portions of the copper layers that are not required.

On the laminate 600, the copper layer 605 is etched to leave portions 614, 174, and 612, and the copper layer 610 is etched to leave

portions 187 and 186 with part 189, thus producing etched laminate 601. On laminate 700, the copper layer 705 is etched to form portions 710 and 172, thus producing etched laminate 701. And, on laminate 800, the copper layer 805 is etched to form portions 190, 191, 192 and 193, to produce the lower section 184.

Subsequently, after imaging with a second photolithographic process, in accordance with a second predetermined pattern, an electro-deposition process 520 builds up thicker portions on some of the portions of the first layer of metallization. The etched laminate 601 has copper layers 616, 618 and 620 deposited thereon to form the inner section 182. Similarly, the etched laminate 701 has copper layers 715 and 717 deposited thereon to form the upper section 182. As indicated earlier, after etching, the laminate 800 becomes the lower section 184 as it does not require thicker portions to be formed thereon.

Returning briefly to FIG. 4, if in the process 400, the substrate provided in step 410 has a layer of metallization of sufficient thickness to form the thicker conductive portions, an alternative process 900 for fabricating the inner, upper and lower sections 180, 182 and 184 can be employed, and will now be described.

With reference to FIGS. 9 and 10A-C the process 900 will now be described for making the inner section 180, however, the process can be used to make the upper and lower sections 182 and 184, as will be appreciated by one skilled in the art based on the description that follows, without significant variation.

The process 900 starts 905 with providing 910 a laminate 1000 having a middle substrate layer 1005 and upper and lower layers of copper 1010 and 1020. Using the processes of photolithography and etching, the copper layers 1010 and 1020 are etched 915 in accordance with a first predetermined pattern to leave portions 1021, 1023, 1025, 1027 and 1029, all having a first thickness, on the substrate 1005, thus producing etched substrate 1001.

Subsequently, the processes of photolithography and etching are applied a second time to the etched substrate 1001 to etch 920 the portions 1023, 1027 and part of 1029, which produces substrate 1002 having portions 130, 132, 133 and 134 with a second thickness that is less than the first thickness. After the second etching 920, the process 900 ends 925. Note that the resultant etched substrate 1002 is identical to the inner section 180.

Alternatively, with reference to FIGS. 9 and 11A-C, the two step etching process 900 using a different set of first and second etching patterns can be used to produce the inner section 180, and as will be understood by one skilled in the art, is also applicable to the formation of the upper and lower sections 182 and 184 without significant variation.

As before, the process 900 starts with providing the laminate 1000 having a middle substrate layer 1005 and upper and lower layers of copper 1010 and 1020. Then using the processes of photolithography and etching, the copper layers 1010 and 1020 are etched 910 in accordance with an alternative first predetermined pattern to leave portions 1121, 1122 and 1123 unaffected by etching, and having the original first thickness of the copper layers 1010 and 1015. The etching 910 etches away parts of the copper layers 1010 and 1015 to leave portions 1105, 1110, 1115, 1120 and 1125 having a second thickness which is less than the first thickness. This produces an etched laminate 1101 which is subsequently etched 920 a second time in accordance with an alternative second predetermined pattern. The second etching produces the etched laminate 1102 having thicker copper portions, i.e. the first thickness, 1121, 1122 and 1123, and thinner copper portions, i.e. the second thickness, 1131, 1132, 1133 and part 1125. As a result, the etched laminate 1102 is identical to the inner section 180.

Referring now to FIGS. 12 and 13A-E, an alternative process for forming the PCB 100 starts 1205 with forming 1210 the inner, upper and lower sections 180, 182 and 184. Any of the processes 500 or 900,

as described earlier can be used to form the sections inner, upper and lower sections 180, 182 and 184. Next, insulating layers 1310 and 1320 are formed 1215 having contoured surfaces 1311 and 1312, and 1321 and 1322, respectively. The insulating layers 1310 and 1320 can be
5 made of preformed prepreg which may be fabricated with a molding process. Such molding processes include injection and/or transfer molding as will be known to one skilled in the art.

Alternatively, the insulating layers 1310 and 1320 can be formed of any suitable dielectric material and appropriate adhesive or bonding
10 agents employed to bind 1225 the insulating layers 1310 and 1320 and the sections 180, 182 and 184 together, under imposed heat and pressure.

The insulating layers 1310 and 1320 can be formed using the same processes. Taking the insulating layer 1310, as an example, the
15 contoured surface 1311 is formed having deeper contoured portions 1313 and shallower contoured portions 1314, and the contoured surface 1312 is formed having deeper contoured portions 1315 and shallower contoured portions 1316. The contoured portions 1313 and 1314 complement the portions 171 and 172 on the patterned layer of
20 metallization 110, such that the contoured portions 1313 and 1314 fit with the portions 171 and 172 on the patterned layer of metallization 110.

Similarly, the contours 1315 and 1316 complement the portions 173 and 174 on the patterned layer of metallization 115, and the same
25 fitting applies for the insulation layer 1320 and the patterned layers of metallization 120 and 125.

As the layers of insulation 1310 and 1320 are preformed before assembly, the thickness at various portions of the layers of insulation 1310 and 1320 are predetermined. As the thickness of the layer of
30 insulation determines the capacitance, the predetermined thickness at various portions of the layer of insulation advantageously determines the capacitance at the desired portions of the completed PCB.

The present invention, as described, provides a capacitive printed circuit board having more easily manufactured wider traces that have required trace impedance.

5 This is accomplished by a dielectric layer in a PCB having thicker portions that form decoupling capacitors between power and ground planes, and thinner portions that form capacitors having a lower capacitance that provide desired trace impedance for signal traces in the PCB.

10 The present invention therefore provides a method for forming a printed circuit board and a printed circuit board formed thereby, which overcomes or at least reduces the abovementioned problems of the prior art.

15 It will be appreciated that although only one particular embodiment of the invention has been described in detail, various modifications and improvements can be made by a person skilled in the art without departing from the scope of the present invention.

Claims

1. A multi-layered substrate comprising:
 - a dielectric layer having a substantially uniform dielectric
 - 5 constant, the dielectric layer having a first surface and a second surface, and the dielectric layer having thicker portions and thinner portions between the first and second surfaces;
 - a first conductive layer on the first surface of the dielectric layer;
 - and
 - 10 a second layer comprising a plurality of conductive pieces on the second surface of the dielectric layer,
 - wherein a first of the plurality of conductive pieces, one of the thicker portions of the dielectric layer, and the first conductive layer form a first capacitor, and
 - 15 wherein a second of the plurality of conductive pieces, one of the thinner portions of the dielectric layer, and the first conductive layer form a second capacitor.
2. A multi-layered substrate in accordance with claim 1 wherein the
- 20 first conductive layer comprises a plurality of conductive pieces,
 - wherein the first of the plurality of conductive pieces of the second layer, the one of the thicker portions of the dielectric layer, and a first of the plurality of conductive pieces of the first conductive layer form the first capacitor, and
 - 25 wherein the second of the plurality of conductive pieces of the second layer, the one of the thinner portions of the dielectric layer, and a second of the plurality of conductive pieces of the first conductive layer form the second capacitor.
- 30 3. A multi-layered substrate in accordance with claim 2 wherein the first of the plurality of conductive pieces of the second layer, the one of the thicker portions of the dielectric layer, and the first of the plurality

of conductive pieces of the first conductive layer are substantially aligned along a first common axis extending between the first conductive layer and the second layer.

5 4. A multi-layered substrate in accordance with claim 2 wherein the second of the plurality of conductive pieces of the second layer, the one of the thinner portions of the dielectric layer, and the second of the plurality of conductive pieces of the first conductive layer are substantially aligned along a second common axis extending between
10 the first conductive layer and the second layer.

5. A multi-layered substrate in accordance with claim 2 wherein the first and second of the plurality of conductive pieces of the first conductive layer have substantially unequal thickness extending from a
15 first common plane.

6. A multi-layered substrate in accordance with claim 2 wherein the first and second of the plurality of conductive pieces of the first conductive layer have substantially equal thickness extending from a
20 first common plane.

7. A multi-layered substrate in accordance with claim 2 wherein the first and second of the plurality of conductive pieces of the second layer have substantially equal thickness extending from a common plane.
25

8. A multi-layered substrate in accordance with claim 2 wherein the first and second of the plurality of conductive pieces of the second layer have substantially unequal thickness extending from a common plane.

30 9. A printed circuit board comprising:
at least one dielectric layer having at least a first portion with a first thickness and having at least a second portion with a second

thickness, wherein the second thickness is different from the first thickness;

at least a first pair of metallization layers having the at least the first portion therebetween forming a first capacitor with a first value.

5 at least a second pair of metallization layers having the at least the second portion therebetween forming a second capacitor with a second value different from the first value.

10. A multi-layered substrate in accordance with claim 9 wherein the
10 at least one dielectric layer comprises a contoured dielectric layer having a range of thickness including the first thickness and the second thickness to provide a range of capacitor values.

11. A multi-layered substrate in accordance with claim 9, wherein at
15 least one of each of the first and second pairs of metallization layers are substantially aligned with a horizontal plane.

12. A substrate comprising:

a layer of dielectric material having a first surface and a second
20 surface, wherein the second surface is opposite the first surface; and

a plurality of conductive portions comprising:

at least a first pair of the plurality of conductive portions,
wherein one of the first pair of the plurality of
conductive portions being disposed in the layer of dielectric material
25 proximal to the first surface, wherein at least part of the one of the first pair of the plurality of conductive portions extending from the first surface towards the second surface, and

wherein the other one of the first pair of the plurality
of conductive portions being disposed proximal to the second surface
30 and being spaced apart from the at least part of the one of the first pair of the plurality of conductive portions by a first distance; and

at least a second pair of the plurality of conductive portions,

wherein one of the second pair of the plurality of conductive portions being disposed in the layer of dielectric material proximal to the first surface, wherein at least part of the one of the second pair of the plurality of conductive portions extending from the first surface towards the second surface, and

wherein the other one of the second pair of conductive portions being disposed proximal to the second surface and being spaced apart from the at least part of the one of the second pair of conductive portions by a second distance, wherein the first distance is greater than the second distance.

13. A method for forming a multi-layered substrate comprising:

- a) forming a plurality of sections, each of the plurality of sections comprising at least one substrate layer and at least one patterned layer of metallization, wherein the patterned layer of metallization has thicker portions and thinner portions;
- b) stacking the plurality of sections with intervening layers of dielectric material;
- c) forming the stack of the plurality of sections and the intervening layers of dielectric material into the multi-layered substrate.

14. A method in accordance with claim 13, wherein step (a) comprises the steps of:

- d) providing a substrate;
- e) forming a first patterned layer of metallization on at least one surface of the substrate;
- f) forming a second patterned layer of metallization on the first patterned layer of metallization.

15. A method in accordance with claim 14, wherein step (e) comprises the steps of:

- forming a first mask on the at least one surface of the substrate;
- depositing metal on the masked at least one surface; and
- 5 stripping the first mask.

16. A method in accordance with claim 14, wherein step (f) comprises the steps of:

- forming a second mask on the first patterned layer of
- 10 metallization on at least one surface of the substrate; and
- depositing metal on the masked first patterned layer of
- metallization on the at least one surface of the substrate
- stripping the second mask.

15 17. A method in accordance with claim 13, wherein step (a) comprises the steps of:

- g) providing a laminate having a substrate layer and a layer of metallization;
- h) etching the layer of metallization in accordance with the first
- 20 predetermined pattern to produce an etched laminate; and
- i) etching the etched laminate in accordance with the second predetermined pattern of metallization.

18. A method in accordance with claim 17, wherein step (h) comprises the steps of:

- forming a first mask on the on the layer of metallization;
- exposing the masked layer of metallization to an etchant that
- removes exposed portion of the layer of metallization; and
- stripping the first mask.

30

19. A method in accordance with claim 17, wherein step (i) comprises the steps of:

forming a second mask on the etched laminate;
exposing the masked etched laminate to an etchant that removes
exposed portion of the layer of metallization; and
stripping the second mask.

5

20. A method in accordance with claim 13, wherein step (a) comprises the steps of:

j) providing a laminate having a substrate layer and a layer of metallization;

10 k) etching the layer of metallization in accordance with a first predetermined pattern to produce an etched laminate; and

l) forming a layer of metallization on the etched laminate in accordance with a second predetermined pattern.

15 21. A method in accordance with claim 20, wherein step (k) comprises the steps of:

forming a first mask on the layer of metallization in accordance with the first predetermined pattern;

20 exposing the masked layer of metallization to an etchant that removes exposed portions of the layer of metallization; and
stripping the first mask.

22. A method in accordance with claim 20, wherein step (l) comprises the steps of:

25 forming a second mask on the etched layer of metallization in accordance with the second predetermined pattern;

depositing metal on exposed portions of the etched layer of metallization; and

stripping the second mask.

30

23. A method in accordance with claim 13, prior to step (b) comprises the step of providing the layers of dielectric material.

24. A method in accordance with claim 23, wherein the step of providing the layers of dielectric material comprises the step of providing pre-cut layers of prepreg.

5 25. A method in accordance with claim 23, prior to the step of providing the layers of dielectric material comprises the step of forming the layers of dielectric material.

26. A method in accordance with claim 25, wherein the step of
10 forming the layers of dielectric comprises the step of molding the layers of dielectric material.

27. A method in accordance with claim 13, wherein step (c) comprises the step of aligning the at least one patterned layer of metallization in
15 each of the plurality of sections and the intervening layers of dielectric material.

28. A method in accordance with claim 27, wherein step (c) further comprises the step of disposing adhesive between the plurality of
20 sections and the intervening layers of dielectric material.

29. A method in accordance with claim 27, wherein step (c) further comprises the step of applying pressure to compress the at least one patterned layer of metallization in each of the plurality of sections and
25 the intervening layers dielectric material.

30. A method in accordance with claim 29, wherein step (c) further comprises the step of applying heat.

1/13

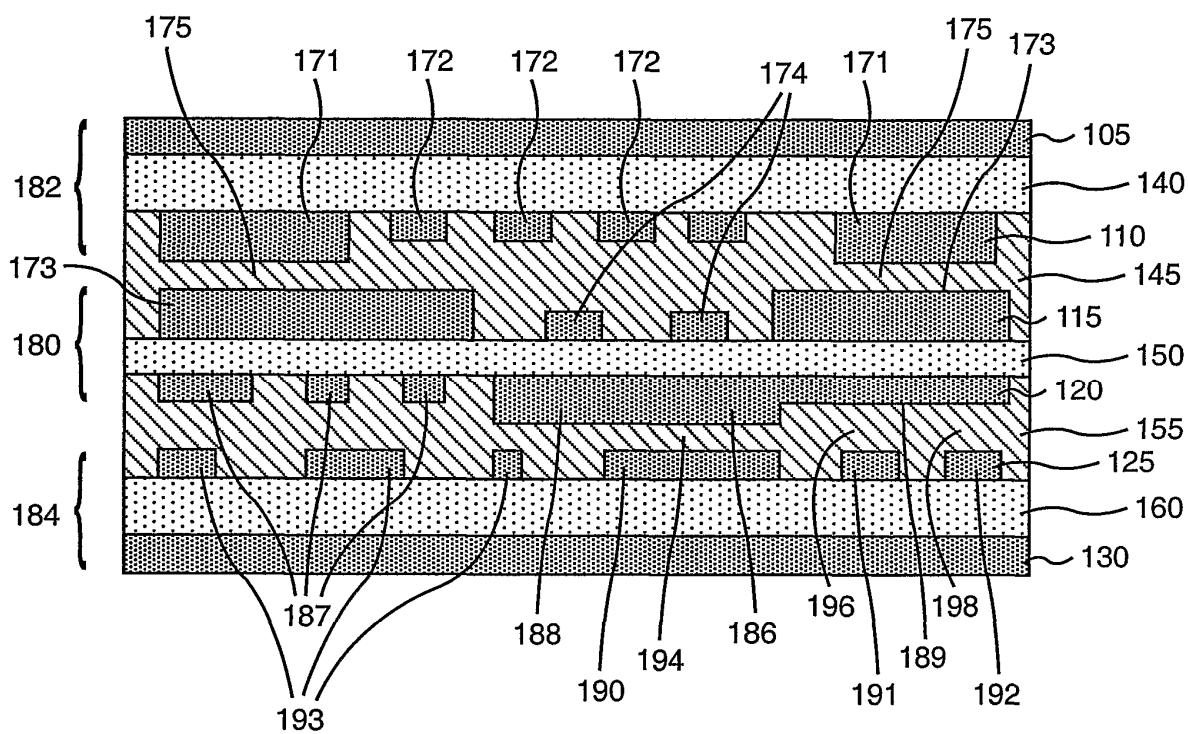
100

FIG. 1

2/13

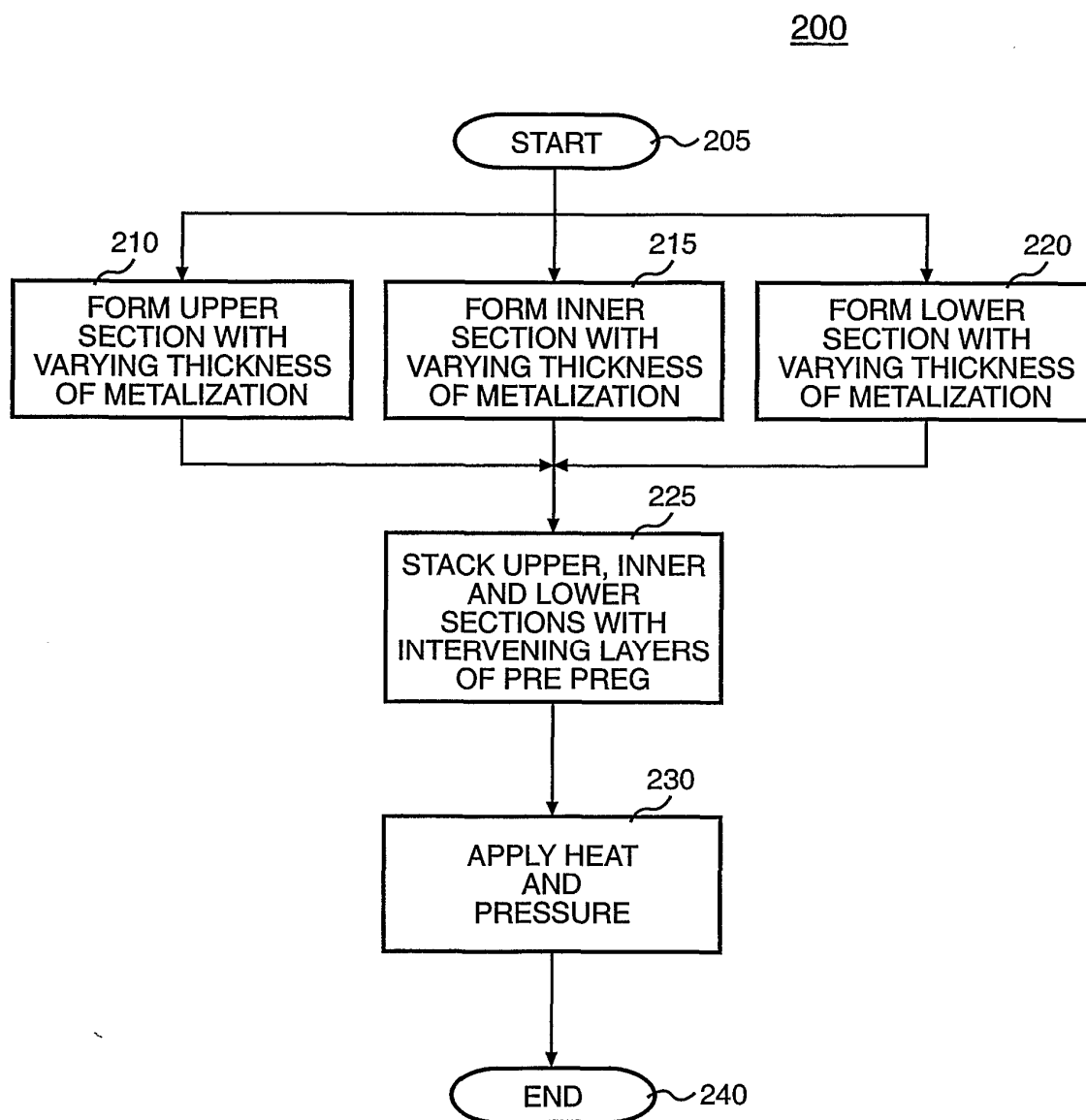


FIG. 2

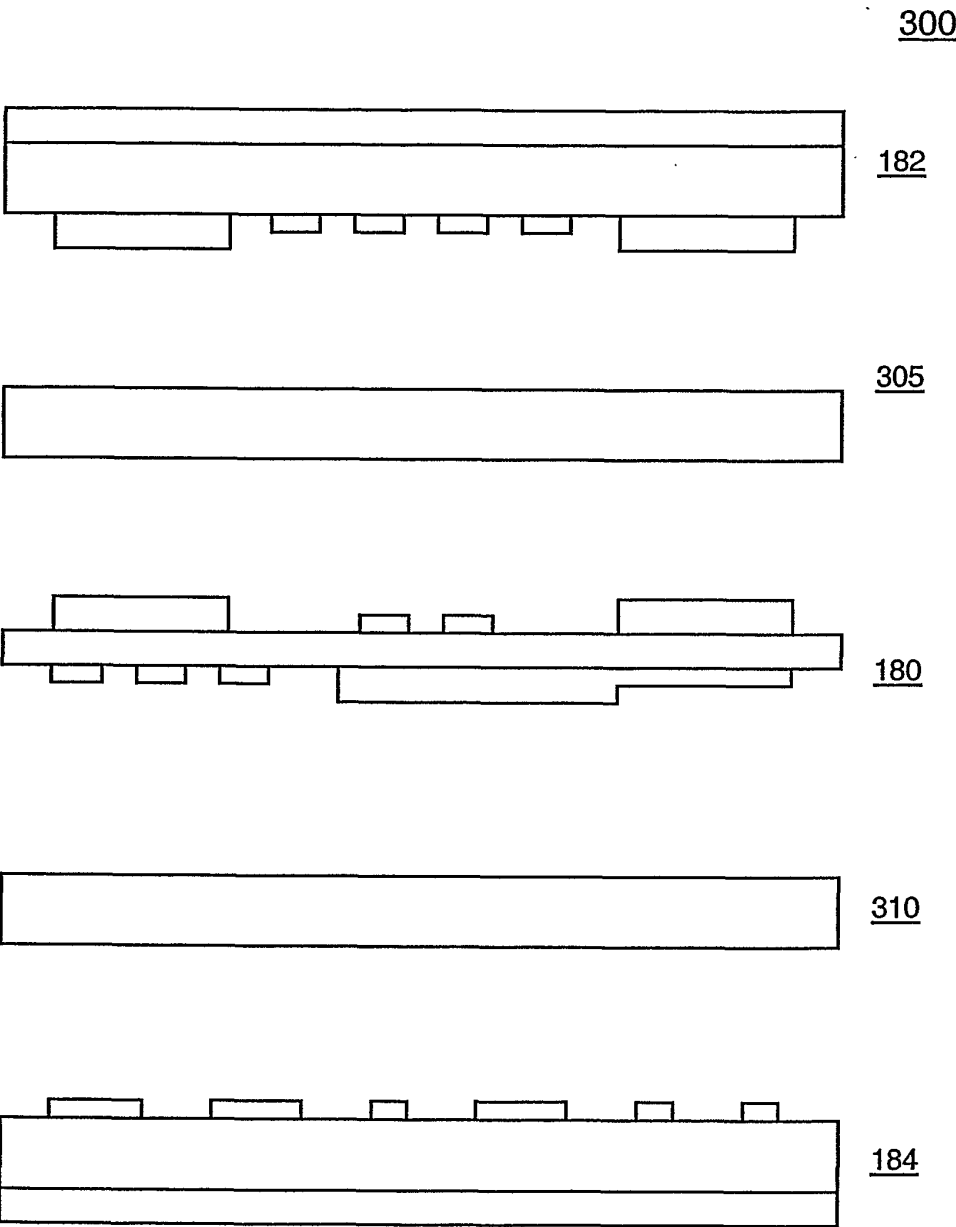


FIG. 3

4/13

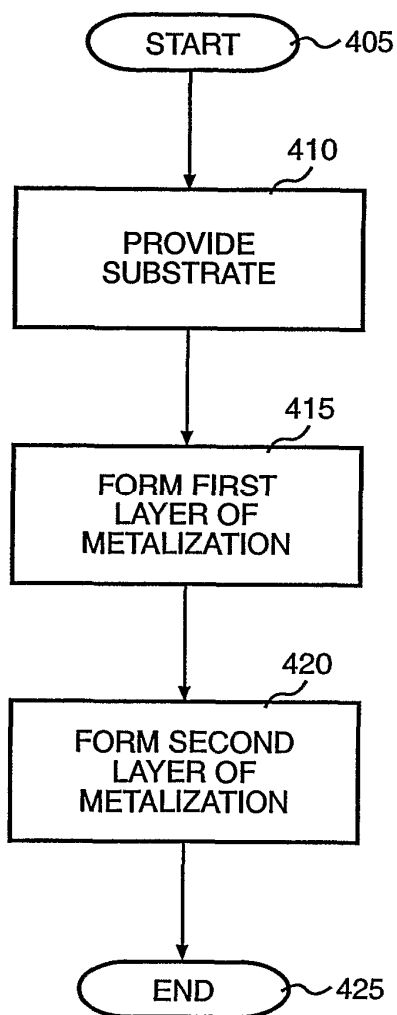
400

FIG. 4

5/13

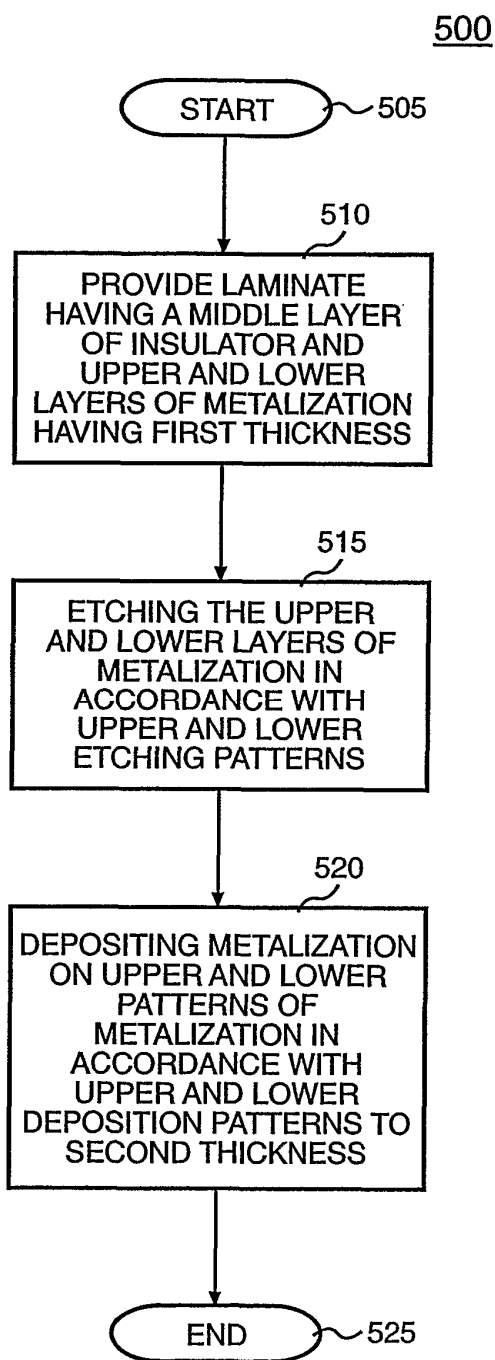


FIG. 5

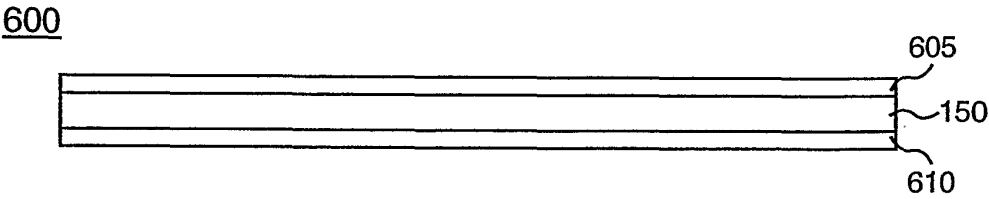


FIG. 6A

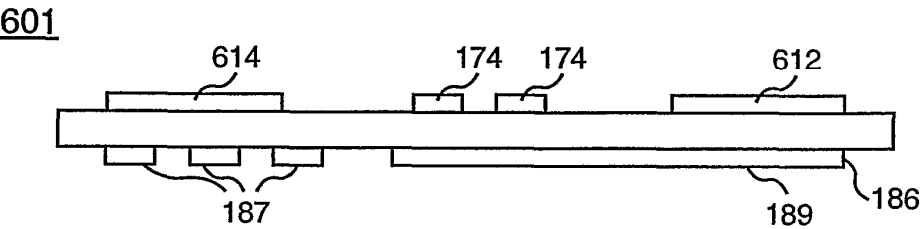


FIG. 6B

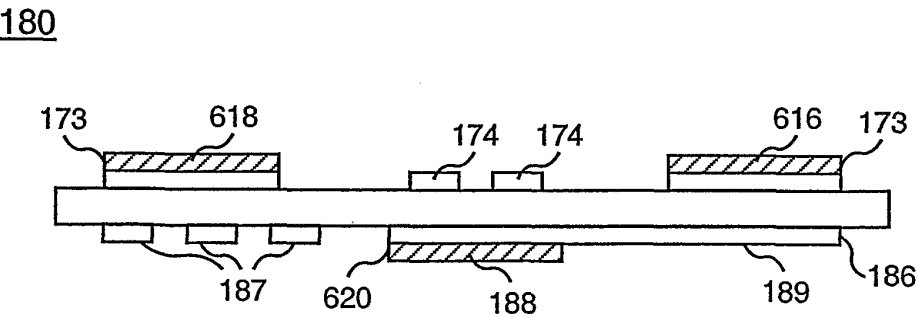


FIG. 6C

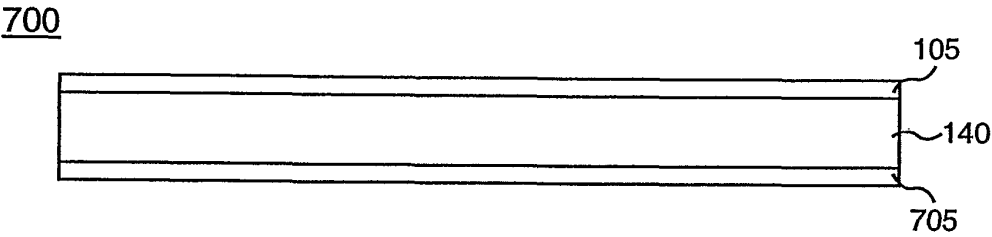


FIG. 7A

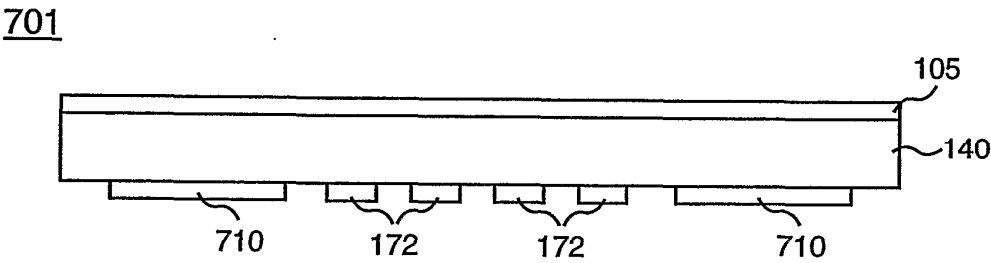


FIG. 7B

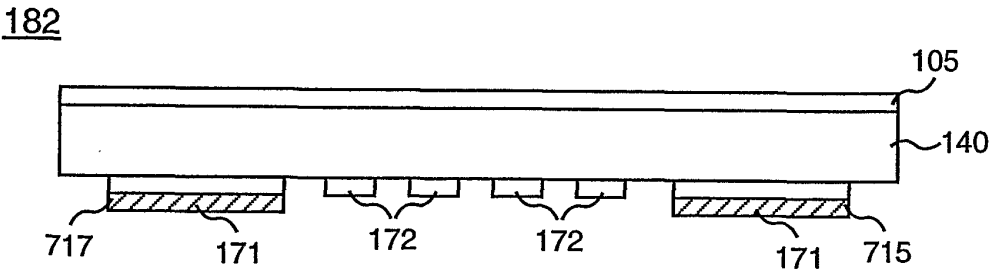


FIG. 7C

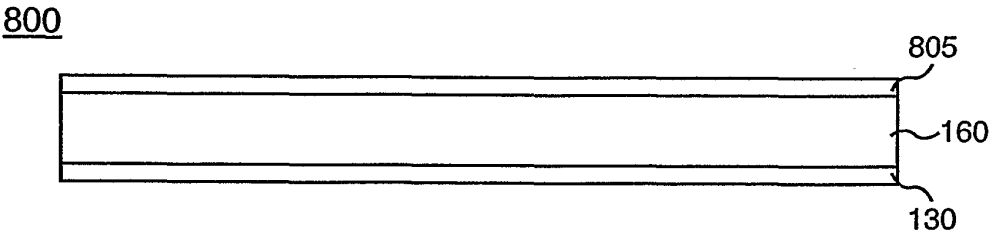


FIG. 8A

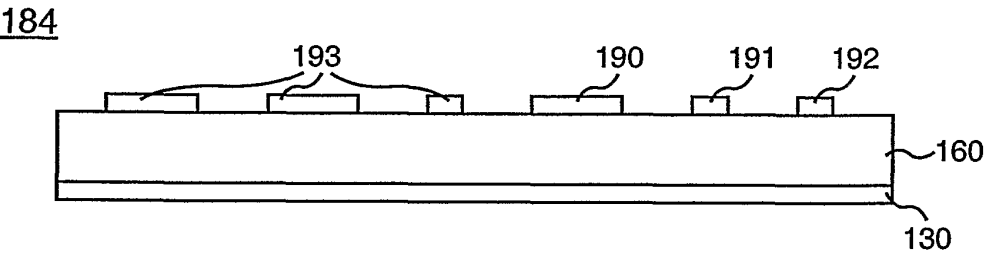


FIG. 8B

9/13

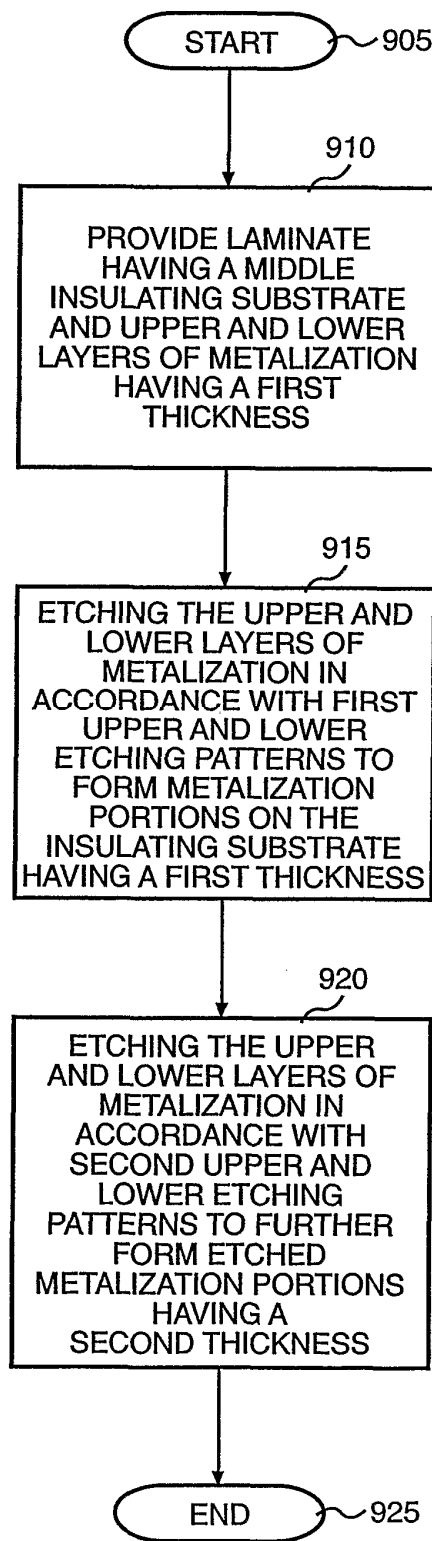
900

FIG. 9

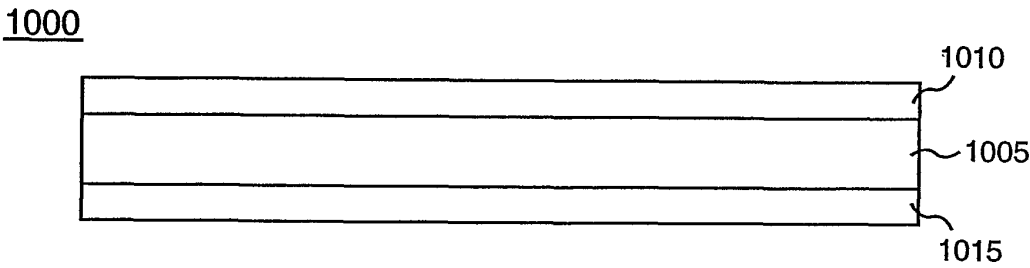


FIG. 10A

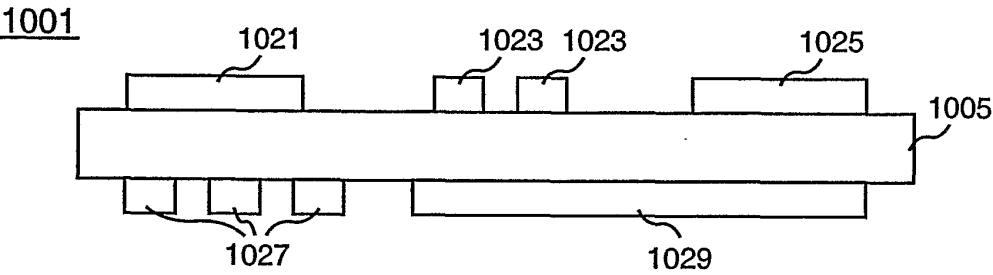


FIG. 10B

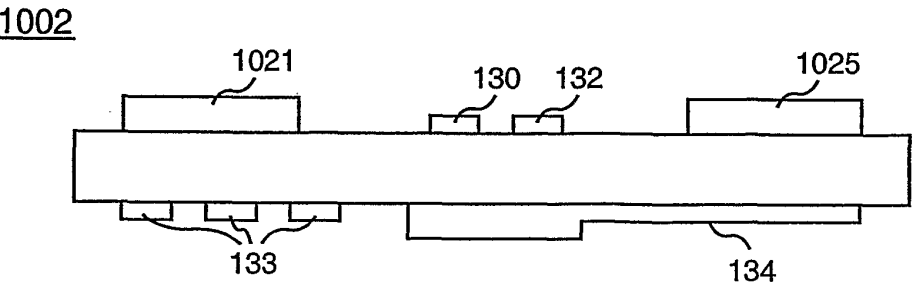


FIG. 10C

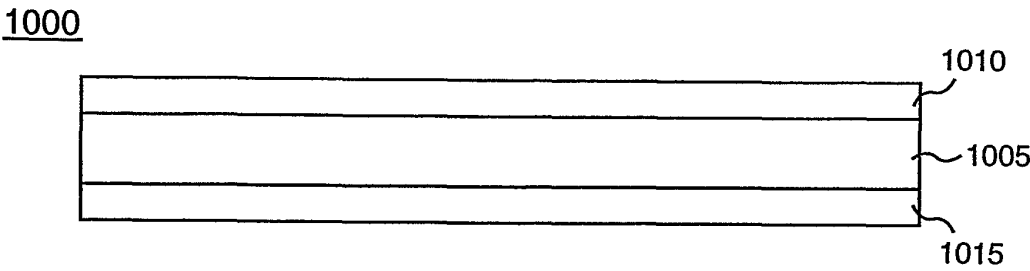


FIG. 11A

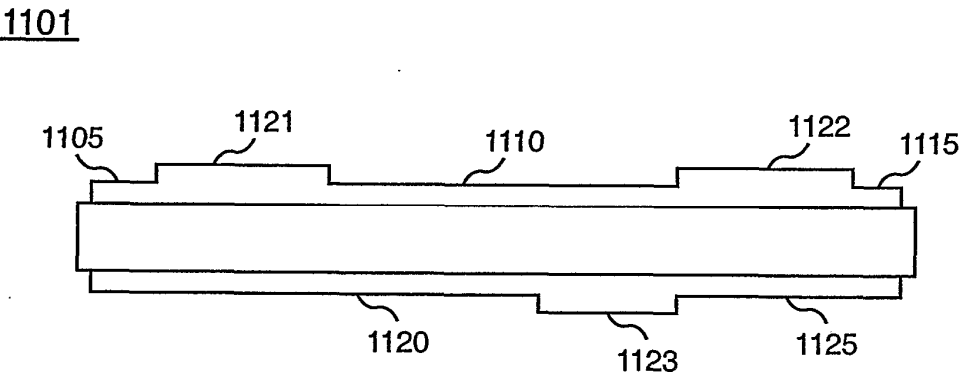


FIG. 11B

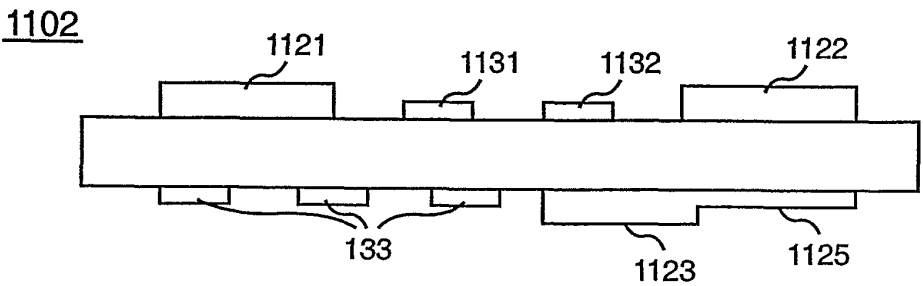


FIG. 11C

12/13

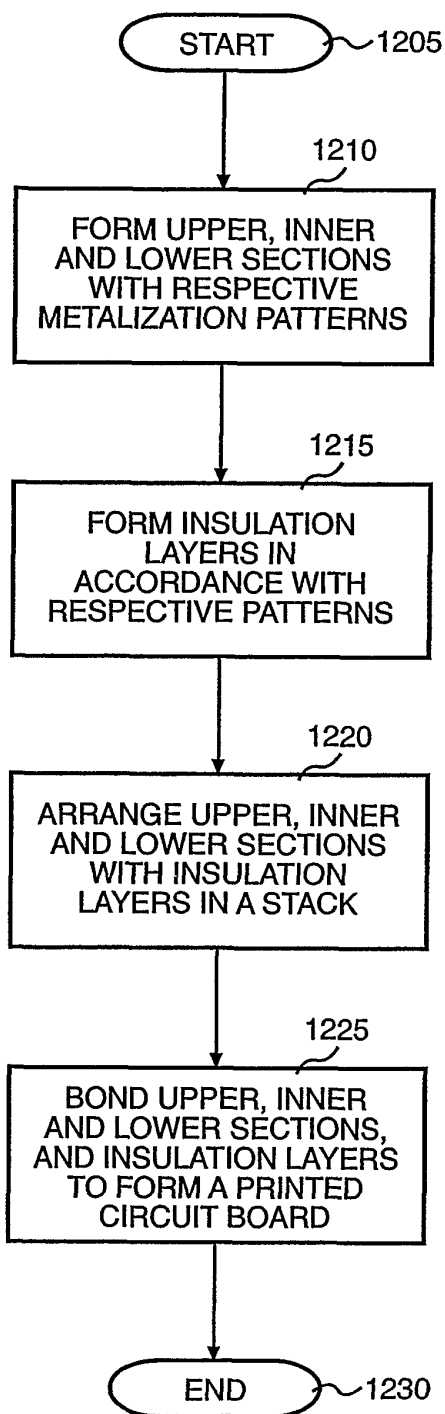
1200

FIG. 12

13/13

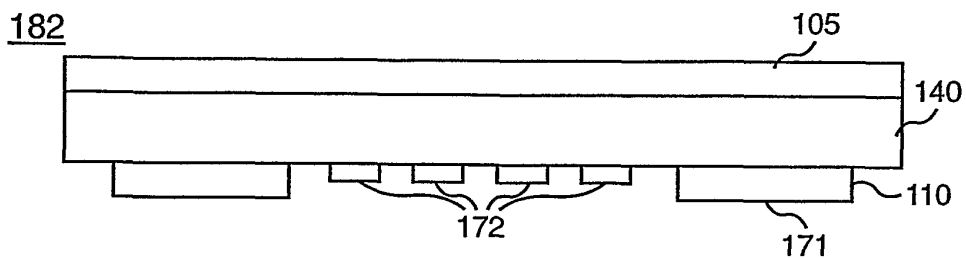


FIG. 13A

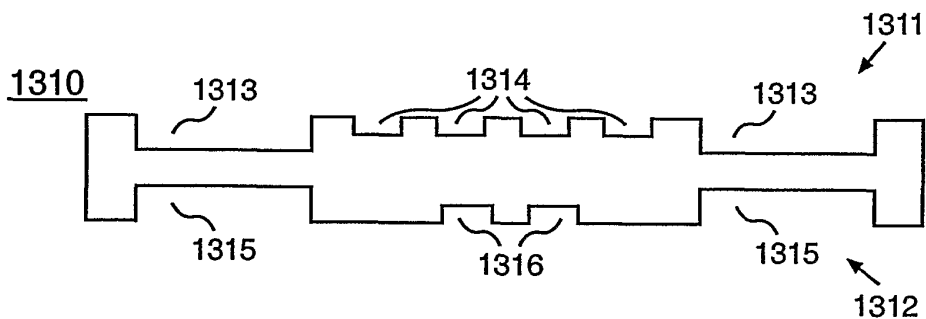


FIG. 13B

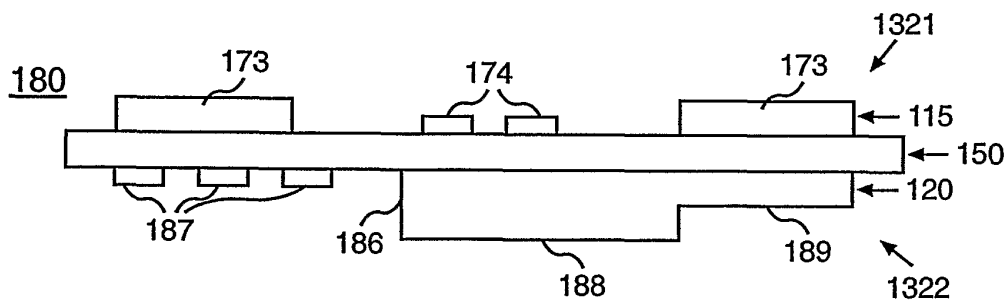


FIG. 13C

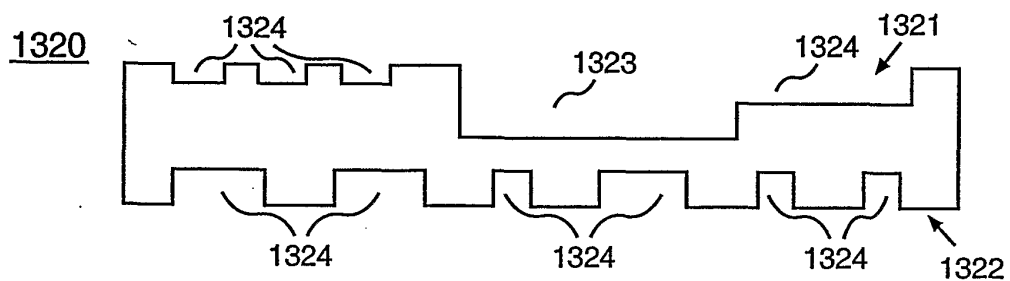


FIG. 13D

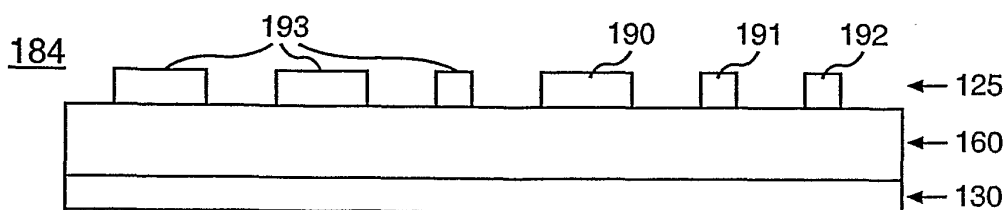


FIG. 13E

INTERNATIONAL SEARCH REPORT

International application No.

PCT/SG02/00050

A. CLASSIFICATION OF SUBJECT MATTER		
Int. Cl. ⁷ : H05K 1/00, 3/00		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
REFER ELECTRONIC DATA BASE CONSULTED BELOW		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
DWPI IPC H05K, H01L 21/-, 23/-, 27/-, H01G & keywords: PCB, PRINTED CIRCUIT, LAYER, THICK, THIN, CAPACIT, DIELECTRIC, METAL, PIECE, PATCH and similar terms		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6068782 (BRANDT ET AL) A 30 May 2000 See whole document	1-30
A	US 5010641 (SISLER) A 30 April 1991 See whole document	
A	US 5261153 (LUCAS) A 16 November 1993 See whole document	
☐ Further documents are listed in the continuation of Box C ☒ See patent family annex		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search		Date of mailing of the international search report
13 May 2002		22 MAY 2002
Name and mailing address of the ISA/AU		Authorized officer
AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaaustralia.gov.au Facsimile No. (02) 6285 3929		DALE SIVER Telephone No : (02) 6283 2196

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/SG02/00050

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report	Patent Family Member
US 6068782	WO 9941019
US 5261153	
US 5010641	
END OF ANNEX	