

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, AND
SAMSUNG ELECTRONICS AMERICA, INC.,

Petitioner,

v.

HARBOR ISLAND DYNAMIC, LLC,

Patent Owner.

Case IPR2024-01402
U.S. Patent No. 7,745,886

**DECLARATION OF DR. SCOTT E. THOMPSON, PH.D.,
IN SUPPORT OF PETITION FOR INTER PARTES REVIEW OF
UNITED STATES PATENT NO. 7,745,886**

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I. INTRODUCTION

1. I, Scott E. Thompson, Ph.D., have been retained as an independent expert by Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc. (“Petitioner” or “Samsung”) in connection with an *inter partes* review (IPR) of U.S. Patent No. 7,745,886 (“the ’886 patent”) (Ex. 1001). I have prepared this declaration in connection with Samsung’s Petition for *Inter Partes* Review.

2. Specifically, this document contains my opinions about the technology in claims 1-19 of the ’886 patent and the grounds against these claims that have been asserted by Samsung. I was not asked to provide any opinions about the ’886 patent that are not expressed herein.

II. SUMMARY OF OPINIONS

3. This declaration considers claims 1-19 of the ’886 patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for these opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

4. Based on my experience, knowledge of the art at the time of the applicable priority date (I was told to assume a priority date of December 10, 2007), it is my opinion that claims 1-19 of the ’886 patent would have been anticipated and/or obvious based on the asserted grounds discussed below.

5. I am being compensated for my time at my normal hourly rate. My compensation is in no way contingent upon the nature of my findings, the presentation of my findings in testimony, or the outcome of this proceeding.

III. QUALIFICATIONS AND BACKGROUND

6. I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below. A copy of my curriculum vitae is attached as Appendix A to this declaration.

7. Based on my education, research, and work experience, I am knowledgeable about the subject matter of the '886 patent and the related prior art.

8. I have over 30 years of academic and industrial experience in designing, applying, studying, teaching, manufacturing and writing about semiconductor devices, microprocessors, and computer chip technologies, including the design, process integration, fabrication, and yield of various types of semiconductor devices.

9. I received my Bachelor of Electrical Engineering with Highest Honors from the University of Florida in 1987. I also received my Master of Science of Electrical Engineering in 1988 and my Ph.D. in Electrical Engineering in 1992, both from the University of Florida. My Ph.D. was funded by the Semiconductor Research Corporation. My Ph.D. dissertation studied CMOS integrated circuits, and I did extensive measurements and fabrication of CMOS test structures. My

Ph.D. dissertation earned a best paper award from the Semiconductor Research Corporation and a Best Ph.D. award from the University of Florida.

10. In 1992, after receiving my Ph.D., I joined Intel working on research and development of CMOS integrated circuits. From 1992 to 2004, I worked in Integrated Circuit development and semiconductor manufacturing. During this time, I managed the development of several integrated circuit manufacturing technologies for Intel including a 90 nanometer¹ and 130 nanometer² technologies.

11. These semiconductor manufacturing technologies used CMOS transistors, Copper interconnects and ball/pad connections. I won several Intel Achievement Awards for this work (Intel's highest award).

¹ See S. Thompson et al., "A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layers of Cu interconnects, low k ILD, and 1 /spl mu/m/sup 2/ SRAM cell," Digest. International Electron Devices Meeting, San Francisco, CA, USA, 2002, pp. 61-64, doi: 10.1109/IEDM.2002.1175779.

² See S. Thompson et al., "130nm Logic Technology Featuring 60nm Transistors, Low-K Dielectrics and Cu Interconnects"

(<https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=0691ee478ab78508ef236ccb63fc3a04660f2850>).

12. In 2000, I was promoted to Director of Semiconductor Technology Development in the Technology and Manufacturing Group at Intel. In that role, I was responsible for current and next-generation technology for integrated circuits. In that role I managed different areas including transistor technology, interconnects, integrated circuit package integration, integrated circuit yield, in-line defect metrology, and strategic long ranges plans for semiconductor technology. The Intel Technology and Manufacturing Group manufactured billions of dollars of CMOS integrated circuits each year. In 2002, I was appointed to the position of Intel Fellow, which is the highest technical position at Intel, and awarded for outstanding technical achievement both within Intel and industry. In that Intel role, I managed the development and manufacturing of the most advanced CMOS integrated circuits in the semiconductor industry—from 2000 to 2004, Intel surpassed IBM in integrated circuit development and became the industry leader. My team and I presented this work at many international conferences and invited talks and short courses.

13. Since 2004, I have been a professor of electrical and computer engineering at the University of Florida. I was granted tenure and promoted to full professor in 2006. During my teaching career, I developed graduate level courses on advanced semiconductor chip design, semiconductor manufacturing, and packaging technology (e.g., chip stacking). I also teach a graduate level course on

the chip technology used for CPU, DRAM, GPU, image sensors, and 2D and 3D image sensor processing. My current research areas include modeling and reliability integrated circuits. I currently have a Research Contract with Texas Instruments on how package balls and pads introduce mechanical stress and shift the electrical characteristics of integrated circuits. My research in advanced chip technology at the University of Florida has been funded by contracts worth \$4M. I have supervised approximately 20 Ph.D. candidates on topics related to CMOS integrated circuits and have won several University of Florida teaching awards.

14. In 2009, I founded SuVolta, a company that developed ultra-low power chip technology for image sensors, system-on-chip microchips, radio frequency integrated circuits, memory, CPUs, image sensors processors, and other chips. The technology developed by SuVolta was sold to Fujitsu in 2015 and was used in the commercial production of Milbeaut image sensor processors. The technology allowed Fujitsu to lower the power consumption of the image sensor processor by 50%. Working with Fujitsu, we also developed CMOS chips that operated at ultra-low power and operate at less than 0.5V power supply. SuVolta received several awards and honors: (1) 2011 EuroAsia IC Industry Award for start-ups; (2) 2012 ACE Award IEEE Spectrum: IEEE Emerging Technology; and (3) 2014 TiE 50 Top Startup. SuVolta was granted about 80 patents directed to low power transistor structures and integrated circuits on which I am a named inventor.

15. In 2006, I was elected as an IEEE Fellow for Advancing Fabrication of nanoscale MOSFET. In 2008, I received the Semi Award North America for Development of Strained Silicon Transistors.

16. Since 2005, I have worked as a consultant for leading companies in the semiconductor and computer chip industry, including Applied Materials, Cypress Semiconductor, Qualcomm, SanDisk, and Taiwan Semiconductor. I am the author of over 60 papers and one book related to semiconductors and am a named inventor on over 100 granted patents directed to integrated circuits and transistor structures.

17. A full list of my patents and journal publications in addition to my academic and industrial experience is further detailed in my curriculum vitae, which is attached to this declaration as Appendix A.

IV. MATERIALS CONSIDERED

18. In forming my opinions, I have analyzed the materials listed in the Table below. My opinions are based on my experience, knowledge of the relevant art, the documents identified in the Table below, as well as the documents directly cited to in this declaration.

Exhibit	Description
Ex. 1001	U.S. Patent No. 7,745,886 to Zwingman (“’886 patent”)
Ex. 1003	Prosecution History of the ’886 patent (downloaded from Public PAIR)

Exhibit	Description
Ex. 1004	U.S. Patent No. 6,836,172 to Okashita et al. (“ <i>Okashita</i> ”)
Ex. 1005	U.S. Patent No. 6,737,682 to Yu (“ <i>Yu</i> ”)
Ex. 1006	U.S. Patent Publication No. 2006/0270367 to Burgener et al. (“ <i>Burgener</i> ”)
Ex. 1007	Webster’s Ninth New Collegiate Dictionary, Merriam-Webster, Inc., Springfield, Massachusetts, 1985, p. 211.
Ex. 1008	“Fundamentals of Semiconductor Physics and Devices,” Rolf Enderlin and Norman J.M. Horing, World Scientific, 1996, pp. 535-539, 620-622.
Ex. 1009	“Electronics Circuits and Analysis,” Dinesh C. Dube, Alpha Science International Ltd., 2005, pp. 202-207.
Ex. 1010	“SOI Design: Analog, Memory and Digital Techniques,” Andrew Marshall and Sreedhar Natarajan, Kulwer Academic Publishers, 2003, pp. 1-46, 75-84, 125-179, 289-338, 340-358.
Ex. 1011	“CMOS Logic Circuit Design,” John P. Uyemura, Kluwer Academic Publishers, 2002, pp. 1-2, 19, 35-36, 78-83, 94-96, 359-362.
Ex. 1012	“The Stuff Dreams Are Made Of [Part 1],” Paul DeMone, May 8, 2002, Available at: https://www.realworldtech.com/cmos-basics
Ex. 1013	“SOI for Digital CMOS VLSI: Design Considerations and Advances,” Ching-Te Chuang et al., Proceedings of the IEEE, Vol. 86, No. 4, April 1998, pp. 689-720.
Ex. 1014	“1 Giga bit SOI DRAM with fully bulk compatible process and body-contacted SOI MOSFET structure,” Yo-Hwan Koh et al., 1997 International Electron Devices Meeting Technical Digest, Washington, DC, USA, 1997, pp. 579-582.
Ex. 1015	U.S. Patent No. 6,121,148 to Bashir et al. (“ <i>Bashir</i> ”), published September 19, 2000.
Ex. 1016	“Speeding up Transistors: IBM to Make SOI Chips,” Katherine Derbyshire, Semiconductor Online, August 18, 1998.
Ex. 1017	“SOI-CMOS Device Technology,” Yasuhiro Fukuda, et al., Special Edition on 21st Century Solutions, OKI Technical Review 185, Vol. 68, March 2001, pp. 54-57.

Exhibit	Description
Ex. 1018	“Impact of high-k gate stack material with metal gates on LF noise in n- and p-MOSFETs,” P. Srinivasan et al., <i>Microelectronic Engineering</i> 80 (2005) 226–229.
Ex. 1019	U.S. 2004/0150045 A1 to Nonaka et al., published August 5, 2004 (“ <i>Nonaka</i> ”).
Ex. 1020	U.S. Patent No. 6,498,371 B1 to Krishnan et al., published December 24, 2002 (“ <i>Krishnan</i> ”).
Ex. 1021	U.S. Patent No. 6,933,569 B2 to Koh et al., published August 23, 2005 (“ <i>Koh</i> ”).
Ex. 1022	“Temperature-Dependent Thermal Conductivity of Single-Crystal Silicon Layers in SOI Substrates,” M. Asheghi et al., <i>Transactions of the ASME, Journal of Heat Transfer</i> , Vol. 120, February 1998, pp. 30-36.
Ex. 1023	“Current Mode Digital Gates for Mixed Mode Reprogrammable Integrated System,” P. Pawlowski, <i>Proceedings of the 1st IEEE International Conference on Circuits and Systems for Communications</i> , 26-28 June, 2002, St. Petersburg State Polytechnic University Publishing House, 2002, pp. 178-181.

V. LEGAL STANDARDS

19. I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

20. I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art

can “anticipate” a claim. Second, I have been informed that the prior art can render a claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

21. I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

22. I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 1-19 of the '886 patent from the perspective of a person of ordinary skill in the art at the '886 patent's earliest claimed priority date (December 10, 2007), as described in more detail below.

23. I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means “more likely than not.”

24. For purposes of this declaration, I have been asked to provide my opinions on issues regarding unpatentability. I have been informed of the following legal standards, which I have applied in forming my opinions.

A. Level of Ordinary Skill

25. I have been informed a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

26. I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Prior Art

27. I have been advised and understand the information used to evaluate whether an invention was new and not obvious when made is generally referred to as “prior art.” I understand that prior art includes patents and printed publications that existed before the earliest claimed priority date or the earliest filing date of the patent (which I have been informed is also called the “effective filing date”). I have been informed and understand that a patent or published patent application is prior art if it was filed before the earliest filing date of the claimed invention and that a printed publication is prior art if it was publicly available before the earliest filing date.

C. Anticipation

28. I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if it is not novel, including if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

D. Obviousness

29. I have been informed that under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

30. I have been informed that a proper obviousness analysis includes the following:

- a. Determining the scope and content of the prior art;
- b. Ascertaining the differences between the prior art and the claims at issue;

- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of non-obviousness (if available). I am not aware of any evidence of secondary considerations that would support a determination of non-obviousness of the claimed subject matter in the '886 patent.

31. I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to assume that the date of invention for the Challenged Claims is December 10, 2007. My opinions would not change if I assumed a later date of invention.

32. I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

33. I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary

skill in the art. I have also been informed that, while there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

34. In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;

- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—but not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

35. I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the

benefit of doing so, that variation is likely to have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

36. I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

37. I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or

motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

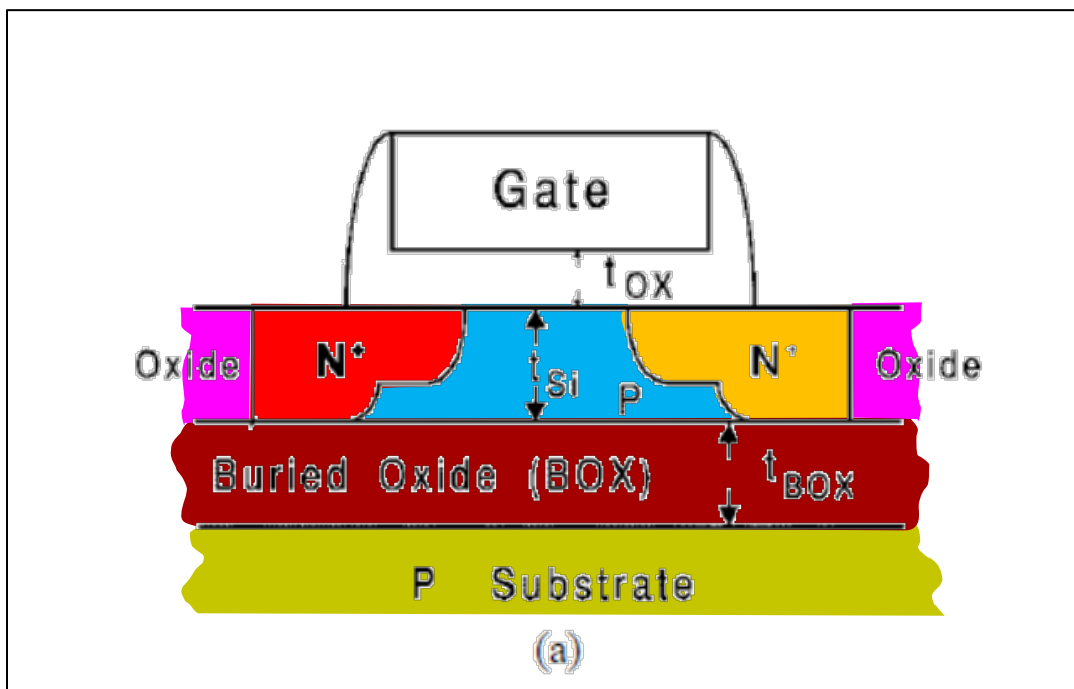
38. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

VI. TECHNOLOGY BACKGROUND AND STATE OF THE PRIOR ART

A. SOI Transistors

39. Semiconductor-On-Insulator (SOI) (also called Silicon-On-Insulator) is a semiconductor structure consisting of a layer of silicon separated from the bulk substrate by a layer of insulator. SOI transistors, thus, are transistors that are built on a thin layer of silicon separated from the bulk silicon substrate by an insulating layer, typically made of silicon dioxide (SiO₂). The insulating layer is often called a buried oxide (or BOX) layer. *See* Ex. 1013, 2; Ex. 1010, 30.

40. There are two basic types of MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) widely used for switching and amplifying signals in electronic devices – the N-channel MOSFET (or NFET) and the p-channel MOSFET (or the PFET). Ex. 1008, 20. To facilitate my explanations, I have provided below a schematic cross-sectional view of an NFET that is fabricated on a SOI structure. Ex. 1013, 2.



Ex. 1013, 2 (Fig. 1).³

41. The above NFET starts with an underlying body of p-type silicon. By doping (or implanting) a higher concentration of n-type dopant atoms than the

³ All colored annotations in figures of this declaration have been added.

concentration of p-type dopant atoms in the p-type **silicon**, two side-by-side regions in the top of the **silicon** are changed to n-type silicon. Ex. 1013, 2; *see also* Ex. 1011, 7-9; Ex. 1012, 2. This process is also known as an n⁺ implant, where the “+” symbol indicates a relatively high doping density. These two n⁺ regions are known as the **source** and **drain**. The designation of **source** and **drain** is arbitrary because a FET is electrically symmetrical, and the **source** and **drain** can be swapped. Since the **source** and **drain** regions are separated by p-type **silicon**, no current can flow between them.

42. To form a field effect transistor, a polycrystalline silicon (also known as polysilicon or poly) structure called a gate is deposited over the **silicon** between the **source** and **drain** regions. The gate is electrically isolated from the **source**, **drain**, and the p-type **silicon** region by an extremely thin layer of insulator called the gate dielectric.

43. “The PFET is a mirror image (or complement) of the NFET.” Ex. 1012, 2. In contrast to an NFET, which has a p-type silicon body with an n-type source and drain regions, a PFET is formed on an n-type silicon body (or an n-type well within p-type silicon) where p-type source and drain regions are implanted on both sides of the gate structure. Ex. 1011, 12-17; Ex. 1012, 2; Ex. 1008, 20. The figure below shows an NFET and a PFET formed side-by-side on p-type bulk silicon. *See* Ex. 1011, 17.

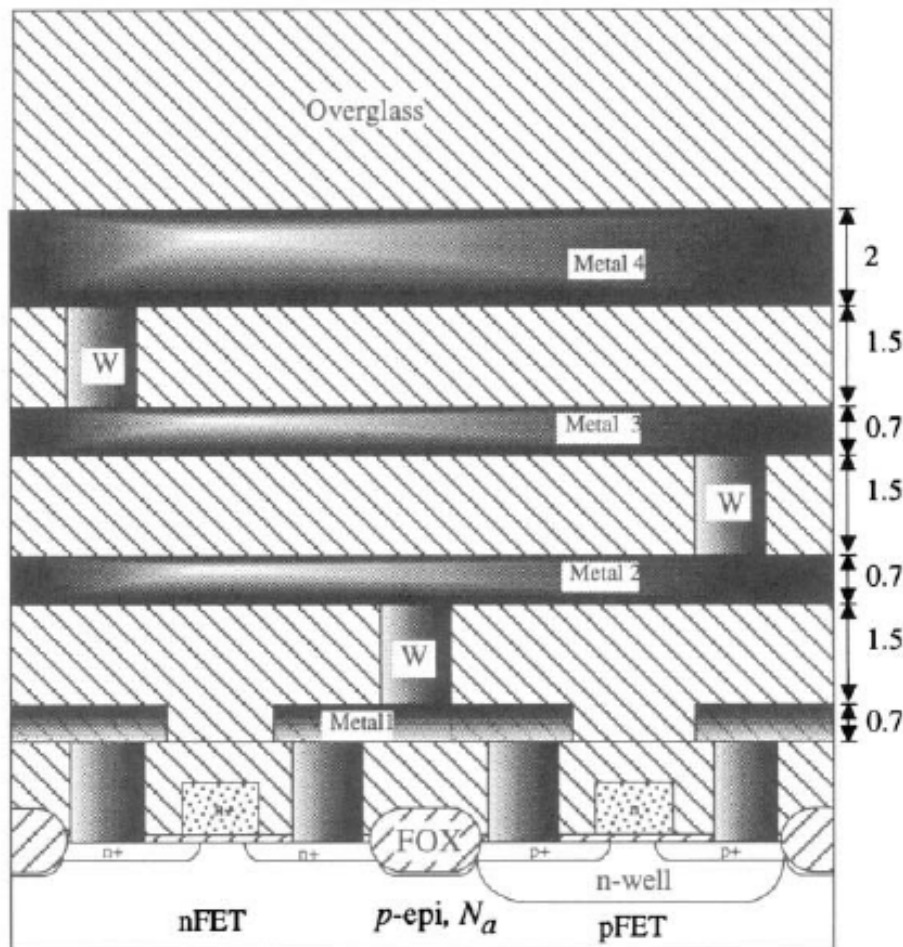


Figure 2.22 Visualization of 4-metal interconnect structure

Ex. 1011, 17 (Fig. 2.22).

44. In the figure, since NFET requires a p-type body, the NFET is formed directly on the p-type bulk silicon. Ex. 1011, 17. And since PFET requires an n-type body, a region of the p-type bulk silicon is doped (by ion implantation) to form an n-well and the source and drain of the PFET are formed on the n-well. Ex. 1011, 12-17; *see also* Ex. 1010, 37.

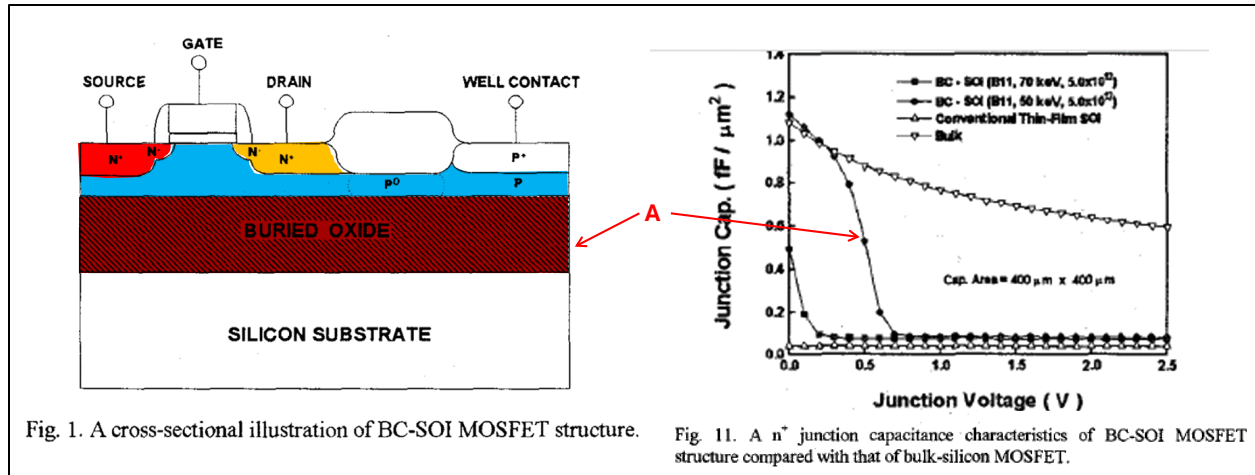
B. Junction Capacitance

45. In a bulk silicon transistor, the junctions between the **source/drain** regions and the **substrate** creates capacitance (called junction capacitance). *See* Ex. 1011, 10 (“pn junctions [] are formed by the **drain-bulk** and **source-bulk** interfaces in a MOSFET”), 11 (*see* Fig. 1.36); *see* Ex. 1010, 43, 45.

46. SOI transistors, however, have a lower junction capacitance than comparable transistors fabricated on a bulk silicon. Ex. 1010, 24. This is because the SOI transistors’ **source** and **drain** regions are isolated from the **substrate** by an **insulating layer**. As such, the junction capacitance is significantly reduced or even eliminated. Ex. 1010, 39 (explaining that SOI devices have low **drain/source**-substrate capacitances due to the **buried oxide region**); *see, e.g.*, ’886 patent, 3:13-21.

C. SOI Transistors With an Intervening Silicon Layer Between the Source and Drain and the Buried Oxide Layer Were Well Known in the Art

47. It was well known that, when a **silicon layer** remains between the bottom of the **source** and **drain** of the transistor structure and the top of the **insulating layer** (i.e., the **buried oxide layer**), such a “structure has larger junction capacitance than the normal SOI structure.” Ex. 1013, 25-26; Ex. 1014, 2-3, 5. This phenomenon is shown below.



Ex. 1014, 3 (Fig. 1), 5 (Fig. 11).

48. For example, the transistor shown above is fabricated with an intervening **silicon** layer between the bottom of the **source** and **drain** and the top of the **buried oxide layer**. In such a transistor, its **source/drain** junction capacitance, (see Figure 11, curve ● marked **A**), is greater than that of a conventional thin-film SOI transistor (curve Δ) and less than that of a conventional bulk silicon transistor (curve ▽). See Ex. 1014, 2-5.

49. Junction capacitance also influences the delay time at the transistor gate, such that the bigger the junction capacitance, the longer the delay time. See Ex. 1012, 2, 4; see Ex. 1013 (explaining that reducing the junction capacitance allows circuits to operate at higher speed). As a result, the junction capacitance created by the intervening **silicon** layer between the bottom of the **source** and **drain** and the top of the **buried oxide layer** is also seen in the delay time of the transistor gate, as shown below.

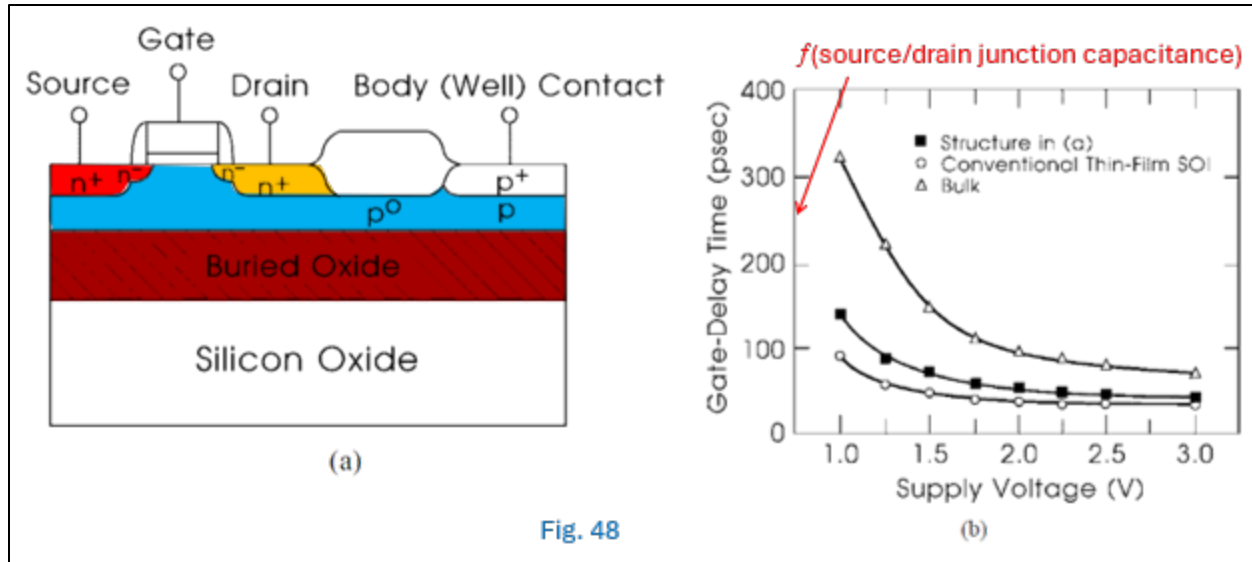


Fig. 48

Ex. 1013, 26 (Figs. 48(a)-(b)).

50. The figure above shows the effect of the intervening **silicon** layer on the gate delay time (and by inference, the source/drain junction capacitance). The figure compares a conventional SOI structure (curve $\circ$), a bulk semiconductor structure (curve Δ), and a structure having an intervening **silicon film** of 75 nm between the bottom of the **source** and **drain** and the top of the **buried oxide layer** above the SOI substrate (i.e., structure (a) in figure 48(a); curve $\blacksquare$). Ex. 1013, 26.

51. Although an SOI transistor results in a lower junction capacitance and lower delay time, the buried oxide layer reduces thermal conductivity to the substrate and, thereby, causes localized temperature increases that can impact circuit performance and reliability. See Ex. 1010, 59-60, 192; Ex. 1022, 1. Since the thermal conductivity of silicon dioxide is about 100 times lower than that of silicon, channel temperature rise in SOI transistors can be up to ten times higher

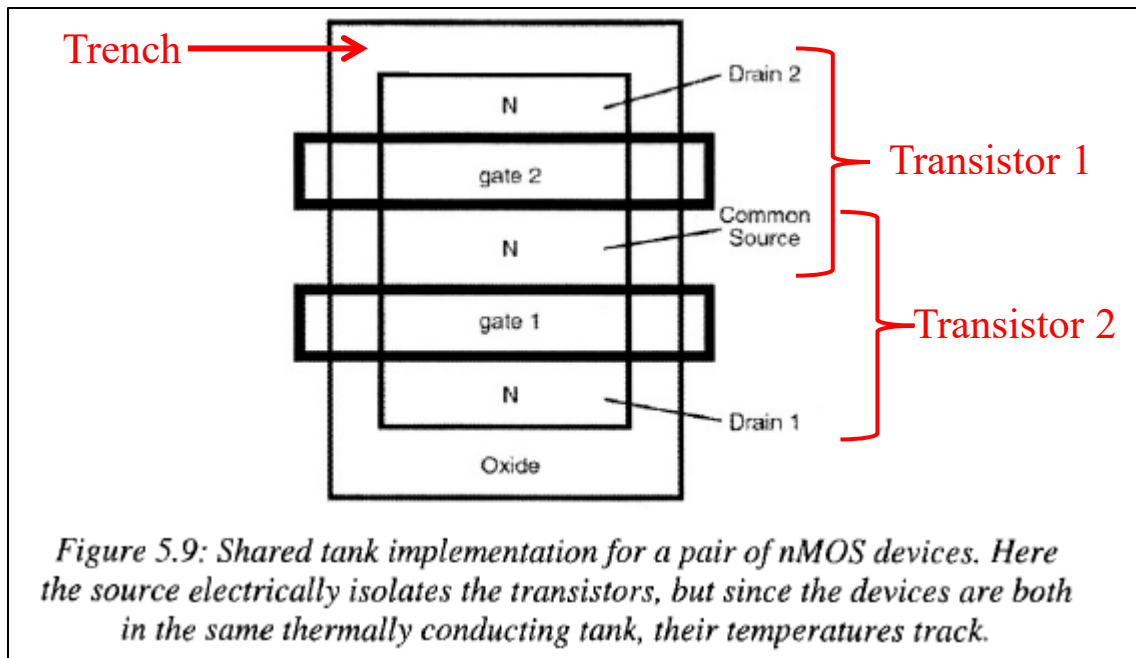
than in bulk silicon transistors, posing a design challenge for SOI transistors. Ex. 1013, 27-28; Ex. 1022, 1 (explaining that the buried silicon dioxide results in a large thermal resistance between the device and the substrate causing a major problem for SOI transistors). The self-heating issue with SOI devices is exacerbated where the devices are isolated from adjacent devices by insulating trenches around them. *see* Ex. 1010, 60; *see Yu* (Ex. 1005), 2:4-9. *Yu*, discussed *infra* VIII.B, explains that the insulating trench (STI 36) around its transistors reduces lateral heat transfer from the transistors and suggests that retaining an intervening silicon layer (silicon layer 34) between the source and drain of the transistor and the buried oxide layer 32 may prevent heat related failures of the transistors during electrostatic discharge (ESD) events. *Yu*, 2:4-9; *see also* Ex. 1022, 1 (explaining that lateral heat conduction can reduce strongly reduce the temperature rise in active regions).

D. SOI Transistors Surrounded by a Trench Were Also Well Known in the Art

52. It was well known to electrically isolate transistors of a circuit on an SOI substrate using isolating trenches to improve the electrical performance of the circuit. *See, e.g.*, Ex. 1010, 36 (noting that in SOI, individual devices can be dielectrically isolated using trench-type isolation, preventing electrical latchup); Ex. 1015, 1:22-28 (explaining that semiconductor devices in an integrated circuit can be electrically isolated using insulator-filled vertical trenches in the

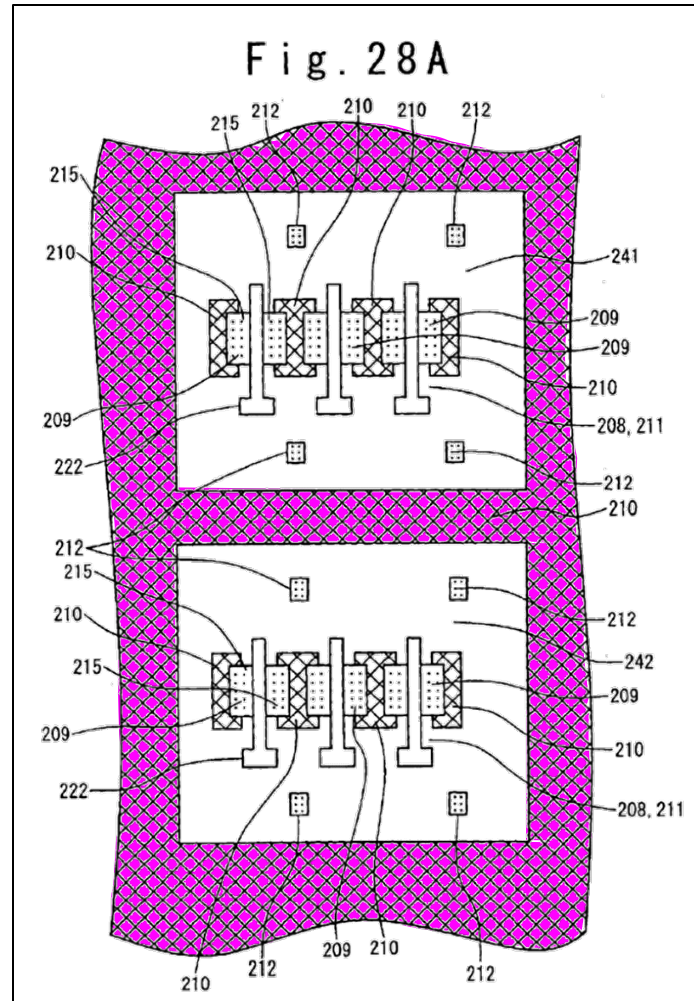
semiconductor substrate to block lateral electrical leakage). Below are four examples.

53. As illustrated in the figure below, both transistors 1 and 2 have consistent electrical properties because the transistors are located in a common thermally conducting tank surrounded by an oxide trench. *See Ex. 1010, Fig. 5.9.* “[S]ince the devices are both in the same thermally conducting tank, their temperatures track.” Ex. 1010, 75.



Ex. 1010, 75 (Fig. 5.9).

54. In Ex. 1021, multiple transistors are located in the same isolated region surrounded by an insulating trench to ensure that these transistors have consistent performance characteristics. Ex. 1021, Fig. 28A, 16:15-57, 13:5-42.

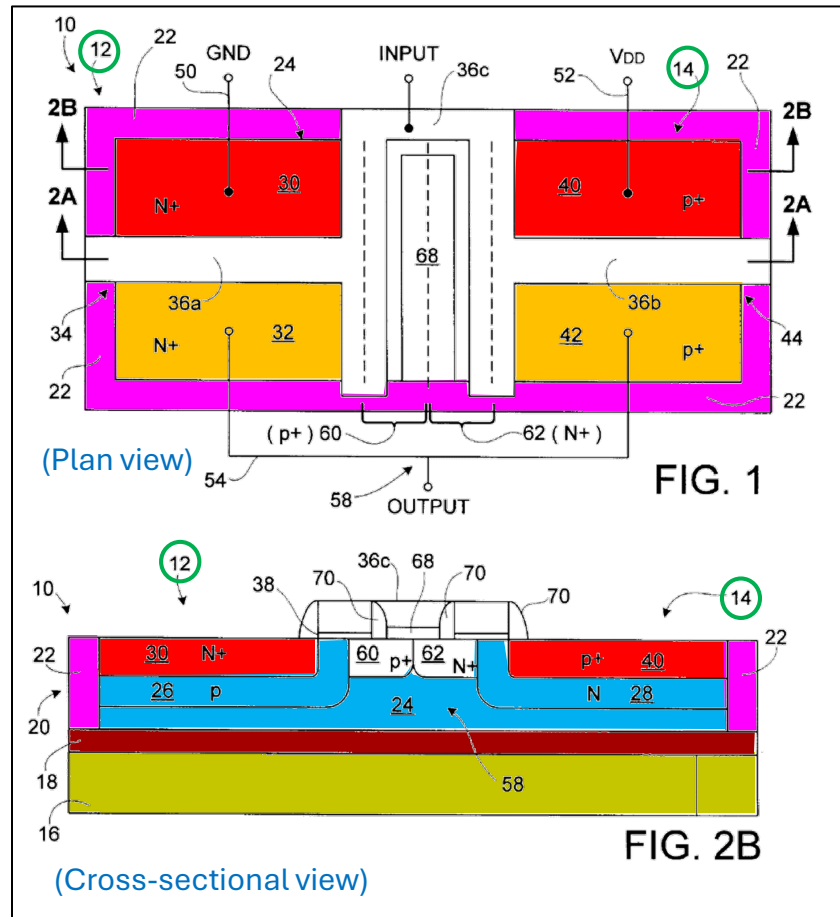


Ex. 1021, 31 (Fig. 28A).

55. As shown above, active regions (blocks 241 and 242) are defined on an SOI substrate surrounded by isolating **trenches**. Multiple transistors (three in Fig. 28A above) are fabricated in each active region. Ex. 1021, 16:15-57 (“a plurality of FET transistors can be formed within one block surrounded by the full isolating region (a block isolating film) 210 as shown in FIG. 28A”).

56. As another example, Ex. 1020 discloses an inverter circuit with transistors fabricated on an SOI substrate and surrounded by an insulating trench to

ensure a consistent switching rate for both transistors. Ex. 1020, Abstract, 1:47-63, 3:22-59, Figs. 1-2B. Notably, the bottom surfaces of the **sources** and **drains** of these transistors are also separated from the **buried oxide layer** by **silicon** material. See, e.g., Ex. 1020, Figs. 2A-2B.

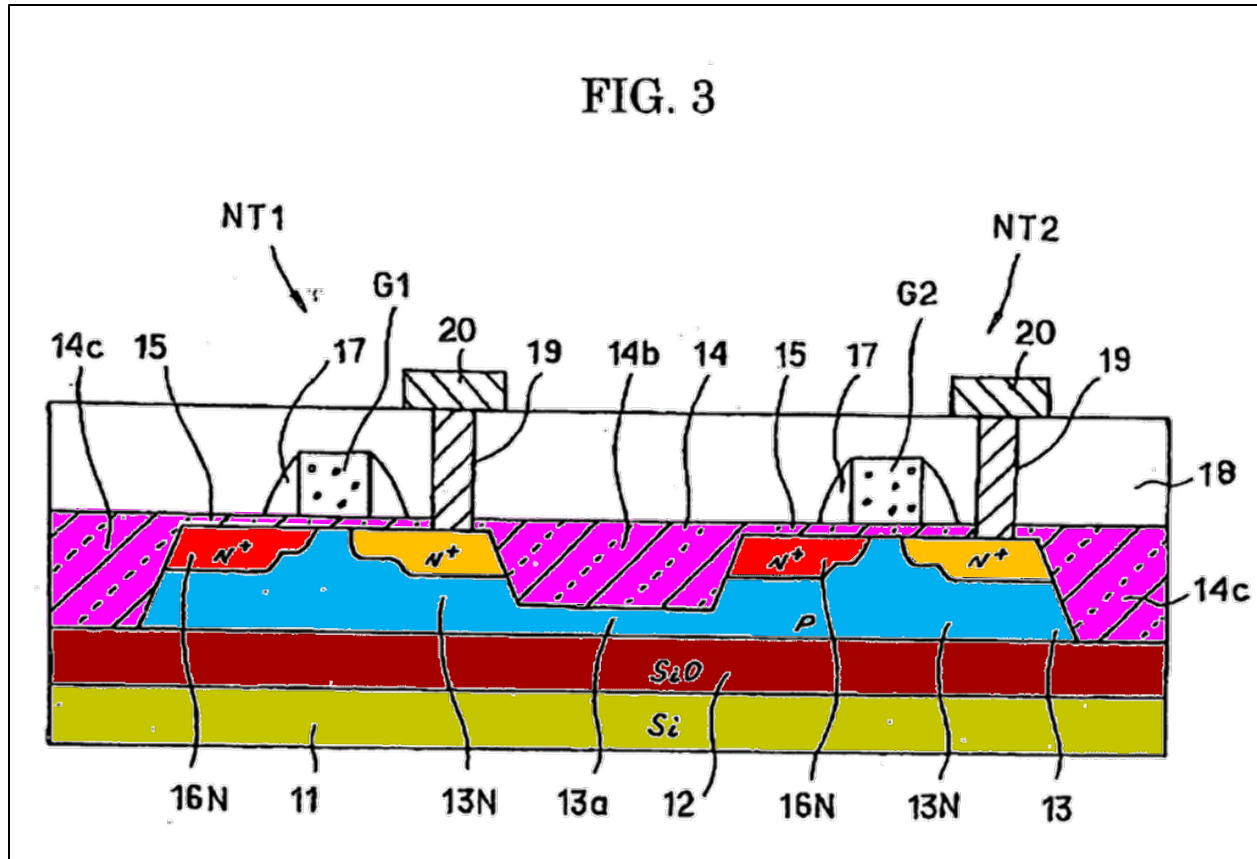


Ex. 1020, 2 (Figs. 1, 2B).

57. In Ex. 1020, an **active semiconductor layer 20** of silicon is formed on top of a **buried oxide layer** disposed atop a **bulk silicon substrate 16**. Ex. 1020, 3:23-33. An isolation barrier 22 (or insulating **trench**), that extends to the **buried oxide layer 18**, surrounds a region of the **silicon layer 20** to define an electrically

isolated **active region 24**. Ex. 1020, 3:34-42, Figs, 1-2B. An NFET 12 (with a **source 30**, **drain 32**, and a gate 36a) and a PFET 14 (with a **source 40**, **drain 42**, and a gate 36b) are fabricated in the **active region 24** above the **buried oxide layer 18**. Ex. 1020, 3:22-59, Figs, 1-2B. In Ex. 1020 (similar to *Yu* and the '886 patent), a layer of the **silicon material** is retained between the bottom of the **sources 30, 40** and **drains 32, 42** of the two transistors 12, 14 and the top of the buried oxide layer 12. *See* Ex. 1020, 3:43-59, Figs. 2A-2B, 4A-4C.

58. Lastly, Ex. 1019 discloses another exemplary circuit with a plurality of transistors located on an isolated island in an SOI substrate surrounded by a trench. Ex. 1019, Abstract, ¶¶[0042]-[0044], [0063], Fig. 3.



Ex. 1019, 4 (Fig. 3).

59. In Ex. 1019, a pair of transistors (NT1 and NT2) are fabricated on a silicon semiconductor layer 13 that is formed on top of a silicon oxide film 12 (BOX) over a silicon substrate 11. Ex. 1019, ¶¶ [0042], [0044], Fig. 3. Specifically, the pair of transistors NT1 and NT2 are fabricated on an isolated island on the semiconductor layer 13 that is surrounded by a trench 14C that extends through the semiconductor layer 13 to contact the BOX layer 12. Ex. 1019, ¶¶ [0063], [0005]. In Ex. 1019 also, the bottom surfaces of the sources and drains of transistors NT1 and

NT2 are separated from the top surface of the BOX layer 12 by silicon. See Ex. 1019, Fig. 3.

60. Moreover, as discussed in the section *infra* (§§VIII.A-VIII.B), *Okashita* and *Yu* also disclose SOI transistors in a switching circuit surrounded by an insulating trench. The transistors of *Okashita* and *Yu* also have an intervening silicon layer between their sources and drains and the buried oxide layer. *Okashita*, 6:43-67, Fig. 9; *Yu*, 2:4-9.

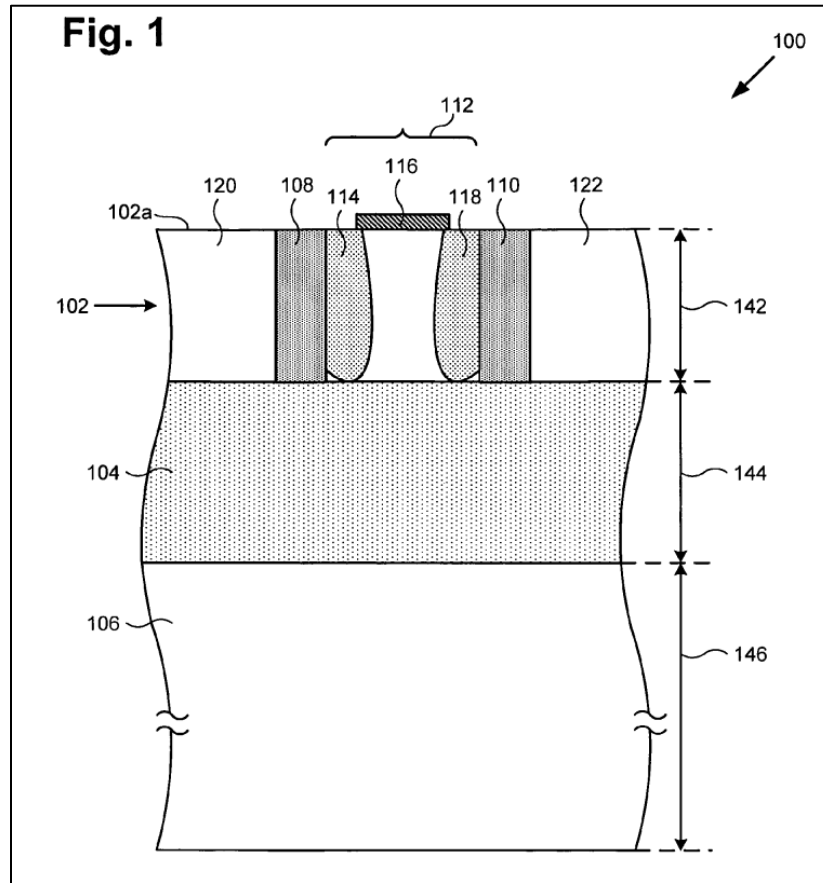
VII. THE '886 PATENT

A. Alleged Invention of the '886 patent

61. The '886 patent acknowledges that transistors and isolating trenches have been conventionally fabricated on both bulk silicon wafers and SOI wafers. Ex. 1001, '886 patent, 1:19-27. According to the '886 patent, the transistors fabricated on a bulk silicon wafer face challenges with current leakage and interference between neighboring transistor devices, whereas the transistors fabricated on an SOI wafer benefit from better isolation due to the additional buried oxide layer. Ex. 1001, '886 patent, 1:28-42.

62. The '886 patent further notes that to redesign circuits for fabrication on an SOI wafer increases cost and integration complexity. Ex. 1001, '886 patent, 1:42-50, 3:17-36. The '886 patent notes that transistors have been conventionally

fabricated in SOI wafers and illustrates such a conventional transistor 112 structure on an SOI wafer in Fig. 1 shown below. Ex. 1001, '886 patent, 2:29-3:48.



Ex. 1001, '886 patent, Fig. 1.

63. The conventional transistor 112 depicted in Fig. 1 is fabricated on a silicon device layer 102, which is formed on a buried oxide layer 104 that sits atop a bulk semiconductor layer 106. Ex. 1001, '886 patent, 2:29-42. This transistor 112 also includes trenches 108 and 110, filled with insulative oxide, that extend through the device layer 102 to contact the top surface of the buried oxide layer 104, as illustrated in FIG. 1. Ex. 1001, '886 patent, 2:60-67. According to the '886

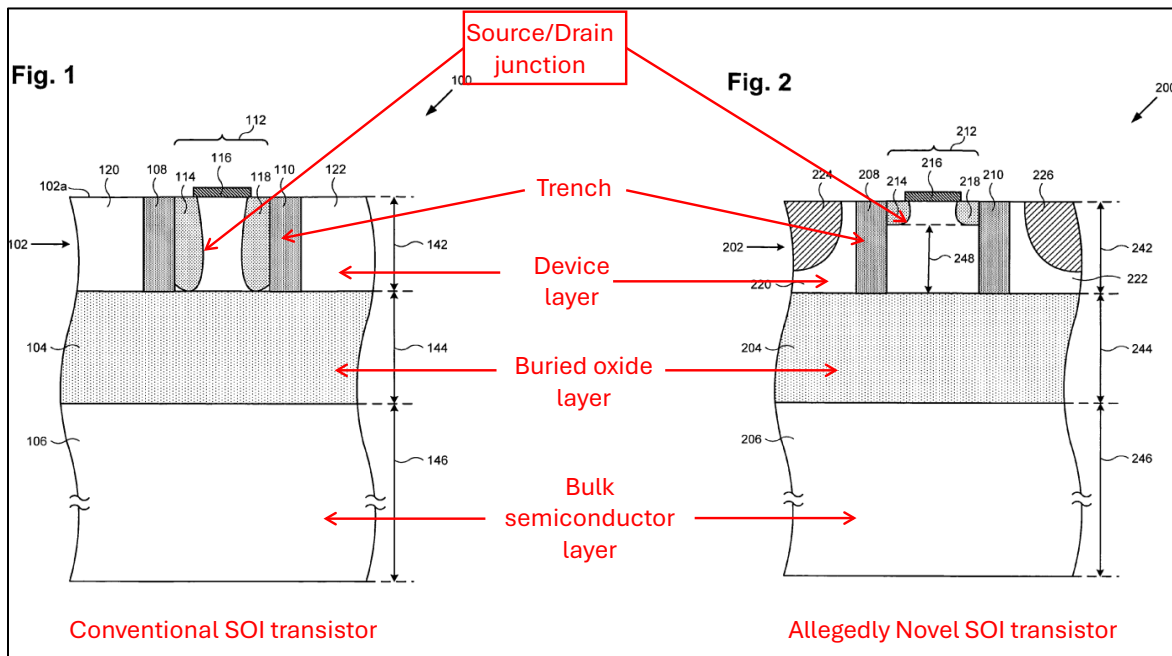
patent, transistor 112 is fabricated in the device layer 102, between trenches 108 and 110, in such a way that it is electrically isolated from neighboring islands 120 and 122 by these trenches and the buried oxide layer 104. Ex. 1001, '886 patent, 2:67-3:5. The '886 patent acknowledges that this electrical isolation is a conventional advantage of constructing transistor 112 on an SOI wafer, as it allows the transistor to endure positive and negative voltage excursions without affecting adjacent devices. Ex. 1001, '886 patent, 3:5-12.

64. The '886 patent describes that the conventional transistor 112 (which can be either an NFET or a PFET) in figure 1 features a source 114 and a drain 118. The source 114 and drain 118 typically extend entirely through the device layer 102, making contact with the top surface of the buried oxide layer 104. Ex. 1001, '886 patent, 3:13-17. Since there is little to no semiconductor material (such as silicon) between the source 114 or drain 118 and the buried oxide layer 104, there is minimal to no semiconductor junction to generate a capacitive load. Ex. 1001, '886 patent, 3:17-21. According to the '886 patent, the absence or extremely low junction capacitance of transistor 112 prevents the use of established bulk silicon wafer design methodologies, device models, and design kits to design such transistors. Ex. 1001, '886 patent, 3:21-28. Instead, as stated in the '886 patent, transistors on SOI wafers need to be designed using less mature models, and

design kits, resulting in higher development costs and inefficiencies in the design and fabrication of SOI devices. Ex. 1001, '886 patent, 3:28-35.

65. To address this alleged deficiency and ensure that the “source/drain junction capacitances of [its disclosed] transistor 212 behave similarly to the junction capacitances of a transistor implemented in a conventional bulk silicon wafer, instead of a conventional SOI wafer,” like transistor 112 in figure 1, the disclosed transistor 212 includes some device layer material (i.e., silicon) between the bottom of the source and drain and the top of the buried oxide layer. Ex. 1001, '886 patent, 3:49-4:39.

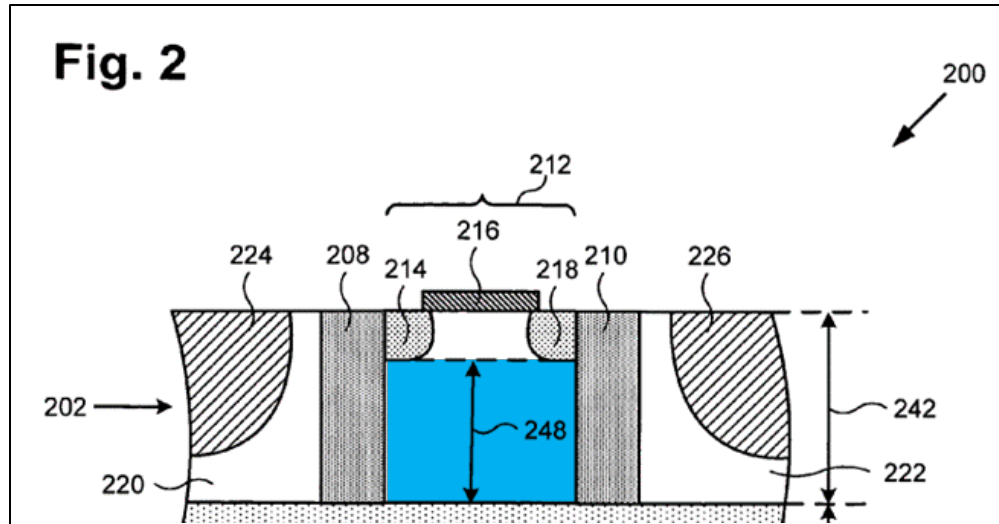
66. Shown below is a side-by-side comparison of the “conventional” transistor 112 of Fig. 1 with the '886 patent's claimed transistor 212 of Fig. 2.



Ex. 1001, '886 patent, Figs. 1-2; 1:62-65, 2:29-4:64

67. Both transistors 112 and 212 are fabricated on a SOI wafer (Figure 1's layers 102, 104, 106 and Figure 2's layers 202, 204, 206). Notably, both transistors 112 and 212 are surrounded by trenches (108 and 110 in Figure 1 and 208 and 210 in Figure 2) that extend through the respective device layer to contact the top surface of the buried oxide layer to form an isolated island in the device layer between the trenches such that both transistors 112 and 212 are formed in an isolated island in the device layer surrounded by trenches. Ex. 1001, '886 patent, 2:60-3:5, 4:37-47, Figs. 1-2.

68. However, to address the concerns with the increased cost and complexity in fabricating transistors on a SOI wafer, the '886 patent suggests adding "junction capacitance" to the transistors, as shown in Figure 2, which simply means to maintain an "intervening thickness 248" of the device layer material (silicon) between the bottom surfaces of the source and drain and the top surface of the buried oxide layer as shown below. Ex. 1001, '886 patent, 4:11-36.



'886 patent, Fig. 2 (excerpted).

69. This “intervening thickness 248” forms a corresponding source/drain junction capacitance. Ex. 1001, '886 patent, 4:11-36. According to the '886 patent, Figure 1's conventional transistor has “no, or almost no” semiconductor material between the source and drain (114, 118) and the buried oxide layer (104), resulting in “low or non-existent” junction capacitance. Ex. 1001, '886 patent, 3:17-28. In contrast, the intervening thickness 248 of silicon in Figure 2 results in a junction capacitance similar to that of a transistor fabricated on a bulk silicon wafer, and thus, enables the use of existing design tools meant for bulk silicon transistors. Ex. 1001, '886 patent, 4:11-36, 5:63-65 (“This remaining semiconductor would result in source/drain junction capacitance of structure 200” of figure 2).

70. In my opinion, the presence of the *additional device layer material* between the bottom surfaces of the source and drain and the top surface of the

buried oxide layer *is the only distinction* between the conventional transistor structure (transistor 112) and the disclosed transistor structure (transistor 212) and the only reason for the resulting source/drain junction capacitance. *See* Ex. 1001, '886 patent, 3:17-28, 4:11-18.

B. Prosecution History

71. I understand that during prosecution of the '886 patent, the examiner allowed the claims in a first Office Action. Ex. 1003, 33-37. However, during prosecution, the Examiner did not consider any of the references used in this declaration—Okashita, Yu, and Burgener. In my opinion, as explained below, these references render claims 1-19 of the '886 patent unpatentable.

C. Claim Construction

72. I have been instructed that the “intrinsic record” includes the patent itself, including the claims, description, and figures (Ex. 1001), and the patent’s prosecution history—i.e., the record of proceedings at the U.S. Patent and Trademark Office (“Patent Office”) concerning the patent (Ex. 1003). I understand that, like the claims and written description, the prosecution history provides evidence to a person of ordinary skill in the art of how the inventor intended his patent to be understood, and how the Patent Office understood the patent. I understand that the inventor is permitted to apply a special definition to the terms or to limit the scope of claim terms in his patent claims, which may differ from the

term's plain and ordinary meaning. That special definition or limitation on scope may be provided in the patent's written description, the patent's prosecution history, or both.

73. I understand that claim interpretation may also be informed by "extrinsic evidence" (that is, evidence outside of the patent record itself). I have been informed that extrinsic evidence may include dictionaries, technical treatises, and other materials evidencing the meaning of a claim term and the understanding held by a person of ordinary skill in the art (POSITA) in the relevant time period.

74. I have been asked for purposes of this declaration to apply the plain and ordinary meaning of the claim terms as they would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the '886 patent. Based on my review of the materials and my personal knowledge and experience, I have considered each term of the '886 patent as it would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the '886 patent (December 10, 2007).

VIII. SUMMARY OF THE PRIOR ART

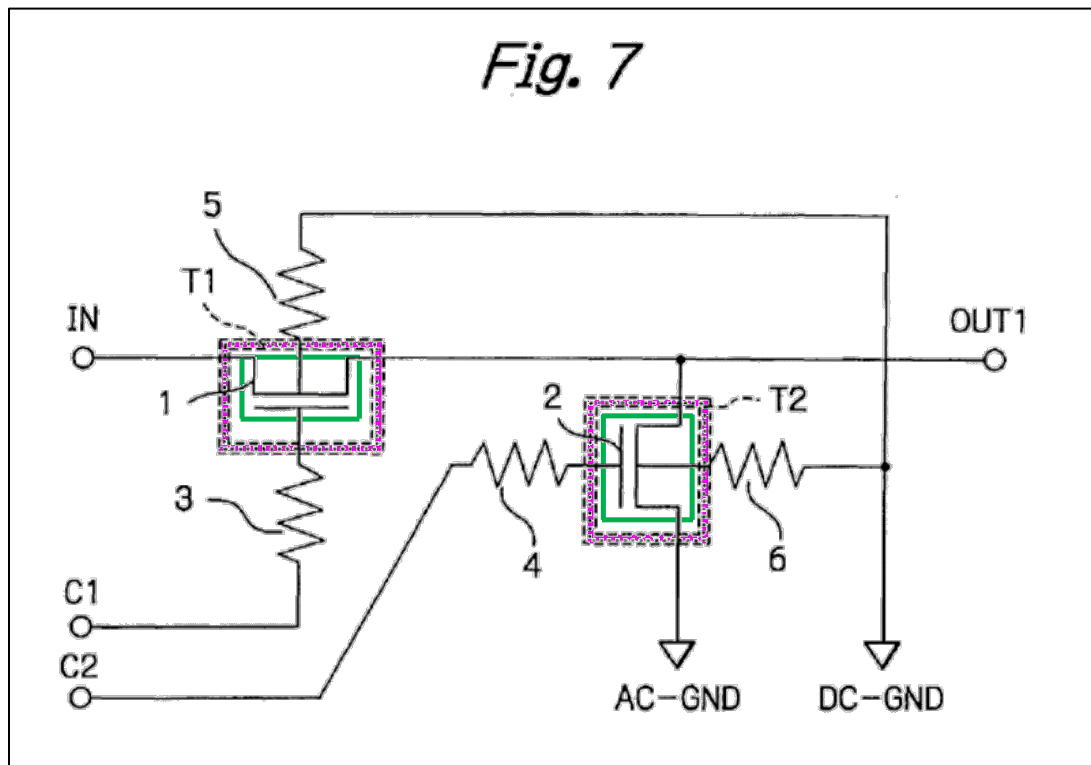
A. *Okashita*

75. *Okashita*, titled "Semiconductor Switch Apparatus Including Isolated MOS Transistors," was filed on May 22, 2003, and published on December 28,

2004. I understand that *Okashita* is prior art to the '886 patent based both on its filing date and its publication date.

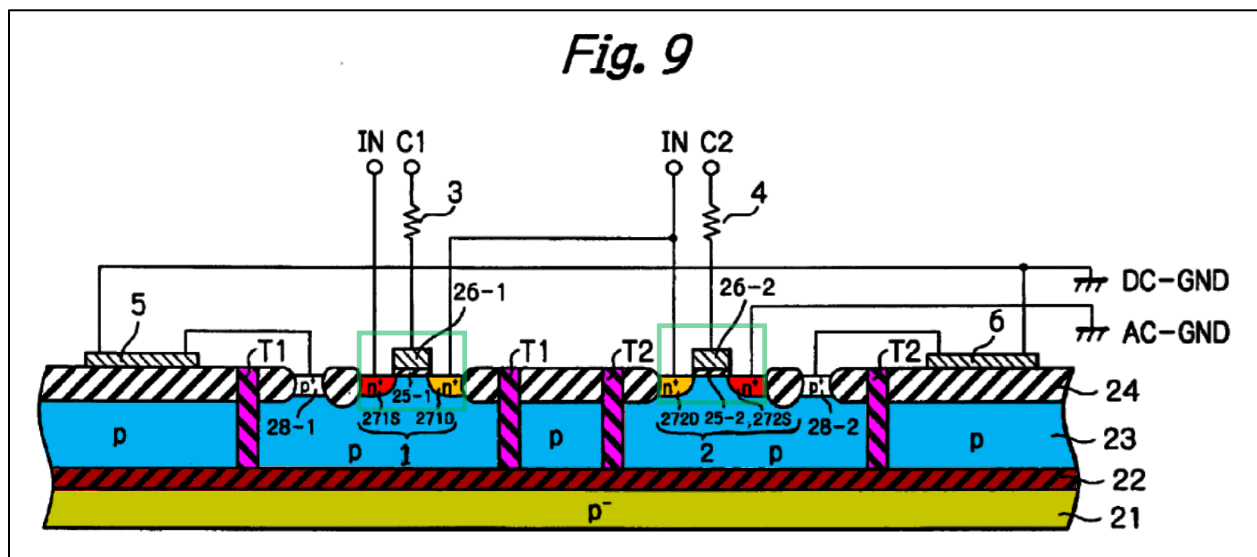
76. *Okashita* discloses several embodiments of a “semiconductor switch apparatus[] used for switching the operation of an antenna circuit and a receiving and transmitting circuit” in a mobile telephone. *Okashita*, 1:7-15.

77. *Okashita* is analogous art to the '886 patent since both are from the same field of endeavor. *Okashita*, 1:7-15. For example, both relate to a semiconductor switching circuit with cascaded transistors having an SOI configuration. See *Okashita*, 1:43-61, 9:27-12:44; '886 patent, 1:14-17, 7:25-31, 8:63-10:55.



Okashita, Fig. 7

78. In one embodiment of *Okashita*'s switch apparatus (the first embodiment illustrated in Figures 7-9), a MOS transistor 1 isolated by an insulating trench T1 is connected to a MOS transistor 2 isolated by an insulating trench T2. *Okashita*, 5:22-40, 8:30-37.



Okashita, Fig. 9.

79. As shown in Figure 9, *Okashita*'s semiconductor switch apparatus, with MOS transistors 1, 2, is fabricated in an SOI configuration, where a p-type silicon layer 23 is grown on a silicon oxide layer 22 that is formed on a monocrystalline silicon substrate 21. *Okashita*, Abstract, 5:41-44. In *Okashita*, silicon oxide layer 22 is the buried oxide layer of the SOI substrate.

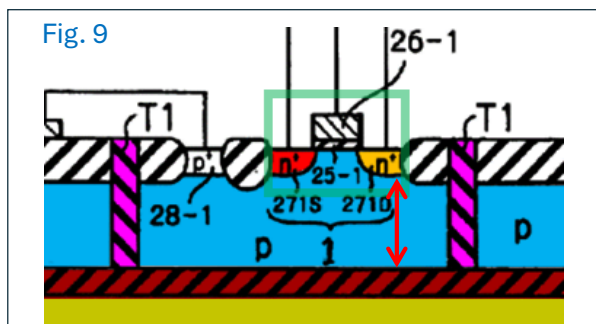
80. Trenches T1 and T2 are then etched into the silicon layer 23 and filled with silicon oxide. *Okashita*, 5:47-54. Within an area enclosed by trench T1,

regions 271S and 271D of the p-type silicon layer 23 on opposite sides of a gate are doped with an n⁺-type impurity to form the source and drain of transistor 1.

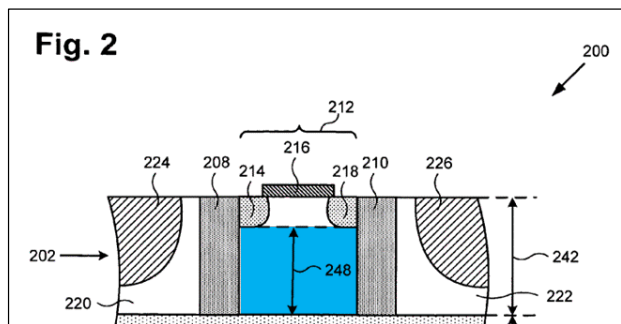
Okashita, 5:55-59. Source 272S and drain 272D of transistor 2 are similarly formed by doping with n⁺-type impurity within the area surrounded by trench T2.

Okashita, 5:59-63. In my opinion, a POSITA would have known that, since transistors 1 and 2 have a p-type silicon body (p-type silicon layer 23) and an n⁺-type source 271S and drain 271D, they are n-channel MOSFETs (also called NMOSFETs or NFETs). See, e.g., Ex. 1011, 7-8; Ex. 1010, 36-37; Ex. 1012, 2, 4.

81. *Okashita* explains that the SOI substrate helps to suppress the leakage of radio frequency signals via the silicon substrate 21. *Okashita*, 6:1-7. *Okashita* further explains that, since the transistors 1 and 2 are each surrounded by trenches T1, T2, as shown in Figures 7-9, leakage of radio frequency signals via the p-type silicon layer 23 is also suppressed. *Okashita*, 6:8-17.



Okashita, excerpt of Fig. 9



886 patent, excerpt of Fig. 2

82. Notably, similar to the transistors in the '886 patent, *Okashita*'s transistors 1 and 2 also show an intervening thickness of the silicon layer 23

between the bottom surfaces of their **sources** and **drains** and the **buried oxide layer**

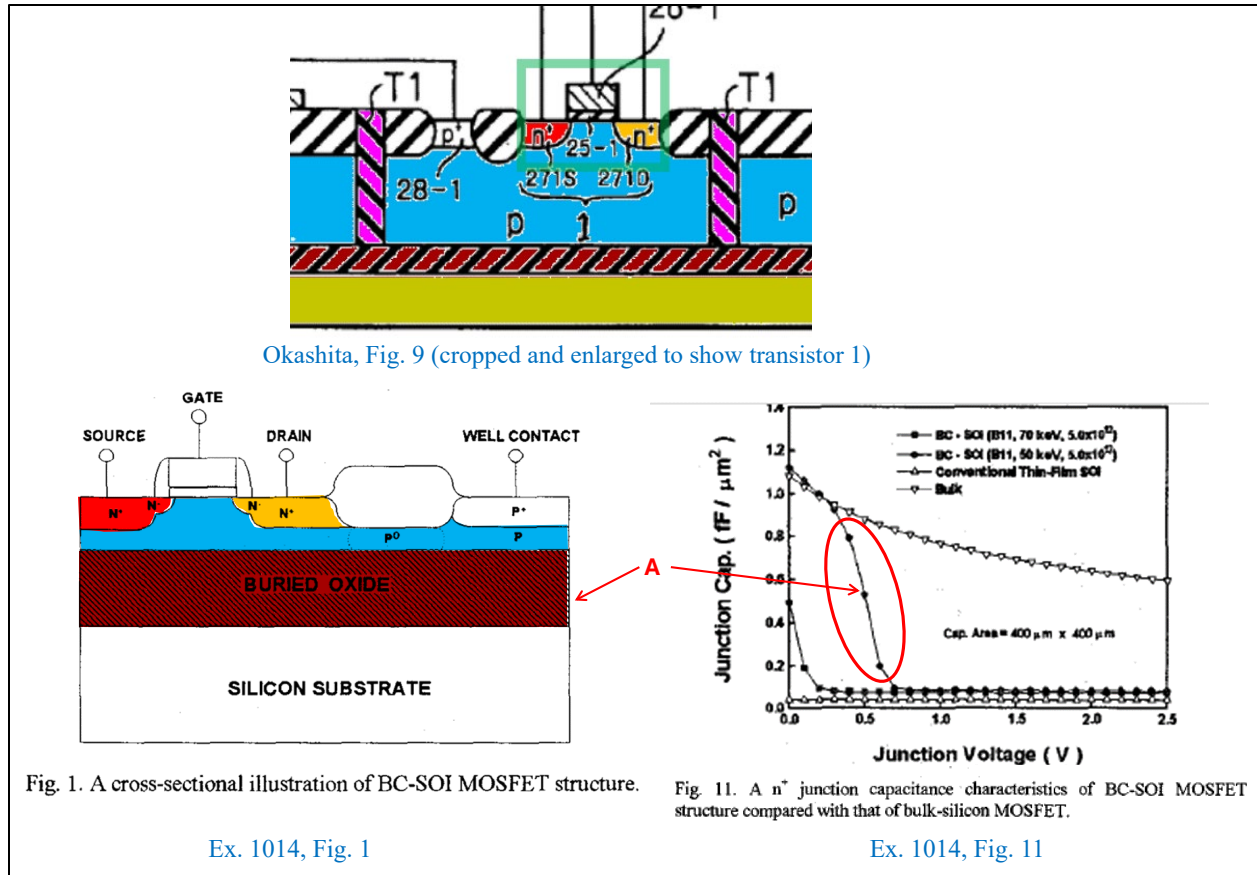
22. *Okashita*, Fig. 9. For example, this intervening thickness of the **silicon layer** **23** is marked for transistor 1 in the portion of *Okashita*'s Figure 9 reproduced above using the red double-headed arrow. Similarly, a thickness of the **silicon layer** **23** separates the bottom surfaces of the **source** **272S** and **drain** **272D** of **transistor** **2** and the top surface of the **buried oxide layer** **22**. *Okashita*, Fig. 9.

83. The presence of this intervening **silicon layer** **23** (between the bottoms of the **sources** and **drains** and the top of the **buried oxide layer** **22**) in **transistors** **1** and **2** can also be seen in Figures 11, 14, and 15 (which depict modifications of the switch apparatus of Figures 7-9), thus reaffirming this characteristic of *Okashita*'s **transistors**. See *Okashita*, 6:43-67.

84. Consistent with my explanation *supra* §VII.A with the '886 patent, the presence of the intervening **silicon layer** between the **source** and the **drain** and the **buried oxide layer** results in the **transistor** having a **source/drain** junction capacitance. Therefore, the presence of **silicon layer** **23** between the bottom of the **source** **271S**, **272S** and **drain** **271D**, **272D** and the top of **buried oxide layer** **22** in *Okashita*'s **transistors** **1** and **2**, results in these **transistors** having a **source/drain** junction capacitance (also referred to as pn junction capacitance or simply junction capacitance).

85. Indeed, as I explained, it was well known in the art that the presence of semiconductor material (such as, for example, silicon) between the source and drain and the buried oxide layer of an SOI transistor will result in the transistor having a source/drain junction capacitance. *See supra* §VI.C.

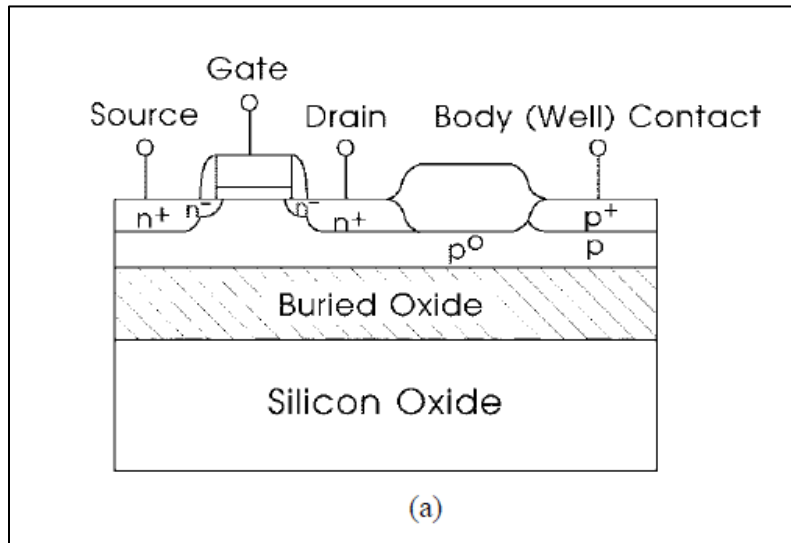
86. For example, a POSITA would have recognized that *Okashita*'s transistors 1 and 2 are body-tied (or body-contacted) SOI transistors where the p-type body (or bulk) of transistor 1 is electrically connected or "tied" to a specific voltage using taken-out region 28-1 (and the p-type body of transistor 2 is tied using taken-out region 28-2). *See Okashita*, Fig. 9. As explained *supra* §VI.C, and illustrated in the figures below, similar body-contacted transistors are known to have junction capacitance due to the semiconductor material between the source and drain and the buried oxide layer.



Okashita, Fig. 9 (cropped and enlarged); Ex. 1014, 3 (Fig. 1), 5 (Fig. 11).

87. Similar to Okashita's transistor 1 (and 2), the body-contacted (or BC) SOI MOSFET of Ex. 1014 has an n^+ -type source and drain on a p-type silicon body. As illustrated in the circled region of the curve marked A in Figure 11 on the right, until a certain value of junction voltage, this transistor has a junction capacitance higher than the normal SOI transistor. For example, Ex. 1014 notes that, "[a]s expected, BC-SOI MOSFET structure has a unique junction capacitance[.]" Ex. 1014, 3.

88. Reporting on a similar BC-SOI MOSFET structure, Ex. 1013 further explains that “[d]ue to the capacitance between the source/drain diffusion and the remaining silicon film, this device structure has larger junction capacitance than the normal SOI structure.” Ex. 1013, 26.



Ex. 1013, 26 (Fig. 48(a)).

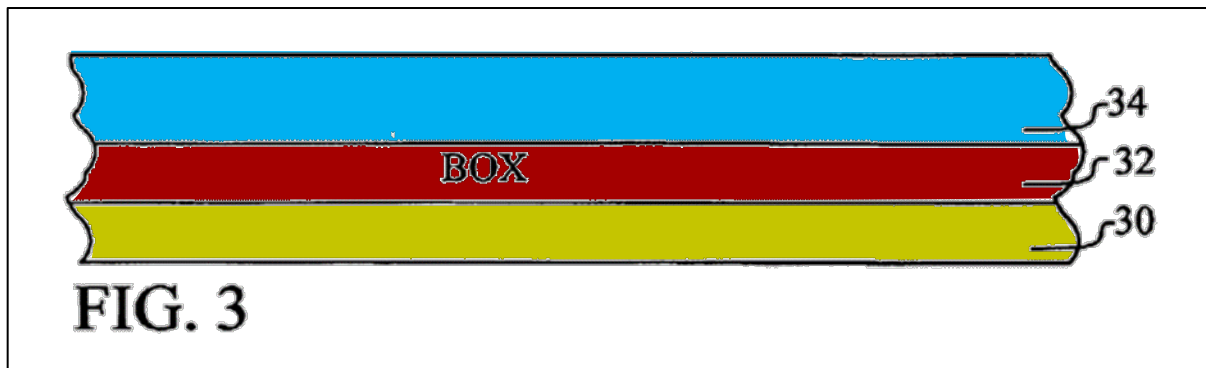
B. Yu

89. Yu, titled “High Voltage Tolerant and Low Voltage Triggering Floating-Well Silicon Controlled Rectifier on Silicon-On-Insulator for Input or Output,” was filed on July 30, 2002, and issued as a patent on May 18, 2004. I understand that Yu is prior art to the ’886 patent based both on its filing date and its issue date.

90. Yu is analogous art to the ’886 patent since both are from the same field of endeavor. For example, both patents relate to a semiconductor switching

circuit with cascaded transistors having an SOI configuration. *See Yu*, 3:43-4:15, 5:44-57, 6:4-11, 55-60; *see* '886 patent, 8:63-10:55.

91. *Yu* discloses “a low-voltage triggering, silicon-controlled rectifier” (LVT-SCR) that is fabricated as an SOI system. *Yu*, 1:10-13, 3:53-62. An SCR is a “switching device.” Ex. 1011, 18; *see also Yu*, 6:4-12. As *Yu* explains, the SOI system consists of a silicon layer 34 that is formed on top of the buried oxide layer 32, which is formed on a substrate 30, as shown in *Yu*’s Figure 3.

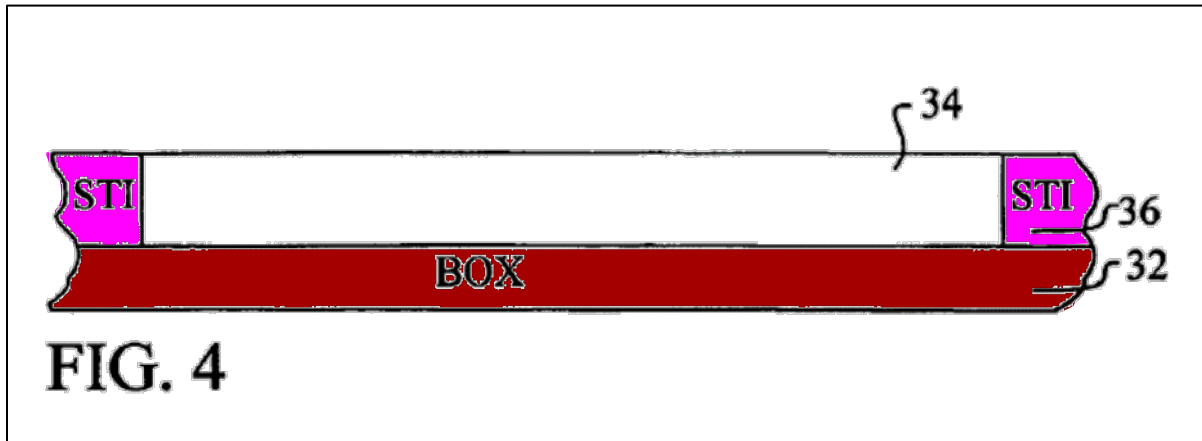


Yu, Fig. 3

92. According to *Yu*, prior art SCR devices fabricated using a bulk semiconductor uses shallow trench isolation (STI) to define areas for active devices, or OD area. *Yu*, 1:28-33. Forming SCR devices in an SOI process with STI, however, presents several problems. *Yu*, 2:4-17, 6:55-60.

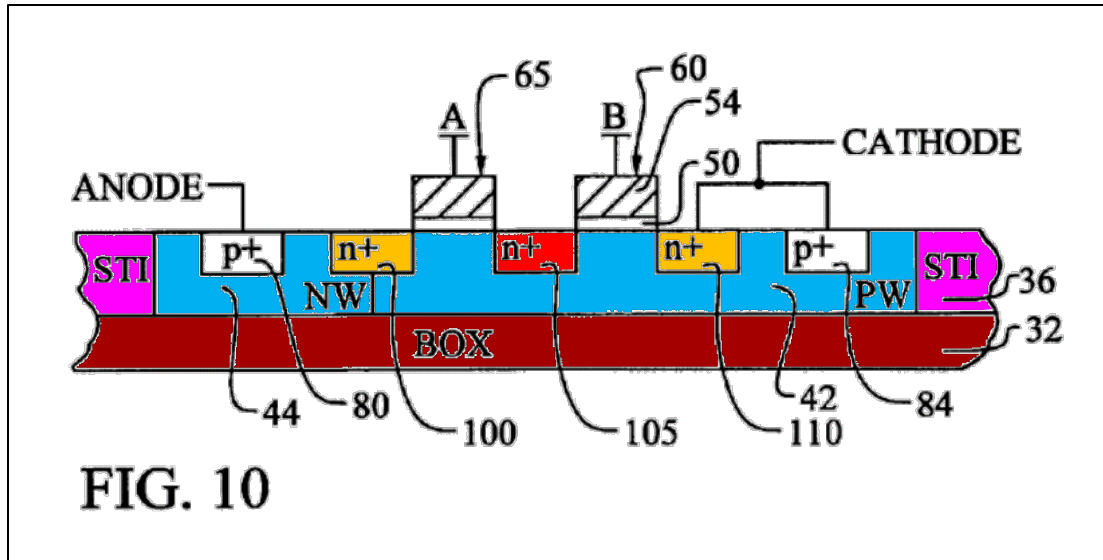
93. To address these problems, *Yu* teaches that it is important not only to form the STI regions in the silicon layer 34 of the SOI to define an active area, but to keep the STI regions outside of the active area of the planned LVT-SCR device

as shown below, contrary to prior art processes. *Yu*, 4:8-15. Indeed, these **STI regions** “do not extend into the LVT-SCR device nor do they separate the first or second type doped regions [formed in silicon layer 42, 44].” *Yu*, 5:16-19.



Yu, Fig. 4.

94. Notably, “the **STI regions** are formed down to the **buried insulator layer** such that each active area is completely isolated from other active areas.” *Yu*, 1:67-2:3. In *Yu*, the **buried oxide layer** and the **STI regions**, “reduce[] substrate coupling issues by providing excellent device-to-device isolation.” *See Yu*, 1:63-67. Accordingly, any transistors within the active area are situated within an isolated island that is surrounded by **STI regions**. *Yu*, 4:8-10, Fig. 10. Within the active area are, for example, two MOS transistors that are connected “in series” or “cascaded, or stacked,” as shown below. *Yu*, 5:44-57.



Yu, Fig. 10.

95. In Yu, “[t]wo MOS transistors are formed by the gates 60 and 65. In particular, a **first NMOS transistor** is formed by first gate 60, third doped region 110, and fourth doped region 105. A **second MOS transistor** is formed by second gate 65, fourth doped region 105, and fifth doped region 100. The **first and second transistors are in series** between the third doped region 110 and the fifth doped region 100. . . .Therefore, **the first and second NMOS transistors are cascaded**, or stacked, between the cathode terminal and the second well 44.” Yu, 5:44-57.

96. In particular, the first NMOS transistor is formed by a gate 60, a **doped region 110**, and a **doped region 105**. Yu, 5:44-46. And the second MOS transistor is formed by a gate 65, a **doped region 105**, and a **doped region 100**. Yu, 5:46-48. These doped regions 100, 105, and 110 serve as the **source** and **drains** of the **first and second transistors**. See Yu, 6:40-45. The interfaces between these

doped regions and the silicon layer 34 form source/drain junctions. *Yu*, 6:40-45, Fig. 11; *see* Ex. 1011, 10 (“pn junctions [] are formed by the drain-bulk and source-bulk interfaces in a MOSFET”), 11 (Fig. 1.36).

97. According to *Yu*, an “important feature” of its transistors is that “[t]he doped regions 80, 84, 100, 105, and 110, are formed in the upper part of the wells 42 and 44 and do not extend to the buried oxide layer 32.” *Yu*, 6:46-49, Fig. 10. In other words, “the original silicon layer ... is thick enough so that the doped regions do not completely deplete the wells 42 and 44” into the buried oxide layer 32. *Yu*, 6:50-54, Fig. 10.

98. *Yu* suggests that, since the STI 36 regions around the transistors reduce lateral heat transfer from the transistors, retaining the silicon layer 34 between the source and drain and the buried oxide layer 32 prevents heat related failures of the transistors during electrostatic discharge (ESD) events. *Yu*, 2:4-9.

C. *Burgener*

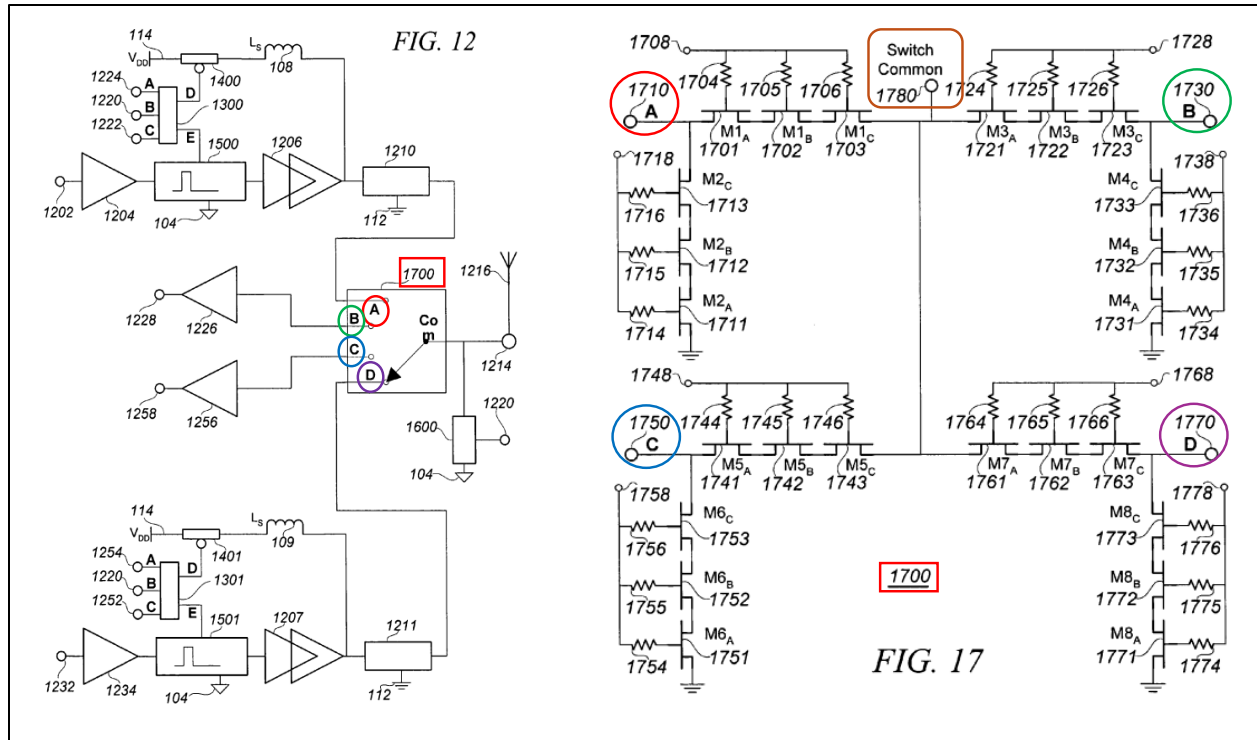
99. *Burgener*, titled “Integrated RF Front End With Stacked Transistor Switch,” was filed on August 7, 2006 and published as U.S. Patent Publication No. 2006/0270367 A1 on November 30, 2006. I understand that *Burgener* is prior art to the ’886 patent based both on its filing date and its publication date.

100. *Burgener* discloses an “integrated circuit (IC)” that includes “all RF front end or transceiver elements for a portable communication device,” such as a

cellular telephone and other wireless communications device. *Burgener*, Abstract, ¶[0006]. According to *Burgener*, the RF front end may be implemented by stacks of multiple FETs connected in series to operate as a switching device. *Burgener*, Abstract.

101. *Burgener* is analogous art to the '886 patent since both are from the same field of endeavor. For example, both relate to a semiconductor switching circuit with cascaded transistors having an SOI configuration. See *Burgener*, Abstract, ¶¶[0005]-[0006], [0105]; '886 patent, 1:14-17, 7:25-31.

102. *Burgener*'s RF transceiver, as shown in Figure 12 below, includes an "antenna switch 1700" (i.e., "a power-switching circuit" as shown in Figure 17 below) that selectably directs incoming signals from an antenna 1216 to low-noise amplifiers 1226, 1256 and outgoing signals from power amplifiers 1206, 1207 to the antenna 1216. *Burgener*, ¶¶[0085], [0090]-[0094].



Burgener, Figs. 12, 17

103. The antenna switch 1700, for example, enables the antenna 1216 (connected to common node 1780) to be selectably coupled to the different RF ports (port A 1710, port B 1730, port C 1750, or port D 1770) and to the respective low-noise and power amplifiers. *Burgener*, ¶[0102]. As an example, to transmit outgoing signals from a power amplifier 1206 or 1207, the antenna switch 1700 would connect the antenna (via a common node 1780) to port A 1710 or port D 1770. But to transmit incoming signals to low-noise amplifier 1226 or 1256, the antenna switch 1700 would connect the antenna (via a common node 1780) to port B 1730 or port C 1750. This switching function is accomplished by applying control voltages to the selected control nodes of the FETs (e.g., nodes 1708, 1718,

1728, 1738, etc.). *Burgener*, ¶¶[0090], [0092], [0101]. As illustrated in Figure 17, the antenna switch 1700 of the RF transceiver (Figure 12) includes multiple cascaded FETs. *Burgener*, Fig. 17.

104. *Burgener* discloses that “semiconductor-on-insulator (SOI) techniques” may be used to fabricate the cascaded FETs but does not provide details of their geometry or fabrication. *Burgener*, ¶[0105].

IX. LEVEL OF ORDINARY SKILL IN THE ART

105. In rendering the opinions set forth in this declaration, I have been asked to consider the '886 patent's claims and the prior art through the eyes of a person of ordinary skill in the art (which I may also refer to as “one skilled in the art,” “skilled artisan,” “POSITA,” or similar variation). I have considered factors such as the educational level and years of experience of those working in the pertinent art, the types of problems encountered in the art, the teachings of the prior art, patents and publications of other persons or companies, and the sophistication of the technology.

106. Taking the factors described in the Legal Standards – Level of Ordinary Skill section into consideration, it is my opinion that a person of ordinary skill in the art pertinent to the '886 patent (December 10, 2007) would have had at least a master's degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems and semiconductor dice.

Additional relevant work experience can compensate for less education, and vice versa.

107. I was at least a person of ordinary skill in the art as of December 10, 2007.

X. GROUNDS OF UNPATENTABILITY

108. Based on my review of the materials set forth above, including my application of the knowledge of a person of ordinary skill in the art, it is my opinion that claims 1-19 of the '886 patent would have been anticipated and/or obvious to one of ordinary skill in the art.

109. In particular, it is my opinion that claims 1-19 of the '886 patent would have been anticipated and/or obvious to a person of ordinary skill in the art based on the prior art shown below:

Ground	Challenged Claims	Basis	Prior Art
1	1, 2, 4, and 5	§102	<i>Okashita</i>
2	1-7	§103	<i>Okashita</i>
3	1-7	§103	<i>Okashita</i> and <i>Yu</i>
4	1-3	§102	<i>Yu</i>
5	1-19	§103	<i>Burgener</i> and <i>Okashita</i>
6	1-19	§103	<i>Burgener</i> , <i>Okashita</i> , and <i>Yu</i>

XI. THE CHALLENGED CLAIMS ARE UNPATENTABLE OVER THE PRIOR ART

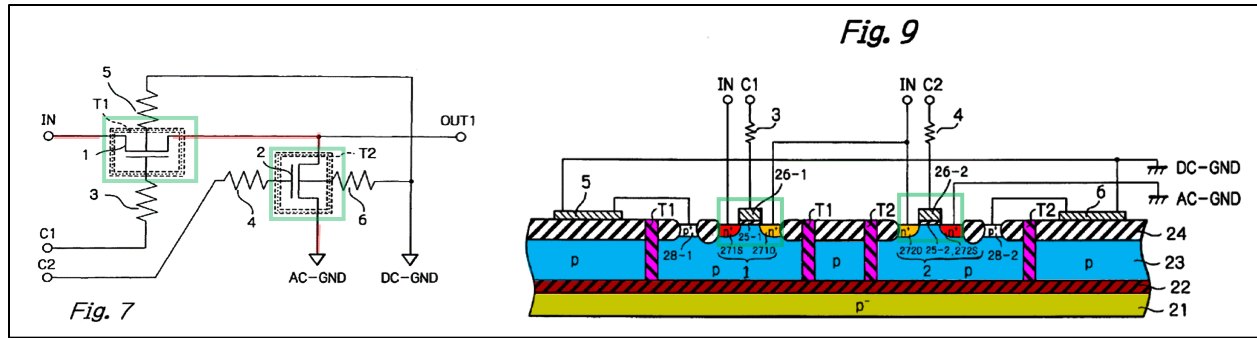
110. In my opinion, claims 1-19 would have been anticipated and/or obvious to one skilled in the art as of the earliest priority date of the '886 patent.

A. Ground 1: Claims 1, 2, 4, and 5 Are Anticipated by *Okashita***1. Independent Claim 1****a. [1pre]: “A switching circuit comprising:”**

111. To the extent the preamble is limiting, *Okashita* discloses a “semiconductor switch apparatus[] used for switching the operation of an antenna circuit and a receiving and transmitting circuit.” *Okashita*, 1:7-15. In my opinion, because *Okashita*’s “semiconductor switch apparatus” is “used for switching the operation of an antenna circuit and a receiving and transmitting circuit,” it is a switching circuit.

b. [1a]: “a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;”

112. *Okashita* discloses this limitation because *Okashita*’s MOS transistors 1, 2 are fabricated in a p-type silicon layer that is over a silicon oxide layer and a monocrystalline silicon substrate, as shown below.



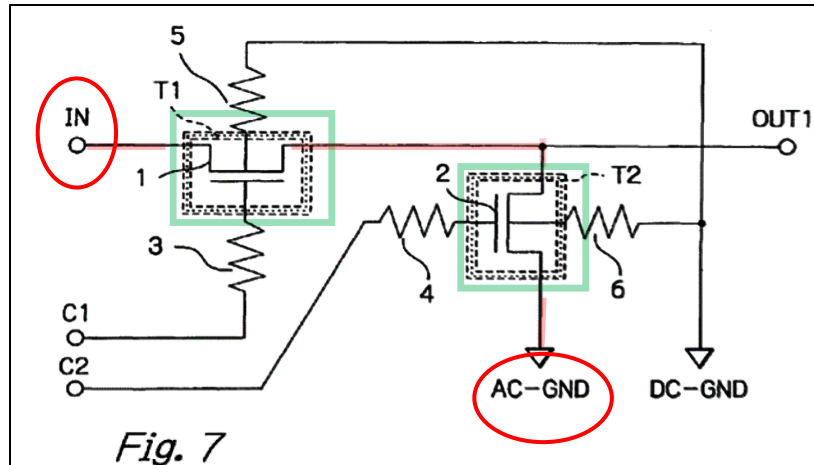
Okashita, Figs. 7, 9.

113. Figs. 7-9 illustrate an embodiment of *Okashita*'s switch apparatus with cascaded MOS transistors 1 and 2. *Okashita*, Figs. 7-9; see also Ex. 1011, 21-24 (showing examples of cascaded transistors). In *Okashita*, a silicon oxide layer 22 is formed on a monocrystalline silicon substrate 21 and a p-type silicon layer 23 is grown on the silicon oxide layer 22. *Okashita*, 5:41-46.

114. As evident from Fig. 9 above, transistors 1 and 2 are fabricated in the p-type silicon layer 23. Moreover, in its claims, *Okashita* states that its switch apparatus includes a semiconductor substrate, an insulating layer formed on the semiconductor substrate, a semiconductor layer formed on the insulating layer, "at least one series MOS transistor formed within a first region of said semiconductor layer," and "at least one shunt MOS transistor formed within a second region of said semiconductor layer." *Okashita*, 9:36-42, 10:7-16; see also *Okashita*, 5:45-49, 55-63. Given the SOI configuration outlined in the claims and detailed in the description of its embodiments (and depicted in its figures), a POSITA would have

understood that the terms “semiconductor substrate,” “insulating layer,” and “semiconductor layer” in *Okashita*’s claims correspond to the silicon substrate 21, silicon oxide layer 22, and p-type silicon layer 23, respectively, as described in the written description and figures. Additionally, *Okashita* describes MOS transistor 1 as a “series MOS transistor” and MOS transistor 2 as a “shunt MOS transistor” in its description. *Okashita*, 5:55-63. Therefore, a POSITA would have recognized that transistors 1 and 2 are “formed within” the p-type silicon layer 23. Because transistors 1, 2 are fabricated in the p-type silicon layer 23, it is the claimed device layer that is situated over a silicon oxide layer 22 and a semiconductor substrate. *Okashita*, 9:36-42, 5:40-45.

115. In my opinion, *Okashita*’s MOS transistors 1 and 2 of Figures 7-9 are “cascaded transistors.” “Cascaded transistors” refer to transistors “arranged ... in a series or in a succession of stages so that each stage derives from or acts upon the product of the preceding.” Ex. 1007, 5; *see also* Ex. 1011, 21-24 (providing multiple examples of cascaded transistors where each subsequent transistor operates on the output of the preceding one). The ’886 patent also acknowledges that transistors “coupled in series” are considered “cascaded.” ’886 patent, 6:50-51. In my opinion, a POSITA would have recognized that MOS transistors 1 and 2 in *Okashita*’s Figures 7-9 are connected in series at least from the input terminal (IN) to the AC ground terminal (AC-GND).



Okashita, Fig. 7

116. Moreover, MOS transistor 2 acts upon the output of MOS transistor 1. See Okashita, Figs. 7, 9. Specifically, when control voltages of 3V and 0V are applied to control terminals C1 and C2, MOS transistor 1 is turned ON and MOS transistor 2 is turned OFF, thereby transferring radio frequency signals applied to input terminal (IN) to output terminal (OUT). Okashita, 7:7-12; see Okashita, 3:11-16, 5:21-45, 4:11-18. When the amplitude of the radio frequency signal applied to input terminal (IN) is ΔV_{in} , $\frac{1}{2} \Delta V_{in}$ gets applied between the drain and gate of MOS transistor 2. Okashita, 7:12-15. When $\frac{1}{2} \Delta V_{in}$ exceeds the threshold voltage of MOS transistor 2, it would turn ON and the radio frequency signals passing through MOS transistor 1 would pass through MOS transistor 2 to the ground. Okashita, 7:15-17. Thus, at least when C1=3V, C2=0V, and the threshold voltage of MOS transistor 2 $< \frac{1}{2} \Delta V_{in}$ (or when $\frac{1}{2} \Delta V_{in}$ exceeds the threshold voltage (V_{th}) of MOS transistor 2), MOS transistor 2 receives, and acts upon, the

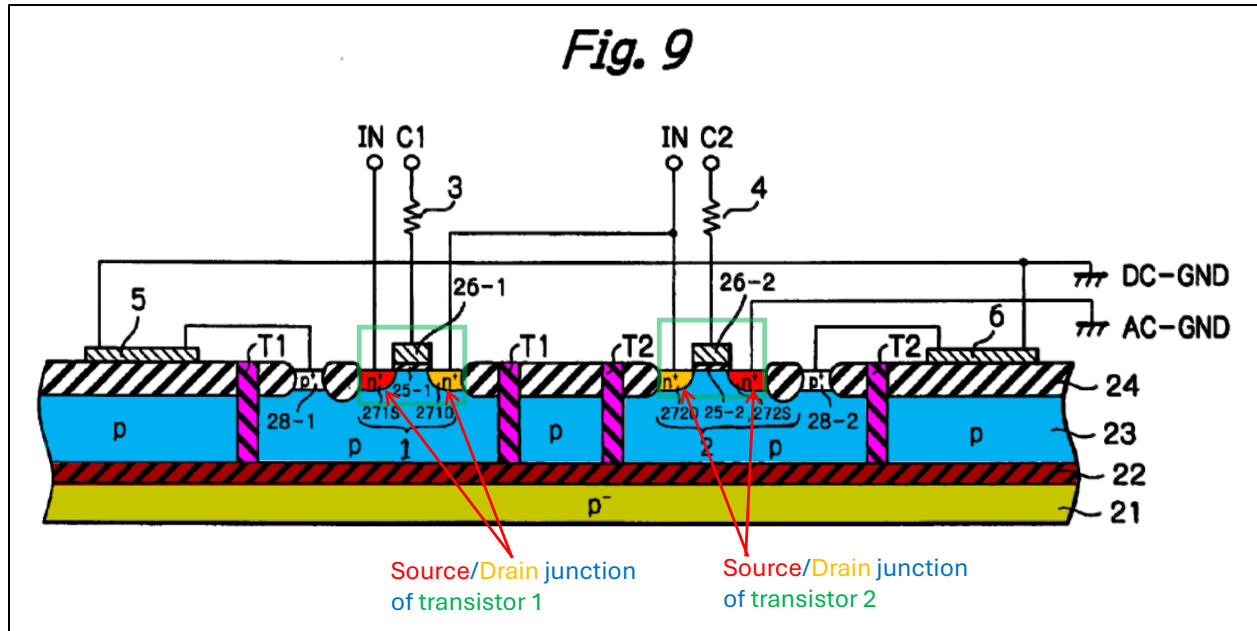
output of MOS transistor 1. Therefore, in my opinion, MOS transistors 1 and 2 are “cascaded.”

117. Thus, cascaded transistors 1 and 2 are fabricated in silicon layer 23 (“device layer”) situated over silicon oxide layer 22 (“buried oxide layer”) and silicon substrate 21 (“bulk semiconductor layer”).

c. [1b(i)]: “each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer,”

118. *Okashita* discloses this limitation because the source/drain junctions of MOS transistors 1, 2 do not contact the silicon oxide layer 22.

119. In my opinion, a POSITA would have recognized that the source/drain junction of a transistor refers to the interface between the source and drain regions and the silicon layer on which the source and drain are formed. *See, e.g.*, Ex. 1011, 10 (“pn junctions [] are formed by the drain-bulk and source-bulk interfaces in a MOSFET”), 11 (Fig. 1.36); *see* Ex. 1010, 43. Specifically, the source/drain junction of transistor 1 is where its doped source and drain regions (n+-type impurity doped regions 271S and 271D) meet the p-type silicon layer 23. *See Okashita*, 5:55-63. Similarly, the source/drain junction of transistor 2 is where its doped source and drain regions (n+-type impurity doped regions 272S and 272D) meet the p-type silicon layer 23.



Okashita, Fig. 9.

120. As depicted in Fig. 9, the interface between **source 271S** and the **p-type silicon layer 23** does not make contact with the **buried oxide layer 22**, nor does the interface between **drain 271D** and **silicon layer 23**. This results in the **source/drain junction of transistor 1** being separated from **buried oxide layer 22**. Similarly, the interface between **silicon layer 23** and **source 272S** and **drain 272D** of **transistor 2** (and thus its **source/drain junction**) also does not contact **buried oxide layer 22**. Instead, there is an intervening layer of **silicon material (layer 23)** between the **source/drain junctions of transistors 1 and 2** and the top of **buried oxide layer 22**. See Okashita, Fig. 9.

121. The cross-sectional views of **transistors 1 and 2** in Figures 11, 14, and 15, which depict modifications of the switch apparatus shown in Figures 7-9 (see

Okashita, 6:43-67), also demonstrate the presence of the intervening silicon layer 23 between the source/drain junctions of transistors 1 and 2 and the top surface of buried oxide layer 22, thus reaffirming this characteristic of *Okashita*'s transistors 1 and 2.

122. In my opinion, these figures (Figs. 9, 11, 14-15) in *Okashita* clearly and unambiguously convey to a POSITA that the source/drain junctions of transistors 1 and 2 do not make contact with the top surface of the buried oxide layer 22. Instead, there is an intervening silicon layer 23 between the bottom of the sources and drains of these transistors and the top of the buried oxide layer 22. This conclusion is based on what is clearly illustrated in the figures rather than on any measurements made on these figures. For example, the presence of the silicon layer 23 between the bottom of the sources and drains of transistors 1 and 2 and the top of the buried oxide layer 22 is clearly visible in these figures and needs no measurements.

d. [1b(ii)]: “thereby forming a source/drain junction capacitance;”

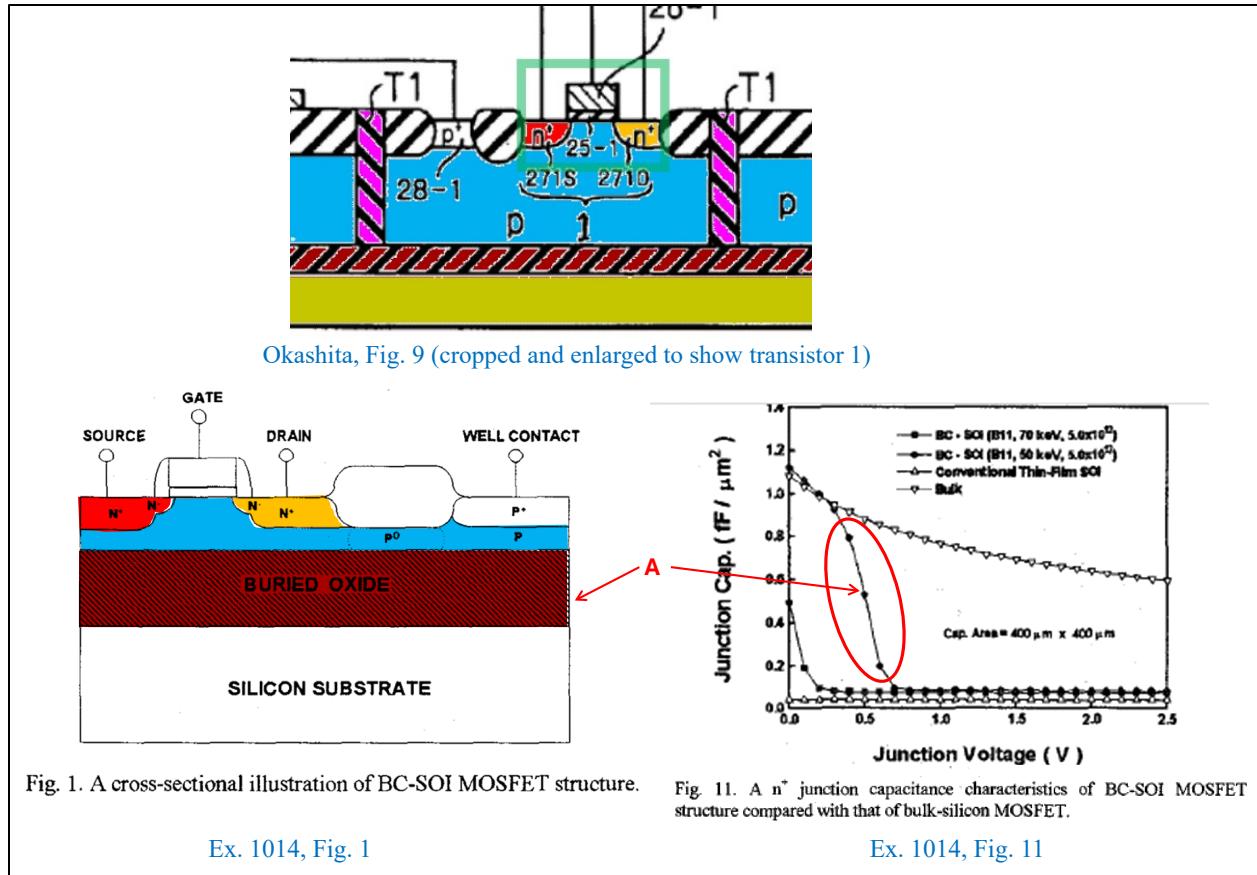
123. In my opinion, *Okashita*'s cascaded MOS transistors 1 and 2 have a source/drain junction that forms a source/drain junction capacitance. As explained *supra* §VII.A, even according to the '886 patent, when device layer remains between the bottom surfaces of the source and drain and the top surface of the buried oxide layer, a semiconductor junction with associated source/drain junction

capacitance is formed within the **device layer**. '886 patent, 4:11-18, 5:63-65 (“This remaining semiconductor **would** result in source/drain junction capacitance[.]”).

Conversely, when there is little to no semiconductor material (**device layer**) between the **source** or **drain** and the top surface of the **buried oxide layer**, there is minimal or no semiconductor junction to create a capacitive load resulting in low or non-existent junction capacitance. '886 patent, 3:17-28.

124. Thus, in my opinion, consistent with the '886 patent, a POSITA would have recognized that the presence of **silicon layer 23** between the bottom surfaces of the **sources** (271S and 272S) and the **drains** (271D and 272D) of **transistors 1 and 2**, and the top surface of **buried oxide layer 22** (*see supra* §XI.A.1.c; *see also Okashita*, Fig. 9) results in the **source/drain** junctions of **transistors 1 and 2** having a **source/drain** junction capacitance.

125. Moreover, as explained *supra* §VI.C, it was well known in the art that when an SOI transistor has a **silicon layer** between the bottom of its **source** and **drain** and the top of the **buried oxide layer**, such “structure has larger junction capacitance than the normal SOI structure.” Ex. 1013, 25-26; Ex. 1014, 3, 5. Furthermore, as explained *supra* §VIII.A, a body-contacted NFET similar to *Okashita*’s **transistor 1 and 2**, was known to have a junction capacitance higher than the normal SOI transistor and lower than bulk silicon transistor. Ex. 1014, 3, 5; Ex. 1013, 26.



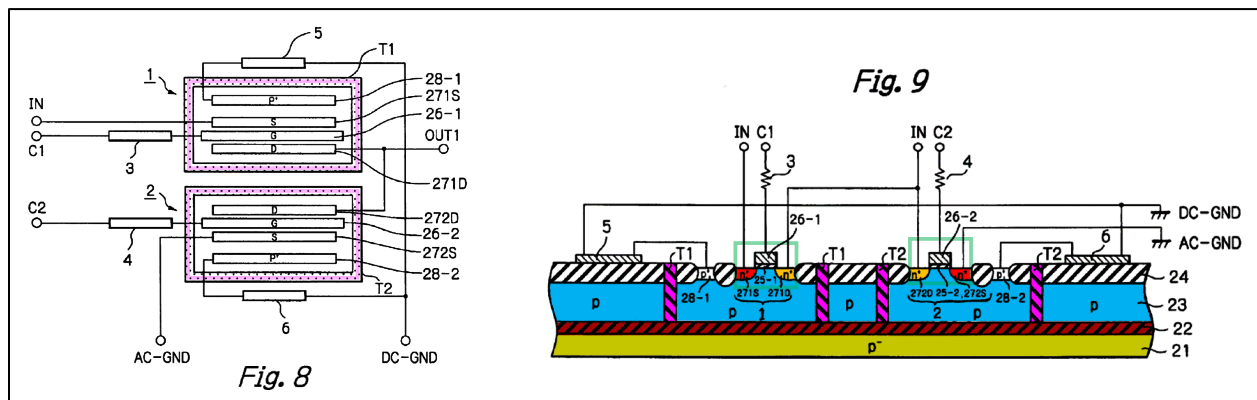
Okashita, Fig. 9 (cropped and enlarged); Ex. 1014, 3 (Fig. 1), 5 (Fig. 11).

126. Specifically, in the transistor of Ex. 1014, which is similar to Okashita's transistors 1 and 2, the presence of silicon material between the bottom surfaces of the source and drain and the top surface of the buried oxide layer resulted in a junction capacitance (see the circled region of the curve marked A in Figure 11 on the right above), higher than that in a conventional thin-film SOI transistor (curve with datapoints marked Δ) and lower than that in a bulk silicon transistor (curve with datapoints marked ∇). Ex. 1014, 2-5; Ex. 1013, 26; *supra* §VI.C.

127. Therefore, in my opinion, *Okashita*'s cascaded MOS transistors 1 and 2 have a source/drain junction that forms a source/drain junction capacitance.

- e. [1c(i)]: “at least one trench extending through said device layer and contacting a top surface of said buried oxide layer,”

128. *Okashita* discloses this limitation because *Okashita*'s trenches T1, T2 extend through the silicon layer 23 to contact the top surface of silicon oxide layer 22, as illustrated in Figure 9 below. See *Okashita*, Fig. 9.



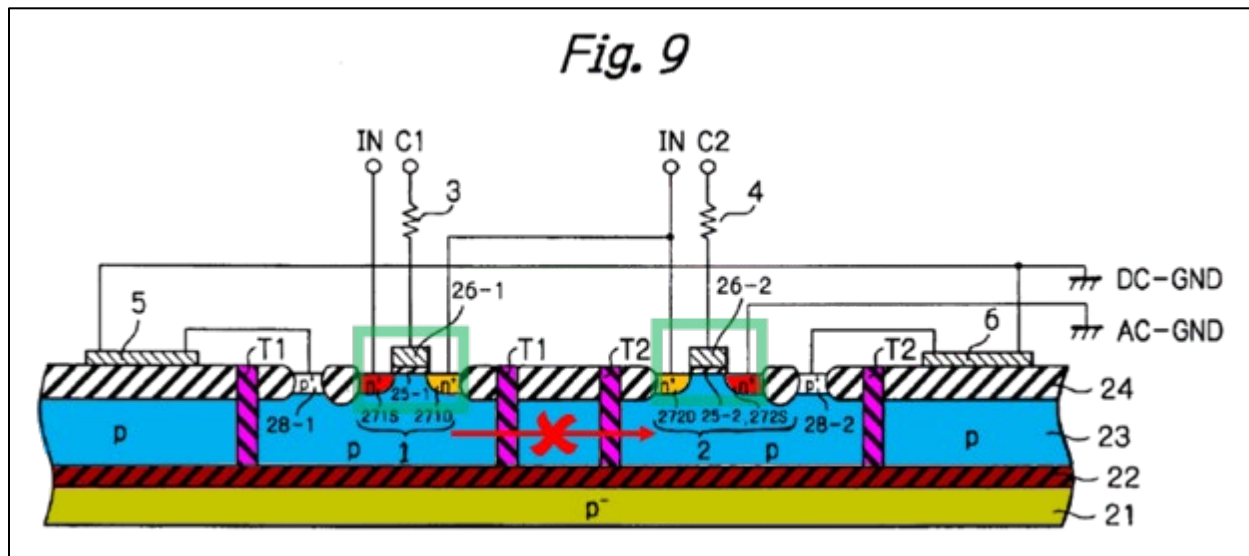
Okashita, Figs. 8-9.

129. In *Okashita*, “[t]rench insulating layers T1 and T2 are buried in trenches (grooves) in the field silicon oxide layer 24 and the silicon layer 23 [“device layer”]. For example, a photoresist pattern for the trenches is formed in the field silicon oxide layer 24 and the silicon layer 23 by a photolithography process. Then, a plasma dry etching process is performed upon the field silicon oxide layer 24 and the silicon layer 23 using the photoresist pattern as a mask. Finally, a silicon oxide layer is buried in the trenches.” *Okashita*, 5:46-54. As

illustrated in Figure 9, *Okashita's* trenches T1 and T2 extend through the silicon layer 23 and contact the top surface of buried oxide layer 22. See *Okashita*, Fig. 9.

This conclusion is based on what is clearly illustrated in Figure 9 rather than on any measurements made on this figure. For example, trenches T1 and T2 extending through the silicon layer 23 and contacting the top surface of buried oxide layer 22 is clearly visible in Figure 9 and needs no measurements.

130. Moreover, in my opinion, a POSITA reading *Okashita* would have understood that trenches T1, T2 contact the top surface of silicon oxide layer 22 because the trenches T1, T2 not only completely surround the respective MOS transistors 1, 2 (*Okashita*, 5:55-63), they also suppress any leakage of radio frequency signals through the silicon layer 23, as shown by the “x” mark in the figure below. *Okashita*, 6:1-16.



Okashita, Fig. 9.

131. With reference to Figure 9, *Okashita* discloses that, “since the [] MOS transistor 1 is surrounded by the trench insulating layer T1 and the [] MOS transistor 2 is surrounded by the trench insulating trench layer T2,” leakage of radio frequency signals from silicon layer 23 surrounded by the trench insulating layer T1 via the silicon layer 23 between the trenches T1 and T2 to the silicon layer 23 surrounded by the trench T2 can be suppressed. *Okashita*, 6:8-16. Based at least on this disclosure, it is my opinion that a POSITA would have understood that the trenches T1, T2 contact the top surface of the silicon oxide layer 22 to suppress signal leakage through a gap that may otherwise exist between the trenches T1 and T2 and the silicon oxide layer 22.

132. Similarly, because of trenches T1 and T2, leakage of signals from the silicon layer 23 surrounded by the trench T1 to the silicon layer 23 surrounded by trench T2 via the silicon substrate 21 can be suppressed. *Okashita*, 6:1-7. In my opinion, a POSITA would have understood that, to prevent leakage of signals between silicon layer 23 surrounded by trench T1 and silicon layer 23 surrounded by trench T2 in this manner, the trenches, T1 or T2 must contact the top surface of the buried oxide layer 22. This contact is necessary to prevent signal leakage through any gap between the bottom of trenches T1 and T2 and the buried oxide layer 22. *Okashita*, 6:1-7.

- f. [1c(ii)]: “thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.”

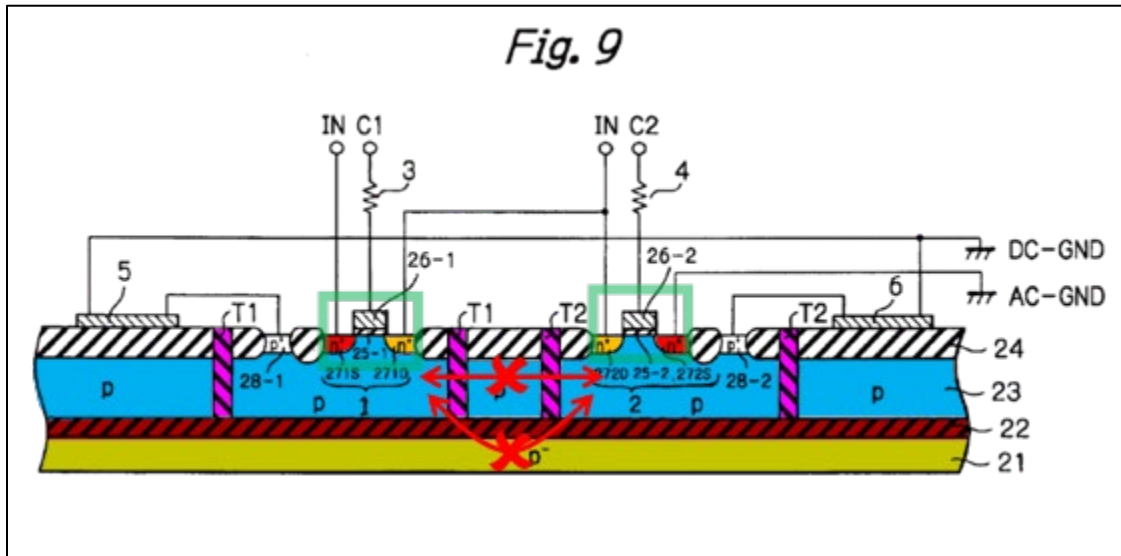
133. *Okashita* discloses this limitation because the trenches T1, T2, extending through the silicon layer 23 and contacting a top surface of the silicon oxide layer 22, suppress any leakage of electrical signals between the MOS transistor 1 and the MOS transistor 2 through the silicon layer 23 and via the silicon substrate 21. *Okashita*, 6:1-16; *supra* §XI.A.1.e.

134. As explained *supra* §XI.A.1.e, because of trenches T1 and T2 extending through the silicon layer 23 to contact the buried oxide layer 22, leakage of radio frequency signals from silicon layer 23 surrounded by the trench insulating layer T1 via the silicon layer 23 between the trenches T1 and T2 to the silicon layer 23 surrounded by the trench T2 can be suppressed. *Okashita*, 6:8-16. *Okashita* also discloses that, because of the trenches T1 and T2, leakage of signals from the silicon layer 23 surrounded by the trench T1 to the silicon layer 23 surrounded by trench T2 via the silicon substrate 21 can also be suppressed. *Okashita*, 6:1-7. Moreover, *Okashita* discloses that “MOS transistor 1 is isolated by a trench insulating layer T1 from the other elements, and [] MOS transistor 2 is isolated by a trench insulating layer T2 from the other elements.” *Okashita*, 5:29-32.

135. Thus, in my opinion, a POSITA would have recognized that trench T1 electrically isolates transistor 1 from other components (including transistor 2) of the switch apparatus, and trench T2 electrically isolates transistor 2 from other components (including transistor 1). This isolation prevents signals from these components from reaching silicon layer 23 around transistor 1 and transistor 2 and inducing voltage and current fluctuations in that area. *See* Ex. 1023, 3 (explaining that “oxide vertical trenches” between two circuits reduce “voltage and current fluctuations” (e.g., substrate noise) resulting from the switching of transistors in one circuit from causing spurious state changes in the transistors of another circuit).

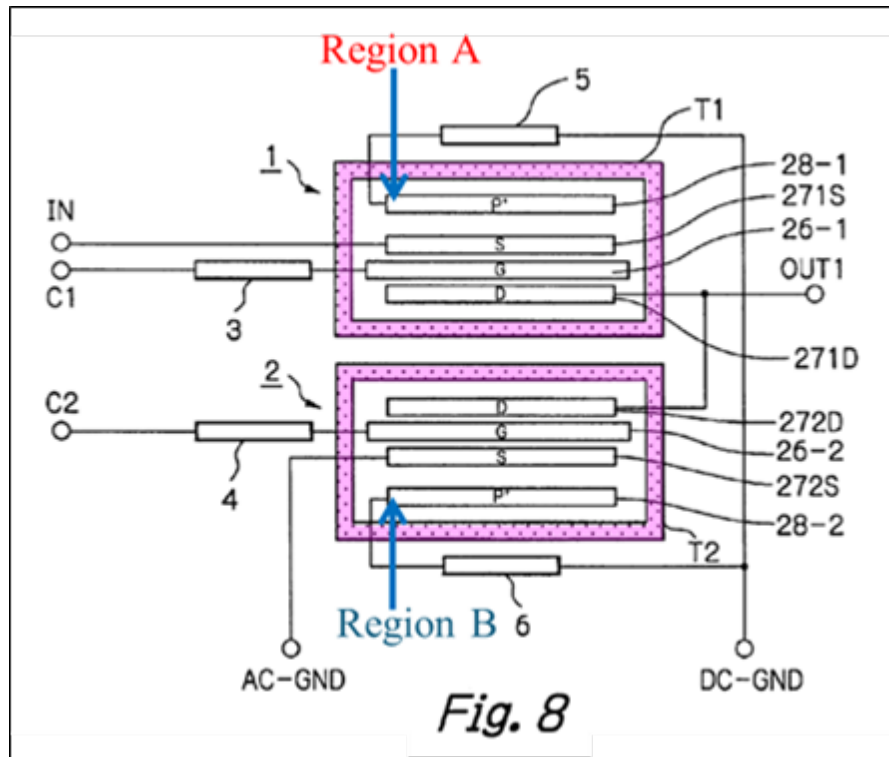
136. As the '886 patent explains, when a transistor is fabricated in an island surrounded by trenches that extend through the device layer and contact the buried oxide layer, the transistor “is electrically isolated from neighboring islands ... by trenches ... and buried oxide layer ... [thereby allowing the transistor] to experience positive and negative voltage excursions without affecting neighboring devices[.]” '886 patent, 2:65-3:11; *see also* '886 patent, 6:10-15. As a result of such electrical isolation, the switching circuit “exhibit[s] reduced voltage and current fluctuations on the device layer.” '886 patent, 6:33-42. *Okashita's* MOS transistors 1, 2 are similarly fabricated in islands that are surrounded by trenches

T1, T2, which electrically isolate the MOS transistors 1, 2 from other components of the switch apparatus, as shown below. *Okashita*, 5:29-32.



Okashita, Fig. 9.

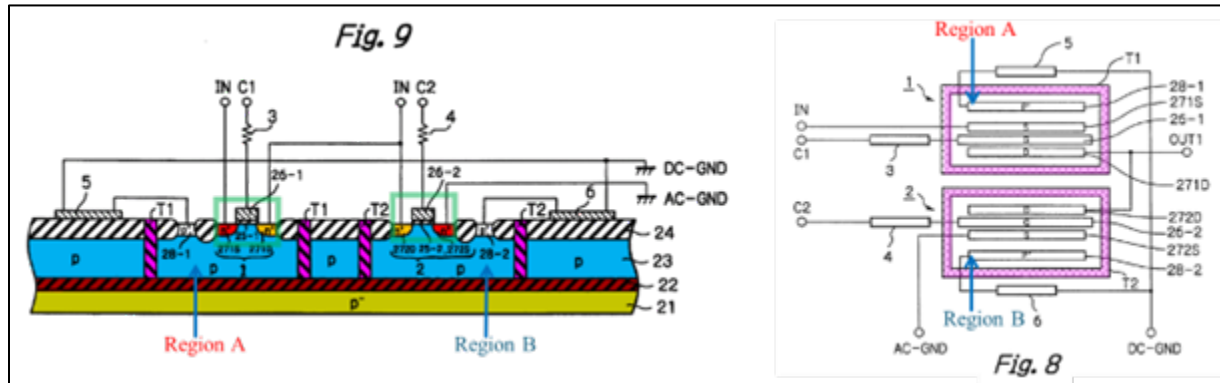
137. In my opinion, a POSITA would have recognized that, without such electrical isolations, any leakages of electrical signals from the MOS transistor 1 (Region A in the below Figure 9) to the MOS transistor 2 (Region B) would cause the voltage and current in the MOS transistor 2 to change or fluctuate. *Okashita*, 3:11-16, 7:7-12.



Okashita, Fig. 8.

138. For example, when 3V is applied to control terminal C1 of the MOS transistor 1 to turn it ON, and 0V is applied to control terminal C2 of the MOS transistor 2 to turn it OFF (to transfer signals from IN to OUT1, (see Okashita, 3:11-16, 7:7-12), leakage of electrical signals from silicon layer 23 of Region A to silicon layer 23 of Region B would cause the voltage and current in silicon layer 23 of Region B to change or fluctuate from a value of 0. Electrically isolating Region A from Region B in Okashita using trenches T1 and T2 suppresses any leakage of electrical signals and, thereby, reduces the resulting voltage and current fluctuations (or electrical noise) in the silicon layer 23 of Region B. Okashita, 5:29-32; see Ex. 1010, 187-189 (explaining that the use of dielectric isolation

reduces circuit noise); *see* Ex. 1023, 3 (explaining that “oxide vertical trenches” between two circuits reduce “voltage and current fluctuations” (e.g., substrate noise) resulting from the switching of transistors in one circuit from causing spurious state changes in the transistors of another circuit).



Okashita, Figs. 8-9.

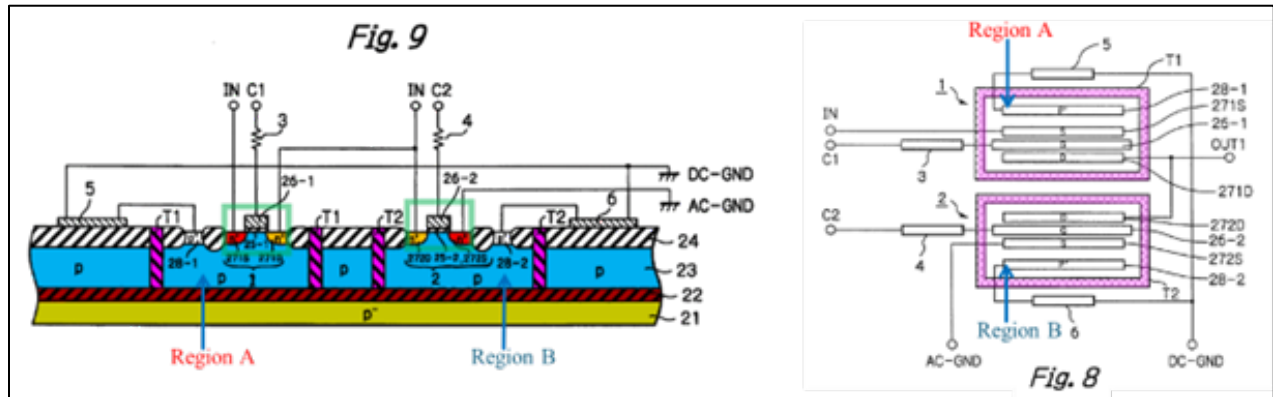
139. Thus, in my opinion, a POSITA would have recognized that *Okashita*’s MOS transistors 1, 2 are fabricated in electrically isolated islands that are surrounded by trenches T1 and T2 that extend through silicon layer 23 to contact the top surface of silicon oxide layer 22. Consequently, the voltage and current fluctuations in silicon layer 23 will be reduced. *See* Ex. 1010, 187-189.

2. Claim 2

- a. [2]: “The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer.”

140. *Okashita* discloses this limitation because at least *Okashita*’s MOS transistor 1 is formed in “an area” (i.e., Region A) that is “surrounded by” trench

T1 and “isolated” from the other elements of the switch apparatus. *Okashita*, 5:29-32, 55-63; *supra* §§XI.A.1.e-XI.A.1.f.



Okashita, Figs. 8-9.

141. In *Okashita*, the MOS transistor 1 is formed “[i]n an area surrounded by the trench insulating layer T1.” *Okashita*, 5:55-63. As I explained *supra* §§XI.A.1.e-XI.A.1.f, trench T1 extends through silicon layer 23 to contact the top surface of buried oxide layer 22. Moreover, *Okashita* discloses that “transistor 1 is isolated by [] trench insulating layer T1 from the other elements” of the switch apparatus. *Okashita*, 5:29-32. Thus, the MOS transistor 1 is situated within an isolated island (i.e., Region A) in silicon layer 23 defined by the side walls of trench T1 and the top surface of buried oxide layer 22.

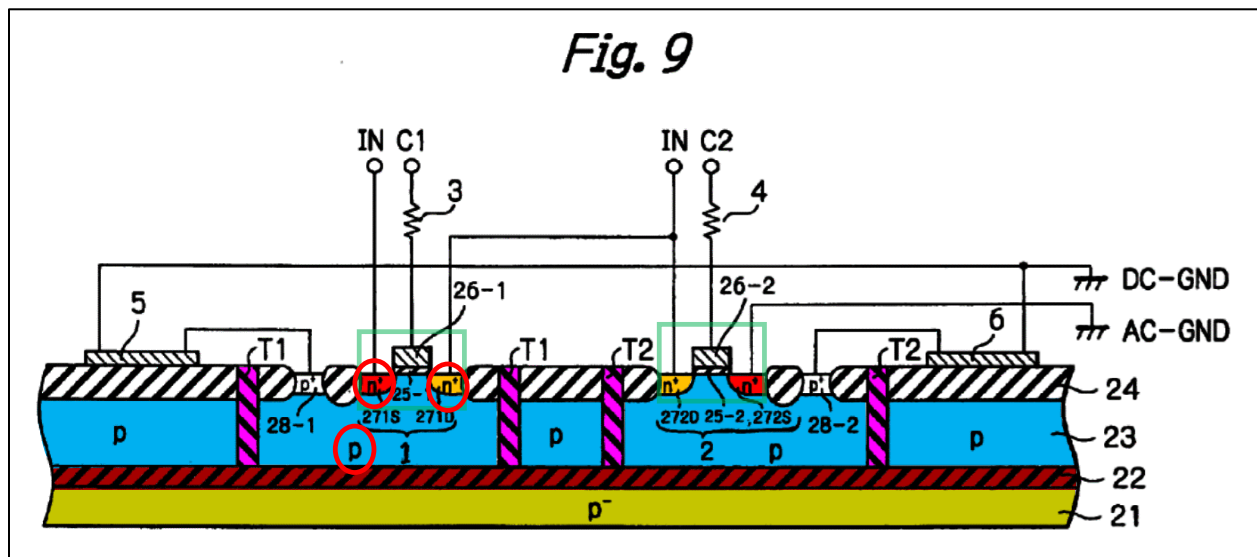
3. Claim 4

- a. [4]: “The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is an

NFET with a gate driven by a switch control signal in a wireless communications device.”

142. *Okashita* discloses this limitation because *Okashita*’s MOS transistors 1 and 2 are NFETs. *Okashita*’s MOS transistors 1 and 2 are composed of a p-type silicon body (p-type silicon layer 23) with n⁺-type source 271S and drain 271D.

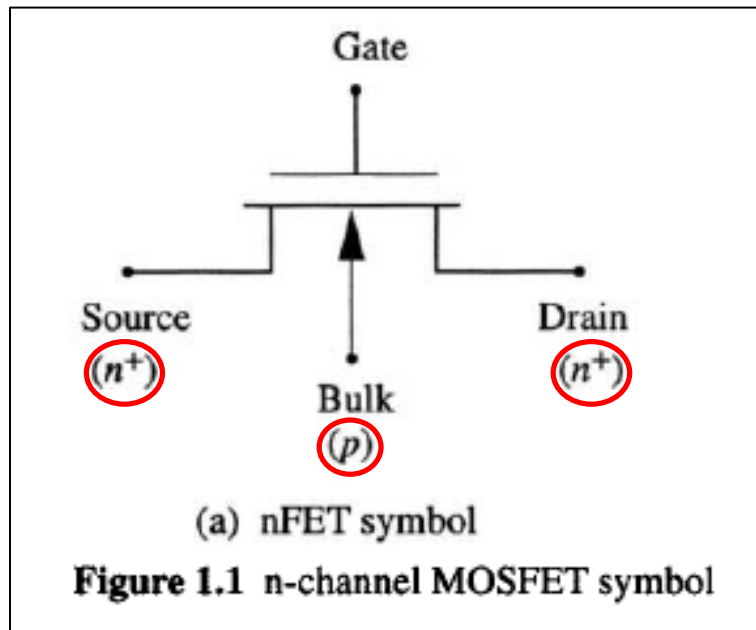
Okashita, 5:40-43, 55-63, Fig. 9.



Okashita, Fig. 9.

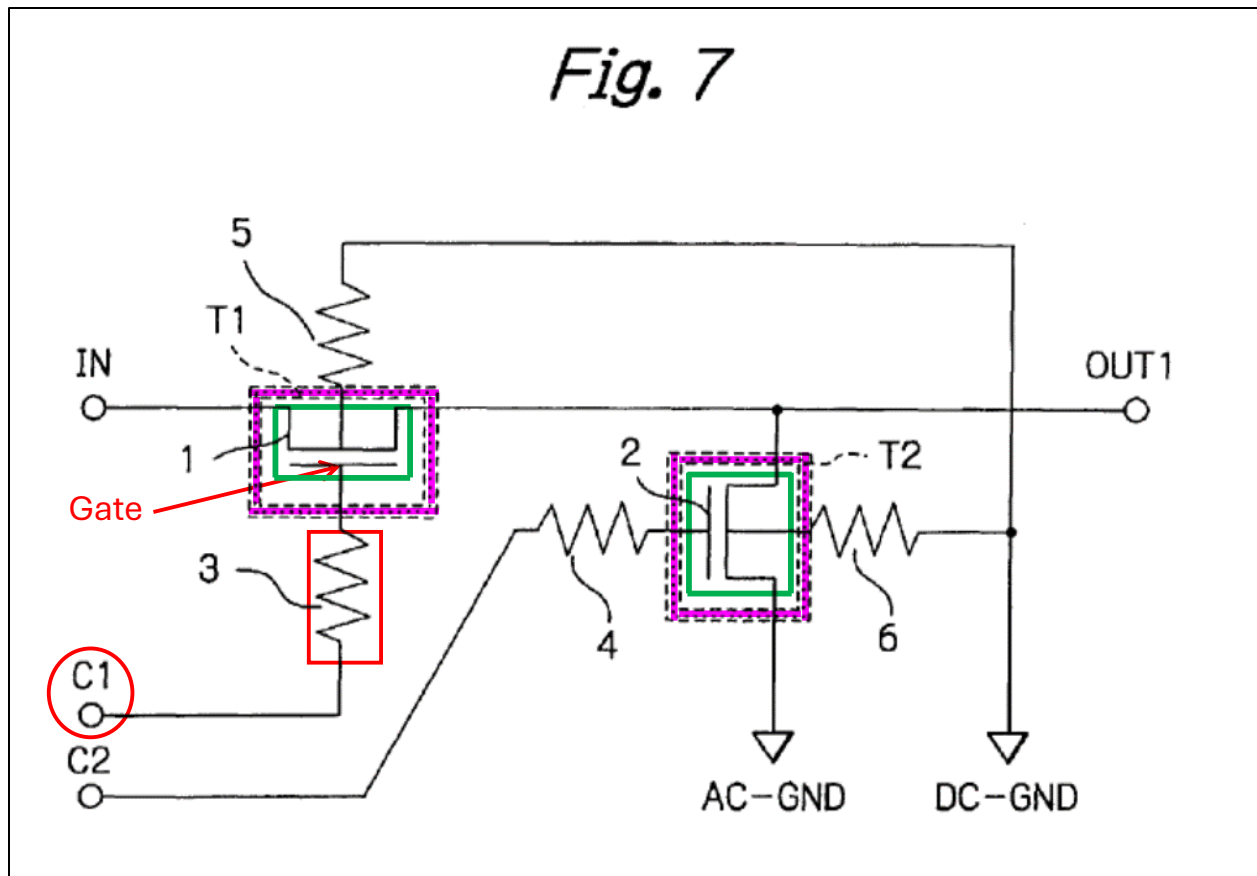
143. In my opinion, a POSITA would have recognized this configuration as an NMOSFET (or NFET) structure. See Ex. 1011, 7-8; Ex. 1010, 36-37; Ex. 1012, 2 (“The NFET starts with an underlying body or substrate of p-type silicon. Two side by side regions in the top of the substrate are changed to n-type silicon by introducing (or implanting) a higher concentration of n-type dopant atoms than the concentration of p-type dopant atoms in the substrate.”). Moreover, as

illustrated in the below figure, an NFET has n⁺-type **source** and **drain** with a **p-type body**, which is identical in structure with *Okashita*'s **MOS transistors 1, 2**.



Ex. 1011, 7 (Fig. 1.1(a)).

144. In addition, the gate of *Okashita*'s MOS transistor 1 is driven by a switch control signal C1. *Okashita*, 7:7-12. For example, *Okashita* explains that “the control voltages applied to the control terminals C1 and C2” control whether the MOS transistors 1 and 2 are turned ON or OFF. *Okashita*, 7:7-12.



Okashita, Fig. 7.

145. When 0V is applied to control terminal C1, transistor 1 is turned OFF and when 3V is applied to C1, **transistor 1** is turned ON. *Okashita, 7:7-13*. Thus, **MOS transistor 1** is driven between an OFF state and an ON state by applying 0V and 3V to control terminal C1 connected to its gate.

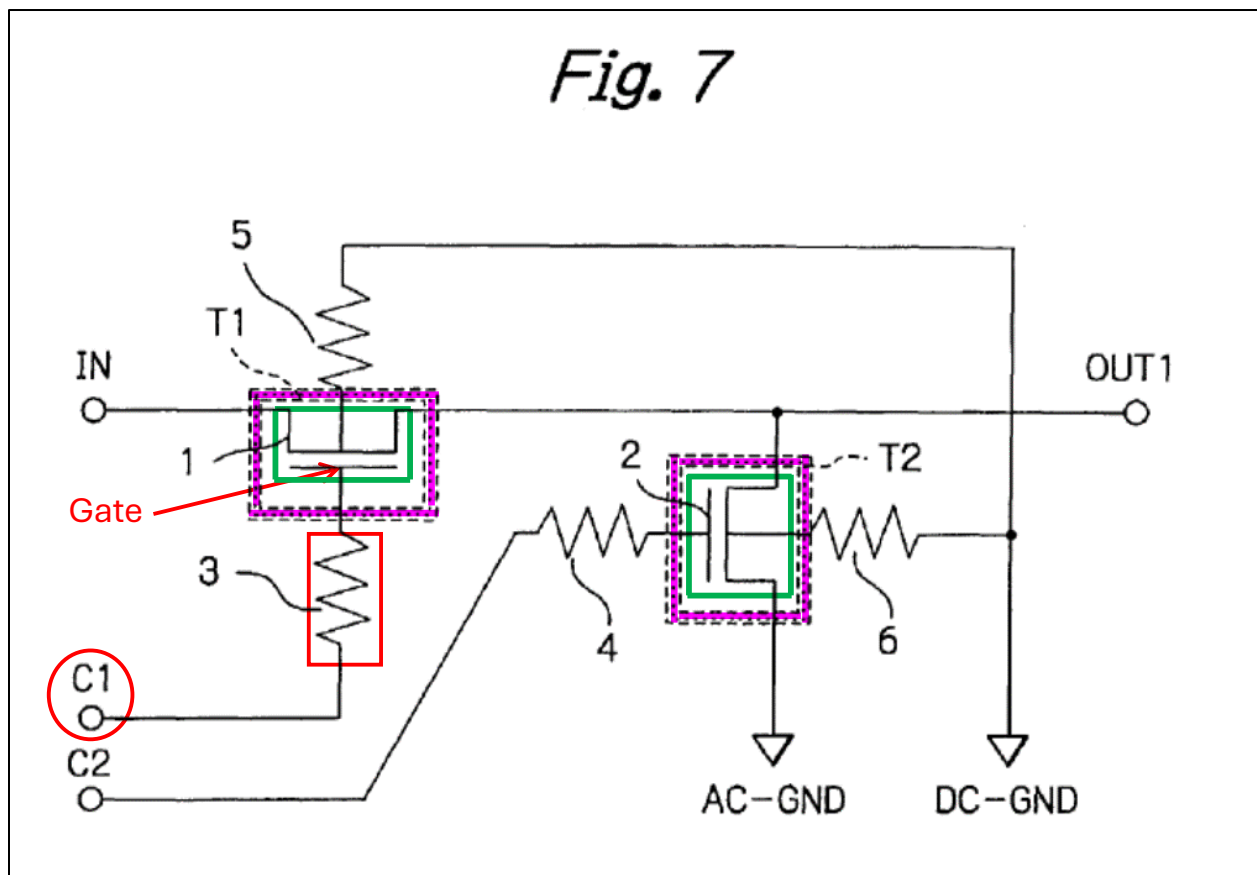
146. *Okashita's* also discloses that its switch apparatus may be used in "a mobile communication apparatus such as a mobile telephone apparatus ... for switching the operation of an antenna circuit and a receiving and transmitting

circuit.” *Okashita*, 1:11-15. Thus, *Okashita*’s MOS transistor 1 is an NFET with its gate driven by a switch control signal in a wireless communications device.

4. Claim 5

- a. [5]: “The switching circuit of claim 4, wherein said switch control signal drives said gate of said NFET through at least one resistor.”

147. *Okashita* discloses this limitation because the control terminal C1 is connected to the gate of the MOS transistor 1 through a gate protection resistor 3, as shown in Figure 7. *Okashita*, 5:64-67, Figs. 7-9.



Okashita, Fig. 7.

148. As shown in Figures 7-9, control terminal C1 is connected to the gate of transistor 1 through a gate protection resistor 3. *Okashita*, 5:64-67. Therefore, the switch control signal discussed *supra* §XI.A.3.a drives the gate of transistor 1 through resistor 3.

B. Ground 2: Claims 1-7 Are Obvious over *Okashita*

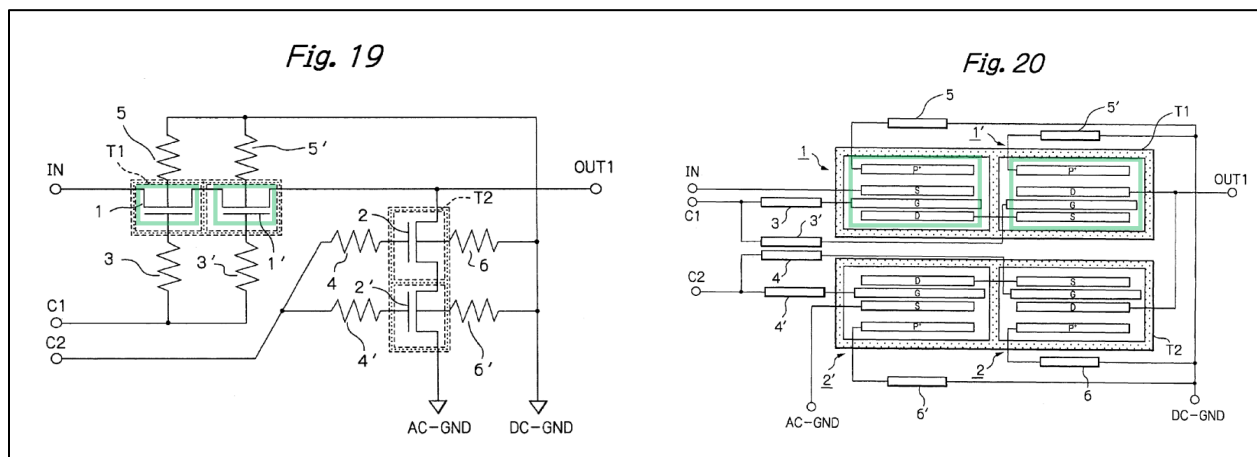
1. Independent Claim 1

a. [1pre]: “A switching circuit comprising:”

149. To the extent the preamble is limiting, *Okashita* discloses this limitation for the same reasons as stated for [1pre] of ground 1. *Supra*, §XI.A.1.a.

b. [1a]: “a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;”

150. *Okashita* teaches this limitation because *Okashita*’s switch apparatus includes a plurality of transistors connected in series, as shown below. For example, in Figures 19-20, a MOS transistor 1’ is “connected in series” to the “MOS transistor 1 of Fig. 7[.]” *Okashita*, 8:30-37.



Okashita, Figs. 19-20.

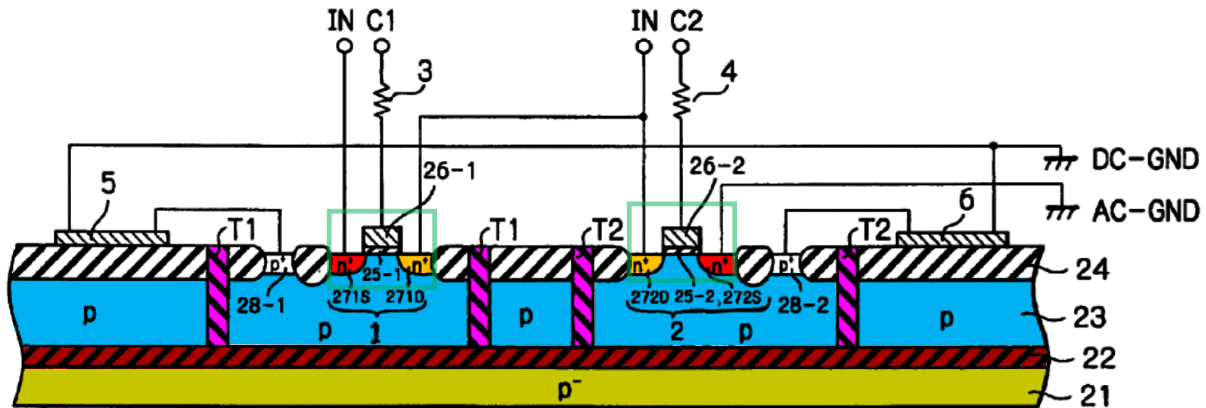
151. For example, *Okashita* discloses that, in switch apparatus of Figures 19-20, “a series MOS transistor 1’ along with its gate protection resistor 3’ ... is connected in series to the series MOS transistor 1 of FIG. 7.” *Okashita*, 8:30-34. Although a specific number of resistors are shown connected in series, *Okashita* notes that “three or more series MOS transistors can be connected in series.” *Okashita*, 8:65-67; *see also Okashita*, 2:19-21, 5:36-40, Figs. 7-9; ’886 patent, 6:50-51. Accordingly, **transistors 1 and 1’** are cascaded transistors.

152. As explained *supra* §XI.A.1.b, *Okashita*’s **MOS transistor 1** is fabricated in a device layer (**silicon layer 23**) situated over a buried oxide layer (**silicon oxide layer 22**) and a bulk semiconductor layer (**monocrystalline silicon substrate 21**). *Okashita*, 5:41-49, 55-63. Regarding the switch apparatus of Figs. 19-20, *Okashita* explains that “series MOS transistor 1’ ... is connected in series to the series **MOS transistor 1 of FIG. 7.**” *Okashita*, 8:30-37⁴. Fig. 9 presents the cross-sectional view of *Okashita*’s apparatus of Fig. 7. *Okashita*, 2:19-21, 5:36-40. In my opinion, A POSITA would have recognized that the **MOS transistor 1’**, which is connected in series to the **MOS transistor 1** in Figure 7, would have also

⁴ Throughout this declaration, all emphases are added unless otherwise indicated.

been fabricated in exactly the same way as the MOS transistor 1.

Fig. 9



Okashita, Fig. 9.

153. A POSITA would have recognized that the MOS transistor 1 would have also been fabricated in the silicon layer 23. In its claim 3, *Okashita* discloses that its apparatus includes “a plurality of series MOS transistors formed within a first region of [a] semiconductor layer [formed on an insulating layer over a semiconductor substrate] and connected in series.” *Okashita*, 10:43-57. As explained *supra* §XI.A.1.b, based on the structure of the substrate outlined in the claims and detailed in the description and illustrated in the figures, a POSITA would have understood that the terms “semiconductor substrate,” “insulating layer,” and “semiconductor layer” in *Okashita*’s claims correspond to the silicon substrate 21, silicon oxide layer 22, and p-type silicon layer 23, respectively, as

described in the written description and figures. Additionally, *Okashita* describes MOS transistors 1 and 1' as “series MOS transistors.” *Okashita*, 8:30-37.

154. Moreover, it would have been obvious that both of *Okashita*'s MOS transistors 1 and 1' would have been fabricated with the SOI configuration of Figure 7. *Okashita*, Abstract, 1:47-58, 5:41-44, 6:1. In *Okashita*, the substrate on which transistors 1 and 1' are formed have a silicon-on-insulator (SOI) configuration. *Okashita*, Abstract, 1:47-58, 5:41-44, 6:1. Based on common knowledge in the art, a POSITA would have known that transistors in an SOI substrate are formed on the silicon layer 23 over the buried silicon oxide layer 22 (or BOX). See Ex. 1010, 36-38; Ex. 1016, 1 (“As the name implies, SOI fabricates circuits on a thin layer of silicon on top of an insulator.”); Ex. 1017, 1 (“The term SOI means Silicon On Insulator structure, which consists of devices on silicon thin film (SOI layers) that exists on insulating film.”). Since *Okashita* teaches the fabrication of the MOS transistor 1 in a silicon layer 23, a POSITA would have had a reasonable expectation of success in fabricating the MOS transistor 1' also in a silicon layer 23.

155. Moreover, in my opinion, it would have been obvious that both MOS transistors 1' and MOS transistor 1 will have a similar geometry—with an intervening silicon layer separating their source/drain junctions from the top

surface of the **silicon oxide layer** (as shown in Figure 9)—for at least the following three reasons.

156. First, in my opinion, a POSITA would have been motivated to maintain a consistent geometry for the adjacently located **MOS transistors 1, 1'** (see *Okashita*, Fig. 20) because doing so would simplify the manufacturing process by enabling the same processes (such as doping, etching, and metal deposition) to be used to fabricate both transistors at the same time. *See* Ex. 1011, 12-17. Moreover, a POSITA would have been motivated to ensure uniform device geometry for the **MOS transistors 1, 1'** to enable the use of the same “design methodology,” “device models,” and “design kits” during their design and fabrication, and thus, significantly reduce manufacturing and integration complexity as well as costs. '886 patent, 3:24-35; 1:43-47.

157. Second, having consistent geometry ensures similar electrical characteristics (such as threshold voltage, junction capacitance, gate delay time, etc.) between the transistors. *See* Ex. 1013, 25-29; Ex. 1014, 2-5. In my opinion, a POSITA would have been motivated to keep consistent geometry for both **MOS transistors 1, 1'** to ensure that both transistors would have similar electrical characteristics. Otherwise, there may be uneven threshold voltages between the two **MOS transistors 1', 1** due to a lack of uniformity in their geometries. *See* Ex. 1013, 29 (“SOI MOSFET’s are typically designed to have higher threshold voltage

than their bulk counterparts.”). Such variations in threshold voltages (V_{Th}) would cause discrepancies in the switching behavior of the MOS transistors 1 and 1' during the operation of the switch apparatus. *See* Ex. 1013, 29 (“ V_T variation has been shown to cause 5-6% frequency-dependent delay variation in simple circuits[.]”). To avoid this, a POSITA would have been motivated to keep consistent geometry between the transistors to ensure similar electrical characteristics.

158. Third, in my opinion, having consistent geometry also ensures similar thermal characteristics (such as operating temperature, thermal resistance, etc.) between the transistors. In general, the silicon dioxide used in the buried oxide layer generally has lower thermal conductivity compared to silicon in the bulk silicon layer. Ex. 1013, 27 (explaining that the self-heating in SOI poses a design challenge due to silicon dioxide's thermal conductivity being about 100 times lower than silicon's); Ex. 1022, 1 (explaining that the buried silicon dioxide results in a large thermal resistance between the device and the substrate causing a major problem for SOI transistors). This reduction in thermal conductivity increases localized temperature, which further impacts circuit performance and reliability. Ex. 1010, 60; Ex. 1013, 28 (explaining that channel temperature rise in SOI devices can be up to ten times higher than in bulk silicon devices). Thus, uneven geometry would cause the MOS transistors 1, 1' to operate at different

temperatures. To avoid this, a POSITA would have been motivated to keep consistent geometry between the transistors to ensure similar thermal characteristics.

159. Accordingly, in my opinion, a POSITA would have recognized that differences in electrical and thermal characteristics between the serially connected MOS transistors 1, 1' could cause signal delays and other errors, thereby motivating the POSITA to maintain consistent geometry for the two MOS transistors 1, 1'. Ex. 1010, 75 ("two devices [] have different electrical properties due to the devices being at different temperatures"), *see also id.* 34, 52-53, 59-60, 140, 155-156. Moreover, fabricating the MOS transistor 1' with the same geometry as the MOS transistor 1 to have the intervening silicon layer would yield entirely predictable results for a POSITA. A POSITA would have thus had a reasonable expectation of success in doing so.

160. Therefore, it would have been obvious that the source/drain junction of the MOS transistor 1' would have been also fabricated in exactly the same way as the MOS transistor 1 so as not to contact the silicon oxide layer. Accordingly, it would have been obvious that Okashita's MOS transistors 1 and 1' are fabricated in a silicon layer situated over a silicon oxide layer and a monocrystalline silicon substrate.

- c. **[1b(i)]: “each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer,”**

161. *Okashita* teaches this limitation. As I explained in [1b(i)] of Ground 1, *Okashita*’s MOS transistor 1’s source/drain junction does not contact the silicon oxide layer 22.

162. Moreover, in my opinion, it would have been obvious that the MOS transistor 1’, which is connected in series with the earlier MOS transistor 1, would also have a source/drain junction that does not contact the silicon oxide layer, as explained in [1(a)]. *Okashita*, Fig. 9; see also *Okashita*, Fig. 20.

- d. **[1b(ii)]: “thereby forming a source/drain junction capacitance;”**

163. *Okashita* teaches this limitation. For the same reasons I discussed earlier that the structure of *Okashita* in ground 1 forms a source/drain junction capacitance, *supra* §XI.A.1.d, the corresponding structure in this ground, namely source/drain junctions of the MOS transistors, 1, 1’ with the intervening silicon layer, also forms a source/drain junction capacitance.

- e. **[1c(i)]: “at least one trench extending through said device layer and contacting a top surface of said buried oxide layer,”**

164. *Okashita* teaches this limitation for the same reasons as stated in ground 1.

- f. **[1c(ii)]: “thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.”**

165. *Okashita* teaches this limitation for the same reasons as stated in ground 1.

2. Claim 2

- a. **[2]: “The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer.”**

166. *Okashita* teaches the additional limitation of claim 2 for the same reasons as stated in ground 1 for claim 2. *See supra* §§XI.A.2.a, XI.A.1.e-XI.A.1.f-XI.B.1.e-XI.B.1.f. The MOS transistor 1 of the cascaded pair of MOS transistors 1, 1' is situated within an isolated island in the silicon layer. *Okashita*, 8:30-37, 47-54, Figs. 9, 19-20.

3. Claim 3

- a. **[3]: “The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.”**

167. *Okashita* teaches the additional limitation of claim 3. For example, *Okashita* teaches (1) a plurality of MOS transistors “connected in series” and “formed within a first region of” the silicon layer and (2) a trench that surrounds the plurality of MOS transistors connected in series. *Okashita*, 10:43-67; *supra* §§XI.B.1.e-XI.B.1.f, XI.B.1.b. In my opinion, a POSITA reading *Okashita* would

have understood that **trench T1** surrounding the plurality of **MOS transistors 1, 1'** effectively places these **MOS transistors** within an isolated “first region” in the **silicon layer** to minimize radio frequency signal leakage from, and to, the first region. *See Okashita*, 6:1-17, 8:47-54, 9:21-25; *supra* §§XI.B.1.e-XI.B.1.f.

168. To the extent Patent Owner contends otherwise, a POSITA would have recognized that situating both **MOS transistors 1, 1'** within the same isolated region, as *Okashita* teaches, ensures consistent performance characteristics among the transistors. Ex. 1010, 75; Ex. 1020, 3:22-59, 1:47-63, Figs. 1-2B (A pair of SOI transistors are formed within an isolated island, which is surrounded by an isolation trench, to ensure consistent switching rates for both transistors). In my opinion, a POSITA would have known that locating multiple transistors in an isolated region provides at least two benefits: better tracking of thermal temperature and consistent switching rate. Ex. 1010, 75; Ex. 1020, 3:22-59, 1:47-63, Figs. 1-2B. Moreover, as I explained, it was well known in the art to situate multiple transistors in the same isolated region surrounded by an insulating trench to ensure that these transistors have consistent performance characteristics. *Supra* §VI.D. Thus, in my opinion, a POSITA would have been motivated to situate the **MOS transistor 1'** within the same isolated island with the **MOS transistor 1** to ensure consistent electrical performance and reliability. *See* Ex. 1010, 75-77; Ex. 1020, 3:22-59, 1:47-63, Figs. 1-2B. And a POSITA would have had a reasonable

expectation of success in doing so. Such an approach was standard practice in the field and would have been no more than applying a known technique to a known device to produce predictable results.

4. Claim 4

- a. **[4]: “The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is an NFET with a gate driven by a switch control signal in a wireless communications device.”**

169. *Okashita* teaches the additional limitation of claim 4 for the same reasons as stated in ground 1 for claim 4. *See supra* §XI.A.3.a.

5. Claim 5

- a. **[5]: “The switching circuit of claim 4, wherein said switch control signal drives said gate of said NFET through at least one resistor.”**

170. *Okashita* teaches the additional limitation of claim 5 for the same reasons as stated in ground 1 for claim 5. *See supra* §XI.A.3.a, XI.A.4.a, XI.B.4.a.

6. Claim 6

- a. **[6]: “The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is a PFET with a gate driven by a switch control signal in a wireless communications device.”**

171. *Okashita* teaches the additional limitation of claim 6. In my opinion, although MOS transistor 1 (of in Figure 19) is an NFET, *supra* XI.A.3.a, it would have been obvious to a POSITA to implement the MOS transistor 1 as a PFET instead.

172. *Okashita* teaches using both “p-channel MOS transistors” and “N-channel MOS transistors.” *Okashita*, 7:30-33, Fig. 16. In my opinion, it would have also been obvious to substitute the NFET with a PFET because there are two basic types of field-effect transistor (FET) (e.g., PFET and NFET). Ex. 1008, 20 (explaining that there two types of MOSFETS—n-channel MOSFETS and p-channel MOSFETS); Ex. 1012, 2 (PFET “starts with an n-type substrate...into which p-type source and drain regions are implanted on either side of a gate structure.”); Ex. 1010, 70 (“pMOS is very similar [to nMOS], except for the diffusions being of opposite type.”). Indeed, the ’886 patent itself acknowledges that in a conventional switching circuit, the transistors can be NFETs or PFETs. ’886 patent, 3:13-15.

173. Moreover, in my opinion, a POSITA would have been motivated to substitute the NFET with a PFET to enable the use of the switch apparatus in noise-sensitive applications. It was well-established that PFETs (or PMOS transistors) generate less noise compared to NFETs (or NMOS transistors). Ex. 1018, 4 (pMOS devices exhibit lower noise magnitude compared to nMOS devices), 3 (a noise spectral density two orders of magnitude lower was observed in pMOS compared to nMOS). Therefore, a POSITA would have been motivated to implement the MOS transistor 1 as a PFET in a switch apparatus that is intended for noise-sensitive devices. *See Okashita* 1:11-15.

174. When a PFET is used in *Okashita*'s switch apparatus, the transistor gate would continue to be driven by the switch control signal. Ex. 1012, 2 (A "PFET operates when the voltage of the gate is lowered relative to that of the source or drain region."). Thus, it would have been well within the skill of a POSITA to substitute a PFET in *Okashita*'s switch apparatus in place of an NFET, a POSITA would have had a reasonable expectation of success in doing so, and the results of the substitution would have been predictable. Ex. 1011, 9; *Burgener*, ¶[0079].

7. Claim 7

- a. [7]: "The switching circuit of claim 6, wherein said switch control signal drives said gate of said PFET through at least one resistor."

175. *Okashita* teaches the additional limitation of claim 7. *Okashita*'s MOS transistor 1, as modified to use a PFET, would have been driven by the switch control signal through a gate protection resistor for the same reasons as stated in ground 1 for claim 5. *Supra* §§XI.A.4.a, XI.B.5.a, XI.B.6.a; *Okashita*, 4:17-21.

C. Ground 3: Claims 1-7 Are Obvious Over *Okashita* and *Yu*

1. Combining *Okashita* and *Yu*

176. *Okashita* and *Yu* are similar. *See supra* §§VIII.A, VIII.B. Both devices have transistors that are fabricated on an SOI structure. *Okashita*, 1:47-58, 5:41-46, Fig. 9; *Yu*, 3:53-4:3, Fig. 3. The transistors in *Okashita* and *Yu* are also both "cascaded," (*Okashita*, 8:30-34; *Yu*, 5:44-57), and are situated within an

isolated island that is surrounded by a **shallow trench isolation (STI) region 36**.

Okashita, 6:50-51; *Yu*, 4:8-10, Fig. 10.

177. In *Yu*, “OD region 200 [of Figure 12] represents the active device area. The **shallow trench isolation (STI) regions** are formed in the area outside of the OD box 200.” *Yu*, 6:55-60. And “the STI regions are formed down to the buried insulator layer such that each active area is completely isolated from other active areas.” *Yu*, 1:67-2:3 As explained *supra* §VIII.B, *Yu* teaches that it is important not only to form the **STI 36 regions** in the silicon layer 34 of the SOI to define an active area, but to keep the **STI regions** outside of the active area of the planned LVT-SCR contrary to prior art processes. *Yu*, 4:8-15. *Yu*’s **STI regions** “do not extend into the LVT-SCR device nor do they separate the first or second type doped regions [formed in silicon layer 42, 44].” *Yu*, 5:16-19.

178. In my opinion, a POSITA would have found it obvious to fabricate *Okashita*’s transistors using an SOI process, as *Yu* teaches, so the transistors would have been within the active area that is surrounded by a trench isolation region. In my opinion, a POSITA would have been motivated to ensure that *Okashita*’s trench isolation regions are not formed within the active area and to maintain a sufficient thickness in the silicon layer so that the transistors’ **source/drain** interfaces do not extend to the **silicon oxide layer**, as taught by *Yu* (*supra* §VIII.B), because doing so would have achieved similar thermal and electrical benefits as

described by *Yu* in *Okashita*'s switching device. *See Yu*, 2:4-17. For example, *Yu* discloses "problems [with] SCR devices formed in an SOI process having STI isolation. First, the presence of the STI regions within the SCR and LVT-SCR devices reduces the lateral heat transfer property during an ESD event. Consequently, the devices fail at a lower energy dissipation level." *Yu*, 2:4-9; *see also Yu*, 2:10-17.

179. Indeed, a POSITA would have recognized that, due to the lower thermal conductivity of silicon dioxide compared to silicon, if the source/drain junctions of *Okashita*'s cascaded transistors were to contact the silicon oxide layer, the transistors would operate at higher temperatures, which could then negatively impact circuit performance and "fail at a lower energy dissipation level" as taught by *Yu*. *Yu*, 2:4-17; *see also* Ex. 1010, 59-60; Ex. 1013, 27-28; *see* Ex. 1022, 1 (explaining that lateral heat conduction can reduce strongly reduce the temperature rise in active regions).

180. Since both *Okashita* and *Yu* disclose a switching circuit with cascaded transistors that are formed in an isolated island that is surrounded by a trench, a POSITA would have had a reasonable expectation of success in fabricating *Okashita*'s transistors based on *Yu*'s SOI process. For example, due to their commonalities between *Okashita* and *Yu*, a POSITA would have recognized that

applying *Yu*'s teaching to *Okashita* would have been a straightforward use of a known technique to enhance *Okashita*'s similar device in the same manner.

2. Independent Claim 1

a. [1pre]: "A switching circuit comprising:"

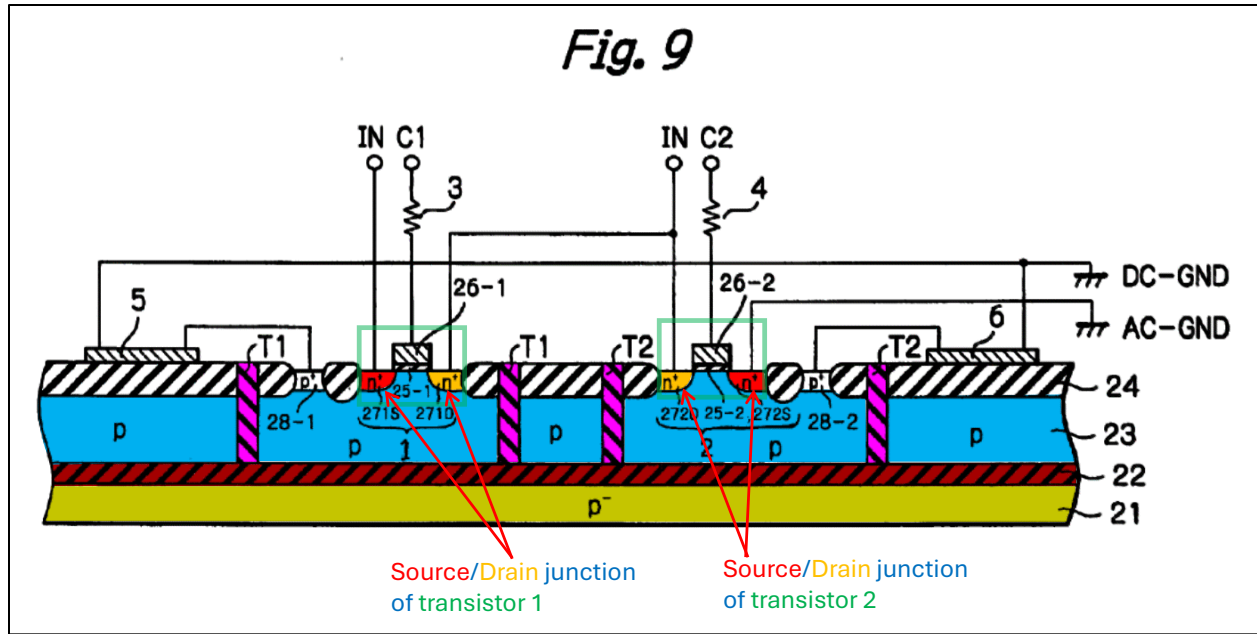
181. To the extent the preamble is limiting, *Okashita* discloses it for the same reasons as stated in claim [1pre] for grounds 1 and 2. *Supra* §§XI.A.1.a, XI.B.1.a.

b. [1a]: "a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;"

182. *Okashita* teaches this limitation for the same reasons as stated in claim [1a] for ground 2. *Supra* §XI.B.1.b.

c. [1b(i)]: "each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer,"

183. *Okashita* in view of *Yu* teaches this limitation. As previously discussed, it would have been obvious to a POSITA that the source/drain junction of *Okashita*'s MOS transistors 1, 1' are spaced apart from the top surface of the buried oxide layer 22 for the same reasons as stated in ground 2 for claim [1b(i)]. *Supra* §XI.B.1.c;



Okashita, Fig. 9.

184. To the extent Patent Owner contends that *Okashita* does not explicitly mention this feature, in my opinion, it would have been obvious in view of *Okashita* and *Yu*. Based on the teachings of *Yu*, a POSITA would have been motivated to ensure that a sufficiently thick **silicon layer 23** remains between the **source/drain** junctions of *Okashita*'s **transistors 1 and 1'** and the top surface of the **silicon oxide layer 22**, as *Yu* teaches, to achieve similar thermal and electrical benefits as taught by *Yu*. *Supra* §§VIII.B, XI.C.1; *Yu*, 2:4-17.

d. [1b(ii)]: “thereby forming a source/drain junction capacitance;”

185. *Okashita* in view of *Yu* teaches this limitation. For the same reasons that the structure of *Okashita* in ground 1 forms a source/drain junction capacitance, the corresponding structure in this ground, namely **source/drain**

junctions of MOS transistors, 1, 1' separated from the silicon oxide layer by the silicon layer, as *Yu* teaches, also forms a source/drain junction capacitance. *Supra* §§XI.A.1.d, XI.B.1.d.

- e. **[1c(i)]: “at least one trench extending through said device layer and contacting a top surface of said buried oxide layer,”**

186. *Okashita* teaches this limitation for the same reasons as stated in grounds 1 and 2. *Supra* §§XI.A.1.e, XI.B.1.e;

- f. **[1c(ii)]: “thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.”**

187. *Okashita* teaches this limitation for the same reasons as stated in grounds 1 and 2. *Supra* §§XI.A.1.f, XI.B.1.f;

3. Claims 2

- a. **[2]: “The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer.”**

188. *Okashita* teaches the additional limitation of claim 2 for the same reasons as stated in grounds 1 and 2 for claim 2. *Supra* §§XI.A.2.a, XI.B.2.a.

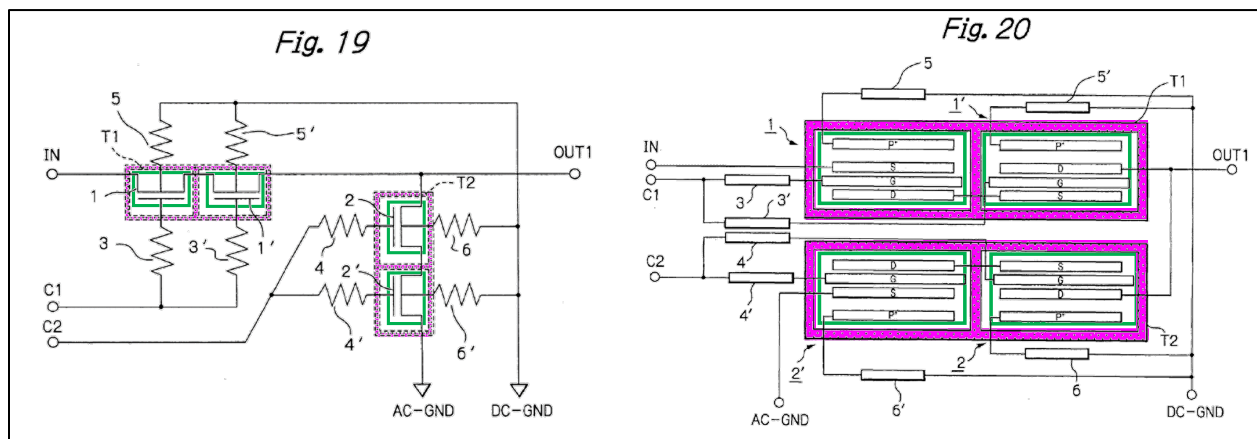
4. Claim 3

- a. **“The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.”**

189. In my opinion, *Okashita* in view of *Yu* teaches the additional limitation of claim 3 for the same reasons as stated in ground 2 for claim 3.

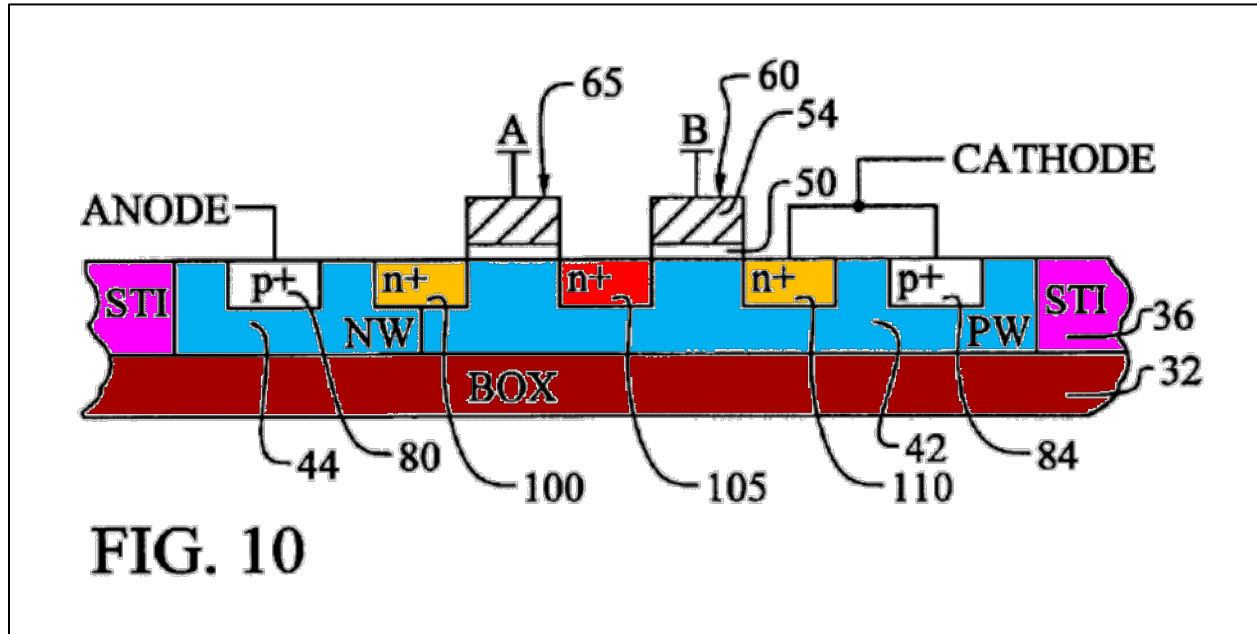
Okashita, 10:49-67. To the extent Patent Owner disputes this, a POSITA would have been motivated to situate the MOS transistor 1' on the same isolated island as the MOS transistor 1, as *Yu* teaches.

190. *Okashita* discloses “each of the MOS transistors 1, 1', 2 and 2' is isolated by the trench insulating layers T1 and T2, so that the leakage of radio frequency signals from the silicon layer 23 of the MOS transistor 1 to that of the MOS transistor 1' ... can be sufficiently suppressed.” *Okashita*, 8:47-54.



Okashita, Figs. 19-20.

191. In my opinion, it would have been obvious to place both of *Okashita's* cascaded MOS transistors 1, 1' within the same isolated island to ensure consistent performance characteristics of these two transistors. *Yu* discloses two cascaded transistors situated in the same isolated island surrounded by trenches.



Yu, Fig. 10.

192. For example, in *Yu*, the first and second transistors are cascaded and located in an isolated island that is surrounded by STI regions. *Supra* §§VIII.B, XI.C.1; *Yu*, 5:44-55, 6:46-60. Specifically, in *Yu*, “the STI regions are formed down to the buried insulator layer such that each active area is completely isolated from other active areas.” *Yu*, 1:67-2:3, 6:55-60. Importantly, these STI regions “do not extend into the LVT-SCR device nor do they separate the first or second type doped regions [formed in silicon layer 42, 44].” *Yu*, 5:16-19.

193. As I explained with reference to claims [1b(i)] and [3] of ground 2, a POSITA would have recognized that *Okashita*'s MOS transistors 1' will have a different electrical performance and reliability than the MOS transistor 1 if they operate at different temperatures. *See* Ex. 1010, 75; *supra* §§XI.B.1.c, XI.B.3.a. For example, *Yu* discloses that devices with STI isolation experience reduced lateral heat transfer during an ESD event that may cause the device to "fail at a lower energy dissipation level," and result in changes in its performance characteristics. *Yu*, 2:7-13. Moreover, as I explained *supra* §§VI.D, XI.B.1.c, XI.B.3.a, it was well understood that placing multiple transistors within the same isolated region surrounded by a trench reduces temperature differences and performance variations between the transistors. It was also well known that reduced heat transfer increases device temperatures which negatively affects device performance. *See* Ex. 1010, 75-78. In my opinion, a POSITA, therefore, would have been motivated to situate both MOS transistors 1, 1' in the same isolated island, as *Yu* teaches, so they both have consistent temperatures and electrical properties.

194. Since both *Okashita* and *Yu* teach switching circuits with cascaded transistors in an SOI configuration with trench isolation, a POSITA would have had a reasonable expectation of success in incorporating this teaching of *Yu* in *Okashita*.

5. Claim 4-7

195. *Okashita* teaches the additional limitations of claim 4-7 for the same reasons as stated in claims 4-7 of grounds 1 and 2.

Claim	Corresponding Claim
Claim 4	<i>Supra</i> §§XI.A.3.a, XI.B.4.a,
Claim 5	<i>Supra</i> §§XI.A.4.a, XI.B.5.a
Claim 6	<i>Supra</i> §§XI.B.6.a
Claim 7	<i>Supra</i> §§XI.B.7.a

D. Ground 4: Claims 1, 2, and 3 Are Anticipated by *Yu*

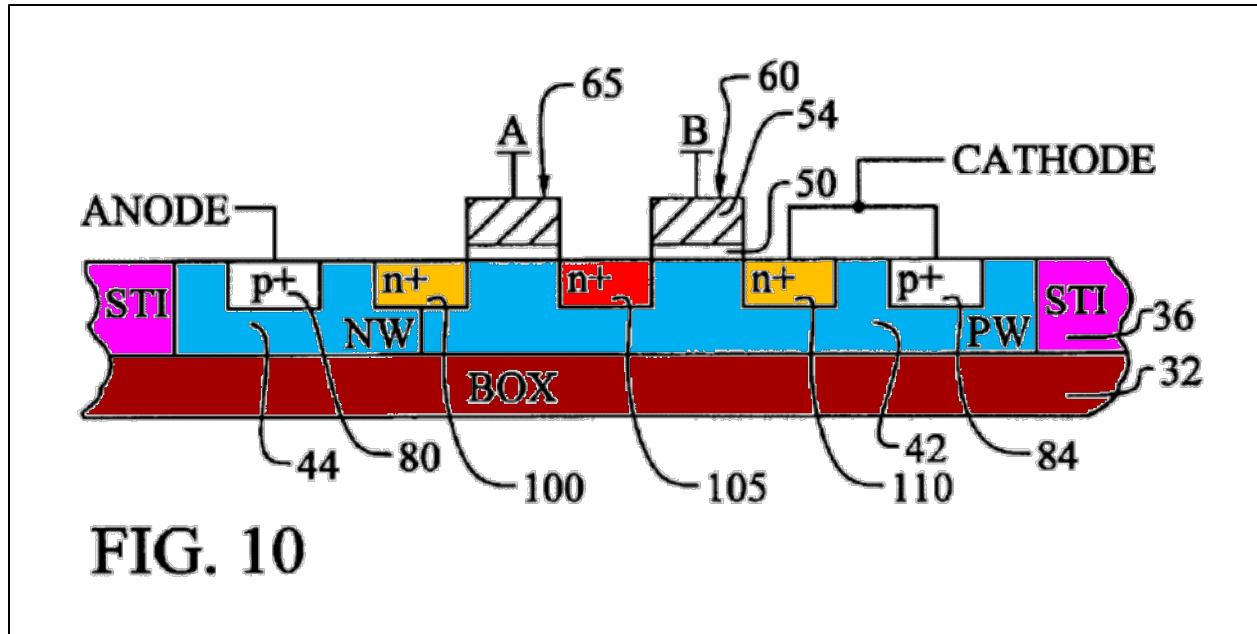
1. Independent Claim 1

a. [1pre]: “A switching circuit comprising:”

196. To the extent the preamble is limiting, *Yu* discloses an LVT-SCR, which is a switching circuit. *Yu*, 1:10-13, 3:53-62, 6:4-11; Ex. 1011, 18; *supra* §VIII.B.

b. [1a]: “a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;”

197. *Yu* discloses this limitation. *Yu*’s LVT-SCR includes two MOS transistors that are connected “in series” and, therefore, are “cascaded, or stacked.” *Yu*, 5:44-57. *Yu*’s cascaded transistors are also fabricated in a **silicon layer** that is situated over a **buried oxide layer 32**, as shown below. *Yu*, 5:58-66.



Yu, Fig. 10

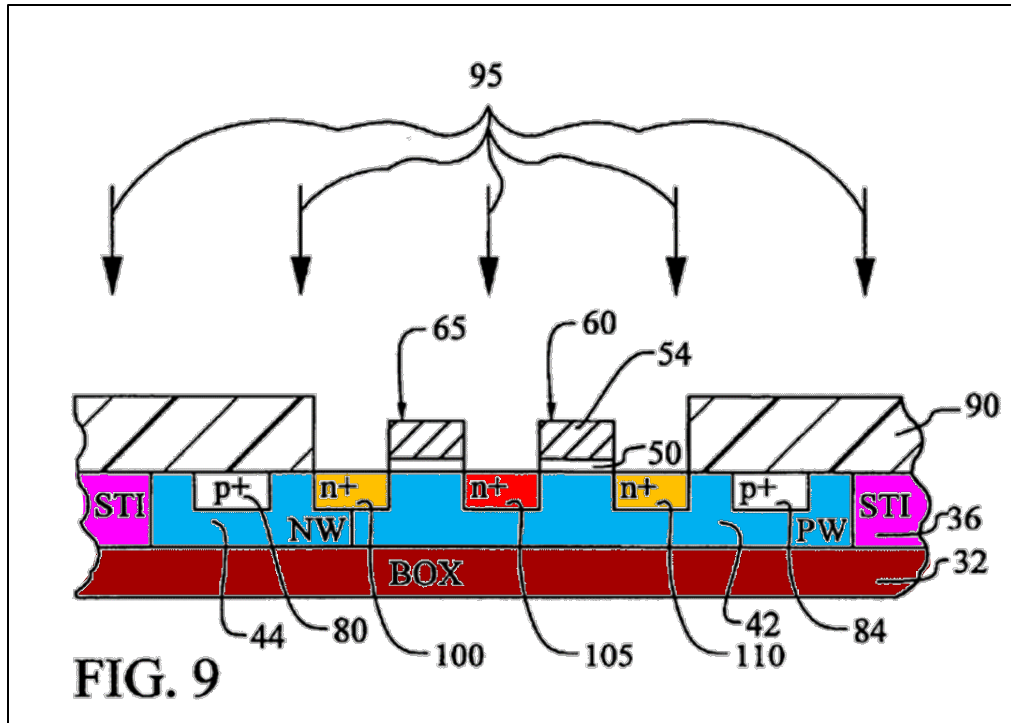
198. Yu's SOI system consists of a **buried oxide layer 32** positioned above a **substrate 30** (see Yu, Fig. 3) with a **silicon layer 34** formed on top of the **buried oxide layer 32**. Yu, 5:58-66. "Two MOS transistors are formed by the gates 60 and 65. In particular, a **first NMOS transistor** is formed by first gate 60, third doped region 110, and fourth doped region 105. A **second MOS transistor** is formed by second gate 65, fourth doped region 105, and fifth doped region 100. The **first and second transistors** are in series between the third doped region 110 and the fifth doped region 100. Therefore, **the first and second NMOS transistors** are cascaded, or stacked, between the cathode terminal and the second well 44." Yu, 5:44-57.

199. In Yu, **STI regions** define the "active area regions of **silicon layer 34** where active devices may be subsequently formed." Yu, 4:8-12, 6:55-60.

Accordingly, the **silicon layer** (e.g., the active area where the cascaded **first and second NMOS transistors** are formed) is the claimed device layer. While the bulk semiconductor substrate layer is not shown in Figure 10 for “simplicity,” *Yu*’s LVT-SCR device is formed on an SOI system where the **buried oxide layer** “is either grown or deposited over a **bulk silicon substrate**.” *Yu*, 3:44-47, 53-62, 4:5-7, Fig. 3. Accordingly, Accordingly, the plurality of the cascaded transistors are fabricated in a device layer situated over a BOX layer and a bulk semiconductor layer.

- c. **[1b(i)]: “each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer,”**

200. *Yu* discloses this limitation. As *Yu* explains, each of the transistors includes doped regions that form the **source** and **drain** of the transistors, as shown below.



Yu, Fig. 9.

201. In *Yu*, a first p-type well 42 and a second n-type well 44 is formed on silicon layer 34 by ion implantation, and n⁺ doped regions 100, 105, and 110 are formed in these wells 42, 44 on the silicon layer 42. *Yu*, 4:17-24, 5:4-11. In my opinion, a POSITA would have recognized that the first NMOS transistor 60 includes an n⁺ doped region 105 as its source and an n⁺ doped region 110 as its drain. *Yu*, 5:44-57; see also *Yu*, 4:17-24, 5:4-11. The second MOS transistor 65 shares the n⁺ doped region 105 as its source and has an n⁺ doped region 100 as its drain. *Yu*, 5:44-57; see also *Yu*, 4:17-24, 5:4-11. In my opinion, a POSITA would have also recognized that the interfaces between these doped regions and the silicon layer 34 form the source/drain junctions for the respective transistors. See

Yu, 6:40-45, Fig. 11; *see, also* Ex. 1011, 10 (“pn junctions [] are formed by the drain-bulk and source-bulk interfaces in a MOSFET”), 11 (see Fig. 1.36); Ex. 1009, 4; Ex. 1010, 35-39. Importantly, the **source/drain** junction for each of the cascaded first and second NMOS transistors 60, 65 does not extend to the **buried oxide layer 32**. *Yu*, 6:46-54, Fig. 10 (showing a “thick” **silicon layer 34** between the **source/drain** junctions of the transistors and the **buried oxide layer 32**).

202. Moreover, *Yu* expressly states that an “**important feature** of the present invention is ... [that] [t]he doped regions 80, 84, **100**, **105**, and **110**, are formed in the upper part of the wells 42 and 44 and **do not extend to the buried oxide layer 32**. That is, the original silicon layer in which the doped regions are formed is thick enough so that the doped regions do not completely deplete the wells 42 and 44.” *Yu*, 6:46-54, Fig. 10. In my opinion, a POSITA would have known that, if the doped region **105** that forms the **source** and the doped regions **100** and **110** that form the **drains** of *Yu*’s first and second transistors 60, 65 do not extend to the **buried oxide layer 32**, then the **source/drain** junctions of these transistors do not contact the **buried oxide layer 32**. Instead, the **source/drain** junctions are formed within **silicon layer 34**.

d. [1b(ii)]: “thereby forming a source/drain junction capacitance;”

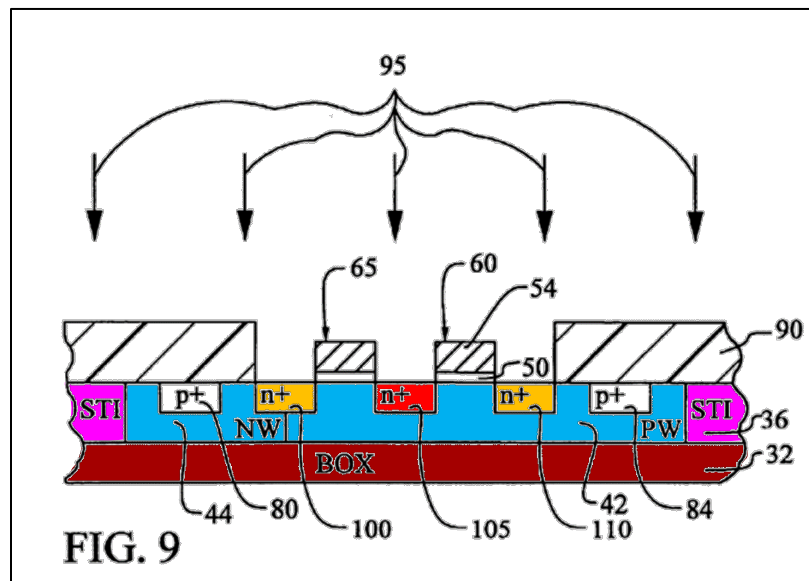
203. For the same reasons that the structure of *Okashita* in ground 1 forms a source/drain junction capacitance, the corresponding structure in this ground,

namely the source/drain junctions of transistors 60, 65 separated from the BOX layer by the “thick” silicon layer, also forms a source/drain junction capacitance.

Supra §XI.A.1.d; *Yu*, 6:46-54; *see also* Ex. 1013, 25-26; Ex. 1014, 2-5.

- e. [1c(i)]: “at least one trench extending through said device layer and contacting a top surface of said buried oxide layer,”

204. *Yu* discloses this limitation because *Yu*’s STI regions “are formed down to the buried insulator layer such that each active area is completely isolated from other active areas,” as shown below. *Yu*, Fig. 9; 1:67-2:3.



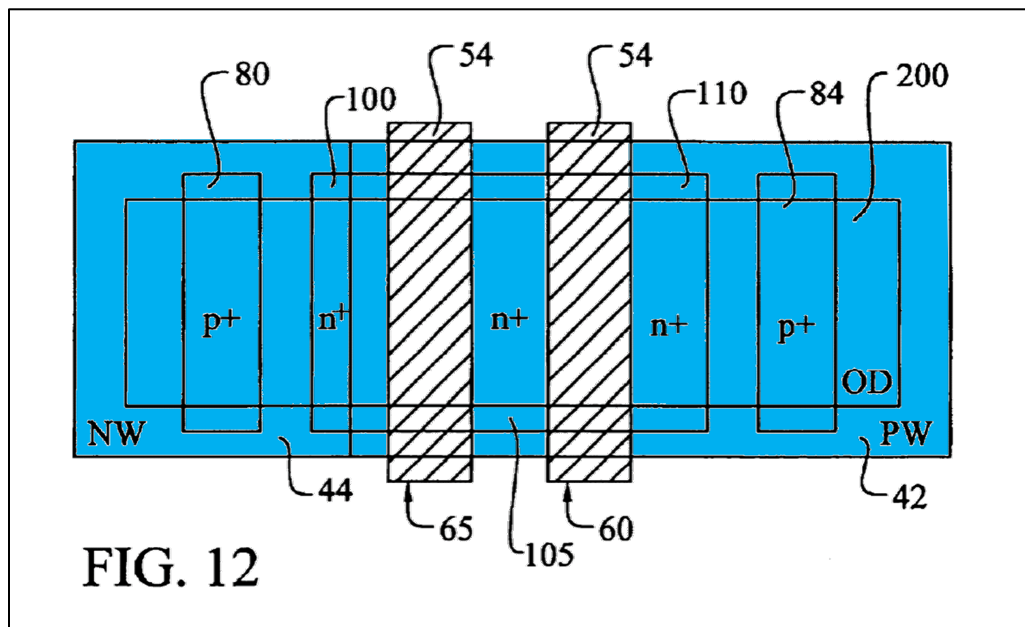
Yu, Fig. 9.

205. Accordingly, *Yu*’s STI region 36 extends through the silicon layer and contacts a top surface of the buried oxide layer 32.

- f. [1c(ii)]: “thereby electrically isolating at least one of said plurality of cascaded transistors in said switching

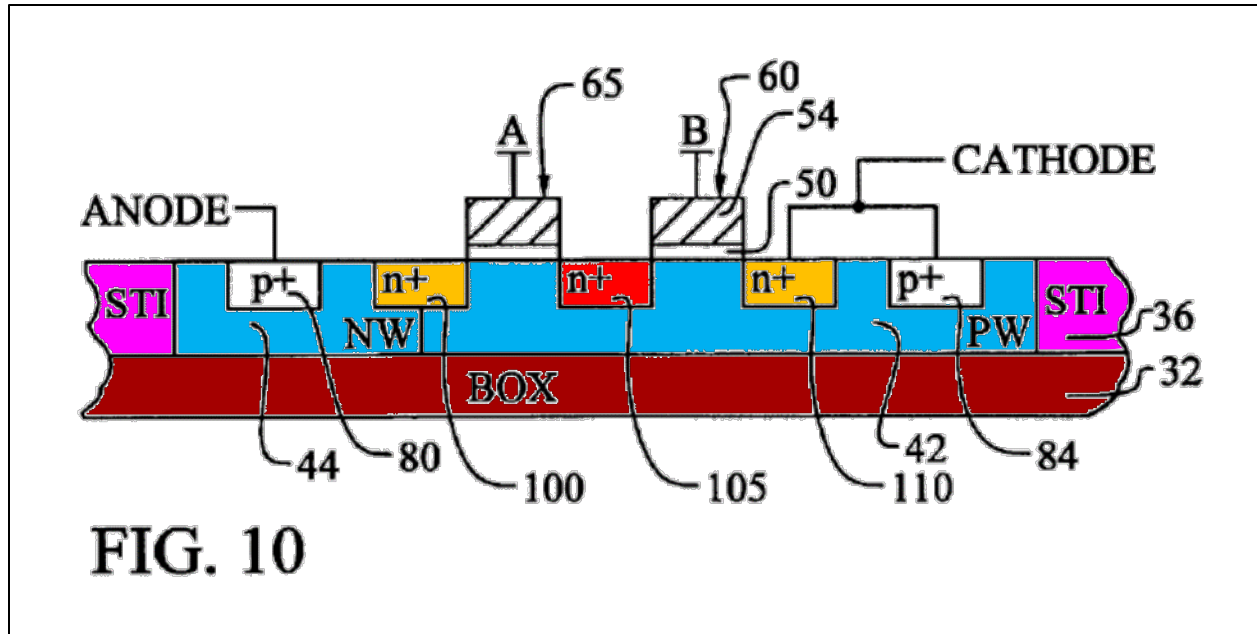
circuit so as to reduce voltage and current fluctuations in said device layer.”

206. *Yu* discloses this limitation. As explained *supra* §XI.D.1.e, *Yu*’s STI regions define an “active area region” (or “OD region”) where “active devices may be subsequently formed.” *Yu*, 4:8-15. As shown in Figure 12 below, “[t]he OD region 200 represents the active device area.” *Yu*, 6:55-60.



Yu, Fig. 12.

207. In Fig. 12, “OD region 200 represents the active device area.” While the STI regions are not shown in Figure 12, *Yu* explains that the STI regions are “formed in the area outside of the OD box 200,” (*Yu*, 6:55-60, 4:8-15), and, importantly, “do not extend into the LVT-SCR device nor do they separate the first or second type doped regions [formed in silicon layer 42, 44],” as shown below. *Yu*, 5:16-19.



Yu, Fig. 10.

208. *Yu* notes that, because the STI regions are formed down to the buried oxide layer 32, “each active area is completely isolated from other active areas,” thereby “reduc[ing] substrate coupling issues by providing excellent device-to-device isolation.” See *Yu*, 1:63-2:3. Therefore, the STI regions electrically isolate the first and second transistors from devices in other active areas. As explained previously with reference to claim [1c(ii)] of ground 1, as a result of this electrical isolation of the transistors, electrical signals from the silicon layer surrounding the first and second transistors will not leak and cause voltage and current fluctuations in the silicon layer of adjacent active areas. See also ’886 patent, 2:65-3:11, 6:10-15, 33-42. Accordingly, *Yu*’s STI regions will also reduce voltage and current fluctuations in the device layer.

2. Claim 2

- a. [2]: “The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer.”

209. *Yu* discloses this limitation. As explained above with reference to claims [1c(i)] and [1c(ii)], the first NMOS and second MOS transistors are formed in an active area of silicon layer that is surrounded by STI regions that extend through the silicon layer to the buried oxide layer 32, such that the active area is “completely isolated” from other active areas. *Yu*, 1:67-2:3, 4:8-15; *supra* §§XI.D.1.e-XI.D.1.f. In other words, the first NMOS and second MOS transistors are situated within an isolated island in the silicon layer that is defined by the walls of the surrounding STI region 36 and the top surface of the buried oxide layer 32.

3. Claim 3

- a. [3]: “The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.”

210. *Yu* discloses this limitation, because as explained above with reference to claim 2, both of the cascaded NMOS and MOS transistors are situated within the isolated island in the silicon layer. *Supra* §XI.D.2.a.

E. Ground 5: Claims 1-19 Are Obvious Over *Burgener* and *Okashita*

1. Combining *Burgener* with *Okashita*

211. Both *Okashita* and *Burgener* disclose a switching apparatus with multiple stacked FETs for a wireless device such as a cellular telephone. *Supra*

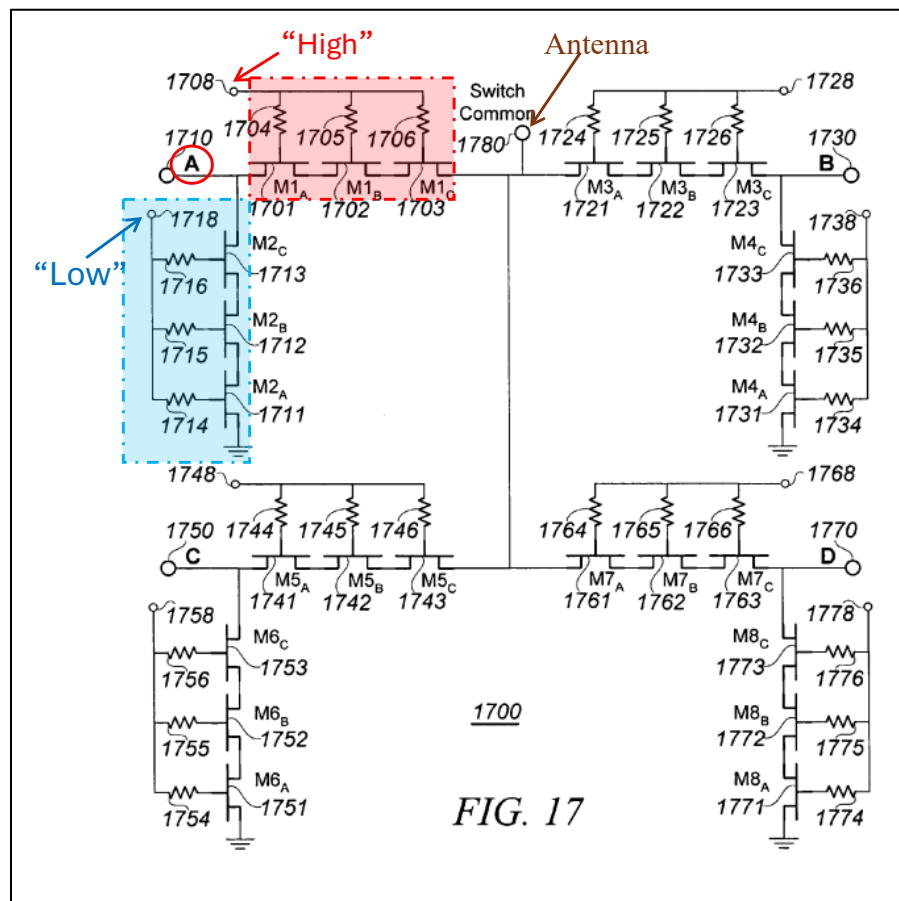
§§VIII.A, VIII.C. While *Burgener* does not expressly provide details related to the fabrication of its integrated circuit, *Burgener* explains that its integrated circuit may be fabricated using “semiconductor-on-insulator (SOI) techniques,” such as those taught by *Okashita*. *Burgener*, ¶[0105]; *Okashita*, 1:7-15, 5:41-43, Fig. 9.

212. As I explained with reference to claims [1pre]-[1b(ii)] of ground 2, *supra* §XI.B.1, *Okashita* discloses a “semiconductor switch apparatus” that includes cascaded MOS transistors 1, 1' having an SOI configuration with an intervening silicon layer between the transistors' source/drain junctions and the buried silicon oxide layer. *Okashita*, 1:7-15, 5:41-43, Fig. 12. Further, as I explained with reference to claims [1c(i)]-[1c(ii)] of ground 2, *Okashita*'s MOS transistors are isolated by a trench T1 that extends through the silicon layer to contact the silicon oxide layer to prevent leakage of radio frequency signals from these MOS transistors to other components of the switch apparatus. *Supra* §§XI.B.1.e-XI.B.1.f, XI.B.3.a.

213. In my opinion, it would have been obvious for a POSITA to fabricate *Burgener*'s integrated circuit (e.g., antenna switch 1700 and the corresponding cascaded FETs) with an intervening silicon layer and trenches, as *Okashita* teaches. In my opinion, a POSITA would have been motivated to combine *Burgener* and *Okashita* for at least the following three reasons.

214. First, a POSITA would have been motivated to fabricate *Burgener's* cascaded FETs with an intervening **silicon layer**, as *Okashita* teaches, such that the **source/drain** junctions of these FETs are separated from the **buried oxide layer** by the intervening **silicon layer**. In my opinion, as I explained with reference to claims [1b(i)]-[1b(ii)] of ground 2, a POSITA would have recognized that, because the buried oxide layer has lower thermal conductivity compared to the bulk silicon layer, conventional SOI transistors tend to operate at higher temperatures, which can adversely affect their performance and reliability. *See, e.g.*, Ex. 1010, 60; Ex. 1013, 26-28; *see supra* §XI.B.1.c. In my opinion, instead of using a conventional SOI structure, a POSITA would have been motivated to add an intervening **silicon layer** between the source/drain junction and the buried oxide layer, as *Okashita* discloses, because doing so would have reduced the operating temperature of the transistors and, thereby, enhance their performance and reliability. *See, e.g.*, Ex. 1010, 60; Ex. 1013, 27; *see supra* §XI.B.1.c. Accordingly, in my opinion, it would have been obvious for a POSITA to fabricate *Burgener's* cascaded FETs with an intervening silicon layer between the bottoms of the sources and the drains of the transistors and the top of the buried oxide layer, as *Okashita* teaches, to decrease the operating temperature of *Burgener's* transistors and improve their performance and reliability. *Supra* §§XI.B.1.c, XI.B.3.a.

215. Second, a POSITA would have been motivated to fabricate *Burgener's* cascaded SOI FETs that are electrically isolated by trenches, as *Okashita* teaches, to prevent leakage of radio frequency signals from the cascaded SOI FETs to other components of antenna switch 1700. As illustrated in below Figure 17, the gates of FETs $M1_A$ 1701, $M1_B$ 1702, $M1_C$ 1703 are connected to control node 1708 while the gates of FETs $M2_A$ 1711, $M2_B$ 1712, $M2_C$ 1713 are connected to control node 1718. To selectively connect port A 1710 to the antenna, a “high” voltage is applied to control node 1708, and a “low” voltage is applied to control node 1718. *Burgener*, ¶[0103]; *supra* §VIII.C.



Burgener, Fig. 17.

216. Because *Burgener*'s antenna switch 1700 selectively switches between different RF ports (A, B, C, D) by applying high and low control voltages to various cascaded FETs, a POSITA would have been motivated to place, for example, the cascaded FETs M1_A 1701, M1_B 1702, M1_C 1703 together in one isolated region surrounded by a trench and/or the cascaded FETs M2_A 1711, M2_B 1712, M2_C 1713 together in another isolated region surrounded by a second trench, as *Okashita* teaches, because doing so would have prevented the voltage applied to FETs 1701-1703 from leaking and causing voltage and current fluctuations in FETs 1711-1713, and vice versa. *supra* §VIII.C.

217. Third, as I explained previously with reference to claims [1b(i)] and [3] of ground 2, a POSITA would have been motivated to locate each set of FETs together in one isolated region that is surrounded by a trench, as *Okashita* teaches, to ensure that these FETs have consistent performance characteristics because doing so would also “minimize the effect of mismatch due to” the FETs having different electrical properties and being at different temperatures. *Supra* §§XI.B.1.c, XI.B.3.a; Ex. 1010, 75-78.

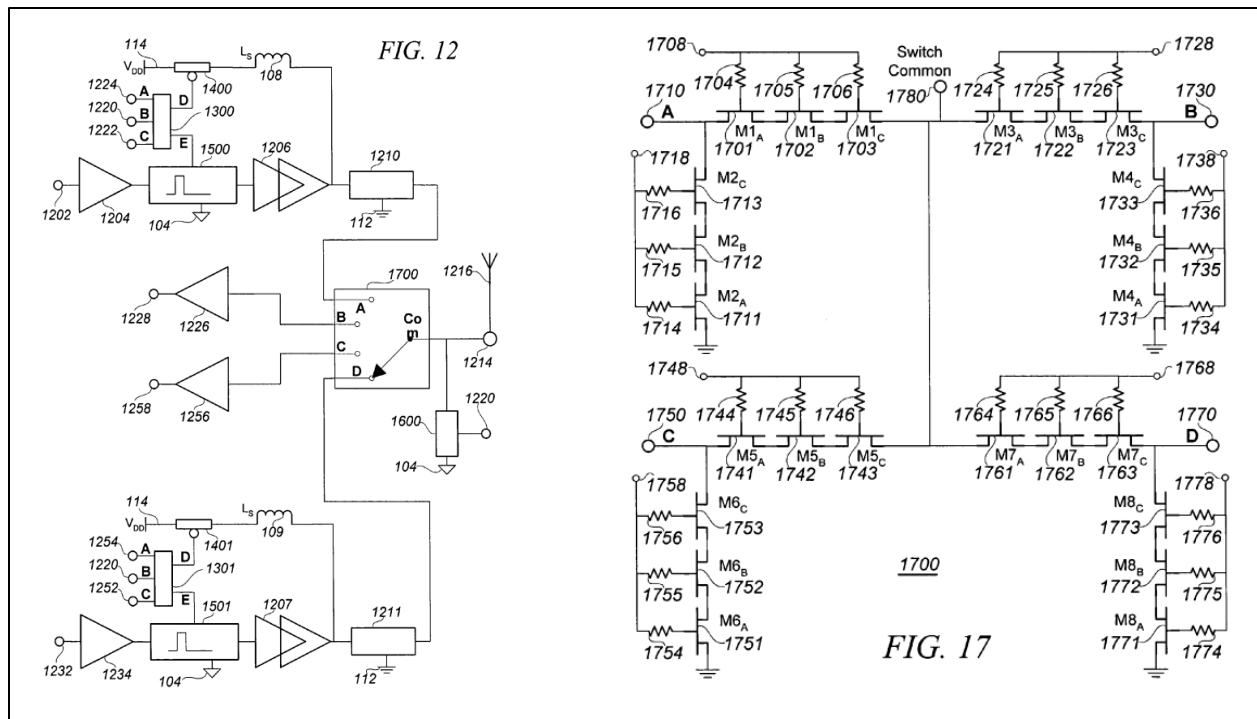
218. In my opinion, a POSITA would have reasonably expected success in fabricating *Burgener*'s integrated circuits using the SOI techniques that *Okashita* teaches because both references describe switching circuits that use cascaded

transistors in an SOI configuration. *See supra* §§VIII.A, VIII.C. In my opinion, a POSITA would have recognized that incorporating *Okashita*'s IC fabrication techniques to fabricate *Burgener*'s FETs would merely have been applying a known technique to a known device to yield predictable results. Moreover, as explained *supra*, both fabricating an SOI transistor with an intervening silicon layer between the source/drain and the buried oxide layer or situating multiple transistors within an isolated region of the SOI system were already well-established in the field. *See supra* §§VI.C-VI.D, XI.B.1.c, XI.B.1.f, XI.B.3.a; *see, e.g.*, Ex. 1010, 24-25; Ex. 1016, 1 Ex. 1013, 25-26; Ex. 1015, 1:22-28; Ex. 1020, 4:47-5:12. Accordingly, in my opinion, applying these teachings of *Okashita* to *Burgener* would have been a straightforward use of a known technique to improve a similar device in the same way.

2. Independent Claim 1

a. [1pre]: "A switching circuit comprising:"

219. To the extent the preamble is limiting, *Burgener* discloses this limitation because *Burgener*'s antenna switch 1700 is a switching circuit.



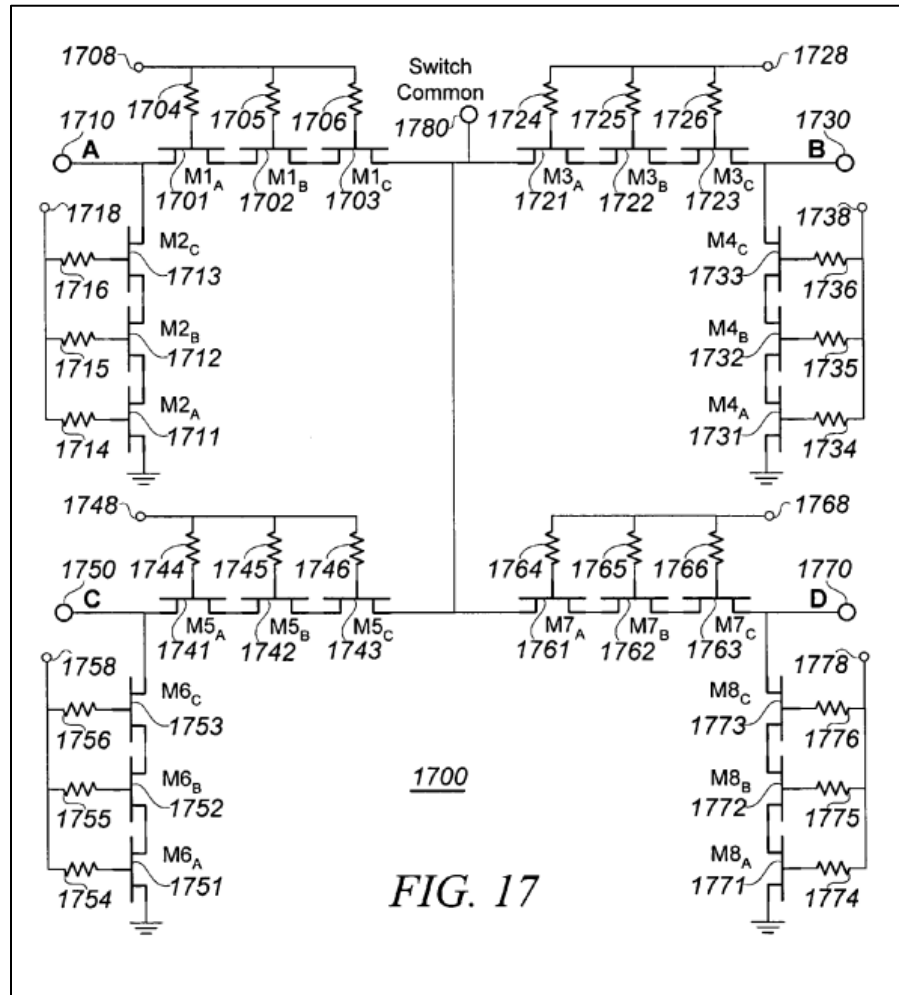
Burgener, Figs. 12, 17

220. *Burgener* discloses an integrated circuit (IC) with an antenna switch 1700 that includes “FET stacks (such as FETs 1701, 1702 and 1703) that provide the switching functions.” *Burgener*, ¶¶[0088], [0090]-[0094], [0104]; *supra* §VIII.C. Therefore, in my opinion, antenna switch 1700 is a switching circuit.

b. [1a]: “a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer;”

221. *Burgener* in view of *Okashita* teaches this limitation. *Burgener's* antenna switch 1700 includes “[s]tacks of multiple FETs in series to operate as a switching device.” *Burgener*, Abstract, Fig. 17. Moreover, a POSITA would have understood that *Burgener's* FETs are cascaded transistors because they are

connected in series. *Yu*, 5:53-55; '886 patent, 6:50-51 (acknowledging that transistors “coupled in series” are considered “cascaded”).



Burgener, Fig. 17

222. In *Burgener*, “[i]ntegrated circuit fabrication details are not provided.” *Burgener*, ¶[0105]. However, *Burgener* discloses that “semiconductor-on-insulator (SOI) techniques” may be used to fabricate them. *Burgener*, ¶[0105]. As explained in *supra* §XI.E.1, it would have been obvious for a POSITA to fabricate *Burgener*’s integrated circuit (e.g., antenna switch 1700 and the corresponding

cascaded FETs) using *Okashita*'s SOI configuration. In *Burgener*'s antenna switch as modified by *Okashita*, the plurality of cascaded transistors of the antenna switch 1700 would have been fabricated in *Okashita*'s silicon layer 23 that is situated over silicon oxide layer 22 and the silicon substrate 21 as described with reference to claim [1a] of ground 2. *Supra* §XI.B.1.b.

- c. [1b(i)-1b(ii)]: “each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;”

223. *Burgener* in view of *Okashita* teaches these limitations. In *Burgener*'s antenna switch 1700 as modified by *Okashita*, as described with reference to claims [1b(i)]-[1b(ii)] of grounds 1 and 2, each of the plurality of cascaded transistors have a source/drain junction that does not contact the silicon oxide layer 22, thereby forming a source/drain junction capacitance. *Supra* §§XI.B.1.c-XI.B.1.d, XI.E.1. As discussed *supra* §XI.E.1, it would have been obvious for a POSITA to maintain an intervening silicon layer between the source/drain junction and the silicon oxide layer. In my opinion, a POSITA would have recognized that doing so would have formed a source/drain junction capacitance. *Supra* §§VI.C, XI.A.1.c-XI.A.1.d, XI.B.1.c-XI.B.1.d, XI.E.1.

- d. [1c(i)-1c(ii)]: “at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in

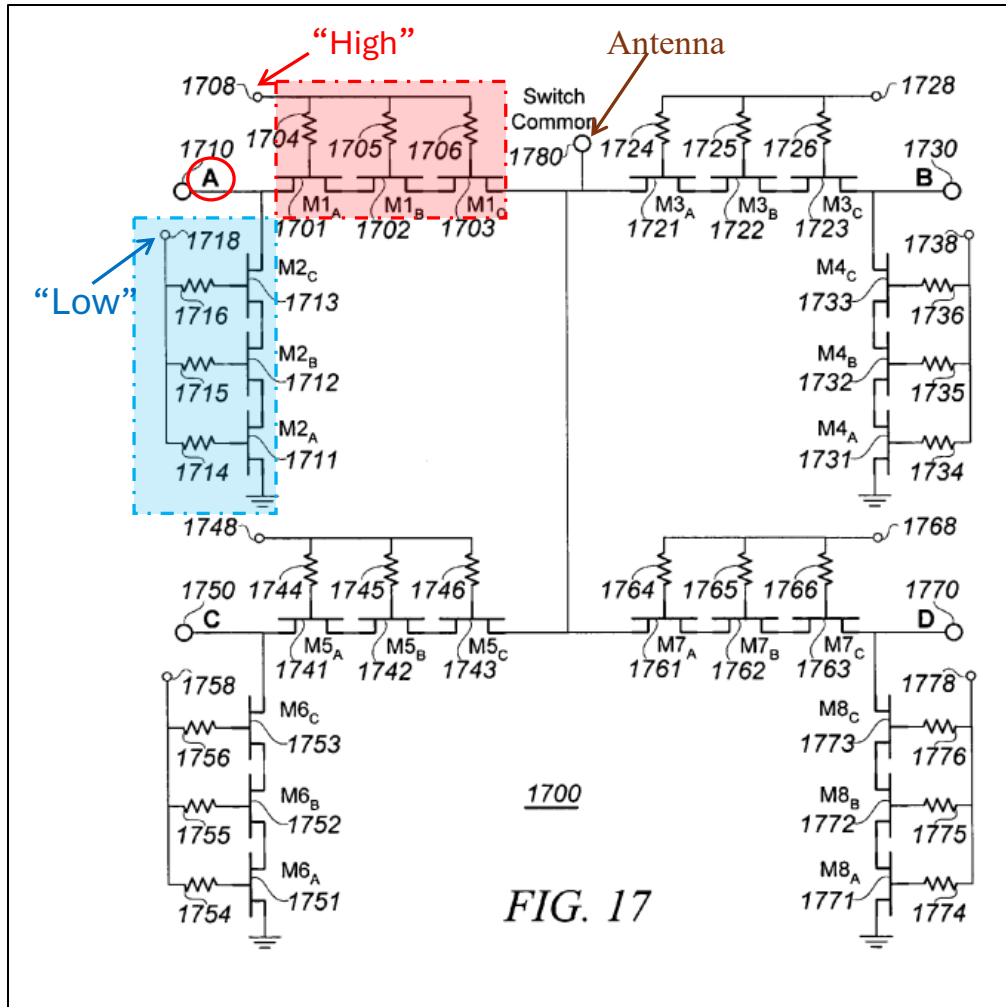
said switching circuit so as to reduce voltage and current fluctuations in said device layer.”

224. *Burgener* in view of *Okashita* teaches these limitations. In *Burgener*’s antenna switch as modified by *Okashita*, as described with reference to claims [1c(i)]-[1c(ii)] of grounds 1 and 2, there would be at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer. *Supra* §§XI.A.1.e-XI.A.1.f, XI.B.1.e-XI.B.1.f, XI.E.1.

3. Claim 2

- a. [2]: “The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is situated within an isolated island in said device layer.”**

225. *Burgener* in view of *Okashita* teaches this limitation. For example, at least one of the plurality of *Burgener*’s FETs would be situated within an isolated island, as *Okashita* teaches. *See supra* §§XI.B.2.a, XI.B.3.a, XI.E.1.



Burgener as modified by *Okashita*, at least one of the cascaded transistors (e.g., one of the FETs in **FETs 1701-1703** or one of the FETs in **FETs 1711-1713**) is located within an isolated island in the device layer.

4. Claims 3

- a. [3]: “The switching circuit of claim 1, wherein said plurality of cascaded transistors is situated within an isolated island in said device layer.”

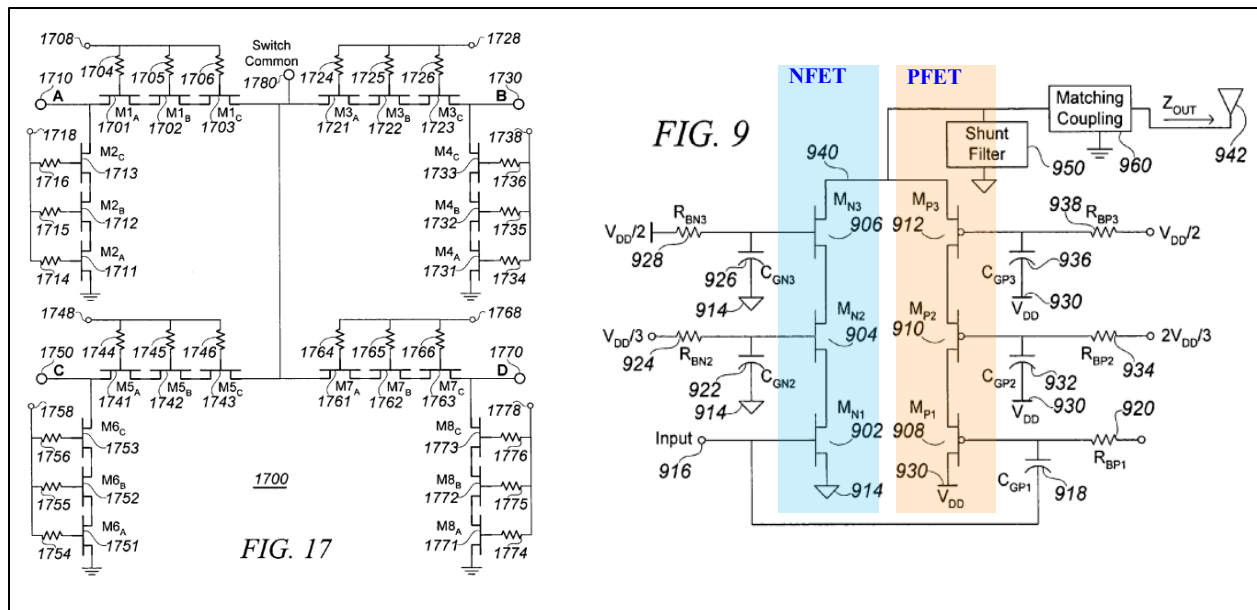
227. *Burgener* in view of *Okashita* teaches the additional limitation of this claim. As I explained with reference to claim 2, *supra* §§XI.E.1, XI.E.3.a, *Burgener*’s cascaded **FETs 1701-1703** would have been situated within an isolated island surrounded by a **trench**. For example, as *Okashita* teaches, the cascaded **FETs 1701-1703** would have been situated within an isolated island surrounded by a **trench**. *Supra* §XI.E.1. Alternatively, or additionally, the cascaded **FETs 1711-1713** would have been situated within an isolated island surrounded by a **trench**. *Id.* Therefore, in my opinion, a POSITA would have known that *Burgener* in view of *Okashita* teaches a plurality of the cascaded **transistors** that are located within an isolated island in the device layer.

5. Claim 4

- a. [4]: “The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is an

NFET with a gate driven by a switch control signal in a wireless communications device.”

228. *Burgener* teaches the additional limitation of this claim. According to *Burgener*, a FET stack may be N-channel FETs (NFETs) or P-channel FET (PFET). *Burgener*, ¶[0079]. To fabricate PFET stacks, “the polarity of each voltage and the polarized component associated with the stack” is reversed. *Burgener*, ¶[0079]. *Burgener*’s Figure 9, as shown below, shows an exemplary circuit that employs both NFET stack and PFET stack. *Burgener*, ¶[0080].



Burgener, Figs. 9, 17.

229. *Burgener* does not explicitly state that the FETs of antenna switch 1700 of Figure 17 are NFETs. However, based on the symbols of NFETs and PFETs used in *Burgener*, a POSITA would have recognized that the transistors of antenna switch 1700 of Figure 17 are NFETs. For example, the symbol of a PFET

has a small circle on the gate in the symbol, but the symbol of an NFET does not. This is shown in *Burgener*'s Figure 9, which shows the circuit of a power amplifier that "employs both an N-channel FET stack comprising N-channel FETs M_{N1} 902, M_{N2} 904 and M_{N3} 906, plus a P-channel FET stack comprising P-channel FETs M_{P1} 908, M_{P2} 910 and M_{P3} 912." *Burgener*, ¶[0080]. By comparing the symbols used to represent PFETs and NFETs in Figure 9 (e.g., the addition of a small circle on the gate in the symbol of the PFET) to the symbols used to represent the FETs in antenna switch 1700 (of Figure 17), a POSITA would have understood that the FETs of antenna switch 1700 are NFETs.

230. Moreover, the FET stacks are also controlled by a control signal that is applied to the gates of the FETs. For example, the FETs in antenna switch 1700 are also controlled by applying a control signal to the gates of its FETs. *Burgener*, ¶[0104]; *supra* §§VIII.C, XI.E.1. In my opinion, a POSITA would have known that applying "high" and "low" control voltages to the gates of these FETs selectively switches them ON and OFF to direct signals from the antenna to one of the ports (A-D). *Supra* §§VIII.C, XI.E.1; *Burgener*, ¶¶[0102]-[0103]. Therefore, the gates of these FETs are driven by a switch control signal. *Burgener*, ¶¶[0102]-[0103].

231. Additionally, *Burgener* discloses that its IC with the antenna switch 1700 is used in a wireless communications device. *Burgener*, ¶[0005]. Thus, a

POSITA would have recognized that, in *Burgener* as modified by the teachings of *Okashita*, at least one of the cascaded FETs of antenna switch 1700 is an NFET with a gate driven by a switch control signal in a wireless communications device.

6. Claim 5

- a. **[5]: “The switching circuit of claim 4, wherein said switch control signal drives said gate of said NFET through at least one resistor.”**

232. *Burgener* teaches the additional limitation of this claim. As *Burgener* shows, the control signal drives the gates of the FETs through gate resistors (e.g., resistors 1704, 1705, 1706 of Fig. 17). See *Burgener*, Fig. 17.

7. Claim 6

- a. **[6]: “The switching circuit of claim 1, wherein said at least one of said plurality of cascaded transistors is a PFET with a gate driven by a switch control signal in a wireless communications device.”**

233. *Burgener* teaches the additional limitation of this claim. As I discussed with reference to claim 6 of ground 2, it would have been obvious for a POSITA to use PFET in noise-sensitive applications because PFETs exhibit lower noise than NFETs and are more suitable in noise sensitive applications. Ex. 1018, 3-4; see *supra* §XI.B.6.a. Further, *Burgener* teaches that PFETs may be analogously fabricated by “reversing the polarity of each voltage and polarized component associated with the stack.” *Burgener*, ¶¶[0079]-[0080]; §XI.E.5.a.

234. In my opinion, a POSITA would have a reasonable expectation of success in incorporating PFETs in antenna switch 1700, as *Burgener* suggests, because there are only two ways to make a transistor (either as a NFET or a PFET). *Supra* §XI.B.6.a; Ex. 1012, 2 (explaining that there are two basic types of FETs - the NFET and PFET, and that the PFET is the mirror image of the NFET); Ex. 1008, 20 (explaining that there two types of MOSFETS—n-channel MOSFETS and p-channel MOSFETS); Ex. 1010, 70 (“pMOS is very similar [to nMOS], except for the diffusions being of opposite type.”). Thus, a POSITA would have been motivated to use PFETs in the modified *Burgener* antenna switch 1700 for use in noise-sensitive mobile phone application. *See Burgener*, ¶[0005].

235. As I discussed above with reference to claim 4, *supra* §XI.E.5.a, the gates of the FETs in *Burgener*’s antenna switch 1700 are controlled by a switch control signal in a mobile phone. In my opinion, a POSITA would have that, when a PFET stack is used in an antenna switch 1700, its gates would still be driven by a control signal by reversing the gate voltage. Ex. 1012, 2.

8. Claim 7

- a. [7]: “The switching circuit of claim 6, wherein said switch control signal drives said gate of said PFET through at least one resistor.”

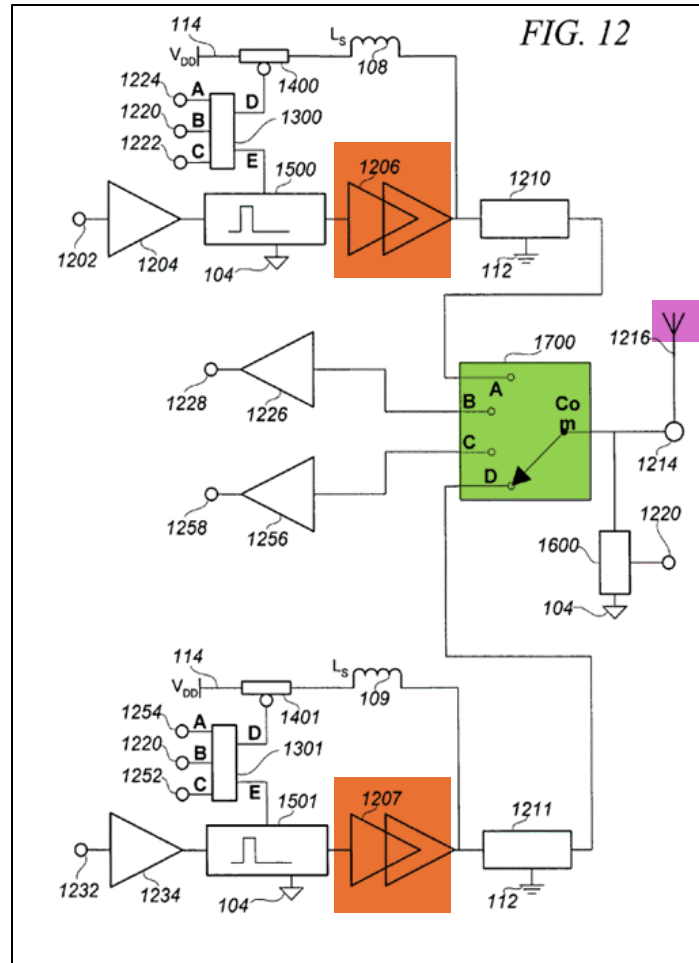
236. *Burgener* teaches the additional limitation of this claim. As I explained with reference to claim 5 of this ground, the control signal drives the

gates of *Burgener*'s FETs through gate resistors (e.g., resistors 1704, 1705, 1706 of Figure 17). *See Burgener*, Fig. 17. When PFETs are used in *Burgener*'s modified antenna switch 1700, the gates of the PFETs will continue to be driven by the switch control signal through gate resistors. *Supra* §§XI.E.5.a-XI.E.7.a.

9. Claim 8

- a. [8a]: “The switching circuit of claim 1, wherein a power amplifier in a wireless communications device provides an input to said switching circuit, and wherein an output of said switching circuit drives an antenna in said wireless communications device,”**

237. *Burgener* teaches these additional limitations. *Burgener*'s RF transceiver uses a power amplifier (PA) 1206, 1207 to provide a conditioned PA signal to the antenna switch 1700, as shown below. *Burgener*, Abstract, ¶¶[0011], [0015], [0037].



Burgener, Fig. 12.

238. *Burgener*'s IC includes a power amplifier (PA) and antenna switch 1700 which connects the conditioned PA signal to an antenna of the communications device. *Burgener*, Abstract, ¶¶[0011], [0015], [0037]. The IC may be used in "wireless communication units, such as cellular telephones." *Burgener*, ¶¶[0005]-[0006].

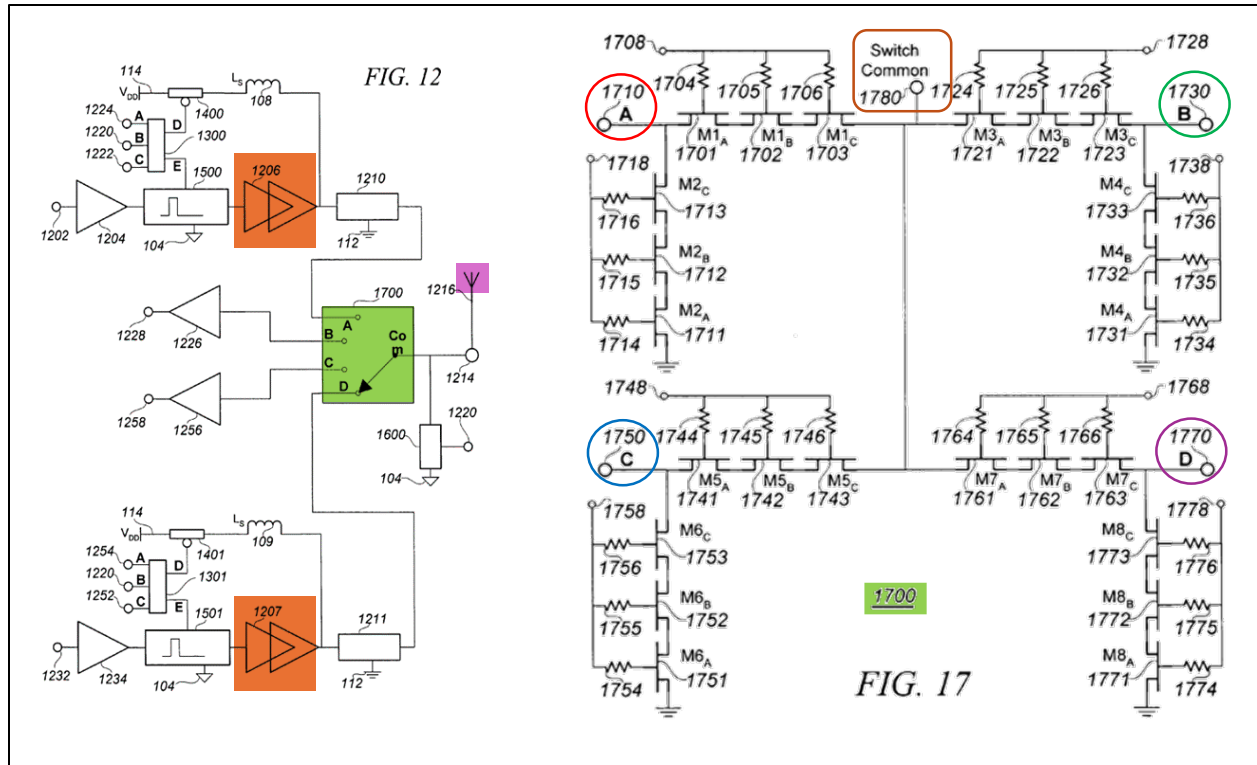
239. With reference to Figure 12, *Burgener* discloses that "[t]he output of the pulse adjustment circuit 1500 is the input to the PA 1206, ... Such a network

may couple the PA output signal to the antenna switch [1700] ... The antenna switch 1700 selectably couples the conditioned PA signal to the antenna node 1214, from whence it may be coupled, for example by transmission line, to an antenna[.]” *Burgener*, ¶[0090]. Accordingly, the output of the antenna switch 1700 drives the antenna of a wireless communication unit, such as a cellular telephone. *Burgener*, ¶[0005]-[0006].

240. Thus, in *Burgener*’s wireless communication device, a power amplifier 1206 or 1207 provides an input to the antenna switch 1700, and an output of the antenna switch 1700 drives an antenna of the wireless communication device. *Burgener*, Abstract, ¶[0011], [0015], [0037].

b. [8b]: “and said switching circuit is controlled by a switch control signal in said wireless communications device.”

241. *Burgener* teaches the additional limitation. As explained *supra* §§VIII.C, XI.E.1, *Burgener*’s antenna switch 1700 selectively connects different RF ports (A, B, C, D) to an antenna by applying high and low control voltages to control the RF nodes. *Burgener*, ¶[0090]-[0092].



Burgener, Figs. 12, 17.

242. For example, as I explained *supra* §§VIII.C, XI.E.1, to connect port A 1710 to the antenna via common node 1780, a “high” voltage is applied to control nodes 1708, 1738, 1758, and 1778, while a “low” voltage is applied to the other control nodes (1718, 1728, 1748, and 1768). *Burgener*, ¶[0090]. The antenna switch 1700 can selectively disconnect the antenna from port A and instead connect the antenna to port B by similarly applying “high” and “low” voltages to the control nodes to route a signal received from the antenna to a receive preamplifier 1226 (a low noise amplifier (LNA)). *Burgener*, ¶[0092]. By applying control signals to the FET control nodes, the antenna switch 1700 can similarly

disconnect the antenna from port B and connect it to port C to route the received signal to another LNA 1256. *Burgener*, ¶[0092]. Therefore, antenna switch 1700 is controlled by a switch control signal in the wireless communications device.

10. Claim 9

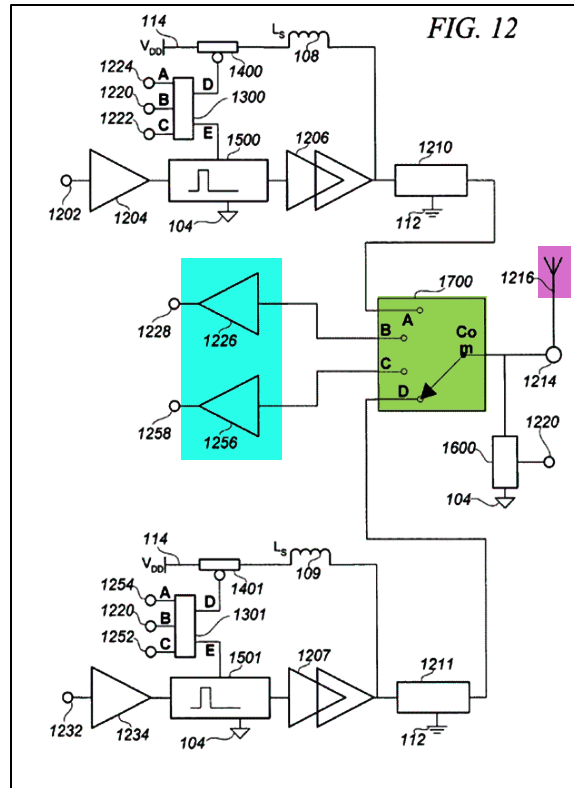
- a. [9]: “The switching circuit of claim 8, wherein said wireless communications device is selected from the group consisting of a cellular telephone, a wireless personal computer, a wireless audio player, a wireless video player, and a wireless personal assistance device.”

243. *Burgener* discloses the additional limitations of this claim. *Burgener*’s antenna switch 1700 may be used in “[w]ireless communications devices ... [such as] cellular mobile telephones.” *Burgener*, ¶[0005].

11. Claim 10

- a. [10a]: “The switching circuit of claim 1, wherein an antenna in a wireless communications device provides an input to said switching circuit, and wherein an output of said switching circuit drives a low noise amplifier in said wireless communications device,”

244. *Burgener* discloses these additional limitations. *Burgener*’s RF transceiver includes low noise amplifiers (LNA) 1226, 1256. *Burgener*, Abstract, ¶¶[0005], [0037], [0092].



Burgener, Fig. 12.

245. In *Burgener*, the wireless communication device includes an IC with preamplifiers 1226, 1256 (low noise amplifier (LNA)) and a four-way antenna switch 1700, and an antenna. *Burgener*, Abstract, ¶¶[0005], [0037], [0092].

246. For example, the antenna switch 1700 selectably couples the antenna to RF ports B or C “to deliver a signal received from the antenna” to one of the LNAs 1226, 1256. *Burgener*, ¶[0092]. Thus, the output of the antenna switch 1700 drives a LNA in said wireless communications device.

- b. [10b]: “and wherein said switching circuit is controlled by a switch control signal in said wireless communications device.”**

247. *Burgener* discloses this additional limitation. As discussed previously with reference to claim [8b] of this ground, *Burgener*’s antenna switch 1700 is controlled by a switch control signal in the wireless communications device. *Supra* §XI.E.9.b.

12. Claim 11

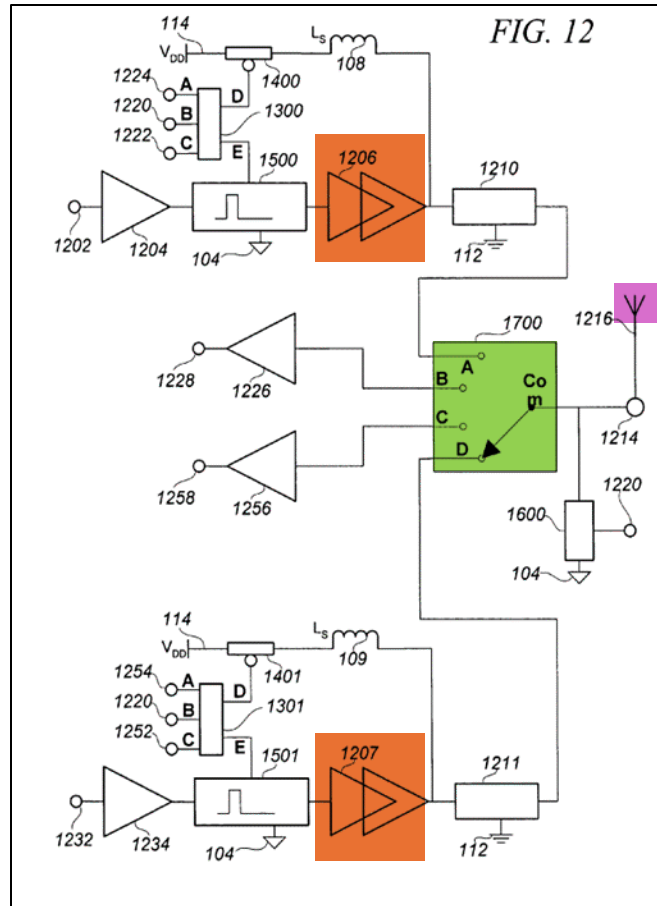
- a. [11]: “The switching circuit of claim 10, wherein said wireless communications device is selected from the group consisting of a cellular telephone, a wireless personal computer, a wireless audio player, a wireless video player, and a wireless personal assistance device.”**

248. *Burgener* discloses this additional limitation. In *Burgener*, the wireless communications device is a cellular telephone. *Supra* §XI.E.12.a.

13. Independent Claim 12

- a. [12pre]: “A wireless communications device ... comprising:”**

249. To the extent the preamble is limiting, *Burgener* discloses a “wireless communications device,” such as “cellular mobile telephone” with a RF transceiver that includes power amplifiers (PA) 1206, 1207 and an antenna. *Burgener*, Abstract, ¶¶[0005], [0037], [0090], [0093]; *supra* XI.E.9.a.



Burgener, Fig. 12.

- b. [12a]: “a switching circuit controlled by a switch control signal and interposed between said power amplifier and said antenna, said switching circuit including:”

250. *Burgener* discloses this limitation. As I explained in claim [1pre] of this ground, §§XI.E.1, XI.E.2.a, *Burgener*’s antenna switch 1700 is a switching circuit. *Burgener*, ¶¶ [0090]-[0094], [0104]. As I explained in claim [8b] of this ground, *supra* §§XI.E.1, XI.E.9.b, the antenna switch 1700 is controlled by a switch control signal to select one of the RF ports A, B, C, or D. Further, the

and an **antenna**, as shown below.



Burgener, Fig. 12.

251. *Burgener's* integrated circuit (IC) includes an antenna switch 1700 that selectably directs incoming signals from the antenna 1216 to receive preamplifiers 1226, 1256 and outgoing signals from power amplifiers (PA) 1206, 1207 to the antenna 1216. *Burgener*, ¶¶[0090]-[0094]; *supra* §§XI.E.1, XI.E.9.a. For example, the output signal from the power amplifier 1206 is directed to the port A input of the antenna switch 1700, which selectably couples this signal to the

antenna 1216. *Burgener*, ¶[0090]. Similarly, antenna switch 1700 selectably couples output signal from the power amplifier 1207 to the antenna 1216.

Burgener, ¶[0093]. Thus, antenna switch 1700 is interposed between power amplifiers 1206, 1207 and antenna 1216.

- c. [12b]: “a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer, each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;”

252. *Burgener* in view of *Okashita* teaches these additional limitations for the same reasons stated in claim 1 of this ground. *Supra* §§VIII.A, XI.E.1, XI.E.2.b-XI.E.2.c, XI.B.1.b-XI.B.1.d.

- d. [12c]: “at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.”

253. *Burgener* in view of *Okashita* teaches these additional limitations for the same reasons stated in claim 1 of this ground. *Supra* §§VIII.A, XI.E.1, XI.B.1.e-XI.B.1.f.

14. Claims 13-15

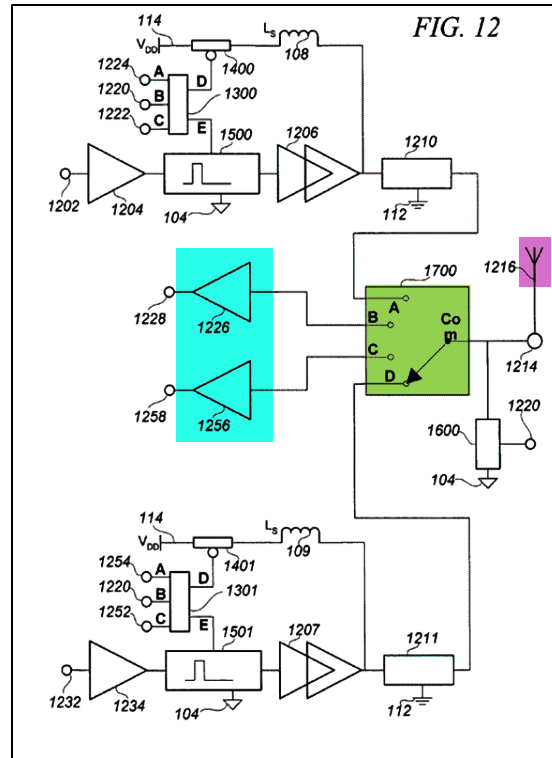
254. *Burgener* in view of *Okashita* renders the additional limitations of each of claims 13-15 obvious for the same reasons as stated in claims 2, 3, and 9, respectively, of this ground.

Claim	Corresponding Claim
Claim 13	Claim 2. §§XI.B.2.a, XI.E.3.a,
Claim 14	Claim 3. §§XI.B.3.a, XI.E.4.a
Claim 15	Claim 9. §XI.E.10.a

15. Independent Claim 16

- a. [16pre]: “A wireless communications device comprising an antenna and a low noise amplifier, said wireless communications device further comprising:”

255. To the extent the preamble is limiting, *Burgener* discloses a “wireless communications device,” such as a “cellular mobile telephone,” with a RF transceiver that includes an antenna 1216, an antenna switch 1700, and low noise amplifiers 1226, 1256, as shown below. *Burgener*, Abstract, ¶¶[0005], [0037], [0092]; *supra* §§XI.E.1, XI.E.11.a, XI.E.13.a.



Burgener, Fig. 12.

- b. [16a]: “a switching circuit controlled by a switch control signal and interposed between said antenna and said low noise amplifier, said switching circuit including:”

256. *Burgener* discloses this limitation. As I explained in claims [1pre], [10b], and [12a] of this ground, antenna switch 1700 is a switching circuit that is controlled by a switch control signal. *Burgener*, ¶[0104]; see *supra* §§XI.E.1, XI.E.11.a-XI.E.11.b, XI.E.13.b. Because the antenna switch 1700 delivers “a signal received from the antenna [1216] to” the low noise amplifier 1226 or low noise amplifier 1256, (*Burgener*, ¶[0092]), the antenna switch 1700 is interposed between the low noise amplifiers 1226, 1256 and the antenna 1216.

- c. **[16b]: “a plurality of cascaded transistors fabricated in a device layer situated over a buried oxide layer and a bulk semiconductor layer, each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer, thereby forming a source/drain junction capacitance;”**

257. *Burgener* in view of *Okashita* teaches these additional limitations for the same reasons stated in claim 1 of this ground. *Supra* §§VIII.A, XI.B.1.c-XI.B.1.d, XI.E.2.b-XI.E.2.c, XI.E.1.

- d. **[16c]: “at least one trench extending through said device layer and contacting a top surface of said buried oxide layer, thereby electrically isolating at least one of said plurality of cascaded transistors in said switching circuit so as to reduce voltage and current fluctuations in said device layer.”**

258. *Burgener* in view of *Okashita* teaches these additional limitations for the same reasons stated in claim 1 of this ground. *Supra* §§VIII.A, XI.B.1.e-XI.B.1.f, XI.E.2.d, XI.E.4.a, XI.E.13.d.

16. Claims 17-19

259. *Burgener* in view of *Okashita* renders the additional limitations of each of claims 17-19 obvious for the same reasons as stated in claims 2, 3, and 9, respectively, of this ground.

Claim	Corresponding Claim
Claim 17	Claim 2. §§XI.B.2.a, XI.E.3.a
Claim 18	Claim 3. §§XI.B.3.a, XI.E.4.a

Claim 19	Claim 9. §XI.E.10.a
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F. Ground 6: Claims 1-19 Are Obvious Over *Burgener*, *Okashita*, and *Yu*

1. Combining *Burgener* with *Okashita* and *Yu*

260. As explained in Ground, *supra* §XI.E.1, it would have been obvious for a POSITA to (1) isolate *Burgener*'s cascaded FETs using surrounding **trenches**, as *Okashita* teaches, to prevent leakage of radio frequency signals between these cascaded FETs. *See supra* §§XI.B.1.e-XI.B.1.f, XI.B.3.a, XI.E.1. Additionally, it would have been obvious to (2) maintain an intervening **silicon layer**, as *Okashita* teaches, to separate the **source/drain** junctions of *Burgener*'s FETs from the **buried oxide layer** to decrease the operating temperature of the FETs and, thereby, improve their performance and reliability. *See* Ex. 1010, 60; Ex. 1013, 27; *see also supra* §§XI.B.1.c-XI.B.1.d, XI.E.1.

261. To the extent that Patent Owner contends otherwise, it would have been obvious in further view of *Yu*. *See supra* §§VIII.B, XI.C.1. *Yu* teaches two “important” features to reduce problems for devices formed in a conventional SOI process: (1) maintaining a sufficiently “thick” intervening silicon layer so that the doped regions “do not extend to the buried oxide layer” (*Yu*, 6:46-54; *supra* §§VIII.B, XI.C.1); and (2) using trench insulation structures that remain completely outside of the active device region. *Yu*, 5:16-19 (“The STI regions 36

do not extend into the LVT-SCR device nor do they separate the first or second type doped regions [formed in silicon layer 42, 44].”). *Supra* §§VIII.B, XI.C.1; *see also Yu*, 2:4-17; Ex. 1010, 60; Ex. 1013, 27-28.

262. In my opinion, a POSITA would have been motivated to ensure that an intervening silicon layer is sufficiently thick in the active area and that the cascaded FETs are completely within an isolated island of the active area, as *Yu* teaches, to ensure that the switching device does not fail at a lower energy dissipation level and to achieve the electrical benefits described by *Yu* (*see Yu*, 2:4-17). *Supra* §§VIII.B, XI.C.1. Since *Burgener*, *Okashita*, and *Yu* all disclose switching circuits with cascaded transistors having an SOI configuration (*see supra* §§VIII.A-VIII.C), a POSITA would have had a reasonable expectation of success in incorporating *Yu*’s teaching into *Burgener* and *Okashita*.

2. Claims 1-19

263. *Burgener* in view of *Okashita* teaches all the limitations of claims 1-19 as described in ground 5 above. To the extent Patent Owner contends that *Okashita* does not explicitly mention that “each of said plurality of cascaded transistors having a source/drain junction that does not contact said buried oxide layer,” as recited in claims [1b(i)], [12b], and [16b], it would have been obvious in view of *Okashita* and *Yu*.

264. As I explained previously, a POSITA would have been motivated to ensure that the intervening silicon layer between the source/drain junctions of *Burgener*'s FET as modified by *Okashita* is sufficiently thick in the active area, as taught by *Yu*, such that the source/drain junctions remain separated from the buried oxide layer to ensure that the modified *Burgener* switching device does not fail at a lower energy dissipation level and to achieve the electrical benefits described by *Yu*. See *Yu*, 2:4-17. Thus, in my opinion, *Burgener* in view of *Okashita* and *Yu* renders obvious claims 1-19.

XII. CONCLUSION

265. For the reasons set forth above, it is my opinion that one skilled in the art would have found claims 1-19 of the '886 patent anticipated by or obvious over the prior art. My opinion would remain the same even if the level of skill in the art was slightly lower (e.g., requiring only a bachelor's degree instead of a master's degree).

266. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for

cross-examination within the United States during the time allotted for cross-examination.

267. I declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001.

Date: September 24, 2024


By: _____

Scott E. Thompson, Ph.D.

APPENDIX A

SCOTT EMMET THOMPSON

Prof. Electrical Engineering and Computer Science Department / Univ. of Florida
IEEE Fellow for contributions on advancing MOSFETs
Former Intel Corporation Fellow and Director of Computer Chip Technology

A. Education and Training

Education

- 1992 Ph.D. (Electrical Engineering), University of Florida
- 1988 Master of Science in Electrical Engineering, University of Florida
- 1987 Bachelor of Electrical Engineering with Highest Honors, University of Florida

B. Professional Experience

- ❑ Tenured Full Professor and Faculty/ Electrical and Computer Engineering, University of Florida (2/2004 to present).
- ❑ Founder and CTO of SuVolta (a low power chip company) (2009 - 2/2015).
 - Technology sold to Fujitsu and used in Mibeaut image sensor processor
- ❑ Researcher on advanced chip technology at University of Florida totaling \$4M worth of research contracts.
 - 2019-2021 Research funding from Semiconductor Research Corporation (SRC)
- ❑ Consultant (non litigation) last 5 years: Xperi Corporation
- ❑ **Intel Corporation** 1992 to 2004. Intel Fellow (highest technical level) and Director of computer chip technology (semiconductor manufacturing) including transferring and bringing up new manufacturing facilities worldwide.
- ❑ Intel Corporation experience and industry consulting on semiconductor manufacturing, semiconductor technology, yield and quality.
- ❑ Developed ultra low power chip technology for image sensors, SOC, RFIC, Memory, CPU, image sensors processors and other chips.
- ❑ Developed graduate level courses at University of Florida on advanced semiconductor chip, semiconductor design and packaging technology (chip stacking) and computer chip technology including CPU, DRAM, GPU, image sensors, 2D and 3D image sensor processing.
- ❑ National Science Foundation Panel Reviewer for semiconductor/computer chip funding.

C. Legal cases

- ❑ Bold is the client
 - Godo Kaisha IP Bridge v/ **Xilinx/TSMC**
 - Case No. 2:17-CV-00100-JRG-RSP (E.D. Tex.) - filed 1/31/2017

- **KAIST IP v. Apple**
 - March /2019 Report to Intellectual Property Trial and Appeals board regarding Korean Patent No. 10-0458288
 - Case in Korea : Intellectual Property Trial and Appeal Board (“IPTAB”) regarding Korean Patent No. 10-0458288 (hereinafter, “KR ‘288 patent”).
- **Godo Kaisha IP Bridge, Inc. v. NVIDIA**
 - NVIDIA Singapore Pte Ltd. as a technical expert in the customs proceeding initiated by petitioner Godo Kaisha IP Bridge 1
- **Chinese Academy of Sciences v. Intel**
 - IPR report Sept / 2018 in case IPR2018-01574 - filed 9/18/2018
 - IPR report Mar / 2019 in case IPR2019-00834 - filed 3/19/2019
 - Beijing Court Testimony IME vs Lenovo 11/21/2021
 - Beijing court Testimony IME vs Intel China 1/12/2022
- **IFT v. TSMC (ITC case)**
 - Case 1:19-cv-00308-UNA (D. Del.) - filed 2/13/2019
 - Inv. No. 337-TA-1149 - initial notice 4/3/2019
- **NXP v. Impinj**
 - 9,495,631, IPR2020-00543 - filed 2/10/2020
 - 9,633,302, IPR2020-00516 - filed 2/5/2020
 - 6,680,523, IPR2020-01630 - filed 9/17/2020
 - 7,538,444, IPR2021-00003 - filed 10/5/2020
 - Oakland District Court Case No. 4:19-cv-03161-YGR
- **Katana Silicon Technology LLC v. GlobalFoundries 2022**
 - IPR2022-01083
- **Ericsson v. Apple** Brazil Patent BRPI 9811639-8 filed 2022
- **Greenthread v. Intel** Case 6:22-cv-105-ADA filed 12/2022
- **ITC Daedalus v. TSMC** Case 337-TA-1336 filed 10/2022
- **Oasis Tooling, Inc v. GlobalFoundries** C.A. No. 22-312-CJB 3/2023
- **BiTMICRO LLC v. Intel** IPR2023-00781 filed 3/31/2023
- **Longitude Licensing LTD, v Western Digital Technologies, Inc.** IPR2023-01286 filed 8/08/2023

D. Honors and Awards

- ❑ 100 granted US patents, 60 publications and 1 book on semiconductors
- ❑ Elected to **IEEE Fellow** in 2006 for Advancing Fabrication of nanoscale MOSFET
- ❑ Elected to Intel Fellow in 2003
- ❑ Thompson and co-workers were the first to publish at the International Electron Device Meeting (IEDM) in 2002 on a 90nm logic technology which introduced high levels of strain for significant mobility enhancement using SiGe
- ❑ 2008 SEMI award North American Recipient
- ❑ 2014 TiE 50: Top Startup (SuVolta)

- ❑ 2012 ACE Award IEEE Spectrum: IEEE Emerging Technology: SuVolta
- ❑ 2011 EuroAsia IC Industry Award for start-up
- ❑ 2008 Semi Award North America (for Develop of Strained Silicon Transistors)

E. Publications/Patents

- [1] T. A. Weingartner, C. -H. Kuo, A. Thomas, S. E. Thompson and M. E. Law, "Negative Impact of Compressive Biaxial Stress on High Precision Bipolar Devices," in *IEEE Transactions on Components, Packaging and Manufacturing Technology*, doi: 10.1109/TCPMT.2021.3095670.
- [2] C.-H. Kuo, T. A. Weingartner, M. E. Law, S. E. Thompson, and A. Appaswamy, *Effect of Stress on Bipolar Transistor*, SRC TECHCON 2021
- [3] S. E. Thompson et al., "Digital Circuits Having Improved Transistors, and Methods therefor" US Patent 10,250,257, 2019.
- [4] S. E. Thompson et al., "Advanced Transistors with Punch Through Suppression", US Patent US10325986B2, 2019.
- [5] S. E. Thompson et. al., "Electronic Devices and Systems And Methods For Making And Using The Same," US Patent 10,217,668, 2019.
- [6] S. E. Thompson et. al., "Electronic Devices and Systems And Methods For Making And Using The Same," US Patent 10224244B2, 2019.
- [7] S. E. Thompson et al., "Digital Circuits Having Improved Transistors, and Methods therefor" US Patent US20180248548A1, 2018.
- [8] S.E. Thompson et.al., "Low Power Semiconductor Transistor Structure and Method of Fabrication Thereof", US9865596B2, 2018.
- [9] S.E. Thompson et al. "Integrated Circuit Devices and Methods", US Patent US9966130B2, 2018
- [10] S.E. Thompson et al. "Buried Channel Deeply Depleted Channel Transistor, US Patent US9991300B2, 2018.
- [11] S. E. Thompson et. al., "Electronic Devices and Systems And Methods For Making And Using The Same," US Patent US10074568B2, 2018
- [12] S.E. Thompson et al., Transistor With Threshold Voltage Set Notch and Method of Fabrication Thereof" US Patent US9922977B2, 2018.
- [13] S. E. Thompson et. al., "Buried Channel Deeply Depleted Channel Transistor," US 9,786,703 B2, 2017.
- [14] S. E. Thompson et. al., "Electronic Devices and Systems And Methods For Making And Using The Same," US 2017/0117366 A1, 2017.
- [15] S. E. Thompson et. al., "Field Effect Transistor And Method For Producing The Same," JP2017055140A, 2017.
- [16] S. E. Thompson et. al., "Advanced Transistors With Punch Through Suppression," US 2017/0040419 A1, 2017.

- [17] S. E. Thompson et. al., “Digital Circuits Having Improved Transistor, and Methods Therefor,” US 9,838,012 B2, 2017.
- [18] S. E. Thompson et. al., “Low Power Semiconductor Transistor Structure And Method Of Fabrication Thereof,” US 2017/0012044 A1, 2017.
- [19] S. E. Thompson et. al., “Integrated Circuit Devices And Methods,” US 9,741,428 B2, 2017.
- [20] S. E. Thompson et. al., “Low Power Semiconductor Transistor Structure and Method of Fabrication Thereof,” US 9,496,261, 2016.
- [21] S. E. Thompson et. al., “CMOS Gate Stack Structures And Processes,” US 9,508,728 B2, 2016.
- [22] S. E. Thompson et. al., “Integrated Circuit Devices and Methods,” US 9,362,291 B1, 2016.
- [23] S. E. Thompson et. al., “Method For Fabricating A Transistor With Reduced Junction Leakage Current,” US 9,368,624 B2, 2016.
- [24] S. E. Thompson et. al., “Advanced Transistors With Punch Through Suppression,” US 9,263,523 B2, 2016.
- [25] S. E. Thompson et. al., “Analog Circuits Having Improved Transistors, And Methods Therefor,” US 9,231,541 B2, 2016.
- [26] S. E. Thompson et. al., “Electronic Devices and Systems, and Methods for Making and Using the Same,” US 2016/0358918 A1, 2016.
- [27] S. E. Thompson et. al., “Buried Channel Deeply Depleted Channel Transistor,” US 9,478,571 B1, 2016.
- [28] S. E. Thompson et. al., “Transistor With Threshold Voltage Set Notch and Method of Fabrication Thereof,” US 9,418,987 B2, 2016.
- [29] S. E. Thompson et. al., “Method For Fabricating Multiple Transistor Devices on a Substrate With Varying Threshold Voltages,” US 9,406,567 B1, 2016.
- [30] S. E. Thompson et. al., “CMOS Structures and Processes Based On Selective Thinning,” US 9,391,076 B1, 2016.
- [31] S. E. Thompson et. al., “Epitaxial Channel Transistor and Die With Diffusion Doped Channels,” US 2016/0211346 A1, 2016.
- [32] S. E. Thompson et. al., “Digital Circuits Having Improved Transistors, and Methods Therefor,” US 2016/0020768 A1, 2016.
- [33] S. E. Thompson et. al., “Analog Circuits Having Improved Transistors, And Methods Therefor,” US 2015/0015334 A1, 2015.
- [34] S. E. Thompson et. al., “High Uniformity Screen And Epitaxial Layers For CMOS Devices,” US 9,196,727 B2, 2015.
- [35] S. E. Thompson et. al., “Porting A Circuit Design From A First Semiconductor Process To A Second Semiconductor Process,” US 9,117,746 B1, 2015.
- [36] S. E. Thompson et. al., “Digital Circuits Having Improved Transistors, And Methods Therefor,” US 9,184,750 B1, 2015.
- [37] S. E. Thompson et. al., “Embedded Channel Type Deep Depletion Channel Transistor,”

JP2015226059A, 2015.

[38] S. E. Thompson et. al., "Deeply Depleted MOS Transistors Having A Screening Layer And Methods Thereof," US 9,041,126 B2, 2015.

[39] S. E. Thompson et. al., "Field Effect Transistor (FET) And Method For Fabricating The Same," JP2015195403A, 2015.

[40] S. E. Thompson et. al., "Analog Transistor," US 9,093,469 B2, 2015.

[41] S. E. Thompson et. al., "Semiconductor Devices Having Fin Structures and Fabrication Methods Thereof," US 9,054,219 B1, 2015.

[42] S. E. Thompson et. al., "Field Effect Transistor and Methods for Producing The Same," JP2015213200A, 2015.

[43] S. E. Thompson et. al., "Electronic Devices and Systems, And Methods For Making And Using The Same," US 8,975,128 B2, 2015.

[44] S. E. Thompson, "Advanced CMOS Device Physics for 7nm and Beyond," in Invited Short Course at International Electron Device Meeting, Washington D.C., 2015.

[45] S. E. Thompson et. al., "Advanced Transistor With Punch Through Suppression," US 2014/0167156 A1, 2014.

[46] S. E. Thompson et. al., "Analog Circuits Having Improved Transistors, And Methods Therefor," US 8,847,684 B2, 2014.

[47] S. E. Thompson et. al., "Integrated Circuit Devices And Methods," US 8,811,068 B1, 2014.

[48] S. E. Thompson et. al., "Transistor With Threshold Voltage Set Notch And Method Of Fabrication Thereof," US 8,759,872 B2, 2014.

[49] S. E. Thompson et. al., "Monitoring And Measurement of Thin Film Layers," US 8,796,048 B1, 2014.

[50] S. E. Thompson et. al., "Deeply Depleted MOS Transistors Having A Screening Layer And Methods Thereof," US 2014/0084385 A1, 2014.

[51] S. E. Thompson et. al., "Electronic Devices and Systems, And Methods For Making and Using the Same," US 2014/0077312 A1, 2014.

[52] S. E. Thompson et. al., "Process For Manufacturing Of Integrated Circuits With Different Channel Doping Transistors Architectures and Devices Therefrom," US 8,877,619 B1, 2014.

[53] S. E. Thompson et. al., "Transistor Having Reduced Junction Leakage And Methods of Forming Thereof," US 8,883,600 B1, 2014.

[54] S. E. Thompson et. al., "Process For Manufacturing An Improved Analog Transistor," US 8,748,270 B1, 2014.

[55] S. E. Thompson et. al., "CMOS Gate Stack Structures And Processes," US 8,735,987 B1, 2014.

[56] S. E. Thompson et. al., "Porting A Circuit Design From A First Semiconductor Process To A Second Semiconductor Process," US 8,645,878 B1, 2014.

[57] S. E. Thompson et. al., "Multiple Transistor Types Formed In A Common Epitaxial Layer By Differential Out-Diffusion From A Doped Underlayer," US 8,629,016 B1, 2014.

- [58] S. E. Thompson et. al., “Cmos Structures And Processes Based On Selective Thinning,” US 8,614,128 B1, 2013.
- [59] S. E. Thompson et. al., “Low Power Semiconductor Transistors Structure and Method of Fabrication Thereof,” US 8,530,286 B2, 2013.
- [60] S. E. Thompson et. al., “Electronic Devices And Systems, And Methods For Making And Using The Same,” US 2013/0020639 A1, 2013.
- [61] S. E. Thompson et. al., “Semiconductor Devices Having Fin Structures and Fabrication Methods Thereof,” WO2013022753A2, 2013.
- [62] S. E. Thompson et. al., “Analog Circuits Having Improved Transistors, And Methods Therefor,” US 8,400,219 B2, 2013.
- [63] S. E. Thompson et. al., “Advanced Transistors With Punch Through Suppression,” US 8,421,162 B2, 2013.
- [64] S. E. Thompson et. al., “Digital Circuits Having Improved Transistors, And Methods Therefor,” US 8,461,875 B1, 2013.
- [65] L. T. Clark, D. Zhao, T. Bakhishev, H. Ahn, E. Boling, M. Duane, K. Fujita, P. Gregory, T. Hoffmann, M. Hori, D. Kanai, D. Kidd, S. Lee, Y. Liu, J. Mitani, J. Nagayama, S. Pradhan, P. Ranade, R. Rogenmoser, L. Scudder, L. Shifren, Y. Torii, M. Wojko, Y. Asada, T. Ema, and S. Thompson, “A highly integrated 65-nm SoC process with enhanced power/performance of digital and analog circuits,” in 2012 International Electron Devices Meeting, 2012, p. 14.4.1-14.4.4.
- [66] M. O. Baykan, S. E. Thompson, and T. Nishida, “Size- and Orientation-Dependent Strain Effects on Ballistic Si p-Type Nanowire Field-Effect Transistors,” IEEE Trans. Nanotechnol., vol. 11, no. 6, pp. 1231–1238, Nov. 2012.
- [67] S.E. Thompson et. al., “Electronic Devices And Systems, And Methods For Making And Using The Same,” US 8,273,617 B2, 2012.
- [68] S. E. Thompson et. al., “Analog Circuits Having Improved Transistors, and Methods Therefor,” US 2012/024209 A1, 2012.
- [69] S. E. Thompson et. al., “Electronic Devices And Systems, And Methods For Making and Using The Same,” EP2483915A1, 2012.
- [70] K. Fujita, Y. Torii, M. Hori, J. Oh, L. Shifren, P. Ranade, M. Nakagawa, K. Okabe, T. Miyake, K. Ohkoshi, M. Kuramae, T. Mori, T. Tsuruta, S. Thompson, and T. Ema, “Advanced channel engineering achieving aggressive reduction of VT variation for ultra-low-power applications,” in 2011 International Electron Devices Meeting, 2011, p. 32.3.1-32.3.4.
- [71] C. D. Young and M. O. Baykan and A. Agrawal and H. Madan and K. Akarvardar and C. Hobbs and I. Ok and W. Taylor and C. E. Smith and M. M. Hussain and T. Nishida and S. Thompson and P. Majhi and P. Kirsch and S. Datta, “Critical discussion on (100) and (110) orientation dependent transport: nMOS planar and FinFET,” in VLSI Technology (VLSIT), 2011 Symposium on, 2011, pp. 18–19.
- [72] S. E. Thompson et. al., “Electronic Devices And Systems, And Methods For Making And Using The Same,” WO2011062788A1, 2011.
- [73] S. E. Thompson et. al., “CMOS Fabrication Process Utilizing Special Transistor

Orientation,” US 7,888,710 B2, 2011.

[74] S. E. Thompson et. al., “Electronic Devices And Systems, And Methods For Making And Using The Same,” US 2011/0074498 A1, 2011.

[75] S. E. Thompson et. al., “Low Power Semiconductor Transistor Structure And Method Of Fabrication Thereof,” US 2011/0248352 A1, 2011.

[76] S. E. Thompson et. al., “Transistor With Threshold Voltage Set Notch And Method Of Fabrication Thereof,” US 2011/0309447 A1, 2011.

[77] S. E. Thompson et. al., “Electronic Devices And Systems, And Methods For Making And Using The Same,” WO2011041109A1, 2011.

[78] D. J. Cummings, H. Park, S. E. Thompson, and M. E. Law, “An Adaptive Grid Scheme for Single-Event Upset Device Simulations,” IEEE Trans. Nucl. Sci., Dec. 2010.

[79] D. J. Cummings, A. F. Witulski, H. Park, R. D. Schrimpf, S. E. Thompson, and M. E. Law, “Mobility Modeling Considerations for Radiation Effects Simulations in Silicon,” IEEE Trans. Nucl. Sci., vol. 57, no. 4, pp. 2318–2326, Aug. 2010.

[80] A. D. Koehler, A. Gupta, Min Chu, S. Parthasarathy, K. J. Linthicum, J. W. Johnson, T. Nishida, and S. E. Thompson, “Extraction of AlGaIn/GaN HEMT Gauge Factor in the Presence of Traps,” IEEE Electron Device Lett., vol. 31, no. 7, pp. 665–667, Jul. 2010.

[81] S. E. Thompson, “Power, cost and circuit IP reuse: The real limiter to Moore’s Law over the next 10 years,” in Proceedings of 2010 International Symposium on VLSI Technology, System and Application, 2010, pp. 88–89.

[82] S. E. Thompson et. al., “Methods And Articles Incorporating Local Stress For Performance Improvement of Strained Semiconductor Devices,” US 7,723,720 B2, 2010.

[83] H. Park, D. J. Cummings, R. Arora, J. A. Pellish, R. A. Reed, R. D. Schrimpf, D. McMorro, S. E. Armstrong, U. Roh, T. Nishida, M. E. Law, and S. E. Thompson, “Laser-Induced Current Transients in Strained-Si Diodes,” IEEE Trans. Nucl. Sci., vol. 56, no. 6, pp. 3203–3209, Dec. 2009.

[84] U. Aghoram, J. Liu, M. Chu, A. D. Koehler, S. E. Thompson, S. Sridhar, R. Wise, S. Pendharkar, and M. Denison, “Effect of mechanical stress on LDMOSFETs: Dependence on orientation and gate bias,” in 2009 21st International Symposium on Power Semiconductor Devices & IC’s, 2009, pp. 220–223.

[85] Zhichao Lu, J. G. Fossum, Ji-Woon Yang, H. R. Harris, V. P. Trivedi, Min Chu, and S. E. Thompson, “A Simplified Superior Floating-Body/Gate DRAM Cell,” IEEE Electron Device Lett., vol. 30, no. 3, pp. 282–284, Mar. 2009.

[86] Y. Sun, S. E. Thompson, and T. Nishida, Strain Effect in Semiconductors: Theory and Device Applications. Springer Science, 2009.

[87] S. E. Thompson et. al., “Methods and Articles Incorporating Local Stress For Performance Improvement of Strained Semiconductor Devices,” US 2009/0072371 A1, 2009.

[88] Y. S. Choi, T. Numata, T. Nishida, R. Harris, and S. E. Thompson, “Impact of mechanical stress on gate tunneling currents of germanium and silicon p -type metal-oxide-semiconductor field-effect transistors and metal gate work function,” J. Appl. Phys., vol. 103, no. 6, pp. 1–6, 2008.

- [89] H. Park, S. K. Dixit, Y. S. Choi, R. D. Schrimpf, D. M. Fleetwood, T. Nishida, and S. E. Thompson, "Total Ionizing Dose Effects on Strained HfO₂ -Based nMOSFETs," *IEEE Trans. Nucl. Sci.*, vol. 55, no. 6, pp. 2981–2985, Dec. 2008.
- [90] S. Suthram, Y. Sun, P. Majhi, I. Ok, H. Kim, H. R. Harris, N. Goel, S. Parthasarathy, A. Koehler, T. Acosta, T. Nishida, H.-H. Tseng, W. Tsai, J. Lee, R. Jammy, and S. E. Thompson, "Strain additivity in III-V channels for CMOSFETs beyond 22nm technology node," in 2008 Symposium on VLSI Technology, 2008, pp. 182–183.
- [91] S. Suthram, H. R. Harris, M. M. Hussain, C. Smith, C. D. Young, J.-W. Yang, K. Mathews, K. Freeman, P. Majhi, H. H.-H. Tseng, R. Jammy, and S. E. Thompson, "Understanding Strain Effects on Double-Gate FinFET Drive-Current Enhancement, Hot-Carrier Reliability and Ring-Oscillator Delay Performance via Uniaxial Wafer Bending Experiments," in 2008 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 2008, pp. 163–164.
- [92] S. Suthram, M. M. Hussain, H. R. Harris, C. Smith, H.-H. Cheng, R. Jammy, and S. E. Thompson, "Comparison of Uniaxial Wafer Bending and Contact-Etch-Stop-Liner Stress Induced Performance Enhancement on Double-Gate FinFETs," *IEEE Electron Device Lett.*, vol. 29, no. 5, pp. 480–482, May 2008.
- [93] A. M. Noori, M. Balseanu, P. Boelen, A. Cockburn, S. Demuynck, S. Felch, S. Gandikota, A. J. Gelatos, A. Khandelwal, J. A. Kittl, A. Lauwers, W.-C. Lee, J. Lei, T. Mandrekar, R. Schreuterkamp, K. Shah, S. E. Thompson, P. Verheyen, C.-Y. Wang, L.-Q. Xia, and R. Arghavani, "Manufacturable Processes for < 32-nm-node CMOS Enhancement by Synchronous Optimization of Strain-Engineered Channel and External Parasitic Resistances," *IEEE Trans. Electron Devices*, vol. 55, no. 5, pp. 1259–1264, May 2008.
- [94] Y. S. Choi, T. Numata, T. Nishida, R. Harris, and S. E. Thompson, "Impact of mechanical stress on gate tunneling currents of germanium and silicon p -type metal-oxide-semiconductor field-effect transistors and metal gate work function," *J. Appl. Phys.*, vol. 103, no. 6, pp. 1–6, 2008.
- [95] G. Sun, Y. Sun, T. Nishida, and S. E. Thompson, "Hole mobility in silicon inversion layers: Stress and surface orientation," *J. Appl. Phys.*, vol. 102, no. 8, pp. 1–7, 2007.
- [96] R. Arghavani, H. M'Saad, E. Yieh, G. Miner, S. Kuppurao, and S. Thompson, "Strain engineering push to the 32nm logic technology node," London, UK Semicond. Fabtech, pp. 2–6, 2007.
- [97] S. Suthram, P. Majhi, G. Sun, P. Kalra, H. R. Harris, K. J. Choi, D. Heh, J. Oh, D. Kelly, R. Choi, B. J. Cho, M. M. Hussain, C. Smith, S. Banerjee, W. Tsai, S. E. Thompson, H. H. Tseng, and R. Jammy, "High Performance pMOSFETs Using Si/Si," *Appl. Phys.*, no. figure 5, pp. 727–730, 2007.
- [98] H. R. Harris, P. Kalra, P. Majhi, M. Hussain, D. Kelly, J. Oh, D. He, C. Smith, J. Barnett, P. D. Kirsch, G. Gebara, J. Jur, D. Lichtenwalner, A. Lubow, T. P. Ma, G. Sung, S. Thompson, B. H. Lee, H. H. Tseng, and R. Jammy, "Band-engineered low PMOS v_T with high-K/metal gates featured in a dual channel CMOS integration scheme," *Dig. Tech. Pap. - Symp. VLSI Technol.*, pp. 154–155, 2007.
- [99] R. A. R. Arghavani, N. D. N. Derhacopian, V. B. V Banthia, M. B. M. Balseanu, N. I. N. Ingle, H. Ms. H. M'Saad, S. V. S. Venkataraman, E. Y. E. Yieh, Z. Y. Z. Yuan, L. Q. X. L. Q. Xia, Z. K. Z. Krivokapic, U. A. U. Aghoram, K. M. K. MacWilliams, and S. E. T. S. E.

Thompson, "Strain Engineering to Improve Data Retention Time in Nonvolatile Memory," IEEE Trans. Electron Devices, vol. 54, no. 2, pp. 362–365, 2007.

[100] S. Suthram, J. C. Ziegert, T. Nishida, and S. E. Thompson, "Piezoresistance coefficients of (100) silicon nMOSFETs measured at low and high (~1.5 GPa) channel stress," IEEE Electron Device Lett., vol. 28, no. 1, pp. 58–61, 2007.

[101] S. Suthram, P. Majhi, G. Sun, P. Kalra, H. R. Harris, K. J. Choi, D. Heh, J. Oh, D. Kelly, R. Choi, B. J. Cho, M. M. Hussain, C. Smith, S. Banerjee, W. Tsai, S. E. Thompson, H. H. Tseng, and R. Jammy, "High Performance pMOSFETs Using Si / Si $1-x$ Ge x / Si Quantum Wells with High- k / Metal Gate Stacks and Additive Uniaxial Strain for 22 nm Technology Node," pp. 727–730, 2007.

[102] Y. Sun, S. E. Thompson, and T. Nishida, "Physics of strain effects in semiconductors and metal-oxide-semiconductor field-effect transistors," J. Appl. Phys., vol. 101, no. 10, pp. 1–22, 2007.

[103] G. Sun, Y. Sun, T. Nishida, and S. E. Thompson, "Hole mobility in silicon inversion layers: Stress and surface orientation," J. Appl. Phys., vol. 102, no. 8, pp. 1–8, 2007.

[104] S. Suthram, P. Majhi, G. Sun, P. Kalra, H. R. Harris, K. J. Choi, D. Heh, J. Oh, D. Kelly, R. Choi, B. J. Cho, M. M. Hussain, C. Smith, S. Banerjee, W. Tsai, S. E. Thompson, H. H. Tseng, and R. Jammy, "High Performance pMOSFETs Using Si/Si $1-x$ Ge x /Si Quantum Wells with High- k /Metal Gate Stacks and Additive Uniaxial Strain for 22 nm Technology Node," in 2007 IEEE International Electron Devices Meeting, 2007, pp. 727–730.

[105] X. Yang, Y. Choi, T. Nishida, and S. E. Thompson, "Gate Direct Tunneling Currents in Uniaxial Stressed MOSFETs," in 2007 International Workshop on Electron Devices and Semiconductor Technology (EDST), 2007, pp. 149–152.

[106] H. R. Harris, S. E. Thompson, S. Krishnan, P. Kirsch, P. Majhi, C. E. Smith, M. M. Hussain, G. Sun, H. Adhikari, S. Suthram, B. H. Lee, H.-H. Tseng, and R. Jammy, "Flexible, simplified CMOS on Si(110) with metal gate / high k for HP and LSTP," in 2007 IEEE International Electron Devices Meeting, 2007, pp. 57–60.

[107] R. Arghavani, H. M'Saad, E. Yieh, G. Miner, S. Kuppurao, and S. Thompson, "Strain engineering push to the 32nm logic technology node," London, UK Semicond. Fabtech, pp. 2–6, 2007.

[108] G. Sun, Y. Sun, T. Nishida, and S. E. Thompson, "Hole mobility in silicon inversion layers: Stress and surface orientation," J. Appl. Phys., vol. 102, no. 8, pp. 1–8, 2007.

[109] S. Suthram, J. C. Ziegert, T. Nishida, and S. E. Thompson, "Piezoresistance coefficients of (100) silicon nMOSFETs measured at low and high (~1.5 GPa) channel stress," IEEE Electron Device Lett., vol. 28, no. 1, pp. 58–61, 2007.

[110] H. R. Harris, P. Kalra, P. Majhi, M. Hussain, D. Kelly, J. Oh, D. He, C. Smith, J. Barnett, P. D. Kirsch, G. Gebara, J. Jur, D. Lichtenwalner, A. Lubow, T. P. Ma, G. Sung, S. Thompson, B. H. Lee, H. H. Tseng, and R. Jammy, "Band-engineered low PMOS v_T with high- K /metal gates featured in a dual channel CMOS integration scheme," Dig. Tech. Pap. - Symp. VLSI Technol., pp. 154–155, 2007.

[111] R. A. R. Arghavani, N. D. N. Derhacopian, V. B. V Banthia, M. B. M. Balseanu, N. I. N. Ingle, H. Ms. H. MSaad, S. V. S. Venkataraman, E. Y. E. Yieh, Z. Y. Z. Yuan, L. Q. X. L. Q.

- Xia, Z. K. Z. Krivokapic, U. A. U. Aghoram, K. M. K. MacWilliams, and S. E. T. S. E. Thompson, "Strain Engineering to Improve Data Retention Time in Nonvolatile Memory," *IEEE Trans. Electron Devices*, vol. 54, no. 2, pp. 362–365, 2007.
- [112] G. Sun, Y. Sun, T. Nishida, and S. E. Thompson, "Hole mobility in silicon inversion layers: Stress and surface orientation," *J. Appl. Phys.*, vol. 102, no. 8, pp. 1–7, 2007.
- [113] S. Suthram, P. Majhi, G. Sun, P. Kalra, H. R. Harris, K. J. Choi, D. Heh, J. Oh, D. Kelly, R. Choi, B. J. Cho, M. M. Hussain, C. Smith, S. Banerjee, W. Tsai, S. E. Thompson, H. H. Tseng, and R. Jammy, "High Performance pMOSFETs Using Si/Si," *Appl. Phys.*, no. figure 5, pp. 727–730, 2007.
- [114] Y. Sun, S. E. Thompson, and T. Nishida, "Physics of strain effects in semiconductors and metal-oxide-semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 101, no. 10, pp. 1–22, 2007.
- [115] S. E. Thompson, G. Sun, Y. S. Choi, and T. Nishida, "Uniaxial-process-induced Strained-Si: Extending the CMOS roadmap," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1010–1020, 2006.
- [116] S. E. Thompson and S. Parthasarathy, "Moore's law: the future of Si microelectronics," *Mater. Today*, vol. 9, no. 6, pp. 20–25, 2006.
- [117] S. E. Thompson, S. Suthram, Y. Sun, G. Sun, S. Parthasarathy, M. Chu, and T. Nishida, "Future of Strained Si / Semiconductors in Nanoscale MOSFETs," *Iedm*, pp. 8–11, 2006.
- [118] X. Yang, J. Lim, G. Sun, K. Wu, T. Nishida, and S. E. Thompson, "Strain-induced changes in the gate tunneling currents in p-channel metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 88, no. 5, pp. 1–3, 2006.
- [119] S. A. Krishnan, H. R. Harris, P. D. Kirsch, C. Krug, M. Quevedo-lopez, C. Young, H. Lee, R. Choi, N. Chowdhury, S. Suthram, S. Thompson, G. Bersuker, and R. Jammy, "High Performing pMOSFETs on Si (110) for Application to Hybrid Orientation Technologies – Comparison of HfO₂ and HfSiON," *IEEE Electron Devices Meet.*, no. 110, pp. 8–11, 2006.
- [120] Y. Sun, G. Sun, S. Parthasarathy, and S. E. Thompson, "Physics of process induced uniaxially strained Si," *Mater. Sci. Eng. B Solid-State Mater. Adv. Technol.*, vol. 135, no. 3, pp. 179–183, 2006.
- [121] S. E. Thompson, "Industry Examples at the State-of-the-Art: Intel's 90nm Logic Technologies," in *Silicon heterostructure handbook : materials, fabrication, devices, circuits, and applications of SiGe and Si strained-layer epitaxy*, CRC Taylor & Francis, 2006.
- [122] S. E. Thompson, "Uniaxial Stressed Si MOSFET," in *Silicon heterostructure handbook : materials, fabrication, devices, circuits, and applications of SiGe and Si strained-layer epitaxy*, CRC Taylor & Francis, 2006.
- [123] J.-S. Lim, X. Yang, T. Nishida, and S. E. Thompson, "Measurement of conduction band deformation potential constants using gate direct tunneling current in n-type metal oxide semiconductor field effect transistors under mechanical stress," *Appl. Phys. Lett.*, vol. 89, no. 7, p. 73509, 2006.
- [124] S. Thompson and G. Sun, "Strained Si and the Future Direction of CMOS," in *2006 International Symposium on VLSI Technology, Systems, and Applications*, 2006, pp. 1–2.

- [125] R. Arghavani, L. Xia, H. M'Saad, M. Balseanu, G. Karunasiri, A. Mascarenhas, and S. E. Thompson, "A reliable and manufacturable method to induce a stress of > 1 GPa on a P-channel MOSFET in high volume manufacturing," *IEEE Electron Device Lett.*, vol. 27, no. 2, pp. 114–116, Feb. 2006.
- [126] S. A. Krishnan, H. R. Harris, P. D. Kirsch, C. Krug, M. Quevedo-Lopez, C. Young, B. H. Lee, R. Choi, N. Chowdhury, S. Suthram, S. Thompson, G. Bersuker, and R. Jammy, "High Performing pMOSFETs on Si(110) for Application to Hybrid Orientation Technologies -- Comparison of HfO₂ and HfSiON," in *2006 International Electron Devices Meeting*, 2006, pp. 1–4.
- [127] I. Polishchuk, S. Levy, R. Kapre, O. Pohland, K. Ramkumar, N. Shah, and S. Thompson, "A Low-Cost Strained Silicon SRAM Technology with Reduced Contact Resistance," in *2006 64th Device Research Conference*, 2006, pp. 263–264.
- [128] S. E. Thompson, G. Sun, Y. S. Choi, and T. Nishida, "Uniaxial-process-induced Strained-Si: Extending the CMOS roadmap," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1010–1020, 2006.
- [129] S. E. Thompson and S. Parthasarathy, "Moore's law: the future of Si microelectronics," *Mater. Today*, vol. 9, no. 6, pp. 20–25, 2006.
- [130] S. E. Thompson, S. Suthram, Y. Sun, G. Sun, S. Parthasarathy, M. Chu, and T. Nishida, "Future of Strained Si / Semiconductors in Nanoscale MOSFETs," *Iedm*, pp. 8–11, 2006.
- [131] X. Yang, J. Lim, G. Sun, K. Wu, T. Nishida, and S. E. Thompson, "Strain-induced changes in the gate tunneling currents in p-channel metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 88, no. 5, pp. 1–3, 2006.
- [132] Y. Sun, G. Sun, S. Parthasarathy, and S. E. Thompson, "Physics of process induced uniaxially strained Si," *Mater. Sci. Eng. B Solid-State Mater. Adv. Technol.*, vol. 135, no. 3, pp. 179–183, 2006.
- [133] N. Mohta and S. E. Thompson, "Mobility enhancement," *IEEE Circuits Devices Mag.*, vol. 21, no. 5, pp. 18–23, 2005.
- [134] S. E. Thompson, R. S. Chau, T. Ghani, K. Mistry, S. Tyagi, and M. T. Bohr, "In search of 'forever,' continued transistor scaling one new material at a time," *IEEE Trans. Semicond. Manuf.*, vol. 18, no. 1, pp. 26–35, 2005.
- [135] S. E. Thompson, "Strained Si and the future direction of CMOS," in *Fifth International Workshop on System-on-Chip for Real-Time Applications (IWSOC'05)*, 2005, pp. 14–16.
- [136] S. E. Thompson, R. S. Chau, T. Ghani, K. Mistry, S. Tyagi, and M. T. Bohr, "In search of 'forever,' continued transistor scaling one new material at a time," *IEEE Trans. Semicond. Manuf.*, vol. 18, no. 1, pp. 26–35, 2005.
- [137] N. Mohta and S. E. Thompson, "Mobility enhancement," *IEEE Circuits Devices Mag.*, vol. 21, no. 5, pp. 18–23, 2005.
- [138] S. E. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, "Key Differences For Process-induced Uniaxial vs . Substrate-induced Biaxial Stressed Si and Ge Channel MOSFETs," *IEEE Electron Devices Meet.*, pp. 221–224, 2004.
- [139] S. E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus,

Z. Ma, B. McIntyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. El-Mansy, "A logic nanotechnology featuring strained-silicon," IEEE Electron Device Lett., vol. 25, no. 4, pp. 191–193, 2004.

[140] S. E. Thompson, M. Armstrong, C. Auth, M. Alavi, M. Buehler, R. Chau, S. Cea, T. Ghani, G. Glass, T. Hoffman, C. H. Jan, C. Kenyon, J. Klaus, K. Kuhn, Z. Ma, B. McIntyre, K. Mistry, A. Murthy, B. Obradovic, R. Nagisetty, P. Nguyen, S. Sivakumar, R. Shaheed, L. Shifren, B. Tufts, S. Tyagi, M. Bohr, and Y. El-Mansy, "A 90-nm logic technology featuring strained-silicon," IEEE Trans. Electron Devices, vol. 51, no. 11, pp. 1790–1797, 2004.

[141] J. S. Lim, S. E. Thompson, and J. G. Fossum, "Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs," IEEE Electron Device Lett., vol. 25, no. 11, pp. 731–733, 2004.

[142] C. H. Jan, N. Anand, C. Allen, J. Bielefeld, M. Buehler, V. Chikamane, K. Fischer, K. Jain, J. Jeong, S. Klopcec, T. Marieb, B. Miner, P. Nguyen, A. Schmitz, M. Nashner, T. Scherban, B. Schroeder, C. Ward, R. Wu, K. Zawadzki, S. Thompson, and M. Bohr, "A 90nm high volume manufacturing logic technology featuring Cu metallization and CDO low-k ILD interconnects on 300 mm wafers," in Proceedings of the IEEE 2004 International Interconnect Technology Conference (IEEE Cat. No.04TH8729), 2004, pp. 205–207.

[143] S. E. Thompson, G. Sun, K. Wu, J. Lim, and T. Nishida, "Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs," in IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004., 2004, pp. 221–224.

[144] K. Mistry, M. Armstrong, C. Auth, S. Cea, T. Coan, T. Ghani, T. Hoffmann, A. Murthy, J. Sandford, R. Shaheed, K. Zawadzki, K. Zhang, S. Thompson, and M. Bohr, "Delaying forever: Uniaxial strained silicon transistors in a 90nm CMOS technology," in Digest of Technical Papers. 2004 Symposium on VLSI Technology, 2004., 2004, pp. 50–51.

[145] Scott. E. Thompson et. al., "Nitrogen Controlled Growth of Dislocations Loop In Stress Enhanced Transistors," US 2004/0191975 A1, 2004.

[146] S. E. Thompson, M. Armstrong, C. Auth, M. Alavi, M. Buehler, R. Chau, S. Cea, T. Ghani, G. Glass, T. Hoffman, C. H. Jan, C. Kenyon, J. Klaus, K. Kuhn, Z. Ma, B. McIntyre, K. Mistry, A. Murthy, B. Obradovic, R. Nagisetty, P. Nguyen, S. Sivakumar, R. Shaheed, L. Shifren, B. Tufts, S. Tyagi, M. Bohr, and Y. El-Mansy, "A 90-nm logic technology featuring strained-silicon," IEEE Trans. Electron Devices, vol. 51, no. 11, pp. 1790–1797, 2004.

[147] S. E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Z. Ma, B. McIntyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. El-Mansy, "A logic nanotechnology featuring strained-silicon," IEEE Electron Device Lett., vol. 25, no. 4, pp. 191–193, 2004.

[148] J. S. Lim, S. E. Thompson, and J. G. Fossum, "Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs," IEEE Electron Device Lett., vol. 25, no. 11, pp. 731–733, 2004.

[149] Scott. E. Thompson et. al., "Nitrogen Controlled Growth of Dislocations Loop In Stress Enhanced Transistors." 2004.

[150] K. Zhang, U. Bhattacharya, L. Ma, Y. Ng, B. Zheng, M. Bohr, and S. Thompson, "A fully synchronized, pipelined, and re-configurable 50 Mb SRAM on 90 nm CMOS technology for

logic applications,” in 2003 Symposium on VLSI Circuits. Digest of Technical Papers (IEEE Cat. No.03CH37408), 2003, pp. 253–254.

[151] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, “A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors,” in IEEE International Electron Devices Meeting 2003, 2003, p. 11.6.1-11.6.3.

[152] S. E. Thompson et. al., “Structure and Process Flow For Fabrication of Dual Gate Floating Body Integrated MOS Transistors,” US 6,624,032 B2, 2003.

[153] S. E. Thompson et. al., “Structure and Process Flow For Fabrication of Dual Gate Floating Body Integrated MOS Transistors.” 2003.

[154] S. Vangal, M. A. Anders, N. Borkar, E. Seligman, V. Govindarajulu, V. Erraguntla, H. Wilson, A. Pangal, V. Veeramachaneni, J. W. Tschanz, Y. Ye, D. Somasekhar, B. A. Bloechel, G. E. Dermer, R. K. Krishnamurthy, K. Soumyanath, S. Mathew, S. G. Narendra, M. R. Stan, S. Thompson, V. De, and S. Borkar, “5-GHz 32-bit integer execution core in 130-nm dual-V/sub T/ CMOS,” IEEE J. Solid-State Circuits, vol. 37, no. 11, pp. 1421–1432, Nov. 2002.

[155] M. Anders, S. Mathew, B. Bloechel, S. Thompson, R. Krishnamurthy, K. Soumyanath, and S. Borkar, “A 6.5GHz 130nm single-ended dynamic ALU and instruction scheduler loop,” in 2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.02CH37315), 2002, vol. 2, pp. 332–534.

[156] M. Anders, S. Mathew, B. Bloechel, S. Thompson, R. Krishnamurthy, K. Soumyanath, and S. Borkar, “A 6.5 GHz 130 nm single-ended dynamic ALU and instruction-scheduler loop,” in 2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.02CH37315), 2002, vol. 1, pp. 410–477.

[157] S. Vangal, N. Borkar, E. Seligman, V. Govindarajulu, V. Erraguntla, H. Wilson, A. Pangal, V. Veeramachaneni, M. Anders, J. Tschanz, Y. Ye, D. Somasekhar, B. Bloechel, G. Dermer, R. Krishnamurthy, S. Narendra, M. Stan, S. Thompson, V. De, and S. Borkar, “5GHz 32b integer-execution core in 130nm dual-V/sub T/ CMOS,” in 2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.02CH37315), 2002, vol. 2, pp. 334–535.

[158] S. Vangal, N. Borkar, E. Seligman, V. Govindarajulu, V. Erraguntla, H. Wilson, A. Pangal, V. Veeramachaneni, M. Anders, J. Tschanz, Y. Ye, D. Somasekhar, B. Bloechel, G. Dermer, R. Krishnamurthy, S. Narendra, M. Stan, S. Thompson, V. De, and S. Borkar, “A 25 GHz 32 b integer-execution core in 130 nm dual-V/sub T/ CMOS,” in 2002 IEEE International Solid-State Circuits Conference. Digest of Technical Papers (Cat. No.02CH37315), 2002, vol. 1, pp. 412–478.

[159] S. E. Thompson et. al., “CMOS Fabrication Process Utilizing Special Transistor Orientation,” US 2002/0063292 A1, 2002.

[160] T. Ghani, K. Mistry, P. Packan, M. Armstrong, S. Thompson, S. Tyagi, and M. Bohr, “Asymmetric source/drain extension transistor structure for high performance sub-50 nm gate length CMOS devices,” in 2001 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.01 CH37184), 2001, pp. 17–18.

[161] S. Thompson, M. Alavi, R. Arghavani, A. Brand, R. Bigwood, J. Brandenburg, B. Crew,

- V. Dubin, M. Hussein, P. Jacob, C. Kenyon, E. Lee, B. McIntyre, Z. Ma, P. Moon, P. Nguyen, M. Prince, R. Schweinfurth, S. Sivakumar, P. Smith, M. Stettler, S. Tyagi, M. Wei, J. Xu, S. Yang, and M. Bohr, "An enhanced 130 nm generation logic technology featuring 60 nm transistors optimized for high performance and low power at 0.7 - 1.4 V," in International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224), 2001, p. 11.6.1-11.6.4.
- [162] Scott. E. Thompson et. al., "Method Of Fabricating A Supply Decoupling Capacitor," US 2001/0009785 A1, 2001.
- [163] S. E. Thompson et. al., "Integrated Circuit With Borderless Contacts," US 6,228,777 B1, 2001.
- [164] K. Mistry, T. Ghani, M. Armstrong, S. Tyagi, P. Packan, S. Thompson, S. Yu, and M. Bohr, "Scalability revisited: 100 nm PD-SOI transistors and implications for 50 nm devices," in 2000 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.00CH37104), 2000, pp. 204–205.
- [165] S. Tyagi, M. Alavi, R. Bigwood, T. Bramblett, J. Brandenburg, W. Chen, B. Crew, M. Hussein, P. Jacob, C. Kenyon, C. Lo, B. McIntyre, Z. Ma, P. Moon, P. Nguyen, L. Rumaner, R. Schweinfurth, S. Sivakumar, M. Stettler, S. Thompson, B. Tufts, J. Xu, S. Yang, and M. Bohr, "A 130 nm generation logic technology featuring 70 nm transistors, dual Vt transistors and 6 layers of Cu interconnects," in International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138), 2000, pp. 567–570.
- [166] T. Ghani, K. Mistry, P. Packan, S. Thompson, M. Stettler, S. Tyagi, and M. Bohr, "Scaling challenges and device design requirements for high performance sub-50 nm gate length planar CMOS transistors," in 2000 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.00CH37104), 2000, pp. 174–175.
- [167] S. E. Thompson et. al., "Channel Dopant Implantation With Automatic Compensation For Variation in Critical Dimensions," US 6,020,244, 2000.
- [168] S. E. Thompson et. al., "Process For Forming Doped Regions From Solid Phase Diffusion Source," US 5,877,072, 1999.
- [169] S. E. Thompson et. al., "Low Damage Doping Technique For Self-Aligned Source And Drain Regions," US 5,976,939, 1999.
- [170] S. E. Thompson et. al., "Two Step Source/Drain Anneal To Prevent Dopant Evaporation," US 5,874,344, 1999.
- [171] S. Thompson, P. Packan, T. Ghani, M. Stettler, M. Alavi, I. Post, S. Tyagi, S. Ahmed, S. Yang, and M. Bohr, "Source/drain extension scaling for 0.1 μm and below channel length MOSFETs," in 1998 Symposium on VLSI Technology Digest of Technical Papers (Cat. No.98CH36216), 1998, pp. 132–133.
- [172] P. Packan, S. Thompson, E. Andideh, S. Yu, T. Ghani, M. Giles, J. Sandford, and M. Bohr, "Modeling solid source boron diffusion for advanced transistor applications," in International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217), 1998, pp. 505–508.
- [173] Thompson, Young, Greason, and Bohr, "Dual Threshold Voltages And Substrate Bias: Keys To High Performance, Low Power, 0.1 μm Logic Designs," in Symposium on VLSI Technology, 1997, pp. 69–70.
- [174] P. Packan, H. Kennel, S. Thompson, S. Corcoran, and M. Taylor, "Understanding implant

damage by implant channeling profile measurements,” in Proceedings of 11th International Conference on Ion Implantation Technology, 1996, pp. 539–542.

[175] S. E. Thompson, P. A. Packan, and M. T. Bohr, “Linear versus saturated drive current: tradeoffs in super steep retrograde well engineering,” in 1996 Symposium on VLSI Technology. Digest of Technical Papers, 1996, pp. 154–155.

[176] M. Bohr, S. S. Ahmed, S. U. Ahmed, M. Bost, T. Ghani, J. Greason, R. Hainsey, C. Jan, P. Packan, S. Sivakumar, S. Thompson, J. Tsai, and S. Yang, “A high performance 0.25 μm logic technology optimized for 1.8 V operation,” in International Electron Devices Meeting. Technical Digest, 1996, pp. 847–850.

[177] M. Bohr, S. U. Ahmed, L. Brigham, R. Chau, R. Gasser, R. Green, W. Hargrove, E. Lee, R. Natter, S. Thompson, K. Weldon, and S. Yang, “A high performance 0.35 μm logic technology for 3.3 V and 2.5 V operation,” in Proceedings of 1994 IEEE International Electron Devices Meeting, 1994, pp. 273–276.

[178] T. Nishida, S. E. Thompson, J. T. Kavalieros, Y. Lu, and M. K. Han, “Characterization of ULSI gate oxide reliability using substrate and channel electron injection stresses,” in Proceedings Ninth Biennial University/Government/Industry Microelectronics Symposium, 1991, pp. 84–88.

[179] T. Nishida and S. E. Thompson, “Oxide field and temperature dependences of gate oxide degradation by substrate hot electron injection,” in 29th Annual Proceedings Reliability Physics 1991, 1991, pp. 310–315.

[180] S. E. Thompson and F. A. Lindholm, “Influence of heavily doped contacts on photoconductive switch properties,” IEEE Trans. Electron Devices, vol. 37, no. 12, pp. 2542–2553, 1990.

[181] *Strain Effects in Semiconductors: Theory and Device Applications*, S. Yongke, S.E. Thompson, and T. Nishida, Springer US, ISBN 978-1-4419-0551-2