

# Electronics

## Circuits and Analysis

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Alpha  
Science

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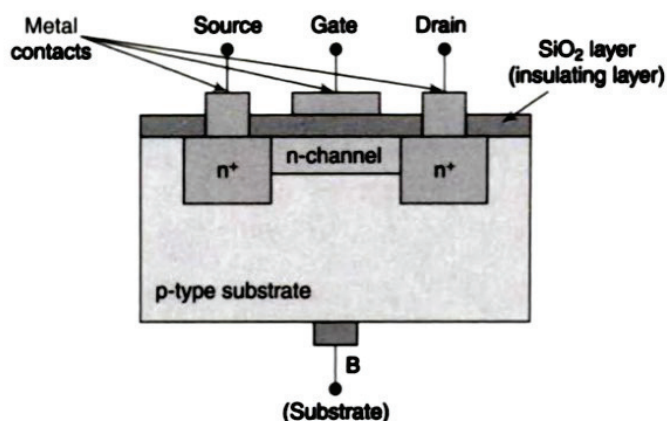


**Fig. 9.10** Basic structure of an n-channel depletion MOSFET. Note the presence of insulating  $\text{SiO}_2$  layer between gate and channel.

An n-channel depletion MOSFET is normally operated with a positive voltage between drain and source terminals. The substrate is usually internally connected to source. The voltage between the gate and source,  $V_{GS}$ , can be positive, zero or negative. This is **another distinction with JFET** where  $V_{GS}$  is negative for n-channel JFET and positive for p-channel JFET. Figure 9.11(a) shows device with negative  $V_{GS}$ . Initially let us assume  $V_{GS} = 0$  V. If  $V_{DS}$  is increased from zero volt, the drain current increases and follows ohms law [Eq. (9.5)] till  $V_{DS}$  is sufficient to pinch-off the channel (in the manner it happens in n-channel JFET at a voltage  $|V_p|$ ). Increasing  $V_{DS}$  beyond  $|V_p|$  does not increase the drain current significantly. The drain current then is a weak function of  $V_{DS}$  and the slop of  $I_D$  versus  $V_{DS}$  curves is finite for  $V_{DS} > |V_p|$ . The region beyond pinch off is called '**saturation region**'. The drain current at  $V_{DS} = |V_p|$  with  $V_{GS} = 0$  is termed as drain-to-source saturation current  $I_{DSS}$ .

When gate is negative with respect to source through voltage  $V_{GS}$ , the field produced induces positive charges in the channel. The process of induction of positive charges in n-channel through the insulating layer is schematically shown in Figure 9.11(a).

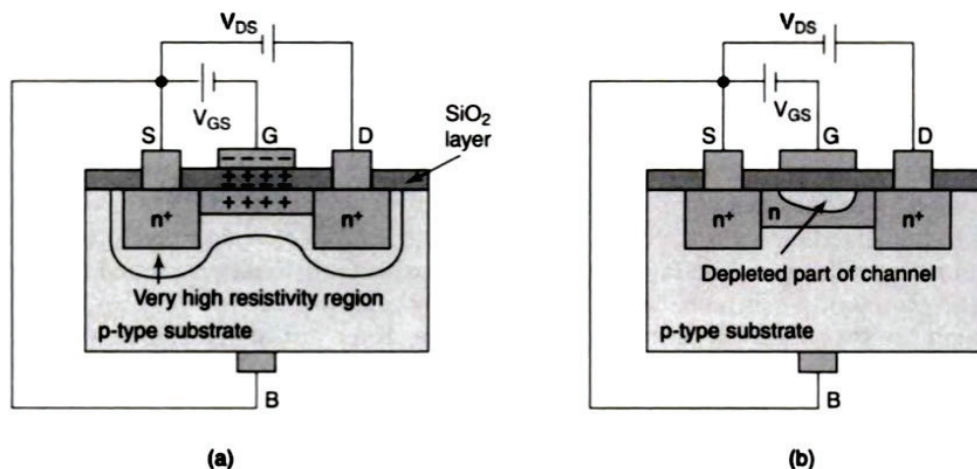


**Fig. 9.11** (a) A negative  $V_{GS}$  induced positive charges in the n-channel. (b) Depletion of channel as a result of induced charges due to negative  $V_{GS}$ .

Some of the electrons in the channel recombine with the induced positive charges and are lost, thus a depletion region is created below the oxide layer as shown in [Figure 9.11(b)]. As a result, the channel becomes narrower, its resistance increases due to loss of mobile electrons and the drain current falls. With more negative gate voltage the depletion region increases and finally the electrons can be virtually depleted and the channel eliminated altogether. The drain current drops to zero in that situation.

The least negative gate-source voltage,  $V_{GS}$ , which completely depletes the majority carriers from the channel, is called the 'threshold voltage  $V_T$ ' (same as pinched off voltage  $V_p$  for JFET). The channel is pinched off along its entire length when negative  $V_{GS}$  is equal to or more than  $V_T$ . The drain current is then zero for all values of  $V_{DS}$ . For negative  $V_{GS}$  values between zero and  $V_T$ , the drain characteristics drawn in Figure 9.12 are similar to n-channel JFET.

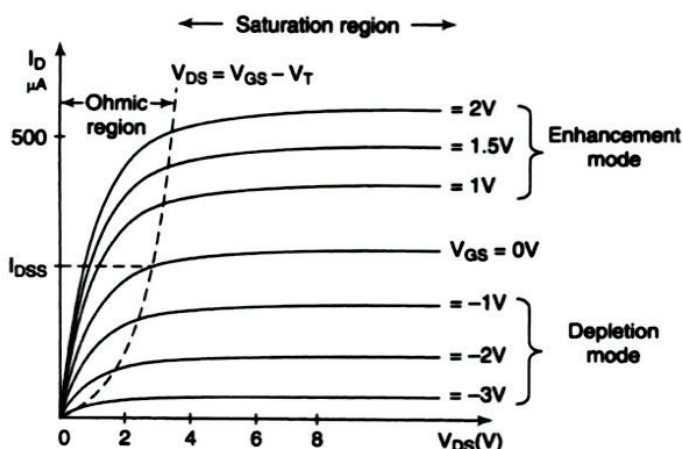


Fig. 9.12 Drain characteristics for n-channel depletion MOSFET, in enhancement and depletion modes.

The absence of a p-n junction between gate and channel region in a MOSFET allows a positive gate-source voltage for n-channel depletion MOSFET. A positive  $V_{GS}$  produces field that induces more mobile negative charges (electrons) into the channel. This enhances the conductivity of the channel and increases drain current. With  $V_{GS}$  positive, the transistor is said to be operating in the 'enhancement mode'. A depletion-MOSFET, therefore, can be operated either in enhancement mode or depletion mode and it is called enhancement-depletion MOSFET.

### The Drain and Transfer Characteristics of Depletion MOSFET

Figure 9.12 shows complete drain characteristics with all possible values of gate-source voltage  $V_{GS}$  for n-depletion MOSFET.

These characteristics can be divided into three regions:

- (a) ohmic region,
- (b) saturation region, and
- (c) cutoff region

### Ohmic Region

In the ohmic region, the drain-source voltage is small but insufficient to pinch-off the channel. The drain current varies linearly with  $V_{DS}$  and can be expressed as,

$$I_D = K [2(V_{GS} - V_T)V_{DS} - V_{DS}^2] \text{ for } 0 < V_{DS} \leq (V_{GS} - V_T) \quad (9.8)$$

For small values of  $V_{DS}$  i.e.  $V_{DS} \ll |V_T|$ , above equation is reduced to,

$$I_D = K [2(V_{GS} - V_T) V_{DS}] \quad (9.9)$$

Where, 
$$K = \frac{I_{DSS}}{V_T^2} \quad (9.10)$$

Equation (9.9) gives drain current  $I_D$  to be proportional to voltage  $V_{DS}$  as observed experimentally.

### Saturation Region

In saturation region,  $V_{DS} \geq (V_{GS} - V_T)$ . The drain current is constant and independent of  $V_{DS}$ . Substituting  $V_{DS}$  by  $V_{GS} - V_T$  in Eq.(9.9) gives  $I_D$  as,

$$I_D = K(V_{GS} - V_T)^2 \quad (9.11)$$

which represents transfer characteristics shown in Figure 9.13(a) for n-depletion MOSFET. For p-depletion MOSFET (since  $V_T$  is positive), the transfer characteristics are plotted in Figure 9.13(b).

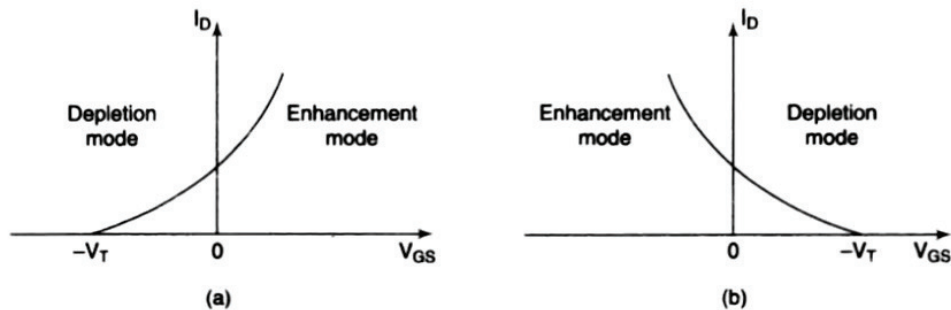


**Fig. 9.13** (a) Transfer characteristics of n-channel depletion MOSFET. (b) Transfer characteristics of p-channel depletion MOSFET.

The boundary between the ohmic and saturation regions is the locus of pinch-off points and can be obtained from the condition  $V_{DS} \geq (V_{GS} - V_T)$  in the limit,

$$V_{DS} = (V_{GS} - V_T) \quad (9.12)$$

or,

$$V_{GS} = (V_{DS} + V_T)$$

which on substitution in Eq. (9.11) results in,

$$I_D = K(V_{DS} + V_T - V_T)^2 \quad (9.13)$$

or,

$$I_D = K V_{DS}^2$$

Equation (9.13) is the equation of a parabola and defines the pinch-off locus.

### Cut off Region

In the cutoff region,  $V_{GS} < V_T$  for n-channel and  $V_{GS} > V_T$  for p-channel depletion MOSFET. Under this condition, the channel is totally depleted and the drain current is reduced to zero, the MOSFET is off.

The circuit symbols for n-channel depletion MOSFETs are shown in Figure 9.14. A separated gate terminal with rest of the symbol may be noted. The abbreviated symbol shown in Figure 9.14(b) is commonly used.

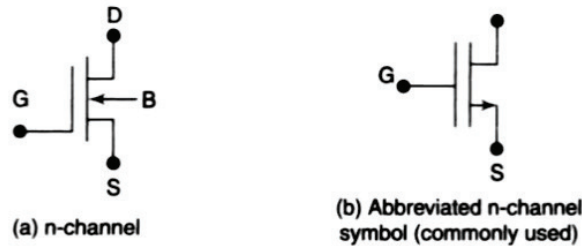


Fig. 9.14 Circuit symbol for n-channel depletion MOSFET.

The p-channel depletion MOSFET is fabricated on n-type substrate. A p-channel is formed between heavily doped p-type drain and source and the conduction in the channel is by holes.

The drain characteristics for p-channel depletion MOSFET are similar to n-channel with a difference that depletion mode needs positive  $V_{GS}$  and enhancement mode needs negative  $V_{GS}$ . The circuit symbol for p-channel depletion MOSFETs are shown in Figure 9.15. Since the mobility of electrons is higher by a factor of 2 or more as compared to mobility of holes, n-channel MOSFETs are faster and perform satisfactorily up to higher frequency.

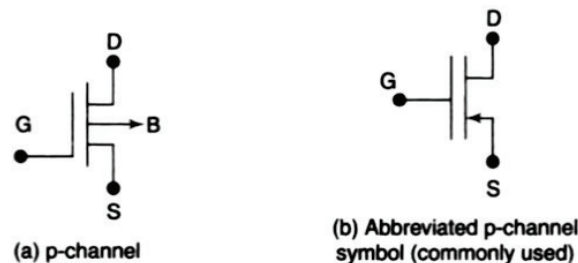


Fig. 9.15 Circuit symbol for p-channel depletion MOSFET.

### The Enhancement MOSFET

The structure of n-channel enhancement MOSFET is shown in Figure 9.16. The device construction is similar to that of depletion MOSFET except that the n-channel is not implanted or formed by doping. The n-channel between the drain and source, in fact is physically absent in enhancement MOSFET. The channel is created through charges induced by the field established by gate voltage in the manner described below.

Figure 9.17 shows enhancement MOSFET where the source and substrate are shorted together and grounded and the drain-to-source voltage  $V_{DS}$  is set to zero. The metal gate and p-semiconductor with insulator oxide layer between them in channel region form a parallel –

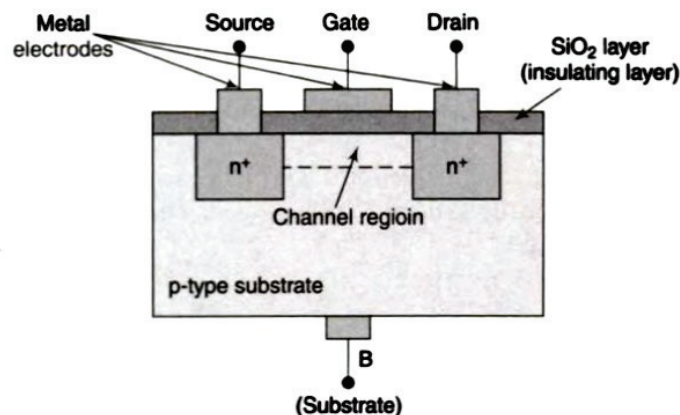


Fig. 9.16 Structure of n-channel enhancement MOSFET.

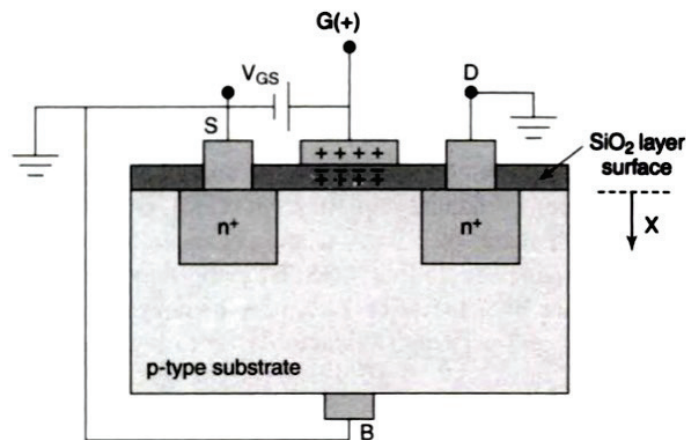


Fig. 9.17 The field due to  $V_{GS}$  pushes holes away from the channel region beneath oxide layer in enhancement MOSFET.

plate capacitor. It can then be visualized that a positive gate voltage establishes an electric field through the oxide layer that repels holes from channel region. The hole density in the channel area falls, (say by 10%) over the equilibrium value in p-substrate as shown in Figure 9.18 (a) and thus depletion region is formed. The electron concentration  $n_0$  increases near the surface according to the relation  $p_0 \cdot n_0 = n_i^2$  (discussed in Chapter 1). Further increase in gate-source voltage induces more electrons in the channel region. When applied  $V_{GS}$  is more than a particular value  $V_T$ , these mobile electrons are sufficient in number to form an inversion layer just below the oxide layer shown in Figure 9.18(b). The layer at the semiconductor-oxide interface is rich in electrons and it is in p-semiconductor (substrate) region—in other words, the p-layer (originally rich in holes) is converted into an n-layer (now rich in electrons). So, it is called 'inversion layer'. The inversion layer is formed only when  $V_{GS}$  exceeds a threshold value  $V_T$ . The charges thus induced constitute an n-channel just below the oxide layer (Figure 9.19). If the gate voltage is increased beyond  $V_T$ , more charges are induced in the channel. This way conductivity of channel increases. A current flows through the induced channel on application of a positive potential between drain and source.

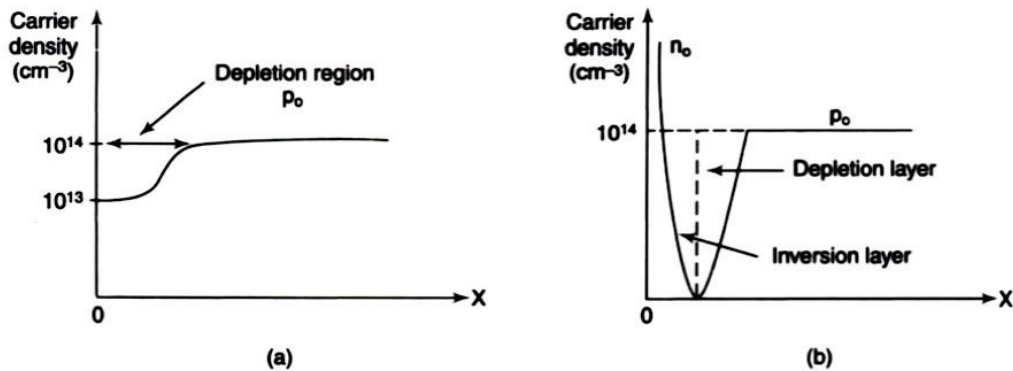


**Fig. 9.18** (a) Formation of a depletion region due to fall in hole density. (b) Formation of inversion layer when  $V_{GS} = V_T$ .

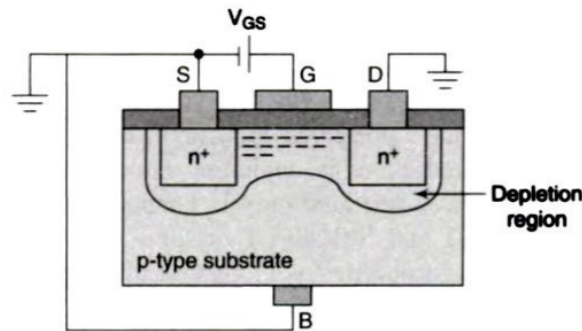


**Fig. 9.19** Induced charges (electrons here) form an n-channel when  $V_{GS} > V_T$ .

The positive gate voltage enhances the induced charges and thus the drain current increases and therefore this device is called **enhancement MOSFET**.

The channel in an enhancement MOSFET, in general, extends 30 to 300 angstroms into the silicon from oxide-silicon interface. And the conduction occurs primarily due to the drift under the electric field produced by drain-source voltage  $V_{DS}$ .

We now investigate the variation of drain current with positive drain-source voltage  $V_{DS}$ . For gate-source voltage smaller than the threshold voltage  $V_T$  i.e.  $V_{GS} < V_T$ , there is no channel formation and no drain current is expected to flow in the device, that is  $I_D = 0$  for all practical values of  $V_{DS}$ . With  $V_{GS} > V_T$ , for small values of  $V_{DS}$  i.e.  $V_{DS} < (V_{GS} - V_T)$ , the drain current varies linearly in proportion to  $V_{DS}$ . And the device is operating in the **ohmic region**. As  $V_{DS}$  increases further, the effective voltage between gate and drain  $V_{GD} (= V_{GS} - V_{DS})$  becomes smaller. The electric field at the drain end is reduced and the channel gets narrowed down near the drain region (Fig. 9.20), as a consequence the channel resistance begins to rise and the drain current begins to level off. At the value of  $V_{DS}$  such that  $V_{GD} \approx V_T$ , the channel is almost reduced to zero at the drain end (thus a kind of pinch off situation arises) and no significant change in drain current occurs with higher values of  $V_{DS}$ . The device is then operating in the **saturation region**. The saturation, of course depends on the gate - source voltage  $V_{GS}$  beyond  $V_T$  and higher values of  $V_{GS}$  result in increasing saturation values of  $I_D$ .