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1Giga Bit SOI DRAM with Fully Bulk Compatible Process and Body-Contacted SOI MOSFET Structure

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Abstract

1G Bit SOI DRAM with body-contacted (BC) SOI MOSFET structure is successfully realized for the first time. The fabricated 1G SOI DRAM has fully compatible process with 0.17 μm bulk CMOS technology except for the isolation process. The key advantage of BC-SOI MOSFET is free from floating-body effect, since the body-potential increase can be suppressed by the well contact through the remaining thin-silicon film beneath the field oxide. The BC-SOI structure has several advantages, such as relatively high isolation punchthrough voltage, high drain-to-source breakdown voltage compared with conventional thin-film SOI MOSFET and small junction capacitance compared with bulk MOSFET, resulting in high-speed circuit operation.

Introduction

Recently, DRAM chip using an SOI (silicon-on-insulator) wafer is widely acknowledged because of its inherent high-speed, low-power characteristics, where improvement of circuit speed resulting from small junction characteristics is the most remarkable feature of SOI MOSFET (1). In general, conventional SOI MOSFETs have active area isolated entirely by field oxide, in which the field oxide is in touch with the buried oxide. This structure may lead to latch-up-free devices and leakage-free field transistors, but cannot avoid the floating-body effect, the most serious problem in conventional SOI MOSFETs. It is well known that the floating-body effect is responsible for a small drain-to-source breakdown voltage (BV_{dss}) (2), a body potential instability (3), and a dynamic retention time problem (4). Although various body-fixed structures have been proposed and implemented to overcome the floating-body effect (5)-(8), most of them require additional mask layout and/or process steps.

In order to suppress the floating-body effect, we proposed a body-contacted SOI (BC-SOI) MOSFET structure (9). With

no additional mask layout and/or process steps in (5)-(8), BC-SOI MOSFETs can be implemented by mask layouts and process steps completely compatible with bulk MOSFETs. In the BC-SOI MOSFET structure, the field oxide does not consume silicon film completely; that is, there exists a thin silicon film between the field oxide and the buried oxide. Therefore, the increase of body potential can be successfully suppressed by a well contact through the remaining thin silicon film beneath the field oxide, so that kink effect and BV_{dss} characteristics can be dramatically improved. Using the BC-SOI structure, the world's first 1G bit SOI DRAM chip has been materialized.

In this paper, we present experimental results of fabricated BC-SOI MOSFETs, such as I-V characteristics, junction capacitance, gate delay time, breakdown voltage. In addition, some features of 1G bit SOI DRAM with 0.17 μm CMOS technology and fully bulk-compatible process are presented.

Cell Structure and Fabrication

Fig. 1 shows a cross-sectional illustration of BC-SOI MOSFET structure. The key process parameters to realize the BC-SOI MOSFET structure are SOI film thickness, field oxide thickness, and field-stop implantation condition; that is, the thickness of SOI film and field oxide are 200 nm and 250 nm, respectively, and the field stop implantation conditions are B¹¹, 50 keV, $5.0 \times 10^{12} / \text{cm}^2$ for nMOSFETs and P³¹, 150 keV, $1.0 \times 10^{13} / \text{cm}^2$ for pMOSFETs. LDD (Lightly-Doped Drain) structure is adopted for NMOSFETs to improve the short-channel effect, while PMOSFET has normal source/drain junction. A cross-sectional SEM photograph of SOI DRAM cell with BC-SOI MOSFET structure fabricated on SOI wafer with 40 nm buried oxide is shown in Fig. 2. It can be clearly observed that there exists a thin silicon film (about 75 nm) beneath the field oxide.

The lateral isolation is made by advanced LOCOS process with nitride spacer, as shown in Fig. 3. In the LOCOS process, about 10 nm silicon film is recessed to improve gate

oxide integrity. In order to isolate the word line from the bit line, the ultra small contact hole of $0.1\ \mu\text{m}$ is successfully defined by using a semi-self-aligned contact technology, as shown in Fig. 4. The cell capacitor has a cylindrical shape and conventional NO film with equivalent SiO_2 thickness of $4.3\ \text{nm}$ as a capacitor dielectric. The cell capacitance is about $15\ \text{fF} / \text{cell}$. Typical process features of 1G bit SOI DRAM are summarized in Table 1.

DRAM Cell Characteristics

Isolation punchthrough characteristics as a function of isolation spacing is shown in Fig. 5. It can be observed that when considering the supply voltage of $2.2\ \text{V}$, the punchthrough characteristics are safe up to the isolation spacing of $0.2\ \mu\text{m}$. Fig. 6 and 7 show the $I_{\text{DS}}\text{-}V_{\text{GS}}$ characteristics for peripheral and cell transistors with the BC-SOI MOSFET structure, respectively. It can be seen that BC-SOI MOSFETs have no current hump in the drain current characteristics (see the inset).

Fig. 8 shows threshold voltage dependence on a well bias for BC-SOI MOSFETs as compared with bulk counterpart. It should be noted that the threshold voltage of BC-SOI MOSFETs show the same trend as the bulk counterpart up to $-2\ \text{V}$ and that there is relatively small dependence in terms of the well pick-up distance. Fig. 9 shows the drain-to-source breakdown voltage as a function of gate length. Since the body-potential increase is suppressed by the well pick-up, BC-SOI MOSFETs show excellent BV_{DSS} characteristics as compared with conventional thin-film SOI MOSFETs. In terms of latch-up characteristics, BC-SOI MOSFETs are as good as bulk counterpart, as shown in Fig. 10.

As expected, BC-SOI MOSFET structure has a unique junction capacitance characteristics which decreases abruptly at certain junction voltage, as shown in Fig. 11. At certain junction voltage, which depends on the field-stop implantation condition, source/drain junction depletion region reaches the buried oxide so that junction capacitance abruptly decreases. As shown in Fig. 11, since junction capacitance varies with field-stop implantation condition, field oxide thickness and field-stop implantation condition should be optimized for better isolation and junction characteristics. This feature is an attractive point of BC-SOI MOSFET structure capable of high-speed operation. Fig. 12 shows gate-delay time with supply voltage for the ring oscillator with BC-SOI MOSFET structure as compared with conventional and bulk counterparts. BC-SOI MOSFETs have the gate delay characteristics superior to bulk devices due to unique junction capacitance mentioned above.

With nitride spacer LOCOS process, BC-SOI MOSFET structure, semi-self-aligned contact scheme, and $0.17\ \mu\text{m}$

CMOS technology, 1G bit SOI DRAM chip with chip size of $691\ \text{mm}^2$ has been fabricated and its photograph is shown in Fig. 13.

Conclusions

In conclusion, we have successfully fabricated 1G bit SOI DRAM with the BC-SOI MOSFET structure for the first time. The key feature in the BC-SOI MOSFET structure is immune to floating-body effect so that the body potential can be controlled by the well bias. It should be also noted that the 1G bit SOI DRAM fabrication process is fully compatible with the bulk-silicon counterpart.

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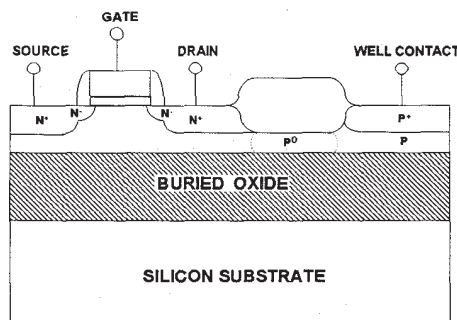


Fig. 1. A cross-sectional illustration of BC-SOI MOSFET structure.

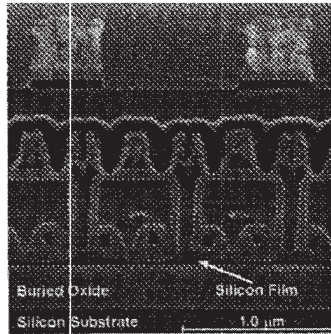
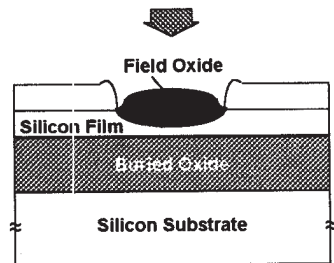
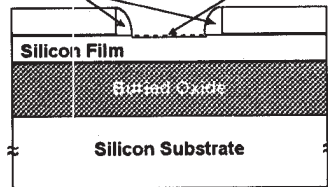
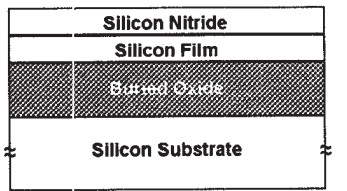
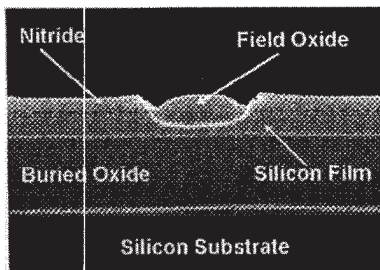


Fig. 2. A cross-sectional SEM photograph of fabricated SOI DRAM cell with BC-SOI MOSFET structure.



(a)



(b)

Fig. 3. Nitride spacer LOCOS process sequence (a) and cross-sectional SEM view (b).

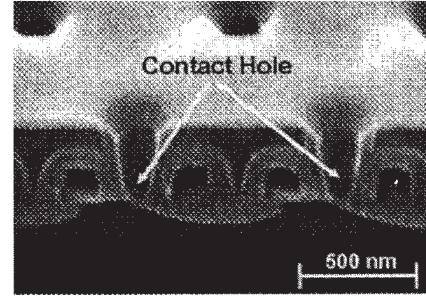


Fig. 4. A cross-sectional SEM photograph of contact hole with final contact size of 0.1 μm in diameter.

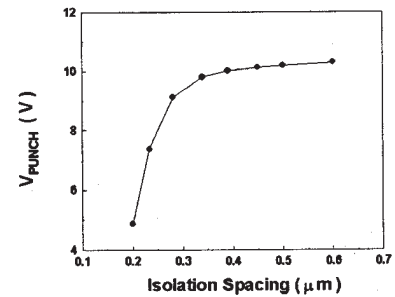
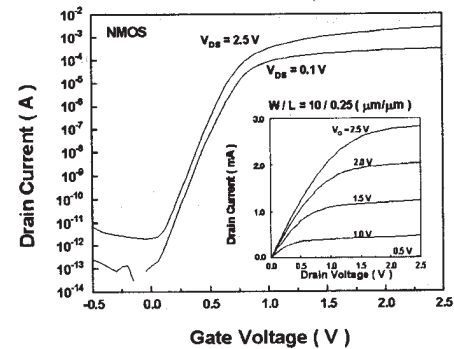
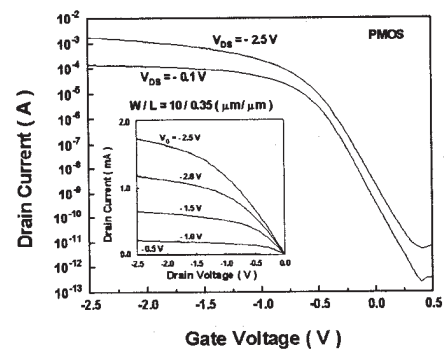


Fig. 5. Isolation punchthrough characteristics as a function of isolation spacing of BC-SOI MOSFET structure.



(a) NMOS Transistor



(b) PMOS Transistor

Fig. 6. $I_{DS} - V_{GS}$ characteristics for peripheral transistors with the BC-SOI MOSFET structure, (a) NMOS and (b) PMOS transistors, respectively.

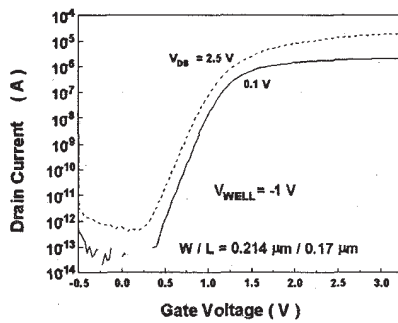


Fig. 7. I_{DS} - V_{GS} characteristics of cell transistor with the BC-SOI MOSFET structure.

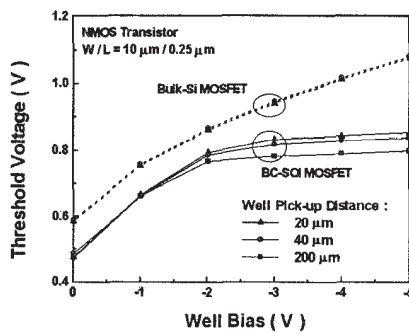


Fig. 8. Threshold voltage dependence on a well bias for BC-SOI MOSFET as compared with that of bulk-silicon MOSFET.

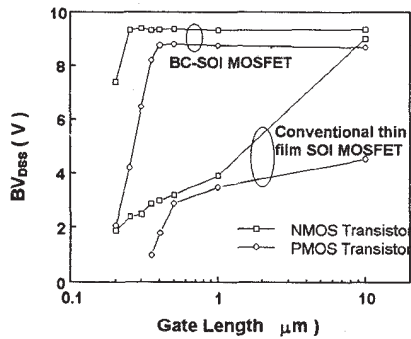


Fig. 9. Drain-to-source breakdown voltage (BV_{DSS}) as a function of gate length for BC-SOI transistors.

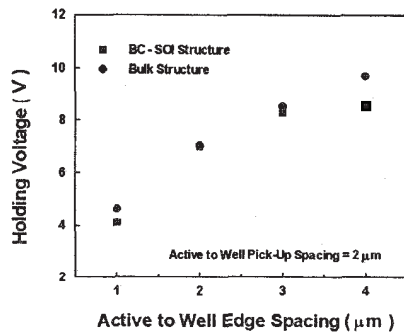


Fig. 10. Latch-up characteristics as a function of active-to-well edge spacing for BC-SOI and bulk MOSFET structure.

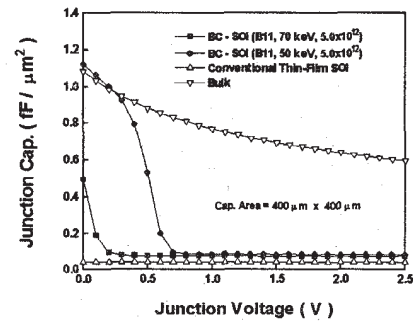


Fig. 11. A n^+ junction capacitance characteristics of BC-SOI MOSFET structure compared with that of bulk-silicon MOSFET.

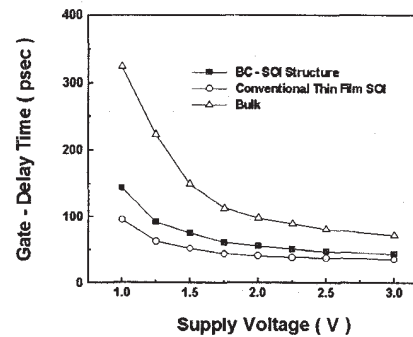


Fig. 12. Gate-delay time characteristics with supply voltage with field-stop implantation condition as a parameter with conventional and bulk counterparts.

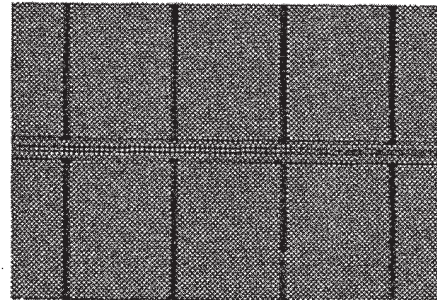


Fig. 13. A photograph of 1G bit SOI DRAM chip fabricated on a SOI wafer.

SOI Substrate	
Top Silicon Film	200 nm
Buried Oxide	400 nm
Dielectric Film	
Field Oxide	250 nm
Gate Oxide	6.0 nm
NO Layer (equivalent SiO_2)	4.3 nm
Cell Transistor	
Gate Length	0.17 μm
Peripheral Transistor	
Gate Length (NMOSFET)	0.25 μm
Gate Length (PMOSFET)	0.35 μm
Cell Capacitance	15 fF / cell
Cell Size	0.33 μm^2
Chip Size	691 mm ²
Power Supply Voltage	2.2 V

Table 1. Typical process and device features in fabricated 1G bit SOI DRAM.