

Impact of high-k gate stack material with metal gates on LF noise in n- and p-MOSFETs

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Abstract

The aim of this paper is to study the 1/f noise performance of n- and p-channel MOSFETs with different Hf-based gate stacks, deposited by MOCVD and using metal (PVD TaN) as a gate material. The drain current dependence is different for n- and p- channel devices over the noise spectra, showing different noise origin mechanisms – mobility fluctuations for pMOS and number fluctuations for nMOS. Asymmetric trap density distributions with energy between n- and pMOS have been observed which is a possible reason for the observed lower noise magnitude in pMOS devices. A fair comparison using Hooge's parameter and trap densities as figures of merit shows weak correlation on the Hf-composition, allowing a large window for gate stack processing of devices.

Keywords: LF noise, high-K, Hf silicates, metal gates, number fluctuations, mobility fluctuations

1. Introduction

High-k gate stacks have been proposed as substitutes for SiO₂, to meet the challenges arising from a continued downscaling of CMOS devices. In order to eliminate the poly-depletion and resistivity effects, metal gates as alternatives are being considered. Hf-based devices - Hf_xSi_{1-x}ON, where 0 < x < 1, are considered to be a promising choice [1]. For analog applications in the 45 nm node, which require lower leakage currents, the noise level is of

great importance [2]. We report here the low frequency (LF) noise performance of n- and p-channel MOSFETs with Hf_xSiO_{1-x}N gate oxide deposited by an Metal Organic Chemical Vapor Deposition (MOCVD) process and using Physical Vapor Deposition (PVD) TaN as gate material. The LF noise spectra are predominantly of the 1/f^γ type where γ ~ 1. Different dominant 1/f noise mechanisms have been noticed. While the pMOS devices rather follow mobility fluctuations (δμ) theory, number fluctuations (δn) were observed to

dominate for the nMOS devices. As figures of merit, Hooge's parameter and the effective oxide trap densities suggest a weak correlation with the Hf-composition. Also the noise magnitude in these Hf-based devices is seen to be higher by an order of magnitude when compared to SiON reference devices.

2. Experimental

The $1/f$ noise performance was investigated in $W/L = 10/1 \mu\text{m}$ n- and pMOSFET devices fabricated using a conventional CMOS process flow. A 0.8 nm thin interfacial chemical oxide layer was employed on top of which $\text{Hf}_x\text{Si}_{1-x}\text{ON}$ with various Hf-contents, where $x = 30\%$, 55% to 70% were deposited by MOCVD. PVD TaN was employed as metal gate. These devices were subjected to a post-deposition anneal in NH_3 at 800°C for 60 s. This was followed by a forming gas anneal (FGA) at 520°C for 20 min. As references, devices with 1.5 nm SiON gate dielectric have been processed. The Equivalent Oxide Thickness (EOT) of the $\text{Hf}_x\text{Si}_{1-x}\text{ON}$ devices is in the same range.

On-wafer noise measurements were performed in linear operation at a constant drain voltage $|V_{ds}|=0.05 \text{ V}$ for gate voltages $|V_{gs}|$ between 0.5 - 2 V, in steps of 50mV using BTA9812 noise analyzer hardware and NoisePro software from Cadence. A channel length of $1\mu\text{m}$ was chosen, to reduce the device-to-device scatter in the noise magnitude.

3. Results and discussion

As seen from Fig 1, the LF noise spectra of n- and p-MOSFETs for all high-k gate stack materials are predominantly of the $1/f^k$ type, with the frequency exponent close to 1, for $|V_{gs}-V_t| = 1 \text{ V}$, where V_t – threshold voltage. The noise spectra of p-devices for all different high-k gate stacks are 2 orders of magnitude lower when compared to their n-counterparts for the same gate voltage overdrive, but corresponding with a one decade smaller current (see Fig. 2).

In order to investigate the origin of the $1/f$ noise, the normalized noise spectral density S_{id}/I_d^2 dependence versus the drain current $|I_d|$ at a constant frequency $f=25\text{Hz}$ is studied as in Fig. 2 [3]. In case number (δn) fluctuations dominate, a leveling off in

weak inversion will be noticed and a roll-off with $1/I_d^k$ in strong inversion ($k \sim 1$) [3]. This is clearly seen in Fig. 2a for the nMOSFETs.

The p-channel devices, on the other hand, show an S_{id} that varies with $1/I_d$ in Fig. 2b, over the whole current range studied. This points to a mobility fluctuations ($\delta\mu$) origin for pMOS devices [3]. Moreover, no strong dependence on the Hf-content was found for the normalized noise of pMOSFETs in Fig. 2b.

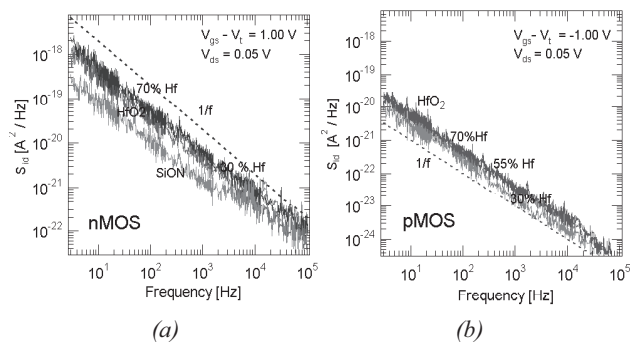


Fig 1. Drain current noise spectral density S_{id} versus frequency f for different high-k gate oxides of a) nMOS and b) pMOS.

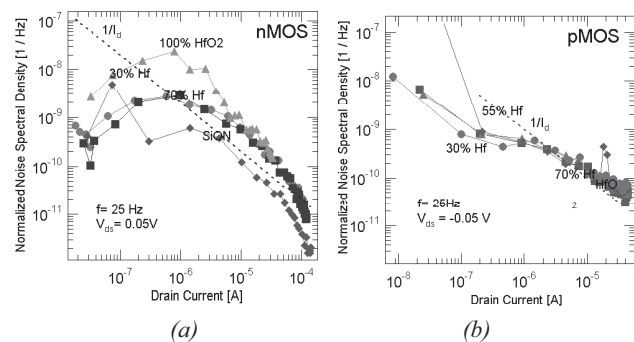


Fig 2. Normalized drain current noise spectral density S_{id}/I_d^2 versus drain current $|I_d|$ for different high-k gate oxides of a) nMOS and b) pMOS.

The input-referred noise ($S_{vg} = S_{id}/g_m^2$) at $f=25\text{Hz}$ is represented in Fig. 3. A pronounced dependence on the gate voltage overdrive ($V_{gs}-V_t$) for both n- and pMOS was observed with significant slope variations among the different high-k nMOS. Higher S_{vg} values are noticed for pure HfO_2 n-channel transistors while $\text{Hf}_x\text{Si}_{1-x}\text{ON}$ devices with $x = 30\%$,

55% and 70% give rise to values between the data for HfO_2 and reference SiON . The difference in noise magnitude among high-k materials is higher for nMOS, with Hf-silicates performing between HfO_2 and SiON . The differences in noise magnitude observed for pMOS with different high-k materials are within the measurement accuracy.

The parabolic increase of S_{vg} in strong inversion observed from Fig. 3 for nMOS shows that fluctuations are due to both carrier and correlated mobility fluctuations [3],[4]. For pMOS, the continuous increase of S_{vg} with $(V_{gs}-V_t)$ confirms the predominance of mobility fluctuations.

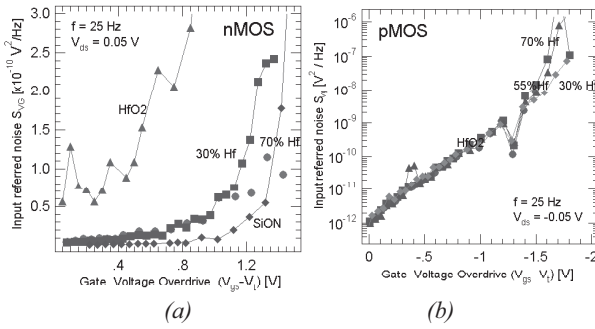


Fig 3. Input referred noise S_{vg} versus gate voltage overdrive $(V_{gs}-V_t)$ for different high-k gate oxides of (a) nMOS and (b) pMOS.

In order to calculate trap densities from the $1/f$ noise, a suitable value for the tunneling parameter (α) [5] is required which is calculated from the effective mass m_e^* and barrier height ϕ_b using the formula,

$$\alpha = \sqrt{(2 m_e^* \phi_b) / \hbar^2} \dots \dots \dots (1)$$

α is estimated to be $0.5 \times 10^8 \text{ cm}^{-1}$ for pure HfO_2 and 10^8 cm^{-1} for SiON . For $\text{Hf}_x\text{Si}_{1-x}\text{ON}$, α is assumed to vary linearly with x . The thus interpolated values are used in first approximation, as the presence of an interfacial layer (IL) has not been considered.

The effective volume trap density N_t and the surface density have been estimated as a figure of merit from S_{vg} using the formula

$$S_{vg} = (q^2 k T N_t) / (\alpha C_{EOT}^2 W L f) [4] \dots (2)$$

with q being the electron charge, C_{EOT} the gate oxide capacitance per unit area [$C_{EOT} = \epsilon_0 \epsilon_{ox} / EOT$], f the frequency and kT the thermal energy. The results are

plotted against the gate voltage overdrive in Fig 4a. The surface trap values (D_i) is estimated using the formula $(4kTzN_i)$, where z is the tunneling distance of an electron from the Si/IL (interfacial layer) interface at $f=1\text{Hz}$ [4].

From Fig. 4a, it follows that the values of volume and surface trap densities for the nMOS silicate ratios, are better than for pure HfO_2 for $V_{gs} \sim V_t$ though worse when compared with the SiON reference devices. In the case of pMOS (not shown), no major variation in trap values are observed among various high-k oxides while the magnitude is one decade lower than observed for nMOS. This is in line with the S_{id} spectra for the n- and pMOS transistors shown in Fig 1, where a two orders of lower noise spectral density was observed for pMOS.

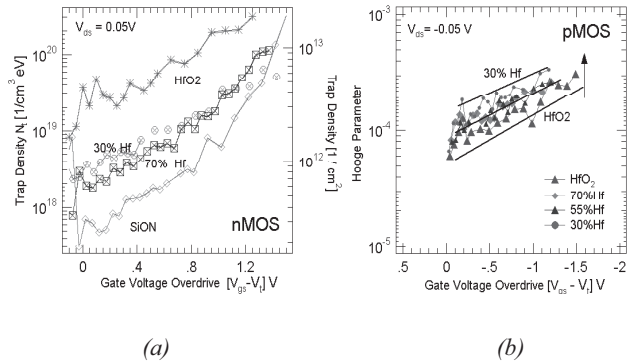


Fig 4a. Volume and surface trap density versus gate voltage overdrive $(V_{gs}-V_t)$ for different high-k gate oxides for nMOS. Fig 4b. Hoope's parameter versus gate voltage overdrive $|V_{gs}-V_t|$ for different high-k gate oxides for pMOS.

One possible reason is the energy distribution profile in the upper and the lower part of the bandgap for n- and pMOS devices, respectively, as shown in Fig 5 [6], [7] for the cases of $\text{Hf}_x\text{Si}_{1-x}\text{ON}$, where $x=30\%, 100\%$. The band gap distribution is calculated by estimating the tunneling distance z at $f=1\text{Hz}$ for the given device multiplied by the electric field E_{ox} at the Si/IL. Higher effective trap densities are noticed for nMOS than for pMOS in the mid energy gap region. Similar behavior was observed by Han *et al* [8] where an asymmetric spatial energy distribution causes higher mobility degradation in nMOS than pMOS, in poly-Si gated devices. We believe that the noise variation between nMOS and pMOS could be

due to the asymmetric distribution of traps along the energy mid-band gap.

As mobility fluctuations dominate the noise in pMOSFETs, the Hooge parameter (α_H) [9] is used as a metric for the noise performance, which is represented in Fig. 4b. As can be seen, it shows weak gate voltage dependence, confirming the $\delta\mu$ theory.

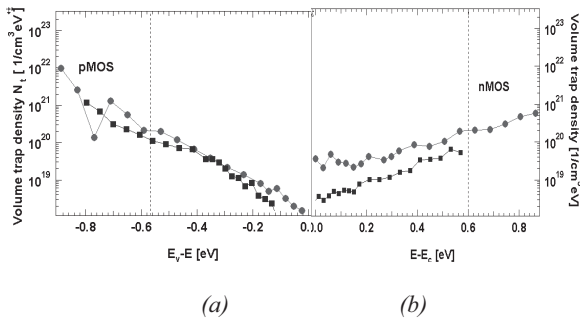


Fig 5. Spatial energy distribution of volume trap densities of (a) nMOS and (b) pMOS metal gate/Hf_xSi_{1-x}ON ($x=30,100\%$) devices across the Si energy band gap. Asymmetric profile distribution in the mid-band gap could cause variation in noise magnitude observed between nMOS and pMOS devices.

For a fair comparison between n- and pMOSFETs, the Hooge parameter is considered as a figure of merit for both cases. The resulting values are plotted in Fig. 6 as a function of the Hf-content for $|V_{gs}-V_t|=0.5$ V. The α_H values are fairly identical for both n- and pMOS. No strong dependence is observed with regard to the Hf-content, as the values are $\sim 10^{-4}$, although there is a tendency for the noise being higher around 30%. This stands in contrast with recent observations made in [10], where a one decade higher noise was found around 50 % Hf. Of course, the processing of the gate stacks is quite different in the two cases, which makes a direct comparison delicate.

4. Conclusions

In conclusion, for $V_{gs} > V_t$, the $1/f$ noise in p- and n-channel devices has a comparable performance. The drain current dependence is different for n- and p-channel devices pointing towards a different noise origin. An asymmetric energy distribution between n- and pMOS is observed which may be the reason for the observed lower noise magnitude in pMOS devices. From a noise point of view, the behavior of

MOCVD high-k insulating films shows no strong dependence on the gate stack composition, allowing a large processing window. In general, from the standpoint of gate stack optimization, noise is not a critical factor for metal gate devices with Hf-based high-k dielectrics, but is noticed to be higher by an order of magnitude when compared to SiON reference devices.

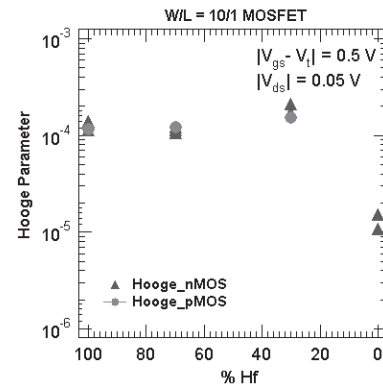


Fig 6. Hooge parameter versus %Hf for the high-k gate oxides for nMOS and pMOS with metal gate.

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