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# Current Mode Digital Gates for Mixed Mode Reprogrammable Integrated System\*

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**Abstract** - This paper presents some aspects of building reprogrammable system using current mode gates. With this approach it is possible to extend system on a chip solutions into the area of mixed mode applications. CMOS current mode gates consume almost constant current from the power supply and therefore are suitable for mixed mode operations. Contrary to voltage mode digital gates, presented in the paper current mode gates do not produce strong voltage and current fluctuations in the common substrate of the SoC. Paper shows three generations of current mode gates. It is described, in which way static noise margins were achieved in this technique, from the basic concept to the advanced design. Results of PSPICE simulations, based on BSIM3v3 models, are presented as well as a report of ASIC chip tests.

**Index terms** - reprogrammable, mixed analog-digital system, current mode gate, current mode logic, digital circuit, system on-a-chip

## I. INTRODUCTION.

Current progress in scaling down the main feature of integrated circuit which is the length of transistor gate make it possible to implement on a single chip a system. When starting to plan a system, designers often take into account classical, static voltage digital gates exclusively, even for mixed analog-digital systems. However, voltage-mode gates are not the best option for mixed mode circuits. Strong variation of currents as well as voltages during switching causes undesirable fluctuations of substrate voltage (called substrate noise), as well as additional varying voltage drops on power supply lines (dI/dt noise). It is not easy to avoid spreading of these fluctuations through the substrate (crosstalk) from the source of disturbances to a victim circuit. A victim can be an analog circuit, but also a digital circuit when its noise margins are crossed. From the analog circuit point of view fluctuations correlated with digital signal changes may be interpreted as a kind of noise, which limits achievable S/N ratio. Varying voltages in the substrate of classical digital circuit structure can make spurious state changes. To lower mentioned above disturbances one may use several physical level solutions. These are special guard rings, back plane contacts, silicon on insulator (SOI) processes, oxide vertical trenches, etc. Remedial approaches used to diminish substrate noise are signal frequency dependent, though. SOI-based process and a special back-plane contacts provide high isolation from

crosstalk at low operating frequencies, but their benefit is lost at high frequencies, while guard rings appear to be the technique best suited for crosstalk prevention at high operating frequencies. Furthermore SOI is an expensive technology and causes a problem known as the floating body effect. In [1] is shown that because of possible signal modulation it is not enough to assure low level of substrate noise in a frequency range consistent with operating frequency of the sensitive circuit. From the other hand guard rings take some extra area and therefore also increase costs. A method, which helps overcome such obstacles, is in fundamental circuit design methodology. This alternative approach, for minimizing substrate crosstalk, is based on the implementation of the digital part of a mixed system with the current mode gates. These gates draw almost constant, continuous current from power supply at a time of normal operation. Due to the nearly constant value of power supply current at different gate states (for example, logical "0" and "1"), the level of dI/dt noise is essentially lower in comparison with the classical voltage type gates. Substrate noise is also lowered, because of lower current and voltage variations in the structure of an individual gate [2]. Moreover, with current-mode gates several digital circuits were designed, which are characterized by lower hardware overheads (number of gates) in comparison with their prototypes constructed with classical voltage type gates [4, 5]. Note that physical and logical properties of the current-mode gates differ from corresponding properties of classical voltage-mode gates. Classical, static voltage CMOS inverter transfer characteristic is shown in Fig. 1.

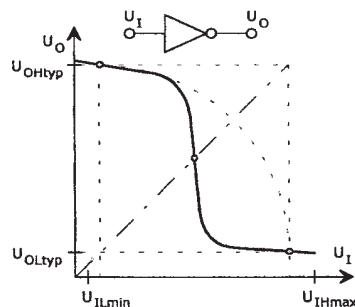


Fig. 1. Transfer characteristic of classical, static CMOS inverter

The shape of this characteristic aims to ideal for big widths of transistors, but even for relatively small transistor sizes the circuit have good enough noise

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margins for preventing mistaken interpreting of input signal levels. Generally, circuits with appropriate noise margins make it possible to regenerate typical output levels in a cascade of identical gates as shown graphically in Fig. 2. The more steep transfer characteristic, the less number of gates is needed to regenerate the typical signal levels from distorted ones.

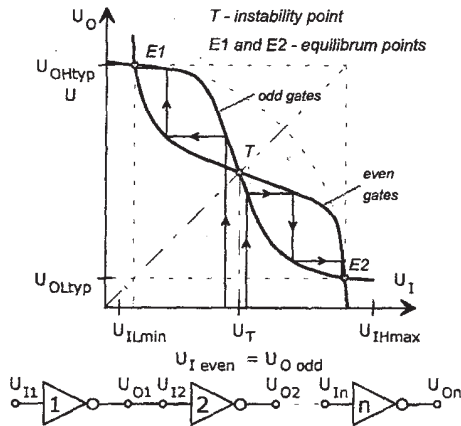


Fig. 2. Illustration of a process of digital signal regeneration to the typical values in a cascade of inverters

In the next sections it will be shown that it is possible to realize current mode digital circuits of the transfer characteristic comparable to voltage circuits one, maintaining low noise feature and additional ability to operate in a reprogrammable system.

## II. 1-ST GENERATION OF CURRENT-MODE GATE

In 1998 in [3] CMOS current mode digital gate with noise margins was presented for a world-wide audience, though preliminary works had been published since 1994. This gate was the starting point for current mode digital circuit research works at Technical University of Gdansk, Poland, which are continued at Technical University of Koszalin. The concept of this gate is shown in Fig. 3, and the graphical representation of current mode gate is shown in Fig. 4b. As one can see currents represent here logical signals. Current that flows into the input of the gate is considered as the input signal.

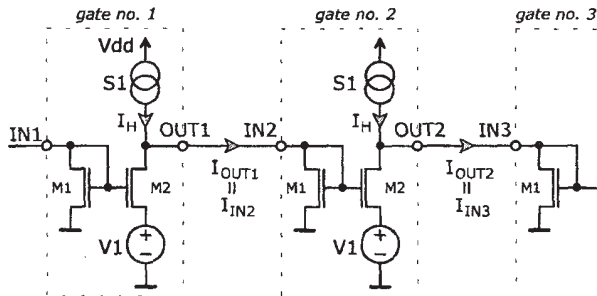


Fig. 3. Concept of the 1-st generation current mode gate

For instance consider the gate no. 2 from Fig. 3. It consists of two nMOS transistors (abbr. nMOSTs), a current source S1 and a voltage source V1. M1 and M2 form a current mirror. Assuming input current (of IN2) of zero value, a current, which flows out of the output

OUT2 has the value equal to  $I_H$ . Therefore,  $I_H$  is the maximal value of a current on the output of each gate. For the operation as the digital gate, similarly to voltage technique the transfer characteristic should be as the one presented in Fig. 4a. In such a case the output current  $I_{OUT2}$  is equal  $I_{OLtyp}$ , when the input current  $I_{IN2}$  approaching  $I_{IHmax}$ .

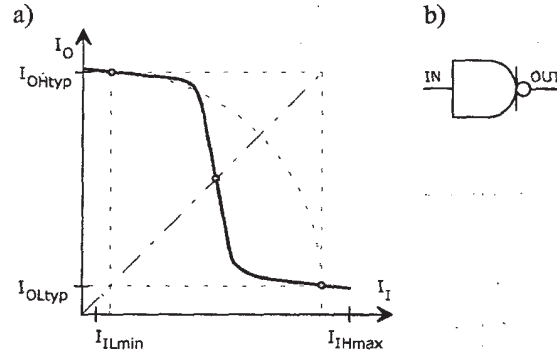


Fig. 4. Transfer characteristic of CMOS current mode gate (a) and the symbol of this gate (b)

Diode-like input stage of the gate allows current as well as voltage mode steering. M1 is able to conduct a current for the input voltage exceeding the threshold voltage of nMOST  $V_{thn}$ . When one neglects the body effect for simplicity, then one can state that transistor M2 starts to conduct a current for the gate voltage higher than resulting from the sum  $V + V_{thn}$ , where  $V$  is the value of the voltage source V1. The voltage  $V_{act}$  equal to this sum was named *an activation voltage*. In these conditions current mirror is set to the normal operation mode. The drain current of M2 is equal to  $I_H$  (and the output current equals 0), when two conditions are fulfilled:

- first – gate voltage of M2 should comply with the equation (1).

$$V_{g2} \geq V + V_{thn} + \sqrt{I_H / K_2} \quad (1)$$

$$\text{where } K_2 = \frac{K'}{2} (W_2 / L_2)$$

- second – lumped resistance of M2 and V1 should be much smaller than that of transistor M1 of the next gate (in the chain of gates).

These conditions are fulfilled by adequate choice of transistor sizes accordingly to the fixed value assigned to  $I_H$ .  $I_H$  represents a logical "1" in the current mode circuits family. The logical "0" is represented by the current  $I_L$  of the value near 0A. For presented here realizations  $I_H$  is set to 50  $\mu$ A, but it can also assume some other values,  $I_L$  typically achieves 1-5  $\mu$ A. CMOS realization of the gate from Fig. 3 is shown in Fig. 5a. The current source S1 is built with the transistor M4, the voltage source V1 is built with the transistor M3. For the CMOS technology AMS CYE 0.8  $\mu$ m transistor dimensions are as follows (in  $\mu$ m):  $W/L_{(M1)}=2/2$ ,  $W/L_{(M2)}=9/0.8$ ,  $W/L_{(M3)}=9/0.8$ ,  $W/L_{(M4)}=4/2$ .

One of the main differences between current mode and voltage mode gates is that a current mode gate has only one input, but it can have multiply output to provide replicas of output variables. Adding a next output to the symbol (see Fig. 5b) on the logical level corresponds to the circuit extension with the next 3 transistors of the output part (M2-4 with suffix 'b') to a gate as is shown in Fig. 5a. A second difference is that the simplest current mode gate is the inverter and the NOR gate at the same time. According to the Kirchhoff's current law, we have a sum of current signals on the input of the gate, to which more than one output of other gates is connected.

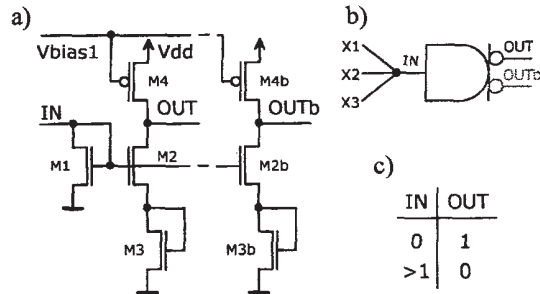


Fig. 5. CMOS realization of the 1-st generation of current mode gate (a), its symbolic representation (b), and the truth table showing possibility of NOR operation

Using BSIM 3v3 models for AMS CYE 0.8  $\mu\text{m}$  technology PSPICE simulations were executed. Resulting transfer characteristic is shown in Fig. 6

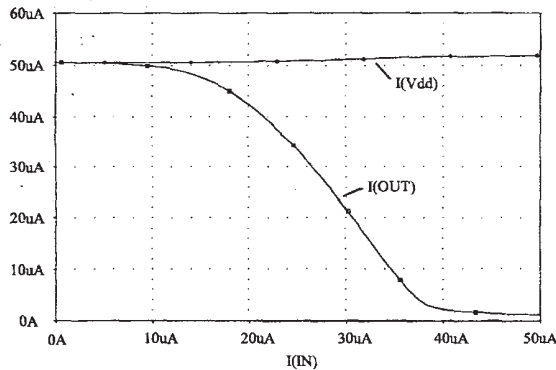


Fig. 6. Transfer characteristic and  $I(V_{dd})$  vs.  $I(IN)$  of the 1-st generation of current mode gate

### III. 2-ND GENERATION OF CURRENT GATES

To overcome some limitations of 1-st gen. gate a next generation was elaborated [4]. This generation allows lowering supply voltage much below typical for a given technology, thus reducing power dissipation. The new circuit also eliminates the drawback of 1-st gen. gate, where transistor sizes had to be physically suited to the preliminary fixed value of  $I_H$ . In this approach the circuit adapts to an arbitrary chosen value of the current  $I_H$  in a wide range (e.g. from 10 $\mu\text{A}$  to 100 $\mu\text{A}$ ). Furthermore, new approach enables to reduce overshoots during switching. The concept of the new

gate is shown in Fig. 7. Voltage source V1 is replaced by the current source/limiter S2, though the exact role of V1 plays here a new source/limiter S3. In Fig. 8 a CMOS realization of this gate is presented. For this realization, the activation voltage  $V_{act}$  is set to  $\max(V_{thp}, V_{thn} + V_{satM3})$ , where  $V_{thp}$  is the threshold voltage of pMOST. A diagram of currents of this circuit is shown in Fig. 9, assuming that it is one of gates in a cascade of identical gates. For the mentioned above technology, transistor sizes have the following values (given in  $\mu\text{m}$ ):  $W/L_{(M1)}=2.2/0.8$ ,  $W/L_{(M2)}=2/1.6$ ,  $W/L_{(M3)}=6/0.8$ ,  $W/L_{(M4)}=4.3/1.2$ ,  $W/L_{(M5)}=6/0.8$ ,  $W/L_{(M6)}=4.4/0.8$ . An additional polarization circuit is needed. It consists of the transistors Mp1-3 of sizes:  $W/L_{(Mp1)}=4.4/1.2$ ,  $W/L_{(Mp2)}=4.4/1.2$ ,  $W/L_{(Mp3)}=4/0.8$ . This circuit can be added as one for the whole row of gates in the layout of the system core.

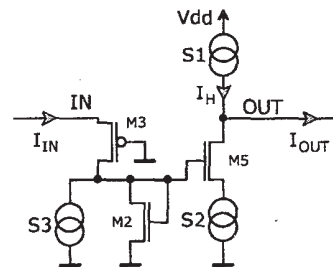


Fig. 7. Concept of the 2-nd generation current mode gate

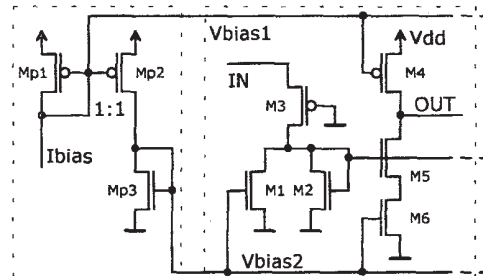


Fig. 8. CMOS realization of the 2-nd generation of current mode gate with the polarization circuit

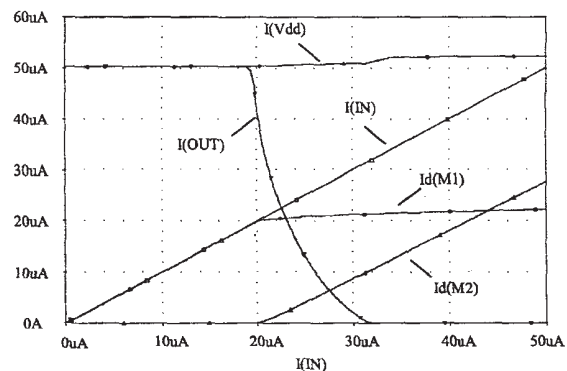


Fig. 9. Plot of currents versus  $I(IN)$  in the circuit of 2-nd generation of current mode gate

Let us consider the simplified scheme of the gate (Fig. 7). When input voltage exceeds  $V_{act}$ , then current flows into the current limiter S3. The limit value of S3

is set to about a half of  $I_H$ . Surplus over  $I_H/2$  polarizes diode-connected M2. For the adequate ratio of the current mirror M5 can conduct all the current of S1 for a slight increase of  $I_{IN}$  over  $I_H/2$ . As a result transfer characteristic has a sufficient place for wide noise margins. The slope of this characteristic is greater for the higher ratio of the mirror, but for wide channel of M5 the propagation time increases, due to higher parasitic capacitances.

Albeit 2-nd generation approach allows exploit a new idea. If we eliminate current source S1 from one output, such an output can draw current from another output connected together. In this case, limiter S2 plays additional role – limits drawn current to the value of  $I_H$ . The new output type is called ANTINOR (logical levels on such an output one may assign to "0" and "-1"). Using a simplified version of an inverting output one can also make an OR gate (or better say OR output type of the gate). These possibilities with an example of usage are described in [4]. An ASIC containing 4-bit ALU based on these gates was fabricated. Tests of this circuit showed proper operation in all modes.

#### IV. 3-RD GENERATION OF CURRENT GATES

In Fig. 10 a CMOS realization of the 3-rd generation of current mode gate with one NOR and one ANTINOR output. Transistor sizes are as follows:  $W/L_{(M1)}=2.4/0.8$ ,  $W/L_{(M3)}=4/0.8$ ,  $W/L_{(M4a)}=4.3/1.2$ ,  $W/L_{(M5a/b)}=3/0.8$ ,  $W/L_{(M6a/b)}=4.4/0.8$ ,  $W/L_{(M7)}=4/0.8$ ,  $W/L_{(M8)}=4/0.8$  (all in  $\mu\text{m}$ ). There is a one extra transistor in comparison to the 2-nd gen., but the sizes of transistors are smaller. Polarization circuit is the same as in Fig. 8.

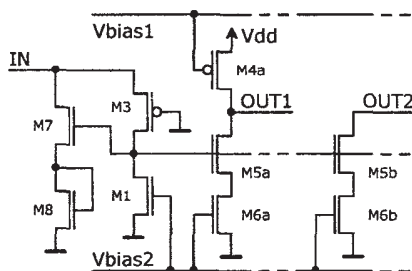


Fig. 10. CMOS realization of the 3-rd generation of current mode gate with NOR and ANTINOR outputs

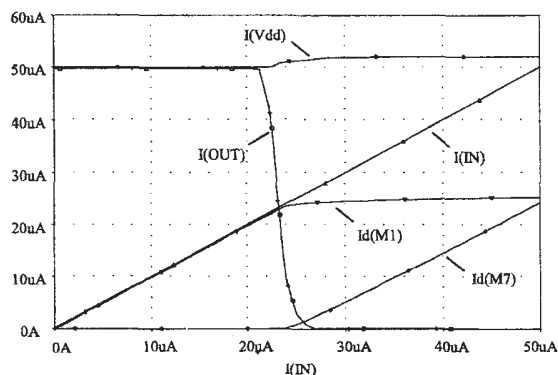


Fig. 11. Plot of currents versus  $I_{(IN)}$  in the circuit of 3-rd generation of current mode gate

#### V. BUILDING REPROGRAMMABLE MIXED MODE CIRCUIT WITH CURRENT MODE GATES

Current mode circuits may be applied to reprogrammable integrated circuit design. The programming input is added to the current mode gate by applying additional transistor M9, which gate is also connected to the gate of M3. In such a way, constant value of the current drawn from the power supply by a digital gate connected to the input IN is maintained.

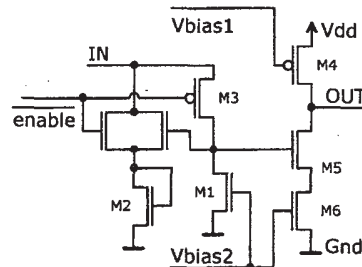


Fig. 12. Current mode gate with the *enable* input for a programmable system

Outside the programmable megacell circuitry a configuration memory is placed. Reprogramming is not a frequent activity for typical applications, thus we use a voltage mode register as the configuration memory. During normal operation strong variation of global current are not observed. The output voltage of the register is either  $0V + V_{satnMOS}$  or  $V_{dd} - V_{satpMOS}$ .

#### VI. CONCLUSIONS

Recent achievements in current mode gates transfer characteristic improvement were shown. The 3-rd generation inverter gate is characterized by a steep transfer characteristic  $I_{OUT}$  vs.  $I_{IN}$ . These circuits are very promising for analog-digital mixed mode solutions of SoC reprogrammable circuits, because of almost constant value of the current drawn from the power supply, and due to small changes of current and voltages during switching, which results in a low level of  $dI/dt$  and substrate noise. A method of basic programming option was also shown.

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