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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/385,213	10/30/2023	Shih-Yuan WANG	309-0015USCIP	7381

139982 7590 09/10/2024

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER	
RODELA, EDUARDO A	

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
09/10/2024	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

APPLICATION NO.	ISSUE DATE	PATENT NO.
18/385,213	10-Sep-2024	12087871

Wissing Miller LLP
Industrious at Hudson Yards
New York, NY 10001

EGRANT NOTIFICATION

Your electronic patent grant (eGrant) is now available, which can be accessed via Patent Center at https://patentcenter.uspto.gov

The electronic patent grant is the official patent grant under 35 U.S.C. 153. For more information, please visit https://www.uspto.gov/electronicgrants

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/385,213	09/10/2024	12087871	309-0015USCIP	7381

139982 7590 08/21/2024

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

ISSUE NOTIFICATION

The projected patent number and issue date are specified above. The patent will issue electronically. The electronically issued patent is the official patent grant pursuant to 35 U.S.C. § 153. The patent may be accessed on or after the issue date through Patent Center at https://patentcenter.uspto.gov/. The patent will be available in both the public and the private sides of Patent Center. Further assistance in electronically accessing the patent, or about Patent Center, is available by calling the Patent Electronic Business Center at 1-888-217-9197.

The USPTO is implementing electronic patent issuance with a transition period, during which period the USPTO will mail a ceremonial paper copy of the electronic patent grant to the correspondence address of record. Additional copies of the patent (i.e., certified and presentation copies) may be ordered for a fee from the USPTO's Certified Copy Center at https://certifiedcopycenter.uspto.gov/index.html. The Certified Copy Center may be reached at (800)972-6382.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Center (https://patentcenter.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PATENT CENTER site https://patentcenter.uspto.gov for additional inventors):

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping WANG, Los Altos, CA;

APPLICANT(s) (Please see PATENT CENTER site https://patentcenter.uspto.gov for additional applicants):

W&W Sens Devices, Inc., Los Altos, CA;

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
18/385,213	**08/12/2024 05:17:01 PM Z ET**	**309-0015USCIP**

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	7381	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	66753538	FILING DATE	10/30/2023
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIP_Issue_Fee-LtrWithStatementOfAllowance-Final.pdf	2	Miscellaneous Incoming Letter	501 KB
309-0015USCIP_IssueFeeTransmittal-Final.pdf	1	Issue Fee Payment (PTO-85B)	470 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
309-0015USCIP_Issue_Fee-LtrWithStatementOfAllowance-Final.pdf	973A64759280F5CFC0252D1D8643DAADEB9DEDE4A496E50DE9E84945DD7DD00D821CE23C35239306C1EC9B4E69BF7D6F1490A84EE6D9D26E205B4894603E5895

309-0015USCIP_IssueFeeTransmittal-Final.pdf	8DFD335B822D519527741806FFD11DDE1114BB54A4D20EB0C72BAF8C1E8B242A7CB1FF67CF182953495F2C65C63F2D472371C2584FC92EF09CE8B8EA6848E101

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
18/385,213	**08/12/2024 05:17:01 PM Z ET**	**309-0015USCIP**

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	7381	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	66753538	AUTHORIZED BY	Ivan Kavrukov
CUSTOMER #	139982	FILING DATE	10/30/2023
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Shih-Yuan WANG

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 2892	**E20248BH18179907**	**Mary Ellen Finnegan**

PRE-AUTHORIZED ACCOUNT	PRE-AUTHORIZED CATEGORY
600125	**37 CFR 1.21 (Miscellaneous fees and charges)**

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2501	UTILITY ISSUE FEE	480.00	1	480.00
			TOTAL AMOUNT:	**$480.00**

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Shih-Yuan WANG
Serial No.:	18/385,213
Filing Date:	January 11, 2021
Art Unit:	2893
Confirmation No.:	7381
Examiner:	EDUARDO A RODELA
For:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

31 Hudson Yards, 11th Floor
New York, New York 10001

CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: August 12, 2024

I hereby certify that this correspondence is being transmitted via Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER ACCOMPANYING ISSUE FEE PAYMENT

Submitted herewith for filing in the U.S. Patent and Trademark Office are the following:

☒ Part B – Issue Fee Transmittal;
☒ Payment by credit card and Authorization to charge Deposit Account 600125 in payment of any fee deficiencies;

Applicant Comments to Examiner's Statement of Reasons for Allowance

The applicant recognizes that in accordance with M.P.E.P. § 1302.14, the Examiner's reasons for allowance need not set forth all of the details as to why the claims are allowed. In the above identified application, the applicant does not concede that the examiner's stated reasons for allowance are the only reasons for which the claims are allowable. In particular, the applicant does not concede

that all of the recited limitations are necessary to distinguish the prior art of record or to satisfy the requirements of 35 U.S.C. § 112. In addition, the dependent claims are allowable on their own merits, and are allowable on the basis of a sub-combination of the recited features of the dependent claims and their respective base claims.

If there are any questions regarding this submission, the Examiner is encouraged to contact the undersigned via telephone at (917) 945-0121. I hereby authorize the USPTO to communicate any subject matter of this application by electronic mail at [wmdocket@wissingmiller.com]. I understand that a copy of these communications will be made of record in the application file.

By: /Ivan S. Kavrukov/
Ivan S. Kavrukov
Reg. No. 25,161
Tel. (917) 945-0121

Date: August 12, 2024
Address: (associated with Customer Number: 139982)
31 Hudson Yards, 11th Floor
New York, New York 10001
Attorney's Telephone No.: (917) 945-0121

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
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Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

139982 7590 05/16/2024
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

Mary Ellen Finnegan	(Typed or printed name)
/Mary Ellen Finnegan/	(Signature)
August 12, 2024	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/385,213	10/30/2023	Shih-Yuan WANG	309-0015USCIP	7381

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0.00	$0.00	$480	08/16/2024

EXAMINER	ART UNIT	CLASS-SUBCLASS
RODELA, EDUARDO A	2893	136-256000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Wissing Miller LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: W&W Sens Devices, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Los Altos, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ☒ Corporation or other private group entity ❑ Government

4a. Fees submitted: ☒ Issue Fee ❑ Publication Fee (if required)

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via the USPTO patent electronic filing system ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 600125

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Ivan S. Kavrukov/ Date August 12, 2024

Typed or printed name Ivan S. Kavrukov Registration No. 25,161

PTOL-85 Part B (11/23) Approved for use through 03/31/2026 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Number * 18/385,213 *	Application/Control No. 18/385,213	Applicant(s)/Patent under Reexamination WANG et al.	
	Examiner RODELA, EDUARDO A	Art Unit 2893	

Document Code - DISQ	Internal Document - DO NOT MAIL

TERMINAL DISCLAIMER	☑ APPROVED	☐ DISAPPROVED
Date Filed: 18 July 2024	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:

/JEAN PROCTOR/

Technology Center: OPLC

Telephone: (571)272-1040

16 TD'S

PTO/AIA/26 (04-14)
Approved for use through 11/30/2020. OMB 0651-0031
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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIP

In re Application of: Shih-Yuan WANG

Application No.: 18/385,213

Filed: October 30, 2023

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 10,468,543 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
July 18, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/25 (04-13)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION	Docket Number (Optional) 309-0015USCIP

In re Application of: Shih-Yuan WANG

Application No.: 18/385,213

Filed: October 30, 2023

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending **reference** Application Number 17/434,382, filed, September 21, 2020, as the term of any patent granted on said **reference** application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending **reference** application. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the **reference** application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term of any patent granted on said **reference** application, "as the term of any patent granted on said **reference** application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending **reference** application," in the event that: any such patent granted on the pending **reference** application expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
July 18, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) is included.

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Privacy Act Statement

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIP

In re Application of: Shih-Yuan WANG

Application No.: 18/385,213

Filed: October 30, 2023

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 11,830,954 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
July 18, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIP

In re Application of: Shih-Yuan WANG

Application No.: 18/385,213

Filed: October 30, 2023

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 11,791,432 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
July 18, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIP

In re Application of: Shih-Yuan WANG

Application No.: 18/385,213

Filed: October 30, 2023

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 9,530,905 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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is held unenforceable;
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1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
July 18, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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In re Application of: Shih-Yuan WANG

Application No.: 18/385,213

Filed: October 30, 2023

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July 18, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIP

In re Application of: Shih-Yuan WANG

Application No.: 18/385,213

Filed: October 30, 2023

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 10,622,498 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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is held unenforceable;
is found invalid by a court of competent jurisdiction;
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has all claims canceled by a reexamination certificate;
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/Ivan S. Kavrukov/ — Signature
July 18, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
18/385,213	**07/18/2024 02:03:11 PM Z ET**	**309-0015USCIP**

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	7381	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	66422361	FILING DATE	10/30/2023
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 16

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIP_TerminalDisclaimer_9525084.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIP_TerminalDisclaimer_9496435.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIP_TerminalDisclaimer_10446700.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIP_TerminalDisclaimer_10468543.pdf	2	Terminal Disclaimer Filed	157 KB

309-0015USCIP_TerminalDisclaimer_9818893.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIP_TerminalDisclaimer_9530905.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIP_TerminalDisclaimer_10622498.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIP_TerminalDisclaimer_11121271.pdf	2	Terminal Disclaimer Filed	157 KB
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309-0015USCIP_TerminalDisclaimer_10700225.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIP_TerminalDisclaimer_11791432.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIP_TerminalDisclaimer_11621360.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIP_TerminalDisclaimer_11830954.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIP_TerminalDisclaimer_17434382.pdf	2	Terminal Disclaimer Filed	240 KB

309-0015USCIP_TerminalDisclaimer_18385213.pdf	2	Terminal Disclaimer Filed	240 KB
309-0015USCIP_TerminalDisclaimer_18113474.pdf	2	Terminal Disclaimer Filed	240 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIP

In re Application of: Shih-Yuan WANG

Application No.: 18/385,213

Filed: October 30, 2023

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

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/Ivan S. Kavrukov/ — Signature
July 18, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

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/Ivan S. Kavrukov/ — Signature
July 18, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/25 (04-13)
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TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION	Docket Number (Optional) 309-0015USCIP

In re Application of: Shih-Yuan WANG

Application No.: 18/385,213

Filed: October 30, 2023

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending **reference** Application Number 18/113,474, filed, February 23, 2023, as the term of any patent granted on said **reference** application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending **reference** application. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the **reference** application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/	July 18, 2024
Signature	Date
Ivan S. Kavrukov	
Typed or printed name	
Attorney of Record	917-945-0121
Title	Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) is included.

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UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
18/385,213	07/18/2024 02:03:11 PM Z ET	309-0015USCIP

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	7381	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	66422361	AUTHORIZED BY	Ivan Kavrukov
CUSTOMER #	139982	FILING DATE	10/30/2023
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Shih-Yuan WANG

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 2892	E20247HE04586359	Mary Ellen Finnegan
PRE-AUTHORIZED ACCOUNT	PRE-AUTHORIZED CATEGORY	
600125	37 CFR 1.21 (Miscellaneous fees and charges)	

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2814	STATUTORY DISCLAIMER, INCLUDING TERMINAL DISCLAIMER	170.00	16	2720.00
			TOTAL AMOUNT:	$2,720.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIP

In re Application of: Shih-Yuan WANG

Application No.: 18/385,213

Filed: October 30, 2023

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 11,121,271 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
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2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
July 18, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIP

In re Application of: Shih-Yuan WANG

Application No.: 18/385,213

Filed: October 30, 2023

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 11,621,360 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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/Ivan S. Kavrukov/ — Signature
July 18, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIP

In re Application of: Shih-Yuan WANG

Application No.: 18/385,213

Filed: October 30, 2023

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

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/Ivan S. Kavrukov/ — Signature
July 18, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIP

In re Application of: Shih-Yuan WANG

Application No.: 18/385,213

Filed: October 30, 2023

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 9,496,435 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
July 18, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIP

In re Application of: Shih-Yuan WANG

Application No.: 18/385,213

Filed: October 30, 2023

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 10,700,225 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

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2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
July 18, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION	Docket Number (Optional) 309-0015USCIP

In re Application of: Shih-Yuan WANG

Application No.: 18/385,213

Filed: October 30, 2023

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending **reference** Application Number 18/385,213, filed, October 30, 2023, as the term of any patent granted on said **reference** application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending **reference** application. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the **reference** application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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/Ivan S. Kavrukov/	July 18, 2024
Signature	Date
Ivan S. Kavrukov	
Typed or printed name	
Attorney of Record	917-945-0121
Title	Telephone Number

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/385,213	10/30/2023	Shih-Yuan WANG	309-0015USCIP	7381

139982 7590 06/10/2024

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER	
RODELA, EDUARDO A	

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
06/10/2024	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

Notice of Allowability	Application No. 18/385,213	Applicant(s) WANG et al.	
	Examiner Eduardo A Rodela	Art Unit 2893	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to printer rush 5/21/2024.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 13-30 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/EDUARDO A RODELA/
Primary Examiner, Art Unit 2893

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NOTICE OF ALLOWANCE AND FEE(S) DUE

139982 7590 05/16/2024

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER	
RODELA, EDUARDO A	
ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 05/16/2024

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/385,213	10/30/2023	Shih-Yuan WANG	309-0015USCIP	7381

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0.00	$0.00	$480	08/16/2024

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 11/23)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

139982 7590 05/16/2024
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/385,213	10/30/2023	Shih-Yuan WANG	309-0015USCIP	7381

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0.00	$0.00	$480	08/16/2024

EXAMINER	ART UNIT	CLASS-SUBCLASS
RODELA, EDUARDO A	2893	136-256000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required)

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via the USPTO patent electronic filing system ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Samsung Exhibit 1003, Page 55 of 654

UNITED STATES PATENT AND TRADEMARK OFFICE

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Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 11/23)

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013).
https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf

Routine uses of the information in this record may include disclosure to:

1) law enforcement, in the event that the system of records indicates a violation or potential violation of law;
2) a federal, state, local, or international agency, in response to its request;
3) a contractor of the USPTO having need for the information in order to perform a contract;
4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record;
5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record;
6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations;
7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals;
8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c));
9) the Office of Personnel Management (OPM) for personnel research purposes; and
10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Notice of Allowability	Application No. 18/385,213	Applicant(s) WANG et al.	
	Examiner Eduardo A Rodela	Art Unit 2893	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 4/10/2024.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 13-30 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☑ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☑ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☑ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/EDUARDO A RODELA/
Primary Examiner, Art Unit 2893

DETAILED ACTION

This correspondence is in response to the communications received April 10, 2023. Claims 13-30 are pending. This application has been granted expedited examination status on December 8, 2023.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Priority

It is acknowledged that this application is a continuation of several US applications including 14/947,718 (now US 10,622,498) which has priority benefit of at least Provisional applications 61/905,109 (with date November 15, 2013) and 61/843,021 (with date July 4, 2013). The effective filing date is the earliest of the supported parent applications which appears to be the provisional application 61/843,021, dated **July 4, 2013**.

Information Disclosure Statement

The IDS document dated March 13, 2024 has been annotated by Examiner to include the publication date for the #3 Non-Patent Literature Documents (on page 8) as June 2019.

Applicant's Representative provided the following two citations for the Jonghoon Park et al. "Pixel Technology for improving IR Quantum Efficiency of Backside-illuminated CMOS Image Sensor" document. The citation dates were found via Google Search in the citation section.

First citation:

Park, Jonghoon, Yunki Lee, Bumsuk Kim, Bomi Kim, Junsung Park, Eunju Yeom, Yunji Jung et al. "Pixel technology for improving IR quantum efficiency of backside-illuminated CMOS image sensor." In Proc. Int. Image Sensor Workshop, vol. 4, pp. 1-4. 2019.

Second citation:

Park, J., Lee, Y., Kim, B., Kim, B., Park, J., Yeom, E., ... & Park, Y. (2019, June). Pixel technology for improving IR quantum efficiency of backside-illuminated CMOS image sensor. In Proc. Int. Image Sensor Workshop (Vol. 4, pp. 1-4).

Claim Objections

The claim objections have been withdrawn in light of Applicant's newly presented amendment, which does not contain the language that previously warranted the objection.

Relevant Prior Art

Kuriyama et al. (US 2004/0157354) Figs. 2A, 2B, shown below. This reference shows plural light sensitive pillars, but are lacking the holes formed in the pillars with dielectric filling.

FIG. 2A

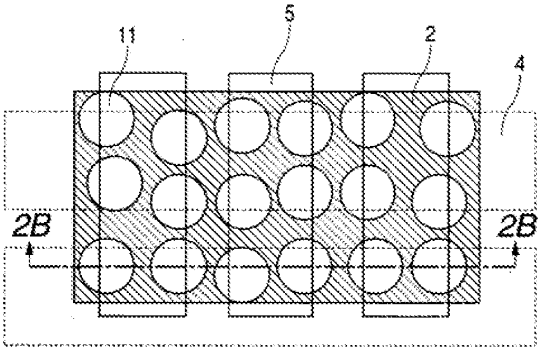
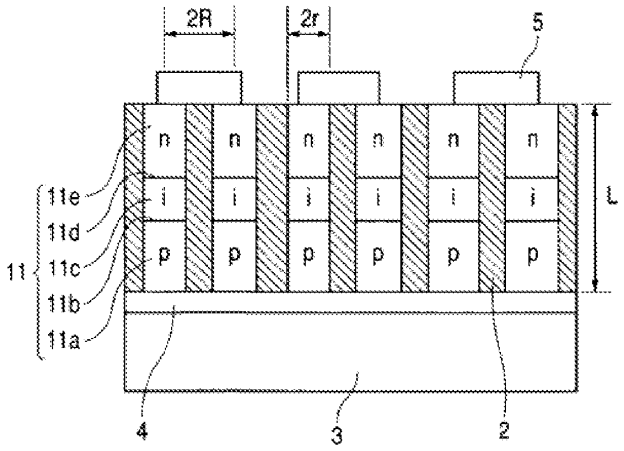


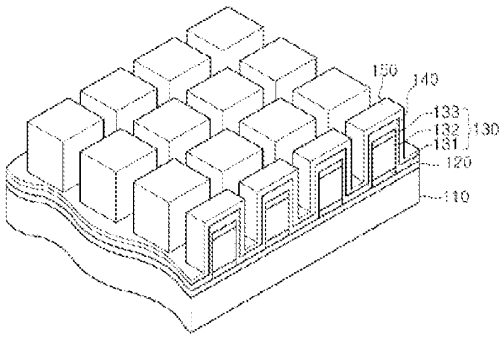
FIG. 2B



Hong et al. (US 2010/0193022) Fig. 12, shown below. "The light-converting layer 130 is formed in plurality spaced apart from each other. Each of the light-converting layers 130 includes a plurality of semiconductor layers. For example, each of the light-converting layers

130 includes a stack of a p-type amorphous silicon layer 131, an i-type amorphous silicon layer 132, and an n-type amorphous silicon layer 133. Herein, the p-type amorphous silicon layer 131 is a layer that is doped with p-type impurities, the i-type amorphous silicon layer 132 is a layer that is not doped with impurities, and the n-type amorphous silicon layer 133 is a layer that is doped with n-type impurities.", ¶ 0039. This reference shows plural light sensitive pillars, but are lacking the holes formed in the pillars with dielectric filling.

[Fig. 12]



Hsu et al. (US 2008/0083963) Fig. 3G shown below. This reference shows plural light sensitive pillars, but are lacking the holes formed in the pillars with dielectric filling.

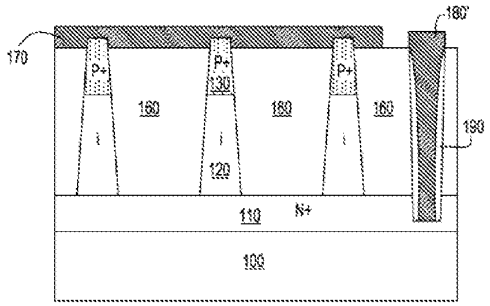


FIG. 3G

Han et al. (US 2013/0014814) Fig. 8, shown below, which depicts lattice constant on efficiency and Absorption, shown below.

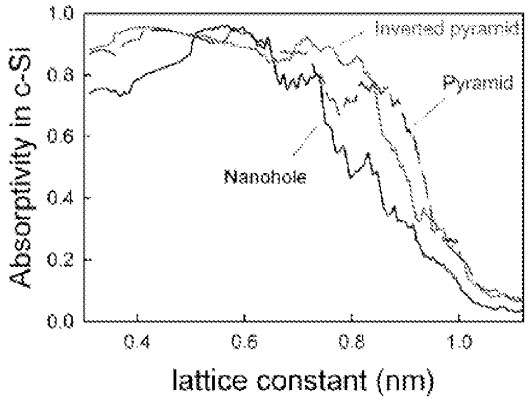


FIG. 9

Bandyopahyay et al. (US 8,207,064) Fig. 10G, shown below. This reference shows plural light sensitive pillars, but are lacking the holes formed in the pillars with dielectric filling.

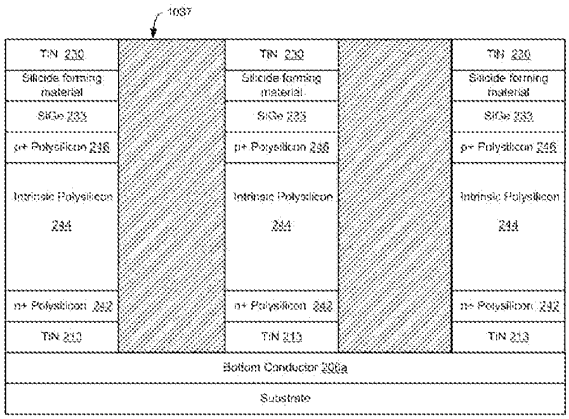


Fig. 10G

Applicant's Claim to Figure Comparison

It is noted that this comparison is merely for the benefit of reviewers of this office action during prosecution, to allow for an understanding of the examiner's interpretation of the Applicant's independent claims as compared to disclosed embodiments in Applicant's Figures. No response or comments are necessary from Applicant.

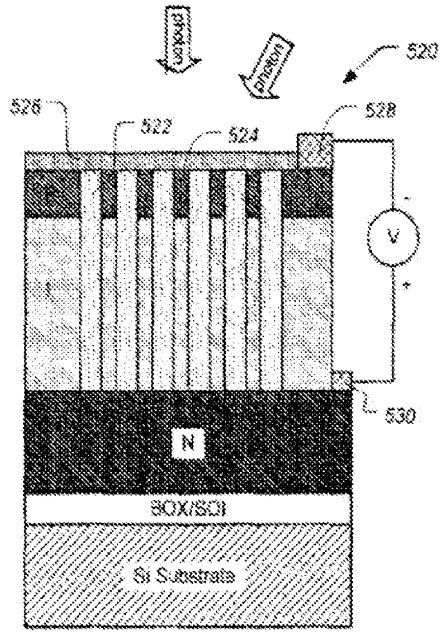


FIG. 5B

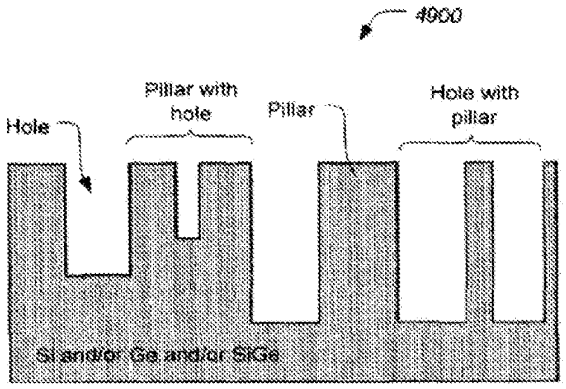


FIG. 49

Regarding claim 13, the Applicant discloses in Figs. 5B and 49, provided above, an integrated structure comprising:

an array of pillars comprising Si, Ge, and/or SiGe alloy semiconductor material wherein at least some of the pillars are configured as photodetectors that have respective light-receiving surfaces and have sides (from ¶ 0132, "Fig. 5B shows a microstructured pillar and or hole PD 520 in silicon with the starting material 500 consisting of a P-I-N Si layer grown on an Si substrate 502…");

wherein at least some of the photodetectors comprise P-doped and N- doped regions and regions therebetween (P-I-N structure shown in Fig. 5B) and are configured to respond to illumination with light in selected visible and infrared wavelength ranges by generating electrical charge carriers (from ¶ 0132, "the optical signal wavelengths range from 750-1100 nm");

one or more holes that are deliberately formed into the light-receiving surfaces (noted "holes" are understood to be further holes that are within surfaces of the pillars, and are in

addition to the "holes" or discontinuities in material that allow for the creation of the pillars), have elongated and/or other shapes at said light- receiving surfaces (see Fig. 49), extend into the photodetectors to a depth of 100 to10000 nm (¶ 0154), and are filled at least partly with solid dielectric material (¶ 0095, "when structures such as … holes (which can be filled with low index material …"):

side-isolation comprising solid material at said sides of at least some of the photodetectors (passivation 522 in Fig. 5B, which isolates each pillar from a neighboring pillar);

a solid dielectric material forming a base dielectric region for said array ('BOX/SOI' layer shown in Fig. 5B); and

electrical contacts (528 and 530 as shown in Fig. 5B) configured to provide electrical pathways to at least some of the photodetectors, including for selected reverse-biasing thereof (discussed in at least ¶ 0023);

wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to an otherwise like photodetectors lacking said holes (discussed in ¶ 0114).

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in an interview with Ivan S. Kavrukov on May 8, 2024.

The application has been amended as follows:

In the Claims:

Please amend claim 13 as follows. On the second to last line of the recitation of "photodetectors relative to ~~an~~ otherwise like photodetectors lacking said holes", please delete the term "an".

REASONS FOR ALLOWANCE

Claims 13-30 are allowed.

The following is an Examiner's statement of reasons for allowance: The integrated structure as recited in the claims of the instant invention fail to be taught by the prior art cited of interest.

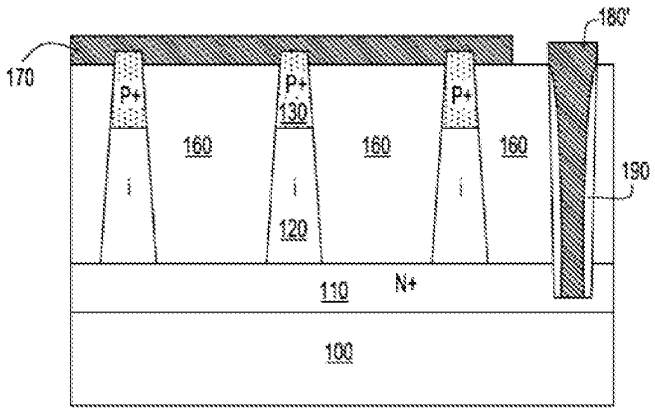


FIG. 3G

Regarding claim 13, the prior art of Hsu et al. (US 2008/0083963) discloses in Fig. 3G, a light converting pillar diode array, but fails to disclose the specific characteristic recited in the claims of the instant invention e.g. the combination of claimed limitations of an array of pillars and their particular semiconductor material that are configured as photodetectors, the photodetectors comprise P-I-N doping arrangement, holes are formed in the light receiving surfaces of the pillars, the holes are of a dimension as claimed, side-isolation, solid dielectric material, electrical contacts, the holes improve absorption by a particular amount. The prior art fails to disclose the particulars of the holes formed in the light receiving surfaces of the pillars. The Hsu reference (above) shows plural light sensitive pillars, but are lacking the particulars of the holes formed in the pillars, which are then filled with dielectric filling.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A Rodela whose telephone number is (571)272-8797. The examiner can normally be reached M-F, 8:30-5:00pm ET.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yara B Green can be reached on (571) 270-3035. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EDUARDO A RODELA/
Primary Examiner, Art Unit 2893

Examiner-Initiated Interview Summary	**Application No.** 18/385,213	**Applicant(s)** WANG et al.		
	Examiner Eduardo A Rodela	**Art Unit** 2893	**AIA (First Inventor to File) Status** Yes	**Page** 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	**Title**	**Type**
Eduardo A Rodela	Primary Examiner	Telephonic
Ivan S. Kavrukov	Attorney of Record	

Date of Interview: 08 May 2024

Issues Discussed:

Other

Examiner sought to have Applicant, resubmit the document #3 on page 8 of the IDS (dated March 13, 2024), to include the date of publication, which is not currently present in the document. Applicant's Representative then supplied the date as June 2019 for said citation of the IDS document. Next, Examiner sought clarification on the support for claim 13 limitation of "side isolation". Applicant's Representative then supplied an explanation that the features were captured in para 0144 and in Fig. 9D as "filler 916". This is analogous to Fig. 5B's fillers identified as elements 522.

	/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893

Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Notice of References Cited	Application/Control No. 18/385,213	Applicant(s)/Patent Under Reexamination WANG et al.	
	Examiner Eduardo A Rodela	Art Unit 2893	Page 1 of 1

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*	B	US-20120255603-A1	2012-10-11	Yu; Young-June	H01L31/02363	257/E31.127
*	C	US-8207064-B2	2012-06-26	Bandyopadhyay; Abhijit	H01L29/456	438/682
*	D	US-20150096613-A1	2015-04-09	TJAHJONO; BUDI	H01L31/02363	136/256
*	E	US-20080083963-A1	2008-04-10	Hsu; Louis Lu-Chen	H01L27/1446	257/431
*	F	US-20100193022-A1	2010-08-05	Hong; Jin	H01L31/035281	257/E31.127
*	G	US-20040157354-A1	2004-08-12	Kuriyama, Akira	H01L31/105	438/45
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	I					
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	O					
	P					
	Q					
	R					
	S					
	T					

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*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in YYYY-MM-DD format are publication dates. Classifications may be US or foreign.

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	18/385,213	WANG et al.
	Examiner	Art Unit
	Eduardo A Rodela	2893

CPC						
Symbol					Type	Version
H01L	/	31	/	035272	F	2013-01-01
H01L	/	31	/	035281	I	2013-01-01
H01L	/	31	/	075	I	2013-01-01
H01L	/	31	/	105	I	2013-01-01
G02B	/	6	/	136	I	2013-01-01
H01L	/	31	/	0284	I	2013-01-01
H01L	/	31	/	035227	I	2013-01-01
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H01L	/	31	/	035209	I	2013-01-01
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NONE		Total Claims Allowed:	
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/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893	07 May 2024	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	13	5B, 49

U.S. Patent and Trademark Office — Part of Paper No.: 20240408

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	18/385,213	WANG et al.
	Examiner	Art Unit
	Eduardo A Rodela	2893

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G02B	/	2006	/	12176	A	2013-01-01
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H01L	/	2223	/	6627	A	2013-01-01

CPC Combination Sets							
Symbol					Type	Set	Ranking	Version
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	18	
/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893	07 May 2024	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	13	5B, 49

U.S. Patent and Trademark Office — Part of Paper No.: 20240408

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	18/385,213	WANG et al.
	Examiner	Art Unit
	Eduardo A Rodela	2893

INTERNATIONAL CLASSIFICATION					
CLAIMED					
H01L	/	31	/	0236	
H01L	/	31	/	0232	

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE (Assistant Examiner)	(Date)	Total Claims Allowed: 18	
/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893 (Primary Examiner)	07 May 2024 (Date)	O.G. Print Claim(s) 13	O.G. Print Figure 5B, 49

U.S. Patent and Trademark Office — Part of Paper No.: 20240408

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	18/385,213	WANG et al.
	Examiner	Art Unit
	Eduardo A Rodela	2893

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10	7	19	16	28								
	2		11	8	20	17	29								
	3		12	9	21	18	30								
	4	1	13	10	22										
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	8	5	17	14	26										
	9	6	18	15	27										

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	18	
/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893	07 May 2024	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	13	5B, 49

U.S. Patent and Trademark Office Part of Paper No.: 20240408

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	18/385,213	WANG et al.
	Examiner	Art Unit
	Eduardo A Rodela	2893

CPC - Searched*		
Symbol	Date	Examiner
H01L31/02019; H01L31/022408; H01L31/02327; H01L31/02363; H01L31/028; H01L31/035281; H01L31/105; H01L31/107; H01L27/1446,146,14607,14625,14643,14649; H01L31/02027,02327,02363,035281,09,107,105	05/07/2024	EAR

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
PE2E search - see history for complete details	05/07/2024	EAR
Inventor & Applicant search	05/07/2024	EAR
IEEE Xplore	12/29/2023	EAR

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
noted CPC search area	in conjunction with a text limited search	05/07/2024	EAR

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	18/385,213	WANG et al.
	Examiner	Art Unit
	Eduardo A Rodela	2893

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Bibliographic Data

Application No: 18/385,213

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☐ No ☐ Met After Allowance

Verified and Acknowledged: /EDUARDO A RODELA/ (Examiner's Signature) | (Initials)

Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
10/30/2023	136	2893	309-0015USCIP
RULE			

APPLICANTS

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INVENTORS

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Shih-Ping WANG, Los Altos, CA, UNITED STATES

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14945003 has PRO of 62154675 04/29/2015

14945003 has PRO of 62153443 04/27/2015

PCT/US15/61120 has PRO of 62153443 04/27/2015

14943898 has PRO of 62153443 04/27/2015

14945003 has PRO of 62139511 03/27/2015

PCT/US15/61120 has PRO of 62139511 03/27/2015

14943898 has PRO of 62139511 03/27/2015

PCT/US15/61120 has PRO of 62111582 02/03/2015

14945003 has PRO of 62111582 02/03/2015

14943898 has PRO of 62111582 02/03/2015

PCT/US15/61120 has PRO of 62100025 01/05/2015

14945003 has PRO of 62100025 01/05/2015

14943898 has PRO of 62100025 01/05/2015

PCT/US15/61120 has PRO of 62090879 12/11/2014

14945003 has PRO of 62090879 12/11/2014

14943898 has PRO of 62090879 12/11/2014

14943898 has PRO of 62081583 11/19/2014ABN

14945003 has PRO of 62081538 11/18/2014

PCT/US15/61120 has PRO of 62081538 11/18/2014

14947718 is a CON of PCT/US14/39208 05/22/2014

PCT/US14/39208 has PRO of 61905109 11/15/2013

PCT/US14/39208 has PRO of 61843021 07/04/2013

PCT/US14/39208 has PRO of 61834873 06/13/2013

PCT/US14/39208 has PRO of 61826446 05/22/2013

FOREIGN APPLICATIONS

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L72	70	((US-10622498-B2 OR US-11621360-B2 OR US-7525170-B2 OR US-9257583-B2 OR US-9841510-B2 OR US-6538299-B1 OR US-6177289-B1 OR US-6111305-A OR US-9496435-B2 OR US-11536914-B2 OR US-11757072-B2 OR US-8357960-B1 OR US-11855239-B2 OR US-11728457-B2 OR US-10854656-B2 OR US-9184202-B2 OR US-7183127-B2 OR US-7396696-B2 OR US-11502219-B2 OR US-9362448-B2 OR US-8946675-B2 OR US-8664636-B2 OR US-8659037-B2 OR US-8476637-B2 OR US-8431817-B2 OR US-7132677-B2 OR US-8129710-B2 OR US-9559231-B2 OR US-8330173-B2 OR US-7161220-B2 OR US-7022544-B2 OR US-6879014-B2 OR US-11550099-B2 OR US-11101304-B2 OR US-6027956-A OR US-5757057-A OR US-5625636-A OR US-4571559-A OR US-8829460-B2 OR US-11764248-B2 OR US-10651225-B2 OR US-11211419-B2 OR US-11152408-B2 OR US-11088189-B2).did. AND USPT.dbnm.) OR ((US-20230215962-A1 OR US-20180182806-A1 OR US-20180012918-A1 OR US-20120153127-A1 OR US-20120012741-A1 OR US-20160225631-	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/06 09:24 AM

		A1 OR US-20150054997-A1 OR US-20140263975-A1 OR US-20140001528-A1 OR US-20040144985-A1 OR US-20040048092-A1 OR US-20110000545-A1 OR US-20100313941-A1 OR US-20100288341-A1 OR US-20100221866-A1 OR US-20100193768-A1 OR US-20090225804-A1 OR US-20090008735-A1 OR US-20080218740-A1 OR US-20070134840-A1 OR US-20050184354-A1).did. AND PGPB.dbnm.) OR ((CN-103348486-A).did. AND FTDB.dbnm.) OR ((WO-2012160662-A1 OR US-20120168613-A1 OR US-11094846-B1 OR US-20150008554-A1).did. AND DWPI.dbnm.)					
L73	14	"20180182806"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/06 11:29 AM
L74	13	("4827114" | "5055894" | "6111305" | "6177289" | "6300648" | "6451702" | "6538299" | "6707126").pn. OR ("7525170").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/05/06 04:12 PM
L75	35	(@rlpd<="20130704" OR @rlad<="20130704"	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY,	OR	ON	ON	2024/05/06 04:12 PM

		OR @pd<="20130704" OR @ad<="20130704") AND L74	CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L76	15	("6515315" | "6841807" | "6897471" | "7233051" | "7259444" | "7525170" | "20040108516" | "20040157354" | "20050173712" | "20060060933" | "20060076589" | "20080265357" | "20110180894" | "20110309240").pn. OR ("9166091").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/05/06 04:13 PM
L77	38	(Artificial Intelligence) More like doc: US-20040157354-A1 Text: (US-7183127-B2 OR JP-2004193527-A OR JP-4235440-B2 OR JP-2005353828-A OR WO-2011156266-A2 OR EP-2580791-A2 OR KR-101786765-B1 OR KR-20140010921-A OR CN-103069585-B OR CN-103069585-A OR EP-2580791-B1 OR EP-3116036-A1 OR WO-2017005792-A1 OR EP-3320567-A1 OR US-20180199409-A1 OR WO-2011156266-A3 OR US-10201054-B2 OR EP-3320567-B1 OR JP-2020181937-A OR WO-2023064157-A1).did.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/06 04:47 PM
L78	26099	(P-I-N OR "P-I-N") WITH (apd OR (avalanche NEAR photo NEAR diode) OR junction OR diode)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	OR	ON	ON	2024/05/06 05:37 PM

			EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L79	507	(P-I-N OR "P-I-N") WITH (apd OR (avalanche NEAR photo NEAR diode) OR junction OR diode) WITH (column OR pillar)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/06 05:37 PM
L80	444	(@rlpd<="20130704" OR @rlad<="20130704" OR @pd<="20130704" OR @ad<="20130704") AND L79	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/06 05:37 PM
L81	9	("7435996" | "7453097" | "20060207647" | "20080083963" | "20090165844" | "20090194160" | "20100078055" | "20100193022" | "20110240099").pn. OR ("9966486").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/05/07 09:11 AM
L82	41	(Artificial Intelligence) More like doc:	(US-PGPUB; USPAT; USOCR; FIT (AU, AP,	OR	ON	ON	2024/05/07 09:21 AM

		US-20080083963-A1 Text: (US-7525170-B2 OR CN-101159277-A OR CN-100568516-C OR CN-115295660-A OR EP-2747154-B1 OR WO-2012054436-A1 OR CN-103415929-B OR KR-20100138391-A OR CN-103415929-A OR KR-101033028-B1 OR EP-2717322-A1 OR US-20140166100-A1 OR WO-2013009615-A1 OR US-20130009265-A1 OR US-8368159-B2 OR WO-2012160662-A1 OR JP-WO2012160662-A1 OR WO-2022138050-A1 OR US-9257583-B2 OR TW-I466307-B).did.	AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L83	3581639	(face OR surface) NEAR (textur$2 OR pattern OR shapes OR pyramids OR divots OR dimples OR holes)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/07 09:29 AM
L84	21358	H01L31/0236,02363.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/07 10:03 AM
L85	11	(@rlpd<="20130704"	(US-PGPUB; USPAT;	OR	ON	ON	2024/05/07

		OR @rlad<="20130704" OR @pd<="20130704" OR @ad<="20130704") AND L79 AND L84	USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				10:04 AM
L86	4780	(@rlpd<="20130704" OR @rlad<="20130704" OR @pd<="20130704" OR @ad<="20130704") AND L83 AND L84	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/07 10:27 AM
L87	26100	(P-I-N OR "P-I-N") WITH (apd OR (avalanche NEAR photo NEAR diode) OR junction OR diode)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/07 10:27 AM
L88	194	(@rlpd<="20130704" OR @rlad<="20130704" OR @pd<="20130704" OR @ad<="20130704") AND L83 AND L84 AND L87	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL,	OR	ON	ON	2024/05/07 10:28 AM

			PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L89	4	("20080006319" | "20080185036" | "20090194160" | "20100001359").pn. OR ("9331220").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/05/07 12:48 PM
L90	35	(Artificial Intelligence) More like doc: US-20120255603-A1 Text: (WO-2023221714-A1 OR US-10658529-B2 OR US-10230010-B2 OR US-20160204286-A1 OR DE-102012210875-A1 OR US-20150255641-A1 OR US-20130000704-A1 OR US-9741880-B2 OR US-20170288071-A1 OR DE-102012210875-B4 OR US-10347779-B2 OR US-11011655-B2 OR US-20190237597-A1 OR WO-2013186945-A1 OR KR-20150104431-A OR WO-2013125036-A1 OR JP-WO2013125036-A1 OR CN-115117198-A OR KR-20120086593-A OR AT-411409-B).did.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/07 01:08 PM
L91	38	(Artificial Intelligence) More like doc: US-20130014814-A1 Text: (WO-2011085297-A1 OR WO-2013028510-A2 OR US-20140209154-A1 OR US-20230231066-A1 OR CH-633631-A5 OR US-20120060913-A1 OR US-8314327-B2 OR KR-101575854-B1 OR WO-2019194911-A1 OR US-10935702-B2 OR US-20070204901-	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/07 02:15 PM

		A1 OR WO-2013171286-A1 OR US-20090293931-A1 OR JP-2023123575-A OR JP-7381486-B2 OR US-20190302325-A1 OR TW-201001729-A OR EP-3776666-A1 OR US-8829337-B1 OR CN-103237745-B).did.					
L92	25	("4514748" | "5604136" | "5714772" | "6452218" | "7008813").pn. OR ("7186611").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/05/07 03:14 PM
L93	2	((("W&W") near3 ("Sens") near3 ("Devices") near3 ("Inc"))).AS,AANM.	(US-PGPUB; USPAT)	OR	ON	ON	2024/05/07 04:45 PM
L94	859	((("WANG") near3 ("Shih-Yuan")) OR (("WANG") near3 ("Shih-Ping"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2024/05/07 04:45 PM
L95	0	(L93 OR L94) AND ((array)(pillar$1)("Si" OR "Ge" OR "SiGe" OR silicon OR germanium OR (silicon NEAR germainum))(photo NEAR detect$3)(light NEAR recciving NEAR surface$1)((p-dop$1 OR p-type OR "P") NEAR region)((n-dop$1 OR n-type OR "N") NEAR region)((undop$3 OR intrinsic) NEAR (region))(holes OR divots OR textur$2 OR (inverted NEAR (pyramid OR cylinder)))(contacts)(absorption OR abosorb$3))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2024/05/07 05:05 PM
L96	1	single WITH micro-hole WITH per WITH pixel	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO,	OR	ON	ON	2024/05/07 06:04 PM

			RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L97	15	(single WITH (micro NEAR hole) WITH pixel) AND cmos	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/07 06:05 PM
L98	11	(@rlpd<="20130704" OR @rlad<="20130704" OR @pd<="20130704" OR @ad<="20130704") AND L97	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/07 06:05 PM
L99	36	(Artificial Intelligence) More like doc: WO-2005072370-A2 Text: (EP-1712087-A2 OR US-20050225654-A1 OR EP-2315448-A1 OR JP-2007520166-A OR KR-20070019979-A OR EP-2315448-B1 OR US-7773143-B2 OR JP-4797151-B2 OR KR-101227544-B1 OR JP-2011072039-A OR EP-1712087-B1 OR JP-5646445-B2 OR JP-2012070431-A OR CN-1934872-A OR CN-1934872-B OR CN-105141933-A OR CN-	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/07 06:06 PM

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		105141933-B OR WO-2005072370-A3 OR US-20050073603-A1 OR US-7405761-B2).did.					
L100	44	("4479143" | "4804249" | "5355222" | "5568197" | "5671073" | "5748371" | "5757423" | "5760832" | "6069738" | "6108036" | "6137535" | "6346969" | "6366319" | "6414296" | "6417950" | "6541284" | "6611289" | "6632701" | "6882364" | "7003177" | "7009652" | "7034866" | "20020089596" | "20020122124" | "20020163582" | "20020181123" | "20020181126" | "20050073603" | "20050104991" | "20050128335" | "20050242410" | "20050248680" | "20050258350" | "20060044450").pn. OR ("7773143").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/05/07 06:06 PM
L101	2	(single WITH (micro NEAR hole) WITH (pillar OR column)) AND pixel AND cmos	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/07 06:08 PM
L102	7	(single WITH (micro NEAR hole) WITH (pillar OR column)) AND pixel	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL,	OR	ON	ON	2024/05/07 06:08 PM

			PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L103	8	"20160307939"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/07 06:09 PM
L104	31	("11211419"|"11728457"|"20180182806"|"6879014"|"7396696"|"7525170"|"8129710"|"8357960"|"8946675"|"9184202").PN.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/07 06:18 PM
L105	61	(US-10411053-$ | US-10522582-$ | US-11309444-$ | US-6879014-$ | US-7396696-$ | US-7525170-$ | US-8558336-$ | US-9000492-$).DID. OR (US-11211419-$ | US-11728457-$ | US-20100320444-$ | US-20110309331-$ | US-20180182806-$ | US-8129710-$ | US-8357960-$ | US-8946675-$ | US-9184202-$).DID. OR (US-20110156195-$ | US-20120012741-$ |	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/05/07 06:27 PM

		US-20120153127-$ | US-20160240579-$ | US-20170141153-$ | US-20180012918-$ | US-20180102442-$ | US-20190166317-$ | US-20200006407-$).DID. OR (US-20200006407-$ | US-20200006416-$).DID. OR (US-20050145779-$ | US-20120153416-$).DID. OR (US-0103255-$ | US-09040854-$ | US-20080101301-$).DID.					
L106	8	("6147732" | "8711263" | "20050040440" | "20110222145" | "20120153416" | "20130075849" | "20140184810" | "20150268394").pn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/05/07 06:36 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	0	(((H01L31/02019 OR H01L31/022408 OR H01L31/02327 OR H01L31/02363 OR H01L31/028 OR H01L31/035281 OR H01L31/105 OR H01L31/107).cpc.) OR L84) AND ((array)(pillar$1)("Si" OR "Ge" OR "SiGe" OR silicon OR germanium OR (silicon NEAR germainum))(photo NEAR detect$3)(light NEAR recciving NEAR surface$1)((p-dop$1 OR p-type OR "P") NEAR region)((n-dop$1 OR n-type OR "N") NEAR region)((undop$3 OR intrinsic) NEAR (region))(holes OR divots OR textur$2 OR (inverted NEAR (pyramid OR cylinder)))(contacts)(ab	(US-PGPUB; USPAT)	AND	ON	ON	2024/05/07 05:15 PM

		sorption OR abosorb$3)).clm.					

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	18385213
	Filing Date	2023-10-20
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIP

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	11309444		2022-04-19	Wang et al.	
	2	8558336		2013-10-15	Su	
	3	10411053		2019-09-10	Yokogawa	
	4	10522582		2019-12-31	Maruyama et al.	
	5	9000492		2015-04-07	Suzuki et al.	
	6	6879014		2005-04-12	Wagner	
	7	7396696		2008-07-08	Kim	
	8	7525170		2009-04-28	Hsu	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.A.R/

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	9	8129710		2012-03-06	Cho	
	10	8357960		2013-01-22	Dutta	
	11	8946675		2015-02-03	Yu	
	12	9184202		2015-11-10	Dutta	
	13	11211419		2021-12-28	Wu	
	14	11728457		2023-08-15	Sung	

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U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20100320444		2010-12-23	Dutta	
	2	20110309331		2011-12-22	Yu et al.	
	3	20180182806		2018-06-28	Jin et al.	

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	4	20110156195		2011-06-30	Tivarus et al.	
	5	20120153127		2012-06-21	Hirigoyen et al.	
	6	20180012918		2018-01-11	Na et al.	
	7	20190166317		2019-05-30	Tanaka et al.	
	8	20120012741		2012-01-19	Vasylyev	
	9	20180102442		2018-04-12	Wang	
	10	20160240579		2016-08-18	Sun et al.	
	11	20170141153		2017-05-18	Lee et al.	
	12	20180102442		2018-04-12	Wang et al.	
	13	20200006407		2020-01-02	Yokogawa	
	14	20200006416		2020-01-02	Baba et al.	

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	15	20050145779		2005-07-07	Mochizuki et al.		
	16	20120153416		2012-06-21	Tanaka et al.		

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	20080101301	KR		2008-11-21	Dongbu Hitek Co. Ltd.		☐
	2	2002314116	JP		2002-10-25	Seiko Epson Corp.		☐
	3	0103255	WO		2001-01-11	Scott		☐
	4	2019018846	WO		2019-01-24	W&W Sens Devices Inc.		☐
	5	09040854	EP		1999-09-08	IBM United Kingdom Limited		☐
	6	2007013065	JP		2007-01-18	Matsushita Electric Works Ltd.		☐
	7	103956403	CN		2017-02-15	Suzhou Beipeng Photoelectric Technology Co. Ltd.		☐

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NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Copy of International Search Report and Written Opinion for PCT/US2020/051733 mailed December 17, 2020.	☐
	2	Copy of Written Opinion of International Search Report for PCT/US2020/051733 dated December 17, 2020.	☐
	3	BEAUSOLEIL, Nanoelectronic and Nanophotonic Interconnect, The emerging integrated circuit interconnection bottleneck may be overcome if tiny, efficient photon-transport waveguides and small transceivers for photon-electron information exchange can be developed, 18 pages, January 29, 2007; revised September 25, 2007.	☐
	4	Copy of International Search Report and Written Opinion for PCT/US2021/050717 mailed December 6, 2021.	☐
	5	B. F. LEVIN et al., 1 Gb/s Si High Quantum Efficiency Monolithically Integrable, Applied Physics Letters, AIP Publishing LLC, Vol. 66, No. 22, May 29, 1995, Pages 2984-2986.	☐
	6	GAO YANG et al., Photon-trapping Microstructures Enable High-speed High-efficiency Silicon Photodiodes, Nature Photonics, Vol. 11, No. 5, April 3, 2017, Pages 301-308.	☐
If you wish to add additional non-patent literature document citation information please click the Add button			

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Examiner Signature	/EDUARDO A RODELA/	Date Considered	05/07/2024

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8022390		2011-09-20	Kim et al.	
	2	8680591		2014-03-25	Haddad et al.	
	3	9299865		2016-03-29	Marty et al.	
	4	9871147		2018-01-16	Kotani et al.	
	5	10600930		2020-03-24	Suzuki et al.	
If you wish to add additional U.S. Patent citation information please click the Add button.						
U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20120313204		2012-12-13	Haddad et al.	

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	2	20130167915		2013-07-14	Moslehi et al.	
	3	20170141243		2017-05-18	Kotani et al.	
	4	20170263798		2017-09-14	Suzuki et al.	
	5	20200075656		2020-03-05	Lee et al.	
	6	20200083389		2020-03-12	Wu et al.	
	7	20200083390		2020-03-12	Wu et al.	
	8	20200266231		2020-08-20	Cheng et al.	
	9	20200266232		2020-08-20	Cheng et al.	
	10	20110156195		2011-03-30	Tivarus et al.	
	11	20120153127		2012-06-21	Hirigoyen et al.	
	12	20120012741		2012-01-19	Vasylyev	

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	13	20180012918		2018-01-11	Na et al.	
	14	20180102442		2018-04-12	Wang et al.	
	15	20190166317		2019-05-30	Tanaka et al.	

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	1							☐

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NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	E. PONIZOVSKAYA DEVINE et al., Single Microhole per Pixel in CMOS Image Sensors with Enhanced Optical Sensitivity in Near-Infrared, IEEE Sensors Journal, 2021, pages 1-7.	☐
	2	CHANG-FU HAN et al., Deep Trench Isolation and Inverted Pyramid Array Structures Used to Enhance Optical Eciency of Photodiode in CMOS Image Sensor via Simulations, Department of Mechanical Engineering, National Cheng Kung University, Tainan 701, Taiwan, May 28, 2020, pages 1-14.	☐
	3	JONGHOON PARK et al., Pixel Technology for Improving IR Quantum Efficiency of Backside-illuminated CMOS Image Sensor, 1System LSI Division, Samsung Electronics Co., Ltd, 2Foundry Division, Samsung Electronics Co., Ltd. Yongin-city, Gyeonggi-do, Korea, 4 pages. June 2019. /EAR/	☐

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	4	SOZO YOKOGAWA, Nanophotonics Contributions to State-of-the-art CMOS Image Sensors, Sony Semiconductor Solutions Corporation, Kanagawa, Japan, 2019, 4 pages.	☐
	5	SOZO YOKOGAWA et al., IR Sensitivity Enhancement of CMOS Image Sensor with Diffractive Light Trapping Pixels, Scientific Reports, Sony Semiconductor Solutions Corporation, Atsugi Tec., 4-14-1 Asahi-cho, Atsugi, Kanagawa, 243-0014, Japan, June 19, 2017, 9 page.	☐
	6	Copy of International Search Report for PCT Application No. PCT/US20/51733, mailed December 17, 2020.	☐

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EXAMINER SIGNATURE

Examiner Signature	/EDUARDO A RODELA/	Date Considered	05/07/2024

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	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIP

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2024-03-13
Name/Print	Ivan S. Kavrukov	Registration Number	25,161

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/385,213	10/30/2023	Shih-Yuan WANG	309-0015USCIP	7381

139982 7590 04/12/2024

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER	
RODELA, EDUARDO A	

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
04/12/2024	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

Applicant-Initiated Interview Summary	**Application No.** 18/385,213	**Applicant(s)** WANG et al.		
	Examiner Eduardo A Rodela	**Art Unit** 2893	**AIA (First Inventor to File) Status** Yes	**Page** 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	**Title**	**Type**
Eduardo A Rodela	Primary Examiner	Telephonic
Ivan Kavrukov	Attorney of Record	

Date of Interview: 09 April 2024

Issues Discussed:

Proposed Amendment(s)

Examiner stated that Applicant needs to file the claims, since the claims are not in condition for allowance. Examiner further stated that in order to preclude 112 rejections, the claims need to include both 1. the material system of either of silicon, germanium or SiGe, and 2. the most basic of device structure of the P-I-N diode arrangement. The claimed pillars and holes should be tied to the device structure.

☑ Attachment

	/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893

Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

13. An integrated structure comprising:

an array of pillars of semiconductor material at least some of which are configured as photodetectors that have respective light-receiving surfaces and have sides;

wherein said photodetectors are configured to respond to illumination with light in selected visible and infrared wavelength ranges by generating electrical charge carriers;

one or more holes that are deliberately formed into the light-receiving surface of each of at least some of said photodetectors, have elongated and/or other shapes at said light-receiving surfaces, extend into the photodetectors to a depth of 100 to10000 nm, and are filled at least partly with solid dielectric material;

side-isolation comprising solid material at said sides of at least some of the photodetectors;

a solid dielectric material forming a base dielectric region for said array; and

electrical contacts configured to provide electrical pathways to said photodetectors, including for selected reverse-biasing of the photodetectors;

wherein the presence of said one or more holes in each of the photodetectors increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to an otherwise like photodetectors lacking said holes.

14. The integrated structure of claim 13, wherein said array of photodetectors is monolithically integrated with SI electronic devices.

15. The integrated structure of claim 14, wherein each of at least some of said photodetectors includes a least one of said holes with elongated shapes at the light-receiving surface thereof.

16. The integrated structure of claim 14, wherein each of at least some of said photodetectors includes a plurality of said holes with elongated shapes at the light receiving surface thereof.

17. The integrated structure of claim 14, wherein in each of at least some of said photodetectors at least some of said holes with elongated shapes have closed contours at the light receiving surface thereof and said closed contours are spaced inwardly from an outline of the light receiving surface.

18. The integrated structure of claim 14, in which each of at least some of the photodetectors includes a P-doped portion, and N-doped portion, and a portion that is between the P-doped and N-doped portions and is less doped therefrom or is undoped.

19. The integrated structure of claim 13, wherein each of at least some of said photodetectors includes at least one of said holes with elongated shapes at the light receiving surface thereof.

20. The integrated structure of claim 13, wherein each of at least some of said photodetectors includes a plurality of said holes with elongated shapes at the light receiving surface thereof.

21. The integrated structure of claim 13, wherein in each of at least some of said photodetectors at least some of said holes with elongated shapes have closed contours at the light receiving surface thereof and said closed contours are spaced inwardly from an outline of the light receiving surface.

22. The integrated structure of claim 13, in which each of said photodetectors includes a first doped portion and an undoped or less doped portion.

23. The integrated structure of claim 22, in which each of at least some of the photodetectors includes a second doped portion, wherein the undoped or less

doped portion is between the first and second doped portions and the first doped portion is P-doped and the second doped portion is N-doped.

24. The integrated structure of claim 13, in which said electrical contacts are configured to provide electrical fields across at least some of said photodetectors.

25. The integrated structure of claim 1, in which two or more of said photodetectors share at least some of said electrical contacts.

26. The integrated structure of claim 13, wherein said array of photodetectors is monolithically integrated with SI electronic devices that include devices for signal processing and transmission.

27. The integrated structure of claim 13, wherein at least some of said holes are configured as elongated trenches at said light-receiving surfaces.

28. The integrated structure of claim 27, in which at least some of said elongated trenches have widths at said light-receiving surfaces no greater than a wavelength of visible and/or infrared light illuminating said photodetectors.

29. The integrated structure of claim 27, in which at least some of said elongated trenches crisscross.

30. The integrates structure of claim 27, in which said array of photodetectors is monolithically integrated with Si electronic devices that include CMOS devices.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
18/385,213	**04/10/2024 12:59:41 PM Z ET**	**309-0015USCIP**

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	7381	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	65037490	FILING DATE	10/30/2023
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIP_PetitionForEOT.pdf	2	Extension of Time	295 KB
309-0015USCIP_Amendment_IRT_NFOA-04-10-2024--Signed.pdf	11	Amendment Copy Claims/Response to Suggested Claims	3536 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)

309-0015USCIP_PetitionForEOT.pdf	24E8DA0B3C2C336A3B64438A583CF1CC50C085EC36D92BDDA78F60DAA3DE45F4C94A81E61782C6E78DB12ABE8BD9C3DF9B3DECD03094BADA6427CA75243DA959
309-0015USCIP_Amendment_IRT_NFOA-04-10-2024--Signed.pdf	58A1B73AD6AD5D370056EACAC89A1018684A0C3EE2624A44256045E7F60CCE9AAD08CA50634E88D32279E17199C349888FAFF856D042148FC60456A63434C2C5

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/22 (11-23)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)	Docket Number (Optional) 309-0015USCIP
Application Number 18/385,213	Filed October 30, 2023
For MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	
Art Unit 2893	Examiner EDUARDO A RODELA

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

		Fee	Small Entity Fee	Micro Entity Fee	
☑	One month (37 CFR 1.17(a)(1))	$220	$88	$44	$ 88.00
☐	Two months (37 CFR 1.17(a)(2))	$640	$256	$128	$
☐	Three months (37 CFR 1.17(a)(3))	$1,480	$592	$296	$
☐	Four months (37 CFR 1.17(a)(4))	$2,320	$928	$464	$
☐	Five months (37 CFR 1.17(a)(5))	$3,160	$1,264	$632	$

☑ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number 600125.

☑ Payment made via USPTO patent electronic filing system.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 25,161.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Ivan S. Kavrukov/ — Signature

April 10, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

(917) 945-0121 — Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☐ * Total of _____ forms are submitted.

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0031. Public burden for this form is estimated to average 6 minutes per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS**. If filing this completed form by mail, send to: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

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Privacy Act Statement

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1) law enforcement, in the event that the system of records indicates a violation or potential violation of law;
2) a federal, state, local, or international agency, in response to its request;

3) a contractor of the USPTO having need for the information in order to perform a contract;

4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record;

5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record;

6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations;

7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals;

8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c));

9) the Office of Personnel Management (OPM) for personnel research purposes; and

10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
18/385,213	04/10/2024 12:59:41 PM Z ET	309-0015USCIP

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	7381	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	65037490	AUTHORIZED BY	Ivan Kavrukov
CUSTOMER #	139982	FILING DATE	10/30/2023
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Shih-Yuan WANG

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 2892	E202440D05177857	Mary Ellen Finnegan
PRE-AUTHORIZED ACCOUNT	PRE-AUTHORIZED CATEGORY	
600125	37 CFR 1.21 (Miscellaneous fees and charges)	

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2251	EXTENSION FOR RESPONSE WITHIN FIRST MONTH	88.00	1	88.00
			TOTAL AMOUNT:	$88.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Shih-Yuan WANG et al.
Serial No.:	18/385,213
Examiner:	EDUARDO A RODELA
Group Art Unit:	2893
Filing Date:	October 30, 2023
Conf. No.:	7381
For:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, New York 10001

CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: April 10, 2024

I hereby certify that this correspondence is being transmitted via Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the Office Action dated January 5, 2024, please amend the above-identified application as follows:

Amendments to the Claims begin on page 2.

Remarks begin on page 5.

Amendment to Claims:

This listing of claims will replace all prior versions and listings of the claims in the application.

Claims 1-12 (canceled)

13. (new) An integrated structure comprising:

an array of pillars comprising Si, Ge, and/or SiGe alloy semiconductor material wherein at least some of the pillars are configured as photodetectors that have respective light-receiving surfaces and have sides;

wherein at least some of the photodetectors comprise P-doped and N-doped regions and regions therebetween and are configured to respond to illumination with light in selected visible and infrared wavelength ranges by generating electrical charge carriers;

one or more holes that are deliberately formed into the light-receiving surfaces, have elongated and/or other shapes at said light-receiving surfaces, extend into the photodetectors to a depth of 100 to10000 nm, and are filled at least partly with solid dielectric material;

side-isolation comprising solid material at said sides of at least some of the photodetectors;

a solid dielectric material forming a base dielectric region for said array; and

electrical contacts configured to provide electrical pathways to at least some of the photodetectors, including for selected reverse-biasing thereof;

wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to an otherwise like photodetectors lacking said holes.

14. (new) The integrated structure of claim 13, wherein said array of photodetectors is monolithically integrated with SI electronic devices.

15. (new) The integrated structure of claim 14, wherein each of at least some of said photodetectors includes a least one of said holes with elongated shapes at the light-receiving surface thereof.

16. (new) The integrated structure of claim 14, wherein each of at least some of said photodetectors includes a plurality of said holes with elongated shapes at the light receiving surface thereof.

17. (new) The integrated structure of claim 14, wherein in each of at least some of said photodetectors at least some of said holes with elongated shapes have closed contours at the light receiving surface thereof and said closed contours are spaced inwardly from an outline of the light receiving surface.

18. (new) The integrated structure of claim 14, in which said regions that are between the P-doped and N-doped regions are less doped than at least one of the P-doped and the N-doped regions or are undoped.

19. (new) The integrated structure of claim 13, wherein each of at least some of said photodetectors includes at least one of said holes with elongated shapes at the light receiving surface thereof.

20. (new) The integrated structure of claim 13, wherein each of at least some of said photodetectors includes a plurality of said holes with elongated shapes at the light receiving surface thereof.

21. (new) The integrated structure of claim 13, wherein said holes with elongated shapes have closed contours at said light receiving surfaces and said closed contours are spaced inwardly from outlines of the light receiving surfaces.

22. (new) The integrated structure of claim 13, in which said regions between the P-doped and N-doped regions are undoped or less doped than at least one of the P-doped and N-doped regions.

23. (new) The integrated structure of claim 22, in which the P-doped regions and N-doped regions are configured such that either the P-doped regions intercept said light before the N-doped regions or the N-regions intercept the light before the P-regions.

24. (new) The integrated structure of claim 13, in which said electrical contacts are configured to provide electrical fields across at least some of said photodetectors.

25. (new) The integrated structure of claim 13, in which two or more of said photodetectors share at least some of said electrical contacts.

26. (new) The integrated structure of claim 13, wherein said SI electronic devices include devices for signal processing and transmission.

27. (new) The integrated structure of claim 13, wherein at least some of said holes are configured as elongated trenches at said light-receiving surfaces.

28. (new) The integrated structure of claim 27, in which at least some of said elongated trenches have widths at said light-receiving surfaces no greater than a wavelength of the visible and/or infrared light illuminating said photodetectors.

29. (new) The integrated structure of claim 27, in which at least some of said elongated trenches crisscross.

30. (new) The integrates structure of claim 27, in which said array of photodetectors is monolithically integrated with Si electronic devices that include CMOS devices.

REMARKS

This paper follows brief telephone interviews with Examiner Eduardo A Rodela on March 15 and April 9, 2024. The substance of the first interview is recorded in the Examiner Interview Summary Record dated March 20, 2024 and included the Examiner's suggestion to refer in the independent claim to Si, Ge, and/or SiGe alloys.

In the first interview, Applicant's representative pointed to the following figures as examples of support for claim elements: FIGs. 5A-B, 49, 46, 9D, 4B-3B, and 57A-B. For the Examiner's convenience, a copy of these FIGs. is attached to this paper. Proposed claims were briefly discussed as well as priority for claims 13-26 to ultimate parent patent 10,622,498 that in turn claims priority to PCT/US14/39208 filed 05/22/2014 with provisionals including 61/834,873 filed 06/13/2013. Support for claim 2 further includes the sentence bridging pages 1 and 2 of said provisional. Dependent claims 27-30 claim later priority -- to an indirect parent patent 11,121,271 filed 08/01/2019 (paragraph 270 and FIGs. 57A-B in the subject application are carried from this indirect parent).

The second Interview briefly recounted the first interview and further included a suggestion by the Examiner to add in the sole independent claim 13 not only a reference to the nature of the semiconductor material but also a reference to P-doping and N-doping of regions.

Claim 13 submitted herewith is the claim briefly discussed in the first interview except that per the Examiner's suggestion the claim now refers to (1) "Si, Ge, and/or SiGe alloys," and (2) "P-doped and N-doped regions and regions therebetween." The claim also includes some clarifying edits, Dependent claims 18, 22, and 23 are edited to conform to the language added to claim 13.

Applicant invites the Examiner to call the undersigned if it appears that a call might help advance prosecution.

Please charge any shortfall and credit any overpayments to our Deposit Account number 600125.

Respectfully Submitted,

WISSING MILLER LLP
Attorney for Applicants

By: /Ivan S. Kavrukov/
Ivan S. Kavrukov
Reg. No. 41,943
Tel. (917) 945-0121

Address: (associated with Customer Number: 139982)

Attachment: Copy of FIGs. 5A-B, 49, 46, 9D, 4B-3B, and 57A-B.

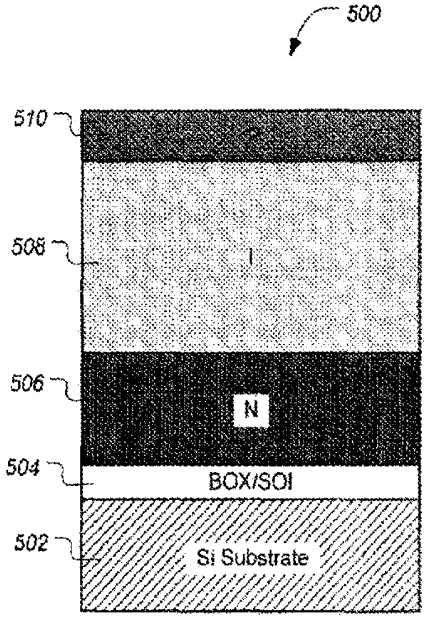

500
510
508
I
506
N
504
BOX/SOI
502
Si Substrate

FIG. 5A

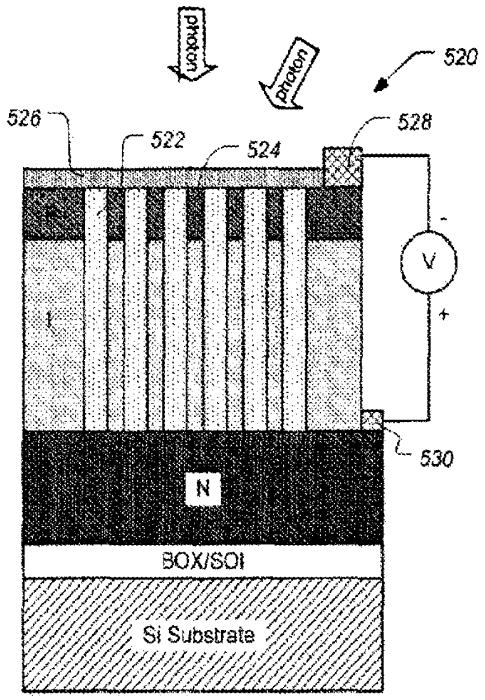

photon
photon
520
526
522
524
528
P
I
N
V
-
+
530
BOX/SOI
Si Substrate

FIG. 5B

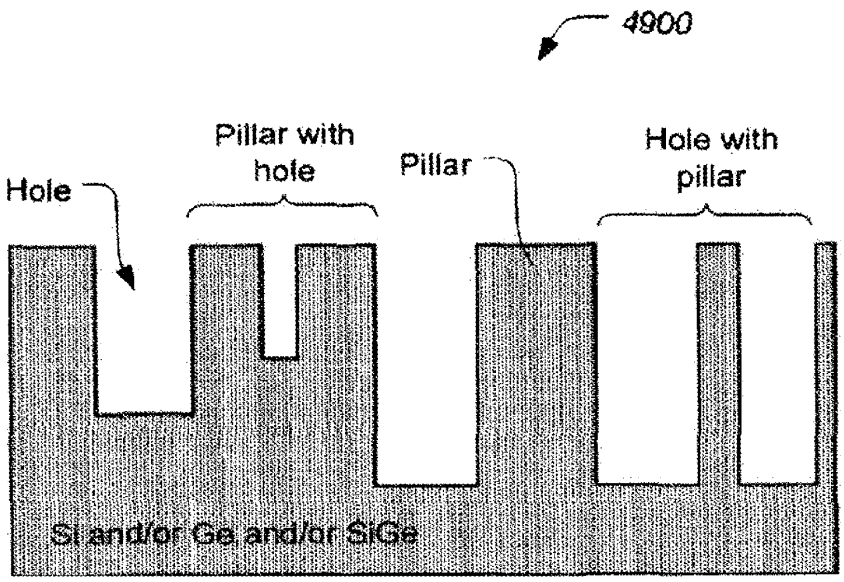

4900
Hole
Pillar with hole
Pillar
Hole with pillar
Si and/or Ge and/or SiGe

FIG. 49

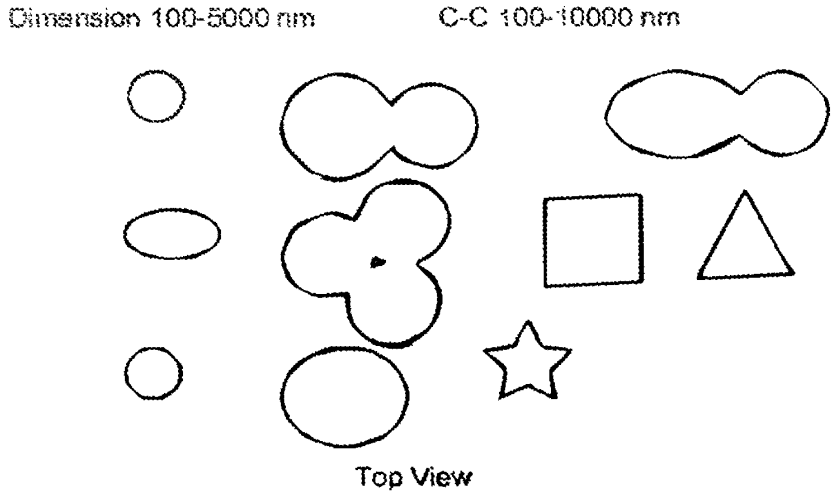

Dimension 100-5000 nm
C-C 100-10000 nm
Top View

FIG. 46

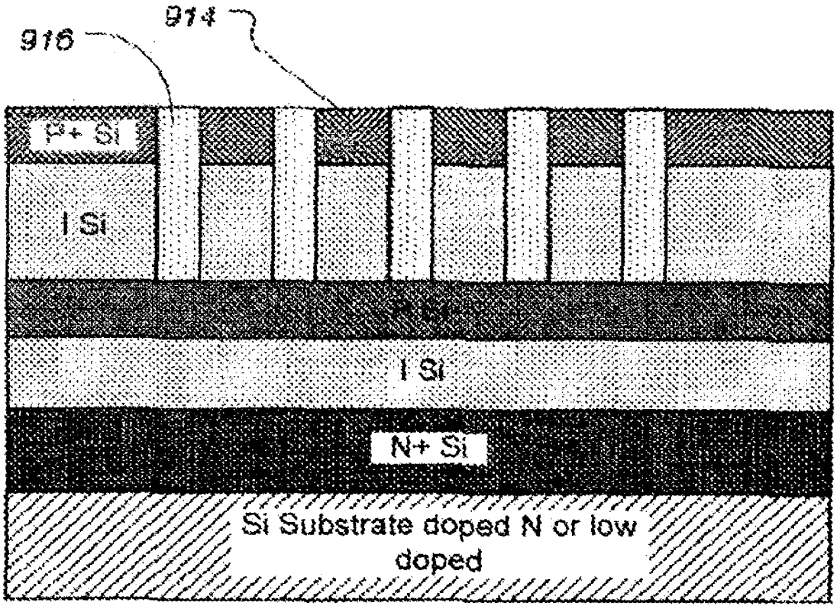


FIG. 9D

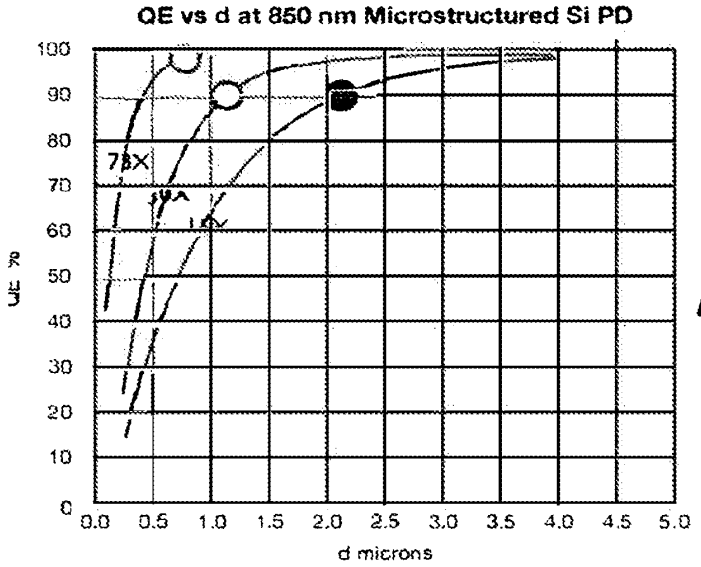


FIG. 4B

420

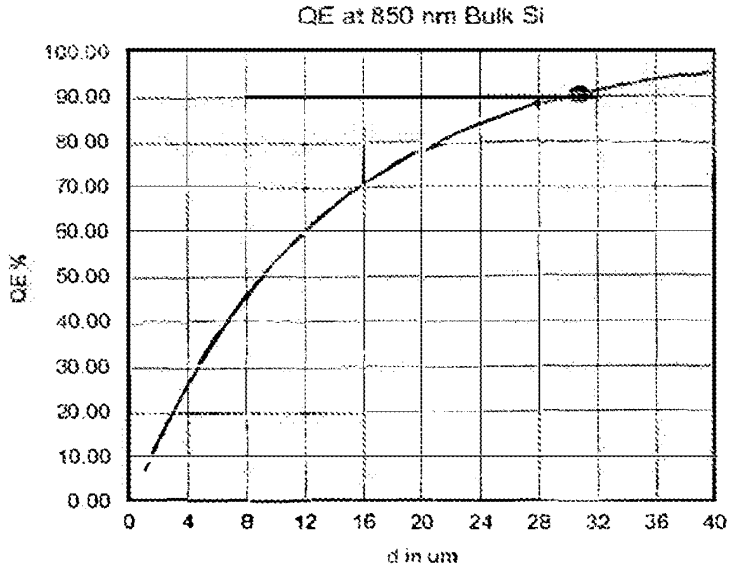


FIG. 3B
(prior art)

312

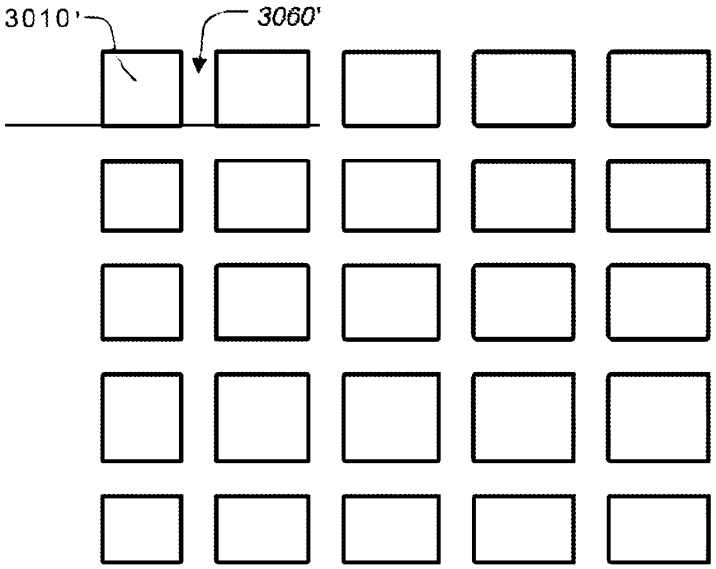


FIG. 57A

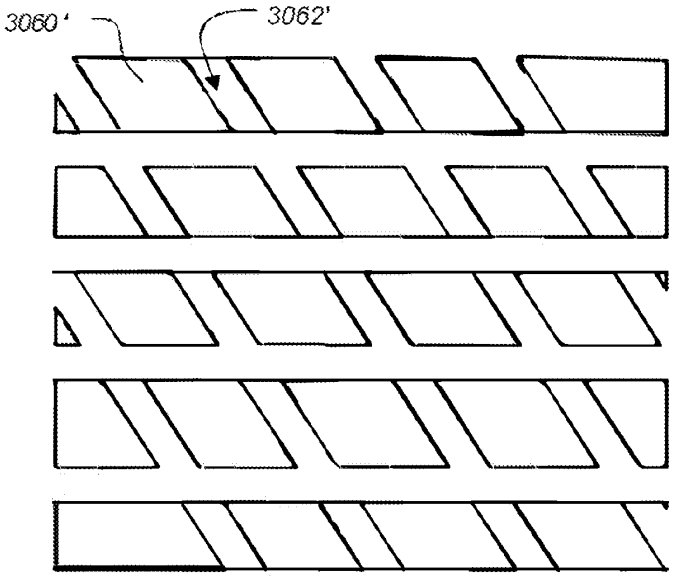


FIG. 57B

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 18/385,213	Filing Date 10/30/2023	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $40 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $ 192 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	04/10/2024	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0		x $40 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $ 192 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	SLIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/APRIL L. WALKER/
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The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/385,213	10/30/2023	Shih-Yuan WANG	309-0015USCIP	7381

139982 7590 03/20/2024

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER	
RODELA, EDUARDO A	

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
03/20/2024	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

Applicant-Initiated Interview Summary	**Application No.** 18/385,213	**Applicant(s)** WANG et al.		
	Examiner Eduardo A Rodela	**Art Unit** 2893	**AIA (First Inventor to File) Status** Yes	**Page** 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	**Title**	**Type**
Eduardo A Rodela	Primary Examiner	Telephonic
Ivan Kavrukov	Attorney of Record	

Date of Interview: 15 March 2024

Issues Discussed:

Proposed Amendment(s)

Applicant, in response to the office action dated January 5, 2024, proposes to amend the claim set, by canceling claims 1-12, and submitting new claims 13-30. It was noted by Applicant's Representative that the content of claims 27-30 are supported by a later disclosure of an earlier Application which is now US 11,121,171. As the claims are newly presented to overcome the 112 issues raised in the last office action and other clarifying considerations, Examiner stated the need for further search and consideration to determine the next course of action. Examiner stated that the material systems of including silicon, germanium or SiGe limitation into the independent claim would prevent a 112(a) scope of enablement rejection in future filings.

	/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893

Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

PTO/SB/08a (02-18)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	18385213
	Filing Date	2023-10-20
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIP

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	11309444		2022-04-19	Wang et al.	
	2	8558336		2013-10-15	Su	
	3	10411053		2019-09-10	Yokogawa	
	4	10522582		2019-12-31	Maruyama et al.	
	5	9000492		2015-04-07	Suzuki et al.	
	6	6879014		2005-04-12	Wagner	
	7	7396696		2008-07-08	Kim	
	8	7525170		2009-04-28	Hsu	

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	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIP

	9	8129710		2012-03-06	Cho	
	10	8357960		2013-01-22	Dutta	
	11	8946675		2015-02-03	Yu	
	12	9184202		2015-11-10	Dutta	
	13	11211419		2021-12-28	Wu	
	14	11728457		2023-08-15	Sung	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20100320444		2010-12-23	Dutta	
	2	20110309331		2011-12-22	Yu et al.	
	3	20180182806		2018-06-28	Jin et al.	

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	4	20110156195		2011-06-30	Tivarus et al.	
	5	20120153127		2012-06-21	Hirigoyen et al.	
	6	20180012918		2018-01-11	Na et al.	
	7	20190166317		2019-05-30	Tanaka et al.	
	8	20120012741		2012-01-19	Vasylyev	
	9	20180102442		2018-04-12	Wang	
	10	20160240579		2016-08-18	Sun et al.	
	11	20170141153		2017-05-18	Lee et al.	
	12	20180102442		2018-04-12	Wang et al.	
	13	20200006407		2020-01-02	Yokogawa	
	14	20200006416		2020-01-02	Baba et al.	

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	15	20050145779		2005-07-07	Mochizuki et al.	
	16	20120153416		2012-06-21	Tanaka et al.	

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FOREIGN PATENT DOCUMENTS

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	1	20080101301	KR		2008-11-21	Dongbu Hitek Co. Ltd.		☐
	2	2002314116	JP		2002-10-25	Seiko Epson Corp.		☐
	3	0103255	WO		2001-01-11	Scott		☐
	4	2019018846	WO		2019-01-24	W&W Sens Devices Inc.		☐
	5	09040854	EP		1999-09-08	IBM United Kingdom Limited		☐
	6	2007013065	JP		2007-01-18	Matsushita Electric Works Ltd.		☐
	7	103956403	CN		2017-02-15	Suzhou Beipeng Photoelectric Technology Co. Ltd.		☐

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NON-PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Copy of International Search Report and Written Opinion for PCT/US2020/051733 mailed December 17, 2020.	☐
	2	Copy of Written Opinion of International Search Report for PCT/US2020/051733 dated December 17, 2020.	☐
	3	BEAUSOLEIL, Nanoelectronic and Nanophotonic Interconnect, The emerging integrated circuit interconnection bottleneck may be overcome if tiny, efficient photon-transport waveguides and small transceivers for photon-electron information exchange can be developed, 18 pages, January 29, 2007; revised September 25, 2007.	☐
	4	Copy of International Search Report and Written Opinion for PCT/US2021/050717 mailed December 6, 2021.	☐
	5	B. F. LEVIN et al., 1 Gb/s Si High Quantum Efficiency Monolithically Integrable, Applied Physics Letters, AIP Publishing LLC, Vol. 66, No. 22, May 29, 1995, Pages 2984-2986.	☐
	6	GAO YANG et al., Photon-trapping Microstructures Enable High-speed High-efficiency Silicon Photodiodes, Nature Photonics, Vol. 11, No. 5, April 3, 2017, Pages 301-308.	☐
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	1	8022390		2011-09-20	Kim et al.	
	2	8680591		2014-03-25	Haddad et al.	
	3	9299865		2016-03-29	Marty et al.	
	4	9871147		2018-01-16	Kotani et al.	
	5	10600930		2020-03-24	Suzuki et al.	
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U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20120313204		2012-12-13	Haddad et al.	

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	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIP

	2	20130167915		2013-07-14	Moslehi et al.	
	3	20170141243		2017-05-18	Kotani et al.	
	4	20170263798		2017-09-14	Suzuki et al.	
	5	20200075656		2020-03-05	Lee et al.	
	6	20200083389		2020-03-12	Wu et al.	
	7	20200083390		2020-03-12	Wu et al.	
	8	20200266231		2020-08-20	Cheng et al.	
	9	20200266232		2020-08-20	Cheng et al.	
	10	20110156195		2011-03-30	Tivarus et al.	
	11	20120153127		2012-06-21	Hirigoyen et al.	
	12	20120012741		2012-01-19	Vasylyev	

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	13	20180012918		2018-01-11	Na et al.	
	14	20180102442		2018-04-12	Wang et al.	
	15	20190166317		2019-05-30	Tanaka et al.	

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	1	E. PONIZOVSKAYA DEVINE et al., Single Microhole per Pixel in CMOS Image Sensors with Enhanced Optical Sensitivity in Near-Infrared, IEEE Sensors Journal, 2021, pages 1-7.	☐
	2	CHANG-FU HAN et al., Deep Trench Isolation and Inverted Pyramid Array Structures Used to Enhance Optical Eciency of Photodiode in CMOS Image Sensor via Simulations, Department of Mechanical Engineering, National Cheng Kung University, Tainan 701, Taiwan, May 28, 2020, pages 1-14.	☐
	3	JONGHOON PARK et al., Pixel Technology for Improving IR Quantum Efficiency of Backside-illuminated CMOS Image Sensor, 1System LSI Division, Samsung Electronics Co., Ltd, 2Foundry Division, Samsung Electronics Co., Ltd. Yongin-city, Gyeonggi-do, Korea, 4 pages.	☐

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	Attorney Docket Number	309-0015USCIP

	4	SOZO YOKOGAWA, Nanophotonics Contributions to State-of-the-art CMOS Image Sensors, Sony Semiconductor Solutions Corporation, Kanagawa, Japan, 2019, 4 pages.	☐
	5	SOZO YOKOGAWA et al., IR Sensitivity Enhancement of CMOS Image Sensor with Diffractive Light Trapping Pixels, Scientific Reports, Sony Semiconductor Solutions Corporation, Atsugi Tec., 4-14-1 Asahi-cho, Atsugi, Kanagawa, 243-0014, Japan, June 19, 2017, 9 page.	☐
	6	Copy of International Search Report for PCT Application No. PCT/US20/51733, mailed December 17, 2020.	☐

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	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIP

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☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

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Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2024-03-13
Name/Print	Ivan S. Kavrukov	Registration Number	25,161

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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 940 854 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
28.10.2009 Bulletin 2009/44

(51) Int Cl.:
H01L 27/144 *(2006.01)* ***H01L 31/0352*** *(2006.01)*
H01L 31/0312 *(2006.01)*

(21) Application number: **99301205.3**

(22) Date of filing: **18.02.1999**

(54) Si/SiGe optoelectronic integrated circuits

Si/SiGe optoelektronische integrierte Schaltungen

Si/SiGe circuits intégrés optoélectroniques

(84) Designated Contracting States:
DE FR GB

(30) Priority: **02.03.1998 US 76462 P**
19.06.1998 US 99978

(43) Date of publication of application:
08.09.1999 Bulletin 1999/36

(73) Proprietor: **International Business Machines Corporation**
Armonk, NY 10504 (US)

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(74) Representative: **Moss, Robert Douglas**
IBM United Kingdom Limited
Intellectual Property Department
Hursley Park
Winchester
Hampshire SO21 2JN (GB)

(56) References cited:
US-A- 5 525 828

- **RIEH J -S ET AL: "MONOLITHICALLY INTEGRATED SIGE-SI PIN-HBT FRONT-END TRANSIMPEDANCE PHOTORECEIVERS" PROCEEDINGS IEEE/CORNELL CONFERENCE ON ADVANCED CONCEPTS IN HIGH SPEED SEMICONDUCTORS DEVICES AND CIRCUITS, 4 - 6 August 1997, pages 322-331, XP002116931 Ithaca, NY ISSN: 1041-1135**
- **LIU M ET AL: "140 GHZ MSM PHOTODETECTORS IN SILICON-ON-INSULATOR" SUMMARIES OF PAPERS PRESENTED AT THE CONFERENCE ON LASERS AND ELECT OPTICS (CLEO), ANAHEIM, MAY 8 - 13, 1994, 8 May 1994 (1994-05-08), page 22 XP000601776 INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS**
- **ARAFA M ET AL: "A 70-GHZ FT LOW OPERATING BIAS SELF-ALIGNED P-TYPE SIGE MODFET" IEEE ELECTRON DEVICE LETTERS, vol. 17, no. 12, 1 December 1996 (1996-12-01), pages 586-588, XP000635369 ISSN: 0741-3106**
- **ARAFA M. ET AL: 'High speed P-type SiGe modulation-doped field-effect transistors' IEEE ELECTRON DEVICE LETTERS vol. 17, no. 3, 03 March 1996, pages 124 - 126, XP011018025**

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EP 0 940 854 B1

Description

[0001] This invention relates to semiconductors and more particularly to integrated optoelectronic receiver devices and circuits incorporating photodetectors and MODFETs formed with SiGe layers.

[0002] The advent of fiber-optic communications technology has increased the demand for high-speed optoelectronic devices and circuits that operate with data rates of greater than 1 Gbit/sec. In particular, a growing market exists for local area networks and short-haul optical connections that operate at wavelengths of $\lambda = 850$ nm. It would be desirable to fabricate these circuits monolithically due to the lower cost of production and performance advantages over discrete components. It would also be desirable to fabricate such circuits entirely in a silicon-based technology due to the reduced cost arising from their compatibility with existing Si-based technologies including CMOS logic circuits.

[0003] In the prior art, GaAs has been the previous choice for monolithically integrated optical receivers operating at $\lambda = 850$ nm. This is due to the favorable intrinsic material properties of GaAs; the absorption length for 850 nm-radiation in GaAs is $\alpha^{-1} = 1$ μm, and the electron mobility in GaAs is roughly 8500 cm^2/Vs at room temperature. J. S. Wang et al., IEEE Phot. Tech. Lett. 5, 316 (1993) demonstrated the fabrication of high-speed integrated photoreceiver circuits composed of GaAs metal-semiconductor-metal (MSM) photodiodes and MESFETs with -3 dB bandwidths as high as 11 GHz at $\lambda =$ 850 nm. Further improvement of GaAs-based receiver performance has been obtained using GaAs MSM photodetectors integrated with AlGaAs/GaAs modulation-doped field effect transistors (MODFETs). V. Hurm et al., Electron. Lett. 29, 9 (1993) demonstrated photoreceiver circuits of this type with -3 dB bandwidths as high as 14 GHz at $\lambda = 850$ nm.

[0004] In order to replace GaAs, an integrated Si-based technology must have comparable performance to GaAs and a relatively low-cost process. However, the intrinsic material properties of Si are much less favorable compared to GaAs. The absorption length in Si for 850 nm-radiation is $\alpha^{-1} = 20$ μm, which is over an order of magnitude longer than in GaAs. Therefore, for a Si photodetector to have high responsivity it must have a thick absorbing region making the detector very slow, and for high speed the absorbing region should be very thin resulting in an extremely poor responsivity. For instance, Y. S. He et al., Electron. Lett. 29, 9 (1993) demonstrated the operation of a lateral p-i-n photodiode integrated with a Si NMOS technology with a responsivity of 0.48 A/W at $\lambda = 870$ nm, but with a -3 dB bandwidth of only 900 MHz. Moreover, these results were only made possible by using ultra-high purity Si, and an extremely large bias voltage of 30 V. On the other hand, M. Y. Liu et al., Appl. Phys. Lett. 65, 887 (1994) demonstrated operation of a Si on insulator (SOI) MSM photodiode with an absorbing region thickness of only 0.1 μm that had a bandwidth over 100 GHz, but a severely-degraded responsivity at $\lambda = 780$ nm of 0.0057 A/W. Improvements in the bandwidth/responsivity tradeoff of Si photodiodes are possible, for instance, in U.S. Pat. No. 5,589,704 which was issued on Dec. 31, 1996 to B. F. Levine, the responsivity of an MSM detector was shown to increase by a factor of close to 4 by roughening the surface of a Si epi-layer grown on an SOI wafer. However such a technique is limited to use with SOI substrates, and may not be suitable for practical applications due to the complexities of the roughening process. Si photodetectors are further hindered by the fact that the electron mobility in Si/SiO_2 inversion layers is several times lower than GaAs at room temperature, and the frequency performance and gain of Si NMOS devices is considerably poorer compared to GaAs MESFETs.

[0005] In U.S. Pat. No. 5,525,828 which was issued on Jun. 11, 1996 to E. Bassous et al., it was noted that the speed and/or responsivity of Si MSM photodetectors could be increased by adding a certain percentage of Ge to the absorbing layer. Increasing the percent Ge-composition of $Si_{1-x}Ge_x$ alloy decreases the absorption length, and increases the electron and hole mobilities thereby leading to potentially faster devices.

[0006] It has also been shown that field-effect transistors fabricated on $Si/Si_{1-x}Ge_x$ layer structures offer considerable advantages over bulk Si transistors. For n-channel MODFETs incorporating tensile-strained $Si/Si_{1-x}Ge_x$ quantum wells, frequency performance is considerably better than Si MOSFETs for a given gate length device. Similar performance advantages can be obtained in p-channel MODFETs fabricated on compressive-strained $Si_{1-y}Ge_y/Si_{1-x}Ge_x$ quantum wells. For instance, M. Arafa et al., IEEE Electron. Dev. Lett. 17, 586 (1996) obtained unity current-gain cutoff frequencies of 70 GHz for 0.1 μm gate length p-channel transistors fabricated on compressive-strained $Si_{0.7}Ge_{0.3}/Si_{0.3}Ge_{0.7}$ heterostructures. In U.S. Pat. No. 5,659,187 which was issued on Aug. 19, 1997 to F. K. Legoues and B.S. Meyerson, it was shown that a low-defect density layer of relaxed $Si_{1-x}Ge_x$, with arbitrary Ge composition can be grown on a lattice-mismatched substrate using an intermediate graded-composition buffer layer where strain has been relieved in the buffer layer or below via activation of modified Frank Read sources which is a mechanism to generate new dislocations. This work demonstrated the practicality of producing devices and circuits using Si/SiGe heterostructures grown on a SiGe graded composition buffer layer on Si substrates. Finally, U.S. Pat. No. 5,534,713 which was issued on Jul. 9, 1996 to K. Ismail and F. Stern showed that complementary logic circuits could be fabricated using high-mobility electron and hole channels fabricated in strained Si/SiGe layers grown on relaxed SiGe buffer layers.

[0007] Despite the apparent advantages of SiGe technology over bulk Si for photodetectors, MODFETs, and CMOS logic circuits, the concept of combining these devices to form integrated photoreceiver circuits has not

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been suggested, nor has a clear method for monolithically integrating these structures in such a way as to allow high-frequency operation and low cost Si manufacturing been suggested.

[0008] It is an object of the present invention to provide a simple means of monolithically integrating a photodetector with high speed and responsivity with a microwave transistor on a Si substrate in such a way as to allow high frequency performance better than Si and comparable to that achievable in GaAs.

[0009] It is a further object of this invention to provide a method for fabricating an optoelectronic integrated circuit using a process that is fully compatible with standard Si processing.

[0010] It is still a further object of this invention to provide a means for monolithically integrating a high-speed photoreceiver circuit with a practical CMOS logic manufacturing technology.

[0011] According to the present invention provides a semiconductor structure according to claim 1.

[0012] The semiconductor structure includes spaced apart drain and source regions extending to the quantum well layer and a Schottky gate contact to control charge in the conducting channel to form a MODFET. Portions of the quantum well layer, said undoped $Si_{1-y}Ge_y$ spacer layer and said doped $Si_{1-y}Ge_y$ supply layer are removed to expose said relaxed $Si_{1-y}Ge_y$ layer wherein electrodes are formed on said exposed relaxed $Si_{1-y}Ge_y$ layer to form a photodetector. The quantum well layer is under tensile strain and consists of Si. The electrodes include two or more interdigitated Schottky electrodes. y is in the range from 0.2 - 0.35.

[0013] Preferably, further included is a trench extending through said exposed relaxed $Si_{1-y}Ge_y$ layer surface and surrounding said photodetector. The trench is filled with material including dielectric material. Further included is a layer of Si over said doped $Si_{1-y}Ge_y$ supply layer. Preferably, the doped $Si_{1-y}Ge_y$ supply layer is n-type. The positively-biased electrodes of said photodetector provide Schottky contacts with barrier height for holes that is greater than half the band gap of said exposed relaxed $Si_{1-y}Ge_y$ layer, and negatively-biased electrodes of said photodetector provide Schottky contacts with barrier height for electrons that is greater than half the band gap of said exposed relaxed $Si_{1-y}Ge_y$ layer. The negatively-biased electrodes of said photodetector provide Schottky contacts with barrier height for electrons that is greater than half the band gap of said exposed relaxed $Si_{1-y}Ge_y$ layer, and positively-biased electrodes of said photodetector form Ohmic contact to an n-type doped region. Negatively-biased electrodes of said photodetector form Ohmic contacts to a p-type doped region and said positively-biased electrodes of said photodetector form an Ohmic contact to an n-type doped region.

[0014] Preferably, said substrate is heavily-doped greater than 10^{18} atoms/cm^3 and said substrate is an SOI substrate comprising a thick Si layer, a SiO_2 layer, and a Si overlayer. The substrate is lightly-doped Si, and the region of said substrate underneath said photodetector is heavily-doped greater than 10^{18} atoms/cm^3.

[0015] Preferably, said photodetector absorbing region is bordered by deep trenches extending from said photodetector surface down to said Si substrate, and filled with a dielectric material, so as to prevent photogenerated carriers generated in said $Si_{1-y}Ge_y$, buffer layer from diffusing laterally past said deep trenches.

[0016] Preferably, further included are spaced apart drain and source regions extending to said quantum well layer, a gate dielectric layer above said supply layer between said drain and source and a gate electrode above said dielectric layer to form a MOSFET. Further included are first and second spaced apart doped regions, one above the other, with a portion of said relaxed $Si_{1-y}Ge_y$ layer there between to form a photodetector and an Ohmic contact to said respective first and second doped regions for applying a potential there between and further included is a trench extending into said exposed relaxed $Si_{1-y}Ge_y$ layer to provide a barrier to electrical charge. The first doped region includes a region of said quantum well layer, said undoped $Si_{1-y}Ge_y$ spacer layer and said doped $Si_{1-y}Ge_y$ supply layer. The second doped region includes a region of said substrate.

[0017] The invention further provides a method of forming semiconductor structure as claimed in claim 15.

[0018] Preferably, further included is the step of doping said substrate underneath said photodetector greater than 10^{18} atoms/cm^3, the steps of forming spaced apart drain and source regions extending to said quantum well layer, forming a gate dielectric layer above said supply layer between said drain and source and forming a gate electrode above said dielectric layer to form a MOSFET, the steps of forming first and second spaced apart doped regions, one above the other with a portion of said relaxed $Si_{1-y}Ge_y$ layer there between to form a photodetector and forming an Ohmic contact to said respective first and second doped regions for applying a potential therebetween, the step of forming a trench extending through said exposed relaxed $Si_{1-y}Ge_y$ layer to provide a barrier to electrical charge, and wherein the step of forming said second doped region includes the step of doping said substrate.

[0019] These and other features, objects, and advantages of the present invention will become apparent upon consideration of the following detailed description of the invention when read in conjunction with the drawing in which:

Figs. 1A - 1E are cross-sectional diagrams of the fabrication sequence of one embodiment of the invention where a metal-semiconductor-metal (MSM) photodetector and an n-channel modulation-doped field effect transistor (MODFET) are integrated using an epitaxially-grown Si/SiGe heterostructure.

Fig. 2 is a circuit diagram of a simple photoreceiver circuit.

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Fig. 3 is a cross-sectional diagram of a second embodiment of the invention, where an n-channel Si/SiGe MODFET is integrated with a SiGe MSM photodetector with planar, deep trench isolation.

Fig. 4A is a cross-sectional diagram of a not claimed semiconductor structure where the absorbing layer is composed of a symmetrically-strained superlattice, and Fig. 4B is an energy-band diagram of the absorbing layer in Fig. 4A.

Fig. 5 is a cross-sectional diagram of a not claimed semiconductor structure where an MSM photodetector and a p-channel MODFET are integrated using an epitaxially-grown Si/SiGe heterostructure.

Fig. 6A is a cross-sectional diagram of a further embodiment of the invention where the positively (negatively) biased electrode of the MSM photodetector is composed of a material with high Schottky barrier for holes (electrons). Fig. 6B is a cross-sectional diagram of a further embodiment of the invention where the negatively biased photodetector electrode is composed of a material with high Schottky barrier for electrons, and the positively biased electrode is composed of an n-type Ohmic contact. Fig. 6C is a cross-sectional diagram of a further embodiment of the invention where the positively (negatively) biased photodetector electrode is composed of an n-type (p-type) Ohmic contact.

Fig. 7A is a cross-sectional diagram of an further embodiment of the invention where the substrate is an SOI wafer. Fig. 7B is a cross-sectional diagram of a further embodiment of the invention where the substrate is a heavily-doped n- or p-type Si wafer. Fig. 7C shows a cross-sectional diagram of a further embodiment of the invention where the substrate has a heavily-doped implanted region located directly underneath the MSM photodetector.

Fig. 8A shows a cross-sectional view along the line 8A-8A of Fig. 8B. Fig. 8B shows a top view of a SiGe MSM photodetector. Fig. 8C is a graph of the normalized photoresponse versus frequency of the SiGe MSM photodetector shown in Figs. 8A and 8B.

Fig. 9 is a graph of current gain and of maximum available gain plotted versus frequency for an n-channel Si/SiGe MODFET.

Fig. 10 is a cross-sectional diagram of a not claimed example of a semiconductor structure where a vertical p-i-n photodetector and an n-channel MODFET are integrated using an epitaxially-grown Si/SiGe heterostructure.

Fig. 11 is a cross-sectional diagram of a further embodiment of the invention where an MSM photodetector and an n-channel modulation-doped MOSFET are integrated using a standard self-aligned polygate, salicide process.

Fig. 12 is a cross-sectional diagram of a not claimed example of a semiconductor structure where an MSM photodetector and a strained Si n-MOSFET are integrated using a planar fabrication process.

Fig. 13 is a cross-sectional diagram of a not claimed example of a semiconductor structure where an MSM photodetector is integrated with both an n-channel and a p-channel MODFET using an epitaxially-grown Si/SiGe heterostructure.

[0020] Figs. 1A-1E show the fabrication sequence for one embodiment of the invention where an n-channel, Si/SiGe modulation-doped field effect transistor (MODFET) 15 is integrated with a SiGe metal-semiconductor-metal (MSM) photodetector. A typical layer structure is shown in Fig. 1A. The layers are epitaxially grown on a Si substrate 1 using a high-precision epitaxy technique such as molecular beam epitaxy, rapid thermal chemical vapor deposition, or ultra high vacuum chemical vapor deposition (UHV-CVD). Substrate 1 may also be SiGe, Ge, GaAs, SiC, SOS and SOI. Suitable adjustments will be required to accomodate a different substrate lattice constant compared to Si. The following description is directed to a Si substrate. For a description of how to grow epitaxial Si and $Si_{1-x}Ge_x$ layers by UHV-CVD, reference is made to U.S. Pat. No. 5,298,452 which was issued on Mar. 29, 1994 to B. S. Meyerson. For $Si_{1-x}Ge_x$ layers, GeH_4 is added to Si-containing gas such as SiH_4 or Si_2H_6 in the UHV-CVD reactor. Ge is incorporated into the crystal lattice in place of Si during formation of the layer in the amount or proportion of x. Layer 2 comprises a $Si_{1-x}Ge_x$ buffer layer that has a thickness in the range from 0.2 to 1.5 μm, with a preferred value of about 0.5 μm, and has a percent Ge composition that is increased from x = 0 (in a continuous or stepwise fashion) to a value in the range from x = 0.10 to 1.0 with a preferred value of x = 0.25. Layer 2 serves to relax the strain caused by the lattice mismatch between layer 2 of graded Ge composition $Si_{1-x}Ge_x$ and Si substrate 1. Ge has a lattice spacing of 1.04 times the lattice spacing of Si. Thus for a relaxed top surface of buffer layer 2 where x equals 0.25, the lattice spacing of the unit cell along each axis in the top surface is about 1.01 times the lattice spacing of the unit cell of Si along each axis. For a description of how to grow relaxed low defect top surfaces of $Si_{1-x}Ge_x$ layers, reference is made to U.S. Pat. No. 5,659,187 which was issued on Aug. 19, 1997 to F. K. Legoues and B. S. Meyerson . After the graded region of layer 2, a 0.25 to about 10 μm thick, undoped or not-intentionally doped layer 3 of $Si_{1-y}Ge_y$ is grown, where the Ge composition, typically y = 0.25, is in the range from y = 0.10 to 1.0. Layer 3 acts as the absorbing medium for radiant

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energy as well as a relaxed, device quality pseudosubstrate for growth of subsequent layers. The background impurities in layer 3 should be low enough to allow penetration of the electric field from the surface electrodes into the entire layer.

[0021] In one embodiment, the subsequent layers are a Si quantum well layer 4, a $Si_{1-y}Ge_y$ undoped or not-intentionally doped offset layer 5, a doped $Si_{1-y}Ge_y$ supply layer 6 and optionally a Si layer 7. By an undoped layer, it is meant a not-intentionally doped layer which may have a background dopant concentration so low as to not substantially affect the function of the layer. The Ge composition of layers 5 and 6 are in the range of y = 0.1 to 1.0 and y is preferably the same as the composition of layer 3. A quantum well for electrons is formed in Si layer 4 due to the conduction band splitting arising from the tensile strain in Si layer 4. The isolation for MODFET 15 is achieved by forming an etched mesa region, thereby exposing the surface 8 of $Si_{1-y}Ge_y$ buffer layer 3 in the etched regions, as shown in Fig. 1B. Next, in Fig. 1C, n-type implanted regions 9 are formed to facilitate making low-resistance contacts to the Si quantum well layer 4. The source and drain metallization 10 can then be deposited as depicted in Fig. 1D, followed by the gate metallization 12 shown in Fig. 1E.

[0022] The MSM photodetector is created by depositing interdigitated Schottky electrodes 11 on the exposed surface 8 of buffer layer 3. To simplify the fabrication process, it is possible for MSM electrodes 11 to be defined in the same lithographic step as the Ohmic metallization 10, as depicted in Fig. 1D. MSM electrodes 11 are configured in such a way such that a bias applied between adjacent electrodes, as shown in Fig. 1E, creates an electric field that penetrates into the underlying absorbing layer 3. Light or radiant 14 energy incident from or passing. through surface 8 creates free carriers, electrons 15 and holes 16, in layer 3 that travel to electrodes 11, creating a current signal that is proportional to the power of the incident light.

[0023] Fig. 2 depicts the manner in which the devices shown in Fig. 1 are connected to form a simple photoreceiver circuit 17. A bias voltage, V_{diode}, is applied to the positive MSM electrode, while the negative electrode is connected to the gate of depletion-mode transistor 18, and to a bias resistor 19, R_{bias}, which is connected to a negative supply voltage, $-V_{ss}$. The transistor source is connected to ground, while the drain is connected to a load resistor 20, R_{load}, which is connected to the supply voltage, V_{dd}. In this configuration, the photocurrent induced by the incident light creates a voltage across the bias resistor 19 which is input to the gate of the transistor 18, thereby modulating the transistor current, and creating an amplified signal at the output lead 21, V_{out}. Resistors 19 and 20 may be formed and interconnected on the chip with the photodetector 22 and transistor 18 which is well known in the art. Other optoelectronic circuits may be formed which for example use more transistors to optimize the circuit to the application.

[0024] Fig. 3 shows another embodiment of the invention that is the same as that shown in Fig. 1E, except that the MSM photodetector is surrounded by a deep isolation trench 23 that extends from the surface 8 of the relaxed buffer layer 3 down into the substrate 1. Isolation trench 23 serves to confine the carriers that are generated in $Si_{1-y}Ge_y$ buffer layer 3 from diffusing laterally outside the region directly beneath the detector geometry. The trench also serves to isolate slow carriers generated outside the high-field region directly beneath the detector geometry from being collected by the surface electrodes 11, thereby leading to improved high-frequency performance. Furthermore, deep isolation trench 23 can be planarized by filling with a dielectric material 24. The trench can readily be incorporated into the fabrication scheme shown in Figs. 1A-1E, by etching deep isolation trench 23 before the mesa isolation in Fig. 1B, then filling the trench with dielectric material 24, followed by a planarization step. The subsequent fabrication steps can then be performed as depicted in Fig. IB-IE.

[0025] Fig. 4A shows a not claimed semiconductor structure that is the same as that shown in Fig. 1E, except that the relaxed buffer layer 38, over layer 2, is composed of a symmetrically strained superlattice instead of a constant-composition alloy $Si_{1-y}Ge_y$. The superlattice consists of alternating layers of $Si_{1-x}Ge_x$, 35, and $Si_{1-z}Ge_z$, 36, where $x < y < z$, and have Ge-compositions such that the average composition in buffer layer 38 is equal to y where y is in the range from 0.1 to 0.9, with a preferred value of 0.25. The tensile strain in $Si_{1-x}Ge_x$ layer 35, and the compressive strain in $Si_{1-z}Ge_z$ layer 36 enhances the absorption of radiation by reducing the effective band gap of buffer layer 38. To ensure that the photogenerated carriers are not trapped in the potential wells formed by strained layers 35 and 36, the Ge composition of buffer layer 38 can be graded in a continuous fashion, to produce a smooth, rather than abrupt, potential profile. This situation is shown schematically in Fig. 4B, where the conduction and valence band edges, shown by curves 41 and 42, of alternating strained layers 35 and 36 are plotted along with the conduction and valence band edges, shown by curves 43 and 44, of a constant composition layer. The average band gap of the symmetric superlattice E_{g2}, shown by arrow 45, is reduced compared to that of the constant composition layer, E_{g1}, shown by arrow 46, leading to greater photoabsorption in the symmetric superlattice. The operation of the MODFET 15 structure shown in Fig. 4A is not affected by the symmetric superlattice because no net strain is built up in layer 38. Therefore, after the growth of the superlattice 38, only a thin, constant-composition $Si_{1-y}Ge_y$ layer 37, needs to be deposited before growing the MODFET 15 layers 4-7. For layer 37, y is in the range from 0.1 to 0.9, and is preferably equal to the average Ge-composition of layer 38.

[0026] Another not claimed semiconductor structure is shown in Fig. 5, where a SiGe MSM photodetector is integrated with a p-channel MODFET 47. This configuration consists of a graded buffer layer 2 followed by a

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constant composition $Si_{1-y}Ge_y$ absorbing layer 3 , similar to that of Figs. IA-IE. These layers are followed by a layer structure for a p-channel MODFET 47, consisting of a $Si_{1-w}Ge_w$, doped layer 48, where w < y, an undoped $Si_{1-y}Ge_y$ layer 49, a compressive-strained $Si_{1-z}Ge_z$ quantum well layer 50, where z > y, an undoped $Si_{1-y}Ge_y$ layer 51, and optionally a thin Si layer 52. The Ge percentages for this embodiment can vary from y = 0.1 to 0.9, w = 0 to 0.5, and z = 0.5 to 1.0. This example could be particularly useful because the high Ge-content buffer layer 3 produces very efficient optical absorption, yet is also ideal for producing very high hole mobilities in p-channel MODFETs due to the compressive strain in the $Si_{1-z}Ge_z$ quantum well layer 50, particularly for the case of a pure-Ge channel where the mobility is not degraded by alloy scattering. MODFET 47 can be fabricated similar to the n-type device process shown in Figs. 1A-1E, where a mesa etch is used to isolate MODFET 47 and expose the surface 8 of photodetector absorbing layer 3. Next, p-type implanted regions 53 are formed to create low-resistance contacts to the $Si_{1-z}Ge_z$ quantum well layer 50. The source and drain metallization 54 can then be deposited, followed by the gate metallization 56. The example in Fig. 5 could also be fabricated with a reduced number of fabrication steps by defining the MSM electrodes 55 in the same lithographic step as the gate metallization 56 for MODFET 47.

[0027] As the Ge content of the buffer layers is increased, the band gap shrinks, leading to larger dark currents for the photodiode. A method of reducing the dark current without a dramatic increase in process complexity is to use different materials for alternate electrodes of the photodetector. Fig. 6A shows one embodiment of the invention, where the positively-biased electrodes 60 of the MSM photodiode have a high Schottky barrier height for holes, and the negatively-biased electrodes 61 have a high Schottky barrier height for electrons. To simplify the fabrication process, it is possible for the positively-biased (negatively-biased) electrodes 60 (61) to be defined in the same lithographic step as the Ohmic (gate) metallization, 10 (12). Possible candidates for the positively-biased MSM electrodes and Ohmic contact material are Er, W, Ti, Ni and Co, while the negatively-biased MSM electrodes and gate material might be Pt or Ir.

[0028] Fig. 6B shows another embodiment of the invention where negatively biased photodiode electrode 61 is composed of a material with high Schottky barrier for electrons, such as Pt or Ir, and the positively biased electrode is composed of n-type doped region 63, and electrode 64 which makes an Ohmic contact to region 63. As in Fig. 6A, the fabrication process can be simplified by fabricating n-type doped region 63 and positively-biased electrode 64 at the same time as MODFET 15 source-drain implant 9, and Ohmic metallization 10, and negatively-biased electrode 61 at the same time as MODFET gate metallization 12.

[0029] Fig. 6C shows another embodiment of the invention where the photodiode consists of a lateral p-i-n geometry, and where the positively-biased photodiode electrode is composed of n-type doped region 63, and electrode 64 which makes an Ohmic contact to region 63, and the negatively-biased photodiode electrode is composed of p-type doped region 65, and an electrode 66 which makes an Ohmic contact to region 65.

[0030] The photodetector performance can be optimized by varying the properties of the substrate. For instance, Fig. 7A shows a structure similar to Fig. 1E, where the substrate is an SOI wafer 70 and consists of a thick Si substrate 71, a SiO_2 layer 72, and a roughly 200 nm-thick Si layer 73. Without degrading MODFET 15 performance, SiO_2 layer 72 can improve the performance of the SiGe MSM photodetector by preventing slow carriers generated in Si substrate 71 below SiO_2 layer 72 from reaching the MSM surface electrodes 11, thereby increasing the detector speed. The amount of light reflected back into buffer layer 3 can be maximized by adjusting the thickness of SiO_2 layer 72 to equal odd integer multiples of 1/4n, where 1 is the wavelength of the incident light, and n is the refractive index of SiO_2.

[0031] Similarly, as shown in Fig. 7B, the substrate could consist of a heavily doped (> 10^{18} cm^{-3}) Si wafer 74 that causes photogenerated carriers in the layer to recombine before they can reach surface electrodes 11. The heavily-doped substrate 74 also acts to prevent the electric field produced by MSM interdigitated electrodes 11 from penetrating into substrate 74, thereby increasing the electric field strength in undoped SiGe absorbing layer 3, and subsequently increasing the detector speed.

[0032] As shown in Fig. 7C, the substrate capacitance can be reduced compared to the embodiment shown in Fig. 7B by selectively doping substrate 1 only in region 75 underneath MSM interdigitated electrodes 11. Selectively-doped region 75 can easily be formed before the growth of the Si/SiGe epi-layers using ion implantation, and then later aligned to MSM interdigitated electrodes 11.

[0033] Fig. 8C, curve 77, is a graph of the frequency response of the SiGe MSM photodetector comprising a $Si_{0.75}Ge_{0.25}$ absorbing layer at a thickness of 2.8 μm depicted in the cross-sectional and top-view diagrams of Figs. 8A and 8B. In Fig. 8C, the ordinate represents normalized photoresponse (dB) and the abscissa represents frequency (Hz). This device had a dc responsivity of 0.1 A/w, and displayed a -3 dB (-6 dB) bandwidth of 0.95 GHz (2.7 GHz), at λ = 850 nm, for a bias voltage of +5 V. To our knowledge, this is the highest bandwidth achieved to date for a crystalline SiGe MSM photodetector for an incident radiation of λ = 850nm.

[0034] Fig. 9 shows the frequency response of an n-channel MODFET fabricated very similar to MODFET 15 shown in Fig. 1E. In Fig. 9, curve 78 shows the current gain versus frequency of the n-channel MODFET and curve 79 shows the maximum available gain versus frequency. In Fig. 9, the left ordinate represents current gain (dB), and the right ordinate represents maximum avail-

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able gain (dB), and the abscissa represents frequency. The device shows a unity-gain cutoff frequency of 31 GHz, for a gate length of 0.7 μm, performance which is far superior to bulk Si MOSFETs of the same gate length. These results shown by curve 77 in Figs. 8C and by curves 78 and 79 in Fig. 9 on the individual components of the integrated circuit indicate the viability of the present invention, particularly given the straightforward method of integration described herein.

[0035] The selectively-doped substrate configuration shown in Fig. 7C can also be modified to integrate a vertical p-i-n photodetector 80 with an n- or p-channel MODFET 15. One such example is shown in Fig. 10, where p-i-n photodetector 80 and an n-channel MODFET 15 are fabricated using an n-type modulation-doped heterostructure, as described in Fig. 1E. In this embodiment, the p-i-n photodetector 80 is created when an n-type implanted region 80 and top contact 81 are aligned to a heavily-doped p-type region 82 created before the growth of the Si/SiGe epi-layers 2 and 3. The bottom contact 83 is made by etching down to and into substrate 1 as shown in Fig. 10. The example in Fig. 10 has the advantage that the n-channel, modulation-doped regions 4-7 do not need to be etched away to make top contact 81 of the p-i-n detector 80, because this contact already needs to be doped n-type. This example can also be used with a buffer layer 38 consisting of a symmetric superlattice as described in Fig. 4. MODFET 15 shown in this example is an n-channel device. For integration with a p-channel MODFET, the doping and polarity of the p-i-n contacts 80-83 can be reversed. The p-i-n configuration has the advantage that the carriers are always generated in a high-field region, and the distance the photogenerated carriers have to travel is reduced because detector electrodes 81 and 83 are on both the top and bottom of absorbing region 3.

[0036] Fig. 11 shows how an MSM photodiode 85 and MODFET 86 can be integrated using a fabrication scheme similar to that of a standard Si MOSFET or CMOS process. In the preferred embodiment, the layer structure is the same as that used in Fig. 1A. The MODFET 86 can be fabricated by depositing a thin gate oxide layer 90 followed by an undoped poly-silicon layer that is patterned and etched to define the gate electrode 91. Next an ion implant is performed to define n-type source and drain regions 92 where poly-silicon gate electrode 91 is used as a self-aligned implant mask. Next, a mesa isolation etch is performed which exposes the surface 8 of the buffer layer 3 in the etched regions. Next an insulating layer 93, such as silicon nitride, is deposited and then etched to form sidewall spacer regions 94. Finally, a self-aligned silicide (salicide) process is performed, where metal is deposited, heated to form metal-silicide or metal-germanosilicide contacts 95 to n-type source and drain regions 92 and the unreacted metal selectively etched away. The main feature of this embodiment is that the MSM photodetector 85 can be fabricated at the same time as MODFET 86 source and drain contacts 95 using the salicide process, by patterning windows in insulating layer 93 above SiGe buffer layer 3 to form metal-silicide or metal-germanosilicide photodetector electrodes 96 in openings of insulating layer 93.

[0037] Fig. 12 shows another not claimed example of a semiconductor structure where a SiGe MSM 97 and a strained-Si n-channel MOSFET 98 are integrated using a planar processing scheme. For this structure, the layer structure consists of the same graded $Si_{1-x}Ge_x$ layer 2 and constant composition, $Si_{1-y}Ge_y$ buffer layer 3 grown on Si substrate 1 as shown in Fig. 1E. On top of buffer layer 3 is grown a tensile-strained Si layer 100, as shown in Fig. 12. In the example, the MOSFET 98 is fabricated by depositing or growing a thin gate oxide layer 101, followed by an undoped poly-silicon layer, which is patterned and etched to define the gate electrode 102. Next an optional p-well implant 103, is performed for threshold voltage control, and an ion implant is performed to define n-type source and drain regions 104, where poly-silicon gate electrode 102 is used as a self-aligned implant mask. Next, trench isolation regions 105, are formed and filled with dielectric material 106, and a second insulating layer 107, such as silicon nitride, is deposited and etched to form sidewall spacer regions 108. Finally, a self-aligned silicide (salicide) process is performed, where metal is deposited, heated to form metal-silicide, or metal-germanosilicide contacts 109 on n-type source and drain regions 104, and the unreacted metal selectively etched away. The MSM photodetector 97 is fabricated using the same salicide process used to create the MOSFET 98 source and drain regions, by patterning windows in insulating layer 107 above SiGe buffer layer 3 to form metal-silicide or metal-germanosilicide photodetector electrodes 110 in the openings of insulating layer 107. This example has the advantage of utilizing a planar processing scheme, because Si layer 100 is not etched away. Because Si layer 100 is only ~ 10 nm thick, it has little effect on the photoabsorption, and can act as a stable surface material for formation of MSM electrodes 110.

[0038] Fig. 13 shows another not claimed example of a semiconductor structure where MSM photodetector 85 is integrated with both a p-channel and an n-channel Si/SiGe MOSFET, 139 and 140, using an epitaxial multilayer structure. The layer structure consists of a Si substrate 1, a graded $Si_{1-x}Ge_x$ layer 2 and constant composition $Si_{1-y}Ge_y$ buffer layer 3 as described in Fig. 1A. In the example, on top of $Si_{1-y}Ge_y$ buffer layer 3 are grown an n-type doped $Si_{1-y}Ge_y$ supply layer 120, an undoped $Si_{1-y}Ge_y$ offset layer 121, a tensile-strained Si quantum well layer 122, which acts as the electron channel for the NMOS device, another undoped $Si_{1-y}Ge_y$ offset layer 123, a compressive-strained $Si_{1-z}Ge_z$ layer 124, where $z > y$, which acts as the hole channel for the PMOS device, an undoped $Si_{1-y}Ge_y$ offset layer 125, and an undoped Si layer 126. In this example, the Ge-percentages of layers 120, 121, 123 and 125 is in the range $y = 0.1$ to 0.9, with a preferred value of $y = 0.25$. The Ge-percentage of layer 124 is in the range $z = 0.3$ to 1.0, and preferably

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has a value where z-y is greater than 0.2. Next a thin gate oxide layer 127, is grown or deposited, followed by a p-type doped poly-silicon layer. The CMOS circuit can be fabricated by etching the poly-silicon to form the gates of the n- and p-type CMOS devices 128, which then act as implant masks for formation of p-type doped region 129, and n-type doped region 130. Doped regions 129 and 130 form contacts to the buried quantum well channel layers 124 and 122, respectively. Next, trench isolation regions 131, are formed and filled with dielectric material 132, for planarization. At this point, an etch is performed to expose the surface 8 of $Si_{1-y}Ge_y$ buffer layer 3, and a blanket insulating layer 134, such as silicon nitride, is deposited. windows for forming the photodiode electrodes are patterned and etched at the same time as nitride sidewall regions 135 are formed. Finally, a salicide step is performed, as described in Fig. 11, to create the MSM electrodes 136, as well as the source and drain contacts 137 and 138 of the PMOS and NMOS devices, respectively. The example shown in Fig. 13 is a versatile configuration where not only PMOS device 139 or NMOS device 140 can be combined with MSM photodetector 85 to act as part of a photoreceiver amplifier circuit, but PMOS device 139 and NMOS device 140 can be combined and used to form a CMOS logic circuit. Therefore, the embodiment in Fig. 13 can potentially be used to fabricate a high-speed photoreceiver circuit on the same chip as a high-speed, low-power CMOS technology, for future "system-on-a-chip" applications.

[0039] An integrated optoelectronic circuit and process for making is described incorporating a photodetector and a MODFET on a chip. The chip contains a single-crystal semiconductor substrate, a buffer layer of SiGe graded in composition, a relaxed SiGe layer, a quantum well layer, an undoped SiGe spacer layer and a doped SiGe supply layer. The photodetector may be a metal-semiconductor-metal (MSM) or a p-i-n device. The detector may be integrated with an n- or p-type MODFET, or both in a CMOS configuration, and the MODFET can incorporate a Schottky or insulating gate. The invention overcomes the problem of producing Si-manufacturing-compatible monolithic high-speed optoelectronic circuits for 850 nm operation by using epixially-grown Si/SiGe heterostructure layers.

Claims

1. A semiconductor structure comprising a single crystal semiconductor substrate (1), a $Si_{1-x}Ge_x$ buffer layer (2) graded from x = 0 to y where y is in the range from 0.1 to 1.0 , a layer of relaxed Si_{1-y} Ge_y (3) having a thickness in the range from 0.25 μm to 10 μm, a quantum well layer (4), an undoped Si_{1-y} Ge_y spacer layer (5), and a doped Si_yGe_y supply layer (6), spaced apart drain and source regions (9) extending to the quantum well layer (4) so that said quantum well layer (4) is the conducting channel of a field-effect transistor; wherein said undoped $Si_{1-y}Ge_y$ spacer layer (5) separates dopants in said doped $Si_{1-y}Ge_y$ supply layer (6) from said conducting channel; and wherein portions of said quantum well layer (4), said undoped $Si_{1-y}Ge_y$ spacer layer (5) and said doped $Si_{1-y}Ge_y$ supply layer (6) are removed to provide an expose portion of said relaxed $Si_{1-y}Ge_y$ (3) layer to form a photodetector and wherein said exposed layer of relaxed $Si_{1-y}Ge_y$ (3) layer is the absorbing region of said photodetector.

2. The semiconductor structure of claim 1 further including a Schottky gate contact to control charge in said conducting channel to form a MODFET.

3. The semiconductor structure of claim 1 wherein electrodes (60, 61, 64, 65) are formed on said exposed portion of said relaxed Si_{1-y} Ge_y layer to form a photodetector.

4. The semiconductor structure of claim 1 wherein said quantum well layer is under tensile strain and consists of Si.

5. The semiconductor structure of claim 3 wherein said electrodes include two or more interdigitated Schottky electrodes.

6. The semiconductor structure of claim 3 further including a trench extending through said exposed relaxed Si_{1-y} Ge_y layer surface and surrounding said photodetector; optionally said trench is filled with a dielectric material.

7. The semiconductor structure of claim 3 wherein positively-biased electrodes of said photodetector comprise Er, W, Ti, Ni or Co, and provide Schottky contacts (60) with barrier height for holes that is greater than half the band gap of said exposed relaxed Si_{1-y} Ge_y layer, and negatively-biased electrodes (61) of said photodetector comprise Pt or Ir and provide Schottky contacts with barrier height for electrons that is greater than half the band gap of said exposed relaxed Si_{1-y} Ge_y layer.

8. The semiconductor structure of claim 5 wherein negatively-biased electrodes (61) of said photodetector comprise Pt or Ir and provide Schottky contacts with barrier height for electrons that is greater than half the band gap of said exposed relaxed Si_{1-y} Ge_y layer, and positively-biased electrodes (64) of said photodetector comprise Er, W, Ti, Ni or Co, and form Ohmic contact to an n-type doped region (63).

9. The semiconductor structure of claim 5 wherein negatively-biased electrodes (66) of said photodetector form Ohmic contacts to a p-type doped region (65) and said positively-biased electrodes (64) of said

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photodetector form an Ohmic contact to an n-type doped region (63).

10. The semiconductor structure of claim 1 wherein said substrate is heavily-doped greater than 10^{18} atoms/cm^3, or wherein said substrate is an SOI substrate comprising a thick Si layer, a SiO_2 layer, and a Si overlayer.

11. The semiconductor structure of claim 3 wherein said substrate is lightly-doped Si, and the region of said substrate underneath said photodetector is heavily-doped greater than 10^{18} atoms/cm^3.

12. The semiconductor structure of claim 3 wherein said photodetector absorbing region is bordered by deep trenches extending from said photodetector surface down to said Si substrate, and filled with a dielectric material, so as to prevent photogenerated carriers generated in said Si_{1-y} Ge_y, buffer layer from diffusing laterally past said deep trenches.

13. The semiconductor structure of claim 1 further including spaced apart drain and source regions extending to said quantum well layer, a gate dielectric layer above said supply layer between said drain and source and a gate electrode above said dielectric layer to form a MOSFET.

14. The semiconductor structure of claim 1 further including first and second spaced apart doped regions, one above the other, with a portion of said relaxed Si_{1-y} Ge_y layer there between to form a photodetector and an Ohmic contact to said respective first and second doped regions for applying a potential there between, and optionally one of the following;

a) further including a trench extending into said exposed relaxed Si_{1-y} Ge_y layer to provide a barrier to electrical charge;
b) wherein said first doped region includes a region of said quantum well layer, said undoped Si_{1-y} Ge_y spacer layer and said doped Si_{1-y} Ge_y supply layer; or
c) wherein said second doped region includes a region of said substrate.

15. A method for forming a semiconductor structure comprising the steps of:

selecting a single crystal semiconductor substrate (1),
forming a Si_{1-x} Ge_x buffer layer (2) graded from x = 0 to y in the range from 0.1 to 1.0,
forming a layer of relaxed Si_{1-y} Ge_y (3) having a thickness in the range from 0.25 μm to 10 μm,
forming a quantum well layer (4),
forming an undoped Si_{1-y} Ge_y spacer layer (5),
forming a doped Si_{1-y} Ge_y supply (6),
formning spaced apart drain and source regions extending to said quantum well layer(4) so that said quantum well layer (4) is the conducting channel of a field-effect transistor,
removing portions of said quantum well layer (4), said undoped Si_{1-y} Ge_y spacer layer (5) and said doped Si_{1-y} Ge_y supply layer (6) to expose said relaxed Si_{1-y} Ge_y layer and forming electrodes (11) on said exposed relaxed Si_{1-y} Ge_y layer to form a photodetector, wherein said exposed layer of relaxed Si_{1-y} Ge_y (3) is the absorbing region of said photodetector.

Patentansprüche

1. Halbleiterstruktur, welche ein monokristallines Halbleitersubstrat (1), eine $Si_{1-x}Ge_x$-Pufferschicht (2), die einen Gradienten von x = 0 bis y aufweist, wobei y im Bereich von 0,1 bis 1,0 liegt, eine Schicht aus relaxiertem $Si_{1-y}Ge_y$ (3) einer Dicke im Bereich von 0,25 μm bis 10 μm, eine Quantentopfschicht (4), eine undotierte $Si_{1-y}Ge_y$-Abstandsschicht (5) und eine dotierte $Si_{1-y}Ge_y$-Versorgungsschicht (6) umfasst, wobei sich Drain- und Source-Zonen (9), die einen Abstand voneinander aufweisen, bis zu der Quantentopfschicht (4) erstrecken, derart, dass es sich bei der Quantentopfschicht (4) um den leitenden Kanal eines Feldeffekttransistors handelt; wobei die undotierte $Si_{1-y}Ge_y$-Abstandsschicht (5) die Dotierstoffe in der dotierten $Si_{1-y}Ge_y$-Versorgungsschicht (6) von dem leitenden Kanal trennt; und wobei Abschnitte der Quantentopfschicht (4), der undotierten $Si_{1-y}Ge_y$-Abstandsschicht (5) und der dotierten $Si_{1-y}Ge_y$-Versorgungsschicht (6) entfernt sind, um einen frei liegenden Abschnitt der relaxierten $Si_{1-y}Ge_y$-Schicht (3) bereitzustellen, um einen Photodetektor zu bilden, und wobei es sich bei der frei liegenden Schicht der relaxierten $Si_{1-y}Ge_y$-Schicht (3) um die absorbierende Zone des Photodetektors handelt.

2. Halbleiterstruktur nach Anspruch 1, welche ferner einen Schottky-Gate-Kontakt umfasst, um die Ladung in dem leitenden Kanal zu regeln, um einen MODFET zu bilden.

3. Halbleiterstruktur nach Anspruch 1, wobei auf dem frei liegenden Abschnitt der relaxierten $Si_{1-y}Ge_y$-Schicht Elektroden (60, 61, 64, 65) ausgebildet sind, um einen Photodetektor zu bilden.

4. Halbleiterstruktur nach Anspruch 1, wobei die Quantentopfschicht unter Zugspannung steht und aus Si besteht.

5. Halbleiterstruktur nach Anspruch 3, wobei die Elek-

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troden zwei oder mehr ineinander greifende Schottky-Elektroden umfassen.

6. Halbleiterstruktur nach Anspruch 3, welche ferner einen Graben umfasst, der sich durch die Fläche der frei liegenden relaxierten $Si_{1-y}Ge_y$-Schicht hindurch erstreckt und den Photodetektor umgibt; gegebenenfalls ist der Graben mit einem dielektrischen Material gefüllt.

7. Halbleiterstruktur nach Anspruch 3, wobei Elektroden mit positiver Vorspannung des Photodetektors Er, W, Ti, Ni oder Co umfassen und Schottky-Kontakte (60) einer Barrierenhöhe für Defektelektronen bereitstellen, die größer ist als die Hälfte des Bandabstands der frei liegenden relaxierten $Si_{1-y}Ge_y$-Schicht, und Elektroden (61) mit negativer Vorspannung des Photodetektors Pt oder Ir umfassen und Schottky-Kontakte einer Barrierenhöhe für Elektronen bereitstellen, die größer ist als die Hälfte des Bandabstands der frei liegenden relaxierten $Si_{1-y}Ge_y$-Schicht.

8. Halbleiterstruktur nach Anspruch 5, wobei Elektroden (61) mit negativer Vorspannung des Photodetektors Pt oder Ir umfassen und Schottky-Kontakte einer Barrierenhöhe für Elektronen bereitstellen, die größer ist als die Hälfte des Bandabstands der frei liegenden relaxierten $Si_{1-y}Ge_y$-Schicht, und Elektroden (64) mit positiver Vorspannung einen Ohmschen Kontakt zu einer n-leitend dotierten Zone (63) bilden.

9. Halbleiterstruktur nach Anspruch 5, wobei Elektroden (66) mit negativer Vorspannung des Photodetektors Ohmsche Kontakte zu einer p-leitend dotierten Zone (65) bilden und die Elektroden (64) mit positiver Vorspannung des Photodetektors einen Ohmschen Kontakt zu einer n-leitend dotierten Zone (63) bilden.

10. Halbleiterstruktur nach Anspruch 1, wobei das Substrat mit mehr als 10^{18} Atomen/cm^3 stark dotiert ist oder wobei es sich bei dem Substrat um ein SOI-Substrat handelt, welches eine dicke Si-Schicht, eine SiO_2-Schicht und eine Si-Deckschicht umfasst.

11. Halbleiterstruktur nach Anspruch 3, wobei es sich bei dem Substrat um leicht dotiertes Si handelt und die Zone des Substrats unterhalb des Photodetektors mit mehr als 10^{18} Atomen/cm^3 stark dotiert ist.

12. Halbleiterstruktur nach Anspruch 3, wobei die absorbierende Photodetektorzone von tiefen Gräben begrenzt ist, welche sich von der Photodetektorfläche aus nach unten bis zu dem Si-Substrat erstrecken und mit einem dielektrischen Material gefüllt sind, um zu verhindern, dass Ladungsträger, die in der $Si_{1-y}Ge_y$-, Pufferschicht durch Photonen erzeugt werden, seitlich über die tiefen Gräben hinaus diffundieren.

13. Halbleiterstruktur nach Anspruch 1, welche ferner Drain- und Source-Zonen, die einen Abstand voneinander aufweisen und sich bis zu der Quantentopfschicht erstrecken, eine Gate-Dielektrikums-Schicht oberhalb der Versorgungsschicht zwischen der Drain- und der Source-Zone und eine Gate-Elektrode oberhalb der dielektrischen Schicht umfasst, um einen MOSFET zu bilden.

14. Halbleiterstruktur nach Anspruch 1, welche ferner, eine über der anderen, eine erste und zweite dotierte Zone umfasst, die einen Abstand voneinander aufweisen, wobei sich zwischen diesen ein Abschnitt der relaxierten $Si_{1-y}Ge_y$-Schicht befindet, um einen Photodetektor und einen Ohmschen Kontakt zu der ersten bzw. zweiten dotierten Zone zu bilden, um zwischen diesen eine Potentialdifferenz anzulegen, und wobei wahlweise eine der folgenden Bedingungen erfüllt ist:

a) sie umfasst ferner einen Graben, welcher sich in die frei liegende relaxierte $Si_{1-y}Ge_y$-Schicht erstreckt, um eine Barriere für eine elektrische Ladung zu schaffen;
b) wobei die erste dotierte Zone eine Zone der Quantentopfschicht, der undotierten $Si_{1-y}Ge_y$-Abstandsschicht und der dotierten $Si_{1-y}Ge_y$-Versorgungsschicht umfasst; oder
c) wobei die zweite dotierte Zone eine Zone des Substrates umfasst.

15. Verfahren zur Bildung einer Halbleiterstruktur, welches die folgenden Schritte umfasst:

Auswählen eines monokristallinen Halbleitersubstrats (1),
Bilden einer $Si_{1-x}Ge_x$-Pufferschicht (2), welche einen Gradienten von x = 0 bis y im Bereich von 0,1 bis 1,0 aufweist,
Bilden einer Schicht aus relaxiertem $Si_{1-y}Ge_y$ (3), welche eine Dicke im Bereich von 0,25 µm bis 10 µm aufweist,
Bilden einer Quantentopfschicht (4),
Bilden einer undotierten $Si_{1-y}Ge_y$-Abstandsschicht (5),
Bilden einer dotierten $Si_{1-y}Ge_y$-Versorgungsschicht (6),
Bilden von Drain- und Source-Zonen, die einen Abstand voneinander aufweisen und sich bis zu der Quantentopfschicht (4) erstrecken, derart, dass es sich bei der Quantentopfschicht (4) um den leitenden Kanal eines Feldeffekttransistors handelt,
Entfernen von Abschnitten der Quantentopf-

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schicht (4), der undotierten $Si_{1-y}Ge_y$-Abstandsschicht (5) und der dotierten $Si_{1-y}Ge_y$-Versorgungsschicht (6), um die relaxierte $Si_{1-y}Ge_y$-Schicht frei zu legen, und Bilden von Elektroden (11) auf der frei liegenden relaxierten $Si_{1-y}Ge_y$-Schicht, um einen Photodetektor zu bilden, wobei es sich bei der frei liegenden Schicht aus relaxiertem $Si_{1-y}Ge_y$ (3) um die absorbierende Zone des Photodetektors handelt.

Revendications

1. Structure à semi-conducteur, comprenant un substrat (1) en semi-conducteur monocristallin, une couche tampon (2) en $Si_{1-x}Ge_x$, dans laquelle x = 0 à y, avec y dans la fourchette de 0,1 à 1,0, une couche (3) en $Si_{1-y}Ge_y$ relaxé, ayant une épaisseur dans la fourchette de 0,25 μm à 10 μm, une couche de puits quantique (4), une couche d'espacement (5) en $Si_{1-y}Ge_y$ non dopé, et une couche d'alimentation (6) en $Si_{1-y}Ge_y$ dopé, des régions de drain et de source (9) espacées, s'étendant vers la couche de puits quantique (4), de manière que ladite couche de puits quantique (4) soit le canal conducteur d'un transistor à effet de champ ; dans lequel ladite couche d'espacement (5) en $Si_{1-y}Ge_y$ non dopé sépare des dopants, situés dans ladite couche d'alimentation (6) en $Si_{1-y}Ge_y$ dopé, vis-à-vis dudit canal conducteur ; et dans lequel des parties de ladite couche de puits quantique (4), ladite couche d'espacement (5) en $Si_{1-y}Ge_y$ non dopé et ladite couche d'alimentation (6) en $Si_{1-y}Ge_y$ dopé sont éliminées pour fournir une partie exposée de ladite couche (3) en $Si_{1-y}Ge_y$ relaxé, de manière à former un photodétecteur et dans lequel ladite couche exposée de couche (3) en $Si_{1-y}Ge_y$ relaxé est la région absorbante dudit photodétecteur.

2. Structure à semi-conducteur selon la revendication 1, comprenant en outre un contact de grille de Schottky, pour commander la charge dans ledit canal conducteur, de manière à former un MODFET.

3. Structure à semi-conducteur selon la revendication 1, dans laquelle des électrodes (60, 61, 64, 65) sont formées sur ladite partie exposée de ladite couche en $Si_{1-y}Ge_y$ relaxé, de manière à former un photodétecteur.

4. Structure à semi-conducteur selon la revendication 1, dans laquelle ladite couche de puits quantique est placée sous une contrainte de traction et est composée de Si.

5. Structure à semi-conducteur selon la revendication 3, dans laquelle lesdites électrodes comprennent deux électrodes de Schottky interdigitées, ou plus.

6. Structure à semi-conducteur selon la revendication 3, comprenant en outre une tranchée, s'étendant à travers ladite surface de couche en $Si_{1-y}Ge_y$ relaxé exposée et entourant ledit photodétecteur ; ladite tranchée étant, en option, remplie d'un matériau diélectrique.

7. Structure à semi-conducteur selon la revendication 3, dans laquelle des électrodes, polarisées de manière positive, dudit photodétecteur sont composées de Er, W, Ti, Ni ou Co, et fournissent des contacts de Schottky (60) avec une hauteur de barrière pour des trous supérieure à la moitié de la largeur de bande interdite de ladite couche en $Si_{1-y}Ge_y$ relaxé exposée, et des électrodes (61), polarisées de manière négative, dudit photodétecteur sont composées de Pt ou Ir et fournissent des contacts de Schottky avec une hauteur de barrière pour des électrons supérieure à la moitié de la largeur de bande interdite de ladite couche en $Si_{1-y}Ge_y$ relaxé exposée.

8. Structure à semi-conducteur selon la revendication 5, dans laquelle des électrodes (61), polarisées de manière négative, dudit photodétecteur sont composées de Pt ou Ir et fournissent des contacts de Schottky avec une hauteur de barrière pour des électrons supérieure à la moitié de la largeur de bande interdite de ladite couche en $Si_{1-y}Ge_y$ relaxé exposée, et des électrodes (64), polarisées de manière positive, dudit photodétecteur sont composées de Er, W, Ti, Ni ou Co, et forment un contact ohmique avec une région (63) à dopage de type n.

9. Structure à semi-conducteur selon la revendication 5, dans laquelle des électrodes (66), polarisées de manière négative, dudit photodétecteur forment des contacts ohmiques avec une région (65) à dopage de type p, et lesdites électrodes (64), polarisées de manière positive, dudit photodétecteur forment un contact ohmique avec une région (63) à dopage de type n.

10. Structure à semi-conducteur selon la revendication 1, dans laquelle ledit substrat est fortement dopé, à plus de 10^{18} atomes/cm^3, ou dans lequel ledit substrat est un substrat SOI, comprenant une épaisse couche en Si, une couche en SiO_2, et une surcouche en Si.

11. Structure à semi-conducteur selon la revendication 3, dans laquelle ledit substrat est en Si légèrement dopé, et la région dudit substrat située au-dessous dudit photodétecteur est fortement dopée, à plus de 10^{18} atomes/cm^3.

12. Structure à semi-conducteur selon la revendication 3, dans laquelle ladite région absorbante de photodétecteur est délimitée par des tranchées profondes,

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s'étendant à partir de ladite surface de photodétecteur en descendant vers ledit substrat, et remplies d'un matériau diélectrique, de manière à empêcher que des porteurs photogénérés, générés dans ladite couche tampon en $Si_{1-y}Ge_y$, diffusent latéralement, au delà desdites tranchées profondes.

13. Structure à semi-conducteur selon la revendication 1, comprenant en outre des régions de drain et de source espacées, s'étendant vers ladite couche de puits quantique, une couche diélectrique de grille, située au-dessus de ladite couche d'alimentation, entre drain et source, et une électrode de grille, située au-dessus de ladite couche diélectrique, pour former un MOSFET.

14. Structure à semi-conducteur selon la revendication 1, comprenant en outre des première et deuxième région dopées, espacées, l'une au-dessus de l'autre, avec, entre elles, une partie de ladite couche en $Si_{1-y}Ge_y$ relaxé, pour former un photodétecteur et un contact ohmique avec lesdites première et deuxième régions dopées respectives, pour appliquer entre elles un potentiel et, en option, l'un des suivants :

a) comprenant en outre une tranchée, s'étendant dans ladite couche en $Si_{1-y}Ge_y$ relaxé exposée, pour fournir une barrière à une charge électrique ;
b) dans laquelle ladite première région dopée comprend une région de ladite couche de puits quantique, ladite couche d'espacement en $Si_{1-y}Ge_y$ non dopé et ladite couche d'alimentation en $Si_{1-y}Ge_y$ dopé ; ou
c) dans laquelle ladite deuxième région dopée comprend une région dudit substrat.

15. Procédé pour former une structure à semi-conducteur, comprenant les étapes consistant à :

sélectionner un substrat (1) en semi-conducteur monocristallin,
former une couche tampon (2) en $Si_{1-x}Ge_x$, dans laquelle x = 0 à y, avec y dans la fourchette de 0,1 à 1,0,
former une couche (3) en $Si_{1-y}Ge_y$ relaxé, ayant une épaisseur dans la fourchette de 0,25 µm à 10 µm,
former une couche de puits quantique (4),
former une couche d'espacement (5) en $Si_{1-y}Ge_y$ non dopé,
former une couche d'alimentation (6) en $Si_{1-y}Ge_y$ dopé,
former des régions de drain et de source espacées, s'étendant vers ladite couche de puits quantique (4), de manière que ladite couche de puits quantique (4) soit le canal conducteur d'un transistor à effet de champ,
éliminer des parties de ladite couche de puits quantique (4), de ladite couche d'espacement (5) en $Si_{1-y}Ge_y$ non dopé et de ladite couche d'alimentation (6) en $Si_{1-y}Ge_y$ dopé, pour exposer ladite couche en $Si_{1-y}Ge_y$ relaxé, et former des électrodes (11) sur ladite couche en $Si_{1-y}Ge_y$ relaxé exposée, de manière à former un photodétecteur, dans lequel ladite couche (3) en $Si_{1-y}Ge_y$ relaxé exposée est la région absorbante dudit photodétecteur.

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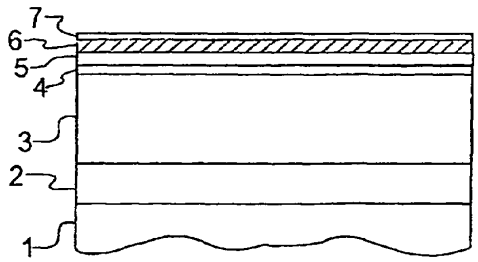


Fig. 1A

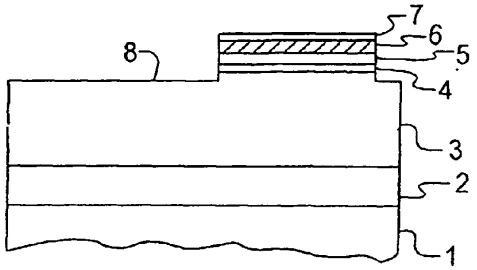


Fig. 1B

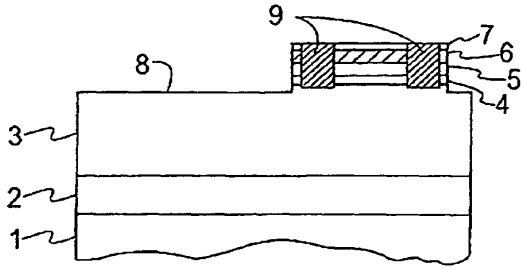


Fig. 1C

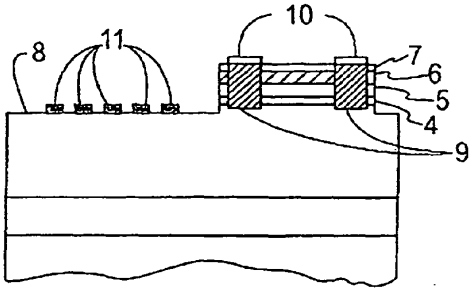


Fig. 1D

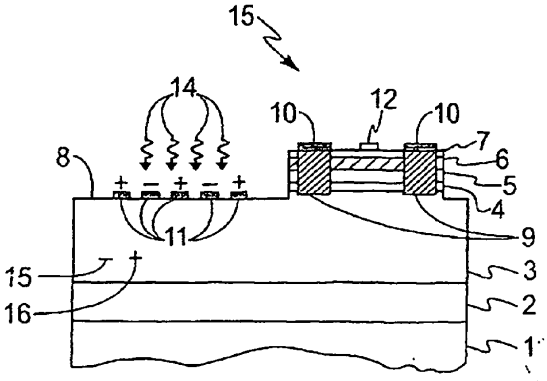


Fig. 1E

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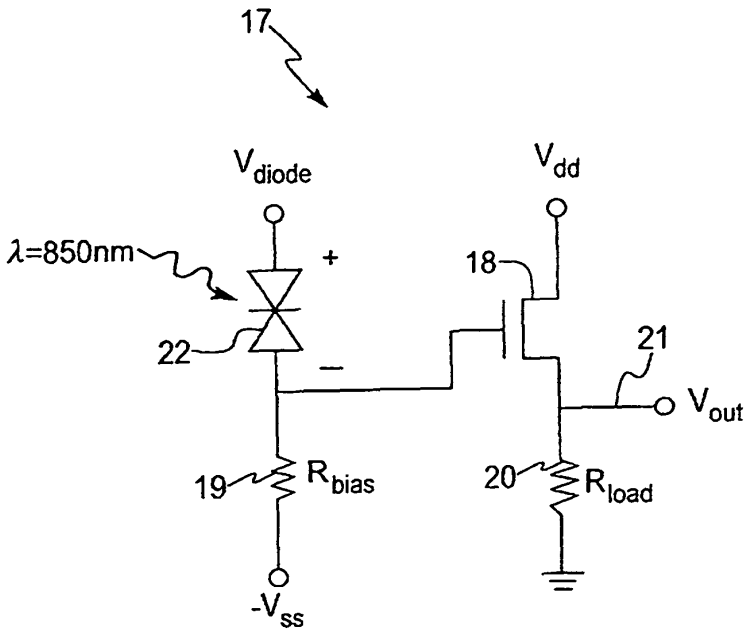


Fig. 2

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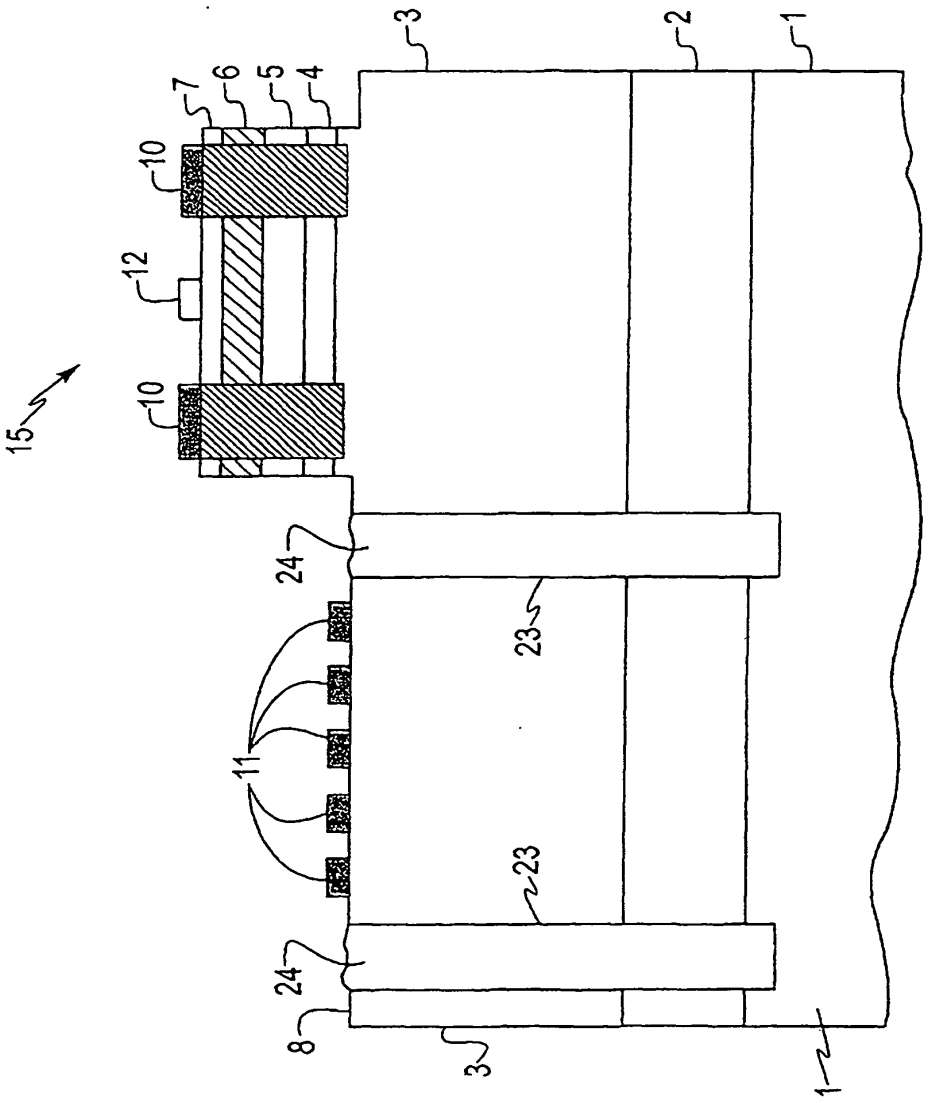


Fig. 3

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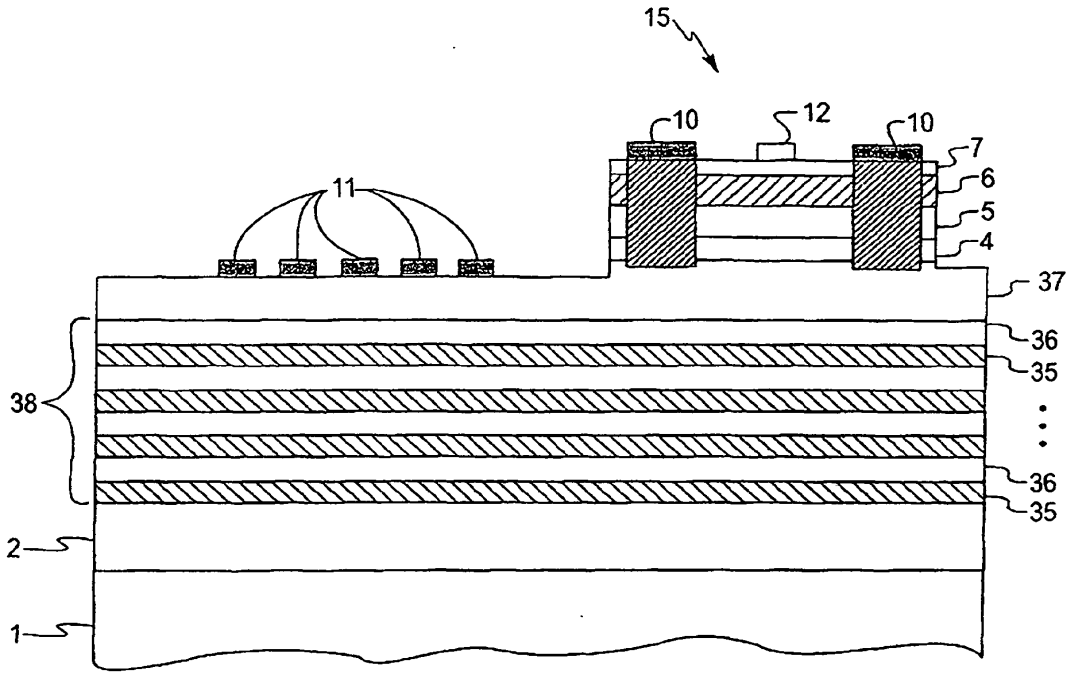


Fig. 4A

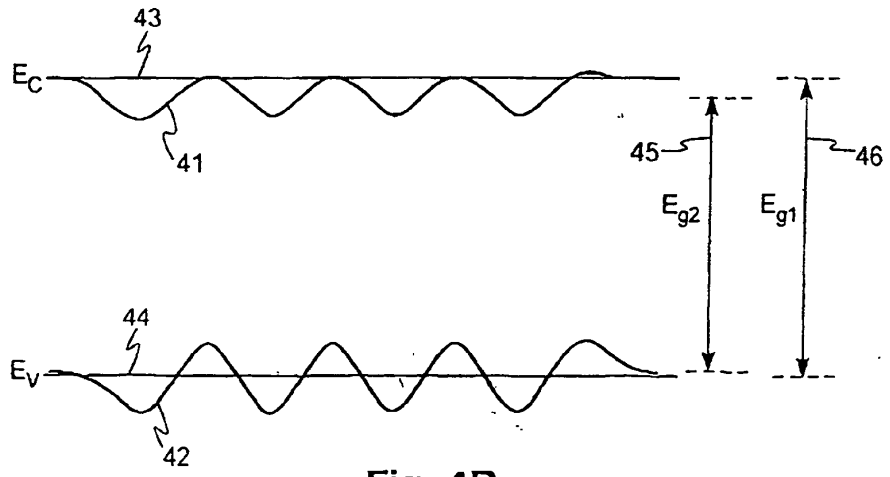


Fig. 4B

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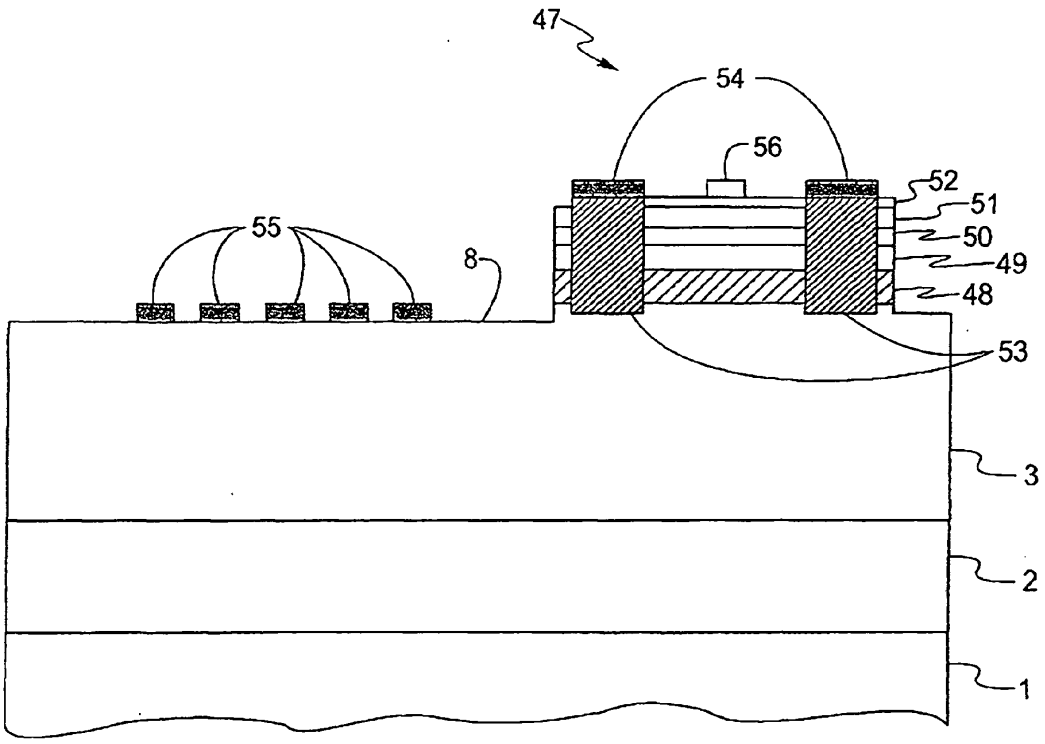


Fig. 5

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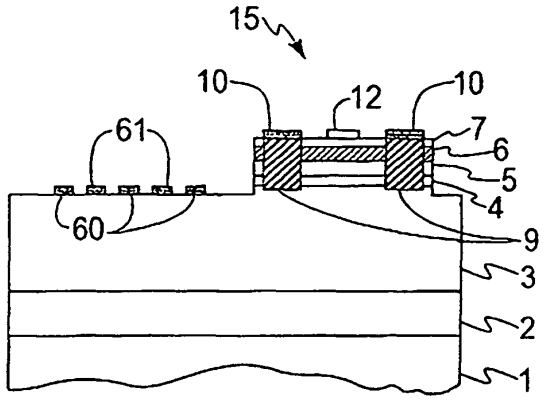


Fig. 6A

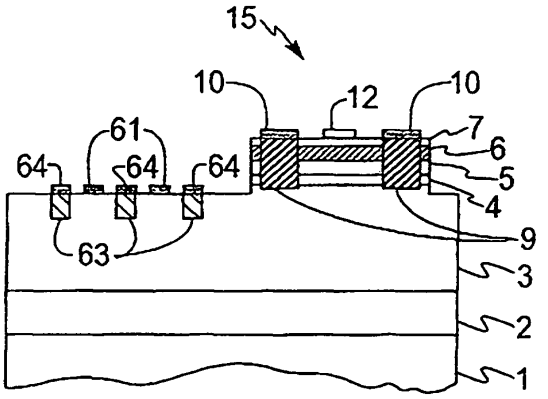


Fig. 6B

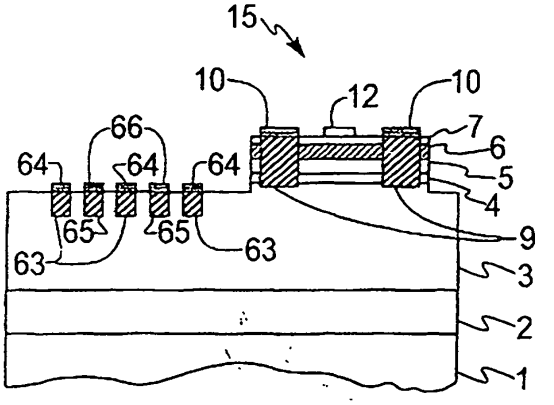


Fig. 6C

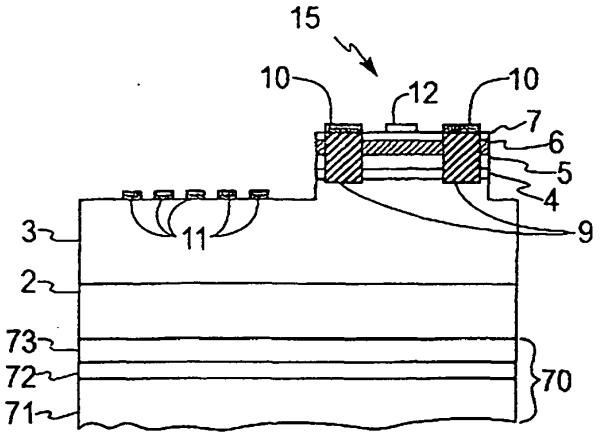


Fig. 7A

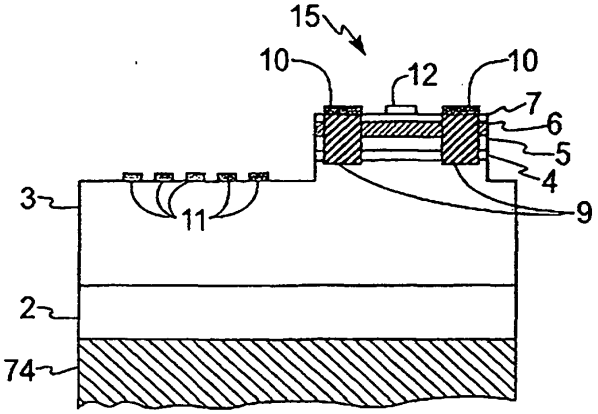


Fig. 7B

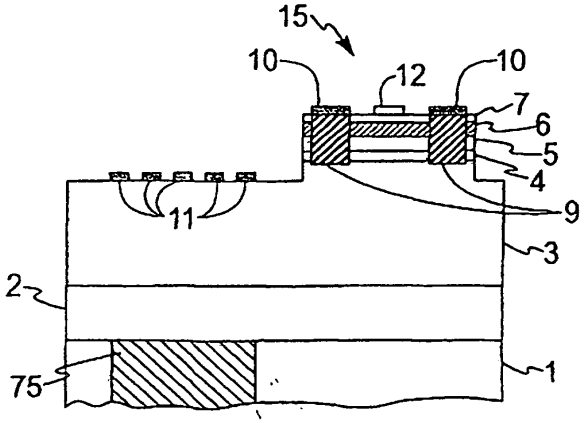


Fig. 7C

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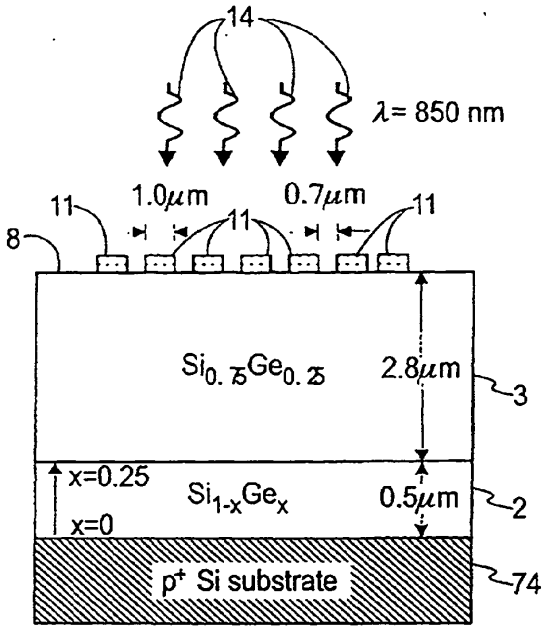


Fig. 8A

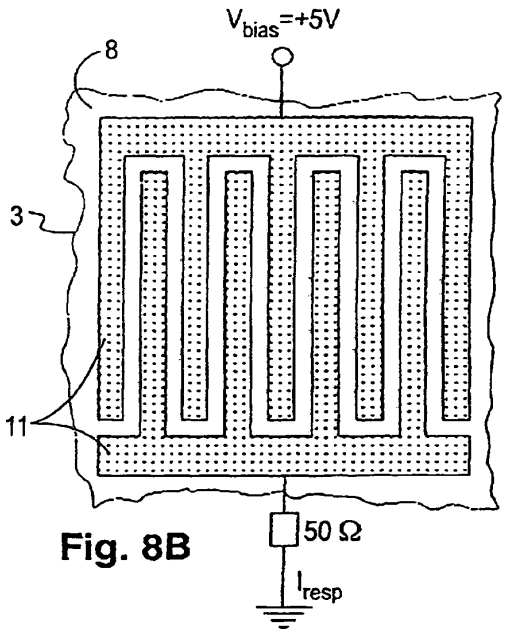


Fig. 8B

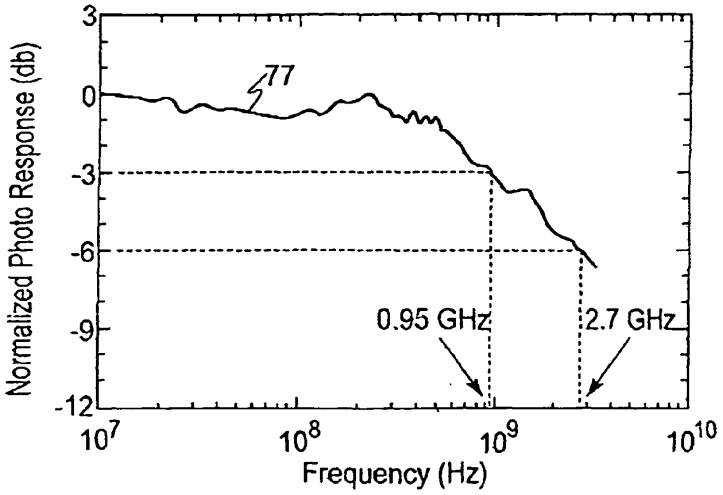


Fig. 8C

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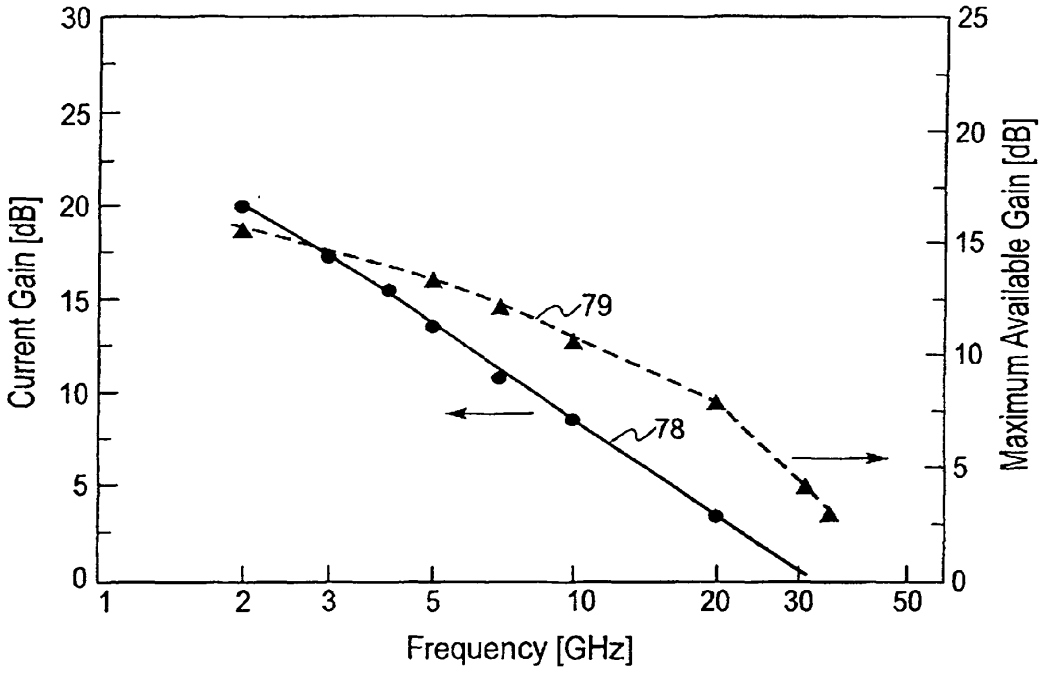

30
25
20
15
10
5
0
Current Gain [dB]
25
20
15
10
5
0
Maximum Available Gain [dB]
1
2
3
5
10
20
30
50
Frequency [GHz]
79
78

Fig. 9

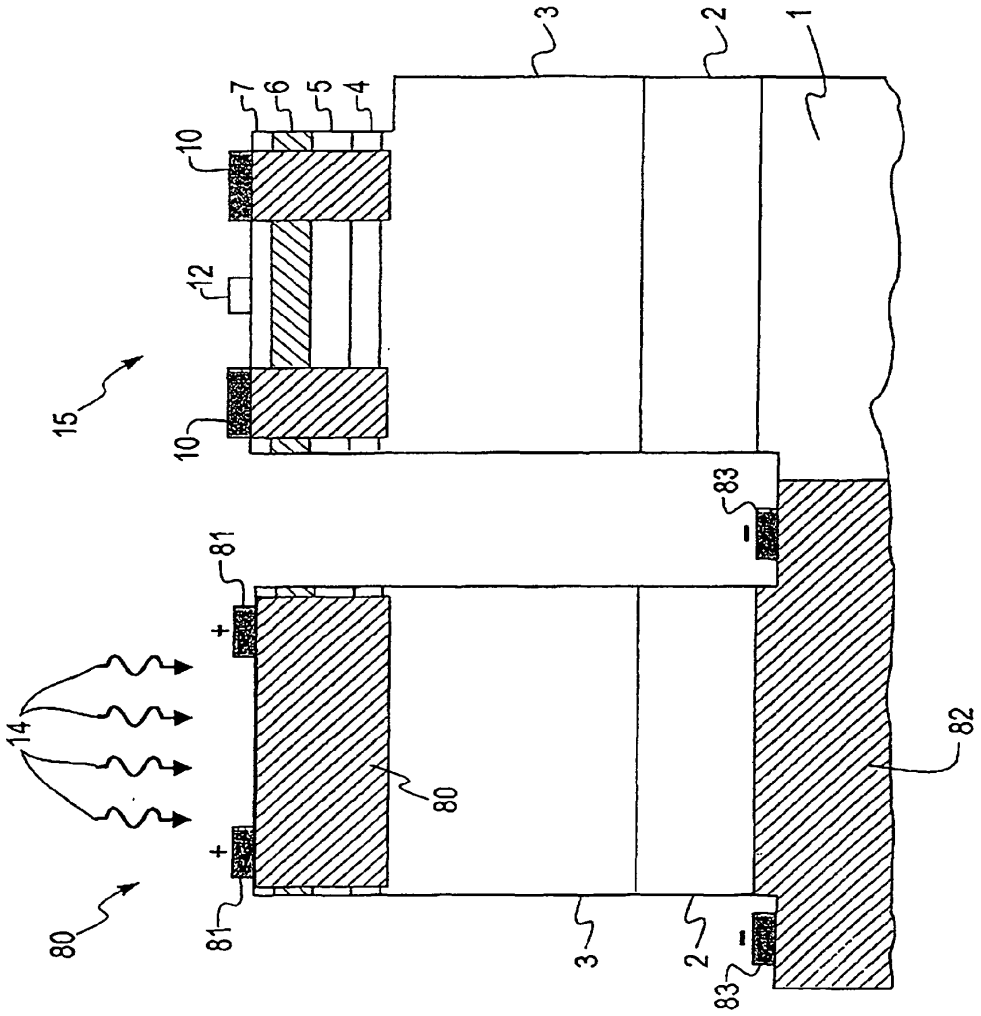


Fig. 10

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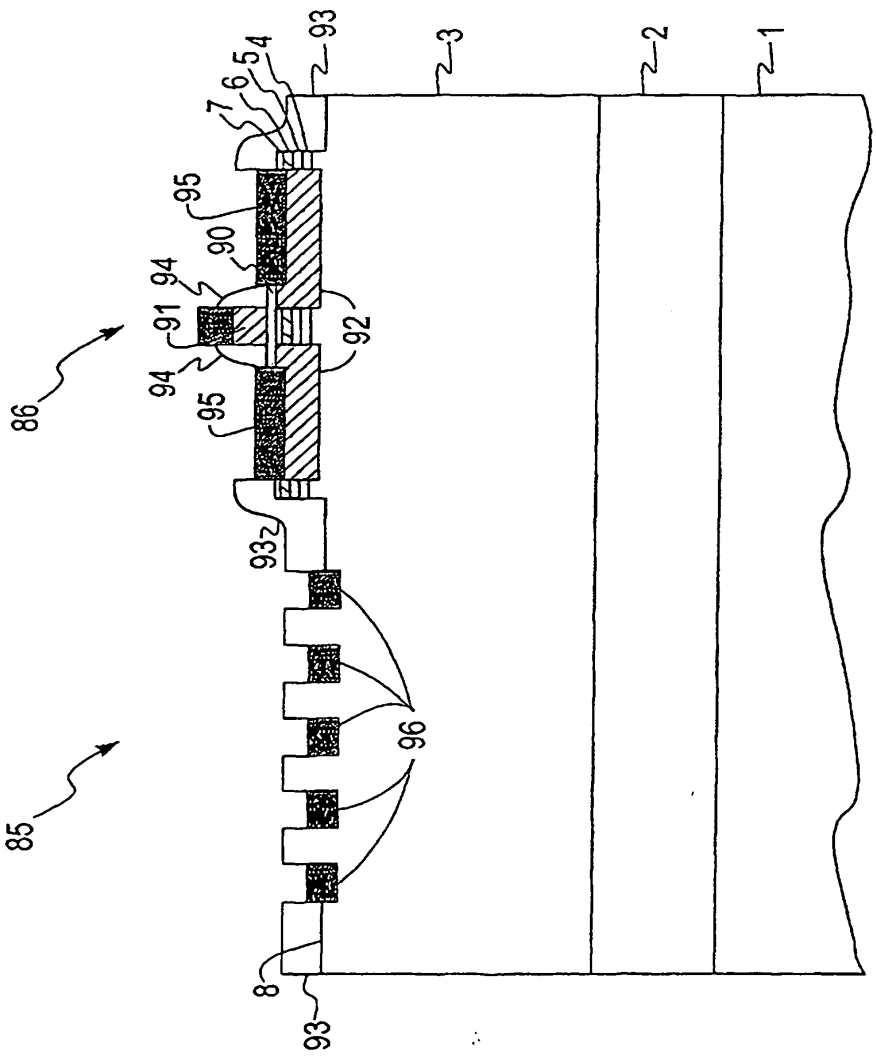


Fig. 11

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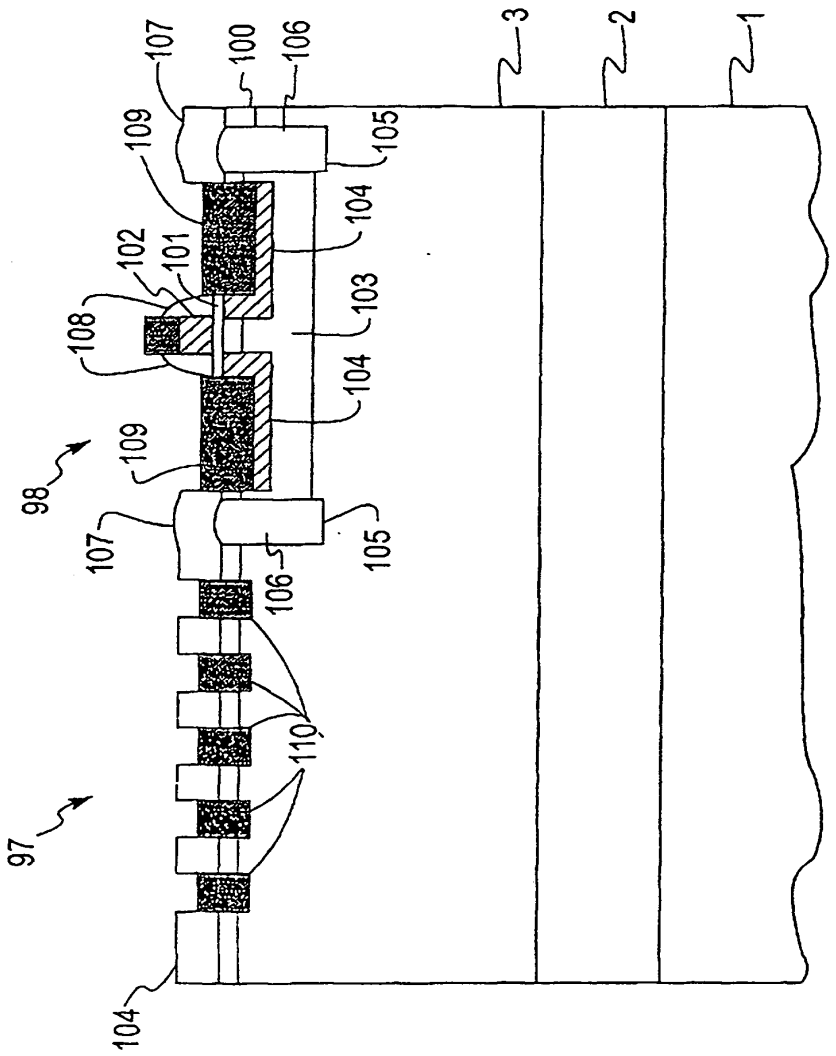


Fig. 12

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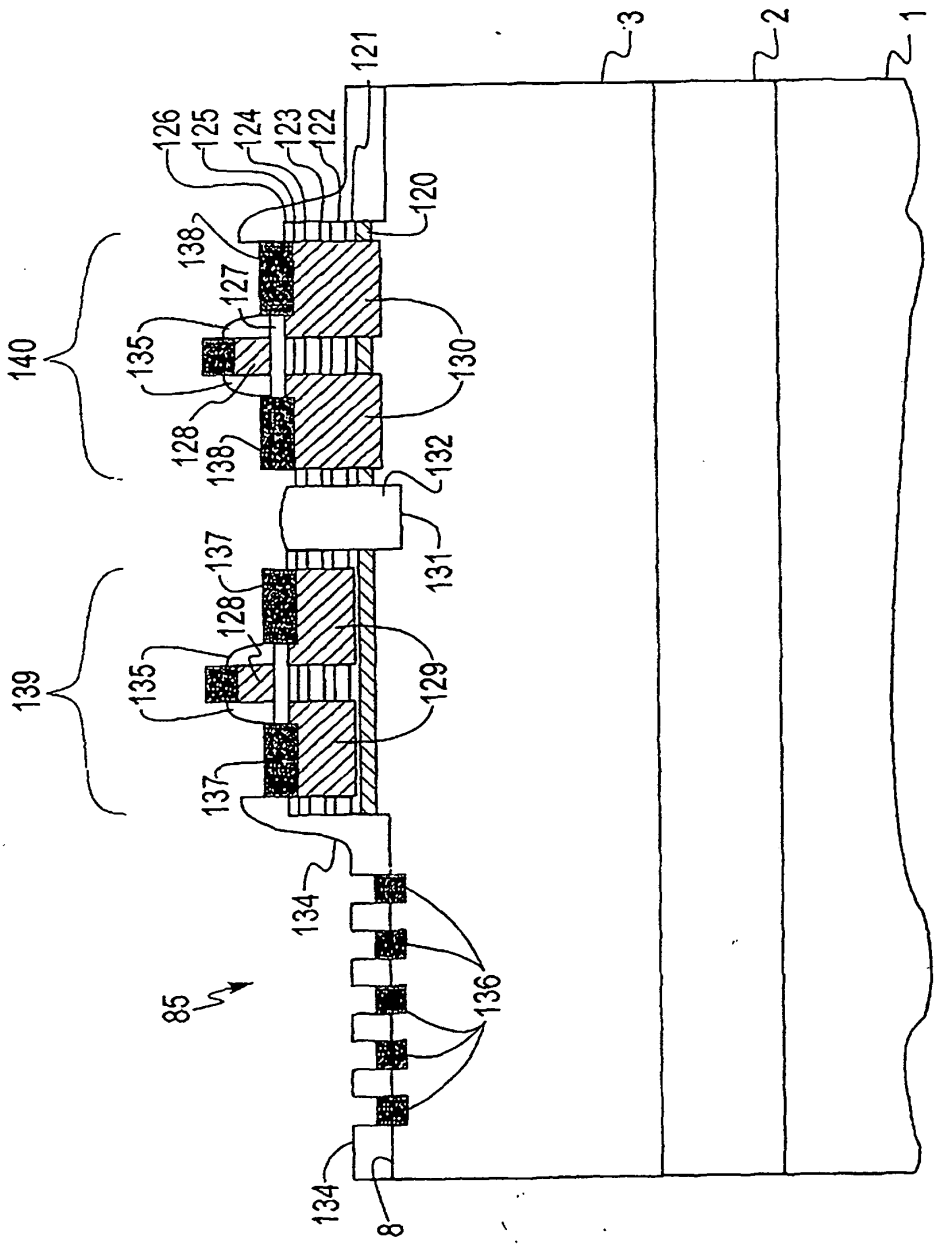


Fig. 13

Samsung Exhibit 1003, Page 168 of 654

REFERENCES CITED IN THE DESCRIPTION

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- US 5525828 A **[0005]**
- US 5659187 A **[0006] [0020]**
- US 5534713 A **[0006]**
- US 5298452 A **[0020]**

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- **J. S. Wang et al.** *IEEE Phot. Tech. Lett.,* 1993, vol. 5, 316 **[0003]**
- **V. Hurm et al.** *Electron. Lett.,* 1993, vol. 29, 9 **[0003]**
- **Y. S. He et al.** *Electron. Lett.,* 1993, vol. 29, 9 **[0004]**
- **M. Y. Liu et al.** *Appl. Phys. Lett.,* 1994, vol. 65, 887 **[0004]**
- **M. Arafa et al.** *IEEE Electron. Dev. Lett.,* 1996, vol. 17, 586 **[0006]**

Samsung Exhibit 1003, Page 169 of 654

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
24 January 2019 (24.01.2019)

WIPO | PCT

(10) International Publication Number
WO 2019/018846 A3

(51) International Patent Classification:
H01L 31/105 (2006.01) *H01L 27/144* (2006.01)
H01L 31/107 (2006.01) *G02B 6/122* (2006.01)
H01L 31/0232 (2014.01) *G02B 6/136* (2006.01)

(21) International Application Number:
PCT/US2018/043289

(22) International Filing Date:
23 July 2018 (23.07.2018)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:

62/535,801	21 July 2017 (21.07.2017)	US
62/540,524	02 August 2017 (02.08.2017)	US
62/542,243	07 August 2017 (07.08.2017)	US
62/547,728	18 August 2017 (18.08.2017)	US
62/553,844	02 September 2017 (02.09.2017)	US
62/556,426	10 September 2017 (10.09.2017)	US
62/561,869	22 September 2017 (22.09.2017)	US
62/591,072	27 November 2017 (27.11.2017)	US
62/599,246	15 December 2017 (15.12.2017)	US
62/607,860	19 December 2017 (19.12.2017)	US
62/615,314	09 January 2018 (09.01.2018)	US
62/623,971	30 January 2018 (30.01.2018)	US
62/628,764	09 February 2018 (09.02.2018)	US
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62/643,010	14 March 2018 (14.03.2018)	US
62/645,810	21 March 2018 (21.03.2018)	US
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62/651,053	30 March 2018 (30.03.2018)	US
62/651,087	31 March 2018 (31.03.2018)	US
62/652,830	04 April 2018 (04.04.2018)	US
62/659,072	17 April 2018 (17.04.2018)	US
62/659,067	17 April 2018 (17.04.2018)	US

(54) Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

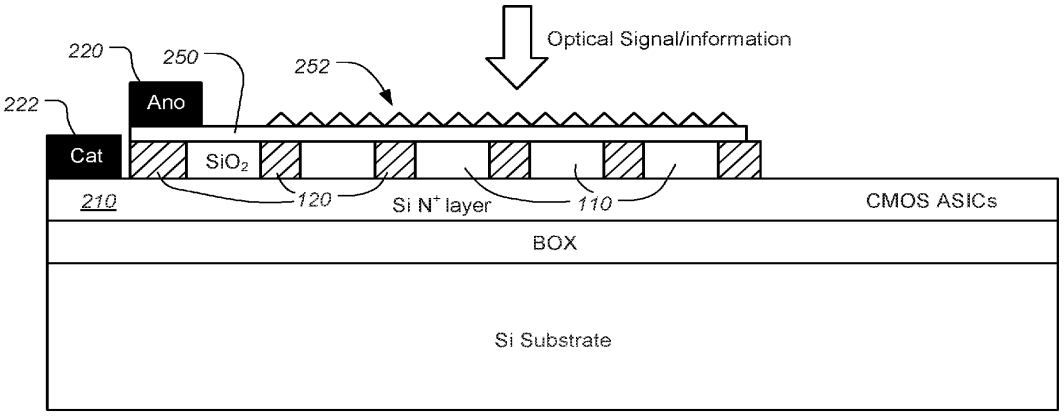


FIG. 2

(57) Abstract: Lateral and vertical micro structure enhanced photodetectors and avalanche photodetectors are monolithically integrated with CMOS/BiCMOS ASICs and can also be integrated with laser devices using fluidic assembly techniques. Photodetectors can be configured in a vertical PIN arrangement or lateral metal- semiconductor-metal arrangement where electrodes are in an inter-digitated pattern. Microstructures, such as holes and protrusions, can improve quantum efficiency in silicon, germanium and lll-V materials and can also reduce avalanche voltages for avalanche photodiodes. Applications include optical communications within and between datacenters, telecommunications, LIDAR, and free space data communication.

[Continued on next page]

WO 2019/018846 A3

62/662,217	24 April 2018 (24.04.2018)	US
62/666,005	02 May 2018 (02.05.2018)	US
62/669,194	09 May 2018 (09.05.2018)	US
62/675,130	22 May 2018 (22.05.2018)	US
62/677,609	29 May 2018 (29.05.2018)	US
62/682,909	09 June 2018 (09.06.2018)	US

(71) Applicant: W&WSENS, DEVICES INC. [US/US]; 4546 El Camino Real, Suite 215, Los Altos, CA 94022 (US).

(72) Inventors: WANG, Shih-Yuan; 766 Encina Grande Dr., Palo Alto, CA 94306 (US). **WANG, Shih-Ping**; 38 3rd Street, Suite #307, Los Altos, CA 94022 (US).

(74) Agent: KAVRUKOV, Ivan, S.; Cooper & Dunham LLP, 30 Rockefeller Plaza, 20th Floor, New York, NY 10112 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(88) Date of publication of the international search report:
28 March 2019 (28.03.2019)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US18/13289

A. CLASSIFICATION OF SUBJECT MATTER
IPC - H01L 31/105, 31/107, 31/0352, 31/0232, 27/144; G02B 6/122, 6/136 (2019.01)
CPC - H01L 31/105, 31/1075, 31/02024, 31/035281, 31/02005, 31/02327, 27/1443; G02B 6/122, 6/136

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y -- A	US 2016/0307939 A1 (WANG, S et al.) 20 October 2016; entire document	1-6, 9-14, 17-19, 21-23, 25-30, 33, 35-47, 49 -- 7-8, 15-16, 24, 31-32, 48 -- 20, 34, 50
Y -- A	US 2016/0254407 A1 (WANG, S et al.) 01 September 2016; entire document	7-8, 15-16, 24, 31-32 -- 20, 34, 50
Y	US 2004/0222357 A1 (KING, D et al.) 11 November 2004; abstract; figure 1; paragraph [0016]	48
A	US 5,525,828 A (BASSOUS, E et al.) 11 June 1996; entire document	1-50
A	US 2002/0097962 A1 (YOSHIMURA, T et al.) 25 July 2002; entire document	1-50
A	US 2015/0340538 A1 (CORIANT ADVANCED TECHNOLOGY, LLC) 26 November 2015; entire document	1-50
A	US 7,605,406 B2 (IGUCHI, Y) 20 October 2009; entire document	1-50

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 January 2019 (14.01.2019)	12 FEB 2019
Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (January 2015)

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To: IVAN S. KAVRUKOV
COOPER & DUNHAM LLP
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Date of mailing *(day/month/year)*	17 DEC 2020
Applicant's or agent's file reference: 5176/91538-PCT	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No.: PCT/US 20/51733	International filing date *(day/month/year)*: 21 September 2020 (21.09.2020)
Applicant: W&WSENS DEVICES INC.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46).

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   How? Directly to the International Bureau preferably through ePCT, or on paper to:
   The International Bureau of WIPO, 34, chemin des Colombettes, 1211 Geneva 20, Switzerland

   For more detailed instructions, see the *PCT Applicant's Guide*, International Phase, paragraphs 9.004 – 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:
   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.
   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   The applicant *may* **submit comments on an informal basis on the written opinion of the International Searching Authority** to the International Bureau. These comments will be made available to the public after international publication. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established.

   Shortly after the expiration of **18 months from the priority date, the international application will be published** by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for **entry into the national phase** before those designated Offices. In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months. For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

   Within **22 months from the priority date, the applicant may request that a supplementary international search be carried out** by a different International Searching Authority that offers this service (Rule 45*bis*.1). The procedure for requesting supplementary international search is described in the *PCT Applicant's Guide*, International Phase, paragraphs 8.006-8.032.

Name and mailing address of the ISA/US: Mail Stop PCT, Attn: ISA/US, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450	Authorized officer: Lee Young
Facsimile No. 571-273-8300	Telephone No. PCT Helpdesk: 571-272-4300

Form PCT/ISA/220 (revised January 2020)

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PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference		FOR FURTHER ACTION
6176/91538-PCT		see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US 20/51733	21 September 2020 (21.09.2020)	24 September 2019 (24.09.2019)
Applicant		
W&WSENS DEVICES INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 59

☒ as suggested by the applicant.

☐ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 20/51733

A. CLASSIFICATION OF SUBJECT MATTER
IPC - H01L 27/146, 31/101, 31/102 (2020.01)
CPC - H01L 27/14609, 27/14612, 27/14643, 31/101, 31/102

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2018/0102442 A1 (W&WSENS, DEVICES INC) 12 April 2018 (12.04.2018) entire document; especially Fig. 8; Fig. 45; para [0038], para [0203-[0248], para [0333]-[0336], para [0469]	1, 2, 6-11, 13-16, 20, 22-32, 34, 35, 37, 39-41

A		3-5, 12, 17-19, 21, 33, 36, 38, 42
Y	US 2011/0156195 A1 (TIVARUS et al.) 30 June 2011 (30.06.2011) entire document; especially Fig. 13; para [0001], [0032], [0062]	1, 2, 6-11, 13-16, 20, 22-32, 34, 35, 37, 39-41

A		3-5, 12, 17-19, 21, 33, 36, 38, 42
Y	US 2012/0153127 A1 (HIRIGOYEN et al.) 21 June 2012 (21.06.2012) entire document; especially Fig. 4; para [0052], [0057]	10

A		17
Y	US 2018/0012918 A1 (ARTILUX CORPORATION) 11 January 2018 (11.01.2018) entire document, especially para [0059]	32
A	US 2019/0166317 A1 (BRILLNICS, INC) 30 May 2019 (30.05.2019) entire document; especially para [0010]-[0012]	3-4, 33
A	US 2012/0012741 A1 (VASYLYEV) 19 January 2012 (19.01.2012) entire document; especially Fig. 10-11; para [0084], [0089]	3, 5, 12

☐ Further documents are listed in the continuation of Box C ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 November 2020	17 DEC 2020
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Lee Young Telephone No. PCT Helpdesk: 571-272-4300

Form PCT/ISA/210 (second sheet) (July 2019)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: IVAN S. KAVRUKOV
COOPER & DUNHAM LLP
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	17 DEC 2020
Applicant's or agent's file reference: 5176/91538-PCT	FOR FURTHER ACTION: See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US 20/51733	21 September 2020 (21.09.2020)	24 September 2019 (24.09.2019)

International Patent Classification (IPC) or both national classification and IPC

IPC - H01L 27/146, 31/101, 31/102 (2020.01)

CPC - H01L 27/14609, 27/14612, 27/14643, 31/101, 31/102

Applicant

W&WSENS DEVICES INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	15 November 2020	Lee Young PCT Help Desk Telephone No. 571-272-4300

Form PCT/ISA/237 (cover sheet) (revised January 2019)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/61733

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(b)).

3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:

   a. ☐ forming part of the international application as filed:

      ☐ in the form of an Annex C/ST.25 text file.

      ☐ on paper or in the form of an image file.

   b. ☐ furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.

   c. ☐ furnished subsequent to the international filing date for the purposes of international search only:

      ☐ in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).

      ☐ on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/61733

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-42	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	3-5, 12, 17-19, 21, 33, 36, 38, 42	YES
	Claims	1, 2, 6-11, 13-16, 20, 22-32, 34, 35, 37, 39-41	NO
Industrial applicability (IA)	Claims	1-42	YES
	Claims	NONE	NO

2. Citations and explanations:

Claims 1, 2, 6-9, 11, 13-16, 20, 22-31, 34, 35, 37, and 39-41 lack an inventive step under PCT Article 33(3) as being obvious over US 2018/0102442 A1 to W&Wsens, Devices Inc. (hereinafter "Wsens") in view of US 2011/0156195 A1 to Tivarus et al. (hereinafter "Tivarus").

Regarding claim 1, Wsens discloses a photosensor wafer of crystalline Si and a CMOS Logic Processor (CLP) wafer stacked on each other for electrical interaction and forming a structure (Fig.8; para [0038]- an integrated combination of a microstructure-enhanced photodetector (MSPD) and an active electronic circuit; para [0203]- Silicon chip 800 can any combination of the following devices: MSPDs; MSAPDs; vertical cavity surface emitting lasers (VCSEL) that are either wafer bonded to the chip and/or have a precision cavity for dropping the VCSEL into as in a silicon platform; CMOS/BICMOS ASICs configured for functions such as signal processing, amplifying, transmission, storage, conditioning, analyzing, and/or configured as laser drivers and/or power amplifiers; Fig.45 shows cmos layer and MSPC layer stacked on each other; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration; para [0489]- the microstructure holes can be very complex, as for example in Sierenschot et al, Fabrication of 3D fractal structures using nanoscale anisotropic etching of single crystalline silicon) comprising:
an array of laterally spaced pixels formed in said photosensor wafer (Fig. 20 and 21 shows array of laterally spaced pixels (the structures comprises MSPD 1, MSPD2 or MSPD3) in wafer; Fig. 45 shows a single pixel structure with a CMOS layer; para [0248]- FIG. 21 is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics);
wherein said pixels comprise photosensors each including one or more microstructure holes (4412) extending into said photosensor wafer (Fig. 45 shows holes 4412 extending into the said photo wafer (i Si and/or GeSi layer); para [0333]- microstructure holes 4412; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration) and further including plural N-doped and/or P-doped regions (4482, 4484) of the photosensor wafer configured to interact with light photons impinging on said pixels, including on said holes (Fig. 45; para [0330]- Ion implantation to form region 4482 can be implemented from the bottom surface; para [0333]- a depth etch monitor layer 4466 that can be implanted with ions such as Ar, Ne, Xe, O, and/or N...Also shown are upper ion implanted region 4484; para [0349]-Light and/or optical signal can impinge from the surface with the holes and in some cases light/optical signal can impinge from the substrate side through a via. The optical signal is brought to the MSPD/MSAPD via an optical fiber that can have a lens and is focused onto the surface with a certain numerical aperture such that there may be an angular distribution of light rays that are impinging on the surface of the MSPD/MSAPD.);
one or more active CMOS circuits formed in said CLP wafer (Fig.45; para [0038], [0248], [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration...reinforcement of the MSPD/MSAPD structure and CMOS/BiCMOS IC electronics.); and
electrical interconnects between said pixels and said one or more active CMOS circuits, wherein said interconnects are configured to convey electrical signals between said pixels and said one or more active CMOS circuits (Fig. 21; para [0248]- The MSPDs/MSAPDs (MSPD1, MSPD2, MSPD3, MSPD4, etc.) are connected to the CMOS/BiCMOS electronics with a transmission line 2142...The monolithically integrated chip 2100 can be flipped and the electronics can be solder bumped to external circuits such as on a printed circuit board (PCB) (not shown) for electrical signal transmission and electrical power.).
Wsens fails to discloses respective lenses over said pixels; light photons impinging on said pixels through said lenses; wherein said CLP wafer is at a side of said photosensor wafer that is opposite said lenses.
Tivarus, drawn to a stacked CMOS sensor, discloses respective lenses (1304) over pixels (1204, 1206); light photons impinging on said pixels through said lenses; wherein CLP wafer (1306) is at a side of said photosensor wafer (1300) that is opposite said lenses (1304) (Fig. 13 shows the wafer 1306 is at a side of said photosensor wafer 1300 that is opposite the lenses 1304; para [0001]-more particularly to CMOS image sensors having two separate stacked semiconductor wafers with each wafer including a portion of the electrical circuitry; para [0032]- light 302 from a subject scene is input to an imaging stage 304. Imaging stage 304 can include conventional elements such as a lens; para [0062]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1215, and charge-to-voltage conversion regions 1216. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300; para [0063]- Circuit wafer 1306;). It would have been obvious to a person having ordinary skill in the art to combine the lenses and the stacked structure disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0005]-[0006]).

--see supplemental box

Form PCT/ISA/237 (Box No. V) (revised January 2019)

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/61733

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made.

Claims 27 and 35 lack antecedent basis for terms "said lenses". For purposes of this search, claims 27 and 35 are interpreted as depending from claim 26.

Claim 42 depends on claim 3408 which is not exist. For purposes of this search, claim 42 is interpreted as depending on claim 40.

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/51733

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
Box V.2 - Citations and Explanations:

Regarding claim 2, Wsens in view of Tivarus disclose the structure of claim 1. Tivarus further discloses including respective color filters between said lenses and pixels configured to select respective wavelength ranges (Fig. 13 shows color filters 1302 between lenses 1304 and photodetectors 1202, 1204, 1206, 1208; para [0247]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300.).

Regarding claim 6, Wsens in view of Tivarus disclose the structure of claim 1, Wsens further discloses in which said at least some of said holes in the photosensor wafer are generally cylindrical (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 7, Wsens in view of Tivarus disclose the structure of claim 1, Wsens further discloses in which said at least some of said holes in the photosensor wafer are inverted pyramids (Fig. 24; para [0186]- scanning electron micrographs of holes in the shape of inverted pyramids; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.)

Regarding claim 8, Wsens in view of Tivarus disclose the structure of claim 1, Wsens further discloses in which said at least some of said holes in the photosensor wafer are funnel shaped (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 9, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which said hole of each of at least some of said pixels comprises a cluster of nanoholes (9212) into said photosensor wafer (Fig. 92 shows a cluster of nanoholes 9212, para [0560]- The nano/micro structure holes 9212 can have lateral surface dimensions ranging from 30 nm to 5000 nm or more and spacing between the nano micro structure holes can range from 10 nm to 10000 nm or more. The holes can be shaped as a circle, oval, square, polygon, hourglass, fractal, amoeba, star or a combination of shapes).

Regarding claim 11, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses including light reflectors under said pixels (Fig. 9B; para [0208]- a via 930 can be etched to remove most or all of the substrate to the etch stop layer which can in addition be patterned with nano-micro structures 914 and/or can be coated with dielectric distributed Bragg reflectors.).

Regarding claim 13, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which at least some of said holes differ in shape from one another (Fig. 24 shows the different shape of holes; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.)

Regarding claim 14, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which each of said pixels comprises laterally spaced doped regions (4284) (Fig. 41-42; para [0319]- after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-i-N to N-i-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants; para [0330]).

Regarding claim 15, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which each of said pixels comprises vertically spaced doped regions (4280) (Fig. 41-42; para [0319]- A N+ connecting well 4280 formed by ion implantation and/or diffusion can connect the cathode on the surface to the N+ layer/region 4282 and in the case of an N substrate the cathode can be on the bottom of the substrate with or without additional connect wells.; para [0330]).

Regarding claim 16, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which said pixels include Ge regions in said photosensor wafer, configured to extend a response of said pixels to light in a 2 micrometers wavelength range (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer; para [0344]- Operating wavelength range for Si I layer can range from 750 nm to 1070 nm and for GeSi can range from 750 nm to 1350 nm and in some cases 900 nm to 1350 nm and in some cases 1100 nm to 1350 nm and in some cases 1250 nm to 1550 nm and in some cases 1250 nm to 1650 nm and in some cases to 2000 nm depending on the Ge fraction in the GeSi alloy.).

Regarding claim 20, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses including doped Si conformally lining at least some of said holes and hyperdoping over said doped Si lining (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-i-N to N-i-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants (it is noted P+ or N+ doping is hyperdoping.)).

Regarding claim 22, Wsens in view of Tivarus disclose the structure of claim 1, further including a first layer of electrically insulating material under said pixels (Fig.4E shows BOX layer under the pixel; para [0215]- buried oxide (BOX) layer of 2000 nm on silicon substrate (Therefore the BOX layer is SiO2, which is an insulating material.)) and a second layer of an electrically insulating material over said active CMOS circuits (para [0442]- entire monolithically integrated MSPD/AMSPD with CMOS and/or BiCMOS electronics chip can be entirely and/or partially hermetically sealed with dielectrics such as silicon oxide, silicon nitride, aluminum oxide, aluminum nitride, polymers such as polyimide, and/or spin-on-glass.).

--see next page

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/51733

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
Box V.2 - Citations and Explanations:

Regarding claim 23, Wsens in view of Tivarus disclose the structure of claim 22. Wsens further discloses wherein the first and second layers of electrically insulating material are selected from a group consisting of Si Oxide and Si Nitride (*para* Fig.46 shows BOX layer under the pixel; *para* [0215]- buried oxide (BOX) layer of 2000 nm on silicon substrate (Therefore the BOX layer is SiO2, which is an insulating material); [0442]- entire monolithically integrated MSPD/AMSPD with CMOS and/or BiCMOS electronics chip can be entirely and/or partially hermetically sealed with dielectrics such as silicon oxide, silicon nitride, aluminum oxide, aluminum nitride, polymers such as polyimide, and/or spin-on-glass.).

Regarding claim 24, Wsens in view of Tivarus disclose The structure of claim 22. Wsens further discloses wherein one or more additional layers of electrically insulating material are formed on said first and/or second layers of electrically insulating material (Fig. 24 shows a Bragg reflector layer on BOX layer; para [0215]- buried oxide (BOX) layer of 2000 nm on silicon substrate (Therefore the BOX layer is SiO2, which is an insulating materia); para [0255]- Starting with a silicon substrate that can have a buried oxide (BOX) layer and/or buried hole layer (SOH silicon on hole), and/or with or without an etch stop layer; para [0256]- in addition a dielectric Bragg reflector; para [0319]).

Regarding claim 25, Wsens discloses a high-speed photodetector array (HSPA) wafer of crystalline Si and a CMOS Logic Processor (CLP) wafer stacked on each other for electrical interaction and forming a structure (Fig.8; *para* [0186]- FIGS. 1A-1H are top-view scanning electron micrographs of holes in the shape of inverted pyramids used in a microstructure high speed photodiode (MSPD) and/or a high speed microstructure avalanche photodiode (MSAPD); para [0208]- Arrays of MSPD/MSAPD can be monolithically integrated with CMOS/BiCMOS electronics; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration; para [0489]- the microstructure holes can be very complex, as for example in Berenschot et al, Fabrication of 3D fractal structures using nanoscale anisotropic etching of single crystalline silicon) comprising:
an array of laterally spaced photodetectors formed in said HSPA wafer (Fig. 20 and 21 shows array of laterally spaced pixels (the structures comprises MSPD 1, MSPD2 or MSPD3) in wafer; Fig. 45 shows a single pixel structure with a CMOS layer; para [0248]- FIG. 21 is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics);
wherein each of said photodetectors includes at least one microstructure hole (4412) extending into said HSPA wafer (Fig. 45 shows holes 4412 extending into the said photo wafer (I Si and/or GeSi layer); para [0333]- microstructure holes 4412; *para* [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration) and further includes plural N-doped and/or P-doped regions (4482, 4484) of the HSPA wafer configured to interact with light photons impinging on said photodetector from a first side of the HSPA wafer (Fig. 45; para [0330]- Ion implantation to form region 4482 can be implemented from the bottom surface; para [0333]- a depth etch monitor layer 4466 that can be implanted with ions such as Ar, Ne, Xe, O, and/or N...Also shown are upper ion implanted region 4484; para [0349]-Light and/or optical signal can impinge from the surface with the holes and in some cases light/optical signal can impinge from the substrate side through a via. The optical signal is brought to the MSPD/MSAPD via an optical fiber that can have a lens and is focused onto the surface with a certain numerical aperture such that there may be an angular distribution of light rays that are impinging on the surface of the MSPD/MSAPD.);
one or more active CMOS circuits formed in said CLP wafer (Fig.45; para [0038], [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration...reinforcement of the MSPD/MSAPD structure and CMOS/BiCMOS IC electronics); and
electrical interconnects between said high speed photodetector array and said one or more active CMOS circuits. wherein said interconnects are configured to convey electrical signals between said HSPA and said one or more active CMOS circuits (Fig. 21; para [0248]- The MSPDs/MSAPDs (MSPD1, MSPD2, MSPD3, MSPD4, etc.) are connected to the CMOS/BiCMOS electronics with a transmission line 2142...The monolithically integrated chip 2100 can be flipped and the electronics can be solder bumped to external circuits such as on a printed circuit board (PCB) (not shown) for electrical signal transmission and electrical power).
Wsens fails to disclose wherein said CLP wafer is at a side of said HSPA wafer that is opposite said first side.
Tivarus, drawn to a stacked CMOS sensor, discloses CLP wafer (1306) is at a side of a wafer (1300) that is opposite the first side (Fig. 13 shows the wafer 1306 is at a side of the wafer 1300 that is opposite the side with photodetectors; para [0001]-more particularly to CMOS image sensors having two separate stacked semiconductor wafers with each wafer including a portion of the electrical circuitry; para [0062]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300; para [0063]- Circuit wafer 1306;). It would have been obvious to a person having ordinary skill in the art to combine the stacked structure disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0005]-[0006]).

Regarding claim 26, Wsens in view of Tivarus disclose the structure of claim 25 and the HSPA wafer as discussed above. Tivarus further discloses including an array of lenses (1304) formed over the photodetectors (1204, 1206) on said first side of the wafer (1300) (Fig. 13; para [0062]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300). It would have been obvious to a person having ordinary skill in the art to combine the lenses disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0005]-[0006]).

Regarding claim 27. Wsens in view of Tivarus disclose the structure of claim 26. Wsens further discloses plural holes in pixels in said HSPA wafer (Fig. 45 shows plural holes in a single pixel structure; para [0333]- microstructure holes 4412; said photodetectors and said active CMOS circuits are configured to operate at 56 Gb/s or greater data rates that include 112 Gb/s (para [0218]- With thinner I layer, 50 Gb/s, 60 Gb/s, 80 Gb/s, 100 Gb/s can be achieved). Tivarus further discloses in which each of said lenses overlies each pixel (See Tivarus, Fig. 13; para [0062]- A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300). Therefore the lenses disclosed in Tivarus overlies the holes of Wsens since they overly the substrate of Tivarus and the substrate of Wsens has holes.

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Regarding claim 28, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which at least some of said holes in the HSPA wafer are generally cylindrical (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 29, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which at least some of said holes in the HSPA wafer are inverted pyramids (Fig. 24; para [0186]- scanning electron micrographs of holes in the shape of inverted pyramids; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 30, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which at least some of said holes in the HSPA wafer are funnel shaped (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 31, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses including an array of optical filters (2014, 2016, 2018) formed at said first side of the HSPA wafer over said photodetectors (Fig. 20, para [0246]- Bandpass filters can also be fabricated on the top surface where the microstructured holes for absorption enhancement are etched; para [0247]- Note that some or all of the MSPDs can also be MSAPDs. The MSPDs form an array where each MSPD1, MSPD2, MSPD3. . . . MSPDn has a bandpass filter with its own unique bandpass wavelength. Having a different bandpass wavelength for each of the MSPD in the array allows for the selection of specific wavelengths in a CWDM optical signal).

Regarding claim 34, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which said photodetectors include Ge regions in said HSPA wafer, configured to enhance a response of said photodetectors to light in a wavelength range that includes 1350 nm and / or in a wavelength range that includes1550 nm (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer; para [0344]- Operating wavelength range for SI I layer can range from 750 nm to 1070 nm and for GeSI can range from 750 nm to 1350 nm and in some cases 900 nm to 1350 nm and in some cases 1100 nm to 1350 nm and in some cases 1250 nm to 1550 nm and in some cases 1250 nm to 1650 nm and in some cases to 2000 nm depending on the Ge fraction in the GeSi alloy).

Regarding claim 35, Wsens in view of Tivarus disclose the structure of claim 26. Wsens further discloses plurality of holes in pixels (Fig. 45 shows plurality of holes in a single pixel structure; para [0333]- microstructure holes 4412). Tivarus further discloses in which at least some of said lenses overlies each pixel (See Tivarus, Fig. 13; para [0062]- A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300). Therefore the lenses overlies the holes since they overly the substrate and the substrate of Wsens has holes. Wsens further discloses said photodetector array and said CMOS active circuits are configured to operate at data rates of 56 Gb/s or higher (para [0218]- With thinner I layer, 50 Gb/s, 60 Gb/s, 80 Gb/s, 100 Gb/s can be achieved.)

Regarding claim 37, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses including doped Si conformally lining said holes and hyperdoping over said doped Si lining the holes (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSI layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants (It is noted P+ or N+ doping is hyperdoping.)).

Regarding claim 39, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which said CLP wafer includes clock recovery circuits and transimpedance amplifiers (para [0045]- The additional active electronic circuits can comprise one or more transimpedance amplifiers (TIAs); para [0273]- The CMOS/BiCMOS ASICs can include one or more of the following: TIAs; clock data recovery (CDR) circuitry; equalizers; and limiting amplifiers (LA),), and wherein said HSPA and CLP wafers are configured to operate at aggregated data rates of 400-1000 Gb/s or more (para [0268]- increase the aggregated data rates to greater than 40 Gb/s and in some cases greater than 100 Gb/s and in some cases greater than 1 Tb/s.).

Regarding claim 40, Wsens discloses a monolithic wafer of crystalline Si having a first side and a second side (Fig. 39; para [0325]- and/or polycrystalline silicon layers; para [0489]- the microstructure holes can be very complex, as for example in Berenschot et al, Fabrication of 3D fractal structures using nanoscale anisotropic etching of single crystalline silicon), comprising: an array of laterally spaced photosensor or photodetector pixels formed at said first side of the wafer (Fig. 20 and 21 shows array of laterally spaced pixels (the structures comprises MSPD 1, MSPD2 or MSPD3) in wafer; Fig. 45 shows a single pixel structure with a CMOS layer; para [0248]- FIG. 21 is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics);
wherein each of said pixels includes at least one hole (4412) formed into said first side of the wafer (Fig. 45 shows holes 4412 formed into the said photo wafer (I Si and/or GeSI layer); para [0333]- microstructure holes 4412; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration) and further includes plural N-doped and/or P-doped regions (4482, 4484) of the wafer configured to interact with light photons impinging on said pixels, including on said holes (Fig. 45; para [0330]- Ion implantation to form region 4482 can be implemented from the bottom surface; para [0333]- a depth etch monitor layer 4466 that can be implanted with ions such as Ar, Ne, Xe, O, and/or N.. Also shown are upper ion implanted region 4484; para [0349]-Light and/or optical signal can impinge from the surface with the holes and in some cases light/optical signal can impinge from the substrate side through a via. The optical signal is brought to the MSPD/MSAPD via an optical fiber that can have a lens and is focused onto the surface with a certain numerical aperture such that there may be an angular distribution of light rays that are impinging on the surface of the MSPD/MSAPD.);
CMOS logic processors (para [0038], [0246]- FIG. 21 is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics); and (claim 40 continued)

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(claim 40 continued) electrical interconnects in said wafer configured to convey electrical signals between said pixels and said one or more active CMOS circuits (Fig. 21; para [0248]- The MSPDs/MSAPDs (MSPD1, MSPD2, MSPD3, MSPD4, etc.) are connected to the CMOS/BiCMOS electronics with a transmission line 2142...The monolithically integrated chip 2100 can be flipped and the electronics can be solder bumped to external circuits such as on a printed circuit board (PCB) (not shown) for electrical signal transmission and electrical power). Wsens fails to disclose respective optical lenses over said pixels configured to direct to said pixels and said holes light impinging on said first side of the wafer; CMOS logic processors formed at said second side of the wafer.
Tivarus, drawn to a stacked CMOS sensor, discloses respective optical lenses (1304) over the pixels (1302, 1304) configured to direct to said pixels light impinging on the first side of the wafer (upper side); CMOS logic processors (1306) formed at the second side of the wafer (lower side). (Fig. 13; para [0001]-more particularly to CMOS image sensors having two separate stacked semiconductor wafers with each wafer including a portion of the electrical circuitry; para [0032]- light 302 from a subject scene is input to an imaging stage 304. Imaging stage 304 can include conventional elements such as a lens; para [0062]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300; para [0063]- Circuit wafer 1306;). It would have been obvious to a person having ordinary skill in the art to combine the lenses and the stacked structure disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0005]-[0006]).

Regarding claim 41, Wsens in view of Tivarus disclose the monolithic wafer of claim 40. Wsens further discloses plurality of holes in pixels in the wafer (Fig. 45 shows plurality of holes in a single pixel structure; para [0333]- microstructure holes 4412). Tivarus further discloses in which at least some of said lenses overlies each pixel (See Tivarus, Fig. 13; para [0062]- A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300). Therefore the lenses disclosed by Tivarus overlies the holes disclosed in Wsens since they overly the substrate in Tivarus and the substrate of Wsens has holes.

Claim 10 lacks an inventive step under PCT Article 33(3) as being obvious over Wsens in view of Tivarus and further in view of US 2012/0153127 A1 to Hirigoyen et al. (hereinafter "Hirigoyen").

Regarding claim 10, Wsens in view of Tivarus disclose the structure of claim 1, but fails to discloses further including light blockers between adjacent pixels to reduce crosstalk. Hirigoyen, drawn to image sensor, discloses light blocker (40) between adjacent pixels (S1, S2) to reduce crosstalk (Fig. 4; para [0008], [0052]-isolation region 11.. reduces optical crosstalk thanks to an optical waveguide formed by the differences in refractive indices between the substrate 10, the conductive material 30, and the optical isolator 40. para [0057]- Image sensor IS3 differs from image sensor IS2 in that the color filters F1, F2, F3 and the microlenses L1, L2, L3 are arranged on the backside of the substrate 10...the optical isolator 40 extends entirely through the trench 15). It would have been obvious to a person having ordinary skill in the art to combine the light blockers disclosed by Hirigoyen to the structure disclosed by Wsens to enhance the performance by reducing the corsstalk between pixels (See Hirigoyen, para [0052]).

Claim 32 lacks an inventive step under PCT Article 33(3) as being obvious over Wsens in view of Tivarus and further in view of US 2018/0012916 A1 to Artilux Corporation (hereinafter "Artilux").

Regarding claim 32, Wsens in view of Tivarus disclose the structure of claim 31. Wsens further discloses array of optical filters (para [0241]- each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array). Wsens in view of Tivarus fail to disclose said array of optical filters includes Near InfraRed (NIR) filters to select specific NIR wavelength ranges. Artilux, drawn to image sensor array, discloses NIR filter to select specific NIR wavelength ranges (para [0059]- the optical signal 406 may be filtered by a wavelength filter not shown in this figure, such as an NIR filter in the filter layer). It would have been obvious to a person having ordinary skill to include some of the NIR filters disclosed by Artilux to the array of optical filters to increase the performance of the filter by enabling electing specific NIR wavelength ranges (See Artilux, para [0059]).

Claims 3-6, 12, 17-19, 21, 33, 36, 38, and 42 meet the criteria set forth under PCT Article 33(2)-(3) because the prior art does not teach or fairly suggest the subject matter claimed.

The prior art for claim 3 is exemplified by Wsens, Tivarus, US 2019/0166317 A1 to Brillnics, Inc (hereinafter "Brillnics"), and US 2012/0012741 A1 (Vasylyev).

Regarding claim 3,
Wsens in view of Tivarus disclose the structure of claim 2. Wsens further discloses at least one Near InfraRed (NIR) pixel and an NIR optical filter over said NIR pixel to select specific NIR wavelength ranges (para [0192]- The wavelength range, depending on the percentage of Ge in Si, for 0% Ge can range from 840-960 nm, and with 10% Ge or less in GeSi alloy that is either relaxed or not relaxed, the wavelength can range from 840-990 nm for not relaxed GeSi layer and 840-960 nm for relax, for 20% or less Ge, the wavelength can be extended to 1000 nm and in some cases to 1250 nm for not relaxed GeSi layer and for 40% or less Ge, the wavelength can be extended to 1310 nm (it is noted the wavelength of 840-1310 nm is in the NIR wavelength range); para [0241]- each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array.) Wsens in view of Tivarus fail to disclose in which said pixels are configured in a Bayer array and each of at least several pixels in the Bayer array encompasses only a single hole in said photosensor wafer.

Brillnics, drawn to a CMOS sensor, discloses pixels are configured in a Bayer array (para [0068]-when the unit pixel groups are arranged in the Bayer array) that includes at least one Near InfraRed (NIR) pixel (para [0096]- The color pixels in the unit RGB pixel group 200 configured as described above not only have an inherent particular responsibility in a visible range (400 nm to 700 nm), but also have a high responsibility in a near-infrared (NIR) region (800 nm to 1,000 nm)). However, Brillnics otherwise fails to remedy the deficiencies of Wsens and Tivarus.

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Vasylyev, drawn to a light detector, discloses one lenses with one hole (Fig. 10-11; para [0089]- FIG. 10 shows a cone-shape cavity forming light input port 14; para [0084]- Light input ports 14 have the same number as the number of lenses 10 in focusing array 6 disposed on top of photovoltaic layer 4. Light input ports 14 are also distributed over surface 32 in accordance with the distribution of lenses 10 in the lens array so that there is a pairwise optical relationship between each lens 10 and the corresponding light input port 14). However, Vasylyev fails to remedy the deficiencies of Wsens , Tivarus and Brillnics.

None of the prior art discloses each of at least several pixels in the Bayer array encompasses only a single hole in said photosensor wafer. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 3, therefore claim 3 meets the criteria set out in PCT Article 33(2)-(3).

The prior art for claim 4 and 33 is exemplified by Wsens, Tivarus and Brillnics.

Regarding claim 4, Wsens in view of Tivarus disclose the structure of claim 2, but fail to disclose in which said pixels include one or more Bayer arrays at least one of which comprises a Near InfraRed (NIR) pixel, and wherein the at least one NIR pixel in at least one of said one or more Bayer arrays is larger than other pixels therein.

Brillnics, drawn to a CMOS sensor, discloses pixels include one or more Bayer arrays at least one of which comprises a Near InfraRed (NIR) pixel (para [0068]-when the unit pixel groups are arranged in the Bayer array; para [0098]- the photodiode PD22 serving as the second green (Gr) photoelectric conversion part also operate as infrared (NIR) photoelectric conversion parts.). However, Brillnics otherwise fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses wherein the at least one NIR pixel in at least one of said one or more Bayer arrays is larger than other pixels therein. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 4, therefore claim 4 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 33, Wsens in view of Tivarus disclose the structure of claim 32, but fail to disclose wherein said array of photodetectors includes some that are larger than others, and said larger photodetectors are under said NIR filters.

Brillnics, drawn to a CMOS sensor, discloses NIR photodetector are larger (para [0012]-Further, there has been known an infrared (IR, NIR) sensor in which the four pixels in a unit pixel group are replaced with one NIR dedicated pixel having a larger pixel size.). However, Brillnics otherwise fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses wherein said array of photodetectors includes some that are larger than others, and said larger photodetectors are under said NIR filters. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 33, therefore claim 33 meets the criteria set out in PCT Article 33(2)-(3).

The prior art for claim 5 and 12 is exemplified by Wsens, Tivarus and Vasylyev

Regarding claim 5, Wsens in view of Tivarus disclose the structure of claim 1, but fail to disclose in which each of said at least some of said pixels has only a single one of said holes.

Vasylyev, drawn to a light detector, discloses one lenses with one hole (Fig. 10-11; para [0084]- Light input ports 14 have the same number as the number of lenses 10 in focusing array 6 disposed on top of photovoltaic layer 4. Light input ports 14 are also distributed over surface 32 in accordance with the distribution of lenses 10 in the lens array so that there is a pairwise optical relationship between each lens 10 and the corresponding light input port 14; para [0089]- FIG. 10 shows a cone-shape cavity forming light input port 14.). However, Vasylyev fails to remedy the deficiencies of Wsens.

None of the prior art discloses in which each of said at least some of said pixels has only a single one of said holes. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 5, therefore claim 5 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 12, Wsens in view of Tivarus disclose the structure of claim 1, but fail to disclose in which at least some of said pixels have only a single hole each and said single hole is an off-center hole.

Vasylyev, drawn to a light detector, discloses photodetector have only a single hole each (Fig. 10-11; para [0089]- FIG. 10 shows a cone-shape cavity forming light input port 14; para [0084]- Light input ports 14 have the same number as the number of lenses 10 in focusing array 6 disposed on top of photovoltaic layer 4. Light input ports 14 are also distributed over surface 32 in accordance with the distribution of lenses 10 in the lens array so that there is a pairwise optical relationship between each lens 10 and the corresponding light input port 14). However, Vasylyev fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses said single hole is an off-center hole. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 12, therefore claim 12 meets the criteria set out in PCT Article 33(2)-(3).

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The prior art for claim 17 is exemplified by Wsens, Tivarus and Hirigoyen.

Regarding claim 17, Wsens in view of Tivarus discloses the structure of claim 1, but fails to discloses in which said pixels have slanted sidewalls configured to reduce crosstalk between adjacent pixels and improve optical confinement.

Hirigoyen, drawn to image sensor, discloses sidewalls (40) configured to reduce crosstalk between adjacent pixels and improve optical confinement (Fig. 4; para [0052]- isolation region 11.. reduces optical crosstalk thanks to an optical waveguide formed by the differences in refractive indices between the substrate 10, the conductive material 30, and the optical isolator 40. para [0057]- Image sensor IS3 differs from image sensor IS2 in that the color filters F1, F2, F3 and the microlenses L1, L2, L3 are arranged on the backside of the substrate 10...the optical isolator 40 extends entirely through the trench 15). However, Hirigoyen otherwise fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses said pixels have slanted sidewalls configured to reduce crosstalk between adjacent pixels and improve optical confinement. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 17, therefore claim 17 meets the criteria set out in PCT Article 33(2)-(3).

The prior art for claims 18-19, 21, 36, 38 and 42 is exemplified by Wsens and Tivarus.

Regarding claim 18, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which said holes are conformally lined with doped Si (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants). Wsens in view of Tivarus fail to disclose at least some adjacent holes are doped to opposite polarities.

None of the prior art discloses at least some adjacent holes are doped to opposite polarities. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 18, therefore claim 18 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 19, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses graphene (para [0195]- the basic steps consist of etching holes in a device wafer that can include epitaxial layers that can include doped P and/or N and/or I layers, SOI, additional dielectric coatings, metallic layers/fillers, graphene). Wsens in view of Tivarus fail to disclose at least some of said holes are conformally lined with graphene.

None of the prior art discloses at least some of said holes are conformally lined with graphene. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 19, therefore claim 19 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 21, Wsens in view of Tivarus disclose the structure of claim 1, but fail to disclose in which said pixels are in an array in which centrally located pixels are smaller in size that other pixels.

None of the prior art discloses said pixels are in an array in which centrally located pixels are smaller in size that other pixels. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 21, therefore claim 21 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 36, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which said holes are conformally lined with doped Si (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants). Wsens in view of Tivarus fail to disclose adjacent holes are doped to opposite polarities.

None of the prior art discloses adjacent holes are doped to opposite polarities. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 36, therefore claim 36 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 38, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses graphene (para [0195]- the basic steps consist of etching holes in a device wafer that can include epitaxial layers that can include doped P and/or N and/or I layers, SOI, additional dielectric coatings, metallic layers/fillers, graphene). Wsens in view of Tivarus fail to disclose said holes are conformally lined with graphene.

None of the prior art discloses said holes are conformally lined with graphene. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 38, therefore claim 38 meets the criteria set out in PCT Article 33(2)-(3).

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Regarding claim 42. Wsens in view of Tivarus disclose the monolithic wafer of claim 40. Wsens further discloses in which said holes are lined with doped regions of said wafer (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-i-N to N-i-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants). Wsens in view of Tivarus fail to disclose adjacent holes are lined with doped regions of opposite polarities.

None of the prior art discloses adjacent holes are lined with doped regions of opposite polarities. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 42, therefore claim 42 meets the criteria set out in PCT Article 33(2)-(3).

Claims 1-42 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.

SEARCH HISTORY

Application Number	PCT/US 20/51733
Search Conducted By	JQ
Search Approved By	ALK

CPC/IPC Classifications Searched	CPC - H01L 27/14609, 27/14612, 27/14643, 31/101, 31/102 IPC (8)- H01L 27/146, 31/101, 31/102 (2020.01)
Date Conducted	09 November 2020 (09.11.2020)

Documentation Searched	CPC - H01L 27/14609, 27/14612, 27/14643, 31/101, 31/102 IPC (8)- H01L 27/146, 31/101, 31/102 (2020.01)
Search Terms Used	Photosensor/photodetect*/photodiode/hspa Wafer/substrate Crystal/crystalline Si/silicon Cmos/clp Stack~/layer~ Pixel Array/grid Lens/lenses/microlenses Hole/opening/aperture Micro/microstructure/um N/P/dope~ Lines/traces/interconnects
Date Conducted	09 November 2020 (09.11.2020)

Electronic Database Searched	PatBase
Files Searched	Full-text: AU BE BR CA CH CN DE DK EP ES FI FR GB IN JP KR SE TH TW US WO Bibliographic: Europe AT BA BE BG CH CS CY CZ DD DK EE ES FI GE GR HR HU IE IS IT LT LU LV MC MD MT NL NO PL PT RO RS SE SI SK SM TR UA YU Asia EA GC HK ID IL IN KZ MN MY PH RU SG SU TH TJ TW UZ VN North America CA CR CU DO GT HN MX NI PA SV TT South America AR BR CL CO EC PE UY Australasia AU NZ Africa AP DZ EG KE MA MW OA ZA ZM ZW
Date Conducted	09 November 2020 (09.11.2020)
Search Logic:	
Classification Search: 1) IC=(H01L27/146 or H01L31/101 or H01L 31/102) (45716)	

2) CPC=(H01L27/14609 or H01L27/14612 or H01L27/14643 or H01L31/101 or H01L31/102) (9304)
3) 1 or 2 (46498)
4) 3 and FT=(Photosensor? or photodetect* or photodiode? or hspa) (13742)
5) 4 and FT=(wafer or substrate) (11476)
6) 5 and FT=((crystal or crystalline) w3 (Si or silicon)) (1286)
7) 6 and FT=(cmos or clp) (747)
8) 7 and FT=(stack~ or layer~) (733)
9) 8 and FT=(pixel?) (561)
10) 9 and FT=(array or grid) (423)
11) 10 and FT=(lens or lenses or microlenses) (281)
12) 11 and FT=(hole? or opening? or aperture?) (181)
13) 12 and FT=(micro or microstructure or um) (146)
14) 13 and FT=(N or P or doped or doping) (144)
15) 14 and FT=(lines or traces or interconnects) (102)
16) 15 and FT=(color w3 filter?) (57)
17) 16 and FT=("Near InfraRed" or NIR) (26)
18) 16 and FT=(cmos w3 circuit?) (19)
19) 18 not 17 (13)
20) 3 and FT=(cmos or clp) (20106)
21) 20 and FT=((Photosensor? or photodetect* or photodiode? or hspa) w3 (wafer or substrate)) (762)
22) 21 and FT=((array or grid) w3 pixel?) (211)
23) 22 and FT=(lens or lenses or microlenses) (158)
24) 23 and FT=(hole? or opening? or aperture?) (101)
25) 24 and FT=(micro or microstructure or um) (79)
26) 25 and FT=(lines or traces or interconnects) (70)
27) 26 and FT=(color w3 filter?) (49)
28) 27 not (17 or 18) (39)
29) 26 and FT=("Near InfraRed" or NIR) (16)
30) 29 not (17 or 18 or 27) (3)

Search limited only by search terms and not by classifications:
31) FT=((Photosensor? or photodetect* or photodiode? or hspa) w3 (wafer or substrate)) (3738)
32) 31 and FT=(cmos or clp) (1143)
33) 32 and FT=((array or grid) w3 pixel?) (272)
34) 33 and FT=(lens or lenses or microlenses) (205)
35) 34 and FT=(hole? or opening? or aperture?) (126)
36) 35 and FT=(micro or microstructure or um) (98)
37) 36 and FT=(lines or traces or interconnects) (83)
38) 37 and FT=(color w3 filter?) (53)
39) 38 not (17 or 18 or 27 or 29) (4)
40) 37 and FT=("Near InfraRed" or NIR) (20)
41) 40 not (17 or 18 or 27 or 29 or 38) (3)
42) FT=(cmos w3 circuit?) (17544)
43) 42 and FT=((Photosensor? or photodetect* or photodiode? or hspa) w3 (wafer or substrate)) (110)
44) 43 and FT=((array or grid) w3 pixel?) (39)
45) 44 not (17 or 18 or 27 or 29 or 38 or 40) (29)
46) 42 and FT=(Photosensor? or photodetect* or photodiode? or hspa) (1555)
47) 46 and FT=((crystal or crystalline) w3 (Si or silicon)) (443)
48) 47 and FT=((array or grid) w3 pixel?) (64)
49) 48 not (17 or 18 or 27 or 29 or 38 or 40 or 44) (42)

F/B search:
50) PN=(us2018102442 or us2017250211) (2)
51) CTB 50 or CTF 50 (269)
52) 51 not (17 or 18 or 27 or 29 or 38 or 40 or 44 or 48) (265)
53) 52 and FT=(cmos w3 circuit?) (13)

Electronic Database Searched	Google
Files Searched	Google Patents
Date Conducted	09 November 2020 (09.11.2020)

Search Logic:

photosensor cmos logic processor
About 12,000 results

photosensor cmos logic processor wafer
About 3,810 results

photosensor cmos logic processor wafer array pixels
About 2,760 results

photosensor cmos logic processor wafer array pixels lenses
About 2,090 results

photosensor cmos logic processor wafer array pixels lenses n-doped
About 802 results

photosensor cmos logic processor wafer array pixels lenses p-doped
About 1,850 results

photosensor cmos circuits wafer array pixels lenses
About 4,400 results

photosensor cmos circuits wafer array pixels lenses NIR
About 1,270 results

Electronic Database Searched	Google
Files Searched	Google Scholar
Date Conducted	09 November 2020 (09.11.2020)

Search Logic:

photosensor cmos logic processor
About 20,000 results

photosensor cmos logic processor wafer
About 5,410 results

photosensor cmos logic processor wafer array pixels
About 3,250 results

photosensor cmos logic processor wafer array pixels lenses
About 1,980 results

photosensor cmos logic processor wafer array pixels lenses n-doped
About 157 results

photosensor cmos logic processor wafer array pixels lenses p-doped
About 145 results

photosensor cmos circuits wafer array pixels lenses
About 6,740 results

photosensor cmos circuits wafer array pixels lenses NIR
About 1,120 results

Supplemental SAO searching:

Electronic Database Searched	PatBase
Files Searched	Full-text: AU BE BR CA CH CN DE DK EP ES FI FR GB IN JP KR SE TH TW US WO Bibliographic: (Europe) AT BA BE BG CH CS CY CZ DD DK EE ES FI GE GR HR HU IE IS IT LT LU LV MC MD MT NL NO PL PT RO RS SE SI SK SM TR UA YU (Asia) EA GC HK ID IL IN KZ MN MY PH RU SG SU TH TJ TW UZ VN (North America) CA CR CU DO GT HN MX NI PA SV TT (South America) AR BR CL CO EC PE UY (Australasia) AU NZ (Africa) AP DZ EG KE MA MW OA ZA ZM ZW
Date Conducted	20 November 2020 (20.11.2020)
Search Logic:	
Search 1:	(photosens* or photodetect*) (Results 567476)
Search 2:	1 and (wafer or substrate or chip) (Results 212373)
Search 3:	2 and (si or silicon) (Results 111160)
Search 4:	3 and (CMOS) (Results 15125)
Search 5:	4 and (pixel%) (Results 9352)
Search 6:	5 and (dope or doped or doping) (Results 4083)
Search 7:	6 and (lens or lenses or microlenses) (Results 2208)
Search 8:	7 and ((connect* or interconnect*) near pixel%) (Results 813)
Search 9:	8 and (holes OR microholes) (Results 481)
Search 10:	8 and (holes OR microholes or nanohole%) (Results 481)
Search 11:	10 and ((holes OR microholes or nanohole%) near (lens or lenses or microlenses)) (Results 3)
Search 12:	10 and ((holes OR microholes or nanohole%) near (pixel%)) (Results 40)
Search 13:	10 and Bayer (Results 103)
Search 14:	13 and (IR or NIR or infrared or (infra%red) or (infra_red)) (Results 86)
Search 15:	10 and (((holes OR microholes or nanohole%) near (pixel%)) near (one or single)) (Results 8)
Search 16:	10 and (((wall% or sidewall%) near pixel%) near (angle~ or slant~)) (Results 2)

Search 17:	10 and ((hole% or microhole%) near dope~) (Results 18)

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SUBJECT OF THE INVENTION

SUBJECT OF THE INVENTION

Improvement in the speed of a response speed can be achieved, and manufacture provides an easy near-infrared-light sensing element.
PROBLEM to be solved
The photoelectric-conversion part 6 which has a photodiode structure of a pin photodiode which forms in 1 surface side of the semiconductor substrate 1, and the i layer 62 which is a drift area| region interposes between the p form area|region 61 and the n form area|region 63, absorbs near infrared light, and an electronic * hole pair generate|occur|produces,
With respect to the wavelength range of the near infrared light of the detection target which injects from the direction which is a slab type|mold photonic crystal which is laminated|stacked on the light-receiving surface of the photoelectric-conversion part 6, and has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and intersects said light-receiving surface
The slab type|mold photonic crystal 7 by which the refractive-index period structure was designed have a resonance peak is provided.

DETAILED DESCRIPTION of the INVENTION

[**0001**] TECHNICAL FIELD
This invention relates to the near-infrared-light sensing element which detects near infrared light.

DESCRIPTION OF RELATED ART

[0002] Conventionally, in the optical communication, the near-infrared-light sensing element is used as a light receiving element for receiving a light signal.
As this kind of a near-infrared-light sensing element, the photodiode (pn photodiode, a pin photodiode, an avalanche photo-diode, the Schottky photodiode, etc.) in which the pn junction and the schottky junction were formed is widely used for a semiconductor crystal.
It utilizes that the electric current which the electronic-hole pair generate|occur|produced when the light which has the photon energy more than a band gap injects is isolate|separated, travel|drive| works in a depletion layer (drift), and flows into an external circuit changes,
A light signal is detected as electric current change or voltage change.
As a semiconductor crystal material used for a near-infrared-light sensing element in here, there exists compound-semiconductor crystal|crystallization material (InGaAs, InGaAsP, etc.) other than Si or Ge,
However,
It is properly used by the wavelength range of the light used by an optical communication, the transmission speed request|required, the price, etc.

[0003] By the way, the optical communication is already widely used as a communication network between cities and in a city,
However,
In recent years, the motion which employ|adopts an optical communication also, for example in field|areas, such as SAN(Storage Area Network) which connects a highly efficient server and a router, DVI(Digital Visual Interface) which connects what is called an information appliance and a peripheral device, in-vehicle LAN(Local Area Network), a mobile phone, is activating.
The high-speed optical communication is required also in such a field|area,
Progress of improvement in the speed of transmission speed changes with applicable fields,
It is estimated that the transmission speed of 1Gbps or more is request|required also in either field| area.

[0004] Improvement in the speed and a lowering of cost of a response speed will be request|required of the photodiode for optical communications used in the above various field|areas from now on.
In here, it is known that the response speed of a photodiode will be fundamentally limited with two elements with the transit time t of the career|carrier (an electron, a hole) which carries out the drift of the inside of a depletion layer to CR time constant of a photodiode.
In order to raise quantum efficiency (light-reception sensitivity) while making CR time constant small when the pin photodiode using Si as a semiconductor crystal material is considered for an example, the wide depletion layer is formed,
Therefore
It becomes impossible for the transit time t of the electron which carries out the drift of the inside of a depletion layer to ignore at the time of a high-speed response.

[0005] For example, in order for quantum efficiency to be 80 % or more by the pin photodiode of Si, a depletion-layer width W of about 30 micrometer is needed,
However,
When cut-off-frequency fc (CR) decided by CR time constant sets the diameter of a light reception to 250 micrometer, the pn-junction area A will become A=4.9*10<-4>cm<2>,
30 micrometer, then junction-capacitance Cj of a pn junction are set to Cj=0.17pF by the depletion-layer width W,
Therefore
It will become fc(CR)=1/(2(pi)CjR)=18GHz when the external resistance R shall be 50 omega|ohm.

[0006] On the other hand, it will become fc(ttr)=0.44/ttr when the frequency from which the amplitude of a photoelectric current becomes 1/2<1/2> of the amplitude of a low-frequency area|region, and electric power becomes 1/2 (-3 dB) is defined as cut-off-frequency f(ttr),
However,
Since saturated-drift-velocity (nu)ds of the electron which carries out the drift of during Si crystal| crystallization is (nu)ds=1*10<7>cm/sec, transit-time ttr of the electron which carries out the drift of the inside of a depletion layer becomes ttr=W/(nu)ds=0.3nsec,
Cut-off-frequency fc(ttr) becomes fc(ttr)=1.5GHz.
As mentioned above, the diameter of a light reception about 250 micrometer and the pin photodiode of Si whose depletion-layer width W is 30 micrometer
Since cut-off-frequency fc (CR) decided from CR time constant was 18GHz, in this pin photodiode, above-mentioned transit-time ttr will limit a cut off frequency,
It understand|indicate|reveals that the 1.5GHz vicinity is a limit of an operating frequency.

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[0007] Here, in order to achieve improvement in the speed of the response speed of a pin photodiode, it is necessary to enlarge a cut off frequency,
Therefore
The drift velocity in a semiconductor crystal should just use compound-semiconductor material, Ge, etc. which are a quick semiconductor crystal material compared with Si,
However,
Like a silicon-semiconductor process, it is not excellent in mass-production property, and since the diameter of a wafer is also small, a lowering of cost is difficult.

[0008] On the other hand, let the photoelectric-conversion part which has a pin photodiode structure of Si be a basic composition in recent years,
Quantum efficiency can be improved though thickness reduction of i layer which is a drift area| region in which a career|carrier carries out a drift in a photoelectric-conversion part is achieved,
The near-infrared-light sensing element which can achieve improvement in the speed by shortening of transit-time ttr of the career|carrier which furthermore carries out the drift of the inside of i layer is proposed (a nonpatent literature 1, 2).

[0009] This kind of near-infrared-light sensing element as shown in FIG. 4
DBR(Distributed Bragg Reflector)152 which consists of laminated film of the 1st SiO2 layer 152a, the Si layer 152b, and the 2nd SiO2 layer 152c, and reflects near infrared light on the 1 surface of the Si board|substrate 151 is provided.
The photoelectric-conversion part 160 which consists of a pin photodiode structure of Si which the i layer 162 interposes between the n<+> area|region 163 and the p<+> area|region 161 is provided on DBR152,
A surface with the light-receiving surface which consists of a surface of air and the p<+> area| region 161 forms the reflective surface which faces DBR152 (each other) on both sides of the photoelectric-conversion part 160 in the thickness direction (vertical direction) of the Si board| substrate 151,
The vertical resonator which consists of Fabry Perot type resonator (Fabry-Perot Resonator) by said reflective surface and DBR152 is formed.
Therefore, even if it makes thickness of the i layer 162 in the photoelectric-conversion part 160 small (it is small about the width of the i layer 162 in other words), a light-reception sensitivity can

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be improved, and the distance of a career|carrier can also be shortened by making thickness of the i layer 162 thin,
Therefore
Improvement in the speed of a response speed can be achieved.
In addition, the p<+> area|region 161 is electrically connected with the p electrode 165 by 1 said surface side of the Si board|substrate 151, and the n<+> area|region 163 is electrically connected with the n electrode 163 by 1 said surface side of the Si board|substrate 151.
M.K. Emsley, et al, Silicon Resonant Cavity Enhanced Photodetector Arrays for Optical Interconnects, Proc. of SPIE Vol.5246,p409-421,2003
M.K. Emsley, et al, Silicon Substrates With Buried Distributed Bragg Reflectors for Resonant Cavity-Enhanced Optoelectronics, IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS,VOL.8,NO.4,p948-955,JULY/AUGUST 2002

DISCLOSURE OF THE INVENTION

PROBLEM TO BE SOLVED BY THE INVENTION

[0010] However,
In order to manufacture the near-infrared-light sensing element of the structure shown in FIG. 4, it is necessary to repeat twice basic process (Hydrogen-ion injection|grouting work is a bonding process, a peeling|exfoliation process, and a surface grinding|polishing process.) required of the hydrogen injection|pouring peel|exfoliating method known as one of the formation methods of an SOI wafer before formation of the photoelectric-conversion part 160,
The manufacture process was complicated and cost reduction was difficult.
Moreover, the manufacturing method of the above-mentioned infrared-light sensing element cannot be applied when employ|adopting semiconductor crystal materials other than Si as a material of the photoelectric-conversion part 160.

[0011] This invention was comprised in view of said reason,
The objective is to be able to achieve improvement in the speed of a response speed, and for manufacture to provide an easy near-infrared-light sensing element.

MEANS TO SOLVE THE PROBLEM

[0012] The photoelectric-conversion part which has a photodiode structure where invention of Claim 1 was formed in 1 surface side of a semiconductor substrate, and the drift area|region was provided

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between p form area|region and n form area|region, absorbs near infrared light, and an electronic * hole pair generate|occur|produces,
With respect to the wavelength range of the near infrared light of the detection target which injects from the direction which is a slab type|mold photonic crystal which is laminated|stacked on the light-receiving surface of a photoelectric-conversion part, or is formed in said light-receiving-surface side in the inside of a photoelectric-conversion part, and has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and intersects said light-receiving surface
The slab type|mold photonic crystal by which the refractive-index period structure was designed have a resonance peak is comprised,
It is characterized by the above-mentioned.

[0013] According to this invention
To 1 surface side of a semiconductor substrate
To the light-receiving surface of the formed photoelectric-conversion part
With respect to the wavelength range of the near infrared light of the detection target which injects from the direction which is a slab type|mold photonic crystal which is laminated|stacked, or is formed in said light-receiving-surface side in the inside of a photoelectric-conversion part, and has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and intersects said light-receiving surface
By providing the slab type|mold photonic crystal by which the refractive-index period structure was designed have a resonance peak
Quantum efficiency can be raised even if it makes thin the thickness of the drift area|region of the photoelectric-conversion part of photodiode structures, such as a pin photodiode and an avalanche photo-diode, without providing a conventional vertical resonator,
Therefore
Can achieve improvement in the speed of a response speed, without making a light-reception sensitivity reduce, and again
The slab type|mold photonic crystal which was laminated|stacked on the photoelectric-conversion part or was formed in said light-receiving-surface side in the inside of a photoelectric-conversion part can be formed using the thin film coating technology, lithography technology, and etching technique which are general semiconductor manufacture process techniques,
Therefore
It can manufacture easily.

[0014] The near-infrared-light reflection part which invention of Claim 2 surrounds said photoelectric-conversion part in 1 said surface side of said semiconductor substrate in invention of Claim 1 by

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two dimensional surface inside parallel to said light-receiving surface, and reflects the near infrared light of said wavelength range in said photoelectric-conversion part side is comprised,
It is characterized by the above-mentioned.

[0015] By providing the near-infrared-light reflection part which surrounds said photoelectric-conversion part by two dimensional surface inside parallel to said light-receiving surface, and reflects the near infrared light of said wavelength range in said photoelectric-conversion part side according to this invention
It can prevent that the near infrared light of said wavelength range that injected on said photoelectric-conversion part through said light-receiving surface leaks to the side of said photoelectric-conversion part,
Therefore
Quantum efficiency can be raised more and a light-reception sensitivity can be raised further.

[0016] In invention of Claim 2, invention of Claim 3 said near-infrared-light reflection part
It is a two dimensional photonic crystal which has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and consists of a two dimensional photonic crystal by which the refractive-index period structure was designed reflect the near infrared light of said wavelength range in said photoelectric-conversion part side,
It is characterized by the above-mentioned.

[0017] According to this invention, said near-infrared-light reflection part can be easily formed using the lithography technology and etching technique which are general semiconductor manufacture process techniques.

[0018] In invention of Claim 1 thru|or Claim 3, the shape of invention of Claim 4 of said p form area|region in two dimensional surface inside with said photoelectric-conversion part parallel to said light-receiving surface and each said n form area|region is comb-shaped,
Said p form area|region and said n form area|region are mutually complex,
The said drift area|region consists of an i layer interposed between said p form area|region and said n form area|region,
It is characterized by the above-mentioned.

[0019] According to this invention
The thickness (width of i layer) of said drift area|region that consists of an i layer which interposes the mask at the time of forming said p form area|region with a spreading|diffusion or an ion implantation and said n form area|region between said p form area|region and said n form area|

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region with relative position accuracy with the mask at the time of forming with a spreading| diffusion or an ion implantation is decided,
Therefore
The precision of the thickness dimension of said drift area|region can be raised.

[0020] ADVANTAGE OF THE INVENTION
Invention of Claim 1 can achieve improvement in the speed of a response speed, and is effective in the ability to manufacture easily.

PREFERRED EMBODIMENT OF THE INVENTION

[0021] (Embodiment 1)
As shown to FIG. 1 (a), (b), the near-infrared-rays sensing element of this embodiment
While the semiconductor layer 3 which consists of a single-crystal Si layer of low concentration (For example, 10<13>-10<16>cm<-3> extent) via the 1st dielectric layer 2 which consists of a SiO2 film|membrane on the 1 surface of the semiconductor substrate 1 which consists of a Si board| substrate is provided
The 2nd dielectric layer 4 which consists of a SiO2 film|membrane is provided on said semiconductor layer 3,
The photoelectric-conversion part 6 which has a photodiode structure of a pin photodiode, absorbs near infrared light, and an electronic * hole pair generate|occur|produces is formed in the center section of the semiconductor layer 3.
In the center section of the 2nd dielectric layer 4, the light-receiving surface of the photoelectric-conversion part 6
With respect to the wavelength range of the near infrared light of the detection target by which injection|incidence (In this embodiment, it injected from the reverse side with the semiconductor substrate 1 side.) is carried out from the direction which is a slab type|mold photonic crystal which has a refractive-index period structure in two dimensional surface inside parallel to (the upper surface in FIG.1(b)), and intersects said light-receiving surface
The slab type|mold photonic crystal 7 by which the refractive-index period structure was designed have a resonance peak is formed.
In addition, in this embodiment, the material of the 1st dielectric layer 2 and the 2nd dielectric layer 4 is SiO2,
The semiconductor crystal material of the photoelectric-conversion part 6 is Si,
Therefore
The refractive index of the semiconductor layer 3 becomes a high value rather than each refractive index of the 1st dielectric layer 2 and the 2nd dielectric layer 4, and in (The refractive index of

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about 1.5 and Si of the refractive index of SiO2 is about 3.4.) and the photoelectric-conversion part 6
The waveguide mode which confines the near infrared light which injected from the light-receiving surface in the photoelectric-conversion part 6 according to a refractive-index difference with the medium of the both sides of the photoelectric-conversion part 6, and waveguides it exists,
Quantum efficiency can be raised.

[**0022**] In here, the near-infrared-light sensing element of this embodiment is used as a light receiving element of an optical communication,
A 0.8-micrometer belt|band|zone is assumed as a wavelength range of the near infrared light (input-signal light) of a detection target,
Si is employ|adopted as a semiconductor crystal material of the photoelectric-conversion part 6,
Si board|substrate is used as a semiconductor substrate 1.

[**0023**] The photoelectric-conversion part 6 is with the p form area|region 61 where the shape in two dimensional surface inside parallel to said light-receiving surface consists of a comb-shaped p<+> layer, as shown to FIG.1(b) and (c),
The n form area|region 63 where the shape in two dimensional surface inside parallel to said light-receiving surface consists of a comb-shaped n<+> layer is mutually complex,
In the shape in surface inside parallel to said light-receiving surface, the i layer 62 of an undulation state (the shape of a winding path) is interposing between the p form area|region 61 and the n form area|region 63.
In here, the comb-tooth parts 61b and 63b of multiple (the example of illustration three) which it was equally spaced and were spaced apart are continuously formed in the left-right direction of FIG.1(c) at each of comb bone 61a, 63a with circular arc-shaped p form area|region 61 and n form area|region 63,
In the left-right direction of FIG.1(c), the comb-tooth part 61b of the p form area|region 61 and the comb-tooth part 63b of the n form area|region 63 are alternately located in a line.
In addition, the shape in two dimensional surface inside with the photoelectric-conversion part 6 parallel to said light-receiving surface is formed in circular as a whole.
Moreover, in this embodiment, the i layer 62 is comprising the drift area|region provided between the p form area|region 61 and the n form area|region 63.

[0024] Moreover, the contact hole is formed in the region to which the near-infrared-light sensing element of this embodiment overlaps with the p form area|region 61 in the 2nd dielectric layer 4,
The contact electrode 8a which consists of a metal material which was embedded at said contact hole and was electrically connected with the p form area|region 61 is electrically connected via Pad 10a and the metal wiring 9a which were formed on the 2nd dielectric layer 4.
Similarly, the contact hole is formed in the region which overlaps with the n form area|region 63 in the 2nd dielectric layer 4,
The contact electrode 8b which consists of a metal material which was embedded at said contact hole and was electrically connected with the n form area|region 63 is electrically connected via Pad 10b and the metal wiring 9b which were formed on the 2nd dielectric layer 4.

[0025] Moreover, the slab type|mold photonic crystal 7 is arranged so that it may have a 2-dimensional period structure by surface inside (Two dimensional surface inside parallel to the light-receiving surface of the photoelectric-conversion part 6 in other words) which many holes 72 orthogonally cross in the thickness direction of slab 71 which consists of a region currently laminated|stacked on the photoelectric-conversion part 6 among the 2nd dielectric layers 4,
The slab type|mold photonic crystal 7 which has said refractive-index period structure by the low-refractive-index medium which consists of air in the high refractive index medium which comprises slab 71, and hole 72 is comprised.
When a unit cell specifically forms hole 72 in each location corresponding to each lattice point of the hypothetical|virtual two dimensional triangular grating|lattice of an equilateral triangle in slab 71, the slab type|mold photonic crystal 7 is formed.
If it paraphrases, hole 72 is arranged by triangular grating|lattice shape in surface inside orthogonally crossed in the thickness direction of slab 71.
In addition, the refractive index of about 1.5 and air of the refractive index of SiO2 which is the material of the 2nd dielectric layer 4 is 1.

[0026] The said refractive-index period structure is designed in design of the slab type|mold photonic crystal 7 have a resonance peak in the wavelength range of the near infrared light of a detection target as mentioned above.
Specifically, a, then Period a should just set period (It is a period of the refractive-index period structure of the slab type|mold photonic crystal 7, and is the distance during the lattice point of a two dimensional triangular grating|lattice.) of the sequence direction of hole 72 in the slab type|

mold photonic crystal 7 to the half-wave-length extent (For example, 1/2 of the wavelength of an infrared-light) of the infrared-light of said wavelength range, for example.
In addition, about the optical propagation part which is the principal part comprised in the slab type|mold photonic crystal 7 and the photoelectric-conversion part 6 among the near-infrared-light sensing elements of this embodiment
The semiconductor substrate 1 and a reverse side have a refractive-index difference with the air (refractive-index =1) which is a medium of slab type|mold photonic-crystal 7 and slab type|mold photonic-crystal 7 just overhead,
The semiconductor substrate 1 side has the 1st dielectric layer (refractive-index =1.5) 2 and 1st refractive-index difference which are the mediums of photoelectric-conversion part 6 directly under.
When there exist the medium and the above refractive-index differences which said optical propagation part is touching by each of up-and-down both sides (both sides of the thickness direction of the semiconductor substrate 1) in such an optical propagation part
There exist waveguide mode in which the near infrared light which propagates an optical propagation part satisfy|fills the total-reflection conditions of a up-down direction, and is completely

confined in an optical propagation part, and a mode (It calls in-plane resonance mode hereafter) which does not satisfy|fill total-reflection conditions but can be couple|bonded with ambient light.
When near infrared light is injected on such an optical propagation part from the exterior, one part near infrared light will couple|bond with in-plane resonance mode,
Any of in-plane resonance mode and waveguide mode, may not couple|bond another one part and it may be permeate|transmitted.
However,
As negate / after couple|bonding with in-plane resonance mode / the near infrared light re-radiated and the near infrared light to permeate|transmit
In this case, all the near infrared light which injected on the optical propagation part couple|bonds with in-plane resonance mode.
Thus, the light couple|bonded with in-plane resonance mode propagates the inside of an optical propagation part according to Q value of a resonance peak,
Therefore
Without providing a vertical resonator like the conventional structure of FIG. 4, in the thickness of the i layer 62 in the photoelectric-conversion part 6, even if thin, near infrared light is efficiently absorbed in the i layer 62.
Moreover, in this embodiment, all the near infrared light of said wavelength range that injects on an optical propagation part couple|bonds with in-plane resonance mode,
Therefore
It is not necessary to provide a reflection layer like DBR at a reverse side separately with the light-receiving surface in the photoelectric-conversion part 6.
In addition, in-plane resonance mode is reported as guided resonances in publication 1 (Shanhui Fan, et al, Analysis of guided resonances in photonic crystal slabs, PHYSICAL REVIEW B, VOLUME 65, 235112).

[0027] By the way, the near-infrared-light sensing element of this embodiment is formed in the middle of the thickness direction what is called using SOI(Silicon On Insulator) board|substrate which has a SiO2 film|membrane,
Si board|substrate of the back side in an SOI board|substrate comprises the semiconductor substrate 1,
The SiO2 film|membrane of an SOI board|substrate comprises the 1st dielectric layer 2,
Si layer of the main surface side of an SOI board|substrate is comprising the semiconductor layer 3.
That is, the photoelectric-conversion part 6 in a near-infrared-light sensing element is formed by introduce|transducing an impurity to the region corresponding to the each of the p form area| region 61 and the n form area|region 63 with a spreading|diffusion or an ion implantation in the

semiconductor layer 3 which consists of a Si layer of the main surface side of an SOI board| substrate,
Therefore
With relative position accuracy with the mask at the time of forming the mask at the time of forming the p form area|region 61 with a spreading|diffusion or an ion implantation, and the n form area| region 63 with a spreading|diffusion or an ion implantation
The thickness (It is the width of the i layer 62,
Comprising:
The distance of a career|carrier) of the i layer 62 which consists of a region interposed between the p form area|region 61 and the n form area|region 63 among the semiconductor layers 3 is decided,
Therefore
The precision of the thickness dimension of the i layer 62 can be raised.

[**0028**] Moreover, after the slab type|mold photonic crystal 7 forms the photoelectric-conversion part 6 in the semiconductor layer 3 which consists of a Si layer of the main surface side of an SOI board| substrate
After forming the 2nd dielectric layer 4 into a film with thin-film formation methods, such as CVD method, to the whole surface of the main surface side of an SOI board|substrate, the resist layer by which the region corresponding to each hole 72 was pierced using the lithography technology is formed on the 2nd dielectric layer 4,
It can form by etching the region corresponding to each hole 72 by the dry etching apparatus among the 2nd dielectric layers 4 by setting said resist layer as a mask.
In addition, not only SiO2 but Si3N4 may be sufficient as the medium which comprises slab 71, for example.

[**0029**] The near-infrared-light sensing element of this embodiment demonstrated above
The slab type|mold photonic crystal 7 by which the refractive-index period structure of two dimensional surface inside parallel to said light-receiving surface was designed have a resonance peak with respect to the wavelength range of the near infrared light of the detection target which is

laminated|stacked on the light-receiving surface of the photoelectric-conversion part 6, and injects from a reverse side with the photoelectric-conversion part 6 side is provided,
Therefore
Quantum efficiency can be raised even if it makes thin thickness (width) of the i layer 62 of the photoelectric-conversion part 6 of the photodiode structure of a pin photodiode, without providing a vertical resonator like a structure before shown in FIG. 4,
Therefore
Improvement in the speed of a response speed can be achieved without making a light-reception sensitivity reduce.
Moreover, the slab type|mold photonic crystal 7 laminated|stacked on the photoelectric-conversion part 6 can be formed using the thin film coating technology, lithography technology, and etching technique which are general semiconductor manufacture process techniques,
Therefore
It can manufacture easily.

[0030] (Embodiment 2)
The basic composition of the near-infrared-light sensing element of this embodiment is substantially the same as Embodiment 1,
Comprising:
The point currently formed as shown in FIG. 2 in the form where the p form area|region 61 and the i layer 62 in the photoelectric-conversion part 6, and the n form area|region 63 are located in a line with the thickness direction of the semiconductor substrate 1 is different.
In addition, the same code is attached to the same component as Embodiment 1, and description is abbreviate|omitted.

[0031] The p form area|region 61 and the n form area|region 63 of the photoelectric-conversion part 6 in this embodiment are formed in the shape where the shape in two dimensional surface inside parallel to said light-receiving surface notched partial circle as shown in FIG.2(c), (d),
The region interposed between the p form area|region 61 and the n form area|region 63 among the semiconductor layers 3 is comprising the i layer 62.
In addition, the p form area|region 61 and the n form area|region 63 are formed by introduce|transducing an impurity to the region corresponding to the each of the p form area|region 61 and the n form area|region 63 with a spreading|diffusion or an ion implantation in the semiconductor layer 3.

[0032] Moreover, the p form area|region 61 and the n form area|region 63 space apart the near-infrared-light sensing element of this embodiment in the thickness direction of the semiconductor substrate 1, and it is formed,
The n form area|region 63 is formed in the position distant from the 2nd dielectric layer 4,
Therefore
The spreading|diffusion wiring 63c (refer FIG.2(c)) for connecting electrically the n form area|region 63 and the contact electrode 8b is formed in the semiconductor layer 3.
In addition, each contact electrode 8a, 8b are formed in the region which overlaps with each circumference of the p form area|region 61 and the n form area|region 63 in the 2nd dielectric layer 4.

[0033] Thus, without making a light-reception sensitivity reduce, improvement in the speed of a response speed can be achieved, and the near-infrared-light sensing element of this embodiment as well as Embodiment 1 can be manufactured easily.

[0034] (Embodiment 3)
The basic composition of the near-infrared-light sensing element of this embodiment is substantially the same as Embodiment 1,
Comprising:
A point provided with the near-infrared-light reflection part 11 which surrounds the photoelectric-conversion part 6 in 1 said surface side of the semiconductor substrate 1 by two dimensional surface inside parallel to the light-receiving surface of the photoelectric-conversion part 6, and, as shown in FIG. 3, reflects the near infrared light of the wavelength range of a detection target in the photoelectric-conversion part 6 side is different.
In addition, the same code is attached to the same component as Embodiment 1, and description is abbreviate|omitted.

[0035] By the way, the near-infrared-light reflection part 11 in this embodiment is a two dimensional photonic crystal which has a refractive-index period structure in two dimensional surface inside with the near-infrared-light reflection part 11 parallel to said light-receiving surface,
It arranges so that it may have a 2-dimensional period structure by two dimensional surface inside which many holes 11a orthogonally cross in the thickness direction of slab 11b which consists of some semiconductor layers 3,
The two dimensional photonic crystal which has said refractive-index period structure by the low-refractive-index medium which consists of air in the high refractive index medium (here Si) which comprises Slab 11b, and Hole 11a is comprised.
Specifically, when a unit cell forms Hole 11a in Slab 11b at each lattice point of the hypothetical| virtual two dimensional triangular grating|lattice of an equilateral triangle, the two dimensional photonic crystal 11 is formed.
If it paraphrases, Hole 11a is arranged by triangular grating|lattice shape in surface inside orthogonally crossed in the thickness direction of Slab 11b.

[0036] The said refractive-index period structure is designed reflect the near infrared light of the wavelength range of a detection target in the photoelectric-conversion part 6 side as mentioned above in design of the two dimensional photonic crystal 11 in here.
Specifically, b, then Period b should just set period (It is a period of the refractive-index period structure of the two dimensional photonic crystal 11, and is the distance during the lattice point of a two dimensional triangular grating|lattice.) of the sequence direction of hole 11a in the two dimensional photonic crystal 11 to the half-wave-length extent (For example, 1/2 of the wavelength of an infrared-light) of the infrared-light of said wavelength range, for example.

[0037] Thus, in the near-infrared-light sensing element of this embodiment, it can prevent that the near infrared light of said wavelength range that injected on the photoelectric-conversion part 6 through said light-receiving surface leaks to the side of the photoelectric-conversion part 6 by providing the above-mentioned near-infrared-light reflection part 11,
Therefore
Quantum efficiency can be raised more and a light-reception sensitivity can be raised further.
Moreover, it comprises the two dimensional photonic crystal by which the refractive-index period structure was designed so that the near-infrared-light reflection part 11 might be a two dimensional photonic crystal which has a refractive-index period structure in two dimensional surface inside

parallel to said light-receiving surface and might reflect the near infrared light of said wavelength range in the photoelectric-conversion part 6 side,
Therefore
The near-infrared-light reflection part 11 can be easily formed using the lithography technology and etching technique which are general semiconductor manufacture process techniques.
In addition, in this embodiment, the two dimensional photonic crystal 11 is comprised according to the period structure of two kinds of mediums of Si and air,
However,
It is substantial with the dielectric material (For example, SiO2 etc.) into which a refractive index differs Hole 11a from Si, and it is sufficient to make it form the two dimensional photonic crystal 11 by said dielectric material and Si.
By the way, in each said Embodiment, Si is employ|adopted as a semiconductor crystal material of the photoelectric-conversion part 6,
Si board|substrate is used as a semiconductor substrate 1,
However,
Not only Si but Ge and compound-semiconductor crystal|crystallization material may be sufficient as the semiconductor crystal material of the photoelectric-conversion part 6, for example,
Not only Si board|substrate but Ge board|substrate, a GaAs board|substrate, etc. may be sufficient as the semiconductor substrate 1, for example.
Moreover, in each said Embodiment, the slab type|mold photonic crystal 7 was comprised according to the period structure of two kinds of mediums of SiO2 and air,
However,
It is substantial with the dielectric material into which a refractive index differs the inside of hole 72 from SiO2, and it is sufficient to make it form the slab type|mold photonic crystal 7 by said dielectric material and SiO2.
Or it is good also as a period structure of the medium of 3 or more type,
For example
By forming Si3N4 film|membrane which coat|covers the internal peripheral surface of hole 72 provided at slab 71 which consists of SiO2
It is sufficient to make it comprise the slab type|mold photonic crystal 7 by three kinds such as SiO2, Si3N4, and air.

[0038] Moreover, in each said Embodiment, the slab type|mold photonic crystal 7 is laminated|stacked on the light-receiving surface of the photoelectric-conversion part 6,
However,
Instead of laminating|stacking the slab type|mold photonic crystal 7 on the photoelectric-conversion part 6, it is sufficient to make it form in the light-receiving-surface side in the inside of the photoelectric-conversion part 6.
Moreover, in each said Embodiment, the photoelectric-conversion part 6 has a photodiode structure of a pin photodiode where i layer was provided as a drift area|region 62 between the p form area|region 61 and the n form area|region 63,
However,
As long as the drift area|region is provided between the p form area|region 61 and the n form area|region 63, the photodiode structure of an avalanche photo-diode may be sufficient as the photoelectric-conversion part 6.

[0039] Moreover, to slab 71, the slab type|mold photonic crystal 7 in each said Embodiment is formed, when a unit cell forms hole 72 in each location corresponding to each lattice point of the hypothetical|virtual two dimensional triangular grating|lattice of an equilateral triangle,
However,
Not only an equilateral triangle but a square may be sufficient as a unit cell, for example,
In this case, a unit cell should just form hole 72 in the region corresponding to each lattice point of a square hypothetical|virtual two dimensional tetragonal lattice.
Moreover, in each said Embodiment, in order to form the refractive-index period structure of the slab type|mold photonic crystal 7, many holes 72 are formed in slab 71,
However,
Instead of providing hole 72, it is sufficient to provide holes of another aperture|opening shape, such as a triangular-shaped hole and a rectangular hole, for example.

BRIEF DESCRIPTION OF THE DRAWINGS

[0040]

FIG. 1: Embodiment 1 is shown,
(a) is a schematic plan view,
(b) is the schematic perspective view fractured by A-A' of (a),
(c) is a horizontal sectional view.

FIG. 2: Embodiment 2 is shown,
(a) is a schematic plan view,
(b) is the schematic perspective view fractured by A-A' of (a),
(c) is a horizontal sectional view,
(d) is an another horizontal sectional view.

FIG. 3: Embodiment 3 is shown,
(a) is a schematic plan view,
(b) is the schematic perspective view fractured by A-A' of (a),
(c) is a horizontal sectional view.

FIG. 4: It is a schematic sectional drawing which shows a prior art example.

DESCRIPTION OF SYMBOLS

[**0041**] One semiconductor substrate
The dielectric layer of 2 1st
Three semiconductor layers
The dielectric layer of 4 2nd
Six photoelectric-conversion parts
Seven slab type|molds photonic crystal
8a,
8b contact electrode
9a,
9b metal wiring
10a,
10b pad
61 P form area|region
62 I layer
63 N form area|region
71 slabs
72 holes

1. 1. The photoelectric-conversion part which has a photodiode structure where formed in 1 surface side of a semiconductor substrate, and the drift area|region was provided between p form area|region and n form area|region, absorbs near infrared light, and an electronic * hole pair generate|occur|produces, With respect to the wavelength range of the near infrared light of the detection target which injects from the direction which is a slab type|mold photonic crystal which is laminated|stacked on the light-receiving

surface of a photoelectric-conversion part, or is formed in said light-receiving-surface side in the inside of a photoelectric-conversion part, and has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and intersects said light-receiving surface
The slab type|mold photonic crystal by which the refractive-index period structure was designed have a resonance peak is comprised,
The near-infrared-light sensing element characterized by the above-mentioned.

2. 2. The near-infrared-light reflection part which surrounds said photoelectric-conversion part in 1 said surface side of said semiconductor substrate by two dimensional surface inside parallel to said light-receiving surface, and reflects the near infrared light of said wavelength range in said photoelectric-conversion part side is comprised,
The near-infrared-light sensing element of Claim 1 characterized by the above-mentioned.
3. 3. The said near-infrared-light reflection part is a two dimensional photonic crystal which has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and it consists of a two dimensional photonic crystal by which the refractive-index period structure was designed reflect the near infrared light of said wavelength range in said photoelectric-conversion part side,
The near-infrared-light sensing element of Claim 2 characterized by the above-mentioned.
4. 4. The said photoelectric-conversion part has a comb-shaped shape of said p form area|region in two dimensional surface inside parallel to said light-receiving surface, and each said n form area|region,
Said p form area|region and said n form area|region are mutually complex,
The said drift area|region consists of an i layer interposed between said p form area|region and said n form area|region,
The near-infrared-light sensing element in any one of Claim 1 thru|or Claim 3 characterized by the above-mentioned.

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(19)日本国特許庁(JP)　(12)公開特許公報(A)　(11)特許出願公開番号
特開2007-13065
(P2007-13065A)
(43)公開日　平成19年1月18日(2007.1.18)

(51)Int.Cl.		F I		テーマコード（参考）
H01L 31/10	(2006.01)	H01L 31/10	A	5F049

審査請求 未請求　請求項の数 4　ＯＬ　（全 10 頁）

(21)出願番号　特願2005-195567 (P2005-195567)
(22)出願日　平成17年7月4日 (2005.7.4)

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Ｆターム(参考)　5F049 MA04　MB03　NA03　NB01　PA20
QA03　SZ08

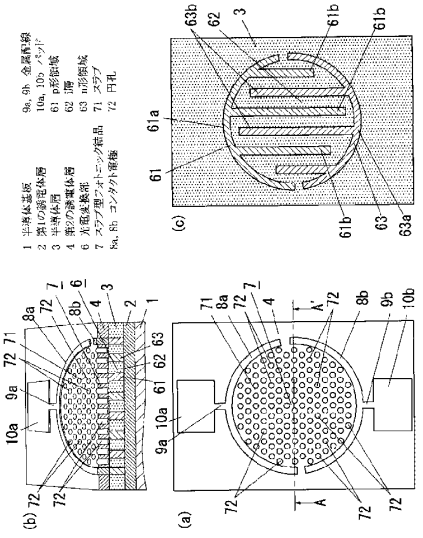
(54)【発明の名称】近赤外光検出素子

(57)【要約】

【課題】応答速度の高速化を図れ且つ製造が容易な近赤外光検出素子を提供する。

【解決手段】半導体基板１の一表面側に形成されｐ形領域６１とｎ形領域６３との間にドリフト領域であるｉ層６２が介在するｐｉｎフォトダイオードのフォトダイオード構造を有し近赤外光を吸収して電子・正孔対が発生する光電変換部６と、光電変換部６の受光面に積層され当該受光面に平行な２次元面内に屈折率周期構造を有するスラブ型フォトニック結晶であって上記受光面に交差する方向から入射される検出対象の近赤外光の波長帯に対して共振ピークを有するように屈折率周期構造が設計されたスラブ型フォトニック結晶７とを備えている。

【選択図】　図１



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【特許請求の範囲】
【請求項１】
半導体基板の一表面側に形成されｐ形領域とｎ形領域との間にドリフト領域が設けられたフォトダイオード構造を有し近赤外光を吸収して電子・正孔対が発生する光電変換部と、光電変換部の受光面に積層され若しくは光電変換部内における前記受光面側に形成され前記受光面に平行な２次元面内に屈折率周期構造を有するスラブ型フォトニック結晶であって前記受光面に交差する方向から入射される検出対象の近赤外光の波長帯に対して共振ピークを有するように屈折率周期構造が設計されたスラブ型フォトニック結晶とを備えてなることを特徴とする近赤外光検出素子。
【請求項２】
前記半導体基板の前記一表面側において前記受光面に平行な２次元面内で前記光電変換部を囲み前記波長帯の近赤外光を前記光電変換部側へ反射する近赤外光反射部を備えてなることを特徴とする請求項１記載の近赤外光検出素子。
【請求項３】
前記近赤外光反射部は、前記受光面に平行な２次元面内に屈折率周期構造を有する２次元フォトニック結晶であって前記波長帯の近赤外光を前記光電変換部側へ反射するように屈折率周期構造が設計された２次元フォトニック結晶からなることを特徴とする請求項２記載の近赤外光検出素子。
【請求項４】
前記光電変換部は、前記受光面に平行な２次元面内における前記ｐ形領域および前記ｎ形領域それぞれの形状が櫛形状であり、前記ｐ形領域と前記ｎ形領域とが互いに入り組んでおり、前記ドリフト領域が前記ｐ形領域と前記ｎ形領域との間に介在するｉ層からなることを特徴とする請求項１ないし請求項３のいずれかに記載の近赤外光検出素子。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、近赤外光を検出する近赤外光検出素子に関するものである。
【背景技術】
【０００２】
従来から、光通信では、光信号を受信するための受光素子として近赤外光検出素子が用いられている。この種の近赤外光検出素子としては、半導体結晶にｐｎ接合やショットキ接合を形成したフォトダイオード（ｐｎフォトダイオード、ｐｉｎフォトダイオード、アバランシェフォトダイオード、ショットキフォトダイオードなど）が広く用いられ、バンドギャップ以上の光子エネルギを有する光が入射された時に発生する電子－正孔対が分離されて空乏層内を走行（ドリフト）し外部回路に流れる電流が変化することを利用して、光信号を電流変化あるいは電圧変化として検出する。ここにおいて、近赤外光検出素子に用いられる半導体結晶材料としては、ＳｉやＧｅの他に、化合物半導体結晶材料（ＩｎＧａＡｓ、ＩｎＧａＡｓＰなど）があるが、光通信で用いられる光の波長帯、要求されている通信速度、価格などにより使い分けられている。
【０００３】
ところで、光通信は、都市間、都市内の通信網として既に広く使われているが、近年では、例えば高性能サーバとルータとをつなぐＳＡＮ（Storage Area Network）、いわゆる情報家電と周辺機器とをつなぐＤＶＩ（Digital Visual Interface）、車載ＬＡＮ（Local Area Network）、携帯電話機などの分野においても光通信を採用する動きが活発化している。このような分野でも高速の光通信が必要とされており、応用分野によって通信速度の高速化の進展は異なるが、いずれの分野においても１Gbps以上の通信速度を要求されることが予測されている。
【０００４】
上述のような各種分野で用いられる光通信用のフォトダイオードには今後、応答速度の高速化や低価格化が要求される。ここにおいて、フォトダイオードの応答速度は基本的に

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はフォトダイオードのＣＲ時定数と、空乏層内をドリフトするキャリア（電子、正孔）の走行時間ｔとの２つの要素で制限されることが知られている。半導体結晶材料としてＳｉを用いたｐｉｎフォトダイオードを例に考えると、ＣＲ時定数を小さくするとともに量子効率（受光感度）を高めるために、広い空乏層が形成されているので、空乏層内をドリフトする電子の走行時間ｔが高速応答時には無視できなくなる。

【０００５】

例えば、Ｓｉのｐｉｎフォトダイオードで量子効率を８０％以上とするためには、３０μｍ程度の空乏層幅Ｗが必要となるが、ＣＲ時定数で決まる遮断周波数$f_c(CR)$は、受光径を２５０μｍとすると、ｐｎ接合面積Ａが$A=4.9\times10^{-4}\ cm^2$となり、空乏層幅Ｗが３０μｍとすればｐｎ接合の接合容量C_jが$C_j=0.17\ pF$となるから、外部抵抗Ｒを５０Ωとすると、$f_c(CR)=1/(2\pi C_j R)=18\ GHz$となる。

【０００６】

一方、光電流の振幅が低周波領域の振幅の$1/2^{1/2}$、すなわち、電力が１／２（－３ｄＢ）になる周波数を遮断周波数$f(t_{tr})$と定義すると、$f_c(t_{tr})=0.44/t_{tr}$となるが、Ｓｉ結晶中をドリフトする電子の飽和ドリフト速度v_{ds}が$v_{ds}=1\times10^7\ cm/sec$であるため、空乏層内をドリフトする電子の走行時間$t_{tr}$が$t_{tr}=W/v_{ds}=0.3\ nsec$となり、遮断周波数$f_c(t_{tr})$は、$f_c(t_{tr})=1.5\ GHz$となる。上述のように、受光径が２５０μｍ、空乏層幅Ｗが３０μｍのＳｉのｐｉｎフォトダイオードについては、ＣＲ時定数から決まる遮断周波数$f_c(CR)$が１８ＧＨｚであったから、このｐｉｎフォトダイオードでは上述の走行時間t_{tr}が遮断周波数を制限することとなり、１．５ＧＨｚ近辺が動作周波数の限界であることが分かる。

【０００７】

ここで、ｐｉｎフォトダイオードの応答速度の高速化を図るには、遮断周波数を大きくする必要があるので、半導体結晶中のドリフト速度がＳｉに比べて速い半導体結晶材料である化合物半導体材料やＧｅなどを用いればよいが、シリコン半導体プロセスほどは量産性に優れておらず、また、ウェハ径も小さいので、低価格化が難しい。

【０００８】

これに対して、近年、Ｓｉのｐｉｎフォトダイオード構造を有する光電変換部を基本構成とし、光電変換部においてキャリアがドリフトするドリフト領域であるｉ層の薄型化を図りながらも量子効率を向上することができ、しかもｉ層中をドリフトするキャリアの走行時間t_{tr}の短縮による高速化を図れる近赤外光検出素子が提案されている（非特許文献１，２）。

【０００９】

この種の近赤外光検出素子は、図４に示すように、Ｓｉ基板１５１の一表面上に第１のSiO_2層１５２ａとＳｉ層１５２ｂと第２のSiO_2層１５２ｃとの積層膜からなり近赤外光を反射するＤＢＲ（Distributed Bragg Reflector）１５２が設けられ、ＤＢＲ１５２上にn^+領域１６３とp^+領域１６１との間にｉ層１６２が介在するＳｉのｐｉｎフォトダイオード構造からなる光電変換部１６０が設けらており、空気とp^+領域１６１の表面からなる受光面との界面がＳｉ基板１５１の厚み方向（縦方向）において光電変換部１６０を挟んでＤＢＲ１５２に対向する反射面を形成し、当該反射面とＤＢＲ１５２とでファブリペロー共振器（Fabry-Perot Resonator）からなる縦型の共振器を形成している。したがって、光電変換部１６０におけるｉ層１６２の厚みを小さく（つまり、ｉ層１６２の幅を小さく）しても受光感度を向上することができ、ｉ層１６２の厚みを薄くすることでキャリアの走行距離も短くできるので、応答速度の高速化を図ることができる。なお、p^+領域１６１はＳｉ基板１５１の上記一表面側でｐ電極１６５と電気的に接続され、n^+領域１６３はＳｉ基板１５１の上記一表面側でｎ電極１６３と電気的に接続されている。

【非特許文献１】M.K.Emsley,et al,「Silicon Resonant Cavity Enhanced Photodetector Arrays for Optical Interconnects」, Proc. of SPIE Vol.5246,p409-421,2003

【非特許文献２】M.K.Emsley,et al,「Silicon Substrates With Buried Distributed Br

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agg Reflectors for Resonant Cavity-Enhanced Optoelectronics」, IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS,VOL.8,NO.4,p948-955,JULY/AUGUST 2002

【発明の開示】

【発明が解決しようとする課題】

【００１０】

しかしながら、図４に示した構成の近赤外光検出素子を製造するには、光電変換部１６０の形成前に、ＳＯＩウェハの形成方法の１つとして知られている水素注入剥離法で必要な基本工程（水素イオン注入工程、貼り合わせ工程、剥離工程、表面研磨工程）を２回繰り返す必要があり、製造プロセスが複雑で低コスト化が難しかった。また、上述の赤外光検出素子の製造方法はＳｉ以外の半導体結晶材料を光電変換部１６０の材料として採用する場合には適用することができない。

【００１１】

本発明は上記事由に鑑みて為されたものであり、その目的は、応答速度の高速化を図れ且つ製造が容易な近赤外光検出素子を提供することにある。

【課題を解決するための手段】

【００１２】

請求項１の発明は、半導体基板の一表面側に形成されｐ形領域とｎ形領域との間にドリフト領域が設けられたフォトダイオード構造を有し近赤外光を吸収して電子・正孔対が発生する光電変換部と、光電変換部の受光面に積層され若しくは光電変換部内における前記受光面側に形成され前記受光面に平行な２次元面内に屈折率周期構造を有するスラブ型フォトニック結晶であって前記受光面に交差する方向から入射される検出対象の近赤外光の波長帯に対して共振ピークを有するように屈折率周期構造が設計されたスラブ型フォトニック結晶とを備えてなることを特徴とする。

【００１３】

この発明によれば、半導体基板の一表面側に形成された光電変換部の受光面に積層され若しくは光電変換部内における前記受光面側に形成され前記受光面に平行な２次元面内に屈折率周期構造を有するスラブ型フォトニック結晶であって前記受光面に交差する方向から入射される検出対象の近赤外光の波長帯に対して共振ピークを有するように屈折率周期構造が設計されたスラブ型フォトニック結晶を備えていることにより、従来のような縦型の共振器を設けることなくｐｉｎフォトダイオードやアバランシェフォトダイオードなどのフォトダイオード構造の光電変換部のドリフト領域の厚さを薄くしても量子効率を高めることができるので、受光感度を低下させることなく応答速度の高速化を図れ、また、光電変換部に積層され若しくは光電変換部内における前記受光面側に形成されたスラブ型フォトニック結晶は一般的な半導体製造プロセス技術である薄膜形成技術とリソグラフィ技術とエッチング技術とを利用して形成することができるので、容易に製造することができる。

【００１４】

請求項２の発明は、請求項１の発明において、前記半導体基板の前記一表面側において前記受光面に平行な２次元面内で前記光電変換部を囲み前記波長帯の近赤外光を前記光電変換部側へ反射する近赤外光反射部を備えてなることを特徴とする。

【００１５】

この発明によれば、前記受光面に平行な２次元面内で前記光電変換部を囲み前記波長帯の近赤外光を前記光電変換部側へ反射する近赤外光反射部を備えていることにより、前記受光面を通して前記光電変換部へ入射された前記波長帯の近赤外光が前記光電変換部の側方へ漏れるのを防止することができるので、量子効率をより高めることができ、受光感度をより一層高めることができる。

【００１６】

請求項３の発明は、請求項２の発明において、前記近赤外光反射部は、前記受光面に平行な２次元面内に屈折率周期構造を有する２次元フォトニック結晶であって前記波長帯の近赤外光を前記光電変換部側へ反射するように屈折率周期構造が設計された２次元フォト

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ニック結晶からなることを特徴とする。

【００１７】

この発明によれば、前記近赤外光反射部を一般的な半導体製造プロセス技術であるリソグラフィ技術とエッチング技術とを利用して容易に形成することができる。

【００１８】

請求項４の発明は、請求項１ないし請求項３の発明において、前記光電変換部は、前記受光面に平行な２次元面内における前記ｐ形領域および前記ｎ形領域それぞれの形状が櫛形状であり、前記ｐ形領域と前記ｎ形領域とが互いに入り組んでおり、前記ドリフト領域が前記ｐ形領域と前記ｎ形領域との間に介在するｉ層からなることを特徴とする。

【００１９】

この発明によれば、前記ｐ形領域を拡散もしくはイオン注入により形成する際のマスクと前記ｎ形領域を拡散もしくはイオン注入により形成する際のマスクとの相対的な位置精度により前記ｐ形領域と前記ｎ形領域との間に介在するｉ層からなる前記ドリフト領域の厚み（ｉ層の幅）が決まるので、前記ドリフト領域の厚み寸法の精度を高めることができる。

【発明の効果】

【００２０】

請求項１の発明は、応答速度の高速化を図れ且つ容易に製造することができるという効果がある。

【発明を実施するための最良の形態】

【００２１】

（実施形態１）

本実施形態の近赤外線検出素子は、図１（ａ），（ｂ）に示すように、Ｓｉ基板からなる半導体基板１の一表面上にSiO_2膜からなる第１の誘電体層２を介して低濃度（例えば、10^{13}～$10^{16}cm^{-3}$程度）の単結晶Ｓｉ層からなる半導体層３が設けられるとともに、当該半導体層３上にSiO_2膜からなる第２の誘電体層４が設けられており、半導体層３の中央部にｐｉｎフォトダイオードのフォトダイオード構造を有し近赤外光を吸収して電子・正孔対が発生する光電変換部６が形成され、第２の誘電体層４の中央部に光電変換部６の受光面（図１（ｂ）における上面）に平行な２次元面内に屈折率周期構造を有するスラブ型フォトニック結晶であって上記受光面に交差する方向から入射（本実施形態では、半導体基板１側とは反対側から入射）される検出対象の近赤外光の波長帯に対して共振ピークを有するように屈折率周期構造が設計されたスラブ型フォトニック結晶７が形成されている。なお、本実施形態では、第１の誘電体層２および第２の誘電体層４の材料がSiO_2であり、光電変換部６の半導体結晶材料がＳｉであるので、第１の誘電体層２および第２の誘電体層４それぞれの屈折率よりも半導体層３の屈折率が高い値となっており（SiO_2の屈折率は１．５程度、Ｓｉの屈折率は３．４程度である）、光電変換部６には、受光面から入射された近赤外光を光電変換部６の両側の媒質との屈折率差により光電変換部６内に閉じ込めて導波する導波モードが存在しており、量子効率を高めることができる。

【００２２】

ここにおいて、本実施形態の近赤外光検出素子は、光通信の受光素子として用いるものであり、検出対象の近赤外光（入力信号光）の波長帯として０．８μｍ帯を想定しており、光電変換部６の半導体結晶材料としてＳｉを採用し、半導体基板１としてＳｉ基板を用いている。

【００２３】

光電変換部６は、図１（ｂ），（ｃ）に示すように、上記受光面に平行な２次元面内における形状が櫛形状のp^+層からなるｐ形領域６１と、上記受光面に平行な２次元面内における形状が櫛形状のn^+層からなるｎ形領域６３とが、互いに入り組んでおり、ｐ形領域６１とｎ形領域６３との間に上記受光面に平行な面内における形状が蛇行状（つづら折れ状）のｉ層６２が介在している。ここにおいて、ｐ形領域６１およびｎ形領域６３は円

弧状の櫛骨部６１ａ，６３ａそれぞれに、図１（ｃ）の左右方向に等間隔で離間した複数（図示例では、３つ）の櫛歯部６１ｂ，６３ｂが連続して形成されており、図１（ｃ）の左右方向においてｐ形領域６１の櫛歯部６１ｂとｎ形領域６３の櫛歯部６３ｂとが交互に並んでいる。なお、光電変換部６は、上記受光面に平行な２次元面内における形状が、全体として円形状に形成されている。また、本実施形態では、ｉ層６２がｐ形領域６１とｎ形領域６３との間に設けられたドリフト領域を構成している。

【００２４】

また、本実施形態の近赤外光検出素子は、第２の誘電体層４においてｐ形領域６１に重なる部位にコンタクト孔が形成されており、当該コンタクト孔に埋め込まれｐ形領域６１と電気的に接続された金属材料からなるコンタクト電極８ａが、第２の誘電体層４上に形成されたパッド１０ａと金属配線９ａを介して電気的に接続されている。同様に、第２の誘電体層４においてｎ形領域６３に重なる部位にコンタクト孔が形成されており、当該コンタクト孔に埋め込まれｎ形領域６３と電気的に接続された金属材料からなるコンタクト電極８ｂが、第２の誘電体層４上に形成されたパッド１０ｂと金属配線９ｂを介して電気的に接続されている。

【００２５】

また、スラブ型フォトニック結晶７は、多数の円孔７２が、第２の誘電体層４のうち光電変換部６に積層されている部位からなるスラブ７１の厚み方向に直交する面内（つまり、光電変換部６の受光面に平行な２次元面内）で２次元的な周期構造を有するように配列されており、スラブ７１を構成する高屈折率媒質と円孔７２内の空気からなる低屈折率媒質とで上記屈折率周期構造を有するスラブ型フォトニック結晶７を構成している。具体的には、スラブ７１において、単位格子が正三角形の仮想的な２次元三角格子の各格子点に対応する各部位に円孔７２を形成することにより、スラブ型フォトニック結晶７を形成してある。言い換えれば、円孔７２はスラブ７１の厚み方向に直交する面内において三角格子状に配列されている。なお、第２の誘電体層４の材料であるSiO_2の屈折率は１．５程度、空気の屈折率は１である。

【００２６】

スラブ型フォトニック結晶７の設計にあたっては、上述のように検出対象の近赤外光の波長帯に共振ピークを有するように上記屈折率周期構造が設計されている。具体的には、例えば、スラブ型フォトニック結晶７における円孔７２の配列方向の周期（スラブ型フォトニック結晶７の屈折率周期構造の周期であって２次元三角格子の格子点間の距離）をａとすれば、周期ａは上記波長帯の赤外光の半波長程度（例えば、赤外光の波長の２分の１）に設定すればよい。なお、本実施形態の近赤外光検出素子のうちスラブ型フォトニック結晶７と光電変換部６とで構成された主要部である光伝搬部については、半導体基板１と反対側はスラブ型フォトニック結晶７とスラブ型フォトニック結晶７直上の媒質である空気（屈折率＝１）との屈折率差があり、半導体基板１側は光電変換部６直下の媒質である第１の誘電体層（屈折率＝１．５）２と屈折率差がある。このような光伝搬部では、当該光伝搬部が上下両側（半導体基板１の厚み方向の両側）それぞれで接している媒質と上述のような屈折率差があることにより、光伝搬部を伝搬する近赤外光が上下方向の全反射条件を満たして完全に光伝搬部内に閉じ込められる導波モードと、全反射条件を満たさず外部光と結合可能なモード（以下、面内共振モードと呼ぶ）とがある。このような光伝搬部に外部から近赤外光を入射すると、一部の近赤外光が面内共振モードに結合し、別の一部は面内共振モードおよび導波モードのいずれにも結合せず透過する場合もあるが、面内共振モードに結合した後に再放射される近赤外光と透過する近赤外光とが打ち消されるような場合も存在し、この場合には光伝搬部に入射された全ての近赤外光が面内共振モードに結合する。このように面内共振モードに結合した光は、共振ピークのＱ値に応じて光伝搬部内を伝搬していくことになるので、図４の従来構成のような縦型の共振器を設けることなく光電変換部６におけるｉ層６２の厚みを薄くてもｉ層６２にて近赤外光が効率良く吸収されることになる。また、本実施形態では、光伝搬部に入射される上記波長帯の近赤外光の全てが面内共振モードに結合するので、光電変換部６における受光面とは反対側にＤ

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ＢＲのような反射層を別途設ける必要もない。なお、面内共振モードは、刊行物１（Shanhui Fan,et al, 「Analysis of guided resonances in photonic crystal slabs」, PHYSICAL REVIEW B,VOLUME 65,235112）において「guided resonances」として報告されている。

【００２７】

ところで、本実施形態の近赤外光検出素子は、厚み方向の中間にSiO_2膜を有する所謂ＳＯＩ（Silicon On Insulator）基板を用いて形成してあり、ＳＯＩ基板における裏面側のＳｉ基板が半導体基板１を構成し、ＳＯＩ基板のSiO_2膜が第１の誘電体層２を構成し、ＳＯＩ基板の主表面側のＳｉ層が半導体層３を構成している。すなわち、近赤外光検出素子における光電変換部６は、ＳＯＩ基板の主表面側のＳｉ層からなる半導体層３においてｐ形領域６１およびｎ形領域６３それぞれに対応する部位に不純物を拡散もしくはイオン注入によって導入することにより形成されているので、ｐ形領域６１を拡散もしくはイオン注入により形成する際のマスクとｎ形領域６３を拡散もしくはイオン注入により形成する際のマスクとの相対的な位置精度により、半導体層３のうちｐ形領域６１とｎ形領域６３との間に介在する部位からなるｉ層６２の厚さ（ｉ層６２の幅であって、キャリアの走行距離）が決まるので、ｉ層６２の厚み寸法の精度を高めることができる。

【００２８】

また、スラブ型フォトニック結晶７は、ＳＯＩ基板の主表面側のＳｉ層からなる半導体層３に光電変換部６を形成した後で、ＳＯＩ基板の主表面側の全面に第２の誘電体層４を例えばＣＶＤ法などの薄膜形成方法により成膜してから、第２の誘電体層４上にリソグラフィ技術を利用して各円孔７２に対応する部位が開孔されたレジスト層を形成し、当該レジスト層をマスクとして第２の誘電体層４のうち各円孔７２に対応する部位をドライエッチング装置によりエッチングすることによって形成することができる。なお、スラブ７１を構成する媒質はSiO_2に限らず、例えば、Si_3N_4でもよい。

【００２９】

以上説明した本実施形態の近赤外光検出素子は、光電変換部６の受光面に積層され光電変換部６側とは反対側から入射される検出対象の近赤外光の波長帯に対して共振ピークを有するように上記受光面に平行な２次元面内の屈折率周期構造が設計されたスラブ型フォトニック結晶７を備えているので、図４に示した従来構成のような縦型の共振器を設けることなくｐｉｎフォトダイオードのフォトダイオード構造の光電変換部６のｉ層６２の厚み（幅）を薄くしても量子効率を高めることができるので、受光感度を低下させることなく応答速度の高速化を図れる。また、光電変換部６に積層されたスラブ型フォトニック結晶７は一般的な半導体製造プロセス技術である薄膜形成技術とリソグラフィ技術とエッチング技術とを利用して形成することができるので、容易に製造することができる。

【００３０】

（実施形態２）

本実施形態の近赤外光検出素子の基本構成は実施形態１と略同じであって、図２に示すように、光電変換部６におけるｐ形領域６１とｉ層６２とｎ形領域６３とが半導体基板１の厚み方向に並ぶ形で形成されている点が相違する。なお、実施形態１と同様の構成要素には同一の符号を付して説明を省略する。

【００３１】

本実施形態における光電変換部６のｐ形領域６１およびｎ形領域６３は、図２（ｃ），（ｄ）に示すように、上記受光面に平行な２次元面内における形状が円の一部を切り欠いた形状に形成されており、半導体層３のうちｐ形領域６１とｎ形領域６３との間に介在する部位がｉ層６２を構成している。なお、ｐ形領域６１およびｎ形領域６３は、半導体層３においてｐ形領域６１およびｎ形領域６３それぞれに対応する部位に不純物を拡散もしくはイオン注入によって導入することにより形成されている。

【００３２】

また、本実施形態の近赤外光検出素子は、ｐ形領域６１とｎ形領域６３とが半導体基板１の厚み方向に離間して形成されており、ｎ形領域６３が第２の誘電体層４から離れた位

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置に形成されているので、ｎ形領域６３とコンタクト電極８ｂとを電気的に接続するための拡散配線６３ｃ（図２（ｃ）参照）を半導体層３に形成してある。なお、各コンタクト電極８ａ，８ｂは、第２の誘電体層４において、ｐ形領域６１およびｎ形領域６３それぞれの周部に重なる部位に形成されている。

【００３３】

しかして、本実施形態の近赤外光検出素子も、実施形態１と同様に、受光感度を低下させることなく応答速度の高速化を図れ且つ容易に製造することができる。

【００３４】

（実施形態３）

本実施形態の近赤外光検出素子の基本構成は実施形態１と略同じであって、図３に示すように、半導体基板１の上記一表面側において光電変換部６の受光面に平行な２次元面内で光電変換部６を囲み検出対象の波長帯の近赤外光を光電変換部６側へ反射する近赤外光反射部１１を備えている点が相違する。なお、実施形態１と同様の構成要素には同一の符号を付して説明を省略する。

【００３５】

ところで、本実施形態における近赤外光反射部１１は、近赤外光反射部１１が上記受光面に平行な２次元面内に屈折率周期構造を有する２次元フォトニック結晶であり、多数の円孔１１ａが半導体層３の一部からなるスラブ１１ｂの厚み方向に直交する２次元面内で２次元的な周期構造を有するように配列されており、スラブ１１ｂを構成する高屈折率媒質（ここでは、Ｓｉ）と円孔１１ａ内の空気からなる低屈折率媒質とで上記屈折率周期構造を有する２次元フォトニック結晶を構成している。具体的には、スラブ１１ｂに、単位格子が正三角形の仮想的な２次元三角格子の各格子点に円孔１１ａを形成することにより、２次元フォトニック結晶１１を形成してある。言い換えれば、円孔１１ａはスラブ１１ｂの厚み方向に直交する面内において三角格子状に配列されている。

【００３６】

ここにおいて、２次元フォトニック結晶１１の設計にあたっては、上述のように検出対象の波長帯の近赤外光を光電変換部６側へ反射するように上記屈折率周期構造が設計されている。具体的には、例えば、２次元フォトニック結晶１１における円孔１１ａの配列方向の周期（２次元フォトニック結晶１１の屈折率周期構造の周期であって２次元三角格子の格子点間の距離）をｂとすれば、周期ｂは上記波長帯の赤外光の半波長程度（例えば、赤外光の波長の２分の１）に設定すればよい。

【００３７】

しかして、本実施形態の近赤外光検出素子では、上述の近赤外光反射部１１を備えていることにより、上記受光面を通して光電変換部６へ入射された上記波長帯の近赤外光が光電変換部６の側方へ漏れるのを防止することができるので、量子効率をより高めることができ、受光感度をより一層高めることができる。また、近赤外光反射部１１が上記受光面に平行な２次元面内に屈折率周期構造を有する２次元フォトニック結晶であって上記波長帯の近赤外光を光電変換部６側へ反射するように屈折率周期構造が設計された２次元フォトニック結晶により構成されているので、近赤外光反射部１１を一般的な半導体製造プロセス技術であるリソグラフィ技術とエッチング技術とを利用して容易に形成することができる。なお、本実施形態では、２次元フォトニック結晶１１をＳｉと空気との２種類の媒質の周期構造により構成しているが、円孔１１ａをＳｉとは屈折率の異なる誘電体材料（例えば、SiO_2など）により充実して当該誘電体材料とＳｉとで２次元フォトニック結晶１１を形成するようにしてもよい

ところで、上記各実施形態では、光電変換部６の半導体結晶材料としてＳｉを採用し、半導体基板１としてＳｉ基板を用いているが、光電変換部６の半導体結晶材料はＳｉに限らず、例えば、Ｇｅや化合物半導体結晶材料でもよく、半導体基板１もＳｉ基板に限らず、例えば、Ｇｅ基板やＧａＡｓ基板などでもよい。また、上記各実施形態では、スラブ型フォトニック結晶７をSiO_2と空気との２種類の媒質の周期構造により構成していたが、円孔７２内をSiO_2とは屈折率の異なる誘電体材料により充実して当該誘電体材料と

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SiO_2とでスラブ型フォトニック結晶７を形成するようにしてもよいし、あるいは３種類以上の媒質の周期構造としてもよく、例えば、SiO_2からなるスラブ７１に設けた円孔７２の内周面を被覆するSi_3N_4膜を形成することによってSiO_2とSi_3N_4と空気との３種類でスラブ型フォトニック結晶７を構成するようにしてもよい。

【００３８】

また、上記各実施形態では、スラブ型フォトニック結晶７を光電変換部６の受光面に積層してあるが、スラブ型フォトニック結晶７を光電変換部６に積層する代わりに、光電変換部６内における受光面側に形成するようにしてもよい。また、上記各実施形態では、光電変換部６がｐ形領域６１とｎ形領域６３との間にドリフト領域６２としてｉ層が設けられたｐｉｎフォトダイオードのフォトダイオード構造を有しているが、光電変換部６はｐ形領域６１とｎ形領域６３との間にドリフト領域が設けられていればアバランシェフォトダイオードのフォトダイオード構造でもよい。

【００３９】

また、上記各実施形態におけるスラブ型フォトニック結晶７は、スラブ７１に対して、単位格子が正三角形の仮想的な２次元三角格子の各格子点に対応する各部位に円孔７２を形成することにより形成されているが、単位格子は正三角形に限らず、例えば正方形でもよく、この場合には単位格子が正方形の仮想的な２次元正方格子の各格子点に対応する部位に円孔７２を形成すればよい。また、上記各実施形態では、スラブ型フォトニック結晶７の屈折率周期構造を形成するためにスラブ７１に多数の円孔７２を形成してあるが、円孔７２を設ける代わりに、例えば三角形状の孔や四角形状の孔など別の開口形状の孔を設けてもよい。

【図面の簡単な説明】

【００４０】

【図１】実施形態１を示し、（ａ）は概略平面図、（ｂ）は（ａ）のＡ－Ａ’で破断した概略斜視図、（ｃ）は水平断面図である。

【図２】実施形態２を示し、（ａ）は概略平面図、（ｂ）は（ａ）のＡ－Ａ’で破断した概略斜視図、（ｃ）は水平断面図、（ｄ）は他の水平断面図である。

【図３】実施形態３を示し、（ａ）は概略平面図、（ｂ）は（ａ）のＡ－Ａ’で破断した概略斜視図、（ｃ）は水平断面図である。

【図４】従来例を示す概略断面図である。

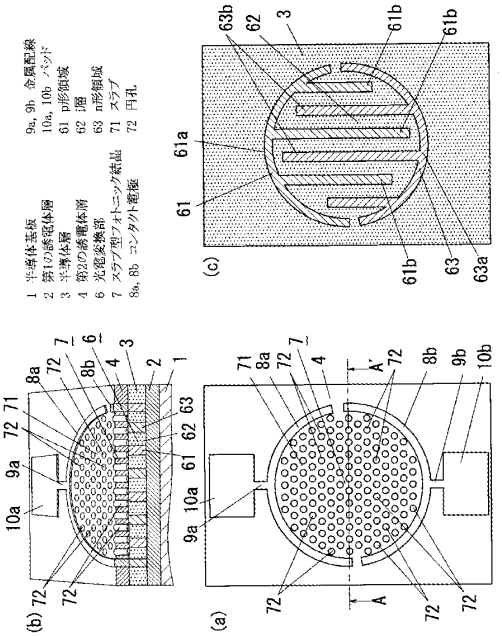
【符号の説明】

【００４１】

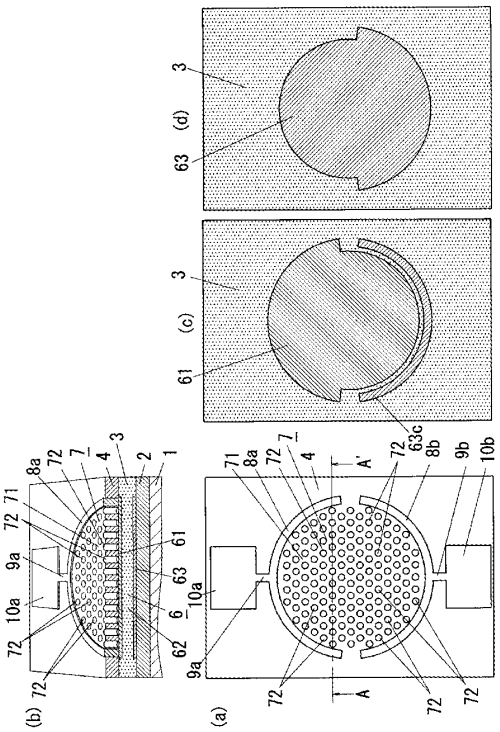
１　半導体基板
２　第１の誘電体層
３　半導体層
４　第２の誘電体層
６　光電変換部
７　スラブ型フォトニック結晶
８ａ，８ｂ　コンタクト電極
９ａ，９ｂ　金属配線
１０ａ，１０ｂ　パッド
６１　ｐ形領域
６２　ｉ層
６３　ｎ形領域
７１　スラブ
７２　円孔

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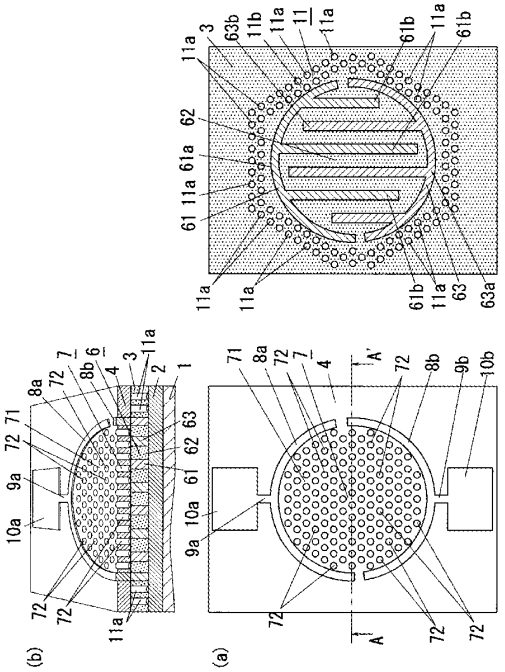
【図１】


1 半導体基板
2 第1の誘電体層
3 半導体層
4 第2の誘電体層
6 光電変換部
7 スタック型フォトニック結晶
8a, 8b コンタクト電極
9a, 9b 金属配線
10a, 10b バンド
61 p形領域
62 i層
63 n形領域
71 スタブ
72 円孔

【図２】



【図３】



【図４】

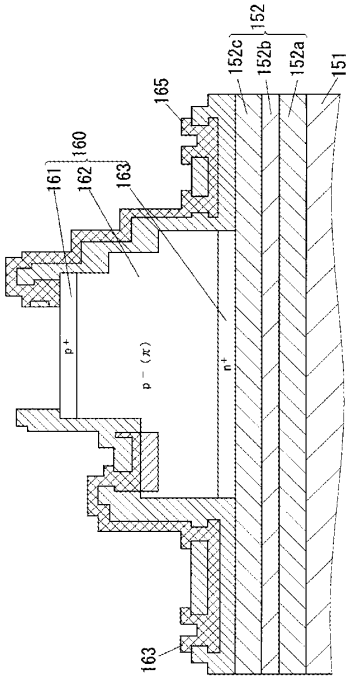
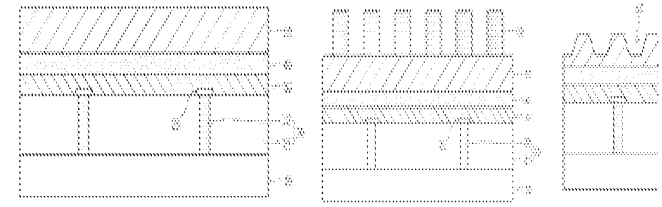

151
152
152a
152b
152c
160
161
162
163
165
p+
p− (π)
n+

Image sensor and method for manufacturing thereof

Abstract

An image sensor and a manufacturing method thereof are provided to improve condensing rate and simplify its process while adopting a vertical photodiode of which resolution and sensitivity are improved. A CMOS(Complementary Metal Oxide Silicon) circuit is formed at a semiconductor circuit, and a metallic wiring layer which includes a metal wire and an inter insulation film is formed at a semiconductor substrate. A first conductivity type conductive layer is formed at the metallic wiring layer, and an intrinsic layer is formed at the first conductivity type conductive layer. A second conductivity type conductive layer(51) is formed at the intrinsic layer is formed at the intrinsic layer. At one or more than one layer of those three layers, the first conductivity conductive layer, the intrinsic layer and the second conductivity conductive layer, a concavo-convex part is formed.

Images (14)



Classifications

H01L27/14607 Geometry of the photosensitive area

View 4 more classifications

KR20080101301A

South Korea

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Other languages: Korean

Inventor: 심종민

Worldwide applications

2007 KR

Application KR1020070047886A events

2007-05-17 Application filed by 주식회사 동부하이텍

2007-05-17 Priority to KR1020070047886A

2008-11-21 Publication of KR20080101301A

Info: Cited by (2), Legal events, Similar documents, Priority and Related Applications

External links: Espacenet, Global Dossier, Discuss

Claims (10)

Hide Dependent

translated from Korean

A semiconductor substrate on which a CMOS circuit is formed; A metal wiring layer including a metal wiring and an interlayer insulating film formed on the semiconductor substrate; A first conductivity type conductive layer formed on the metal wiring layer; An intrinsic layer formed on the first conductivity type conductive layer; And A second conductivity type conductive layer formed on the intrinsic layer, At least one of the first conductive type conductive layer, the intrinsic layer and the second conductive type conductive layer is an image sensor, characterized in that at least one uneven portion is formed on the upper surface. The method of claim 1, At least one trench is formed in any one of the first conductive conductive layer, the intrinsic layer and the second conductive conductive layer formed on the metal wiring. The method of claim 1, And an upper electrode and a color filter array formed on the second conductive conductive layer. The method of claim 1, And an adhesive layer formed between the upper electrode and the

color filter array. The method of claim 4, wherein The adhesive layer is an image sensor, characterized in that formed of a thermal resin. Forming a metal wiring layer including a metal wiring and an interlayer insulating film on the semiconductor substrate on which the CMOS circuit is formed; Forming a first conductivity type conductive layer on the metallization layer; Forming an intrinsic layer on the first conductivity type conductive layer; And Forming a second conductivity type conductive layer on the intrinsic layer; At least one uneven portion is formed on an upper surface of any one of the first conductive conductive layer, the intrinsic layer, and the second conductive conductive layer. The method of claim 6, Forming the uneven portion on the upper surface of any one of the first conductive conductive layer, the intrinsic layer and the second conductive conductive layer formed on the metal wiring, Forming at least one mask pattern on any one of the first conductivity type conductive layer and the intrinsic layer; And forming at least one trench on an upper surface of any one of the first conductive type conductive layer, the intrinsic layer, and the second conductive type conductive layer by using the mask pattern as an etching mask. The method of claim 7, wherein The trench is a method of manufacturing an image sensor, characterized in that formed by a dry etching method or a wet etching method. The method of claim 6, Forming an upper electrode on the second conductive conductive layer; And And forming a color filter array on the upper electrode. The method of claim 1, Forming an adhesive layer formed of a thermal resin on the upper electrode.

Description

translated from Korean

Image sensor and method for manufacturing thereof

1 to 5A are diagrams illustrating a manufacturing process of the image sensor of the first embodiment.

6 to 9 are diagrams illustrating a manufacturing process of the image sensor of the second embodiment.

10 to 13 are diagrams illustrating a manufacturing process of the image sensor of the third embodiment.

The embodiment discloses an image sensor and a method of manufacturing the same.

An image sensor is a semiconductor device that converts an optical image into an electrical signal, and is classified into a charge coupled device (CCD) image sensor and a complementary metal oxide silicon (CMOS) image sensor (CIS). do.

CCD image sensor has complex driving method, high power consumption, multi-stage photo process, and manufacturing process has complicated disadvantage. Therefore, as a next generation image sensor to overcome the disadvantage of the charge coupling device, Morse image sensor is attracting attention.

The CMOS image sensor implements an image by sequentially detecting an electrical signal of each unit pixel by a switching method by forming a photodiode and a MOS transistor in the unit pixel.

This CMOS image sensor is simpler to drive than the CCD image sensor, which is widely used as a conventional image sensor, and can realize various scanning methods, and can integrate signal processing onto a single chip, thereby miniaturizing the product. The use of compatible CMOS technology reduces manufacturing costs and lowers power consumption.

The CMOS image sensor according to the related art may be divided into a photo diode region (not shown) that receives a light signal and converts the light signal into an electrical signal, and a transistor region (not shown) that processes the electrical signal.

However, the CMOS image sensor according to the related art has a structure in which a photodiode and a transistor are horizontally disposed on a semiconductor substrate.

Of course, although the disadvantages of the CCD image sensor have been solved by the horizontal CMOS image sensor according to the prior art, there are still problems in the horizontal CMOS image sensor according to the prior art.

That is, according to the horizontal CMOS image sensor according to the prior art, the photodiode and the transistor are formed adjacent to each other horizontally on the substrate. Accordingly, there is a need for an additional area for forming a photodiode, thereby reducing the fill factor area and limiting the possibility of resolution.

In addition, according to the horizontal CMOS image sensor according to the prior art there is a problem that it is very difficult to achieve the optimization for the process of manufacturing the photodiode and transistor at the same time. That is, in a fast transistor process, a shallow junction is required for low sheet resistance, but such a shallow junction may not be suitable for a photodiode.

In addition, according to the horizontal CMOS image sensor according to the prior art, the size of the unit pixel is increased or decreased to maintain the sensor sensitivity of the image sensor as additional on-chip functions are added to the image sensor. Should be.

However, when the pixel size is increased, the resolution of the image sensor is reduced, and the area of the photodiode decreases in the sensor sensitivity of the image sensor.

The embodiment provides an image sensor and a method of manufacturing the same that can provide new integration of transistor circuits and photodiodes.

The present invention also provides an image sensor and a method of manufacturing the same, in which resolution and sensor sensitivity can be improved together.

In addition, to provide an image sensor and a method of manufacturing the same that can achieve a light condensation rate and simplify the process while employing a vertical photodiode.

An image sensor according to an embodiment includes a semiconductor substrate on which a CMOS circuit is formed; A metal wiring layer including a metal wiring and an interlayer insulating film formed on the semiconductor substrate; A first conductivity type conductive layer formed on the metal wiring layer; An intrinsic layer formed on the first conductivity type conductive layer; And a second conductive conductive layer formed on the intrinsic layer, wherein any one of the first conductive conductive layer, the intrinsic layer, and the second conductive conductive layer has at least one uneven portion formed thereon. It includes.

In addition, the manufacturing method of the image sensor according to the embodiment comprises the steps of: forming a metal wiring layer including a metal wiring and an interlayer insulating film on the semiconductor substrate on which the CMOS circuit is formed; Forming a first conductivity type conductive layer on the metallization layer; Forming an intrinsic layer on the first conductivity type conductive layer; And forming a second conductive conductive layer on the intrinsic layer, and forming an uneven portion on an upper surface of any one of the first conductive conductive layer, the intrinsic layer, and the second conductive conductive layer. Steps.

Hereinafter, an image sensor and a method of manufacturing the same according to an embodiment will be described in detail with reference to the accompanying drawings.

In the description of the embodiments, where described as being formed "on / over" of each layer, the on / over may be directly or through another layer (indirectly) includes everything formed.

In the drawings, the thickness or size of each layer is exaggerated, omitted, or schematically illustrated for convenience and clarity of description. In addition, the size of each component does not necessarily reflect the actual size.

In addition, the same code | symbol was used about the same part in description of each Example.

<First Embodiment>

5A is a cross-sectional view of the image sensor according to the first embodiment.

5A, the image sensor of the embodiment includes a semiconductor substrate 10 on which a CMOS circuit is formed; A metal wiring layer 20 including a metal wiring 22 and an interlayer insulating film 21 formed on the semiconductor substrate 10; A first conductivity type conductive layer 30 formed on the metal wiring layer 20; An intrinsic layer 40 formed on the first conductivity type conductive layer 30; And a second conductivity type conductive layer 51 having an uneven portion 53 formed on an upper surface of the intrinsic layer 40.

The lower electrode 25 may be formed on the metal line 22.

An upper electrode 60 and a color filter array 80 may be formed on the second conductive conductive layer 51.

In addition, an adhesive layer 70 may be formed between the upper electrode 60 and the color filter array 80. For example, the adhesive layer 70 is formed of a thermal resin.

A plurality of trenches 52 may be formed in the second conductive conductive layer 51 so that the upper surface of the second conductive conductive layer 51 may have an uneven portion 53 having a plurality of uneven shapes. .

Alternatively, as illustrated in FIG. 5B, one uneven portion 53b may be formed in the second conductive conductive layer 51b connected to the metal wire 22 to form one pixel.

As shown in FIGS. 5A and 5B, the photodiode formed on the metal wire 25 connected to the CMOS circuit (not shown) is formed to have at least one uneven portion.

Therefore, since the photodiode having at least one uneven portion is formed in one pixel including the CMOS circuit and the photodiode, the area of the photodiode can be increased to increase the light sensing efficiency.

An image sensor according to an embodiment may provide vertical integration of a transistor circuit and a photodiode.

In addition, the fill factor can be approached to 100% by vertical integration of the transistor circuit and the photodiode.

In addition, the vertical integration can provide higher sensitivity at the same pixel size than the prior art.

In addition, each unit pixel can implement a more complex circuit without reducing the sensitivity.

In addition, the surface of the photodiode formed in the unit pixel is formed in a dome shape, so that the surface area per unit pixel is increased, so that the light receiving region of the photodiode is enlarged, thereby increasing the light efficiency.

In addition, the surface of the photodiode formed in the unit pixel is formed in the shape of a dome such as a micro lens to maximize the light collecting rate.

In addition, since the photodiode is formed in a shape similar to a lens, a separate microlens forming process may not be performed, thereby simplifying the process.

A method of manufacturing the image sensor of the first embodiment will be described with reference to FIGS. 1 to 5A.

Refering to FIG. 1, a metal wiring layer 20 including a metal wiring 22 and an interlayer insulating film 21 is formed on a semiconductor substrate 10 on which a CMOS circuit (not shown) is formed.

Although not illustrated, an isolation layer (not shown) defining an active region and a field region is formed in the semiconductor substrate 10, and the photoelectric charges received by the photodiodes connected to a photodiode described later to form a unit pixel are used as electrical signals. A CMOS circuit (not shown) may be formed of a transistor structure for changing the circuit into a transistor.

Although not shown, the metal wiring layer 20 may be formed of a plurality of layers to connect the power line or the signal line to the CMOS circuit.

The metal wiring layer 20 is formed of a plurality of metal wirings 22 formed through the interlayer insulating film 21 and the interlayer insulating film 21 on the semiconductor substrate 10.

For example, the interlayer insulating film 21 may be formed of an oxide film, and the metal wire 22 may be formed of various conductive materials including metal, alloy, or silicide, that is, aluminum, copper, cobalt, or tungsten. .

The lower electrode 25 may be formed on the metal wiring layer 20 to be electrically connected to the metal wiring 22. For example, the lower electrode 25 may be formed of metals such as Cr, Ti, TiW, and Ta. Of course, the lower electrode 25 may not be formed.

A metal pixel 22 connected to the CMOS circuit of the semiconductor substrate 10 may be formed on the interlayer insulating layer 21, and then a photodiode may be formed on the metal wiring layer 20 to form a unit pixel.

The photodiode is formed on the metal wiring layer 220 to receive and receive light incident from the outside to convert and store in an electrical form. In this embodiment, a pin diode is used.

The pin diode is formed of a structure in which an n-type amorphous silicon layer, an intrinsic amorphous silicon layer, and a p-type amorphous silicon layer are bonded to each other. The performance of the photodiode is determined by the efficiency of converting it into electrical form by receiving external light and the total charge capacitance. The existing photodiode is depleted when heterojunction of PN, NP, NPN, PNP, etc. Although the charge is generated and stored in the region, the pin diode is a photodiode having a structure in which an intrinsic amorphous silicon layer, which is a pure semiconductor, is bonded between a p-type silicon layer and an n-type silicon layer. All of the intrinsic amorphous silicon layers formed therebetween become depletion regions, which is advantageous for generation and storage of charges.

As described above, in the exemplary embodiment, a pin diode is used as the photodiode, and the pin diode may have a structure of P-I-N or N-I-P. Particularly, in the embodiment, a pin structure having a PIN structure is used as an example, and the n-type amorphous silicon layer includes a first conductive type conductive layer 30 and the intrinsic amorphous silicon layer. In this case, the intrinsic layer 40 and the p-type amorphous silicon layer are referred to as a second conductivity type conductive layer 50.

A method of forming the photodiode using the pin diode will be described below.

A first conductivity type conductive layer 30 is formed on the metal wiring layer 20. The first conductivity type conductive layer 30 may serve as the N layer of the P-I-N diode employed in the present embodiment. That is, the first conductivity type conductive layer 30 may be an N type conductivity type conductive layer, but is not limited thereto.

The first conductivity type conductive layer 30 may be formed using n-doped amorphous silicon doped with N-type impurities, but is not limited thereto.

That is, the first conductivity type conductive layer 30 is a-Si: H, a-SiGe: H, a-SiC, a-SiN: H a- by adding germanium, carbon, nitrogen or oxygen to amorphous silicon. SiO: H or the like.

In addition, the first conductivity type conductive layer 30 may be formed by chemical vapor deposition (CVD), in particular, PECVD. For example, the first conductive conductive layer 30 may be formed of amorphous silicon by PECVD by mixing PH_3, P_2H_5, and the like with silane gas (SiH_4).

Next, an intrinsic layer 40 is formed on the first conductivity type conductive layer 30. The intrinsic layer 40 may serve as an I layer employed in the embodiment.

The intrinsic layer 40 may be formed using intrinsic amorphous silicon. The intrinsic layer 40 may be formed by chemical vapor deposition (CVD), in particular, PECVD. For example, the intrinsic layer 40 may be formed of amorphous silicon by PECVD using silane gas (SiH_4).

In addition, the intrinsic layer 40 is preferably formed to a thickness of about 10 to 1,000 times the thickness of the first conductive type conductive layer 30. This is because the thicker the intrinsic layer 40 is, the more the depletion region of the photodiode increases, which is advantageous for storing and generating a large amount of photocharges.

Next, a second conductivity type conductive layer 50 is formed on the intrinsic layer 40.

The second conductivity type conductive layer 50 may serve as a P layer of the P-I-N diode employed in the embodiment. That is, the second conductivity type conductive layer 50 may be a P type conductivity type conductive layer, but is not limited thereto.

For example, the second conductivity type conductive layer 50 may be formed using P-doped amorphous silicon, but is not limited thereto.

The second conductivity type conductive layer 50 may be formed by chemical vapor deposition (CVD), in particular, PECVD. For example, the second conductivity type conductive layer 50 may be formed of amorphous silicon by PECVD by mixing a gas such as BH_3 or B_2H_6 with silane gas (SiH_4).

As described above, since the circuit region formed on the semiconductor substrate 10 and the photodiode are vertically formed, the fill factor of the photodiode may approach 100%.

Referring to FIG. 2, a mask pattern 100 is formed on the second conductive conductive layer 50.

The mask pattern 100 is to form the second conductive conductive layer 50 in the form of irregularities. The mask pattern 100 is formed by applying and patterning a photoresist film.

At least one mask pattern 100 may be formed on the second conductive conductive layer 50 so that the upper surface of the second conductive conductive layer 50 has a step difference.

Referring to FIG. 3, the trench 52 is formed by etching the second conductive conductive layer 50 using the mask pattern 100 as an etch mask. Then, the concave-convex portion 53 of the concave-convex shape is formed on the upper surface of the second conductivity type conductive layer 51 by the trench 52.

The second conductive conductive layer 51 may be etched by a dry or wet etching process. In particular, the etching of the second conductivity type conductive layer 51 proceeds so that the intrinsic layer 40 under the second conductivity type conductive layer 51 is not exposed.

As described above, since the uneven portion 53 is formed on the upper surface of the second conductive conductive layer 51, the surface area of the second conductive conductive layer 51 is increased, and thus the light receiving area of the photodiode is increased. This can be extended to improve the light detection rate of the image sensor.

In addition, at least one convex dome-shaped lens is formed in one pixel by the concave-convex portion 53 of the second conductivity type conductive layer 51 to increase the light efficiency of the photodiode.

Referring to FIG. 4, the upper electrode 60 is formed on the second conductive type conductive layer 51 on which the uneven portion 52 is formed.

The upper electrode 60 may be formed of a transparent electrode having good light transmittance and high conductivity. For example, the upper electrode 60 may be formed of indium tin oxide (ITO) or cardium tin oxide (CTO).

By the shape of the uneven portion 53, the upper electrode 60 may also be formed in the uneven shape having a step.

Referring to FIG. 5A, an adhesive layer 70 and a color filter 80 are formed on the upper electrode 60.

The adhesive layer 70 is to improve the adhesion between the upper electrode 60 and the color filter 80. The adhesive layer 70 is formed by depositing a thermal resin on the upper electrode 60 and then performing a planarization process. To form.

In addition, a color filter 80 is formed on the adhesive layer 70.

In the image sensor formed as described above, photodiodes having a plurality of dome shapes may be formed in one pixel, thereby improving light condensation.

Alternatively, as illustrated in FIG. 5B, one uneven portion 53b may be formed in the second conductive conductive layer 51b formed on the metal wiring 22.

As a result, the light receiving area is extended by the uneven shape of the photodiode, thereby increasing the photosensitive index.

Second Embodiment

9 is a sectional view of an image sensor according to a second embodiment.

The image sensor of the embodiment with reference to FIG. 9 includes: a semiconductor substrate 10 on which a CMOS circuit is formed; A metal wiring layer 20 including a plurality of metal wirings 22 and an interlayer insulating film 21 formed on the semiconductor substrate 10; A first conductivity type conductive layer 31 having at least one uneven portion 33 formed on an upper surface of the metal wiring layer 20; An intrinsic layer 40 formed on the first conductivity type conductive layer 31; And a second conductivity type conductive layer 50 formed on the intrinsic layer 40.

At least one trench 32 may be formed in the first conductive conductive layer 31 so that one or more uneven portions 33 may be formed on an upper surface of the first conductive conductive layer 31.

The lower electrode 25 may be formed on the metal line 22.

An upper electrode 60 and a color filter array 80 may be formed on the second conductive conductive layer 50.

In addition, an adhesive layer 70 may be formed between the upper electrode 60 and the color filter array 80. For example, the adhesive layer 70 is formed of a thermal resin.

A manufacturing process of the image sensor of the second embodiment will be described with reference to FIGS. 6 to 9.

Referring to FIG. 6, a metal wiring layer 20 and a lower electrode 25 are formed on the semiconductor substrate 10.

Since the semiconductor substrate 10, the metallization layer 20, and the lower electrode 25 are the same as in the above-described first embodiment, description thereof will be omitted.

After forming the metal wiring 22 connected to the CMOS circuit of the semiconductor substrate 10 on the interlayer insulating film 21, a photodiode is formed on the metal wiring layer 20.

The photodiode is formed on the metal wiring layer 220 to receive and receive light incident from the outside to convert and store in an electrical form. In this embodiment, a pin diode is used. Since the photodiode used in the second embodiment is the same as the first embodiment, a detailed description thereof will be omitted and only the process sequence will be described.

A method of forming the photodiode using the pin diode will be described below.

After forming the first conductive conductive layer 30 on the metal wiring layer 20, at least one mask pattern 100 is formed on the first conductive conductive layer 30.

The mask pattern 100 is for forming the first conductivity type conductive layer 30 in the form of irregularities. The mask pattern 100 is formed by coating and patterning a photoresist film. At least one mask pattern 100 may be formed on the first conductivity type conductive layer 30 so that the upper surface of the first conductivity type conductive layer 30 has a step difference.

Referring to FIG. 7, the trench 32 is formed by etching the first conductive conductive layer 30 using the mask pattern 100 as an etch mask. Then, the concave-convex portion 33 having the concave-convex shape is formed on the upper surface of the first conductivity type conductive layer 31 by the trench 32.

The first conductive conductive layer 31 may be etched by a dry or wet etching process. In particular, the etching of the first conductivity type conductive layer 31 proceeds so that the metal wiring layer 20 positioned under the first conductivity type conductive layer 31 is not exposed.

Referring to FIG. 8, an intrinsic layer 40 and a second conductive conductive layer 50 are sequentially formed on the first conductive conductive layer 30.

Then, the intrinsic layer 40 formed along the upper surface of the first conductivity type conductive layer 31 has a stepped upper surface by the uneven portion 33 of the first conductivity type conductive layer 31. The second conductive conductive layer 50 has a stepped upper surface by the intrinsic layer 40.

Therefore, the surface of the photodiode including the first conductive conductive layer 31, the intrinsic layer 40, and the second conductive conductive layer 50 is formed in an uneven shape to improve the light sensing rate due to the increase of the surface area. it becomes possible.

In addition, since the photodiode has a shape such as a convex lens, it is possible to improve the light collecting rate.

In addition, the photodiode may have at least one uneven portion per pixel to increase the light detection rate of the photodiode.

Referring to FIG. 9, an upper electrode 60 is formed on the second conductive conductive layer 50.

The upper electrode 60 may be formed of a transparent electrode having good light transmittance and high conductivity. For example, the upper electrode 60 may be formed of indium tin oxide (ITO) or cardium tin oxide (CTO).

The adhesive layer 70 and the color filter 80 are formed on the upper electrode 60.

The adhesive layer 70 is to improve the adhesion between the upper electrode 60 and the color filter 80. The adhesive layer 70 is formed by depositing a thermal resin on the upper electrode 60 and then performing a planarization process. To form.

In addition, a color filter 80 is formed on the adhesive layer 70.

Third Embodiment

13 is a sectional view of an image sensor according to a third embodiment.

The image sensor of the embodiment with reference to FIG. 13 includes a semiconductor substrate 10 having a CMOS circuit formed thereon; A metal wiring layer 20 including a plurality of metal wirings 22 and an interlayer insulating film 21 formed on the semiconductor substrate 10; A first conductivity type conductive layer 30 formed on the metal wiring layer 20; An intrinsic layer 41 having at least one uneven portion 43 formed on an upper surface of the first conductive conductive layer 30; And a second conductivity type conductive layer 50 formed on the intrinsic layer 41.

At least one trench 42 may be formed in the intrinsic layer 41, and at least one uneven portion 43 may be formed on an upper surface of the intrinsic layer 41.

The lower electrode 25 may be formed on the metal line 22.

An upper electrode 60 and a color filter array 80 may be formed on the second conductive conductive layer 50.

In addition, an adhesive layer 70 may be formed between the upper electrode 60 and the color filter array 80. For example, the adhesive layer 70 is formed of a thermal resin.

A manufacturing process of the image sensor of the second embodiment will be described with reference to FIGS. 10 to 13.

Referring to FIG. 10, a metal wiring layer 20 and a lower electrode 25 are formed on the semiconductor substrate 10.

Since the semiconductor substrate 10, the metallization layer 20, and the lower electrode 25 are the same as those of the first embodiment described above, description thereof will be omitted.

After forming the metal wiring 22 connected to the CMOS circuit of the semiconductor substrate 10 on the interlayer insulating film 21, a photodiode is formed on the metal wiring layer 20.

The photodiode is formed on the metal wiring layer 220 to receive and receive light incident from the outside to convert and store in an electrical form. In this embodiment, a pin diode is used. Since the photodiode used in the second embodiment is the same as the first embodiment, a detailed description thereof will be omitted and only the process sequence will be described.

A method of forming the photodiode using the pin diode will be described below.

The first conductivity type conductive layer 30 and the intrinsic layer 40 are sequentially formed on the metal wiring layer 20.

The mask pattern 100 is formed on the intrinsic layer 40.

The mask pattern 100 is for forming the intrinsic layer 40 in the form of irregularities. The mask pattern 100 is formed by applying and patterning a photoresist film. At least one mask pattern 100 may be formed on the intrinsic layer 40 so that the upper surface of the intrinsic layer 41 has a step.

Referring to FIG. 11, the trench 42 is formed by etching the intrinsic layer 40 using the mask pattern 100 as an etch mask. Then, the uneven portions 43 having the uneven shape are formed on the upper surface of the intrinsic layer 41 by the trench 42.

The intrinsic layer 41 may be etched by a dry or wet etching process. In particular, the etching of the intrinsic layer 41 proceeds so that the first conductivity type conductive layer 30 positioned below the intrinsic layer 41 is not exposed.

Referring to FIG. 12, a second conductivity type conductive layer 50 is formed on the intrinsic layer 41.

Then, in the second conductive type conductive layer 50 formed along the upper surface of the intrinsic layer 41, the upper surface is stepped by the uneven portion 43 of the intrinsic layer 41.

Therefore, the surface of the photodiode including the first conductive conductive layer 30, the intrinsic layer 41, and the second conductive conductive layer 50 is formed in an uneven shape to improve the light sensing rate due to the increase of the surface area. It becomes possible.

In addition, since the photodiode has a shape such as a convex lens, it is possible to improve the light collecting rate.

Referring to FIG. 9, an upper electrode 60 is formed on the second conductive conductive layer 50.

The upper electrode 60 may be formed of a transparent electrode having good light transmittance and high conductivity. For example, the upper electrode 60 may be formed of indium tin oxide (ITO) or cardium tin oxide (CTO).

The adhesive layer 70 and the color filter 80 are formed on the upper electrode 60.

The adhesive layer 70 is to improve the adhesion between the upper electrode 60 and the color filter 80. The adhesive layer 70 is formed by depositing a thermal resin on the upper electrode 60 and then performing a planarization process. To form.

In addition, a color filter 80 is formed on the adhesive layer 70.

The embodiments described above are not limited to the above-described embodiments and drawings, and it is to be understood that various changes, modifications, and changes can be made without departing from the technical spirit of the present embodiments. It will be obvious to those who have it.

According to the image sensor and the manufacturing method thereof according to the embodiment, it is possible to provide vertical integration of the transistor circuit and the photodiode.

In addition, the fill factor can be approached to 100% by vertical integration of the transistor circuit and the photodiode.

In addition, the vertical integration can provide higher sensitivity at the same pixel size than the prior art.

In addition, each unit pixel can implement a more complex circuit without reducing the sensitivity.

In addition, by adopting a vertical photodiode, insulation between unit pixels is secured, thereby preventing crosstalk between pixels and the like, thereby improving reliability of the image sensor.

In addition, in implementing the unit pixel of the photodiode, the light sensing ratio may be improved by increasing the surface area of the photodiode in the unit pixel.

In addition, the photodiode corresponding to the unit pixel may have a lens shape such as a convex lens, thereby improving the light condensing ratio.

Cited By (2)

Publication number	Priority date	Publication date	Assignee	Title
CN109723127A *	2017-10-30	2019-05-07	上海箩寰技术有限公司	Photodiode and forming method thereof, imaging sensor, fingerprint imaging mould group
US20210242354A1 *	2015-11-17	2021-08-05	W&Wsens Devices, Inc.	Microstructure enhanced absorption photosensitive devices

Family To Family Citations

* Cited by examiner, † Cited by third party, ‡ Family to family citation

Similar Documents

Publication	Publication Date	Title
KR100851756B1	2008-08-11	Image sensor and method for manufacturing thereof
KR100894391B1	2009-04-20	Image Sensor and Method for Manufacturing Thereof
KR100935771B1	2010-01-06	Image Sensor and Method for Manufacturing Thereof
KR100872719B1	2008-12-05	Image Sensor and Method for Manufacturing thereof
KR100913019B1	2009-08-20	Image Sensor and Method for Manufacturing Thereof
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KR100884204B1	2009-02-18	Image Sensor and Method for Manufacturing thereof
KR100997312B1	2010-11-29	Image Sensor and Method for Manufactruingg thereof
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KR100924412B1	2009-10-29	Image Sensor and Method for Manufacturing Thereof
KR100935768B1	2010-01-06	Method for Manufacturing of Image Sensor
KR20090044117A	2009-05-07	Image sensor and method for manufacturing thereof

Priority And Related Applications

Priority Applications (1)

Application	Priority date	Filing date	Title
KR1020070047886A	2007-05-17	2007-05-17	Image sensor and method for manufacturing thereof

Applications Claiming Priority (1)

Application	Filing date	Title
KR1020070047886A	2007-05-17	Image sensor and method for manufacturing thereof

Legal Events

Date	Code	Title	Description
2007-05-17	A201	Request for examination	
2008-04-15	E902	Notification of reason for refusal	
2008-10-20	E601	Decision to refuse application	

Concepts

machine-extracted

Download Filter table

Name	Image	Sections	Count	Query match
manufacturing process		title,claims,abstract,description	20	0.000
metal		claims,abstract,description	53	0.000
metal		claims,abstract,description	53	0.000
semiconductor		claims,abstract,description	28	0.000
substrate		claims,abstract,description	26	0.000
layer		claims,description	228	0.000
adhesive		claims,description	21	0.000
adhesive		claims,description	21	0.000
interlayer		claims,description	14	0.000

resin	claims,description	8	0.000
resin	claims,description	8	0.000
etching	claims,description	7	0.000
dry etching	claims,description	4	0.000
metallisation	claims,description	4	0.000
wet etching	claims,description	4	0.000
method	abstract,description	16	0.000
sensitivity	abstract,description	8	0.000
silicon	abstract,description	4	0.000
silicon	abstract,description	4	0.000
complement	abstract,description	2	0.000
insulation	abstract,description	2	0.000
metal oxide	abstract,description	2	0.000
metal oxides	abstract,description	2	0.000

Show all concepts from the description section

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(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(11) 공개번호 10-2008-0101301
(43) 공개일자 2008년11월21일

(51) Int. Cl.
H01L 27/146 (2006.01)
(21) 출원번호 10-2007-0047886
(22) 출원일자 2007년05월17일
심사청구일자 2007년05월17일

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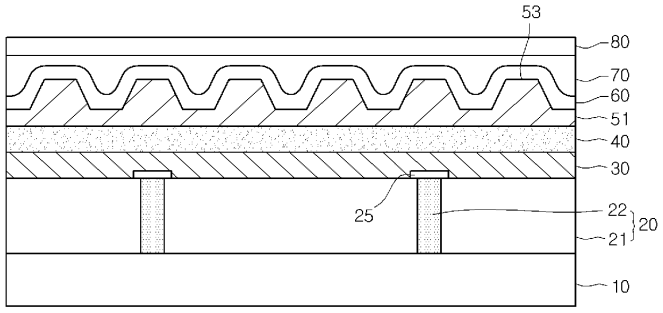
전체 청구항 수 : 총 10 항

(54) 이미지 센서 및 그의 제조방법

(57) 요 약

실시예는 이미지 센서에 관한 것으로, 씨모스 회로가 형성된 반도체 기판; 상기 반도체 기판 상에 형성된 금속배선 및 층간절연막을 포함하는 금속배선층; 상기 금속배선층 상에 형성된 제1 도전형 전도층; 상기 제1 도전형 전도층 상에 형성된 진성층; 및 상기 진성층 상에 상부 표면에 적어도 하나 이상의 요철부가 형성된 제2 도전형 전도층을 포함한다.

대 표 도 - 도5a



Samsung Exhibit 1003, Page 234 of 654

특허청구의 범위

청구항 1

씨모스 회로가 형성된 반도체 기판;

상기 반도체 기판 상에 형성된 금속배선 및 층간절연막을 포함하는 금속배선층;

상기 금속배선층 상에 형성된 제1 도전형 전도층;

상기 제1 도전형 전도층 상에 형성된 진성층; 및

상기 진성층 상에 형성된 제2 도전형 전도층을 포함하며,

상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층은 그 상부 표면에 적어도 하나 이상의 요철부가 형성된 것을 특징으로 하는 이미지 센서.

청구항 2

제1항에 있어서,

상기 금속배선 상에 형성된 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층에는 적어도 하나 이상의 트렌치가 형성된 것을 포함하는 이미지 센서.

청구항 3

제1항에 있어서,

상기 제2 도전형 전도층 상부에는 상부전극 및 컬러필터 어레이가 형성된 것을 포함하는 이미지 센서.

청구항 4

제1항에 있어서,

상기 상부전극과 컬러필터 어레이 사이에는 접착층이 형성된 것을 포함하는 이미지 센서.

청구항 5

제4항에 있어서,

상기 접착층은 열 수지로 형성된 것을 특징으로 하는 이미지 센서.

청구항 6

씨모스 회로가 형성된 반도체 기판 상에 금속배선 및 층간절연막을 포함하는 금속배선층을 형성하는 단계;

상기 금속배선층 상에 제1 도전형 전도층을 형성하는 단계;

상기 제1 도전형 전도층 상에 진성층을 형성하는 단계; 및

상기 진성층 상에 제2 도전형 전도층을 형성하는 단계를 포함하며,

상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층의 상부 표면에는 적어도 하나 이상의 요철부가 형성되는 단계를 포함하는 이미지 센서의 제조방법.

청구항 7

제6항에 있어서,

상기 금속배선 상에 형성된 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층의 상부표면에 요철부를 형성하는 단계는,

상기 제1 도전형 전도층, 진성층 중 어느 하나의 층 상에 적어도 하나 이상의 마스크 패턴을 형성하는 단계;

상기 마스크 패턴을 식각 마스크로 하여 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의

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층 상부 표면에 적어도 하나 이상의 트렌치를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 8

제7항에 있어서,

상기 트렌치는 건식식각 또는 습식식각 방법으로 형성된 것을 특징으로 하는 이미지 센서의 제조방법.

청구항 9

제6항에 있어서,

상기 제2 도전형 전도층 상에 상부전극을 형성하는 단계; 및

상기 상부전극 상에 컬러필터 어레이를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 10

제1항에 있어서,

상기 상부전극 상에 열 수지로 형성된 접착층을 형성하는 단계를 포함하는 이미지 센서의 제조방법.

명 세 서

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

<4> 실시예는 이미지 센서 및 그의 제조방법을 개시한다.

<5> 이미지 센서는 광학적 영상(Optical Image)을 전기 신호로 변환시키는 반도체 소자로서, 크게 전하결합소자(charge coupled device:CCD) 이미지 센서와 씨모스(Complementary Metal Oxide Silicon:CMOS) 이미지 센서(CIS)로 구분된다.

<6> CCD 이미지 센서는 구동방식이 복잡하고, 전력소비가 클 뿐만 아니라, 다단계의 포토공정이 요구되므로 제조공정이 복잡한 단점을 갖고 있으므로, 최근에는 상기 전하결합소자의 단점을 극복하기 위한 차세대 이미지 센서로서 씨모스 이미지 센서가 주목을 받고 있다.

<7> 씨모스 이미지 센서는 단위 화소 내에 포토다이오드와 모스트랜지스터를 형성시킴으로써 스위칭 방식으로 각 단위 화소의 전기적 신호를 순차적으로 검출하여 영상을 구현한다.

<8> 이러한 씨모스 이미지 센서는 종래 이미지 센서로 널리 사용되고 있는 CCD 이미지 센서에 비하여 구동방식이 간편하고 다양한 스캐닝 방식의 구현이 가능하며, 신호처리를 단일칩에 집적할 수 있어 제품의 소형화가 가능할 뿐만 아니라, 호환성의 씨모스 기술을 사용하므로 제조단가를 낮출 수 있고,전력 소모 또한 낮다는 장점을 지니고 있다.

<9> 종래기술에 의한 씨모스 이미지 센서는 빛 신호를 받아서 전기신호로 바꾸어 주는 포토다이오드(Photo diode) 영역(미도시)과 이 전기 신호를 처리하는 트랜지스터 영역(미도시)으로 구분할 수 있다.

<10> 그런데 종래기술에 따른 씨모스 이미지 센서는 포토다이오드와 트랜지스터가 반도체 기판에 수평으로 배치되는 구조이다.

<11> 물론, 종래기술에 의한 수평형 씨모스 이미지 센서에 의해 CCD 이미지 센서의 단점이 해결되기는 하였으나, 종래기술에 의한 수평형 씨모스 이미지 센서에는 여전히 문제점들이 있다.

<12> 즉, 종래기술에 의한 수평형 씨모스 이미지 센서에 의하면 포토다이오드와 트랜지스터가 기판 상에 상호 수평으로 인접하여 형성된다. 이에 따라, 포토다이오드 형성을 위한 추가적인 영역이 요구되며, 이에 의해 필 팩터(fill factor) 영역을 감소시키고 레졸루션(Resolution)의 가능성을 제한하는 문제가 있다.

<13> 또한, 종래기술에 의한 수평형 씨모스 이미지 센서에 의하면 포토다이오드와 트랜지스터를 동시에 제조하는 공

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정에 대한 최적화를 달성하는 점이 매우 어려운 문제가 있다. 즉, 신속한 트랜지스터 공정에서는 작은 면저항(low sheet resistance)을 위해 샐로우 정션(shllow junction)이 요구되나, 포토다이오드에는 이러한 샐로우 정션(shllow junction)이 적절하지 않을 수 있다.

<14> 또한, 종래기술에 의한 수평형 씨모스 이미지 센서에 의하면 추가적인 온칩(on-chip) 기능들이 이미지 센서에 부가되면서 단위화소의 크기가 이미지 센서의 센서티버티(sensitivity)를 유지하기 위해 증가되거나 또는 감소되어야 한다.

<15> 그런데, 픽셀사이즈가 증가되면 이미지 센서의 레졸루션(Resolution)이 감소하게 되며, 또한 포토다이오드의 면적이 이미지 센서의 센서티버티(sensitivity)가 감소하는 문제가 발생한다.

발명이 이루고자 하는 기술적 과제

<16> 실시예는 트랜지스터 회로와 포토다이오드의 새로운 집적을 제공할 수 있는 이미지 센서 및 그의 제조방법을 제공한다.

<17> 또한, 레졸루션(Resolution)과 센서티버티(sensitivity)가 함께 개선될 수 있는 이미지 센서 및 그의 제조방법을 제공한다.

<18> 또한, 수직형의 포토다이오드를 채용하면서 집광률 향상과 동시에 공정 단순화를 이룰 수 있는 이미지 센서 및 그의 제조방법을 제공하고자 한다.

발명의 구성 및 작용

<19> 실시예에 따른 이미지 센서는, 씨모스 회로가 형성된 반도체 기판; 상기 반도체 기판 상에 형성된 금속배선 및 층간절연막을 포함하는 금속배선층; 상기 금속배선층 상에 형성된 제1 도전형 전도층; 상기 제1 도전형 전도층 상에 형성된 진성층; 및 상기 진성층 상에 형성된 제2 도전형 전도층을 포함하고, 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층은 그 상부 표면에 적어도 하나 이상의 요철부가 형성된 것을 포함한다.

<20> 또한, 실시예에 따른 이미지 센서의 제조방법은, 씨모스 회로가 형성된 반도체 기판 상에 금속배선 및 층간절연막을 포함하는 금속배선층을 형성하는 단계; 상기 금속배선층 상에 제1 도전형 전도층을 형성하는 단계; 상기 제1 도전형 전도층 상에 진성층을 형성하는 단계; 및 상기 진성층 상에 제2 도전형 전도층을 형성하는 단계를 포함하며, 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층의 상부 표면에 요철부를 형성하는 단계를 포함한다.

<21> 이하, 실시예에 따른 이미지 센서 및 그의 제조방법을 첨부된 도면을 참조하여 상세히 설명한다.

<22> 실시예의 설명에 있어서, 각 층의 "상/위(on/over)"에 형성되는 것으로 기재되는 경우에 있어, 상/위(on/over)는 직접(directly)와 또는 다른 층을 개재하여(indirectly) 형성되는 것을 모두 포함한다.

<23> 도면에서 각층의 두께나 크기는 설명의 편의 및 명확성을 위하여 과장되거나 생략되거나 또는 개략적으로 도시되었다. 또한 각 구성요소의 크기는 실제크기를 전적으로 반영하는 것은 아니다.

<24> 또한, 각 실시예의 설명에 있어서 동일한 부분에 대하여 동일한 부호를 사용하였다.

<25> <제1 실시예>

<26> 도 5a는 제1 실시예에 따른 이미지 센서의 단면도이다.

<27> 도 5a를 참조하여, 실시예의 이미지 센서는, 씨모스 회로가 형성된 반도체 기판(10); 상기 반도체 기판(10) 상에 형성된 금속배선(22) 및 층간절연막(21)을 포함하는 금속배선층(20); 상기 금속배선층(20) 상에 형성된 제1 도전형 전도층(30); 상기 제1 도전형 전도층(30) 상에 형성된 진성층(40); 및 상기 진성층(40) 상에 상부표면에 요철부(53)가 형성된 제2 도전형 전도층(51)을 포함한다.

<28> 상기 금속배선(22) 상부에는 하부전극(25)이 형성될 수 있다.

<29> 상기 제2 도전형 전도층(51) 상부에는 상부전극(60) 및 컬러필터 어레이(80)가 형성될 수 있다.

<30> 또한, 상기 상부전극(60)과 컬러필터 어레이(80) 사이에는 접착층(70)이 형성될 수 있다. 예를 들어 상기 접착층(70)은 열 수지(thermal resin)로 형성된다.

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<31> 상기 제2 도전형 전도층(51)에는 복수개의 트렌치(52)가 형성되어 상기 제2 도전형 전도층(51)의 상부표면은 복수개의 요철형상을 갖는 요철부(53)가 형성될 수 있다.

<32> 또는, 도 5b에 도시된 바와 같이 상기 금속배선(22)과 연결되어 하나의 픽셀을 이루는 상기 제2 도전형 전도층(51b)에는 하나의 요철부(53b)가 형성될 수 있다.

<33> 도 5a 및 도 5b에 도시된 바와 같이, 씨모스 회로(미도시)와 연결되는 금속배선(25) 상에 형성된 포토다이오드가 적어도 하나 이상의 요철부를 가지도록 형성된다.

<34> 따라서, 씨모스 회로와 포토다이오드로 이루어지는 하나의 픽셀에 적어도 하나 이상의 요철부를 갖는 포토다이오드가 형성되므로써 상기 포토다이오드의 면적이 증가되어 광감지 효율을 증가시킬 수 있다.

<35> 실시예에 따른 이미지 센서는 트랜지스터 회로와 포토다이오드의 수직형 집적을 제공할 수 있다.

<36> 또한, 트랜지스터 회로와 포토다이오드의 수직형 집적에 의해 필 팩터(fill factor)를 100%에 근접시킬 수 있다.

<37> 또한, 수직형 집적에 의해 종래기술보다 같은 픽셀 사이즈에서 높은 센서티비티(sensitivity)를 제공할 수 있다.

<38> 또한, 각 단위 픽셀은 센서티비티(sentivity)의 감소없이 보다 복잡한 회로를 구현할 수 있다.

<39> 또한, 단위 픽셀 내에 형성된 포토다이오드의 표면이 돔 형태로 형성되어 단위 픽셀 당 표면적이 증가하여 포토다이오드의 수광영역이 확대되어 광효율을 증가지시킬 수 있다.

<40> 또한, 단위 픽셀 내에 형성된 포토다이오드의 표면이 마이크로렌즈와 같은 돔형태로 형성되어 집광율을 극대화 시킬 수 있다.

<41> 또한, 상기 포토다이오드의 형태가 렌즈와 유사한 형태로 형성되어 별도의 마이크로렌즈 형성공정을 진행하지 않아도 되므로 공정을 단순화 시킬 수 있다.

<42> 도 1 내지 도 5a를 참조하여 제1 실시예의 이미지 센서의 제조방법을 설명한다.

<43> 도 1을 참조하여, 씨모스 회로(미도시)가 형성된 반도체 기판(10) 상에는 금속배선(22) 및 층간절연막(21)을 포함하는 금속배선층(20)이 형성되어 있다.

<44> 도시하지는 않았지만, 상기 반도체 기판(10)에는 액티브 영역 및 필드 영역을 정의하는 소자분리막(미도시)이 형성되어 있으며, 단위 픽셀을 형성하기 위해 후술되는 포토다이오드에 연결되어 수광된 광전하를 전기신호로 변화시키기 위한 트랜지스터 구조물로 이루어진 씨모스 회로(미도시)가 형성되어 있을 수 있다.

<45> 도시하지는 않았지만, 상기 금속배선층(20)은 전원라인 또는 신호라인과 씨모스 회로를 접속시키기 위해 복수의 층으로 형성될 수 있다.

<46> 상기 금속배선층(20)은 반도체 기판(10) 상에 층간절연막(21)과 상기 층간절연막(21)을 관통하여 형성되는 복수의 금속배선(22)으로 형성되어 있다.

<47> 예를 들어, 상기 층간절연막(21)은 산화막으로 형성될 수 있으며, 상기 금속배선(22)은 금속, 합금 또는 실리사이드를 포함한 다양한 전도성 물질, 즉 알루미늄, 구리, 코발트 또는 텅스텐 등으로 형성할 수 있다.

<48> 상기 금속배선층(20) 상에 상기 금속배선(22)과 전기적으로 연결되는 하부전극(25)을 형성할 수도 있다. 예를 들어, 상기 하부전극(25)은 Cr, Ti, TiW 및 Ta과 같은 금속으로 형성할 수 있다. 물론 상기 하부전극(25)은 형성되지 않을 수 있다.

<49> 상기 층간절연막(21)에 상기 반도체 기판(10)의 씨모스 회로와 연결되는 금속배선(22)을 형성한 후 상기 금속배선층(20) 상부로 포토다이오드를 형성하여 단위픽셀을 형성할 수 있다.

<50> 상기 포토다이오드는 금속배선층(220) 상부에 형성되어 외부에서 입사되는 빛을 받아 전기적 형태로 전환 및 보관하기 위한 것으로 실시예에서는 핀 다이오드(PIN diode)를 사용한다.

<51> 상기 핀 다이오드는 n형 비정질 실리콘층(n-type amorphous silicon), 진성 비정질 실리콘층(intrinsic amorphous silicon), p형 비정질 실리콘층(p-type amorphous silicon)이 접합된 구조로 형성되는 것이다. 포토다이오드의 성능은 외부의 빛을 받아 전기적 형태로 전환하는 효율과 총 보관 가능 전기량(charge capacitanc

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e)에 따라 결정되는 것으로 기존의 포토다이오드는 P-N, N-P, N-P-N, P-N-P 등의 이종접합시 생성되는 공핍영역(Depletion region)에 전하를 생성 및 보관하였으나, 상기 핀 다이오드는 p형 실리콘층과 n형 실리콘층 사이에 순수한 반도체인 진성 비정질 실리콘층이 접합된 구조의 광 다이오드로서, 상기 p형과 n형 사이에 형성되는 진성 비정질 실리콘층이 모두 공핍영역이 되어 전하의 생성 및 보관에 유리하게 된다.

<52> 이와 같이 실시예에서는 포토다이오드로서 핀 다이오드를 사용하며 핀 다이오드의 구조는 P-I-N 또는 N-I-P의 구조로 형성될 수 있다. 특히, 실시예에서는 P-I-N 구조의 핀 다이오드가 사용되는 것을 예로 하며, 상기 n형 비정질 실리콘층(n-type amorphous silicon)은 제1 도전형 전도층(30), 상기 진성 비정질 실리콘층(intrinsic amorphous silicon)은 진성층(40), 상기 p형 비정질 실리콘층(p-type amorphous silicon)은 제2 도전형 전도층(50)이라 칭하도록 한다.

<53> 상기 핀 다이오드를 이용한 포토다이오드를 형성하는 방법에 대하여 설명하면 다음과 같다.

<54> 상기 금속배선층(20) 상에 제1 도전형 전도층(30)을 형성한다. 상기 제1 도전형 전도층(30)은 본 실시에에서 채용하는 P-I-N 다이오드의 N층의 역할을 할 수 있다. 즉, 상기 제1 도전형 전도층(30)은 N타입 도전형 전도층 일 수 있으나 이에 한정되는 것은 아니다.

<55> 상기 제1 도전형 전도층(30)은 N형 불순물이 도핑된 비정질 실리질 실리콘(n-doped amorphous silicon)을 이용하여 형성될 수 있으나, 이에 한정되는 것은 아니다.

<56> 즉, 상기 제1 도전형 전도층(30)은 비정질 실리콘에 게르마늄, 탄소,질소 또는 산소 등을 첨가하여 a-Si:H, a-SiGe:H, a-SiC, a-SiN:H a-SiO:H 등으로 형성될 수도 있다.

<57> 또한, 상기 제1 도전형 전도층(30)은 화학기상증착(CVD) 특히, PECVD 등에 의해 형성될 수 있다. 예를 들어, 상기 제1 도전형 전도층(30)은 실란가스(SiH_4)에 PH_3, P_2H_5 등을 혼합하여 PECVD에 의해 비정질 실리콘으로 형성될 수 있다.

<58> 그 다음, 상기 제1 도전형 전도층(30) 상으로 진성층(intrinsic layer)(40)을 형성한다. 상기 진성층(40)은 실시예에서 채용하는 I층의 역할을 할 수 있다.

<59> 상기 진성층(40)은 비정질 실리콘(intrinsic amorphous silicon)을 이용하여 형성될 수 있다. 상기 진성층(40)은 화학기상증착(CVD) 특히, PECVD 등에 의해 형성될 수 있다. 예를 들어, 상기 진성층(40)은 실란가스(SiH_4) 등을 이용하여 PECVD에 의해 비정질 실리콘으로 형성될 수 있다.

<60> 또한, 상기 진성층(40)은 상기 제1 도전형 전도층(30)의 두께 보다 약 10~1,000배 정도의 두꺼운 두께로 형성하는 것이 바람직하다. 이는 상기 진성층(40)의 두께가 두꺼울수록 포토다이오드의 공핍영역이 늘어나 많은 양의 광전하를 보관 및 생성하기에 유리하기 때문이다.

<61> 그 다음, 상기 진성층(40) 상으로 제2 도전형 전도층(50)을 형성한다.

<62> 상기 제2 도전형 전도층(50)은 실시예에서 채용하는 P-I-N 다이오드의 P층의 역할을 할 수 있다. 즉, 상기 제2 도전형 전도층(50)은 P 타입 도전형 전도층일 수 있으나 이에 한정되는 것은 아니다.

<63> 예를 들어, 상기 제2 도전형 전도층(50)은 P 도핑된 비정질 실리콘(p-doped amorphous silicon)을 이용하여 형성될 수 있으나, 이에 한정되는 것은 아니다.

<64> 상기 제2 도전형 전도층(50)은 화학기상증착(CVD) 특히, PECVD 등에 의해 형성될 수 있다. 예를 들어, 상기 제2 도전형 전도층(50)은 실란가스(SiH_4)에 BH_3 또는 B_2H_6 등의 가스를 혼합하여 PECVD에 의해 비정질 실리콘으로 형성될 수 있다.

<65> 상기와 같이 반도체 기판(10)에 형성된 회로영역과 포토다이오드가 수직형으로 형성됨으로써 포토다이오드의 필팩터(fill factor)를 100%에 근접시킬 수 있다.

<66> 도 2를 참조하여, 상기 제2 도전형 전도층(50) 상부로 마스크 패턴(100)을 형성한다.

<67> 상기 마스크 패턴(100)은 상기 제2 도전형 전도층(50)을 요철형태로 형성하기 위한 것으로, 포토레지스트 필름을 도포하고 패터닝하여 형성한다.

<68> 상기 마스크 패턴(100)은 상기 제2 도전형 전도층(50) 상에 적어도 하나 이상 형성되어 상기 제2 도전형 전도층(50)의 상부 표면이 단차를 가지도록 형성할 수 있다.

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