<69> 도 3을 참조하여, 상기 마스크 패턴(100)을 식각마스크로 하여 상기 제2 도전형 전도층(50)을 식각하여 트렌치(52)를 형성한다. 그러면 상기 트렌치(52)에 의해 상기 제2 도전형 전도층(51)의 상부 표면은 요철형태의 요철부(53)가 형성된다.

<70> 상기 제2 도전형 전도층(51)의 식각은 건식 또는 습식식각 공정으로 진행될 수 있다. 특히, 상기 제2 도전형 전도층(51)의 식각은 상기 제2 도전형 전도층(51) 하부에 위치한 진성층(40)이 노출되지 않도록 진행한다.

<71> 상기와 같이, 상기 제2 도전형 전도층(51)의 상부 표면에 요철부(53)가 형성됨으로써 상기 제2 도전형 전도층(51)의 표면적은 증가하게 되고, 이로 인해 포토다이오드의 수광영역이 확장되어 이미지 센서의 광감지율을 향상시킬 수 있다.

<72> 또한, 상기 제2 도전형 전도층(51)의 요철부(53)에 의하여 하나의 픽셀 내에 볼록한 돔 형상의 렌즈가 적어도 하나 이상 형성되어 포토다이오드의 광 효율을 증가시킬 수 있다.

<73> 도 4를 참조하여, 상기 요철부(52)가 형성된 제2 도전형 전도층(51)의 상부로 상부전극(60)을 형성한다.

<74> 상기 상부전극(60)은 빛의 투과성이 좋고 전도성이 높은 투명전극으로 형성될 수 있다. 예를 들어, 상기 상부전극(60)은 ITO(indium tin oxide) 또는 CTO(cardium tin oxide) 등으로 형성될 수 있다.

<75> 상기 요철부(53)의 형태에 의하여 상기 상부전극(60)도 단차를 가지는 요철형태로 형성될 수 있다.

<76> 도 5a를 참조하여, 상기 상부전극(60) 상으로 접착층(70) 및 컬러필터(80)를 형성한다.

<77> 상기 접착층(70)은 상기 상부전극(60)과 컬러필터(80)의 접착력을 향상시키기 위한 것으로, 상기 상부전극(60) 상으로 열 수지(thermal resin)를 증착하여 형성한 후 평탄화 공정을 진행하여 형성한다.

<78> 그리고, 상기 접착층(70)의 상부로 컬러필터(80)를 형성한다.

<79> 상기와 같이 형성된 이미지 센서는 하나의 픽셀 내에 복수의 돔형태를 갖는 포토다이오드가 형성되어 집광율을 향상시킬 수 있다.

<80> 또는 도 5b에 도시된 바와 같이, 상기 금속배선(22) 상에 형성된 제2 도전형 전도층(51b)에 하나의 요철부(53b)가 형성될 수 있다.

<81> 그러면 상기 포토다이오드의 요철형태에 의하여 수광면적이 확장되어 감광지율을 높일 수 있다.

<82> <제2 실시예>

<83> 도 9는 제2 실시예에 따른 이미지 센서의 단면도이다.

<84> 도 9를 참조하여 실시예의 이미지 센서는, 씨모스 회로가 형성된 반도체 기판(10); 상기 반도체 기판(10) 상에 형성된 복수의 금속배선(22) 및 층간절연막(21)을 포함하는 금속배선층(20); 상기 금속배선층(20) 상에 상부표면에 적어도 하나 이상의 요철부(33)가 형성된 제1 도전형 전도층(31); 상기 제1 도전형 전도층(31) 상에 형성된 진성층(40); 및 상기 진성층(40) 상에 형성된 제2 도전형 전도층(50)을 포함한다.

<85> 상기 제1 도전형 전도층(31)에는 적어도 하나 이상의 트렌치(32)가 형성되어 상기 제1 도전형 전도층(31)의 상부표면은 하나 이상의 요철부(33)가 형성될 수 있다.

<86> 상기 금속배선(22) 상부에는 하부전극(25)이 형성될 수 있다.

<87> 상기 제2 도전형 전도층(50) 상부에는 상부전극(60) 및 컬러필터 어레이(80)가 형성될 수 있다.

<88> 또한, 상기 상부전극(60)과 컬러필터 어레이(80) 사이에는 접착층(70)이 형성될 수 있다. 예를 들어 상기 접착층(70)은 열 수지(thermal resin)로 형성된다

<89> 도 6 내지 도 9를 참조하여 제2 실시예의 이미지 센서의 제조공정을 설명한다.

<90> 도 6을 참조하여, 반도체 기판(10) 상에는 금속배선층(20) 및 하부전극(25)이 형성되어 있다.

<91> 상기 반도체 기판(10), 금속배선층(20) 및 하부전극(25)은 상술된 제1 실시예와 동일하므로 이에 대한 설명은 생략하기로 한다.

<92> 상기 층간절연막(21)에 상기 반도체 기판(10)의 씨모스 회로와 연결되는 금속배선(22)을 형성한 후 상기 금속배선층(20) 상부로 포토다이오드를 형성한다.



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<93> 상기 포토다이오드는 금속배선층(220) 상부에 형성되어 외부에서 입사되는 빛을 받아 전기적 형태로 전환 및 보관하기 위한 것으로 실시예에서는 핀 다이오드(PIN diode)를 사용한다. 제2 실시예에서 사용되는 포토다이오드는 제1 실시예와 동일하므로 이에 대한 구체적은 설명은 생략하고 공정순서에 대해서만 설명하도록 한다.

<94> 상기 핀 다이오드를 이용한 포토다이오드를 형성하는 방법에 대하여 설명하면 다음과 같다.

<95> 상기 금속배선층(20) 상에 제1 도전형 전도층(30)을 형성한 후, 상기 제1 도전형 전도층(30) 상부로 적어도 하나 이상의 마스크 패턴(100)을 형성한다.

<96> 상기 마스크 패턴(100)은 상기 제1 도전형 전도층(30)을 요철형태로 형성하기 위한 것으로, 포토레지스트 필름을 도포하고 패터닝하여 형성한다. 상기 마스크 패턴(100)은 상기 제1 도전형 전도층(30) 상에 적어도 하나 이상 형성되어 상기 제1 도전형 전도층(30)의 상부 표면이 단차를 가지도록 형성할 수 있다.

<97> 도 7을 참조하여, 상기 마스크 패턴(100)을 식각마스크로 하여 상기 제1 도전형 전도층(30)을 식각하여 트렌치(32)를 형성한다. 그러면 상기 트렌치(32)에 의해 상기 제1 도전형 전도층(31)의 상부 표면에는 요철형태의 요철부(33)가 형성된다.

<98> 상기 제1 도전형 전도층(31)의 식각은 건식 또는 습식식각 공정으로 진행될 수 있다. 특히, 상기 제1 도전형 전도층(31)의 식각은 상기 제1 도전형 전도층(31) 하부에 위치한 금속배선층(20)이 노출되지 않도록 진행한다.

<99> 도 8을 참조하여, 상기 제1 도전형 전도층(30) 상으로 진성층(intrinsic layer)(40) 및 제2 도전형 전도층(50)을 순차적으로 형성한다.

<100> 그러면, 상기 제1 도전형 전도층(31)의 상부 표면을 따라 형성되는 상기 진성층(40)은 상기 제1 도전형 전도층(31)의 요철부(33)에 의해 상부 표면이 단차를 가지게 되고, 상기 제2 도전형 전도층(50)은 상기 진성층(40)에 의해 상부 표면이 단차를 가지게 된다.

<101> 따라서, 상기 제1 도전형 전도층(31), 진성층(40) 및 제2 도전형 전도층(50)으로 이루어지는 포토다이오드의 표면은 요철형태로 형성되어 표면적 증가로 인하여 광감지율을 향상시킬 수 있게 된다.

<102> 또한, 상기 포토다이오드의 형태가 볼록렌즈와 같은 형태를 가지게 되므로 집광율을 향상시킬 수 있게 된다.

<103> 또한, 상기 포토다이오드는 하나의 픽셀당 적어도 하나 이상의 요철부가 형성되어 포토다이오드의 광감지율을 높일 수 있다.

<104> 도 9를 참조하여, 상기 제2 도전형 전도층(50)의 상부로 상부전극(60)을 형성한다.

<105> 상기 상부전극(60)은 빛의 투과성이 좋고 전도성이 높은 투명전극으로 형성될 수 있다. 예를 들어, 상기 상부전극(60)은 ITO(indium tin oxide) 또는 CTO(cardium tin oxide) 등으로 형성될 수 있다.

<106> 그리고, 상기 상부전극(60) 상으로 접착층(70) 및 컬러필터(80)를 형성한다.

<107> 상기 접착층(70)은 상기 상부전극(60)과 컬러필터(80)의 접착력을 향상시키기 위한 것으로, 상기 상부전극(60) 상으로 열 수지(thermal resin)를 증착하여 형성한 후 평탄화 공정을 진행하여 형성한다.

<108> 그리고, 상기 접착층(70)의 상부로 컬러필터(80)를 형성한다.

<109> <제3 실시예>

<110> 도 13은 제3 실시예에 따른 이미지 센서의 단면도이다.

<111> 도 13을 참조하여 실시예의 이미지 센서는, 씨모스 회로가 형성된 반도체 기판(10); 상기 반도체 기판(10) 상에 형성된 복수의 금속배선(22) 및 층간절연막(21)을 포함하는 금속배선층(20); 상기 금속배선층(20) 상에 형성된 제1 도전형 전도층(30); 상기 제1 도전형 전도층(30) 상에 상부표면에 적어도 하나 이상의 요철부(43)가 형성된 진성층(41); 및 상기 진성층(41) 상에 형성된 제2 도전형 전도층(50)을 포함한다.

<112> 상기 진성층(41)에는 적어도 하나 이상의 트렌치(42)가 형성되어 상기 진성층(41)의 상부표면은 적어도 하나 이상의 요철부(43)가 형성될 수 있다.

<113> 상기 금속배선(22) 상부에는 하부전극(25)이 형성될 수 있다.

<114> 상기 제2 도전형 전도층(50) 상부에는 상부전극(60) 및 컬러필터 어레이(80)가 형성될 수 있다.



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<115> 또한, 상기 상부전극(60)과 컬러필터 어레이(80) 사이에는 접착층(70)이 형성될 수 있다. 예를 들어 상기 접착층(70)은 열 수지(thermal resin)로 형성된다

<116> 도 10 내지 도 13을 참조하여 제2 실시예의 이미지 센서의 제조공정을 설명한다.

<117> 도 10을 참조하여, 반도체 기판(10) 상에는 금속배선층(20) 및 하부전극(25)이 형성되어 있다.

<118> 상기 반도체 기판(10), 금속배선층(20) 및 하부전극(25)은 상술된 제1 실시예와 동일하므로 이에 대한 설명은 생략하기로 한다.

<119> 상기 층간절연막(21)에 상기 반도체 기판(10)의 씨모스 회로와 연결되는 금속배선(22)을 형성한 후 상기 금속배선층(20) 상부로 포토다이오드를 형성한다.

<120> 상기 포토다이오드는 금속배선층(220) 상부에 형성되어 외부에서 입사되는 빛을 받아 전기적 형태로 전환 및 보관하기 위한 것으로 실시예에서는 핀 다이오드(PIN diode)를 사용한다. 제2 실시예에서 사용되는 포토다이오드는 제1 실시예와 동일하므로 이에 대한 구체적은 설명은 생략하고 공정순서에 대해서만 설명하도록 한다.

<121> 상기 핀 다이오드를 이용한 포토다이오드를 형성하는 방법에 대하여 설명하면 다음과 같다.

<122> 상기 금속배선층(20) 상에 제1 도전형 전도층(30) 및 진성층(40)을 순차적으로 형성한다.

<123> 상기 진성층(40) 상으로 상부로 마스크 패턴(100)을 형성한다.

<124> 상기 마스크 패턴(100)은 상기 진성층(40)을 요철형태로 형성하기 위한 것으로, 포토레지스트 필름을 도포하고 패터닝하여 형성한다. 상기 마스크 패턴(100)은 상기 진성층(40) 상에 적어도 하나 이상 형성되어 상기 진성층(41)의 상부 표면이 단차를 가지도록 형성할 수 있다.

<125> 도 11을 참조하여, 상기 마스크 패턴(100)을 식각마스크로 하여 상기 진성층(40)을 식각하여 트렌치(42)를 형성한다. 그러면 상기 트렌치(42)에 의해 상기 진성층(41)의 상부 표면에는 요철형태의 요철부(43)가 형성된다.

<126> 상기 진성층(41)의 식각은 건식 또는 습식식각 공정으로 진행될 수 있다. 특히, 상기 진성층(41)의 식각은 상기 진성층(41) 하부에 위치한 제1 도전형 전도층(30)이 노출되지 않도록 진행한다.

<127> 도 12를 참조하여, 상기 진성층(41) 상으로 제2 도전형 전도층(50)을 형성한다.

<128> 그러면, 상기 진성층(41)의 상부 표면을 따라 형성되는 상기 제2 도전형 전도층(50)은 상기 진성층(41)의 요철부(43)에 의해 상부 표면이 단차를 가지게 된다.

<129> 따라서, 상기 제1 도전형 전도층(30), 진성층(41) 및 제2 도전형 전도층(50)으로 이루어지는 포토다이오드의 표면은 요철형태로 형성되어 표면적 증가로 인하여 광감지율을 향상시킬 수 있게 된다.

<130> 또한, 상기 포토다이오드의 형태가 볼록렌즈와 같은 형태를 가지게 되므로 집광율을 향상시킬 수 있게 된다.

<131> 도 9를 참조하여, 상기 제2 도전형 전도층(50)의 상부로 상부전극(60)을 형성한다.

<132> 상기 상부전극(60)은 빛의 투과성이 좋고 전도성이 높은 투명전극으로 형성될 수 있다. 예를 들어, 상기 상부전극(60)은 ITO(indium tin oxide) 또는 CTO(cardium tin oxide) 등으로 형성될 수 있다.

<133> 그리고, 상기 상부전극(60) 상으로 접착층(70) 및 컬러필터(80)를 형성한다.

<134> 상기 접착층(70)은 상기 상부전극(60)과 컬러필터(80)의 접착력을 향상시키기 위한 것으로, 상기 상부전극(60) 상으로 열 수지(thermal resin)를 증착하여 형성한 후 평탄화 공정을 진행하여 형성한다.

<135> 그리고, 상기 접착층(70)의 상부로 컬러필터(80)를 형성한다.

<136> 이상에서 설명한 실시예는 전술한 실시예 및 도면에 한정되는 것이 아니고, 본 실시예의 기술적 사상을 벗어나지 않는 범위 내에서 여러 가지 치환, 변형 및 변경할 수 있다는 것은 본 실시예가 속하는 기술 분야에서 통상의 지식을 가진자에게 있어 명백할 것이다.

## 발명의 효과

<137> 실시예에 따른 이미지 센서 및 그의 제조방법에 의하면 트랜지스터 회로와 포토다이오드의 수직형 집적을 제공할 수 있다.



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<138> 또한, 트랜지스터 회로와 포토다이오드의 수직형 집적에 의해 필 팩터(fill factor)를 100%에 근접시킬 수 있다.

<139> 또한, 수직형 집적에 의해 종래기술보다 같은 픽셀 사이즈에서 높은 센서티비티(sensitivity)를 제공할 수 있다.

<140> 또한, 각 단위 픽셀은 센서티비티(sentivity)의 감소없이 보다 복잡한 회로를 구현할 수 있다.

<141> 또한, 수직형 포토다이오드를 채용하면서 단위 픽셀 간의 절연성을 확보함으로써 픽셀간의 크로스토크 등을 방지하여 이미지 센서의 신뢰성을 향상시킬 수 있다.

<142> 또한, 포토다이오드의 단위픽셀을 구현함에 있어 단위 픽셀 내의 포토다이오드의 표면적을 증가시켜 광감지율을 향상시킬 수 있다.

<143> 또한, 상기 단위픽셀에 해당하는 포토다이오드가 볼록렌즈와 같은 렌즈형태를 가지게 되어 집광율을 향상시킬 수 있다.

## 도면의 간단한 설명

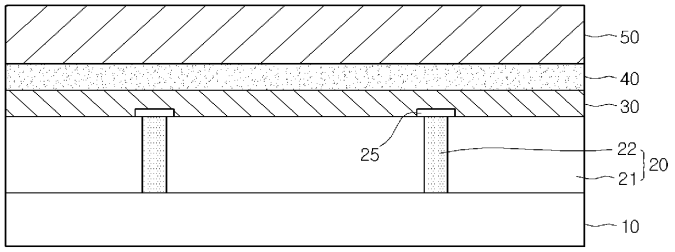
<1> 도 1 내지 도 5a는 제1 실시예의 이미지 센서의 제조 공정을 나타내는 도면이다.

<2> 도 6 내지 도 9는 제2 실시예의 이미지 센서의 제조 공정을 나타내는 도면이다.

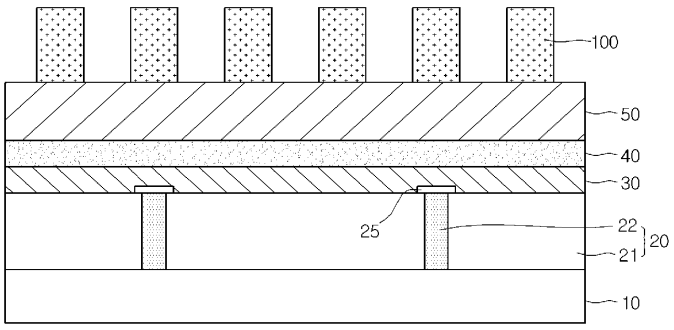
<3> 도 10 내지 도 13은 제3 실시예의 이미지 센서의 제조 공정을 나타내는 도면이다.

## 도면

### 도면1



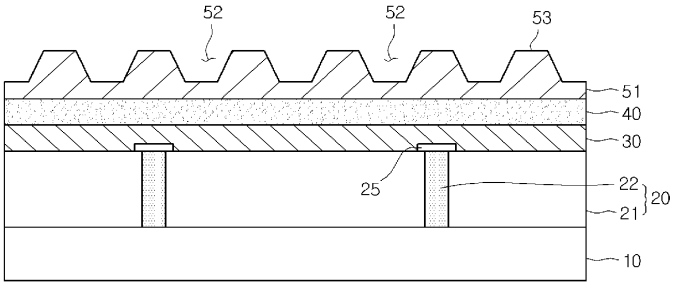

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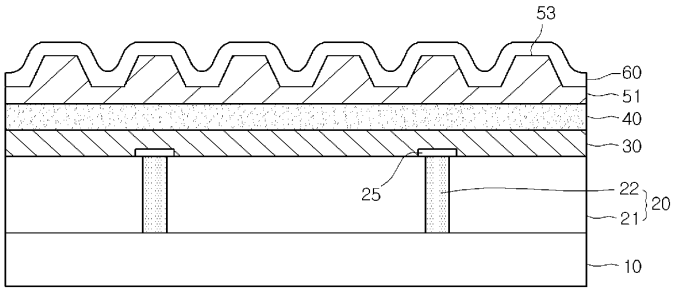



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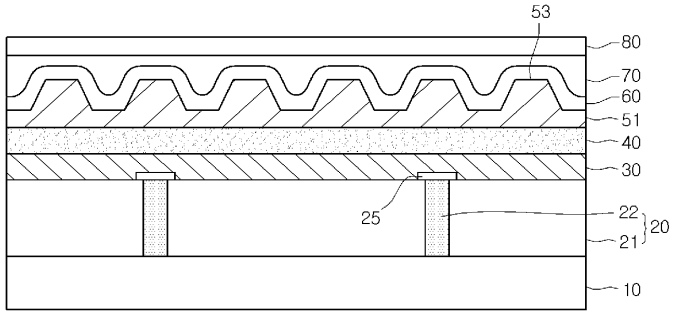
도면3




도면4



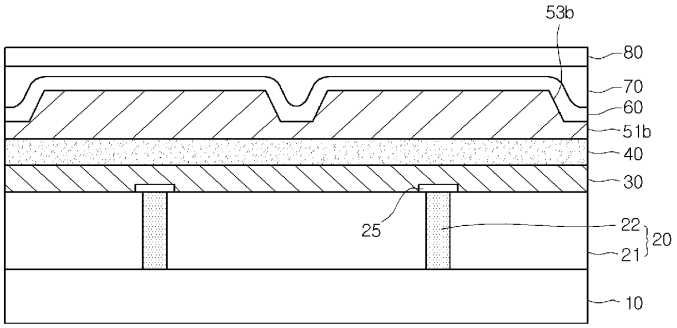

도면5



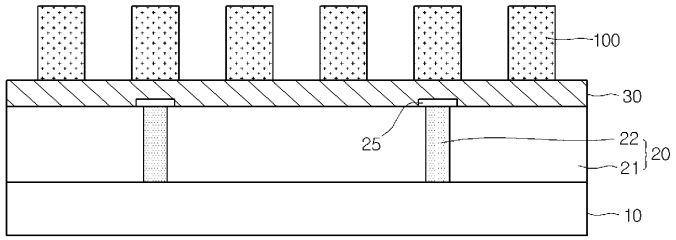



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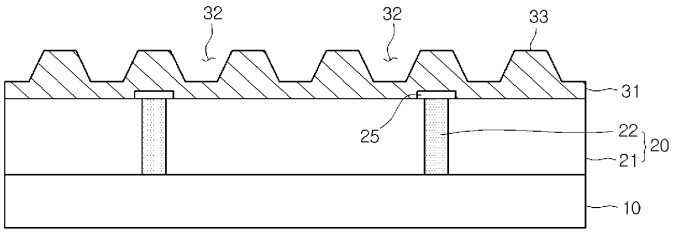
도면5




도면6



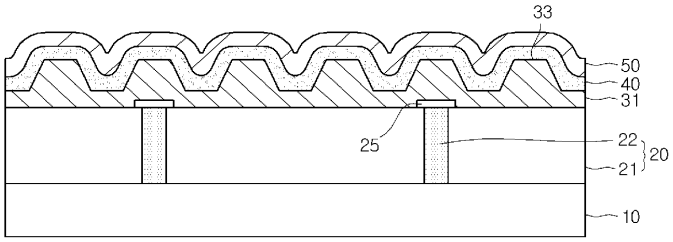

도면7



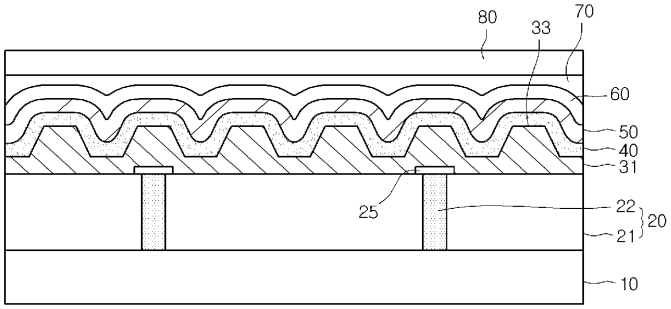



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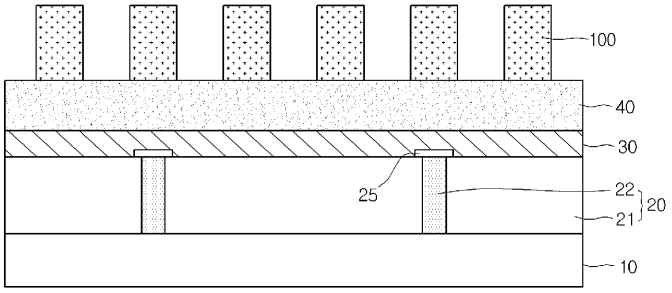
도면8




도면9



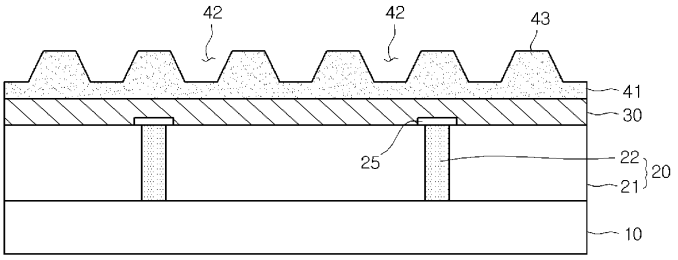

도면10



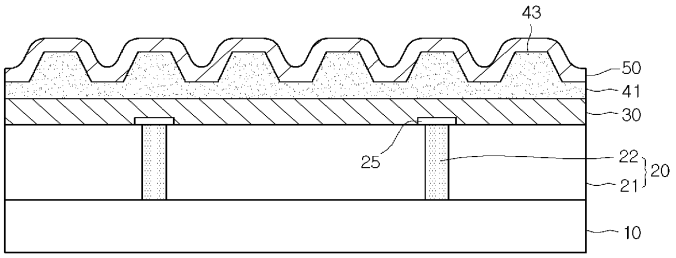



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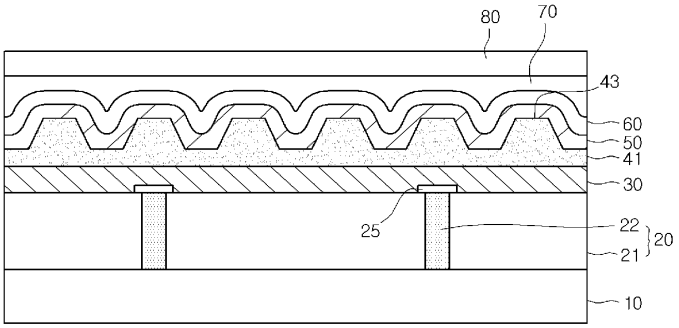
도면11




도면12




도면13






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(71) Applicant and
(72) Inventor: SCOTT, Jeffrey, W. [US/US]; 1085 Miami Way, Boulder, CO 80303 (US).

(72) Inventor: WASSERBAUER, John; 565 Mohawk Drive A6, Boulder, CO 80303 (US).

(74) Agent: HASAN, Syed, A.; Christie, Parker & Hale, LLP, P.O. Box 7068, Pasadena, CA 91109-7068 (US).

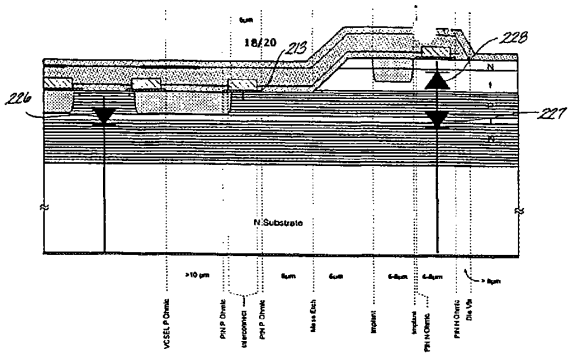
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(54) Title: A CLOSELY-SPACED VCSEL AND PHOTODETECTOR FOR APPLICATIONS REQUIRING THEIR INDEPENDENT OPERATION




(57) Abstract: A monolithically integrated VCSEL and photodetector, and a method of manufacturing the same, are disclosed for applications where the VCSEL and photodetector require separate operation such as duplex serial data communications applications. A first embodiment integrates a VCSEL with an MSM photodetector on a semi-insulating substrate. A second embodiment builds layers of a p-i-n photodiode on top of layers forming a VCSEL using a standard VCSEL process. The p-i-n layers are etched away in areas where VCSELs are to be formed and left where photodetectors are to be formed. The VCSELs underlying the photodetectors are inoperable, and serve to recirculate photons which are not initially absorbed back into the photodetector. The transmit and receive pairs are packaged into a single package for interface to multifiber ferrules. The distance between the devices is precisely defined photolithographically, thereby making alignment easier. In a further alternate embodiment, an FET is coupled to the p-i-n photodiode to form an integrated detector preamplifier along with the VCSEL transmitter all on the same optical reference plane.

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# A CLOSELY-SPACED VCSEL AND PHOTODETECTOR FOR APPLICATIONS REQUIRING THEIR INDEPENDENT OPERATION

## FIELD OF THE INVENTION

The present invention relates to vertical cavity surface emitting lasers (VCSELs) and photodetectors, and more particularly to the application of such optoelectronic devices where they must operate independently but where it is also desirable to have a transmitter and a receiver closely-spaced.

## BACKGROUND OF THE INVENTION

There are a number of data communications applications that make use of optoelectronic sending and receiving devices (i.e. light emitters and photodetectors). For fiber optic data communication applications requiring less than 200 MBits/sec, light emitting diodes (LEDs) are the light emitters of choice because they are relatively inexpensive to manufacture. For applications requiring higher speeds, lasers are typically used as the light emitters.

Until recently, most high speed data communications applications employed edge emitting lasers in a serial (single channel) format. With the advent of VCSELs, many such applications are now implemented using VCSEL arrays that can be interfaced to ferrules carrying multiple fibers to transmit several bits of data in parallel. At the receiving end, an array of photodetectors is coupled to the multiple fibers. The ability to manufacture VCSELs in arrays (an advantage of LEDs), combined with their high speed of operation (an advantage of lasers), makes VCSELs desirable in such applications.

For high-speed serial duplex data communications applications, however, separately packaged light emitters (usually edge emitting lasers) and photodetectors are still employed. For long-haul applications (typically having distances greater than 1 kilometer), wavelength division multiplexing is often employed to transmit and receive data for a duplex channel over the same fiber. Because the primary cost of a long-haul duplex serial data channel resides in the



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fiber and its installation, complex beam-splitting techniques can be justified at the ends of the channel to separate the transmit and receive data streams from the single fiber.

For short-haul or "premises" applications, however, the cost of fiber and fiber installation is relatively less important than the cost of the many transmit and receive functions. Thus, it is the cost of the data transmit and receive components, and particularly the optoelectronic devices and their packaging, that drives cost considerations for short-haul applications. Typical short-haul implementations of a high-speed serial fiber optics data communications channel operating in full duplex still employ two multimode fibers, each one to connect an individually packaged transmitting light emitter to an individually packaged receiving photodetector. This is because the cost of complex beam-splitting components often cannot be justified.

FIGS. 1(a) and 1(b) illustrate the components comprising a typical implementation of a transmit or receive link for a short-haul high-speed duplex data communications application. FIG. 1(a) illustrates a fiber assembly 12. A round ferrule 26 houses an optical fiber 28, which is located precisely in the center of ferrule 26. A typical diameter for ferrule 26 is approximately 2.5 mm. Ferrule 26 comes with a latching mechanism 30, which is used to clamp and secure the ferrule to a barrel 32 of an optical sub-assembly 10, which is depicted in Fig. 1(b). Barrel 32 houses optoelectronic device 14 typically in a TO can package 16 centrally located in the barrel as shown. Optoelectronic device 14 is typically located at an appropriate point within can 16 by a standoff 2. Driver or amplifier circuitry is coupled to optoelectronic device 14 through leads 22. A window 18 is provided in the top of the can package to allow transmitted light out or received light in, depending upon whether the optoelectronic device is a light emitter or a photodetector. The TO package is aligned with fiber 28 and epoxied using epoxy 24 to fix the position of the optoelectronic device with respect to the ferrule 26 and hence fiber 28. Optical elements such as lens 20 are typically provided to focus the light for optimal

optical efficiency, particularly where the light emitter is an edge emitting laser. Barrel 32 is designed to mate with latching mechanism 30 of fiber assembly 12.

Both fiber assembly 12 and barrel 10 are precision manufactured for precise mating. Active alignment of TO package 16 and optoelectronic device is ordinarily performed in the x, y and z axes. First, the optoelectronic device is precisely aligned within the package 16. Second, the package 16 is precisely aligned within barrel 10. Finally, optical element 20 is precisely aligned with respect to its distance from the optoelectronic device 14 to achieve proper optical operation. Because a separate package is required for both the transmit side and the receive side of the duplex data channel, a total of twelve active alignments are typically performed for each channel and each channel includes the cost of eight precision-manufactured coupling parts.

FIGS. 1(c) and 1(d) provide schematic illustrations of the fiber assembly 12 and optoelectronics subassembly 10 of FIGS. 1(a) and 1(b), respectively.

FIG. 2 illustrates a typical duplex serial data communications module 40, which has mounted to it an optical subassembly 52 containing a light emitting device 13 disposed in a TO can package 9 having a window 17, which is to be mated with an optical fiber assembly 46 and which is dedicated to data transmission. Module 40 also has an optical subassembly 50 mounted to it containing a photodetector 15 disposed in TO can package 11 and which is to be mated with optical fiber assembly 48 and dedicated to receiving data from a remote module not shown. Because of the differing optical requirements of the transmit and receive devices, the modules must often be mounted in a staggered fashion as shown. Moreover, the transmit devices are located at an optically appropriate point in their can packages by standoffs 4 and 6 respectively.

Because of the cost of the precision components and the large number of alignments required for implementing duplex serial modules 40, it is highly desirable to integrate the transmit and receive optoelectronic devices (i.e. light

emitter and photodetector) into one package. Integration of the two devices into a single package is not, however, easily achieved. The prior art implementations as illustrated in FIGS. 1a-d and 2 cannot be readily adapted to multifiber ferrules currently available for unidirectional data transmission using VCSEL arrays. These multifiber ferrules have fiber spacings which are typically about 250 microns and can be less. The diameter of the TO can package 14 commonly used in present implementations is itself 5600 microns in diameter. Thus, the standard ferrule and barrel would have to grow substantially in diameter to accommodate two fibers having the spacing dictated by the TO cans housing the optoelectronic devices.

Even if a substantially larger barrel could be created to integrate the light emitter and photodetector as commonly packaged to receive both a transmit and a receive fiber, it is not clear that the resulting package could provide the necessary separation of incoming and scattered outgoing light beams to prevent crosstalk between the transmit and receive signals (at least not without complex optics and possibly some form of isolation). Although solutions have been disclosed to stack a light emitter (typically an LED) on top of a photodetector to transmit and receive wavelength division multiplexed signals (the light emitter is transparent to the received wavelength), beam-splitting must still be employed at the opposite end.

Closely spaced VCSELs and photodetectors can suffer leakage effects which can degrade the sensitivity of and induce excess noise into the operation of the photodetector. Also, current leakage from the VCSEL to the photodetector can unacceptably alter the operating characteristics of the photodetector over time.

Conventional photodetectors output low amplitude current signals that are highly susceptible to noise and crosstalk with the VCSEL. Therefore, conventional photodetectors require highly sensitive interface electronics, typically Gallium Arsenide (GaAs) for high speed, low noise integration with the photodetector. The use of GaAs receiver electronics,



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however, greatly adds to the cost of high speed data communications.

Thus, there is room in the art for an improvement in the area of optoelectronic device fabrication which facilitates the integration of one or more pairs of transmit and receive devices, without current leakage between them, for interfacing with a single ferrule carrying one or more pairs of fibers having spacings of 250 microns or less, to substantially reduce the cost and complexity of implementing high-speed serial duplex data communications channels including the cost of receiver interface electronics.

SUMMARY OF THE INVENTION

It is therefore an objective of the present invention to provide a VCSEL device sufficiently close to a photodetector device to permit the use of commercially available multifiber ferrules having fibers spaced on the order of 750 microns to 250 microns or less. Ferrules having fiber spacing of 750 microns are referred to as having a small form factor (SMFF).

An exemplary embodiment of the present invention provides closely-spaced but independently operable optoelectronic devices by monolithically integrating the two devices on the same substrate. The invention also provides a process by which multiple pairs of VCSELs and photodetectors can be arrayed on the same substrate. The invention further provides a process by which the closely-spaced but independently operable optoelectronic devices can be packaged using known lead-frame or ceramic packaging technologies. The invention may be used to integrate any requisite optics with either the semiconductor manufacturing technology or the packaging technology.

The invention simplifies significantly the alignment of the fibers to the closely-spaced optoelectronic devices by taking advantage of the photolithographic nature of monolithic semiconductor processing to precisely define the separation between the optoelectronic devices.

The invention also provides closely-spaced but independently operable VCSEL and photodetector pairs capable

of near-field operation requiring no optics and which permit butt coupling between a package containing the optoelectronic devices and a flat faced multifiber ferrule.

In a first preferred embodiment of the invention, one or more VCSELs are formed using a known process for manufacturing such devices. The one or more VCSELs comprise an n-type GaAs substrate and a first mirror formed on the substrate, which is a well-known distributed Bragg reflector (DBR), and a first spacer or cladding layer which is formed on top of mirror. This first mirror is also preferably doped n-type. An active region is then formed on top of the first cladding layer, the active region comprising at least one quantum well layer or bulk layer. A second spacer or cladding layer is formed on the active region, with a second DBR being formed on the second spacer layer and doped to have p-type conductivity.

On top of the VCSEL layers is grown an etch-stop layer of AlGaAs having about 90% or greater Al content. An extended p-type layer of AlGaAs having more typical alloy proportions is then grown on top of the etch-stop layer. On top of this p-type layer is grown an intrinsic layer (i) which is undoped GaAs. On top of the intrinsic layer is grown an n-type region of AlGaAs. An etching process is then performed to etch away the extended p, i, and n layers where the one or more VCSELs are to be formed. The etching process uses the etch-stop layer to mark the end of the etching process so that the VCSEL area has exposed the top surface of an appropriately designed mirror. A proton implant region is created which separates the one or more VCSELs and the photodetectors formed by the unetched p, i, and n layers. Anode contacts are formed over the non-implanted p regions to form apertures for the VCSELs. A VCSEL cathode contact is formed on the substrate. Anode contacts are also formed on the p region of the p-i-n photodiode and a cathode contact is made to the n region of the p-i-n photodiode.

Thus, in this preferred embodiment, a VCSEL circuit can be isolated from a p-i-n photodiode using a proton implant isolation region which is commonly used to isolate VCSELs formed in arrays. The anode contacts to the p region of the



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p-i-n photodiode may be coupled to ground so that the VCSEL structure which lies underneath the p-i-n photodiode is never turned on and other bipolar parasitic effects are avoided. The width of the proton implant isolation region is typically between 50 and 100 microns. Thus, the VCSEL and the p-i-n photodiode can be separated by an accurately known distance, significantly less than 25 microns if desired. Moreover, the difference in thickness between the VCSEL and the p-i-n photodiode is small, thereby permitting near-field coupling of the optoelectronic devices to fibers.

One significant advantage of the first embodiment of the invention is that it requires very few additional steps to an otherwise typical VCSEL manufacturing process. A second advantage is that, when an anti-reflection coating of silicon nitride is applied to the photo-receiving n region of the photodiode, in conjunction with the p-type mirror which underlies the p-i-n photodiode, a high degree of efficiency is achieved. The silicon nitride anti-reflection coating increases transmission of incoming light into the surface of the p-i-n photodiode. Additionally, any light which is not absorbed by the intrinsic layer of the photodiode on its way through will be reflected from the underlying p-type mirror back into the intrinsic layer and will then have a second opportunity to be absorbed.

Another embodiment of the invention employs a VCSEL with an MSM photodiode. The VCSEL is manufactured on a semi-insulating substrate. Because the MSM photodetector employs the semi-insulating layer as its common cathode, the two optoelectronic devices are virtually isolated from one another electronically as a result. A photolithographically defined minimum spacing of 250 microns or less can also be achieved using the second preferred embodiment of the invention. An anti-reflection coating is also preferably employed over the MSM photodetector to increase efficiency. To further enhance electrical isolation between the two devices, an isolation region can also be formed, preferably by implantation. Another advantage of using an MSM photodiode is that the two

anode terminals can be used to drive a differential amplifier, thereby permitting common-mode rejection of noise.

Each embodiment can be integrated with optically transmissive materials that can be formed into lenses on the surface of the semiconductor. Either embodiment can also be implemented within standard precision manufactured barrels to be aligned with circular ferrules containing multiple fibers. Finally, either embodiment can be encapsulated using known lead-frame or ceramic packaging technology to permit near-field flat coupling between a flat package having an optically transmissive surface and a commercially available flat rectangular ferrule containing multiple fibers.

A further embodiment of the present invention provides a low cost method of repeatably manufacturing a closely-spaced or small form factor (SMFF) package for optical transceivers. The system includes a highly insulative, proton implantation region that isolates the photodetector and eliminates current leakage (i.e. crosstalk) between the VCSEL and photodetector. In an alternate embodiment of the present invention, the photodetector is integrated with a FET to form a high speed integrated detector preamplifier on a single chip.

In one aspect, the present inventions provides a method of manufacturing monolithic VCSEL and photodetector pairs by forming VCSEL layers directly on a semiconductor wafer substrate by forming first mirror layers, forming a first cladding layer on the first mirror layers, forming an active region on the first cladding layer, forming a second cladding layer on the active region, forming second mirror layers on the second cladding layer, forming photodiodes distributed across the wafer, and defining active and inactive VCSELs by forming isolation regions around the second mirror layers of the active VCSELs.

In another aspect, the present inventions provides method of manufacturing monolithic VCSEL and photodetector pairs by forming VCSEL layers directly on a semiconductor wafer substrate by forming first mirror layers, forming a first cladding layer on the first mirror layers, forming an active region on the first cladding layer, forming a second cladding

layer on the active region, forming second mirror layers on the second cladding layer, forming photodiodes distributed across the wafer, and defining active and inactive VCSELs by forming proton implant isolation regions around the second mirror layers of the active VCSELs.

In a still further aspect, the present invention provides a method of manufacturing monolithic VCSEL and photodetector pairs by forming VCSEL layers directly on a semiconductor wafer substrate by forming first mirror layers, forming a first cladding layer on the first mirror layers, forming an active region on the first cladding layer, forming a second cladding layer on the active region, forming second mirror layers on the second cladding layer, forming photodiodes distributed across the wafer, and defining active and inactive VCSELs by forming proton implant isolation regions 50-100 microns wide around the second mirror layers and extending vertically through the second mirror layers to the second cladding layer.

In still another aspect, the present invention provides a method of manufacturing monolithic VCSEL and photodetector pairs by forming VCSEL layers directly on a semiconductor wafer substrate by forming first mirror layers, forming a first cladding layer on the first mirror layers, forming an action region on the first cladding layer, forming a second cladding layer on the active region, forming second mirror layers on the second cladding layer, forming photodiodes distributed across the wafer, and forming VCSEL anode contacts overlapping a topmost second mirror layer and the isolation region of the active VCSELs.

In still another aspect, the present invention provides a method of manufacturing monolithic VCSEL and photodetector pairs by forming VCSEL layers directly on a semiconductor wafer substrate, then forming photodiodes distributed across the wafer directly on the semiconductor wafer substrate at discrete locations.

In still another aspect, the present invention provides a method of manufacturing monolithic VCSEL and photodetector pairs by forming VCSEL layers directly on a semiconductor



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wafer substrate by forming first mirror layers, forming a first cladding layer on the first mirror layers, forming an active region on the first cladding layer, forming a second cladding layer on the active region, forming second mirror layers on the second cladding layer, defining active regions and inactive regions by forming isolation regions in the VCSEL layers, and then forming photodiodes distributed across the wafer on the second mirror layers of inactive VCSELs.

In still another aspect, the present invention provides a method of manufacturing monolithic VCSEL and photodetector pairs by forming VCSEL layers directly on a semiconductor wafer substrate by forming first mirror layers, forming an active region on the first cladding layer, forming a second cladding layer on the active region, forming second mirror layers on the second cladding layer, forming photodiodes distributed across the wafer by forming distributed p-type layers on a topmost second mirror layer, forming an intrinsic layer on the distributed p-type layers, forming an n-type layer on the intrinsic layers, forming a photodiode cathode contact on each of the n-type layers, and forming distributed photodiode anode contacts on the topmost second mirror layer.

In another aspect, the present invention provides a method of manufacturing an integrated VCSEL and photodetector pair by forming layers of VCSEL on a semiconductor substrate, forming layers of a photodiode on a top-most layer of a first portion of the VCSEL layers, isolating a second portion of the VCSEL layers from the photodiode layers by implanting an isolation region between the first and second portions of the VCSEL layers, forming a VCSEL cathode contact connected to the semiconductor substrate, forming a VCSEL anode contact connected to the top-most VCSEL layer in the second portion, forming a photodiode cathode contact on a topmost layer of the photodiode layers, and forming a photodiode anode contact on the top-most VCSEL layer of the first portion of the VCSEL layers.

The present invention provides a method of manufacturing an integrated VCSEL and photodetector pairs by forming VCSEL layers directly on a semiconductor wafer substrate, then



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forming photodiodes distributed across the VCSEL layers at discrete locations, forming active and inactive regions of the VCSEL by forming isolation regions in the VCSEL layers, and isolating the VCSEL from the photodiodes by forming proton implant isolation regions around the photodiodes.

The present invention further provides a method of manufacturing an integrated VCSEL and photodetector pairs by forming VCSEL layers directly on a semiconductor wafer substrate; then forming photodiodes on the VCSEL at discrete locations, forming a photodiode n-type contact (cathode) on the upper most photodiode layer; and forming a photodiode p-type contact (anode) on the upper most VCSEL layer, forming a VCSEL p-type contact (anode) on the topmost VCSEL layer; forming a VCSEL n-type contact (cathode) coupled to the semiconductor substrate; forming active and inactive regions of the VCSEL by creating isolation regions in the VCSEL layers; then isolating the VCSEL layers from the photodiodes by forming proton implant isolation regions around the photodiodes.

In another aspect, the present invention provides a method of manufacturing monolithic VCSEL and photodetector pairs by forming VCSEL layers directly on a semiconductor wafer substrate, then forming an etch stop layer on the VCSEL layers, then forming photodiodes distributed across the wafer directly on the etch stop layer at discrete locations.

In still another aspect, the present invention provides a method of manufacturing monolithic VCSEL and photodetector pairs by forming VCSEL layers directly on a semiconductor wafer substrate by; forming first mirror on the substrate, forming a cladding layer on the first mirror, forming an active region on the first cladding layer, forming a second cladding layer on the active region, forming a second mirror on the second cladding layer, forming an etch stop layer on the second mirror, forming photodiodes distributed across the wafer at discrete locations by forming distributed p-type layers on a top most second mirror layer, forming an intrinsic layer on the distributed p-type layers, forming an n-type layer on the intrinsic layers, forming a photodiode n-type



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contact on each of the n-type layers, and forming distributed photodiode p-type contacts on the topmost second mirror.

In still another aspect, the present invention provides a method of manufacturing monolithic VCSEL and photodetector pairs by: forming VCSEL layers directly on a semiconductor wafer substrate; then forming an etch stop layer directly on the VCSEL; then forming photodiode layers distributed across said etch stop layer at discrete locations then forming a photodiode n-type contact (cathode) on said upper most photodiode layer; and forming a photodiode p-type contact (anode) on said upper most VCSEL layer; then forming a VCSEL p-type contact (anode) on said topmost VCSEL layer; forming a VCSEL n-type contact (cathode) coupled to said semiconductor substrate; defining active and inactive regions of the VCSEL by forming isolation regions in the VCSEL layers; then isolating said VCSEL layers from said photodiodes layers by forming proton implant isolation regions around said photodetector.

In still another aspect, the present invention provides a method of manufacturing monolithic VCSEL and photodetector pairs by: forming VCSEL layers directly on a semiconductor wafer substrate; then forming photodiode layers distributed across the VCSEL layers at discrete locations; forming a photodiode n-type contact (cathode) on said upper most photodiode layer; and forming a photodiode p-type contact (anode) on said upper most VCSEL layer; forming a VCSEL p-type contact (anode) on said topmost VCSEL layer; forming a VCSEL n-type contact (cathode) coupled to said semiconductor substrate; defining active and inactive regions of the VCSEL by forming isolation regions in the VCSEL layers; then isolating said VCSEL layers from said photodiodes layers by forming proton implant isolation regions around said photodiodes, forming interconnect metal pads on said photodiode anode and cathode and VCSEL anode; forming a dielectric matching layer on said VCSEL layers; forming vias in the dielectric matching layer for the interconnect metal pads; forming an anti-reflective coating on said photodetector.

In still another aspect, the present invention provides a method of manufacturing a monolithic VCSEL and integrated photodetector preamplifier by: forming VCSEL layers directly on a semiconductor wafer substrate; then forming an etch stop layer on the uppermost VCSEL layer; forming photodiodes distributed across said wafer directly on said VCSEL layers at discrete locations; then forming one or more transistors coupled to the photodiode.

In still another aspect, the present invention provides a method of manufacturing an integrated photodetector preamplifier by forming photodiodes directly on a semiconductor wafer substrate, and then forming one or more transistors coupled to the photodiodes.

## BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing objectives and the features of the preferred embodiments of the present invention will be better understood by those skilled in the art with reference to the following detailed description in conjunction with the accompanying drawings, wherein:

FIG. 1(a) (prior art) illustrates a fiber assembly of a typical implementation of a high-speed data transmission link using a single optoelectronic device for each half of a duplex channel;

FIG. 1(b) (prior art) illustrates an optical assembly of a typical implementation of a high-speed data transmission link using a single optoelectronic device for each half of a duplex channel;

FIG. 1(c) (prior art) illustrates a schematic view of the fiber assembly of Fig. 1(a) and the optical assembly of Fig 1(b);

FIG. 1(d) (prior art) illustrates the high-speed duplex data communications module using known precision manufactured parts to implement the transmit and receive links of a high-speed duplex data communications channel of Fig. 2;

FIG. 2 (prior art) illustrates a high-speed duplex data communications module using known precision manufactured parts



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to implement the transmit and receive links of a high-speed duplex data communications channel;

FIG. 3 illustrates a cross-section of an integrated VCSEL and an MSM photodetector in accordance with the present invention;

FIG. 4 illustrates a monolithic plan view of a preferred embodiment of the invention;

FIG. 5a illustrates a cross-section of a VCSEL and a p-i-n photodiode in accordance with the present invention;

FIG. 5(b) illustrates the orientation of the VCSEL laser diode and p-i-n photodiode as illustrated by the cross-section in FIG. 5(a);

FIG. 6(a) (prior art) illustrates a commercially available dual fiber version of a round fiber ferrule;

FIG. 6(b) (prior art) illustrates a commercially available rectangular multifiber ferrule;

FIG. 7(a) illustrates how the present invention can be packaged using conventional lead-frame technology to facilitate interface to a rectangular multifiber ferrule.

FIG. 7(b) illustrates how optical lenses can be integrated with the present invention;

FIG. 7(c) illustrates how the present invention can be implemented using butt coupling technology;

FIG. 8 illustrates how a transmit and receive pair made in accordance with the present invention can be packaged to interface with a round multifiber ferrule such as the one illustrated in Fig. 6(a);

FIG. 9 is a cross-sectional view of a conventional VCSEL structure deposited upon a semiconductor substrate having a p-i-n photodiode formed on the VCSEL in accordance with an exemplary embodiment of the present invention;

FIG. 10(a) is a cross-section of a conventional VCSEL structure deposited upon a semiconductor substrate with a p-i-n photodiode formed on the VCSEL having an integrated n-ohmic ring formed on the photodiode in accordance with an exemplary embodiment of the present invention;

FIG. 10(b) is a top view demonstrating the integration of a p-i-n photodiode mesa on a VCSEL with an n-ohmic ring



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formed on the photodiode in accordance with an exemplary embodiment of the present invention;

FIG. 11(a) is a cross-section of a VCSEL with an integrated p-i-n photodiode mesa, with an n-ohmic ring formed on the photodiode in accordance with an exemplary embodiment of the present invention;

FIG. 11(b) is a top view demonstrating the integration of the p-i-n photodiode mesa on a VCSEL, with an n-ohmic ring formed on the photodiode mesa in accordance with an exemplary embodiment of the present invention;

FIG. 12(a) is a cross-section of a VCSEL and associated p-ohmics, integrated with a p-i-n photodiode mesa, having a n-ohmic ring formed on the mesa and a p-ohmic ring formed on the photodiode mesa, in accordance with an exemplary embodiment of the present invention;

FIG. 12(b) is a top view demonstrating the integration of the p-i-n photodiode mesa on a VCSEL, with n-ohmic and p-ohmic rings in accordance with an exemplary embodiment of the present invention;

FIG. 13(a) is a cross-section demonstrating the integration of proton implant isolation regions in accordance with an exemplary embodiment of the present invention;

FIG. 13(b) is a top view demonstrating the integration of the p-i-n photodiode mesa on a VCSEL, with proton implant isolation regions in accordance with an exemplary embodiment of the present invention;

FIG. 14(a) is a cross-sectional view demonstrating the integration of Ohm vias into the dielectric layer for the photodiode and VCSEL in accordance with an exemplary embodiment of the present invention;

FIG. 14(b) is a top view demonstrating the integration Ohm vias into the dielectric layer for the photodiode and VCSEL in accordance with an exemplary embodiment of the present invention;

FIG. 15(a) is a cross-section demonstrating the integration of interconnect metal pads for the VCSEL and photodiode ohmic contacts in accordance with an exemplary embodiment of the present invention;



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FIG. 15(b) is a top view demonstrating the integration of interconnect metal pads for the VCSEL and photodiode ohmic contacts in accordance with an exemplary embodiment of the present invention;

FIG. 16(a) is a cross-section demonstrating the integration of a VCSEL dielectric matching layer with photodiode via in accordance with an exemplary embodiment of the present invention;

FIG. 16(b) is a top view demonstrating the integration of a VCSEL dielectric matching layer with photodiode via in accordance with an exemplary embodiment of the present invention;

FIG. 17(a) is a cross-section demonstrating the integration of a one quarter wavelength anti-reflective coating on the photodiode in accordance with an exemplary embodiment of the present invention;

FIG. 17(b) is a top view demonstrating the integration of a one quarter wavelength anti-reflective coating on the photodiode in accordance with an exemplary embodiment of the present invention;

FIG. 18(a) is a cross-section demonstrating the mask layout to produce the present invention in accordance with an exemplary embodiment of the present invention;

FIG. 18(b) is a top view demonstrating the mask layout to produce the present invention in accordance with an exemplary embodiment of the present invention;

FIG. 19 is a perspective view demonstrating the integration of an FET with a p-i-n photodetector to form an integrated photodetector and preamplifier in accordance with an exemplary embodiment of the present invention; and

FIG. 20 is a top view of a transmit / receive / amplifier circuit integrated onto one wafer which utilizes low cost wire bond / lead frame technology in accordance with an exemplary embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

The present invention generally pertains to a monolithic semiconductor device having a VCSEL integrated with a



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photodetector on the same substrate, the VCSEL and photodetector to be operated independently as a transmit and receive device respectively. The VCSEL and photodetector are physically situated in close enough proximity to permit packaging of one or more pairs of the VCSEL and photodetector such that they may be coupled to multifiber ferrules having fiber spacings on the order of 250 microns or less. The present invention also includes a method of manufacturing the independently operated VCSEL and photodetector, as well as the packaging and coupling of one or more pairs of the integrated VCSEL and photodetector and their coupling to multifiber ferrules.

A first preferred embodiment of the invention is now discussed in detail in conjunction with FIGS. 3 and 4. As shown in FIG. 3, a VCSEL and a metal-semiconductor-metal (MSM) photodetector are integrated on the same semi-insulating GaAs substrate. The conductance of the semi-insulating substrate is typically between about $10^{-12}$ and $10^{-5}$ ohm-cm. The VCSEL is built on top of the substrate beginning with an n- layer 68, upon which an n+ layer 70 is grown which forms the cathode of the VCSEL.

A first mirror 78 is formed on layer 70, which is preferably an epitaxially formed distributed Bragg reflector (DBR) which comprises a plurality of alternating semiconductor layers having high and low indices of refraction, with each layer having a thickness of $\lambda/4n$, where $\lambda$ is the wavelength of the optical radiation emitted from the laser and n is the index of refraction of the layer. The semiconductor layers are doped to achieve n-type conductivity. A quantum well (QW) active region 74 is formed between a first spacer 73 and a second spacer 75, with first spacer 73 formed on the top layer of the first mirror. Active region 74 has at least one QW layer.

A second mirror 76 is formed on second spacer 75 and is preferably an epitaxially grown DBR which is comprised of a plurality of alternating semiconductor layers having high and low indices of refraction, with each layer having a thickness of $\lambda/4n$, where $\lambda$ is the wavelength of the optical radiation



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emitted from the laser and n is the index of refraction of the layer. The second mirror 76 is doped to achieve a p-type conductivity. An isolation implant 80 is formed around the second mirror 76, and preferably extends to a depth just inside spacer 75. A mesa region is then etched around the outside of the VCSEL 89 to a depth which exposes the cathode layer 70. A cathode contact 72 is then formed on the exposed surface of cathode layer 70, and an anode contact 82 is formed which overlaps the surface of isolation implant region 80 and the topmost layer of second mirror 76, and which further defines an aperture 88 which comprises a portion of the surface of the top-most layer of second mirror 76. Radiation 84 is emitted through aperture 88.

The MSM photodetector 62 is formed on the surface of the semi-insulating substrate 60 as two non-electrically coupled metal patterns 62 and 64, each having fingers which are interdigitated with one another. When one or both of the patterns is biased to some voltage, carriers generated by received light are swept to the anodes of the two diodes by the applied electric field. Because the MSM operates without conducting any current through the substrate 60, there is virtually no electrical crosstalk or leakage between the VCSEL 89 and the MSM photodetector 62. Thus, the VCSEL 89 can emit radiation 84 from aperture 88 based on digital data to be transmitted while MSM photodetector 62 can receive radiation 86 in which is encoded digital data received from a remote data source. To achieve even better isolation, an isolation region 80 can be formed preferably by proton implant between VCSEL 89 and MSM photodetector 62.

FIG. 4 illustrates a plan view of the device which is shown as a cross-section in FIG. 3. For clarity, corresponding structures will be indicated by identical index numbers. The cathode layer 70 and its metal cathode contact 72 of the VCSEL are extended to the boundary of substrate 60 which is furthest away from MSM photodetector 86. Bond wire 71 can then be used to connect cathode contact 72 to a bond pad of, for example, a lead frame. The VCSEL anode contact 82 is brought to the same substrate boundary by bond wire 77,

metal extender 79 and bond wire 69. Metal patterns 66 and 64, which form the anode and anode terminals of MSM photodetector 62, are also bonded to the leads of whatever form of packaging is used. One of the metal patterns is typically coupled to a bias voltage while the other is coupled to ground or a different bias voltage. An anti-reflection coating can be employed on the MSM to increase optical efficiency.

A second preferred embodiment is disclosed in FIG. 5a. For convenience and clarity, like structures will be denoted by the same index numbers as in previous figures. This particular embodiment is preferred because it can be implemented using more standard VCSEL manufacturing processes. A first mirror 78 is formed on a standard semiconductor GaAs substrate 79. The first mirror is preferably a semiconductor DBR comprising twenty to thirty periods of AlAs/AlGaAs layers. Each of the layers has a thickness of $\lambda/(4n)$ and is doped to have n-type conductivity. A first spacer or cladding layer 73 is then formed on first mirror 78, which is either undoped or very lightly doped. An active region 74 is then formed on the first spacer 73 which comprises at least one GaAs QW layer. A second mirror 76 is then formed on top of a second undoped or very lightly doped spacer or cladding layer 75. The second mirror 76 again preferably consists of alternating layers of AlAs/AlGaAs layers, each being $\lambda/(4n)$ thick. Second mirror 76 is doped to have p-type conductivity. On top of second mirror 76 is formed a thin etch-stop layer 93, which has a significantly higher ratio of Al to Ga, about 9 to 1 or greater. On top of the etch-stop layer 93, an extended p-type layer 100 of AlGaAs is formed. On top of p-type layer 100 is formed an intrinsic layer (i) 102 of undoped GaAs. Finally, an n-type layer 104 is formed on top of intrinsic layer 102.

The structure is then etched in those areas where a VCSEL is to be formed, and not etched where a p-i-n photodiode is to be formed. The etch strips away the n-type layer 104 and intrinsic layer 102 and continues into p-type layer 100 until the etch-stop layer 93 is detected. The etching process is terminated so that the etch-stop layer is etched away and an appropriately thick top layer of second mirror 76 is exposed.



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Those of skill in the art will recognize that there are other well-known techniques by which the endpoint of an etching process may be detected to end the etching process at the appropriate time and which are intended to be within the scope of the present invention.

A proton isolation implant is performed to create isolation region 80 between VCSEL 92 and p-i-n photodiode 90. The implant region 80 typically achieves a depth which extends just inside spacer layer 75 and has a width preferably between about 50 and 100 microns. A circular metal contact 82 is then formed on the top of mirror 76 and which overlaps slightly implant region 80. Contact 82 provides access to the anode of VCSEL 92. A contact 81 is then formed on the back side of substrate 79 and serves as the cathode terminal of VCSEL 92. Contacts 94 are preferably formed on both sides of p-i-n photodiode 90 which provide electrical access to the anode of p-i-n photodiode 90 as well as to the anode of the VCSEL 91 which underlies p-i-n photodiode 90. Finally, contact 96 is formed on n-type layer 104 to form the cathode of p-i-n in photodiode 90. An anti-reflection coating preferably having a thickness of about one quarter wavelength is applied to photo-receiving surface 101.

A simplified schematic of the structure of FIG. 5a is shown in FIG. 5b. VCSEL 92 is operated with forward bias between anode terminal 82 and cathode terminal 98 to produce radiation 84 having a wavelength of $\lambda$. In an exemplary embodiment p-i-n photodiode 90 is operated with reverse bias between cathode contact 96 and anode contacts 94. Moreover, anode contacts 94 are shorted to substrate contact 98 to ensure that VCSEL 91 will not become forward biased and emit light. Thus, VCSEL 92 can be operated to emit light encoded with data to be transmitted to a remote receiver employing a similar structure, and p-i-n photodiode 90 can operate to receive radiation 86 which is encoded with data received from the same remote terminal.

Those of skill in the art will recognize that one of the many advantages of the second preferred embodiment of FIG. 5a is that a typical process used to create arrays of VCSELs,

including the isolation implant commonly used to separate the individual VCSELs of the array, can be used to create arrays of VCSEL/p-i-n photodiode pairs. The additional steps required to build the p-i-n photodiode on top of the VCSEL process are negligible in cost. Moreover, the difference in the thickness of the two devices is also negligible for purposes of facilitating near-field coupling of the devices to fibers to eliminate the need for optics. Additionally, due to the underlying second mirror of inoperable VCSEL 91, any light not absorbed by the intrinsic layer 102 of p-i-n photodiode 90 will be reflected back into intrinsic layer 102, thus having a second chance to be absorbed. Finally, the thicker the intrinsic layer, the lower the capacitance of the p-i-n diode (the faster its operation) and the better its optical efficiency.

FIG. 6(a) illustrates how the commonly used single fiber round ferrule can be implemented using two or more fibers. Such fibers are now currently available from Siecor as prototypes. The cylindrical ferrule 110 has the same dimensions (i.e., 2.5 mm) as those ferrules commonly used with only one fiber. Thus, one fiber 112 can be used for transmitting data as coupled to a VCSEL while fiber 114 can be used to receive data from a remote transmitter as coupled to a photodetector.

FIG. 6(b) illustrates a commonly available rectangular ferrule which can have eight or more fibers 122, and which has guides 120 for receiving alignment pins. Rectangular ferrule 116 typically has a polished face 118 for coupling to an array of transmitting VCSELs. This rectangular ferrule 116 can be easily adapted to devices made in accordance with the present invention, such that each pair of fibers 122 can be aligned with a pair of integrated VCSEL/photodetectors.

FIG. 7(a) illustrates how a single VCSEL/photodetector pair could be packaged using standard lead-frame technology to be interfaced to a rectangular multifiber ferrule such as the one illustrated in Fig. 6(b). Integrated transmit/receive chip 130 can be epoxied to lead frame 128 and then bonded to bond pads 141 via bond wires 143. If optics are required,



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lenses 138 and 136 can be formed over VCSEL 89, 92 and photodetector 62,90 respectively, either using materials which are formed over chip 130 during the manufacturing of chip 130 or such optics can be integrated within the surface of the plastic encapsulation formed by the package. Lead frame 128 can also have guide pins 140 to be used in conjunction with a rectangular ferrule such as the one shown in FIG. 6(b). FIG. 7(b) shows a side view of FIG. 7a to illustrate the use of optics over photodetector 62, 90 and VCSEL 89, 92.

FIG. 7(c) illustrates how lead frame 128 can be butt coupled to a rectangular ferrule 150 containing two fibers 124 and 126. If distance 160 is fairly precisely known, and distance 147 between fibers 124 and 126 is fairly precise, a fairly accurate alignment can be achieved between fibers 124 and 126 and VCSEL 89, 92 and photodetector 62, 90 because the distance between VCSEL 89, 92 and photodetector 62, 90 are fairly precise based on the photo-optical alignment process used in manufacturing the integrated semiconductor 130. Thus, a fairly accurate positioning of the chip 130 with respect to the lead frame 128 during packaging will provide a reasonably accurate passive alignment. Of course, fine alignment can be achieved using well-known active alignment techniques. A further advantage of the coupling technique shown in FIG. 8 is that no optics must be interposed between package 146 and ferrule 150 if the coupling distance 152 is close enough. Of course, a flat transmissive surface 148 can be easily achieved on package 146.

Fig. 8 illustrates a lead-frame package which can be used to interface with a round multifiber ferrule such as the two-fiber ferrule of Fig. 6(a). Barrel 127 is designed to precisely mate with the round ferrule of Fig. 6(b)

An alternate embodiment of the present invention relates to a monolithic semiconductor device having a VCSEL integrated with a photodetector and preamplifier on the same substrate, the VCSEL and photodetector to be operated independently as a transmit and receive device respectively. The present invention also includes a method of manufacturing the



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independently operated VCSEL and photodetector with an integrated FET preamplifier.

This alternate embodiment of the present invention is implemented using standard VCSEL manufacturing techniques. The conventional VCSEL portion 200 of this alternative embodiment of the present invention as shown in FIG. 9 includes a substrate 201, a first or lower mirror 202, an optical cavity 203, and a second or upper mirror 204. The substrate 201 is made of gallium arsenide (GaAs) or any other suitable material. The first and second mirrors 202, 204 are comprised of multilayered distributed Bragg reflectors, (DBRs) as is conventional in the art.

In this alternate embodiment, aluminum gallium arsenide (AlGaAs) and aluminum arsenide (AlAs), with varying concentrations of aluminum and gallium are used to fabricate the upper and lower mirrors 202, 204. The optical thickness of each mirror layer is typically designed to be a quarter wavelength of the emitted light of the laser where the optical thickness is given by the product of the physical thickness and the index of refraction.

The conventional optical cavity 203 includes an active region surrounded by first and second cladding regions. The first and second cladding regions are made of AlGaAs in the exemplary embodiment. In the active region 203, at least one quantum well made of GaAs is disposed on adjacent barrier layers made of $Al_{0.25}Ga_{0.75}As$. As is generally understood in the art, the number of and materials forming the quantum wells and surrounding barrier layers can be varied depending on the design.

In this alternate embodiment, the first or lower mirror 202 is doped to n-type conductivity while the second or upper mirror 204 is doped to have p-type conductivity. The p-type second mirror 204 is capped by a layer of GaAs 205 which is approximately 100 Angstroms thick.

A thin etch stop layer 206, consisting of approximately 100-200 Angstroms of AlAs is deposited on the p-type mirror cap 205. On top of the etch stop layer 206 an additional intrinsic i-type layer 207 is deposited, consisting of an



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absorbing GaAs material. The p-doping extends through the AlAs etch stop layer 206 into the i-type region 207 to avoid heterostructural barriers and band problems. Finally an n-type layer 208 of $Al_{0.25}Ga_{0.75}As$ is formed on top of the intrinsic layer 207 with a thin GaAs cap.

This alternate embodiment minimizes photodetector pulse deformation due to minority carrier drift within the p-i-n photodiode 211 structure. The GaAs i-type layer 207 absorbs light at 850 nanometer whereas the n-type layer 208 is non absorbent at this wavelength. Therefore photon absorption is confined to the i-type layer 207 wherein the photons are removed by the reverse electric fields. If photocarrier absorption occurs in the n-type region 208 or the p-type region 204 on either side of the i-type region 207, minority photons are absorbed, and minority carriers are generated. There is no electric field within the background doped n-type region 208 or p-type region 204 to remove these minority carriers. These minority carriers must then drift and diffuse through normal diffusion processes eventually being swept into the i-type region 207. These diffusion processes may deform the shape of the photodetector output pulse by creating a long time tail to the trailing edge of the pulse.

As shown in the cross-sectional view of FIG. 10(a) circular n-ohmic 209 is formed to make contact with the photodiode n-type region 208 while the surface is planar. FIG. 10 (b) is a top view of the ring contact 209 deposited on the n-type region 208. The structure is then masked and etched in those areas where the transmit VCSEL 210 is to be formed, FIG. 11(a), and not etched where the photodetector 211 is to be formed. There are well known techniques by which the endpoint of an etching process may be detected to end the etching process at the appropriate time. A disadvantage of these etch techniques is the non uniformity of etch rates over the surface of the wafer. Etch rate variation is created by fluid motion, surface effects, light effects and various other phenomenon. This variation in etch rate results in imperfections in the surface finish of the VCSEL and added complexity in the manufacturing control process.

In response to the drawbacks of the prior art, this alternate embodiment of the present invention incorporates an AlAs etch stop layer 206 to facilitate selective etching of the upper n-type region 208 and i-type region 207. The n-type region 208 and i-type region 207 are etched using a known combination of citric acid with a high percentage of peroxide. When the etch solution reaches the etch stop layer 206 the peroxide interacts with the AlAs to form an oxide surface. The citric acid solution is not sufficiently strong to remove the aluminum oxides so that the oxide surface in effect inhibits or stops the etch. This selective etch technique removes the time critical aspect of conventional etch techniques and greatly simplifies the manufacturing process. From a timing standpoint, the device can now be over etched assuring the uniform removal of the upper n-type region 208 and i-type region 207 over the entire surface of the VCSEL 210.

Next, the etch stop layer 206 is removed using an alternate etch solution which will not etch the GaAs cap 205 on the upper p-type mirrors 204. Preferably, a solution of hydrochloric acid, with 10 percent water is used to remove the etch stop layer. As is shown in FIG. 11(a), a photodetector mesa 211, with a slight undercut in the AlAs etch stop layer 206, is closely coupled to a surrounding VCSEL 210. The present invention achieves the required device uniformity without implementation of rigorous process controls required by other known techniques. FIG. 11(b) is a top view of the photodetector mesa 211 with integrated n-type contact 209.

Referring to FIG. 12(a) in this alternate embodiment of the present invention, a metal contact 212 is formed on the bottom of the substrate 201 and serves as the cathode 212 terminal of the VCSEL 210. The contact metalization forming the n-ohmic contact 212 on the bottom of the substrate 201 may be, for example, eutectic gold germanium deposited by electron beam evaporation or sputtering. Additionally, p-ohmic contacts 213, 214, and 215 are then formed on the top of the second or upper mirror 204. As shown in the top view of FIG.



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12(b) a circular metal contact 213 is formed on the outside of the photodetector 211, while at the same time circular contacts 214, 215 are formed on the upper most surface 205 of the VCSEL 210. The top contact metalization forming p-ohmic contacts 213, 214, and 215 may be, for example, gold with 2% beryllium added or a layered structure of titanium/platinum/gold, preferably deposited by electron beam evaporation.

In this alternate embodiment of the present invention a proton implant forms an isolation region 216 between the VCSEL 210 and the photodetector 211 (FIG 13(a)). The standard proton implantation process that is used for current constriction within the conventional VCSEL 217, 218, may be used to create a highly insulative ring 216 (top view FIG. 13(b)) around the photodetector 211 thereby isolating the VCSEL 210 structure from the photodetector 211. In the top view of FIG. 13(b) it can be seen that a guard band 216 of highly insulative material is formed between the n-type contact 209 and the p-ohmic contact 213 of the photodetector 211.

This alternate embodiment has several advantages over prior art isolation mechanisms. For example, the operating time constants of a p-i-n photodetector 211 are inversely proportional to the capacitance of the device. The capacitance of the device is directly proportional to the surface area of the device. As is shown in the top view of FIG. 13(b) the highly insulative proton implant region 216 decreases the active surface area of the device, thereby reducing the capacitance of the device and increasing the maximum operating speed of the photodetector 211.

The photodetector proton implant region 216 also increases the sensitivity of the photodetector 211 by eliminating leakage paths through which current could otherwise flow between the VCSEL 210 and the photodetector 211. Typical photodetectors must receive very low optical power levels so that most photodetectors are low current devices. Therefore, a relatively small amplitude leakage current can severely degrade the sensitivity of the

photodetector 211 by introducing excess noise into the receiver system as well as unacceptably changing the performance of the p-i-n photodetector 211 over time. The proton implant region 216 effectively stops electrical conduction at the edge of the highly resistive proton implant region 216 between the p-type contact 213 and n-type contact 209, thereby eliminating all leakage paths.

Current constriction within the conventional VCSEL 210 is provided by using proton implant regions 217 and 218 to creating active and inactive regions of the VCSEL. The VCSEL proton implant regions 217 and 218 convert the upper mirror DBR 204 into areas of high resistivity around the active VCSEL 210 device. The VCSEL proton implant regions 217, 218 typically achieve depths which extend just inside the spacer layer. In this alternate embodiment of the present invention, the thicknesses of the photodetector 211 i-type region 207 and n-type region 208 are chosen so that the implant depth that is appropriate for the VCSEL 210 is also appropriate for the photodetector 211.

The forced commonality between the proton implant region 217, 218 of the VCSEL 210 and the proton implant region 216 of the photodetector 211 allows for a more efficient manufacturing process. The process sequence that was appropriate for the VCSEL 210, with a modified mask layout is also appropriate for the photodetector 211. Therefore, all proton implantations 216, 217 and 218 can be performed in a single process step with a single mask layout.

Referring to FIG. 13(a) the photodetector proton implant region 216 completely transects the n-type region 207 and penetrates into the i-type region 208. However, the proton implant region 216 does not penetrate the p-type region 204 providing a conduction path to the p-type contact 213, to maintain the required continuity between the n-type contact 209 and p-type contact 213 of the photodetector 211. In this alternate embodiment of the present invention, the n-type region 208 is approximately 3000 Angstroms thick, the absorbing i-type region 207 is approximately 2.5 microns in thickness and the area where the p-type region extends over

into the i-type region 207 is approximately 2000 Angstroms so that the entire thickness of the photodetector mesa 211 is approximately 3 microns.

A dielectric protective layer 219 (FIG 14(a)) is deposited to protect the outermost surface 205 of the VCSEL 210 and the photodetector 211. Silicon nitride is preferably used for the dielectric protective layer 219. Therefore, vias must be etched into the dielectric protective layer 219 to provide access to the p-type contacts 214 and 215 of the VCSEL 210, as well as the n-type contact 209 and p-type contact 213 of the photodetector 211.

A thicker inter-connect metal 220 and 221 is deposited on the photodetector n-type contact 209 and p-type contact 213 respectively, as shown in the cross section of FIG. 15(a). Also, a thicker inter-connect metal 222 and 223 is deposited on the p-type contacts 214 and 215 of VCSEL 210. The inter-connect metal deposits 220-223, provide a low resistance, good electrical conductor contact for wire bonding, probing, etc. The metal deposits used for the n-type and p-type contacts 209, 213-215, are generally very thin and relatively high resistance and are designed for transitioning from metal to semiconductors through ohmic contacts that have a non-barrier between the work function of the two materials. Therefore, the inter-connect metal is chosen to provide low contact resistance for current flow. FIG. 15(b) shows a top view of the interconnect metal 220 and 221 integrated with the photodetector 211.

In an alternate embodiment of the present invention, a dielectric phase shifting layer 224, is preferably disposed on the conventional VCSEL structure 210 (FIG. 16(a)). The dielectric phase shifting layers 224 increase the total transmission out of the VCSEL 210 as is disclosed in U.S. Patent Application "VERTICAL CAVITY SURFACE EMITTING CONSISTENT SLOPE EFFICIENCIES", Application No. 09/237,580; the contents of which are incorporated herein by reference. In this alternate embodiment of the present invention, deposition of the dielectric phase shifting layers 224 is halted prior to the deposition of the last quarter optical

wavelength of the material. The dielectric phase shifting layers 224 are then completely etched off the photodetector 211 as shown in FIG. 16(a). Next a quarter optical wavelength of the dielectric material 225 is deposited over the VCSEL 210 to complete it's mirror as well as on the photodetector 211 to create an anti-reflective coating(FIG 17(a)). The quarter optical wavelength material is preferably silicon nitride as is known in the art.

When the anti-reflective coating 225 of silicon nitride is applied to the photodetector 211 n-type region, in conjunction with the p-type region of the upper mirror 204, which underlies the photodiode 211, a high degree of efficiency is achieved. The anti-reflective coating 225 increases the transmission of incoming light into the p-i-n photodiode structure 211. Additionally, any light that does not get absorbed in the i-type region 207 is reflected off the upper mirror 204 of the VCSEL 210 and is absorbed as it propagates back through the i-type region 207 for the second time. Because of this double pass mechanism the absorption characteristics of the i-type region 207 is twice what it otherwise would be, providing excellent quantum efficiencies, and very high response at gigabit speeds.

In an alternate embodiment of the present invention, a variable tuning layer is deposited on the outer surface of the dielectric phase shifting layer 224. The variable tuning layer facilitates predictable adjustment of the optical efficiency of the laser during fabrication to achieve lasers with substantially similar slopes on a wafer to wafer basis. The manufacture and use of a variable tuning layer is disclosed in U.S. Provisional Patent Application "ENCAPSULATED LASER WITH CONTROLLED SLOPE EFFICIENCY", Application No. 60/125,916, filed on March 24, 1999, the contents of which are hereby incorporated by reference. In this alternate embodiment the initial VCSELs are tested by any conventional technique, preferably on a representative sample, to determine characteristics of the initial VCSELs, such as the slope efficiency distribution.



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The thickness of the variable thickness dielectric layer required to tune the slope efficiency distribution to within the target specification is calculated. This calculated thickness is then used to interrupt the prior layer deposition, etch the dielectric layers off the photodetector and then deposit the remaining phase shifting layer thickness and tuning layer. If the calculated thickness of the dielectric tuning layers was 1/8 of a wavelength, the phase shifting layer deposition would be interrupted at 1/8 of a wavelength less complete, the dielectric would be etched off the photodetector 211 and the remaining phase shifting layer dielectric and tuning layer thickness would be deposited. The combination of the two materials would then be a quarter wavelength to complete the design of the anti-reflective coating 225 for the photodetector 211.

FIG. 18(a) is a cross section of the present invention, including the mask layout, with approximate dimensions, for manufacturing this alternate embodiment of the present invention. Also shown are the p-i-n laser 226, a parasitic VCSEL 227 underneath the photodetector 211 and the p-i-n photo diode 228. The p-type contact 213 of the p-i-n photodetector 211 may be coupled to ground so that the parasitic VCSEL 227 structure which lies underneath the p-i-n photodetector 211 is never turned on and other bipolar parasitic effects are avoided.

Referring to Fig. 19, in an alternate embodiment of the present invention, an epitaxial n-i-p structure, 230, 231 and 232 respectively, along with highly insulative proton implant regions 233 and 234, are used to integrate a FET onto the photodetector 211 to create an integrated detector pre-amplifier. FIG. 19 shows a perspective view of the integrated detector pre-amplifier 229. Metal deposits are formed on the outer most surface 235 of the photodetector 211 to form the source 236, gate 237 and drain 238 on an n-type channel of a typical transistor structure. In this alternate embodiment the proton implant regions 233 and 234 intersect the back of the source 236, gate 237 and drain 238 as well as the lower surface of the source 237 and drain 238. In this way the



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proton implant regions 233 and 234 form an isolated conductive region 239 or well, within a highly insulative field formed by the proton implantations 233 and 234.

The width of the conductive region is arbitrary and can be tailored to produce a predetermined transistor. To achieve gigabit data communication rates, the length of the gate 237, which is the critical transistor design parameter, can be on the order of one micron. The GaAs layer upon which the metal layers are deposited is a highly conductive material also with very good frequency response. A one micron metal deposit is well within reasonable process control technology known in the art. The gate 237, is typically a layered structure of titanium, platinum and gold which can be deposited by any suitable method known in the art, such as by sputtering or electron beam vaporization. The thicknesses of the metal deposit is typically 500A, 1000A, 3000A for the Ti, Pt, Au respectively as is well known in the GaAs transistor art.

The source 236 and the drain 238 are typically layered structures of Nickel with Gold on Gold Germanium, n- ohmics. The nickel acts as a barrier to prohibit the gold from interfusing with the gold germanium and changing the eutectics of the gold germanium. In the preferred embodiment of the present invention a ratio of 88 percent gold to 12 percent germanium is used to form a eutectic which has a phase melting point near 360°C to make a good ohmic contact.

This alternate embodiment of the present invention is less susceptible to receiver noise, crosstalk, etc. than conventional photodetector designs. The coupled FET and photodetector create an integrated detector pre-amp such that the output signal of the photo detector is amplified by the FET and converted from a current signal to a voltage signal. Therefore, a relatively large voltage single is being modulated rather than a low level current signal.

In conventional SMFF transceiver designs, the photodetector is susceptible to crosstalk from the high drive currents of the VCSEL as well as receiver noise and other degradations to receiver sensitivity. In this alternate embodiment the photo detector is integrated on the same mesa



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as the amplifying transistor circuitry so that the output signals of the integrated detector pre-amp are no longer very low current signals that are sensitive to noise, crosstalk and the like but are more stable amplified voltage signals.

The signal to noise ratio of conventional optical receiver is limited by the front end noise. Currently, front end receivers which interface with conventional high speed photodetectors, utilize GaAs technology because high speed, highly sensitive, low noise performance is required to accurately amplify the low level current output of the conventional photodetector.

In this embodiment of the present invention, the low noise circuitry is integrated with the photodetector on the same wafer. In this embodiment the integrated amplifier is realized with relatively simple transistor circuits. The transistor circuits are readily implemented with techniques known in the art without resorting to the highly integrated processes required for GaAs integrated circuits. These relatively simple transistor circuits are generally bond pad limited. Coupling the photodetector to the transistors eliminates capacitance and bond wire inductance which otherwise limit system performance. The amplified output signal of the integrated detector preamplifier, which is no longer susceptible to noise and other degradations, allows the front end receiver amplifier to be implemented with CMOS integrated circuit technology that is comparably a much lower cost than the more complex GaAs integrated circuit technology required for conventional photodetectors.

In an alternate embodiment of the present invention the integrated detector preamplifier is coupled with VCSEL transmit technology to provide a closely spaced transmit 241, receive 242, amplifier 243 circuit 240 on a single integrated circuit chip as shown in the top view of FIG. 20. Conventional transceiver designs require closely coupled high speed integrated circuitry for reduced delay times. The high speed integrated circuitry generally considerable power dissipation and heat to the packaged system. The integrated device with the wire bonds 244 coming off the VCSEL and

integrated receive amplifier can then be mounted onto lead frames 245, which is a low cost packaging technology.

The transmit/receive amplifier circuit embodiment of the present invention has the added benefit of being relatively easy to manufacture. This alternate embodiment of the present invention is implemented using standard VCSEL manufacturing techniques and process sequences as previously described. The AlAs etch stop layer would be deposited on a conventional VCSEL. On top of the etch stop layer an additional intrinsic i-type layer is deposited, consisting of an absorbing GaAs material. The p-doping extends through the AlAs etch stop layer into the i-type region to avoid heterostructural barriers and band problems. Finally an n-type layer of $Al_{0.25}Ga_{0.75}As$ is formed on top of the intrinsic layer with a thin GaAs cap.

Next the transistor, source 236, gate 237 and drain 238 and n-type contacts 209 for the photodetector 211 are deposited preferably by electron beam evaporation. In this alternate embodiment the source 236 and drain 238 contacts are the same n-type contact that was used for the photodetector 209. Next selective etching to expose the VCSEL and form the integrated photodetector preamplifier mesa is performed. The p-type contacts 213, 214 and 215 may then be deposited, preferably by electron beam evaporation, followed by a proton implantation for the transistor 233 & 234, photodetector guard ring 216 and VCSEL 217.

As previously described, dielectric layers are next deposited. Dielectric material is deposited on the transistor to decrease degradation and increase the operating life of the device. Silicon nitride is the preferred dielectric material. Next vias are etched into the dielectric layers to allow the interconnect metal 220, 221, 222 and 223 to be deposited. Finally an anti-reflective coating 225 is applied to the photodetector 211.

It should be noted that a number of variations to the inventions described above will be apparent to those skilled in the art. For example, the p-i-n photodiode can be deposited directly on a semiconductor substrate along with the



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proton implant guard ring to create a high performance photodetector. In this alternate embodiment the device capacitance can be matched exactly with the mask design and the reverse bias to achieve complete depletion of the i-type region as is required for high speed performance. In addition, the above photodetector can be integrated with the FET to form a high speed integrated detector preamplifier. The VCSEL could include a power monitoring photodetector, wherein the monitoring photodetector may be below the VCSEL or on the side or in another location within the package to provide controlled monitoring and feedback.

Those of skill in the art will recognize that the exact order in which the process steps take place, as well as the particular material system used, are irrelevant to the patentability of the present invention. For example, one material system might include a GaAs substrate, GaAs quantum wells, DBR layers of AlAs and AlGaAs, and an intrinsic layer of GaAs. The p and n layers of the p-i-n would also be made of AlGaAs. Other known material systems may be used to produce different wavelengths of emitted radiation and the particular dimensions of the integrated devices may be changed to suit particular transmission modes or packaging requirements. Moreover, although it is desirable that the photolithographically defined spacings between the transmit and receive pairs are preferably small, of course larger spacings can be easily accommodated by the present invention.



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CLAIMS

1. A method of manufacturing monolithic VCSEL and photodetector pairs, said method comprising the steps of:

forming VCSEL layers directly on a semiconductor wafer substrate;

forming photodetectors distributed across said wafer directly on said VCSEL layers at discrete locations;

defining active and inactive regions of the VCSEL by forming isolation regions in the VCSEL layers; and

isolating said VCSEL layers from said photodetectors layers by forming proton implant isolation regions around said photodetectors.

2. The method of claim 1 further comprising the step of:

prohibiting operation of said inactive VCSELs by short circuiting said semiconductor wafer substrate to said photodiode anode contact to ensure that said active VCSELs will not become forward biased.

3. A method of manufacturing monolithic VCSEL and photodetector pairs, said method comprising the steps of:

forming VCSEL layers directly on a first side of a semiconductor wafer substrate;

forming photodiode layers distributed across said VCSEL layers at discrete locations;

forming a photodiode n-type contact (cathode) on an uppermost photodiode layer;

forming a photodiode p-type contact (anode) on an uppermost VCSEL layer;

forming a VCSEL p-type contact (anode) on an uppermost VCSEL layer;

forming a VCSEL n-type contact (cathode) on a second side of said semiconductor substrate;

defining active and inactive regions of the VCSEL by forming isolation regions in the VCSEL layers; and

isolating said VCSEL layers from said photodiodes layers by forming proton implant isolation regions around said photodiodes.



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4. The method of claim 3 wherein the step of forming VCSEL layers directly on a semiconductor wafer substrate further comprises:

forming first mirror layers on a semiconductor wafer;

forming a first cladding layer on said first mirror layer;

forming an active region on said first cladding layer;

forming a second cladding layer on said active region; and

forming second mirror layers on said second cladding layer.

5. The method of claim 3 wherein the step of forming said photodiode layers directly on said VCSEL layers further comprises:

forming distributed p-type layers on said VCSEL layers;

forming an intrinsic layer on said distributed p-type layers; and

forming an n-type layer on said intrinsic layers.

6. The method of claim 3 wherein the step of forming photodiode layers directly on said VCSEL layers at discrete locations further comprises:

forming said photodiode layers distributed across said VCSEL layers; and

selectively removing said photodiode layers from said VCSEL layers at discrete locations.

7. The method of claim 3 further comprising the step of:

prohibiting operation of said inactive VCSELs by short circuiting said semiconductor wafer substrate to said photodiode anode contact to ensure that said active VCSELs will not become forward biased.

8. A method of manufacturing monolithic VCSEL and photodetector pairs, said method comprising the steps of:

forming VCSEL layers directly on a first side of a semiconductor wafer substrate;

forming an etch stop layer directly on said VCSEL layers;

forming photodiode layers distributed across said etch stop layer at discrete locations;

forming a photodiode n-type contact (cathode) on an uppermost photodiode layer;

forming a photodiode p-type contact (anode) on an uppermost VCSEL layer;

forming a VCSEL p-type contact (anode) on an uppermost VCSEL layer;

forming a VCSEL n-type contact (cathode) on a second side of said semiconductor substrate;

defining active and inactive regions of the VCSEL by forming isolation regions in the VCSEL layers; and

isolating said VCSEL layers from said photodiodes layers by forming proton implant isolation regions around said photodetector.

9. The method of claim 8 wherein the step of forming VCSEL layers directly on a semiconductor wafer substrate further comprises:

forming first mirror layers on a semiconductor wafer;

forming a first cladding layer on said first mirror layer;

forming an active region on said first cladding layer;

forming a second cladding layer on said active region; and

forming second mirror layers on said second cladding layer.

10. The method of claim 8 wherein the step of forming said photodiode layers directly on said etch stop layer further comprises:

forming distributed p-type layers on said VCSEL layers;

forming an intrinsic layer on said distributed p-type layers; and

forming an n-type layer on said intrinsic layers.



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11. The method of claim 8 wherein the step of forming photodiode layers directly on said etch stop layer at discrete locations further comprises:

forming said photodiode layers distributed across said etch stop layer;

selectively removing said photodiode layers from said etch stop layer at discrete locations, and

selectively removing said etch stop layer from said uppermost VCSEL layer where said photodiode layers have been selectively removed.

12. The method of claim 11 wherein the etch stop layer is aluminum arsenide.

13. The method of claim 12 wherein the step of selectively removing said photodiode layers from said etch stop layer at discrete locations comprises selectively etching said photodiode layers using a solution of citric acid with a high percentage of peroxide.

14. The method of claim 12 wherein the step of selectively removing said etch stop layer comprises selectively etching said etch stop layer using a solution of hydrochloric acid with water.

15. The method of claim 6 further comprising the step of:

prohibiting operation of said inactive VCSELs by short circuiting said semiconductor wafer substrate to said photodiode anode contact to ensure that said active VCSELs will not become forward biased.

16. A method of manufacturing monolithic VCSEL and photodetector pairs, said method comprising the steps of:

forming VCSEL layers directly on a first side of a semiconductor wafer substrate;

forming photodiode layers distributed across said VCSEL layers at discrete locations;

forming a photodiode n-type contact (cathode) on an uppermost photodiode layer;

forming a photodiode p-type contact (anode) on an uppermost VCSEL layer;

forming a VCSEL p-type contact (anode) on an uppermost VCSEL layer;

forming a VCSEL n-type contact (cathode) on a second side of said semiconductor substrate;

defining active and inactive regions of the VCSEL by forming isolation regions in the VCSEL layers;

isolating said VCSEL layers from said photodiodes layers by forming proton implant isolation regions around said photodiodes;

forming interconnect metal pads on said photodiode anode and cathode and VCSEL anode;

forming a dielectric phase shifting layer on said VCSEL layers;

forming vias in the dielectric phase shifting layer for the interconnect metal pads; and

forming an anti-reflective coating on said photodetector.

17. The method of claim 16 further comprising the step of:

prohibiting operation of said inactive VCSELs by short circuiting said semiconductor wafer substrate to said photodiode anode contact to ensure that said active VCSELs will not become forward biased.

18. A method of manufacturing a monolithic VCSEL and integrated photodetector preamplifier, said method comprising the steps of:

forming VCSEL layers directly on a semiconductor wafer substrate;

forming photodiodes distributed across said wafer directly on said VCSEL layers at discrete locations; and

forming one or more transistors coupled to the photodiodes.



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19. The method of claim 18 wherein the step of forming VCSEL layers directly on a semiconductor wafer substrate comprises:

forming first mirror layers on a semiconductor wafer;

forming a first cladding layer on said first mirror layer;

forming an active region on said first cladding layer;

forming a second cladding layer on said active region; and

forming second mirror layers on said second cladding layer.

20. The method of claim 18 wherein the step of forming said photodiode layers directly on said VCSEL layers comprises:

forming distributed p-type layers on said VCSEL layers;

forming an intrinsic layer on said distributed p-type layers; and

forming an n-type layer on said intrinsic layers.

21. The method of claim 19 wherein the step of forming photodiode layers directly on said VCSEL layers at discrete locations comprises:

forming said photodiode layers distributed across said VCSEL layers; and

selectively removing said photodiode layers from said VCSEL layers at discrete locations.

22. The method of claim 20 wherein the transistor is a FET.

23. The method of claim 22 wherein the step of forming a FET comprises:

forming insulating regions on the surface of said photodiode materials wherein said insulating regions form a conductive well for the FET and isolate said photodiodes from said VCSEL;

forming ohmic electrical contacts for a source and drain which overlap said insulating regions and conductive well; and



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forming a contact for the gate within the conductive well formed by the isolation regions on the uppermost photodetector layer.

24. A method of manufacturing a monolithic VCSEL and integrated photodetector and preamplifier, said method comprising the steps of:

forming VCSEL layers directly on a semiconductor wafer substrate;

forming an etch stop layer on an uppermost VCSEL layer;

forming photodiodes distributed across said wafer directly on said etch stop at discrete locations; and

forming one or more transistors coupled to the photodiode.

25. The method of claim 24 wherein the step of forming VCSEL layers directly on a semiconductor wafer substrate further comprises:

forming first mirror layers on a semiconductor wafer;

forming a first cladding layer on said first mirror layer;

forming an active region on said first cladding layer;

forming a second cladding layer on said active region; and

forming second mirror layers on said second cladding layer.

26. The method of claim 25 wherein the step of forming said photodiode layers directly on said etch stop layer further comprises:

forming distributed p-type layers on said VCSEL layers;

forming an intrinsic layer on said distributed p-type layers; and

forming an n-type layer on said intrinsic layers.

27. The method of claim 26 wherein the step of forming photodiode layers directly on said etch stop layer at discrete locations comprises:

forming said photodiode layers distributed across said etch stop layer;

selectively removing said photodiode layers from said etch stop layer at discrete locations, and

selectively removing said etch stop layer from said VCSEL layer where said photodiode layers have been selectively removed.

28. The method of claim 27 wherein the etch stop layer is aluminum arsenide, with high content of aluminum.

29. The method of claim 28 wherein the step of selectively removing said photodiode layers from said etch stop layer at discrete locations comprises selectively etching said photodiode layers using a solution of citric acid with a high percentage of peroxide.

30. The method of claim 28 wherein the step of selectively removing said etch stop layer comprises selectively etching said etch stop layer using a solution of hydrochloric acid with water.

31. The method of claim 26 wherein the transistor is a FET.

32. The method of claim 28 wherein the step of forming a FET comprises:

forming insulating regions around said photodiodes wherein said insulating regions form a conductive well for the FET and isolate said photodiodes from said VCSEL;

forming first a electrical contact for a source and a second electrical contact for a drain on said insulating regions; and

forming a third electrical contact for a gate within the conductive well formed by the insulating regions.

33. A method of manufacturing a semiconductor photodetector, said method comprising the steps of:

forming distributed photodiodes on a semiconductor substrate by forming p-type layers directly on a semiconductor substrate;

forming an intrinsic layer on said p-type layers;

forming an n-type layer on said intrinsic layers; and

forming a proton implant isolation region between the p-type contact and the n-type contact (cathode) of the photodiodes.

34. A method of manufacturing an integrated photodetector preamplifier, said method comprising the steps of:

forming photodiodes directly on a semiconductor wafer substrate; and

forming one or more transistors on said photodiodes.

35. The method of claim 34 wherein the step of forming said photodiode layers directly on said semiconductor substrate further comprises:

forming distributed p-type layers on said VCSEL layers;

forming an intrinsic layer on said distributed p-type layers; and

forming an n-type layer on said intrinsic layers.

36. The method of claim 35 wherein the transistor is an FET.

37. The method of claim 36 wherein the step of forming a FET further comprises:

forming insulation regions around said photodiodes wherein said insulation regions form a conductive well for the FET;

forming a first electrical contact for a source and a second electrical contact for a drain, wherein said first and second electrical contacts overlap said insulation regions and conductive well on an uppermost photodiode layer; and

forming a third electrical contact for a gate within the conductive well formed by the insulation regions on said uppermost photodiode layer.

38. A monolithic optical transmitter and receiver pair comprising:

a substrate;

an optical transmitter formed on said substrate;



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an optical receiver formed laterally adjacent to said optical transmitter; and

an isolation region that electrically isolates said optical transmitter from said optical receiver.

39. The monolithic optical transmitter and receiver pair of claim 38 wherein the optical receiver comprises a photodiode.

40. The monolithic optical transmitter and receiver pair of claim 38 wherein the optical transmitter comprises a VCSEL with a plurality of layers.

41. The optical transmitter of claim 40 wherein the plurality of VCSEL layers further comprises:

a first mirror layers on a semiconductor wafer;

a first cladding layer on said first mirror layer;

an active region on said first cladding layer;

a second cladding layer on said active region; and

a second mirror layers on said second cladding layer.

42. The optical receiver of claim 39 wherein the photodiode further comprises:

distributed p-type layers formed on said VCSEL layers;

an intrinsic layer formed on said distributed p-type layers; and

an n-type layer formed on said intrinsic layers.

43. A monolithic optical transmitter and receiver pair comprising:

a substrate;

a multi-layer VCSEL structure formed on said substrate;

a photodiode formed on said VCSEL structure at discrete locations;

a first proton implant isolation region within said VCSEL structure defining active and inactive regions of the VCSEL structure; and

a second proton implant isolation region formed around said photodiode.

44. The monolithic optical transmitter and receiver pair of claim 43 wherein the VCSEL structure further comprises:

first mirror layers on a semiconductor wafer;

a first cladding layer on said first mirror layer;

an active region on said first cladding layer;

a second cladding layer on said active region; and

a second mirror layers on said second cladding layer.

45. The monolithic optical transmitter and receiver pair of claim 43 wherein the photodiode further comprises:

distributed p-type layers formed on said VCSEL layers;

an intrinsic layer formed on said distributed p-type layers; and

an n-type layer formed on said intrinsic layers.

46. A monolithic optical transmitter and receiver pair comprising:

a substrate;

a multi-layer VCSEL structure formed on said substrate;

an etch stop layer formed on the uppermost layer of said VCSEL;

a photodiode formed on said etch stop layer at discrete locations;

a first proton implant isolation region within said VCSEL structure defining active and inactive regions of the VCSEL structure; and

a second proton implant isolation region formed around said photodiode.

47. The monolithic optical transmitter and receiver pair of claim 46 wherein the VCSEL structure further comprises:

a first mirror formed on a semiconductor wafer;

a first cladding layer formed on said first mirror;

an active region formed on said first cladding layer;

a second cladding layer formed on said active region; and

a second mirror formed on said second cladding layer.

48. The monolithic optical transmitter and receiver pair of claim 46 wherein the photodiode further comprises:

distributed p-type layers formed on said VCSEL layers;

an intrinsic layer formed on said distributed p-type layers; and

an n-type layer formed on said intrinsic layers.

49. A monolithic optical transmitter and receiver pair comprising:

a substrate;

a multi-layer VCSEL structure formed on a first side of said substrate;

an etch stop layer formed on the uppermost layer of said VCSEL;

a photodiode formed on said etch stop layer at discrete locations;

a photodiode n-type contact (cathode) formed on said photodiode;

a photodiode p-type contact (anode) formed on said VCSEL;

a VCSEL p-type contact (anode) formed on said VCSEL;

a VCSEL n-type contact (cathode) coupled to a second side of said semiconductor substrate;

a first proton implant isolation region within said VCSEL structure defining active and inactive regions of the VCSEL structure;

a second proton implant isolation region around said photodiode;

interconnect metal pads formed on said photodiode anode and cathode and VCSEL anode;

a dielectric phase shifting layer formed on said VCSEL ; and

an anti-reflective coating formed on said photodiode.

50. A monolithic optical transmitter and receiver pair comprising:

a substrate;

a multi-layer VCSEL structure formed on said substrate;



Samsung Exhibit 1003, Page 294 of 654

one or more photodiodes formed on said VCSEL structure at discrete locations; and

one or more transistors coupled to the photodiodes.

51. The monolithic optical transmitter and receiver pair of claim 50 wherein the VCSEL structure further comprises:

a first mirror formed on a semiconductor wafer;

a first cladding layer formed on said first mirror;

an active region formed on said first cladding layer;

a second cladding layer formed on said active region; and

a second mirror formed on said second cladding layer.

52. The monolithic optical transmitter and receiver pair of claim 50 wherein the photodiode further comprises:

distributed p-type layers formed on said VCSEL layers;

an intrinsic layer formed on said distributed p-type layers; and

an n-type layer formed on said intrinsic layers.

53. The monolithic optical transmitter and receiver pair of claim 52 wherein the transistor is a FET.

54. The monolithic optical transmitter and receiver pair of claim 53 wherein the FET further comprises:

insulation regions formed around said photodiodes wherein said insulation regions form a conductive well for the FET and isolate said photodiodes from said VCSEL;

a first electrical contact forming a source and a second electrical contact forming a drain, wherein said first and second electrical contacts overlap said insulation regions and said conductive well on an uppermost surface of said photodiode; and

a third electrical contact forming a gate on said uppermost photodiode layer within the conductive well created by the isolation regions on the uppermost photodiode layer.

55. An integrated photodetector and preamplifier comprising:

a substrate;

photodiodes formed on said substrate; and

one or more transistors coupled to the photodiodes.

56. The integrated photodetector and preamplifier of claim 55 wherein the photodiode further comprises:

distributed p-type layers formed on said substrate;

an intrinsic layer formed on said distributed p-type layers; and

an n-type layer formed on said intrinsic layers.

57. The integrated photodetector and preamplifier of claim 56 wherein the transistor is a FET.

58. The integrated photodetector and preamplifier of claim 57 wherein the FET further comprises:

insulation regions formed around said photodiodes wherein said insulation regions form a conductive well for the FET;

a first electrical contact forming a source and a second electrical contact forming a drain, wherein said first and second electrical contacts overlap said insulation regions and said conductive well on said photodiode; and

a third electrical contact forming a gate on said photodiode within the conductive well formed by the isolation regions on the uppermost photodiode layer.

59. The monolithic optical transmitter and receiver pair of claim 54 wherein the insulation regions formed around said photodiodes are proton implantation regions.

60. The integrated photodetector and preamplifier of claim 58 wherein the insulation regions formed around said photodiodes are proton implantation regions.

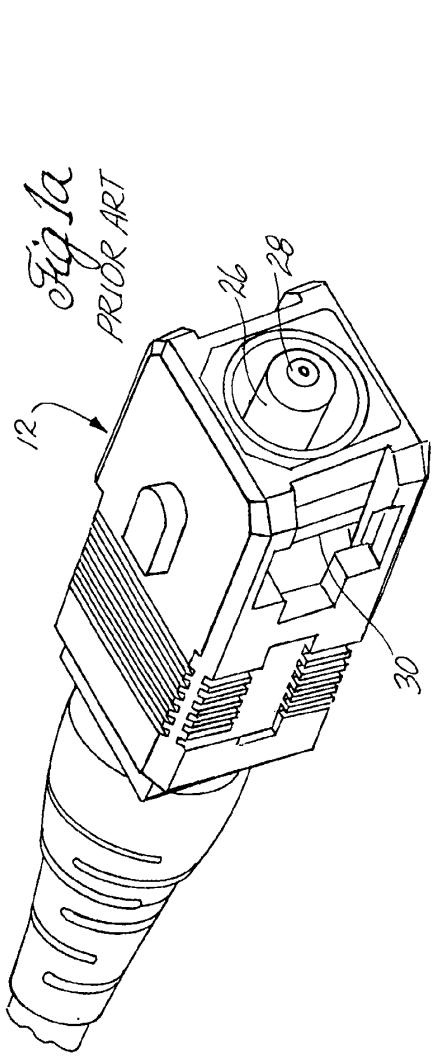



Fig 1a
PRIOR ART

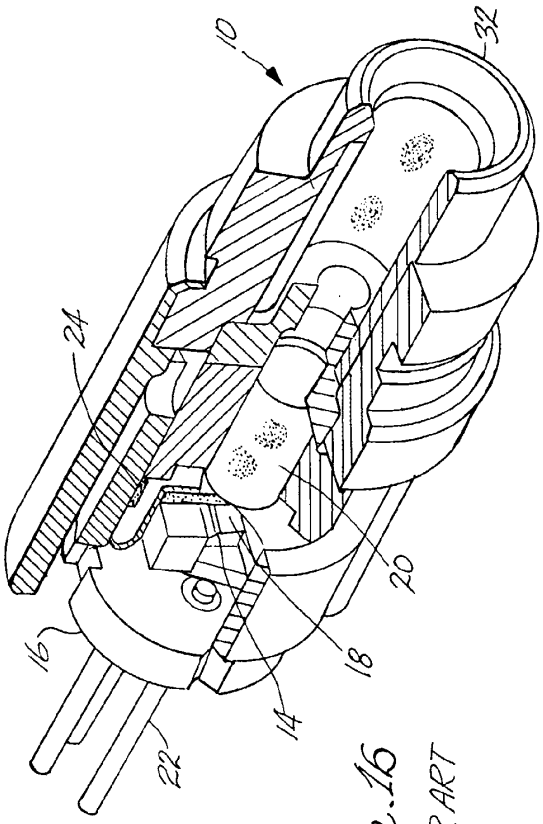



Fig. 1b
PRIOR ART

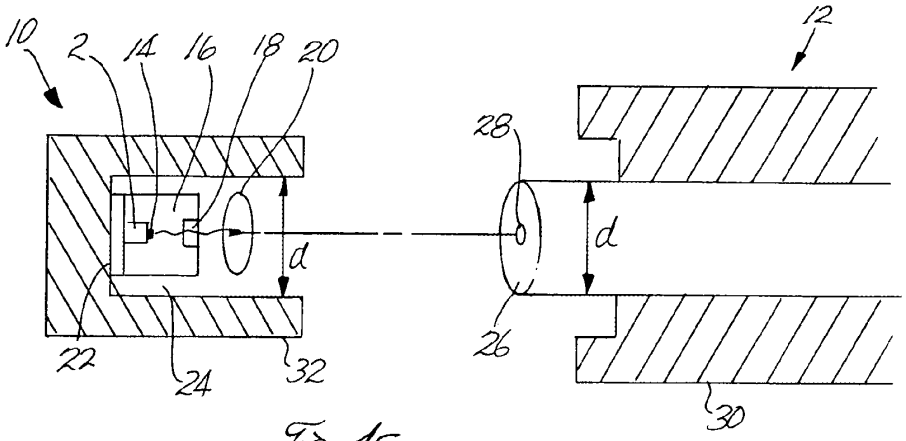



Fig. 1C
PRIOR ART

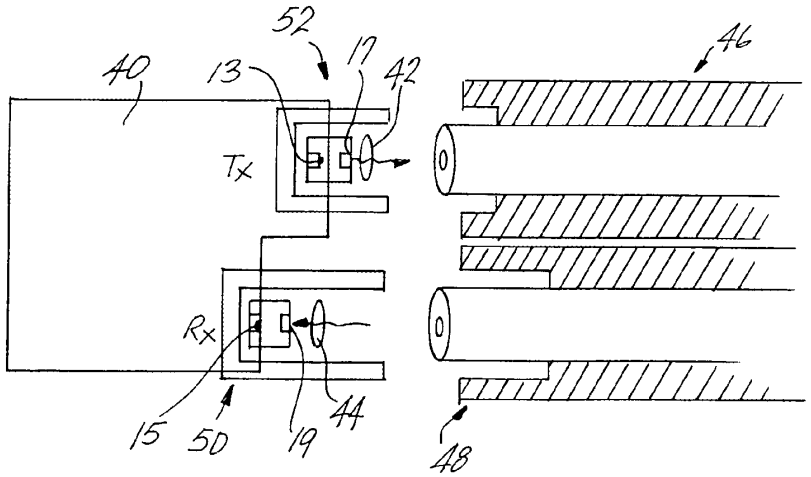



Fig. 1d
PRIOR ART

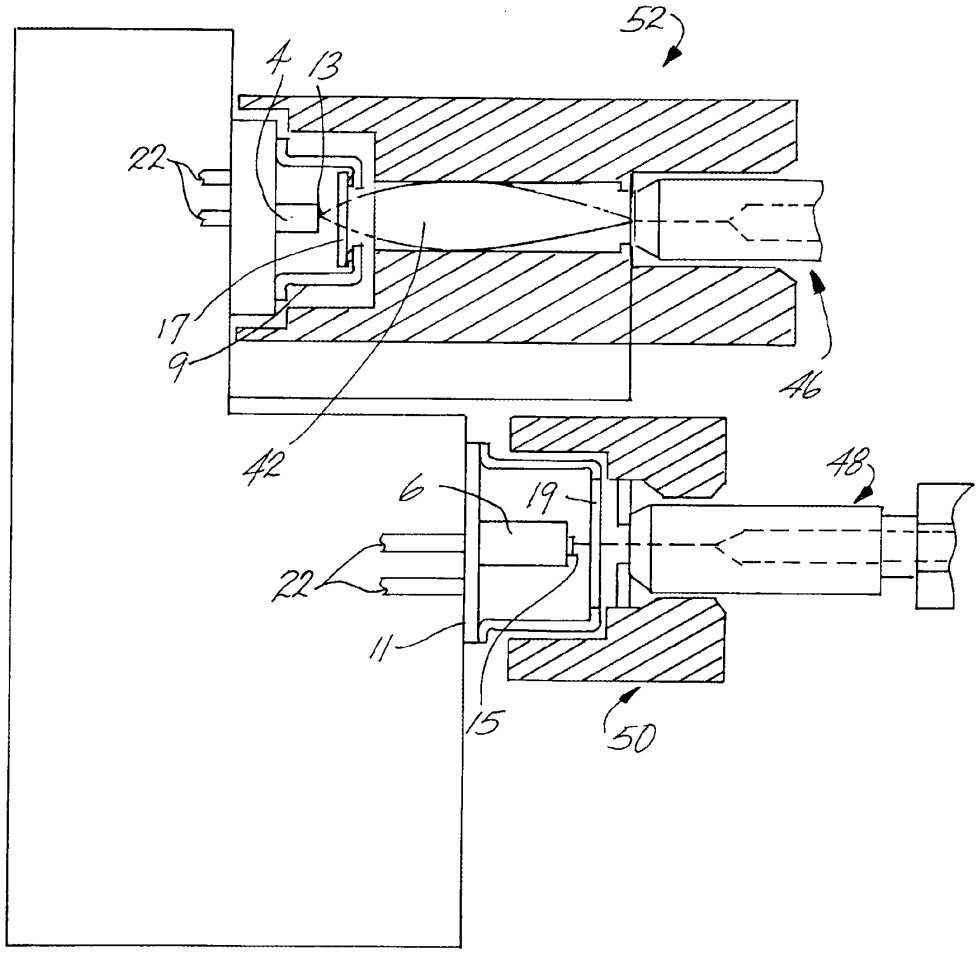
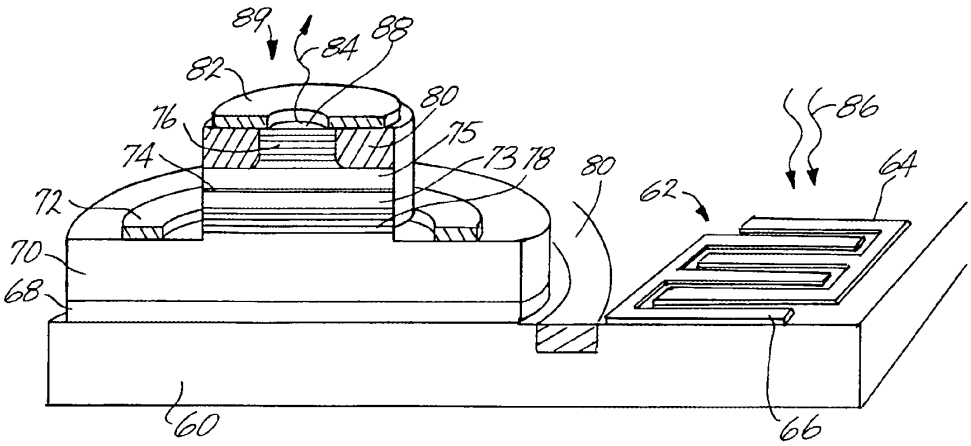



Fig. 2
PRIOR ART

Fig. 3


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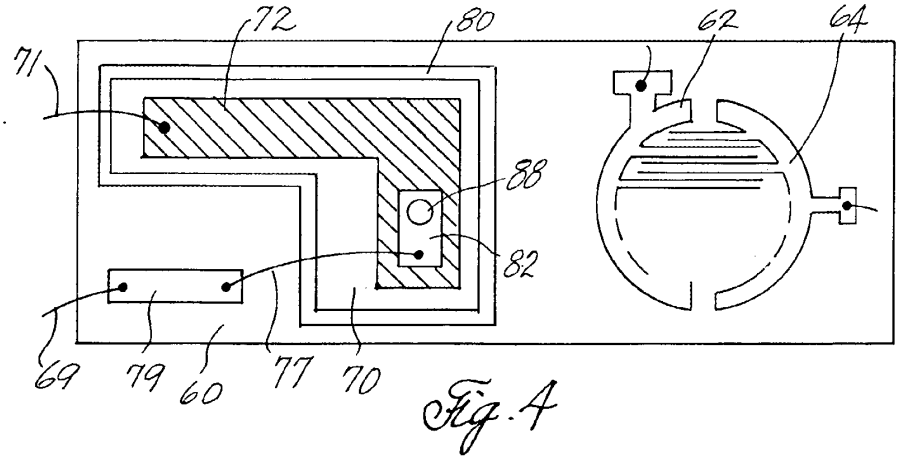

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Fig. 4

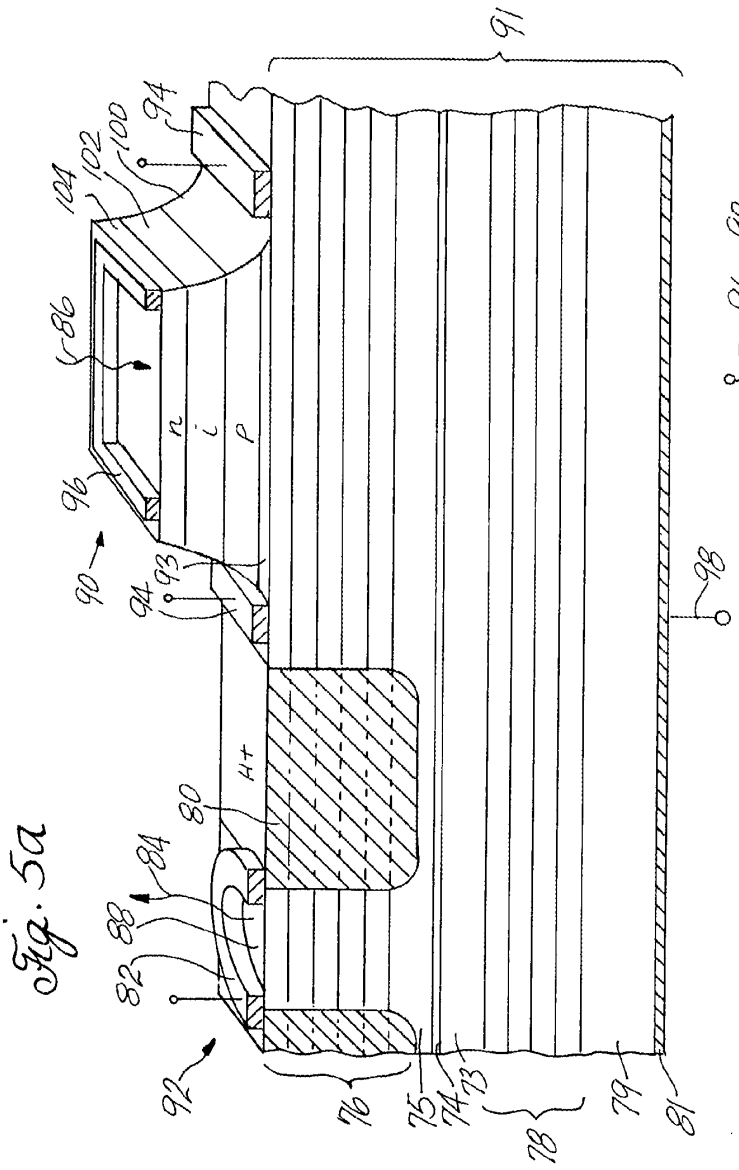



Fig. 5a

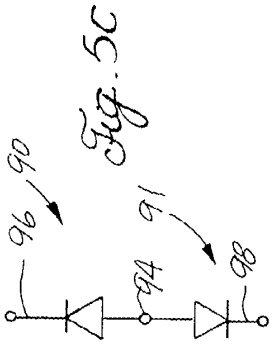



Fig. 5c

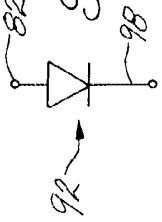
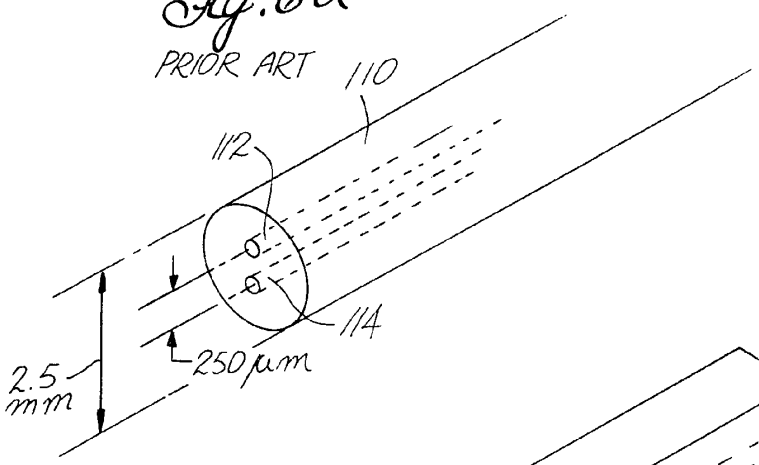



Fig. 5b

Fig. 6a
PRIOR ART



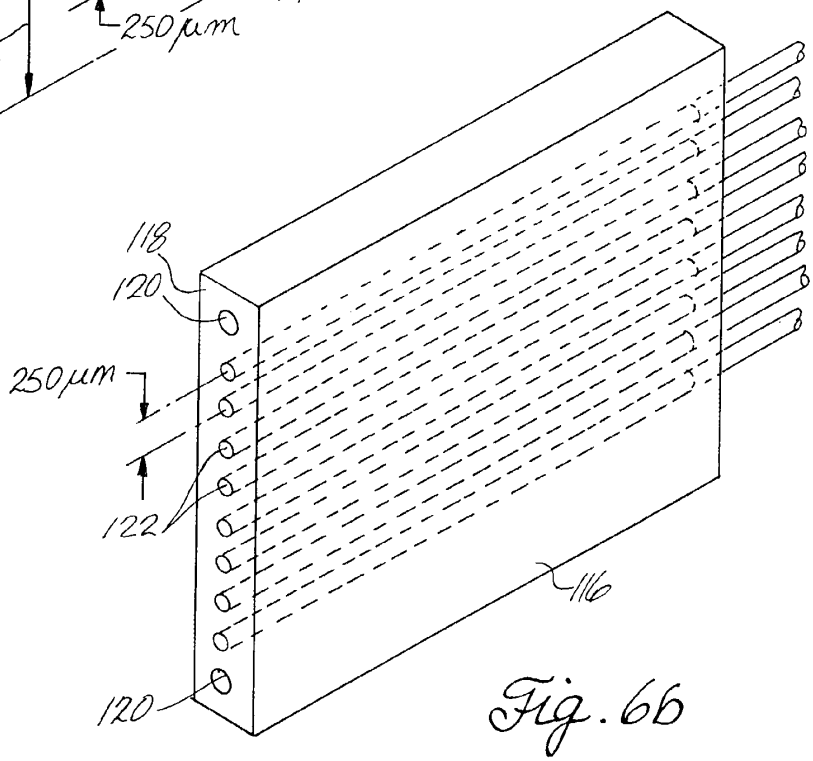




Fig. 6b
PRIOR ART

Fig. 7a

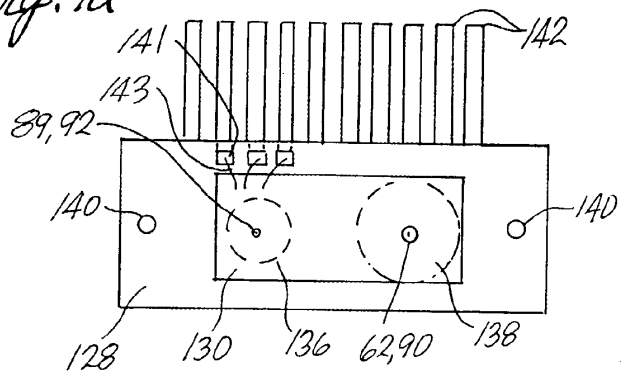



Fig. 7b

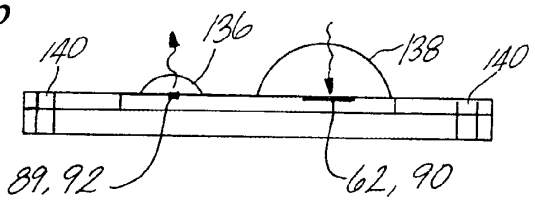
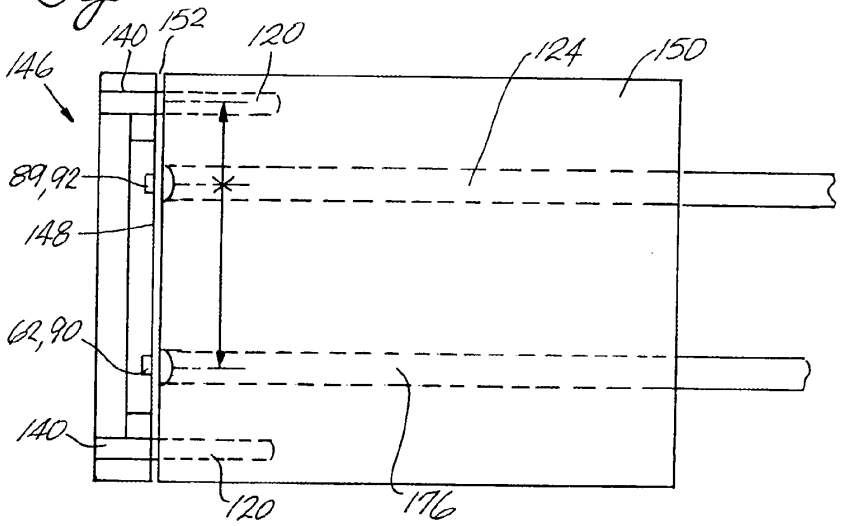



Fig. 7c



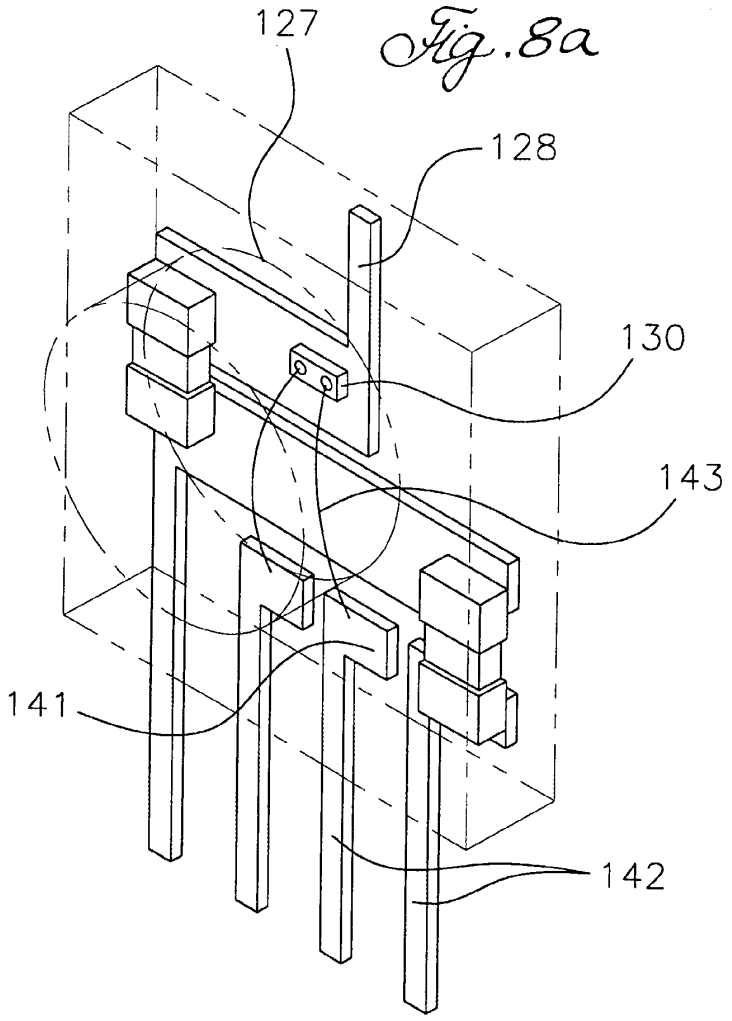



Fig. 8a

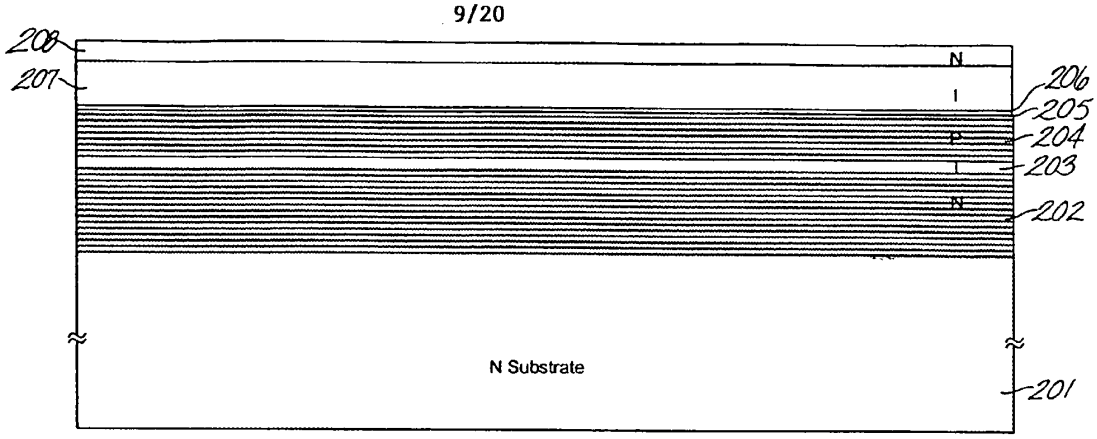



Fig. 9

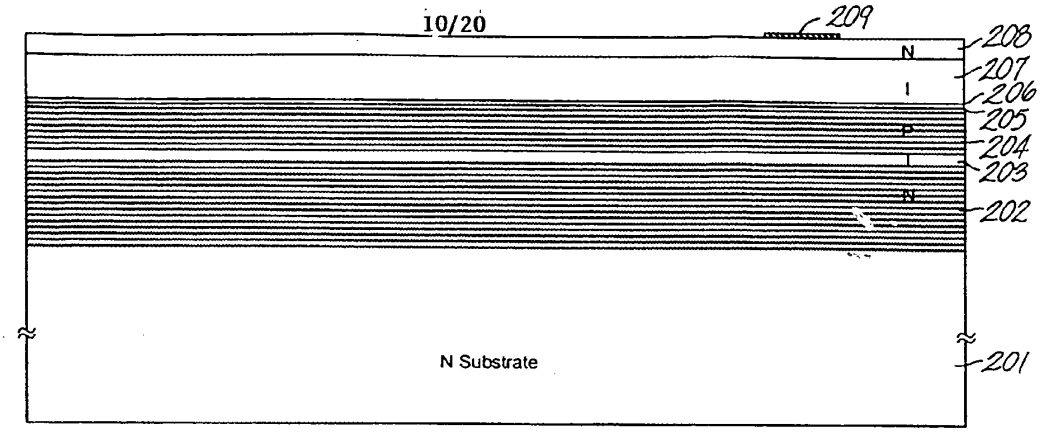



Fig. 10a

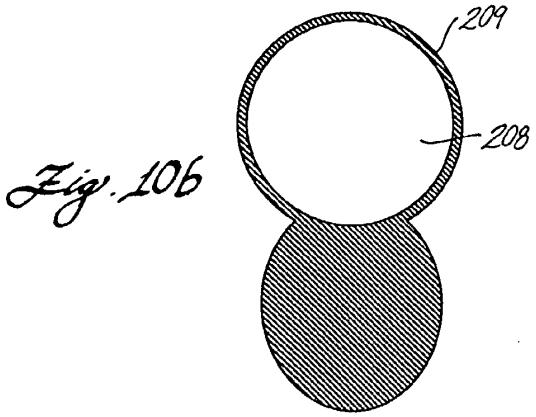



Fig. 10b

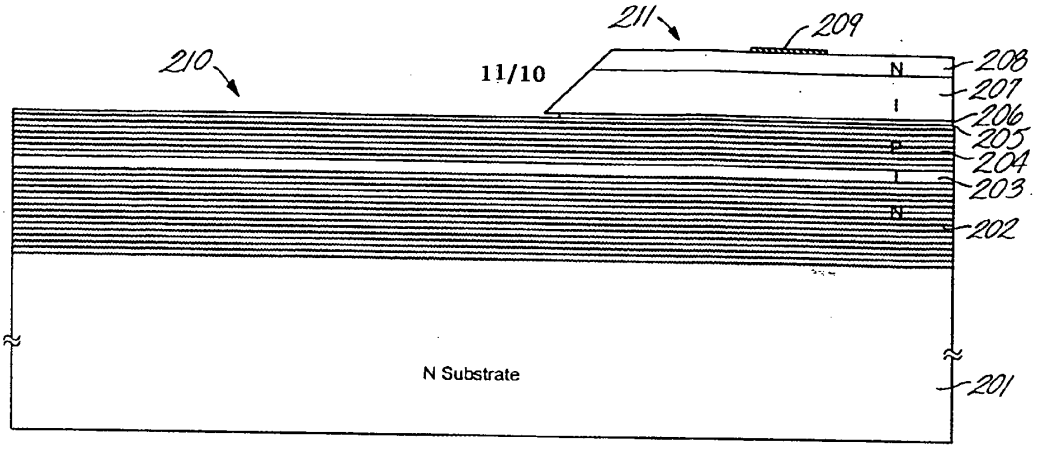



Fig. 11a

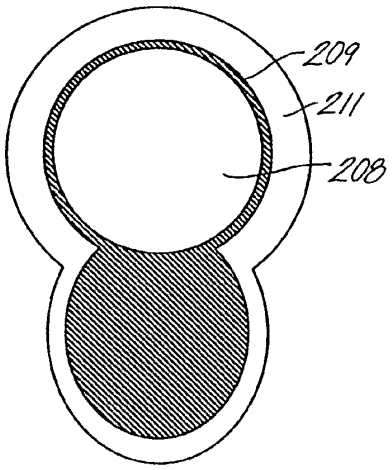



Fig. 11b

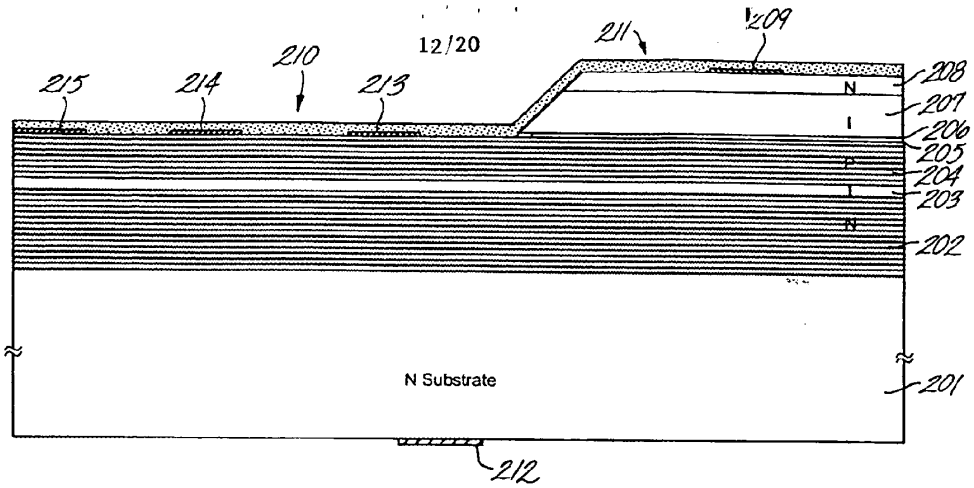



Fig. 12a

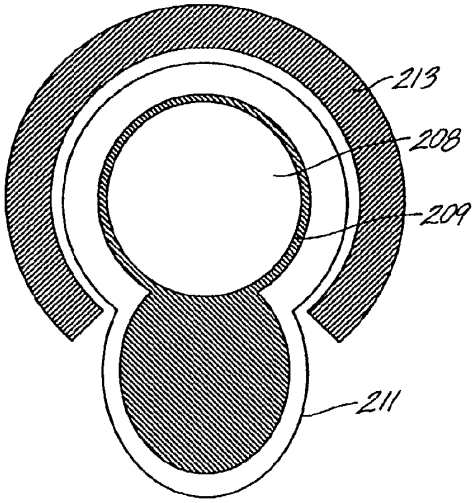



Fig. 12b

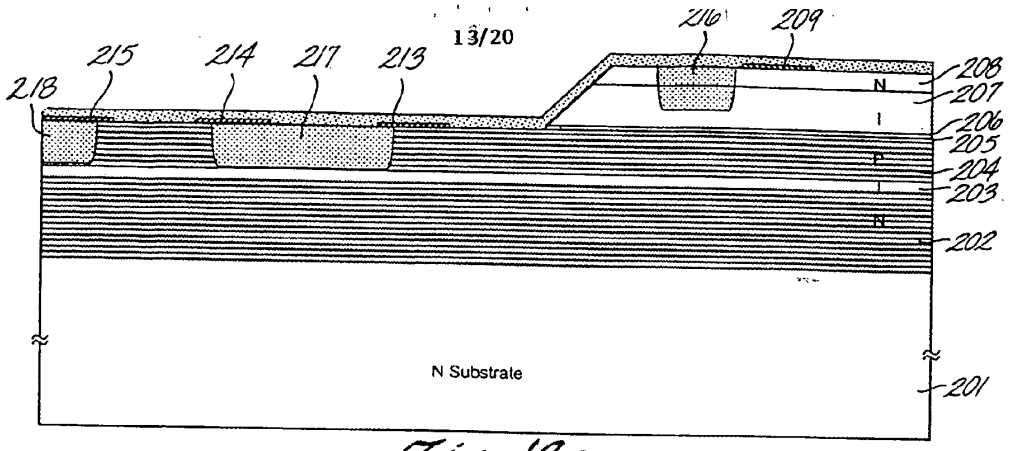
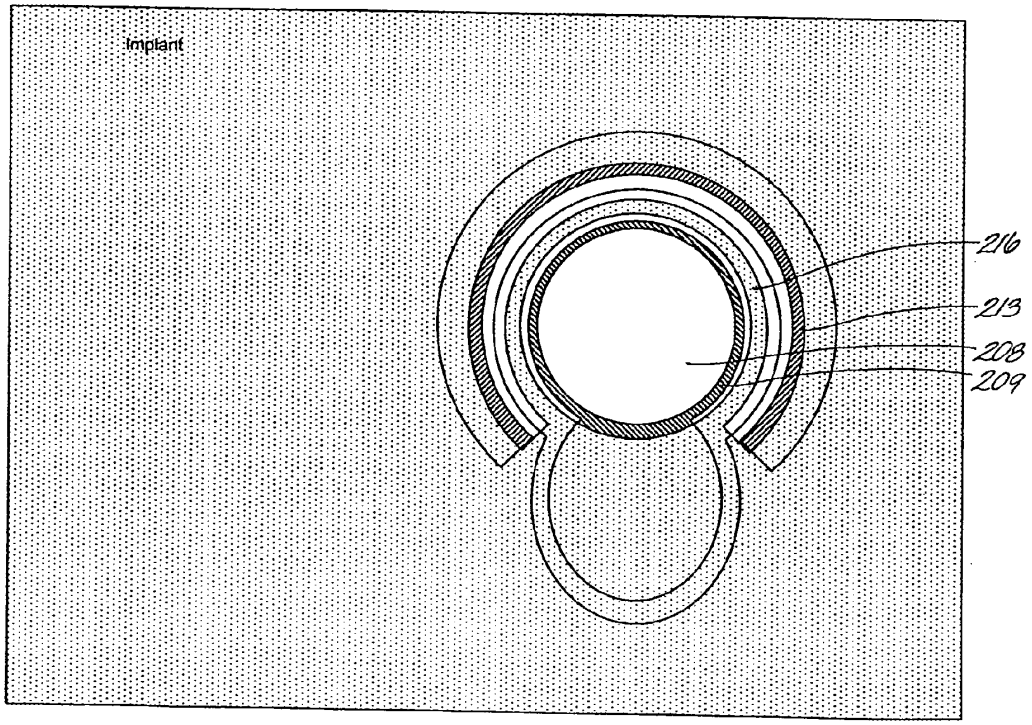



Fig. 13a

Fig. 13b



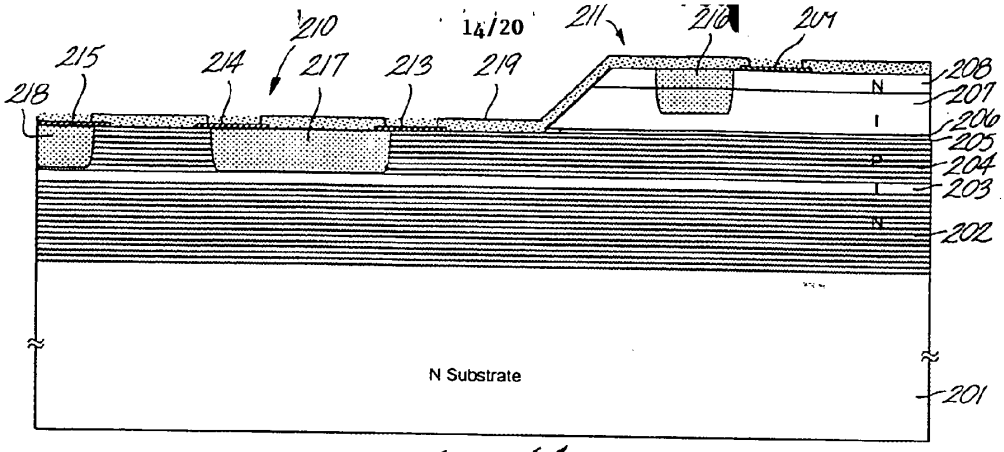
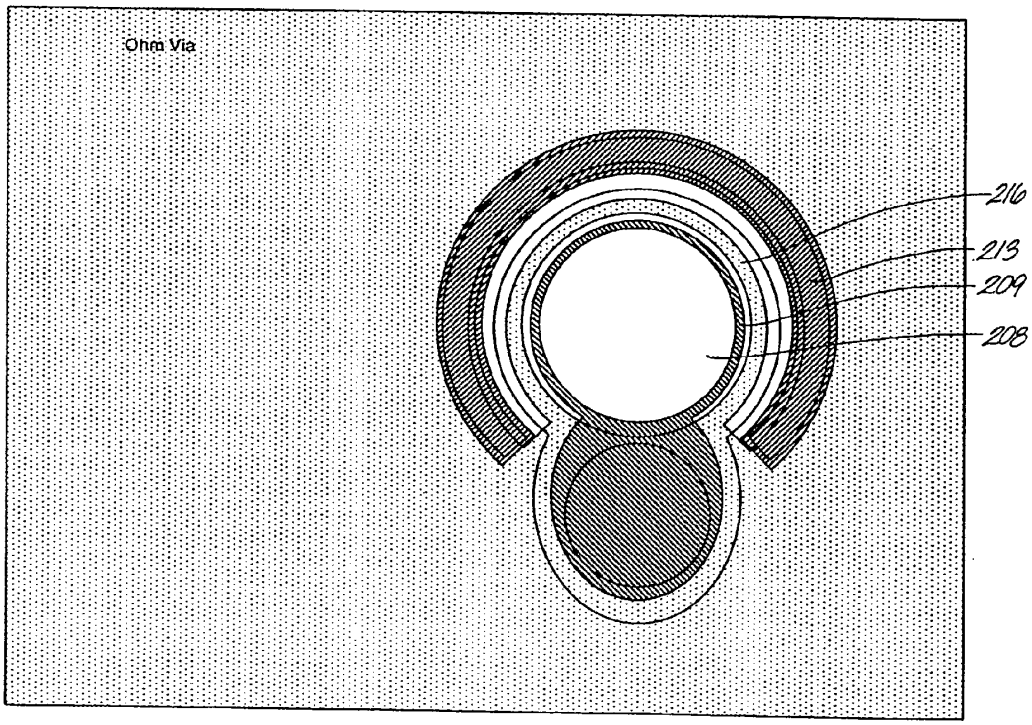



Fig. 14a

Fig. 14b



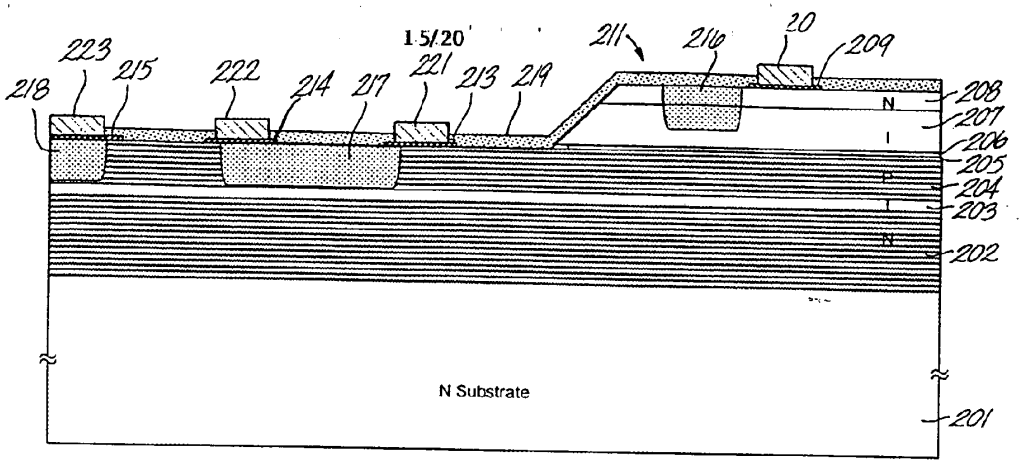
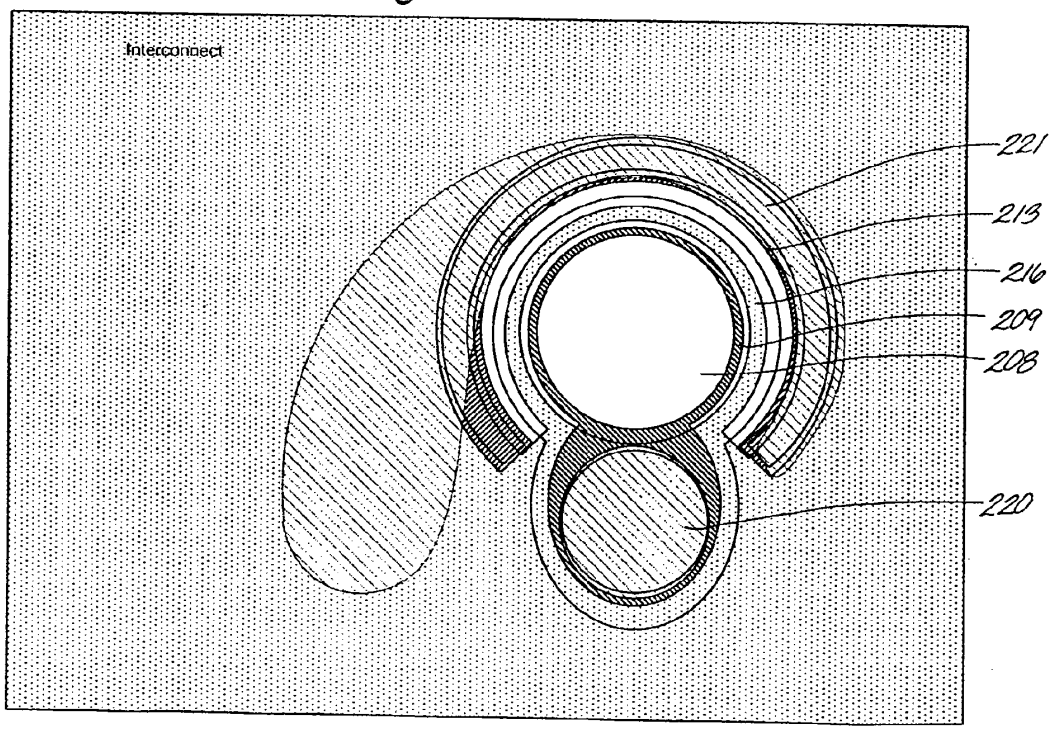



Fig. 15a

Fig. 15b



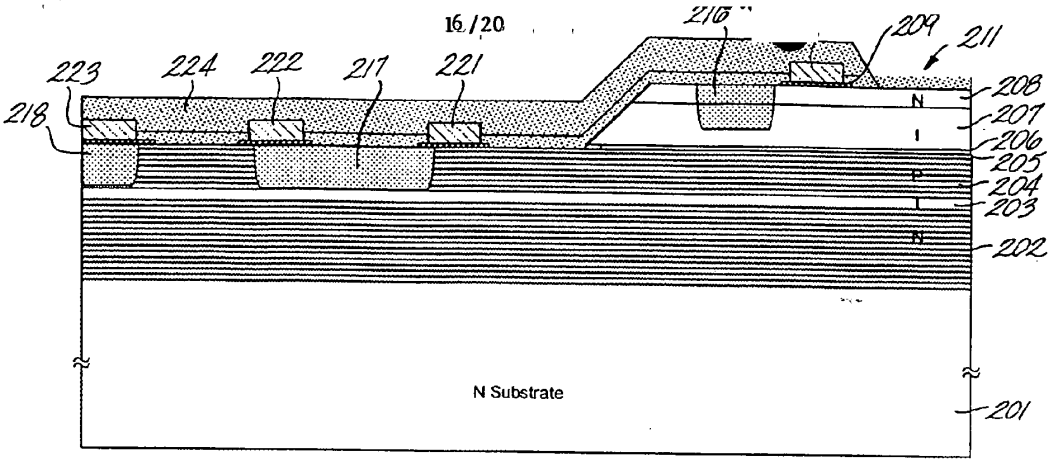
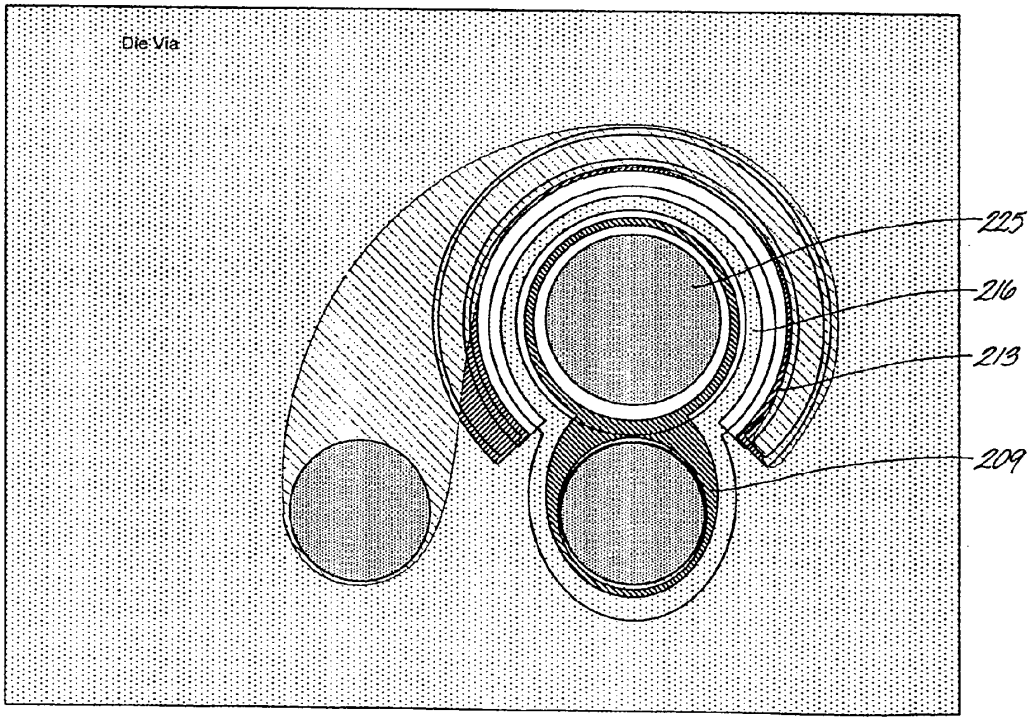



Fig. 16a

Fig. 16b



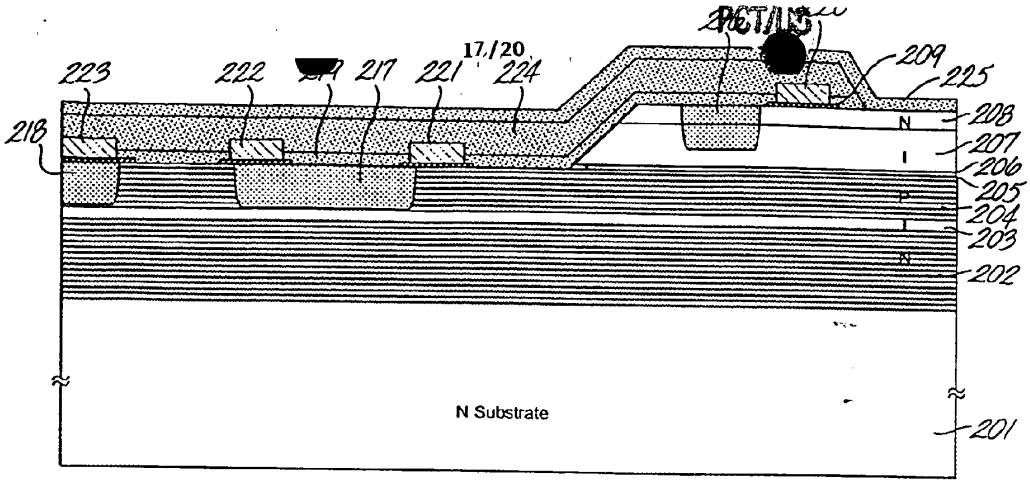



Fig. 17a

Fig. 17b

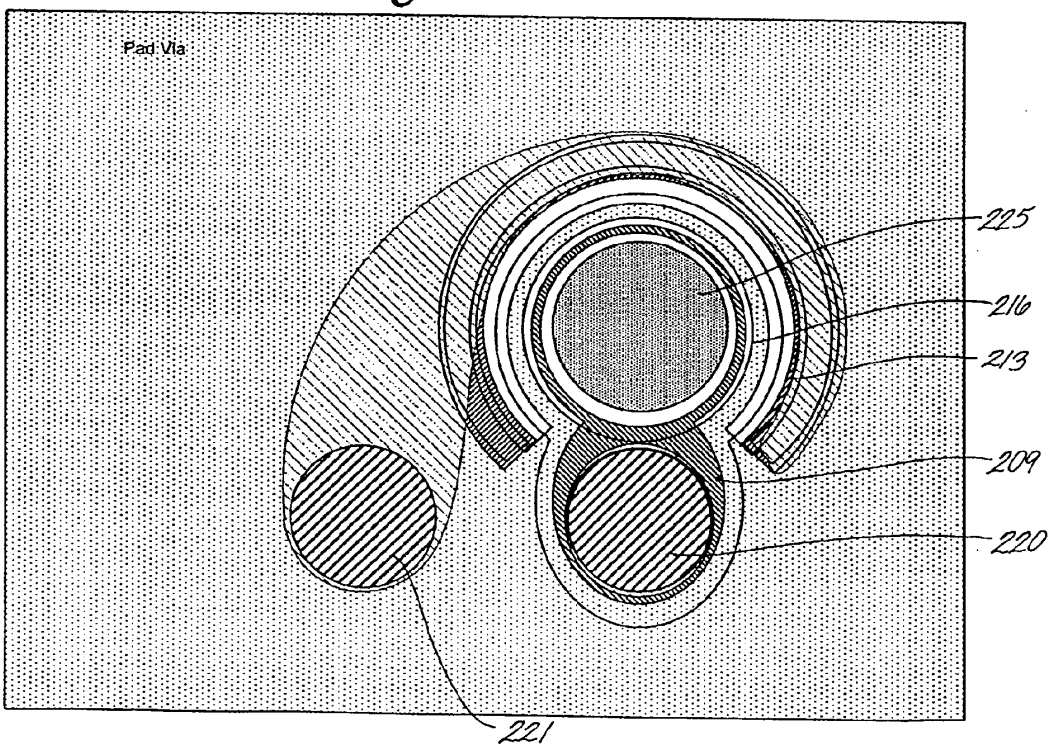


Fig. 18a

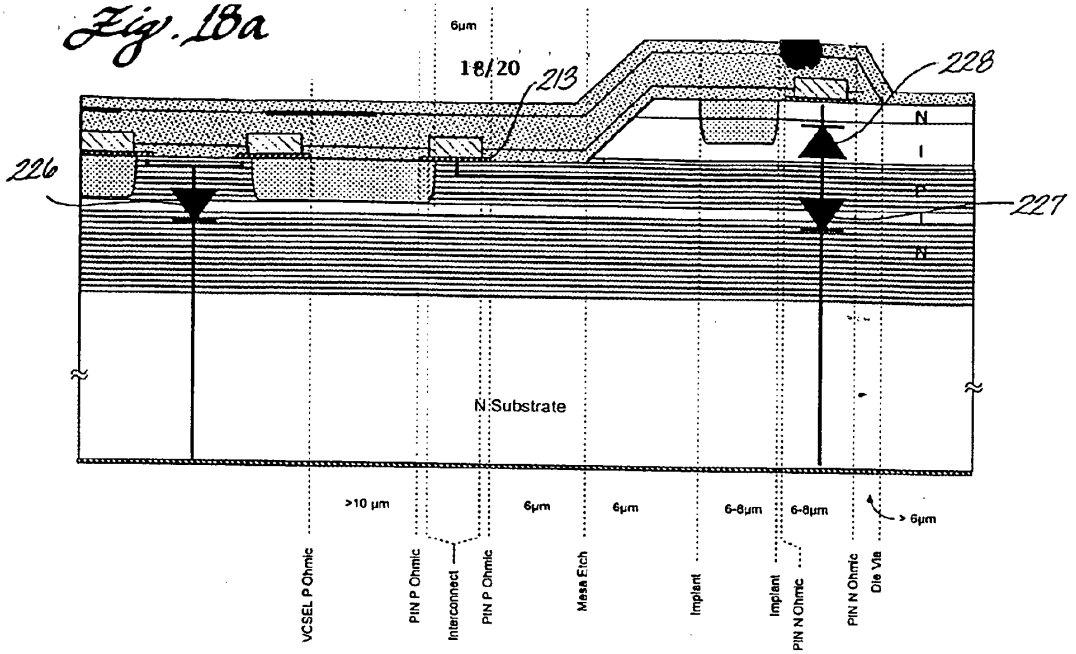
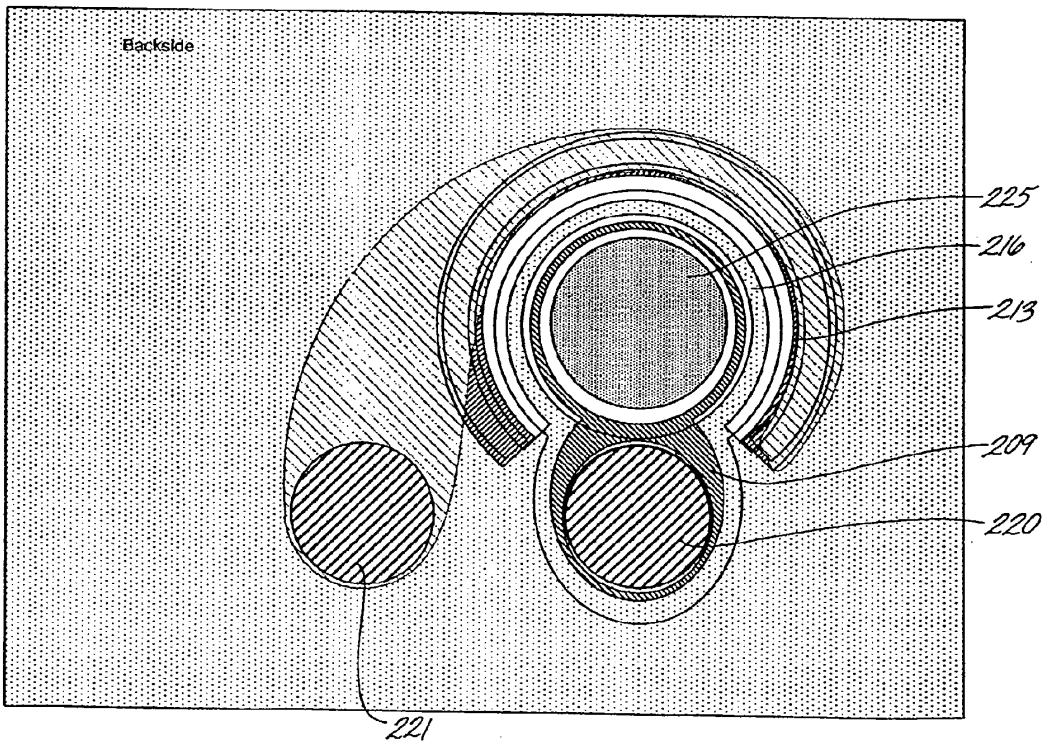



Fig. 18b



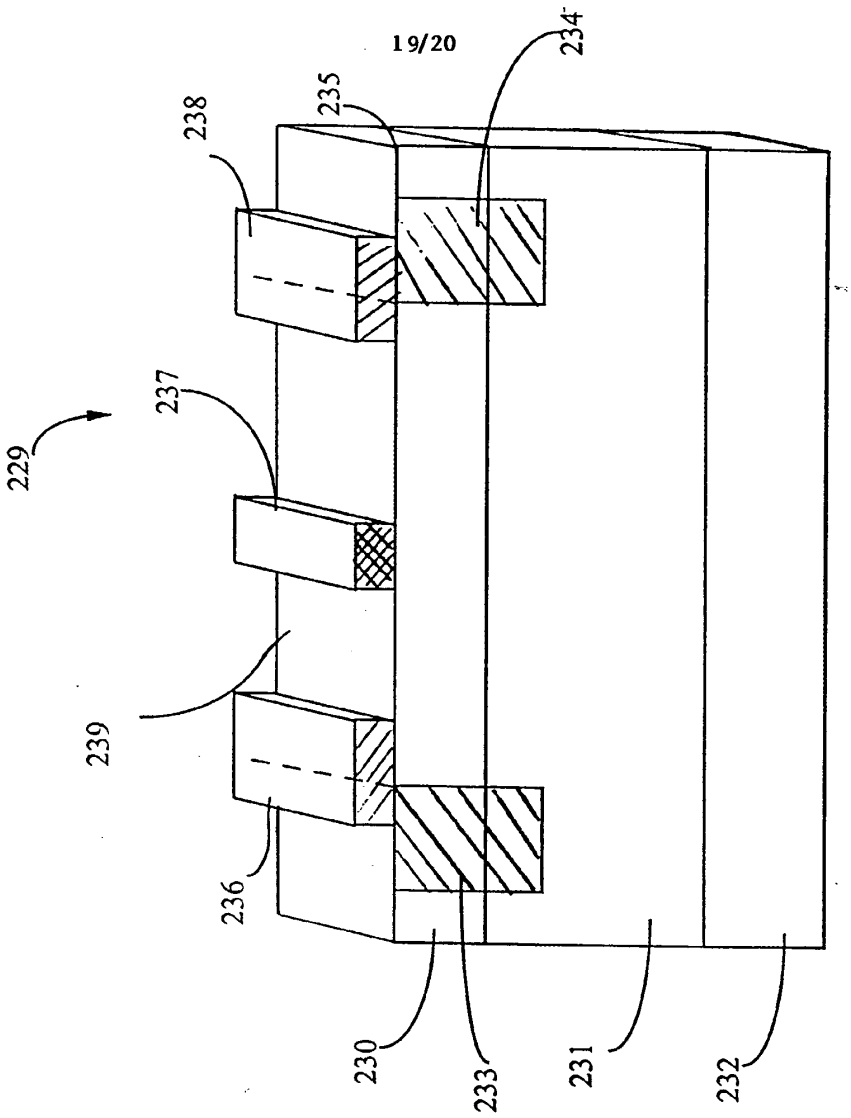



FIG. 19

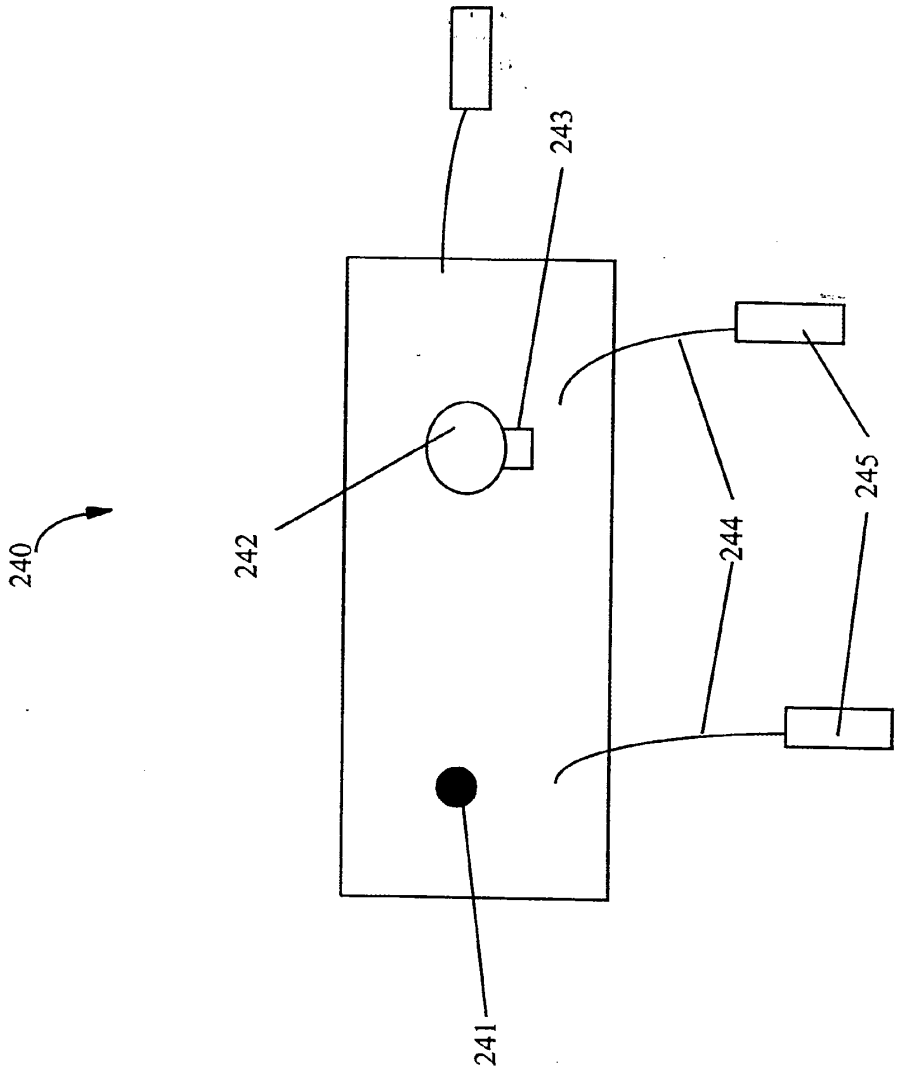



FIG. 20

**PATENT COOPERATION TREATY**

From the INTERNATIONAL SEARCHING AUTHORITY

To: IVAN S. KAVRUKOV
WISSING MILLER LLP
434 WEST 33RD STREET, 7TH FLOOR
NEW YORK, NY 10001

# PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

| | |
|---|---|
| Applicant's or agent's file reference<br>309-0013PCT | Date of mailing *(day/month/year)* DEC 06 2021<br>**FOR FURTHER ACTION** See paragraphs 1 and 4 below |
| International application No.<br>PCT/US 21/50717 | International filing date *(day/month/year)* 16 September 2021 (16.09.2021) |
| Applicant W&WSENS DEVICES, INC. | |

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   **Filing of amendments and statement under Article 19:**
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   **When?** The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   **How?** Directly to the International Bureau preferably through ePCT, or on paper to:
   The International Bureau of WIPO, 34, chemin des Colombettes, 1211 Geneva 20, Switzerland

   **For more detailed instructions,** see the *PCT Applicant's Guide*, International Phase, paragraphs 9.004 – 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:
   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.
   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   The applicant may **submit comments on an informal basis on the written opinion of the International Searching Authority** to the International Bureau. These comments will be made available to the public after international publication. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established.

   Shortly after the expiration of **18 months from the priority date, the international application will be published** by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for **entry into the national phase** before those designated Offices. In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months. For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

   Within **22 months from the priority date, the applicant may request that a supplementary international search be carried out** by a different International Searching Authority that offers this service (Rule 45*bis*.1). The procedure for requesting supplementary international search is described in the *PCT Applicant's Guide*, International Phase, paragraphs 8.006-8.032.

| | |
|---|---|
| Name and mailing address of the ISA/US<br>Mail Stop PCT, Attn: ISA/US<br>Commissioner for Patents<br>P.O. Box 1450, Alexandria, Virginia 22313-1450<br>Facsimile No. 571-273-8300 | Authorized officer<br>Kari Rodriquez<br>Telephone No. PCT Helpdesk: 571-272-4300 |

Form PCT/ISA/220 (revised January 2020)

PATENT COOPERATION TREATY

# PCT

## INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

| Applicant's or agent's file reference | | FOR FURTHER ACTION |
|---|---|---|
| 309-0013PCT | | see Form PCT/ISA/220 as well as, where applicable, item 5 below. |
| International application No. | International filing date *(day/month/year)* | (Earliest) Priority Date *(day/month/year)* |
| PCT/US 21/50717 | 16 September 2021 (16.09.2021) | 21 September 2020 (21.09.2020) |
| Applicant<br>W&WSENS DEVICES, INC. | | |

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 25

☒ as suggested by the applicant.

☐ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 21/50717

A. CLASSIFICATION OF SUBJECT MATTER

IPC - G01S 7/4865; G01S 17/894; G01S 13/08; G01J 1/42; G02B 6/42; G02F 1/16762 (2021.01)

CPC - G01S 7/4865; G01S 17/894; G01S 13/08; G01J 1/42; G02B 6/42; G02F 1/16762; H04N 5/36965; H01G 9/2045

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | US 2018/0102442 A1 (W&WSENS, DEVICES INC.) 12 April 2018 (12.04.2018) entire document, especially: para [0031], [0223], [0241], [0263], [0456], [0549] | 1-22 |
| A | US 2016/0240579 A1 (OMNIVISION TECHNOLOGIES INC.) 18 August 2016 (18.08.2016) entire document, especially: para [0002], [0020], [0023], [0024], [0034], [0038] | 1-22 |
| A | US 2017/0141153 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 18 May 2017 (18.05.2017) entire document, especially: [0015]-[0019], [0023], [0024], [0055] | 1-22 |

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 08 November 2021 | DEC 06 2021 |
| Name and mailing address of the ISA/US<br>Mail Stop PCT, Attn: ISA/US, Commissioner for Patents<br>P.O. Box 1450, Alexandria, Virginia 22313-1450<br>Facsimile No. 571-273-8300 | Authorized officer<br>Kari Rodriquez<br>Telephone No. PCT Helpdesk: 571-272-4300 |

Form PCT/ISA/210 (second sheet) (July 2019)

# PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: IVAN S. KAVRUKOV
WISSING MILLER LLP
434 WEST 33RD STREET, 7TH FLOOR
NEW YORK, NY 10001

# PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

| | |
|---|---|
| Date of mailing *(day/month/year)* | DEC 06 2021 |
| Applicant's or agent's file reference<br>309-0013PCT | **FOR FURTHER ACTION**<br>See paragraph 2 below |

| International application No. | International filing date *(day/month/year)* | Priority date *(day/month/year)* |
|---|---|---|
| PCT/US 21/50717 | 16 September 2021 (16.09.2021) | 21 September 2020 (21.09.2020) |

International Patent Classification (IPC) or both national classification and IPC

IPC - G01S 7/4865; G01S 17/894; G01S 13/08; G01J 1/42; G02B 6/42; G02F 1/16762 (2021.01)

CPC - G01S 7/4865; G01S 17/894; G01S 13/08; G01J 1/42; G02B 6/42; G02F 1/16762; H04N 5/36965; H01G 9/2045

Applicant W&WSENS DEVICES, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

| Name and mailing address of the ISA/US | Date of completion of this opinion | Authorized officer |
|---|---|---|
| Mail Stop PCT, Attn: ISA/US<br>Commissioner for Patents<br>P.O. Box 1450, Alexandria, Virginia 22313-1450<br>Facsimile No. 571-273-8300 | 08 November 2021 | Kari Rodriquez<br>PCT Help Desk<br>Telephone No. 571-272-4300 |

Form PCT/ISA/237 (cover sheet) (revised January 2019)

**WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US 21/50717

**Box No. I Basis of this opinion**

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(b)).

3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:

   a. ☐ forming part of the international application as filed:

      ☐ in the form of an Annex C/ST.25 text file.

      ☐ on paper or in the form of an image file.

   b. ☐ furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.

   c. ☐ furnished subsequent to the international filing date for the purposes of international search only:

      ☐ in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).

      ☐ on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

**WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US 21/50717

**Box No. V** **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement**

1. Statement

| | | | |
|---|---|---|---|
| Novelty (N) | Claims | 1-22 | YES |
| | Claims | NONE | NO |
| Inventive step (IS) | Claims | 1-22 | YES |
| | Claims | NONE | NO |
| Industrial applicability (IA) | Claims | 1-22 | YES |
| | Claims | NONE | NO |

2. Citations and explanations:
Claims 1-22 meet the criteria set out in PCT Article 33(2)-(3) because the prior art does not teach or fairly suggest the subject matter claimed.

The prior art for claim 1-22 is exemplified by US 2018/0102442 A1 to W&WSens, Devices Inc. (hereinafer 'W&WSens'), US 2016/0240579 A1 to Omnivision Technologies Inc. (hereinafter 'Omnivision'), and US 2017/0141153 A1 to Taiwan Semiconductor Manufacturing Co. Ltd. (hereinafter 'Taiwan').

Regarding Claim 1,
W&WSens discloses a microstructure enhanced absorption photosensitive device (para [0031]- This patent specification relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics.) comprising: a CMOS ASIC wafer (120) (para [0223]- FIG. 14 is a cross section schematic of a MSPD monolithically integrated with CMOS/BiCMOS electronics in a single chip, according to some embodiments. The chip can include multiple MSPD (and/or MSAPD) with single and/or multiple CMOS/BiCMOS electronic application specific integrated circuits.) the CMOS ASIC wafer is configured to process signals (para [0203]- CMOS/BiCMOS ASICs configured for functions such as signal processing, amplifying, transmission, storage, conditioning, analyzing, and/or configured as laser drivers and/or power amplifiers);
a semiconductor material (102) in which an array is formed (para [0241]- MSPD/MSAPD arrays can be fabricated over the holes either in the oxide and/or in the silicon such that each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array.);
wherein a region of undoped or low-doped Si (FIG. 24; element "I Si"; para [0263]- In the case of integration with CMOS/BiCMOS electronics, the I layer can be low doped and/or undoped) between said doped Si regions (see arrangement of elements of "P Si and/or GeSi and /or Ge", "I Si" and "N Si and/or Bragg reflecctor layers of Si/GeSi"), and a single microhole (2540) (FIG. 24, 2412; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.);
wherein a region of undoped or low-doped Ge or an alloy (FIG. 24; element "I Si and/or GeSi and /or Ge"; para [0263]- In the case of integration with CMOS/BiCMOS electronics, the I layer can be low doped and/or undoped) thereof between said doped regions of Ge or an alloy thereof (see arrangement of elements of "P Si and/or GeSi and /or Ge", "I Si and/or GeSi and /or Ge" and "N Si and/or GeSi and /or Ge");
deep trench (FIG. 89, element 8970; para [0549]- In some cases, instead of a highly doped connecting well, a deep trench with oxide 8970 on its sidewalls and the center can have conducting silicide 8972 and/or metal as shown in FIG. 89);
and connecting electrodes (para [0456]- In some cases a metal connecting electrode can be formed from the surface to the P+ substrate via a trench (not shown) and in some cases a TSV (not shown) can be formed to the bottom anode metal).
W&WSens fails to disclose a CMOS image sensor wafer (CIS) stacked to each other, the CMOS ASIC wafer is configured to receive the signals that the CIS wafer produces, wherein the CIS wafer comprises: an array of both Si pixels and Ge pixels; each Si pixel comprises an upper and a lower region of Si doped to opposite polarities and the microhole extending into the Si pixel; each Ge pixel comprises an upper and a lower region of Ge or an alloy thereof doped to opposite polarities and and a single microhole extending into the Ge pixel; wherein the deep trench is a trench isolation between adjacent Si pixels and Ge pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes in the Si and Ge pixels; and pixel electrodes coupled to said Si and Ge pixels, wherein connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Omnivision discloses a microstructure enhanced absorption photosensitive device (para [0002]-This invention is related to image sensors; para [0020]- each of the plurality of visible light pixels includes a photosensitive element, such as for example a photodiode, to receive a portion of light, and pixel support circuitry to generate a signal representative of an intensity of the received portion of light.) comprising:
a CMOS ASIC wafer (para [0034]- Digital counter 480 may be implemented using CMOS circuitry disposed on the ASIC die fabricated using a standard CMOS process of the stacked die system) and a CMOS image sensor wafer (CIS) (FIG. 2, image sensor 200) stacked to each other (para [0024]- Since stacked 3D color image sensor 200 includes a sensor die stacked with an ASIC die in a stacked chip scheme) such that signals that the CIS wafer produces (para [0023]- In one example, each of the plurality of visible light pixels 211 includes a photosensitive element such as a photodiode to receive a portion of light, as well as pixel support circuitry to generate a signal representative of an intensity of the received portion of light.), wherein the CIS wafer comprises:
a semiconductor material (FIG. 5, semiconductor layer 510) in which an array is formed of Si pixels (para [0020]- For instance, in one example, an imaging system includes an image pixel array having a plurality of visible light pixels, and a plurality of silicon photon avalanche diode (SPAD) pixels). (claim 1 continued)
--see supplemental box

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 21/50717

**Supplemental Box**

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
---Box V.2 - Citations and Explanations---

(claim 1 continued)
Omnivision fails to disclose the CMOS ASIC wafer is configured to receive and process signals, and wherein an array is formed of both Si pixels and Ge pixels; wherein each Si pixel comprises an upper and a lower region of Si doped to opposite polarities and a region of undoped or low-doped Si between said doped Si regions, and a single microhole extending into the Si pixel; wherein each Ge pixel comprises an upper and a lower region of Ge or an alloy thereof doped to opposite polarities and a region of undoped or low-doped Ge or an alloy thereof between said doped regions of Ge or an alloy thereof, and a single microhole extending into the Ge pixel; deep trench insulation between adjacent Si pixels and Ge pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes in the Si and Ge pixels; and pixel electrodes coupled to said Si and Ge pixels, connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Taiwan discloses a microstructure enhanced absorption photosensitive device (para [0017]- The present application is directed to a CMOS image sensor with elemental silicon and silicon germanium for long-wavelength pixel sensors; By arranging the photodetector in the silicon germanium layer, the photodetector advantageously has good sensitivity to and absorption of long-wavelength radiation, such as, for example, infrared radiation) comprising: a CMOS image sensor wafer (CIS) (FIG.1, 100; para [0018]- With reference to FIG. 1, a cross-sectional view 100 of some embodiments of a CMOS image sensor with a semiconductor stack 102 of silicon and silicon germanium is provided.), wherein the CIS wafer comprises:
a semiconductor material in which an array is formed of both Si pixels and Ge pixels (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer; para [0016]- Another solution is to use silicon germanium in place of elemental silicon for the semiconductor layer);
wherein each Si pixel comprises an upper (FIG.2A, upper silicon layer 104; para [0023]- an upper silicon layer 104 a of the pair is arranged over and directly abuts the silicon germanium layer 106 a.) and a lower region of Si (FIG.2A, lower silicon layer 204; para [0023]- Further, in some embodiments, a lower silicon layer 204 of the pair is arranged over and directly abuts the semiconductor substrate 202) doped (para [0023]- The semiconductor stack 102 a is doped with p- or n-type dopants, and comprises a pair of silicon layers 104 a, 204);
wherein each Ge pixel comprises a region of Ge or an alloy thereof doped (para [0023]- The semiconductor stack 102 a is doped with p- or n-type dopants, and comprises a pair of silicon layers 104 a, 204 and a silicon germanium layer 106 a arranged between the silicon layers 104 a, 204);
deep trench insulation (FIG. 1, deep trench isolation 112; para [0024]- The isolation region 112 is, for example, a shallow trench isolation (STI) region, a deep trench isolation (DTI) region, or an implant isolation region.) between adjacent Si pixels and Ge pixels (para [0055]- The isolation region 112 is configured to isolate the pixel sensors 110, 502, 504 and is, for example, a STI or DTI region; para [0016]- Another solution is to use silicon germanium in place of elemental silicon for the semiconductor layer.) in said array (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer) and an electrically and optically isolating material in said deep trench insulation (para [0061]- In some embodiments, the process for forming the isolation region 112 comprises filling the trench with a dielectric material, such as silicon dioxide.) in the Si and Ge pixels (para [0055]- The isolation region 112 is configured to isolate the pixel sensors 110, 502, 504 and is, for example, a STI or DTI region; para [0019]- The pixel sensor 110 comprises a photodetector 114 at least partially buried in the silicon germanium layer 106, and one or more pixel transistors arranged on the upper surface 108 of the silicon layer 104.);
and pixel electrodes coupled to said Si and Ge pixels (Claim 21- wherein the transistor further comprises a gate electrode, a gate dielectric layer, and an additional source/drain region, wherein the gate dielectric layer spaces the gate electrode over the surface of the silicon layer; para [0017]- A photodetector is at least partially buried in the silicon germanium layer and a transistor is arranged on a surface of the elemental silicon layer with a source/drain region electrically coupled to the photodetector);

Taiwan fails to discloses a CMOS ASIC wafer and a CMOS image sensor wafer (CIS) stacked to each other such that the CMOS ASIC wafer is configured to receive and process signals that the CIS wafer produces, wherein a region of Si to opposite polarities and a region of undoped or low-doped Si between said doped Si regions, and a single microhole extending into the Si pixel, wherein an upper and lower region of Ge or an alloy thereof to opposite polarities and a region of undoped or low-doped Ge or an alloy thereof between said doped regions of Ge or an alloy thereof, and a single microhole extending into the Ge pixel; an electrically and optically isolating material in said microholes; connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

None of the prior art discloses, the CMOS ASIC wafer is configured to receive signals; a region of Si to opposite polarities and the microhole extending into the Si pixel; an upper and a lower region of Ge or an alloy thereof to opposite polarities and a single microhole extending into the Ge pixel; an electrically and optically isolating material in said microholes; wherein connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular elements as required by claim 1, therefore claim 1 meets the criteria set out in PCT Article 33(2)-(3).

Claims 2-13 depend from claim 1, and therefore, meet the criteria set out in PCT Article 33(2)-(3) as well.

--see next page

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 21/50717

**Supplemental Box**

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
---Supplemental Box - Box V.2 - Citations and Explanations---

Regarding Claim 14,
W&WSens discloses a method (para [0031]- This patent specification relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics; para [0061]- According to some embodiments, a method of making a microstructure-enhanced photodetector (MSPD) configured to convert an optical input that at least some of the time has a cross-section that is essentially continuous spatially to an electrical output) comprising:
a CMOS ASIC wafer (120) (para [0223]- FIG. 14 is a cross section schematic of a MSPD monolithically integrated with CMOS/BiCMOS electronics in a single chip, according to some embodiments. The chip can include multiple MSPD (and/or MSAPD) with single and/or multiple CMOS/BiCMOS electronic application specific integrated circuits.) such that the CMOS ASIC wafer is configured to process signals (para [0203]- CMOS/BiCMOS ASICs configured for functions such as signal processing, amplifying, transmission, storage, conditioning, analyzing, and/or configured as laser drivers and/or power amplifiers);
forming a semiconductor material (102) by fabricating an array of pixels (2530 and/or 2532) therein (para [0241]- MSPD/MSAPD arrays can be fabricated over the holes either in the oxide and/or in the silicon such that each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array.)
forming a region of undoped or low-doped semiconductor material (FIG. 24; element "I Si and/or GeSi and /or Ge"; para [0263]- In the case of integration with CMOS/BiCMOS electronics, the I layer can be low doped and/or undoped) between said doped regions (see arrangement of elements of "P Si and/or GeSi and/or Ge", "I Si and/or GeSi and/or Ge" and "N Si and/or GeSi and/or Ge"), and a single microhole (2540) (FIG. 24, 2412; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.);
forming deep trench (FIG. 89, element 8970; para [0549]- In some cases, instead of a highly doped connecting well, a deep trench with oxide 8970 on its sidewalls and the center can have conducting silicide 8972 and/or metal as shown in FIG. 89);
and forming connecting electrodes (para [0456]- In some cases a metal connecting electrode can be formed from the surface to the P+ substrate via a trench (not shown) and in some cases a TSV (not shown) can be formed to the bottom anode metal).
W&WSens fails to disclose stacking and bonding to each other a CMOS image sensor wafer (CIS) (110), and the CMOS ASIC wafer is configured to receive the signals that the CIS wafer produces; forming at each pixel an upper and a lower region of semiconductor material doped to opposite polarities (2534, 2536), wherein the microhole (2540) extending into the pixel; wherein the deep trench is a trench isolation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes in the pixels; and forming pixel electrodes (154) coupled to said pixels, wherein connecting electrodes (152) coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Omnivision discloses a method (para [0002]-This invention is related to image sensors; para [0027]- In the example, the sensor die and ASIC die are stacked and coupled together during fabrication in a stacked chip scheme) comprising:
stacking and bonding (para [0024]- Since stacked 3D color image sensor 200 includes a sensor die stacked with an ASIC die in a stacked chip scheme; para [0038]- FIG. 5 includes a first device die 506, a second device die 508 and a bonding interface 507 at which first device die 506 is bonded to second device die 508.) to each other a CMOS ASIC wafer (para [0034]- Digital counter 480 may be implemented using CMOS circuitry disposed on the ASIC die fabricated using a standard CMOS process of the stacked die system) and a CMOS image sensor wafer (CIS) (FIG. 2, image sensor 200; para [0024]- Since stacked 3D color image sensor 200 includes a sensor die stacked with an ASIC die in a stacked chip scheme) such signals that the CIS wafer produces (para [0023]- In one example, each of the plurality of visible light pixels 211 includes a photosensitive element such as a photodiode to receive a portion of light, as well as pixel support circuitry to generate a signal representative of an intensity of the received portion of light.);
forming the CIS wafer in a semiconductor material (FIG. 5, semiconductor layer 510) by fabricating an array of pixels therein (para [0020]- For instance, in one example, an imaging system includes an image pixel array having a plurality of visible light pixels, and a plurality of silicon photon avalanche diode (SPAD) pixels; para [0038]- The illustrated example shows a plurality of visible light pixels, 502A, 502B, 502C and 502D, as well as a plurality of SPAD pixels 503A and 503B).
Omnivision fails to disclose the CMOS ASIC wafer is configured to receive and process signals; forming at each pixel an upper and a lower region of semiconductor material doped to opposite polarities and a region of undoped or low-doped semiconductor material between said doped regions, and a single microhole extending into the pixel; wherein the deep trench insulation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes in the pixels; forming deep trench insulation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes in the pixels; and forming pixel electrodes coupled to said pixels, connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Taiwan discloses a method (para [0056]- With reference to FIGS. 6-12, a series of cross-sectional views of some embodiments of a method for manufacturing a CMOS image sensor with silicon and silicon germanium is provided.) comprising:
a CMOS image sensor wafer (CIS) (FIG.1, 100; para [0018]- With reference to FIG. 1, a cross-sectional view 100 of some embodiments of a CMOS image sensor with a semiconductor stack 102 of silicon and silicon germanium is provided.);
forming the CIS wafer in a semiconductor material by fabricating an array of pixels therein (para [0015]- Some complementary metal-oxide -semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer);
forming at each pixel an upper (FIG.2A, upper silicon layer 104; para [0023]- an upper silicon layer 104 a of the pair is arranged over and directly abuts the silicon germanium layer 106 a.) and a lower region of semiconductor material (FIG.2A, lower silicon layer 204; para [0023]- Further, in some embodiments, a lower silicon layer 204 of the pair is arranged over and directly abuts the semiconductor substrate 202) doped (para [0023]- The semiconductor stack 102 a is doped with p- or n-type dopants, and comprises a pair of silicon layers 104 a, 204) to opposite polarities and a region of undoped or low-doped semiconductor material between said doped regions, and a single microhole extending into the pixel; (claim 14 continued)

--see next page

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 21/50717

**Supplemental Box**

**In case the space in any of the preceding boxes is not sufficient.**
Continuation of:
---Supplemental Box - Box V.2 - Citations and Explanations---

(claim 14 continued) forming deep trench insulation (FIG. 1, deep trench isolation 112; para [0024]- The isolation region 112 is, for example, a shallow trench isolation (STI) region, a deep trench isolation (DTI) region, or an implant isolation region.) between adjacent pixels (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer) in said array (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer) and an electrically and optically isolating material in said deep trench insulation in the pixels (para [0061]- In some embodiments, the process for forming the isolation region 112 comprises filling the trench with a dielectric material, such as silicon dioxide.;para [0055]- The isolation region 112 is configured to isolate the pixel sensors 110, 502, 504 and is, for example, a STI or DTI region); and forming pixel electrodes coupled to said pixels (Claim 21- wherein the transistor further comprises a gate electrode, a gate dielectric layer, and an additional source/drain region, wherein the gate dielectric layer spaces the gate electrode over the surface of the silicon layer).
Taiwan fails to disclose stacking and bonding to each other a CMOS ASIC wafer and a CMOS image sensor wafer (CIS) such that the CMOS ASIC wafer is configured to receive and process signals that the CIS wafer produces; forming a region to opposite polarities and a region of undoped or low-doped semiconductor material between said doped region; optically isolating material in said microholes; connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

None of the prior art discloses, the CMOS ASIC wafer is configured to receive signals; a region to opposite polarities and the microhole extending into the pixel; optically isolating material in said microholes in the pixels; connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular steps as required by claim 14, therefore claim 14 meets the criteria set out in PCT Article 33(2)-(3).

Claim 15 depends from claim 14, and therefore, meet the criteria set out in PCT Article 33(2)-(3) as well.

Regarding Claim 16,
W&WSens discloses a microstructure enhanced absorption photosensitive device (para [0031]- This patent specification relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics.) comprising: a CMOS ASIC wafer (para [0223]- FIG. 14 is a cross section schematic of a MSPD monolithically integrated with CMOS/BiCMOS electronics in a single chip, according to some embodiments. The chip can include multiple MSPD (and/or MSAPD) with single and/or multiple CMOS/BiCMOS electronic application specific integrated circuits.) the CMOS ASIC wafer is configured to process signals (para [0203]- CMOS/BiCMOS ASICs configured for functions such as signal processing, amplifying, transmission, storage, conditioning, analyzing, and/or configured as laser drivers and/or power amplifiers);
a layer in which an array of pixels is formed (para [0241]- MSPD/MSAPD arrays can be fabricated over the holes either in the oxide and/or in the silicon such that each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array);
wherein a region of undoped or low-doped semiconductor material (FIG. 24; element "I Si and/or GeSi and /or Ge"; para [0263]- In the case of integration with CMOS/BiCMOS electronics, the I layer can be low doped and/or undoped) between said doped regions (see arrangement of elements of "P Si and/or GeSi and /or Ge", "I Si and/or GeSi and /or Ge" and "N Si and/or GeSi and /or Ge"), and a single microhole (2540) (FIG. 24, 2412; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.);
deep trench (FIG. 89, element 8970; para [0549]- In some cases, instead of a highly doped connecting well, a deep trench with oxide 8970 on its sidewalls and the center can have conducting silicide 8972 and/or metal as shown in FIG. 89);
and connecting electrodes (para [0456]- In some cases a metal connecting electrode can be formed from the surface to the P+ substrate via a trench (not shown) and in some cases a TSV (not shown) can be formed to the bottom anode metal).
W&WSens fails to disclose a CMOS image sensor wafer (CIS) (110) stacked to each other, the CMOS ASIC wafer is configured to receive the signals that the CIS wafer produces, wherein each pixel comprises an upper and a lower region of semiconductor material doped to opposite polarities (2534, 2536), and the microhole extending into the pixel; wherein the deep trench is a trench isolation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes; and pixel electrodes (154) coupled to said pixels, wherein connecting electrodes (152) coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Omnivision discloses a microstructure enhanced absorption photosensitive device (para [0002]-This invention is related to image sensors; para [0020]- each of the plurality of visible light pixels includes a photosensitive element, such as for example a photodiode, to receive a portion of light, and pixel support circuitry to generate a signal representative of an intensity of the received portion of light.) comprising:
a CMOS ASIC wafer (para [0034]- Digital counter 480 may be implemented using CMOS circuitry disposed on the ASIC die fabricated using a standard CMOS process of the stacked die system) and a CMOS image sensor wafer (CIS) (FIG. 2, image sensor 200) stacked to each other (para [0024]- Since stacked 3D color image sensor 200 includes a sensor die stacked with an ASIC die in a stacked chip scheme) such that signals that the CIS wafer produces (para [0023]- In one example, each of the plurality of visible light pixels 211 includes a photosensitive element such as a photodiode to receive a portion of light, as well as pixel support circuitry to generate a signal representative of an intensity of the received portion of light.), wherein the CIS wafer comprises:
a layer (FIG. 5, semiconductor layer 510) in which an array of pixels is formed (para [0020]- For instance, in one example, an imaging system includes an image pixel array having a plurality of visible light pixels, and a plurality of silicon photon avalanche diode (SPAD) pixels; para [0038]- The illustrated example shows a plurality of visible light pixels, 502A, 502B, 502C and 502D, as well as a plurality of SPAD pixels 503A and 503B); (claim 16 continued)

--see next page

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 21/50717

**Supplemental Box**

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
---Supplemental Box - Box V.2 - Citations and Explanations---

(claim 16 continued) Omnivision fails to disclose the CMOS ASIC wafer is configured to receive and process signals; wherein each pixel comprises an upper and a lower region of semiconductor material doped to opposite polarities, a region of undoped or low-doped semiconductor material between said doped regions, and a single microhole extending into the pixel; wherein the deep trench insulation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes; deep trench insulation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes; and pixel electrodes coupled to said pixels, connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Taiwan discloses a microstructure enhanced absorption photosensitive device (para [0017]- The present application is directed to a CMOS image sensor with elemental silicon and silicon germanium for long-wavelength pixel sensors; By arranging the photodetector in the silicon germanium layer, the photodetector advantageously has good sensitivity to and absorption of long-wavelength radiation, such as, for example, infrared radiation) comprising: a CMOS image sensor wafer (CIS) (FIG.1, 100; para [0018]- With reference to FIG. 1, a cross-sectional view 100 of some embodiments of a CMOS image sensor with a semiconductor stack 102 of silicon and silicon germanium is provided.), wherein the CIS wafer comprises:
a layer in which an array of pixels is formed (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer);
wherein each pixel comprises an upper (FIG.2A, upper silicon layer 104; para [0023]- an upper silicon layer 104 a of the pair is arranged over and directly abuts the silicon germanium layer 106 a.) and a lower region of semiconductor material (FIG.2A, lower silicon layer 204; para [0023]- Further, in some embodiments, a lower silicon layer 204 of the pair is arranged over and directly abuts the semiconductor substrate 202) doped (para [0023]- The semiconductor stack 102 a is doped with p- or n-type dopants, and comprises a pair of silicon layers 104 a, 204);
deep trench insulation (FIG. 1, deep trench isolation 112; para [0024]- The isolation region 112 is, for example, a shallow trench isolation (STI) region, a deep trench isolation (DTI) region, or an implant isolation region.) between adjacent pixels (para [0055]- The isolation region 112 is configured to isolate the pixel sensors 110, 502, 504 and is, for example, a STI or DTI region) in said array (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer) and an electrically and optically isolating material in said deep trench insulation (para [0061]- In some embodiments, the process for forming the isolation region 112 comprises filling the trench with a dielectric material, such as silicon dioxide);
and pixel electrodes coupled to said pixels (Claim 21- wherein the transistor further comprises a gate electrode, a gate dielectric layer, and an additional source/drain region, wherein the gate dielectric layer spaces the gate electrode over the surface of the silicon layer);
Taiwan fails to disclose a CMOS ASIC wafer and a CMOS image sensor wafer (CIS) stacked to each other such that the CMOS ASIC wafer is configured to receive and process signals that the CIS wafer produces, wherein a region of semiconductor material to opposite polarities and a region of undoped or low-doped semiconductor material between said doped regions, and a single microhole extending into the pixel; an electrically and optically isolating material in said microholes; connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

None of the prior art discloses, the CMOS ASIC wafer is configured to receive signals; a region of semiconductor material to opposite polarities and the microhole extending into the pixel; an electrically and optically isolating material in said microholes; wherein connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular elements as required by claim 16, therefore claim 16 meets the criteria set out in PCT Article 33(2)-(3).

Claims 17-22 depend from claim 16, and therefore, meet the criteria set out in PCT Article 33(2)-(3) as well.

Claims 1-22 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used by industry.

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SUBJECT OF THE INVENTION

The Radix Rumiciss photodetector of photodetector preparation method and preparation

[**0001**] Technical field

[**0002**] The present invention relates to the Radix Rumiciss photodetector of a kind of photodetector preparation method and preparation, belong to semiconductor optoelectronic Sub- technical field.

[**0003**] Background technology

[**0004**] Photodetector is visited in biomedicine, data storage medium, flame monitoring, ultraviolet dosage measurement, high-energy ray It is used widely in the fields such as survey, medical treatment, safety check, industrial flaw detection.When incident illumination energy is more than photodetector material forbidden band width When spending, electronics will be made to transit to conduction band from valence band, produce electron hole pair, the electron hole pair of generation is collected by electrode, It is the formation of photoelectric current output.Quantum efficiency is to weigh one of most important performance indications of photodetector, mainly by Photon incident efficiency, internal quantum efficiency and carrier collection efficiency determine.Because the refractivity of quasiconductor and air is big, quite Light reflected by interface and be collected it is impossible to enter in device, lead to device efficiency to reduce.Generally according to incident illumination and reflected light Interference cancellation principle, design and prepare anti-reflection film so that the vertical incidence light incident efficiency of single wavelength reaches more than 95%. But the problem that this design brings is, when incident wavelength offset design wavelength, or angle of incidence offset from perpendicular, visit Survey efficiency drastically to decline.

[**0005**] According to Theory of Electromagnetic Field, taking for electric field perpendicular to the TE ripple of the plane of incidence as a example, can according to the seriality of interface With the Fresnel reflection coefficient deriving TE ripple it is :

[**0006**] Wherein, $\theta_0$For angle of incidence, $\theta_1$For the angle of emergence, $\theta_0$With $\theta_1$Meet :

[**0007**] Wherein $n_0$For the refractive index of incident medium, $n_1$Refractive index for emergent medium.Incident illumination with 650nm （TE ripple） From Air incidence, to silicon materials

surface, as shown in Figure 1 it can be deduced that TE wave reflection rate increases with the increase of angle of incidence, is said The sub- incident efficiency in Mingguang City is relevant with angle, the photon incident efficiency highest in vertical normal incidence direction.What generally people adopted is anti-reflection Film, according to anti-reflection film thickness be $\lambda/4$ when to wavelength the light transmission highest for $\lambda$, the two of one layer of 100nm of silicon materials superficial growth Silicon oxide is used for the incident illumination of anti-reflection 600nm, by equivalent to the silicon dioxide of 100nm and silicon materials become an interface, its admittance is Y, defining its eigenmatrix is :

[0008] Wherein, $n_1$And $n_2$It is respectively the refractive index of silicon dioxide and silicon,

[0009] For the phase thickness of silicon dioxide, $d_1$For the actual (real) thickness of silicon dioxide, Y=C/B, after therefore adding anti-reflection film Reflection coefficient is :

[0010] Wherein, $n_0$Refractive index for air.

[0011] Result of calculation as shown in fig. 2, it can be seen that increasing to 60 ° with angle of incidence from 0 °, to 600nm wavelength, absorbance It is reduced to 75% from 91%, transmittance peak wavelength, also with the centre wavelength of the increase off-design of angle, is reduced to from 600nm 470nm, absorbance constantly declines.

[0012] At present, all Radix Rumiciss photodetection is had strongly at aspects such as space optical communication, weak light detection, return laser beam detections Demand, such as diffuse-reflectance detection in space optical communication, return laser beam are dissipated due to the echo that laser beam divergence leads in detecting Penetrate etc. it is characterised in that the ranges of incidence angles of incident illumination is big, intensity is faint, and therefore these applications are required to photodetector in energy While the incident illumination of reception wider angle scope, there is high sensitivity and quantum efficiency.

[0013] Just because of current anti-reflection film design requirement incident illumination vertical incidence, in actual detection system, need extra Detector Rotable Control System, due to being limited by Rotable Control System speed, scan efficiency is too low, therefore it is further proposed that Form focal plane arrays (FPA) with the Focused Optical system of photodetector cooperation and by increasing detector, realize to all directions The detection of signal, but extra system not only increases the volume of whole photodetector module, more increases and realizes difficulty.

[0014] Content of the invention



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[0015] Present invention aim at solution above-mentioned technical problem, provide a kind of photodetector structure of Radix Rumiciss and preparation side Method.

[0016] The technical solution used in the present invention is :

[0017] A kind of preparation method of photodetector, comprises the steps :

[0018] Lithography step, makes the figure of structure photosurface again by lithography in the upper surface of photodetection structure,

[0019] Remove surface damage layer step, described photodetection structure is placed in 60-100 DEG C, in the KOH solution of 20wt%, goes Surface damage layer except about 10 μm being located at again in structure photosurface;

[0020] Structure step again, described photodetection structure is placed in 60-100 DEG C, the isopropanol mixing of KOH and 8vol% of 3wt% In solution, form Radix Rumiciss structure in structure photosurface again.

[0021] Preferably, also include the step protecting the region outside photosurface using photoresist in described lithography step;Described again The step removing the photoresist of protection is also included after structure step.

[0022] Preferably, also comprise the steps, under 800-1200 DEG C of wet oxygen environment after described removal photoresist step Front grows the SiO of $50nm_2$, photoetching simultaneously erodes region outside structure photosurface again, forms passivation layer.

[0023] Preferably, described Radix Rumiciss structure be described in structure photosurface again out-of-flatness surface, in order to make oblique incident ray contact institute The part of the reflected light producing after stating again structure photosurface enters in described photodetection structure as oblique incident ray again.

[0024] Preferably, the out-of-flatness surface of the described photosurface of structure again is the continuous section of rule.

[0025] Preferably, the continuous section of the described photosurface of structure again is taper, trapezoidal, rectangle, spherical, bulb-shaped recess shape, its figure Shape dutycycle 50% to 100%.

[0026] Present invention further teaches a kind of Radix Rumiciss photodetector, including for producing photoelectric photodetection structure, The upper surface of described photodetection structure is provided with structure photosurface again, and the upper surface of the described photosurface of structure again is used for out-of-flatness surface So that the part of the reflected light producing after structure photosurface again described in oblique incident ray contact enter to as oblique incident ray again described In photodetection structure.

[0027] Preferably, the upper surface of the described photosurface of structure again is additionally provided with passivation layer, described passivation layer cover all described in again Structure photosurface, the material of described passivation layer is $SiO_2$、$SiN_x$、$MgF_2$、ITO.

[0028] Preferably, the described photosurface of structure again can be applicable to by silicon, polysilicon, GaAs, GaN, InP, SiC, ZnO, SOI, tellurium In the photodetection structure of cadmium mercury preparation.

[0029] Preferably, described photodetection structure is the avalanche photodetector of linear model and Geiger mode angular position digitizer, or is PIN light Electric explorer, or be MSM photoelectric detector.

[0030] The beneficial effects of the present invention is: Provide a kind of preparation method of Radix Rumiciss photodetector, high efficient and reliable, pass through In photodetector surfaces structure again, break the restriction of Fresnel reflection coefficient angle of incidence, reduce the sensitivity to incident wavelength, no Extra system need to be added, only Radix Rumiciss are realized by single photodetector and detect.

[0031] Brief description

[0032] Below in conjunction with the accompanying drawings and embodiment the invention will be further described:

[0033] Fig. 1:, from air incidence to silicon materials surface, reflectance is with the change curve of angle of incidence for TE ripple.

[0034] Fig. 2: SiO containing 100nm$_2$The transmission of the incident illumination to 0 °, 30 ° and 60 ° angle of incidence for the silicon materials substrate of anti-reflection film is bent Line chart.

[0035] Fig. 3: The structural representation of the Radix Rumiciss photodetector of the present invention.



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[0036] Fig. 4 : Input path schematic diagram on the photosurface of structure again of the present invention for the oblique incident ray.

[0037] Fig. 5 to Fig. 9 : The cross-sectional schematic of the photosurface of structure again of the present invention.

[0038] Figure 10 : The corresponding profile of each step of the preparation method of Radix Rumiciss photodetector of the present invention.

[0039] Specific embodiment

[0040] Present invention is disclosed a kind of Radix Rumiciss photodetector, its structure is as shown in figure 3, include successively from top to bottom : Passivation Layer 101, again structure photosurface 102 and photodetection structure 103.Described photodetection structure 103 is used for producing photoelectric effect, and this is Prior art, will not be described here.In conjunction with shown in Fig. 4, the upper surface of the described photosurface of structure again 102 is out-of-flatness surface in order to make The part of the reflected light producing after structure photosurface 102 again described in oblique incident ray contact enters to described light as oblique incident ray again In electrical resistivity survey geodesic structure 103, described passivation layer 101 envelope completely described in structure photosurface 102 again.

[0041] Specifically, when incident illumination incides the photosurface of structure again 102 of photodetection structure 103 according to certain angle, due to At incidence point, actual incident angle changes, and reduces actual incident angle for inclined plane, therefore, it is possible to improve tilt into Penetrate the absorbance of light.Meanwhile, the light of reflection reflects in multiple interfaces, increases the probability being transmitted into quasiconductor, thus Increase absorbance, break the restriction of Fresnel reflection coefficient angle of incidence, reduce the sensitivity to incident wavelength, realize Radix Rumiciss and visit Survey.

[0042] The photosurface of structure again 102 in the present invention, can be carved by chemical attack, laser grooving, reactive ion etching, machinery The methods such as groove, epitaxial growth are formed, deeper 0.1 μm to 50 μm of structure structure.The surface topography of the described photosurface of structure again is rule Continuous section, can be taper as disclosed in Fig. 5 to Fig. 9, trapezoidal, rectangle, spherical, bulb-shaped recess etc., its figure dutycycle 50% To 100%.

[0043] The photodetection structure 103 of the present invention can by structure photosurface 102 again increase passivation layer 101 repair because The surface damage that structure introduces again, reduces surface recombination, reduces dark current.And, because described passivation layer



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101 has certain thickness Degree, between 1nm to 10 μm, therefore it can be used as a kind of presence of anti-reflection film.This passivation layer 101 material can be $SiO_2$、 $SiN_x$、$MgF_2$, ITO etc..Certainly, if being in the consideration of cost, this passivation layer 101 can also be saved, that is, Radix Rumiciss photodetector is only Only include photodetection structure and the structure photosurface again being provided thereon, at least part of surface of the described photosurface of structure again is out-of-flatness Surface, in order to make oblique incident ray contact described in the part of reflected light that produces after structure photosurface 102 again again as oblique incident ray Enter in described photodetection structure 103.

[0044] The photosurface of structure again 102 of the present invention is applied to by silicon, polysilicon, GaAs, GaN, InP, SiC, ZnO, SOI, tellurium cadmium The photodetector of the various material such as hydrargyrum preparation.

[0045] The photosurface of structure again 102 of the present invention is applied to the avalanche photodetector of linear model and Geiger mode angular position digitizer, is also suitable In PIN photoelectric detector, MSM photoelectric detector etc..

[0046] The preparation method of the Radix Rumiciss photodetector of the present invention once is described below.

[0047] As shown in Figure 10, photodetection structure 103 adopts the PIN photoelectric detector that the silicon materials of N-shaped doping manufacture, its Structure photosurface 102 forms as a example taper by the method by chemical attack again, and preparation process and method are as follows:

[0048] Step (a), make the figure of structure photosurface 102 again by lithography in the upper surface of photodetection structure 103, using photoresist Region outside 104 protection photosurfaces 102;

[0049] Step (b), the photodetection structure 103 protected using photoresist 104 is placed in 60-100 DEG C, the KOH of 20wt% is molten A period of time is processed in liquid (About 40 seconds), remove the surface damage layer of about 10 μm being located at again in structure photosurface 102;

[0050] Step (c), the photodetection structure 103 protected using photoresist 104 is placed in 60-100 DEG C, the KOH of 3wt% and A period of time is processed in the isopropyl alcohol mixture of 8vol % (About 30 minutes), form inverted pyramid in structure photosurface 102 again Radix Rumiciss structure;

**[0051]** Step (d) , remove the photoresist 104 of protection, front growth 50nm under 800-1200 DEG C of the wet oxygen environment $SiO_2$, photoetching simultaneously erodes region outside structure photosurface 102 again, forms passivation layer 101, that is, obtain the preferred embodiment of the present invention Radix Rumiciss photodetector.

**[0052]** All technical sides that the present invention still has numerous embodiments, all employing equivalents or equivalent transformation and formed Case, is within the scope of the present invention.

1. 1. a kind of preparation method of photodetector it is characterised in that : Comprise the steps, Lithography step, makes the figure of structure photosurface (102) by lithography in the upper surface of photodetection structure (103) again, removes surface Damage layer step, described photodetection structure (103) is placed in 60-100 DEG C, in the KOH solution of 20wt%, remove and be located at structure again The surface damage layer of about 10 μm in photosurface (102) ;
   Structure step again, described photodetection structure (103) is placed in 60-100 DEG C, and the isopropanol of KOH and 8vol% of 3wt% mixes Close in solution, form Radix Rumiciss structure in structure photosurface (102) again, described Radix Rumiciss structure is the described photosurface of structure again (102) The continuous section of rule, in order to make oblique incident ray contact described in structure photosurface (102) produces afterwards again reflected light again as oblique Penetrate light to enter in described photodetection structure (103).
2. 2. photodetector according to claim 1 preparation method it is characterised in that : Also include in described lithography step The step protecting again structure photosurface (102) region outward using photoresist (104) ; Also include removing after the described step of structure again protecting The step of the photoresist (104) of shield.
3. 3. photodetector according to claim 2 preparation method it is characterised in that : Described removal photoresist step it Also comprise the steps afterwards, under 800-1200 DEG C of wet oxygen environment, front grows the SiO of 50nm$_2$, photoetching simultaneously erodes structure again Photosurface (102) region outward, forms passivation layer (101).
4. 4. the preparation method according to the arbitrary described photodetector of claim 1-3 it is characterised in that : Described structure photosurface again (102) continuous section is taper, trapezoidal, rectangle, spherical, bulb-shaped recess shape, its figure dutycycle 50% to 100%.
5. 5. a kind of Radix Rumiciss photodetector of preparation method according to claim 1 preparation it is characterised in that : Including for Produce photoelectric photodetection structure (103), the upper surface of described photodetection structure (103) is provided with structure photosurface again (102), the upper surface of the described photosurface of structure again (102) be out-of-flatness surface in order to make oblique incident ray contact described in structure light again The reflected



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light that quick face (102) produces afterwards enters in described photodetection structure (103) as oblique incident ray again.

6. 6. Radix Rumiciss photodetector according to claim 5 it is characterised in that : The upper table of the described photosurface of structure again (102) Face is additionally provided with passivation layer (101), described passivation layer (101) cover all described in structure photosurface (102) again, described passivation layer (101) material is $SiO_2$、SiNx、$MgF_2$Or ITO.
7. 7. Radix Rumiciss photodetector according to claim 6 it is characterised in that : The described photosurface of structure again (102) can be applied In the photodetection structure (103) prepared by silicon, polysilicon, GaAs, GaN, InP, S iC, ZnO, SOI or mercury cadmium telluride.
8. 8. Radix Rumiciss photodetector according to claim 7 it is characterised in that : Described photodetection structure (103) is line Sexual norm and the avalanche photodetector of Geiger mode angular position digitizer, or be PIN photoelectric detector, or be MSM photoelectric detector.



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(73)专利权人 苏州北鹏光电科技有限公司
地址 215021 江苏省苏州市工业园区金鸡湖大道99号纳米城中北区23幢

(72)发明人 郭霞 周弘毅 郭春威 李冲

(74)专利代理机构 南京苏科专利代理有限责任公司 32102
代理人 陆明耀 姚姣阳

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审查员 周洁

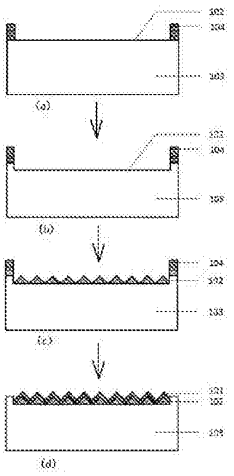
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(54)发明名称

光电探测器制备方法及制备的广角光电探测器

(57)摘要

本发明公开了一种光电探测器的制备方法，包括如下步骤：在光电探测结构的上表面光刻出再构光敏面的图形，去除位于再构光敏面内的表面损伤层，在再构光敏面内形成广角结构。本发明的有益效果在于：提供了一种广角光电探测器的制备方法，高效可靠，通过在光电探测器表面再构，打破菲涅尔反射系数入射角的限制，降低对入射波长的敏感度，不需加入额外的系统，仅通过单个光电探测器实现广角探测。



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1.一种光电探测器的制备方法,其特征在于:包括如下步骤,

光刻步骤,在光电探测结构(103)的上表面光刻出再构光敏面(102)的图形,去除表面损伤层步骤,将所述光电探测结构(103)置于60-100℃,20wt%的KOH溶液中,去除位于再构光敏面(102)内的大约10μm的表面损伤层;

再构步骤,将所述光电探测结构(103)置于60-100℃,3wt%的KOH及8vol%的异丙醇混合溶液中,在再构光敏面(102)内形成广角结构,所述广角结构为所述再构光敏面(102)的规则连续截面,用以使斜入射光接触所述再构光敏面(102)后产生的反射光再次作为斜入射光进入至所述光电探测结构(103)内。

2.根据权利要求1所述的光电探测器的制备方法,其特征在于:所述光刻步骤中还包括使用光刻胶(104)保护再构光敏面(102)外的区域的步骤;所述再构步骤之后还包括去除保护用的光刻胶(104)的步骤。

3.根据权利要求2所述的光电探测器的制备方法,其特征在于:所述去除光刻胶步骤之后还包括如下步骤,在800-1200℃的湿氧环境下正面生长50nm的$SiO_2$,光刻并腐蚀掉再构光敏面(102)外的区域,形成钝化层(101)。

4.根据权利要求1-3任一所述的光电探测器的制备方法,其特征在于:所述再构光敏面(102)的连续截面为锥形、梯形、矩形、球形、球形凹陷形,其图形占空比50%到100%。

5.一种根据权利要求1所述的制备方法制备的广角光电探测器,其特征在于:包括用于产生光电效应的光电探测结构(103),所述光电探测结构(103)的上表面上设有再构光敏面(102),所述再构光敏面(102)的上表面为不平整表面用以使斜入射光接触所述再构光敏面(102)后产生的反射光再次作为斜入射光进入至所述光电探测结构(103)内。

6.根据权利要求5所述的广角光电探测器,其特征在于:所述再构光敏面(102)的上表面还设有钝化层(101),所述钝化层(101)完全覆盖住所述再构光敏面(102),所述钝化层(101)的材料为$SiO_2$、SiNx、$MgF_2$或ITO。

7.根据权利要求6所述的广角光电探测器,其特征在于:所述再构光敏面(102)可应用于由硅、多晶硅、GaAs、GaN、InP、S iC、ZnO、SOI或碲镉汞制备的光电探测结构(103)上。

8.根据权利要求7所述的广角光电探测器,其特征在于:所述光电探测结构(103)为线性模式和盖革模式的雪崩光电探测器,或为PIN光电探测器,或为MSM光电探测器。



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# 光电探测器制备方法及制备的广角光电探测器

## 技术领域

[0001] 本发明涉及一种光电探测器制备方法及制备的广角光电探测器，属于半导体光电子技术领域。

## 背景技术

[0002] 光电探测器在生物医学、数据存储媒介、火焰监测、紫外线剂量测量、高能射线探测、医疗、安检、工业探伤等领域得到广泛应用。当入射光能量大于光电探测器材料禁带宽度时，就会使得电子从价带跃迁至导带，产生电子空穴对，产生的电子空穴对被电极收集，就形成了光电流输出。量子效率是衡量光电探测器的一个最重要的性能指标之一，主要由光子入射效率、内量子效率和载流子收集效率决定。由于半导体和空气的折射率差大，相当的光被界面反射，无法进入到器件中被收集，导致器件效率降低。通常根据入射光和反射光的干涉相消原理，设计并制备增透膜，使得单一波长的垂直入射光入射效率达到95%以上。然而这种设计带来的一个问题是，当入射波长偏移设计波长，或者入射角偏离垂直方向，探测效率急剧下降。

[0003] 根据电磁场理论，以对于电场垂直于入射面的TE波为例，根据界面处的连续性可以推导出TE波的菲涅尔反射系数为：

[0004] $$r_{TM}=\frac{\sin(\theta_1-\theta_0)}{\sin(\theta_1+\theta_0)}$$

[0005] 其中，$\theta_0$为入射角，$\theta_1$为出射角，$\theta_0$与$\theta_1$满足：

[0006] $$n_1\sin\theta_1=n_0\sin\theta_0$$

[0007] 其中$n_0$为入射介质的折射率，$n_1$为出射介质的折射率。以650nm的入射光(TE波)从空气入射至硅材料表面为例，如图1所示，可以得出TE波反射率随入射角的增加而增加，说明光子入射效率与角度有关，垂直正入射方向的光子入射效率最高。通常人们采用的增透膜，根据增透膜厚度为λ/4时对波长为λ的光透射率最高，在硅材料表面生长一层100nm的二氧化硅用于增透600nm的入射光，将100nm的二氧化硅和硅材料等效成一个界面，其导纳为Y，定义其特征矩阵为：

[0008] $$\begin{bmatrix}B\\C\end{bmatrix}=\begin{bmatrix}\cos\delta_1 & \frac{i}{n_1}\sin\delta_1\\ in_1\sin\delta_1 & \cos\delta_1\end{bmatrix}\begin{bmatrix}1\\n_2\end{bmatrix}$$

[0009] 其中，$n_1$和$n_2$分别为二氧化硅和硅的折射率，

[0010] $$\delta_1=\frac{2\pi}{\lambda}n_1d_1\cos\theta_1$$

[0011] 为二氧化硅的相位厚度，$d_1$为二氧化硅的实际厚度，Y=C/B，因此加入增透膜后的反射系数为：

[0012] $$r=\frac{n_0-Y}{n_0+Y}$$



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[0013] 其中，$n_0$为空气的折射率。

[0014] 计算结果如图2所示，可以看出，随着入射角从0°增加到60°，对600nm波长，透射率从91%降低到75%，透射率峰值波长也随着角度的增加偏离设计的中心波长，从600nm降低至470nm，透射率不断下降。

[0015] 目前，在空间光通信、弱光探测、激光回波探测等方面均对广角光电探测有着强烈的需求，例如空间光通信中的漫反射探测、激光回波探测中由于激光发散角导致的回波散射等，其特征在于入射光的入射角范围大，强度微弱，因此这些应用均要求光电探测器在能接收较宽角度范围的入射光的同时，具有高的灵敏度及量子效率。

[0016] 正是由于目前增透膜设计要求入射光垂直入射，在实际探测系统中，需要额外的探测器旋转控制系统，由于受到旋转控制系统速度的限制，扫描效率太低，因此进一步提出了与光电探测器配合的聚焦光学系统及通过增加探测器组成焦平面阵列，实现对各个方向信号的探测，但是额外的系统不仅提高了整个光电探测器模块的体积，更加大了实现难度。

## 发明内容

[0017] 本发明目的在于解决上述技术问题，提供一种广角的光电探测器结构及制备方法。

[0018] 本发明采用的技术方案是：

[0019] 一种光电探测器的制备方法，包括如下步骤：

[0020] 光刻步骤，在光电探测结构的上表面光刻出再构光敏面的图形，

[0021] 去除表面损伤层步骤，将所述光电探测结构置于60-100℃，20wt%的KOH溶液中，去除位于再构光敏面内的大约10μm的表面损伤层；

[0022] 再构步骤，将所述光电探测结构置于60-100℃，3wt%的KOH及8vol%的异丙醇混合溶液中，在再构光敏面内形成广角结构。

[0023] 优选的，所述光刻步骤中还包括使用光刻胶保护光敏面外的区域的步骤；所述再构步骤之后还包括去除保护用的光刻胶的步骤。

[0024] 优选的，所述去除光刻胶步骤之后还包括如下步骤，在800-1200℃的湿氧环境下正面生长50nm的$SiO_2$，光刻并腐蚀掉再构光敏面外的区域，形成钝化层。

[0025] 优选的，所述广角结构为所述再构光敏面的不平整表面，用以使斜入射光接触所述再构光敏面后产生的反射光的部分再次作为斜入射光进入至所述光电探测结构内。

[0026] 优选的，所述再构光敏面的不平整表面为规则的连续截面。

[0027] 优选的，所述再构光敏面的连续截面为锥形、梯形、矩形、球形、球形凹陷形，其图形占空比50%到100%。

[0028] 本发明还揭示了一种广角光电探测器，包括用于产生光电效应的光电探测结构，所述光电探测结构的上表面上设有再构光敏面，所述再构光敏面的上表面为不平整表面用以使斜入射光接触所述再构光敏面后产生的反射光的部分再次作为斜入射光进入至所述光电探测结构内。

[0029] 优选的，所述再构光敏面的上表面还设有钝化层，所述钝化层完全覆盖住所述再构光敏面，所述钝化层的材料为$SiO_2$、$SiN_x$、$MgF_2$、ITO。

[0030] 优选的，所述再构光敏面可应用于由硅、多晶硅、GaAs、GaN、InP、SiC、ZnO、SOI、磷



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镉汞制备的光电探测结构上。

[0031] 优选的，所述光电探测结构为线性模式和盖革模式的雪崩光电探测器，或为PIN光电探测器，或为MSM光电探测器。

[0032] 本发明的有益效果在于：提供了一种广角光电探测器的制备方法，高效可靠，通过在光电探测器表面再构，打破菲涅尔反射系数入射角的限制，降低对入射波长的敏感度，不需加入额外的系统，仅通过单个光电探测器实现广角探测。

## 附图说明

[0033] 下面结合附图及实施例对本发明作进一步描述：

[0034] 图1：TE波从空气入射至硅材料表面，反射率随入射角的变化曲线图。

[0035] 图2：含100nm $SiO_2$增透膜的硅材料衬底对0°、30°及60°入射角的入射光的透射曲线图。

[0036] 图3：本发明的广角光电探测器的结构示意图。

[0037] 图4：斜入射光在本发明的再构光敏面上的入射光路示意图。

[0038] 图5至图9：本发明的再构光敏面的剖视示意图。

[0039] 图10：本发明的广角光电探测器的制备方法的各个步骤对应的剖面图。

## 具体实施方式

[0040] 本发明揭示了一种广角光电探测器，其结构如图3所示，自上而下依次包括：钝化层101、再构光敏面102和光电探测结构103。所述光电探测结构103用于产生光电效应，此为现有技术，在此不再赘述。结合图4所示，所述再构光敏面102的上表面为不平整表面用以使斜入射光接触所述再构光敏面102后产生的反射光的部分再次作为斜入射光进入至所述光电探测结构103内，所述钝化层101完全包覆住所述再构光敏面102。

[0041] 具体的，当入射光按照一定角度入射到光电探测结构103的再构光敏面102，由于入射点处实际入射角度发生变化，对于倾斜面降低了实际入射角度，因此能够提高倾斜入射光的透射率。与此同时，反射的光在多个界面中反射，增加透射进入半导体的几率，从而增加透射率，打破菲涅尔反射系数入射角的限制，降低对入射波长的敏感度，实现广角探测。

[0042] 本发明中的再构光敏面102，可以由化学腐蚀、激光刻槽、反应离子刻蚀、机械刻槽、外延生长等方法形成，再构结构深0.1μm到50μm。所述再构光敏面的表面形貌为规则的连续截面，可以为如图5至图9揭示的锥形、梯形、矩形、球形、球形凹陷等，其图形占空比50%到100%。

[0043] 本发明的光电探测结构103可以通过在再构光敏面102上增加钝化层101来修复因再构引入的表面损伤，降低表面复合，降低暗电流。并且，由于所述钝化层101具有一定的厚度，在1nm到10μm之间，因此其可以作为一种增透膜的存在。该钝化层101材料可以为$SiO_2$、$SiN_x$、$MgF_2$、ITO等。当然，如果处于成本的考虑，也可省去该钝化层101，即广角光电探测器仅仅包括光电探测结构和设于其上的再构光敏面，所述再构光敏面的至少部分表面为不平整表面，用以使斜入射光接触所述再构光敏面102后产生的反射光的部分再次作为斜入射光进入至所述光电探测结构103内。



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[0044] 本发明的再构光敏面102适用于由硅、多晶硅、GaAs、GaN、InP、SiC、ZnO、SOI、碲镉汞等各种材料制备的光电探测器。

[0045] 本发明的再构光敏面102适用于线性模式和盖革模式的雪崩光电探测器，也适用于PIN光电探测器、MSM光电探测器等。

[0046] 下面描述一下本发明的广角光电探测器的制备方法。

[0047] 如附图10所示，光电探测结构103采用n型掺杂的硅材料制造的PIN光电探测器，其再构光敏面102以通过化学腐蚀的方法形成锥形为例，制备过程和方法如下：

[0048] 步骤(a)、在光电探测结构103的上表面光刻出再构光敏面102的图形，使用光刻胶104保护光敏面102外的区域；

[0049] 步骤(b)、将使用光刻胶104保护的光电探测结构103置于60-100℃，20wt%的KOH溶液中处理一段时间(大约40秒)，去除位于再构光敏面102内的大约10μm的表面损伤层；

[0050] 步骤(c)、将使用光刻胶104保护的光电探测结构103置于60-100℃，3wt%的KOH及8vol%的异丙醇混合溶液中处理一段时间(大约30分钟)，在再构光敏面102内形成倒金字塔的广角结构；

[0051] 步骤(d)、去除保护用的光刻胶104，在800-1200℃的湿氧环境下正面生长50nm的$SiO_2$，光刻并腐蚀掉再构光敏面102外的区域，形成钝化层101，即得到本发明优选实施例的广角光电探测器。

[0052] 本发明尚有多种实施方式，凡采用等同变换或者等效变换而形成的所有技术方案，均落在本发明的保护范围之内。



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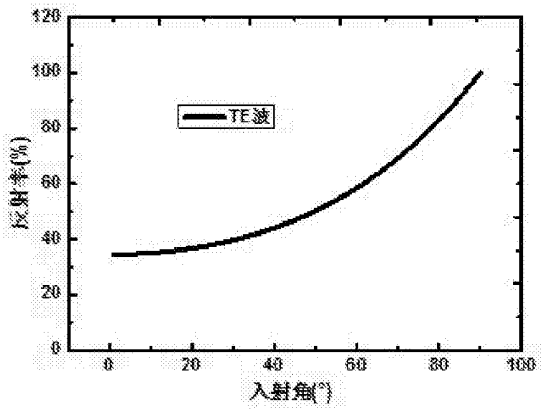



图1

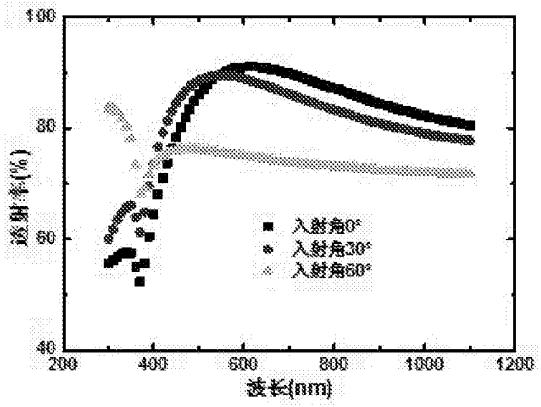



图2

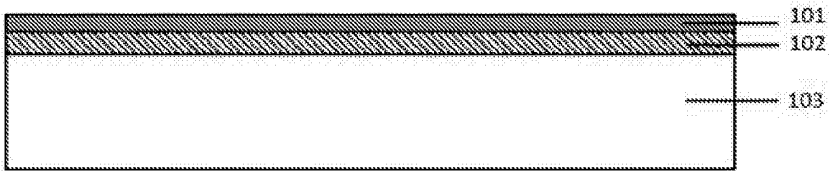



图3



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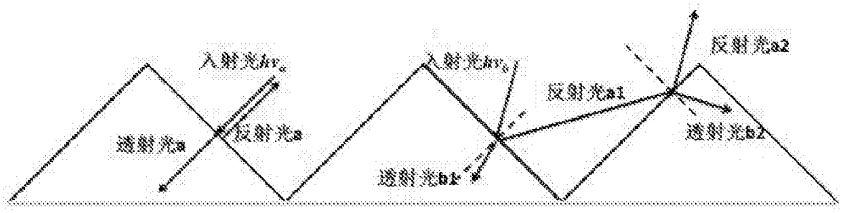



图4

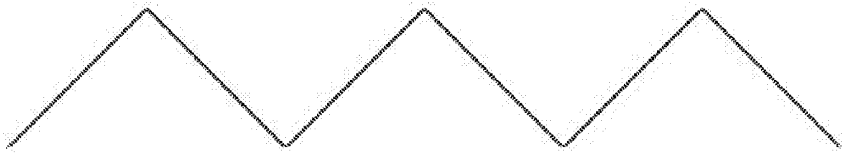


图5



图6

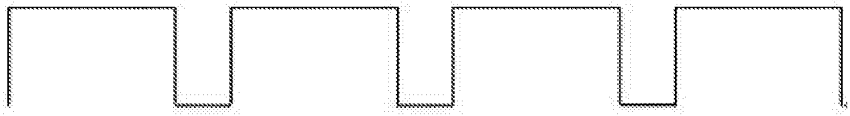


图7



图8



图9



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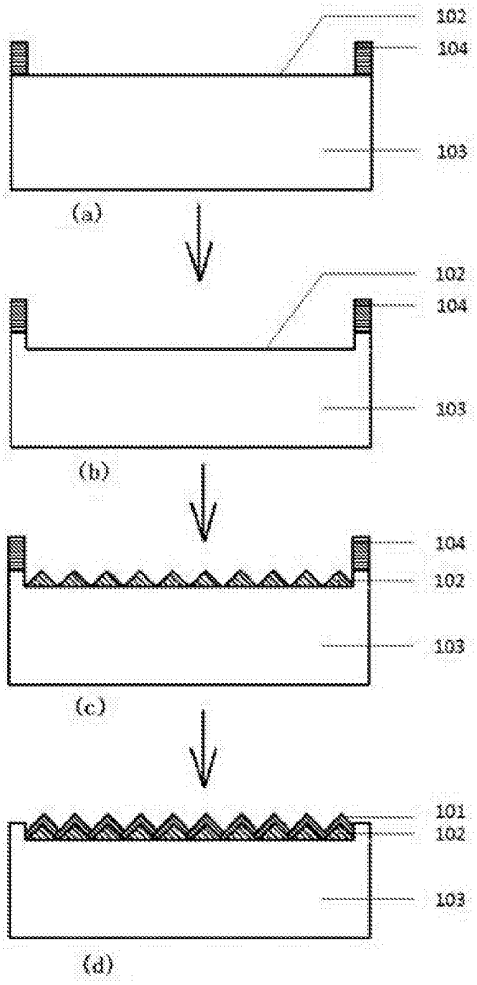



图10



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Attorney Docket No.: 309-0015USCIP **PATENT**
Confirmation No.: 7381

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | |
|---|---|
| In re Application of:<br>Shih-Yuan WANG<br><br>Application No.: 18/385,213<br><br>Filed: October 30, 2023<br><br>Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | Examiner: EDUARDO A RODELA<br><br>Art Unit: 2893<br><br>**CERTIFICATE OF TRANSMISSION**<br>I hereby certify that this correspondence is being submitted through the USPTO Electronic Filing Service addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450<br>/Mary Ellen Finnegan/<br>Date: March 13, 2024 Name: Mary Ellen Finnegan |

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SIR:

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

It is respectfully requested that the documents listed on the attached Information Disclosure Citation form PTO/SB/08a be considered by the Patent Examiner in connection with the above-identified application and be made of record therein.

A copy of the non-U.S. patent document is enclosed herewith, in compliance with 37 CFR 1.98.

Independent consideration and acknowledgement of the enclosed document are respectfully requested.

The Commissioner is hereby authorized to charge U.S. PTO Deposit Account 600125 any payment due and to credit any overpayment thereto.

Respectfully submitted,

/Ivan S. Kavrukov/
Ivan S. Kavrukov
Registration No. 25,161
Attorney for Applicant

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001
Attorney's Telephone No.: 917-945-0121
Attorney's E-mail: ikavrukov@wissingmiller.com

# Lateral semiconductor photodetector of pin structure


## Abstract

PROBLEM TO BE SOLVED: To provide a PIN structure lateral semiconductor photodetector which is improved in sensitivity for detecting light without deteriorating its response speed. SOLUTION: A lateral semiconductor photodetector of PIN structure has interfaces at an I layer 15, a P layer 5, and an N layer, the interfaces are set vertical to the surface of a semiconductor substrate, light impinging on the I layer 15 is converted into a current, and the current is detected. A hole 4 is bored in a light receiving region 2 from a light receiving surface 3 to a certain point as deep as prescribed inside the I layer 15



JP2002314116A
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**Other languages:** Japanese

**Inventor:** Atsushi Harada, 篤 原田, Tsugio Ide, 次男 井出, Shojiro Kitamura, 象二郎 北村

**Current Assignee :** Seiko Epson Corp

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**Info:** Cited by (7), Legal events, Similar documents, Priority and Related Applications

**External links:** Espacenet, Global Dossier, Discuss


## Claims (1)

Hide Dependent
translated from Japanese

[Claims] 1. A lateral semiconductor light receiving device wherein an interface between an I-layer, a p-layer, and an n-layer having a PIN structure is formed perpendicular to a surface of a semiconductor substrate, and converts light incident on the I-layer into current and detects the current. A lateral semiconductor light-receiving element having a PIN structure, wherein a hole extending from the light-receiving surface to a predetermined depth of the I-layer is provided in the light-receiving region.

## Description

translated from Japanese

DETAILED DESCRIPTION OF THE INVENTION

[0001]

The present invention relates to a lateral semiconductor light receiving device having a PIN structure.

[0002]

2. Description of the Related Art In a vertical photodiode in which a pn junction surface is formed parallel to a semiconductor substrate surface, light is incident on a depletion layer through a p-layer or an n-layer.
In a lateral photodiode in which the n-junction surface is formed perpendicular to the semiconductor substrate surface, light is directly incident on the depletion layer (not through the p-layer or the n-layer). For this reason, lateral photodiodes are better than vertical photodiodes.
This is advantageous in light receiving efficiency.

Conventionally, in a photodiode,
An I layer (intrinsic layer) is provided between a p layer and an n layer to increase the thickness of a depletion layer. In a vertical photodiode having such a PIN structure, the I-layer is formed to have a thickness equal to or more than the absorption length in order to increase the light receiving sensitivity. As a result, a quantum efficiency of 70% or more can be obtained at a wavelength of about 700 nm to 870 nm.

Lateral photodiode having a PIN structure (a photodiode in which an interface between an I-layer, a p-layer, and an n-layer having a PIN structure is formed perpendicular to a semiconductor substrate surface)
For example, after a region having an extremely low impurity concentration forming an I-layer is provided in a surface layer portion of a semiconductor substrate, a p-type impurity and an n-type impurity are added to respective positions of this region at predetermined intervals from an upper surface. To form a p-layer and an n-layer, and leave an I-layer between both layers

Therefore, in the case of a lateral photodiode having a PIN structure, the thickness of the I-layer (depth from the light incident surface)
in order to increase p, it is necessary to form the p-layer and the n-layer deeply. In order to form the p-layer and the n-layer deep while keeping the width of the I-layer (the distance between the p-layer and the n-layer) uniform in the thickness direction of the substrate, the p-layer and the n-layer on the substrate surface must be If is

necessary to increase the distance. When the distance between the p-layer and the n-layer on the substrate surface is increased, the width of the i-layer increases. If the width of the i-layer is large, the movement distance of electrons generated on the p-layer side of the i-layer to reach the electrode of the n-layer increases, and the response speed decreases.

Therefore, in the lateral type photodiode having the PIN structure, as a method for increasing the light receiving sensitivity, simply increasing the thickness of the i-layer (the depth from the light incident surface) cannot be simply employed. Therefore, PIN
As a method for increasing the light receiving sensitivity of the lateral type photodiode having the structure, it is effective to provide an antireflection film on the upper surface of the i-layer to increase the efficiency of incidence on the i-layer.

[0007]

However, a lateral type photodiode having a PIN structure having an antireflection film on the upper surface of the i-layer has a problem that the response speed is low when an element for receiving a high-speed signal is used. There is. SUMMARY OF THE INVENTION The present invention has been made in view of such a problem of the related art, and it is an object of the present invention to improve the light receiving sensitivity without lowering the response speed in a lateral semiconductor light receiving element having a PIN structure.

[0008]

In order to solve the above-mentioned problems, the present invention provides a semiconductor device having an i-layer having a PIN structure in which an interface between a p-layer and an n-layer is formed perpendicular to a semiconductor substrate surface. In a lateral type semiconductor light receiving element for detecting incident light by converting the light into a current, a hole extending from the light receiving surface to a predetermined depth of the i layer (a position shallower than the depths of the p layer and the n layer) is provided in the light receiving region. A lateral type semiconductor light receiving element having a PIN structure is provided.

[0009]

Embodiments of the present invention will be described below. FIG. 1 is a sectional view showing a photodiode corresponding to one embodiment of the present invention. FIG. 2 is a diagram showing an example of a planar shape when the photodiodes of this embodiment are formed in an array. FIG. 1 corresponds to a sectional view taken along line AA of FIG.

This photodiode is a lateral photodiode (semiconductor light receiving element) having a PIN structure formed perpendicular to the substrate surface of a silicon substrate (semiconductor substrate) 1 and has a light receiving region (p layer of i layer 15). A hole 4 extending in a direction perpendicular to the surface of the silicon substrate 1 from the light receiving surface 3 to a predetermined depth of the i-layer 15 is provided in a region (a region between the n-layer 5 and the n-layer 7).

On the upper surfaces of the p layer 5 and the n layer 7, a p electrode 6
And an n electrode 8 are formed. On the lower surface of the silicon substrate 1, a p-electrode 11 is formed. An element protection layer 9 made of a silicon oxide film or the like is provided on the upper surface of the silicon substrate 1 except for the positions of the electrodes 6 and 8 and the hole 4.
is formed with a predetermined thickness. This photodiode can be manufactured, for example, by the following method.

First, n is added to the surface layer of the p-type silicon substrate 1.
A well (a region having an extremely low impurity concentration) 10 is provided.
Next, a p-type impurity is added to one of the two regions of the n-well 10 at a predetermined interval, and an n-type impurity is added to the other, and diffused. As a result, the p layer 5 and the n layer 7 are formed in the n well 10, and the portion between the p layer 5 and the n layer 7 of the n well 10 remains as the i layer 15. Next, after forming the electrodes 6 and 8 on the p-layer 5 and the n-layer 7, the element protection layer 9 is formed.

Next, a focused ion beam processing apparatus (FI
Using B), a portion of the upper surface of the silicon substrate 1 sandwiched between the electrodes 6 and 8 is irradiated with an ion beam, and the element protection layers 9 and i are irradiated.
By etching the layer 15, a hole 4 extending in the thickness direction of the silicon substrate 1 from the light receiving surface 3 to a predetermined depth of the i layer 15 (a position shallower than the depths of the p layer 5 and the n layer 7) is formed.

Here, the dimension of the hole 4 in the direction between the p layer 5 and the n layer 7 is determined between the hole 4 and the p layer 5 and between the hole 4 and the n layer 7. is set to the dimension where exists. When the light receiving surface 3 between each pair of electrodes is large, it is preferable to provide a plurality of holes 4 in the light receiving surface 3 as shown in FIG. In this case, for example, the width W of the electrodes 6 and 8
1 is 1 μm, the interval W2 between the electrodes 6 and 8 is 2 to 4 μm, and the hole 4
is 2 to 4 μm, and the diameter of the hole 4 is 1 μm.

In this photodiode, a power supply is connected between the n-electrode 8 in contact with the upper surface of the n-layer 7 and the p-electrode 11 on the lower surface of the substrate 1 with the n-layer 7 side being positive and a reverse bias voltage applied. Then, by connecting the p-electrode 6 in contact with the upper surface of the p-layer 5 to the output circuit, light incident on the i-layer 15 from the light receiving surface 3 can be converted into a current and detected. Also,
In this photodiode, the light (partially shown by a two-dot chain line in FIG. 1) that has entered the hole 4 from the light receiving surface 3 directly enters the light receiving region 2 from the bottom or side surface of the hole 4 and By being reflected on the side surface, the light is incident on the light receiving region 2 from the bottom surface to the side surface, or is incident on the light receiving region 2 from the side surface toward the opposing side surface. Therefore, the light receiving efficiency in the light receiving region 2 is higher than in the case where there is no hole 4.

If the light receiving surface 3 is simply enlarged without providing the hole 4 in order to increase the light receiving area, it takes a long time for electrons generated on the p layer side of the i layer to reach the electrode of the n layer. As the parasitic capacitance increases, the response speed decreases. In contrast, in this photodiode, By providing the hole 4, the light receiving area is larger by the side surface of the hole 4 than when no hole 4 is provided. Therefore, in this photodiode, electrons generated on the p-layer side of the i-layer are n
The movement time until reaching the electrode of the layer is not longer than when the light receiving surface 3 is the same size and the hole 4 is not provided.
The parasitic capacitance of the photodiode is smaller than that in the case where the light receiving surface 3 has the same size and the hole 4 is not provided. For these reasons, according to this photodiode, the light receiving area can be increased and the light receiving efficiency can be increased without reducing the response speed.

Further, since the photodiode has the hole 4, the intensity of the electric field applied to the peripheral portion of the hole 4 of the i-layer 15 is locally increased. This allows
Since holes and electrons generated by absorbing light in the peripheral portion of the hole 4 of the i-layer 15 can move at high speed through the i-layer 15,
The response speed is faster than the case without the hole 4. Therefore, according to this photodiode, by providing the hole 4, the light receiving efficiency in the light receiving region 2 is increased, the light receiving sensitivity is improved, and the response speed is also increased.

in this embodiment, a lateral type photodiode having a PiN structure is described. However, the lateral type semiconductor light receiving element having a PIN structure of the present invention is not limited to this. It is also applied to the lateral type phototransistor and the like.

[0019]

As described above, according to the lateral semiconductor light receiving device having the PIN structure of the present invention, the light receiving sensitivity can be improved without lowering the response speed.

**[Brief description of the drawings]**

FIG. 1 is a cross-sectional view showing a photodiode corresponding to an embodiment of the present invention, and is a view corresponding to a cross-sectional view taken along line AA of FIG.

FIG. 2 is a diagram showing an example of a planar shape when the photodiodes of FIG. 1 are formed in an array.

**[Explanation of symbols]**

REFERENDE SIGNS LIST 1 silicon substrate (semiconductor substrate) 10 n-well 11 p-electrode 15 i-layer 2 light-receiving area 3 light-receiving surface 4 hole 5 p-layer 6 p-electrode 7 n-layer 8 n-electrode 9 element protection layer

---------- Continuing on the front page (72) Inventor Shojiro Kitamura 3-3-5 Yamato, Suwa-shi, Nagano F-term (reference) in Seiko Epson Corporation 5F049 MA04 MB03 NA01 NA03 NA15 PA14 PA20 QA01 QA20 SZ13

## Cited By (7)

| Publication number | Priority date | Publication date | Assignee | Title |
|---|---|---|---|---|
| WO2006129427A1 * | 2005-05-31 | 2006-12-07 | Sharp Kabushiki Kaisha | Light sensor and display device |
| JP2007214405A * | 2006-02-10 | 2007-08-23 | Epson Imaging Devices Corp | Light receiving apparatus, electro-optical apparatus, and electronic appliance |
| JP2009130278A * | 2007-11-27 | 2009-06-11 | Hitachi Displays Ltd | Optical sensor device and image display device |
| US7936648B2 | 2004-06-23 | 2011-05-03 | Lg Electronics Inc. | Method and apparatus for overwriting data on recording medium and the recording medium |
| JP2011238942A * | 2002-12-18 | 2011-11-24 | Noblepeak Vision Corp | Semiconductor device having reduced defect of active region, and unique contact scheme |
| JP2015056651A * | 2013-09-13 | 2015-03-23 | 株式会社東芝 | Light receiving element and optically coupled insulating device |
| JP2020537816A * | 2017-07-21 | 2020-12-24 | ダブリュアンドダブリュセンス デバイシーズ、インコーポレイテッドW&Wsens Devices, Inc. | Microstructure improved absorption photosensitizer |
| Family To Family Citations | | | | |

* Cited by examiner, † Cited by third party, ‡ Family to family citation

## Similar Documents

| Publication | Publication Date | Title |
|---|---|---|
| US8916945B2 | 2014-12-23 | Semiconductor light-detecting element |
| EP2403012B1 | 2019-03-27 | Photodiode and photodiode array |
| US7576371B1 | 2009-08-18 | Structures and methods to improve the crosstalk between adjacent pixels of back-illuminated photodiode arrays |
| US20220065848A1 | 2022-01-06 | Photodetector |
| US20130001709A1 | 2013-01-03 | High Fill-Factor Laser-Treated Semiconductor Device on Bulk Material with Single Side Contact Scheme |
| JP3912024B2 | 2007-05-09 | PIN type lateral type semiconductor photo detector |
| JP2006060155A | 2006-03-02 | Semiconductor light receiving device and ultraviolet sensor |
| JP2002314118A | 2002-10-25 | Photodetector |
| JP4622531B2 | 2010-08-11 | Semiconductor energy detector |
| KR950003950B1 | 1995-04-21 | Photo-sensing device |
| US10636933B2 | 2020-04-28 | Tilted photodetector cell |
| JP2002314118A | 2002-10-25 | Lateral semiconductor photodetector of pin structure |

| | | |
|---|---|---|
| US6798001B2 | 2004-09-28 | Semiconductor device having photo diode with sensitivity to light of different wavelengths |
| JP2773960B2 | 1998-07-09 | Light detection device |
| US6809989B1 | 2004-10-26 | Short-wavelength photodiode of enhanced sensitivity with low leak current and method of manufacturing photodiode |
| JP2000252512A5 | 2005-11-24 | |
| KR100676733B1 | 2007-02-23 | UV detector having NIP Structure |
| Hinckley et al. | 2002 | Modelling of device structure effects on electrical crosstalk in back illuminated CMOS compatible photodiodes |
| JP2000252512A | 2000-09-14 | Pin photo-diode |
| KR100424366B1 | 2004-03-24 | A Photodiode With A Diffusion-Layer Of Dispersion-Distribution Pattern And Fabrication Method Thereof And A Substrate And An Electronic Machine Thereby |
| US8829432B2 | 2012-10-23 | High quantum efficiency optical detectors |
| US20210234057A1 | 2021-07-29 | Single photon avalanche diode device |
| JPH10190041A | 1998-07-21 | Photodiode |
| JP2020161739A | 2020-10-01 | Photodetector |
| JP4951552B2 | 2012-06-13 | Semiconductor photodetection device |

## Priority And Related Applications

### Priority Applications (1)

| Application | Priority date | Filing date | Title |
|---|---|---|---|
| JP2001110168A | 2001-04-09 | 2001-04-09 | Lateral semiconductor photodetector of pin structure |

### Applications Claiming Priority (1)

| Application | Filing date | Title |
|---|---|---|
| JP2001110168A | 2001-04-09 | Lateral semiconductor photodetector of pin structure |

### Legal Events

| Date | Code | Title | Description |
|---|---|---|---|
| 2006-07-01 | A300 | Withdrawal of application because of no request for examination | **Free format text**: JAPANESE INTERMEDIATE CODE: A300<br>**Effective date**: 20060701 |

### Concepts

machine-extracted

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|---|---|---|---|---|
| semiconductor | | title,claims,abstract,description | 22 | 0.000 |
| substrate | | claims,abstract,description | 22 | 0.000 |
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| deteriorative | | abstract | 1 | 0.000 |

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|---|---|---|---|
| Ｈ０１Ｌ　31/10 | | Ｈ０１Ｌ　31/10 | Ａ　５Ｆ０４９ |

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(71)出願人　000002369
セイコーエプソン株式会社
東京都新宿区西新宿２丁目４番１号

(72)発明者　原田　篤
長野県諏訪市大和３丁目３番５号　セイコーエプソン株式会社内

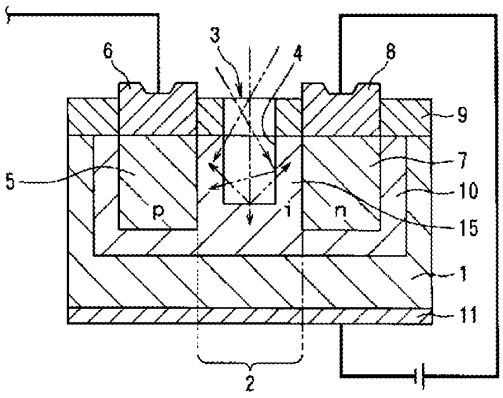
(72)発明者　井出　次男
長野県諏訪市大和３丁目３番５号　セイコーエプソン株式会社内

(74)代理人　100095728
弁理士　上柳　雅誉　（外１名）

最終頁に続く

(54)【発明の名称】　ＰＩＮ構造のラテラル型半導体受光素子

(57)【要約】　（修正有）
【課題】応答速度を低下させることなく受光感度を向上させたＰＩＮ構造のラテラル型半導体受光素子を提供する。
【解決手段】ＰＩＮ構造のｉ層１５とｐ層５とｎ層７との界面が半導体基板面に対して垂直に形成され、ｉ層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、受光領域２に、受光面３からｉ層１５の所定深さまで延びる穴４を設けた。



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【特許請求の範囲】

【請求項１】　ＰＩＮ構造のｉ層とｐ層およびｎ層との界面が半導体基板面に対して垂直に形成され、ｉ層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、

受光領域に、受光面からｉ層の所定深さまで延びる穴を設けたことを特徴とするＰＩＮ構造のラテラル型半導体受光素子。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、ＰＩＮ構造のラテラル型半導体受光素子に関する。

【０００２】

【従来の技術】ｐｎ接合面が半導体基板面に対して平行に形成されている縦型フォトダイオードでは、ｐ層またはｎ層を通して空乏層に光が入射されるのに対して、ｐｎ接合面が半導体基板面に対して垂直に形成されているラテラル型フォトダイオードでは、空乏層に直接（ｐ層やｎ層を介さずに）光が入射される。そのため、ラテラル型フォトダイオードは縦型フォトダイオードよりも、受光効率の点で有利である。

【０００３】従来より、フォトダイオードにおいては、ｐ層とｎ層との間にｉ層（真性層）を設けて、空乏層を厚くすることが行われている。このようなＰＩＮ構造を有する縦型フォトダイオードでは、受光感度を高くするために、ｉ層を吸収長以上の厚さに形成することが行われている。これにより、波長７００ｎｍ～８７０ｎｍ前後において、７０％以上の量子効率が得られるようになる。

【０００４】ＰＩＮ構造のラテラル型フォトダイオード（ＰＩＮ構造のｉ層とｐ層およびｎ層との界面が半導体基板面に対して垂直に形成されたフォトダイオード）は、例えば、ｉ層をなす不純物濃度の極めて薄い領域を半導体基板の表層部に設けた後、この領域の所定間隔を開けた各位置に、上面からｐ型不純物及びｎ型不純物をそれぞれ添加して拡散させることによりｐ層及びｎ層を形成し、両層の間をｉ層として残すことによって作製される。

【０００５】そのため、ＰＩＮ構造のラテラル型フォトダイオードの場合にｉ層の厚さ（光入射面からの深さ）を大きくしようとすると、ｐ層及びｎ層を深く形成する必要がある。基板の厚さ方向でｉ層の幅（ｐ層とｎ層との距離）を均一に保持しながら、ｐ層及びｎ層を深く形成するためには、基板表面でのｐ層とｎ層との距離を大きくとる必要がある。基板表面でのｐ層とｎ層との距離を大きくとるとｉ層の幅が大きくなる。ｉ層の幅が大きいと、ｉ層のｐ層側で生じた電子がｎ層の電極に達するまでの移動距離が長くなって、応答速度が遅くなる。

【０００６】したがって、ＰＩＮ構造のラテラル型フォトダイオードでは、受光感度をより高くする方法として、ｉ層の厚さ（光入射面からの深さ）を大きくすることを単純に採用することができない。そのため、ＰＩＮ構造のラテラル型フォトダイオードの受光感度をより高くする方法としては、ｉ層の上面に反射防止膜を設けてｉ層への入射効率を高くすることが有効である。

【０００７】

【発明が解決しようとする課題】しかしながら、ｉ層の上面に反射防止膜を有するＰＩＮ構造のラテラル型フォトダイオードには、高速の信号を受光する素子とした場合に応答速度が低くなるという問題点がある。本発明は、このような従来技術の問題点に着目してなされたものであり、ＰＩＮ構造のラテラル型半導体受光素子において、応答速度を低下させることなく受光感度を向上させることを課題とする。

【０００８】

【課題を解決するための手段】上記課題を解決するために、本発明は、ＰＩＮ構造のｉ層とｐ層およびｎ層との界面が半導体基板面に対して垂直に形成され、ｉ層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、受光領域に、受光面からｉ層の所定深さ（ｐ層およびｎ層の深さより浅い位置）まで延びる穴を設けたことを特徴とするＰＩＮ構造のラテラル型半導体受光素子を提供する。

【０００９】

【発明の実施の形態】以下、本発明の実施形態について説明する。図１は本発明の一実施形態に相当するフォトダイオードを示す断面図である。図２は、この実施形態のフォトダイオードがアレイ状に形成されている場合の平面形状の一例を示す図である。図１は図２のＡ－Ａ線断面図に相当する。

【００１０】このフォトダイオードは、ＰＩＮ構造がシリコン基板（半導体基板）１の基板面に対して垂直に形成されたラテラル型フォトダイオード（半導体受光素子）であり、受光領域（ｉ層１５のｐ層５とｎ層７とで挟まれた領域）２に、受光面３からｉ層１５の所定深さまで、シリコン基板１面に垂直に延びる穴４が設けてある。

【００１１】ｐ層５およびｎ層７の上面には、ｐ電極６およびｎ電極８がそれぞれ形成されている。シリコン基板１の下面にはｐ電極１１が形成されている。また、シリコン基板１の上面の両電極６，８および穴４の位置を除いた部分に、シリコン酸化膜等からなる素子保護層９が所定の厚さで形成されている。このフォトダイオードは、例えば以下の方法で作製できる。

【００１２】先ず、ｐ型のシリコン基板１の表層部にｎウエル（不純物濃度の極めて薄い領域）１０を設ける。次に、ｎウエル１０の所定間隔を開けた２つの領域の一方にｐ型不純物を、他方にｎ型不純物をそれぞれ添加して拡散させる。これにより、ｎウエル１０にｐ層５及びｎ層７が形成され、ｎウエル１０のｐ層５とｎ層７との

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間の部分がｉ層１５として残る。次に、ｐ層５及びｎ層７の上に電極６，８を形成した後、素子保護層９を形成する。

【００１３】次に、集束イオンビーム加工装置（ＦＩＢ）を用い、シリコン基板１上面の両電極６，８で挟まれた部分にイオンビームを照射して、素子保護層９とｉ層１５をエッチングすることにより、受光面３からｉ層１５の所定深さ（ｐ層５およびｎ層７の深さより浅い位置）まで、シリコン基板１の厚さ方向に延びる穴４を開ける。

【００１４】ここで、穴４のｐ層５－ｎ層７間方向の寸法は、穴４とｐ層５との間および穴４とｎ層７との間にそれぞれ所定厚さのｉ層１５が存在する寸法に設定する。また、各電極対間の受光面３が大きい場合には、図２に示すように、受光面３内に複数の穴４を設けることが好ましい。この場合には、例えば、電極６，８の幅Ｗ１を１μｍ、電極６，８の間隔Ｗ２を２～４μｍ、穴４のピッチＫを２～４μｍ、穴４の直径を１μｍとする。

【００１５】このフォトダイオードは、ｎ層７の上面に接触するｎ電極８と基板１の下面のｐ電極１１との間に、ｎ層７側を正として電源を接続して逆バイアス電圧を付与し、ｐ層５の上面に接触するｐ電極６を出力回路に接続することにより、受光面３からｉ層１５に入射された光を電流に変換して検出することができる。また、このフォトダイオードでは、受光面３から穴４内に入射された光（一部を図１に２点鎖線で表示）は、穴４の底面や側面から受光領域２に直接入射するとともに、底面や側面で反射されることで、底面から側面に向かって受光領域２に入射されたり、側面から対向する側面に向かって受光領域２に入射されたりする。そのため、穴４が無い場合よりも受光領域２での受光効率が高くなる。

【００１６】受光面積を大きくするために穴４を設けず単純に受光面３を大きくした場合には、ｉ層のｐ層側で生じた電子がｎ層の電極に達するまでの移動時間が長くなるとともに、寄生容量が大きくなるため、応答速度が遅くなる。これに対して、このフォトダイオードでは、穴４を設けることで、穴４が無い場合よりも穴４の側面の分だけ受光面積が大きくなっている。そのため、このフォトダイオードでは、ｉ層のｐ層側で生じた電子がｎ層の電極に達するまでの移動時間が、受光面３が同じ大きさで穴４を設けない場合よりも長くなることはない。また、このフォトダイオードの寄生容量は、受光面３が同じ大きさで穴４を設けない場合よりも小さくなる。これらのことから、このフォトダイオードによれば、応答速度を遅くすることなく、受光面積を大きくして受光効率を高くすることができる。

【００１７】さらに、このフォトダイオードは、穴４を有することによって、ｉ層１５の穴４の周囲部分に掛かる電界強度が局所的に大きくなっている。これにより、ｉ層１５の穴４の周囲部分で光を吸収して発生した正孔と電子はｉ層１５を高速で移動することができるため、穴４の無い場合と比較して応答速度が速くなる。したがって、このフォトダイオードによれば、穴４を設けることによって、受光領域２での受光効率が高くなって受光感度が向上するとともに、応答速度も高くなる。

【００１８】なお、この実施形態では、ＰＩＮ構造のラテラル型フォトダイオードについて説明しているが、本発明のＰＩＮ構造のラテラル型半導体受光素子はこれに限定されず、ベースとコレクタの部分がＰＩＮ構造になっているラテラル型フォトトランジスタ等にも適用される。

【００１９】

【発明の効果】以上説明したように、本発明のＰＩＮ構造のラテラル型半導体受光素子によれば、応答速度を低下させることなく受光感度を向上させることができる。

【図面の簡単な説明】

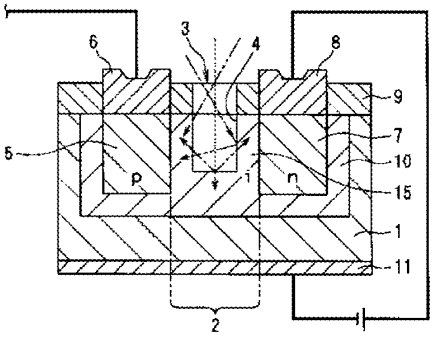
【図１】本発明の一実施形態に相当するフォトダイオードを示す断面図であって、図２のＡ－Ａ線断面図に相当する図である。

【図２】図１のフォトダイオードがアレイ状に形成されている場合の平面形状の一例を示す図である。

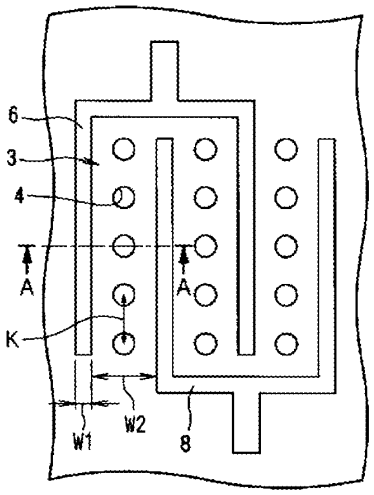
【符号の説明】

１　シリコン基板（半導体基板）
１０　ｎウエル
１１　ｐ電極
１５　ｉ層
２　受光領域
３　受光面
４　穴
５　ｐ層
６　ｐ電極
７　ｎ層
８　ｎ電極
９　素子保護層

【図１】




【図２】




フロントページの続き

(72)発明者　北村　昇二郎
長野県諏訪市大和３丁目３番５号　セイコーエプソン株式会社内

Ｆターム(参考)　5F049 MA04 MB03 NA01 NA03 NA15 PA14 PA20 QA01 QA20 SZ13

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# ELECTRONIC ACKNOWLEDGEMENT RECEIPT

| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **18/385,213** | **03/13/2024 02:42:05 PM Z ET** | **309-0015USCIP** |

## Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 7381 | FILED BY | Mary Ellen Finnegan |
| PATENT CENTER # | 64666225 | FILING DATE | 10/30/2023 |
| CUSTOMER # | 139982 | FIRST NAMED INVENTOR | Shih-Yuan WANG |
| CORRESPONDENCE ADDRESS | - | AUTHORIZED BY | Ivan Kavrukov |

## Documents

**TOTAL DOCUMENTS: 19**

| DOCUMENT | PAGES | DESCRIPTION | SIZE (KB) |
|---|---|---|---|
| 309-0015USCIP_IDSTransmittal.pdf | 1 | Transmittal Letter | 447 KB |
| 309-0015USCIP_1449-Signed.pdf | 10 | Information Disclosure Statement (IDS) Form (SB08) | 1637 KB |
| Warning: This is not a USPTO supplied IDS fillable form. Data in the form cannot be automatically loaded to other USPTO systems. | | | |
| KR20080101301A.pdf | 26 | Foreign Reference | 782 KB |
| JP2002314116.pdf | 8 | Foreign Reference | 3578 KB |
| WO2019018846A3.pdf | 3 | Foreign Reference | 148 KB |
| WO0103255.pdf | 69 | Foreign Reference | 9889 KB |

| | | | |
|---|---|---|---|
| EP0940854B1.pdf | 26 | Foreign Reference | 380 KB |
| JP2007013065.pdf | 30 | Foreign Reference | 10154 KB |
| CN103956403B.pdf | 17 | Foreign Reference | 4311 KB |
| ISR_WrittenOpinionPCTUS2150717-12-17-2020.pdf | 19 | Non Patent Literature | 24213 KB |
| Nanoelectronic_and_Nanophotonic_Interconnect.pdf | 18 | Non Patent Literature | 2566 KB |
| ISR_WrittenOpinionPCTUS2150717.pdf | 10 | Non Patent Literature | 749 KB |
| BFLevine_GBSi_HighQuantumEfficiencyMonolithically.pdf | 3 | Non Patent Literature | 1040 KB |
| YangGAO_PhotonTrappingMicrostructures.pdf | 9 | Non Patent Literature | 2485 KB |
| DEVINE_SingleMicroholePixelCMOSImageSensors.pdf | 7 | Non Patent Literature | 1222 KB |
| HAN_DeepTrenchIsolationInvertedPyramidArrayStructuresUsedEnhanceOpticalEfficiencyPhotodiodeCMOS.pdf | 14 | Foreign Reference | 10939 KB |
| PARKSamsungPixelTechnologyImprovingQuantum.pdf | 4 | Non Patent Literature | 2089 KB |
| YOKOGAWA_Sony3NanophotonicsContributionsStateOfTheArtCMOSImageSensors.pdf | 4 | Non Patent Literature | 1408 KB |
| YOKOGAWA_SonySensitivityEnhancementCMOSImageSensorDiffractiveLightTrappingPixels.pdf | 9 | Non Patent Literature | 2680 KB |

## Digest

| DOCUMENT | MESSAGE DIGEST(SHA-512) |
|---|---|
| 309-0015USCIP_IDSTransmittal.pdf | 380FAD5963AB11D94C8FA8FA6B201D581C716A2F65054B7E4CEB9DCF46F3B8406CD28825202BCD16FFC0D0970F87450EB0DBC5773BB9B4E6B5932D341993FD46 |
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| JP2002314116.pdf | B3EC13D9FBFC5229A470373AB2F4C48F924F6BD2317000633<br>36F938EC8B670D7B6CDDAE37A93EFD30748BC684815612557<br>6FF9561721E1A9FA824C2EBE1460F2 |
| WO2019018846A3.pdf | 345007BD360E48A3BC04B4E5882176AFB32D944921A5F73BA<br>C28A4E069B5A6A7353C15E9CB5CB7590603FD833BA297A8F0<br>8130B44181686172124039C3D34B58 |
| WO0103255.pdf | 39FB07AD2F3678F17D5133C5E8CF017573CC1DB0FB83DC2C<br>7887DF0820A052F6A4186DA169119969D9B3F40D5EBA45B92<br>9E2A7B767F326EF2FAEC65C4FA96347 |
| EP0940854B1.pdf | 64BEB78C41A204EC1F8C05851DB0A267A160D66503EBF78D1<br>59AD14E52A19F2A89F5619ABD696BFFB5C27513E9C787A62A<br>2F27511EB3A24C299D89C231B7CFCD |
| JP2007013065.pdf | 5D4A395E638BB06DFFFB688588014E18C1EC4E0F67037095D<br>A4BBE81AE15321A1327D01C100663D8312075A92E7A1C9BD1<br>5DD479938803EC3480442546DC7578 |
| CN103956403B.pdf | 6ACCEECC779A0D38CFF6986FE11DF54778E7684E8864876B<br>F2C8C4B57E15D240FFF016AF5E0196FFC07793D13B8A71AC8<br>A7A24FB2312361144C8026680729591 |
| ISR_WrittenOpinionPCTUS215<br>0717-12-17-2020.pdf | 5C80AC79BEFA1AA5E41B028EDE4809D72BA9A57449627A36<br>9344E63ECF7C346BFCA6FD230ECA2A18847DF926FC00DF2C<br>5325B749B20CBBCF04BC5658DB3C2126 |
| Nanoelectronic_and_Nanophot<br>onic_Interconnect.pdf | D18E8098416FFC24A975218B349C12339779DC14D530D66CC<br>D6F6F58DDCA1B55B3FBEB2ACD742C5AA10AF65F91BEDD90<br>9B0C8B77990625C332725F2C409299C0 |
| ISR_WrittenOpinionPCTUS215<br>0717.pdf | 5E0F3D5F12327B3CBF4E01CBC5ED1DA0BC862E1821D477F6<br>3CD7634682E7B695FB23F8A97F1C3E7D215E9FDE2DC1A9BD<br>A994C5956E79255F1B1C3E07B269E96E |
| BFLevine_GBSi_HighQuantum<br>EfficiencyMonolithically.pdf | E134581E9348C0E3011B18DDF3B066AB46DF6B6FC8CDBC66<br>17BF64E10D754D8B87EC6E148657FE415FD0D9070F8B93883<br>F27C9633AB3C0477FE7BCA0C6F4A334 |
| YangGAO_PhotonTrappingMicr<br>ostructures.pdf | 1CE7BC0F36228A2E81E02378A5FA4FA1CDC508AAAA6596F6<br>38911AC20EC0017CF821497D33491D936E654C7A91727159B1<br>131BAE434934923FC8391B70C31F16 |
| DEVINE_SingleMicroholePixel<br>CMOSImageSensors.pdf | 7E3D5BACA4568E2877D6927DE317C10792A0BB6A45F7761C<br>D56B9918F0D90827D8AEBB01E6C8181868D80F2D63363D160<br>5797EE4D0E7CFE68723CED86B593CE0 |

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|---|---|
| HAN_DeepTrenchIsolationInvertedPyramidArrayStructuresUsedEnhanceOpticalEfficiencyPhotodiodeCMOS.pdf | 8021B7C56AC030183FFDD2D2EFEC49BC76D5EC935B41A53CDC6D844A69955FF8414344BF4FE903F3636486E56642D4412E964378D180A6D50D9552FAD9216E87 |
| PARKSamsungPixelTechnologyImprovingQuantum.pdf | 74E2CB20BCABC1DD860037203358760FFB20B23C4283D557E754E961C793956B10D5FEA34B63864AEC6DD6953F5F9AD480ED607AF135220B60CD1CBE57D5A15A |
| YOKOGAWA_Sony3NanophotonicsContributionsStateOfTheArtCMOSImageSensors.pdf | 58EC6C061A934F15D61B37F4B3F45C064F52E4FD4BAA0B07C6F59CC8D785DD611FC4AD5521C5314495498601FC317D9B7D913290B5F5D8B9881D4F974151C806 |
| YOKOGAWA_SonySensitivityEnhancementCMOSImageSensorDiffractiveLightTrappingPixels.pdf | 77CF192176DB7773AEE0BA59C73EFAD888A7B2495639B95B0428781BBC157C6320291A6D36DA6FFA2FA55A829BE42D6AA62CF5851ACCBAE2C677088D78BFE6CF |

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**New Applications Under 35 U.S.C. 111**

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**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: ECOMM.AUTH/ECOMM.WTDW
Doc Description: Internet Communications Authorization/Internet Communications Authorization Withdrawal

PTO/SB/439 (11-15)

| **AUTHORIZATION FOR INTERNET COMMUNICATIONS IN A PATENT APPLICATION OR REQUEST TO WITHDRAW AUTHORIZATION FOR INTERNET COMMUNICATIONS** | | |
|---|---|---|
| | Application No. | 18/385,213 |
| | Filing Date | 10/30/2023 |
| | First Named Inventor | Shih-Yuan WANG |
| | Art Unit | 2893 |
| | Examiner Name | Eduardo A RODELA |
| | Practitioner Docket No. | 309-0015USCIP |

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**I. To authorize permission for Internet Communications.**

☒ Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via video conferencing, instant messaging, or electronic mail. I understand that a copy of these communications will be made of record in the application file. (MPEP 502.03)

**II. To withdraw authorization for Internet Communications.**

☐ The authorization given on _____, to the USPTO to communicate with the undersigned and any practitioner in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via Internet communications such as video conferencing, instant messaging, or electronic mail is hereby withdrawn. I understand that the withdrawal is effective when approved rather than when received.

I am the

☐ applicant.

☒ attorney or agent of record. Registration number 25,161.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

| /Ivan Kavrukov/ | 03/13/2024 |
|---|---|
| Signature | Date |
| Ivan Kavrukov | 917-945-0121 |
| Typed or printed name | Telephone Number |

**NOTE:** This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Juristic entities must be represented by a patent practitioner (see 37 CFR 1.31, which is applicable to any paper filed on or after September 16, 2012, that is presented on behalf of a juristic entity, regardless of application filing date). Submit multiple forms if more than one signature is required, see below*.

☒ * Total of 1 forms are submitted.

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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# ELECTRONIC ACKNOWLEDGEMENT RECEIPT

| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **18/385,213** | **03/13/2024 12:55:19 PM Z ET** | **309-0015USCIP** |

## Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 7381 | FILED BY | Mary Ellen Finnegan |
| PATENT CENTER # | 64666121 | FILING DATE | 10/30/2023 |
| CUSTOMER # | 139982 | FIRST NAMED INVENTOR | Shih-Yuan WANG |
| CORRESPONDENCE ADDRESS | - | AUTHORIZED BY | Ivan Kavrukov |

## Documents

**TOTAL DOCUMENTS: 1**

| DOCUMENT | PAGES | DESCRIPTION | SIZE (KB) |
|---|---|---|---|
| 309-0015USCIP_AuthorizationForInternetCommunications.pdf | 2 | Internet Communications Authorization | 208 KB |

## Digest

| DOCUMENT | MESSAGE DIGEST(SHA-512) |
|---|---|
| 309-0015USCIP_AuthorizationForInternetCommunications.pdf | 1CBFBAD9B26E2C7941DA86724F3A1AFACF6B283DDD7B9C7D1B5F04175BBFCC39C7939DA492E0B6D11C27F5FABABCB8809E33268E1A43E836DB398BD6584FF53B |

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**New Applications Under 35 U.S.C. 111**

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| APPLICATION NUMBER | FILING or 371(c) DATE | GRP ART UNIT | FIL FEE REC'D | ATTY.DOCKET.NO | TOT CLAIMS | IND CLAIMS |
|---|---|---|---|---|---|---|
| 18/385,213 | 10/30/2023 | 2893 | 896 | 309-0015USCIP | 12 | 1 |

**CONFIRMATION NO. 7381**

**CORRECTED FILING RECEIPT**

139982
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

Date Mailed: 03/05/2024

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

**Please verify the accuracy of the data presented on this receipt.** If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

**Inventor(s)**

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping WANG, Los Altos, CA;

**Applicant(s)**

W&W Sens Devices, Inc., Los Altos, CA;

**Power of Attorney:** The patent practitioners associated with Customer Number 139982

**Domestic Priority data as claimed by applicant**

This application is a CIP of 17/974,325 10/26/2022 PAT 11,830,954
and is a CIP of 18/113,474 02/23/2023
which is a DIV of 17/707,429 03/29/2022 PAT 11,621,360
which is a CIP of 17/182,954 02/23/2021 PAT 11,791,432
which is a DIV of 16/528,958 08/01/2019 PAT 11,121,271
which is a CIP of 15/979,821 05/15/2018 PAT 10,624,300
and said 17/707,429 03/29/2022 is a DIV of 17/532,831 11/22/2021 PAT 11,309,444
which is a CIP of 17/182,954 02/23/2021 PAT 11,791,432
and said 16/528,958 08/01/2019 is a CIP of 14/947,718 11/20/2015 PAT 10,622,498
and is a CIP of PCT/US16/67977 12/21/2016
and is a CIP of 16/042,535 07/23/2018 PAT 10,700,225
and is a CIP of 16/296,985 03/08/2019 PAT 10,468,543
and is a CIP of PCT/US18/43289 07/23/2018
and is a CIP of PCT/US18/57963 10/29/2018
and claims benefit of 62/713,455 08/01/2018

and claims benefit of 62/716,310 08/08/2018
and claims benefit of 62/717,750 08/10/2018
and claims benefit of 62/719,689 08/19/2018
and claims benefit of 62/724,449 08/29/2018
and claims benefit of 62/733,476 09/19/2018
and claims benefit of 62/737,062 09/26/2018
and claims benefit of 62/750,016 10/24/2018
and claims benefit of 62/770,656 11/21/2018
and claims benefit of 62/772,498 11/28/2018
and claims benefit of 62/777,157 12/09/2018
and claims benefit of 62/779,693 12/14/2018
and claims benefit of 62/784,342 12/21/2018
and claims benefit of 62/794,330 01/18/2019
and claims benefit of 62/797,141 01/25/2019
and claims benefit of 62/797,263 01/26/2019
and claims benefit of 62/800,371 02/01/2019
and claims benefit of 62/802,171 02/06/2019
and claims benefit of 62/802,718 02/08/2019
and claims benefit of 62/805,850 02/14/2019
and claims benefit of 62/808,949 02/22/2019
and claims benefit of 62/819,604 03/17/2019
and claims benefit of 62/819,669 03/17/2019
and claims benefit of 62/820,695 03/19/2019
and claims benefit of 62/828,976 04/03/2019
and claims benefit of 62/841,798 05/01/2019
and claims benefit of 62/843,206 05/03/2019
and claims benefit of 62/846,554 05/10/2019
and claims benefit of 62/853,280 05/28/2019
and claims benefit of 62/860,115 06/11/2019
and claims benefit of 62/863,231 06/18/2019
and claims benefit of 62/863,852 06/19/2019
and claims benefit of 62/867,186 06/26/2019
and claims benefit of 62/868,911 06/29/2019
and claims benefit of 62/870,533 07/03/2019
and claims benefit of 62/873,891 07/13/2019
and claims benefit of 62/874,418 07/15/2019
and said PCT/US18/57963 10/29/2018 is a CON of 15/797,821 10/30/2017 PAT 10,446,700
and said 15/979,821 05/15/2018 is a CIP of 14/947,718 11/20/2015 PAT 10,622,498
and is a CIP of 15/309,922 11/09/2016 PAT 9,818,893
and is a CIP of PCT/US16/67977 12/21/2016
and claims benefit of 62/465,734 03/01/2017
and claims benefit of 62/474,179 03/21/2017
and claims benefit of 62/484,474 04/12/2017
and claims benefit of 62/487,606 04/20/2017
and claims benefit of 62/488,998 04/24/2017
and claims benefit of 62/500,581 05/03/2017
and claims benefit of 62/505,974 05/14/2017
and claims benefit of 62/509,093 05/20/2017
and claims benefit of 62/510,249 05/23/2017
and claims benefit of 62/514,889 06/04/2017
and claims benefit of 62/521,504 06/18/2017

and claims benefit of 62/522,169 06/20/2017
and claims benefit of 62/527,962 06/30/2017
and claims benefit of 62/530,281 07/09/2017
and claims benefit of 62/533,078 07/16/2017
and claims benefit of 62/533,603 07/17/2017
and claims benefit of 62/535,801 07/21/2017
and claims benefit of 62/540,524 08/02/2017
and claims benefit of 62/542,243 08/07/2017
and claims benefit of 62/547,728 08/18/2017
and claims benefit of 62/553,844 09/02/2017
and claims benefit of 62/556,426 09/10/2017
and claims benefit of 62/561,869 09/22/2017
and said PCT/US18/43289 07/23/2018 claims benefit of 62/542,243 08/07/2017
and claims benefit of 62/535,801 07/21/2017
and claims benefit of 62/540,524 08/02/2017
and claims benefit of 62/639,472 03/06/2018
and claims benefit of 62/628,764 02/09/2018
and claims benefit of 62/643,010 03/14/2018
and claims benefit of 62/640,522 03/08/2018
and claims benefit of 62/599,246 12/15/2017
and claims benefit of 62/645,810 03/21/2018
and claims benefit of 62/666,005 05/02/2018
and claims benefit of 62/556,426 09/10/2017
and claims benefit of 62/607,860 12/19/2017
and claims benefit of 62/631,630 02/17/2018
and claims benefit of 62/677,609 05/29/2018
and claims benefit of 62/634,692 02/23/2018
and claims benefit of 62/652,830 04/04/2018
and claims benefit of 62/891,072 08/23/2019
and claims benefit of 62/639,356 03/06/2018
and claims benefit of 62/615,314 01/09/2018
and claims benefit of 62/623,971 01/30/2018
and claims benefit of 62/561,869 09/22/2017
and claims benefit of 62/637,945 03/02/2018
and claims benefit of 62/651,053 03/30/2018
and claims benefit of 62/553,844 09/02/2017
and claims benefit of 62/682,909 06/09/2018
and claims benefit of 62/659,072 04/17/2018
and claims benefit of 62/569,067 10/06/2017
and claims benefit of 62/669,194 05/09/2018
and claims benefit of 62/675,130 05/22/2018
and claims benefit of 62/547,728 08/18/2017
and claims benefit of 62/651,087 03/31/2018
and claims benefit of 62/646,871 03/22/2018
and claims benefit of 62/662,217 04/24/2018
and claims benefit of 62/639,920 03/07/2018
and claims benefit of 62/633,514 02/21/2018
and said 16/528,958 08/01/2019 is a CON of 15/797,821 10/30/2017 PAT 10,446,700
and said 16/042,535 07/23/2018 is a CIP of 15/797,821 10/30/2017 PAT 10,446,700
and claims benefit of 62/535,801 07/21/2017
and claims benefit of 62/540,524 08/02/2017

and claims benefit of 62/542,243 08/07/2017
and claims benefit of 62/547,728 08/18/2017
and claims benefit of 62/553,844 09/02/2017
and claims benefit of 62/556,426 09/10/2017
and claims benefit of 62/561,869 09/22/2017
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and claims benefit of 62/615,314 01/09/2018
and claims benefit of 62/623,971 01/30/2018
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and claims benefit of 62/633,514 02/21/2018
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and claims benefit of 62/637,945 03/02/2018
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and claims benefit of 62/639,472 03/06/2018
and claims benefit of 62/639,920 03/07/2018
and claims benefit of 62/640,522 03/08/2018
and claims benefit of 62/643,010 03/14/2018
and claims benefit of 62/645,810 03/21/2018
and claims benefit of 62/646,871 03/22/2018
and claims benefit of 62/651,053 03/30/2018
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and claims benefit of 62/652,830 04/04/2018
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and claims benefit of 62/662,217 04/24/2018
and claims benefit of 62/666,005 05/02/2018
and claims benefit of 62/669,194 05/09/2018
and claims benefit of 62/675,130 05/22/2018
and claims benefit of 62/677,609 05/29/2018
and claims benefit of 62/682,909 06/09/2018
and said PCT/US16/67977 12/21/2016 claims benefit of 62/270,577 12/21/2015
and claims benefit of 62/304,907 03/07/2016
and claims benefit of 62/290,391 02/02/2016
and claims benefit of 62/334,934 05/11/2016
and claims benefit of 62/338,263 05/18/2016
and claims benefit of 62/346,850 06/07/2016
and claims benefit of 62/359,349 07/07/2016
and claims benefit of 62/366,188 07/25/2016
and claims benefit of 62/368,109 07/28/2016
and claims benefit of 62/374,828 08/13/2016
and claims benefit of 62/376,869 08/18/2016
and claims benefit of 62/380,364 08/27/2016
and claims benefit of 62/383,391 09/03/2016
and claims benefit of 62/383,479 09/04/2016
and claims benefit of 62/394,222 09/14/2016
and claims benefit of 62/398,607 09/23/2016
and claims benefit of 62/401,126 09/28/2016
and claims benefit of 62/406,999 10/12/2016

and claims benefit of 62/414,671 10/29/2016
and claims benefit of 62/415,339 10/31/2016
and said 15/309,922 11/09/2016 is a 371 of PCT/US15/61120 11/17/2015
and is a CON of 14/943,898 11/17/2015 PAT 9,530,905
and is a CON of 14/945,003 11/18/2015 PAT 9,525,084
which claims benefit of 62/232,716 09/25/2015
and claims benefit of 62/213,558 09/02/2015
and claims benefit of 62/209,311 08/24/2015
and claims benefit of 62/205,717 08/15/2015
and claims benefit of 62/199,607 07/31/2015
and claims benefit of 62/197,120 07/27/2015
and claims benefit of 62/188,876 07/06/2015
and claims benefit of 62/182,602 06/21/2015
and claims benefit of 62/175,855 06/15/2015
and claims benefit of 62/174,498 06/11/2015
and claims benefit of 62/171,915 06/05/2015
and claims benefit of 62/157,876 05/06/2015
and claims benefit of 62/154,675 04/29/2015
and claims benefit of 62/153,443 04/27/2015
and claims benefit of 62/139,511 03/27/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/100,025 01/05/2015
and claims benefit of 62/090,879 12/11/2014
and claims benefit of 62/081,538 11/18/2014
and said 14/943,898 11/17/2015 claims benefit of 62/232,716 09/25/2015
and claims benefit of 62/213,556 09/02/2015
and claims benefit of 62/209,311 08/24/2015
and claims benefit of 62/205,717 08/15/2015
and claims benefit of 62/199,607 07/31/2015
and claims benefit of 62/197,120 07/27/2015
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and claims benefit of 62/182,602 06/21/2015
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and claims benefit of 62/174,498 06/11/2015
and claims benefit of 62/171,915 06/05/2015
and claims benefit of 62/157,876 05/06/2015
and claims benefit of 62/154,675 04/29/2015
and claims benefit of 62/153,443 04/27/2015
and claims benefit of 62/139,511 03/27/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/100,025 01/05/2015
and claims benefit of 62/090,879 12/11/2014
and claims benefit of 62/081,583 11/19/2014 ABN
and said PCT/US15/61120 11/17/2015 claims benefit of 62/232,716 09/25/2015
and claims benefit of 62/213,556 09/02/2015
and claims benefit of 62/209,311 08/24/2015
and claims benefit of 62/205,717 08/15/2015
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and claims benefit of 62/197,120 07/27/2015
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and claims benefit of 62/182,602 06/21/2015

and claims benefit of 62/175,855 06/15/2015
and claims benefit of 62/174,498 06/11/2015
and claims benefit of 62/171,915 06/05/2015
and claims benefit of 62/157,876 05/06/2015
and claims benefit of 62/154,675 04/29/2015
and claims benefit of 62/153,443 04/27/2015
and claims benefit of 62/139,511 03/27/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/100,025 01/05/2015
and claims benefit of 62/090,879 12/11/2014
and claims benefit of 62/081,538 11/18/2014
and said 14/947,718 11/20/2015 is a CON of PCT/US14/39208 05/22/2014
which claims benefit of 61/826,446 05/22/2013
and claims benefit of 61/843,021 07/04/2013
and claims benefit of 61/905,109 11/15/2013
and claims benefit of 61/834,873 06/13/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the Patent Prosecution Highway program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

**Permission to Access Application via Priority Document Exchange:** Yes

**Permission to Access Search Results:** Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

**If Required, Foreign Filing License Granted:** 11/14/2023
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 18/385,213**
**Projected Publication Date:** 02/22/2024
**Non-Publication Request:** No
**Early Publication Request:** No
**** SMALL ENTITY ****
**Title**

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

**Preliminary Class**

136

**Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications:** No

## PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same

effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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## Title 35, United States Code, Section 184

## Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with

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**NOT GRANTED**

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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www.uspto.gov

| APPLICATION NUMBER | FILING OR 371(C) DATE | FIRST NAMED APPLICANT | ATTY. DOCKET NO./TITLE |
|---|---|---|---|
| 18/385,213 | 10/30/2023 | Shih-Yuan WANG | 309-0015USCIP |

**CONFIRMATION NO. 7381**

139982
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

**IMPROPER CFR REQUEST**

*OC000000069149536*

Date Mailed: 03/05/2024

## RESPONSE TO REQUEST FOR CORRECTED FILING RECEIPT

***Continuity, Priority Claims, Petitions, and Non-Publication Requests***

In response to your request for a corrected Filing Receipt, the Office is unable to comply with your request because:

- One or more of the benefit claims under 35 U.S.C. § 120 cannot be included on the Filing Receipt since applicant did not specify whether the application is a continuation, divisional or continuation-in-part of the prior application. Applicant must submit a new application data sheet (ADS) that sets forth the relationship, and the ADS must be accompanied by a petition under 37 CFR 1.78 if filed after the time period set forth in 37 CFR 1.78.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/hteffera/

PATENT
309-0015USCIP

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | |
|---|---|
| First Named Inventor: | Shih-Yuan WANG |
| Serial No.: | 18/385,213 |
| Filing Date: | October 30, 2023 |
| Examiner: | Eduardo A. Rodela |
| Art Unit: | 2893 |
| Confirmation No.: | 7381 |
| For: | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES |

Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

**CERTIFICATE OF ELECTRONIC FILING**

Date of Transmission: February 29, 2024

I hereby certify that this correspondence is being transmitted via Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

**COMMUNICATION IN RESPONSE TO REQUEST FOR CORRECTED FILING RECEIPT**

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is in response to the Response to Request for Corrected Filing Receipt mailed November 16, 2023. The Application Data Sheet that was submitted with the application on October 30, 2023, incorrectly lists some priority claims. Applicant hereby submits a Corrected Application Data Sheet to correct the priority claim in the Domestic Claims Benefit Section of the ADS.

Correction of the ADS and issuance of a corrected Filing Receipt application is earnestly solicited.

Respectfully Submitted,

WISSING MILLER LLP
Attorney for Applicants

/Ivan S. Kavrukov/

Ivan S. Kavrukov
Registration No. 25,161
Attorney for Applicant

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

## Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

## Inventor Information:

**Inventor 1** Remove

**Legal Name**

| Prefix | Given Name | Middle Name | Family Name | Suffix |
|---|---|---|---|---|
| | Shih-Yuan | | WANG | |

**Residence Information (Select One)** ◉ US Residency ○ Non US Residency ○ Active US Military Service

| City | Palo Alto | State/Province | CA | Country of Residence | US |
|---|---|---|---|---|---|

**Mailing Address of Inventor:**

| Address 1 | 766 Encina Grande Drive | | |
|---|---|---|---|
| Address 2 | | | |
| City | Palo Alto | State/Province | CA |
| Postal Code | 94306 | Country | US |

**Inventor 2** Remove

**Legal Name**

| Prefix | Given Name | Middle Name | Family Name | Suffix |
|---|---|---|---|---|
| | Shih-Ping | | WANG | |

**Residence Information (Select One)** ◉ US Residency ○ Non US Residency ○ Active US Military Service

| City | Los Altos | State/Province | CA | Country of Residence | US |
|---|---|---|---|---|---|

**Mailing Address of Inventor:**

| Address 1 | 38 Third Street, Suite 307 | | |
|---|---|---|---|
| Address 2 | | | |
| City | Los Altos | State/Province | CA |
| Postal Code | 90422 | Country | US |

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

## Correspondence Information:

**Enter either Customer Number or complete the Correspondence Information section below.**
**For further information see 37 CFR 1.33(a).**

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| ☐ An Address is being provided for the correspondence Information of this application. | | | |
|---|---|---|---|
| **Customer Number** | 139982 | | |
| **Email Address** | wmdocket@wissingmiller.com | Add Email | Remove Email |

## Application Information:

| **Title of the Invention** | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | | |
|---|---|---|---|
| **Attorney Docket Number** | 309-0015USCIP | **Small Entity Status Claimed** | ☒ |
| **Application Type** | Nonprovisional | | |
| **Subject Matter** | Utility | | |
| **Total Number of Drawing Sheets (if any)** | 48 | **Suggested Figure for Publication (if any)** | 5B |

## Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

| Application number of the previously filed application | Filing date (YYYY-MM-DD) | Intellectual Property Authority or Country |
|---|---|---|
| | | |

## Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

## Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

| Please Select One: | ◉ Customer Number | ○ US Patent Practitioner | ○ Limited Recognition (37 CFR 11.9) |
|---|---|---|---|
| Customer Number | 139982 | | |

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| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | 567-0002USD |
|---|---|---|
| | Application Number | |
| Title of Invention | STORAGE CONTAINER FOR VEHICLE | |

## Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

| Prior Application Status | ~~Pending~~ Patented | Remove |
|---|---|---|

| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
|---|---|---|---|---|---|
| 18385213 | Continuation in part of | 17974325 | 2022-10-26 | 11830954 | 2023-11-28 |

| Prior Application Status | Patented ~~Pending~~ | Remove |
|---|---|---|

| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
|---|---|---|---|
| 18385213 | Continuation in part of | 18113474 | 2023-02-23 |

| Prior Application Status | Patented | Remove |
|---|---|---|

| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
|---|---|---|---|---|---|
| 18113474 | Division of | 17707429 | 2022-03-29 | 11621360 | 2023-04-04 |

| Prior Application Status | Patented | Remove |
|---|---|---|

| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
|---|---|---|---|---|---|
| 17707429 | Continuation in part of | 17182954 | 2021-02-23 | 11791432 | 2023-10-17 |

| Prior Application Status | Patented | Remove |
|---|---|---|

| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
|---|---|---|---|---|---|
| 17182954 | Division of | 16528958 | 2019-08-01 | 11121271 | 2021-09-14 |

| Prior Application Status | Patented | Remove |
|---|---|---|

| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
|---|---|---|---|---|---|
| 16528958 | Continuation in part of | 15797821 | 2017-10-30 | 10446700 | 2019-10-15 |

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

## Foreign Priority Information:

PTO/AIA/14 (02-18)
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| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

## Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

| Prior Application Status | Patented | | | Remove | |
|---|---|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
| 18113474 | Division of | 17/707429 | 2022-03-29 | 11621360 | 2023-04-04 |
| Prior Application Status | Patented | | | Remove | |
| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
| 17/707429 | Division of | 17/532831 | 2021-11-22 | 11309444 | 2022-04-19 |
| Prior Application Status | Patented ~~Pending~~ | | | Remove | |
| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
| 17/532831 | Continuation in part of | 17182954 | 2021-02-23 | 11791432 | 2023-10-17 |
| Prior Application Status | Patented | | | Remove | |
| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
| 17/182954 | Division of | 16/528958 | 2019-08-01 | 11121271 | 2021-09-14 |
| Prior Application Status | Patented | | | Remove | |
| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
| 16/528958 | Continuation in part of | 14/947718 | 2015-11-20 | 10622498 | 2020-03-25 |
| Prior Application Status | Expired | | | Remove | |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) | | |
| 16/528958 | Continuation in part of | PCT/US16/67977 | 2016-12-21 | | |
| Prior Application Status | Patented | | | Remove | |
| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
| 16/528958 | Continuation in part of | 15/797821 | 2017-10-20 | 10446700 | 2019-09-25 |
| Prior Application Status | Patented ~~Pending~~ | | | Remove | |
| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
| 16/528958 | Continuation in part of | 16/042535 | 2018-07-23 | 10700225 | ~~2020-06-10~~ 2020-06-30 |
| Prior Application Status | Patented | | | Remove | |
| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
| 16/528958 | Continuation in part of | 16/296985 | 2019-03-08 | 10468543 | 2019-10-16 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Abandoned | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Continuation in part of | PCT/US18/43289 | 2018-07-23 |
| Prior Application Status | Abandoned | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Continuation in part of | PCT/US18/57963 | 2018-10-29 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/713455 | 2018-08-01 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/716310 | 2018-08-08 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/717750 | 2018-08-10 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/719689 | 2018-08-19 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/724449 | 2018-08-29 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/733476 | 2018-09-19 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/737062 | 2018-09-26 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/750016 | 2018-10-24 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/770656 | 2018-09-21 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/772498 | 2018-09-28 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/777157 | 2018-12-09 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/779693 | 2018-12-14 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/784342 | 2018-12-21 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/794330 | 2019-01-18 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/797141 | 2019-01-25 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/797263 | 2019-01-26 |

| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/800371 | 2019-02-01 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/802171 | 2019-02-06 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/802718 | 2019-02-08 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/805850 | 2019-02-14 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/808949 | 2019-02-22 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/819604 | 2019-03-17 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/819669 | 2019-03-17 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/820695 | 2019-03-19 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/828976 | 2019-04-03 |

| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/841798 | 2019-05-01 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/843206 | 2019-05-03 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/846554 | 2019-05-10 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/853280 | 2019-05-28 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/860115 | 2019-06-11 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/863231 | 2019-06-18 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/863852 | 2019-06-19 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/867186 | 2019-06-26 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/868911 | 2019-06-29 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/870533 | 2019-07-03 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/873891 | 2019-07-13 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/528958 | Claims benefit of provisional | 62/874418 | 2019-07-15 |
| Prior Application Status | Patented | | Remove |

| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
|---|---|---|---|---|---|
| PCT/US18/57963 | Continuation of | 15/797821 | 2017-10-30 | 10446700 | 2019-10-15 |
| Prior Application Status | Patented | | | Remove | |
| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
| 15/797821 | Continuation in part of | 14/947718 | 2015-11-20 | 10622498 | 2020-03-25 |
| Prior Application Status | Patented | | | Remove | |
| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
| 15/797821 | Continuation in part of | 15/309922 | 2016-11-09 | 9818893 | 2017-10-25 |

| Prior Application Status | Pending | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Continuation in part of | PCT/US16/67977 | 2016-12-21 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/465734 | 2017-03-01 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/474179 | 2017-03-21 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/484474 | 2017-04-12 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/487606 | 2017-04-20 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/488998 | 2017-04-24 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/500581 | 2017-05-03 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/505974 | 2017-05-14 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/509093 | 2017-05-20 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/510249 | 2017-05-23 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/514889 | 2017-06-04 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/521504 | 2017-06-18 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/522169 | 2017-06-20 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/527962 | 2017-06-30 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/530281 | 2017-07-19 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/533078 | 2017-07-16 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/533603 | 2017-07-17 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/535801 | 2017-07-21 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/540524 | 2017-08-02 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/542243 | 2017-08-07 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/547728 | 2017-08-18 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/553844 | 2017-09-02 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/556426 | 2017-09-10 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/797821 | Claims benefit of provisional | 62/561869 | 2017-09-22 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/542243 | 2017-08-07 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/535801 | 2017-07-21 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/540524 | 2017-08-02 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/639472 | 2018-03-06 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/628764 | 2018-02-09 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/643010 | 2018-03-14 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/640522 | 2018-03-08 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/599246 | 2017-12-15 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/645810 | 2018-03-21 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/666005 | 2018-05-02 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/556426 | 2017-09-10 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/607860 | 2017-12-19 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/631630 | 2018-02-17 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/677609 | 2018-05-29 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/634692 | 2018-02-23 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/652830 | 2018-04-04 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/591072 | 2017-09-27 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/639356 | 2018-03-06 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/615314 | 2018-01-09 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/623971 | 2018-01-30 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/561869 | 2017-09-22 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/637945 | 2018-03-02 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/651053 | 2018-03-30 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/553844 | 2017-09-02 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/682909 | 2018-06-09 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/659072 | 2018-04-17 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/659067 | 2018-04-17 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/669194 | 2018-05-09 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/675130 | 2018-05-22 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/547728 | 2017-08-18 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/651087 | 2018-03-31 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/646871 | 2018-03-22 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/662217 | 2018-04-24 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/639920 | 2018-03-07 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US18/43289 | Claims benefit of provisional | 62/633514 | 2018-02-21 |
| Prior Application Status | Patented | | Remove |

| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
|---|---|---|---|---|---|
| 16/296985 | Continuation of | 15/797821 | 2017-10-30 | 10446700 | 2019-10-15 |

| Prior Application Status | Patented | | Remove |
|---|---|---|---|

| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
|---|---|---|---|---|---|
| 16/042535 | Continuation in part of | 15/797821 | 2017-10-30 | 10446700 | 2019-10-15 |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/535801 | 2017-07-21 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/540524 | 2017-08-02 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/542243 | 2017-08-07 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/547728 | 2017-08-18 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/553844 | 2017-09-02 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/556426 | 2017-09-10 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/561869 | 2017-09-22 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/591072 | 2017-11-27 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/599246 | 2017-12-15 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/607860 | 2017-12-19 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/615314 | 2018-01-09 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/623971 | 2018-01-30 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/628764 | 2018-02-09 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/631630 | 2018-02-17 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/633514 | 2018-02-21 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/634692 | 2018-02-23 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/637945 | 2018-03-02 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/639356 | 2018-03-06 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/639472 | 2018-03-06 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/639920 | 2018-03-07 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/640522 | 2018-03-08 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/643010 | 2018-03-14 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/645810 | 2018-03-21 |

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| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/646871 | 2018-03-22 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/651053 | 2018-03-30 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/651087 | 2018-03-31 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/652830 | 2018-04-04 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/659067 | 2018-04-17 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/659072 | 2018-04-17 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/662217 | 2018-04-24 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/666005 | 2018-05-02 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/669194 | 2018-05-09 |

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| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/675130 | 2018-05-22 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/677609 | 2018-05-29 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 16/042535 | Claims benefit of provisional | 62/682909 | 2018-06-09 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/270577 | 2015-12-21 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/304907 | 2016-03-07 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/290391 | 2016-02-02 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/334934 | 2016-05-11 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/338263 | 2016-05-18 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/346850 | 2016-06-07 |

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|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/359349 | 2017-07-07 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/366188 | 2016-07-25 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/368109 | 2016-07-28 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/374828 | 2016-08-13 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/376869 | 2016-08-18 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/380364 | 2016-08-27 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/383391 | 2016-09-03 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/383479 | 2016-09-04 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/394222 | 2016-09-14 |

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U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/398607 | 2016-09-23 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/401126 | 2016-09-28 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/406999 | 2016-10-12 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/414671 | 2016-10-29 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US16/67977 | Claims benefit of provisional | 62/415339 | 2016-10-31 |
| Prior Application Status | ~~Pending~~ Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 15/309922 | a 371 of international | PCT/US15/61120 | 2015-11-17 |
| Prior Application Status | Patented | | Remove |

| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
|---|---|---|---|---|---|
| 15/309922 | Continuation of | 14/943898 | 2015-11-17 | 9530905 | 2016-12-27 |
| Prior Application Status | Patented | | | | Remove |

| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
|---|---|---|---|---|---|
| 15/309922 | Continuation of | 14/945003 | 2015-11-18 | 9525084 | 2016-12-20 |
| Prior Application Status | Expired | | | | Remove |

| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
|---|---|---|---|
| 14/945003 | Claims benefit of provisional | 62/232716 | 2015-09-25 |

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| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/213558 | 2015-09-02 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/209311 | 2015-08-24 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/205717 | 2015-08-15 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/199607 | 2015-07-13 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/197120 | 2015-07-27 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/188876 | 2015-07-06 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/182602 | 2015-06-21 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/175855 | 2015-06-15 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/174498 | 2015-06-11 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/171915 | 2015-06-05 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/157876 | 2015-05-06 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/154675 | 2015-04-29 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/153443 | 2015-04-27 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/139511 | 2015-03-27 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/111582 | 2015-02-03 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/100025 | 2015-01-05 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/090879 | 2014-12-11 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/945003 | Claims benefit of provisional | 62/081538 | 2014-11-18 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/232716 | 2015-09-25 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/213556 | 2015-09-02 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/209311 | 2015-08-24 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/205717 | 2015-08-15 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/199607 | 2015-07-31 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/197120 | 2015-07-27 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/188876 | 2015-07-06 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/182602 | 2015-06-21 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/175855 | 2015-06-15 |

| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/174498 | 2015-06-11 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/171915 | 2015-06-05 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/157876 | 2015-05-06 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/154675 | 2015-04-29 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/153443 | 2015-04-27 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/139511 | 2015-03-27 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/111582 | 2015-02-03 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/100025 | 2015-01-05 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/090879 | 2014-12-11 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/943898 | Claims benefit of provisional | 62/081538 | 2014-11-18 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/232716 | 2015-09-25 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/213556 | 2015-09-02 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/209311 | 2015-08-24 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/205717 | 2015-08-15 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/199607 | 2015-07-31 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/197120 | 2015-07-27 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/188876 | 2015-07-06 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/182602 | 2015-06-21 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/175855 | 2015-06-15 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/174498 | 2015-06-11 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/171915 | 2015-06-05 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/157876 | 2015-05-06 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/154675 | 2015-04-29 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/153443 | 2015-04-27 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/139511 | 2015-03-27 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/111582 | 2015-02-03 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/100025 | 2015-01-05 |

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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/090879 | 2014-12-11 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US15/61120 | Claims benefit of provisional | 62/081538 | 2014-11-18 |
| Prior Application Status | ~~Pending~~ Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/947718 | Continuation of | PCT/US14/39208 | 2014-05-22 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US14/39208 | Claims benefit of provisional | 61/826446 | 2013-05-22 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US14/39208 | Claims benefit of provisional | 61/843021 | 2013-07-04 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US14/39208 | Claims benefit of provisional | 61/905109 | 2013-11-15 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US14/39208 | Claims benefit of provisional | 61/834873 | 2013-06-13 |
| Prior Application Status | ~~Pending~~ Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| 14/892821 | a 371 of international | PCT/US14/39208 | 2014-05-22 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US14/39208 | Claims benefit of provisional | 61/826446 | 2013-05-22 |

| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

| Prior Application Status | Expired | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US14/39208 | Claims benefit of provisional | 61/843021 | 2013-07-04 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US14/39208 | Claims benefit of provisional | 61/905109 | 2013-11-15 |
| Prior Application Status | Expired | | Remove |
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| PCT/US14/39208 | Claims benefit of provisional | 61/834873 | 2013-06-13 |
| Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. | | | |

## Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

| | | | Remove |
|---|---|---|---|
| Application Number | Country[i] | Filing Date (YYYY-MM-DD) | Access Code[i] (if applicable) |
| | | | |
| Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. | | | |

## Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (02-18)
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|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

## Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

**NOTE**: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

**1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)**

**A. Priority Document Exchange (PDX)** - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

**B. Search Results from U.S. Application to EPO** - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

**2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)**

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

**NOTE:** Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

## Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

**Applicant 1**

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

| | | |
|---|---|---|
| (●) Assignee | ( ) Legal Representative under 35 U.S.C. 117 | ( ) Joint Inventor |
| ( ) Person to whom the inventor is obligated to assign. | ( ) Person who shows sufficient proprietary interest | |

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

| | |
|---|---|
| Organization Name | W&W Sens Devices, Inc. |

**Mailing Address Information For Applicant:**

| | | | |
|---|---|---|---|
| **Address 1** | 38 Third Street, Suite 307 | | |
| Address 2 | | | |
| **City** | Los Altos | **State/Province** | CA |
| **Country** | US | Postal Code | 94022 |
| Phone Number | | Fax Number | |
| Email Address | | | |

Additional Applicant Data may be generated within this form by selecting the Add button.

## Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (02-18)
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| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

**Assignee 1**

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

| Prefix | **Given Name** | Middle Name | **Family Name** | Suffix |
|---|---|---|---|---|
| | | | | |

**Mailing Address Information For Assignee including Non-Applicant Assignee:**

| | | | |
|---|---|---|---|
| **Address 1** | | | |
| Address 2 | | | |
| **City** | | **State/Province** | |
| **Country** i | | Postal Code | |
| Phone Number | | Fax Number | |
| Email Address | | | |

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

## Signature:

**NOTE:** This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

| **Signature** | /Ivan S. Kavrukov/ | | | Date (YYYY-MM-DD) | ~~2023-10-30~~ 2024-02-29 |
|---|---|---|---|---|---|
| First Name | Ivan S. | Last Name | Kavrukov | Registration Number | 25,161 |

Additional Signature may be generated within this form by selecting the Add button.

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | 309-0015USCIP |
|---|---|---|
| | Application Number | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | |

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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# ELECTRONIC ACKNOWLEDGEMENT RECEIPT

| APPLICATION # | RECEIPT DATE / TIME | ATTORNEY DOCKET # |
|---|---|---|
| **18/385,213** | **02/29/2024 11:12:29 AM Z ET** | **309-0015USCIP** |

## Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

## Application Information

| | | | |
|---|---|---|---|
| APPLICATION TYPE | Utility - Nonprovisional Application under 35 USC 111(a) | PATENT # | - |
| CONFIRMATION # | 7381 | FILED BY | Mary Ellen Finnegan |
| PATENT CENTER # | 64496913 | FILING DATE | 10/30/2023 |
| CUSTOMER # | 139982 | FIRST NAMED INVENTOR | Shih-Yuan WANG |
| CORRESPONDENCE ADDRESS | - | AUTHORIZED BY | Ivan Kavrukov |

## Documents

**TOTAL DOCUMENTS: 2**

| DOCUMENT | PAGES | DESCRIPTION | SIZE (KB) |
|---|---|---|---|
| 309-0015USCIP_RequestForCorrectedFilingReceipt_Signed.pdf | 2 | Request for Corrected Filing Receipt | 467 KB |
| 309-0015USCIP__CorrectedADS_FINAL--Signed.pdf | 35 | Application Data Sheet | 9369 KB |

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## Digest

| DOCUMENT | MESSAGE DIGEST(SHA-512) |
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|---|---|
| 309-0015USCIP_RequestForCorrectedFilingReceipt_Signed.pdf | A09D4F365A46D03A9C278286FA6CD6DAFE41573AF862D5CA36572CE6CEFE7A87159FDD827927739BE35B6561054112AE6B75E92A4BCD8404A3D732FD50C7955D |
| 309-0015USCIP__CorrectedADS_FINAL--Signed.pdf | CC0B562AB5DE732AB7ADC276B2DA28542DDCEBCC6E9723F49A2260725C6D8083DA14E568C21410BE03989C13348EC61AD8113D1E0E657603F036511BFB0665A5 |

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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| APPLICATION NUMBER | FILING OR 371(C) DATE | FIRST NAMED APPLICANT | ATTY. DOCKET NO./TITLE |
|---|---|---|---|
| 18/385,213 | 10/30/2023 | Shih-Yuan WANG | 309-0015USCIP |

**CONFIRMATION NO. 7381**

139982
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

**PUBLICATION NOTICE**

*OC000000068651456*

Date Mailed: 02/22/2024

**Title:**MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

**Publication No.**US-2024-0063317-A1
**Publication Date:**02/22/2024

## NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 18/385,213 | 10/30/2023 | Shih-Yuan WANG | 309-0015USCIP | 7381 |

139982 7590 01/05/2024

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

| EXAMINER | |
|---|---|
| RODELA, EDUARDO A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2893 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 01/05/2024 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

| *Office Action Summary* | **Application No.** 18/385,213 | **Applicant(s)** WANG et al. | |
|---|---|---|---|
| | **Examiner** Eduardo A Rodela | **Art Unit** 2893 | **AIA (FITF) Status** Yes |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☑ Responsive to communication(s) filed on 12/8/2023.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims***

5) ☑ Claim(s) 1-12 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-12 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

**Application Papers**

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 10/30/2023 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

**Priority under 35 U.S.C. § 119**

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

**Certified copies:**

a)☑ All b)☐ Some** c)☐ None of the:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

## DETAILED ACTION

This correspondence is in response to the communications received October 30, 2023. Claims 1-12 are pending. This application has been granted expedited examination status on December 8, 2023.

### *Notice of Pre-AIA or AIA Status*

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

### *Priority*

It is acknowledged that this application is a continuation of several US applications including 14/947,718 (now US 10,622,498) which has priority benefit of at least Provisional applications 61/905,109 (with date November 15, 2013) and 61/843,021 (with date July 4, 2013). The effective filing date is the earliest of the supported parent applications which appears to be the provisional application 61/843,021, dated **July 4, 2013**.

### *Claim Objections*

Claim 1 is objected to because of the following informalities: In the recitation, "parts of *at least two of the holes* overlap such that at a surface of each of said pillars each of the *at least to holes* has a portion that overlaps with another of said *at least two holes* and a portion that does

not". The limitation of "at least two of the holes" as a label is seemingly repeated three times, but referred to with variations of "at least to holes" and "at least two holes" appear to inject a degree of confusion as to whether or not the same feature is being referred to. It is assumed that the same feature is being referred to, but a consistent label would prevent any confusion. Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 1 and the claims that depend therefrom are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-AIA 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention.

The claim 1 recitation, "parts of at least two of the holes overlap such that at a surface of each of said pillars each of the at least to holes has a portion that overlaps with another of said at least two holes and a portion that does not;

said at least two holes that overlap thereby form a depression in said surface that comprises a portion of only one of said two or more holes and a portion at which two of said two or more holes overlap", lacks support in the disclosure. It is unclear what all is entailed with regard to the "overlap".

In Applicant's specification, the term "overlap" or "overlapping" are contained within paragraphs 0195 ("overlap" with regard to "spacing between adjacent microstructure structures"), 0202 ("overlap" with regard to "spacing between adjacent microstructure structures"), 0216 ("overlap" with regard to "voids"), 0230 ("overlap" with regard to "voids"), 0233 ("overlap" with regard to "microstructured pillars"), 0235 ("overlap" with regard to "spacing between adjacent microstructures", 0256 ("overlap" with regard to "microstructure … distribution"), 0266 ("overlap" with regard to "optical field"), and 0269 ("overlap" with regard to "voids"). Each of the locations in the specification that discuss overlap, do not fully support the claim limitations as they do not clarify the meaning of what is being claimed.

The most pertinent portion appears to be in ¶ 0216, "FIG. 28 is a cross section showing microstructured voids buried or embedded in Si with a Si capping p+ anode layer 2826, according to some embodiments. The buried voids 2800 can be uniformly spaced, or with chirped spacing, or any complex patterns with a combination of periodic and aperiodic spacing or it can be random or pseudo-random. The buried voids 2800 can have a length ranging

approximately from 0.1 to 10 micrometers and lateral dimension ranging from 10-5000 nm. The voids can also be overlapping one another. Although FIG. 28 shows buried voids in Si, according to some embodiments buried voids can be formed in Ge. For example, in a Ge epitaxial layer on Si, or any other semiconductors, such as lnP, GaAs, lnGaAs, GaN, lnGaN, lnGaAsP, and other semiconductors in the III-V material family. The voids can be non-uniform is size and shape within the void and adjacent voids. The voids may also have nonuniform spacing and/or orientation. However, with proper process control uniformity in size and shape, patterning, random and pseudo-random placements of the voids can be attained. For simplicity the voids are shown to be uniform."

So from Examiner's understanding of this disclosure, if the voids are of different sizes or in different positions, there would be an orientation where when viewed along one direction, there would be overlap between two voids in pillars, and in another direction, there could be no overlap. Seemingly this arrangement would be satisfied by a showing of art which has voids in pillars that are not uniformly shaped or oriented. For purposes of examination, the above recitation will be interpreted in this manner. This however is just a guess by Examiner based upon the disclosure not fully supporting what is written in the highlighted limitation.

The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 and the claims that depend therefrom are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor (or for applications subject to pre-AIA 35 U.S.C. 112, the applicant), regards as the invention. It is unclear from the claim language which embodiment is being referred to, and thus the claim is rendered indefinite. The only embodiments which contain both "**plural pillars** of semiconductor material" and "deliberately formed **holes into said pillars**, filled at least partly with solid dielectric material" are the embodiments of Figs. 31 and 32, hereinafter referred to as the "pillar hole embodiment" (PHE). The PHE as claimed are further rendered indefinite as they lack any of the claim 1 limitations,

A. "parts of at least two of the holes overlap such that at a surface of each of said pillars each of the at least to holes has a portion that overlaps with another of said at least two holes and a portion that does not;

said at least two holes that overlap thereby form a depression in said surface that comprises a portion of only one of said two or more holes and a portion at which two of said two or more holes overlap", (the term "depression" in this limitation itself renders the claim indefinite as it is unclear in the PHE how the voids/holes "form a depression in said surface")

B. "side-isolation comprising solid material at sides of said pillars",

C. "a base dielectric region under the pillars that comprises solid dielectric material".

As such it is unclear what the metes and bounds of the light sensor array of pillars of claim 1 are being set forth.

***Relevant Prior Art***

Hsu et al. (US 7,525,170) Fig. 1A, 3G, 4G, shown below. This reference shows plural light sensitive pillars, but are lacking the holes formed in the pillars with dielectric filling.

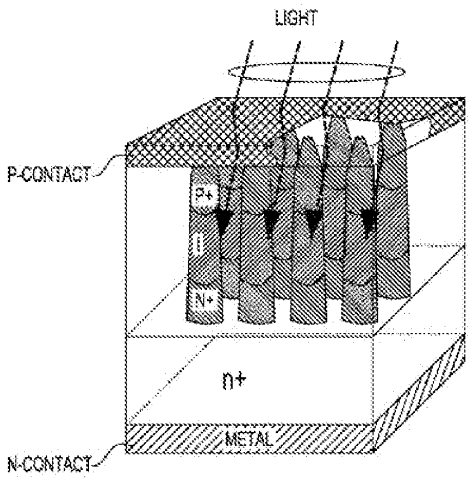



FIG. 1A

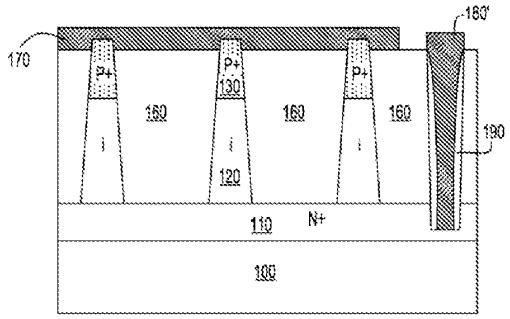



FIG. 3G

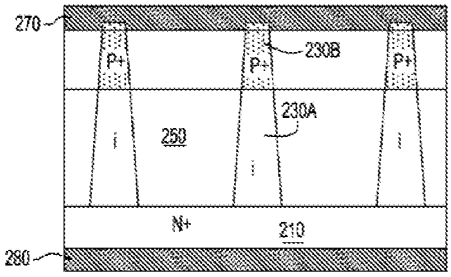



FIG. 4G

Dutta (US 8,357,960) Fig. 3A, shown below. This reference shows plural light sensitive pillars, but are lacking the holes formed in the pillars with dielectric filling.

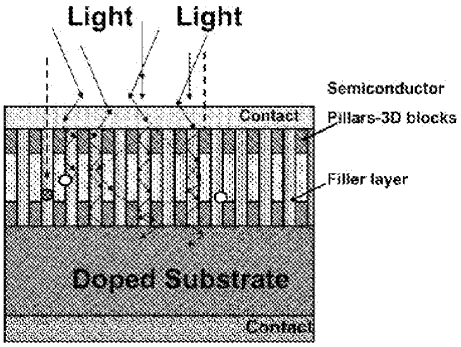
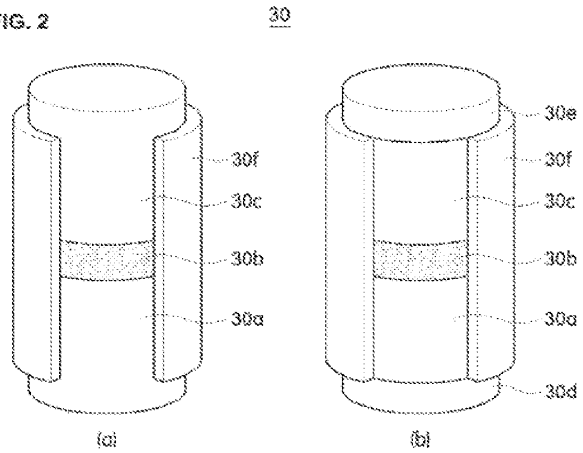


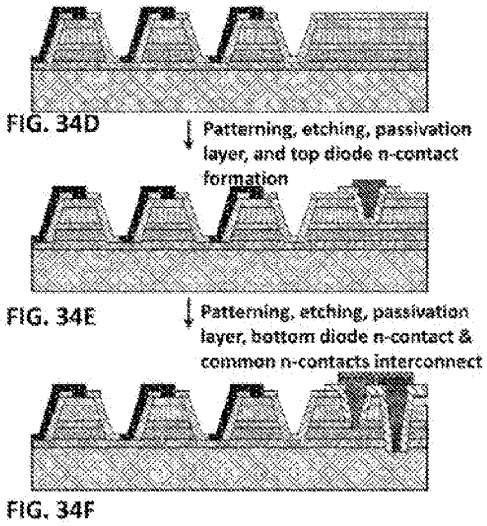

FIG.3A

Sung (US 11,728,457) Fig. 2, shown below, with dielectric sleeves 30f. This reference shows plural light sensitive pillars, but are lacking the holes formed in the pillars with dielectric filling.

FIG. 2

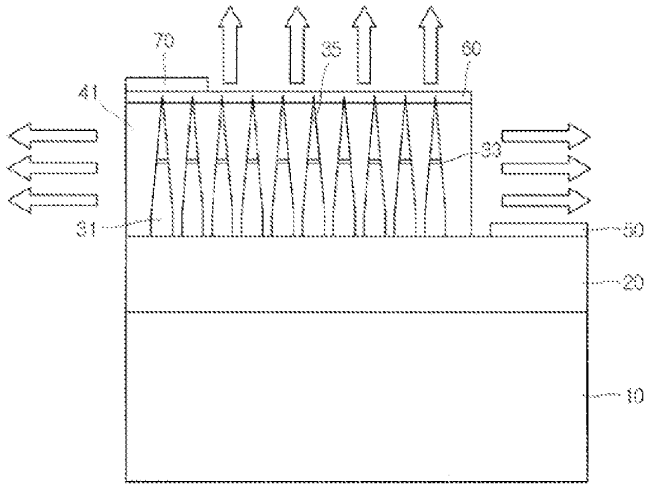



Dutta (US 9,184,202) Fig. 34F shown below. This reference shows plural light sensitive pillars, but are lacking the holes formed in the pillars with dielectric filling.




Kim et al. (US 7,396,696) Fig. 1a shown below. This reference shows plural light sensitive pillars, but are lacking the holes formed in the pillars with dielectric filling.

FIG. 1a




Yu et al. (US 8,946,675) Fig. 1a, shown below. This reference shows plural light sensitive pillars, but are lacking the holes formed in the pillars with dielectric filling.

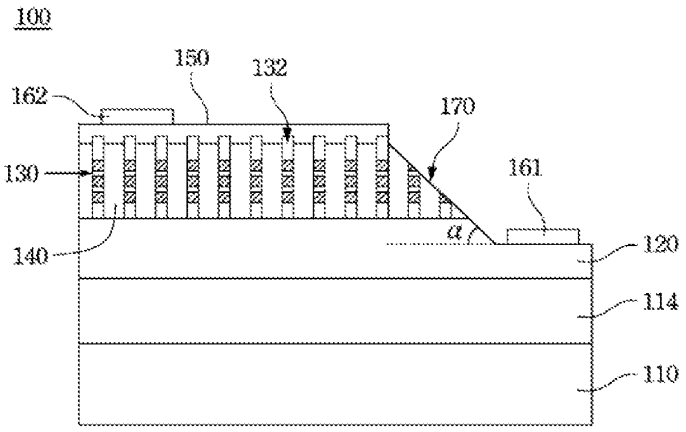



Fig. 1A

Cho et al. (US 8,129,710) Fig. 3, shown below. This reference shows plural light sensitive pillars, but are lacking the holes formed in the pillars with dielectric filling.

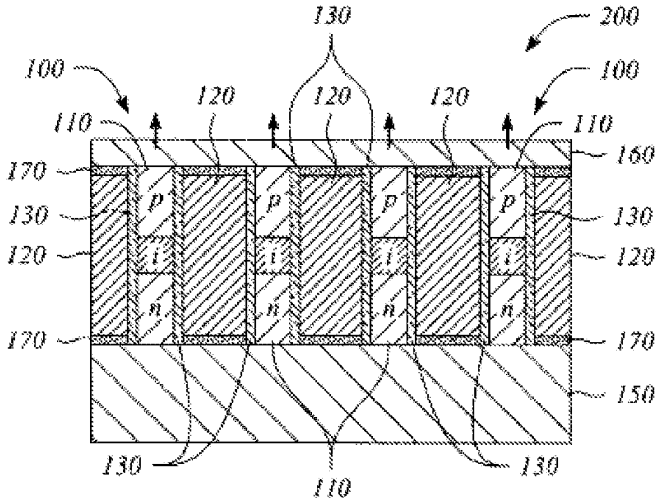



FIG. 3

Wagner et al. (US 6,879,014) Fig. 9 shown below. This reference shows plural light sensitive pillars, but are lacking the holes formed in the pillars with dielectric filling.

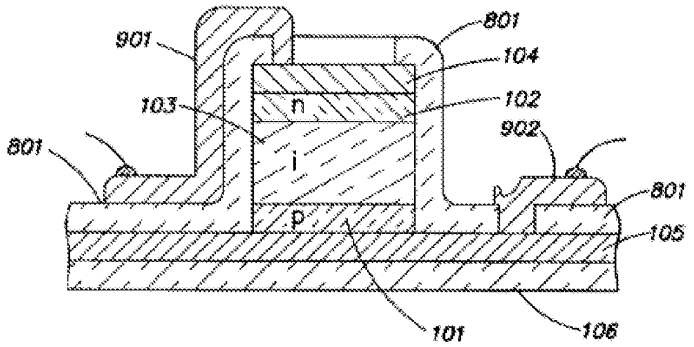
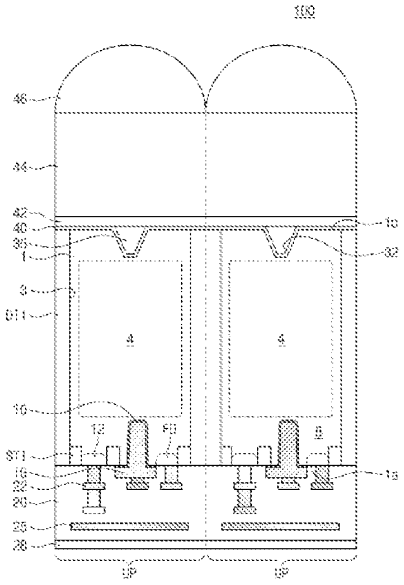



FIG. 9

Jin et al. (US 2018/0182806) Figs. 2, shown below, where there are individual pixel elements which have hole elements 35, ¶ 0052, “A light splitter 35”. This reference could be combined in a rejection of claim 1 content PHE, but lacks the claim language centered around the limitations of the hole/void “overlap” aspects.

FIG. 2



Wu et al. (US 11,211,419) Fig. 1A, shown below, is a light sensing array with pillar like cells which have voids/holes with dielectric fill, see elements 112, “absorption enhancement structures 112”, col. 4, line 32. This reference could be combined in a rejection of claim 1 content PHE, but lacks the claim language centered around the limitations of the hole/void “overlap” aspects.

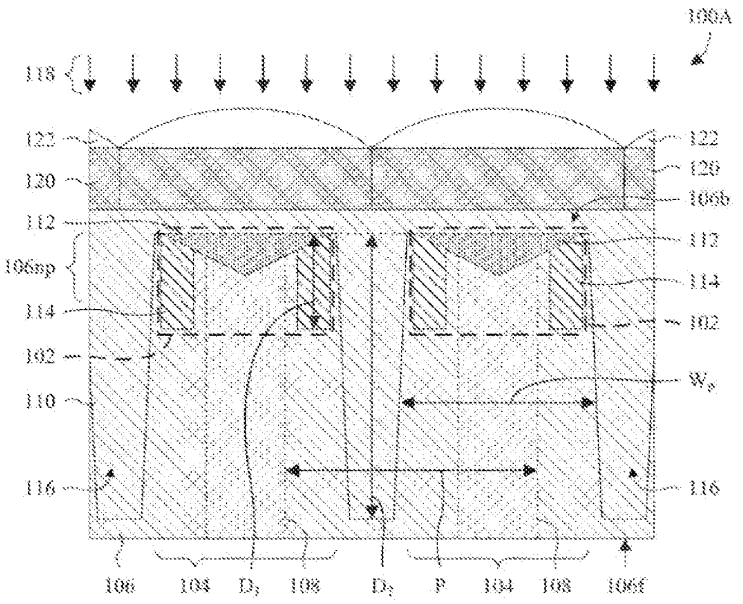



Fig. 1A

***Applicant's Claim to Figure Comparison***

It is noted that this comparison is merely for the benefit of reviewers of this office action during prosecution, to allow for an understanding of the examiner's interpretation of the Applicant's independent claims as compared to disclosed embodiments in Applicant's Figures. No response or comments are necessary from Applicant.

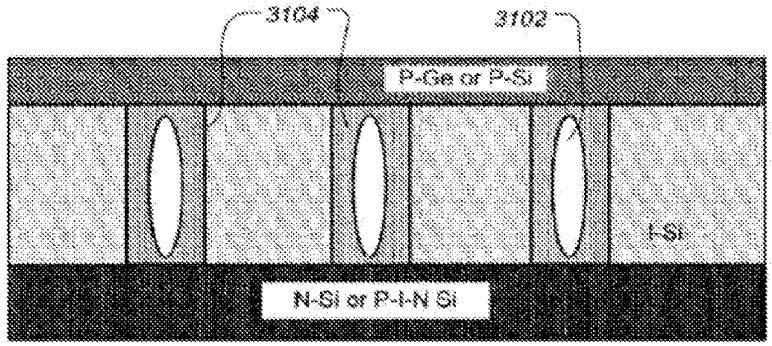



FIG. 31

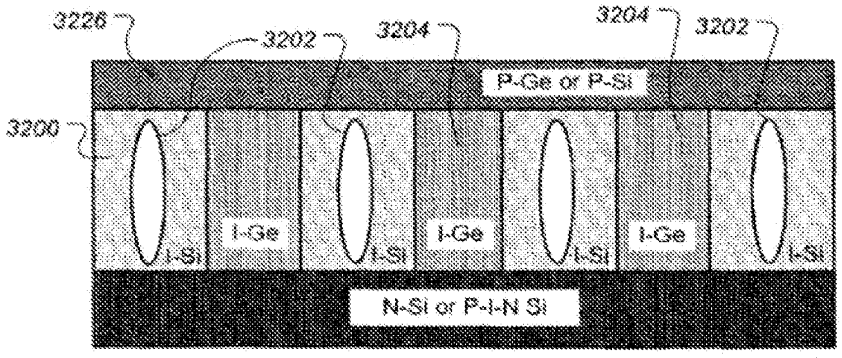



FIG. 32

**Regarding claim 1**, the Applicant discloses in Fig. 31 and 32, an integrated, single-chip structure of **plural pillars of semiconductor material** (3200) formed as respective photodetectors configured to generate electrical signals in response to illumination with light including light in the infrared and/or near infrared spectrum, said structure comprising:

**deliberately formed holes into said pillars** (3202), filled at least partly with solid dielectric material:

wherein:

parts of at least two of the holes overlap such that at a surface of each of said pillars each of the at least to holes has a portion that overlaps with another of said at least two holes and a portion that does not (it is unclear where and how this limitation relates to the PHE);

said at least two holes that overlap thereby form a depression in said surface that comprises a portion of only one of said two or more holes and a portion at which two of said two or more holes overlap (it is unclear where and how this limitation relates to the PHE), and

said two or more holes have: depths in the range of 100-10000 nm from said surface, and widths in the range of 100-2000 or 100-5000 nm along said surface in at least one direction;

side-isolation comprising solid material at sides of said pillars (it is unclear where and how this limitation relates to the PHE); and

a base dielectric region under the pillars that comprises solid dielectric material (it is unclear where and how this limitation relates to the PHE):

wherein said pillars are configured to receive said light directly or through other materials; and

wherein the presence of said holes and side-isolation increases effective quantum efficiency (EQE) of the pillars to illumination with said light relative to an otherwise same pillars lacking said holes (it is unclear where and how this limitation relates to the PHE).

***Contact Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A Rodela whose telephone number is (571)272-8797. The examiner can normally be reached M-F, 8:30-5:00pm ET.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yara B Green can be reached on (571) 270-3035. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC)

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Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EDUARDO A RODELA/
Primary Examiner, Art Unit 2893

| Notice of References Cited | Application/Control No. 18/385,213 | Applicant(s)/Patent Under Reexamination WANG et al. | |
|---|---|---|---|
| | Examiner Eduardo A Rodela | Art Unit 2893 | Page 1 of 1 |

**U.S. PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date YYYY-MM-DD | Name | CPC Classification | US Classification |
|---|---|---|---|---|---|---|
| * | A | US-7525170-B2 | 2009-04-28 | Hsu; Louis Lu-Chen | H01L31/1804 | 257/656 |
| * | B | US-8357960-B1 | 2013-01-22 | Dutta; Achyut Kumar | H01L31/1013 | 257/292 |
| * | C | US-11728457-B2 | 2023-08-15 | Sung; Yeon Goog | H01L33/0075 | 257/13 |
| * | D | US-9184202-B2 | 2015-11-10 | Dutta; Achyut | H01L27/1464 | 1/1 |
| * | E | US-7396696-B2 | 2008-07-08 | Kim; Hwa-Mok | H01L33/08 | 438/34 |
| * | F | US-8946675-B2 | 2015-02-03 | Yu; Chang-Chin | H01L33/06 | 257/14 |
| * | G | US-8129710-B2 | 2012-03-06 | Cho; Hans | H01L33/18 | 257/14 |
| * | H | US-6879014-B2 | 2005-04-12 | Wagner; Sigurd | H01L31/1872 | 257/434 |
| * | I | US-20180182806-A1 | 2018-06-28 | JIN; YOUNGGU | H01L27/14627 | 1/1 |
| * | J | US-11211419-B2 | 2021-12-28 | Wu; Wei Chuang | H01L27/14603 | 1/1 |
| | K | | | | | |
| | L | | | | | |
| | M | | | | | |

**FOREIGN PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date YYYY-MM-DD | Country | Name | CPC Classification |
|---|---|---|---|---|---|---|
| | N | | | | | |
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Dates in YYYY-MM-DD format are publication dates. Classifications may be US or foreign.

| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 18/385,213 | WANG et al. |
| | Examiner | Art Unit |
| | Eduardo A Rodela | 2893 |

| CPC - Searched* | | |
|---|---|---|
| Symbol | Date | Examiner |
| H01L31/02019; H01L31/022408; H01L31/02327; H01L31/02363; H01L31/028; H01L31/035281; H01L31/105; H01L31/107; H01L27/1446,146,14607,14625,14643,14649; H01L31/02027,02327,02363,035281,09,107,105 | 12/29/2023 | EAR |

| CPC Combination Sets - Searched* | | |
|---|---|---|
| Symbol | Date | Examiner |
| | | |

| US Classification - Searched* | | | |
|---|---|---|---|
| Class | Subclass | Date | Examiner |
| | | | |

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

| Search Notes | | |
|---|---|---|
| Search Notes | Date | Examiner |
| PE2E search - see history for complete details | 12/29/2023 | EAR |
| Inventor & Applicant search | 12/29/2023 | EAR |
| IEEE Xplore | 12/29/2023 | EAR |

| Interference Search | | | |
|---|---|---|---|
| US Class/CPC Symbol | US Subclass/CPC Group | Date | Examiner |
| | | | |

## PE2E SEARCH - Search History (Prior Art)

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | British Equivalents | Time Stamp |
|---|---|---|---|---|---|---|---|
| L1 | 77009 | (H01L31/02019 OR H01L31/022408 OR H01L31/02327 OR H01L31/02363 OR H01L31/028 OR H01L31/035281 OR H01L31/105 OR H01L31/107).cpc. | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/12/28 04:00 PM |
| L3 | 857 | ((("WANG") near3 ("Shih-Yuan")) OR (("WANG") near3 ("Shih-Ping"))).INV. | (US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT) | OR | ON | ON | 2023/12/28 04:01 PM |
| L9 | 6 | (W&W NEAR sens ) | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/12/28 04:04 PM |
| L10 | 0 | (L9 OR L3) AND ((integrated)(chip)(structure)(plural NEAR pillars)(semiconductor NEAR material)(photodetector $1)(light OR infrared)(holes)(filled)(solid NEAR dielectric NEAR material)(overlaps)(depression)(side-isolation)) | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) | AND | ON | ON | 2023/12/28 04:08 PM |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| L11 | 4374 | (pillar OR column) WITH ((P-I-N OR PIN) near3 (diode OR (light NEAR emitting NEAR diode) OR LED)) | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/12/28 04:30 PM |
| L12 | 4773380 | (pillar OR column) WITH (void OR gap OR cavity OR crevice OR hole) | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/12/28 04:31 PM |
| L13 | 2 | "10622498".pn. | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/12/28 04:46 PM |
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|---|---|---|---|---|---|---|---|
| | | | NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | | | | |
| L15 | 10 | ("11309444" \| "20100320444" \| "20110156195" \| "20110309331" \| "20120012741" \| "20120153127" \| "20180012918" \| "20180102442" \| "20180182806" \| "20190166317").pn. OR ("11621360").urpn. AND (PGPB \| USPT \| USOC).dbnm. | (US-PGPUB; USPAT; USOCR) | OR | ON | ON | 2023/12/28 05:09 PM |
| L16 | 1 | "7525170".pn. | (US-PGPUB; USPAT; USOCR) | OR | ON | ON | 2023/12/28 05:16 PM |
| L17 | 41 | (Artificial Intelligence) More like doc: US-7525170-B2<br>Text: (US-20080083963-A1 OR CN-101159277-A OR CN-100568516-C OR EP-2747154-B1 OR WO-2012054436-A1 OR EP-2717322-A1 OR US-20140166100-A1 OR CN-103415929-B OR CN-103415929-A OR WO-2012160662-A1 OR JP-WO2012160662-A1 OR TW-202147598-A OR US-9257583-B2 OR CN-103548149-A OR JP-5808400-B2 OR TW-I466307-B OR CN-103348486-B OR CN-103348486-A OR WO-2013009615-A1 OR US-20130009265-A1).did. | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/12/28 05:20 PM |
| L18 | 13 | ("4827114" \| "5055894" \| "6111305" \| "6177289" \| "6300648" \| "6451702" \| "6538299" \| "6707126").pn. OR ("7525170").urpn. AND (PGPB \| USPT \| USOC).dbnm. | (US-PGPUB; USPAT; USOCR) | OR | ON | ON | 2023/12/28 05:23 PM |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| L19 | 124019 | H01L27/1446,146,1460 7,14625,14643,14649.c pc. OR H01L31/02027,02327,0 2363,035281,09,107,10 5.pn. | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/12/28 05:37 PM |
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| L21 | 12 | (@rlpd<="20130704" OR @rlad<="20130704" OR @pd<="20130704" OR @ad<="20130704") AND L12 AND L11 AND L20 | (US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/12/28 05:37 PM |
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| | | | NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB) | | | | |
| L23 | 10 | ("11309444" \| "20100320444" \| "20110156195" \| "20110309331" \| "20120012741" \| "20120153127" \| "20180012918" \| "20180102442" \| "20180182806" \| "20190166317").pn. OR ("11621360").urpn. AND (PGPB \| USPT \| USOC).dbnm. | (US-PGPUB; USPAT; USOCR) | OR | ON | ON | 2023/12/28 05:40 PM |
| L24 | 60 | ("4571559" \| "4637129" \| "4716449" \| "5451767" \| "5457327" \| "5625636" \| "5757057" \| "5886374" \| "6027956" \| "6177289" \| "6667528" \| "7115971" \| "7397101" \| "7495306" \| "7601597" \| "7674563" \| "7772615" \| "7795064" \| "7893348" \| "7898052" \| "7972934" \| "8114695" \| "8129710" \| "8436370" \| "20050092925" \| "20050184354" \| "20070092192" \| "20070190434" \| "20080047604" \| "20080102582" \| "20080218740" \| "20080229941" \| "20080248608" \| "20080265449" \| "20090188557" \| "20090267049" \| "20100029067" \| "20100126548" \| "20100193768" \| "20100197068" \| "20100221866" \| "20100313941" \| "20120193676" \| "20120292676" \| "20130207222" \| "20140001528" \| "20150041965" \| "20160225631").pn. OR ("9496435").urpn. AND | (US-PGPUB; USPAT; USOCR) | OR | ON | ON | 2023/12/28 05:41 PM |

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| | | (PGPB \| USPT \| USOC).dbnm. | | | | | |
| L25 | 113 | ("4292512" \| "4571559" \| "4637129" \| "4716449" \| "4814847" \| "5244749" \| "5451767" \| "5457327" \| "5525828" \| "5625636" \| "5757057" \| "5886374" \| "6027956" \| "6177289" \| "6392282" \| "6406984" \| "6667528" \| "6724798" \| "6845034" \| "6879014" \| "7115971" \| "7161220" \| "7251386" \| "7340709" \| "7397101" \| "7495306" \| "7601597" \| "7605406" \| "7674563" \| "7772615" \| "7795064" \| "7893348" \| "7898052" \| "7972934" \| "7977637" \| "8114695" \| "8129710" \| "8319241" \| "8357960" \| "8436370" \| "8728847" \| "9045418" \| "9360554" \| "9496435" \| "9525084" \| "9530905" \| "9818893" \| "20020097962" \| "20030059820" \| "20030122210" \| "20040222357" \| "20050092925" \| "20050184354" \| "20060186501" \| "20060267054" \| "20070092192" \| "20070134840" \| "20070170536" \| "20070190434" \| "20070215968" \| "20070277869" \| "20080006891" \| "20080047604" \| "20080079022" \| "20080080854" \| "20080218740" \| "20080229941" \| "20080248608" \| "20080265449" \| "20090008735" \| "20090188557" \| "20090225804" \| "20090230498" \| "20090267049" \| "20090321868" \| "20100029067" \| "20100059789" \| "20100059822" \| "20100126548" \| | (US-PGPUB; USPAT; USOCR) | OR | ON | ON | 2023/12/28 05:42 PM |

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| L27 | 22 | ("3890161" \| "4990988" \| "5581091" \| "6027796" \| "6602620" \| "6946597" \| "20040033339" \| "20040043208" \| "20040048092" \| "20040144985" \| "20050032226" \| "20050053773").pn. OR ("7183127").urpn. AND (PGPB \| USPT \| USOC).dbnm. | (US-PGPUB; USPAT; USOCR) | OR | ON | ON | 2023/12/28 05:54 PM |
| L28 | 47 | ("6635494" \| "6773616" \| "6773946" \| "6791105" | (US-PGPUB; USPAT; USOCR) | OR | ON | ON | 2023/12/28 06:51 PM |

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| L29 | 25 | ("20060177660" \| "20060289761" \| "20070111493" \| "20070292080").pn. OR ("8129710").urpn. AND (PGPB \| USPT \| USOC).dbnm. | (US-PGPUB; USPAT; USOCR) | OR | ON | ON | 2023/12/29 10:12 AM |
| L30 | 39 | (Artificial Intelligence) More like doc: US-8129710-B2 Text: (US-20090267049-A1 OR US-20090179192-A1 OR US-8148800-B2 OR JP-2013508965-A OR JP-5903383-B2 OR CN-105594000-B OR CN-105594000-A OR KR-20160064109-A OR WO-2010027322-A1 OR EP-2321856-A1 OR JP-2012502466-A OR US-20110180894-A1 OR US-8692301-B2 OR JP-2010514207-A OR CN-107210350-A OR CN-107210350-B OR CN-102473802-A OR WO-2022040780-A1 OR EP-4205186-A1 OR WO-2014011202-A2).did. | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR | ON | ON | 2023/12/29 10:13 AM |
| L31 | 22 | ("3990059" \| "4875084" \| "5285078" \| "5318676" \| "5525828" \| "5696629" \| "5942771" \| "6177289" \| "6265823" \| "6451702" \| "6683367" \| "20030094664" \| "20040038503").pn. OR ("7161220").urpn. AND (PGPB \| USPT \| USOC).dbnm. | (US-PGPUB; USPAT; USOCR) | OR | ON | ON | 2023/12/29 10:37 AM |
| L32 | 40 | (Artificial Intelligence) More like doc: | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, | OR | ON | ON | 2023/12/29 10:38 AM |

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|---|---|---|---|---|---|---|---|
| | | US-7161220-B2<br>Text:<br>(US-20060118894-A1 OR US-7022544-B2 OR US-20040119093-A1 OR KR-20040054490-A OR TW-I252591-B OR KR-100558803-B1 OR JP-3872473-B2 OR JP-2004200685-A OR CN-1278431-C OR CN-1508885-A OR TW-200419817-A OR KR-20160039150-A OR EP-3000134-A2 OR CN-114188426-A OR CN-114188426-B OR EP-3000134-B1 OR KR-102358584-B1 OR CA-2493465-C OR CN-106847958-A OR EP-1258927-A1).did. | AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) | | | | |
| L33 | 13 | ("3990059" \| "4875084" \| "5285078" \| "5318676" \| "5525828" \| "5696629" \| "6177289" \| "6265823" \| "6451702" \| "6683367" \| "20030094664").pn. OR ("7022544").urpn. AND (PGPB \| USPT \| USOC).dbnm. | (US-PGPUB; USPAT; USOCR) | OR | ON | ON | 2023/12/29 10:39 AM |
| L34 | 75 | ("4885622" \| "5162239" \| "5185272" \| "5528071" \| "5539848" \| "5599403" \| "5742630" \| "5751757" \| "5767712" \| "5790255" \| "5942050" \| "5953355" \| "6037644").pn. OR ("6879014").urpn. AND (PGPB \| USPT \| USOC).dbnm. | (US-PGPUB; USPAT; USOCR) | OR | ON | ON | 2023/12/29 11:57 AM |
| L35 | 1 | "11309444".pn. | (USPAT) | OR | ON | ON | 2023/12/29 02:56 PM |
| L36 | 1 | "20180182806" | (US-PGPUB) | OR | ON | ON | 2023/12/29 03:00 PM |
| L37 | 37 | (Artificial Intelligence)<br>More like doc:<br>US-20180182806-A1<br>Text:<br>(US-10050078-B2 OR CN-108257985-A OR KR-20180077393-A OR US-20230307482-A1 OR JP-6441711-B2 OR KR-20230138186-A OR US-20230136919-A1 | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, | OR | ON | ON | 2023/12/30 09:25 AM |

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|---|---|---|---|---|---|---|---|
| | | OR US-20220109014-A1 OR US-20210335862-A1 OR JP-2023036529-A OR KR-20220147503-A OR KR-20230033963-A OR CN-104282703-A OR US-20220020804-A1 OR US-10651225-B2 OR US-20220045117-A1 OR US-11158664-B2 OR US-11764248-B2 OR US-20220149101-A1 OR KR-20210053152-A).did. | RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) | | | | |
| L38 | 5 | ("2018/0182806").urpn. AND (PGPB \| USPT \| USOC).dbnm. | (US-PGPUB; USPAT; USOCR) | OR | ON | ON | 2023/12/30 10:21 AM |

## PE2E SEARCH - Search History (Interference)

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|---|
| There are no Interference searches to show. |

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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 18/385,213 | 10/30/2023 | Shih-Yuan WANG | 309-0015USCIP | 7381 |

139982 7590 12/08/2023

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

| EXAMINER | |
|---|---|
| CENTRAL, DOCKET | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2893 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 12/08/2023 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

PTOL-90A (Rev. 04/07)

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United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
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| | | |
|---|---|---|
| In re Application of | : | |
| W&W Sens Devices, Inc. | : | |
| Application No. 18/385,213 | : | |
| Filed: October 30, 2023 | : | DECISION ON PETITION |
| For: MICROSTRUCTURE ENHANCED | : | |
| ABSORPTION PHOTOSENSITIVE | : | |
| DEVICES | : | |

This is a decision on the petition under 37 CFR 1.102(c)(1), filed October 30, 2023, to make the above-identified application special based on applicant's age as set forth in MPEP § 708.02, Section II.

The petition is **GRANTED**.

A grantable petition to make an application special under 37 CFR 1.102(c)(1) and MPEP § 708.02, Section II: Applicant's Age, must be accompanied by evidence showing that the applicant is 65 years of age, or more, such as applicant's statement or a statement from a registered practitioner that he or she has evidence that the applicant is 65 years of age or older. No fee is required.

The instant petition includes a statement from the inventor declaring that he is 65 years of age or older. Accordingly, the above-identified application has been accorded "special" status.

Telephone inquiries concerning this decision should be directed to Terri Johnson at 571-272-2991. All other inquiries concerning either the examination or status of the application should be directed to the Technology Center.

/TERRI S JOHNSON/
Paralegal Specialist, OPET

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NUMBER | FILING or 371(c) DATE | GRP ART UNIT | FIL FEE REC'D | ATTY.DOCKET.NO | TOT CLAIMS | IND CLAIMS |
|---|---|---|---|---|---|---|
| 18/385,213 | 10/30/2023 | | 896 | 309-0015USCIP | 12 | 1 |

**CONFIRMATION NO. 7381**

139982
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

**FILING RECEIPT**




Date Mailed: 11/16/2023

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

**Please verify the accuracy of the data presented on this receipt.** If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

**Inventor(s)**

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping WANG, Los Altos, CA;

**Applicant(s)**

W&W Sens Devices, Inc., Los Altos, CA;

**Power of Attorney:** The patent practitioners associated with Customer Number 139982

**Domestic Priority data as claimed by applicant**

This application is a CIP of 17/974,325 10/26/2022 PAT 11,830,954
and is a CIP of 18/113,474 02/23/2023
which is a DIV of 17/707,429 03/29/2022 PAT 11,621,360
which is a DIV of 17/532,831 11/22/2021 PAT 11,309,444
which is a CIP of 17/182,954 02/23/2021 PAT 11,791,432
which is a DIV of 16/528,958 08/01/2019 PAT 11,121,271
which is a CIP of 14/947,718 11/20/2015 PAT 10,622,498
and is a CIP of PCT/US16/67977 12/21/2016
and is a CIP of 15/797,821 10/30/2017 PAT 10,446,700 *
and is a CIP of 16/042,535 07/23/2018 PAT 10,700,225
and is a CIP of 16/296,985 03/08/2019 PAT 10,468,543
and is a CIP of PCT/US18/43289 07/23/2018
and is a CIP of PCT/US18/57963 10/29/2018
and claims benefit of 62/713,455 08/01/2018
and claims benefit of 62/716,310 08/08/2018

and claims benefit of 62/717,750 08/10/2018
and claims benefit of 62/719,689 08/19/2018
and claims benefit of 62/724,449 08/29/2018
and claims benefit of 62/733,476 09/19/2018
and claims benefit of 62/737,062 09/26/2018
and claims benefit of 62/750,016 10/24/2018
and claims benefit of 62/770,656 11/21/2018 *
and claims benefit of 62/772,498 11/28/2018 *
and claims benefit of 62/777,157 12/09/2018
and claims benefit of 62/779,693 12/14/2018
and claims benefit of 62/784,342 12/21/2018
and claims benefit of 62/794,330 01/18/2019
and claims benefit of 62/797,141 01/25/2019
and claims benefit of 62/797,263 01/26/2019
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and claims benefit of 62/802,171 02/06/2019
and claims benefit of 62/802,718 02/08/2019
and claims benefit of 62/805,850 02/14/2019
and claims benefit of 62/808,949 02/22/2019
and claims benefit of 62/819,604 03/17/2019
and claims benefit of 62/819,669 03/17/2019
and claims benefit of 62/820,695 03/19/2019
and claims benefit of 62/828,976 04/03/2019
and claims benefit of 62/841,798 05/01/2019
and claims benefit of 62/843,206 05/03/2019
and claims benefit of 62/846,554 05/10/2019
and claims benefit of 62/853,280 05/28/2019
and claims benefit of 62/860,115 06/11/2019
and claims benefit of 62/863,231 06/18/2019
and claims benefit of 62/863,852 06/19/2019
and claims benefit of 62/867,186 06/26/2019
and claims benefit of 62/868,911 06/29/2019
and claims benefit of 62/870,533 07/03/2019
and claims benefit of 62/873,891 07/13/2019
and claims benefit of 62/874,418 07/15/2019
and said PCT/US18/57963 10/29/2018 is a CON of 16/797,821 02/21/2020 PAT 11,489,420 *
and said 15/797,821 10/30/2017 is a CIP of 14/947,718 11/20/2015 PAT 10,622,498
and is a CIP of 15/309,922 11/09/2016 PAT 9,818,893
and is a CIP of PCT/US16/67977 12/21/2016
and claims benefit of 62/465,734 03/01/2017
and claims benefit of 62/474,179 03/21/2017
and claims benefit of 62/484,474 04/12/2017
and claims benefit of 62/487,606 04/20/2017
and claims benefit of 62/488,998 04/24/2017
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and claims benefit of 62/505,974 05/14/2017
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and claims benefit of 62/514,889 06/04/2017
and claims benefit of 62/521,504 06/18/2017
and claims benefit of 62/522,169 06/20/2017

and claims benefit of 62/527,962 06/30/2017
and claims benefit of 62/530,281 07/09/2017 *
and claims benefit of 62/533,078 07/16/2017
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and claims benefit of 62/542,243 08/07/2017
and claims benefit of 62/547,728 08/18/2017
and claims benefit of 62/553,844 09/02/2017
and claims benefit of 62/556,426 09/10/2017
and claims benefit of 62/561,869 09/22/2017
and said PCT/US18/43289 07/23/2018 claims benefit of 62/542,243 08/07/2017
and claims benefit of 62/535,801 07/21/2017
and claims benefit of 62/540,524 08/02/2017
and claims benefit of 62/639,472 03/06/2018
and claims benefit of 62/628,764 02/09/2018
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and claims benefit of 62/666,005 05/02/2018
and claims benefit of 62/556,426 09/10/2017
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and claims benefit of 62/639,356 03/06/2018
and claims benefit of 62/615,314 01/09/2018
and claims benefit of 62/623,971 01/30/2018
and claims benefit of 62/561,869 09/22/2017
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and claims benefit of 62/669,194 05/09/2018
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and claims benefit of 62/547,728 08/18/2017
and claims benefit of 62/651,087 03/31/2018
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and claims benefit of 62/662,217 04/24/2018
and claims benefit of 62/639,920 03/07/2018
and claims benefit of 62/633,514 02/21/2018
and said 16/296,985 03/08/2019 is a CON of 15/797,821 10/30/2017 PAT 10,446,700
and said 16/042,535 07/23/2018 is a CIP of 15/797,821 10/30/2017 PAT 10,446,700
and claims benefit of 62/535,801 07/21/2017
and claims benefit of 62/540,524 08/02/2017
and claims benefit of 62/542,243 08/07/2017

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and claims benefit of 62/659,072 04/17/2018
and claims benefit of 62/662,217 04/24/2018
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and claims benefit of 62/669,194 05/09/2018
and claims benefit of 62/675,130 05/22/2018
and claims benefit of 62/677,609 05/29/2018
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and claims benefit of 62/334,934 05/11/2016
and claims benefit of 62/338,263 05/18/2016
and claims benefit of 62/346,850 06/07/2016
and claims benefit of 62/359,349 07/07/2016 *
and claims benefit of 62/366,188 07/25/2016
and claims benefit of 62/368,109 07/28/2016
and claims benefit of 62/374,828 08/13/2016
and claims benefit of 62/376,869 08/18/2016
and claims benefit of 62/380,364 08/27/2016
and claims benefit of 62/383,391 09/03/2016
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and claims benefit of 62/394,222 09/14/2016
and claims benefit of 62/398,607 09/23/2016
and claims benefit of 62/401,126 09/28/2016
and claims benefit of 62/406,999 10/12/2016
and claims benefit of 62/414,671 10/29/2016

and claims benefit of 62/415,339 10/31/2016
and said 15/309,922 11/09/2016 is a 371 of PCT/US15/61120 11/17/2015
and is a CON of 14/943,898 11/17/2015 PAT 9,530,905
and is a CON of 14/945,003 11/18/2015 PAT 9,525,084
which claims benefit of 62/232,716 09/25/2015
and claims benefit of 62/213,558 09/02/2015
and claims benefit of 62/209,311 08/24/2015
and claims benefit of 62/205,717 08/15/2015
and claims benefit of 62/199,607 07/31/2015 *
and claims benefit of 62/197,120 07/27/2015
and claims benefit of 62/188,876 07/06/2015
and claims benefit of 62/182,602 06/21/2015
and claims benefit of 62/175,855 06/15/2015
and claims benefit of 62/174,498 06/11/2015
and claims benefit of 62/171,915 06/05/2015
and claims benefit of 62/157,876 05/06/2015
and claims benefit of 62/154,675 04/29/2015
and claims benefit of 62/153,443 04/27/2015
and claims benefit of 62/139,511 03/27/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/100,025 01/05/2015
and claims benefit of 62/090,879 12/11/2014
and claims benefit of 62/081,538 11/18/2014
and said 14/943,898 11/17/2015 claims benefit of 62/232,716 09/25/2015
and claims benefit of 62/213,556 09/02/2015
and claims benefit of 62/209,311 08/24/2015
and claims benefit of 62/205,717 08/15/2015
and claims benefit of 62/199,607 07/31/2015
and claims benefit of 62/197,120 07/27/2015
and claims benefit of 62/188,876 07/06/2015
and claims benefit of 62/182,602 06/21/2015
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and claims benefit of 62/174,498 06/11/2015
and claims benefit of 62/171,915 06/05/2015
and claims benefit of 62/157,876 05/06/2015
and claims benefit of 62/154,675 04/29/2015
and claims benefit of 62/153,443 04/27/2015
and claims benefit of 62/139,511 03/27/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/100,025 01/05/2015
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and said PCT/US15/61120 11/17/2015 claims benefit of 62/232,716 09/25/2015
and claims benefit of 62/213,556 09/02/2015
and claims benefit of 62/209,311 08/24/2015
and claims benefit of 62/205,717 08/15/2015
and claims benefit of 62/199,607 07/31/2015
and claims benefit of 62/197,120 07/27/2015
and claims benefit of 62/188,876 07/06/2015
and claims benefit of 62/182,602 06/21/2015
and claims benefit of 62/175,855 06/15/2015

and claims benefit of 62/174,498 06/11/2015
and claims benefit of 62/171,915 06/05/2015
and claims benefit of 62/157,876 05/06/2015
and claims benefit of 62/154,675 04/29/2015
and claims benefit of 62/153,443 04/27/2015
and claims benefit of 62/139,511 03/27/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/100,025 01/05/2015
and claims benefit of 62/090,879 12/11/2014
and claims benefit of 62/081,538 11/18/2014
and said 14/947,718 11/20/2015 is a CON of PCT/US14/39208 05/22/2014
which claims benefit of 61/826,446 05/22/2013
and claims benefit of 61/843,021 07/04/2013
and claims benefit of 61/905,109 11/15/2013
and claims benefit of 61/834,873 06/13/2013
and claims benefit of 61/826,446 05/22/2013
and claims benefit of 61/843,021 07/04/2013
and claims benefit of 61/905,109 11/15/2013
and claims benefit of 61/834,873 06/13/2013

**(*) Data provided by applicant is not consistent with PTO records.**

Foreign Applications for which priority is claimed (You may be eligible to benefit from the Patent Prosecution Highway program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

**Permission to Access Application via Priority Document Exchange:** Yes

**Permission to Access Search Results:** Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

**If Required, Foreign Filing License Granted:** 11/14/2023

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 18/385,213**

**Projected Publication Date:** 02/22/2024

**Non-Publication Request:** No

**Early Publication Request:** No
**** SMALL ENTITY ****
**Title**

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

**Preliminary Class**

**Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications:** No

## PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

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## Title 37, Code of Federal Regulations, 5.11 & 5.15

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The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

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## PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 18/385,213

### APPLICATION AS FILED - PART I

| FOR | (Column 1) NUMBER FILED | (Column 2) NUMBER EXTRA | SMALL ENTITY RATE($) | SMALL ENTITY FEE($) | OR | OTHER THAN SMALL ENTITY RATE($) | OTHER THAN SMALL ENTITY FEE($) |
|---|---|---|---|---|---|---|---|
| BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | 64 | | N/A | |
| SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | 280 | | N/A | |
| EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | 320 | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | 12 minus 20 = | * 0 | x = | 0 | OR | | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | 1 minus 3 = | * | x = | 0 | | | |
| APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | 168 | | | |
| MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | 0 | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | 832 | | TOTAL | |

### APPLICATION AS AMENDED - PART II

| | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | SMALL ENTITY RATE($) | SMALL ENTITY ADDITIONAL FEE($) | OR | OTHER THAN SMALL ENTITY RATE($) | OTHER THAN SMALL ENTITY ADDITIONAL FEE($) |
|---|---|---|---|---|---|---|---|---|---|---|
| AMENDMENT A | Total (37 CFR 1.16(i)) | * | Minus | ** | = | x = | | OR | x = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | x = | | OR | x = | |
| | Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

| | | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | RATE($) | ADDITIONAL FEE($) | OR | RATE($) | ADDITIONAL FEE($) |
|---|---|---|---|---|---|---|---|---|---|---|
| AMENDMENT B | Total (37 CFR 1.16(i)) | * | Minus | ** | = | x = | | OR | x = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | x = | | OR | x = | |
| | Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| | FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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Kathi Vidal

**Kathi Vidal**
Under Secretary of Commerce for Intellectual Property and
Director of the United States Patent and Trademark Office

**Derrick Brent**
Deputy Under Secretary of Commerce for Intellectual Property and
Deputy Director of the United States Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NUMBER | FILING OR 371(C) DATE | FIRST NAMED APPLICANT | ATTY. DOCKET NO./TITLE |
|---|---|---|---|
| 18/385,213 | 10/30/2023 | Shih-Yuan WANG | 309-0015USCIP |

**CONFIRMATION NO. 7381**

139982
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

**IMPROPER CFR REQUEST**

*OC000000064569531*

Date Mailed: 11/16/2023

## RESPONSE TO REQUEST FOR CORRECTED FILING RECEIPT

***Continuity, Priority Claims, Petitions, and Non-Publication Requests***

In response to your request for a corrected Filing Receipt, the Office is unable to comply with your request because:

- One or more of the benefit claims under 35 U.S.C. § 120 cannot be included on the Filing Receipt since applicant did not specify whether the application is a continuation, divisional or continuation-in-part of the prior application. Applicant must submit a new application data sheet (ADS) that sets forth the relationship, and the ADS must be accompanied by a petition under 37 CFR 1.78 if filed after the time period set forth in 37 CFR 1.78.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/spkannathip/

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Sale Accounting Date:11/14/2023

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| 18385213 | 10/30/2023 |

| Document Number | Fee Code | Fee Code Description | Amount Paid | Payment Method |
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| I2023ADH20119913 | 2081 | UTILITY APPL SIZE FEE PER 50 SHEETS >100 | $168.00 | Deposit Account |

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# DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES |
|---|---|

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 18/385,213 filed on October 30, 2023.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

## WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Shih-Yuan Wang Date (Optional) :

Signature: Shih-Yuan Wang

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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# DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES |
|---|---|

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 18/385,213 filed on October 30, 2023.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: Shih-Ping Wang Date (Optional): _____

Signature: S.P. Wang

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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| Electronic Acknowledgement Receipt | |
|---|---|
| **EFS ID:** | 48804732 |
| **Application Number:** | 18385213 |
| **International Application Number:** | |
| **Confirmation Number:** | 7381 |
| **Title of Invention:** | APPARATUS AND METHOD TO FACILITATE INTRODUCTION OF A CERVICAL BALLOON CATHETER |
| **First Named Inventor/Applicant Name:** | SHIH-PING Wang |
| **Customer Number:** | 139982 |
| **Filer:** | Ivan Kavrukov/Mary Ellen Finnegan |
| **Filer Authorized By:** | Ivan Kavrukov |
| **Attorney Docket Number:** | 309-0015USCIP |
| **Receipt Date:** | 07-NOV-2023 |
| **Filing Date:** | |
| **Time Stamp:** | 10:19:53 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| Submitted with Payment | no |
|---|---|

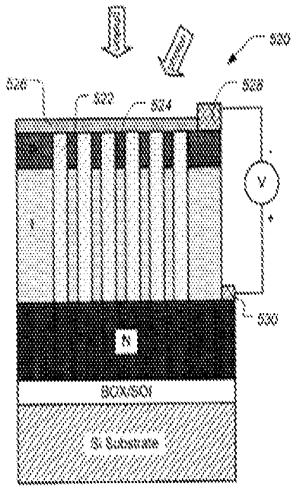
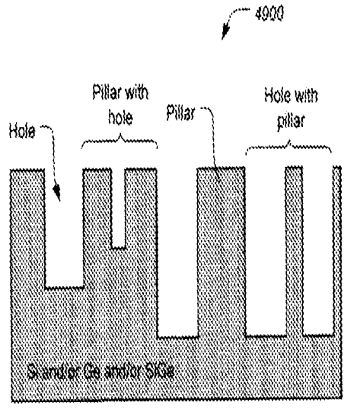
## File Listing:

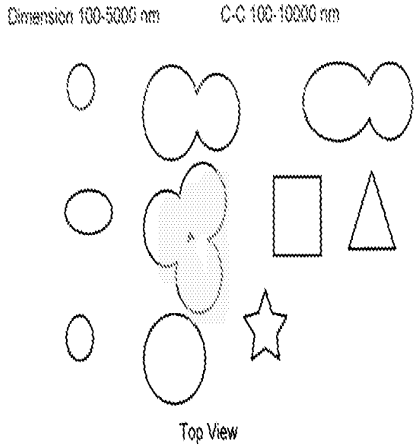
| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | Oath or Declaration filed | 309-0015USCIP_Declaration_Shih-YuanWANG-signed.pdf | 180504<br>4642913f1e303cd2cb0964562352354bec37db56 | no | 2 |
| **Warnings:** | | | | | |

| Information: | | | | | |
|---|---|---|---|---|---|
| 2 | Oath or Declaration filed | 309-0015USCIP_Declaration_ShihPingWANG-signed.pdf | 369283<br>668294d06fe1035fe4f5ac93d76bbd0e3af6b512 | no | 1 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| | | | **Total Files Size (in bytes):** | 549787 | |

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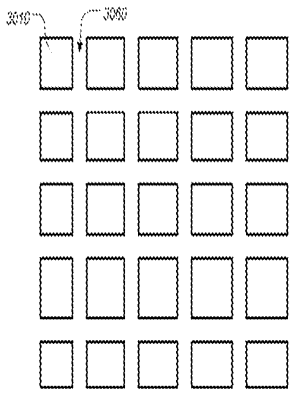
**New Applications Under 35 U.S.C. 111**
**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**
**National Stage of an International Application under 35 U.S.C. 371**
**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**
**New International Application Filed with the USPTO as a Receiving Office**
**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

| | |
|---|---|
| | **Example of support in pending Ser. No. 18/113,474 which claims priority to ultimate U.S. parent filing Ser. No. 14/974,718, now patent 10,622,498, which in turn claims priority to PCT filed 05/22/2014 and its provisionals including 61/834,873.**<br>**Paragraph references below are to published version US 2016/0254407 A1 of Ser. No. 14/947,718.** |
| 1.An integrated, single-chip structure of plural pillars of semiconductor material formed as respective photodetectors configured to generate electrical signals in response to illumination with light including light in the infrared and/or near infrared spectrum, said structure comprising: | FIG. 5B, pillars 524. Para. [0120].<br>  <br><br>FIG. 5B |
| deliberately formed holes into said pillars, filled at least partly with solid dielectric material; | FIG. 49 ("Pillar with hole"). Para. [0239] ("hole(s) can exist in a pillar").<br>  <br><br>FIG. 49 |

| | |
|---|---|
| wherein:<br>parts of at least two of the holes overlap such that at a surface of each of said pillars each of the at least to holes has a portion that overlaps with another of said at least two holes and a portion that does not;<br>said at least two holes that overlap thereby form a depression in said surface that comprises a portion of only one of said two or more holes and a portion at which two of said two or more holes overlap, and<br>said two or more holes have:<br>depths in the range of 100-10000 nm from said surface, and<br>widths in the range of 100-5000 nm along said surface in at least one direction; | FIG. 46. Para. [0235] ("hole array 4600 having various shapes such as oval, circular, rectangle, doublets, triplets, and stars").<br>  <br><br>FIG. 46<br>Para. [0143] ("The depth (or length) of the holes can be 100 to 10000 nm and can be uniform depth of non-uniform depth."). Para. 238 ("According to some embodiments, the holes have diameters ranging from 10 nm to 5000 nm and depths ranging from 0.1 to 10 microns").<br><br>Para. [0234] ("hole array 4300 (also applicable to embedded or buried voids) that is uniformly spaced with a fixed diameter ranging from 100-5000 nm"); para. 235 ("hole array 4500 having both variable diameters (ranging from 100 nm to 5000 nm) . . ."). |
| side-isolation comprising solid material at sides of said pillars; and | FIG. 5B: isolation material 522 surrounds pillars 524. |
| a base dielectric region under the pillars that comprises solid dielectric material; | Fig. 5B: region 504 labeled "BOX/SOI." Para. 119. |

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| wherein said pillars are configured to receive said light directly or through other materials; and | FIG. 5B. The top surfaces of pillars 524 receive light. |
| wherein the presence of said holes and side-isolation increases effective quantum efficiency (EQE) of the pillars to illumination with said light relative to an otherwise same pillars lacking said holes. | Para. [0076]. Compare FIG. 4B (Para. [0115]) and FIG. 3B (Para [0110]) showing QE at 850 nm (in infrared range). |
| | |
| 2.The integrated, single-chip structure of claim 1, wherein said at least two holes comprise at least three holes each of which has a portion that overlaps with another of said at least three holes and a portion that does not. | FIG. 46. Para [0235 ("hole array 49600 having various shapes such as . . . triplets . . .") |
| | |
| 3.The integrated, single-chip structure of claim 1, in which said pillars comprise semiconductor material that is doped at one portion of the pillar but is less doped or is undoped at a portion of the pillar adjacent the doped portion. | FOGs. 5A-B. P-material 510 is doped while |
| | |
| 4.The integrated, single-chip structure of claim 3, in which the pillars are elongated in an up-down direction and the more doped portion of each pillar is over the less doped or undoped portion thereof. | Figs. 5A-B: regions 510 and 506 are doped to opposite polarities and region 508 is undoped or low-doped. Para. 119. |

| | |
|---|---|
| 5.The integrated, single-chip structure of claim 1, further including electrical contacts to said pillars configured to provide an electrical field across said pillars. | FIG. 5B, contacts 528, 530. Para. [0121]. |
| | |
| 6. The integrated, single-chip structure of claim 5, in which two or more of said pillars share one of said electrical contacts. | Provisional appln. 61/834,873 filed June 13, 2013, sentence bridging pages 1 and 2: (". . . the detector array can be monolithically integrated with Si electronic devices such as bipolar transistors, CMOS, Bi-CMOA, application specific integrated circuits (ASIC) for signal processing, storage, signal conditioning, and transmission.") |
| | |
| 7. The integrated, single-chip structure of claim 1, further including active electronic circuits integrated with said pillars. | Provisional application 61/834,873 filed June 13, 2013, sentence bridging pages 1 and 2 ("Another advantage of Si is increase in functionality; the detector array can be monolithically integrated with Si electronic circuit devices such as bipolar transistors, CMOS, bi-CMOS application specific integrated circuits (ASIC) for signal processing, storage, signal conditioning, and transmission.") |
| | |
| 8. The integrated, single-chip structure of claim 7, in which said active electronic circuits comprises Si-based active circuits for signal processing of electrical signals generated by said pillars. | Provisional application 61/834,873 filed June 13, 2013, sentence bridging pages 1 and 2 ("Another advantage of Si is increase in functionality; the detector array can be monolithically integrated with Si electronic circuit devices such as bipolar transistors, CMOS, bi-CMOS application specific integrated circuits (ASIC) for signal processing, storage, signal conditioning, and transmission.") |

| | Example in published version 2020/0028000 A1, of indirect parent Ser. No. 16,528,958 filed 08/01/2019, now patent 11,121,271 |
|---|---|
| 9. The integrated, single-chip structure of claim 1, in which said holes are configured as intersecting elongated trenches. | FIG. 30A. Para. [0410] ("In this case, the microstructure 'holes' are 'connected' to form trenches 3060").<br>  <br>FIG. 30A<br>**[0410]** FIGS. **30**A-B are simplified partial schematic top views of a semiconductor surface having holes configured as trenches, according to some embodiments. The semiconductor **3010** and **3008** can be: Si, Ge, GeSi and/or III-V material such as InP, GaAs, GaN to name a few. In this case the microstructure "holes" are "connected" to form trenches **3060** and **3062**. The microstructure hole/trenches **3060** and **3062** are further configured to crisscross the surface of the semiconductors **3010** and **3008**, respectively. Although the trench-shaped holes in FIGS. **30**A-B are shown in straight lines, they could alternatively be formed in curved lines or a combination of straight and curved lines. The width of each trench is approximately one wavelength, and in some cases can be less than a wavelength, and in some cases can be more than a wavelength, and in some cases can have width ranging from 600 nm to 1600 nm, and can run the length of the photosensitive area. The depth of the trench can range from 100 nm to 1000 nm or more, and in some cases 50 nm to 300 nm. The spacing of the trench can range from 100 nm to 1000 nm or more, and in some cases 100 nm-600 nm. |
| | |

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| 10. The integrated, single-chip structure of claim 9, in which said elongated trenches have widths no greater than a wavelength of said light at said surface. | FIG. 30A. Para [0410] ("The width of each trench is approximately one wavelength, and in come cases can be less than a wavelength . . .."). . |
| | |
| 11. The integrated, single-chip structure of claim 9, in which said elongated trenches run the length of photosensitive areas of said pillars. | FIG. 30A. Para [0410] (". . . and can run the length of the photosensitive area.") |
| | |
| 12. The integrated, single-chip structure of claim 9, in which said elongated trenches intersect at right angles. | FIG. 30A illustrates right angles while FIG. 30B illustrates oblique angles. |

| Electronic Acknowledgement Receipt | |
|---|---|
| **EFS ID:** | 48779629 |
| **Application Number:** | 18385213 |
| **International Application Number:** | |
| **Confirmation Number:** | 7381 |
| **Title of Invention:** | APPARATUS AND METHOD TO FACILITATE INTRODUCTION OF A CERVICAL BALLOON CATHETER |
| **First Named Inventor/Applicant Name:** | SHIH-PING Wang |
| **Customer Number:** | 139982 |
| **Filer:** | Ivan Kavrukov/Mary Ellen Finnegan |
| **Filer Authorized By:** | Ivan Kavrukov |
| **Attorney Docket Number:** | 309-0015USCIP |
| **Receipt Date:** | 30-OCT-2023 |
| **Filing Date:** | |
| **Time Stamp:** | 17:57:59 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| Submitted with Payment | no |
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## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | Miscellaneous Incoming Letter | 309-0015USCIP_TableOfClaims 1-12_WithExamplesOfSupport.pdf | 1066471<br>6090f498fd7aada2985411163454daeab8c2fd62 | no | 6 |
| **Warnings:** | | | | | |

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**National Stage of an International Application under 35 U.S.C. 371**
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**New International Application Filed with the USPTO as a Receiving Office**
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| Electronic Acknowledgement Receipt | |
|---|---|
| **EFS ID:** | 48779536 |
| **Application Number:** | 18385213 |
| **International Application Number:** | |
| **Confirmation Number:** | 7381 |
| **Title of Invention:** | APPARATUS AND METHOD TO FACILITATE INTRODUCTION OF A CERVICAL BALLOON CATHETER |
| **First Named Inventor/Applicant Name:** | SHIH-PING Wang |
| **Customer Number:** | 139982 |
| **Filer:** | Ivan Kavrukov/Mary Ellen Finnegan |
| **Filer Authorized By:** | Ivan Kavrukov |
| **Attorney Docket Number:** | 309-0015USCIP |
| **Receipt Date:** | 30-OCT-2023 |
| **Filing Date:** | |
| **Time Stamp:** | 17:40:12 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| Submitted with Payment | no |
|---|---|

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | Preliminary Amendment | 309-0015USCIP_PreliminaryAmendment-Signed.pdf | 533345<br>0c781a6f45b48a7ebbc375670b6530478eb497bb | no | 6 |
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**New Applications Under 35 U.S.C. 111**

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**National Stage of an International Application under 35 U.S.C. 371**

**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

| | |
|---|---|
| First Named Inventor: | Shih-Yuan WANG et al. |
| Serial No.: | 18/385,213 |
| Examiner: | TBD |
| Group Art Unit: | TBD |
| Filing Date: | October 30, 2023 |
| For: | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES |

Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, New York 10001

**CERTIFICATE OF ELECTRONIC FILING**

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I hereby certify that this correspondence is being transmitted via Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

**PRELIMINARY AMENDMENT**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Claims begins on Page 2.

Remarks begin on page 5.

Attached for the Examiner's convenience is a table relating claim element to examples of support.

**Amendment to Claims:**

This listing of claims will replace all prior versions and listings of the claims.

1. (previously presented) An integrated, single-chip structure of plural pillars of semiconductor material formed as respective photodetectors configured to generate electrical signals in response to illumination with light including light in the infrared and/or near infrared spectrum, said structure comprising:

deliberately formed holes into said pillars, filled at least partly with solid dielectric material;

wherein:

parts of at least two of the holes overlap such that at a surface of each of said pillars each of the at least to holes has a portion that overlaps with another of said at least two holes and a portion that does not;

said at least two holes that overlap thereby form a depression in said surface that comprises a portion of only one of said two or more holes and a portion at which two of said two or more holes overlap, and

said two or more holes have:

depths in the range of 100-10000 nm from said surface, and

widths in the range of 100-2000 or 100-5000 nm along said surface in at least one direction;

side-isolation comprising solid material at sides of said pillars; and

a base dielectric region under the pillars that comprises solid dielectric material;

wherein said pillars are configured to receive said light directly or through other materials; and

wherein the presence of said holes and side-isolation increases effective quantum efficiency (EQE) of the pillars to illumination with said light relative to an otherwise same pillars lacking said holes.

2. (previously presented) The integrated, single-chip structure of claim 1, wherein said at least two holes comprise at least three holes each of which has a portion that overlaps with another of said at least three holes and a portion that does not.

3. (previously presented) The integrated, single-chip structure of claim 1, in which said pillars comprise semiconductor material that is doped at one portion of the pillar but is less doped or is undoped at a portion of the pillar adjacent the doped portion.

4. (previously presented) The integrated, single-chip structure of claim 3, in which the pillars are elongated in an up-down direction and the more doped portion of each pillar is over the less doped or undoped portion thereof.

5. (previously presented) The integrated, single-chip structure of claim 1, further including electrical contacts to said pillars configured to provide an electrical field across said pillars.

6. (previously presented) The integrated, single-chip structure of claim 5, in which two or more of said pillars share one of said electrical contacts.

7. (previously presented) The integrated, single-chip structure of claim 1, further including active electronic circuits integrated with said pillars.

8. (previously presented) The integrated, single-chip structure of claim 7, in which said active electronic circuits comprises Si-based active circuits for signal processing of electrical signals generated by said pillars.

9. (previously presented) The integrated, single-chip structure of claim 9, in which said holes are configured as intersecting elongated trenches.

10. (previously presented) The integrated, single-chip structure of claim 9, in which said elongated trenches have widths no greater than a wavelength of said light at said surface.

11. (previously presented) The integrated, single-chip structure of claim 9, in which said elongated trenches run the length of photosensitive areas of said pillars.

12. (previously presented) The integrated, single-chip structure of claim 9, in which said elongated trenches intersect at right angles.

**REMARKS**

This patent application is a continuation in-part of and incorporates by reference immediate parent applications Ser. Nos. 18/113,474 (pending) and 17/974,325 (allowed on September 29, 2023).

In addition to disclosure that is substantially the same as said immediate parent Ser. No. 18/113, 474 and the ultimate U.S. parent 14/947,718, the subject application includes a copy of FIGs. 30A and 30B and related text of intermediate parent 16/528,958 filed August 1, 2019 (now Pat. 11,121,271). (These FIGs. 30A and 30B are renumbered as 57A-B in the subject application; the related paragraphs 206 and 410 of the immediate parent (as filed) are now paragraphs [0087] and [0270]\, respectively, in the subject application; and a prime –'-- is added to each reference numeral in FIGs. 57A-B and in the related text in the subject application.)

Applicant submits that through a chain of parents claims 1-8 in the paper are entitled to the filing date of ultimate parent US application 14/947,718 filed November 20, 2015 (now U.S. Pat. 10,622,498) and provisionals to which it claims priority through a parent (including 61/834,873 filed June 13, 2013), and claims 9-12 are entitled to the filing date of indirect parent 16/528,958 filed August 1, 2019 (now U.S. Pat. 11,121,271) and provisionals to which it claim priority (including 62/750,016 filed October 24, 2018).

This patent application incorporates by reference and claims priority to each of the US, International, and Provisional applications in the chains of parents and siblings of said immediate parent applications, as identified in the concurrently filed ADS.

Attached to this Preliminary Amendment, for the Examiner's convenience, is a version of the claims with indicated examples of support for claims 1-8 in the published version of ultimate U.S. parent application 14/947,718 filed November 20, 2015 (and provisionals including 61/834,873) and for claims 9-12 in indirect parent application 16/528,958 filed August 1, 2019 (and provisionals including 62/750,016 filed October 24, 2018).

Applicant invites the Examiner to telephone the undersigned if it appears that a call may help advance prosecution.

Please charge any shortfall and credit any overpayments to our Deposit Account number 600125.

Respectfully Submitted,

WISSING MILLER LLP
Attorney for Applicants
By: /Ivan S. Kavrukov/
Ivan S. Kavrukov
Reg. No. 25,161
Tel.: (917) 945-0121

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
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| | |
|---|---|
| Application Number | TBD |
| Filing Date | TBD |
| First Named Inventor | Shih-Yuan WANG |
| Title | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES |
| Art Unit | N/A |
| Examiner Name | N/A |
| Attorney Docket Number | 309-0015USCIP |

**SIGNATURE of Applicant or Patent Practitioner**

| | | | |
|---|---|---|---|
| Signature | /Ivan S. Kavrukov/ | Date (Optional) | |
| Name | Ivan S. Kavrukov | Registration Number | 25,161 |
| Title (if Applicant is a juristic entity) | | | |
| Applicant Name (if Applicant is a juristic entity) | | | |

**NOTE:** This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ *Total of _____ forms are submitted.

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PTO/AIA/82B (07-13)
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# POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

| Application Number | Filing Date |
|---|---|
| | |

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 139982

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

**Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:**

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

| | | | | | |
|---|---|---|---|---|---|
| ☐ Firm or Individual Name | | | | | |
| Address | | | | | |
| City | | State | | Zip | |
| Country | | | | | |
| Telephone | | Email | | | |

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

W&WSens Devices, Inc.

☐ Inventor or Joint Inventor (title not required below)
☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

**SIGNATURE of Applicant for Patent**

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

| | | | |
|---|---|---|---|
| Signature | [signature] | Date (Optional) | Oct. 20, 2020 |
| Name | SHANPING WANG | | |
| Title | PRESIDENT CEO | | |

**NOTE:** Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

Doc code: PET.OP.AGE
Description: Petition to make special based on age/health

PTO/SB/130 (01-19)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number

## PETITION TO MAKE SPECIAL BASED ON AGE FOR ADVANCEMENT OF EXAMINATION UNDER 37 CFR 1.102(c)(1)

### Application Information

| | | | | | |
|---|---|---|---|---|---|
| Application Number | TBD | Confirmation Number | n/a | Filing Date | TBD |
| Attorney Docket Number (optional) | 309-0015USCIP | Art Unit | n/a | Examiner | n/a |
| First Named Inventor | Shih-Yuan WANG | | | | |
| Title of Invention | MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES | | | | |

**Attention: Office of Petitions**

An application may be made special for advancement of examination upon filing of a petition showing that the applicant is 65 years of age, or more. No fee is required with such a petition. See 37 CFR 1.102(c)(1) and MPEP 708.02 (II).

APPLICANT HEREBY PETITIONS TO MAKE SPECIAL FOR ADVANCEMENT OF EXAMINATION IN THIS APPLICATION UNDER 37 CFR 1.102(c)(1) and MPEP 708.02 (II) ON THE BASIS OF THE APPLICANT'S AGE.

A grantable petition requires one of the following items:

(1) Statement by one named inventor in the application that he/she is 65 years of age, or more; or

(2) Certification by a registered attorney/agent having evidence such as a birth certificate, passport, driver's license, etc. showing one named inventor in the application is 65 years of age, or more.

**Name of inventor who is 65 years of age, or older**

| Given Name | Middle Name | Family Name | Suffix |
|---|---|---|---|
| Shih-Ping | | WANG | |

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 11.18. Please see 37 CFR 1.4(d) for the format of the signature.

Select (1) or (2):

☐ (1) I am an inventor in this application and I am 65 years of age, or more.

☒ (2) I am an attorney or agent registered to practice before the Patent and Trademark Office, and I certify that I am in possession of evidence, and will retain such in the application file record, showing that the inventor listed above is 65 years of age, or more.

| | | | |
|---|---|---|---|
| Signature | /Ivan S. Kavrukov/ | Date (YYYY-MM-DD) | 2023-10-30 |
| Name | Ivan S. Kavrukov | Registration Number | 25,161 |

This collection of information is required by 37 CFR 1.102(c)(1). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) a petition to make special based on age for advancement of examination. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETED FORMS TO THE CHIEF INFORMATION OFFICER. **Submit completed forms electronically over EFS-Web, or mail to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

## Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

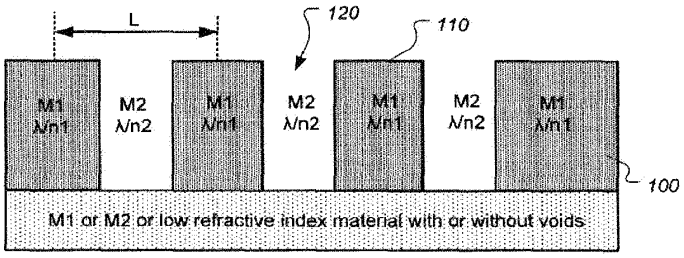



FIG. 1

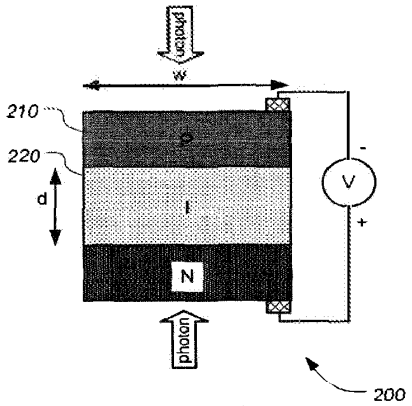



FIG. 2
(prior art)

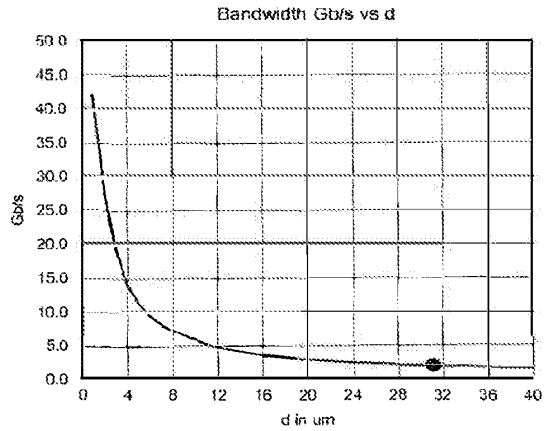



FIG. 3A
(prior art)

310

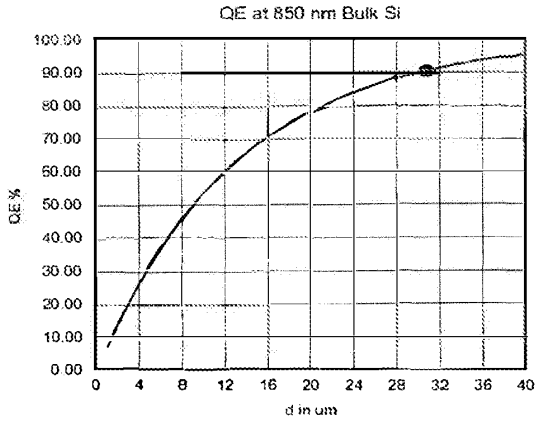



FIG. 3B
(prior art)

312

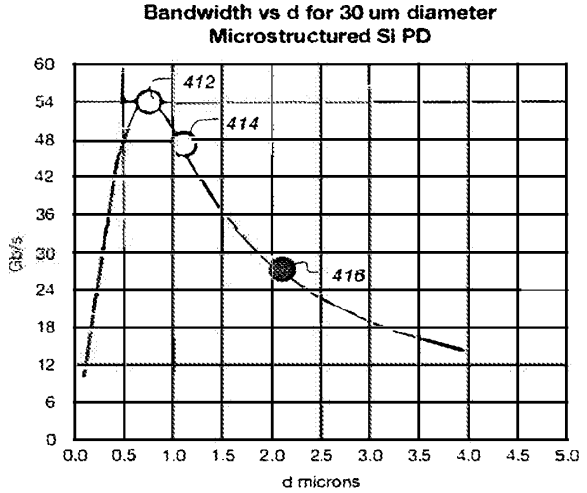



FIG. 4A

410

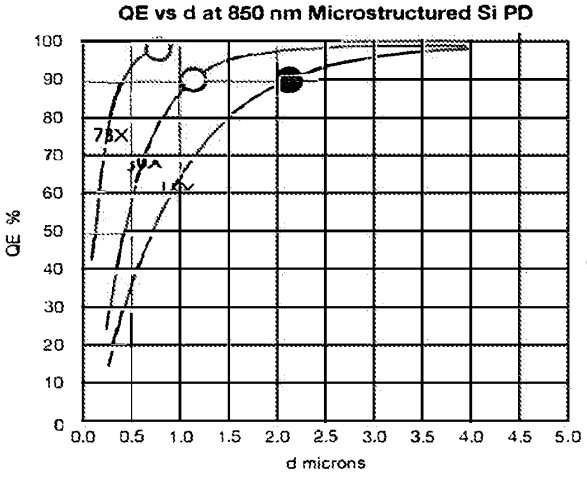



FIG. 4B

420

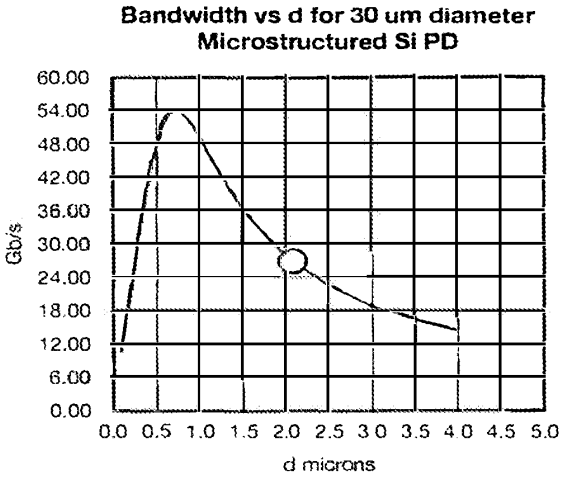



FIG. 4C

430

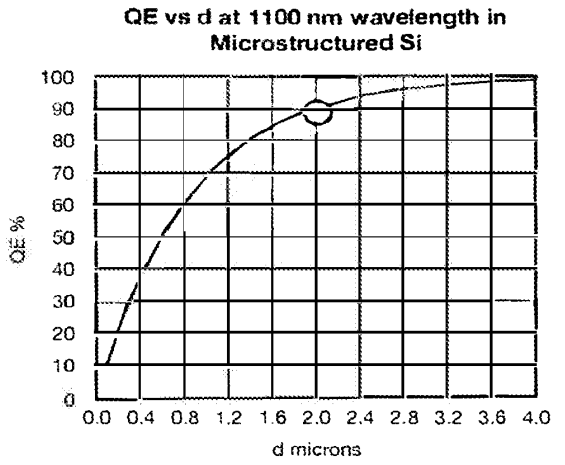



FIG. 4D

440

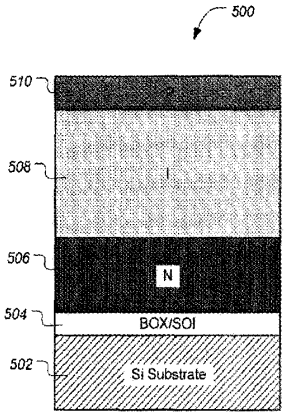



FIG. 5A

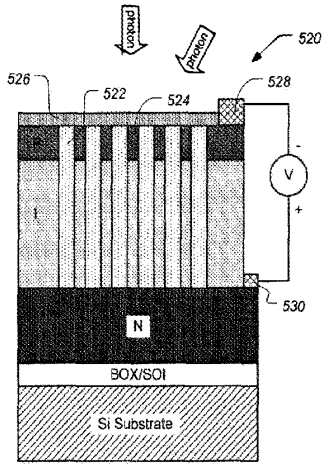



FIG. 5B

5448

309-00151USC1P

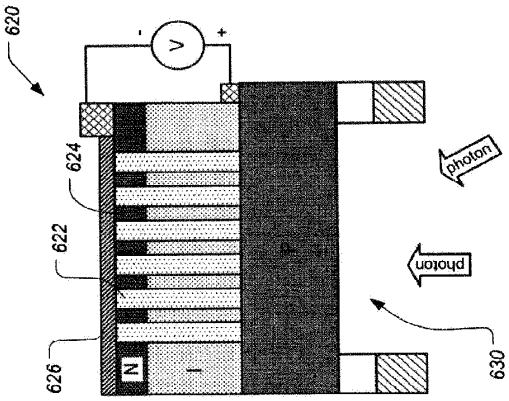

620
-
+
624
622
626
N
I
P
photon
photon
630

FIG. 6B

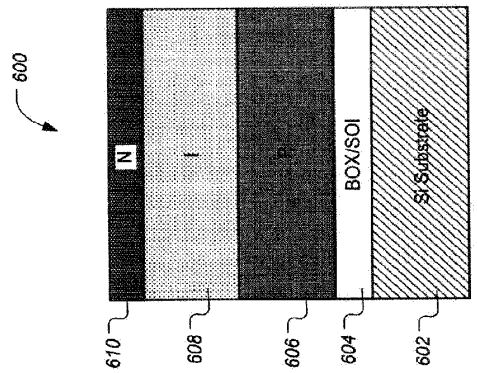

600
N
I
P
BOX/SOI
Si Substrate
610
608
606
604
602

FIG. 6A

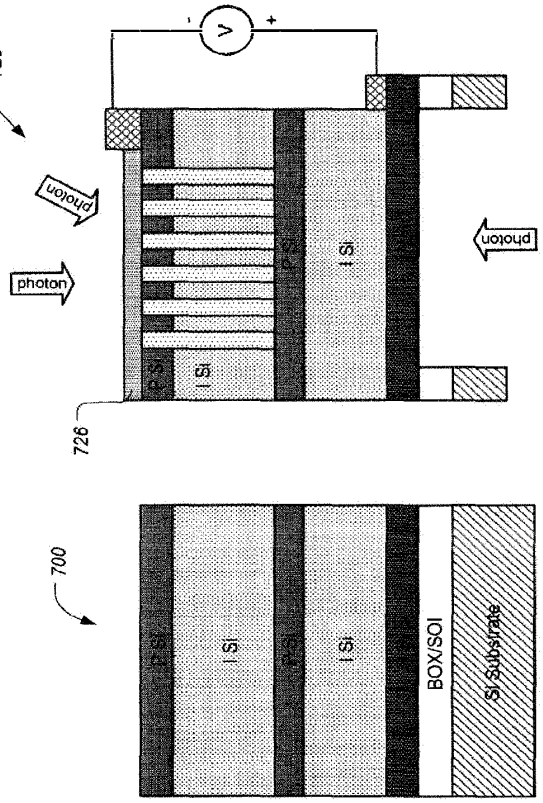

720
V
-
+
photon
photon
photon
P Si
I Si
P Si
I Si
726

FIG. 7B


700
P Si
I Si
P Si
I Si
BOX/SOI
Si Substrate

FIG. 7A

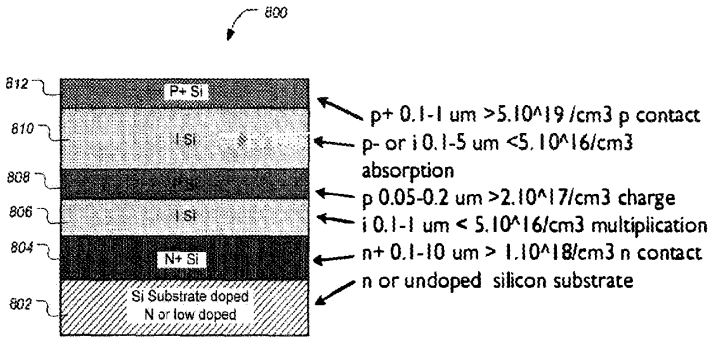



FIG. 8



369-0515USCIP

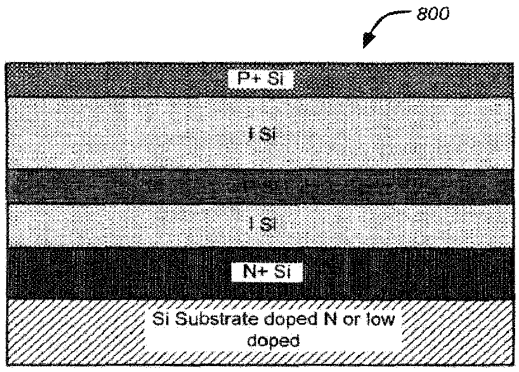

800
P+ Si
I Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9A

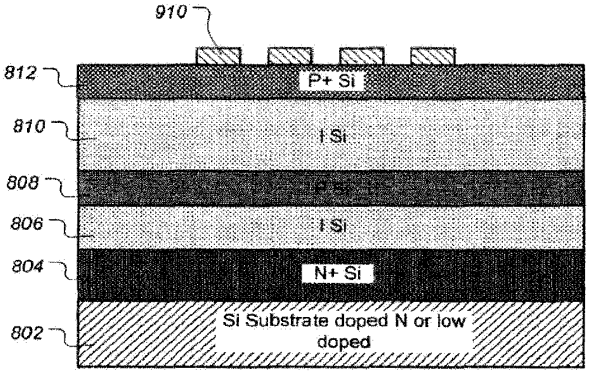

910
812
810
808
806
804
802
P+ Si
I Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9B

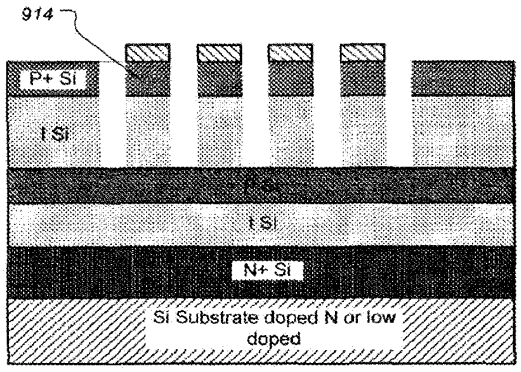

914
P+ Si
I Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9C

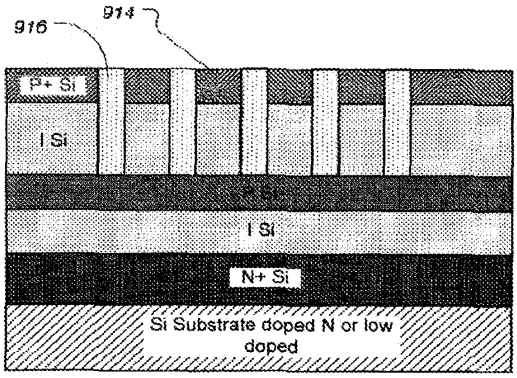

916
914
P+ Si
I Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9D

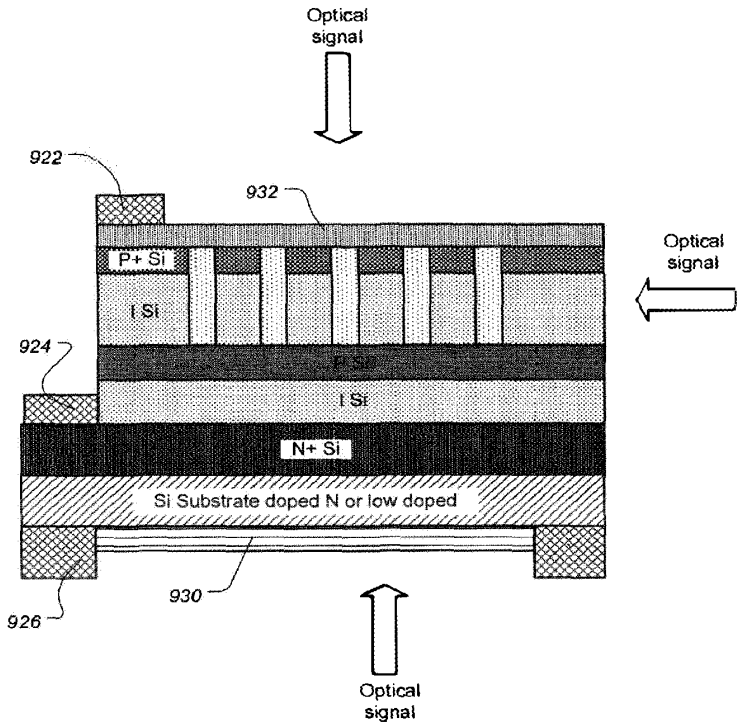

Optical signal
922
932
P+ Si
I Si
Optical signal
924
P+ Si
I Si
N+ Si
Si Substrate doped N or low doped
930
926
Optical signal

FIG. 9E

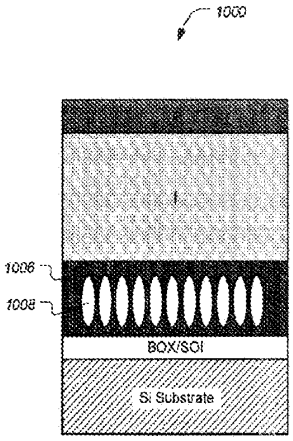



FIG. 10A

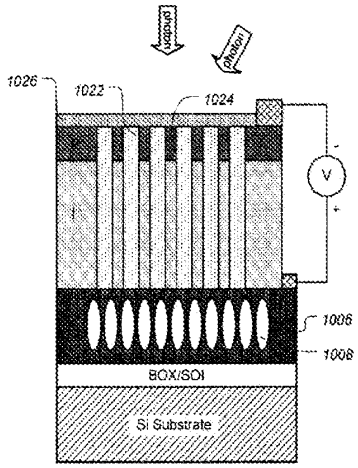



FIG. 10B

32448
309-0015USCIP

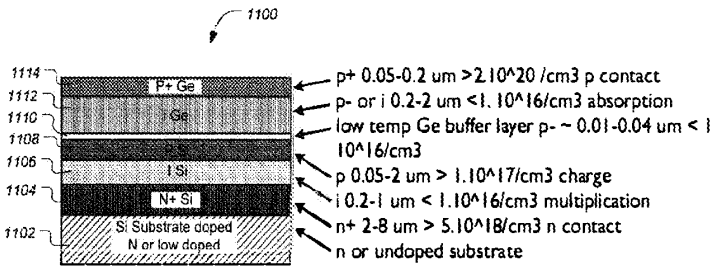

1100
1114
1112
1110
1108
1106
1104
1102
P+ Ge
Ge
I Si
N+ Si
Si Substrate doped
N or low doped
p+ 0.05-0.2 um >2.10^20 /cm3 p contact
p- or i 0.2-2 um <1. 10^16/cm3 absorption
low temp Ge buffer layer p- ~ 0.01-0.04 um < 1
10^16/cm3
p 0.05-2 um > 1.10^17/cm3 charge
i 0.2-1 um < 1.10^16/cm3 multiplication
n+ 2-8 um > 5.10^18/cm3 n contact
n or undoped substrate

FIG. 11A

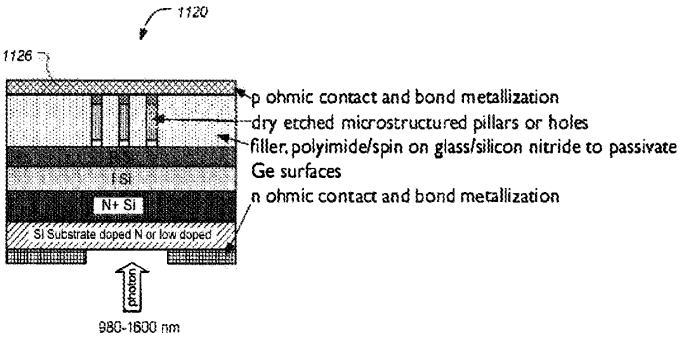

1120
1126
p ohmic contact and bond metallization
dry etched microstructured pillars or holes
filler, polyimide/spin on glass/silicon nitride to passivate
Ge surfaces
n ohmic contact and bond metallization
I Si
N+ Si
SI Substrate doped N or low doped
photon
980-1600 nm

FIG. 11B

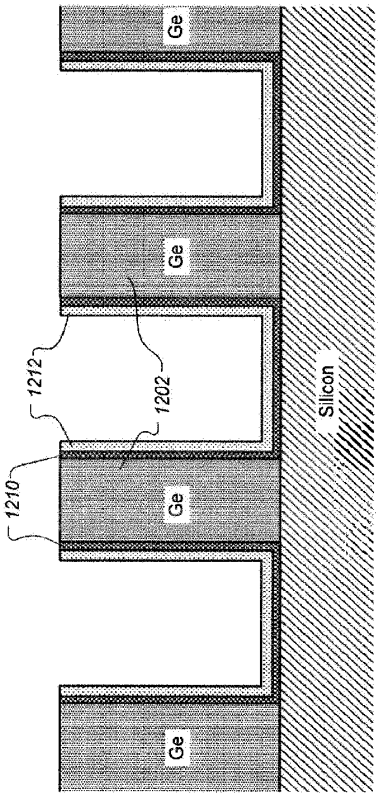



FIG. 12

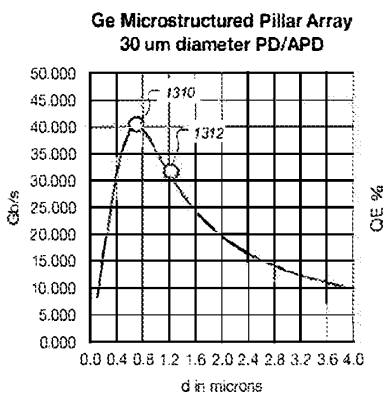



FIG. 13A

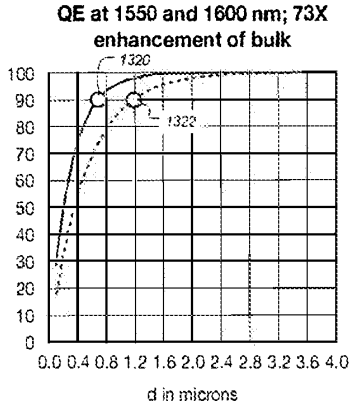



FIG. 13B

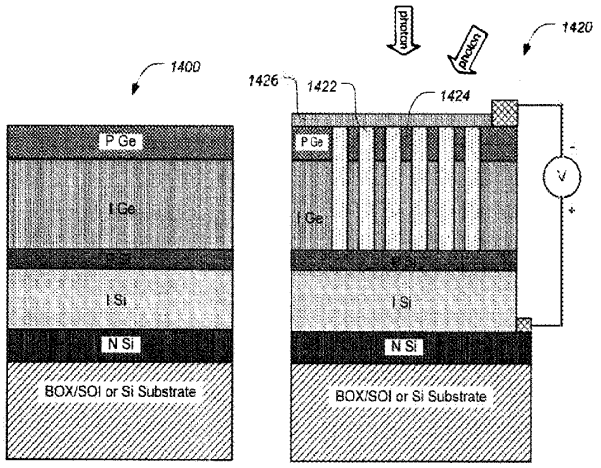



FIG. 14A FIG. 14B

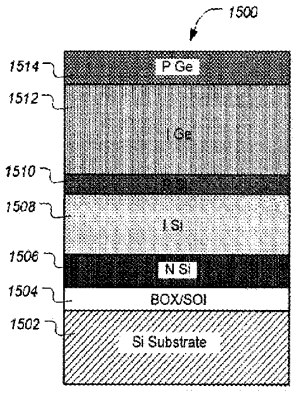



FIG. 15A

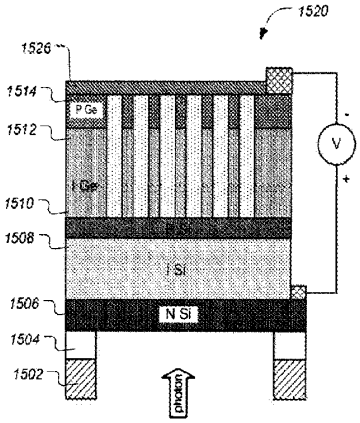



FIG. 15B

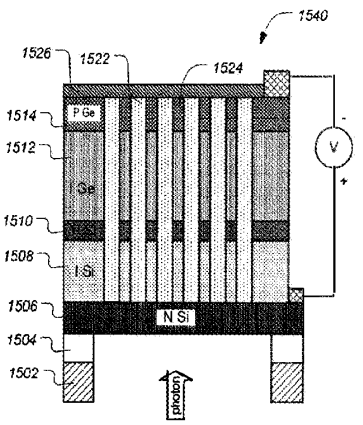



FIG. 15C

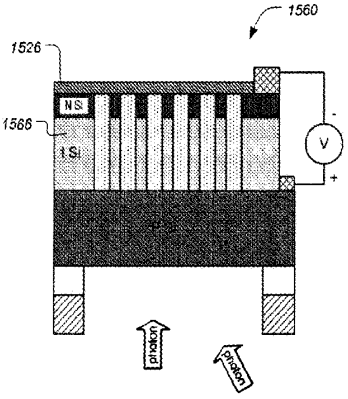



FIG. 15D

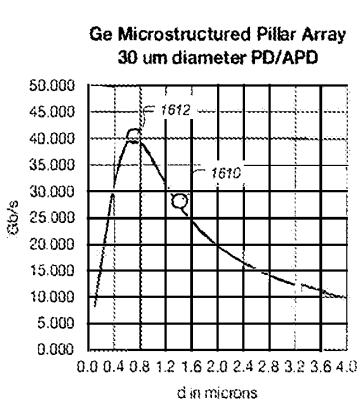



FIG. 16A

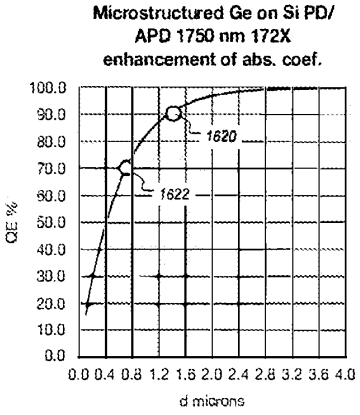



FIG. 16B

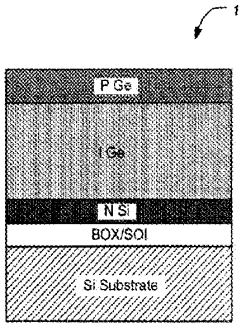



FIG. 17A

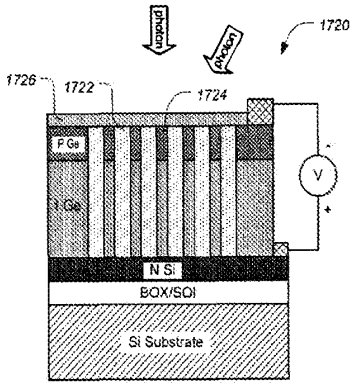



FIG. 17B

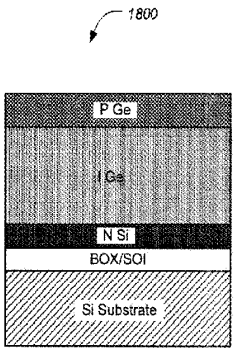



FIG. 18A

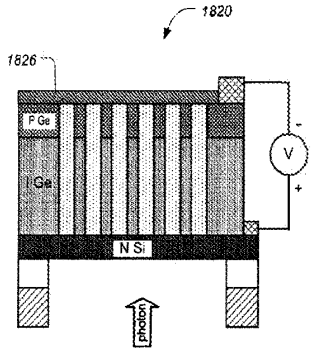



FIG. 18B

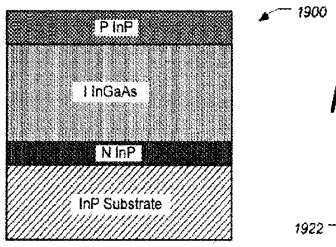



FIG. 19A

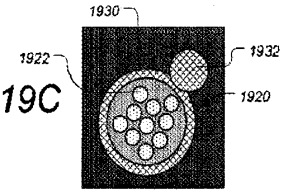



FIG. 19C

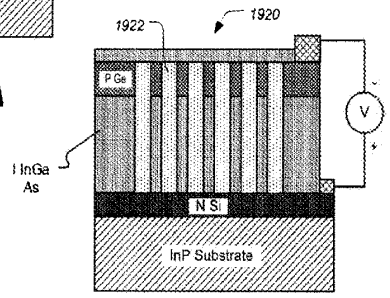



FIG. 19B

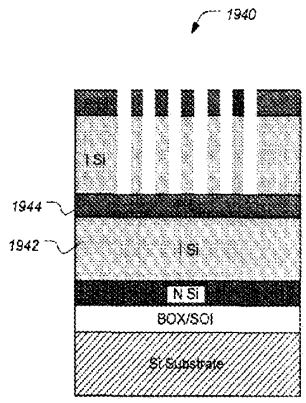



FIG. 19D

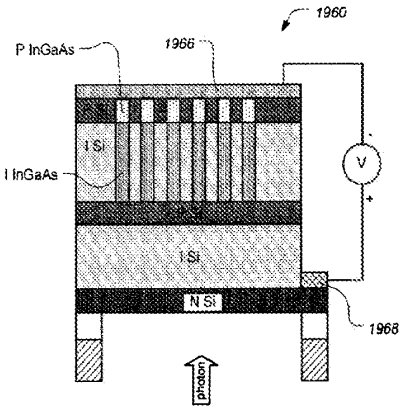



FIG. 19E

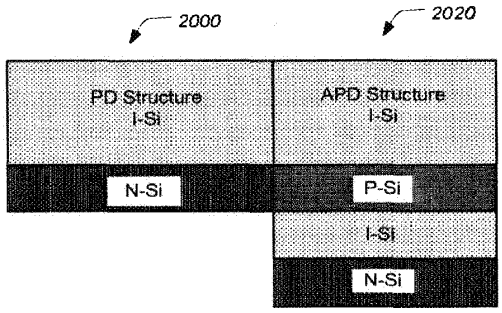

2000
2020
PD Structure
I-Si
APD Structure
I-Si
N-Si
P-Si
I-Si
N-Si

FIG. 20

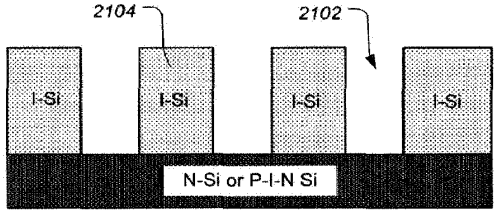

2104
2102
I-Si
I-Si
I-Si
I-Si
N-Si or P-I-N Si

FIG. 21

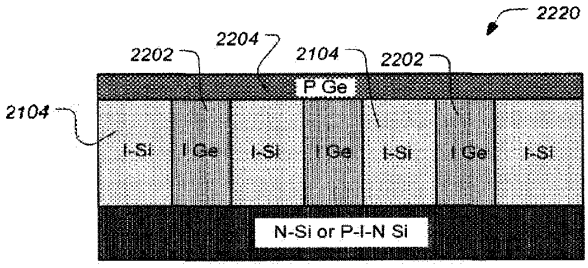

2220
2202
2204
2104
2202
2104
P Ge
I-Si
I Ge
I-Si
I Ge
I-Si
I Ge
I-Si
N-Si or P-I-N Si

FIG. 22

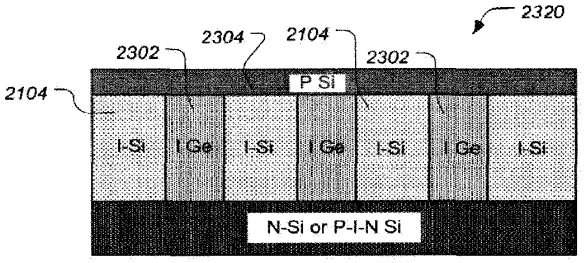

2320
2302
2304
2104
2302
2104
P Si
I-Si
I Ge
I-Si
I Ge
I-Si
I Ge
I-Si
N-Si or P-I-N Si

FIG. 23

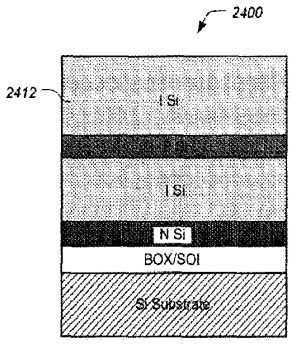



FIG. 24A

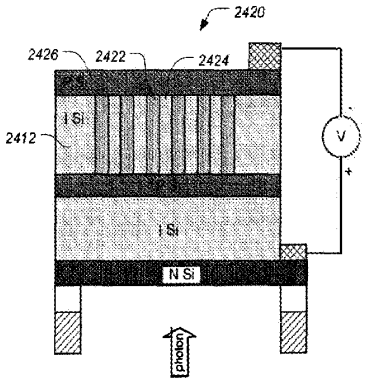



FIG. 24B

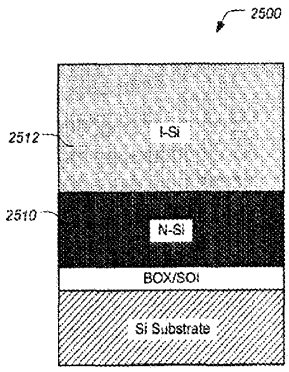



FIG. 25A

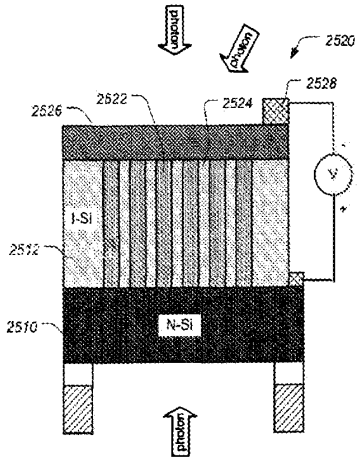



FIG. 25B

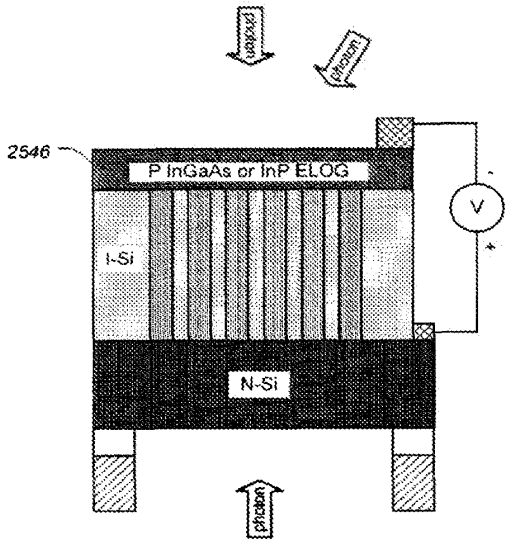



FIG. 25C

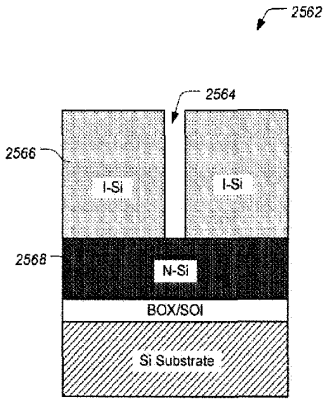



FIG. 25D

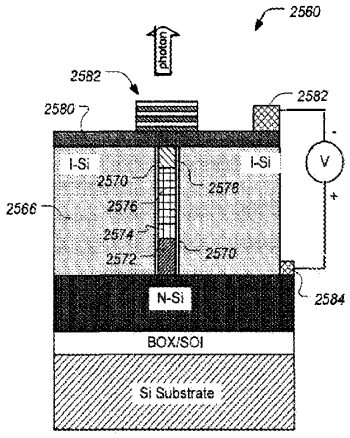



FIG. 25E

30748
309-0015USCIP

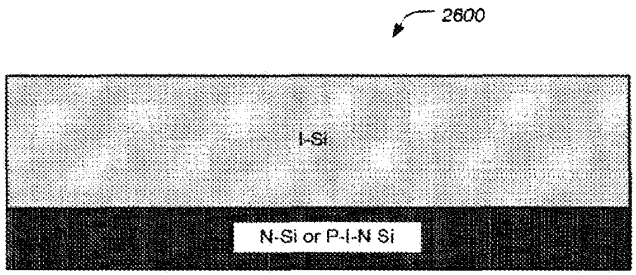



FIG. 26

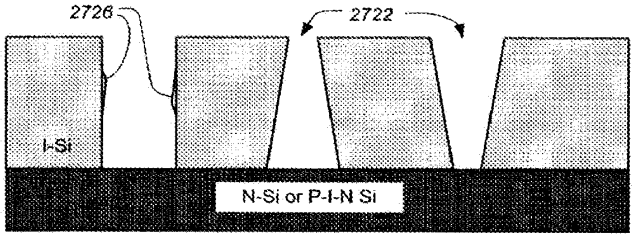



FIG. 27

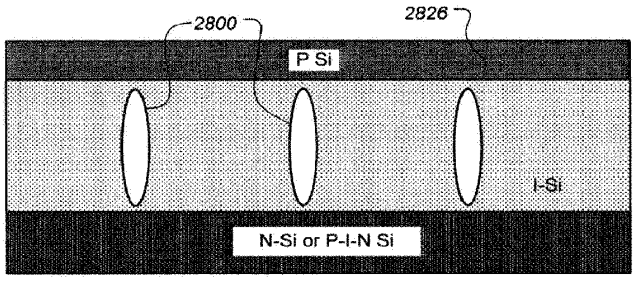

2800
2826
P Si
I-Si
N-Si or P-I-N Si

FIG. 28

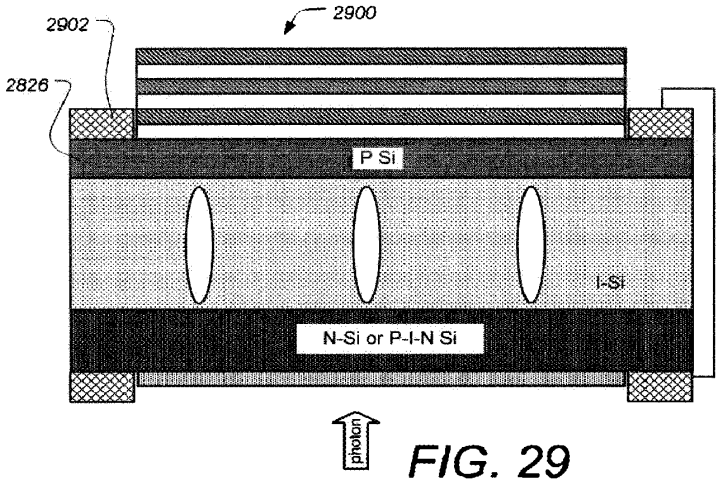

2902
2900
2826
P Si
I-Si
N-Si or P-I-N Si
photon

FIG. 29

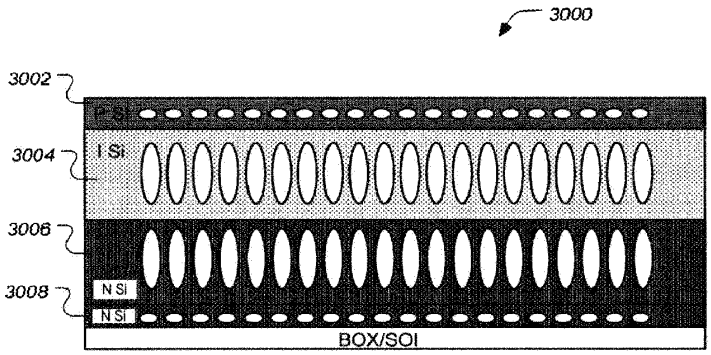

3000
3002
P Si
3004
I Si
3006
3008
N Si
N Si
BOX/SOI

FIG. 30

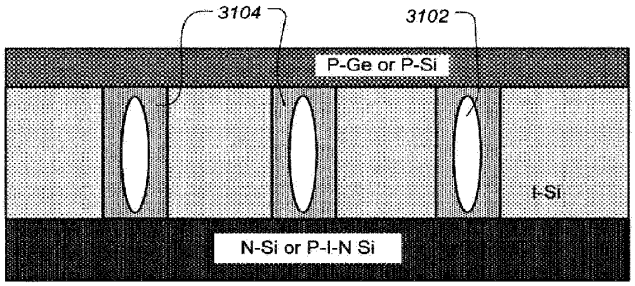

3104
3102
P-Ge or P-Si
I-Si
N-Si or P-I-N Si

FIG. 31

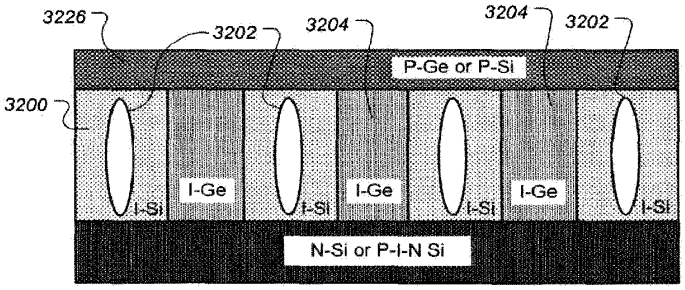

3226
3202
3204
3204
3202
P-Ge or P-Si
3200
I-Si
I-Ge
I-Si
I-Ge
I-Si
I-Ge
I-Si
N-Si or P-I-N Si

FIG. 32

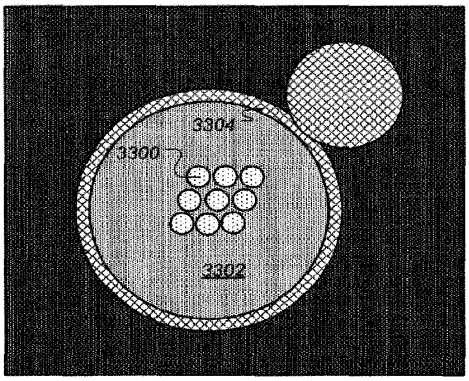

3304
3300
3302

FIG. 33

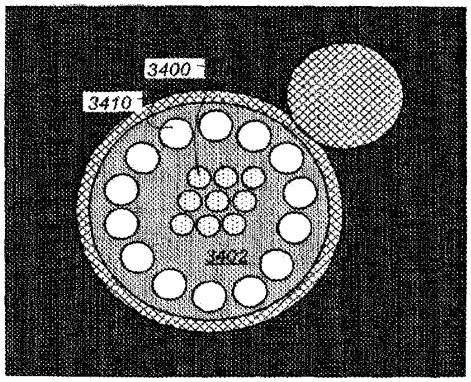



FIG. 34

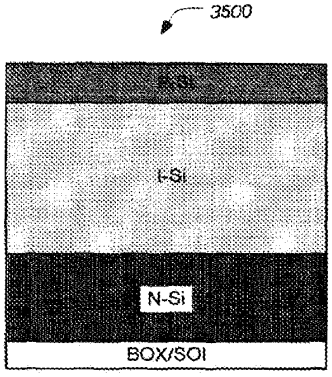



FIG. 35
(prior art)

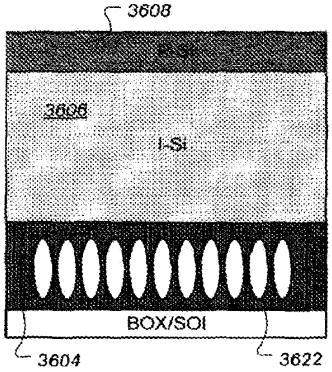



FIG. 36

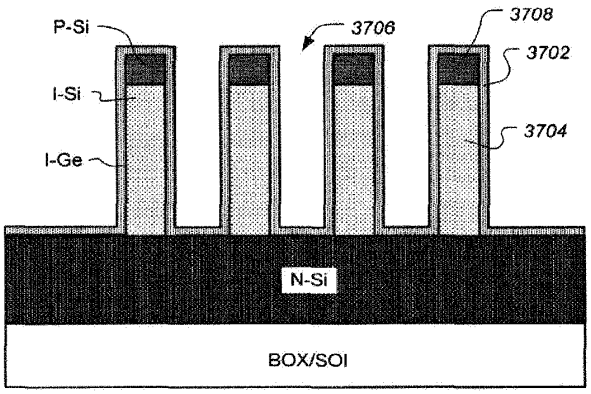

P-Si
3706
3708
3702
I-Si
3704
I-Ge
N-Si
BOX/SOI

FIG. 37

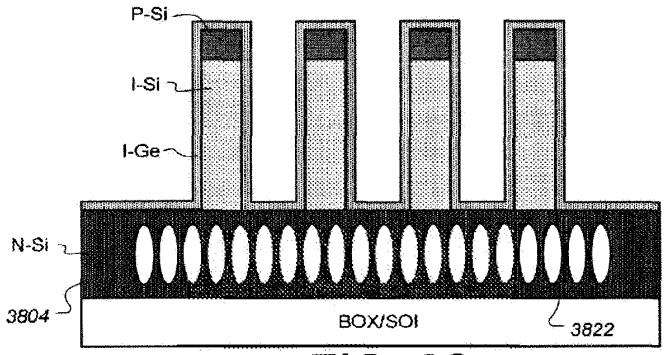

P-Si
I-Si
I-Ge
N-Si
3804
BOX/SOI
3822

FIG. 38