

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS
AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG
AUSTIN SEMICONDUCTOR LLC.,

Petitioner,

v.

W&WSENS DEVICES INC.,

Patent Owner.

Case IPR2025-00993
Patent No. 12,087,871

PETITION FOR *INTER PARTES* REVIEW

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PETITIONER’S EXHIBIT LIST

Exhibit	Description
Ex-1001	U.S. Patent No. 12,087,871 B2 to Wang (“’871 Patent”)
Ex-1002	Declaration of Michael Lebby, Ph.D. (“Lebby”)
Ex-1003	Prosecution History of the ’871 Patent (downloaded from Public PAIR)
Ex-1004	U.S. Patent Application Publication No. 2012/0049044 A1 to Kuboi (“ <i>Kuboi</i> ”)
Ex-1005	U.S. Patent Application Publication No. 2012/0033119 A1 to Shinohara (“ <i>Shinohara</i> ”)
Ex-1006	European Patent Application EP 2 172 974 A1 to NXP B.V. (“ <i>NXP</i> ”)
Ex-1007	U.S. Patent Application Publication No. 2008/0259981 A1 to Wang et al. (“ <i>Wang</i> ”)
Ex-1008 to Ex-1009	Reserved
Ex-1010	Zhihong Huang et al., <i>Microstructured silicon photodetector</i> , Applied Physics Letter, Vol. 89 (2006), pp. 033506-1 to -3.
Ex-1011	Richard A. Myers et al., <i>Enhancing near-infrared avalanche photodiode performance by femtosecond laser microstructuring</i> , Applied Optics, Vol. 45, No. 35 (Dec. 2006), pp. 8825-31.
Ex-1012	Abbas El Gamal et al., <i>CMOS Image Sensors</i> , IEEE Circuits & Devices Magazine (2005), pp. 6-20.
Ex-1013	Eric R. Fossum, <i>CMOS Image Sensors: Electronic Camera-On-A-Chip</i> , IEEE Transactions on Electron Devices, Vol. 44, No. 10 (Oct. 1997), pp. 1689-98.
Ex-1014	Sunetra Mendis et al., <i>CMOS Active Pixel Image Sensor</i> , IEEE Transactions on Electron Devices, Vol. 41, No. 3 (Mar. 1994), pp. 452-53.
Ex-1015	Renato Turchetta et al., <i>Introduction to CMOS Image Sensors</i> , Molecular Expressions™ Optical Microscopy Primer: Digital Imaging in Optical Microscopy - Introduction to CMOS Image Sensors (July 16, 2004), pp. 1-9, <i>available at</i>

Exhibit	Description
	https://web.archive.org/web/20120508153832/https://micro.magnet.fsu.edu/primer/digitalimaging/cmosimagesensors.html
Ex-1016 to Ex-1019	Reserved
Ex-1020	John P. Uyemura, <i>CMOS Logic Circuit Design</i> (Kluwer Academic Publishers 2002), pp. 64, 74-102, 315-17, 458-60.
Ex-1021	Khalil Jumah Tawfiq Haram, Organic Solar Cells Based on High Dielectric Constant Materials: An Approach to Increase Efficiency (June 2013) (Ph.D. dissertation, Western Michigan University), pp. 1-122.
Ex-1022	P. Kalugasalam et al., <i>Dielectric and AC Conduction Studies of Lead Phthalocyanine Thin Film</i> , Chalcogenide Letters, Vol. 6, No. 9 (Sept. 2009), pp. 469-76.
Ex-1023 to Ex-1028	Reserved
Ex-1029	Jurgen Michel et al., <i>Advances in fully CMOS integrated photonic devices</i> , Proceedings of SPIE, Vol. 6477 (2007), pp. 64770P-1 to -11 (“Michel”).
Ex-1030	Mark Beals et al., <i>Process Flow Innovations for Photonic Device Integration in CMOS</i> , Proceedings of SPIE, Vol. 6898 (2008), pp. 689804-1 to -14 (“Beals”).
Ex-1031	Donald A. Neaman, <i>Semiconductor Physics and Devices – Basic Principles</i> (McGraw Hill 3d ed. 2003), pp. 247-50, 260-61.
Ex-1032 to Ex-1033	Reserved
Ex-1034	Matthew Saucedo, <i>Porphyrin Thin Film Dielectrics</i> , SUNFEST Technical Report TR-CST01NOV04, Center for Sensor Technologies, Univ. of Pennsylvania, Philadelphia, PA (2004), pp. 181-98.
Ex-1035	N. Venkatramaiah et al., <i>Spectroscopic and dielectric studies of meso-tetrakis(p-sulfonatophenyl) porphyrin doped hybrid borate glasses</i> , Journal of Alloys and Compounds, Vol. 509 (2011), pp. 2797-803.

Exhibit	Description
Ex-1036	Tom J. Savenije, <i>Photogeneration and transport of charge carriers in a porphyrin p/n heterojunction</i> , Physical Review B, Vol. 55, No. 15 (Apr. 1997), pp. 9685-92.
Ex-1037	Ümit Salan et al., <i>Synthesis, characterization, electrical and dielectric permittivity measurements of 2,9,16,23-tetra(4-ferrocenylimino-3-nitrophenoxy)phthalocyanines</i> , Journal of Porphyrins and Phthalocyanines, Vol. 10 (2006), pp. 1263-70.
Ex-1038	Teresa M. Figueira-Duarte et al., <i>Pyrene-Based Materials for Organic Electronics</i> , Chemical Reviews, Vol. 111 (2011), pp. 7260-314.
Ex-1039 to Ex-1049	Reserved
Ex-1050	U.S. Patent Application Publication No. 2012/0153124 A1 to Yu et al. (“ <i>Yu</i> ”)
Ex-1051	International Patent Publication No. WO 2011/085297 A1 to Han et al. (“ <i>Han</i> ”)
Ex-1052	Japanese Patent Publication No. JP 2007-129024A
Ex-1053	Certified English Language Translation of Japanese Patent Publication No. JP 2007-129024A to Hasegawa (“ <i>Hasegawa</i> ”)
Ex-1054 to Ex-1055	Reserved
Ex-1056	U.S. Patent No. 8,274,122 B2 to Shimotsusa
Ex-1057	U.S. Patent No. 8,378,339 B2 to Nomura et al.
Ex-1058	Reserved
Ex-1059	U.S. Patent Application Publication No. 2008/0157141 A1 to Han
Ex-1060	U.S. Patent No. 8,390,036 B2 to Goto
Ex-1061	H. H. Li, <i>Refractive Index of Silicon and Germanium and Its Wavelength and Temperature Derivatives</i> , J. Phys. Chem. Ref. Data, Vol. 9, No. 3 (1980), pp. 561-658.
Ex-1062	Rei Kitamura et al., <i>Optical constants of silica glass from extreme ultraviolet to far infrared at near room temperature</i> , Applied Optics, Vol. 46, No. 33 (November 20, 2007), pp. 8118-33.

Exhibit	Description
Ex-1063	S.M. Sze et al., <i>Semiconductor Devices Physics and Technology</i> (John Wiley & Sons, Inc. 3d ed. 2012), pp. 205-10, 325-30, 392-400, 416-17, 466-67.
Ex-1064	U.S. Patent Application Publication No. 2012/026286 A1 to Na et al.
Ex-1065	U.S. Patent Application Publication No. 2013/0094865 A1 to Pinguet et al.
Ex-1066 to Ex-1067	Reserved
Ex-1068	P.A. Lane et al., <i>Electroabsorption studies of phthalocynine/perylene solar cells</i> , Solar Energy Materials & Solar Cells, Vol. 63, (2000), pp. 3-13.
Ex-1069	Martin A. Green, <i>Self-consistent optical parameters of intrinsic silicon at 300K including temperature coefficients</i> , Solar Energy Materials & Solar Cells, Vol. 92, (2008), pp. 1305-10.
Ex-1070	Horst Zimmerman, <i>Integrated Silicon Optoelectronics</i> (Springer. 2d ed. 2010), pp. 1-6.
Ex-1071	M.M. El-Nahas et al., <i>Structural and optical properties of Ni (II) tetraphenyl porphyrin thin films</i> , Eur. Phys. J. Appl. Phys. (2012), Vol. 57, pp. 30201-p1 to 30201-p13.
Ex-1072	M.M. El-Nahas et al., <i>Structural and optical properties of thermally evaporated zinc phthalocyanine thin films</i> , Proc. 2 nd Saudi Sc. Conf. (March 2004), pp. 277-293.
Ex-1073	M.E. Azim-Araghi et al., <i>Electrical and optical properties of an organic semiconductor metal-free phthalocyanine (C₃₂H₁₈N₈)</i> , Eur. Phys. J. Appl. Phys. (2012), Vol. 58, pp. 30201-p1 to 30201-p6.
Ex-1074	Reserved
Ex-1075	<i>W&Wsens Devices Inc. v. Samsung Electronics Co. Ltd. et al.</i> , Case No. 2:24-cv-00854, Excerpts from Plaintiff's Infringement Contentions (Jan. 7, 2025)
Ex-1076	<i>Electrical Engineering Dictionary - CRCnetBase</i> (Phillip A. Laplante editor-in-chief, CRCPress LLC 2000).

I. Preliminary Statement

Petitioner Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor LLC (collectively, “Samsung”) requests *inter partes* review of U.S. Patent No. 12,087,871 (Ex-1001) and cancellation of claims 1-4, 6-8, and 10-18.

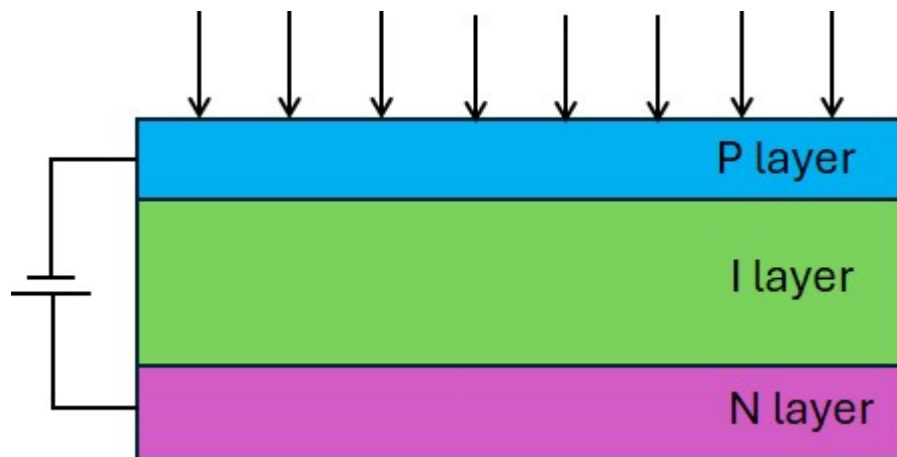
The challenged claims pertain to a photodetector that uses microstructures to enhance photon absorption in a semiconductor device, and recite specific microstructure dimensions that allegedly increase light absorption by 10% over a photodetector that does not include microstructures. Further, the challenged claims require that the image sensor and control circuitry are monolithically integrated on a single semiconductor substrate. These features, however, were all well known. For example, *Kuboi* and *Yu* disclose microstructured photodetectors with the claimed dimensions. And *Kuboi*, *Yu*, and *Shinohara* disclose monolithic integration.

As detailed below and in the supporting declaration of Dr. Michael Lebby (“Lebby”) (Ex-1002), the challenged claims are unpatentable based on the grounds presented. Lebby, ¶¶3-4, 98-100. The Board should institute review and cancel the challenged claims.

II. State of the Art

A. Photodetectors

A photodetector is a semiconductor device that transforms photons into electrical signals, enabling electrical circuits to detect and measure incident light. Leebby, ¶51. Various types of photodetectors exist, including photodiodes and avalanche photodiodes. A PiN photodetector is a specific type of photodiode characterized by an **intrinsic (undoped) layer** positioned between highly doped **P-type** and **N-type** semiconductor layers (hence “**PiN**”):



Id. When light enters the photodetector, the intrinsic layer absorbs photons, generating electron-hole pairs. Applying a negative bias across the photodetector causes the separated electrons to move towards the N-type layer and the holes towards the P-type layer, producing a measurable photocurrent. Leebby, ¶52.

B. Microstructure-Enhanced Photodetectors

Conventional silicon photodetectors exhibit high responsivity at wavelengths of light less than about 850 nm. Ex-1010, 1. The prior art recognized that tailoring silicon's microstructure extends photodetector operability to longer wavelengths. For instance, etching a silicon photodetector surface to create micron-sized pillars was known to enhance a photodetector's responsiveness at longer wavelengths. Ex-1010, 1-2; Ex-1011, 1-6; Lebbby, ¶53.

Photodetectors featuring microstructures enhanced by etched holes were widely known well before the purported invention date. For example, *NXP* (Ex-1006) discloses a single-chip device 1300 where a silicon **PiN** photodiode is integrated with CMOS signal processing circuitry (not shown below) on the same substrate 102.

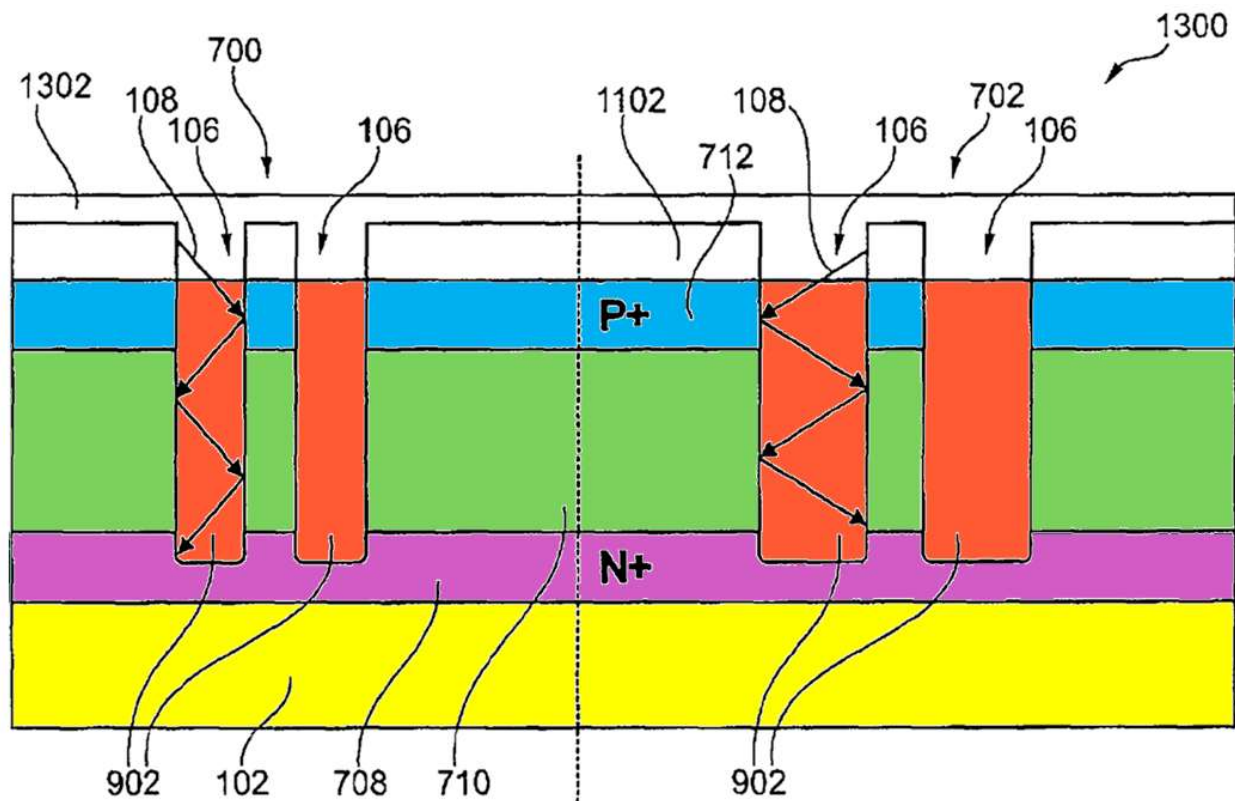


Fig. 13

NXP, Fig. 13, ¶¶[15], [32], [42], [85].¹ The **PiN** photodiode above includes an **intrinsic layer** 710 disposed between an **N⁺ layer** 708 and a **P⁺ layer** 712 and holes or **pores** 106 formed on the **PiN** layers by etching. *NXP*, ¶¶[77]-[78]. *NXP* discloses that **pores** 106 increase the photodiode's quantum efficiency. *NXP*, ¶¶[13], [38]; Lebby, ¶¶53-56.

¹ All color and colored annotations in figures have been added.

III. The '871 Patent

A. Specification

The '871 Patent's photodetector includes microstructures to enhance photoabsorption. '871 Patent, 2:41-42, 3:1-5, 4:1-8, 17:25-27. The photodetector includes a silicon **substrate** with a **first layer** (P^+ layer), a very low doped N or P layer called the **intermediate layer** (I layer), and a **second layer** (N^+ layer) with **holes** etched in one or more of the **PiN** layers. *Id.*, 15:57-59, 16:9-35, 17:47-52. The photodetector (illustrated below) operates in reverse bias mode with negative voltage on the anode (P^+ layer) and positive voltage on the cathode (N^+ layer). *Id.*, 16:40-43, 11:45-51.

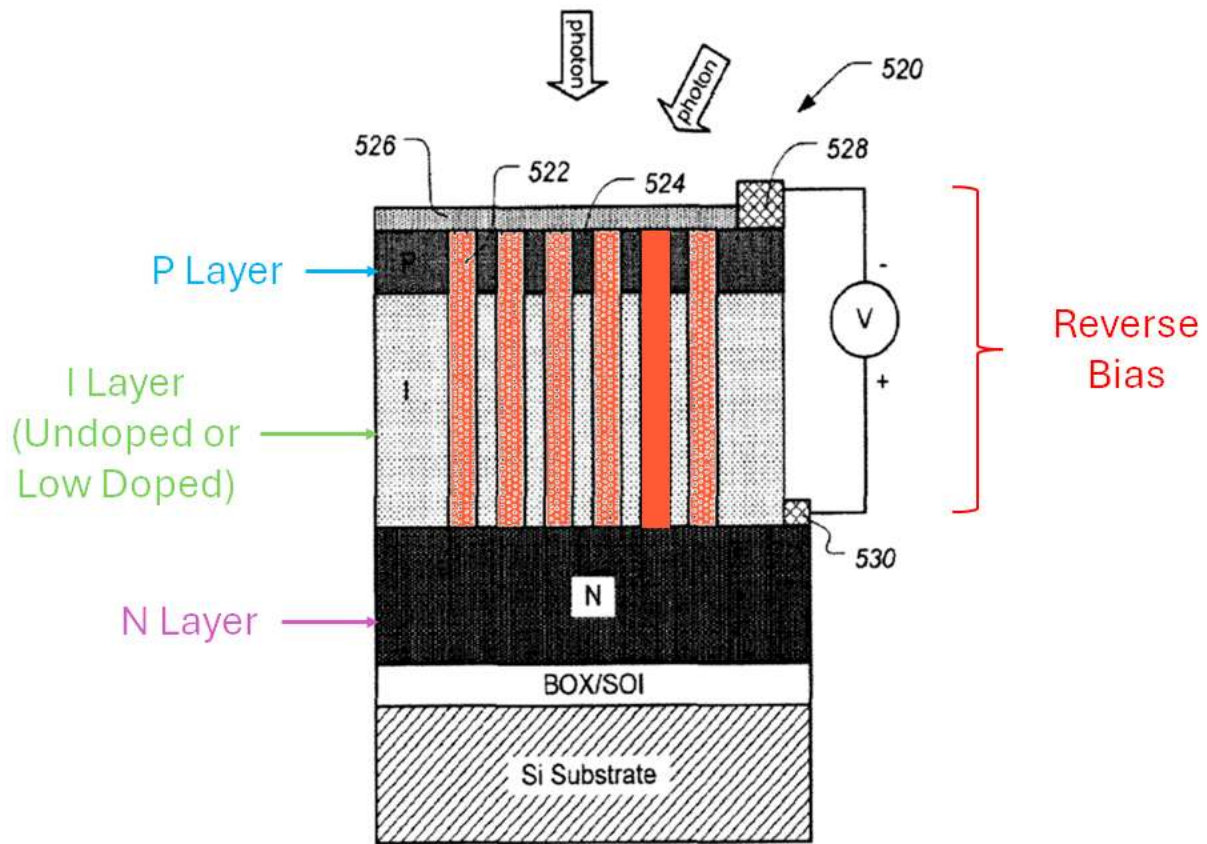


FIG. 5B

Id., Fig. 5B.

The '871 Patent discloses that one of the causes of enhancement of the absorption coefficient of the incident light includes high contrast grating (HCG) effects. *Id.*, 11:51-57. Because of the HCG effect, the microstructured pillar-hole-void array can have an enhanced absorption coefficient over the bulk absorption coefficient by a factor of 1.1 to over 100. *Id.*, 12:49-55. The photodetector can be integrated with ASIC (application specific integrated circuits) such as signal

processing, signal amplification, and other ICs for specific applications. *Id.*, 10:23-27; Lebbby, ¶¶66-69.

B. Claim Construction

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. §42.100(b). Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, no terms need construction to resolve the controversy.²

IV. Statement of Precise Relief Requested

A. Prior Art

The application that resulted in the '871 Patent was filed on October 30, 2023, claiming priority to multiple patent applications, the earliest of which was filed on May 22, 2013.³ Thus, the earliest claimed priority date is May 22, 2013.

- *Kuboi* (Ex-1004), U.S. Patent Publication No. 2012/0049044, which published on March 1, 2012, is prior art under 35 U.S.C. § 102(a)(1), (a)(2).

² Petitioner retains the right to contend in another proceeding that certain limitations are indefinite.

³ Petitioner retains the right to dispute the claimed priority in another proceeding.

- *Shinohara* (Ex-1005), U.S. Patent Publication No. 2012/0033119, which published on February 9, 2012, is prior art under 35 U.S.C. § 102(a)(1), (a)(2).
- *Yu* (Ex-1050), U.S. Patent Publication No. 2012/0153124, which published on June 21, 2012, is prior art under 35 U.S.C. § 102(a)(1), (a)(2).

B. Challenges

Ground	Claims	Basis	Prior Art
1	1-4, 6-8, 10-16, and 18	§ 103	<i>Kuboi</i>
2	1-4, 6-8, 10-16, and 18	§ 103	<i>Kuboi</i> and <i>Shinohara</i>
3	1-4, 7-8, 15, and 17-18	§ 103	<i>Yu</i> , <i>Kuboi</i> , and <i>Shinohara</i>

V. Level of Ordinary Skill in the Art

A person of ordinary skill in the art (“POSITA”) would have had at least a master’s degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems and semiconductor dice. Leiby, ¶¶95-96. Additional relevant work experience can compensate for less education, and *vice versa*. Leiby, ¶¶96-97.

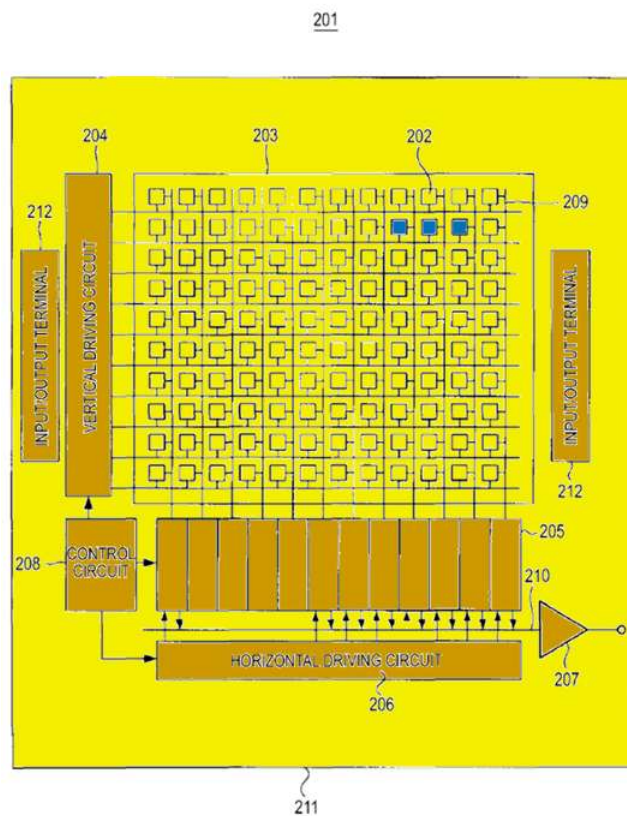
VI. The Challenged Claims Are Unpatentable

A. Claims 1-4, 6-8, 10-16, and 18 are Obvious Over *Kuboi* (Ground 1)

1. Overview of *Kuboi*

Kuboi's CMOS imaging device 201 includes a pixel region 203 and a peripheral circuit portion on a single semiconductor substrate 211. *Kuboi*, ¶[48]; Lebby, ¶¶73-75.

FIG.15



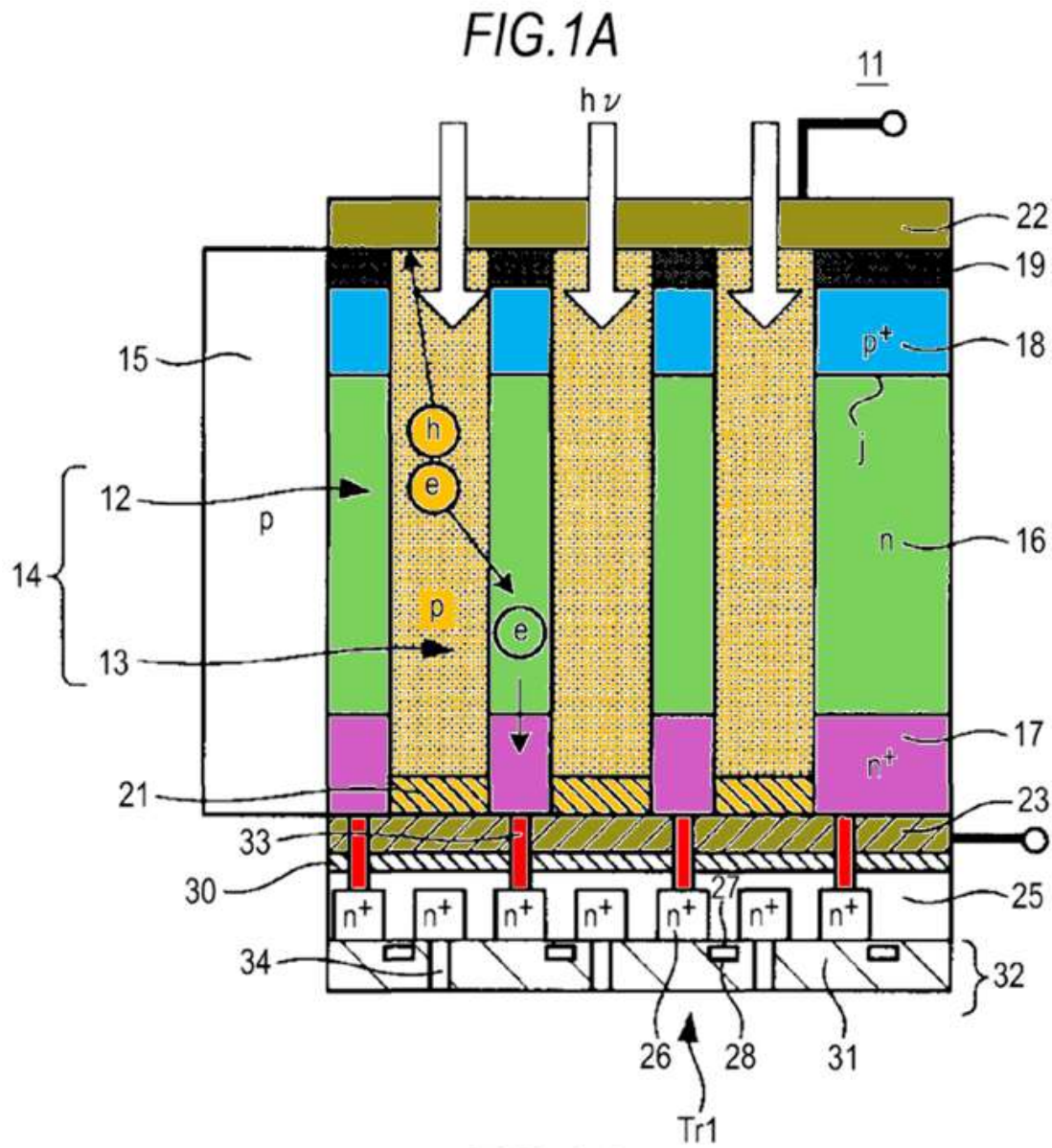
Kuboi, Fig. 15. Pixel region 203 of substrate 211 comprises a plurality of pixels 202 arranged in a two-dimensional array. *Kuboi*, ¶[48]. Each pixel 202 contains one photoelectric conversion portion (or a photodiode) and four pixel

transistors. *Id.* The peripheral circuit portion includes “logic[] circuits” (e.g., circuits 204, 205, 206, 207, and 208), which process the pixel’s electrical output and then output it. *Kuboi*, ¶¶[49]-[54]. The pixels and peripheral circuit portion are fabricated on a single substrate, the pixel transistors are fabricated on another substrate, and the two substrates are bonded together. *Kuboi*, ¶¶[62], [70], [78].

Kuboi describes photoelectric conversion portions suitable for use in imaging device 201. *Kuboi*, ¶[48]. For example, *Kuboi* discloses a basic pixel configuration with reference to Figures 1A/1B. *Kuboi*, ¶[55]. *Kuboi* likewise discloses a pixel configuration in Figures 6A/6B, explaining that the disclosed red and green pixels 53R and 53G have a structure that is the same as the basic configuration of Figures 1A/1B. *Kuboi*, ¶¶[90], [95], [69]. *Kuboi* also discloses that Figure 13 includes pixels 53R, 53G, and 53B, having configurations that are the same as the pixels of Figures 1A/1B. *Kuboi*, ¶[181]. Similarly, *Kuboi* describes Figure 15 as applicable to all of *Kuboi*’s pixel configurations. *Kuboi*, ¶¶[35], [48]. Further, *Kuboi*’s Figures 4A-4F show a method of manufacturing the basic pixel configuration of Figures 1A/1B. *Kuboi*, ¶¶[69]-[76]. Thus, Figures 1A/1B, 6A/6B, 13, and 15 all disclose the pixel configuration of the same imaging device. And *Kuboi*’s Figures 4A-4F disclose methods of manufacturing that same pixel configuration. Accordingly, this Petition relies on Figures 1A/1B, 4A-4F, 6A/6B,

13, and 15, and *Kuboi*'s associated disclosures as representative of the pixel configuration of the same imaging device. Lebbby, ¶¶76-77.

Figure 1A illustrates a photoelectric conversion portion 14 in pixel 11. *Kuboi*, ¶¶[48], [55]-[56]. Pixel 11, including photoelectric conversion portion 14, can be utilized in imaging device 201. *Kuboi*, ¶¶[48], [55]; Lebbby, ¶78.

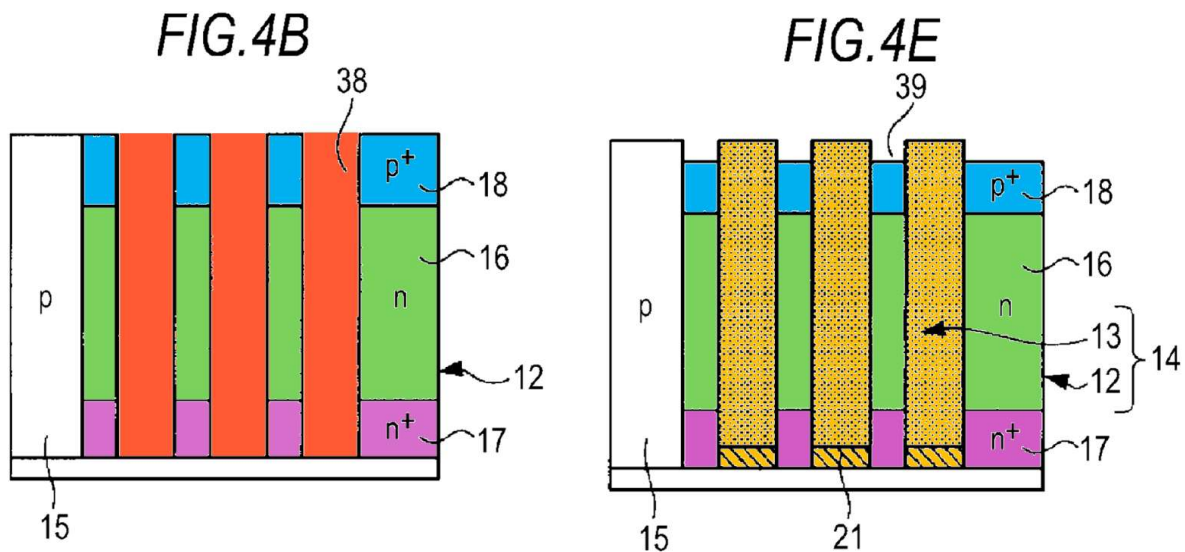


Kuboi, Fig. 1A. Photoelectric conversion portion 14 comprises a silicon semiconductor layer 12 that includes multiple embedded organic material layers 13. Kuboi, ¶[55]. Silicon semiconductor layer 12 is implanted with different impurities (or doped) to form n-type semiconductor (or “intermediate”) region 16 with a p+ type semiconductor region 18 on one side and n+-type semiconductor

region 17 on the opposite side (i.e., stacked PiN regions). Kuboi, ¶¶[56], [71].

Layer 12's doping is such that region 18 and region 17 have a higher concentration of impurities than region 16. Kuboi, ¶[56]; Lebby, ¶79.

After forming regions 18, 16, and 17, holes 38 extending from p⁺ type region 18 to n⁺-type region 17 are etched into the PiN regions (below, left). Kuboi, ¶¶[71]-[72].



Kuboi, Figs. 4B (left), 4E (right). Then, the organic material that forms photoelectric conversion films 13 is deposited in holes 38 (above, right). Kuboi, ¶¶[72]-[73]; Lebby, ¶80.

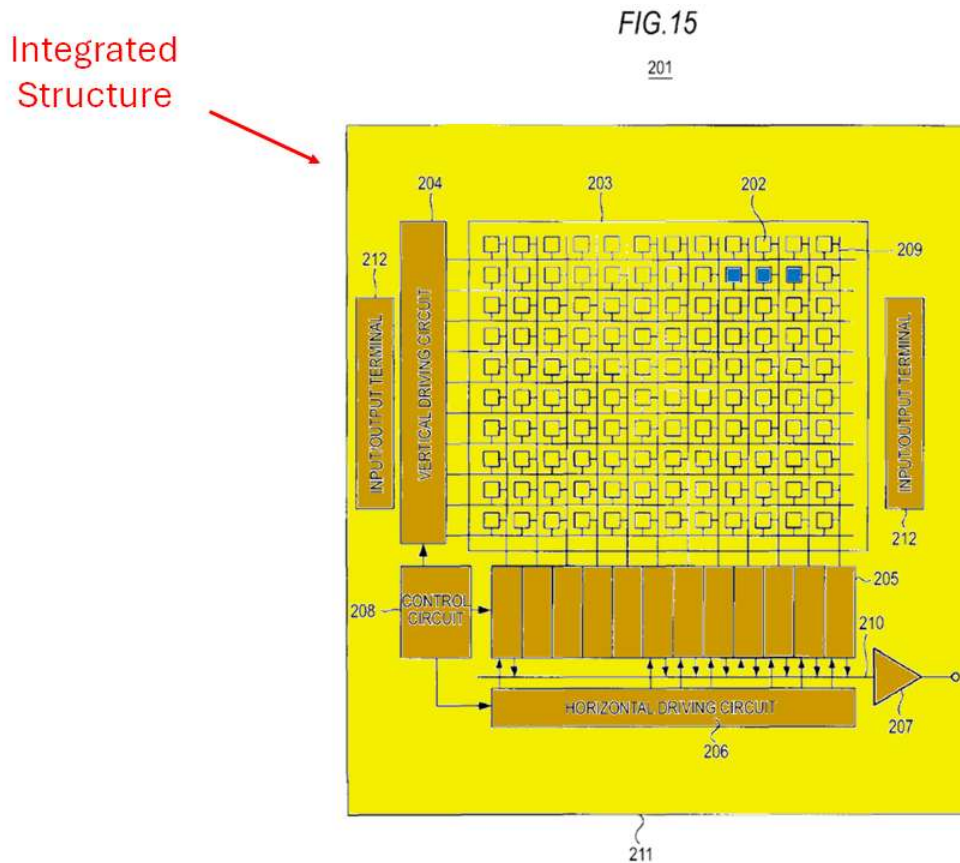
A metal shielding film 19 is applied to region 18's surface such that only holes 38 containing films 13 are exposed to incident light (hν). Kuboi, ¶¶[59], [72]-[73], [76], Figs. 1A, 4F. An upper electrode 22 and a lower electrode 23 are formed on opposite sides of the PiN regions, and a reverse bias is applied. Kuboi,

¶¶[60], [64]. Photoelectric conversion of the incident light (hv) within films 13 (inside holes 38) generates electron-hole pairs that pass through the depleted semiconductor layer 12 into a charge accumulation region 26 of the transfer transistor (Tr1) of the corresponding pixel 11 (via conductors 33). *Kuboi*, ¶¶[62], [64], [73]. After initial signal processing (i.e., amplification) by the pixel transistors, the electrical signals from the pixel 11 are sent to the peripheral circuit portions for further processing. *Kuboi*, ¶¶[48]-[49], [61]-[62]; *Lebby*, ¶¶81-82.

2. Independent Claim 1

a. [1pre]: “An integrated structure comprising:”

To the extent the preamble is limiting, *Kuboi* discloses it. *Lebby*, ¶¶101-103. *Kuboi*’s CMOS imaging device 201 includes pixel region 203 and peripheral circuit portion on a single semiconductor substrate 211. *Kuboi*, ¶[48]. Substrate 211’s pixel region 203 comprises a plurality of pixels 202, each of which contains a photoelectric conversion portion. *Id.* The pixels and peripheral circuit portion are fabricated on a single substrate. *Kuboi*, ¶¶[70], [78]. *Kuboi*’s imaging device is an “integrated structure” because it combines structures, such as, pixels with photoelectric conversion portions and peripheral electric circuits. *Lebby*, ¶103. *Kuboi*’s integrated structure is shown below:

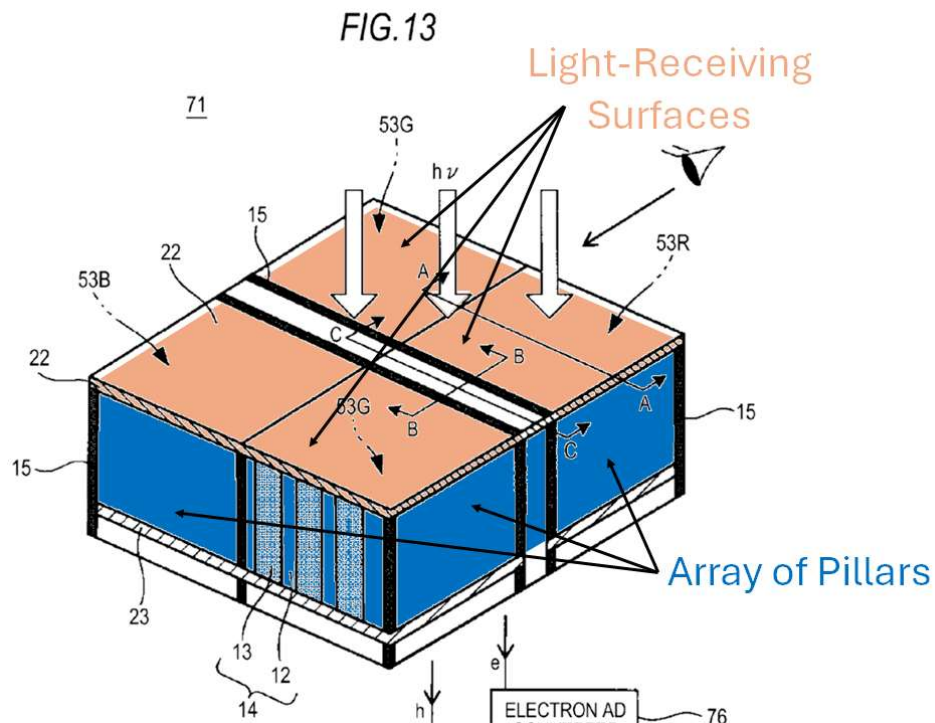


Kuboi, Fig. 15.

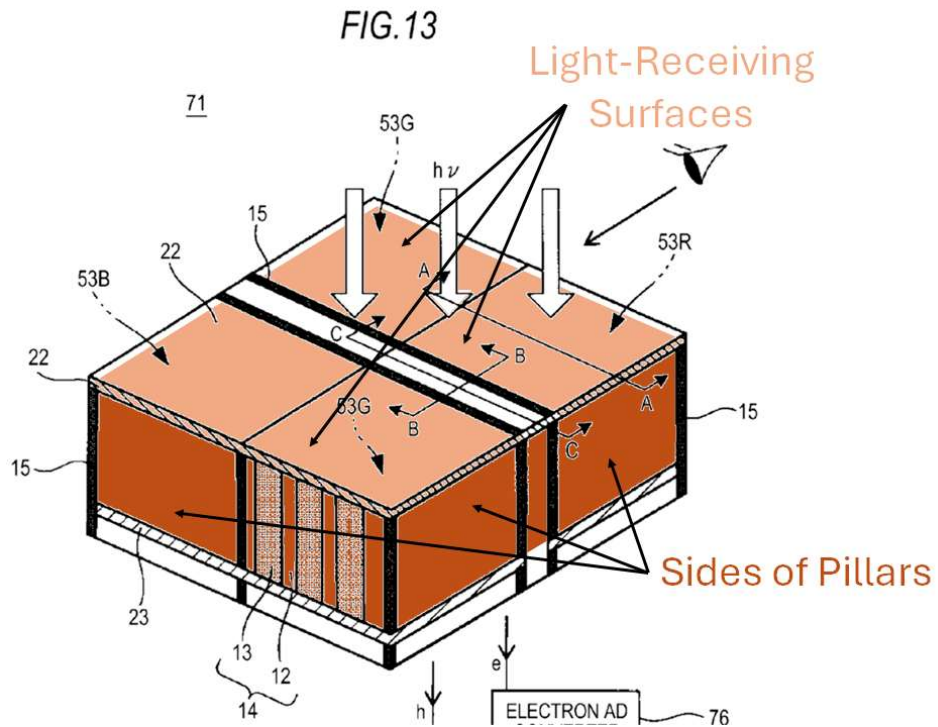
- b. [1a]: “an array of pillars comprising Si, Ge, and/or SiGe alloy semiconductor material wherein at least some of the pillars are configured as photodetectors that have respective light-receiving surfaces and have sides;”

Kuboi discloses [1a]. Lebbby, ¶¶104-110. The pixel region of *Kuboi*’s “imaging device” includes “a plurality of pixels 202 which include a photoelectric conversion portion and which are regularly arranged in a two-dimensional array.” *Kuboi*, ¶[48]. Specifically, *Kuboi*’s imaging device includes “red, blue, green, and green pixels ... arranged in a two-dimensional array.” *Kuboi*, ¶¶[181], [90]. “Light

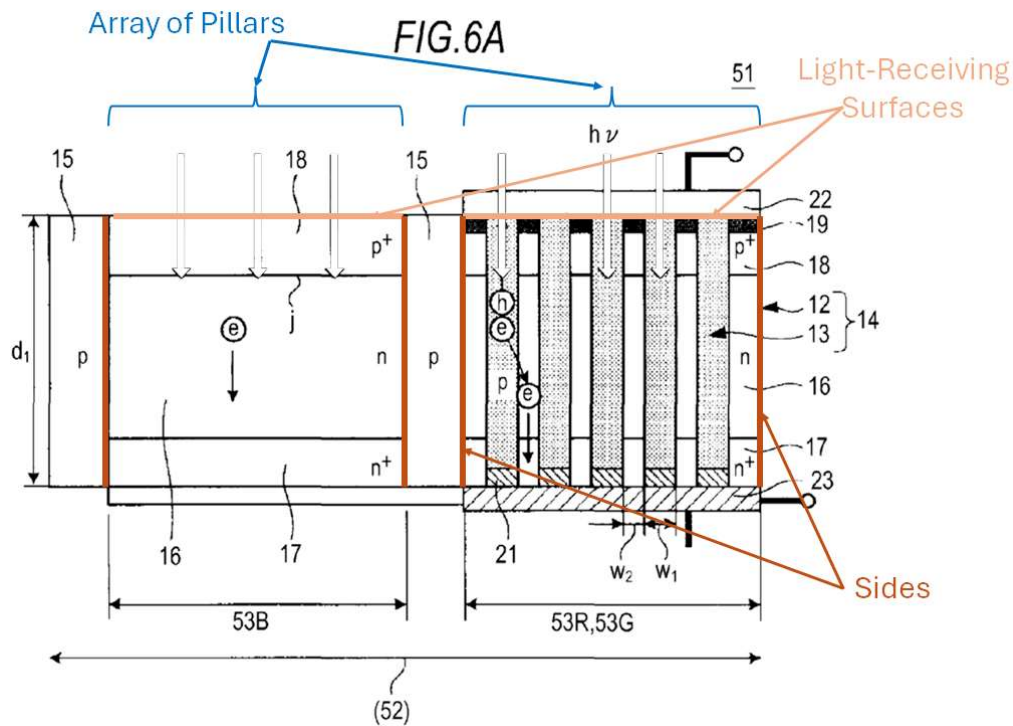
$h\nu$ enters the p-type organic photoelectric conversion films 13” of *Kuboi*’s pixels. *Kuboi*, ¶¶[186], [64]. *Kuboi*’s “upper electrode 22 on the light incident side is formed of a transparent electrode.” *Kuboi*, ¶[93]. A POSITA would have understood that the light incident side (“light-receiving surfaces”) of *Kuboi*’s pixels (i.e., pillars) are located on upper electrode 22’s lower surface because electrode 22 is formed *on* the light incident side. Lebbby, ¶¶106-108. In the figures below, each pixel constitutes a pillar in the two-dimensional array and light $h\nu$ is incident on and enters via each pixel’s light-receiving surface.



Kuboi, Fig. 13. And the pixels (i.e., pillars) have sides:



Kuboi, Fig. 13. A cross-sectional view of *Kuboi*'s array of pillars illustrating these features is shown below.



Kuboi, Fig. 6A.

Kuboi's blue pixel 53B and red and green pixels 53R and 53G include photoelectric conversion portions. *Kuboi*, ¶[90]; see also *Kuboi*, ¶¶[48], [55], [69]-[71], [79]-[80], [91], [108], [181]. *Kuboi* explains that "[l]ight $h\nu$ passes through the on-chip microlens to enter the p-type organic photoelectric conversion film 13, in which the light is subjected to photoelectric conversion, whereby electron-hole pairs are generated." *Kuboi*, ¶[64]. Thus, *Kuboi*'s pixels are photodetectors because its pixels detect light by absorbing light photons and generating electric charge carriers. Lebbby, ¶109.

Kuboi explains that “silicon semiconductor layer 12” is divided into respective **pixels**. *Kuboi*, ¶[91]. Because *Kuboi*’s **pixels** are formed in a silicon (or Si) semiconductor layer, *Kuboi*’s **pixels** (i.e., **pillars**) comprise Si. Lebbby, ¶110.

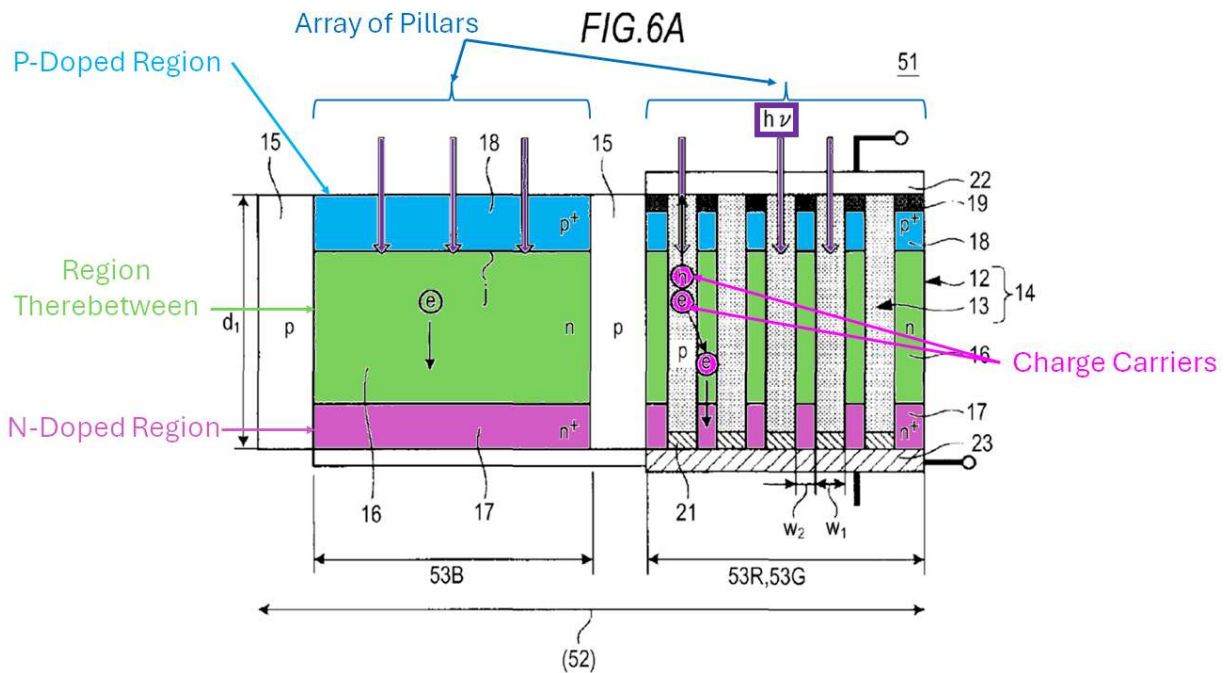
- c. [1b]: “wherein at least some of the **photodetectors** comprise **P-doped** and **N-doped** regions and **regions therebetween** and are configured to respond to illumination with **light** in selected **visible and infrared wavelength ranges** by generating **electrical charge carriers**;

Kuboi discloses [1b]. Lebbby, ¶¶111-118. *Kuboi*’s imaging device includes an **array of pixels**, each of which is a **photodetector**. VI.A.2.b ([1a]); *Kuboi*, ¶[90]. In blue pixel 53B (i.e., a **pillar**), “a **p⁺-type semiconductor region 18**, an **n-type semiconductor region 16**, and a **n⁺-type semiconductor region 17** are formed in that order from the light incident surface of the semiconductor layer 12 toward the opposite surface.” *Kuboi*, ¶[91]; *see also* *Kuboi*, ¶¶[71], [181]. In red pixel 53R (i.e., a **pillar**) and green pixels 53G (i.e., **pillars**), “the same **p⁺-type semiconductor region 18**, **n-type semiconductor region 16**, and **n⁺-type semiconductor region 17** are formed.” *Kuboi*, ¶[91].

Kuboi’s silicon “semiconductor layer 12 is implanted with impurities ... [to form] a **n⁺-type ... region 17** having higher concentration [of impurities] than the **n-type ... region 16**, and a **semiconductor region 18** of second conductivity type (for example, p⁺ type) having higher concentration [of impurities] than the **n-type**

[] region 16.” *Kuboi*, ¶¶[55]-[56]; *see also Kuboi*, ¶¶[111], [151], [7]. The process of implanting impurities into silicon is known as “doping,” and therefore, p⁺-type semiconductor region 18 is a “P-doped” region, and n⁺-type semiconductor region 17 is an “N-doped” region. Lebbby, ¶¶113-115 (citing Ex-1076, 5 (“doping”); Ex-1063, 4, 37; Ex-1020, 4). Region 16 is the “region[] therebetween” because it is positioned between region 18 and region 17. Lebbby, ¶115.

Pixel 11 “include[s] a hybrid photoelectric conversion portion 14” that includes “a plurality of organic material layers 13 embedded in the semiconductor layer 12.” *Kuboi*, ¶¶[55], [91], [181]. *Kuboi* explains that []light hv enters the p-type organic photoelectric conversion film 13, which in response generates electron-hole pairs (or charge carriers). *Kuboi*, ¶[64]. Thus, *Kuboi*’s photodetector pillars generate electron-hole pairs (charge carriers) when illuminated with light hv (light photons incident on said array of pillars). Lebbby, ¶¶116-117; *Kuboi*, ¶[107]. This is illustrated below.

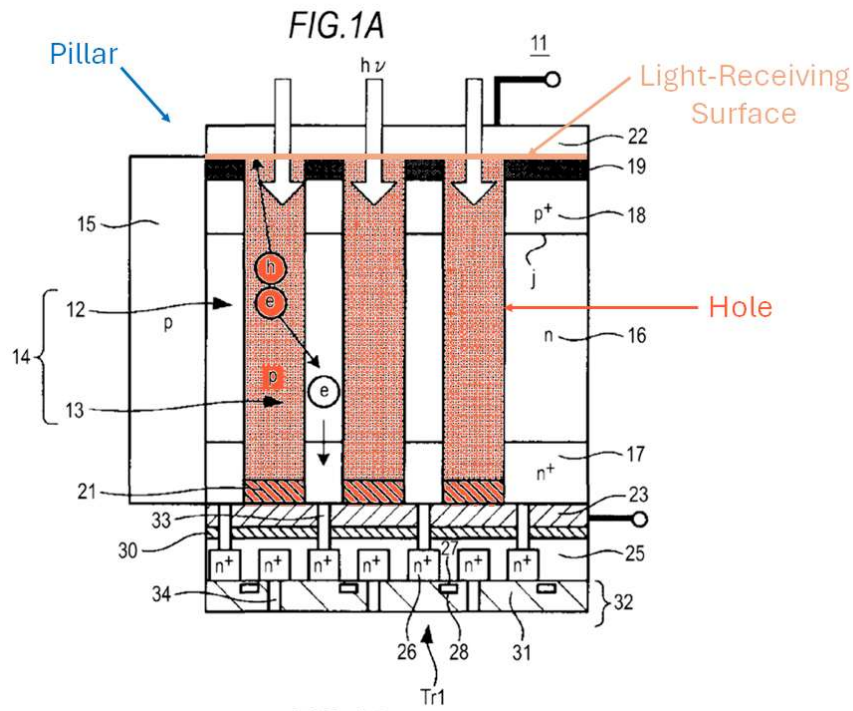


Kuboi, Fig. 6B.

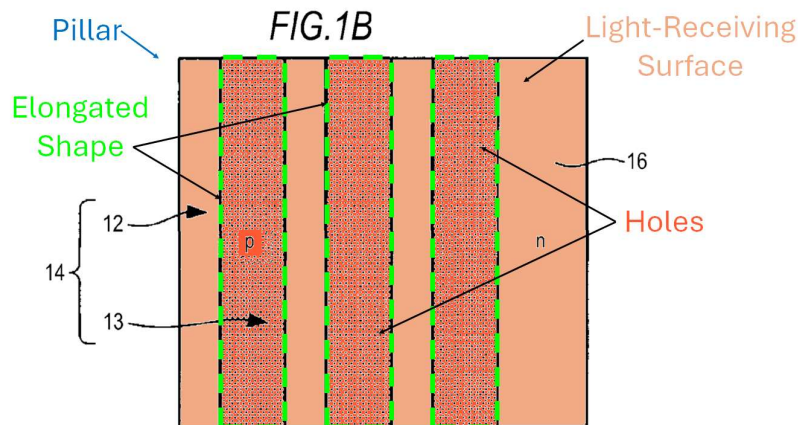
Kuboi's imaging device can be used in the visible light region and in other wavelength bands, including infrared. *Kuboi*, ¶[190]. *Kuboi*'s organic material is sensitive to (i.e., generates electric charge carriers in response to) “visible light” but compounds sensitive to infrared rays can also be used. *Kuboi*, ¶[58]. A POSITA would have found it obvious that by selecting a suitable organic material, *Kuboi*'s photodetectors would respond to light in a wavelength range selected from the visible and infrared light spectrum, as claimed. Lebbby, ¶118. A POSITA would also have had a reasonable expectation of success in doing so because *Kuboi* already discloses selecting the organic photoelectric film material to detect light in selected visible and/or infrared wavelength ranges. *Id.*; *Kuboi*, ¶[58].

- d. [1c]: “one or more **holes** that are deliberately formed into the **light-receiving surfaces**, have **elongated and/or other shapes** at said **light-receiving surfaces**, extend into the **photodetectors** to a depth of 100 to 10000 nm, and are filled at least partly with **solid dielectric material**;

Kuboi discloses or suggests [1c]. Leiby, ¶¶119-135. *Kuboi* discloses that “hole 38 such as a trench or a via extending from the p⁺-type semiconductor region 18 to the n⁺-type semiconductor region is formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching.” *Kuboi*, ¶¶[72], [13]-[14], [95]. A “plurality of **vertical holes 38** are formed at necessary intervals.” *Kuboi*, ¶[72]. *Kuboi* describes its vertical holes as “so-called [] **trench**.” *Kuboi*, ¶[67]. “[A]s shown in FIG. 1A [below], the vertical holes 38 are formed in a **stripe shape** as seen in a planar view.” *Kuboi*, ¶[72].



Kuboi, Fig. 1A. *Kuboi*'s "organic photoelectric conversion film 13 is deposited so as to be embedded in the vertical holes 38." *Kuboi*, ¶[73]. "[A]s shown in FIG. 1B [below], the plurality of organic photoelectric conversion films 13 are formed in a stripe shape so as to divide the semiconductor layer 12 into a plurality of parts as viewed from the upper surface." *Kuboi*, ¶[57].

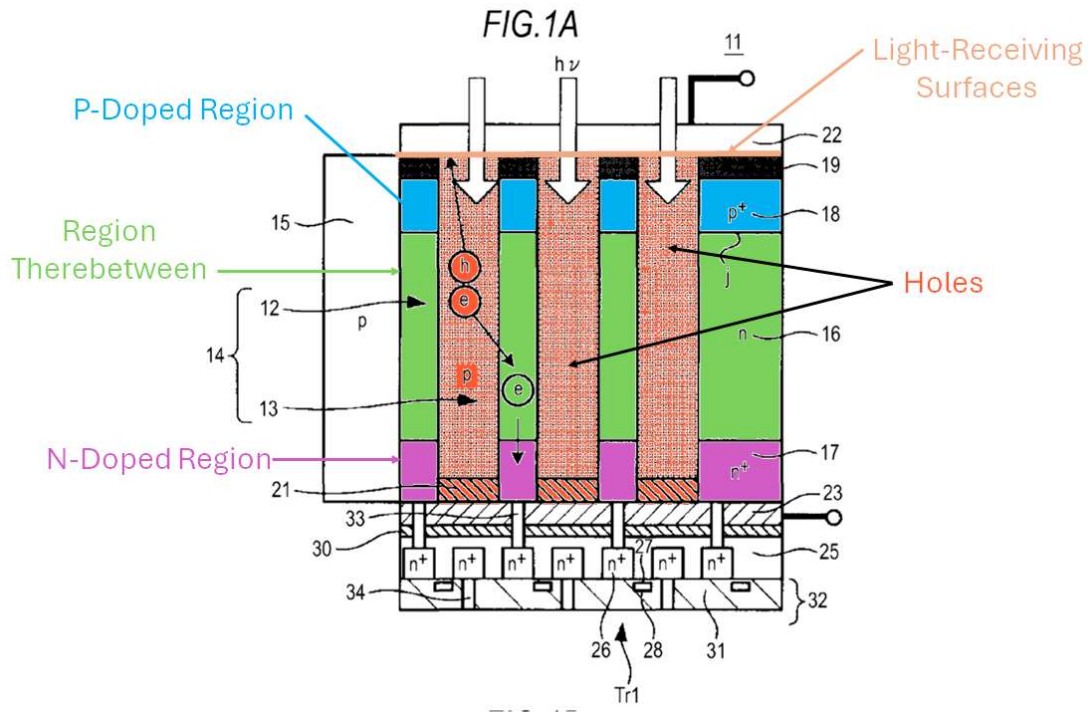


Kuboi, Fig. 1B. As seen in the plan view of Fig. 1B, above, the **holes** in the **light-receiving surface** of *Kuboi*'s **pixel** (i.e., **pillar**) above have **elongated or other shapes**. Lebbby, ¶¶120-122.

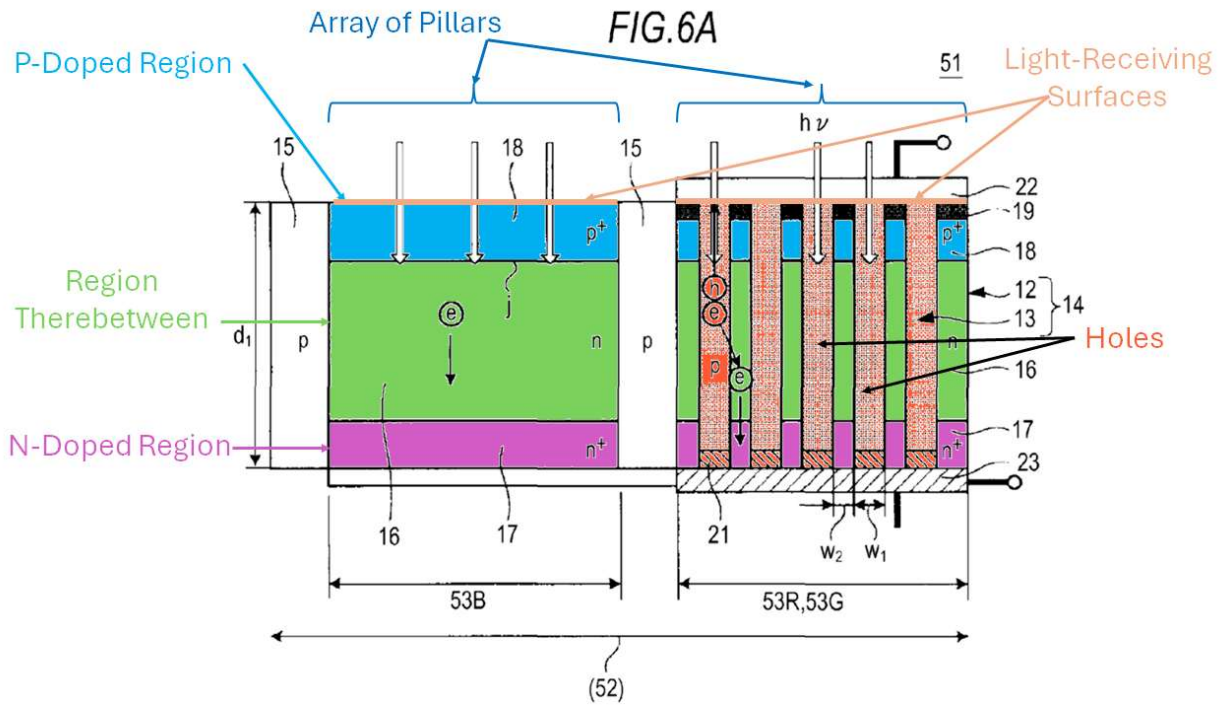
Although Figures 1A/1B illustrate only one **pixel** (i.e., **pillar**), as discussed for [1a], *Kuboi*'s imaging device includes an **array of pixels** (53R and 53G). VI.A.2.b ([1a]). *Kuboi*'s **pixels 53R and 53G** have structures similar to Figure 1A's pixel. *Kuboi* ¶[90]. Thus, a POSITA would have understood that *Kuboi*'s imaging device has a **plurality of pixels 53R and 53G** (i.e., **pillars**), that include one or more **holes** ("at least one," "at least some," or "a plurality of holes") having **elongated or other shapes** (or formed as **elongated trenches**). Lebbby, ¶123.

Kuboi's **holes 38** that extend through the **PIN** regions may be dry-etched using "a CCP (Capacitive Coupled Plasma) etching apparatus." *Kuboi*, ¶¶[72], [95]. Because **holes 38** are formed using an etching apparatus, as shown below, **holes 38** extending from **region 18** to **region 17** are deliberately formed in the

light-receiving surfaces located between region 18 and electrode 22. Lebbby, ¶¶¶124-125.

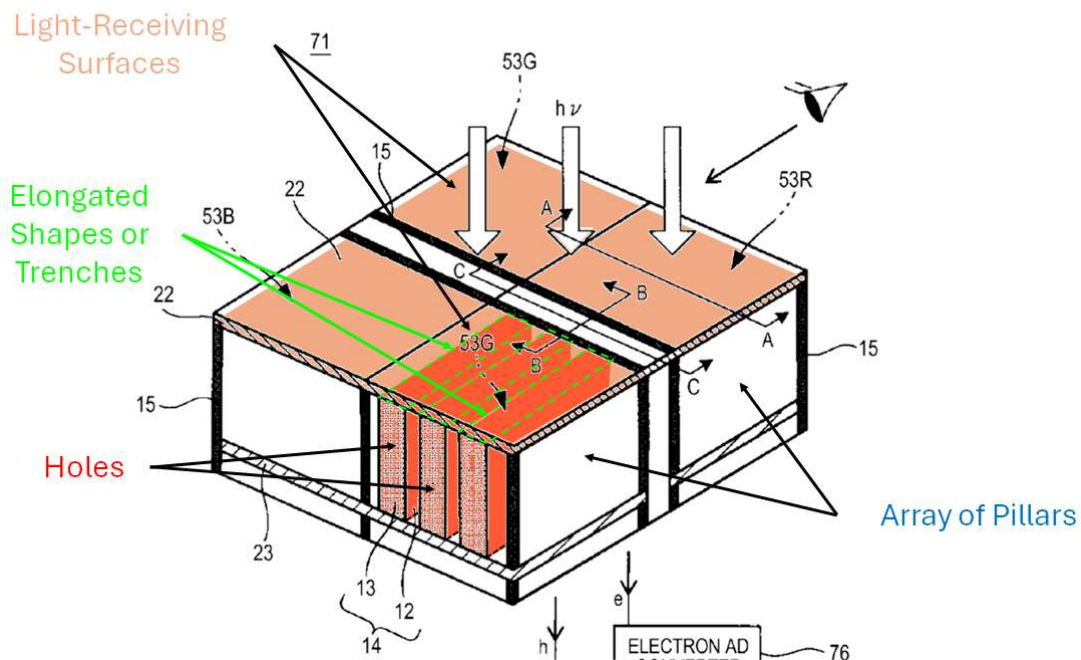


Kuboi, Fig. 1A.



Kuboi, Fig. 6A. A perspective view of *Kuboi*'s **holes** (or **trenches**) having **elongated or other shapes** is illustrated below:

FIG. 13



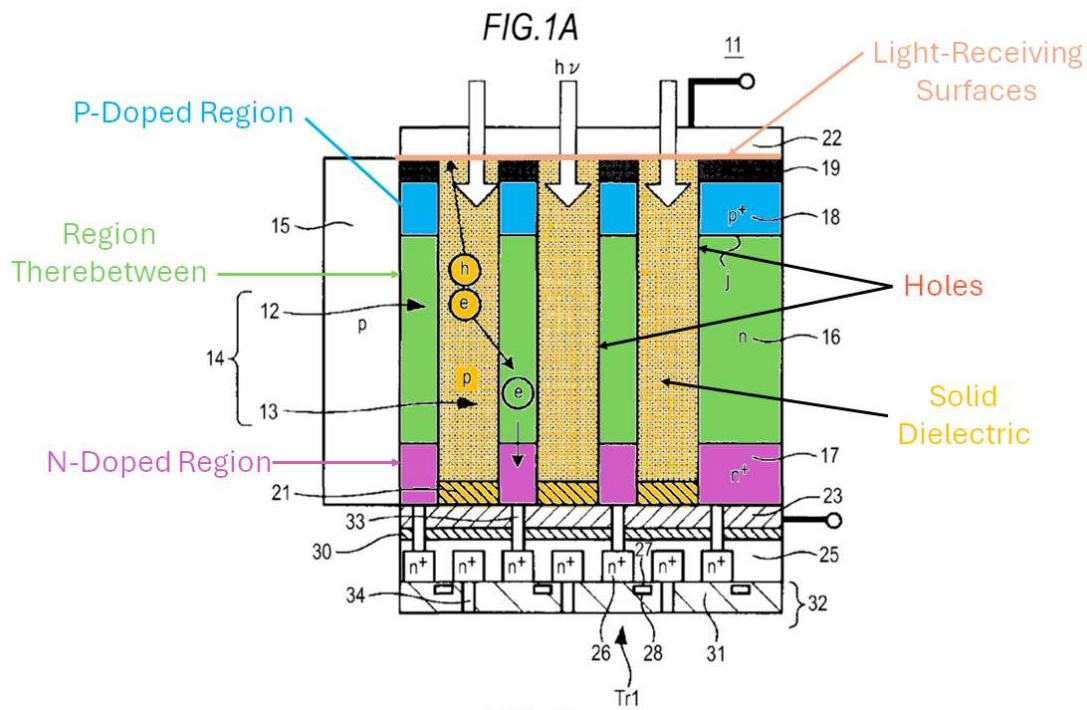
Kuboi, Fig. 13.

Kuboi also discloses that “an **electron blocking film 21** having a thickness of several tens of nm, for example is formed on the bottom portions of the vertical holes 38.” *Kuboi*, ¶¶[73], [91]. “[**F**]ilm 21 is formed by an insulating film such as, for example, a silicon nitride (Si_3N_4) film, a silicon [oxide] (SiO_2) film.” *Kuboi*, ¶[73]. Silicon nitride (Si_3N_4) and silicon oxide (SiO_2) are solid dielectrics. Lebbby, ¶¶126-130 (citing Ex-1020, 34-35; Ex-1063, 20-21, 23, 30, 33).

Like the organic material in the holes of the '871 patent, an organic material is deposited to fill the remaining portions of the **holes**, thereby forming organic **photoelectric conversion films 13** embedded within the hole. *Kuboi*, ¶¶[73], [58], [85], Fig. 4C; '871 Patent, 50:17-21. *Kuboi* discloses that “[a]s the p-type organic

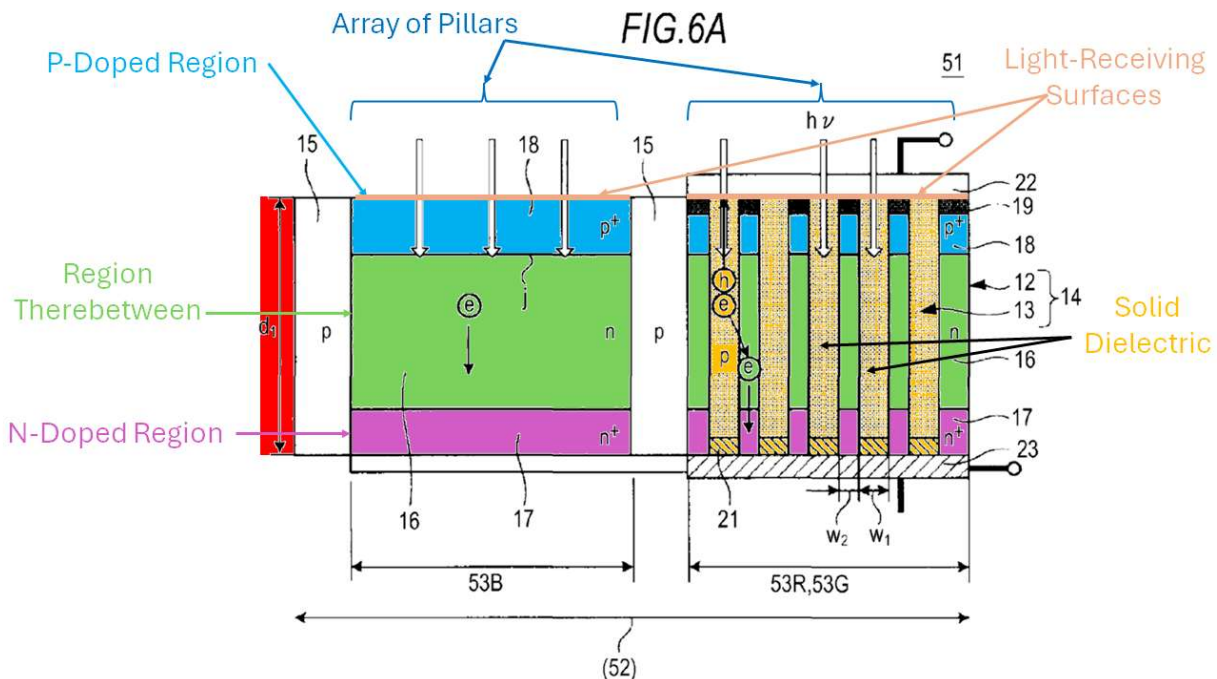
material [is] sensitive to a visible light region, perylene-based compounds, phthalocyanine compounds, quinacridone compounds, porphyrin compounds, merocyanine compounds, and the like can be used.” *Kuboi*, ¶[58]. A POSITA would have understood that phthalocyanine, perylene-based, and porphyrin compounds are **solid dielectrics**. Lebbby, ¶¶131-132 (citing Exs-1021, 1022, and 1034-1038).

Thus, as illustrated below, **electron blocking film 21** and **photoelectric conversion film 13** together entirely fill *Kuboi*’s **holes** and are **solid dielectrics**.



Kuboi, Fig. 1A; Lebbby, ¶133.

Kuboi also discloses that semiconductor layer 12’s thickness d_1 “is set to about 1.4 μm .” *Kuboi*, ¶[94], Fig. 6A. Thickness d_1 is illustrated below:



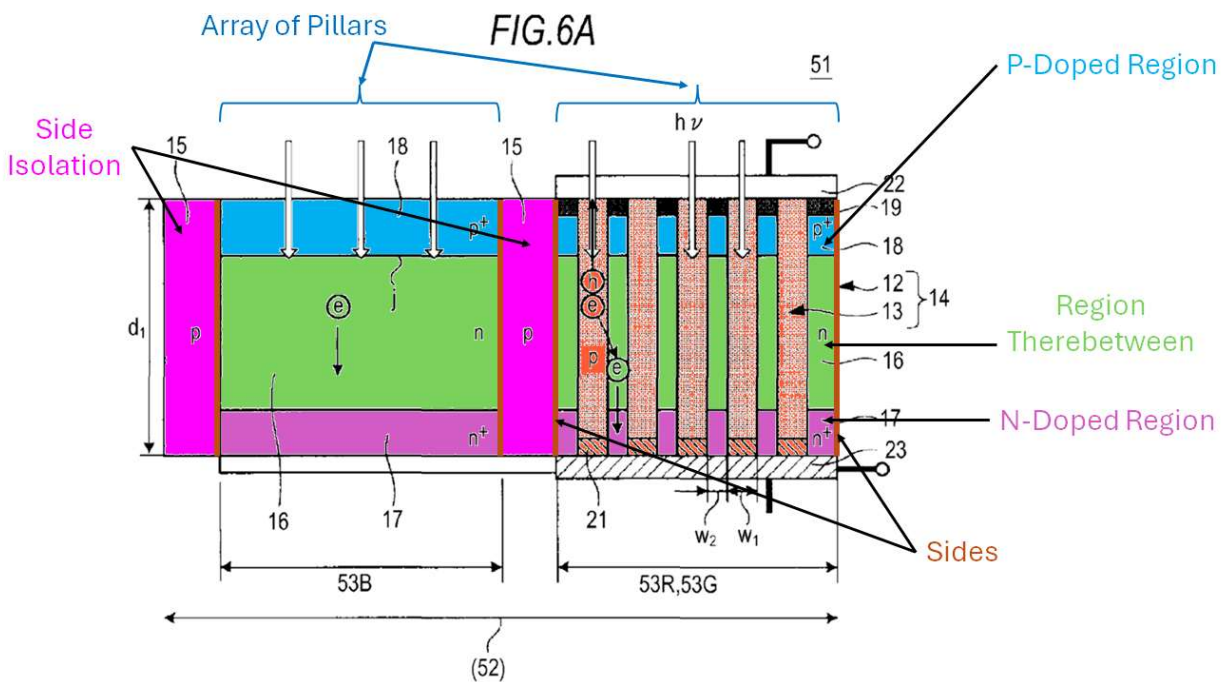
Kuboi, Fig. 6A. Because **holes 38** (filled with **solid dielectric**) extend through thickness **d₁**, **holes 38** extend into the *Kuboi*'s **pixel** (i.e., **photodetector**) for a depth of 1400 nm, which falls within the claimed 100-10,000 nm range. Lebbly, ¶¶134-135.

- e. [1d]: “**side-isolation** comprising solid material at said **sides** of at least some of the **photodetectors**;

Kuboi discloses or suggests [1e]. Lebbly, ¶¶136-137. *Kuboi*'s “silicon semiconductor layer 12 is divided into respective pixels by an element separation region 15 which is formed by a p-type semiconductor region.” *Kuboi*, ¶¶[91], [55]-[56], [71], [182]. *Kuboi*'s “pixel 11 is [also] separated by an element separation region 15.” *Kuboi*, ¶[55]. A POSITA would have understood that element separation region 15 provides side-isolation because it separates adjacent **pixels**,

which are **photodetectors**. Lebbby, ¶137; VI.A.2.b ([1a]). A POSITA would have understood that, because the p-type semiconductor region is part of *Kuboi*'s solid silicon semiconductor layer 12, the p-type semiconductor is a solid material.

Lebbby, ¶137. *Kuboi*'s **side-isolation** provided by the **p-type semiconductor region** at the **sides** of *Kuboi*'s **pixels** (i.e., **photodetectors**) is illustrated below.

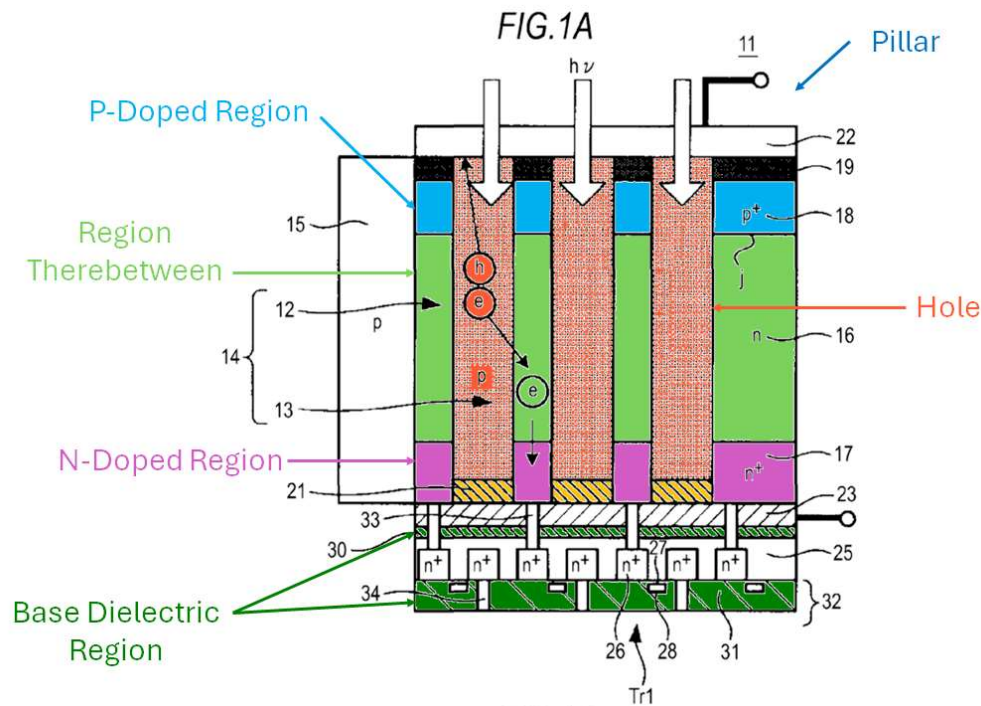


Kuboi, Fig. 6A.

- f. [1e]: “a solid dielectric material forming a **base dielectric region** for said **array**;

Kuboi discloses or suggests [1e]. Lebbby, ¶¶138-143. *Kuboi*'s “semiconductor region 25 formed of silicon [] is disposed on the front surface side of the semiconductor layer 12, namely under the lower electrode 23 with an insulating film 30 disposed therebetween.” *Kuboi*, ¶[61]. *Kuboi* discloses a

semiconductor substrate on which the semiconductor region 25 having pixel transistors, the multilayer wiring layer 32, and the lower electrode 23 are formed. *Kuboi*, ¶[69]. *Kuboi*'s multilayer wiring layer 32 includes a plurality of layers of wiring with an interlayer insulating film 31 disposed therebetween. *Kuboi*, ¶[62]. Insulating film 30 and/or insulating interlayer film 31 constitutes the claimed base dielectric region because they are disposed at the base of *Kuboi*'s pillars. Lebbby, ¶139. *Kuboi*'s base dielectric region (films 30 and/or 31) is illustrated below:



Kuboi, Fig. 1A. Although Figure 1A illustrates only one pixel, *Kuboi*'s imaging device includes a plurality of pixels (53R and 53G) arranged as an array of pixels. VI.A.2.b ([1a]). Pixels 53R and 53G have structures similar to the Figure 1A pixel. *Kuboi* ¶[90]. A POSITA would have understood that *Kuboi*'s multilayer wiring

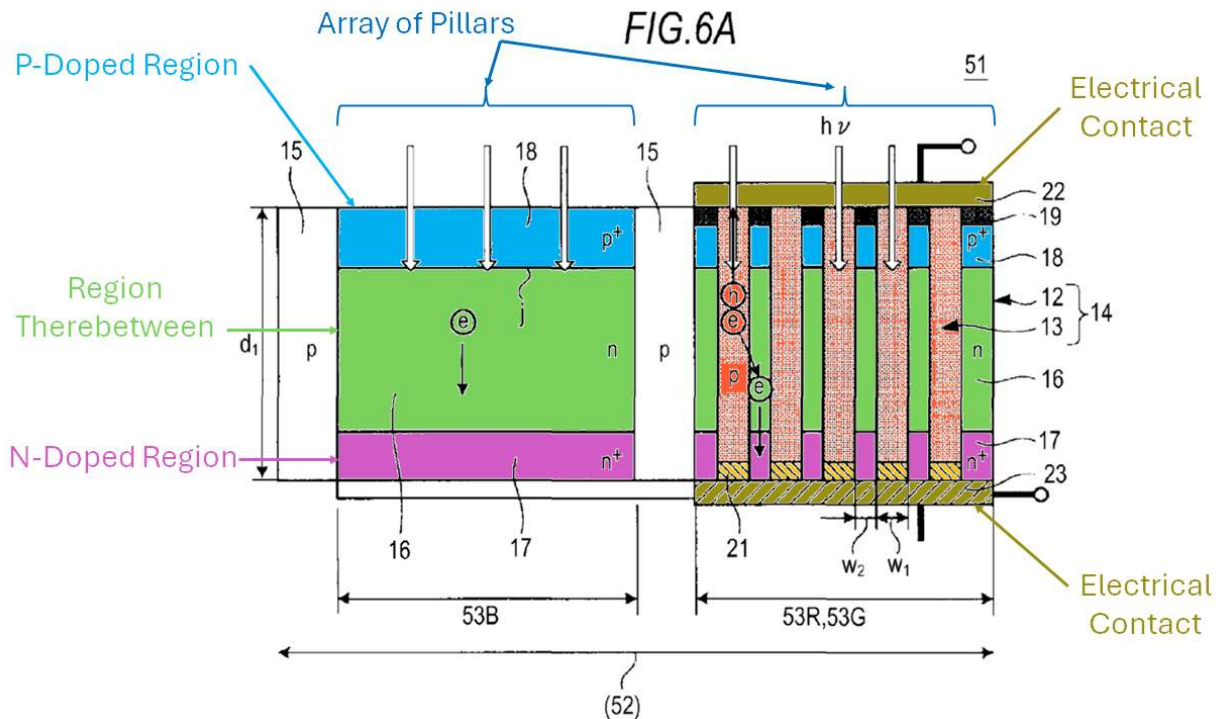
board with film 31 is located below *Kuboi*'s array of pixels, including pixels 53R and 53G. Lebbby, ¶143. Thus, Figure 1A's base dielectric region is a base dielectric region for *Kuboi*'s array of pixels.

Although *Kuboi* does not disclose the material of its semiconductor insulating films (30 and/or 31), a POSITA would have understood that semiconductor insulating films (i.e., 30 and/or 31) like those of *Kuboi* constitute silicon oxide or silicon nitride, which are dielectric materials, or at least would have been motivated to use silicon oxide or silicon nitride because these materials can be fabricated using standard silicon fabrication processes and because these materials provide good barriers to impurity and moisture diffusion. Lebbby, ¶¶140-142 (citing Ex-1020, 34-35; Ex-1059, ¶¶[13]-[14]; Ex-1060, 26:9-14; Ex-1063, 4-5, 20, 34). Thus, a POSITA would have found it obvious to form *Kuboi*'s insulating film 30 or 31 (i.e., base dielectric material) of a solid dielectric material like silicon oxide or silicon nitride. Lebbby, ¶141. A POSITA would also have a reasonable expectation of success in making insulating film 30 or 31 with a solid dielectric material because methods of formation with such materials in semiconductor fabrication were well known in the art. *Id.*

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- g. [1f] “**electrical contacts** configured to provide electrical pathways to at least some of the **photodetectors**, including for selected reverse-biasing thereof;”

Kuboi discloses or suggests [1f]. Lebbby, ¶¶144-148. *Kuboi* discloses “electrodes 22 and 23 [are] formed on the entire rear and [front] surfaces of the semiconductor layer 12.” *Kuboi*, ¶¶[60], [77], [93], [103]. “[U]pper electrode 22 on the rear surface side is formed by a transparent electrode formed of a transparent conductive film.” *Kuboi*, ¶[60]. And “lower electrode 23 is formed of metal exhibiting ohmic properties.” *Id.* *Kuboi*’s electrodes, which are electrical contacts, are illustrated below:



Kuboi, Fig. 6A.

Kuboi explains that “[l]ight $h\nu$ passes through the on-chip microlens to enter the p-type organic photoelectric conversion film 13, in which the light is subjected to photoelectric conversion, whereby **electron-hole pairs** are generated.” *Kuboi*, ¶[64]. A “necessary voltage is applied between the upper electrode 22 and the lower electrode 23.” *Id.* *Kuboi* discloses “**electrons e** ... move from the organic photoelectric conversion film 13 ... toward the semiconductor layer 12 depleted by the applied bias voltage” and “**hole h** moves toward the upper electrode 22 through the organic photoelectric conversion film 13 and is discharged through the upper electrode 22.” *Id.* Because the **holes** generated in *Kuboi*’s pixels (i.e., pillars) move through **electrodes 22**, and because **electrons e** move toward semiconductor layer 12 due to a bias voltage applied between **electrodes 22 and 23**, **electrodes 22 and 23** provide electrical pathways to at least to some of *Kuboi*’s **pixels** (which are **photodetectors**). Lebbby, ¶147; VI.A.2.b ([1a]).

A necessary voltage is applied between **electrodes 22 and 23** so that **p⁺-type region 18** is at a negative potential and **n⁺-type region 17** is at a positive potential. *Kuboi*, ¶¶[64], [87]. A POSITA would have understood that **electrodes 22 and 23** are configured to apply a voltage bias to *Kuboi*’s **pixels** (which include **photodetectors**) with a negative potential to **p⁺ type region 18** and a positive potential to **n⁺-type region 17**, resulting in a reverse bias. Lebbby, ¶148 (citing

Ex-1031, 3-5, 8). Moreover, because *Kuboi* allows reverse biasing of particular pixels and allows for selection of the *necessary* voltage for reverse biasing, a POSITA would understand that *Kuboi*'s **electrical contacts** (**electrodes 22 and 23**) are configured to provide electrical pathways for selected reverse biasing as claimed. Lebbby, ¶148.

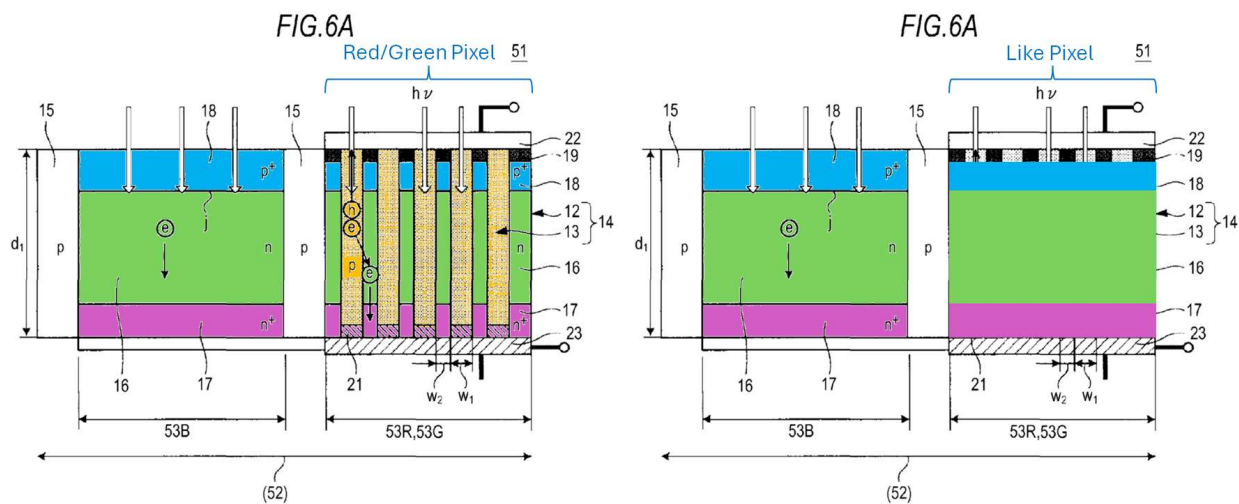
- h. [1g]: “wherein the presence of said one or more **holes** increases by a factor of at least 1.1 the absorption of the light by at least some of the **photodetectors** relative to otherwise like **photodetectors** lacking said holes.”**

Kuboi discloses or suggests [1g] based on a POSITA's knowledge of the state of the art before the '871 Patent's priority date and Patent Owner's statements in the '871 Patent. Lebbby, ¶¶149-175.

A POSITA would have found *Kuboi* discloses [1g]. Lebbby, ¶¶150-161. A POSITA would have understood that the amount of light absorbed by a material of thickness “d” can be determined using the Lambert-Beer expression as $I_0 (1 - e^{-\alpha d}) A$, where I_0 is the incident light intensity, α is the material absorption coefficient, and A is the light incidence area. Lebbby, ¶150 (citing Ex-1070, 23-25). *Kuboi*'s red and green pixels have 1.4 μm deep holes filled with phthalocyanine and porphyrin compounds, respectively. *Kuboi*, ¶¶[92], [94]. Compared to silicon, the absorption coefficient of porphyrin compounds is higher in the green light wavelength range of 510-580 nm, and the absorption coefficient of phthalocyanine

compounds is at least ten times larger for the red light wavelength range of 620-750 nm. Lebbby, ¶¶151-153. The higher absorption coefficient of *Kuboi*'s organic films increases light absorption by more than 10% over a comparable photodetector lacking holes. Lebbby, ¶151.

The figures below illustrate the structure of *Kuboi's* red or green pixels 53R or 53G (left) and a *like* pixel (right) lacking the holes. Lebbly, ¶154. Because both *Kuboi's* 53R or 53G pixel and the *like* pixel include *Kuboi's* light shielding film 19, both have the same area of light incidence, defined by the light shielding film openings. *Id.*



The figures below illustrate the structure of *Kuboi's* red or green pixels 53R or 53G (left) and a *hypothetical like* pixel (right) lacking the holes and the light shielding film. Lebbby, ¶155. The light incidence area for *Kuboi's* red or green

pixels (53R or 53G), as defined by the openings in the light shielding film is about 71% of the light incidence area for the *hypothetical like pixel*. *Id.*

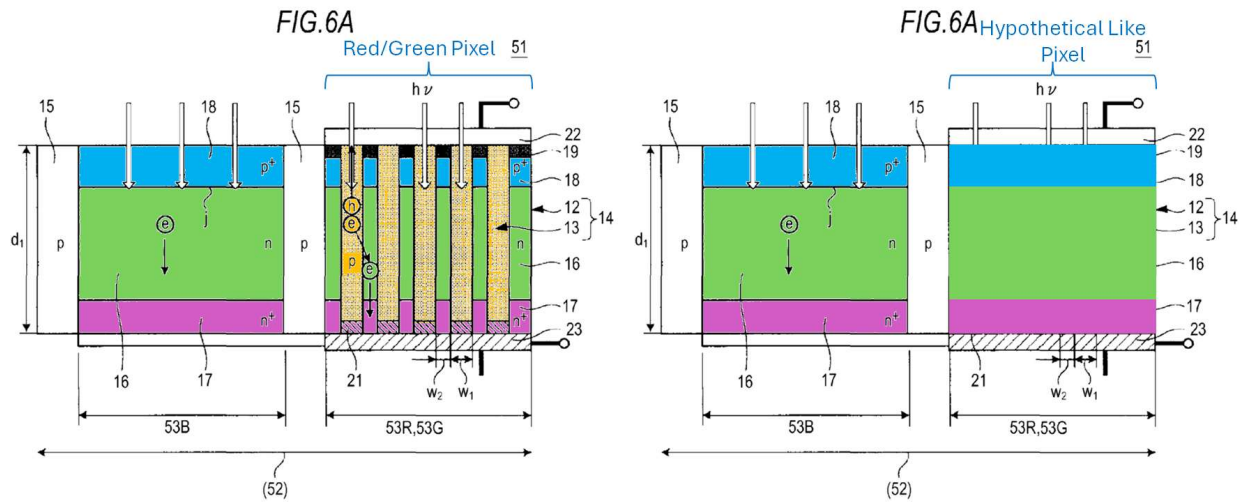


Figure A below illustrates the ratio, $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$, for the green light wavelength range of 490-580 nm (Yu, ¶[23]), where, $P_{\text{abs-organic}}$ represents the amount of light absorbed by *Kuboi's* green pixel and $P_{\text{abs-silicon}}$ represents the amount of light absorbed by a pixel without holes. Lebbby, ¶¶156-158.

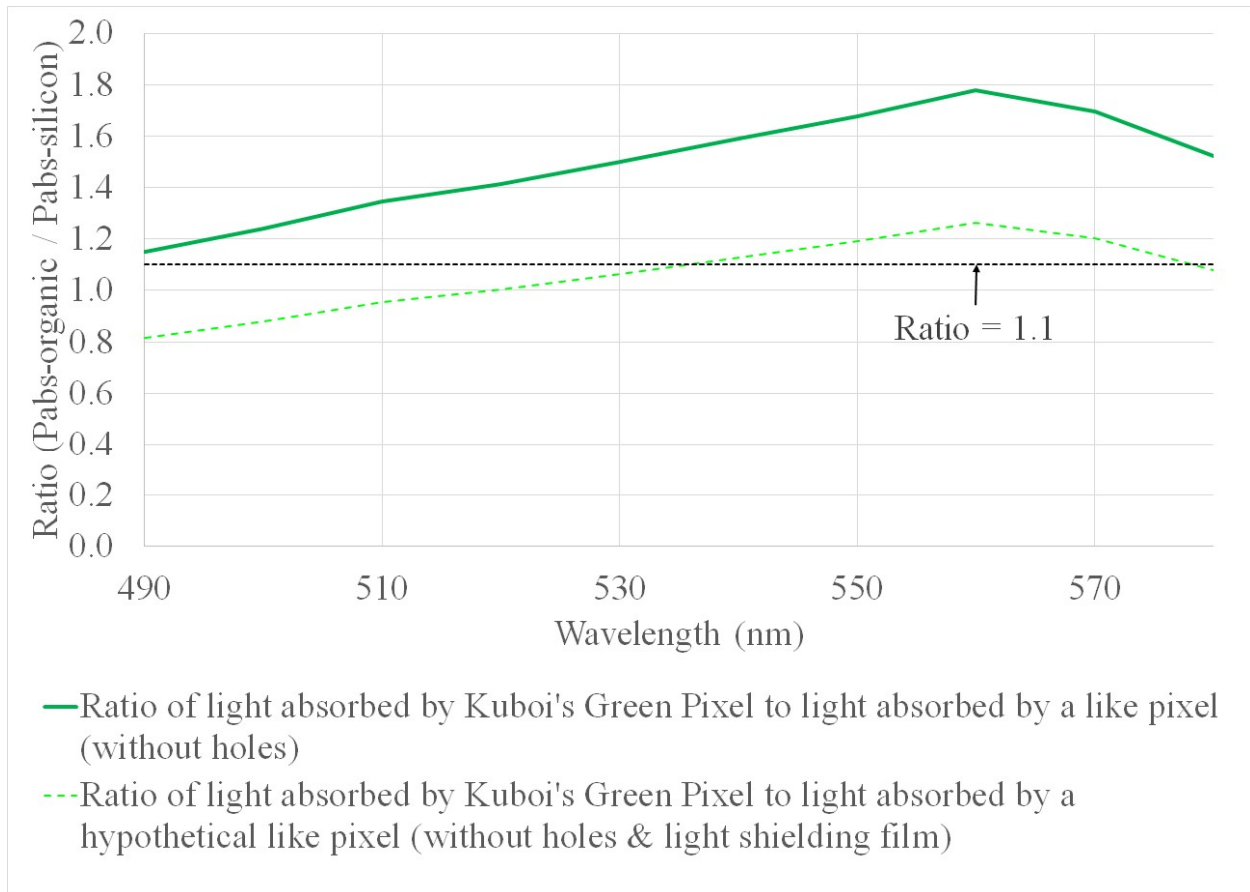


Figure A

In the above figure, the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for the *hypothetical like* pixel is obtained by scaling the same ratio for the *like* pixel by 71%. Lebbly, ¶158. As illustrated, the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ is greater than or equal to 1.1 (shown by the dashed black line) for the entire green light wavelength range for the *like* pixel and for the 540-570 nm wavelength range for the *hypothetical like* pixel. *Id.*

Figure B below illustrates the ratio, $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$, for *Kuboi's* red pixels, in the red light wavelength range of 620-780 nm (*Yu*, ¶[23]). Lebbly, ¶¶159-160.

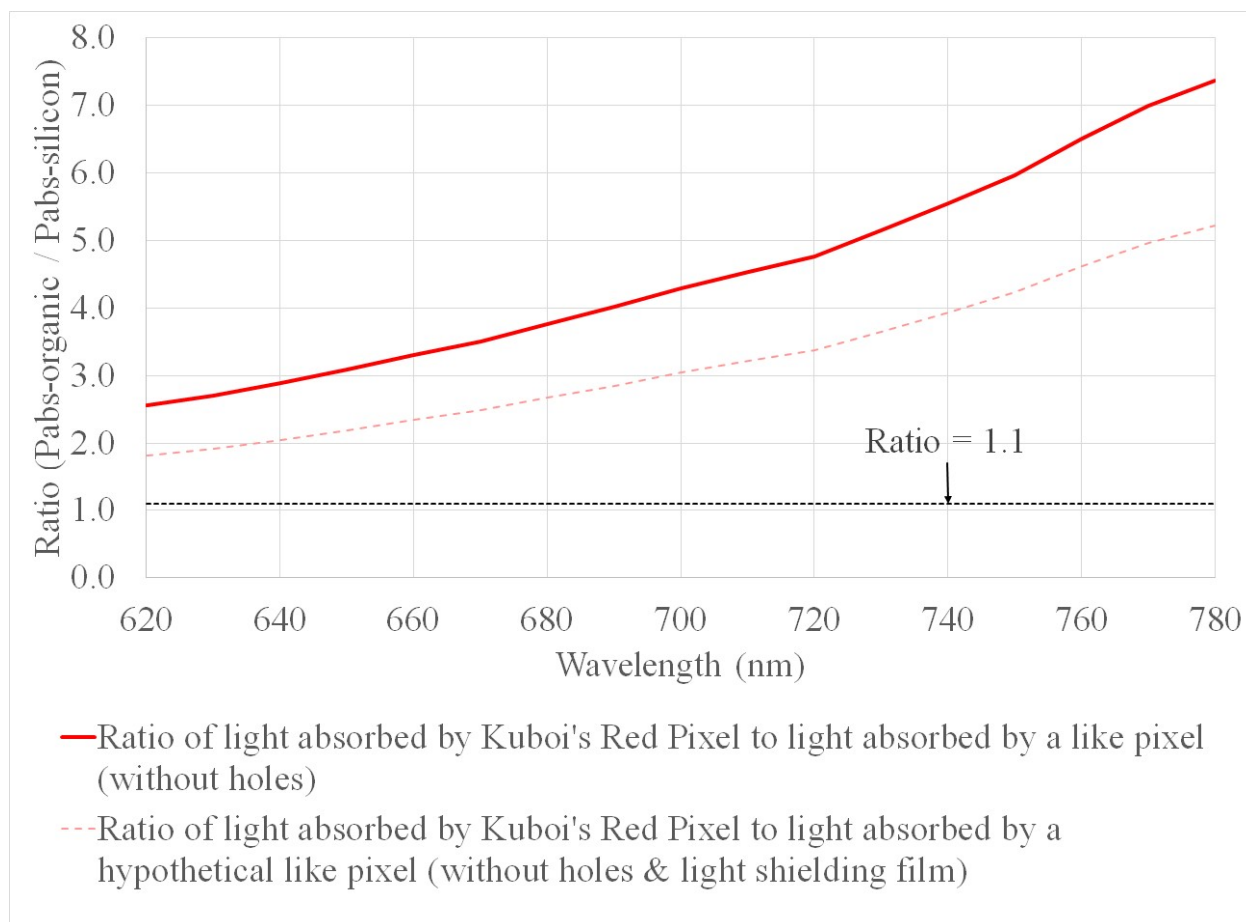


Figure B

As illustrated, the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ is greater than or equal to 1.1 for the entire red light wavelength range for both the *like* pixel and the *hypothetical like* pixel. Thus, a POSITA would have understood that *Kuboi's* photodetector with holes filled with organic material absorbs at least 1.1 times more light relative to a like photodetector having no holes at selected visible and infrared wavelength ranges of the light. Lebbly, ¶¶160-161.

A POSITA would also have found [1g] disclosed in view of Patent Owner's statements in the '871 Patent. Leebby, ¶¶162-173. The '871 Patent details the cause or causes of the enhancement of the absorption coefficient, explaining:

The cause or causes of the enhancement of the absorption coefficient are believed to include one or more of the following: an increase in optical field concentration, resonance effects, constructive and destructive optical interferences (amplitude and phase) effects, scattering, and *high contrast grating (HCG) effects*. See, i.e. Chang-Hasnain et al, High contrast gratings for integrated optoelectronics, *Advances in Optics and Photonics* 4, 379-440 (2012), hereinafter 'Chang-Hasnain.' The HCG effects are at the near-wavelength regime (See, Chang-Hasnain) where the optical wavelength in the material of the grating and the optical wavelength in the surrounding material of the grating is the range of the period of the grating.

'871 Patent, 11:52-64 (emphasis added). "The period of the 3D pillar/hole microstructured array can be seen as a 3D high contrast grating, whose period of the grating Λ can lie between λ/n_1 where n_1 is the optical refractive index of material M_1 and λ/n_2 where n_2 is the optical refractive index of material M_2 ." *Id.*, 12:14-18. Further, "[i]f $n_1 > n_2$ then $\lambda/n_1 < \Lambda < \lambda/n_2$." *Id.*, 12:18-19.

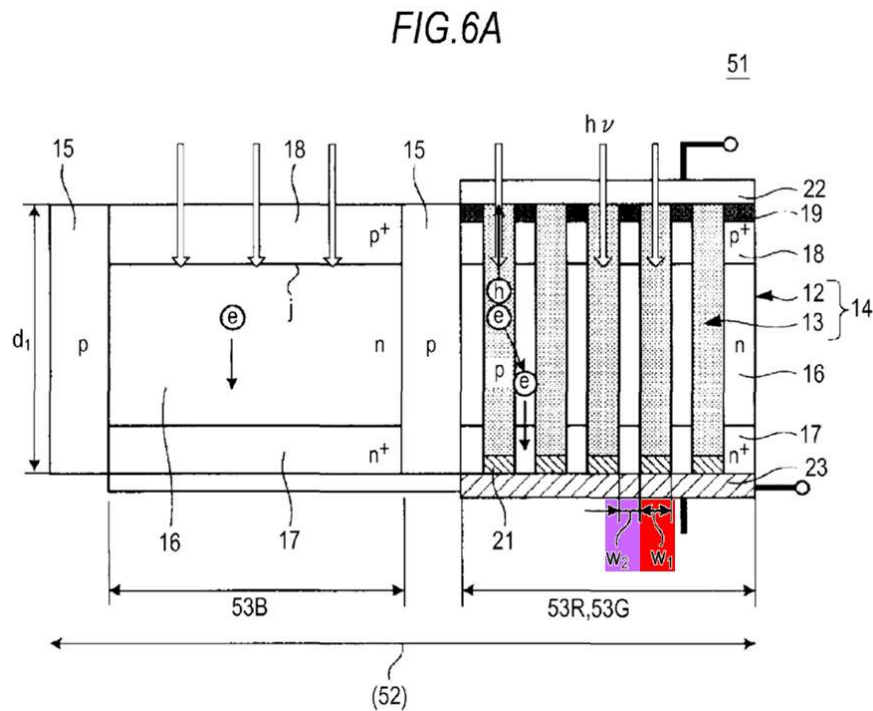
The '871 Patent explains that the HCG effect may explain the high absorption coefficient of semiconductors with holes that satisfy the relationship $\lambda/n_1 < \Lambda < \lambda/n_2$, stating:

The HCG effect that may explain the high enhancement of the absorption coefficient of the bulk material is that a single or multiple HCG layer (or a single microstructured pillar/hole array layer) due to its resonance effects and/or due to a varying of the microstructured pillar/hole period spacing, the optical signal resonating in the HCG/microstructured pillar-hole array can be directed to propagate in the plane of the HCG/microstructured pillar-hole array rather than normal to the surface. Together with resonance and in-plane propagation this can greatly increase the absorption path length in the HCG/microstructured pillar-hole array.

Id., 12:35-45. Finally, “[u]sing the phenomenon of near-wavelength and also deep-wavelength where the HCG period is much less than the optical wavelength, and the diffraction regime where the HCG period is greater than the optical wavelength (See, Chang-Hasnain) the microstructured pillar-hole-void array can have enhanced absorption coefficient over the bulk absorption coefficient by a factor of 1.1 to over 100.” *Id.*, 12:49-55.

Patent Owner thus represents in the '871 Patent that a microstructured pillar hole array having microstructure period Λ and satisfying the relationship $\lambda/n_1 < \Lambda < \lambda/n_2$ forms a high contrast grating (HCG). Leebby, ¶¶162-166. Patent Owner also represents that if the microstructure pillar hole array forms an HCG, then the physical phenomenon of near-wavelength and deep-wavelength result in an enhanced absorption coefficient of 1.1 to 100 times the bulk absorption coefficient. Leebby, ¶166.

Applying these representations to *Kuboi*, as illustrated below, *Kuboi* discloses width **w1** of photoelectric conversion films 13 is 200 nm and width **w2** of semiconductor layer 12 between the photoelectric conversion films is about 50 nm. *Kuboi*, ¶[94].



Kuboi, Fig. 6A. The period Λ or center-to-center distance between holes for *Kuboi* is thus 250 nm. Leebby, ¶167. Visible light has wavelength in the range 400-700 nm and infrared light has wavelength in the range 750 nm-1000 μm . Leebby, ¶168 (citing Ex. 1012, 4; *Yu*, ¶[23]). The refractive index n_1 of silicon varies from about 3.5 (wavelength 1000 nm) to 5.8 (wavelength 300 nm). *Id.* (citing Ex. 1056, 9:43-46, Fig. 4; Ex. 1061, 48). The refractive index n_2 of the organic material in *Kuboi*'s holes ranges between 1.5-3.0. Leebby, ¶169 (citing Ex-1057, 86:35-48, 142:18-25; Ex-1071, 6, Fig. 5, Ex-1072, 13, Fig. 7; Ex-1073, Abstract).

Using the above values for wavelengths and refractive indices, Table A shows the calculated values of λ/n_1 and λ/n_2 for *Kuboi*'s green pixels with porphyrin. *Kuboi*'s 250 nm hole pitch falls in the range λ/n_1 to λ/n_2 for at least part

of the visible light spectrum (400-700 nm wavelengths) and at least part of the near infrared light spectrum (>700 nm wavelengths). Lebbby, ¶170. For example, for the 550 nm green light wavelength, λ/n_1 ($550/4.5 = 123$) $< \Lambda$ (250 nm) $< \lambda/n_2$ ($550/2.0 = 275$).

Table A				
λ (nm)	n_1 (Silicon)	n_2 (Porphyrin)	λ/n_1(nm)	λ/n_2 (nm)
400	5.8	1.7	68	235
550	4.5	2.0	123	275
700	3.8	1.6	186	438
750	3.7	1.8	203	417

Similarly, Table B shows the calculated values of λ/n_1 and λ/n_2 for *Kuboi*'s red pixels with phthalocyanine. *Kuboi*'s 250 nm hole pitch falls in the range λ/n_1 to λ/n_2 for at least part of the visible light spectrum (400-700 nm wavelengths) and at least part of the near infrared light spectrum (>700 nm wavelengths). Lebbby, ¶171. For example, for the 650 nm red light wavelength, λ/n_1 ($650/3.9 = 168$) $< \Lambda$ (250 nm) $< \lambda/n_2$ ($650/2.1 = 302$)

Table B				
λ (nm)	n_1 (Silicon)	n_2 (Phthalocyanine)	λ/n_1 (nm)	λ/n_2 (nm)
400	5.8	1.9	68	211
650	3.9	2.1	168	302
700	3.8	1.8	186	389
750	3.7	2.3	203	326

Thus, the stated period of *Kuboi*'s pillar hole array falls within the range λ/n_1 to λ/n_2 for selected visible and infrared wavelength ranges of the light. Leiby, ¶172.

As a result, based on Patent Owner's representations, *Kuboi*'s pillar-hole array forms an HCG. Leiby, ¶173. And, under those same representations, such an HCG would produce an enhanced absorption coefficient of 1.1 to 100 times the bulk absorption coefficient based on the near-wavelength and deep-wavelength phenomena. *Id.* Thus, consistent with Patent Owner's representations, a POSITA would have understood that the absorption of light, at selected visible and infrared wavelength ranges, by at least some of *Kuboi*'s photodetectors with holes would be at least 1.1 times that of a like photodetectors lacking said holes. *Id.*

Patent Owner's representations were also consistent with those of other prior art teachings. Leiby, ¶¶174-175. For example, *Han* (Ex-1051) is consistent with Patent Owner's representations as to the impact of nanoholes on the ultimate

efficiency associated with photon absorption before the '871 Patent priority date.

Han, 7:19-8:5. According to *Han*, the ultimate efficiency for a device having a semiconductor thickness of about 1.4 μm without nanoholes is approximately 0.12, whereas the ultimate efficiency for a similar device having nanoholes is approximately 0.22. *Han*, Fig. 4; Lebbby, ¶174.

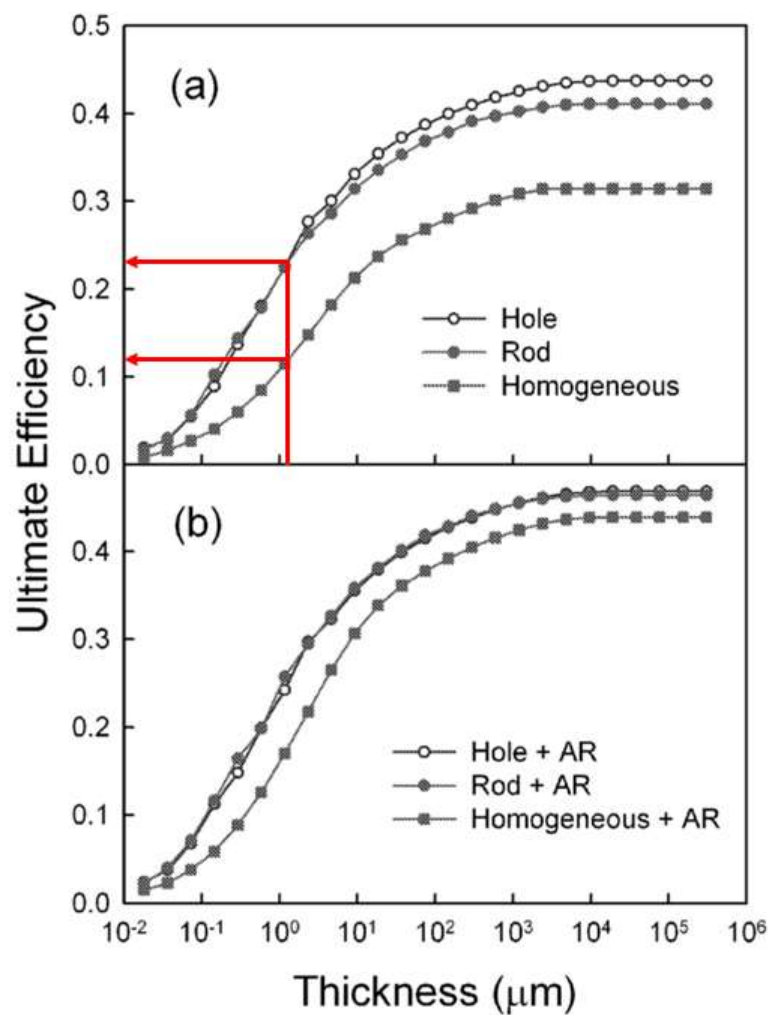


FIG. 4

Han, Fig. 4.

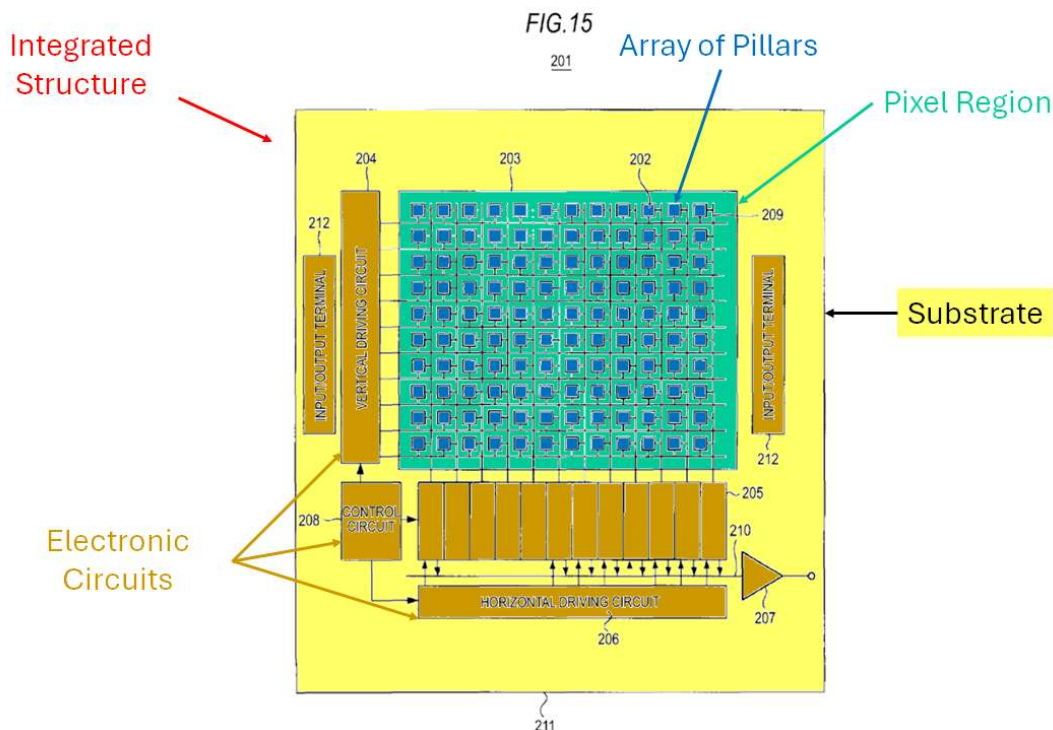
Thus, before the '871 Patent priority date, a POSITA would have understood that *Kuboi*'s 1.4 μm nanohole depth would increase light absorption by a factor of 1.8 ($0.22/0.12 = 1.8$), which is significantly higher than 1.1. Lebbby, ¶174; *Han*, Fig. 4. Accordingly, based on a POSITA's understanding of the state of the art before the '871 Patent's priority date, a POSITA would have understood that *Kuboi*'s 1.4 μm hole depth would have increased the absorption of light, at selected visible and infrared wavelength ranges, in at least some of *Kuboi*'s photodetectors by at least 1.1 times that of a like photodetectors lacking said holes, and even if not readily understood, a POSITA would have found such a result not only obvious but also one having a reasonable expectation of success in achieving this increase because *Kuboi* discloses forming nanoholes of 1.4 μm depth. Lebbby, ¶175.

3. Claims 2 and 18:

- a. [2] “The integrated structure of claim 1, wherein said array of **photodetectors** is monolithically integrated with **SI electronic devices**.”
- b. [18] “The integrate[d] structure of claim 15, in which said **array** of **photodetectors** is monolithically integrated with **Si electronic devices** that include **CMOS devices**.”

Kuboi discloses these additional limitations. Lebbby, ¶¶176-181. *Kuboi* discloses “a simplified exemplary configuration of a **CMOS solid-state imaging**

device.” *Kuboi*, ¶[48]. *Kuboi*’s imaging device 201 “include[s] a pixel region (so-called ... imaging region) 203 and a peripheral circuit portion which are provided on a semiconductor substrate 211 (i.e., a silicon substrate).” *Id.* *Kuboi*’s “pixel [region] and logical circuit portion may be created in advance.” *Kuboi*, ¶[78]. Thus, *Kuboi* teaches that the pixel region (i.e., array of pillars) is monolithically integrated with the logical circuit portion (including circuits 204-208). *Kuboi*, ¶¶[48]-[49]. A POSITA would have understood that circuits 204-208 would include electronic devices. Lebbby, ¶177 (citing Ex-1076, 3). This integrated structure is shown below:



Kuboi, Fig. 15.

Kuboi's disclosure, including Figure 15 and its method of fabrication, show that the **pixels** and the **logical circuit portion** are formed on a single substrate, **substrate 211**. *Kuboi*, ¶¶[70]-[78], [48]-[49]; Lebby, ¶¶178-179. A POSITA would have understood that because the **logical circuit portion** is formed on a **silicon substrate**, the logical circuit portion's electronic devices are **Si electronic devices**. Lebby, ¶179 (citing Ex-1076, 3). And because the **pixel region** (including an **array of pillars**) and **logical circuits** (electronic devices) are formed in or on the same silicon substrate, *Kuboi* discloses monolithically integrating the **array of pillars** (**pixel region**) with **Si electronic devices**, as recited in claim [2]. *Id.*

Furthermore, *Kuboi* discloses a "**CMOS solid-state imaging device**" formed on a silicon substrate. *Kuboi*, ¶[48]. Because *Kuboi*'s imaging device is a CMOS device, the devices in *Kuboi*'s **logical circuit portion** would include **CMOS devices**. Lebby, ¶180 (citing Ex-1076, 4). Because *Kuboi* discloses forming the **pixel region** (including an **array of pillars**) and **logical circuits** (including **CMOS devices**) on the same substrate, *Kuboi* discloses monolithically integrating the **array of pillars** (**pixel region**) with **Si electronic devices** that include **CMOS devices**, as recited in claim [8]. Lebby, ¶181.

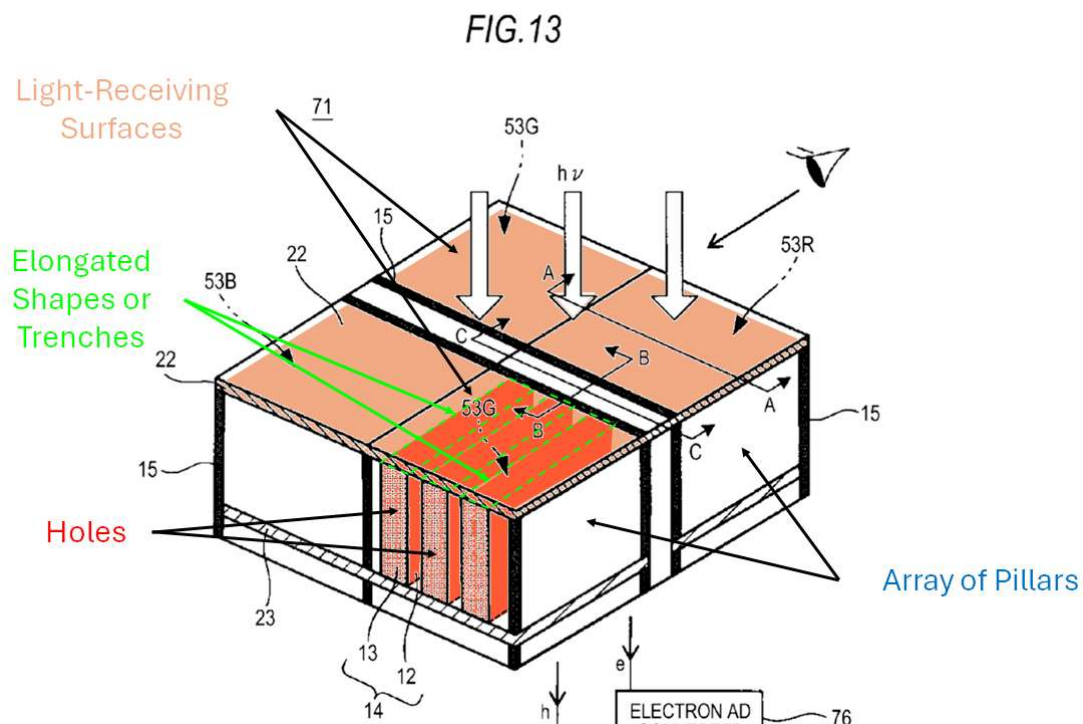
4. Claims 3, 4, 7, 8, and 15:

- a. [3]: “The integrated structure of claim 2, wherein each of at least some of said **photodetectors** includes at least one of said **holes** with **elongated shapes** at the **light-receiving surface** thereof.
- b. [4]: “The integrated structure of claim 2, wherein each of at least some of said **photodetectors** includes a plurality of said **holes** with **elongated shapes** at the **light receiving surface** thereof.”
- c. [7]: “The integrated structure of claim 1, wherein each of at least some of said **photodetectors** includes at least one of said **holes** with **elongated shapes** at the **light receiving surface** thereof.”
- d. [8]: “The integrated structure of claim 1, wherein each of at least some of said **photodetectors** includes a plurality of said **holes** with **elongated shapes** at the **light receiving surface** thereof.”
- e. [15]: “The integrated structure of claim 1, wherein at least some of said **holes** are configured as **elongated trenches** at said **light-receiving surfaces**.”

Kuboi discloses these additional limitations. Lebbby, ¶¶182-185. Each **pillar** in the **array of pillars** in *Kuboi*’s integrated structure is a **photodetector**. VI.A.2.b ([1a]). Claims 3, 4, 7, and 8 recite “*each of at least some of* said photodetectors includes [at least one/a plurality] of said holes with elongated shapes” (emphases added). The term “said photodetectors” refers to claim 1’s recitation of “at least *some* of the photodetectors comprise P-doped and N-doped regions and regions therebetween” (emphasis added). At least some of *Kuboi*’s **photodetectors** (i.e.,

pixels 53R and 53G) include P-doped and N-doped regions and regions therebetween. Lebbby, ¶183. And each pixel 53R and 53G includes a plurality of holes having elongated shapes. Lebbby, ¶183.

As discussed for claim [1c] and shown below, *Kuboi* discloses forming stripe shaped **holes** (or **trenches**) having **elongated shapes** in the **light-receiving surfaces** of its **pixels** (i.e., 53R and 53G). VI.A.2.d; *Kuboi*, ¶¶[72], [13]-[14], [67], [95]; Lebby, ¶184.



Kuboi, Fig. 13. As discussed for claim [1c], *Kuboi*'s imaging device includes a plurality of pixels (i.e., 53R and 53G) that have structures similar to the 53G pixel shown above. VI.A.2.d. Further, as illustrated above and as discussed for claim [1c], *Kuboi*'s imaging device has a plurality of pixels 53R and 53G (i.e.,

pillars), that include one or more holes (“at least one,” “at least some,” or “a plurality of holes”), having elongated shapes (or are in the form of elongated trenches) formed at the light-receiving surfaces of the respective pillars (i.e., photodetectors). VI.A.2.d; Lebbby, ¶185.

5. Claims 6 and 10:

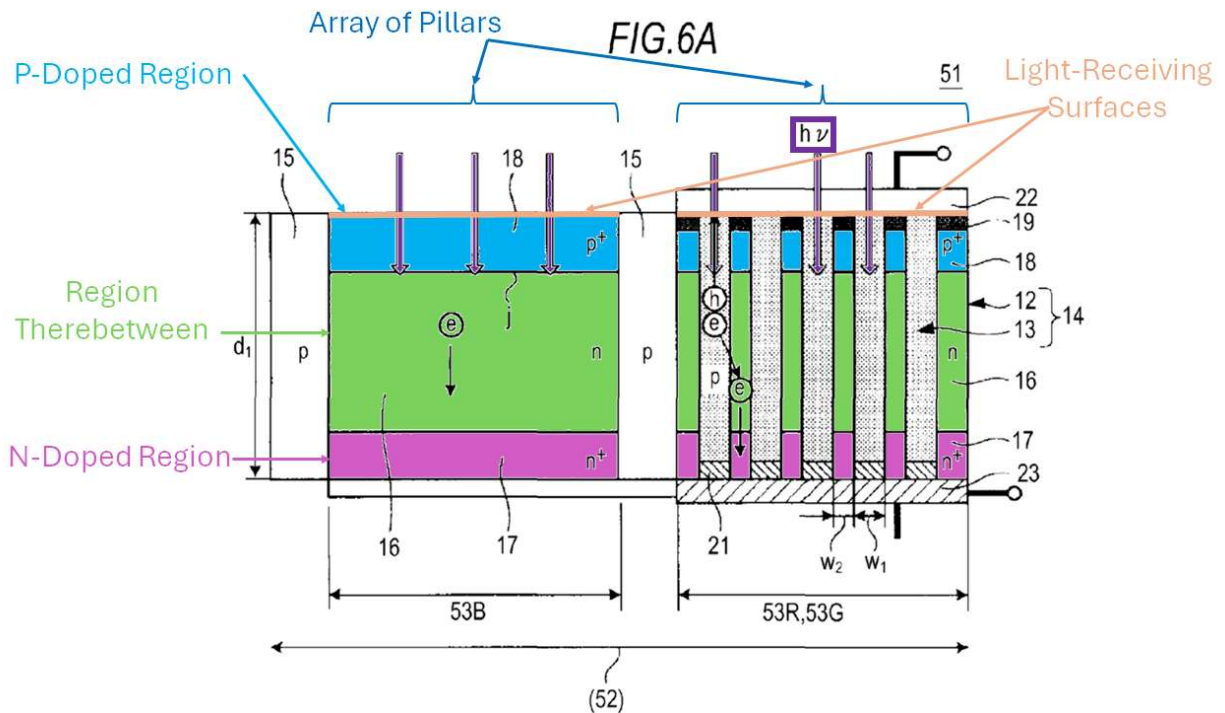
- a. [6] “The integrated structure of claim 2, in which said regions that are between the P-doped and N-doped regions are less doped than at least one of the P-doped and N-doped regions or are undoped.”
- b. [10] “The integrated structure of claim 1, in which said regions between the P-doped and N-doped regions are undoped or less doped than at least one of the P-doped and N-doped regions.”

Kuboi discloses these additional limitations. Lebbby, ¶¶186-188. *Kuboi*’s “semiconductor layer 12 is implanted with impurities.” *Kuboi*, ¶[56]. The process of implanting impurities into silicon material is known as “doping.” VI.A.2.c ([1b]). Semiconductor layer 12 includes “n⁺-type semiconductor region 17 having higher concentration [of impurities] than n-type semiconductor region 16.” *Kuboi*, ¶[56]. Semiconductor layer 12 also includes “semiconductor region 18 of second conductivity type (for example, p⁺ type) having higher concentration [of impurities] than n-type semiconductor region 16.” *Id.* Thus, *Kuboi* discloses that both its P-doped region (region 18) and N-doped region (i.e., region 17) have a higher doping concentration than the region therebetween (i.e., region 16). Lebbby,

¶¶187-188. The region between (i.e., region 16) the P-doped region (region 18) and N-doped region (region 17) is thus doped less than *Kuboi*'s P-doped region and N-doped region. Lebbby, ¶188.

6. **Claim 11: “The integrated structure of claim 10, in which the P-doped regions and N-doped regions are configured such that either the P-doped regions intercept said light before the N-doped regions or the N-doped regions intercept the light before the P-regions.”**

Kuboi discloses this additional limitation. Lebbby, ¶¶189-191. *Kuboi*'s imaging device includes “a blue (B) pixel 53B, a red (R) pixel 53R, a green (G) pixel 53G, and a green (G) pixel 53G ... arranged in a two-dimensional array.” *Kuboi*, ¶[90]; VI.A.2.b ([1a]). Each pixel 53B, 53R, and 53G has a P-doped region 18, region 16, and N-doped region 17 formed in that order from the light-receiving surface of the semiconductor layer 12 toward the opposite surface. *Kuboi*, ¶[91]; VI.A.2.c ([1b]). Thus, as illustrated below, in blue pixel 53B, P-doped region 18 intercepts light $h\nu$ (light photons incident on said array of pillars) before N-doped region 17. Lebbby, ¶¶190-191.

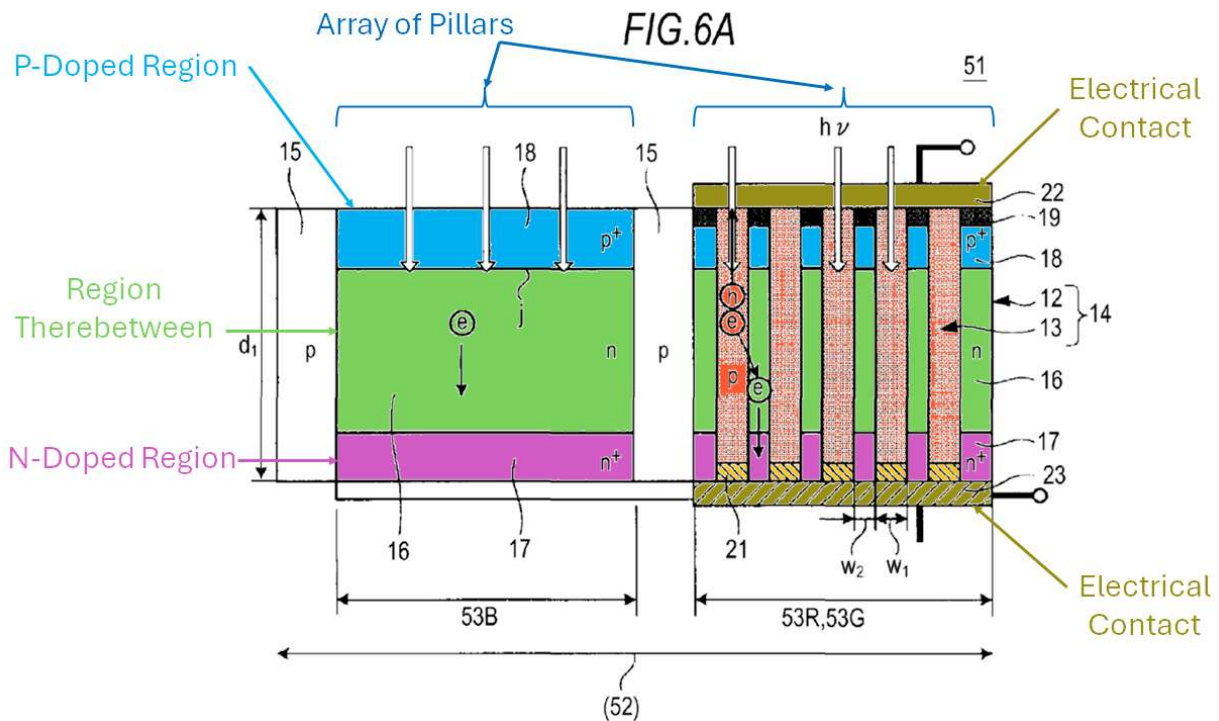


Kuboi, Fig. 6A.

7. **Claim 12:** “The integrated structure of claim 1, in which said **electrical contacts** are configured to provide electrical fields across at least some of said **photodetectors**.”

Kuboi discloses this additional limitation. Lebbby, ¶¶192-194. *Kuboi*’s electrodes 22 and 23 are “electrical contacts.” VI.A.2.g ([1f]). “[E]lectrodes 22 and 23 [are] formed on the entire rear and [front] surfaces of the semiconductor layer 12.” *Kuboi*, ¶¶[60], [77], [93], [103]. A necessary voltage is applied between upper and lower electrodes 22, 23 so that p⁺-type region 18 is at a negative potential and n⁺-type region 17 is at a positive potential. *Kuboi*, ¶¶[64], [87]. As illustrated below, because electrodes 22 and 23 are positioned on opposite sides of

photodetectors (pixel 53G, 53R), the voltage applied between electrodes 22, 23 provides an electric field across those photodetectors. Leiby, ¶¶193-194.

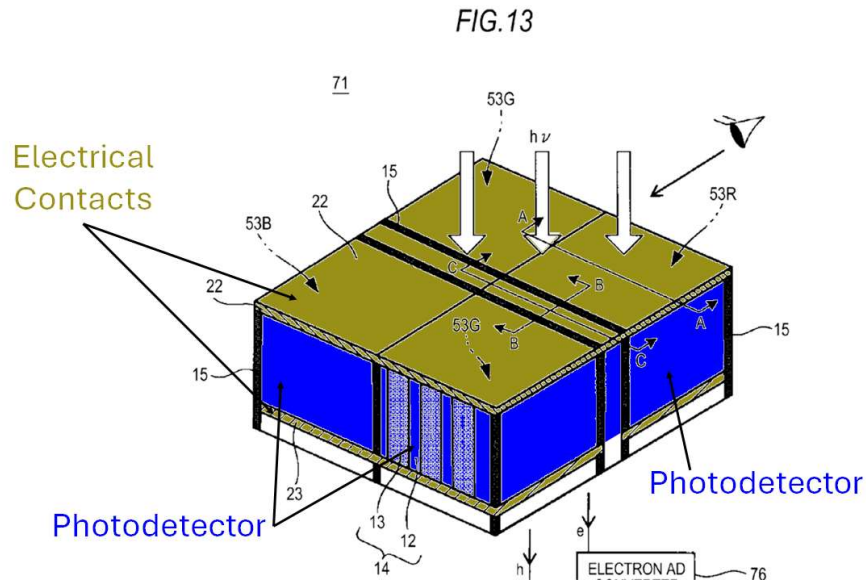


Kuboi, Fig. 6A.

8. **Claim 13:** “The integrated structure of claim 1, in which two or more of said photodetectors share at least some of said electrical contacts.”

Kuboi discloses this additional limitation. Leiby, ¶¶195-196. Kuboi’s electrodes 22 and 23 are “electrical contacts.” VI.A.2.g ([1f]). Kuboi’s “electrodes 22 and 23 [are] formed on the entire rear and [front] surfaces of the semiconductor layer 12.” Kuboi, ¶[60]. Because electrodes 22 and 23 are formed on the entire rear and front surfaces and cover more than one pixel (which is a photodetector, VI.A.2.b ([1a])), more than one photodetector shares electrodes 22

and 23 (electrical contacts). Leiby, ¶196. For example, as illustrated below, at least pixels 53B and 53G share electrical contacts 22 and 23:



Kuboi, Fig. 13.

9. **Claim 14: “The integrated structure of claim 1, wherein said SI electronic devices include devices for signal processing and transmission.”**

Kuboi discloses this additional limitation.⁴ Leiby, ¶¶197-200. *Kuboi*’s imaging device “include[s] a pixel region (so-called ... imaging region) 203 and a

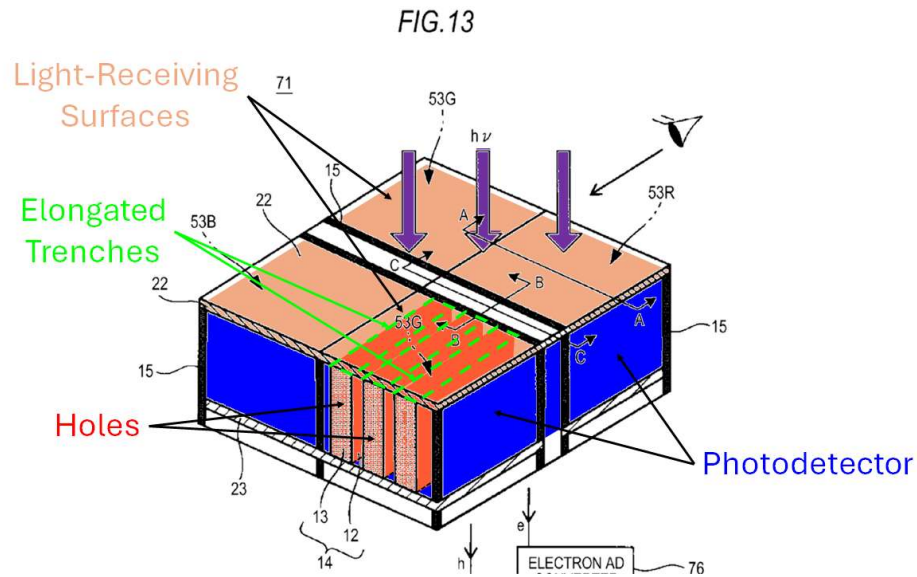
⁴ Claim 14 depends from claim 1, and claim 1 does not recite “SI electronic devices” or otherwise provide an antecedent basis. Nevertheless, Petitioner’s analysis assumes that claim 1 provides an antecedent basis for “SI electronic devices.”

peripheral circuit portion which are provided on a semiconductor substrate 211

(i.e., a silicon substrate).” *Kuboi*, ¶[48]. *Kuboi*’s “peripheral circuit portion is configured to include so-called logical circuits, for example, a vertical driving circuit 204, column signal processing circuits 205, a horizontal driving circuit 206, an output circuit 207, a control circuit 208, and the like,” such as input/output terminal 212. *Kuboi*, ¶[49]. *Kuboi*’s column signal processing circuits are the claimed signal processing circuits, and *Kuboi*’s output circuit and input/output terminal are the claimed signal transmission circuits. Lebbby, ¶¶198-200 (citing Ex-1076, 3, 10-11). These circuits include Si electronic devices because they include electronic devices formed on a silicon substrate. Lebbby, ¶200.

10. **Claim 16: “The integrated structure of claim 15, in which at least some of said elongated trenches have widths at said light-receiving surfaces no greater than a wavelength of the visible and/or infrared light illuminating said photodetectors.”**

Kuboi discloses this additional limitation. Lebbby, ¶¶201-204. As illustrated below, *Kuboi*’s integrated structure includes holes configured as elongated trenches at the light-receiving surface in its photodetectors. VI.A.2.d, VI.A.4 ([1c], [3], [4], [7], [8], [15]).



Kuboi, Fig. 13.

Kuboi also discloses that, as shown below, width **w1** of photoelectric conversion films 13, and therefore of **holes 38**, is 200 nm. *Kuboi*, ¶[94]; VI.A.2.h ([1g]).



FIG. 6A

Light-Receiving Surfaces

- Holes

Kuboi, Fig. 6A. **Visible light** wavelength ranges between 400-700 nm and **infrared**

light has wavelengths greater than 750 nm. Lebbby, ¶¶203-204 (citing Ex-1012, 4;

$Yu, \P[23]$). Thus, the width of 200 nm of the holes or elongated trenches in the

light-receiving surface of *Kuboi's* photodetectors is less than a wavelength of the

visible and/or infrared light illuminating the photodetectors. Lebbby, ¶204.

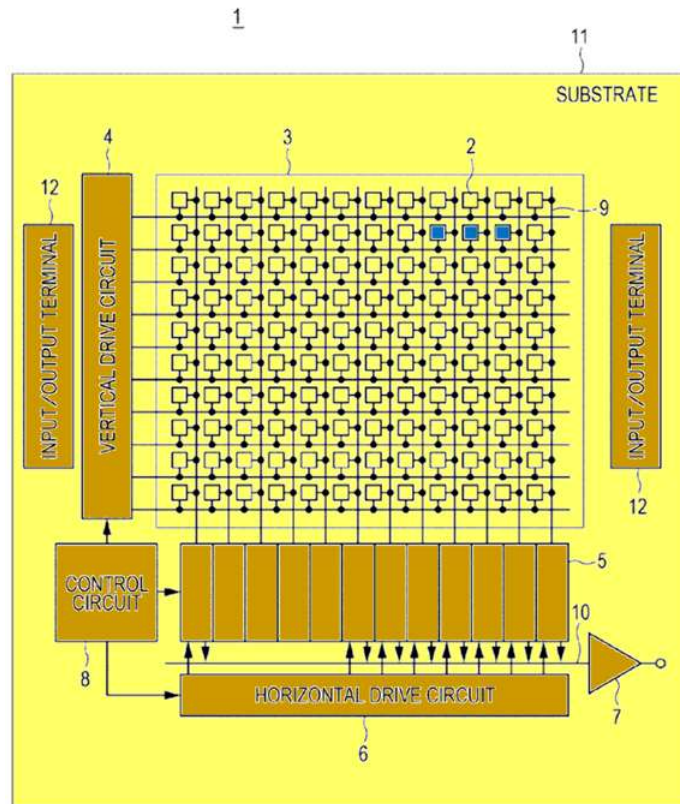
B. Claims 1-4, 6-8, 10-16, and 18 Are Obvious Over *Kuboi* in View of *Shinohara* (Ground 2)

1. Overview of *Shinohara*

Shinohara discloses “a solid-state imaging device which suppresses the generation of white spots and dark current and the occurrence of color mixture and which improves the sensitivity.” *Shinohara*, ¶[13]. *Shinohara* discloses “one

example of a MOS solid-state imaging device.” *Shinohara*, ¶[51]. Solid-state imaging device 1 “includes a pixel region (so-called imaging region) 3 in which a plurality of pixels 2 each having a photoelectric conversion portion is regularly arranged in a semiconductor substrate 11, such as a silicon substrate, in a two-dimensional matrix and a peripheral circuit portion.” *Id.* *Shinohara* discloses forming a pixel region, a peripheral circuit portion, pixel transistors, and a wiring layer *on the same substrate*. *Shinohara*, ¶¶[68]-[89]. “The peripheral circuit portion includes so-called logic circuits, such as a vertical drive circuit 4, a column signal processing circuit 5, a horizontal drive circuit 6, an output circuit 7, and a control circuit 8.” *Shinohara*, ¶[52]; *Lebby*, ¶¶83-88. These features are illustrated below:

FIG. 1



Shinohara, Fig. 1.

2. Motivation to modify *Kuboi's* imaging device in view of *Shinohara's* teaching of monolithic integration

Kuboi and *Shinohara* are analogous art to the '871 Patent because, like the '871 Patent, *Kuboi* and *Shinohara* also aim to improve the light absorption efficiency of their respective imaging devices. Lebbby, ¶216. The '871 Patent is directed to techniques for enhancing photon absorption. '871 Patent, Abstract. Similarly, *Kuboi* is directed to a solid-state imaging device in which light absorption efficiency is increased to improve sensitivity. *Kuboi*, ¶[9]. Likewise, *Shinohara* discloses a solid-state imaging device that improves sensitivity by

improving a pixel's light absorption, thereby reducing leakage of charge into an adjacent pixel. *Shinohara*, ¶¶[12]-[13]; Lebbby, ¶216.

A POSITA would have been motivated to implement *Shinohara*'s teaching of monolithic integration of the array of pillars (or pixels) with electronic circuits that include active elements for signal processing and transmission with *Kuboi*'s imaging device. Lebbby, ¶217. Indeed, the integration of photodetectors and signal processing circuitry on a single substrate to form a single-chip device was known long before the purported invention date. Lebbby, ¶¶57-65.

Kuboi discloses forming a pixel region and a peripheral circuit portion, including logic circuits, input and output circuits, and a control circuit on a substrate. *Kuboi*, ¶¶[48]-[49], [69], [78]. This substrate “may be created in advance and be bonded to the semiconductor substrate on which the semiconductor region 25 having the pixel transistors, the multilayer wiring layer 32, the lower electrode 23, and the like are formed.” *Kuboi*, ¶[78]. *Shinohara* discloses forming a pixel region, a peripheral circuit portion, pixel transistors, and a wiring layer *on the same substrate*. *Shinohara*, ¶¶[68]-[82]. Lebbby, ¶217.

A POSITA would have understood that including the pixel region, peripheral circuit portion, pixel transistors, and wiring layer on the same substrate (i.e., monolithically integrating) provides several advantages. Lebbby, ¶218. For example, monolithically integrating the pixel region and electronic circuits for

signal processing and transmission on the same substrate reduces noise and attenuation of the photoelectric signal generated by the pixel region by shortening the signal travel path in the modified device. *Hasegawa*, ¶[9]; Lebbby, ¶¶218-219. Furthermore, such monolithic integration reduces manufacturing costs and package size. Lebbby, ¶219 (citing *Hasegawa*, ¶[9]; *Michel*, Abstract; *Beals*, 2; *NXP*, ¶¶[16], [32], [37]).

A POSITA therefore would have been motivated to use *Shinohara*'s monolithic integration method to manufacture and further improve *Kuboi*'s imaging device. Lebbby, ¶220. A POSITA would have found that using *Shinohara*'s monolithic integration in *Kuboi* involves nothing more than the use of a known technique—forming the pixel region and all associated electronic circuitry on the same substrate—to improve a similar device—*Kuboi*'s imaging device—in the same way, namely, by improving manufacturing reliability, reducing manufacturing cost and package size, reducing signal attenuation, reducing noise, and improving high-bandwidth performance of *Kuboi*'s device. *Id.*

A POSITA would have had a reasonable expectation of success in using *Shinohara*'s teachings to manufacture *Kuboi*'s imaging device. Lebbby, ¶221. Given that both *Kuboi* and *Shinohara* disclose similar imaging devices that include a pixel region and a peripheral circuit portion, manufacturing *Kuboi*'s pixel region and associated electronic circuitry, including *Kuboi*'s pixel transistors, using

Shinohara's techniques would have been well within a POSITA's skill. *Id.* A POSITA would have had a reasonable expectation of success for the *Kuboi-Shinohara* combination because it merely requires combining well-known prior elements and manufacturing methods already taught by *Shinohara*. *Id.*; *In re Inland Steel Co.*, 265 F.3d 1354, 1364 (Fed. Cir. 2001).

3. Independent Claim 1

a. [1pre]-[1d], [1f], [1g]

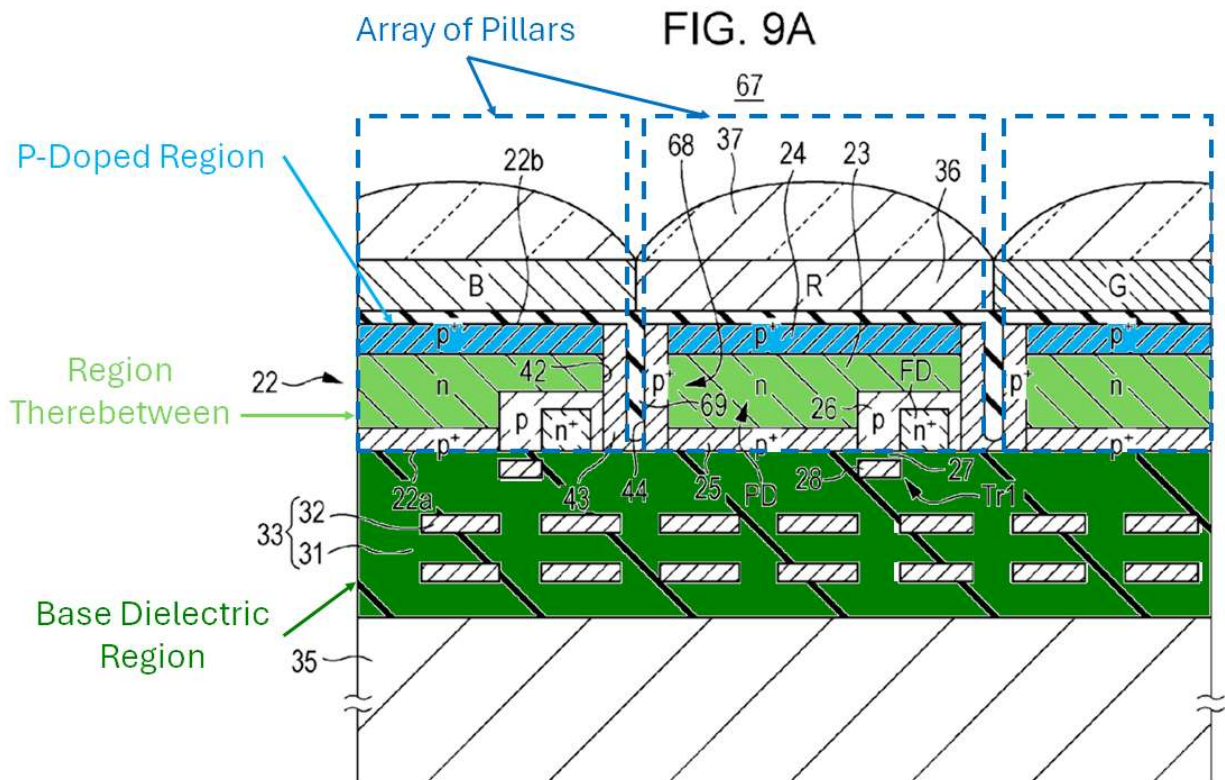
Kuboi discloses or renders obvious these limitations. VI.A.2.a-VI.A.2.e ([1pre]-[1d]), VI.A.2.g ([1f]), VI.A.2.h ([1g]); Lebbby, ¶205.

b. [1e]

Kuboi in view of *Shinohara* renders obvious [1e]. Lebbby, ¶¶206-210. *Kuboi* discloses a semiconductor substrate that includes semiconductor region 25 with a multilayer wiring layer 32 that includes a plurality of layers of wirings with interlayer insulating film 31 disposed between the wirings. *Kuboi*, ¶¶[61]-[62], [69]; VI.A.2.f ([1e]). Further, *Kuboi* discloses bonding the silicon semiconductor substrate with pixels to the semiconductor substrate 25 that includes multilayer wiring layer 32 with interlayer insulating film 31, with insulating film 30 disposed between the substrate with the pixels and semiconductor substrate 25. *Kuboi*, ¶¶[70], [61]-[62], [69]. Thus, *Kuboi* discloses bonding a first substrate, including

insulating film 31 with a second substrate including *Kuboi's* image sensor and peripheral circuits to form its imaging device. Lebbby, ¶207.

Shinohara discloses forming multilayer wiring layer 33, including wires 32 and interlayer insulating film 31, on the same substrate 22 on which pixels B, R, G are formed. *Shinohara*, ¶¶[82], [68]-[89]; VI.B.1. *Shinohara*'s interlayer insulating film 31 is a base dielectric region because it is disposed at the base of *Shinohara*'s pixels B, R, G. *Shinohara*'s base dielectric region is illustrated below.



Shinohara, Fig. 9A; Lebbby, ¶208.

Although *Shinohara* does not disclose the material used to make its semiconductor **insulating films (30 and/or 31)**, a POSITA would have understood

that insulating films for separating wires from each other or from an electrical contact, like *Kuboi*'s *insulating films 30* or *31*, or *Shinohara*'s *insulating film 31* constitute silicon oxide or silicon nitride, which are dielectric materials, or at least would have been motivated to use silicon oxide or silicon nitride because these materials can be fabricated using standard silicon fabrication processes and because these materials provide good barriers to impurity and moisture diffusion. Leiby, ¶209 (citing Ex-1020, 34-35; Ex-1059, ¶¶[13]-[14]; Ex-1063, 4-5, 20-21, 23, 34). Thus, a POSITA would have found it obvious to form *Shinohara*'s *insulating film 31* (i.e., *base dielectric material*) of a solid dielectric material like silicon oxide or silicon nitride. *Id.* A POSITA would also have a reasonable expectation of success in making *Shinohara*'s *insulating film 31* with a solid dielectric material because methods of formation with such materials in semiconductor fabrication were well known in the art before the '871 Patent. *Id.* (citing Ex-1020, 34-35; Ex-1063, 20-21, 23).

As explained above, a POSITA would have found it obvious to modify *Kuboi* in view of *Shinohara* to form the *Kuboi-Shinohara* integrated structure⁵ in which *Kuboi*'s array of pillars (i.e., *photodetectors*) and *Si electronic devices* are

⁵ The Petition refers to *Kuboi*'s integrated structure as modified by *Shinohara*'s teachings as the *Kuboi-Shinohara* integrated structure.

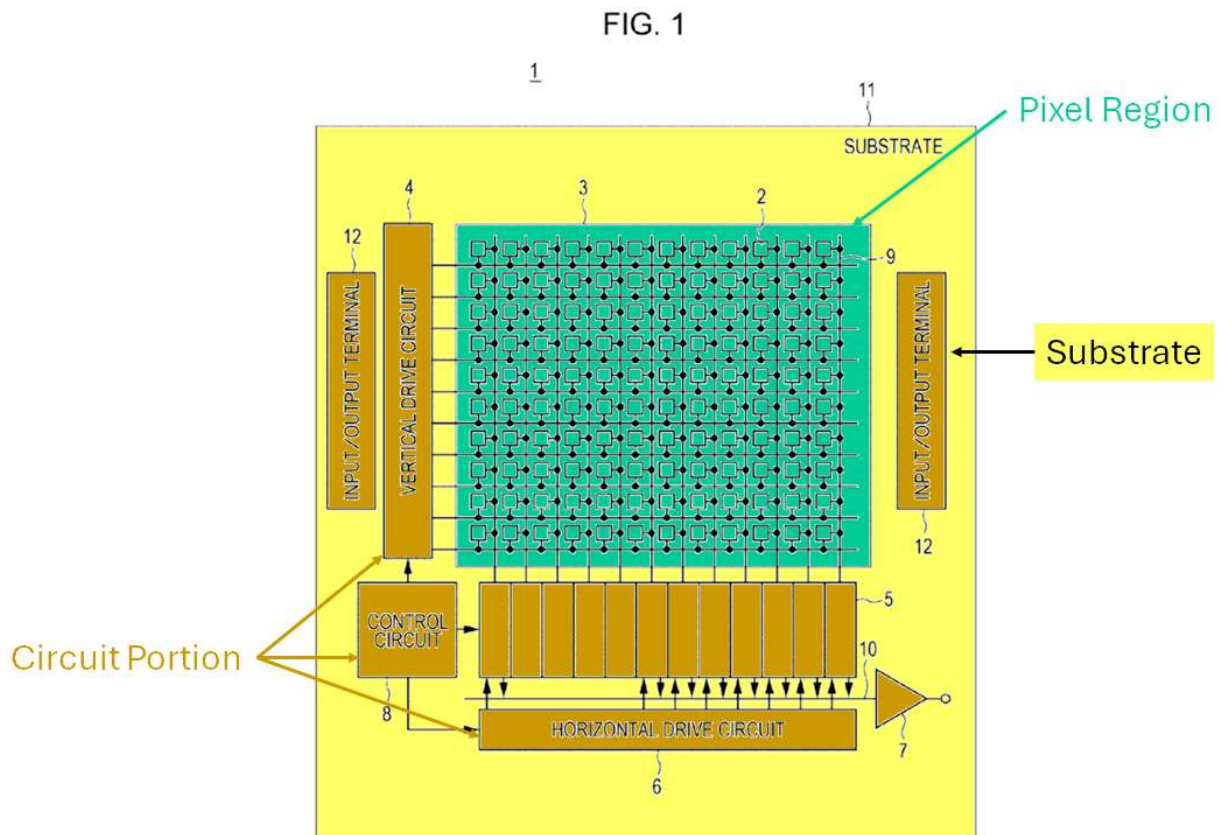
formed on the same substrate. VI.B.2. A POSITA would have also understood that applying *Shinohara*'s monolithic integration to form the *Kuboi-Shinohara* integrated structure would result in forming *Kuboi*'s insulating film 30 and interlayer insulating film 31 to be formed on the same substrate as *Kuboi*'s array of pillars (i.e., photodetectors). Leiby, ¶210. A POSITA would have further understood that in the *Kuboi-Shinohara* integrated structure, *Kuboi*'s insulating films 30 and 31 would be disposed below *Kuboi*'s array of pillars as illustrated in *Kuboi*'s Figure 1A. *Id.* Moreover, because *Kuboi*'s insulating films 30 and 31 are made of solid dielectric material, *Kuboi*'s insulating film 30 and/or 31 would form the claimed base dielectric region below *Kuboi*'s array of pillars in the *Kuboi-Shinohara* integrated structure. *Id.*

4. Claim 2

Kuboi in view of *Shinohara* (Ground 2) renders obvious this additional limitation. Leiby, ¶¶211-222. *Shinohara*'s imaging device includes “a pixel region (so-called imaging region) 3 in which a plurality of pixels 2 each having a photoelectric conversion portion is regularly arranged in a semiconductor substrate 11, such as a silicon substrate, in a two-dimensional matrix and a peripheral circuit portion.” *Shinohara*, ¶[51]; VI.B.1. *Shinohara* discloses a method for manufacturing the imaging device on a “p-type silicon semiconductor substrate 22.” *Shinohara*, ¶[68]. *Shinohara* teaches forming the photodiodes and

the separation regions between the photodiodes on the imaging device on a “p-type silicon semiconductor.” *Shinohara*, ¶¶[69]-[81]. *Shinohara* also teaches that “the peripheral circuit portion ... is formed in the periphery of the pixel region.”

Shinohara, ¶[81]. These features are illustrated below.



Shinohara, Fig. 1; Lebbby, ¶¶212-214.

A POSITA would have understood that forming the **pixel region** (with **photodiodes**) and **peripheral circuit portion** on the same **silicon semiconductor substrate** would yield **photodetectors** monolithically integrated with a **Si electronic devices** (i.e., **devices** in the **peripheral circuit portion**). Lebbby, ¶215 (citing

Ex-1076, 3). As explained above, a POSITA would have found it obvious to combine *Shinohara*'s teachings with *Kuboi*, resulting in the *Kuboi-Shinohara* integrated structure in which the array of pillars (i.e., pixel region) is monolithically integrated with Si electronic devices. VI.B.2; Lebbby, ¶¶216-222.

5. Claims 3, 4, 6-8, and 10-16

As discussed above, *Kuboi* discloses the additional limitations in claims 3, 4, 6-8, and 10-16. VI.A.4-VI.A.10; Lebbby, ¶223. The *Kuboi-Shinohara* integrated structure prepared using *Shinohara*'s monolithic integration would include the features of *Kuboi* identified above for claims 3, 4, 6-8, and 10-16. *Id.* Thus, the *Kuboi-Shinohara* combination renders obvious claims 3, 4, 6-8, and 10-16. *Id.*

6. Claim 18: “The integrate[d] structure of claim 15, in which said array of photodetectors is monolithically integrated with Si electronic devices that include CMOS devices.”

As discussed above, the *Kuboi* and *Shinohara* combination renders these limitations obvious. VI.B.2, VI.B.4; Lebbby, ¶¶224-225. Specifically, *Kuboi* discloses a “CMOS solid-state imaging device” formed on a silicon substrate. *Kuboi*, ¶[48]. Similarly, *Shinohara* discloses a “CMOS Solid-State Imaging Device.” *Shinohara*, ¶[50]. Because both *Kuboi*'s and *Shinohara*'s imaging devices are CMOS devices, a POSITA would have understood that the circuits in both *Kuboi*'s and *Shinohara*'s logical/peripheral circuit portions would include CMOS devices. Lebbby, ¶225. A POSITA would have also understood that forming

Kuboi's photodetectors and Si electronic devices (VI.B.2, VI.B.4) on the same substrate based on *Shinohara*'s teachings, as discussed for claim [2], would yield an integrated structure that includes *Kuboi*'s array of photodetectors monolithically integrated with Si electronic devices that include CMOS devices. Leebby, ¶225.

C. Claims 1-4, 7-8, 15, 17, and 18 are Obvious Over *Yu* in view of *Kuboi* and *Shinohara* (Ground 3)

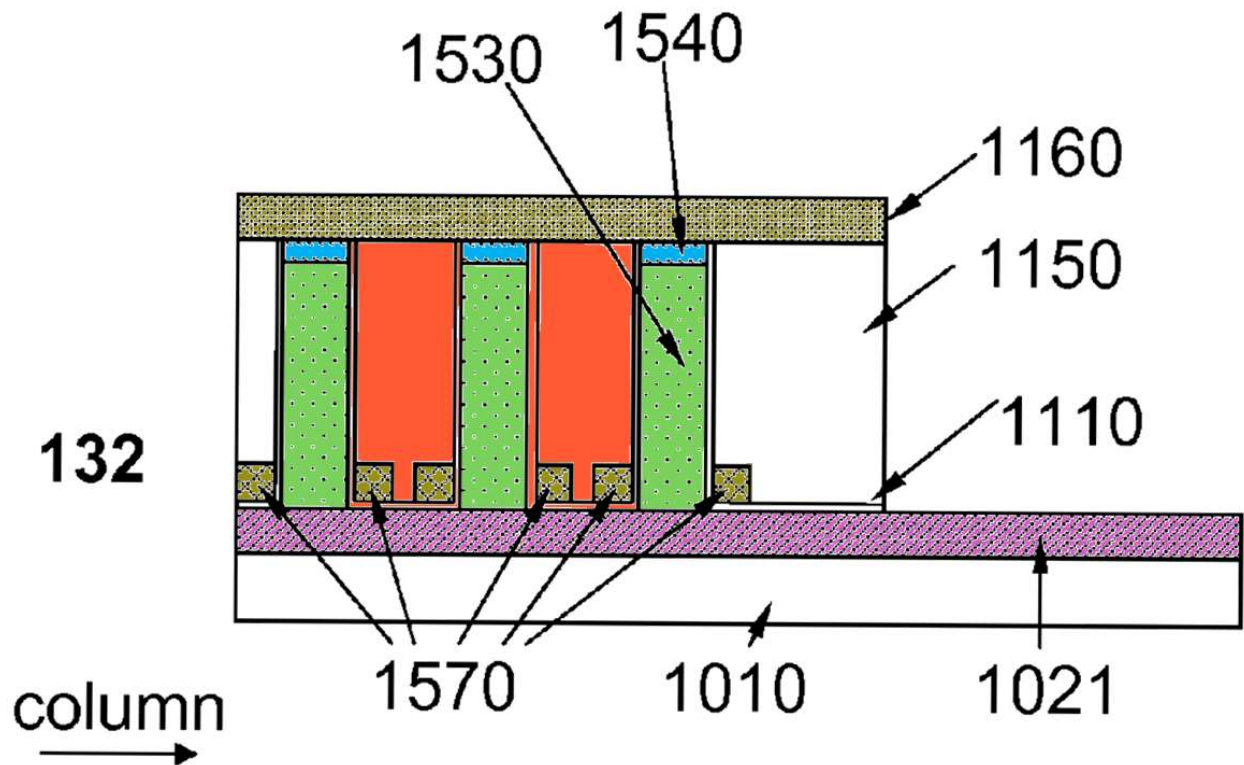
1. Overview of *Yu*

Yu's image sensor includes pixels having at least one nanopillar to convert light to electrical signals. *Yu*, Abstract, ¶[48]; Leebby, ¶¶89-94. *Yu*'s "image sensor and the control circuit can be formed as an integrated circuit or chip." *Yu*, ¶[115].

Yu's image sensor's pixels may include different size nanopillars, including a three-nanopillar pixel and a four-nanopillar pixel. *Yu*, ¶¶[130], [124], Figs. 7A-7B. "[T]he pixels are organized into a plurality of 'rows'" and the "pixels can be organized into a plurality of 'columns.'" *Yu*, ¶¶[51], [9], [17], [25], [48].

Yu's "nanopillars and the substrate can comprise suitable semiconductor materials and/or metals such as Si." *Yu*, ¶¶[55], [27]. The "substrate has an oxide layer 1010, a heavily doped layer (HDL) 1020 on the layer 1010 and an epi layer 1030 on the HDL layer 1020." *Yu*, ¶[62]. *Yu*'s "substrate can have the following doping profiles: (i) the HDL layer 1020 is p⁺ (i.e. heavily doped to p type), the epi layer 1030 is p⁻ (i.e. lightly doped to p type); [and] (ii) the HDL layer 1020 [is]

p+, the epi layer 1030 is i (i.e.,] intrinsic).” *Id.* “[E]pi layer 1030 can be about 3000 to 10000 nm thick.” *Id.* “[A] junction layer 1040 is formed on the epi layer 1030,” and that “junction layer 1040 is of the opposite conduction type as the HDL layer 1020, i.e.,] if the HDL 1020 is p type, the junction layer 1040 is n type.” *Yu*, ¶[63]. *Yu* discloses that “the exposed portion of the junction layer 1040 and the portion of the epi layer 1030 directly therebelow are deep etched until the HDL layer 1020 directly below the exposed portion of the junction layer 1040 is exposed, to form nanopillars 1500.” *Yu*, ¶¶[68], [76]. The deep etching produces holes between adjacent nanopillars. *Id.* *Yu* explains that the “portion of the metal layer 1140 deposited around the lower end of the nanopillars 1500 forms the gate electrodes and gate lines 1570.” *Yu*, ¶[85]. Further, “a transparent conductive layer (TCL) 1160, such as ITO or aluminum doped zinc oxide (AZO) is deposited by a suitable technique such sputtering.” *Yu*, ¶¶[89], [27], [53]. These features are illustrated below, including holes.



Yu, Fig. 1, step 132. *Yu* also discloses “a silicon-on-insulator (SOI)-type substrate or silicon-on-glass (SG)-type substrate is provided.” *Yu*, ¶¶[62], [15], [102].

2. Motivation to modify *Yu*’s integrated structure in view of *Kuboi*’s teaching of reverse bias

Like the ’871 Patent, *Yu* discloses an integrated structure having a plurality of pixels and a control circuit. *Yu*, Abstract, ¶¶[7], [17], [48], [52]; VI.C.4.a. *Yu* is analogous art to the ’871 Patent because, like the ’871 Patent, *Yu*’s image sensor also includes features to improve light absorption. *Yu*, ¶[133]; Lebbby, ¶261. As also discussed above, *Kuboi* is analogous art to the ’871 Patent. VI.B.2.

Kuboi discloses applying a reverse bias to a PIN photodetector. VI.A.2.g. A POSITA would have been motivated to implement *Kuboi*’s teaching of applying

reverse bias for operating *Yu*'s image sensor. Lebbby, ¶262. A POSITA would have understood that applying a reverse bias as taught by *Kuboi* would decrease the response time of the image sensor in the *Yu-Kuboi* integrated structure⁶ by more quickly sweeping charge carriers from the silicon material. Lebbby, ¶¶262-263 (citing Ex-1064, ¶[2]; Ex-1065, ¶[49]; Ex-1063, 13). Further, a POSITA would have been motivated to apply *Kuboi*'s reverse biasing teaching when operating the image sensor in *Yu*'s integrated structure to induce carrier multiplication and increase the image sensor's response speed. Lebbby, ¶264. A POSITA would have found that the combination involves the use of a known technique—applying a reverse bias—to improve a similar device—*Yu*'s integrated structure—in the same way, namely, by sweeping charge carriers towards the electrical contacts by applying a reverse bias across the contacts of *Yu*'s integrated structure. *Id.*

A POSITA would have had a reasonable expectation of success in implementing *Kuboi*'s teachings in *Yu*'s integrated structure. Lebbby, ¶265. Given that *Yu* and *Kuboi* disclose similar imaging devices, and both disclose applying bias voltages to the electrical contacts of their respective imaging devices, applying *Kuboi*'s reverse biasing to *Yu*'s image sensor would have been well within the skill

⁶ The Petition refers to *Yu*'s integrated structure as modified by *Kuboi*'s teachings as the *Yu-Kuboi* integrated structure.

of a POSITA. *Id.* A POSITA would have had a reasonable expectation of success combining *Yu* with *Kuboi* because it merely requires combining well-known prior elements already taught by *Yu* and *Kuboi*. *Id.*; *Inland Steel*, 265 F.3d at 1364.

3. Motivation to modify the *Yu-Kuboi* integrated structure in view of *Shinohara*'s teaching of monolithic integration

As discussed above, *Yu*, *Kuboi*, and *Shinohara* are analogous art to the '871 Patent. VI.C.2; VI.B.2. A POSITA would have been motivated to implement *Shinohara*'s teaching of monolithic integration of the array of pillars (or pixels) with Si electronic devices in manufacturing the *Yu-Kuboi* integrated structure (VI.C.2). Lebbby ¶¶282-283.

Shinohara discloses forming a pixel region, a peripheral circuit portion, pixel transistors, and a wiring layer on the same substrate. *Shinohara*, ¶¶[68]-[82]; VI.B.2. A POSITA would have understood that *Shinohara*'s monolithic integration lowers manufacturing costs, allows high bandwidth operation, improves power efficiency, and enables high-frequency mixed-signal processing. VI.B.2; Lebbby, ¶284. A POSITA therefore would have been motivated to use *Shinohara*'s monolithic integration teaching to manufacture the *Yu-Kuboi* integrated structure and achieve the above-identified benefits. *Id.* A POSITA would have also understood that adding *Kuboi*'s reverse biasing capability to *Yu*'s image sensor would not prohibit implementation of *Shinohara*'s monolithic integration teaching

to manufacture the *Yu-Kuboi* integrated structure. Leebby, ¶285. A POSITA would have found that the combination involved the use of a known technique—forming the pixel region and all associated electronic circuitry on the same substrate—to improve a similar device—the *Yu-Kuboi* integrated structure—in the same way, namely, by improving manufacturing reliability, reducing manufacturing cost, signal attenuation, and noise, and improving high-bandwidth performance of *Yu-Kuboi* integrated structure. *Id.*

A POSITA would have had a reasonable expectation of success in implementing *Shinohara*'s teachings for manufacturing the *Yu-Kuboi* integrated structure. Leebby, ¶286. Given that *Yu*, *Kuboi*, and *Shinohara* disclose similar imaging devices with pixels, manufacturing the pixels in the *Yu-Kuboi* integrated structure and associated electronic circuitry using *Shinohara*'s techniques would have been well within a POSITA's skill. *Id.* A POSITA would have had a reasonable expectation of success combining *Shinohara* with the *Yu-Kuboi* integrated structure because it requires combining well-known prior elements and manufacturing methods already taught by *Yu*, *Kuboi*, and *Shinohara*. *Id.*; *Inland Steel*, 265 F.3d at 1364.

4. Independent Claim 1

a. [1pre]

To the extent the preamble is limiting, *Yu* discloses it. Lebbby, ¶¶226-228. *Yu*'s apparatus comprises the image sensor and a **control circuit** that includes a decoder, a transimpedance amplifier, a multiplexer circuit, and other readout circuitry components. *Yu*, ¶[115]. *Yu*'s "image sensor and [] **control circuit** can be formed as an integrated circuit or chip." *Yu*, ¶[115]. *Yu*'s apparatus is an "**integrated structure**" because it combines various structures, for example, an image sensor and control circuit. Lebbby, ¶228. This is shown below:

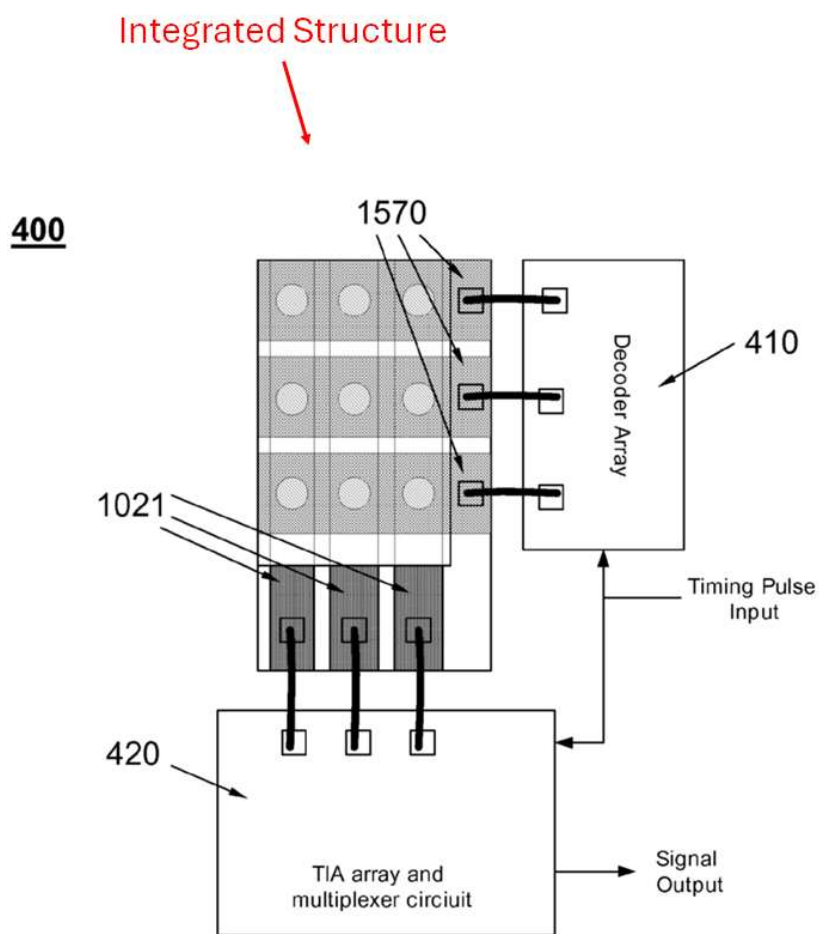


FIG. 4

Yu, Fig. 4.

b. [1a]⁷

Yu discloses [1a]. Lebbby, ¶¶229-237. *Yu*'s image sensor has a plurality of pixels. *Yu*, ¶¶[7], [17], [25]. *Yu*'s pixels “are organized into a plurality of ‘rows’” and “into a plurality of ‘columns.’” *Yu*, ¶¶[51], [9] (“image sensor can comprise first, second, third[,] and fourth pixels”), [17], [25], [48]. Each pixel “has at least a nanopillar that can convert light impinging thereon to electrical signals (e.g. a nanopillar having a vertical p-n or p-i-n junction).” *Yu*, ¶[48]. *Yu*'s pixels are photodetectors because they are “fabricated to absorb light in the ultraviolet (UV), visible (VIS)[,] or infrared (IR) regions and to generate a detectable electrical signal.” *Yu*, ¶¶[48], [52], [58]-[59], [131]-[132]; Lebbby, ¶¶230-231.

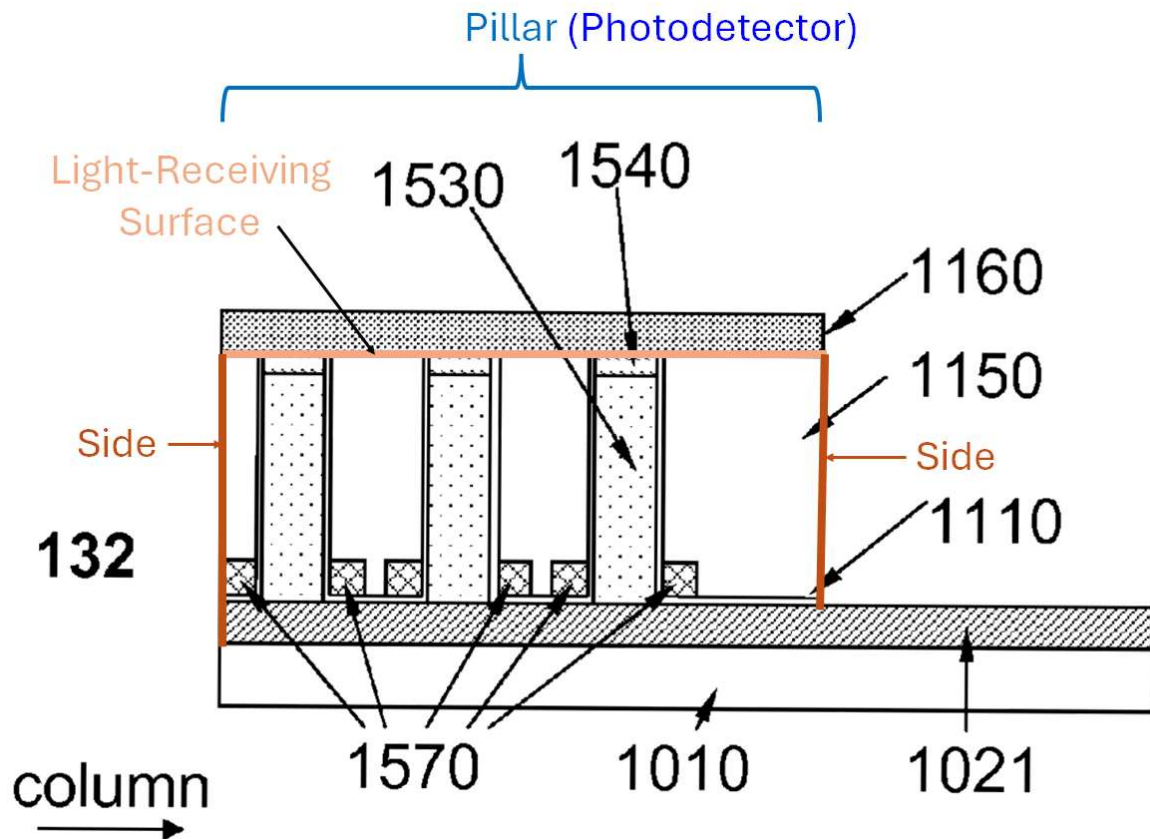
According to *Yu*, “each pixel has at least one nanopillar, which comprises a p-n or p-i-n junction extending in the length direction of the nanopillar.” *Yu*, ¶[52]. *Yu* discloses “an exemplary three-nanopillar pixel and an exemplary four-nanopillar pixel” that “may be incorporated into the image sensor.” *Yu*, ¶¶[130]-[132], Figs. 7A-7B; Lebbby, ¶232.

⁷ Petitioners' mapping of the '871 patent claims to *Yu*, including the terms “array of pillars” and “elongated trenches [that] crisscross” ([17]) is consistent with how Patent Owner maps the same claims to Petitioners' accused products in the parallel litigation. Ex-1075.

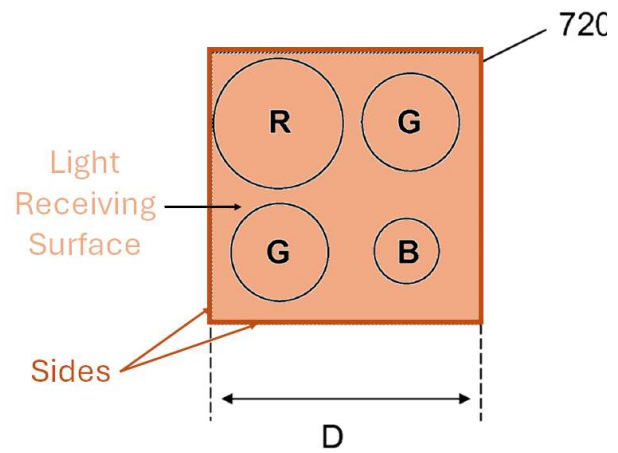
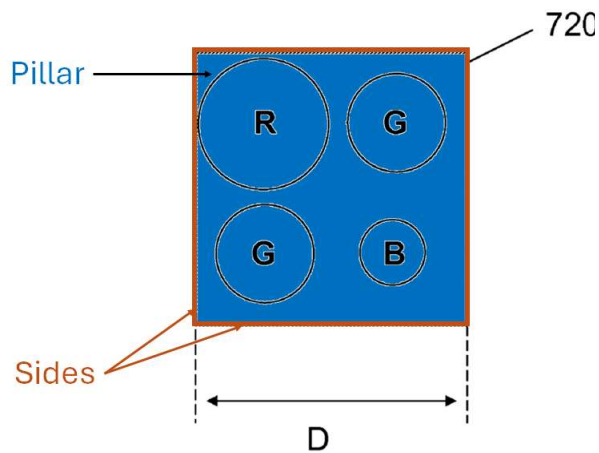
A POSITA would have understood that *Yu*'s "nanopillars" are not the claimed pillars. Lebbby, ¶233. Rather, *Yu*'s pixel is the claimed pillar and each such pixel may have more than one nanopillar. *Id.* Because *Yu*'s pixels can be arranged in rows and columns, *Yu* discloses an array of pixels (i.e., pillars). *Id.*

Yu's pixels include "nanopillars extending vertically from a substrate." *Yu*, ¶¶[48]-[49]. These "nanopillars and the substrate can comprise suitable semiconductor materials and/or metals such as Si." *Yu*, ¶¶[55], [15], [27], [62].

Yu also discloses planarizing an upper surface of oxide or polymer 1150 to expose junction layer 1540 of nanopillars 1500. *Yu*, ¶[88]. "[M]icro lenses can be fabricated on upper ends of the nanopillars 1500 to enhance light collection." *Yu*, ¶[95]. From this, a POSITA would have understood that the light-receiving surfaces of *Yu*'s pixels are at the upper ends of nanopillars 1500 (nearer to junction layer 1540) that receive light from the micro lenses. Lebbby, ¶¶234-235. *Yu*'s pillar with sides and a light-receiving surface is illustrated below:



Yu, Fig. 1, step 132. Yu's exemplary **pixel** (i.e., **pillar**), including multiple nanopillars, and having **sides** and a **light-receiving surface** is illustrated below (Lebby, ¶236):



Although only one **pillar** is illustrated in the above figures, because *Yu* discloses an **array of pillars**, a POSITA would have understood that each of *Yu*'s **pillars** would have a **light-receiving surface** and **sides** similar to the one illustrated above. Lebbby, ¶237.

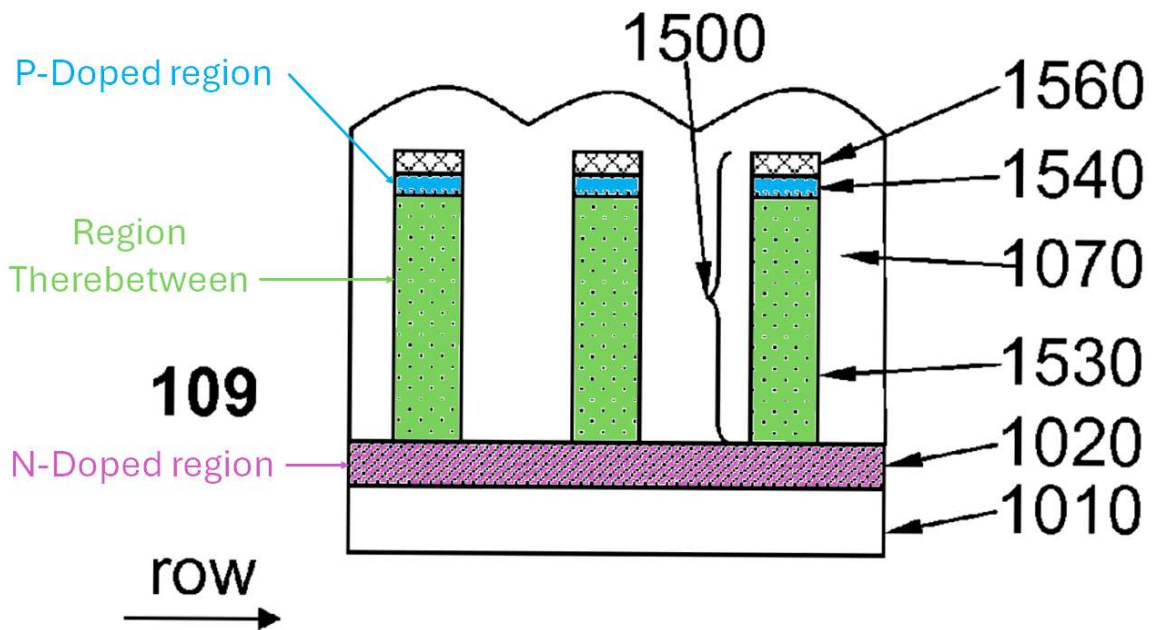
c. [1b]

Yu discloses [1b]. Lebbby, ¶¶238-242. As discussed for [1a], *Yu* discloses an **array of pixels** (or **pillars**), each of which is a **photodetector** and has multiple nanopillars. VI.C.4.b; Lebbby, ¶239.

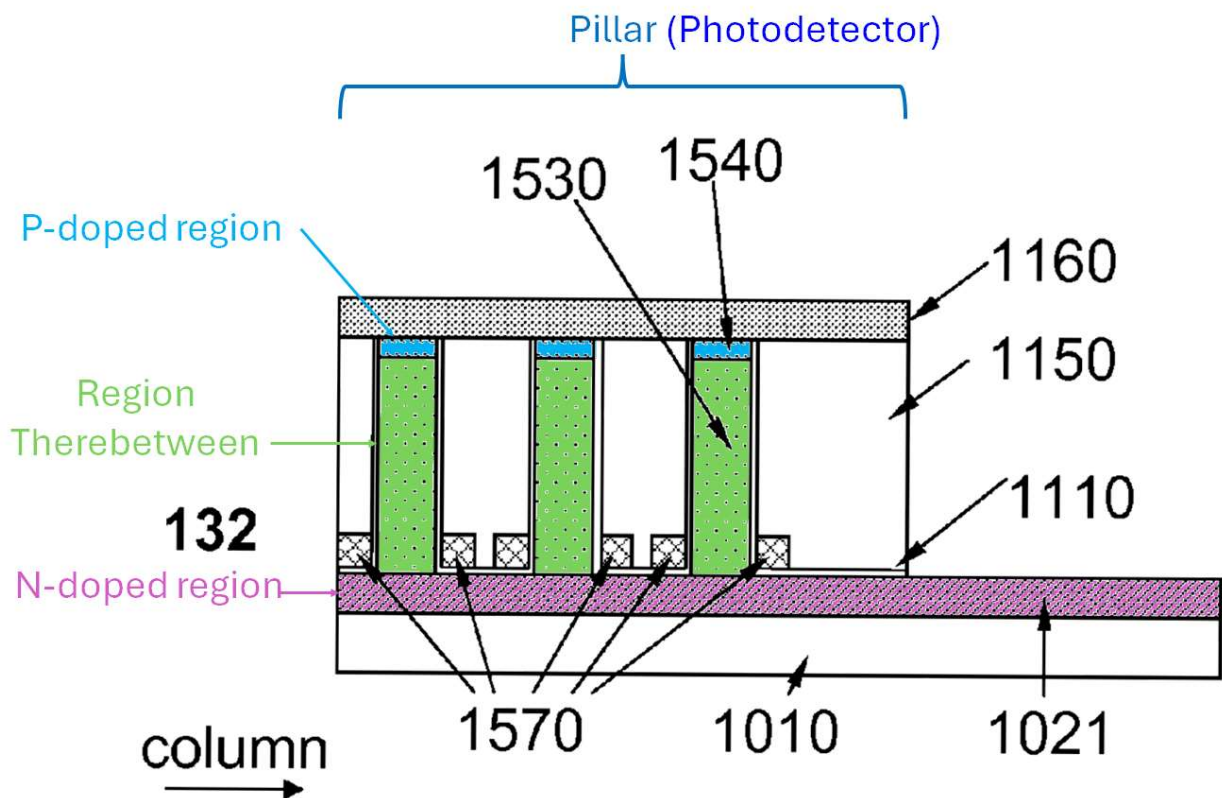
As also discussed, *Yu*'s “nanopillars and the substrate can comprise suitable semiconductor materials and/or metals such as Si.” VI.C.4.b; *Yu*, ¶¶[55], [27]. *Yu*'s “substrate has an oxide layer 1010, a **heavily doped layer (HDL) 1020** on the layer

1010[,] and an epi layer 1030 on the HDL layer 1020.” Yu, ¶[62]. Yu explains that HDL layer 1020 is segmented into readout lines 1021. Yu, ¶[76]. Yu discloses that “junction layer 1040 is formed on the epi layer 1030.” Yu, ¶[63]. Because the epi layer is formed on the HDL layer and because the junction layer is formed on the epi layer, Yu’s epi layer located between the junction layer and HDL layer forms the regions therebetween. Lebbby, ¶240.

Yu’s substrate can have the following doping profile: “the HDL layer 1020 is n-[and] the epi layer 1030 is i” (i.e. intrinsic). Yu, ¶[62]. and that “if the HDL 1020 is n type, the junction layer 1040 is p type.” Yu, ¶[63]. The figures below illustrate “junction layer 1540 which is part of the junction layer 1040” (Yu, ¶[68], i.e., “P-doped region”), intrinsic epi layer (i.e., “region therebetween”), and HDL 1020 (i.e., N-doped region). Lebbby, ¶¶240-241.



Yu, Fig. 1, step 109.

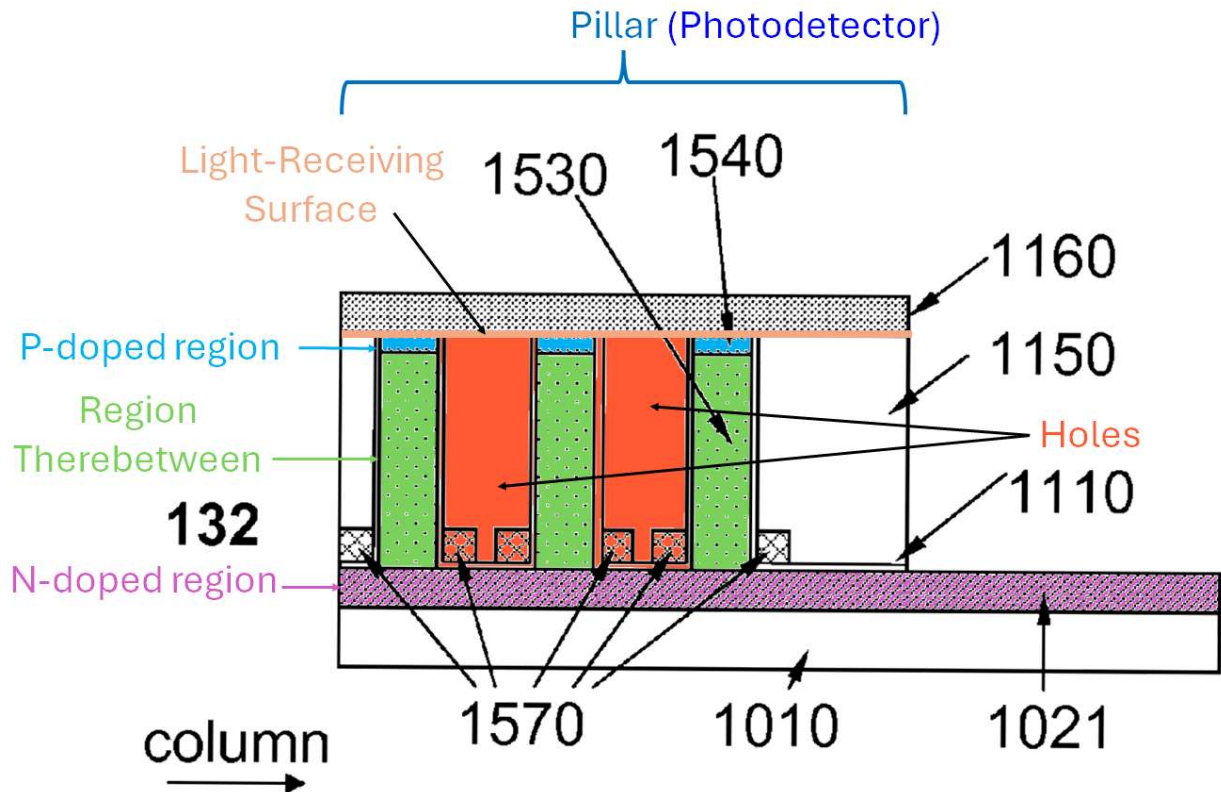


Yu, Fig. 1, step 132.

Each pixel “has at least a nanopillar that can convert light impinging thereon to electrical signals.” *Yu*, ¶¶[48], [17]. *Yu*’s pixels are “fabricated to absorb light in the ultraviolet (UV), visible (VIS)[,] or infrared (IR) regions and to generate a detectable electrical signal in response thereto.” *Yu*, ¶[48]. Thus, *Yu*’s pixels (i.e., photodetectors) are configured to convert light in selected visible and infrared wavelength ranges incident on said array of pillars into electrical signals (i.e., “electric charge carriers”). Lebbby, ¶242.

d. [1c]

Yu discloses or suggests [1c]. Lebbby, ¶¶243-251. *Yu* discloses starting with a substrate and forming an oxide layer, a heavily doped layer (HDL) on the oxide layer, and an epi layer on the HDL layer. *Yu*, ¶[62]. *Yu* also discloses forming a junction layer on the epi layer. *Yu*, ¶[63]. According to *Yu*, “the exposed portion of the junction layer 1040 and the portion of the epi layer 1030 directly therebelow are deep etched until the HDL layer 1020 directly below the exposed portion of the junction layer 1040 is exposed, to form nanopillars 1500.” *Yu*, ¶¶[68], [76]. The spaces between nanopillars are the holes, which are formed in the light-receiving surface of *Yu*’s pillar. Lebbby, ¶¶244-245. The holes are deliberately formed because they are formed by a purposeful deep-etch process. Lebbby, ¶¶246-247. *Yu*’s holes are illustrated below.

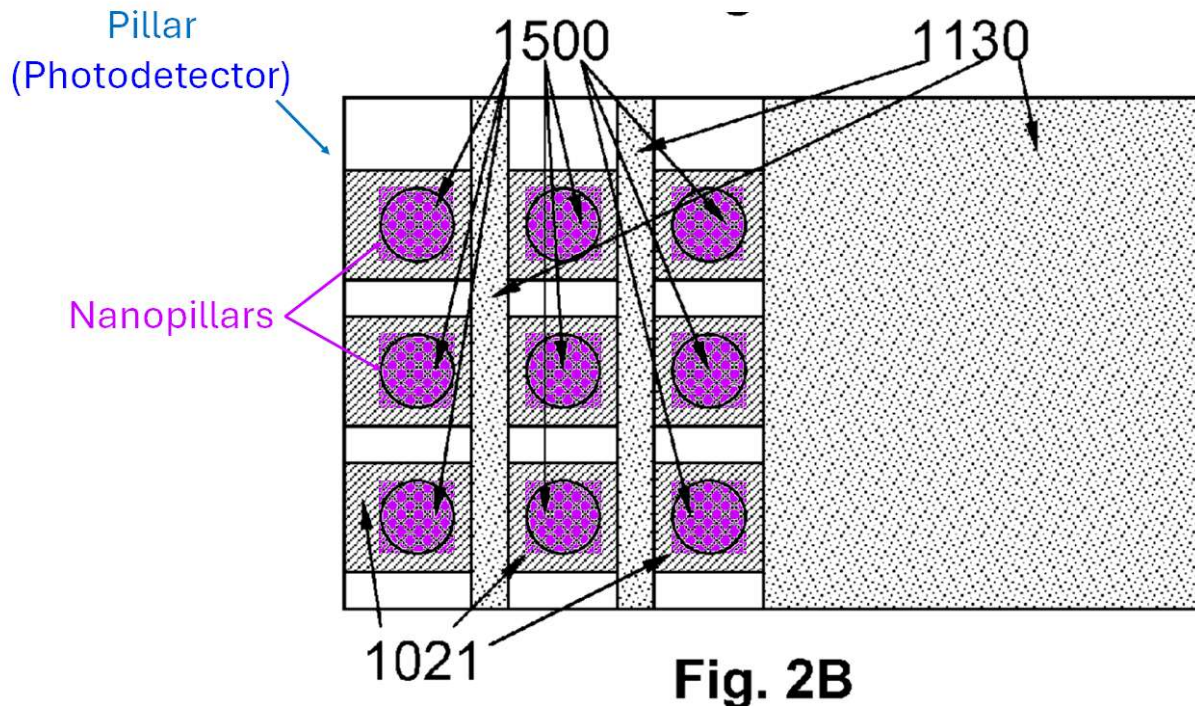


Yu, Fig. 1, step 132. The figure above shows a plurality of (i.e., two) **holes** in each **pixel**. Lebbby, ¶247.

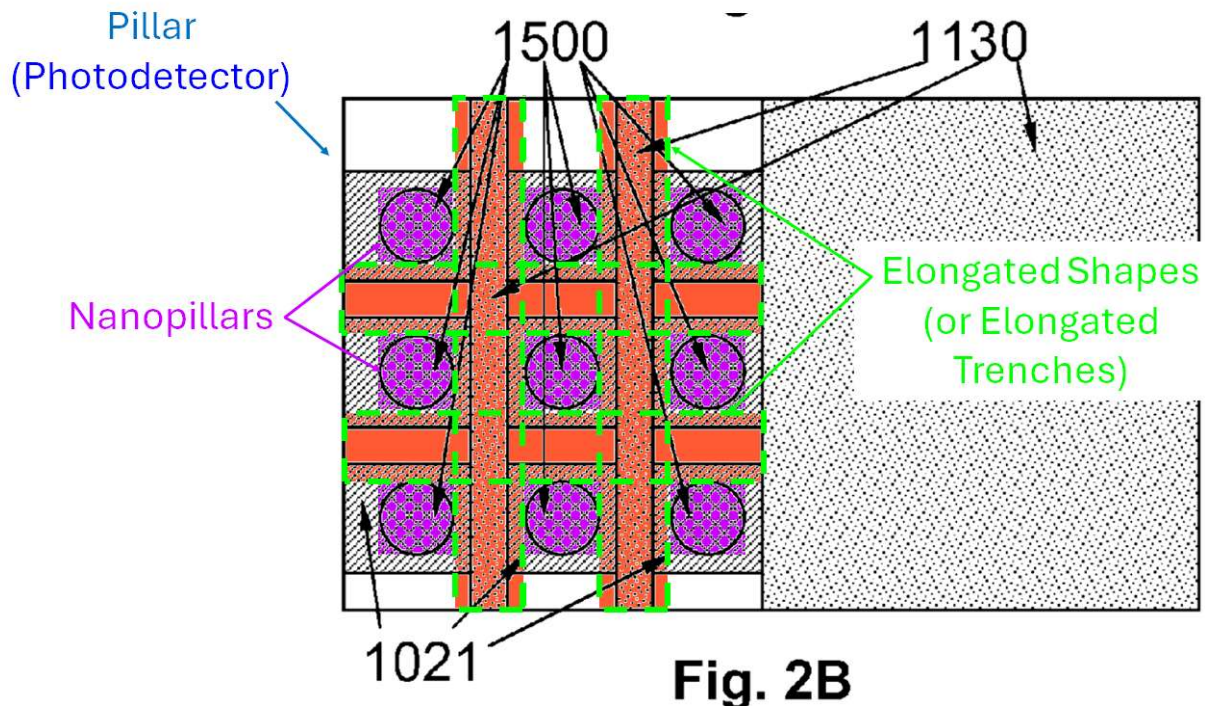
Yu's **epi layer** (i.e., "**region therebetween**") can be "about 3000 to 10000 nm thick." *Yu*, ¶[62]. "[T]he thickness of the **junction layer 1040** [(i.e., '**P-doped region**')]" is from 10 to 200 nm." *Yu*, ¶[63]. Thus, each **hole** has a depth ranging between 3,010-10,200 nm. Lebbby, ¶248. Because *Yu*'s holes have a depth range that overlaps with the claimed range of 100-10,000 nm, *Yu* renders the claimed range obvious. *Id.*; *In re Peterson*, 315 F.3d 1325, 1329 (Fed. Cir. 2003).

Yu's "nanopillars can have any suitable cross-sectional shape such as a circle, a square, [or] a hexagon." *Yu*, ¶[57]. Figure 2B, shown below, illustrates a

plan view of *Yu*'s pillar where each nanopillar has a generally square or rectangular cross-sectional shape. *Id.*; Lebby, ¶249.



Yu, Fig. 2B. According to Dr. Lebby, *Yu*'s square- or rectangular-shaped nanopillars would be formed by deep etching a substrate (*Yu*, ¶¶[68], [76]), to form trenches oriented generally perpendicular to each other. Lebby, ¶250. These trenches (or holes) having elongated shapes are shown below. *Id.*



Yu, Fig. 2B.

According to *Yu*, “space between the nanopillars 1500 is filled by an oxide or a polymer 1150 such as silicon oxide or polyimide.” *Yu*, ¶[87]. Silicon oxide is a solid dielectric. Lebbby, ¶251 (citing Ex-1020, 34-35; Ex-1063, 20-21, 23). Thus, *Yu*’s holes are filled with solid dielectric. *Id.*

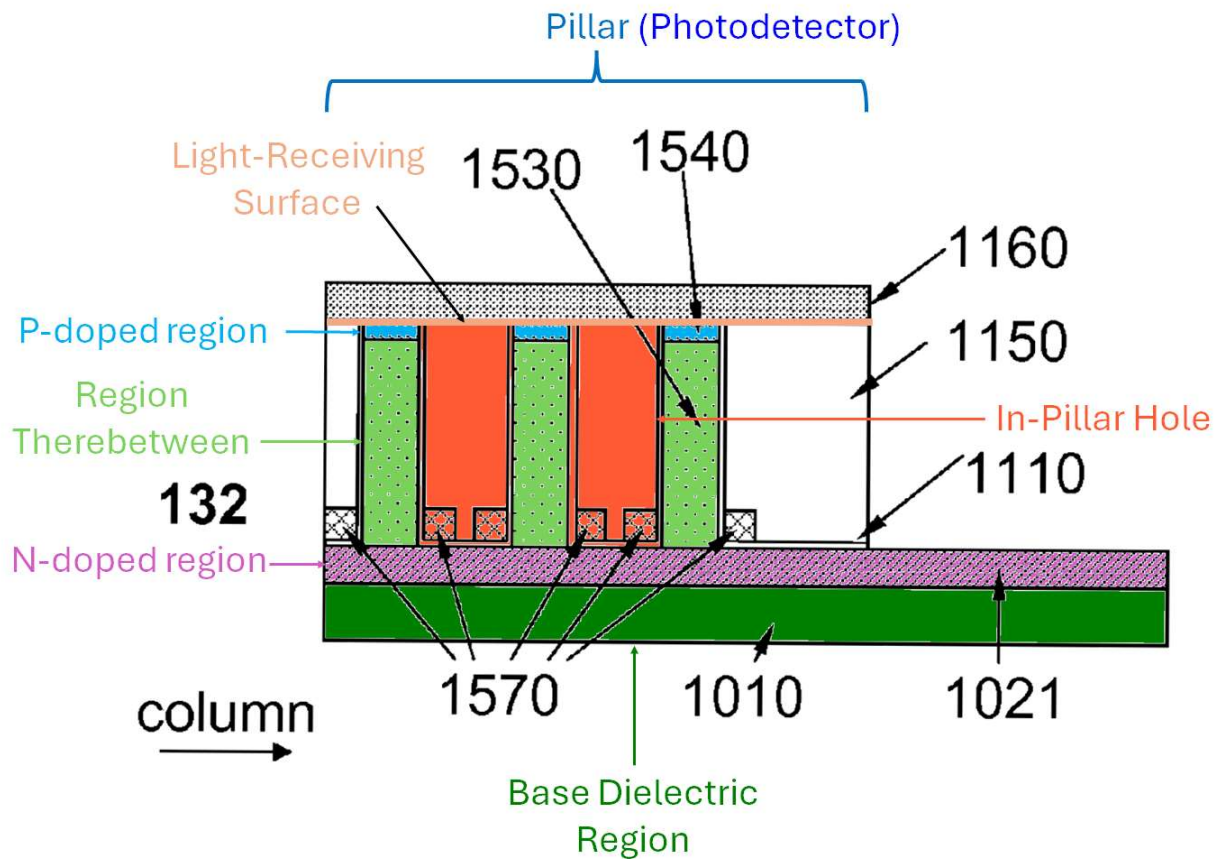
e. [1d]

Yu discloses [1d]. Lebbby, ¶¶252-253. *Yu* discloses an array of pixels (or pillars), each of which is a photodetector and has multiple nanopillars. VI.C.4.b ([1a]); Lebbby, ¶253. According to *Yu*, cladding may surround some or all image sensor pixels, and that the cladding may be formed from silicon nitride. *Yu*, ¶[133]. A POSITA would have understood that silicon nitride cladding on the sides of *Yu*’s

pixels (i.e., a photodetector) provides side isolation, as claimed, because such a layer provides insulation or passivation to protect the pixels from impurities, moisture, and scratches. Lebbby, ¶253 (citing Ex-1063, 20, 33).

f. [1e]

Yu discloses or suggests [1e]. Lebbby, ¶¶254-255. *Yu* discloses “a silicon-on-insulator (SOI)-type substrate or silicon-on-glass (SG)-type substrate is provided.” *Yu*, ¶¶[62], [15], [102]. The “substrate has an oxide layer 1010.” *Yu*, ¶¶[62], [102]. The substrate’s oxide layer 1010 is the base dielectric layer because as shown in the figure below, it is disposed below *Yu*’s pillars. Lebbby, ¶255. And oxide layer 1010 is a solid dielectric material. *Id.* (citing Ex-1020, 34-35; Ex-1063, 20-21, 23); VI.A.2.f.



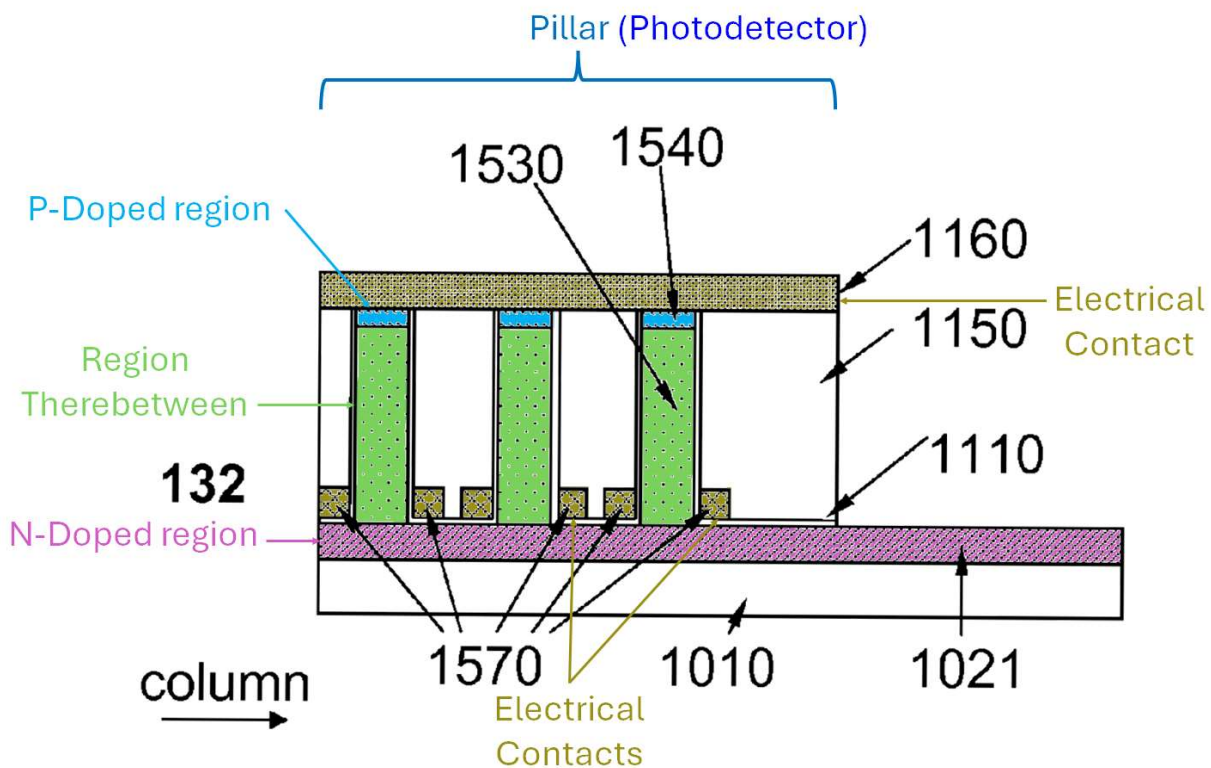
Yu, Fig. 1, step 132.

g. [1f]

The *Yu-Kuboi* combination renders obvious [1f]. Lebbby, ¶¶256-266. When forming Yu’s image sensor, “metal layer 1140 is deposited.” Yu, ¶[85]. The “portion of the metal layer 1140 deposited around the lower end of the nanopillars 1500 forms the gate electrodes and gate lines 1570.” *Id.* Yu discloses applying a gate voltage to one of the gate lines 1570 “to allow electrical current through the nanopillars.” Yu, ¶[114]. Thus, metal layer 1140 forms electrical contacts (i.e., gate

electrodes and gate lines) because they allow electrical current to flow through *Yu*'s nanopillars. Lebbby, ¶257.

Yu further discloses that “a transparent conductive layer (TCL) 1160, such as ITO or aluminum doped zinc oxide (AZO)[,] is deposited.” *Yu*, ¶¶[89], [27], [53]. *Yu* also discloses “applying a bias voltage to the TCL layer 1160.” *Yu*, ¶[114]. TCL also forms an electrical contact for *Yu*'s image sensor because it allows application of a bias voltage. Lebbby, ¶258. *Yu*'s electrical contacts are illustrated below.



Yu, Fig. 1, step 132.

A method of using *Yu*'s image sensor comprises “applying a bias voltage to the transparent conductive layer[and] applying a first gate voltage to all the gate

lines, the first gate voltage being effective to pinch off electrical current through the nanopillars.” *Yu*, ¶¶[28], [114]. Because *Yu*’s transparent conductive layer and gate lines (i.e., “electrical contacts”) are used to apply voltage across the nanopillars in *Yu*’s pixels (which are photodetectors, VI.C.4.b) to pinch off electrical current, *Yu*’s transparent conductive layer and gate lines (“electrical contacts”) provide electrical pathways to *Yu*’s photodetectors. Lebbby, ¶259.

As discussed above, *Kuboi* discloses applying reverse biasing to improve the response time of an optoelectronic device and induce carrier multiplication. VI.A.2.g; VI.C.2. And a POSITA would have found it obvious to implement *Kuboi*’s teaching of reverse bias in *Yu*’s integrated structure. Lebbby, ¶260; VI.C.2. Thus, in *Yu*’s integrated structure modified by *Kuboi*, *Yu*’s electrical contacts provide electrical pathways for reverse biasing as claimed. Lebbby, ¶260.

h. [1g]

Yu discloses or suggests [1g] based on Patent Owner’s statements in the ’871 Patent and a POSITA’s knowledge of the state of the art before the ’871 Patent’s priority date. Lebbby, ¶¶267-277.

Yu discloses an approximately 50 nm spacing between its nanopillars. *Yu*, ¶[65] (disclosing minimum feature size of 50 nm when etching). According to *Yu*, its nanopillars preferably have dimensions of 90-150 nm. *Yu*, ¶[57]. Thus, the period Λ or center-to-center distance between the holes ranges between

about 140-200 nm. Leebby, ¶269. Silicon's refractive index n_1 varies from about 3.5 for light of wavelength 1000 nm to 5.8 for light of wavelength 300 nm (Leebby, ¶270 (citing Ex-1056, 9:43-46, Fig. 4; Ex-1061, 49)). The refractive index n_2 of the silicon dioxide in *Yu*'s holes is about 1.5 over the wavelength range of 400-1000 nm. *Id.* (citing Ex-1062, 6, Fig. 1; Ex-1056, 9:43-46, Fig. 4).

Using the above values for wavelengths and refractive indices, Table C below shows the calculated values of λ/n_1 to λ/n_2 for n_2 of 1.5. As seen from the values in Table C, *Yu*'s hole pitch of 140-200 nm falls within the range λ/n_1 to λ/n_2 for at least a portion of the visible light spectrum. Leebby, ¶271. For example, for the 550 nm green light wavelength, λ/n_1 ($550/4.5 = 123$) $< \Lambda$ (140-200 nm) $< \lambda/n_2$ ($550/1.5 = 367$).

Table C				
λ (nm)	n_1 (Silicon)	n_2 (Dielectric)	λ/n_1 (nm)	λ/n_2 (nm)
400	5.8	1.5	68	267
550	4.5	1.5	123	367
650	3.9	1.5	168	433
700	3.8	1.5	184	467

Thus, the stated period of *Yu*'s hole array falls within the range λ/n_1 to λ/n_2 for selected visible and infrared wavelength ranges of the light. Leebby, ¶272.

Further, based on Patent Owner's representations, *Yu*'s pillar hole array forms an

HCG. *Id.*; VI.A.2.h (introducing Patent Owner's representations). And, under those same representations, such an HCG would produce an enhanced absorption coefficient of 1.1 to 100 times the bulk absorption coefficient based on the near-wavelength and deep-wavelength phenomena. Lebbby, ¶272; VI.A.2.h. Thus, consistent with Patent Owner's representations, a POSITA would have understood that the absorption of light, at selected visible and infrared wavelength ranges, by at least some of *Yu*'s photodetectors with holes would be at least 1.1 times that of like photodetectors lacking said holes. Lebbby, ¶272.

Patent Owner's representations, discussed above, were consistent with those of other prior art teachings that disclosed improvement in light absorption based on the depth of the holes. Lebbby, ¶273. As discussed above, *Yu* discloses that each of its holes has a depth ranging between 3,010-10,200 nm. VI.C.4.d.

According to *Han*, the ultimate efficiency for a device having a semiconductor thickness of about 3,010 nm (3.01 μm) without nanoholes is approximately 0.15, whereas the ultimate efficiency for a similar device having nanoholes is approximately 0.27. *Han*, Fig. 4; Lebbby, ¶275. Thus, before the earliest priority date of the '871 Patent, a POSITA would have understood that *Yu*'s hole depths of 3,010 nm (3.01 μm) increase light absorption by a factor of 1.8 ($0.27/0.15 = 1.8$), which is significantly higher than a factor of 1.1. *Id.*; *Han*, Fig. 4.

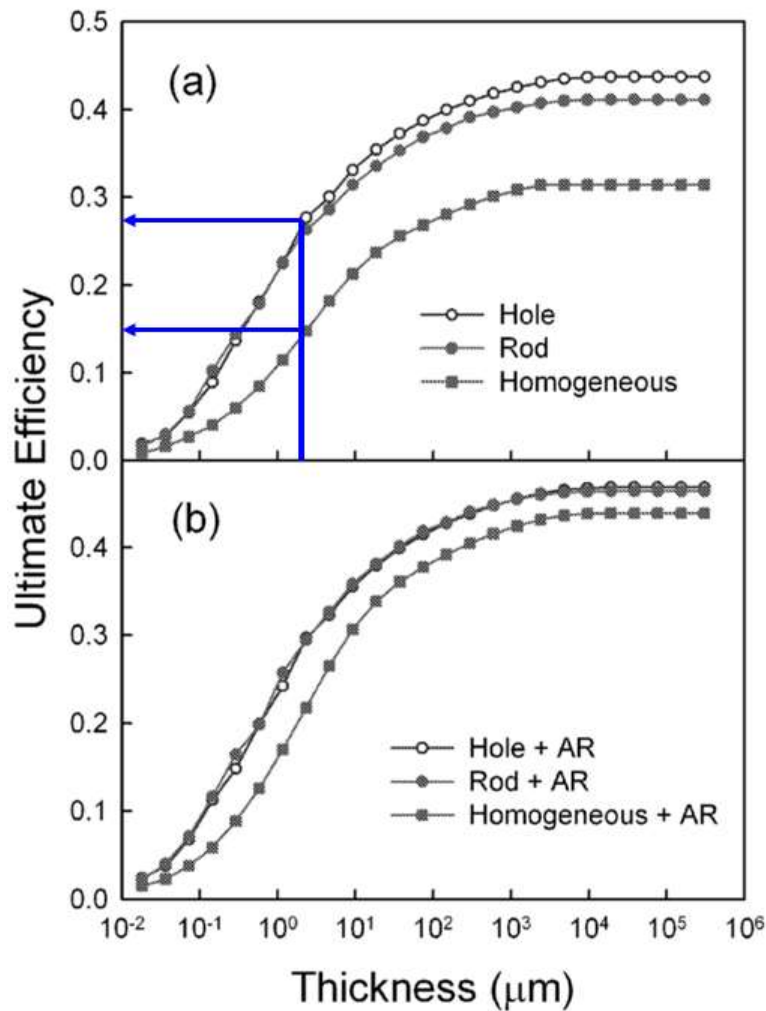


FIG. 4

Han, Fig. 4. As another example, *Han* discloses that the ultimate efficiency for a device having a semiconductor thickness of about 10,200 nm (10.2 μm) without nanoholes is approximately 0.22, whereas the ultimate efficiency for a similar device having nanoholes is approximately 0.33. *Han*, Fig. 4; Lebby, ¶276. Thus, before the earliest priority date of the '871 Patent, a POSITA would have understood that *Yu*'s hole depths of 10,200 nm (10.21 μm) increase light

absorption by a factor of 1.5 ($0.33/0.22 = 1.5$), which is significantly higher than a factor of 1.1. *Id.*; *Han*, Fig. 4.

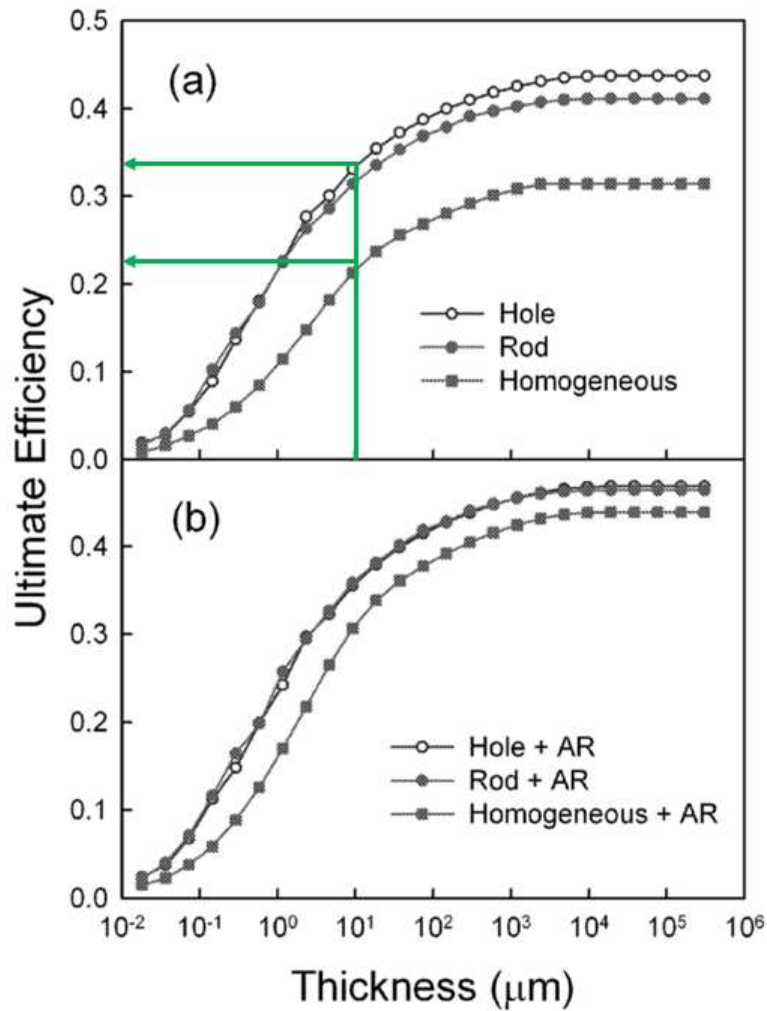


FIG. 4

Han, Fig. 4

Accordingly, based on a POSITA's knowledge of the state of the art before the '871 Patent's priority date, a POSITA would have understood that *Yu*'s holes of depth 3,010-10,200 nm would have increased the absorption of light, at selected

visible and infrared wavelength ranges, in at least some of *Yu*'s photodetectors by at least 1.1 times that of like photodetectors lacking said holes, and even if not readily understood, a POSITA would have found such a result not only obvious but also one having a reasonable expectation of success in achieving this increase because *Yu* discloses forming nanoholes of 3010-10200 nm depth. Lebbby, ¶277.

5. Claims 2 and 18

Yu discloses or the *Yu-Kuboi-Shinohara* combination renders obvious these limitations. Lebbby, ¶¶278-287. *Yu*'s apparatus comprises the image sensor and a **control circuit** that includes a decoder, a transimpedance amplifier, a multiplexer circuit, and other readout circuitry components (*Yu*, ¶[115]), which include electronic devices (VI.A.3; Lebbby, ¶279 (citing Ex-1076, 3)). The “image sensor and the **control circuit** can be formed as an integrated circuit or chip.” *Yu*, ¶[115]. *Yu*'s image sensor includes a plurality of **pixels** arranged in a two-dimensional **array of pillars** configured as **photodetectors**. VI.C.4.b. *Yu*'s “nanopillars and the substrate can comprise suitable semiconductor materials and/or metals such as Si.” *Yu*, ¶¶[55], [15], [27], [62]. Moreover, because *Yu*'s substrate includes Si, *Yu*'s **control circuit** would include **Si** (i.e., silicon based) **electronic devices**. Lebbby, ¶279. As Dr. Lebbby explains, forming the image sensor and **control circuit** as an “integrated circuit” means that *Yu*'s **pixels** (which are **photodetectors**) are

monolithically integrated with the **control circuit** (including **Si electronic devices**) on the same chip or **substrate**. Lebby, ¶280 (citing Ex-1076, 7).

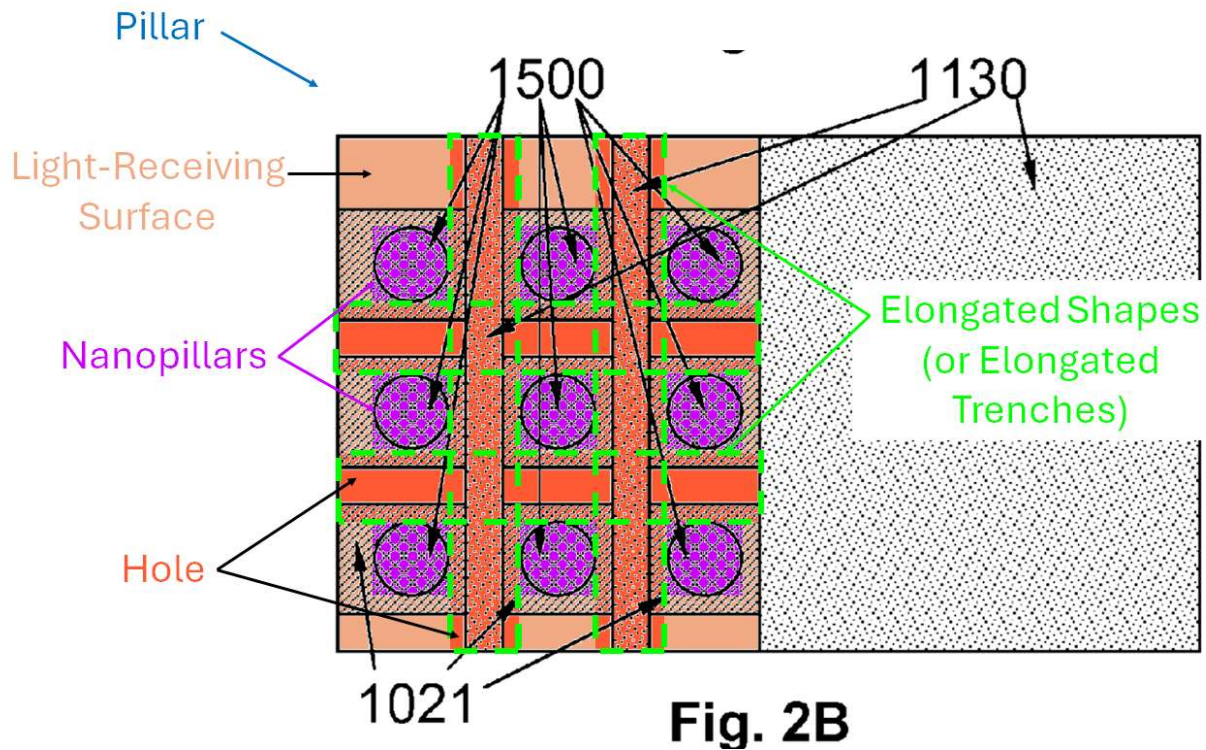
Yu's "[m]ethods of fabrication of the image sensor can include shallow trench isolation (STI), also known as 'Box Isolation Technique'" that "is generally used on CMOS process technology nodes of 250 nanometers and smaller." *Yu*, ¶[56]. Because *Yu*'s image sensor is fabricated using CMOS processes, *Yu*'s **control circuit** would include CMOS devices. Lebby, ¶281 (citing Ex-1076, 4). A POSITA would further have understood that *Yu*'s integrated circuit includes **pixels** (**photodetectors**) monolithically integrated with *Yu*'s CMOS **control circuit** (including **CMOS devices**) on the same chip or **substrate**. Lebby, ¶281.

To the extent Patent Owner argues that *Yu* does not disclose monolithic integration, the *Yu-Kuboi-Shinohara* combination renders these limitations obvious. Lebby, ¶¶282-287. *Shinohara* discloses forming a **pixel region**, a **peripheral circuit portion**, pixel transistors, and a wiring layer on the same **substrate**. *Shinohara*, ¶¶[68]-[82]; VI.B.2. As discussed above, a POSITA would have found it obvious to implement the monolithic integration taught by *Shinohara* to make the *Yu-Kuboi* integrated structure, including CMOS silicon electronic devices. VI.C.3; Lebby, ¶284. As also discussed above, *Shinohara* discloses a monolithically integrated CMOS imaging device. VI.B.6; Lebby, ¶284. Thus, the *Yu-Kuboi-Shinohara* combination renders obvious claims [2] and [18] for reasons

discussed above (VI.C.3) and for reasons similar to those discussed with respect to the *Kuboi-Shinohara* combination (VI.B.2). Lebbby, ¶¶284-286.

6. Claims 3, 4, 7, 8, and 15

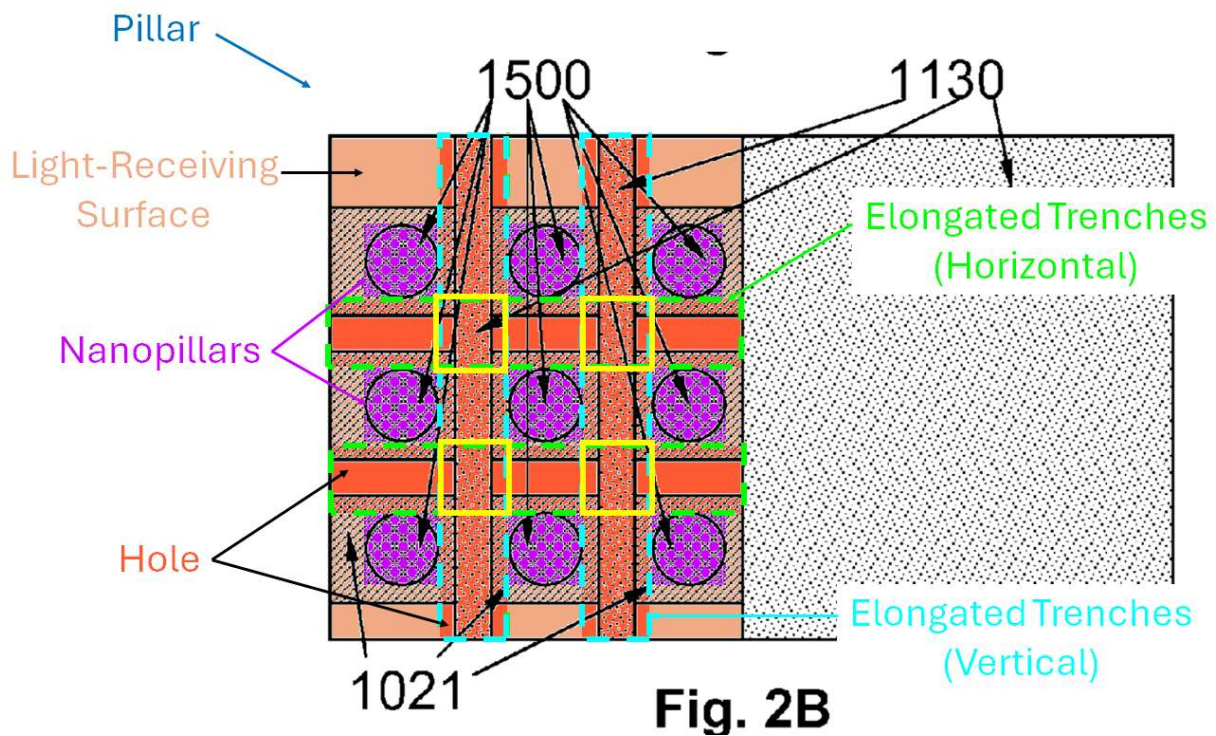
Yu discloses or renders obvious these additional limitations. Lebbby, ¶¶287-289. *Yu*'s **holes** are spaces between respective nanopillars, and those **holes** are formed in the light receiving surface of *Yu*'s **pillar**, which is a **photodetector**. VI.C.4.d ([1c]). *Yu* discloses that nanopillars can have any suitable cross-sectional shape such as a circle, a square, a hexagon. *Yu*, ¶¶[22], [57]. Figure 2B, shown below, illustrates a plan view looking down onto *Yu*'s **light-receiving surface**, and it shows **square shaped nanopillars** with **holes** between the **nanopillars**. Lebbby, ¶288. As illustrated below, a POSITA would have understood that *Yu*'s integrated structure has **pillars**, that include **holes** (“at least one,” “at least some,” or “a plurality of holes”), having **elongated shapes** (or are in the form of **elongated trenches**) formed at the **light-receiving surfaces** of the respective **pillars** (i.e., **photodetectors**). VI.C.4.d; Lebbby, ¶289.



Yu, Fig. 2B.

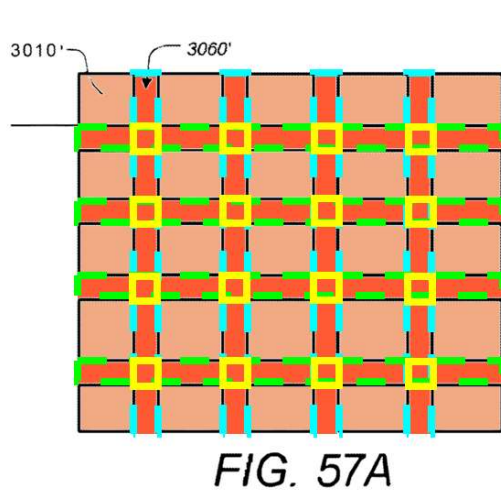
7. **Claim 17: “The integrated structure of claim 15, in which at least some of said elongated trenches crisscross.”**

Yu discloses this additional limitation. Lebbby, ¶¶290-294. Yu’s pixels (i.e., pillars) include square shaped nanopillars with elongated trench shaped holes between the nanopillars. VI.C.6 ([15]). As illustrated below, a POSITA would have understood that in the plan view of Yu’s pillar, the elongated trench shaped holes include trenches along a horizontal direction and trenches along a vertical direction (Lebbby, ¶291):

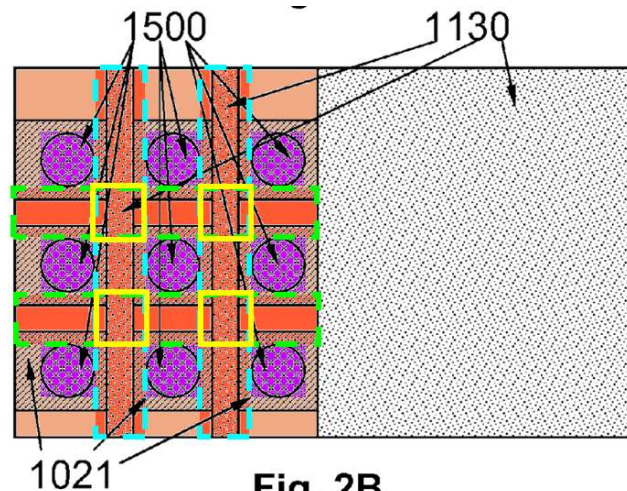


Yu, Fig. 2B. The trenches along the horizontal direction and trenches along the vertical direction crisscross at locations shown by the yellow squares. Lebbby, ¶292.

A POSITA would have understood that *Yu*'s trenches crisscross in a manner similar to that described in the '871 Patent. Lebbby, ¶¶293-294. Referencing Figures 57A-B, the '871 Patent discloses that "microstructure hole/trenches 3060' and 3062' are further configured to crisscross the surface of the semiconductors 3010' and 3008' respectively." '871 Patent, 55:3-11. A comparison of the '871 Patent's Fig. 57A and *Yu*'s Fig. 2B shows that *Yu*'s trenches crisscross at locations shown by the yellow squares similar to the trenches described in the '871 Patent:



'871 Patent, Fig. 57A



Yu, Fig. 2B

'871 Patent, Fig. 57A (left); Yu, Fig. 2B (right); Leebby, ¶¶293-294.

VII. Mandatory Notices

A. Real Parties-in-Interest

The real parties-in-interest are Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor LLC.

B. Related Matters

Patent Owner W&WSens Devices, Inc. asserted the '871 Patent in *W&W Devices Inc. v. Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor LLC*, Case No. 2:24-cv-00854-JRG (E.D. Tex.). Patent Owner also asserted U.S. Patent No. 11,621,360 in that case, which is related to the '871 Patent and is the subject of IPR2025-00994.

C. Lead and Backup Counsel, and Service Information

Lead Counsel	Backup Counsel
Joshua L. Goldberg, Reg. No. 59,369 joshua.goldberg@finnegan.com Finnegan, Henderson, Farabow, Garrett & Dunner, LLP 901 New York Avenue NW Washington, DC 20001-4413 Phone: 202-408-6092 Fax: 202-408-4400	Benjamin Saidman, Reg. No. 69,325 Benjamin.Saidman@finnegan.com Finnegan, Henderson, Farabow, Garrett & Dunner, LLP 271 17 th Street NW, Suite 1400 Atlanta, GA 30363 Phone: 404-653-6510 Fax: 404-653-6444 Abhay A. Watwe, Reg. No. 59,461 abhay.watwe@finnegan.com Finnegan, Henderson, Farabow, Garrett & Dunner, LLP 1875 Explorer Street, Suite 800 Reston, VA 20190-6023 Phone: 571-203-2716 Fax: 202-408-4400 Biju I. Chandran, Reg. No. 63,684 biju.chandran@finnegan.com Finnegan, Henderson, Farabow, Garrett & Dunner, LLP 1875 Explorer Street, Suite 800 Reston, VA, 20190-6023 Phone: 571-203-2414 Fax: 202-408-4400 Kai Rajan, Reg. No. 70,110 Kai.Rajan@finnegan.com Finnegan, Henderson, Farabow, Garrett & Dunner, LLP 901 New York Avenue NW Washington, DC 20001-4413 Phone: 202-408-4307 Fax: 202-408-4400

Please address all correspondence to counsel at the address above. Petitioner consents to electronic service by email at the above email addresses.

VIII. Grounds For Standing

Petitioner certifies that the '871 Patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified herein.

IX. Conclusion

For the reasons above, Petitioner requests institution of IPR and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Date: June 25, 2025

Respectfully submitted,

By: /Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, Petitioner certifies that the word count of Petitioner's Petition for *Inter Partes* Review (exclusive of any table of contents, table of authorities, mandatory notices under §42.8, certificates of service and word count, and list of exhibits or claim listing) as measured by Microsoft Word is 13,703.

Dated: June 25, 2025

By: /Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§42.6(e) and 42.105(a), the undersigned certifies that on June 25, 2025, a copy of the foregoing **Petition for *Inter Partes* Review, the associated powers of attorney, and Exhibits 1001-1007, 1010-1015, 1020-1022, 1029-1031, 1034-1038, 1050-1053, 1056-1057, 1059-1065, 1068-1073, 1075-1076** were served by FedEx Priority Overnight on the correspondence address of record indicated in the Patent Office's public Patent Center system for U.S. Patent No. 12,087,871:

Mr. Ivan S. Kavrukov
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001
UNITED STATES

Date: June 25, 2025

By: /William Esper/
William Esper
Legal Assistant and PTAB Coordinator
FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, LLP