ARTIFACT SHEET

Enter artifact number below. Artifact number is application number + artifact type code (see list below) + sequential letter (A, B, C ...). the first artifact folder for an artifact type receives the letter A, the second B, etc.. Examples: 59123456PA, 59123456PB, 59123456ZA, 59123456ZB

18822880ZA

Indicate quantity of a single type of artifact received but not scanned. Create individual artifact folder/box and artifact number for each Artifact Type.

		Number Of Disc(s)
☐	CD(s)/DVD(s) containing: Computer Program Listing Doc Code: Computer	☐ Artifact Type Code: P
	Sequence listing Doc Code Artifact	☐ Artifact Type Code: S
	Unspecified content Doc Code: Artifact	☐ Artifact Type Code: U
	Table Doc Code: Artifact	☐ Artifact Type Code: T

☐ Set(s) Color Documents or B/W Photographs
Doc Code: Artifact Artifact Type Code: C

☐ Confidential Information Disclosure Statement or Other Documents marked Proprietary, Trade Secrets, Subject to Protective Order, Material Submitted under MPEP 724.02, etc.
Doc Code: Artifact Artifact Type Code: X

1 Other documents, including Microfilm(s), Video Tape(s), Model(s), Bound Document(s), Color NPL, Returned Patent Grants, etc.
Description:
Doc Code: Artifact Artifact Type Code: Z

May 12, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/822,880	09/03/2024	Shih-Yuan WANG	309-0015USCIPDIV	5818

139982 7590 03/04/2025

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER	
RODELA, EDUARDO A	

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
03/04/2025	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

APPLICATION NO.	ISSUE DATE	PATENT NO.
18/822,880	04-Mar-2025	12243948

Wissing Miller LLP
Industrious at Hudson Yards
New York, NY 10001

EGRANT NOTIFICATION

Your electronic patent grant (eGrant) is now available, which can be accessed via Patent Center at https://patentcenter.uspto.gov

The electronic patent grant is the official patent grant under 35 U.S.C. 153. For more information, please visit https://www.uspto.gov/electronicgrants

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/822,880	03/04/2025	12243948	309-0015USCIPDIV	5818

139982 7590 02/12/2025

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

ISSUE NOTIFICATION

The projected patent number and issue date are specified above. The patent will issue electronically. The electronically issued patent is the official patent grant pursuant to 35 U.S.C. § 153. The patent may be accessed on or after the issue date through Patent Center at https://patentcenter.uspto.gov/. The patent will be available in both the public and the private sides of Patent Center. Further assistance in electronically accessing the patent, or about Patent Center, is available by calling the Patent Electronic Business Center at 1-888-217-9197.

The USPTO is implementing electronic patent issuance with a transition period, during which period the USPTO will mail a ceremonial paper copy of the electronic patent grant to the correspondence address of record. Additional copies of the patent (i.e., certified and presentation copies) may be ordered for a fee from the USPTO's Certified Copy Center at https://certifiedcopycenter.uspto.gov/index.html. The Certified Copy Center may be reached at (800)972-6382.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Center (https://patentcenter.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PATENT CENTER site https://patentcenter.uspto.gov for additional inventors):

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping WANG, Los Altos, CA;

APPLICANT(s) (Please see PATENT CENTER site https://patentcenter.uspto.gov for additional applicants):

W&W Sens Devices, Inc., Los Altos, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

139982 7590 01/15/2025
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

Mary Ellen Finnegan	(Typed or printed name)
/Mary Ellen Finnegan/	(Signature)
January 16, 2025	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/822,880	09/03/2024	Shih-Yuan WANG	309-0015USCIPDIV	5818

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0.00	$0.00	$480	04/15/2025

EXAMINER	ART UNIT	CLASS-SUBCLASS
RODELA, EDUARDO A	2893	136-256000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Wissing Miller LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: W&W Sens Devices, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Los Altos, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via the USPTO patent electronic filing system ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 600125

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Ivan S. Kavrukov/ Date January 16, 2025

Typed or printed name Ivan S. Kavrukov Registration No. 25,161

PTOL-85 Part B (11/23) Approved for use through 03/31/2026 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Samsung Exhibit 1090, Page 6 of 786
Samsung v. W&Wsens - IPR2025-00993

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
18/822,880	**01/16/2025 12:41:33 PM Z ET**	**309-0015USCIPDIV**

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68771694	FILING DATE	09/03/2024
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV_IssueFeeTransmittal-Final.pdf	1	Issue Fee Payment (PTO-85B)	408 KB
309-0015USCIPDIV_IssueFeeLtrWithStatementOfAllowance-Final.pdf	2	Miscellaneous Incoming Letter	496 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
309-0015USCIPDIV_IssueFeeTrans	8AAB7CE76E8992CA2444B68989549F47FEFB096D4FBD2333A75565428216E8025E3A58501335123ED5E3D408C9F2D262375

mittal-Final.pdf	EC51F5F566C2269F8FE01A1E0EE47
309-0015USCIPDIV_IssueFeeLtrWithStatementOfAllowance-Final.pdf	89F60478599B652FEF7112DBFF86AB2A985D4F3CF5F8759AD1C8FB1899FEEF6E3320B687DCC29A6BE1E5A9222821A71715D2307997AD2F43811C4EF66566A2EE

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Shih-Yuan WANG et al.
Serial No.:	18/822,880
Examiner:	EDUARDO A RODELA
Group Art Unit	2893
Filing Date:	09/03/2024
For:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
Conf. No.	5818

31 Hudson Yards, 11th Floor
New York, New York 10001

CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: January 16, 2025

I hereby certify that this correspondence is being transmitted via Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER ACCOMPANYING ISSUE FEE PAYMENT

Submitted herewith for filing in the U.S. Patent and Trademark Office are the following:

☒ Part B – Issue Fee Transmittal;
☒ Payment by credit card and Authorization to charge Deposit Account 600125 in payment of any fee deficiencies;

Applicant Comments to Examiner's Statement of Reasons for Allowance

The applicant recognizes that in accordance with M.P.E.P. § 1302.14, the Examiner's reasons for allowance need not set forth all the details as to why the claims are allowed. In the above identified

application, the applicant does not concede that the examiner's stated reasons for allowance are the only reasons for which the claims are allowable. In particular, the applicant does not concede that all the recited limitations are necessary to distinguish the prior art of record or to satisfy the requirements of 35 U.S.C. § 112. In addition, the dependent claims are allowable on their own merits and are allowable based on a sub-combination of the recited features of the dependent claims and their respective base claims. Applicant confirms that the claim amendments were made to expedite the grant of a patent with the allowed claims without prejudice to pursue the subject matter of the original claims in one or more continuing applications.

If there are any questions regarding this submission, the Examiner is encouraged to contact the undersigned via telephone at (917) 945-0121. I hereby authorize the USPTO to communicate any subject matter of this application by electronic mail at [wmdocket@wissingmiller.com]. I understand that a copy of these communications will be made of record in the application file.

By: /Ivan S. Kavrukov/
Ivan S. Kavrukov
Reg. No. 25,161
Tel. (917) 945-0121

Date: January 16, 2025
Address: (associated with Customer Number: 139982)
31 Hudson Yards, 11th Floor
New York, New York 10001
Attorney's Telephone No.: (917) 945-0121

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
18/822,880	**01/16/2025 12:41:33 PM Z ET**	**309-0015USCIPDIV**

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68771694	AUTHORIZED BY	Ivan Kavrukov
CUSTOMER #	139982	FILING DATE	09/03/2024
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Shih-Yuan WANG

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 2892	**E20251FC42506969**	**Mary Ellen Finnegan**

PRE-AUTHORIZED ACCOUNT	PRE-AUTHORIZED CATEGORY
600125	**37 CFR 1.21 (Miscellaneous fees and charges)**

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2501	UTILITY ISSUE FEE	480.00	1	480.00
			TOTAL AMOUNT:	**$480.00**

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

139982 7590 01/15/2025

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER	
RODELA, EDUARDO A	
ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 01/15/2025

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/822,880	09/03/2024	Shih-Yuan WANG	309-0015USCIPDIV	5818

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0.00	$0.00	$480	04/15/2025

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 11/23)

Samsung Exhibit 1090, Page 13 of 786
Samsung v. W&Wsens - IPR2025-00993

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

139982 7590 01/15/2025
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

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(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/822,880	09/03/2024	Shih-Yuan WANG	309-0015USCIPDIV	5818

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0.00	$0.00	$480	04/15/2025

EXAMINER	ART UNIT	CLASS-SUBCLASS
RODELA, EDUARDO A	2893	136-256000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required)

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via the USPTO patent electronic filing system ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Samsung Exhibit 1090, Page 14 of 786
Samsung v. W&Wsens - IPR2025-00993

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/822,880	09/03/2024	Shih-Yuan WANG	309-0015USCIPDIV	5818

139982 7590 01/15/2025

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER	
RODELA, EDUARDO A	
ART UNIT	PAPER NUMBER
2893	

DATE MAILED: 01/15/2025

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 11/23)

Samsung Exhibit 1090, Page 15 of 786
Samsung v. W&Wsens - IPR2025-00993

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/ owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013).
https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf

Routine uses of the information in this record may include disclosure to:

1) law enforcement, in the event that the system of records indicates a violation or potential violation of law;
2) a federal, state, local, or international agency, in response to its request;
3) a contractor of the USPTO having need for the information in order to perform a contract;
4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record;
5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record;
6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations;
7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals;
8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c));
9) the Office of Personnel Management (OPM) for personnel research purposes; and
10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Notice of Allowability	Application No. 18/822,880	Applicant(s) WANG et al.	
	Examiner Eduardo A Rodela	Art Unit 2893	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 11/22/2024.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-2 and 4-17 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☑ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/EDUARDO A RODELA/
Primary Examiner, Art Unit 2893

DETAILED ACTION

This correspondence is in response to the communications received October 31, 2024. Claims 1, 2 and 4-17 are pending. This office action is being examined under an expedited "special" status due to Applicant's Age, see "Petition Decision" document dated October 28, 2024 in the file wrapper.

Response to Arguments

Support for the newly amended claim 1 limitation of, "wherein at least some of the holes are elongated along the respective light receiving surfaces", can be found in ¶ 0249, lines 30-31, "The pillars, holes, **hole(s) in pillar** and pillar(s) in holes **can have any shape, for example a rectangular pillar within a round hole**, can have any mixture thereof to optimize enhancement…" and in Fig. 46 and the associated description in the specification.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Priority

The first instance of pillars having recesses formed therein can be found in provisional application 61/834,873 (dated June 13, 2013), on pg. 39. Therefore, the instant application's effective date is **June 13, 2013**.

Applicant's Claim to Figure Comparison

It is noted that this comparison is merely for the benefit of reviewers of this office action during prosecution, to allow for an understanding of the examiner's interpretation of the Applicant's independent claims as compared to disclosed embodiments in Applicant's Figures. No response or comments are necessary from Applicant.

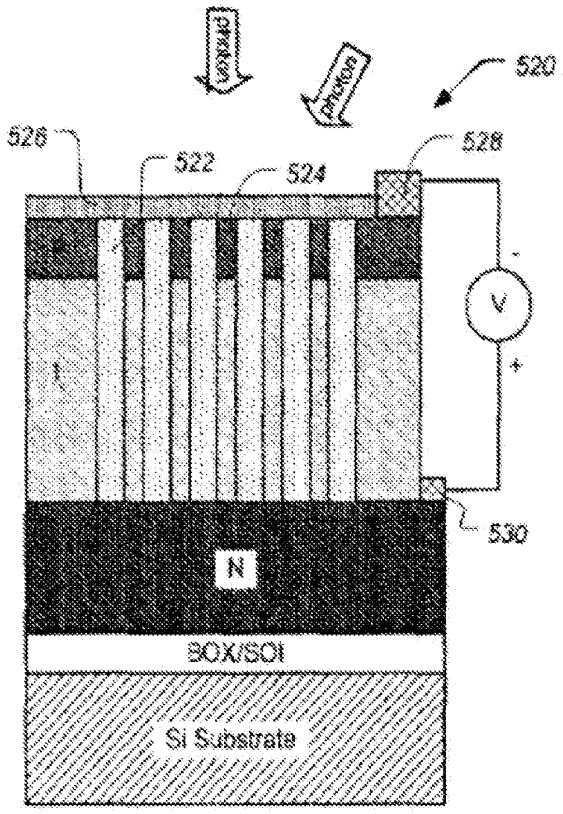


FIG. 5B

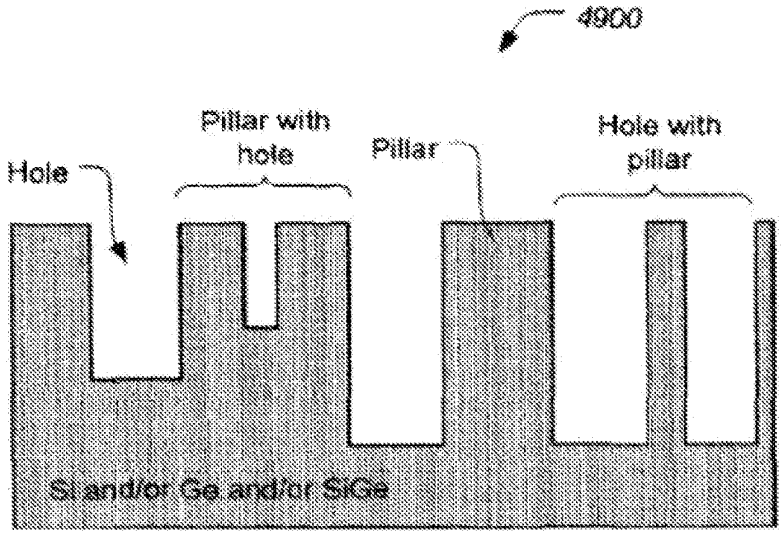


FIG. 49

Regarding claim 1, the Applicant discloses in Figs. 5B and 49, an integrated structure comprising:

an array of pillars ("pillars 524", ¶ 0132) comprising Si, Ge, and/or SiGe alloy semiconductor material, wherein at least some of the pillars are configured to include **photodetectors** and have respective light-receiving surfaces and respective sides ("The PD (and APO) photosensitive area (defined by the P-I-N or P-I-P-I-N junction area)", ¶ 0132);

wherein at least some of the pillars comprise P-doped and N- doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers ("The PD (and APO) photosensitive area (defined by the P-I-N or P-I-P-I-N junction area)", ¶ 0132);

one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars, have elongated or other shapes at or parallel to the light-receiving surfaces, extend into the pillars to a depth of 100 to10000 nm, and are filled at least partly with solid dielectric material;

wherein at least some of the holes are elongated along the respective light receiving surfaces (see Figs. 46 and 49, ¶ 0249)

side-isolation comprising solid material between at least portions of the sides of at least some of the pillars;

a solid dielectric material forming a base dielectric region for the array;

electrical contacts configured to provide electrical pathways coupled electrically to at least some of the **photodetectors**, including for selected reverse-biasing thereof;

wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the **photodetectors** relative to like **photodetectors** lacking said holes.

REASONS FOR ALLOWANCE

Claims 1, 2 and 4-17 are allowed.

The following is an Examiner's statement of reasons for allowance: The pillar shaped photodetector device as recited in the claims of the instant invention fail to be taught by the prior art cited of interest.

Regarding claim 1, the prior art of Yu et al. (US 2011/0309331) discloses in Fig. 5 and Lunev et al. (US 2014/0016660) discloses in Fig. 4B, pillar shaped photodetector devices, but fails to disclose the specific characteristic recited in the claims of the instant invention e.g. the combination of claimed features of an array of pillars with particular material composition and NP junction sensitive to visible and infrared wavelengths, one or more holes that are fabricated as recesses at or under the light receiving surface of at least some of the pillars, wherein at least some of the holes are elongated along the respective light receiving surfaces, side isolation, solid dielectric forming base dielectric, electrical contacts and the presence of the holes increase absorption by a specific amount.

Regarding claim 14, the prior art of Yu et al. (US 2011/0309331) discloses in Figs. 4 and 5, a integrated photoconversion array, but fails to disclose the specific characteristic recited in the claims of the instant invention e.g. the combination of claimed features of an array of pillars comprising Si, Ge, and/or alloyed SiGe semiconductor material, the pillars comprise p-type and n-type doped regions for generating charge carriers, holes in the light receiving surface of at least some of the pillars, the holes are filled with solid dielectric material, side isolation, solid dielectric material forming a base dielectric region for the array, electrical contacts, the presence of holes increases absorption of light by factor of 1.1, and the array is monolithically

integrated with electronic devices for signal processing and transmission, in conjunction with the feature of,

"each of the holes has an elongated shape extending in length over less than the width of the light receiving surface in which the hole is fabricated".

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A Rodela whose telephone number is (571)272-8797. The examiner can normally be reached M-F, 8:30-5:00pm ET.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yara B Green can be reached on (571) 270-3035. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC)

at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service

Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/EDUARDO A RODELA/
Primary Examiner, Art Unit 2893

Examiner-Initiated Interview Summary	**Application No.** 18/822,880	**Applicant(s)** WANG et al.		
	Examiner Eduardo A Rodela	**Art Unit** 2893	**AIA (First Inventor to File) Status** Yes	**Page** 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	**Title**	**Type**
Eduardo A Rodela	Primary Examiner	Telephonic
Ivan Kavrukov	Attorney of Record	

Date of Interview: 19 December 2024

Issues Discussed:

Other

Examiner sought aid in determining support for amendment to claim 1. Support was supplied and the location noted in the current office action.

	/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893

Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Samsung Exhibit 1090, Page 25 of 786
Samsung v. W&Wsens - IPR2025-00993

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	18/822,880	WANG et al.
	Examiner	Art Unit
	Eduardo A Rodela	2893

CPC - Searched*		
Symbol	Date	Examiner
H01L31/02019; H01L31/022408; H01L31/02327; H01L31/02363; H01L31/028; H01L31/035281; H01L31/105; H01L31/107; H01L31/0236,02363,0352	12/19/2024	EAR

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
PE2E search - see history for complete details	12/19/2024	EAR
Applicant & Inventor search	12/19/2024	EAR

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
noted CPC search area	in conjunction with a text limited search	12/19/2024	EAR

Samsung Exhibit 1090, Page 26 of 786
Samsung v. W&Wsens - IPR2025-00993

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	18/822,880	WANG et al.
	Examiner	Art Unit
	Eduardo A Rodela	2893

CPC						
Symbol					Type	Version
H01L	/	31	/	035272	F	2013-01-01
G02B	/	6	/	136	I	2013-01-01
H01L	/	23	/	66	I	2013-01-01
H01L	/	31	/	02005	I	2013-01-01
H01L	/	31	/	02016	I	2013-01-01
H01L	/	31	/	02019	I	2013-01-01
H01L	/	31	/	022408	I	2013-01-01
H01L	/	31	/	022475	I	2013-01-01
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H01L	/	31	/	02363	I	2013-01-01
H01L	/	31	/	024	I	2013-01-01
H01L	/	31	/	028	I	2013-01-01
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H01L	/	31	/	1804	I	2013-01-01
H01L	/	31	/	1808	I	2013-01-01
H01L	/	31	/	1812	I	2013-01-01

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	16	
/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893	19 December 2024	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	46, 49

U.S. Patent and Trademark Office — Part of Paper No.: 20241219

Samsung Exhibit 1090, Page 27 of 786
Samsung v. W&Wsens - IPR2025-00993

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	18/822,880	WANG et al.
	Examiner	Art Unit
	Eduardo A Rodela	2893

CPC						
Symbol					Type	Version
H01L	/	31	/	184	I	2013-01-01
H01L	/	31	/	1844	I	2013-01-01
G02B	/	6	/	122	I	2013-01-01
Y02E	/	10	/	548	A	2013-01-01
G02B	/	2006	/	12097	A	2013-01-01
G02B	/	2006	/	12176	A	2013-01-01
H01L	/	2223	/	6627	A	2013-01-01
Y02E	/	10	/	52	A	2013-01-01

CPC Combination Sets							
Symbol					Type	Set	Ranking	Version
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	16	
/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893	19 December 2024	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	46, 49

U.S. Patent and Trademark Office — Part of Paper No.: 20241219

Samsung Exhibit 1090, Page 28 of 786
Samsung v. W&Wsens - IPR2025-00993

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	18/822,880	WANG et al.
	Examiner	**Art Unit**
	Eduardo A Rodela	2893

INTERNATIONAL CLASSIFICATION					
CLAIMED					
H01L	/	31	/	0232	
H01L	/	31	/	0352	

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	16	
/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893	19 December 2024	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	46, 49

U.S. Patent and Trademark Office — Part of Paper No.: 20241219

Samsung Exhibit 1090, Page 29 of 786
Samsung v. W&Wsens - IPR2025-00993

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	18/822,880	WANG et al.
	Examiner	Art Unit
	Eduardo A Rodela	2893

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	9	10												
2	2	10	11												
	3	11	12												
3	4	12	13												
4	5	13	14												
5	6	14	15												
6	7	15	16												
7	8	16	17												
8	9														

NONE (Assistant Examiner)	(Date)	Total Claims Allowed: 16	
/EDUARDO A RODELA/ Primary Examiner, Art Unit 2893 (Primary Examiner)	19 December 2024 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 46, 49

U.S. Patent and Trademark Office Part of Paper No.: 20241219

Samsung Exhibit 1090, Page 30 of 786
Samsung v. W&Wsens - IPR2025-00993

Bibliographic Data

Application No: 18/822,880

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☐ No ☐ Met After Allowance

Verified and Acknowledged: /EDUARDO A RODELA/ Examiner's Signature | Initials

Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/03/2024	136	2893	309-0015USCIPDIV
RULE			

APPLICANTS

W&W Sens Devices, Inc., Los Altos, CA, UNITED STATES

INVENTORS

Shih-Yuan WANG, Palo Alto, CA, UNITED STATES

Shih-Ping WANG,

CONTINUING DATA

This application is a DIV of 18385213 10/30/2023 PAT 12087871

18385213 is a CIP of 18113474 02/23/2023

18385213 is a CIP of 17974325 10/26/2022 PAT 11830954

18113474 is a DIV of 17707429 03/29/2022 PAT 11621360

17707429 is a DIV of 17532831 11/22/2021 PAT 11309444

17707429 is a CIP of 17182954 02/23/2021 PAT 11791432

17532831 is a CIP of 17182954 02/23/2021 PAT 11791432

17182954 is a DIV of 16528958 08/01/2019 PAT 11121271

16528958 has PRO of 62874418 07/15/2019

16528958 has PRO of 62873891 07/13/2019

16528958 has PRO of 62870533 07/03/2019

16528958 has PRO of 62868911 06/29/2019

16528958 has PRO of 62867186 06/26/2019

16528958 has PRO of 62863852 06/19/2019

16528958 has PRO of 62863231 06/18/2019

16528958 has PRO of 62860115 06/11/2019

16528958 has PRO of 62853280 05/28/2019

16528958 has PRO of 62846554 05/10/2019
16528958 has PRO of 62843206 05/03/2019
16528958 has PRO of 62841798 05/01/2019
16528958 has PRO of 62828976 04/03/2019
16528958 has PRO of 62820695 03/19/2019
16528958 has PRO of 62819604 03/17/2019
16528958 has PRO of 62819669 03/17/2019
16528958 is a CIP of 16296985 03/08/2019 PAT 10468543
16528958 has PRO of 62808949 02/22/2019
16528958 has PRO of 62805850 02/14/2019
16528958 has PRO of 62802718 02/08/2019
16528958 has PRO of 62802171 02/06/2019
16528958 has PRO of 62800371 02/01/2019
16528958 has PRO of 62797263 01/26/2019
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FOREIGN APPLICATIONS

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	18822880
	Filing Date	2024-09-03
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIPDIV

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5315147		1994-05-24	Solomon	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20190001989		2019-01-17	Wang	
	2	20180102442		2018-04-12	Wang	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	8905043	WO		1989-06-01	Santa Barbara Research Center		☐
	2	2018508970	JP		2018-03-29	W&Wsens Devices Inc.		☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.A.R/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	18822880
	Filing Date	2024-09-03
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIPDIV

	3	02502326	JP		1990-07-26	Santa Barbara Research Center		☐

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NON-PATENT LITERATURE DOCUMENTS [Remove]

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Japanese Office Action for application number 2020-131831, dated October 7, 2024.	☐

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EXAMINER SIGNATURE

Examiner Signature	/EDUARDO A RODELA/	Date Considered	12/19/2024

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIPDIV

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2024-12-05
Name/Print	Ivan S. Kavrukov	Registration Number	25,161

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
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Samsung Exhibit 1090, Page 41 of 786
Samsung v. W&Wsens - IPR2025-00993

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L44	863	((("WANG") near3 ("Shih-Yuan")) OR (("WANG") near3 ("Shih-Ping"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2024/12/19 03:20 PM
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Samsung Exhibit 1090, Page 42 of 786
Samsung v. W&Wsens - IPR2025-00993

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Samsung Exhibit 1090, Page 43 of 786
Samsung v. W&Wsens - IPR2025-00993

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L49	101	("20070190434"|"20080047604"|"20080248608"|"20081012582"|"20090267049"|"20100029067"|"20100221866"|"20100313941"|"20120193676"|"20120292676"|"20130207222"|"20140001528"|"20150041965"|"20160225631"|"4571559"|"4716449"|"5451767"|"5625636"|"5757057"|"5886374"|"6027956"|"6177289"|"6667528"|"7495306"|"7772615"|"7898052"|"7972934"|"8114695"|"8357960"|"8436370"). PN.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM
L50	1	"20070007621"	(US-PGPUB)	OR	ON	ON	2024/12/19 03:20 PM
L51	31537	H01L31/0236,02363,0352.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO,	OR	ON	ON	2024/12/19 03:20 PM

			MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L52	95452	L5 OR L14	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM
L53	1111	(@rlpd<="20131115" OR @rlad<="20131115" OR @pd<="20131115" OR @ad<="20131115") AND L15 AND L7 AND L6	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM
L54	391	(@rlpd<="20131115" OR @rlad<="20131115" OR @pd<="20131115" OR @ad<="20131115") AND L15 AND L7 AND L6	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L55	508	("1918848" | "3903427" | "4017332" | "4292512" | "4316048" | "4357415" | "4387265" | "4394571" | "4400221" | "4443890" | "4513168" | "4531055" | "4620237" | "4678772" | "4827335" | "4846556" | "4857973" | "4876586" | "4880613" | "4896941"	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM

		| "4950625" | "4971928" | "4972244" | "4990988" | "5071490" | "5081049" | "5096520" | "5124543" | "5217911" | "5247349" | "5272518" | "5311047" | "5347147" | "5362972" | "5374841" | "5391896" | "5401968" | "5449626" | "5468652" | "5602661" | "5612780" | "5671914" | "5696863" | "5723945" | "5747796" | "5767507" | "5798535" | "5844290" | "5853446" | "5857053" | "5877492" | "5880495" | "5885881" | "5900623" | "5943463" | "5968528" | "6013871" | "6033582" | "6037243" | "6046466" | "6074892" | "6100551" | "6270548" | "6301420" | "6326649" | "6388243" | "6388648" | "6407439" | "6459034" | "6463204" | "6542231" | "6563995" | "6566723" | "6680216" | "6709929" | "6720594" | "6771314" | "6805139" | "6812473" | "6904187" | "6927145" | "6960526" | "6967120" | "6969899" | "6987258" | "6996147" | "7052927" | "7064372" | "7105428" | "7106938" | "7109517" | "7153720" | "7163659" | "7192533" | "7208783" | "7230286" | "7235475" | "7241434" | "7253017" | "7254151" | "7262400" | "7265328" | "7272287" | "7285812" | "7306963" | "7307327" | "7311889" | "7326915" | "7330404" | "7335962" | "7336860" | "7339110" | "7358583" | "7381966" | "7388147" | "7416911" | "7446025" | "7462774" | "7471428" | "7491269" | "7507293" | "7521322" | "7524694" | "7582587" | "7582857" | "7598482" | "7622367" | "7626685" | "7646138" | "7646943" | "7647695" | "7649665" | "7655860" | "7663202" | "7692860" | "7704806"					

		| "7713779" | "7719678" | "7719688" | "7732769" | "7732839" | "7736954" | "7740824" | "7790495" | "7872324" | "7888155" | "7902540" | "7948555" | "8030729" | "8035184" | "8049203" | "8063450" | "8067299" | "8067736" | "8084728" | "8093675" | "8118170" | "8143658" | "8154127" | "8193524" | "8208776" | "8212136" | "8212138" | "8222705" | "8242353" | "8269985" | "8274039" | "8299472" | "8330090" | "8384007" | "8455857" | "8471190" | "8514411" | "8546742" | "8748799" | "8766272" | "8791470" | "8810808" | "8835831" | "8866065" | "9000353" | "20020003201" | "20020020846" | "20020021879" | "20020071468" | "20020104821" | "20020109082" | "20020117675" | "20020130311" | "20020172820" | "20030003300" | "20030006363" | "20030077907" | "20030089899" | "20030103744" | "20030132480" | "20030160176" | "20030189202" | "20030227090" | "20040011975" | "20040021062" | "20040026684" | "20040058058" | "20040065362" | "20040075464" | "20040095658" | "20040109666" | "20040114847" | "20040118337" | "20040118377" | "20040122328" | "20040124366" | "20040155247" | "20040156610" | "20040160522" | "20040180461" |				

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		"20080191298" | "20080211945" | "20080218740" | "20080224115" | "20080225140" | "20080233280" | "20080237568" | "20080246020" | "20080246123" | "20080248304" | "20080251780" | "20080258747" | "20080260225" | "20080264478" | "20080266556" | "20080266572" | "20080271783" | "20080277646" | "20080283728" | "20080283883" | "20080297281" | "20080311693" | "20080311712" | "20090001498" | "20090020150" | "20090020687" | "20090032687" | "20090046362" | "20090046749" | "20090050204" | "20090052029" | "20090057650" | "20090072145" | "20090104160" | "20090120498" | "20090121136" | "20090127442" | "20090146198" | "20090151782" | "20090152664" | "20090153961" | "20090165844" | "20090173976" | "20090179225" | "20090179289" | "20090188552" | "20090189144" | "20090189145" | "20090194160" | "20090199597" | "20090201400" | "20090206405" | "20090211622" | "20090223558" | "20090224245" | "20090224349" | "20090230039" | "20090233445" |				

		"20090242018" | "20090243016" | "20090244514" | "20090260687" | "20090261438" | "20090266418" | "20090266974" | "20090272423" | "20090278998" | "20090289320" | "20090305454" | "20100006817" | "20100019252" | "20100019296" | "20100019355" | "20100025710" | "20100078055" | "20100078056" | "20100090341" | "20100101633" | "20100104494" | "20100110433" | "20100116976" | "20100126573" | "20100127153" | "20100132779" | "20100133986" | "20100136721" | "20100148221" | "20100163714" | "20100163941" | "20100178018" | "20100186809" | "20100187404" | "20100200065" | "20100207103" | "20100218816" | "20100229939" | "20100230653" | "20100237454" | "20100240104" | "20100244108" | "20100244169" | "20100249877" | "20100258184" | "20100276572" | "20100277607" | "20100282314" | "20100295019" | "20100302440" | "20100304061" | "20100308214" | "20100313952" | "20100319763" | "20100320444" | "20110018424" | "20110036396" | "20110037133" |				

Samsung Exhibit 1090, Page 51 of 786
Samsung v. W&Wsens - IPR2025-00993

		"20110049572" | "20110050042" | "20110057231" | "20110057234" | "20110057286" | "20110080508" | "20110084212" | "20110127490" | "20110133060" | "20110133160" | "20110135814" | "20110139176" | "20110146771" | "20110147870" | "20110180894" | "20110195577" | "20110220191" | "20110226937" | "20110248315" | "20110249219" | "20110249322" | "20110253982" | "20110272014" | "20110297214" | "20110309237" | "20110309240" | "20110309331" | "20110315988" | "20110316106" | "20120006390" | "20120009714" | "20120014837" | "20120029328" | "20120031454" | "20120060905" | "20120075513" | "20120153124" | "20120192939" | "20120196383" | "20120196401" | "20120240999" | "20120258563" | "20120280345" | "20120298843" | "20120313078" | "20120318336" | "20120322164" | "20130000704" | "20130020620" | "20130037100" | "20130112256" | "20130125965" | "20130174904" | "20130220406" | "20130341749" | "20140045209" | "20140096816" | "20140117401" |				

		"20150171272").pn. AND (PGPB | USPT | USOC).dbnm.					
L56	1	"9312448".pn.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L57	386	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L15 AND L7 AND L6	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L58	38	("6946682" | "7601993" | "7923753" | "8525227" | "8604511" | "8735941" | "8941146" | "8969198" | "9660043" | "20020142548" | "20070187677" | "20080173898" | "20080217625" | "20080258150" | "20090035884" | "20090127575" | "20090212276" | "20100059781" | "20110018024" | "20110143507" | "20110198641" | "20110233520" | "20110233596" | "20120049152" | "20120119189" | "20120235204" | "20120248500" | "20130026519" | "20130320352" | "20140016660" | "20140264454").pn. OR ("9793439").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L59	36	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L21	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L60	1	"20110309331"	(US-PGPUB)	OR	ON	ON	2024/12/19 03:20 PM
L61	1	"20140016660"	(US-PGPUB)	OR	ON	ON	2024/12/19 03:20 PM
L62	214	(texture OR recesses OR divots OR holes) WITH surface WITH	(US-PGPUB)	OR	ON	ON	2024/12/19 03:20 PM

		(diode) WITH (absorb$3 OR absorption OR efficiency) WITH light					
L63	277	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L25	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L64	1996	(textur$3 OR texturized) WITH (("1" OR "10" OR "20" OR "30 OR "40 OR "50") NEAR (nanometer$1 OR "nm"))	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L65	245	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L27 AND L14	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM
L66	76	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L27 AND L14	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L67	594	(textur$3 OR texturized) WITH surface WITH (increas$3 NEAR (efficiency OR absorb$3 OR absorption))	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L68	78	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND L14	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L69	36	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND L14 AND (percent$3 OR	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM

		"%")					
L70	0	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND (L14 SAME (percent$3 OR "%"))	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L71	0	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND (L14 SAME (percent$3 OR "%"))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM
L72	7638562	(signal NEAR process$3) AND (output OR transmission)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM
L73	244	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L14 AND L35	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L74	4526	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND (cmos NEAR imager) AND L35	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM
L75	747	(@rlpd<="20130613" OR	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM

		@rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND (cmos NEAR imager) AND ((signal NEAR process$3) AND (output OR transmission)) AND monolithic$4					
L76	0	(L2 OR L3 OR L15) AND ((integrated NEAR structure)(array)(pillars)(holes)(p-doped)(n-doped)(light NEAR receiving NEAR surfaces)(visible)(infrared)(wavelengths)(photosensitive NEAR area)(charge NEAR carriers)(holes)(recesses)(side NEAR isolation)(base NEAR dielectric)(electrical NEAR contacts)(factor)(increase)(abosorption)("1.1")).clm.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2024/12/19 03:20 PM
L77	36	((US-11282970-B1 OR US-9515218-B2 OR US-8384007-B2 OR US-9793439-B2 OR US-9312448-B2 OR US-9196763-B2 OR US-8835905-B2 OR US-8970751-B2 OR US-9362459-B2 OR US-7833425-B2 OR US-8592949-B2 OR US-5759292-A OR US-7276749-B2).did. AND USPT.dbnm.) OR ((US-20130125965-A1 OR US-20130112256-A1 OR US-20120313078-A1 OR US-20120298843-A1 OR US-20120196401-A1 OR US-20120153124-A1 OR US-20110315988-A1 OR US-20110309331-A1 OR US-20110297214-A1 OR US-20110272014-A1 OR US-20110253982-A1 OR US-20110226937-A1 OR US-	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM

Samsung Exhibit 1090, Page 56 of 786
Samsung v. W&Wsens - IPR2025-00993

		20110180894-A1 OR US-20110133160-A1 OR US-20110057286-A1 OR US-20140016660-A1 OR US-20130026519-A1 OR US-20140070245-A1 OR US-20140174521-A1 OR US-20130330871-A1 OR US-20110281078-A1 OR US-20100116332-A1 OR US-20140125851-A1).did. AND PGPB.dbnm.)					
L78	36	((US-11282970-B1 OR US-9515218-B2 OR US-8384007-B2 OR US-9793439-B2 OR US-9312448-B2 OR US-9196763-B2 OR US-8835905-B2 OR US-8970751-B2 OR US-9362459-B2 OR US-7833425-B2 OR US-8592949-B2 OR US-5759292-A OR US-7276749-B2).did. AND USPT.dbnm.) OR ((US-20130125965-A1 OR US-20130112256-A1 OR US-20120313078-A1 OR US-20120298843-A1 OR US-20120196401-A1 OR US-20120153124-A1 OR US-20110315988-A1 OR US-20110309331-A1 OR US-20110297214-A1 OR US-20110272014-A1 OR US-20110253982-A1 OR US-20110226937-A1 OR US-20110180894-A1 OR US-20110133160-A1 OR US-20110057286-A1 OR US-20140016660-A1 OR US-20130026519-A1 OR US-20140070245-A1 OR US-20140174521-A1 OR US-20130330871-A1 OR US-20110281078-	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/12/19 03:20 PM

		A1 OR US-20100116332-A1 OR US-20140125851-A1).did. AND PGPB.dbnm.)					
L79	17	("3620829" | "4078945" | "4227942" | "4640001" | "4675466").pn. OR ("5759292").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/12/19 03:20 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	0	(L43 OR L44 OR L52) AND ((array)(pillars)(semiconductor)(photodetectors)(light-receiving NEAR surfaces)(P-doped)(N-doped)(regions)(visible)(infrared)(wavelengths)(electrical NEAR charge NEAR carriers)(holes)(recesses)(elongated)(depth)(isolation)(solid NEAR dielectric NEAR material)(absorption)(factor)).clm.	(US-PGPUB; USPAT)	AND	ON	ON	2024/12/19 05:03 PM

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
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	Application Number	18822880
	Filing Date	2024-09-03
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIPDIV

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	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIPDIV

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2024-11-18
Name/Print	Ivan S. Kavrukov	Registration Number	25,161

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
18/822,880	09/03/2024	Shih-Yuan WANG	309-0015USCIPDIV

CONFIRMATION NO. 5818

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Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

PUBLICATION NOTICE

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Date Mailed: 12/26/2024

Title:MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Publication No.US-2024-0429332-A1
Publication Date:12/26/2024

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Samsung Exhibit 1090, Page 63 of 786
Samsung v. W&Wsens - IPR2025-00993

Patents 2018-508970

Microstructure-enhanced absorption photosensitive device

Abstract

translated from Japanese

A technique for improving photon absorption in a semiconductor using a microstructure is described. The microstructure is, for example, a hole and effectively increases the absorption of photons. Using a microstructure to improve absorption for silicon photodiodes and silicon avalanche photodiodes can result in a bandwidth exceeding 10 Gb / s for photons having a wavelength of 850 nm with a quantum efficiency of about 90% or more. is there. Their thickness dimensions allow them to be conveniently integrated on the same Si chip as CMOS, BiCMOS and other electronics, resulting in packaging advantages, reduced capacitance, Therefore, the speed is further increased. [Solution] [Selection] Figure 1

Classifications

- G02B6/4204 Packages, e.g. shape, construction, internal or external details the coupling comprising intermediate optical elements, e.g. lenses, holograms

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JP2018508970A

Other languages: Japanese

Inventor: [illegible]

Current Assignee : W&Wsens Devices Inc

Worldwide applications

2016 US CN US WO JP EP US

Application JP2017526132A events

2016-11-17 Application filed by W&Wsens Devices Inc

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2021-05-26 Application granted

2021-05-26 Publication of JP6875082B2

Status Active

2036-11-17 Anticipated expiration

Info: Patent citations (70), Cited by (60), Legal events, Similar documents, Priority and Related Applications

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Claims (60)

Hide Dependent

translated from Japanese

In an integrated detector / processor circuit for data communication having both a photodetector with microstructure enhanced light absorption formed in a single semiconductor chip and an electronic processor,

Light sensing having a photon absorption region formed on a semiconductor substrate and configured to absorb photons from an optical source signal modulated for data communication and to provide a corresponding output electrical signal A vessel is provided.

The photon absorption region has a plurality of holes therein, the holes extend toward the substrate, and are configured to simultaneously receive the same source signal in the plurality of holes. And

An electronic processor is also formed on the semiconductor substrate and is operatively associated with the photon absorption region to receive the output electrical signal therefrom and process it into a processed output, thereby receiving the optical source signal and the Forms a single semiconductor chip that outputs processed output.

The photon absorption region and the electronic processor have respective thicknesses that are about the same thickness, and a cathode region and an anode region are operatively associated with the photon absorption region and the reverse bias circuit. The reverse bias circuit is configured to apply a voltage between the cathode region and the anode region such that the cathode region is driven to a more positive voltage than the anode region.

Integrated detector / processor circuit. The integrated detector / processor circuit of claim 1, wherein the photon absorption region has a thickness in the range of 0.5 to 5 micrometers. The electronic processor comprises an application specific integrated circuit (ASIC) having at least one of a complementary metal oxide semiconductor (CMOS) device, a bipolar (BI) device, and a BiCMOS device. The integrated detector / processor circuit of claim 1. 2. The integrated detector / processor circuit of claim 1, wherein the photon absorption region is configured to absorb more than 40% of the incident source signal at a wavelength of 800 nm to 900 nm and provide a corresponding output electrical signal. . 2. The integrated detector / processor circuit of claim 1, wherein the photon absorption region is configured to absorb more than 50% of the incident source signal at a wavelength of 800 nm to 900 nm and provide a corresponding output electrical signal. . 2. The integrated detector / processor circuit of claim 1, wherein the photon absorption region is configured to absorb more than 60% of the incident source signal at a wavelength of 800 nm to 900 nm and provide a corresponding output electrical signal. . 2. The integrated detector / processor circuit of claim 1, wherein the photon absorption region is configured to absorb more than 40% of the incident source signal at a wavelength between 1400 nm and 1700 nm and provide a corresponding output electrical signal . 2. The integrated detector / processor circuit of claim 1, wherein the photon absorption region is configured to absorb more than 50% of the incident source signal at a wavelength between 1400 nm and 1700 nm and provide a corresponding output electrical signal. . 2. The integrated detector / processor circuit of claim 1, wherein the photon absorption region is configured to absorb more than 60% of the incident source signal at a wavelength between 1400 nm and 1700 nm and provide a corresponding output electrical signal. . The photon absorption region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over a selected wavelength span of at least 20 nm of a source signal wavelength from 800 nm to 900 nm. Integrated detector / processor circuit. The integration of claim 1, wherein the photon absorption region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over a wavelength span of at least 20 nm of a source signal wavelength between 1400 nm and 1700 nm. Detector / processor circuit. Each hole has a cross section parallel to the surface of the substrate and the maximum dimension of the cross section is between 400 nm and 2500 nm, and each hole is from the center of the nearest adjacent hole of the plurality of holes. 2. The integrated detector / processor circuit of claim 1 having centers separated by less than 3500 nm. The photodetector further comprises a P layer and an N layer that are highly doped at or above 10^{16} / cm^3 and located on the sides of the photon absorption region, and The integrated detector / processor circuit of claim 1

wherein the photon absorption region is lightly doped or intentionally undoped and at most 10^{16} / cm^3. The integrated detector / processor circuit of claim 1, wherein the photodetector comprises an avalanche photodetector. The integrated detector / processor circuit of claim 1 wherein the photon absorption region comprises Si. The integrated detector / processor circuit of claim 1 wherein the photon absorption region comprises Ge. The photodetector has a tapered or stepped hole configured to receive an optical fiber carrying the source signal and maintain one end of the fiber at a selected distance from the photon absorption region. The integrated detector / processor circuit of claim 1. The integrated detector / processor circuit of claim 17 further comprising a lens between the end of the fiber and the photon absorption region. The integration of claim 1, wherein the photodetector has a reflective structure configured to generate multiple reflections of the source signal such that the source signal traverses the photon absorption region multiple times. Detector / processor circuit. The integrated detector / processor circuit of claim 1, wherein the photodetector is configured to receive the source signal from two opposing sides of the photon absorption region. 2. The integrated detector / processor circuit of claim 1, wherein the holes are configured to generate a coupled resonance in the conversion of optical signals to electrical signals in the plurality of groups of holes to improve source signal absorption. . In addition, one or more additional photodetectors are formed on the semiconductor substrate and receive respective additional source signals and provide respective output electrical signals corresponding thereto. An absorption region, and one or more additional electronic processors are also formed on the semiconductor substrate and are operatively associated with the respective photon absorption regions of the additional photodetector. The integrated detector / processor circuit of claim 1, wherein said integrated detector / processor circuit is configured to receive and process said respective output electrical signals therefrom. 2. The integrated detector / processor circuit according to claim 1, wherein the plurality of holes improve absorption of photons in a wavelength range including the wavelength of the source signal as compared to the other photodetectors that do not have holes. . The integrated detector / processor circuit of claim 1, wherein the electronic processor includes one or more types selected from the group consisting of a transimpedance amplifier, signal processing electronics, and routing electronics. The integration of claim 1 wherein the capacitance associated with the photodetector is reduced compared to the same photodetector except that its anode and cathode regions are operatively connected to a conventional bond pad. Detector / processor circuit. The photodetector further has a multiplication region and has a gain greater than 2 and detects the source signal in a data bandwidth greater than 10 Gb / s at a source signal wavelength of 800 to 900 nm. 2. The integrated detector / processor circuit of claim 1, wherein said integrated detector / processor circuit is an avalanche photodiode. In optical / electronic systems.

The photodetector and the active electronic circuit are constructed on the same semiconductor substrate and are operatively associated with each other to form a single integrated circuit chip;

A laser generates an optical source signal that is modulated at a data rate of 25 / s and carries information at the Gb / s rate;

An optical fiber is associated with the laser and receives the optical source signal at its input and carries it to its output;

The photodetector is associated with the output end of the optical fiber and is configured to receive the optical source signal and convert it to an electrical output signal; and the active electronic circuit comprises the photodetector And is configured to receive the output electrical signal and process the electrical output signal to output the processed electrical signal.

System. 28. The system of claim 27, wherein each of the source signal and the electrical output signal is modulated at a rate of at least 5 Gb / s. 28. The system of claim 27, wherein the photodetector and the active electronic circuit have a thickness that is approximately the same size. The photodetector has a photon absorption region including a plurality of holes extending toward the semiconductor substrate, and the plurality of holes are configured to simultaneously receive the same source signal. 28. The system of claim 27. Highly doped P and N layers are located on the sides of the photon absorption region, and the photon absorption region has a thickness in the range of 0.1-5.0 micrometers; and 28. The system of claim 27, wherein the system is intentionally undoped or lightly doped compared to the P and N regions. 28. The system of claim 27, wherein the photodetector is biased to sweep at least one of electrons or holes in a direction along a direction in which the source signal is received by the light detection. 28. The system of claim 27, wherein each of the photodetector and the active electronic circuit is silicon based. 28. The system of claim 27, wherein the light detector is an avalanche light detector.

in a photodetector having optical absorption with improved microstructure;

A photon absorption region having a thickness between 0.5 and 5 micrometers and configured to absorb photons from a source signal modulated for data communication and provide a corresponding output electrical signal Provided.

The photon absorption region has a plurality of holes, the plurality of holes extending through at least a portion of the thickness of the photon absorption region and the same source signal in the plurality of holes. And the photon absorption region receives and corresponds to more than 40% of the incident source signal at a wavelength in at least one of the range of 800 nm to 900 nm and 1400 nm to 1700 nm. And an output electric signal to be supplied;

Photo detector. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb more than 40% of the incident source signal at a wavelength of 800 nm to 900 nm and provide a corresponding output electrical signal. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb more than 50% of the incident source signal at a wavelength of 800 nm to 900 nm and provide a corresponding output electrical signal. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb more than 60% of the incident source signal at a wavelength of 800 nm to 900 nm and provide a corresponding output electrical signal. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb more than 40% of the incident source signal at a wavelength between 1400 nm and 1700 nm and provide a corresponding output electrical signal. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb more than 50% of the incident source signal at a wavelength between 1400 nm and 1700 nm and provide a corresponding output electrical signal. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb more than 60% of the incident source signal at a wavelength of 1400 nm to 1700 nm and provide a corresponding output electrical signal. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over a wavelength span of at least 20 nm of a source signal wavelength from 800 nm to 900 nm. 36. The photodetector of claim 35, wherein the photon absorption region is configured to absorb the incident source signal at an absorption percentage that varies by less than 20% over a wavelength span of at least 20 nm of a source signal wavelength between 1400 nm and 1700 nm. Each hole has a cross section parallel to the top surface of the substrate and has a maximum dimension between 400 nm and 2500 nm, and each hole is adjacent to the nearest of the plurality of holes. 36. The photodetector of claim 35, having a center spaced from the center of the hole by less than 3500 nm. The photodetector further comprises a P layer and an N layer that are highly doped at or beyond 10^{19} / cm^3 and located on the sides of the photon absorption region; and photodetector of claim 35, wherein said photon absorbing region in the or intentionally being lightly doped is at most 10^{16} / cm^3 being undoped. 36. The photodetector of claim 35, wherein the photodetector comprises an avalanche photodetector. 36. The photodetector of claim 35, wherein the photon absorption region comprises Si. 36. The photodetector of claim 35, wherein the photon absorption region comprises Ge. The photodetector has a tapered or stepped hole configured to receive an optical fiber carrying the source signal and maintain one end of the fiber at a selected distance from the photon absorption region. 36. The photodetector of claim 35. 50. The photodetector of claim 49, further comprising a lens between the end of the fiber and the photon absorption region. 36. The photodetector of claim 35, wherein the photodetector has a reflective structure configured to generate a plurality of reflections of the source signal such that the source signal traverses the photon absorption region a plurality of times. . 36. The light detector of claim 35, wherein the light detector is configured to receive the source signal from two corresponding sides of the photon absorption region. In a photodetector having a microstructure-enhanced light absorption.

Cathode region;

Anode region;

A reverse bias circuit configured to apply a voltage between the cathode region and the anode region such that the cathode region is driven to a more positive voltage than the anode region;

A substrate material having an upper surface; and a photon absorption region that is operatively associated with the cathode region and the anode region and configured to absorb photons from a source signal and is composed of silicon. A plurality of holes, each parallel to the upper substrate surface and having a maximum dimension between 400 nm and 2500 nm, each hole being less than 3500 nm from the center of the adjacent hole closest to the plurality of holes The photon absorption region having the plurality of holes having centers separated by a distance;

Having a light detector. 54. The photodetector of claim 53, wherein the source signal has a wavelength greater than 800 nm and less than 1000 nm. 54. The photodetector of claim 53, wherein the plurality of holes are arranged in an array that is periodically spaced. 55. The photodetector of claim 55, wherein the periodically spaced array has a hexagonal or square grid pattern. 54. The photodetector of claim 53, wherein the plurality of holes improve photon absorption in a wavelength range that includes the wavelength

of the source signal compared to a photodetector that has no holes but is otherwise identical. 54. The photodetector of claim 53, wherein each of the holes has a predominantly circular cross section that is parallel to the upper substrate surface. 54. The photodetector of claim 53, wherein the cathode region and the anode region are operatively connected to integrated circuit electronics, and the photodetector and integrated circuit electronics are integrated on a single silicon chip. 60. The photodetector of claim 59, wherein the integrated circuit electronics includes one or more types selected from the group consisting of mutual impedance amplifiers, signal processing electronics, and routing electronics. 60. The capacity associated with the photodetector is reduced compared to an otherwise identical photodetector that operatively connects its anode and cathode regions to a conventional bond pad. Light detector. Furthermore, it has a multiplication region formed from silicon, and the photodetector is configured to detect the source signal with a data bandwidth greater than 5 Gb / s at a source signal wavelength of 850 nm. 54. The photodetector of claim 53, wherein the photodetector is an avalanche photodiode having a gain greater than two. 54. The light detection of claim 53, wherein the light detector is configured to detect the source signal with a data bandwidth greater than 2.5 Gb / s at a source signal wavelength of 850 nm with a quantum efficiency of at least 30%. vessel. 54. The light detection of claim 53, wherein the light detector is configured to detect the source signal with a data bandwidth greater than 2.5 Gb / s at a source signal wavelength of 850 nm with a quantum efficiency of at least 50%. vessel. 54. The photodetector of claim 53, wherein the photodetector is configured to detect the source signal with a data bandwidth of 5 Gb / s or greater at a source signal wavelength of 850 nm with a quantum efficiency of at least 30%. 54. The photodetector of claim 53, wherein the photodetector is configured to detect the source signal with a data bandwidth of 5 Gb / s or more at a source signal wavelength of 850 nm with a quantum efficiency of at least 50%. 54. The photodetector of claim 53, wherein the plurality of holes are formed by etching away a portion of silicon

The light detector is configured such that a portion of the source signal passes through the photon absorption region for the first time, reflects off a surface, and then passes through the light absorption region for the second time. 54. The photodetector of claim 53. And further comprising a substrate, and wherein the cathode region, the absorption region, and the anode region are formed above the substrate and the photodetector is opposite the substrate. 54. The photodetector of claim 53, wherein the photodetector is configured to receive the source signal from a direction facing the surface. In a photodetector having a microstructure-enhanced light absorption,

Cathode region,

Anode region,

A reverse bias circuit configured to apply a voltage between the cathode region and the anode region such that the cathode region is driven to a more positive voltage than the anode region;

A substrate material having an upper surface, and a photon comprising a germanium-based material that is operatively associated with the cathode region and the anode region and configured to absorb photons from a source signal. An absorption region, the germanium-based absorption region including a plurality of holes each having a cross-section parallel to the upper substrate surface and having a maximum dimension between 750 nm and 3000 nm. And each hole has a center having a center that is separated by less than 5000 nm from the center of the nearest neighboring hole of the plurality of holes,

Having a light detector. 71. The germanium-based photon absorption layer is formed above one or more layers of silicon material by at least one of an epitaxial growth and an epitaxial lateral overgrowth process. Photo detector. 72. The photodetector of claim 71, further comprising a Ge buffer layer configured to initiate Ge crystal growth on the top silicon layer. The photodetector of claim 70, wherein the anode region comprises a P doped germanium layer formed by at least one of an epitaxial growth and an epitaxial lateral overgrowth process. 71. The photodetector of claim 70, wherein the photodetector is an avalanche photodiode and further has a multiplication region made of silicon. 71. The photodetector of claim 70, wherein the source signal has a wavelength greater than 1200 nm and less than 1600 nm. 76. The photodetector of claim 75, wherein the source signal has a wavelength greater than 1400 nm. 72. The light detection of claim 70, wherein the light detector is configured to detect the source signal at a data bandwidth greater than 2 Gb / s at a source signal wavelength of 1330 nm with a quantum efficiency of at least 30%. vessel. 72. The light detection of claim 70, wherein the light detector is configured to detect the source signal in a data bandwidth greater than 2 Gb / s at a source signal wavelength of 1550 nm with a quantum efficiency of at least 50%. vessel. 71. The light detection of claim 70, wherein the light detector is configured to detect the source signal at a data signal bandwidth greater than 5 Gb / s at a source signal wavelength of 1550 nm with a quantum efficiency of at least 30%. vessel. 71. The light detection of claim 70, wherein the light detector is configured to detect the source signal at a data signal bandwidth greater than 5 Gb / s at a source signal wavelength of 1550 nm with a quantum efficiency of at least 50%. vessel.

Description

translated from Japanese

This patent application claims the priority of each of the following provisional applications and is incorporated herein by reference.

US Provisional Application No. 62 / 081,538, filed November 18, 2014 US Provisional Application No. 62 / 090,879, filed December 11, 2014 US Provisional Application No. 62 / 109,025, 2015 Filed on May 5 US provisional application number 62 / 111,582, filed February 3, 2015 US provisional application number 62 / 130,511, filed March 27, 2015 US provisional application number 62 / 153,443 Filed April 27, 2015 United States provisional application number 62 / 154,679, filed April 29, 2015 United States provisional application number 62 / 157,876, filed May 6, 2015 United States provisional application number 62 / U.S. Provisional Application No. 62 / 174,408, filed Jun. 11, 2015 U.S. Provisional Application No. 62 / 175,855, 201 US Provisional Application No. 62 / 182,602, filed June 15, 2015, U.S. Provisional Application No. 62 / 188,876, filed June 21, 2015, U.S. Provisional Application No. 62/197, filed July 6, 2015 , 120, filed July 27, 2015 US provisional application number 62 / 199,607, filed July 31, 2015 US provisional application number 62 / 205,717, filed August 15, 2015 United States provisional application No. 62 / 209,311, filed August 24, 2015 US provisional application number 62 / 213,556, filed September 2, 2015 US provisional application number 62 / 202,716, September 28, 2015 Applications This patent application is related to the following provisional and non-provisional applications, each of which is incorporated herein by reference.

International Patent Application No. PCT / US15 / 39268, filed May 22, 2014 United States provisional application number 61 / 826,446, filed May 22, 2013 United States provisional application number 61 / 834,873, June 2013 US Provisional Application No. 61 / 843,031, filed July 3, 2013 US Provisional Application No. 61 / 905,109, filed November 15, 2013 US Provisional Application No. 62 / 017,915, Application, June 27, 2014 All provisional and non-provisional patent applications cited above are collectively referred to herein as "commonly assigned and incorporated applications".

This patent specification generally presents an invention primarily related to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics.

Optical fiber communications are widely used in applications such as remote communications and communications within large data centers. Because of the attenuation loss associated with using shorter optical wavelengths, most optical fiber communications use optical wavelengths above 800 nm. A commonly used communication window exists between 800 nm and 1675 nm. The main part of an optical receiver used in an optical fiber communication system is a photodetector, which is usually in the form of a photodiode (PD) or an avalanche photodiode (APD).

A high quality, low noise APD can be composed of silicon. However, although silicon absorbs light in the visible and near infrared ranges, it becomes more transparent at longer optical wavelengths. Silicon PD and APD can be made for optical wavelengths above 800 nm by increasing the thickness of the absorption "I" region of the device. However, in order to obtain adequate quantum efficiency, the thickness of the silicon "I" region is too low for the current and future telecommunications and data center applications where the maximum bandwidth of the device is large. It becomes very big.

Other materials are used to avoid the inherent problems that silicon PD and APD have for longer wavelengths and higher bandwidths. Germanium (Ge) detects infrared up to a wavelength of 1700 nm, but has a relatively high multiplication noise. InGaAs can detect even longer than 1600 nm and has less multiplication noise than Ge, but has much higher multiplication noise than silicon. It is known that InGaAs is most typically used as an absorption region for heterostructure diodes involving InP as a substrate and as a multiplication layer. This material system is compatible with an absorption window of approximately 900-1700 nm. However, both InGaAs devices are relatively expensive and have relatively high multiplication noise when compared to silicon, and are difficult to integrate with Si electronics as a single chip.

information published by major companies in the photodetector business (http://files.shareholder.com/downloads/FNSR/0x0x281377/0b3993ea-f808-417d-ac71-84f2f9084b0d/Finisar_Investor_Presentation.pdf) shows on page 18 that the current market for optical communications equipment is 7 billion US it is above the dollar and the compound annual growth rate is 12%. The photodiode (PD) used for the 850 nm wavelength uses a GaAs material, and for the 1550 nm wavelength, the photodiode is based on an InP material, which is expensive and Si-based electronics. It is difficult to integrate with. Thus, there is a long market and there is a long-standing need for the development of better equipment. To date, neither a photodiode based on a Si material for 850 nm nor an avalanche photodiode (APD) exists, and the data rate is 5 Gb / s or more in the top or bottom irradiation type. As is known, there are no commercially available photodiodes or avalanche photodiodes based on Ge / on / Si (Ge on Si) materials for 1550 nm. However, the effort to develop better devices for such a large market was not lacking. For example, a proposal has been made for a resonant photodiode manufactured in Si material (Resonant Cavity Enhanced High-Speed Si Photodiodes Grown by Epitaxial Lateral Overgrowth) Schaub et al., IEEE Photonics Technology Letters, Vol. 11, No. 12, December 1999), but it has not become recognized in the market. Other types of high speed photodiodes in waveguide form have been proposed, for example, a reference 40 GHz Si / Ge uni-travelling carrier waveguide photodiode (Ref. 40 GHz Si / Ge uni-travelling carrier waveguide photodiode), Piels et al. , DOI 10.1109 / JLT. 2014.2310780, Journal of Lightwave Technology, Monolithic Ge / Si Avalanche Photodiodes, Kang et al., 978-1-4244-4403-6 / 09 / $ 25.00 Copyright 2009 IEEE; High-speed Ge monolithically integrated with large cross-section silicon-on-insulator waveguide, Feng et al. Applied Physics Letters 95, 261105 (2009), doi: 10.1063 / 1.3279129, in which case light is coupled into the optical waveguide from the edge and the absorption length is Ge at 1550 nm. 100um or more to compensate for weak absorption coefficient It is possible to in these previously proposed waveguide photodiode structures, light propagates along the length of the waveguide and the PIN waveguide is such that the direction of light propagation and the direction of the electric field are predominantly perpendicular. An electric field is applied across Since light travels about 1000 times faster than the electron / hole saturation rate in Si, the waveguide PD should be, for example, 200 microns long and the "i" in the PIN should be, for example, 2 microns. And a bandwidth exceeding 10 Gb / s can be achieved. Such end coupling of light is costly in packaging compared to surface illumination as described in this patent specification, where the waveguide cross-sectional dimensions are typically a few microns, in contrast to the case of a known surface-illuminated photodiode or avalanche photodiode, it is several tens of microns. Known waveguide PD / APDs are often only single-mode optics, whereas surface-illuminated PD / APDs described in this patent are both single-mode and multimode optics. It is possible to use. In addition, known waveguide photodiodes are difficult to test at the wafer level, whereas the surface illuminated photodiodes described in this patent specification can be easily tested at the wafer level. Known waveguide / avalanche photodiodes are mostly used in special photonic circuits and are not widely available on the market. Top / bottom-illuminated Si and Ge on-Si PD / APD that can be integrated with Si are commercially available with data rates of 5 Gb / s or higher at wavelengths of 850 nm and 1550 nm. That is ignorant. In contrast, photodiodes on Si based materials as described in this patent specification can be monolithically integrated with integrated electronics on a single Si chip, in which case Significantly reducing the cost of packaging. Furthermore, the microstructured PD / APD described in this patent specification at a nominal wavelength of 850 nm can be predominantly for short distances, for example less than 1 meter, and in some cases Optical data transmission distances can be less than 10 meters, and in some cases less than 100 meters, and in some cases less than 1000 meters. The electric field in the microstructured PD / APD direction of the incident optical beam and in the "i" region of the PIN or NIP structure is predominantly collinear and / or approximately collinear. This patent specification is expected to make such devices possible and convert the current data center between blades and / or almost all to optical data transmission within a blade, and that Significantly increases data transmission bandwidth capability and significantly reduces power consumption.

The spirit and scope of the claims are not limited to embodiments that solve any particular disadvantages or that operate only in environments such as those described above. Rather, this background is provided to illustrate one exemplary technology area in which some embodiments described herein may be implemented.

Resonant Cavity Enhanced High-Speed Si Photodiodes Grown by Epitaxial Lateral Overgrowth, Schaub et al., IEEE Photonics Technology Letters, Vol. 11, December 1999 Reference 40 GHz Si / Ge single traveling carrier waveguide photodiode (Ref. 40 GHz Si / Ge uni-travelling carrier waveguide photodiode), Piels et al., DOI 10.1109 / JLT. 2014.2310780, Journal of Lightwave Technology Monolithic Ge / Si Avalanche Photodiodes, Kang et al., 978-1-4244-4403-6 / 09 / $ 25.00 Copyright 2009 IEEE High-speed Ge photolithographic monolithically integrated with large cross-section silicon-on-insulator waveguide, Feng et al., Applied Physics Letters 95, 261105 (2009) doi: 10.1063 / 1.3279129

According to some embodiments, an integrated detector / processor circuit for data communication includes a photodetector with microstructure enhanced optical absorption, and an electronic processor formed on a single semiconductor chip. Have.

The single chip includes a photon absorption region configured to absorb photons from an optical source signal modulated for data communication and to provide a corresponding output electrical signal. The photon absorption region is a plurality of holes extending therethrough toward the substrate, wherein the same source signal is transmitted through the plurality of holes. The plurality of holes configured to receive simultaneously, and an electronic processor is also formed on the semiconductor substrate and is operatively associated with the photon absorption region to receive the output electrical signal. Forming a single semiconductor chip that receives the optical source signal and outputs the processed output, thereby processing the photon absorption region and the electron The processors have respective thicknesses of the same magnitude, and a cathode region and an anode region are operatively associated with the photon absorption region and a reverse bias circuit, the reverse bias circuit being in the cathode region is configured to apply a voltage between the cathode region and the anode region so as to be driven to a more positive voltage than the anode region.

The thickness of the photon absorption region is preferably in the range of 0.5 to 5 μm. The electronic processor can be an application specific integrated circuit (ASIC) having at least one of complementary metal oxide semiconductor (CMOS) devices, bipolar (B) devices, and BiCMOS devices, is there. The photon absorption region is configured to absorb more than 40%, 50%, or 60% of the incident source signal at a wavelength of 800 nm to 900 nm, or 1400 nm to 1700 nm, and provide a corresponding output electrical signal. It is possible. The photon absorption region may be configured to provide the incident source signal at an absorption percentage that varies by less than 20% over a selected wavelength range of at least 20 nm of a source signal wavelength of 800 nm to 900 nm, or 1400 nm to 1700 nm. Is possible.

Each hole has a maximum dimension between 400 nm and 2500 nm and can have a cross section parallel to the surface of the substrate, and each hole is the closest of the plurality of holes. It is possible to have a center that is separated from the center of the adjacent hole by less than 3500 nm. The photodetector preferably further comprises a P layer and an N layer that are highly doped at or beyond 10^{19} / cm^3 and located on the sides of the photon absorption region. And the photon absorption region is preferably lightly doped or intentionally undoped and at most 10^{15} / cm^3. The photodetector can include an avalanche photodetector and the photon absorption region can include at least one of Si and Ge. The photodetector may have a tapered or stepped hole configured to receive an optical fiber carrying the source signal and to maintain an end of the fiber at a selected distance from the photon absorption region. Is possible. A lens can be included between the end of the fiber and the photon absorption region. The photodetector may further include a reflective structure configured to generate multiple reflections of the source signal, thereby causing the source signal to traverse the photon absorption region multiple times. The light detector can be configured to receive the source signal from two opposite sides of the photon absorption region, and the holes are adapted to convert light into electrical signals in groups of the holes. It is possible to generate a coupled resonance, thereby improving the source signal absorption.

One or more additional photodetectors can be formed on the semiconductor substrate, each receiving a respective additional source signal and providing a corresponding respective output electrical signal. A photon absorption region, and one or more additional electronic processors are formed on the semiconductor substrate and the additional output electrical signals are received and processed therefrom. It can also be operatively associated with each photon absorption region of the photodetector. The plurality of holes have no holes in a plurality of wavelength ranges including the wavelength of the source signal, but the others can be configured to improve photon absorption as compared with the same photodetector. The electronic processor may include one or more types selected from the group consisting of mutual impedance amplifiers, signal processing electronics, and routing electronics. The capacitance associated with the photodetector is reduced compared to the

same photodetector, except that the anode and cathode regions are operatively connected to a conventional bond pad. The photodetector can further have a multiplication region, which is an avalanche photodiode that detects the source signal with a data bandwidth greater than 10 gigabits / s at a source signal wavelength of 800-900 nm. And has a gain greater than 2.

In some embodiments, in an optical / electronic system, a photodetector and active electronic circuitry are provided that are built on the same semiconductor substrate and are operatively associated with each other. A laser is provided that forms a single integrated circuit chip and is modulated at the Gb / s rate of data to generate the optical source signal carrying information at the Gb / s rate; and An optical fiber is provided in association with the laser to receive the optical source signal at its input and send it to its output, in which case the photodetector detects the optical source signal. Associated with the output end of the optical fiber for receiving and configured to convert it to an electrical output signal, and the active electronic circuit comprises: There is a light detector to process and electrical output signal being associated with and configured to output an electrical signal of the processed to receive the output electrical signal. Each of the source signal and the electrical output signal can be modulated at a rate of at least 5 Gb / s. The photodetector and the active electronic circuit can have a similar thickness. The photodetector can have a photon absorption region that includes a plurality of holes extending toward the semiconductor substrate, in which case the plurality of holes receive the same source signal. It is supposed to be received at the same time. Highly doped P and N layers can be located on the sides of the photon absorption region, and the photon absorption region can have a thickness in the range of 0.1 to 5.0 μm. Yes, and preferably not intentionally doped or lightly doped compared to the P and N regions. The photodetector can be biased to sweep electrons or holes in a direction along the direction in which the source signal is received by the photodetector. Each of the photodetector and the active electronic circuit may be silicon based. The photodetector can be an avalanche photodetector.

In some embodiments, the photodetector with microstructure enhanced light absorption preferably has a thickness between 0.5 μm and 5 μm and is modulated for data communication. A photon absorption region configured to absorb a photon from a source signal and supply an output electrical signal corresponding to the photon absorption region, wherein the photon absorption region passes through at least part of the thickness of the photon absorption region. A plurality of extending holes, wherein the plurality of holes are configured to simultaneously receive the same source signal in the plurality of holes, and the photon absorption region is 800 nm to Absorbs more than 40% of the incident source signal at a wavelength in 900 nm and at least one of the ranges 1400 nm to 1700 nm and provides a corresponding output electrical signal. It is supposed to be a form to pay. The photon absorption region can be configured to absorb incident source signals at an absorption percentage that varies by less than 20% over a wavelength range of at least 20 nm of a source signal wavelength of 800 nm to 900 nm or 1400 nm to 1700 nm.

Each hole preferably has a cross section parallel to the top surface of the substrate having a maximum dimension between 400 nm and 2500 nm, and each hole is preferably within the plurality of holes. Has a center that is separated by less than 3500 nm from the center of the adjacent hole. The photodetector further comprises a P layer and an N layer, which are preferably highly doped at or above 10^{19} / cm^3 and in the photon absorption region. Located on the side and the photon absorption region is preferably intentionally undoped or lightly doped at most 10^{19} / cm^3. The photodetector can comprise an avalanche photodetector. The photon absorption region can comprise Si or Ge. The photodetector has a tapered or stepped hole configured to receive an optical fiber carrying the source signal and to maintain an end of the fiber at a selected distance from the photon absorption region. A lens can be included between the end of the fiber and the photon absorption region. The light detector may have a reflective structure configured to generate multiple reflections of the source signal, thereby traversing the photon absorption region multiple times with the source signal. The light detector may be configured to receive the source signal from two opposite sides of the photon absorption region.

In some embodiments, a photodetector with microstructure enhanced light absorption includes a cathode region, an anode region, and the cathode region such that the cathode region is driven to a more positive voltage than the anode region. A reverse bias circuit configured to apply a voltage between the anode region, a substrate material having an upper surface, and a photon from a source signal that is operatively associated with the cathode region and the anode region. A photon absorption region composed of silicon, the silicon absorption region being parallel to the upper substrate surface, each having a maximum dimension between 400 nm and 2500 nm. A plurality of holes having a uniform cross section, and each hole is located 85 from the center of the nearest adjacent hole of the plurality of holes. By less than 6nm are spaced apart. The source signal can have a wavelength greater than 800 nm and less than 1000 nm. The plurality of holes can be arranged in a periodically spaced array that can have a hexagonal or square grid pattern. The plurality of holes improve photon absorption compared to those without holes, but the others are the same photodetectors in the wavelength range including the wavelength of the source signal. Each of the holes may have a predominantly circular cross section parallel to the upper substrate surface. The cathode region and anode region can be operatively connected to integrated circuit electronics, and the photodetector and integrated circuit electronics can be integrated on a single silicon chip, in which case the The integrated circuit electronics can include one or more types selected from the group consisting of mutual impedance amplifiers, signal processing electronics, and routing electronics. The capacitance associated with the photodetector can be reduced compared to the same photodetector, except that its anode and cathode regions are operatively connected to a conventional bond pad. The photodetector may further have a multiplication region formed from silicon, in which case the photodetector has a gain greater than 2 at a source signal wavelength of 850 nm. An avalanche photodiode configured to detect the source signal in a data bandwidth greater than 5 Gb / s. The photodetector may be configured to detect the source signal at a data bandwidth of 2.5 Gb / s or higher at a source signal wavelength of 850 nm with a quantum efficiency of at least 30% or 50%, or 5 Gb / s or higher, is possible. The plurality of holes can be formed by etching away a part of silicon. The photodetector can be configured such that a portion of the source signal first passes through the photon absorption region, reflects off the surface, and then passes again through the photon absorption region. The photodetector can further include a substrate, in which case the cathode, absorption and anode regions are formed above the substrate and the photodetector is on the opposite side of the substrate. The source signal is received from the direction facing the side of the photodetector.

In some embodiments, a photodetector with microstructure enhanced light absorption includes a cathode region, an anode region, and the cathode region such that the cathode region is driven to a more positive voltage than the anode region. A reverse bias circuit configured to apply a voltage between the cathode region and the anode region, a substrate material having an upper surface, and photons from the source signal that are operatively associated with the cathode region and the anode region And a photon absorption region composed of a germanium-based material, each of the germanium-based absorption regions having a maximum dimension between 750 nm and 3000 nm. A plurality of holes having a cross-section parallel to the surface of the upper substrate and each hole being a plurality of holes Nearest neighbor of the inner has a center which is spaced from the center of the hole by less than 9000 nm. The germanium-based photon absorption layer may be formed on one or more layers of silicon material by at least one of an epitaxial growth and an epitaxial lateral overgrowth process. Is possible. The photodetector may further include a Ge buffer layer configured to initiate Ge crystal growth on the top silicon layer. The anode region of the photodetector can have a P-doped germanium layer formed by at least one of an epitaxial growth and an epitaxial lateral overgrowth process. The photodetector can be an avalanche photodiode and can further have a multiplication region formed from silicon. The source signal can have a wavelength greater than 1260 nm and less than 1900 nm, or greater than 1400 nm. The photodetector can be configured to detect the source signal in a data bandwidth greater than 2 Gb / s or 5 Gb / s at a source signal wavelength of 1550 nm with a quantum efficiency of at least 30% or 50%, is there.

As used in this document, grammatical conjunctions such as "and", "or", and "and / or" are all examples of their connection, it is intended to represent that one or more of the objects, subjects may occur or exist. Thus, as used in this document, the term "or" in all cases means "inclusive or" rather than "exclusive or". Represents.

As used herein, the term "single hole" or "multiple holes" refers to an opening into or through a substance or substances. I mean. In general, the openings can have any shape and cross section including circular, elliptical, polygonal, and random shapes.

To further clarify the above and other advantages and features of the subject matter of this patent specification, specific examples of embodiments thereof are illustrated in the accompanying drawings. It should be understood that these drawings are merely illustrative of the embodiments and are not to be considered as limiting

the patent specification or the claims. The subject matter of this document will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

1 is a schematic diagram illustrating an optical data transmission system that can use a microstructured photodiode / avalanche photodiode according to some embodiments. FIG. FIG. 4 is a schematic diagram illustrating wavelength selective elements included with a microstructured photodiode (MS-PD) and a microstructured avalanche photodiode (MS-APD) according to some embodiments. 1 is a schematic diagram illustrating an MS-PD / APD with a multi-wavelength selection element according to some embodiments. FIG. (A)-(D) are each plot showing various bandpass filter characteristics according to some embodiments. 1 is a schematic diagram illustrating a coarse wavelength division multiplexing (CWDM) configuration according to some embodiments. FIG. (A) and (B) are schematic diagrams showing some basic parts of a microstructured photodiode according to some embodiments. (A) and (B) are schematic diagrams showing some basic parts of a bottom-illuminated photodiode according to some embodiments. (A) and (B) are schematic diagrams showing some basic parts of an MS-APD structure according to some embodiments. (A) and (B) are schematic diagrams showing aspects of a selective area growth (SAG) APD structure before and after III-V or Ge SAG according to some embodiments. 1 is a schematic diagram illustrating a simplified microstructured silicon photodiode with a PIN epitaxial layer according to some embodiments. FIG. 1 is a schematic diagram illustrating a simplified microstructured silicon photodiode with a PIN epitaxial layer according to some embodiments. FIG. FIGS. 4A to 4C are schematic diagrams illustrating simplified microstructured silicon photodiodes having PIN epitaxial layers according to some embodiments. FIGS. 1 is a schematic diagram illustrating an epitaxial layer structure for a high contrast microstructured photodiode (PD) with P-I-N doping according to some embodiments. FIG. 1 is a schematic diagram illustrating an epitaxial layer structure for a high contrast microstructured photodiode (PD) with P-I-N doping according to some embodiments. FIG. 1 is a schematic diagram illustrating an epitaxial layer structure for a high contrast microstructured photodiode (PD) with P-I-N doping according to some embodiments. FIG. 1 is a schematic diagram illustrating several aspects of manufacturing a high contrast microstructured photodiode (PD) according to some embodiments. FIG. (A) thru | or (D) each schematic which has shown the example of the hole arrangement | sequence, space | interval, dimension, and passivation layer based on some Examples. FIG. 3 is a schematic diagram illustrating some additional aspects of manufacturing a high contrast microstructured photodiode (PD) according to some embodiments. FIG. 3 is a schematic diagram illustrating some additional aspects of manufacturing a high contrast microstructured photodiode (PD) according to some embodiments. FIG. 3 is a schematic diagram illustrating some additional aspects of manufacturing a high contrast microstructured photodiode (PD) according to some embodiments. FIG. 3 is a schematic diagram illustrating several aspects of manufacturing a high contrast microstructured photodiode (PD) according to some other embodiments. (A) And (B) is each schematic which has shown the simulation side surface of the specific microstructure type PD based on some Example. 1 is a schematic diagram illustrating certain aspects of a high contrast microstructure PD according to some embodiments. FIG. 1 is a schematic diagram illustrating certain aspects of a heteroepitaxial microstructure PD according to some embodiments. FIG. 1 is a schematic diagram illustrating a high contrast structure for an optical light emitter such as a light emitting diode (LED) or vertical surface emitting laser (VCSEL) according to some embodiments. 1 is a schematic diagram illustrating a basic structure for, for example, a high contrast 1.3 micron wavelength photo emitter, according to some embodiments. 1 is a schematic diagram illustrating some basic features of a high contrast microstructured photoemitter (PE) with holes etched according to some embodiments. FIG. 3 is a schematic diagram illustrating several aspects of a PE according to some other embodiments. FIG. 3 is a schematic diagram illustrating several aspects of a PE according to some other embodiments. FIG. 3 is a schematic diagram illustrating several aspects of a PE according to some other embodiments. 1 is a schematic diagram illustrating several aspects of a simple PIN photodiode structure according to some embodiments. 1 is a schematic diagram illustrating certain aspects of MS-PD manufacturing according to some embodiments. FIG. 1 is a schematic diagram illustrating certain aspects of MS-PD manufacturing according to some embodiments. FIG. 1 is a schematic diagram illustrating certain aspects of MS-PD manufacturing according to some embodiments. FIG. 1 is a schematic diagram illustrating certain aspects of MS-PD manufacturing according to some embodiments. FIG. 1 is a schematic diagram illustrating certain aspects of MS-PD manufacturing according to some embodiments. FIG. FIG. 5 is a schematic diagram illustrating one technique for reducing minority carrier lifetime based on some other embodiments. (A) thru | or (C) is each explanatory drawing which shows the various parameters with respect to several simulated micro structure type photodiodes. The graph which plotted the simulation result of the micro structure type | mold hole photodiode. 1 is a schematic diagram illustrating a microstructured avalanche photodiode (APD) having a P-I-P-N epitaxial structure according to some embodiments. FIG. FIG. 2 is a schematic diagram illustrating a microstructured avalanche photodiode (APD) with a P-I-P-I-N epitaxial structure according to some other embodiments. 1 is a schematic diagram illustrating a microstructured APD comprising a Ge absorption layer and a GaP capping layer according to some embodiments. (A) thru | or (D) is each explanatory drawing which showed the polarization (polarization) sensitivity of the micro structure type photodiode and APD based on some Examples. 1 is a schematic diagram illustrating an MS-PD / APD integrated with a mutual impedance amplifier and / or other ASIC (Application Specific Integrated Circuit) according to some embodiments. FIG. FIG. 2 is a schematic diagram illustrating several aspects of a flip-chip arrangement for MS-PD / APD with TIA and / or other signal processing ICs integrated on a single silicon chip according to some embodiments. Schematic showing some aspects of a flip-chip arrangement for MS-PD / APD with TIA and / or other signal processing ICs integrated on a single silicon chip according to some other embodiments. Figure. Schematic showing some aspects of a flip-chip arrangement for MS-PD / APD with TIA and / or other signal processing ICs integrated on a single silicon chip according to some other embodiments. Figure. Schematic showing some aspects of a flip-chip arrangement for MS-PD / APD with TIA and / or other signal processing ICs integrated on a single silicon chip according to some other embodiments. Figure. Schematic showing some aspects of a flip-chip arrangement for MS-PD / APD with TIA and / or other signal processing ICs integrated on a single silicon chip according to some other embodiments. Figure. Schematic showing some aspects of a flip-chip arrangement for MS-PD / APD with TIA and / or other signal processing ICs integrated on a single silicon chip according to some other embodiments. Figure. FIG. 2 is a schematic diagram illustrating an array of MS-PD / APD integrated with IC electronics such as TIA and / or other signal processing and routing electronics on a single silicon chip according to some embodiments. 1 is a schematic diagram illustrating an epitaxial structure for high data rate MS-PD according to some embodiments. FIG. 1 is a schematic diagram illustrating an epitaxial structure for high data rate MS-PD according to some embodiments. FIG. 1 is a schematic diagram illustrating an epitaxial structure for high data rate MS-PD according to some embodiments. FIG. Table showing mesa dimensions, hole diameter, hole period distance, and grid pattern for MS-PD according to some examples. (A) and (B) are schematic diagrams showing hexagonal and square lattice hole patterns according to some embodiments. 1 is a schematic diagram illustrating an epitaxial layer structure for silicon MS-PD according to some embodiments. FIG. 1 is a schematic diagram illustrating certain aspects of an MS-PD according to some embodiments. 1 is a schematic diagram illustrating certain aspects of an MS-PD according to some embodiments. 1 is a schematic diagram illustrating certain aspects of an MS-PD according to some embodiments. 1 is a schematic diagram illustrating a Ge-on-Si PIN epitaxial layer structure for MS-PD according to some embodiments. FIG. 1 is a schematic diagram illustrating certain aspects of a Ge-on-Si MS-PD according to some embodiments. FIG. 1 is a schematic diagram illustrating certain aspects of a Ge-on-Si MS-PD according to some embodiments. FIG. 1 is a schematic diagram illustrating certain aspects of a Ge-on-Si MS-PD according to some embodiments. FIG. 1 is a schematic diagram illustrating certain aspects of a Ge-on-Si PD according to some embodiments. FIG. 1 is a schematic diagram illustrating certain aspects of a Ge-on-Si PD according to some embodiments. FIG. 1 is a schematic diagram illustrating certain aspects of an MS-APD according to some embodiments. 1 is a schematic diagram illustrating certain aspects of an MS-APD according to some embodiments. 1 is a schematic diagram illustrating an MS-APD without a SiO_2 layer according to some embodiments. FIG. 1 is a schematic diagram illustrating a Ge-on-Si microstructure avalanche photodiode (MS-APD) according to some embodiments. FIG. 1 is a schematic diagram illustrating a Ge-on-Si microstructure avalanche photodiode (MS-APD) according to some embodiments. FIG. 1 is a schematic diagram illustrating a Ge-on-Si microstructure avalanche photodiode (MS-APD) with an etch stop layer according to some embodiments. 1 is a schematic diagram illustrating a Ge-on-Si microstructure avalanche photodiode (MS-APD) according to some embodiments. FIG. FIG. 3 is a schematic diagram illustrating another SINIP epitaxial layer structure for MS-PD according to some embodiments. (A) thru | or (C), each schematic which shows the SIN-IP epitaxial layer on the buried oxide for MS-PD based on some Examples. 1 is a schematic diagram illustrating an MS-PD comprising a SINIP epitaxial layer and a SiGeB etch stop layer on a PEI substrate according to some embodiments. FIG. 2 is a schematic diagram illustrating a Ge-on-Si NIP on a SiGeB epitaxial layer structure for MS-PD according to some embodiments. 1 is a schematic diagram illustrating a Ge-on-Si epitaxial structure for MS-PD according to some embodiments. FIG. 3 is a schematic diagram illustrating another Ge-on-Si epitaxial structure according to some embodiments. 1 is a schematic diagram illustrating a Ge-on-Si epitaxial structure according to some

embodiments. FIG. 80 is an explanatory diagram relating to a simulation using a finite difference time domain (FDTD) for a Ge-on-Si microstructure photodiode similar to the structure illustrated in FIG. 79; FIG. 80 is an explanatory diagram relating to a simulation using a finite difference time domain (FDTD) for a Ge-on-Si microstructure photodiode similar to the structure illustrated in FIG. 79; FIG. 80 is an explanatory diagram relating to a simulation using a finite difference time domain (FDTD) for a Ge-on-Si microstructure photodiode similar to the structure illustrated in FIG. 79; FIG. 81 is an explanatory diagram relating to a simulation using a finite difference time domain (FDTD) for a Ge-on-Si microstructure photodiode similar to the structure in FIG. FIG. 81 is an explanatory diagram relating to a simulation using a finite difference time domain (FDTD) for a Ge-on-Si microstructure photodiode similar to the structure in FIG. FIG. 81 is an explanatory diagram relating to a simulation using a finite difference time domain (FDTD) for a Ge-on-Si microstructure photodiode similar to the structure in FIG. 79 is a graph showing the results of a simulation using a finite difference time domain (FDTD) for a Ge-on-Si microstructured photodiode similar to the structure in FIG. 79 is a graph showing the results of a simulation using a finite difference time domain (FDTD) for a Ge-on-Si microstructured photodiode similar to the structure in FIG. 1 is a schematic plan view of a microstructure type photodiode chip according to some embodiments. FIG. FIG. 2 is a schematic plan view illustrating an MS-PD / APD integrating a transimpedance amplifier and / or other electronics on a single chip according to some embodiments. Schematic showing a simple epitaxial structure with no microstructure. Schematic showing another simple epitaxial structure with no microstructure. FIG. 83 is a schematic diagram illustrating the same epitaxial structure as in FIG. 87 when a microstructured hole array is etched into a SiP epitaxial layer according to some embodiments. FIG. 89 is a schematic showing the same epitaxial structure as in FIG. 88 when etching a microstructured hole array into a BOXSiO $_2$ layer according to some embodiments. Plot showing simulation results for the exemplary structure illustrated in FIGS. 87-90. Plot showing simulation results for the exemplary structure illustrated in FIGS. 87-90. FIG. 2 is a schematic diagram illustrating a microstructured region in silicon when holes are etched into silicon according to some embodiments. 1 is a schematic diagram illustrating an MS-PD structure with tapered holes according to some embodiments. FIG. FIG. 3 is a schematic diagram illustrating an MS-PD structure with gradually tapered holes according to some embodiments. FIG. 4 is a schematic diagram illustrating a material structure with microstructured holes of different diameters according to some embodiments. FIG. 96 is a plan view of a material structure having microstructured holes of different diameters as illustrated in FIG. The graph which shows the absorption with respect to the light which injects on the microstructure which comprises the layer structure as shown to FIG. 82A. The graph which shows the absorption with respect to the light which injects on the microstructure which comprises the layer structure as shown to FIG. 82A. FIG. 82B is a graph showing simulated absorption for the structure shown in FIG. 82A and simulated in FIGS. 97A and 97B. FIG. 3 is a schematic diagram illustrating another preferred epitaxial structure for a Si avalanche photodiode for operation in the wavelength range of 800 to 1000 nm, according to some embodiments. 1 is a schematic diagram illustrating some features of a microstructured APD according to some embodiments. FIG. Schematic showing some features of microstructured Ge-on-SiAPD. (A) to (C) are diagrams illustrating diameters, periods, and other parameters for microstructured silicon and Ge-on-Si photodiodes and avalanche photodiodes based on some embodiments. . (A) and (B) are simulation results using FDTD (Finite Difference Time Domain) for the absorption-wavelength for the structure shown in FIG. Showing each graph. (A) And (B) is each explanatory drawing for demonstrating the eigenmode with respect to the square lattice hole pattern based on some Examples. FIG. 2 is a schematic diagram illustrating a microstructured hole comprising two square grids arranged to overlap each other according to some embodiments. 1 is a schematic diagram illustrating an epitaxial structure of Ge + on + Si according to some embodiments. FIG. 1 is a schematic diagram illustrating basic features of a Ge-on-Si microstructured photodiode according to some embodiments. FIG. (A) and (B) are graphs showing the results of FDTD simulations using Maxwell's equations for a microstructured hole array based on several examples. Absorption wavelength plots for microstructured / avalanche photodiodes with different hole diameters and grating periods based on some examples. FIG. 82B is a schematic diagram illustrating a simulation using the FDTD method of a structure as in FIG. 82A when two grids and two different hole diameters are used according to some embodiments. FIG. 82B is a schematic diagram illustrating a simulation using the FDTD method of a structure as in FIG. 82A when two grids and two different hole diameters are used according to some embodiments. FIG. 4 is a schematic diagram illustrating another lattice structure when two hexagonal lattices of the same period are combined and interfaced with each other according to some embodiments. Schematic showing a hexagonal grid with 6 unit cells where each cell has an eigenmode and some field propagation / distribution may be an extension of that eigenmode. 1 is a schematic diagram illustrating a SiN^{3} microstructured photodiode having a hole array and a textured surface according to some embodiments. FIG. The graph which shows the absorption coefficient of Si and Ge with respect to a wavelength. FIG. 6 is a graph showing improved effective absorption coefficient of Ge due to a microstructured hole array according to some embodiments. FIG. 6 is a graph showing improved absorption of Si microstructured PD / APD based on some examples.

A detailed description of some examples of preferred embodiments is given below. Although several embodiments will be described, the novel subject matter described in this patent specification is not limited to any one embodiment or combination of embodiments described herein, but many it should be understood to include alternatives, modifications, and equivalents. Furthermore, while a number of specific details are set forth in the following description to provide a thorough understanding, some embodiments may be practiced without some or all of these details. Further, for the convenience of explanation, certain technical materials known in the related art have not been described in detail in order to avoid unnecessarily blurring the new subject matter described herein. It will be apparent that one or several individual features of a particular embodiment described herein may be used in combination with features of other described embodiments. Moreover, like reference numbers and symbols in the various drawings indicate like elements.

According to some embodiments, a microstructure is used to improve the bulk absorption constant or absorption of the material at wavelengths in the vicinity of the band gap of the semiconductor material. This makes it possible to extend the operating optical wavelength and / or operating spectrum of the photosensor. The improved bulk absorption constant (ie, coefficient) is referred to as the effective absorption constant (ie, coefficient). The term "effective" is used because the absorption constant or coefficient is an intrinsic material property. However, if there are resonant effects, coupled resonant effects, slow wave effects, plasmon effects, field enhancement effects, scattering effects, near and subwavelength effects, linear and nonlinear effects, the effective absorption constant or coefficient is the bulk or material absorption constant. That is, it may be larger than the coefficient. Since the absorption depends exponentially on the product of the absorption coefficient and the absorption length, by maintaining the bulk absorption coefficient, the effective absorption length is the PD / APD "I "may be larger than the physical length of the absorption region. As used herein, the following terms are used interchangeably. Improved absorption constant, improved absorption coefficient, improved effective absorption constant, improved effective absorption coefficient, and Effective absorption constant, effective absorption coefficient, improved absorption length, effective absorption length, improved effective absorption length. The improved or effective absorption may be due to either or both an improved absorption coefficient and / or an improved absorption length.

According to some embodiments, improved absorption may have a dramatic effect on path length. In one bulk absorption example, the path length for photons to be absorbed for 1 / e of its original amplitude is 100 μm, while improved based on some embodiments described in this patent specification. Under absorption, the path length is 1 μm for the optical amplitude to attenuate to 1 / e of its original amplitude. Equivalently, if the path length is kept constant at 1 μm, the improved absorption coefficient is 100 times larger than the bulk absorption coefficient and / or the improved effective absorption length is 100 times the actual physical length. large

This is understood from the relationship of $A = A_0 e^{-\alpha L}$, where A is the attenuation amplitude of the incident photon flux A_0, α is an absorption coefficient, and L is a path length in which absorption is performed. Therefore, instead of making L 100 times longer, it is possible to define the effective α so that the effective α is 100 times larger than an unimproved absorption coefficient such as a bulk absorption coefficient. For example, the resonance / coupled resonance / scattering / near field effect of the microstructure provides 100 times longer path length uniformity, in which case the resonance / scattering / near field microstructure is only 1 micron long. Absent. A simpler description of this is that the photons in the resonant / coupled resonant structure make 99 reciprocations before reaching the value of 1 / e of its original amplitude, and therefore its uniform linear length is it is 100 times the length of. For convenience of explanation, resonance / coupled resonance / linear and nonlinear field enhancement / scattering / near-field effects will be collectively referred to herein as "resonant", which means resonance, coupled resonance, slow wave, it can include scattering, near field, plasmon, nonlinear and linear optical field effects.

As used herein, the terms "microstructure" and "microstructure type" refer to dimensions and / or dimensions in which at least one dimension is a micron scale, a submicron scale, and / or a subwavelength scale and / or a wavelength scale. It means various shapes of pillars, voids, holes and mesas.

According to some embodiments, the present technique for improving effective absorption is based on any combination of III-V materials, such as silicon, germanium, InP, GaAs, GaN, GaN, InGaAs, and III-V materials. It is possible to apply to various substances including As used herein, the term "substance group" of III-V materials is lattice matched or nearly lattice matched (within a few percent) to GaAs, InP, GaN, InSb semiconductors. Defined as any substance. For example, the InP material group can include InGaAs, InGaAsP, InAlAs, and InAs. According to some embodiments, in the case of microstructures, there is a thin buffer layer of selective area growth (SAG), epitaxial lateral overgrowth (ELOG), Ge or InGaAs or other III-V material in silicon microstructures. Re-growth, such as with or without epitaxial growth (EG), can be performed without the deleterious effects of lattice mismatch. This is because the size of the lattice mismatch material footprint on silicon is small (approximately a few microns to a submicron). This allows Ge and other III-V materials to be integrated with silicon without using conventional buffer layers (such as amorphous Si in the case of Ge-on-Si growth). The heterogeneous integration of multiple materials is a combination of homo- or heterostructures, crystalline and microcrystalline and amorphous semiconductors, conductors such as carbon, graphene, insulators, dielectrics, oxides, gases, liquids such as glass, Or it can be a polymer that can be semiconducting. Ge and III-V materials can also be grown on Si with or without buffer layers using SOG, ELOG, ES methods that can cover areas that cover the wafer scale from areas larger than a micron scale it is.

According to some embodiments, buried oxide (BOX), silicon-on-insulator (SOI), silicon-on-sapphire (SOS), amorphous semiconductor, etc. are used to reduce the effective refractive index. Low index materials such as low density semiconductors, nanowire semiconductors, voids and holes are used. Refractive index is an intrinsic property of a substance. However, according to some embodiments, structures such as voids, voids, and / or holes (which can be filled or partially filled with a low refractive index material) have dimensions on the order of optical wavelengths. In some cases, the optical electromagnetic field will see an average refractive index consisting of the material refractive index and the structure (which can be filled or partially filled with a low refractive index material). This average is referred to herein as the effective refractive index. According to some embodiments, it is not necessary to use a low index or low effective index material in the microstructure.

According to some embodiments, techniques for improving effective absorption can be applied to various materials, including silicon, germanium, III-V materials such as InP, GaAs, GaN, InGaAs, and any combination of III-V materials. It is possible to apply.

Due to the microstructure, capacitance can also be expressed in terms of effective capacitance: (1) the dielectric constant of one semiconductor and (2) the semiconductor, dielectric, gas, vacuum, partial vacuum, glass or A parallel capacitance with the dielectric constant of another substance that can be a liquid, such as a polymer (polyimide, mylar, or other organic compound). The effective capacity of the device is a combination of the capacities of parallel capacitors, which can be two or more. According to some embodiments, the advantage of using a microstructure is that its effective capacity can be significantly reduced from that of a uniform material such as a semiconductor. The RC time (resistive capacity) is one of basic times for determining the bandwidth of the photodiode and the avalanche photodiode. The lower capacity allows the device to have a larger area while maintaining a reasonably high data rate bandwidth and / or the fundamental time to determine the bandwidth of the PD / APD It is possible to increase the data rate bandwidth by reducing the thickness of the device in order to reduce the transit time of holes and / or.

According to some embodiments, the photosensor may be a photodiode (PD), avalanche photodiode (APD), photovoltaic cell (PV) or solar cell, or any optoelectronic device that converts photons to electrons. Is possible. According to some embodiments, emitters or emitters that convert electrons / holes into photons, such as lasers and light emitting diodes, can also be realized using microstructures.

According to some embodiments, the improved absorption results in APD / PD, (1) weak bulk absorption coefficient, eg, QE (quantum efficiency) is greater than 30% or greater than 50% and data bandwidth Expands the sensitivity of APD / PD to photons with energy (or wavelength) close to the material bandgap when A is greater than 3 Gb / s and about 1000 1 / cm or less, and (2) shorter absorption Operate with higher data rate bandwidth (eg, greater than 10 Gb / s) due to longer and shorter transit times, (3) increase quantum efficiency with improved absorption, and (4) for avalanche photodiodes it can be made of silicon with low excess noise and good multiplication characteristics, and (5) compatible with Si photonics and CMOS processes That. According to some embodiments, the PD / APD includes signal processing, signal amplification, memory, CPU, electrical transmitter, optical waveguide, integrated optics, and other ICs for specific applications, etc. It is possible to integrate with an ASIC (Application Specific Integrated Circuit). This is beneficial for mass production using CMOS foundries. In addition, surface (or bottom) illuminated PD / APD integrated with or without electronics can be tested with wafer level probing and can handle both single mode and multimode. It is. A single optical and electrical chip bypasses the need for a ceramic multichip carrier and significantly reduces assembly and packaging costs. Silicon benches can also be used in connection with optical alignment to optical components such as lenses, fibers, etc. as needed.

According to some embodiments, silicon is used for avalanche gain. Silicon has much lower noise than avalanche photodiodes. By integrating Ge with silicon, absorption occurs in the Ge material and electronic gain occurs in the silicon. Depending on the optical wavelength, eg, below 1100 nm, silicon can be used for both absorption and electronic gain, as well as the use of microstructures.

According to some embodiments, the absorption of photons in the semiconductor is improved using a microstructure. The microstructure provides greater absorption of photons for resonance, coupled resonance, field enhancement, near field and subwavelength effects, scattering, plasmons, linear and nonlinear optical fields, photonic crystals, and given physical length Absorption modes in high contrast gratings in the near-field region that can both effectively increase the effective absorption length and / or improve the absorption coefficient to the effective coefficient, both linear and non-linear effects Alternatively, it is possible to have an effect such as a loss mode.

According to some embodiments, the microstructure used for absorption enhancement for silicon photodiodes and / or avalanche photodiodes has a quantum efficiency of approximately due to increased length and / or modulus. > 50%, in some cases (IE> 70%, wavelength around 850 nm (which is the preferred wavelength for current data communications) and bandwidth 10 Gb / s (or equivalently, digital coding Depending on the format, there may be silicon PDs and APDs that exceed approximately 0.75 GHz.

Silicon optical detectors are very robust due to the maturity of materials and processing techniques, and their surfaces are free of dangling bonds that can generate surface states and carrier recombination centers. It can be easily passivated, and for APD applications, the ionization ratio between holes and electrons (k coefficient, silicon has a lower k coefficient than any III-V material) And low noise, and such detectors are CMOS compatible for integration with signal processing electronics and Si photonics.

According to some embodiments, the light-generated carrier is P for high modulation bandwidth (over 10 Gb / s bandwidth) and high quantum efficiency and for APD for high current gain with gain greater than 3 dB. -Swept out with an external reverse bias in the absorption "I" (sometimes referred to as "I") region of an I-N diode (PD) or P+-P-I-N diode (APD).

Microstructure photodiodes and avalanche photodiodes with bandwidths greater than 3 Gb / s are used in communications. Optical signals use techniques such as binary (intensity), phase / frequency shift (coherent, heterodyne communication), polarization (polarization) coding, multi-wavelength such as wavelength division multiplexing, and polarization multiplexing. And has information stamped on the light. The optical signal travels in the air and / or through a fiber and hits a microstructure photodiode and / or avalanche photodiode, where information imprinted on the optical signal can be extracted as an electrical signal it is. In some cases, it may be necessary to mix one or more other optical sources, such as in heterodyne or homodyne.

FIG. 1 is a schematic diagram illustrating an optical data transmission system capable of using the present microstructured photodiode / avalanche photodiode, according to some embodiments. The optical data transmission system 100 includes an optical source 110, a transmission medium 120 such as air and / or optical fiber, and a microstructure type photodiode / avalanche photodiode MS-PD / APD. According to some embodiments, the optical source 110 can be a laser. Electrical data 112 is imprinted on the optical signal with a power supply 114 that forward biases the laser 110 for direct modulation. The output of the laser 110 can be coupled to the optical fiber 120 via a coupler 122 such as a ball lens. The optical signal propagates through fiber 120 (or air) and can be coupled from fiber 120 to high speed microstructure photodiode / avalanche photodiode 130, for example via lens 124, where the optical signal is The converted data 132 and the resulting data 132 (consistent with data 112) is recovered. The microstructure photodiode / avalanche photodiode is reverse biased using a power supply 134.

According to some embodiments, a wavelength selective element can be integrated with the microstructured photodiode and the microstructured avalanche photodiode. In particular, an array of microstructured photodiodes / avalanche photodiodes is fabricated on a single chip that can contain application specific integrated circuits comprising, for example, CMOS, bi-CMOS, bipolar devices and circuits. It is possible. Wavelength selection elements such as bandpass filters can be used for coarse wavelength division multiplexing (CWDM), in which case each carries, for example, 10-40 Gb / s modulation data. Wavelengths of 810, 820, 830, 840, 850, 860, 870, and 880 nm can have an overall data rate of 80-320 Gb / s within a single transmission medium.

Examples of wavelength selective elements include high contrast subwavelength gratings, arrays of subwavelength holes in metal or dielectric films, and dielectric layers having alternating refractive indices, such as in Bragg reflectors. ing. The wavelength selective element may be a bandpass filter that includes a number of high contrast gratings to form a cavity resonator. The element can also be a combination of grating and other wavelength selective elements such as subwavelength hole arrays and / or Bragg mirrors on metal or semi-metal films.

Furthermore, the photodiode / avalanche photodiode microstructure itself can form reflectors such as high contrast gratings so that it can be both wavelength selective and absorption length enhanced. In particular, the photon absorption region of the photodiode / avalanche photodiode can be improved. According to some embodiments, additional high contrast gratings can be fabricated on top of microstructured / avalanche photodiodes to form a resonant optical cavity for wavelength selectivity. is there. If one of the high contrast gratings can be electrically biased to generate a voltage between the two wavelength selection elements, the selected wavelength, such as a tunable optical fiber, is used. It is possible to synchronize.

FIG. 2 is a schematic diagram illustrating wavelength selection elements included with a microstructured photodiode (MS-PD) and a microstructured avalanche photodiode (MS-APD), according to some embodiments. is there. Using the wavelength selection element 220, only wavelengths within the selected wavelength range are incident on the MS-PD / APD 130. According to some embodiments, the window can be 1-20 nm in width (eg, a central wavelength of 820 nm ± 5 nm, in which case the bandpass is 10 nm centered at 820 nm). In the case shown in FIG. 2, the high contrast grating 220 is made of silicon that can be integrated with the silicon MS-PD / APD 130. According to some embodiments, the microstructure feature 210 of the microstructured photodiode / avalanche photodiode 130 is itself wavelength selective in addition to the ability to improve the absorption characteristics of the photodiode / avalanche photodiode. It is also possible to operate as a container. If the microstructure 210 of the MS-PD / APD 130 is configured as a wavelength selector, the addition of a high contrast grating 220 forms a resonant cavity that can function as a bandpass filter.

FIG. 3 is a schematic diagram illustrating an MS-PD / APD having a plurality of wavelength selection elements according to some embodiments. In this case, a plurality of wavelength selection elements 320 and 322 are manufactured and integrated within the MS-PD / APD 130. Wavelength selection elements 320 and 322 are dual high contrast gratings that function as bandpass filters. According to some embodiments, it is possible to produce a tunable bandpass filter when a voltage is applied to one wavelength selection element relative to the other.

FIGS. 4A to 4D are graphs showing various bandpass filter characteristics based on some embodiments. In the plots in FIGS. 4A, 4B, 4C, and 4D, the center wavelengths are 820, 830, 840, and 850 nm, respectively, and "R" is the reflectance. For example, at the center wavelength for a bandwidth of 10 nm, the reflectivity is practically zero and most of the light is transmitted, while outside the bandwidth, the reflectivity is almost 100% and the transmission is actually Top zero.

FIG. 5 is a schematic diagram illustrating a coarse wavelength division multiplexing (CWDM) configuration according to some embodiments. In this case, four wavelengths propagate through a transmission medium in which the center wavelengths are 820, 830, 840, and 850 nm and each has a modulation data rate of 25 Gb / s with respect to a total data rate of 100 Gb / s. . The optical bands are separated by the band pass filters on the MS-PD / APDs 530, 532, 534, and 546 by being reflected by each wavelength selection MS-PD / APD. After each reflection, the light is reflected through reflector 550 to the next wavelength selective MS-PD / APD and so on until all optical bands are absorbed by the designated MS-PD / APD. is called. Each central wavelength carries one data channel, for example, 820 nm carries channel 1 at a data rate of 25 Gb / s, and an MS-PD 530 with a bandpass filter at 820 nm converts the 820 nm signal into an optical signal. The recovered data channel 1 is generated for further signal processing by a CMOS ASIC (not shown) that is separated from the rest of the chip and integrated.

According to some embodiments, the MS-PD / APD epitaxial layer thickness is compatible with the epitaxial layer thickness and the structure of the CMOS (complementary metal oxide semiconductor) process, and therefore can be integrated with a CMOS ASIC. is possible. In contrast, a conventional silicon photodiode at 850 nm with a data rate of 1.25 Gb / s has an epitaxial layer greater than 10 μm thickness and 50% quantum efficiency. Thus, the relatively thick layers of conventional silicon photodiodes are not easily compatible with CMOS processes.

According to some embodiments, the light absorbing layer can be non-crystalline. In particular, it can be hydrogenated amorphous Si (a-Si: H) deposited by, for example, plasma enhanced chemical vapor deposition (PECVD) and / or hot wire chemical vapor deposition (HWCVD). The layer is typically on the order of 0.3-3 μm thick. High efficiency and high bandwidth for high speed data communication applications by sweeping light generated carriers by applying a reverse bias voltage across the light absorption region (ie, the I region of the pin photodiode structure) Make it possible. The layer on the non-crystalline layer can be a transparent or translucent conductive metal or a conductive oxide such as indium tin oxide. The top layer can be a thin layer of amorphous material doped to form a pin structure.

6A and 6B are schematic diagrams illustrating some basic components of a microstructured photodiode, according to some embodiments. FIG. 6 (A) shows the material structure 600 before etching the microstructure, and FIG. 6 (B) shows the MS-PD 660 after etching. It should be noted that, according to some embodiments, the microstructure is a hole 622, and in some other embodiments, the microstructure is a pillar. In some other embodiments, the microstructure is a combination of holes and pillars. The "Ia" layer 608 can be non-crystalline (eg, hydrogenated amorphous Si (a-Si: H)) grown on a crystalline or non-crystalline N layer. The P layer 610 can also be amorphous and highly doped P or a conductive oxide or metal. N layer 606 can also be a metal or a conductive oxide. Ohmic contacts 628 and 630 are used to apply a bias between the P and N layers to form a high electric field in the I layer 608 that sweeps away hydrogenated carriers. The substrate 602 can be, for example, a non-crystalline and / or dielectric such as quartz, a conductor such as glass, ceramic, and / or metal, silicide, or conductive polymer. According to some embodiments, "Ia", also known as "I" layer 608, can have a thickness range of 0.3 to 3 μm.

FIGS. 7A and 7B are schematic diagrams showing some basic components of a bottom-illuminated photodiode according to some embodiments. FIG. 7A shows the material structure 700 before etching the microstructure, and FIG. 7B shows the bottom-illuminated MS-PD 750 after etching the microstructure (holes 722, etc.). . In the case of bottom-illuminated PD / APD, the "Ia" or "I" region 708 can be non-crystalline such as a-Si: H, and the "N" layer 710 can also be non-crystalline. Meanwhile, the "P" layer 706 can be crystalline or non-crystalline on the BOX / SOI 704 and can be a crystalline or non-crystalline substrate 702. However, it is desirable that the substrate 702 and the P layer 706 be crystalline in order to minimize optical loss. This is because it is less absorptive than amorphous silicon at wavelengths in the range of 800-1100 nm. For a "double or multi-bounce" PD / APD, the absorption region "Ia" layer 708 can have a thickness range of 0.2 to 2 μm. This is because the optical signal

reflects off the N metal contact 726 and returns to the "is" absorbing layer 708. The thickness of the "is" layer 706 can be reduced, thus reducing travel time and increasing the photodiode or avalanche photodiode bandwidth.

FIGS. 8A and 8B are schematic diagrams illustrating some basic parts of an MS-APD structure, according to some embodiments. FIG. 8A shows the material structure 800 before etching the microstructure, and FIG. 8B shows the MS-APD 860 after etching. The "is" region 808 for light absorption can be crystalline or non-crystalline such as a-Si: H. Crystalline avalanche gain regions of PIN silicon (820, 818, and 806) are grown on a silicon substrate or BOX / SOI (buried oxide / silicon-on-insulator) substrate 802. The Pa upper layer 810 can be crystalline or non-crystalline. A transparent metal oxide layer 826 can be provided to form ohmic contacts with the PSi layer 810 and / or to reduce sheet resistance. It should be noted that the optical signal may come straight (vertical) to the top surface, or it may come at an angle as indicated by the photon arrow. The microstructure 822 can be a hole, a pillar, or a combination thereof. Although shown in FIG. 8B is a top-illuminated APD 860, according to some embodiments, BOX / SOI can be used to remove the bulk of the substrate, and the APD can be irradiated from the bottom in the wavelength range of 800-1100 nm. A reverse bias is applied between the P ohmic and bond metal 828 through the P layer 810 and the N ohmic and bond metal 830 through the N substrate 802. The reverse bias sweeps away hydrogenated carriers and provides electronic gain. A typical bias voltage for PD is 1 to 10 volts reverse bias, and in the case of APD, the range is approximately 5 to 50 volts reverse bias. As in all PIN and PIPIN devices described herein, P and N are interchangeable, for example, for photodiodes and avalanche photodiodes, PIN can be NIP and PIPIN is NINIP. is possible. The anode or P layer is negatively biased with respect to the cathode N layer.

FIGS. 9A and 9B are schematic diagrams illustrating certain aspects of a selective area growth (SAG) APD structure before and after SAG of III-V or Ge material, according to some embodiments. is there. FIG. 9A shows a SIAPD structure with etched holes 922 (or areas around the pillars). It is possible to perform selective area growth (SAG) epitaxial growth of III-V material or Ge, in which case the Pa layer 910 and Is layer 908 are a-Si: It can be non-crystalline, such as H, or it can be crystalline silicon. In particular, the microstructure I region 934 can be InGaAs or Ge, and the P region 932 can be InGaAs. According to some embodiments, it is possible to manufacture a SAG PD comprising InGaAs or Ge, starting with a PD structure with the avalanche gain layer (P layer 920 and I layer 918) removed. Other materials such as GaN, ZnSe, InP, and GaAs can also be used in SAG. According to some embodiments, other amorphous semiconductors such as amorphous Ge can be used. According to some embodiments, it is possible to use amorphous silicon due to a higher absorption coefficient than photon crystalline silicon, which has energy above indirect transitions.

FIG. 10 is a schematic diagram illustrating a simplified microstructured silicon photodiode with a PIN epitaxial layer according to some embodiments. Holes 1022 are etched into a buried oxide layer (BOX) 1004 that can be 0.2 to 10 μm thick. This structure 1060 provides high contrast in the refractive index between silicon and silicon dioxide, which can improve absorption. The I layer 1008 can have a thickness in the range of 0.5 to 5 μm, and the P layer 1010 and the N layer 1006 can have a thickness in the range of 0.1 to 5 μm. The absorption enhancement can be over 90% in the wavelength range of 800 to 900 nm or more. Its improved absorption is due to a certain wavelength of the optical signal generated by directly modulating a laser, such as a vertical cavity surface emitting laser, or by indirect modulation in which an optical modulator modulates the laser light. It is possible to optimize for the range. The modulated laser light at Gb / s is the optical signal. The optical signal is incident on the microstructured photodiode 1060 either at normal incidence or at an angle to normal incidence. A reverse bias is applied between the anode 1028 of P-ohmic contact and the cathode 1030 of N-ohmic contact for high-speed operation of the microstructure photodiode 1060. What is not shown is a 10 to 100 nm thick passivation layer on the silicon surface, for example, Si wet (vapor) or dry oxidation to reduce dangling bonds that occur during surface recombination, Grown by atomic layer deposition, vapor deposition of silicon dioxide.

FIG. 11 is a schematic diagram illustrating a simplified microstructured silicon photodiode having a PIN epitaxial layer according to some embodiments. MS-PD 1160 is identical to MS-PD 1060, except that the microstructured hole 1122 is not completely etched through the BOX layer 1004. According to some embodiments, an N layer 1006 of 0.01 to 2 μm can be left.

12 (A)-(C) illustrate a simulation situation using the Finite Difference Time Domain (FDTD) of the Maxwell Propagation Equation Method for a specific microstructured hole pattern, based on some examples. . FIG. 12A shows a hexagonal hole pattern in which the distance between the centers of the holes is 495 nm in the x direction and 860 nm in the y direction. As shown in FIG. 12B, the hole has been etched completely through to a depth of 2 μm, the hole diameter being 385 nm at the top and 430 nm at the bottom. FIG. 12C is a plot showing the results of a simulation using a finite difference time domain technique. Curves 1210, 1212 and 1214 indicate the absorptance, reflectance, and transmittance, respectively. In this particular example, it is understood that for a 2 μm thick silicon, it is possible to absorb more than 60% of light in the wavelength range of 805 to 830 nm. By varying the hole diameter, spacing, and etch depth, it is possible to optimize the absorption for a specific wavelength of the optical signal. According to some embodiments, the hole diameter can be varied from 200 to 1800 nm, the spacing can be varied from 200 to 3300 nm, and the depth can be varied from 0.1 to 2 μm. It is possible.

FIG. 13 is a schematic diagram illustrating an epitaxial layer structure for a high-contrast microstructure photodiode (PD) with P-I-N doping according to some embodiments. Starting with a BOX (buried oxide) 1304 in Si 1302, the thickness of the oxide layer is still in the range of 0.1 to 10 microns or more, and a thin Ge buffer layer 1370 is grown on the NSi 1302. It is possible. With or without the Ge buffer layer 1370, the subsequent N, I, P layers 1306, 1308, 1310 can be made of Ge and / or III-V such as InGaAs, InP, InGaAsP, GaAs, AlGaAs, GaN, InGaN, AlGaN, etc. It can be a substance group. When the N, I, P layers 1306, 1308, and 1310 are Si, the Ge buffer layer 1370 can be omitted. For high speed operation of the PD, the N layer 1306 can range from 0.1 to 5 microns and the I layer 1308 can range from 0.2 to 3 microns thick. And the P layer 1310 can range from 0.1 to 2 microns. The last layer, in this example the P layer 1310, can be a combination of multiple layers, such as an InP and P layer with a thin InGaAs capping.

FIG. 14 is a schematic diagram illustrating an epitaxial layer structure for a high contrast microstructured photodiode (PD) with P-I-N doping according to some embodiments. The PIN heterostructure can be such that the Ge buffer layer 1470 is at or near the interface between the I layer 1408 and the N layer 1406, in which case the I layer 1408 and the P layer 1410 are Ge and / or Or It is the same as that of FIG. 13 except that it can be made into a III-V substance group. The advantage of this example structure is that for photon energies below the Si bandgap, a smaller number of electron-hole pairs are generated in the N layer 1406, where photogenerated carriers are generated by the high electric field in the I layer 1408. It is possible to diffuse into the region, resulting in a slow component in the fast response of the PD. The Ge buffer layer may not be necessary for heterogrowth.

FIG. 15 is a schematic diagram illustrating an epitaxial layer structure for a high contrast microstructured photodiode (PD) with P-I-N doping, according to some embodiments. The PIN heterostructure is similar to that of FIGS. 13 and 14 except that only the I region 1508 is Ge and / or lower bandgap materials such as III-V materials such as InGaAs, InSb, InGaAsP, and InAs, it is the same. Both P layer 1510 and N layer 1506 are composed of a higher band gap material. According to some embodiments, the P layer 1510 and the N layer 1506 have a higher band gap energy than the photon energy, and the I layer 1508 has a band gap energy equal to or lower than the photon energy. Have. For example, the N layer 1506 can be Si, the I layer 1508 can be InGaAs and / or Ge, and the P layer 1510 can be Si and / or InP. The Ge buffer layer may or may not be necessary for heterogrowth. The advantage of having higher band gap materials in the P and N regions is to minimize the photocarriers generated in these regions. The optical carriers generated in the P and N regions can diffuse into the high electric field region, resulting in a relatively slow component in the photodiode response to short optical pulses. Thus, reducing the optical carriers generated in the P and N regions is a "tail effect", ie an optical input pulse or a set of pulses as in a bitstream for optically transmitting data. In response to this, the fall time of the electrical pulse output of the PD is decreased. High doping of the P and N regions also reduces the minority carrier lifetime so that photocarriers generated in these regions can recombine before diffusing into the high electric field "I" region.

FIG. 16 is a schematic diagram illustrating some aspects of the fabrication of a high contrast microstructured photodiode (PD) based on some embodiments. The exemplary structure illustrated in FIG. 13 is shown with holes 1622 etched through the PIN layers 1310, 1308, 1306 all the way to the oxide layer 1304 embedded in the

silicon layer 1302. Dry and / or wet etches can be used and a passivation layer can be added to the exposed surface by atomic layer deposition. In this example, a Ge buffer layer 1370 is provided at the interface between the N layer 1306 and the Si layer 1302. According to some embodiments, similar manufacturing methods are used for the structures shown in FIGS.

FIGS. 17A-D are schematic diagrams illustrating examples of hole placement, spacing, dimensions, and passivation layers based on some embodiments. FIG. 17A shows a hexagonal layout with a passivation layer thickness of 50 nm with an interval of 280 nm. FIG. 17B shows a square layout. FIGS. 17C and 17D show tapered and vertical hole shapes, respectively. Although these illustrated examples are for silicon, the technique can also be applied to Ge and III-V material groups with minor modifications to the dimensions. The holes can have a circular cross section, or, according to some embodiments, can be other shapes, such as an ellipse, a rectangle, and the like.

FIG. 18 is a schematic diagram illustrating further aspects of the fabrication of a high contrast microstructured photodiode (PD) based on some embodiments. The exemplary structure illustrated in FIGS. 13 and 16 is shown after etching the microstructured hole 1622 and depositing and annealing a P-ohmic contact layer 1828.

FIG. 19 is a schematic diagram illustrating some additional aspects of the fabrication of a high contrast microstructured photodiode (PD) based on some embodiments. Illustrative structures illustrated in FIGS. 13, 16, and 18 are shown. After the P-ohmic contact 1828 is deposited and annealed, the mesa can be etched to remove the material 1972 to define the PD capacitance. The mesa diameter can range from 5 microns to over 100 microns, depending on the RC time desired for the PD. Passivation of exposed P, I, and N regions is performed to minimize leakage current due to, for example, dangling bonds. According to some embodiments, using ion implantation such as proton bombardment instead of mesa etching to define the capacity of the PIN structure by generating electrically semi-insulating or insulating regions, is also possible.

FIG. 20 is a schematic diagram illustrating some additional aspects of the fabrication of a high contrast microstructured photodiode (PD) based on some embodiments. Illustrative structures illustrated in FIGS. 13, 16, 18, and 19 are shown. After the mesa etching, a ring or partial ring-shaped N ohmic contact 2030 is formed on the N layer 1306. An insulating layer is formed from a material such as polyimide so that a bridging path is formed to connect the metallization from the P ohmic contact 1828 to a bond pad (not shown) to apply an electrical bias to the P region 1310. Additional processing steps for completing the PD are not shown. For simplification, the metal for connection between the N ohmic contact 2030 and the N bond pad is not shown. A reverse electrical bias is applied to the P and N ohmic contacts 1828 and 2030 to form a high electric field in the I layer 1308. According to some embodiments, a negative 1 to negative 10 volt voltage can be applied.

FIG. 21 is a schematic diagram illustrating several aspects of a lossy high contrast microstructured photodiode (PD) based on some embodiments. FIG. 21 shows a microstructure type PPD in which light travels twice in the absorption layer 1308. This is accomplished by removing a portion 2174 of the Si substrate 1302 down to the oxide layer 1304 and coating the oxide with a metal reflector 2176 such as Au, Ag, Al or Cu. According to some embodiments, it can be in the form of a Bragg reflector for either broadband or wavelength selectivity. According to some embodiments, a Bragg layer may also be included on the top surface of the P layer 1310 to provide additional wavelength selectivity, particularly for use in coarse wavelength division multiplexing, or wavelength division multiplexing, is possible.

FIGS. 22A and 22B show a simulation situation using the FDTD method for a particular microstructure PD based on some embodiments. FIG. 22B is a plot showing simulation results of photon absorption with respect to photon wavelength for the double bounce structure as shown in FIG. Exemplary thicknesses used in the simulation are as follows: oxide 1304 is 2 microns, P silicon 1310 is 300 nm, I/Si 1308 is 2 microns, and N silicon 1302 is 300 nm, and reflector 2176 is 100 nm thick Au. As shown in FIG. 22A, a hexagonal microstructure hole is adopted. As shown in FIG. 22A, the hole has a center-to-center hexagonal period of 600 nm, a hole diameter of 480 nm, and a SiO_2 passivation of 30 nm. These dimensions are just one example for a microstructured hole with a corresponding simulation of absorption characteristics versus wavelength. As can be understood from the curves 2210 (absorption) and 2212 (reflection) in FIG. 22B, the absorption was found to be significantly higher than in the case of Si without a microstructured hole did. For example, in the vicinity of the 850 nm wavelength, the absorption is better than 70%.

FIG. 23 is a schematic diagram illustrating certain aspects of a high-contrast microstructure PD according to some embodiments. Substructure is similar to the structure of FIG. 20, i.e., Si substrate 2302, SiO_2 layer 2304, and a SiN layer 2306. It is also possible to provide a lower SI layer 2308. In this case, Ge is used as the upper I layer 2309 and the P layer 2310. The P layer 2310 can also be composed of InP that can be grown on the GeI layer 2309. The advantage of InPP layer 2310 is that it is less absorptive at wavelengths of 0.9-2 μm. P layer 2310 can also be composed of GaAs grown on GeI layer 2309. Further, a microstructure hole 2322, a P ohmic contact 2328, and an N ohmic contact 2330 are also shown. It should be noted that light can be incident on the top surface of P layer 2310 and / or on Si substrate surface 2302.

FIG. 24 is a schematic diagram illustrating the situation of a heteroepitaxial microstructure PD based on some embodiments. In this case, the I region can be a composite of SI (lower layer 2408) and InGaAs (upper I layer 2409) separated by a Ge layer 2470. The P region 2410 is InP. According to some embodiments, the I region can be InGaAs grown entirely on a thin layer of buffered Ge layer 2470. In addition, Si substrate 2402, oxide layer 2404, N layer 2406, microstructure hole 2422, P ohmic, contact 2428, and N ohmic contact 2430 are also shown. This is an example of a high contrast microstructure PD structure. It can further incorporate a metal reflector as in FIG. 21, in which case SI is removed by etching into the oxide layer underneath the PD and Au, Ag, Al or Cu metal. It is possible to deposit a layer and reflect the light towards the I-absorbing layer. It is also possible to use a Bragg reflector as described above. In this example, light comes from the P layer side. The light can also come from the Si substrate side, in which case a reflector is placed on the P layer to run the I layer twice. The advantages of such a configuration include that the absorption is significantly improved by running the absorption region twice or more while keeping the I layer unchanged from that of the single run. Yes. By reducing the absorption area thickness to, for example, half that of a single running PD, the speed of the PD is increased. This is because the travel time for a light-generated carrier need only travel half the distance of a single travel PD. The high contrast microstructure means that the refractive index difference between the bulk semiconductor material in the space or air and SiO_2 and / or another surface interface in the microstructure and a surface interface. Light interacts with the microstructure in a complex manner of coupled eigenmodes or resonator cells, where each hexagonal or square cell in the grating is a linear and nonlinear optical that may be generated. In addition to field enhancement, it can be thought of as an individual resonator coupled with its adjacent cell or resonator. If there is little or no optical loss, the coupled resonator structure can have a high Q (resonator quality factor), i.e. before the light disappears, for example. It is possible to bounce repeatedly within the microstructure over 10^4 to 10^6 times. However, if there is some optical loss, such as due to weak absorption, Q may be low and light may bounce repeatedly within the microstructure less than 100 times, or less than 20-30 times. The microstructure in PD / APD is a low-Q high-contrast structure or a lossy high-contrast structure, and the Q of each cell is coupled to an adjacent cell.

FIG. 25 shows a high contrast structure for an optical emitter, such as a light emitting diode (LED) or vertical surface emitting laser (VCSEL), according to some embodiments. The optical light emitter 2500 has a heteroepitaxial layer structure. A Si layer 2506 is formed on the Si substrate 2502 and the BOX / SiO_2 layer 2504. A buffer Ge layer 2570 can be formed on the Si layer 2506, followed by a layer 2510, which can be InAs quantum dots 2572 and can be coated with GaAs and AlGaAs. It is. Further, the "I" layer can be as thin as about 1000 nm or less and a simple SIPIN microstructure that is forward biased can be a photon emitter.

FIG. 26 shows a basic structure for a high contrast 1.3 micron wavelength photoemitter (PE), for example, according to some embodiments. The active layer for the 1.3 micron wavelength emitter is the InAs quantum dot layer 2570 (shown in FIG. 25) or 2670 in FIG. 26 sandwiched between the GaAsP layer 2604 and the N layer 2606, and these are AlGaAsP layer 2608 and N layer. And a PGaAs capping layer 2610 as a final layer. Typical thicknesses can be found in the literature. For example, see Quantum Dot Lasers for Silicon Photonics such as AY Liu, S Srinivasan, J Norman, AC Gossard, JE Bowers, Photonics Research 3 (5), B1-B9 (2015). This document is incorporated herein by reference. Furthermore, there may be multiple layers of quantum dots and / or coating layers. The microstructure can be configured such that standing wave

peaks are located in one or more of the QD layers to optimize gain and optical field overlap. In the case of MS-PD / APD, the length of the microstructure is such that an integer number of wavelengths reciprocate at a particular wavelength, for example, to optimize the absorption enhancement at that particular wavelength. It is possible. Furthermore, a single microstructure, eg, a single hole, has improved absorption or emissions for either PE or MS-PD / APD compared to a similar structure without a microstructure. It is possible.

FIG. 27 is a schematic diagram illustrating some basic features of a high contrast microstructured photoemitter (PE) structure with etched holes, according to some embodiments. Its material structure is the same as that of PE 2500 shown in FIG. Microstructure hole 2722 is etched into active layer 2510. P and N ohmic contacts 2728 and 2730 are used to forward bias the device 2700, ie, to make P positive with respect to N to generate photons from the active layer 2510, which is the present example. Have InAs quantum dots 2572 at a wavelength of 1.3 microns. Other active layers and coating layers can be used to generate light at other wavelengths from visible to infrared light. Depending on the wavelength of light, light can be emitted from the top surface and / or from the bottom surface via the oxide layer 2504. An advantage of a microstructured high contrast photon emitter is that photons interact longer with the gain layer in the case of the active layer and / or laser. Because, the high contrast structure can have a very high Q, the Q spans 10^3 to more than one million range, because the structure is almost having an optical loss. This is because the quantum dots provide optical gain. The high contrast, low loss microstructured photoemitter can operate as an LED, as a VCSEL, and / or as a laser and / or a high power LED. The PE is forward biased and the P-ohmic or P layer is at a positive voltage relative to the N-ohmic or N-layer cathode 2730.

FIG. 28 is a schematic diagram illustrating several aspects of a PE based on some embodiments. PE 2800 is similar to PE 2700 shown in FIG. 27 except that a portion 2874 of substrate 2502 has been removed to oxide layer 2504 below the light exit region. A Bragg reflector, such as a metal and / or distributed Bragg reflector (DBR) 2504, is formed on the oxide layer to reflect the light generated in the active layer back to the surface of the P layer 2510. According to some embodiments, device 2800 operates in LED mode and / or laser mode.

FIG. 29 is a schematic diagram illustrating several aspects of a PE based on some embodiments. PE 2900 is similar to PE 2800 of FIG. 28 except that it includes a reflector 2928 that can be metal and optionally can also operate as a P-ohmic contact. According to some embodiments, a separate P-ohmic can be provided. The reflector 2928 may be a distributed Bragg reflector and / or partly metal and partly DBR. Light is emitted from the lower surface of the oxide layer 2504 and through the substrate 2502 from which a portion 2874 has been removed. The photoemitter or light emitter 2900 can operate in a laser mode, such as an LED and / or VCSEL mode. According to some embodiments, the photoemitter 2900 can operate in edge mode, in which case light is emitted in plane rather than perpendicular to the plane of the active layer, along the emission edge. There may or may not be a mirror such as DBR or metal.

FIG. 30 is a schematic diagram illustrating several aspects of a PE based on some embodiments. The PE 3000 is similar to the PE 2800 of FIG. 28, but is configured as a VCSEL (Vertical Cavity Surface Emitting Laser). PE3000 has a high contrast microstructured hole (or column) and is heteroepitaxially grown on Si. It should be noted that only very basic parts are shown for the sake of brevity. The high contrast structure can be sandwiched by reflectors 2928 and 3076. The P layer 2510 can be a DBR grown by semiconductor epitaxy, followed by a P ohmic metallization layer 2928. According to some embodiments, the DBR can be formed from a conductive oxide or a non-conductive oxide, with a P metal on the DBR and / or on its side as in FIG. It is possible to provide. The mirror 3076 on the bottom side of the oxide layer 2504 can be a metal and / or DBR of a dielectric layer of different refractive index. The light output as shown is from the bottom, but can also be from the top.

FIG. 31 is a schematic diagram illustrating some aspects of a simple PIN photodiode structure, according to some embodiments. The "I" layer 3108, P and N layers 3110 and 3106 are highly doped and / or degenerately doped to minimize the diffusion current due to the photocarriers generated in the region outside the high electric field region. Reduce the life of minority carriers. N and P doping can be in the range of 1×10^{18} to 5×10^{21} / cm^3 or more. The I layer 3108 is not intentionally doped and can be less than 5×10^{16} / cm^3. Further, an oxide layer 3104 and a Si substrate 3102 are shown. As in the previous example, Ge and / or III-V materials can be grown with and without the addition of a Ge buffer layer and the P and N layers are also highly doped and / or Degenerative doping is also possible. The doping need not be uniform and can have a gradation, for example, an "I" layer interface to minimize dopant diffusion into the "I" layer during epitaxial growth. Reduce doping in nearby P or N layers.

By reducing the lifetime of minority carriers in the P and N layers, the photogenerated carriers in these layers can diffuse and / or recombine before moving into the high electric field "I". In the high electric field "I", electrons and / or holes may contribute to the photocurrent, resulting in deterioration of the photodiode modulation type frequency response. Therefore, it is desirable to minimize the contribution of photocurrent due to carriers generated outside the high electric field region.

Other methods of reducing minority carrier lifetime include introducing defects such as partial and / or complete via ion implantation in the P and / or N regions. The ions introduced can be inert ions and / or active ions, with or without partial or complete thermal annealing. Furthermore, the microstructured holes (and / or pillars) may or may not be partially passivated, so the low field regions of the N and P layers act as carrier sinks. While in the high field region of the "I" layer, the carriers are quickly swept away. Passivation can be noticeably selective on the "I" layer.

FIG. 32 is a schematic diagram illustrating some aspects of MS-PD manufacturing according to some embodiments. The starting material structure can be as illustrated in structure 3100 of FIG. A simple NIP (N and P are interchangeable for PIN) microstructured photodiode is shown, with holes 3222 etched into the top of the P layer 3106. Its purpose is to passivate the walls of the N and "I" layers and not passivate the walls of the P layer, thereby reducing the lifetime of minority carriers in the P layer generated by light having a wavelength of, for example, 780 to 980 nm. Decrease. The surface state on the non-passivated P wall can act as a potential sink for minority carriers, where the carriers are recombined.

FIG. 33 is a schematic diagram illustrating certain aspects of MS-PD manufacturing according to some embodiments. The passivation of the sidewalls of the N and "I" layer holes 3222 is shown, resulting in the formation of a passivation layer 3324. The passivation may be carried out using thermal oxidation and / or SiO_2 atomic layer deposition. A 5-50 nm thick thermal oxide 3324 can be grown on the sidewall, for example. Other thicknesses can be grown. After thermal oxidation, the hole can be continuously etched, for example, through the P layer 3106 and etched into the SiO_2 layer 3104. Not all process steps are shown, for example, it is possible to protect the N layer with a thermal oxide (not shown) during the duration of the hole etching.

FIG. 34 is a schematic diagram showing aspects of MS-PD manufacturing based on some embodiments. After passivation, hole 3222 is further etched as indicated by area 3422. It should be noted that the N and P layers can be interchanged, and thus a PIN structure can be used instead of the NIP structure as shown in this example. The holes 3222 can be etched into the SiO_2 layer 3104 and / or they can only be partially etched through the P layer 3106 so that a thin P layer remains. The side of the hole 3222 in the P-layer 3106 is not passivated in this example, and its surface state will draw any minority carriers generated by light into the potential sink and recombine. It is possible. According to some embodiments, the P layer 3106 can also be passivated and / or partially passivated. Since layer 3106 can also be highly doped, the minority carrier lifetime can be tens of picoseconds or less.

FIG. 35 is a schematic diagram illustrating certain aspects of an MS-PD according to some embodiments. Microstructured NIP photodiode 3560 has N and "I" layer passivated sidewalls, but the P layer sidewalls have unpassivated microstructure holes 3222. Ohmic contacts 3528 and 3530 to the N and P layers, respectively, are added to provide a reverse bias for high speed operation of the photodiode 3560. The light incident on the N side of the photodiode is either perpendicular and / or deviated from perpendicular to the N layer surface.

FIG. 36 is a schematic diagram illustrating certain aspects of MS-PD, according to some embodiments. The microstructured hole photodiode 3660 has a SINIP layer, in which case the passivation is partial on the sidewall, similar to the PD 3560 shown in FIG. However, in the case of PD 3660, light comes from the Si substrate side.

through the optical fiber 3680 where the via 3672 is etched to allow a self-aligned process, in which case the fiber 3680 has a lens with or without 3682, guided through via 3672 to the correct position for optical coupling into microstructured photodiode 3660. A dielectric layer 3676 approximately 0.1-10 μm thick can be positioned on the N layer 3110 above the hole 3222. On the dielectric layer 3676 towards a metal reflector 3678 such as Ag or Au (or any other suitable metal or alloy, eg, Al, Ni, Cr, etc.) and / or an absorbing "I" layer 3108 in order to reflect the light, a dielectric laminate such as a Bragg reflector (BR) can be provided. It is also possible to provide an anti-reflective coating 3673. It is also possible to grow Ge and / or III-V material with or without the addition of a Ga buffer layer, as in the previous example.

FIG. 37 is a schematic diagram illustrating a technique for reducing minority carrier lifetime according to some embodiments. In this case, instead of passivating or partially passivating the hole surface, surface and bulk recombination is used. High doping greater than 10^{20} / cm^3 can reduce the diffusion length to, for example, less than 0.1 μm (Auger recombination). In addition, ion implantation is used to introduce defects 3770 and 3772 into layers 3710 and 3706. Defects in the semiconductor can also reduce lifetime through a Shockley-Read-Hall recombination process. For example, ions such as Xe, Bi, Ti, Cr, Au, and Ni can be implanted into the N and / or P layers. In contrast to known structures where long minority carrier lifetimes are desired for device operation, the techniques described herein provide epitaxial growth and / or to increase the recombination rate due to the Shockley-Lead-Hall effect. Alternatively, defects are introduced by either ion implantation of metal, non-metal and inert ions. Due to the defects, deep and / or shallow traps can be formed, which can shorten the lifetime of minority carriers. A short minority carrier lifetime is desirable in the P and N regions to minimize the contribution of diffusion currents that can contribute to the photocurrent through the high field region "I" layer. These "slow" diffusion currents that diffuse and / or travel into the "I" region cause degradation of the time response of the photodiode by contributing to a slow component to the photocurrent time response characteristics of the photodiode. There is a case to let you.

38A to 38C show various parameters for the simulated microstructure photodiode. FIG. 38A shows a hexagonal hole pattern having a distance "d" between the hole centers. FIG. 38B shows a square hole pattern having a distance "d" between the hole centers. FIG. 38C is a table of parameters used for the simulation using the FDTD method. SiO having a thickness of 2-2.5 μm with a plurality of holes having a period of 2000 nm and a diameter of 1300 to 1500 nm in the holes of the hexagonal lattice for optical signal wavelengths in the range of 830 to 930 nm and, for example, 950 nm It has been found that it is possible to achieve greater than 90% absorption with a 2 μm thick silicon layer on $_{1300}$ layers. Furthermore, the wavelength can range from 750-1000 nm. The hole diameter can be larger than the sub-wavelength of the wavelength of the incident optical signal and spans a diameter range of 100 to 3000 nm. The thickness of the Si absorption layer can be in the range of 0.3 to 10 μm. The SiO_2 layer can range from 0.2 to 10 μm. According to some embodiments, a mixture of multiple hole diameters can be used to optimize the absorption of incident photons.

FIG. 39 is a graph plotting simulation results for a microstructured hole photodiode using FDTD versus absorption versus wavelength. The photodiode absorbing "I" layer was 2 μm thick and the hole diameters ranged from 1000 to 1500 nm. The incident energy wavelength was in the range of 830 to 950 nm. Three curves 3910, 3912, 3914 are plots of absorption for 1000 nm, 1350 nm and 1500 nm hole diameters, respectively. This simulation shows that for a 1500 nm hole diameter, greater than 90% absorption is achieved over the wavelength range of 850-870 nm, and for a 1300 nm hole diameter, a hole in a hexagonal lattice with a period of 2000 nm. It shows that it is possible to achieve an absorption greater than 80% over the wavelength range of 875 to 930 nm. $_2$ μm Si is on the 2-2.5 μm SiO_2 layer. As will be appreciated, having a hole diameter larger than the incident wavelength can be used to improve absorption over that of conventional silicon layers without any features.

FIG. 40 is a schematic diagram illustrating a microstructured avalanche photodiodes (APD) having a P-I-P-I-N epitaxial structure according to some embodiments. In the case of FIG. 40, all layers of APD 4060 are silicon, for example, for optical communication wavelengths in the range of 780 to 1000 nm. The APD 4060 can also operate in the visible light wavelength range. Data rates can range from 100 Mb / s to 30 Gb / s or more. A reverse bias voltage is applied between the P and N ohmic contacts 4026 and 4030 in the voltage range of ~4 to ~50 volts. The avalanche microstructure photodiode 4060 can have the following doping and thickness, for example, the doping of the P layer 4010 is greater than 1×10^{19} / cm^3 and the thickness is 0.01-1.0 μm, the doping of the I layer 4008 is less than 1×10^{16} / cm^3 and the thickness is 0.5-3 μm, and the doping of the P layer 4020 is $1-8 \times 10^{17}$ / cm^3 and the thickness is 0.1-0.5 μm, the doping of the I layer 4018 is less than 1×10^{16} / cm^3 and the thickness is 0.3-1 μm, and The doping of the N layer 4006 is 1×10^{19} / cm^3 and the thickness is 0.5-3 μm. According to some embodiments, the top two layers 4012 and 4008 can be Ge instead of Si. Hole 4032 can be etched partially through the APD layer or completely etched into the SiO_2 layer 4004 as shown in FIG.

As in the case of microstructure photodiodes, in the case of APD, the optical signal can be incident from the front side (epitaxial layer side) or from the back side (substrate side). Furthermore, if there are vias in the substrate, a reflector can be deposited on the SiO_2, resulting in the optical signal bouncing or bounced twice or many times within the APD structure. According to some embodiments, P and N can be interchanged, resulting in a N-I-N-I-P microstructure APD.

FIG. 41 is a schematic diagram illustrating a microstructured avalanche photodiode (APD) having a P-I-P-IN epitaxial structure, according to some other embodiments. The APD 4160 is the same as the APD 4060 shown in FIG. 40 except that the plurality of holes 4122 (or pillars) are partially etched. In the example shown in FIG. 41, the holes 4122 are partially etched in the P layer 4020 and / or stopped at the P layer 4020. According to some other embodiments, the holes 4122 can be partially etched into the I-absorption layer 4008.

FIG. 42 is a schematic diagram illustrating a microstructured APD comprising a Ge absorption layer and a GeP capping layer according to some embodiments. APD 4260 is similar or identical to APD 4060 illustrated in FIG. 40 except that the top two layers are Ge instead of Si. The APD 4260 can have the same doping and thickness range as described above for the APD 4060, except that the PGe layer 4010 can have a doping level greater than 1×10^{20} / cm^3 is there. After the epitaxial growth of the APD structure P (Ge) -I (Ge) -P (Si) -I (Si) -N (Si) on a buried oxide (BOX) silicon substrate, the microstructure is etched. The microstructure can be a hole, a pillar, or a combination of the two. The etching is capable of performing up to the SiO_2 layer, or be partially etched to the previous depth reaching the SiO_2 layer 4004 are also possible, for example, holes or into its up PSi layer 4020 It is possible to etch. The Ge absorption layer 4208 comprising the microstructure is expected to allow optical signals to operate at wavelengths between 780 and 2000 nm at data rates of 100 Mb / s to 56 Gb / s or higher. The optical signal can be incident from the top surface (epitaxial surface) or from the bottom surface (substrate surface). If there are reflectors deposited on the vias and SiO_2, the optical signal incident from the top surface can be reflected to the absorbing I (Ge) layer 4208 a second time and / or multiple times. Since there is an optical refractive index difference between Si, air, and Ge, it is possible to establish a standing wave and the absorption layer at the peak intensity of the standing wave, also known as a standing wave or eigenmode. It is possible to optimize the thickness of the structure to have. In addition, at wavelengths where Si is transparent, microlenses can be etched into the Si substrate to help couple optical signals from the bottom surface into the APD. SiO_2 and a reflector can be placed on the P (Ge) 4210 to reflect the optical signal incident from the bottom to the absorbing I (Ge) layer 4208. A reverse bias voltage in the range of ~4 to ~50 volts is applied between the P and N ohmic contacts 4026 and 4030.

FIGS. 43A to 43D show the polarization sensitivity of the microstructure photodiode and the APD based on some embodiments. FIG. 43A shows the geometric shape used for the simulation. These holes are symmetric in size and period, and the electric field polarization of the optical signal along either B or A shows a difference of less than 5% in the absorption characteristics of MS-PD / APD. Absorption is equal to incident light minus its transmission and reflection, and quantum efficiency is directly proportional to absorption. If the hole dimensions "a" and "b" are not the same, MS-PD / APD shows polarization sensitivity. In FIG. 43B, curve 4310 plots absorption versus wavelength, in which case the "a" and "b" dimensions are both equal to 1500 nm. The absorption characteristics show a difference of less than 5%. FIG. 43C shows the case where a = 1300 nm and b = 870 nm. Curves 4320 and 4322 show that it is possible to understand that the difference in absorption values in the case of some polarization along A or B is at most twice. FIG. 43D shows the result for the case where a = 1500 nm and b = 650 nm. Curves 4330 and 4332 show that the absorption difference due to polarization orientation is also at most twice. If there are further dimensional changes in both "a", "b", A and B, the absorption difference due

to polarization orientation may differ by 10 to 100 times or more. Both polarization "insensitive" (when the absorption change due to polarization orientation is less than 5%) and polarization sensitivity (when the absorption change due to polarization orientation is 10 times or more) are useful. In mere, if the signal is not polarization multiplexed, eg. using the same wavelength, it is possible to transmit two channels, where one channel is one polarization and another channel is the first it is orthogonal to the channel. For example, each channel can transmit at 25 Gb / s at a specific polarization at the same wavelength. At the receiver end, a polarization sensitive photodetector is used to demultiplex the signal. The total data rate is 50 Gb / s at a wavelength of 850 nm. In the direct modulation of a laser, the spectrum of the laser is always wider than for example a laser operating in CW mode. The spectrum can be broadened by at most several nanometers (eg, 3 nm). Therefore, when the laser is directly modulated at 850 nm, the center frequency can be set to 850 nm by widening at most it about 1.5 wnm. In a vertical cavity surface emitting laser, the transverse mode can contribute significantly to a wider spectrum due to multiple transverse modes. In multi mode systems this is desirable because it reduces mode selection loss.

FIG. 44 illustrates an MS-PD / APD integrated with mutual impedance and / or another ASIC (Application Specific Integrated Circuit) for data processing and / or routing, according to some embodiments. Yes. The process can be CMOS and / or BiCMOS. The MS-PD / APD 4420 is shown electrically connected to electronics 4430 (eg, a mutual impedance amplifier (TIA) and / or another ASIC) via electrical leads 4423. All of the components are integrated on a single silicon substrate 4410. One advantage of integrating microstructured PD / APD with IC electronics is reduced packaging costs, in which case a single chip is used instead of two or more individual devices. It can also be placed directly on the circuit board without using a multi-chip ceramic carrier. Another advantage of integrating MS-PD / APD with electronics on a single chip is potentially lower capacitance due to the omission of relatively large bond pads connected to ohmic contacts. It is to become. The operating wavelength is in the range of 800-990 nm for all silicon microstructure PD / APD. The operating wavelength can be extended to 1800 nm when a Ge microstructured absorption layer is added. Operation at data rates of 10, 25, 56 Gb / s can be achieved alone or in an array. The data rate can also be 1, 5, 20, 25, 50, 40 Gb / s depending on the protocol and link application. Typically, high data rates over multimode fibers and / or multiple fibers are used at distances ranging from less than 1 meter to more than 100 meters. Multiple fiber and microstructured PD / APD (MS-PD / APD) arrays can be used to provide an overall data rate of 100 to 400 Gb / s. For example, each fiber operates at 10 Gb / s with a 10 MS-PD / APD array integrated with IC electronics such as a mutual impedance amplifier (TIA) and / or other signal processing / routing IC electronics on a single silicon chip 10 fiber channels can have a total data rate of 100 Gb / s. If each channel is 56 Gb / s, the 10 channels can have an overall data rate in excess of 500 Gb / s.

FIG. 45 shows some aspects of a flip chip arrangement for MS-PD / APD integrated with TIA and / or another signal processing IC on a single silicon chip, according to some embodiments. FIG. According to some embodiments, TIA and / or other signal processing integrated circuits 4530 are fabricated using CMOS and / or BiCMOS processes. A chip 4510 is attached to a PCB (Printed Circuit Board) 4550 using solder bumps 4512 and 4514 and / or similar bump technology. According to some embodiments, some or all of the solder bumps 4512 are used to make electrical connections between the chip 4510 and the PCB 4550, while the solder bumps 4514 provide physical mounting and / or stabilization. Used for. This is because a direct electrical connection between the MS-PD / APD 4520 and the PCB 4550 may not be necessary. According to some embodiments, chip 4510 is attached to another chip or multi-chip carrier instead of PCB 4550. Packaging the chip 4510 directly on the PCB 4550 is at most 80% compared to the known prior art where PD and IC electronics are first mounted on a multi-chip ceramic carrier before being placed on the PCB. Only reduce the packaging cost. Further, an integrated optical lens 4522 can be fabricated on the silicon chip 4510 to focus light from the optical fiber 4524 to the MS-PD / APD 4520. It should be noted that in this configuration, the optical signal enters from the substrate side of the MS-PD / APD 4520. An integrated lens 4522 on Si is used when a Ge microstructure can be used for absorption of incoming optical signals and the operating wavelength is greater than 1100 nm (eg, 1100 nm to 1800 nm). It is possible.

FIG. 46 shows some aspects of a flip chip arrangement for MS-PD / APD integrated with TIA and / or another signal processing IC on a single silicon chip, based on some embodiments. FIG. The chip and mounting technique is similar or identical to that shown and described in FIG. In this case, chip 4510 includes via 4626 where most or all of the silicon in the optical path to MS-PD / APD 4520 has been removed. An integrated dielectric lens 4622 is provided to collect light and direct it to the MS-PD / APD 4520. According to some embodiments, a light pipe is used instead of lens 4622. The sidewalls of via 4626 can be coated with a dielectric and / or metal to aid in light collection. An anti-reflective coating may be provided on the lens 4622 to reduce the reflection of the optical signal back to the optical fiber 4524. In addition, the fiber 4524 or tip 4510 can be tilted to reduce reflection back to the fiber 4524. Optical fiber 4524 is used to provide optical signals from the laser source to integrated PD / APD and IC electronics circuit 4510 at data rates ranging from less than 1 Gb / s to more than 50 Gb / s. According to some embodiments, data rates of about 1, 5, 10, 20, 28, 50, 56 Gb / s can be used. According to some embodiments, the optical signal wavelength may range from 800-990 nm for all-silicon microstructure PD / APD (MS-PD / APD) and microstructure Ge for the absorber layer. In this case, the wavelength can be extended to 1800 nm.

FIG. 47 shows some of the flip-chip arrangements for MS-PD / APD integrated with TIA and / or another signal processing IC on a single silicon chip, according to some other embodiments. It is the schematic which shows the side surface. The chip and mounting techniques are similar or identical to those shown and described in FIGS. 45 and 46. As in FIGS. 45 and 46, a single chip 4610 includes both optical and electronic elements. Vias 4626 are provided in the substrate of the chip 4610 to remove most or all of the Si in the optical path to the MS-PD / APD 4620 along with the integrated Fresnel lens 4722 so that optical signals are efficiently transmitted from the optical fiber 4524. To be collected. The collected optical signal is incident on the MS-PD / APD 4520. According to some embodiments, high contrast grating (HCG) is used instead of Fresnel lens 4722. According to some embodiments, HCG can have a filter effect, so that only certain optical wavelengths can be transmitted to MS-PD / APD while others can be reflected. This bandpass characteristic is useful for coarse wavelength division multiplexing (CWDM), where multiple wavelengths are used in a single fiber.

FIG. 48 illustrates some aspects of a flip chip arrangement for an MS-PD / APD integrated with a TIA and / or another signal processing IC on a single silicon chip, according to some other embodiments. It is the schematic which shows these. The chip and mounting techniques are similar or identical to those shown and described in FIGS. 45-47. The walls of via 4626 can be coated with a dielectric and / or metal to provide a light pipe for light to enter MS-PD / APD 4520. The optical fiber 4524 can then be inserted into the via 4626, in which case the via provides a guide for aligning the fiber 4524 with the MS-PD / APD 4520, thereby MS-PD / Simplifies optical packing and alignment of the optical fiber to the APD, resulting in a cost reduction of about 30% or more. According to some embodiments, the fiber 4524 can be tapered and / or can have multiple diameters so that the via 4626 provides a step for the fiber 4524. For example, the via 4626 can be stepped to allow the end of the fiber 4524 to abut on that step and attach it to the silicon. This step configuration also provides a precise distance between the fiber and the MS-PD / APD for optimal light collection. According to some embodiments, in order to optimize the transfer of optical signals from the fiber to the MS-PD / APD, refraction in the via 4626, particularly in the space between the fiber 4524 and the MS-PD / APD 4520. It is possible to use rate matching fluids, gels and / or polymers and / or dielectric bulks or thin films.

As mentioned above, when light is incident from the substrate side (bottom illumination), MS-PD / APD can use double and / or multiple bounces of optical signals within the MS-PD / APD. It is. This makes it possible to achieve a high quantum efficiency and to make the absorption layer thinner. A thinner absorbent layer allows for faster travel times, thereby allowing MS-PD / APD to operate at higher data rates.

FIG. 49 illustrates some aspects of a flip chip arrangement for MS-PD / APD integrated with TIA and / or another signal processing IC on a single silicon chip, according to some other embodiments. It is the schematic which shows these. The tip and mount techniques are similar or identical to those shown and described in FIGS. 45-48. In this example, a ball lens 4922 is positioned within the via 4626 to efficiently couple light from the optical fiber 4524 to the MS-PD / APD 4520. Ball lens 4922 may be located in via 4626 for alignment of the lens with respect to MS-PD / APD 4520.

FIG. 50 illustrates some aspects of a flip chip arrangement for MS-PD / APD integrated with TIA and / or another signal processing IC on a single silicon chip, according to some other embodiments. It is the schematic which shows these. The chip and mounting technique is similar or identical to that shown and described in FIGS. 45-49. In this example, the ball lens 5022 is located in the via 4626 where most or all of the silicon is etched away so that most of the light is in the air and / or fluid, gel, polymer,

solid, etc. It runs in the refractive index matching material. Further, the via 4625 acts as a guide and / or stop for alignment of the optical fiber 4626 with respect to the ball lens 5022 and further with respect to the MS-PD / APD 4520.

FIG. 51 shows some aspects of a flip chip arrangement for MS-PD / APD integrated with TIA and / or another signal processing IC on a single silicon chip, based on some embodiments. FIG. The chip and mounting techniques are similar to those illustrated and described in FIGS. 45-50, but the MS-PD / APD 5120 and TIA and / or other signal processing integrated circuits 5130 are on the top surface of the silicon chip 5110. Or it is mounted in the vicinity. The metallic conductor conduits 5132 and 5134 can be made of Al, Cu, Mo, W, Ni, TiN or the like. Conduit 5132 connects MS-PD / APD 5120 to IC electronics 5130. Conduit 5134 connects IC electronics 5130 to traces to PCB 4550 (or chip carrier) using bump technology such as solder bumps, which is a good way to connect the chip to PCB and / or chip carrier. Allows alignment. According to some embodiments, other methods using wire bonding can be used to connect the IC electronics to the traces on the PCB and / or to the chip carrier. The fiber 4524 is located in the immediate vicinity of the MS-PD / APD 5120 and the configuration includes a ball lens on the tip of the fiber 4524 and / or a ball lens between the fiber and the MS-PD / APD. Is possible. As described with respect to FIGS. 45-50, other light focusing elements such as gratings and Fresnel lenses may be used. According to some embodiments, there is a refractive index discontinuity such as buried silicon dioxide (BOX, buried oxide) and / or bulk material as shown in the MS-PD / APD structure described above. When there is a change in the effective refractive index of the microstructure with respect to the refractive index, the light irradiating from the epitaxial surface (top illumination type) is also reflected in the MS-PD / APD 5120 by the optical signal duplex and / or QI it may have multiple bounces. Double and / or multiple bounces of optical signals in MS-PD / APD allow for thinner absorption layers and shorter transit times without significantly sacrificing quantum efficiency, thereby allowing MS-PD / APD Higher data rate operation. Double or multiple bounce of light means light that is not absorbed in the MS-PD / APD path and exits the MS-PD / APD structure, and these photons are MS-PD / APD Reflected back towards the structure. Within a microstructure consisting of a plurality of holes and pillars, light may be in a resonant and / or coupled resonant state, which can result in an improved effective absorption coefficient and / or improved effective absorption length. Is possible.

FIG. 52 is a schematic diagram showing an array of multiple MS-PD / APDs integrated with IC electronics such as TIA and / or other signal processing and routing electronics on a single Si chip. The array can include, for example, 2 to more than 10 MS-PD / APDs integrated with IC electronics such as TIA and / or ASIC for signal processing, routing, storage. In the illustrated example, four MS-PD / APDs 5220, 5222, 5224, and 5226 mounted on a single Si chip 5210 are shown. These MS-PD / APDs 5220, 5222, 5224, and 5226 are connected to IC electronics 5230, 5232, 5234, and 5236, respectively. However, according to some embodiments, multiple MS-PD / APDs are connected to a single IC electronics device on a Si chip, or multiple IC electronics devices are a single MS-PD / APD. Connected to. Multiple MS-PD / APDs in the array can be the same, for example, the hole diameter and period of the microstructure is optimized for the same wavelength, eg 850-870 nm. according to other embodiments, each MS-PD / APD in the array can be optimized for different frequency bands. For example, if there are four MS-PD / APDs in the array, by optimizing the hole diameter and period of each MS-PD / APD, the four MS-PD / APDs are respectively , 850-870 nm, 875-895 nm, 900-920 nm, 920-950 nm (or any combination thereof). See, for example, Molin et al., 850-950 nm wideband OM4 multimode fiber for next generation WDM systems, OFC (2015), for next generation WDM systems, incorporate into this book. 1,5,10,16,20,25,28,32,40,56 and more are all ranges of data rates between them are standards and protocols for optical data links and applications It is possible depending on the. The optical fibers 5240, 5242, 5244, 5246 can be separate fibers or can be provided as parallel fiber ribbons. Optical fibers 5240, 5242, 5244, 5246 each carry a single band wavelength and / or multiple band wavelengths for WDM and CWDM to provide a combined data rate of 100 Gb / s to 1 Tb / s or higher. It is possible. For example, an array of 10 MS-PD / APD with 10 Fiber Channels, each of 10 Gb / s, gives a total data rate of 100 Gb / s. A 4MS-PD / APD array with 4 Fiber Channels each at 25-28 G / bs gives a total data rate of 100 Gb / s, and 2MS-PD with 2 Fiber Channels each at 56 Gb / s The / APD array gives a total data rate of 100 + Gb / s. A fibers If each fiber channel can carry multiple wavelength bands, eg 850-870 nm and 875-895 nm, and each wavelength band can transmit at 25-28 Gb / s. The array can have an overall data rate that effectively exceeds 200 Gb / s.

FIG. 53 is a schematic diagram illustrating an epitaxial structure for high data rate MS-PD, according to some embodiments. The illustrated structure can be larger than 10 Gb / s. Holes 5322 can be etched to the SiO_2 BOX layer 5304, or the holes can be etched to the P layer 5306, and / or partially etched into the P layer 5306, for example. The doping and thickness are as follows: Si substrate 5302 is 150 μm thick, BOX layer 5304 is 2-4 μm thick, and P + layer 5306 is 0.3-1 μm thick. The doping is over 1×10^{20} / cm^3 and the I layer 5308 is 1.5-2 μm thick and is not intentionally doped (less than 5×10^{15} / cm^3) The N + layer 5310 is 0.2-0.5 μm thick and the doping exceeds 1×10^{19} / cm^3. High doping of the N and P layers 5310 and 5306 minimizes the diffusion current that may shorten the minority carrier lifetime and slow down the PD response. According to some embodiments, doping as high as greater than 1×10^{20} and 1×10^{21} / cm^3 is used such that minority carrier lifetime is on the order of picoseconds and series resistance is reduced .

FIG. 54 is a schematic diagram illustrating an epitaxial structure for high data rate MS-PD, according to some embodiments. This structure and doping is similar or identical to that illustrated and described in FIG. 53, but etched until hole 5422 reaches the top of P layer 5306 and / or just enters P layer 5306. It has been different.

FIG. 55 is a schematic diagram illustrating an epitaxial structure for high data rate MS-PD, according to some embodiments. This structure and doping is similar or identical to that illustrated and described in FIGS. 53 and 54 except that the hole 5522 is etched at least halfway into the P layer 5306.

FIG. 56 is a table showing mesa dimensions, hole diameters, hole period distances, and lattice patterns for MD-PDs based on some examples. In these examples, the grid can be hexagonal or square. The hole can be circular, elliptical or polygonal. The holes have a diameter of 1300 nm with a period of 2000 nm, a diameter of 1500 nm with a period of 2050 nm, a diameter of 700 nm with a period of 1000 nm, and a diameter of 830 nm with a period of 900 nm. The operating wavelength is 800-990 nm and the material is Si. It is possible to include a thin passivation layer SiO_2 with a thickness in the range of 3-100 nm. The mesa size partially determines the capacity of the MS-PD (excluding bond pads and contact metals), depending on the data rate of the MS-PD. 5 μm, 10 μm, 20 μm, 25 μm, 30 μm, 40 μm, , 50 μm, and 80 μm. Low capacity and short transit time make MS-PD with higher data rate.

FIGS. 57A and 57B are schematic diagrams illustrating hexagonal and square grid hole patterns according to some embodiments. FIG. 57 (A) shows a hexagonal lattice pattern, and FIG. 57 (B) shows a square pattern, and "d" is the period in each case. According to some embodiments, these layouts are used for the exemplary parameters for the MS-PD shown in FIG.

FIG. 58 is a schematic diagram illustrating an epitaxial layer structure for silicon MS-PD, according to some embodiments. The thickness and doping of this structure is as follows. Si substrate 5802 is 150 μm, BOX (buried oxide) layer 5804 is 2-4 μm thick, SIP layer 5805 is 0.2 μm thick. At a thickness of ~0.5 μm the doping exceeds 2×10^{20} / cm^3 and the SI layer 5808 is about 1.5-2 μm thick and is not intentionally doped (5×10^{15} and a background doping of less than 10^{15} / cm^3). SiN layer 5810 is doped beyond and 2×10^{20} / cm^3 with a thickness of about 0.2 [mu] m. The high doping of the P and N layers can be, for example, greater than 1×10^{19} / cm^3. According to some embodiments, an etch stop layer made of a material such as SiGeB, SiGeC, or SiGeBC and having a thickness of 5 nm to 50 nm may be processed during a microstructured hole and / or mesa etch period. To help, it can be included at the interface between PSI5805 and ISI5808. If highly P-doped SiGeB is used, the structure is preferably NIP. High doping in the P and N regions, in addition to reducing sheet resistance, also reduces the minority carrier lifetime, so photons absorbed in the P and N regions contribute minimally to the photocurrent. The reduced minority carrier lifetime in the P and N regions reduces the diffusion of photogenerated carriers into the high electric field "I" region, where minority carriers are swept to the anode and cathode to photocurrent. Contribute.

FIG. 59 is a schematic diagram illustrating certain aspects of an MS-PD, according to some embodiments. Its material structure, including thickness and doping, is similar or identical to that shown and described in FIG. In the case of FIG. 59, the P and N dopings in layers 5910 and 5906 are exchanged to form a P-I-N configuration. It

should be noted that in either FIG. 58 or 59, the arrangement can be P-I-N or N-I-P. Hole 5922 is etched into SiO_2 5804 and P and N ohmic contacts 5928 and 5930 are formed for P and N layers 5910 and 5906, respectively. The mesa is etched to define the photosensitive area and to define the capacity of the PIN structure. The mesa diameter ranges from 10 μm to 80 μm depending on the data rate for which the MS-PD is designed (as described with respect to FIG. 56). For 20-40 Gb / s, the mesa diameter is typically 20-40 μm. A doped P layer 5910 greater than 2×10^{20} / cm^3 with a thickness of 0.2 μm can have a sheet resistance of less than about 50Ω. A doped N layer 5906 with a thickness of 0.2 μm and greater than 2×10^{20} / cm^3 can provide a sheet resistance of less than about 35Ω. The high doping of the P and N layers can also be set to 1×10^{19} / cm^3, for example. Thinner P and N layers allow a higher percentage of optical power to be in the "I" layer and a lower percentage in the P and N layers, thereby maximizing MS-PD quantum efficiency. Let For convenience of explanation, passivation, polyimide bridges, bond pads and other processing steps are not shown. A reverse bias voltage is applied between the P and N contacts to form a high field region in the "I" layer. The voltage is typically in the range of about 2 eV. In the case shown, the illumination is at an angle that is vertically above or offset from above. The wavelength is in the range of 800-990 nm, but other wavelengths such as 780 nm can also be used. The nominal wavelength is 850 nm, but can include wavelengths such as 810-830, 830-850, 850, 850, 930-950, 960-990, and the like.

FIG. 60 is a schematic diagram illustrating certain aspects of an MS-PD, according to some embodiments. The MS-PD, including material structure thickness and doping, is similar or identical to that illustrated and described in FIGS. In this case, the hole 6022 is etched up to and / or in the N layer 5906, but not to the SiO_2 layer 5804 as shown in FIG. Accordingly, the absorption in the N layer is not improved, and as a result, the percentage of optical power in the "I" layer may be higher. This tends to improve the quantum efficiency of the MS-PD. The SiO_2 layer 5804 may or may not be necessary.

FIG. 61 is a schematic diagram illustrating certain aspects of an MS-PD, according to some embodiments. The MS-PD is similar or identical to that illustrated and described in FIGS. 58-61, including material structure thickness and doping. In this case, the 58MS-PD is irradiated from the substrate side (also referred to as a back irradiation type or a bottom irradiation type in this document). The silicon substrate was removed via 6170 is etched are etched and penetrate up to the SiO_2 layer 5804 or most or the SiO_2 layer to the SiO_2 layer to or the SiO_2 layer in. The Si substrate 5802 is removed to minimize optical loss at the wavelength range of 800-990 nm. A reflector 6132 is fabricated on the surface of the P layer 5910, which uses a filler process such as polyimide, solid carbon dioxide, or spin-on-glass (SOG) to prevent the reflector 6132 from shorting the PIN diode. It is possible to include. It should be noted that the reflector 61.32 need not be exactly planar and can be concave in the area with the holes, which may improve the trapping of the light wave. The reflector 6132 can be a metal or alloy, such as a dielectric, Bragg reflector, conductive transparent metal oxide, silver, gold, or any combination thereof. Indium tin oxide (ITO) can also be used with a non-conductive dielectric to form a Bragg reflector. Metals and / or conductive oxides can further reduce the sheet resistance of the P layer 5910, thereby reducing parasitic resistance and improving the modulated frequency response (data rate) of the MS-PD. . According to some embodiments, the "I" layer 5908 can be made thinner in the case of backside illumination with a reflector. This is because light can travel through the "I" layer at least twice and possibly more times without degrading quantum efficiency, and at the same time the MS-PD modulation frequency (data rate). This is because it improves the response. The reason is that for the thinner "I" layer, the transit time of the photogenerated carrier is shorter. The frequency response of a photodiode is determined by its capacitance and resistance (RC time) and transit time. For example, the optical transit time may be important at a high improved effective absorption length that is greater than a factor of 100 or more for some high data rates.

FIG. 62 illustrates a Ge-on-SiPIN epitaxial layer structure for MS-PD, according to some embodiments. The material structure including thickness and doping is similar or identical to that illustrated and described on FIGS. 58-62. In this case, the NSi layer 6202 having a doping exceeding 2×10^{19} / cm^3 can have a thickness of 0.2-2 μm. A Ge "I" layer 6208 is also provided, which is not intentionally doped, the doping is less than 2×10^{16} / cm^3 and the thickness is 0.5-2 μm. The upper GeP layer 6210 with a doping exceeding 2×10^{20} / cm^3 is formed with a thickness of 0.1-0.2 μm. According to some embodiments, a thin Ge buffer layer (not shown) is used at the interface between the NSi layer 6206 and the "I" Ge layer 6208 to initiate good crystal growth of Ge on Si. It is possible. High doping of P and N also reduces minority carrier lifetime, thereby spreading photogenerated carriers that may be swept into the optical field "I" region that may contribute to the overall photocurrent. is minimized.

FIG. 63 shows a Ge-on-SiMS-PD according to some embodiments. The MS-PD is similar or identical to that illustrated and described in FIGS. 58-62, including material structure thickness and doping. The hole 6322 has been etched to the SiO_2 layer 5804, or the hole can be etched to the NSi layer 6206, in which case the SiO_2 layer 5804 may or may not be necessary. And the MS-PD is irradiated from the top or front (epitaxial surface). Photon absorption in the wavelength range of 1100 to 1800 nm is mostly in the Ge region than in the Si region. By keeping the PGe layer 6210 thin, a large percentage of the photons are absorbed in the Ge "I" layer 6208, thereby increasing quantum efficiency. The high refractive index difference between Ge and Si may require that the hole only be etched to the top of the SiN layer 6206. However, in this example, the hole 6322 is etched down to the SiO_2 layer 5804. The NSi layer 6206 can be up to 2 μm thick in this example and can be doped in the range of 1×10^{19} / cm^3 to provide a sheet resistance of less than 50Ω. is there. For 850 nm operation, or for wavelengths in the range of 800-990 nm, a thin NSi layer can increase the percentage of photons absorbed in the tGe region. A 0.2 μm thick NSi layer with a doping of more than 2×10^{20} / cm^3 provides a sheet resistance of less than 50Ω and reduces minority carrier lifetime. A 2 μm thick NSi layer can also be used for the wavelength range of 800-990 nm or 800-1800 nm. This is because for wavelengths in the 800-990 nm range, Ge absorbs more than 90% of the photons over a length of 2 μm. Therefore, less than 3% of the photons reach the NSi layer. At a wavelength of 850 nm, less than 1% reaches the NSi layer, and at 990 nm, less than 3% reaches it.

In some cases, for a wavelength range of 800-990 nm, the microstructured hole may not be used predominantly to improve absorption, but rather partially or completely within the Ge layer. It may be used to reduce the volume of the etched hole. Furthermore, holes may not be necessary and bulk Ge may be used. According to some embodiments, the microstructure can also be used to reduce reflection.

FIG. 64 shows a Ge-on-SiMS-PD according to some embodiments. The MS-PD is similar or identical to that shown and described in FIGS. 58-63, including material structure thickness and doping. In this case, the hole 6422 is etched up to the Si layer 6206. The refractive index for Ge is about 4 and the refractive index for Si is about 3.45. This difference in refractive index may give sufficiently improved absorption in the Ge region. In this case, the SiO_2 layer 5804 may not be necessary and the MS-PD may be grown on the Si wafer without the BOX layer 5804. For the 1100-1800 nm wavelength range, Si has an acceptable low optical loss and most of the absorption is in the Ge region. In the case of top illuminated MS-PD, the PGe layer can be made thin, so the bulk of the photons is absorbed in the tGe region, which increases the quantum efficiency. ITO (Indium Tin Oxide) may be used in conjunction with the PGe layer 6210 to further reduce the sheet resistance of the P layer.

FIG. 65 shows a Ge-on-SiMS-PD according to some embodiments. The MS-PD is similar or identical to that illustrated and described with respect to FIGS. 58-64, including material structure thickness and doping. In this case, the MS-PD is a back or bottom irradiation type. This structure is very good for a wavelength range of 800-1800 nm using a thin NSi layer of 0.2 μm. Less than 3% of photons having a wavelength at 800 nm are absorbed in the NSi layer 6206. Furthermore, in a single pass of 1 μm Ge, more than 85% of the 990 nm photons are absorbed. In double pass, more than 95% of 990 nm photons are absorbed. In back-illuminated MS PD where Ge is grown on NSi, with the reflector 6332 on the PGe layer, double and / or multiple passes of the photons enable a thinner I-absorption layer 6208. This reduces the transit time of light-generated electrons and holes. It is possible to obtain a photodiode with a higher bandwidth of 40 Gb / s or higher. Hole 6322 can be etched into SiO_2 layer 5804 or can be etched into Si layer 6206 (as shown in FIG. 64). For microstructured hole arrays, improved absorption can occur at wavelengths between 1100-1800 nm. For example, at 1550 nm, less than 9% is absorbed in a double pass through a 1 μm thick bulk Ge, while greater than 30% if there is a microstructured hole in the Ge layer Absorption can be achieved, and in some cases, absorption greater than 50% can be achieved. In some cases, absorption in MS-PD with a Ge layer is 70% at 1550 nm for double pass in 1 μm thick Ge or for single pass in 2 μm thick GeMS-PD. Larger things can be achieved.

The MS-PD can have the following layers: the Ge (or SiGe) P layer 6210 can be doped to a thickness of about 0.1 μm and greater than 2×10^{20} / cm^3. Yes, Ge/ (absorbing layer) 6208 can be 0.5-2.0 μm thick and intentionally undoped (less than 5×10^{15} / cm^3), and finally The SiN layer 6206 can be doped to a thickness of 0.2-0.5 μm and exceeding 2×10^{19} / cm^3. In addition, during the via etch to remove the Si substrate, the SiO_2 layer can be left unchanged, partially etched, or fully etched to remove the SiO_2 is there.

FIG. 66 is a schematic diagram showing Ge-on-SiPD according to some embodiments. The PD is similar to that illustrated and described in FIGS. 58-65, including material structure thickness and doping. FIG. 66 shows what is arranged as a flip chip, but although it slightly deteriorates due to the PSe layer, a front-illuminated arrangement is also possible. The PD is similar to the MS PD shown in FIG. 64 without the microstructured hole array. Ge-on-Si photodiodes with an epitaxial structure as illustrated for operation at 800-1300 nm, particularly utilizing double bounce or double bounce for the 1300 nm wavelength region, yet high data rate operation. Is maintained. The PD can be integrated with SiGeBiCMOS. According to some embodiments, the SiO_2 layer is omitted. With solder bump technology, the PD can be a flip chip mounted directly on a PCB, as described above for other embodiments, for example, as shown in FIGS. 44-52. According to some embodiments, the PD can have the following layers: Ge (or more than 2×10^{20} / cm^3 with a thickness of about 0.1 μm) (or SiGe) P layer 6210, 0.5 2.0 μm thick, intentionally undoped (less than 5×10^{15} / cm^3) Ge/ (absorbing layer) 6208, and finally 0.2-0 SiN layer 6206 doped with a thickness of 5 μm and exceeding 2×10^{19} / cm^3. Further, during the etching period of the via 6670 for removing the Si substrate, the SiO_2 layer 5804 is left unchanged (as shown in FIG. 65), partially etched, or the SiO_2 is removed. Therefore, it is possible to etch completely (as shown in FIG. 66). If the SiO_2 layer is completely etched away, an antireflection layer (not shown) can be applied to the SiN layer to minimize reflection.

FIG. 67 is a schematic diagram showing a Ge-on-SiPD according to some embodiments. The PD is similar to that illustrated and described in FIGS. 58-66, including material structure thickness and doping. In this case, a void 6722 is formed to reduce the device PIN junction capacitance. Void 6722 can be partially etched into the Ge layer to remove a sufficient amount of material to reduce the volume by a certain amount. The capacity reduction allows for a larger area PD while maintaining the same data rate bandwidth as a similar Ge-on-SiPD without voids. The larger area PD allows for greater tolerances in optical fiber and / or light source misalignment with respect to the photodiode. The data rate bandwidth is determined by RC time and travel time. Integration of all the structures described above is possible with electronics such as TIA that can be directly attached to the PCB along with solder bump technology. According to some embodiments, the operating wavelength for this structure is in the range of 800-1300 nm and the data rate is over 40 Gb / s.

Note that it is not necessary to use a BOX structure. This PD is possible to have a layer such as the following, namely, GEP layer is doped beyond the 2×10^{20} / cm^3 with a thickness of about 0.1μm 6210,0.5-1. Ge/ (absorptive layer) 6208 with a thickness of 0 μm and not intentionally doped (less than 5×10^{15} / cm^3), and finally 2×10^{19} / cm with a thickness of 0.2-0.5 μm A SiN layer 6206 doped over ^{3} and a 2-4 μm buried oxide layer 5804.

FIG. 68 is a schematic diagram illustrating certain aspects of a microstructured avalanche photodiode (MS-APD), according to some embodiments. The MS-APD can have the following layers: SiP layers 6810, 0 P-doped with a thickness of about 0.1-0.2 μm and exceeding 2×10^{19} / cm^3. Unintentionally doped with a thickness of 5-2.0 μm (less than 5×10^{15} / cm^3) Si (absorbing layer) 6808, 2×10^{19} with a thickness of 0.2-0.5 μm A SiN layer 6806 that is n-doped over / cm^3 and a 2-4 μm thick buried oxide layer 6804 on the Si substrate 6802. The MS-APD device has two additional layers: a charge layer and a multiplication layer. The charge layer 6820 is directly below the absorption l layer 6808. The SiP charge layer 6820 is doped to about 1.8×10^{17} / cm^3 and has a thickness of about 0.1 μm. Immediately below the charge layer is the MS-APD multiplication layer 6818. The SI layer 6818 is intentionally undoped (less than 1×10^{16} / cm) and has a thickness of about 0.5 μm. Via 6870 has been etched through the silicon substrate to the SiO_2 layer (anti-reflection coating can be applied to minimize reflection) and light having a wavelength in the range of 800-990 nm has passed through the via. Applied through. A reflector 6832 on the top surface of the MS-APD provides double / multiple passage of photons through an absorbing "i" layer 6808. One advantage is a thinner absorbent layer, which allows for shorter transit times. Therefore, the data rate bandwidth of the MS-APD is improved. Microstructure mold cavity array 6822 is etched until until the SiO_2 layer 6804 and / or most the SiO_2 layer. P and N contacts 6828 and 6830 are shown on the same surface to be soldered, so that the MS-APD is flip chip mounted directly on a ceramic multichip carrier and / or on a printed circuit board. It is possible. For convenience of explanation, only the most basic processing steps are shown. Additional steps or elements such as passivation, bond pads, polyimide / spin on glass planarization, antireflective coating, etc. are not shown. Further, after the Si substrate is removed during the etch of via 6870, the SiO_2 layer may be partially etched away or completely etched away for either MS-APD or MS-PD structures. Is possible. In the absence of the reflector 6832, the optical signal can also be incident from the top surface.

FIG. 69 is a schematic diagram illustrating certain aspects of a microstructured avalanche photodiode (MS-APD), according to some embodiments. The MS-APD is similar to that illustrated and described in FIG. 68, including material structure thickness and doping. The microstructured hole array 6922 is etched down to the charge layer 6820, multiplication layer 6818, and / or N layer 6806 of the APD structure. The hole 6922 is not etched until the SiO_2 layer. Light is irradiated through the via 6970 from which the silicon substrate has been removed to the SiO_2. The SiO_2 layer can also be etched so that light is directly incident on the N/SI layer 6806. This is applicable to all bottom illuminated MS-PD and MS-APD devices, in which case the antireflection coating can be applied directly to Si. For wavelengths in the range of 800-990 nm, a thin N/SI layer 6806 of about 0.2 μm is preferred to reduce absorption in regions away from the absorbing "i" layer 6808. Light can also be obtained from the top / front, in which case the reflector 6832 is eliminated. In such cases, vias may be omitted and the Si "i" layer may be increased to 1.5-2 μm for quantum efficiencies greater than 30%. In some cases, the quantum efficiency is over 50%, in some cases over 70%, and in some cases over 80%. The avalanche multiplication factor or gain can be greater than two. In some cases, the gain is greater than 5. In some cases it is more than 10. In some further cases, it is greater than 15 and in some other cases the gain is greater than 20. The data rate bandwidth can exceed 10 Gb / s. In some cases the bandwidth is greater than 15 Gb / s and in some cases greater than 30 Gb / s. Furthermore, the SiO_2 layer can be completely or partially removed and / or it can have voids that are filled or not filled with Si for MS-PD and MS-APD. It is possible to use an etch stop layer such as SiGaB, SiGeC or SiGeBC during the removal of the Si substrate to form vias used for back / bottom illumination.

FIG. 70 is a schematic diagram showing an MS-APD without the SiO_2 layer according to some embodiments. The MS-APD is similar to that illustrated and described in FIGS. 68-69, including material structure thickness and doping. The etch stop layer 7034 is SiGe or SiGeC or SiGeB (the SiGe has about 1% Ge and is highly doped with boron above 1×10^{20} / cm^3) and has a thickness of It is in the range of 0.1 to 2 μm. SiGeBC can be grown on a Si substrate 6802 and / or on a Si epitaxial layer such as NSi layer 6806. According to some embodiments, the MS-APD has the following thicknesses and doping levels: SiN layer 6808 has a thickness and doping level in the range of 0.2-1 μm. SiN layer 6806 has a thickness in the range of 0.2 to 1 μm and a doping in the range of greater than 2×10^{19} / cm^3 to greater than 2×10^{20} / cm^3, and SI/ the multiplication layer 6818 is intentionally undoped (less than 1×10^{16} / cm^3) and has a thickness of about 0.5 μm, and the SiP charge layer 6820 is about 1.8×10^{17}/ SI absorption layer 6808 is intentionally undoped (less than 5×10^{15} / cm^3) and 0.5 μm / cm^3 and has a thickness of about 0.1 μm. -1.0μm thick And which have and have SiP capping layer 6810 2×10^{20} / cm^3 to beyond the thickness of and about 0.1μm is doped. According to some embodiments, multiple etch stop layers can be used. For example, another etch stop layer can be formed at the interface between the Si multiplication layer 6818 and the SiN layer 6806. The thickness of the etch stop layer can range from 1 nm to 100 nm and should be doped to P or N or not intentionally doped to match the electrical properties of adjacent layers. It is possible. The wavelength of the optical signal can range from 800 to 990 nm, and when illuminated from the back side, the reflector can be formed from a dielectric such

as SiO_2 / Ag. According to some embodiments, the reflector 6832 is a Bragg reflector made of two dielectrics such as ITO with SiO_2 and HfO_2 , or Ag, Au and / or Pt with different refractive indices. The reflector 6832 is used to reflect the unabsorbed signal photons through the absorbing SiI region 6808 for double and / or multiple passes. Furthermore, the device can be of the front-illuminated type, in which case the reflector 6832 is omitted and the absorbing SiI layer 6808 is thickened to 1.5-2 μm to optimize quantum efficiency. According to some embodiments, the front / top illuminated MS-APD can also include vias. Similarly, some MS-PDs can use this structure, omitting the SiP charge layer and SiI multiplication layer. Front and back illuminated MS-PD may be beneficial. This is because removal of the Si substrate improves the refractive index contrast and has an improved absorption coefficient in the microstructure, which improves the quantum efficiency.

In the MS-PD / APD data rate response (also called frequency response), high doping of the P and N layers reduces sheet resistance and reduces the lifetime of minority carriers in the P and N layers. Reduces minority carrier diffusion into the high-field SiI absorption layer that may cause degradation. The microstructured hole array can be etched beyond the stop layer either up to the SiGeC and / or SiGeB stop layer and / or during the hole etch period and / or during the via etch period. The etch stop layer can also be completely or partially removed after the hole etch or during the via etch. Thus, there is no SiGeC, SiGeBC or SiGeB layer in the optical path for back-illuminated MS-PD / APD. It should be noted that in SiGeB where Ge is about 1% (eg, $Si_{0.99}Ge_{0.01}$), its band gap is about the same as that of Si. Furthermore, as in FIG. 69, the microstructured hole array is etched to a depth corresponding to the absorbing SiI layer and / or to a depth larger than the SiI absorbing layer and partially into the avalanche region, is possible.

FIG. 71 is a schematic diagram illustrating a Ge-on-Si microstructured avalanche photodiode (MS-APD), according to some embodiments. The MS-APD is similar to that illustrated and described in FIGS. 68-70, including material structure thickness and doping. The GeI absorption layer 7108 is intentionally undoped (less than 5×10^{15} / cm^3) and has a thickness of 0.5-2.0 μm. The top GeP capping layer 7110 is doped in excess of 2×10^{20} / cm^3 and has a thickness of about 0.1 μm. The microstructured hole array 7122 has been etched to the SiP charge layer 6820 or just before the SiP layer. Alternatively, the holes 7122 can be etched into the SiP charge layer 6820 and / or into the SI multiplication layer 6818. Via 6970 is etched to remove the Si substrate from the optical path. The SiO_2 layer can be left unchanged, partially etched or etched completely through, or an NSI substrate without SiO_2 can be used. In the case where the SiN layer 6806 is exposed, an antireflection layer (not shown) can be provided to minimize reflection. The wavelength range can be, for example, 800-1600 nm, 1300-1600 nm, 810-880 nm, 930-990 nm. The hole size and period can be optimized for a range of wavelengths. A reflector 6832 can be formed on the PSe or SiGe layer 7110. The reflector 6832 can be composed of dielectric and metal, ITO (indium tin oxide or similar transparent conductive oxide) and metal, all dielectric such as Bragg reflector, or any combination thereof. It is. Reflector 6832 reflects the photons that were not absorbed in the first pass back toward absorbing GeI layer 7108 for two or multiple passes. It is possible to use a thinner GeI absorber layer 7108 compared to a single pass photodiode. The thinner GeI layer results in shorter transit times and thus higher data rates. Ge-on-Si growth may use a Ge buffer layer, which is grown to initiate high quality crystal growth of Ge. See, for example, Kang et al., Epitaxially-grown Ge / Si avalanche photodiodes for 1.3 Em light detection, Vol. 16, no. 13 / OPTICS EXPRESS 9365 (2008) (hereinafter referred to as "Kang et al"), which is incorporated herein by reference. In the wavelength range of 1200-1750 nm, the via 7270 is not necessary because Si is almost transparent at these wavelengths. Further, in the absence of reflector 6832, the optical signal can be incident from the top surface and Ge "I" layer 7108 can increase the thickness to about 2 microns.

FIG. 72 is a schematic diagram illustrating a Ge-on-Si microstructure avalanche photodiode (MS-APD), according to some embodiments. The MS-APD is similar to that illustrated and described in FIGS. 68-71, including material structure thickness and doping. In this case, the microstructure hole array 7222 is etched down to the SiO_2 layer 6804. According to some embodiments, the holes 7222 are etched to a sufficient number of micrometers of the SiO_2 layer 6804 and the vias 7270 are etched to the SiO_2 layer. The SiO_2 layer can remain unchanged during the via etch, can be partially etched, or can be etched completely through. The light incident from the back side has a wavelength in the range of 800-1800 nm. Other wavelengths such as 630-780 nm can also be used. There may be some photogenerated carriers in the SI layer, but the bulk of the photogenerated carriers is in the GeI layer 7108, especially in the wavelength range of 800-1800 nm, especially 1100 in the wavelength range of ~1800 nm. The epitaxial structure is similar to that shown in FIG. 71 because the reflector 6832 on the GeP layer reflects light back toward the GeI absorbing layer. The removal of the SiO_2 layer allows a high reflection index contrast between the microstructured semiconductor holes, which can improve the light collection characteristics of the microstructured hole array and air. Further, SiO_2 - air interface and SiO_2 - reflections that occur at the semiconductor interface has been removed. In the case of front-illuminated MS-APD, the reflector 6832 is removed and the GeI absorption layer 7108 is thickened to a range of 1-2 μm. The removal of the via and SiO_2 can be performed for front side irradiation type MS-APD. By removing the avalanche layer, P charge and I multiplication, the MS-APD becomes MS-PD.

FIG. 73 is a schematic diagram illustrating a Ge-on-Si microstructure avalanche photodiode (MS-APD) with an etch stop layer, according to some embodiments. The MS-APD is similar to that illustrated and described in FIGS. 68-72, including material structure thickness and doping. An etch stop layer 7334 such as SiGe, SiGeC, SiGeB, or SiGeBC is grown on the Si wafer. It should be noted that the SI substrate (wafer) 6802 already has an NSI epitaxial layer, a subsequent APD layer, other buffer layers, spacer layers, or other etch stop layers (not shown). On the surface, which promote good crystal growth and process reproducibility. The basic APD layer has a SiN layer 6806 with a thickness ranging from 0.2 to 0.5 μm and a doping exceeding 2×10^{19} / cm^3 to exceeding 2×10^{20} / cm^3 . SI multiplication layer 6818, intentionally undoped and having a thickness of about 0.5 μm, doped to about 1.8×10^{17} / cm^3 and has a thickness of about 0.1 μm SiP charge layer 6820, GeI absorption layer 7108 which is not intentionally doped and has a thickness of 0.5-1.0 μm, and the doping is greater than 2×10^{20} / cm^3 and the thickness is A Ge or SiGeP capping layer 7110 that is about 0.1 μm. Microstructured hole arrays are etched with hole diameters and periods that are optimized for specific wavelength ranges. Specific group length ranges include the following: 800-860, 860-880, 880-930, 920-990, 990-1100, 1100-1350, 1350-1450, 1450-1550, 1550-, 1650, 1650-1800 nm. Hole and mesa passivation are omitted for convenience of explanation, examples of which are shown in Kang et al. There are other methods of passivation in the literature. Light enters from the back side through the via 7370, and in this case, the etch stop layer can be removed. Although light can be incident from the front side, the thickness of the absorbing GeI layer 7108 is increased to a range of about 1-2 μm. In the case of front-illuminated MS-APD / PD, for example, the via can be implemented to increase the reflection index contrast between the semiconductor microstructure and air. Other layers such as planarization layers, bridge layers, bond pads, and fillers are not shown for convenience of explanation.

FIG. 74 is a schematic diagram illustrating a Ge-on-Si microstructured avalanche photodiode (MS-APD), according to some embodiments. The MS-APD is similar to that illustrated and described in FIGS. 68-73, including material structure thickness and doping, but to reduce absorption of photocarriers in the P contact layer. The difference is that the GeP layer is replaced with a P layer 7410 of SiGe or SiGeC. SiGe and / or SiGeC have a larger bandgap than Ge, so that for the same thickness, the absorption coefficient is smaller than in Ge. For example, Kolodzey et al., "Optical and electronic properties of SiGeC alloys grown on Si substrates", Journal of Crystal Growth 157, 386-391 (1995) (hereinafter referred to as "Kolodzey et al"), which is incorporated herein by reference. For example, from Kolodzey et al, for $SiGe_{0.99}C_{0.12}$, the band gap is 1.3 eV (direct) compared to 1.11 eV for Si and 0.66 eV for Ge, is there. SiGe alloys provide a band gap between SI and Ge, so any addition of Si to Ge will increase the band gap and reduce absorption in the P layer. According to some embodiments, this P layer replacement technique applies to all MS-PD / APD structures shown and described herein. In particular, the GeP layer is replaced with a SiGeP and / or SiGeCP layer. According to some further embodiments, in all MS-PD / APDs shown and described herein, the SiP and N layers can also be completely or partially replaced by SiGeCP and SiGeCN. Yes, which reduces the absorption of optical signals in the P and N regions of the MS-PD / APD. In some cases, the APD multiplication region, which is Si, can also be replaced with SiGeC I to reduce optical photon absorption in the present invention. At a wavelength of 1200-1750 nm, Si is almost transparent and either or both of via 7370 and etch stop layer 7334 are not needed. In this case, the back surface is polished using an NSI substrate and an antireflection coating is applied.

FIG. 75 is a schematic diagram illustrating another SiNIP epitaxial layer structure for MS-PD, according to some embodiments. Hole 7522 has been etched to a depth of about 2.3 μm and can be terminated a few microns before and / or after SiP layer 7506. The doping and thickness are approximately as follows: SiP substrate 7502, which can exceed 1×10^{19} / cm^3, but with P doping exceeding 2×10^{20} / cm^3 is 0. 2 μm (or 0.1-1 μm range) SiP layer 7506, intentionally undoped, background doping less than 5×10^{16} / cm^3 and in some cases 5×10^{15} SiI layer 7508 that is less than / cm^3 and has a thickness in the range of about 2 or 1-2.5 μm, the doping is greater than 2×10^{19} / cm^3 and the thickness is about 0.3 μm or 0.1μSi layer 7510 in the range of 2-0.5 μm. N contact 7528 is on SiN layer 7150. The P contact may be on the top surface of the SiP substrate as in contact 7530 and / or on the bottom / back side of the substrate as in contact 7532. A mesa etch is used to define the PIN junction area and hence the capacitance. Mesa can be etched down to P layer 7506 and / or P substrate 7502 and P contact 7930 can be deposited on SiP layer 7506 and / or on the back side 7532 of SiP substrate 7502. According to some embodiments, other electrical isolations can be used, such as proton bombardment to define a PIN area or other doping such as PN junction doping or trench doping. Technology. in this structure, light is incident from the front side at a wavelength in the range of about 800-990 nm. A period of 2000 nm and a hole diameter of 1300 nm and a period of 2000 nm and a hole diameter of 1500 nm can be used in either hexagonal and / or square lattice patterns. According to some embodiments, the hole diameter ranges from about 900 nm to 1500 nm and the period ranges from about 900 to 2300 nm.

76 (A)-(C) are schematic diagrams showing SiN-I-P epitaxial layers on a buried oxide for MS-PD, according to some embodiments. In FIG. 76A, holes 7622 have been etched into the SiP layer 7606 and have been partially etched into the SiP layer and / or into the SiO_2 layer 7604. The doping and thickness are approximately as follows: SiBOX (buried oxide) 7604 in the substrate 7602, 1 μm (or 0.1-1 μm of P doping exceeding 2×10^{20} / cm^{-3}) Range) SiP layer 7606, intentionally undoped and having a background doping of less than 5×10^{16} / cm^{-3} and in some cases less than 5×10^{15} / cm^{-3} A SiI layer 7608 with a thickness in the range of 2 μm or 0.5-2.5 μm, and a doping greater than 2×10^{19} / cm^3 and a thickness of eg 0.3 μm or 0.2-0.5 μm The range is the NSi layer 7610. N and P contacts 7628 and 7630 can be on the front side, in which case the P contacts are formed after mesa etching to the P layer 7606. An etch stop layer such as SiGeB or SiGeC can be used at the interface between the P layer 7606 and the I layer 7608. If a reflector is placed on the top surface SiN layer 7610 so that light is incident from the back side and light can pass multiple times through the I layer 7608, the I layer 7608 is The thickness can be reduced, for example, 0.5-1 μm. P and N can be exchanged, and the microstructure photodiode (MS-PD) can be, for example, a PIN. When SiGeB is used as an etch stop layer, the SiGeB is highly P-type and the NIP structure is preferred. The etch stop layer can be, for example, 0.05 to 1 μm thick and can replace the SiP layer in whole or in part. With appropriate modification of the device or the epitaxial layer, light can be incident from the front side and / or from the back side. The wavelength range is about 800-990 nm.

In FIG. 76 (B), the PSi layer 7606 in FIG. 7b (A) has a P doping exceeding 2×10^{20} / cm^3 and a thickness in the range of 0.5 μm or 0.2-1 μm. It is replaced with a $Si_{0.99}$ $Ge_{0.01}$ B layer 7616. All other layers are as shown in FIG. Microstructure mold holes 7622 can be etched and stop in the SiGeB layer and / or pass through the SiGeB layer and stop in the SiO_2 layer and / or can enter the SiO_2 layer It is. It is possible to etch a via 7670 that penetrates either or it stops at or the SiO_2 layer in the stop in the SiO_2 layer. N and P ohmic contacts 7628 and 7630 are formed on the SiN layer and the SiGeBP layer, respectively. Light can be incident either from the top surface (epi surface) and / or from the bottom surface (substrate surface), and with a dielectric spacer layer to pass multiple times through the I absorbing layer It is possible to place a reflector on either the top or bottom. The wavelength is in the range of 800 to 1000 nm. Those not shown for convenience of explanation are other elements such as a passivation layer, a polyimide bridge layer, a mesa, and a bond metal.

In FIG. 76C, a PSi layer 7628 having a thickness of about 0.1 μm and a doping greater than 1×10^{20} / cm^3 is added as a first layer on SiO_2 7604, and P A $Si_{0.99}$ $Ge_{0.01}$ B layer 7616 with a doping greater than 1×10^{20} / cm^3 and a thickness of about 0.3 μm is grown. As in FIGS. 75A and 76B, light can be incident from the top and / or bottom surface where the via is etched. N and P ohmic contacts are respectively disposed on the N and P layers. Microstructured hole array 7622 is etched through SiO_2 layer 7604 and / or partially etched into P layer 7628. If light is incident from the bottom, the via 7670 can be etched into the silicon substrate 7602 and into the SiO_2 layer 7604, where the SiO_2 layer 7604 can be partially or fully etched. A reverse bias voltage of 1-10 volts is applied between the P and N contacts.

In some applications, light can be incident simultaneously from the top and bottom of the MS-PD / APD. The light can have the same or different wavelength, data rate, polarity, and amplitude for coherent optical communications. The advantage of light entering from both the top and bottom is that there is no need to use a beam splitter and a 3 dB savings in optical power loss can be made.

FIG. 77 is a schematic diagram illustrating an MS-PD comprising a SiNIP epitaxial layer and a SiGeB etch stop layer on a PSi substrate, according to some embodiments. The etch stop layer 7716 can be comprised of about 1% Ge in $Si_{0.99}$ $Ge_{0.01}$ B or SiGe, in which case its band gap is substantially the same as Si and B doping is It exceeds 1×10^{20} / cm^3. This high degree of P doping may cause partial or complete replacement of the SiP layer 7706. These layers and thicknesses can be as follows: SiP substrate 7702, SiGeB layer 7716 with a thickness of 0.1-2 μm, P doping exceeding 2×10^{20} / cm^3 A 0.2 μm (or 0.1-1 μm range) SiP layer 7706, intentionally undoped, with a background doping of 5×10^{16} / cm^3 and in some cases $5 \times$ A SiI layer 7708 that is less than 10^{15} / cm^{-3} and has a thickness in the range of 2 μm or 0.5-2.5 μm, and a doping that is greater than 2×10^{19} / cm^3 and a thickness of 0. The NSi layer 7710 is in the range of 3 μm or 0.2-0.5 μm. Both N and P contacts 7728 and 7730 can be on the front side. The P contact can also be on the back side of the PSi, as in contact 7732. Microstructured hole array 7722 can be etched into SiGeB etch stop layer 7716. Mesa is etched into the SiP and / or into the SiGeB layer to define the NIP area and thus the NIP capacity. P contact 7730 can be disposed on PSi layer 7706 or PSiGeB layer 7716. N contact 7728 is disposed on SiN layer 7710. To remove the Si substrate, a via 7770 can be etched down to and / or partially into the SiGeB layer using an etching process different from that for the Si and SiGeB. . The SiGeB layer 7716 can also be etched away, in which case the via 7770 extends to the SiP layer 7706. Further, the SiP layer 7706 can be partially or entirely replaced with the SiGeB layer. In such a case, it is desirable that a SiGeB layer of at least 0.2 to 0.3 μm remains. Light can be incident from the front and / or back side. It is possible to provide a dielectric metal reflector with a dielectric in contact with the semiconductor and a thickness of 0.5-4 μm, in which case the dielectric is SiOx, polyimide, SiO_2, calcium fluoride. Alternatively, it can be silicon nitride, followed by a metal or alloy such as Ag, Au, Al, Ni or the like on either the front side or the back side. For example, when the dielectric metal reflector is disposed on the back side, light from the front side can be reflected many times through the absorbing I layer, and conversely, the reflector is arranged on the front side, the light from the back side can be reflected many times through the absorbing I layer. If there is a reflector, it is possible to use a thinner I layer, for example 1 μm or about half the thickness of MS-PD without a reflector, which means that it is possible to achieve a higher data rate for the MS-PD. In the case of the MS-PD, it is possible to use a wavelength range of 800-990 nm. In some cases, the reflector can simply be a metal such as a Bragg mirror. Furthermore, the via 7770 may not be necessary if the light is incident only from the front surface and two and / or multiple reflections are not realized.

FIG. 78 is a schematic diagram illustrating Ge-on-SiNIP on a SiGeB epitaxial layer for MS-PD, according to some embodiments. Microstructured hole array 7822 has been etched in Ge layers 7810 and 7808 and into or to SiP layer 7806. The etch stop layer 7816 is composed of $Si_{0.99}$ $Ge_{0.01}$ B or about 1% Ge of SiGe, where the band gap is substantially the same as Si and the B doping is 1×10^{20} / Cm^3 is exceeded. This high degree of B doping may partially or fully replace the SiP layer 7806. These layers and thicknesses can be as follows: the SiP substrate 7802, the SiGeB layer 7816 is 0.1-2 μm thick, and the SiP layer 7806 is 0.2 μm (or 0.2 μm). 1-1 μm range), P doping is 1×10^{19} / cm^3, GeI layer 7808 is not intentionally doped and background doping is less than 5×10^{16} / cm^3 and several in this case, the thickness is less than 5×10^{15} / cm^3, the thickness is in the range of 2 μm or 0.5-2.5 μm, and the NGe layer 7810 has a doping exceeding 2×10^{19} / cm^3. The thickness is in the range of 0.2 μm or 0.2-0.5 μm. Both N and P contacts 7828 and 7830 can be on the front side. The P contact may be on the back side on the PSi substrate, as in contact 7832. A Ge buffer

layer of several nm can be grown between the Si layer and the Ge layer, and the growth conditions of the Ge buffer layer in that case are different from the growth conditions of the Ge! layer. Vias 7870 can be etched into the Si substrate 7802 to remove the Si up to the SiGeB layer 7815. The SiGeB layer 7816 can be partially and / or fully etched under different etch conditions. The light can be incident from either the front side or the back side, and in the presence of a reflector, the photons pass multiple times through the I absorption layer and the device operates at a higher data rate. It is possible to use thinner layers for the purpose. This is because the transit time of photogenerated carriers of electrons and holes is much shorter. The wavelength range is 800 to 1600 nm. The hole diameter and array period can be optimized for a range of wavelengths ranging from about 30-100 nm. Via 7870 may not be required if the optical signal is incident from the front / top surface. In addition, if the optical signal has wavelengths in the range of 1200-1750, the silicon is almost transparent at these wavelengths or the optical loss generated is very low, so in the case of bottom illumination. There may be no need for vias.

FIG. 79 is a schematic diagram illustrating a Ge-on-Si epitaxial structure for MS-PD, according to some embodiments. Its material structure is as follows: SiN substrate 7902 (or alternatively NIP structure on PSI substrate), 8.2 μm (or 0.1 μm) with N doping exceeding 2×10^{19} / cm^3. SiN layer 7906 (in the range of ~1 μm), intentionally undoped, with background doping of less than 5×10^{15} / cm^3 and in some cases less than 5×10^{15} / cm^3. A GeI layer 7908 with a thickness of 2 μm or a thickness range of 0.5-2.5 μm, and a doping of 2×10^{20} / cm^3 and a thickness of 0.2 μm or 0.2-0.5 μm The PGe layer 7910 is in the range of Both P and N contacts 7928 and 7930 can be on the front side. The microstructured hole array 7922 is etched to the NSI layer 7906, partially etched into it, or etched through it. A mesa etch defines the PIN area and volume. N contacts 7930 and 7932 are deposited after the mesa etch on either the front or back surface of the NSi substrate. Passivation is not shown, but Kang et al. Can be used to deposit amorphous Si on the exposed Ge surface sidewalls and anneal at high temperatures and / or SiGe on the exposed Ge sidewalls it can be deposited and annealed to reduce leakage current. The mesa diameter in the MS-PD and MS-APD can be in the range of 5 μm to 100 μm depending on the data rate. According to some embodiments, the mesa diameter range is 20-40 μm for a data rate of 30 Gb / s. Furthermore, a buffer Ge layer can be used between NSI 7906 and IGe 7908 to ensure high crystal quality. For example, Kang et al. Good to see. When light enters from the front side, the wavelength can be in the range of 800-1800 nm. In a preferred range, the wavelength can be 1450-1600 nm, and in another preferred range, for example, 1250-1600 nm. The MS-PD / APD can cover both data communication wavelengths and telecommunications wavelengths.

FIG. 80 is a schematic diagram illustrating another Ge-on-Si epitaxial structure according to some embodiments. The MS PD, including the thickness and doping of its material structure, is similar or identical to that illustrated and described in FIG. 79, but it is a buried oxide having a thickness of 0.2-4 μm. The difference is that it is grown on a SiBOX wafer comprising a physical layer 8004. Microstructured hole array 8022 can be etched to NSI layer 7906 and etched into or until NSI layer 7906 or to SiO_2 layer 8004. A mesa etch defines the PIN capacity and the mesa diameter for the MS-PD / MS-APD is in the range of 5-100 μm depending on the data rate bandwidth of the MS PD / APD. A mesa diameter of 20-50 μm is preferred for a data rate bandwidth of 23-35 Gb / s. Light can be incident from the front or back surface. At wavelengths above 1100 nm, the optical loss of Si is very low and the Si substrate can be used, for example, to etch lenses or gratings. Via 8070 can be etched to completely or partially remove SiO_2. Via 8070 can be used to guide light and / or fiber to, for example, the MS-PD. It is possible to deposit a reflector 8070 in the via 8070, in which case the SiO_2 is completely free so that light from the front side bounces off the reflector and traverses the IGe absorption region 7908 multiple times. No removal or no removal at all. If the reflector is on either the front side or the back side, IGe 7908 can be thinner, for example 1 μm, which reduces the electron hole transit time and the MS-PD / MS- increase APD data rate bandwidth. The wavelength can be in the range of 800-1800 nm, which covers both data communication and telecommunications wavelength ranges. In the case of a continuous NSI layer 7906, for example, if the SiO_2 layer is completely etched, an anti-reflective coating can be applied to the bottom surface of the NSi.

FIG. 81 is a schematic diagram illustrating a Ge-on-Si epitaxial structure according to some embodiments. The MS-PD is similar or identical to that illustrated and described in FIGS. 79-80, including the thickness and doping of its material structure, but the via 8170 has a SiO_2 8C8 layer 8084, or the SiO_2 thickness or range of 0.2-4μm the etched and and 2-4um partially etched to either completely etched, or it may be one that does not etch is different. Further, it is possible to form a reflector 8172 made of a material such as Ag, Au, Cr, or Al. The reflector 8172 can also be a broadband, narrowband, or passband Bragg reflector. It should be noted that if the reflector 8172 is a dielectric, it can be deposited directly on the NSI layer 7906 by etching away the SiO_2 layer. Light incident from the front side that was not absorbed in the first pass through the IGe layer 7908 can be reflected back to the IGe layer for multiple passes through the IGe absorption layer. . The IGe layer can be thinner, for example 1 μm, which makes the transit time for electrons and holes in the IGe layer shorter. This increases the data rate bandwidth of the MS-PD / MS-APD.

82A-82C relate to a simulation using finite difference time domain (FDTD) for a Ge-on-Si microstructured photodiode similar to the structure illustrated in FIG. FIG. 82A is a schematic diagram showing a Ge-on-Si microstructure photodiode subjected to simulation. The hole pattern is a square lattice pattern. Simulations are performed for two combinations of hole period and hole diameter: 2500 nm hole period and 1500 nm diameter, and 2300 nm hole period and 1300 nm diameter. In FIGS. 82B and 82C, the horizontal axis is the wavelength in μm and the vertical axis is absorption, which is directly related to quantum efficiency. In each case, a square grid pattern of holes is simulated. In FIG. 82B, for an optical signal having a wavelength in the range of 800 nm to 1000 nm, curve 8210 is a plot of absorption versus 2300 nm hole period and 1300 nm diameter, and curve 8212 is 2500 nm hole period and 1500 nm. is a plot of absorption versus diameter. In FIG. 82C, for an optical signal having a wavelength in the range of 1000 nm to 1600 nm, curve 8220 is a plot of absorption versus 2300 nm hole period and 1300 nm diameter and curve 8222 is 2500 nm hole period and 1500 nm. It is a plot of absorption versus diameter. Absorption ranging from 0.4 (absorbs 40% of photons) to more than 0.9 (absorbs 90% of photons) in the wavelength range of 0.8 to 0.98 μm was determined. . Absorption greater than 0.5 is seen for 1.55 μm and extends to 1.6 μm for an approximately 2 μm absorption layer of Ge. This is significantly larger than the 2 μm thick equivalent Ge layer without the microstructure, especially at 1550 nm and longer wavelengths.

83A-83C relate to a simulation using finite difference time domain (FDTD) for a Ge-on-Si microstructured photodiode similar to the structure in FIG. FIG. 83A is a schematic diagram showing a Ge-on-Si microstructure photodiode that is simulated with light incident from the top surface. In the graphs of FIGS. 83B and 83C, the horizontal axis is the wavelength in μm and the vertical axis is absorption, which has a period of 2500 nm and a diameter of 1500 nm (curves 8312 and 8322), a period of 2300 nm and a diameter of 1300 nm (curve). 8310 and 8320) directly related to the quantum efficiency for a multi-hole square lattice. Absorption greater than 0.7 (absorbs 70% of photons) is seen for 1.55 μm and better than 0.5 absorption (absorbs 50% of photons) for an approximately 2 μm absorption layer of Ge it extends to 1.6 μm. This is significantly greater than, for example, an equivalent InGaAs layer lattice matched to InP having a thickness of 2 μm at 1630 nm and longer wavelengths.

84A and 84B show the results of a simulation using finite difference time domain (FDTD) for a Ge-on-Si microstructured photodiode. The simulated structure is shown in FIG. 82A. In FIGS. 84A and 84B, the horizontal axis of the graph is wavelength in μm and the vertical axis is absorption, which is directly related to quantum efficiency for both square and hexagonal lattices for the hole array. ing. FIG. 84A shows both a square lattice (curve 8410) and a hexagonal lattice (curve 8412) with a period of 2300 nm and a hole diameter of 1300 nm. Absorption greater than 0.9 (absorbing 90% of the photons) is shown for the 1.55 μm wavelength with the region where the absorption varies by less than 10% over the 50 nm wavelength span. FIG. 84B shows both a square (curve 8420) and hexagonal (curve 8422) lattice for a diameter of 1500 nm with a period of 2500 nm, which shows an absorption of 0.7 at 1.55 μm. . Overall, the hexagonal lattice shows better photon absorption than the square lattice. Other combinations of period and hole diameter, hole shape and grating can be used to improve or optimize absorption in certain wavelength ranges.

FIG. 85 shows a schematic plan view of a microstructured photodiode chip, not to scale, according to some embodiments. The approximate dimensions of the chip 8580 are 350 μm × 300 μm × 150 μm. The mesa defined by mesa edge 8582 has a diameter of 30 μm. The mesa defines a NIP or PIN junction capacitance. An upper surface 8510 is visible at the top of the mesa (eg, an N layer taking NIPMS-PD / APD), and a microstructured hole 8522 is also visible. Near the outer edge of the mesa is an N ohmic contact ring 8528 (takes NIPMS-PD). There is a P-ohmic contact ring 8530 outside the mesa. N bond pad 8560 is electrically connected to N ohmic contact

8528 by bridge interconnect 8582. Similarly, P bond pad 8590 is connected to P ohmic contact by interconnect 8592. According to some embodiments, undesired shorts between the bridge interconnect 8582 and the area 8506 (which may be the P layer surface) use an insulator such as polyimide deposited between them. Has been prevented. It should be noted that the above description is also applicable to a PIN placement MS-PD / APD where the N and P layers and contacts are reversed.

According to some embodiments, a simple process flow of the basic manufacturing steps of a NIPMS-PD structure on a BOXSi wafer consists of (1) masking and etching the hole array 8522 into the SiO_2 layer; (2) Mask and deposit N ohmic contact metal ring 8528 on N layer 8510; (3) Etch mesa defining mask and define junction capacitance; Etch to P layer 8506; (4) Mask and SiO_2 (5) Mask and deposit P ohmic contact metal 8530 on P layer 8508; (6) Mask polyimide bridge for contact to N ohmic ring 8528 by bond pad 8560. 7) Mask and bond pad 859 for both P-ohm and N-ohm respectively. And depositing a 8580, it may consist. Since the bond and bond pad capacitances are parallel and are therefore additive, the bond pad is in contact with the N ohmic ring 8528 at approximately 100 × 100 μm^2 . The RC time constant is determined by the total junction, pad, and fringe capacitance. Deleted from the above process are passivation, annealing, curing, antireflection, thinning, backside metallization, dicing, etc. The NIP / PIN mesa diameter can be in the range of 10-100 μm, and MS-PD / APD has less semiconductor material in the mesa compared to the conventional PD / APD, so it has less capacity, so Can have a larger area mesa (or equivalently a larger photosensitive area) for the same data rate bandwidth compared to other PD / APDs, and therefore optical into MS-PD / APD Signal alignment has a larger error margin, which further reduces the cost of packaging. 86 and 87, in the case of a hole having a period of 2000 nm and a diameter of 1300 nm in a square hole lattice, the capacity is the same as the case of mesa having the same diameter but the thickness of the I layer, and the fringe capacity is ignored. About 30% less than that of an equivalent structure. In the case of a hexagonal lattice hole with a period of 2000 nm and a hole diameter of 1300 nm, the area of the MS-PD may be about 35% larger than that of a PD without holes. Other gratings, periods, and hole diameters, holes for capacity reduction but not for absorption enhancement, to reduce capacity and / or increase absorption in, for example, MS-PD / APD structures or It can also be used to optimize. According to some embodiments, multiple periods and / or multiple hole diameters may be used. It is also possible to use holes that are spaced aperiodically.

FIG. 88 is a schematic plan view showing an MS-PD / APD integrated with a mutual impedance amplifier and / or other electronics on a single chip. On a single silicon chip 8600, an MS-PD / APD 8650 is shown connected to a TIA or other electronics 8690 using interconnect lines 8692. Although FIG. 85 shows a stand-alone MS-PD / APD that requires a bond pad to transmit electrical signals to other electronic components for further signal processing and transmission, FIG. 2 shows MS-PD / APD and electronics integrated on a chip. The bond pad adds unwanted capacitance, and this capacitance, along with the junction capacitance, is used to calculate the MS-PD data rate bandwidth. For example, an RC time with a bandwidth of 20 GHz (or about 30 Gb / s) is about 0.16 pF capacity and 50 Ω load resistance. A 30 μm diameter SiPINPD with a 2 μm I layer has a junction capacitance of 37 femtofarads (fF) with the I layer fully depleted by a reverse bias voltage. This allows a 90 μm × 90 μm bond pad on 2 μm polyimide to give a total capacitance of about 0.2 pF. If the MS-PD / APD is integrated with TIA and / or electronics, the bond pads are no longer used and the transmission line capacity from the MS-PD / APD to the TIA and / or electronics is reduced. Neglecting, the MS-PD / APD capacitance can be 0.16 pF, which is about 30 mm in diameter compared to 30 μm in diameter for a stand-alone device. The device becomes 60 μm. This increase in area increases the margin for optical beam alignment errors relative to MS-PD / APD and further reduces packaging costs. Including parasitic capacitance, the diameter of MS-PD is significantly larger than 30 μm of stand-alone MS-PD, and may be, for example, greater than 40 μm, and in some cases, greater than 50 μm in diameter. May be even larger.

It should be noted that, as described in this patent specification, a microstructured hole array (or column) having a diameter approximately the same (more or less) as the wavelength of light is a microstructured hole array (Or absorption of photons over that of a similar substance that does not have a column). For example, in order for SiPINPD to operate at several tens of Gb / s, the thickness of the I layer must be about 2 μm, otherwise electrons and holes that are photogenerated carriers. In some cases, the run time of the system achieves a data rate bandwidth of tens of Gb / s and exceeds about 20% at a nominal wavelength of 850 nm, in some cases 880 nm, and in some cases 980 nm. Is too long to have sufficient quantum efficiency above 40%. This is made possible with the techniques described herein using microstructured hole arrays (or columns), either with a single period and diameter and / or with multiple periods and diameters. The holes and / or holes (columns and / or columns) can be periodic and / or non-periodic and the microstructure absorbs and / or emits.) Can have a cross-sectional shape other than circular. In the absence of the microstructured hole array (or column), the 2 μm or less thick Si layer absorbs about 5% of 980 nm photons, while the microstructured hole array or column Can be absorbed in excess of 20%, and in some cases it can exceed 30%. Furthermore, in some other cases, it is possible to exceed 40%, 50%, and 60% for 900 nm wavelength photons.

This is the same for Ge on Si, and by using this patent specification, for example, at wavelengths of 1550 nm and in some cases 1600 nm and in some cases 1700-1800 nm. Several tens of Gb / s data rate bandwidth can be achieved.

In known nanowire photodiodes, there is no absorption enhancement such that a thin layer of about 2 μm or less over that of an equivalent bulk layer for high data rate bandwidths of tens of Gb / s. For example, a 2 μm long InP nanowire and a 2 μm bulk InP at wavelengths greater than the band gap are approximately equivalent, and the advantage of InP nanowire is only to reduce reflection.

FIG. 87 shows a simple epitaxial structure without any microstructure. The structure of FIG. 87 is used to compare with similar epitaxial structures with microstructures such as hole arrays for the absorption of incident photons having a wavelength range of 800-880 nm. For simulation purposes using FDTD (finite difference time domain), structures with microstructures without P and N contacts, mesa etching, passivation, planarization, and other processes to produce complete photodiodes Only the structures that do not have are shown. The epitaxial structure in Case 1 is grown on a doped and thinned silicon substrate P8702 to about 150 μm, the first layer of which is about 0.2 μm thick using boron at 1×10^{20} / cm^3 a Si intrinsic layer 8706 that is doped beyond cm^3 , then about 2 μm thick, intentionally undoped and having a doping level of less than 5×10^{16} / cm^3 And then a SiN layer 8710 having a thickness of about 0.3 μm and doping with a phosphorous dopant exceeding 1×10^{19} / cm^3 .

FIG. 88 shows another simple epitaxial structure in which no microstructure is present. The structure of FIG. 88 is used to compare with a similar epitaxial structure having a microstructure such as a hole array with respect to absorption of incident photons in the wavelength range of 800-880 nm. For simulation purposes using FDTD (finite difference time domain), structures with microstructures without P and N contacts, mesa etching, passivation, planarization, and other processes to produce complete photodiodes Only the structures that do not have are shown. The epitaxial structure in Case 2 is grown on a silicon substrate P802 with a 2 μm buried oxide (BOX) layer 8804 on which a doping using boron with a thickness of about 0.1 μm is 1×10^{20} / cm^3 is SiP layer 8806 has been exceeded and then be .....) layer 8816 which P doping is over 1×10^{20} / cm^3 Next, a Si intrinsic layer 8808 with a thickness of about 2 μm, which is not intentionally doped and has a doping level of less than 5×10^{16} / cm^3 , and then with a phosphorous dopant with a thickness of about 0.3 μm and 1. This is a SiN layer 8810 doped in excess of $\times 10^{19}$ / cm^3 . For both Case 1 and Case 2, photons are incident from the top surface, ie the surface with the SiN epitaxial layers (8710 and 8810), for simulation studies.

FIG. 89 shows the same epitaxial structure as in FIG. 87 except that the microstructured hole array has been etched down to the SiP epitaxial layer according to some embodiments. In Case 3, the hole #902 has a diameter of 1500 nm and a period of 2000 nm in a square grid array. Photons having a wavelength of 800-880 nm are incident on the upper surface, ie, the SiN epitaxial layer 8710. The N and P layers / substrates can be exchanged in certain applications and the absorption results are about the same.

FIG. 90 shows an epitaxial structure that is the same as in FIG. 88 except that a microstructured hole array has been etched into the BOXSiO $_2$ layer according to some embodiments. In Case 4, the holes 9022 have a diameter of 1500 nm and a period of 2000 nm in a square grid array. Photons having a wavelength of 800-880 nm are

incident on the top surface, ie, the SiN epitaxial layer 8810. The N and P layers / substrates are interchangeable in certain applications and the absorption results are about the same.

Furthermore, the hole can be etched up to the etch stop layer SiGeB8816. The etch stop layer 8816 is highly P-doped and can be used in a layer structure where a P layer and an etch stop layer are desired in the process, which can be used in photodiode and avalanche photodiode structures. Is included.

91A-91B are plots showing the results of a simulation for the exemplary structure illustrated in FIGS. 87-90. FIG. 91A shows a comparison of cases 1-4 (FIGS. 87-90, respectively), in which case "I" Si in each case for wavelengths shown over 800-900 nm using FDTD simulation. The absorption due to the intrinsic layer is calculated. In each case, the photons are incident on the top surface, the NSi epitaxial surface (layers 8710 and 8810 in FIGS. 87-90). Absorption due to other layers other than the "I" layer is not included. Curves 9110, 9112, 9114, 9116 show the results for cases 1, 2, 3, 4 (shown in FIGS. 87, 88, 89,90), respectively. In cases 1 and 2, no microstructure is present and the absorption in the I layer is less than 40%. That means that 40% of the incident photons have been absorbed, in case 1 it is less than 19% and in case 2 it can be just less than 40%, for example at a certain wavelength of 895 nm and less than 20% at the longer wavelengths 880 nm and 850 nm. And less than 10% at 835 nm. Absorption is directly proportional to quantum efficiency. This is because photons are absorbed and converted to electrons and holes, which are then swept out of the "I" region under a bias voltage that depletes the "I" region. This is because when they are not coupled, these photogenerated electrons and holes swept to the N and P regions, respectively, contribute to the photocurrent. In cases 3 and 4, which contain microstructured holes with a diameter of 1500 nm and a period of 2000 nm in a square grating, an absorption level close to 100% is seen at certain wavelengths. In both cases 3 and 4, the absorption is greater than 40% at wavelengths between 800 and 900 nm. In the 800-850 nm range, it is an absorption greater than about 70%. In case 4, the absorption is better than 70% at 850 to 900 nm. At 855 nm in Case 4, the absorption is over 95%, which is in contrast to Case 2, which is less than 10%. The percentage of absorption in the "I" layer in the case of microstructures increases for high absorption at certain wavelengths, eg by changing the hole diameter, period and / or grating, eg from square to hexagonal grating or it is possible to optimize.

In the case of a silicon PIN photodiode with a microstructure as described herein, it has been found that the absorption does not necessarily decrease when the wavelength approaches 1.11 eV silicon band gap at 300 K, ie, about 1117 nm. In comparison, for a PIN (or NiP) photodiode without a microstructure, the absorption decreases as the wavelength approaches 1117 nm. This increases the Q (quality factor) of the microstructure resonance and / or coupling resonance as the optical loss is reduced, so that more time is spent as the photons bounce back and forth within the microstructure. As a result, it is considered that the absorption may exceed 50% even when the wavelength approaches 1117 nm. The refractive index difference within the microstructure can be expressed as an effective index. For example, since the hole removes silicon material and is replaced, for example, with air, the effective index, or effective refractive index, of the region with the hole is less than the refractive index of the region without the hole. A simple estimate is the average of the refractive indices, but, for example, if the hole removes half of the silicon in the region where it has a hole, assuming that the hole is filled with air, its effective refraction The index is about (1 + 3.44) /2=2.22, where the refractive index of bulk Si is about 3.44 at a wavelength of 1000 nm. Thus, the region with and without holes will see a refractive index discontinuity of approximately 1.22, ie a refractive index change of about 35%. This discontinuity in refractive index may result in a high contrast grating with a Q that can approach 1,000,000 or more when the optical loss is low. This can explain the improved absorption in microstructured photodiodes and / or avalanche photodiodes. If photons stay in the microstructure for a time approaching the characteristic time, which is the transit time and RC time of the photodiode / avalanche photodiode, this will adversely affect the data rate bandwidth of the PD / APD. start. However, if the data rate bandwidth is low, a higher Q can be tolerated. The Q factor is defined as being proportional to the energy lost per stored energy / cycle. This is a probable explanation for improved absorption in the microstructure. The microstructure is composed of a lattice and thus is composed of a number of unit cells or cells, each having its set of resonances and closely coupled. Unlike a conventionally known resonant photodiode, which is a single resonator, its resonance is a sharp peak or valley and shows only a single resonance characteristic which is a periodic wave function. The structure has a region in the absorption for which the absorption varies slowly, for example, for wavelengths that vary by less than 10% over a wavelength range, for example 50-100 nm, and an aperiodic wave function. The microstructure PD / APD has a sum of a plurality of resonances, and thus has peaks and valleys that are not so conspicuous as compared to a conventionally known resonant photodiode. An aperiodic hole can also have a resonant cell that is itself aperiodic and can couple to an adjacent neighbor cell, which improves absorption and / or emissions. The coupling type resonance structure is possible.

As a rough estimate, the characteristic time is about 20 ps for about 20 GHz 3 dB bandwidth. At 20 ps, the light travels about 2000 μm in silicon, which means that the light can bounce about 1000 times in a 2 μm microstructure, so a 2 μm thick "I" layer is at an equivalent optical length. Meaning that it can be as thick as 2000 μm, so in the microstructure described in this patent, the light will bounce more and be improved above the bulk absorption coefficient. It is possible to give an effective absorption which can be written approximately as effective absorption = bulk absorption × number of bounces in the microstructure. The time that light spends in the microstructure is called optical transit time, which is another basic time for the MS-PD / APD. The sum of these three basic times, i.e., RC time, travel time, and optical travel time, squared, gives the square of the total time. For example, T (total time) ^{2} = T (RC time) ^{2} + T (travel time) ^{2} + T (optical travel time) ^{2} In the case of 20 GHz, the total time may be 20 ps and is simple For simplicity, assuming that RC time, travel time, and optical travel time are all the same, each time may be only about 11.5 ps. 11.5 ps for the optical transit time is converted to an equivalent optical length of about 1800 μm, ie the optical transit time is longer than 11.5 ps, assuming that all three basic times are equal in some cases, the improved effective absorption length may be a Q of 1000 μm or approximately 250 before it begins to degrade the bandwidth of the MS-PD.

FIG. 91B shows the epitaxial structure in FIG. 90 (case 4) when the microstructured hole array is etched to different depths. Curve 9120 shows the absorption in the "I" Si layer as a function of wavelength from 800 to 900 nm when holes are etched into the SiO_2 layer 8804. Curve 9122 shows absorption versus wavelength for holes etched into the SiGeB layer 8816. In both cases, light is incident from the top or SiN surface 8810. Although the peaks and valleys are shifted, the overall etching to the SiO_2 layer is better than the etching of holes to the SiGeB layer at most wavelengths in the 800-900 range.

FIG. 92 is a schematic diagram illustrating a microstructured region in silicon when holes are etched into silicon, according to some embodiments. The exemplary structure includes a SiP substrate 9202, a SiP layer 9206, a SI layer 9208, and a SiN layer 9210, all of which have thicknesses and doping levels as shown. Hole 9222 is etched to a depth of about 2.3 μm and has a diameter of 1500 nm and a period of 2000 nm in a square grating. Region bore there shown schematically dotted circle 9280 has an effective refractive index n_{eff1} it is smaller than the refractive index of the bulk Si is about 3.44 in 300K at 1000nm wavelength. This assumes that the etched region is in air, vacuum, or filled with a material such as polyimide having a refractive index lower than that of silicon. For the dimensions described above for the microstructure, the effective refractive index in the region with holes is approximately given by the air portion 0.44 × 1 + Si portion 0.56 × 3.44, which is about 2. 36. For example, photons incident on the upper surface 9210 are trapped in the microstructure and bounce between the two refractive index discontinuities. One discontinuity is the interface between air and microstructure, where the refractive index difference is about 1.36, and the other discontinuity is the interface between microstructure and silicon. The refractive index difference there is about 1.07. This refractive index difference makes it possible to view the microstructure as lossy high contrast grating, which can explain the improved absorption observed.

FIG. 93 is a schematic diagram illustrating an MS-PD structure with tapered holes, according to some embodiments. The tapered funnel-shaped hole 9322 gradually changes in the effective refractive index n_{eff}, which has no significant change in the hole diameter but is smaller than that in region 1, for example, the effective refractive index n_{eff2}. The effective refractive index in region 1 is much smaller than the effective refractive index in region 2 due to the fact that it is much smaller than for the region it has, in which case it is simply less silicon material there. In region 1, the effective refractive index near the surface can be 60% or more voids (air or a low refractive index material such as polyimide) and 40% or less silicon, which The reflection is lower with respect to photons incident perpendicularly to the upper surface (in this case, the SiN layer). For photons incident off the vertical, the reflection may be even lower. As a further example, if the hole occupies 90% or more near the surface and Si occupies 10% or less, the Fresnel reflection for normal incidence photons is 1% or less, it may be. As the diameter of the hole gradually decreases with depth, the

effective refractive index in region 1 gradually changes. Although the illustrated example is a funnel, it can be, for example, simply a step with two separate hole diameters, or a plurality of hole diameters with each step diameter becoming smaller as the step moves away from the surface. It is possible to have a plurality of steps.

FIG. 94 is a schematic diagram illustrating an MS-PD structure with progressively tapered holes, according to some embodiments. Another configuration is illustrated with a hole 9422 having a gradual funnel shape extending over the entire length of the hole. Its effective refractive index also increases gradually as a function of depth. According to some embodiments, the holes can be provided with pseudo-random or random holes having multiple diameters, periods, and / or different funnel shapes. Various hole parameters can be used to improve or optimize the absorption characteristics in certain wavelength bands. According to some embodiments, the holes 9422 can be provided with a series of steps, each step having a different diameter. These steps can be uniformly spaced and / or non-uniformly spaced. Their spacing may be a quarter-wave, half-wave, or fast to improve or optimize the absorption characteristics in a particular band of wavelengths, for example, to form a filter or coupled resonator. It can be a fraction of a half wavelength and a half wavelength. In the case of optical emitters, such a step in the diameter of the hole or column can improve, for example, the overlap of the light wave with the gain medium. According to some embodiments, the funnel shape of the hole 9422 can have any shape. For example, it can be V-shaped and the effective refractive index at the air hole interface and at the hole-silicon interface can be optimized to improve reflection and absorption properties or emission properties.

Another explanation for the absorption enhancement associated with the microstructured PD / APD is that the microstructure is a metamaterial and can act as a broadband absorber. For example, S. Daval et al. "Broadband infrared metamaterial absorber with visible transparency using ITO as ground plane", OPTICS EXPRESS 15104 June 2013, N Liu et al. "Infrared Perfect Absorber and Its Application As Plasmonic Sensor", Nano Lett. (2010), 10, 2342-2348, and L. Meng et al. "Polarization-sensitive perfect absorbers at near-infrared wavelengths", Optics Express, A111 Dec. 2012 (hereinafter " Meng et al."), All of which are incorporated herein by reference.

For example, Meng et al. In the case where the plurality of grooves are intersected by a crossbar pattern, the absorption is polarity independent. Instead of long grooves, as described herein, Meng et al. Au in the substrate is replaced by a semiconductor such as silicon and / or germanium, and the hole / groove is a void, which is an air, gas, vacuum, polyimide, and / or any coating that partially or completely covers the hole a is possible to use a dielectric material. In particular, Meng et al. In FIG. 11, when the structure is a cross bar, a square array of dielectrics exists on the Au substrate. According to some embodiments, Au is filled with a semiconductor and a dielectric material such as air, gas, or silicon dioxide, silicon nitride, calcium fluoride, spin-on-glass, polyimide, or a passivation dielectric. It is replaced with a dielectric that has holes. Meng et al. FIG. 11 also shows absorption with respect to wavelength.

High contrast gratings can be considered a class of metamaterials. This, along with other effects, may be able to explain the observed absorption enhancement. Other effects include plasmons, nonlinearities, sub-wavelength and near-wavelength effects, photonic crystals, slow waves, coupled resonances, interference, field enhancement, and resonances with losses.

FIG. 95 is a schematic diagram illustrating a material structure with microstructured holes of different diameters, according to some embodiments. Holes 9522 and 9524 have different diameters. Smaller diameter holes remove less silicon material than larger diameter holes if the period is approximately the same. The effective index of the array of smaller diameter holes 9522 is the effective index n_1 and these holes can be clustered near the center of the MS-PD / APD. An array of larger diameter holes 9524 has an effective refractive index n_2 and can be clustered around the smaller diameter holes (eg, in a ring-shaped pattern). For example, n_1 is greater than n_2 because less material is removed in the smaller diameter hole 9522 than in the larger diameter hole 9524. The light is guided into the n_1 region, so when light bounces back and forth between the hole / silicon (in this example P-silicon) interface and the hole / air interface, for example due to diffraction. The amount of light lost is minimal. Further, the mesa etch removes most if not all of the N silicon layer and the "i" silicon layer in region 9530. Mesa 9540 is etched to define the capacity of the NIP junction as shown in this example. In some cases, ion implantation and / or diffusion can be used to define the NIP junction capacitance. And in some cases it is only necessary to remove only the NSi layer and / or convert it to low or opposite doping. The N and P can be exchanged. (c) example, MS-PD can be PIN and MS-APD can be NINIP or PININ.

FIG. 96 shows a plan view of a material structure with microstructured holes of different diameters as illustrated in FIG. As can be seen, the smaller diameter holes 9522 are clustered within the larger diameter hole 9524. The resulting effective refractive index difference between the regions near the center of this microstructured photodiode / avalanche photodiode (MS-PD / APD) 9600 is more guided to the region where the light has a higher effective refractive index. The same light guiding effect as an optical fiber is generated. Also shown is a mesa 9540 defined by the etched away region 9530, which can further provide a light guiding effect. The mesa 9540 may also define a NIP junction capacitance and simply be etched completely through to N layer, "I" layer, or up to the P layer. Those not shown are ohmic contact metals, bond metals, passivation, planarization, polyimide, and other dielectrics. The numerical aperture of the MS-PD / APD adjusts the diameter of the holes in the core area (smaller diameter holes) compared to the cladding (larger diameter holes) according to some embodiments. It is possible to adjust by. To change the effective refractive index, the hole density and diameter are methods for adjusting the amount of silicon material in a region.

According to some embodiments, a guide structure having a higher refractive index core and lower refractive index cladding may be used to reduce or minimize optical loss due to diffraction, for example. It is possible to operate effectively as a light guide such as an optical waveguide. For example, a square hole grating with a period of 2300 nm and a hole diameter of 1500 nm can have an approximate effective refractive index of 2.63, and a square grating with a period of 2000 nm and a hole diameter of 1500 nm is approximate. The effective refractive index can be 2.36. A higher refractive index can be on the core side and a lower refractive index on the cladding side. A refractive index difference of about 10% between the core and the cladding can be achieved by changing the period of the square grating. Other combinations are possible. The cladding can have a hexagonal grid and the core can have a square grid, in which case the period and diameter can remain the same or can vary.

97A and 97B are graphs showing absorption with respect to light incident on a microstructure having a layer structure as shown in FIG. 82A. Holes are etched in the hexagonal and square grid arrays with a diameter of 1500 nm and a period of 2000 and 2500 nm, respectively. Curve 9712 is for a square grid with the same period and hole diameter. Its absorption is over 80% at wavelengths of 1.4 to 1.6 μm and over 90% for a hexagonal lattice at 1.55 μm. Curve 9714 is absorption without a microstructured hole, giving 10% or less absorption and only 1.5% absorption at 1.55 μm. Furthermore, for a hexagonal lattice, the absorption varies by less than 10% over the wavelength range of 1450 nm to 1600 nm. FIG. 97A also shows data and communication bands; S, C, L, U / XL. In the case of the structure as in FIG. 82A, MS-PD / APD can be used in all these bands from S to U / XL.

In FIG. 97B, curve 9720 shows the absorption for a wavelength of a hexagonal hole grating with a period of 2500 nm and a hole diameter of 1500 nm, and curve 9722 is for a square grating with the same period and diameter. It is less optimal, but at 1.55 μm wavelength, its absorption exceeds 90%. Curve 9714 is also shown for reference.

Absorption and quantum efficiency are directly proportional, and about 90% absorption with minimal reflection may be equivalent to about 90% quantum efficiency. For example, the external quantum efficiency can be defined as $QE = (1-R)(1-e^{-\alpha x})$, where R is the reflection from the surface of the MS-PD / APD, and α is the absorption coefficient. X is the absorption length. Absorption can be given by $(1-e^{-\alpha x})$, which is the amount of photons absorbed at the absorption coefficient α and length x. The 90% absorption at 1.55 μm wavelength is converted to the product of the absorption coefficient and the absorption length, and αx is equal to about 2.3. If a bulk absorption coefficient is used, x is about 50 μm since it is 460 / cm at 1.55 μm wavelength. Compared with the physical length of 2.2 μm of Ge, the light has passed through the absorption region about 23 times. Equivalently, if the physical absorption length is 2.2 μm, the improved effective absorption coefficient is about 10455 / cm at 1.55 μm wavelength, while the bulk absorption coefficient at 1.55 μm wavelength is about Compare with 460 / cm. This also indicates that the improvement is about 23 times.

The absorption enhancement can be caused by any or a combination of the following: field enhancement, interference, plasmon, metamaterial absorber, high contrast grating, wavelength and subwavelength feature dimensions, nonlinear effects, resonance High contrast grating with effect, loss, slow wave, coupled wave, coupled resonance, coupled mode, and photonic crystal (eg Krauss, J. "Slow light in photonic crystal waveguides) ", Phys. D: Appls. Phys. 40 2666-2670 (2007), which is incorporated herein by reference).

Furthermore, the quantum efficiency directly proportional to absorption is high over the range of data / telecommunications wavelengths. Standard bands are S (1460-1530 nm), C (1530-1565 nm), L (1565-1625 nm), and U / XL (1625-1675 nm). Other bands not shown can also have high absorption efficiency, such as O (1260-1360 nm) and E (1360-1460 nm). A single microstructured Ge-on-SiPD / APD can cover the entire data / telecommunications wavelength spectrum. For example, see Bosca, "From C to L: The Future of Optical Wavelength Bands", www.bi-dashandproperties.com, BROADBAND PROPERTIES, June 2008. Well, that is incorporated into this book by citation.

FIG. 98 is a graph showing simulated absorption for the structure shown in FIG. 82A and simulated in FIGS. 97A and 97B. Curves 9810 and 9812 show the absorption for hexagonal and square grids, respectively. In each case, the hole period was 2000 nm and the diameter was 1500 nm. It can be seen that the structure absorbs well in the 850 nm wavelength range and better than 80% between 830 and 1000 nm. One advantage is that wavelength coverage can range from 800 to 1700 nm and beyond with better absorption and / or quantum efficiency of 70% with a single device. Such a Ge-on-SiMS-PD / APD can be integrated with electronics, so a single chip with MS-PD / APD and a transimpedance amplifier or other integrated circuit electronics for signal processing. Which significantly reduces assembly and packaging costs.

FIG. 99 illustrates another preferred epitaxial structure for a Si avalanche photodiode for operation in the wavelength range of 800 to 1000 nm, based on some embodiments. In particular, the structure shown has been found to work very well around 850 nm ± 30 nm and for data rates of 5-40 Gb / s or higher where much of the data communication takes place. A microstructure is used to improve absorption, which can be either an improved absorption coefficient and / or an improved absorption length. The NSI substrate 9902 can be thinned to 150 µm after device processing. As an epitaxial layer, for example, an N contact with a thickness in the range of 0.1-4 µm and in some cases in the range of 0.3-2 µm and a doping exceeding 1×10^{19} / cm^3 NSI layer 9906, which is a layer, and also known as an avalanche layer with a thickness ranging from 0.2 to 1 µm, in some cases 0.5 µm and a background doping of less than 1×10^{16} / cm^{-3} A SI intrinsic or "I" layer 9916, which is a gain or gain layer, and a thickness of 0.02 to 0.3 µm, in some cases 0.1 µm and a doping of $1-6 \times 10^{17}$ PSI layer 9920, which is a charge layer that is in the range of / cm^3 and in some cases 1.8×10^{17} / cm^3, and in some cases in the thickness range of 0.3 to 4 µm is 2 a SI intrinsic "I" layer 9908, an absorption layer with a background doping of less than 1×10^{16} / cm^3, and a thickness of 0.1 to 2 µm and in some cases 0.3 µm And a PSI layer 9910 which is larger than 1×10^{20} / cm^3 and is a P contact layer.

FIG. 100 is a schematic diagram illustrating some features of a microstructured APD based on some embodiments. The MS-APD uses the material structure shown in FIG. Microstructured hole array 10022 is etched either partially or completely into PSI contact layer 9920 and into "I" SI absorber layer 9918. Light is incident from the top surface or PSI layer 9910 perpendicular to the surface and / or off-normal to the surface. Mesa etching is performed down to N contact layer 9906 to define the capacity of the device. A P ohmic contact 10022 and an N ohmic contact 10030 are formed on the PSI contact layer 9910 and the NSI contact layer 9906, respectively. A reverse bias of 10-60 volts is applied to the P and N ohmic contacts. A negative voltage is applied to the P contact (anode) relative to the N contact (cathode). Not shown for simplicity are elements such as a passivation layer, a planarization layer, a bridging layer, a bond metallization layer, and a guard ring. The coupling between the micro-structured photodiode with improved absorption and the SI avalanche or gain layer is such that - it is possible to operate in the wavelength range of 1000 nm, especially at 850 nm ± 30 nm. In other cases, the data rate can be 15-40 Gb / s with multiplication factors of 2, 4, 6, 8, 10 or more. One advantage of Si microstructured APDs is low excess noise, which is even lower than, for example, GaAs and / or InP based APDs.

FIG. 101 shows another suitable epitaxial structure for a Ge on Si avalanche photodiode for operation in the wavelength range of 800-1700 nm, based on some embodiments. In particular, the structure shown has been found to work well for data rates of 5-40 Gb / s or higher around 1550 ± 200 nm where much of the telecommunications occurs. This microstructure can be used to improve absorption, which can be either an improved absorption coefficient and / or an improved absorption length. The NSI substrate 10102 can be thinned to 150 µm after device processing. The epitaxial layer has a thickness in the range of 0.1-4 µm, in some cases 0.3-2 µm and an NSI layer 10106 that is an N contact layer with a doping greater than 1×10^{19} / cm^3. A multiplication factor also known as an avalanche layer with a thickness in the range of 0.2 to 1 µm, in some cases 0.5 µm and a background doping of less than 1×10^{16} / cm^3 SI intrinsic or "I" layer 10118 as a gain layer and a thickness in the range of 0.02 to 0.3 µm, in some cases 0.1 µm and a doping of $1-6 \times 10^{17}$ / a PSI layer 10120 which is a charge layer of cm^3 in some cases 1.8×10^{17} / cm^3 and a thickness in the range of 0.3 to 4 µm and in some cases 2 µm and Backg The Ge intrinsic "I" layer 10108 Wocked doping is an absorbent layer is less than 1×10^{16} 15 / cm^3, a 0.2µm when thickness of several in the range of 0.1 to 2µm and A PGe layer 10110 which is a P contact layer with a doping greater than 1×10^{20} / cm^3. Often it is possible to grow a low temperature Ge buffer layer at the interface between Si and Ge, prior to normal Ge epitaxial growth. In this regard, see, for example, Kang et al. Good to see.

FIG. 102 is a schematic diagram illustrating some features of a microstructured Ge-on-SiAPD based on some embodiments. The MS-APD uses the material structure shown in FIG. The microstructured hole array 10202 is etched in the PGe contact layer 10110 and partially or completely into the "I" Ge absorber layer 10108 with dimensions, diameters and hexagonal grids as in FIG. 97A. Light is incident either from the top surface or PSI layer either perpendicular to the surface and / or offset from the surface. A mesa etch on the N contact layer 10106 defines the capacitance of the device, and a P ohmic contact 10028 and an N ohmic contact 10030 are formed on the PGe contact layer and the NSI contact layer, respectively. A reverse bias of 10-60 volts is applied to the P and N ohmic contacts. What is not shown for simplicity is a passivation layer, a planarization layer, a bridging layer, a bond metallization layer, a guard ring, and the like. The coupling between the microstructured Ge photodiode with improved absorption and the SI avalanche or gain layer is such that the micro-structured Ge-on-SiAPD is greater than 2 and in some cases greater than 4 and some more is greater than 5 Gb / s with a multiplication factor greater than 8-10, and in some cases greater than 10 Gb / s and in some cases 850- at a data rate greater than 15-40 Gb / s. It makes it possible to operate at 1700 nm, especially in the wavelength range of 1550 nm ± 200 nm. One advantage of Ge-on-Si microstructured APDs is lower excess noise, which is even lower than, for example, GaAs and / or InP based APDs.

103 (A)-(C) show the diameter, period, and other parameters for microstructured silicon and germanium-on-Si photodiodes and avalanche photodiodes based on some examples. FIG. 103 (A) is a table showing various parameters used. According to some embodiments, both hexagonal and square grids can be used. Other lattice and / or non-lattice arrangements of holes are possible, but are not shown. Mesa dimensions of 10, 25, 30, 40, 50, 60, and 80 µm are used to achieve capacity to support data rates of 5 to over 80 Gb / s. According to some embodiments, other methods of defining junction capacitance, such as ion implantation or diffusion, can be used to deplete carriers. The hole diameter and period for the operation of Si microstructured PDs and APDs in the wavelength range of 800-1000 nm, especially in the range of 850 nm ± 30 nm, for example 1300/2000, 1500 for either hexagonal and / or square gratings - / 2000, 700/1000, 630/900 (diameter / period in nm). In the case of Ge-on-Si microstructured PDs and APDs, examples of hole diameter and period combinations for either hexagonal or square gratings for operation in the wavelength range of 800-1750 nm, especially 1550 nm ± 200 nm. Includes 1300 nm / 2000 nm, 1500 nm / 2000 nm, 1500 nm / 2500 nm, 1300 nm / 2300 nm. Other hole diameters and periods are possible. Absorption better than 90% and in some cases better than 70% or 80% can be achieved with these diameters and periods at wavelengths of 800-1000 nm and 800-1700 nm, is there. 103 (B) and 103 (C), "d" is shown as a period for hexagonal and square lattice patterns. Although circular holes are illustrated, non-circular holes such as ellipses, rectangles, polygons, and / or other irregular shapes are possible. Circular holes are only selected for simplicity of simulation using FDTD.

104 (A) and 104 (B) show the FDTD (finite difference time domain) for the absorption with respect to the wavelength for the structure shown in FIG. It is a graph which shows the used simulation result. It should be noted that this simulation result can also be applied to the microstructure GePGIISSISISINAPD. The simulation uses a

hexagonal lattice, 1500 nm hole diameter, 2000 nm hole period, in which case the holes are etched into the SiN layer. In this simulation, the wavelength is centered on 1500 nm ± 10 nm (curve 10410 in FIG. 104A) and 1550 nm ± 1 nm (curve 10412 in FIG. 104B). The simulation mesh is finer than 0.1 nm, and from the curve 10412 in FIG. 104 (B), the absorption is higher than 0.9 (90% absorption) and 0.85 (absorption) over the wavelength 1549 to 1551 nm. It can be seen that the variation is less than 10% with a low absorption value exceeding 85% absorption. This property of absorption with respect to wavelength is important in optical telecommunications applications, in which case there is no rapid change in absorption within 2 nm of wavelength variations centered around 1550 nm, for example. A curve 10410 in FIG. 104A shows an absorption fluctuation of 0.8 to 0.99 exceeding a wavelength fluctuation of 20 nm centered on 1550 nm. Over any 2 nm wavelength variation, the absorption variation is less than 15%. In some cases it is less than 5%. The channel spacing in wavelength division multiplexing (WDM) for coarse WDM can be 2 nm or greater, while for dense WDM, the channel spacing is 0.8, 0.4 or less. Thus, for example, at 1550 nm, 3 or more channels can fit within the 2 nm spectral width, while for coarse WDM, 4 nm or more is required. Is done.

FIGS. 105A and 105B relate to eigenmodes for a square grid hole pattern, based on some embodiments. FIG. 105A shows a single unit cell 10510 in a square lattice arrangement. FIG. 105 (B) shows various 2D eigenmodes (stationary mode, standing wave mode, resonance mode) (from FDTD simulation using Maxwell equations) in a unit cell of a microstructured hole in Si (or Ge) material. Yes. The waves propagate, for example, between the air / semiconductor interface and the Ge / Si interface along the length of the microstructured hole array. A waveguide and / or resonator is defined by the region where the microstructured hole is etched. Semiconductor and hole lengths in the unit cell can be thought of as optical waveguides and / or resonators, and many parallel optical waveguides / resonators of adjacent unit cells can be combined to form 2D It can be a coupled wave in the array, a coupled mode, and / or a coupled resonator. High contrast grating (HCG), photonic crystal, slow wave effect and coupled waveguide / resonator eigenmode, supermode, field enhancement, linear and nonlinear effects, transverse mode, guided resonant modes The combination of the Bloch mode, and the combined Bloch mode can produce an observed improvement in the "αx" product in the equation for quantum efficiency proportional to absorption ($1 - e^{-\alpha x}$). Where α is the bulk material absorption coefficient and x is the absorption length. If x is constant, it is possible to improve α, if α is constant, it is possible to improve x, and in some cases between α and x it is possible to improve both. FIG. 105 (B) shows many complex eigenmodes of the unit cell 10510 of the square lattice in FIG. 105 (A). Each cell in the square grid can have any one or more of these eigenmodes and can be combined with the eigenmodes of adjacent cells, with a large amount of all these cells The combined mode is called super mode. This large amount of coupling may result in a "smoother" absorption characteristic for the wavelength, even smoother in a certain wavelength range, eg 50 nm in some cases and 80 nm in some cases and 100 nm in some cases. Or, more than that, it can be defined as the variation in absorption properties over 10%.

FIG. 106 is a schematic diagram illustrating a microstructured hole in two square grids arranged in an overlapping manner according to some embodiments. A dotted square 10610 represents a unit cell of a square lattice having D1 as a hole diameter. Dashed square 10612 represents another square lattice with a similar period but D2 as the hole diameter, and D1 and D2 are not equal. If D1 is equal to D2, it is a square grid (tilted by 45 degrees). Or, equivalently, if the period of these two square gratings is similar, it can also be considered as a hexagonal grating with two different hole diameters. The grid pattern can have more than two different hole diameters, for example, three different hole diameters in a hexagonal grid. For example, in one preferred microstructure consisting of a plurality of holes, D1 can be 1300 nm in diameter and the square grating can have a period of 2000 nm. One advantage of having more than one hole diameter in a microstructure array is that the absorption curve with respect to wavelength is further flattened so that the variation in absorption is the wavelength for microstructured PD / APD configured in Si. Can be less than 20% for a wavelength of 1250-1750 nm for a microstructured PD / APD that spans 800-990 nm and is configured in Ge on-Si as in FIG. It is. In some cases, the variation is less than 10% variation over these wavelength ranges, and in some cases less than 5%. It is also possible to improve the quantum efficiency of the microstructure PD / APD as a whole or equivalently.

Interspersing different hole diameters results in a quantum efficiency directly proportional to absorption at a wider range of wavelengths, particularly 800-990 nm for microstructured PD / APD in silicon and microstructured PD in Ge-on-Si / Allows further flattening over 1000-1800 nm for APD. Other hole diameters and periods are possible according to some embodiments.

Some embodiments improve the quantum efficiency of PD / APD when the bulk absorption coefficient is insufficient to maintain adequate quantum efficiency within design parameters such as the thickness of the absorbing material, for example. Improvements in the absorption of microstructured holes and / or pillars used to make it possible to apply to other devices that use photon absorption such as solar cells, imaging sensors, radiation absorbers, etc. is there.

FIG. 107 is a schematic diagram showing an epitaxial structure of Ge • on • Si according to some embodiments. The structure is similar to that illustrated in FIG. 82A, but is grown on a 0.2 μm (or 0.1-2 μm range) SiN layer 10706 with N doping exceeding 1×10^{19} / cm^3. A Si1 layer 10718 with a background doping (which can be either N or P) of $1-5 \times 10^{18}$ / cm^3 and a thickness of 0.1-0.5 μm is added, and then intentionally is undoped, has a background doping of less than 5×10^{18} / cm^3, in some cases less than 5×10^{15} / cm^3 and a thickness in the range of 2 μm or 0.5-2.5 μm Followed by a Ge1 layer 10708. The PGe layer 10710 is at the top, the doping is over 1×10^{19} / cm^3 and the thickness is in the range of 0.2 μm or 0.2-0.5 μm. All of these layers are grown on the NSi substrate 10702. The microstructured hole array 10722 can be formed using the parameters shown in FIGS. 103 (A)-(C). According to some embodiments, the hole diameter is 1300-1500 nm and the period is 2000 nm in a hexagonal or square grating. According to another embodiment, a layout as shown in FIG. 106 is used. In such a case, the holes having a plurality of diameters can be, for example, 1300 nm and 1500 nm square lattices with a period of 2000 nm that are nested in each other as shown in FIG.

The Si1 layer 10718 is used to lower the dopant in the Si so that dopant diffusion into the Ge1 layer 10708 is reduced or minimized to allow the Ge1 layer to grow.

According to some embodiments, the structure shown in FIG. 107 is for a micro structure type PD, and as shown in FIG. 101, it can be used for a micro structure type APD with a multiplication layer and a charge layer added. It is. The wavelength range for this structure is 800-1700 nm, and can be in particular about 1550 nm ± 200 nm.

The added Si "i" layer 10718 also contributes to reducing the capacity of the device. This is because the "i" layer is now the sum of the Ge1 layer and the Si1 layer. The decrease in capacity helps to increase the modulation bandwidth of PD / APD. The Si "i" layer may in some cases have a thickness in the range of, for example, 0.1 to 3 μm. Hole 10722 can be etched, for example, to the Si "i" layer and / or in some cases can be etched into the Si "i" layer.

FIG. 108 is a schematic diagram showing the basic features of a Ge on-Si microstructured photodiode based on some embodiments. The structure is similar or identical to that shown in FIG. The MS-PD has been found to work well in the 1300-1700 nm and 800-1300 nm wavelength ranges. As shown, light is incident from the top surface where the hole array is etched. With some minor changes, if an opening is made in the N ohmic contact 10832 on the bottom and the bottom of the Si substrate 10702 is polished with an anti-reflective coating, light can also be incident from the bottom of the substrate. Further, vias (not shown) can be formed on the bottom of the Si substrate 10702 so that a guide can be provided to align the optical fiber with the microstructured PD. In this example, hole 10722 is etched down to Si1 layer 10718 According to some embodiments, the holes can be etched into or through the Si1 layer, or not penetrated through to the Si1 layer. The hole array can have a plurality of hole dimensions and a plurality of periods, and can be non-periodic. The hole diameter can be in the range of 500-1700 nm and the period can be in the range of 1000-2500 nm. According to some embodiments, the hole diameter is 1300 and 1500 nm and the period in a square or hexagonal lattice is 2000 nm. Further, the 1300 and 1500 nm holes can be in a square grid with a period of 3000 nm nested within each other as shown in FIG. The hole diameter and period may vary by 10-50 nm and in some cases by 50-100 nm. Not shown is a passivation layer, which may have a thickness of 2-100 nm on the semiconductor wall. Passivation can be used in the high field region of the exposed mesa to reduce leakage current. A reverse bias of −2 to −12 volts is applied between P contact 10828 and N contact 10830 (and / or 10832). Reverse bias means that a negative voltage is applied to P (anode) relative to the N (cathode) contact. A voltage shown with or without a negative sign means that it is negative at the anode relative to the cathode. Furthermore, the plurality of holes can have different shapes, and not all have to be circular.

it is known to use nanowires in photodetectors. The nanowire is InP and the photodetector is shown to be limited to approximately 30 GHz 3 dB modulation bandwidth in the frequency domain for Gaussian transformation, or 14 ps response time. VJ Logeeswaran et al. "A 14 ps full width at half maximum high-speed photoconductor fabricated with intersecting InP nanowires on an amorphous surface", Applied Physics, A91, 1-5 (2008) (hereinafter" Logeswaran et al. "), which is incorporated herein by reference. Logeswaran et al., The incident photon was at 780 nm and the InP absorption coefficient at about 780 nm was about 38000 cm^{-1}, and neither improvement in absorption nor absorption length was required. Similarly, in another known technique, 850 nm photons are incident on the nanowire and the absorption coefficient of GaAs at about 850 nm is about >2000 cm^{-1}, again requiring improved absorption and / or length it wasn't. MA Seyedi et al. "Efficient Schottky-like junction GaAs nanowire features with 9 GHz modulation bandwidth with large active area", Applied Reference may be made to Physics Letters (APPLIED PHYSICS LETTERS), 105, 041105 (2014), which is incorporated herein by reference. In contrast, according to the techniques described herein, high speed photodiodes / avalanche photodiodes are described with ps response times and / or modulation bandwidths of 5 Gb / s or higher. For Si at 850 nm, the absorption efficiency is about 700 cm^{-1} and a quantum efficiency of 40% or better is achieved using improved absorption and / or absorption length. Similarly, at about 1550 nm for Ge, its absorption efficiency is about 450 cm^{-1}, which also uses enhanced absorption and / or absorption length.

For example, in the case of a 2 μm thick absorbing "I" layer for typical high speed or high modulation bandwidth PD / APD for operation at about 10-30 Gb / s (the "I" layer is the PD / APD About 13% of the photons at 850 nm are absorbed without improvement. For example, if the microstructured hole array (or column) described in this patent application has an absorption enhancement and / or absorption length that is about 12 times or more, then more than 80% of the photons can be 2 μm Can be absorbed at a physical "I" absorption length. Adding microstructured holes and / or pillars when using weakly absorbing (about 1000 cm^{-1} or less) materials such as Si and Ge at data communication wavelengths and telecommunications wavelengths of 850 and 1550 nm, respectively, Absorption or absorption coefficient and / or absorption length, the material is strongly absorbing (approximately 2000 cm^{-1} or more) and the microstructured PD / APD is high speed or high modulation bandwidth data and telecommunications applications and systems It has been proved here that it is possible to improve to the point that it can be used for.

In some cases, only about 40% absorption is sufficient for some optical data / telecommunications, and only about a threefold increase in absorption and / or absorption length, eg, at 850 nm is needed only for a 2 μm Si "I" layer, or an enhancement factor of 4.5 times the absorption coefficient or length for Ge at 1550 nm wavelength for a 2 μm Ge "I" layer. Not too much. Higher enhancement factors are possible, with factors greater than 10 and in some cases greater than 20 and in some cases greater than 40. As the absorption coefficient of the semiconductor bulk material becomes smaller, the improvement coefficient becomes larger, 100 or more.

Absorption of Si nanowires is described in Lu Hu, Gang Chen, Nano Lett. "Analysis of Optical Absorption in Silicon Nanowire Arrays for Photovoltaic Applications", Vol. 7, no. 11, 2007 (hereinafter referred to as "Hu et al."), Which is incorporated herein by reference. Absorption at 1.46 eV corresponding to 850 nm is not improved compared to thin Si films, and for wavelengths above about 2.25 eV, ie about 550 nm or shorter, absorption is comparable to thin Si films. Improved. Hu et al. Added, "On the other hand, in the low frequency range, the extinction coefficient of silicon is so small that improvement cannot be achieved".

Similar conclusions have been reached in other publications, namely Chenxi Lin, Michelle L. Povinelli, "Optical absorption enhancement in silicon nanowire", arrays with a large lattice constant for photovoltaic applications), Vol. 17, No. 22 / OPTICS EXPRESS, 19371, October 26, 2009 (hereinafter referred to as "Lin et al."). Which is also incorporated herein by reference. Lin et al. Shows an improvement in absorption resonance at about 1.5 eV, which is described in Lin et al. Is based on a guide resonance mode or a slow Bloch mode that increases the electromagnetic field strength in the nanostructure. Lin et al. States "Coupling of incident light from the air into the high Q leakage mode of 2D periodic structures". High Q mode sharp resonances are undesirable in the use of photodiodes for data and / or telecommunications applications. For example, JD Schaub et al. "Resonant-Cavity-Enhanced High-Speed Si Photodiode Grown by Epitaxial Lateral Overgrowth", IEEE Photonics Technology Letters, Vol. 11, No. 12, December 1999 (hereinafter referred to as" JD Schaub et al. "). The literature is incorporated into this book by citation. Schaub et al. Shows a quantum efficiency of at most 40% at a wavelength of about 800 nm (see, for example, FIG. 3 in Schaub et al.). However, its sharp resonance is not desirable. This is because drift in transmitter wavelength due to temperature (eg 0.3 nm / degree for some diode lasers and laser internal temperature due to Joule heating and environment is (which may change as much as 80 ° C. or more) may cause significant changes in quantum efficiency, for example. Previously known resonant photodiodes with sharp resonances may also be temperature sensitive in terms of peak resonant wavelengths where quantum efficiency is highest. Furthermore, laser sources often have variations in laser wavelength due to manufacturing variations, and it is not desirable that the laser must be precisely matched in wavelength to the photodiode. Variations in the manufacture of resonant photodiodes can result in resonant peaks at varying wavelengths. This reduces yield and increases the cost of the optical system as it is necessary to maintain careful testing and temperature stability due to the need to match the wavelength of the laser source and detector. It will be

Recent publications Rui Ren, Yong-Xin Guo, Ri-Hong Zhu "Enhanced absorption in elliptical silicon nanowire arrays for solar energy harvesting" Optical Engineering Engineering) 53 (2), 027102 (February 2014) Show Similar results that the improvement at 1.5 eV is weak or non-existent but the absorption at higher energy is much stronger. This document is incorporated by reference

Donnelly et al., "Mode-based analysis of silicon nanohole arrays for photovoltaic applications", Vol. 22, no. S5, OPTICS EXPRESS, A1343, August 25, 2014 (hereinafter referred to as "Donnell et al."), Nanoholes were analyzed for photovoltaic applications, and this document is incorporated herein by reference. Into. Since the solar spectrum is very wide (hundreds of nanometers), sharp resonances are not a problem in photovoltaic applications, while in optical data / telecommunications, the laser spectrum is very narrow, eg, distributed feedback. Types of lasers, such as shaped lasers, Fabry-Perot lasers, vertical cavity surface emitting lasers (VCSELs), and whether they are single mode or multimode and CW with external or direct modulation Depending on whether or not it is operated, the range is considerably smaller than 1 nm to several nm, that is, narrower than 0.01 to 3 nm. Donnelly et al. Also shows a sharp resonance in the 850 nm wavelength region with variation in absorption of at most 75% or more over a 20 nm wavelength span at 800 nm in FIG. Donnelly et al. FIG. 5 shows an optimal period of 500 nm at various nanohole depths and also shows a sharp resonance at, for example, 850 nm wavelength, where the absorption is about 100 over a 10 nm wavelength span. % To 20% change, i.e. about 80% change in absorption. In addition to the resonance guided mode, the document also includes a fundamental mode and a channeling mode capable of generating enhanced absorption.

Ripple in absorption directly proportional to quantum efficiency is about 30% -40%, and in some cases less than 20% or less than 10% is acceptable for data communication and telecommunications applications it is. In some cases, for a center wavelength of about 850 nm, eg, ± 5, 10, 20, 50, or 100 nm, it is desirable that the quantum efficiency ripple be 5% or less.

Experimentally, light trapping and improved absorption are shown by Erik Garnett, Peidong Yang "Light Trapping in Silicon Nanowire Solar Cells", Nanolett., 2010, 10, 1082 - 1087 (hereinafter referred to as "Garnett et al."), Which is incorporated herein by reference. Garnett et al. FIG. 4 shows less than 10% light transmission at wavelengths up to 1100 nm and about 5% light transmission at 850 nm wavelength, and if the reflection can be ignored, the absorption is from the equation T + R + A It is assumed that it is about 90-95%, where T is transmissive, R is reflective, A is absorption, and all light is collected.

Katherine T. Fountaine, Christian G. Kendall, Harry A. Atwater, another recent publication, which is incorporated herein by reference. Near-one broadband absorption design for semiconductor nanowire arrays via localized radial mode excitation ("Near-unity broadband absorption design for semiconducting nanowire arrays via localized radial mode excitation", Vol. 22, no. On OPTICS EXPRESS A930, May 5, 2014 (hereinafter referred to as "Fotaine et al."), The simulation results of GaAs nanowires on 3 μm high Si with different diameters are 5 It shows that it is possible to achieve absorption close to 1 with a filling factor of%. Fountine et al. Please refer to FIG. The purpose of the simulation is to reduce the use of materials to achieve a high efficiency photovoltaic device, and a 5% filling rate with 3 μm GaAs nanowires is equivalent to 150 nm of a flat GaAs layer for the amount of material. Is there. However, a good comparison of absorption enhancement is to compare 3 μm GaAs

nanowires with a 3 μm thick GaAs flat layer. In this case, the planar GaAs 3 μm layer has an absorption of 1 until reaching the band gap end of 1.42 eV or 873 nm, and it drops sharply, and at 886 nm the absorption coefficient is about 241 / cm, in which case it is weakly absorbed compared to, for example, about 5917 / cm at 855 nm, which is strongly absorbing, and about 7% of the 3 μm thick layer is absorbed at 886 nm and about 855 nm 85% absorption and about 95% absorption at 827 nm. A 3 μm GaAs layer was formed by Fountain et al. Compared to FIG. 4, no improvement in absorption is observed. Without perceptible absorption enhancement, there is no advantage to using nanowire photodiodes beyond that of bulk layer photodiodes. In this case, a bulk 3 μm GaAs photodiode will perform almost as well, even if not better than a 3 μm GaAs nanowire photodiode for data / telecommunications at 800-850 nm.

According to the technique described in this document, for example, a 2 μm microstructured hole in Si (possible to be a column and / or a column and a hole), for example, data / remote communication with a high data rate of 5 Gb / s or higher. Improvements in absorption (modulus and / or length) are provided to be significantly more absorptive than 2 μm Si bulk layer photodiodes at 800-900 nm wavelengths.

109 (A) and (B) are graphs showing the results of FDTD simulations using Maxwell's equations for a microstructured hole array, based on some examples. The hole array has a hexagonal lattice with a 2000 nm period and has an epitaxial structure similar to FIG. 92 of 2 μm "i" thickness SiNiP and the holes etched through the i layer. And has two hole diameters (as shown in FIG. 106). FIG. 109 (A) shows absorption versus wavelength for four cases including curve 10910 using 1670 and 1500 nm hole diameters, while FIG. 109 (B) uses 1670 and 1500 nm hole diameters. The absorption versus wavelength on an exaggerated scale is shown for two of the four cases involving curve 10910. The simulation shows less than 10% ripple over a wavelength of 840 to 860 nm with an average absorption of about 90%. Furthermore, the region between 835-875 nm wavelengths can have an absorption of 80% or more of incident photons. Adding more than one hole diameter and / or period reduces the ripple in the absorption curve for that wavelength. Coupling of eigenmodes of different structures with different resonant modes, different hole diameters and / or periods reduces ripple and improves absorption over a wider wavelength range and is approximately 2 μm thick. This contributes to achieving a high absorption efficiency that is directly proportional to a quantum efficiency greater than 80% at 850 nm. In some cases, it is possible to achieve greater than 90% at 850 nm ± 10 nm. In some cases, it is possible to achieve quantum efficiency greater than 70%, 60%, 50% or 40% at 850 nm ± 10 nm.

Other hole diameters are also shown, e.g. 1330 and 1500 nm, 1500 and 1500 nm, 1670 and 1670 nm all have a period of 2000 nm and ripple is better in certain wavelength ranges than others, so for example When designing a microstructure PD / APD for a certain wavelength range such as 850 nm ± 10 nm, the 1500 nm hole size in a hexagonal lattice with a period of 2000 nm is less than 10% ripple in a 2 μm Si "i" layer. It is possible to achieve an absorption greater than 80%. In addition, holes of 1330 nm and 1500 nm and, as mentioned above, holes of 1500 and 1670 nm diameter in a hexagonal lattice with a period of 2000 nm can almost achieve this performance. Thus, it is possible to design a specific wavelength range in the spectral range of 20 nm or higher using a hole size range of 800-1700 nm with a period range of 900-2000 nm. Other diameters and periods can also be used, and the described example shows that certain combinations of hole diameter and period will absorb less than 10%, 20%, 30%, 40%, 50% ripple. It shows that it can be improved.

The hole diameter can be greater than or less than the wavelength, and the period in free space is much greater than the wavelength. Subwavelength periods can also be used in conjunction with periods above a certain wavelength.

This example shows a useful spectral range of 20 nm and in some cases 10 nm and in some cases over 40 nm, 5 Gb / s, and in some cases 10 Gb / s and in some cases Various hole diameters can be used with the same period to design an operable 850 nm PD / APD in Si, with data rates of 20 Gb / s and in some cases over 30-40 Gb / s it is shown that. For example, other hole diameters and periods can be used to optimize the absorption enhancement at 850 nm wavelength, 980 nm wavelength, in which case generally the hole diameter and Correspondingly, the period is correspondingly larger. Multiple hole diameters and / or multiple periods can be used to extend the microstructured silicon PD / APD to longer wavelengths, for example, 40% improved absorption at wavelengths from 800 to 1000 nm And in some cases 50% or more, and in some cases 60% or more, and in some cases 70% or more, and in some cases, it is 80% or more, and in some cases 90% or more at a certain wavelength. For longer wavelengths, for example at 1550 nm, the holes and period can be, for example, 1300 nm diameter and 1500 nm diameter with periods of 2300 and 2500 nm, in which case the period is increasing. Other hole diameter / period for 1550 nm wavelength in Ge-on-Si can be, for example, 2300/3100 (nm unit), 2800/3100 (nm unit), in which case the diameter and period Both are increasing.

In addition, other shapes such as chevron or "V" shaped holes can be used to improve absorption. Other shapes can be "X" shapes, rectangular shapes, triangular shapes, polygonal shapes, and / or any combination of multiple shapes to achieve the desired absorption enhancement and spectral width and polarization sensitivity, is there.

FIG. 110 shows a plot of absorption versus wavelength for microstructured / avalanche photodiodes with different hole diameters and grating periods, based on some examples. The simulated MS-PD / APD had a square grid and photons were incident from either the top surface or the bottom surface. The absorption layer is about 2 μm thick with Ge. The structure is the same as that shown in FIG. 82A. In the absorption curve with respect to the wavelength, for example, a microstructure having a period of 2800 nm and a hole diameter of 1500 nm represented by the curve 11010 shows good absorption characteristics of incident photons in the wavelength range from 1500 nm to 1650 nm. Among the absorption curves for that wavelength, for example, a microstructure with a period of 3000 nm and a hole diameter of 2250 nm represented by curve 11012 shows good absorption properties for incident photons in the wavelength range from 1650 to 1700 nm, for example. The combination of these two hole diameters and gratings may result in better than 80% absorption for the wavelength range from 1500 to 1700 nm. To achieve good absorption properties, eg better than 50%, in some cases better than 40%, and in some cases better than 30% etc. It is also possible to use a combination of At some wavelengths, it is possible to achieve better than 80%, for example 1550 nm wavelength ± 10 nm or more. Further, 1664 nm can achieve 80% absorption efficiency better than a few nanometers at the wavelength. Other hole diameters / periods of 1875 nm / 2500 nm are also shown and are represented by curve 11014.

In some cases, the hole diameter can be greater than the wavelength of light incident on the microstructured PD / APD to be absorbed, and in some cases, the hole diameter. The diameter of the hole can be approximately the same as the wavelength of the incident photon, and in some cases the diameter of the hole can be smaller than the wavelength of the incident photon. The same can be said for the period of the grating, in which case the period may be smaller, substantially the same and / or larger than the incident wavelength of the light to be detected, is possible.

111A and 111B show a simulation using the FDTD method of the structure shown in FIG. 82A based on some examples, using two grids and two different hole diameters. Yes. FIG. 111A shows a hole pattern in which a hexagonal lattice having a hole diameter D1 of 1500 nm is combined with D2 of 2250 nm at the center and a square lattice having D1 at four corners. The D1 holes are separated by 3 μm (d2 = 3 μm) in the horizontal direction and about 3.46 μm in the vertical direction. The hexagonal lattice has a period of 2 μm (d1 = 2 μm). FIG. 111B shows a plot of absorption versus wavelength. The two different hole diameter cases for the two gratings (curve 11110) show that at some wavelengths, the absorption is better than that of single grating / hole microstructured PD / APD. It is possible to see what is shown. For example, in the L band at about 1570 nm to 1600 nm, the data / telecommunications wavelength, curve 11110 shows much better absorption. This is compared to, for example, a square grating with a 2 μm period (curve 11112) at a hole diameter of 1500 nm and a 2 μm period (curve 11114) at a hole diameter of 2250 nm. The result is that with different combinations of hole diameter and period, the absorption response can have less resonance and / or less sharp resonance and can be optimally tuned in a certain wavelength range it just shows that. This is just one example, to obtain the desired quantum efficiency, polarization sensitivity, insensitivity, wavelength selectivity and / or nonselectivity, eg, broadband, ripple / resonance reduction, etc., grating, period, hole diameter And other combinations of shapes can be simulated. For example, the diameter or minimum diameter can range from 100 nm to 3000 nm, and the period and / or multiple periods can range from 150 nm to 4000 nm. Further, the hole pattern may not be a grid, for example, a plurality of holes may be non-periodically distributed and / or a spacing between the plurality of holes may be changed. Further, although the hole pattern may not need to be periodic, the pattern can be periodic or aperiodic. Multiple holes can be distributed randomly or pseudo-randomly.

and the hole diameter can vary in a periodic, non-periodic manner, a random manner, or a pseudo-random manner. Further, for example, if the periods are the same, almost the same, or less than the diameter of the holes in a period, the holes can be connected at least at one point. The array of holes can have a plurality of periods, and at least one period can cause the holes to contact and / or overlap.

Using a coupling of a resonant cell with an adjacent neighboring resonant cell according to the techniques described herein, absorption response smoothing is achieved, which has only a single resonator and absorbs for that wavelength. In contrast to existing resonant photodiodes exhibiting sharp resonant operation. A population of resonant cells based on the techniques described herein results in a more tuned absorption response with controlled ripple and wavelength range. Further, the techniques described herein can be used to tune specific absorption characteristics at specific wavelengths for more optimal PD / APD performance at specific wavelengths.

In addition, other microstructures / nanostructures that do not participate in the absorption enhancement process can be used to reduce reflections, for example with dimensions (diameters etc) in the range of tens to hundreds of nanometers. Sub-wavelength holes or pits on the surface, in which case the depth can be in the range of tens to hundreds of nanometers or more.

FIG. 112 is a schematic diagram illustrating another lattice structure in which two hexagonal lattices of the same period are combined and interlaced with each other according to some embodiments. The pattern can use holes of the same or different diameters. As shown, the pattern has two different diameters, for example, the period can be 2500 nm, and D1 can be 1500 nm and D2 can be 700 nm. Is possible. Other combinations of period and diameter are possible, and to adjust the absorption characteristics, and thus the quantum efficiency for the incident photon wavelength, and the wavelength span where the absorption characteristics are acceptable for optical data / telecommunications purposes, and Used to satisfy any particular application condition for that particular optical system or systems.

The unit cells as shown by the dotted lines of the two hexagonal grids overlap each other, so their eigenmodes also overlap each other, which further reduces the ripple of the absorption characteristics in a specific wavelength range. It is also possible to extend the wavelength range in which the ripple in the absorption characteristic is reduced. Sharp changes in the absorption characteristics within a certain wavelength range are undesirable in a photodiode / avalanche photodiode. This is because, for example, drift in the incoming optical signal wavelength and / or drift in the photodiode absorption characteristics with respect to temperature can cause significant changes in optical to electrical signal conversion. Changes of less than 5% are preferred, and in some other cases 10%, 20%, 30 within a wavelength range of 2 nm, 4 nm, 10 nm, 20 nm, 40 nm, 80 nm, 100 nm, or 250 nm. %, 40% or less than 50% is preferred.

FIG. 113 shows a hexagonal lattice with six unit cells, each cell having its own eigenmode, where any field propagation / distribution is an extension of that eigenmode. It may be. The eigenmodes of each cell can be combined with the eigenmodes of neighboring cells, thereby forming a composite coupled supermode, which is for visualization purposes only, but with multiple pendulums Can be thought of as a 2D array of couplings, where each pendulum is connected to all its adjacent pendulums via a weak spring (the weak spring is a mechanical coupling mechanism) The response or motion of this massively coupled 2D array pendulum is very complex and not a simple oscillating motion of a single pendulum. In addition to the coupling, a second nested hexagonal lattice can be added as in FIG. In addition, holes in the cell and / or in any shape and of any depth, of any depth and of any diameter, and any of the parameters can have a plurality of values. It can be added to the boundary of an adjacent cell, which can effect its eigenmode and its coupling with the adjacent cell eigenmode. For example, for convenience of explanation, a plurality of holes of diameter X can be added as shown, where X can have a single value or multiple values and the holes can be Si or Ge. It is possible to etch partially or completely at the surface and within the absorber layer. This can also be such that it does not penetrate the absorbing layer only on the surface. According to some embodiments, the holes can be partially or fully etched into the absorber layer.

The coupling of the cell, which becomes a complex standing wave or super eigenmode, results in a single resonator such as a resonant response as in previously known structures having sharp response characteristics in absorption response (proportional to quantum efficiency) It is possible to give a smoother absorption versus wavelength response compared to

FIG. 114 illustrates a SiNIP microstructured photodiode having a hole array and a textured surface, according to some embodiments. The texture surface 11440 can be on the top surface and / or in the hole 11422 itself. Texturing can be performed at an angle off-vertical, in which case the substrate can be rotated (or stationary) in a tilted manner with respect to the dry etching beam (direction), and the texture can be, for example, it is possible to make it partially on the side wall. According to some embodiments, texture 11440 reduces the reflection of incident illumination. This is because in an optical communication link, the optical signal reflected back to the optical source is undesirable and may cause signal to noise degradation in the data communication system. Texturing, such as black silicon, with or without masking and dry etching on the semiconductor surface can generate a forest of nanostructures that can trap photons and reduce reflections. . In the absence of texturing, the reflection is less than 10% and in some cases less than 5% and in some cases less than 2%, for example as in FIG. It can be seen in the plot of absorption for various wavelengths, where the absorption is greater than 90-95% at certain wavelengths. From the equation T + T + R + A, where T is transmitted light, R is reflected light, A is absorbed light, and when A = 90-95%, T + R is 5-10%. Thus, R is 10% or less, and in some cases 5% or less. Adding texture to the semiconductor surface can further reduce reflection to less than 1% at certain wavelengths. Furthermore, the optical signal can be incident on the microstructured PD / APD at an angle that is off-vertical and can further reduce reflection back into the optical data communication channel. .

FIG. 115 is a graph showing absorption coefficients of Si and Ge with respect to wavelength. For example, FIG. Should be referred to and incorporated herein by reference. At 850 nm for Si and 1550 nm for Ge, both have an absorption coefficient of less than about 360 / cm. This weak absorption results in poor quantum efficiency for high speed photodiodes and / or avalanche photodiodes, for example, which typically have an absorption thickness of about 2 μm for data rates above 10 Gb / s bandwidth. . This is one reason why high-speed photodiodes exceeding the data rate of, for example, 5 Gb / s are not commercially available for the wavelength of 850 nm for Si and 1550 nm for Ge. .

FIG. 116 is a graph illustrating the improved effective absorption coefficient of Ge due to a microstructured hole array, according to some examples. Curve 11610 shows the improved absorption coefficient for Ge in a hexagonal lattice with a 1.25 μm hole diameter and a 1.45 μm period for a 2 μm thick layer of Ge. For comparison, curve 11612 shows the absorption coefficient of bulk Ge (without microstructured holes). According to some embodiments, other microstructures can provide an improved effective absorption coefficient that can be optimized for a wavelength band. For example, the microstructure can be holes or pillars, the spacing can be periodic or aperiodic, and the holes or pillars have a single or multiple diameters. And the shape can be circular or non-circular. As indicated above, absorption is the product of the absorption coefficient and the absorption length. Therefore, it is possible to make the absorption length an improved effective absorption length while maintaining the absorption coefficient as the absorption coefficient of the bulk material (curve 11612 in the case of Ge), that is, 5 or more than the physical absorption length. It can be 10, 20, or even longer. As can be seen from FIG. 116, the improved effective absorption coefficient is more than 10 times greater than the bulk absorption coefficient in Ge in many wavelength ranges. Improved effective absorption coefficient in Ge due to microstructure is greater than 30%, greater than 40%, greater than 50%, greater than 60%, greater than 70%, greater than 80%, greater than 90% knowledge With quantum efficiency (directly proportional to absorption), typically the absorption length at 1550 nm wavelength and longer wavelengths is about 2 μm or less, allowing the development of high-speed PD / APD. It is not known that such a combination of material, absorption length, wavelength, data rate, and quantum efficiency is commercially available for both Si and Ge. The same is true for high data rate bandwidths where the absorption length is typically about 2 μm or less for data rates of 5, 10, 20 Gb / s and faster and for wavelength ranges of 805 nm and longer, for example. It can also be said about the Si microstructure type PD / APD for the operation in FIG.

In addition, the microstructures can be composed of a single element or cell and / or multiple elements or cells, and of a linear optical field effect, a nonlinear optical field effect, a coupled mode effect, and / or a slow wave effect. It is possible to have improved effective absorption and / or improved effective absorption length that may be

the result.

Improved absorption coefficient and / or absorption length using microstructures can be used to extend the operating wavelength of other materials such as III-V materials, GaAs, InP, GaN, etc. at the edge of the band where the absorption coefficient is weaker it is also possible to do. For example, see Figure 3 at Slawomir S. Piatek, http://www.hamamatsu.com/us/en/community/optical_sensors/tutorials/physics_of_mppc/index.html?utm_source=googleplus&utm_medium=social&utm_campaign=no-social. It is for InGaAs in the vicinity of the 1.6 μm wavelength and is incorporated herein by reference. According to some embodiments, the microstructure can be used to extend operating wavelengths near 1.6 μm and longer.

In addition, the use of microstructures to improve absorption can be applied to amorphous materials such as amorphous Si and also other materials such as polymers, ceramics, graphene, alloys and oxides it is also possible to apply to. In addition, other forms of energy propagation, such as acoustic, microwave, UV, X-ray, and pressure waves, can be converted from one form of energy to another. For example, structures with dimensions on the order of approximately acoustic wavelengths on piezoelectric ceramics and / or crystals can, for example, improve the conversion of acoustic energy to electrical energy. Using a structure with dimensions of approximately acoustic wavelengths can improve acoustic absorption, which can be, for example, a thinner piezoelectric material, which can be, for example, more Making it possible to have a high acoustic frequency response.

FIG. 117 is a graph showing improved absorption of Si microstructure PD / APD based on some examples. The simulated MS-PD / APD has a hexagonal lattice hole array, a period of 2000 nm, a diameter of 1500 nm, and photons incident at a deviation of 10, 20, 40 degrees from the vertical, for example. FIG. 39 shows a simulation of improved absorption versus wavelength for a similar structure when photons are incident normal to the surface. As can be seen, photons that are off by 10 degrees from normal do not significantly change the absorption at a wavelength of 850 nm, which is still greater than 90%. At 40 degrees, the absorption at 850 nm is still above 90%, but at 20 degrees, the absorption appears to decrease to 85% at 850 nm. Overall, at certain wavelengths, changes in the incident angle of photons incident on the microstructure can have an absorption change of less than 10% over an angular range of 0-40 degrees, for example. By optimizing hole diameter, period, and non-periodic microstructure over a range of wavelengths, the change in quantum efficiency (directly proportional to absorption) with respect to the incident angle of incident photons can be made less than 10%. And in some cases less than 5% and in some cases less than 3%. This feature is important for minimizing reflected light back toward the laser source, which can transmit electrical signals for transmission in optical fibers and / or free space and / or optical waveguides. When an optical modulator is used to convert to an optical signal, it is modulated directly or indirectly at the data rate for transmitting the optical signal. Using a non-laser source, such as a light emitting diode, as an electrical signal to optical signal converter reduces the condition of the reflected power returned toward the optical source. This is because LEDs are less coherent and / or incoherent optical sources, and reflections at the same wavelength are less disruptive in integrity as electrical to optical signal converters.

Although this patent application refers to certain theories in describing the nature and operation of the device, these theories are based on current understandings, even if the theory is incorrect due to future progress. Obviously, even if it proves, it does not affect the actual operation of the device disclosed herein. This patent specification also refers to numerical ranges of parameters, and it should be understood that insubstantial deviations from such ranges are within the spirit of the progress disclosed herein.

The drawings illustrating the device are not to scale and are somewhat idealized, for example straight lines are sharp corners, etc., while the actual device is not very straight or smooth. It should be understood that there may be no walls and some rounded corners and there is a probability, in fact, depending on the processing parameters, walls such as holes or pillar walls in the microstructure may be uneven and have a rough surface with surface features such as depressions and dents. This may actually contribute to effects such as reduction of unwanted reflections.

Semiconductor layers for light sensing and / or signal processing and distribution integrated circuits may be vapor phase epitaxy, chemical vapor deposition, plasma enhanced chemical vapor deposition, atomic layer deposition, molecular beam epitaxy, etc. and / or, for example, selective area epitaxy Can be grown epitaxially using techniques such as selective area epitaxial lateral overgrowth, epitaxial lateral overgrowth, heteroepitaxy, wafer bonding, epitaxial lift-off process, and any combination of growth, bonding, lift-off processes, etc. It is. A suitable process for the semiconductor layer is vapor phase epitaxy or chemical vapor deposition.

Further, the microstructure holes can only be in the high field "I" region for absorption and necessarily extend into and / or through the N and P regions of the PD / APD is not. The holes can overlap over their entire length and / or adjacent holes can partially overlap along the length of the hole.

The doping of the P / I and N regions often has a gradual transition between different doping level regions due in part to dopant diffusion during epitaxial growth. The transition from high doping to low doping may occur over a distance of 1 to 1000 nm or more, depending on the dopant type, doping level, growth temperature and epitaxial deposition method. The PIN structure is often P + P P-I-N N- N +, where P and P- and N and N- are transition regions and a very narrow transition region is desirable.

Although described above in some detail for purposes of clarity, it will be apparent that certain changes and modifications may be made without departing from the principles thereof. It should be noted that there are many alternative ways of implementing both the processes and apparatus described herein. Accordingly, this example should be considered as illustrative and not limiting, and the content of the performance described herein should not be limited to the details described herein. Changes may be made within the scope of the claims and their equivalents.

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RU2732604C1 *	2019-03-12	2020-09-21	Общество С Ограниченной Ответственностью "Детектор Фотонный Аналитический" (Ооо "Детфан")	Avalanche photodetector (embodiments) and method of manufacturing thereof (embodiments)
US10930747B2 *	2019-05-04	2021-02-23	Nxp B.V.	Semiconductor device with an enclicled electrode
CN110034138B *	2019-05-11	2022-01-28	Oppo广东移动通信有限公司	Pixel structure, image sensor and terminal
CN112862987A	2019-08-01	2021-05-28	艾迈斯欧洲有限公司	Microstructure enhanced absorption photosensitive device
CN112289125A *	2019-08-05	2021-01-29	上海新微技术研发中心有限公司	Waveguide type germanium photoelectric detector based on photonic crystal and preparation method
US11605752B2 *	2019-09-25	2023-03-14	Massachusetts Institute Of Technology	Resonance enhanced surface illuminated sub-bandgap infrared photodetectors
US11448809B2 *	2019-10-17	2022-09-20	Taiwan Semiconductor Manufacturing Co., Ltd.	Multifunctional collimator for contact image sensors
CN110854141A *	2019-11-21	2020-02-28	中国电子科技集团公司第四十四研究所	Monolithic integrated balanced photoelectric detector chip and manufacturing method thereof
US20220035086A1 *	2019-11-22	2022-12-08	The Board Of Trustees Of The Leland Stanford Junior University	High-quality-factor metasurface for phase contrast imaging and spatial frequency filtering
GB2589075A *	2019-11-20	2021-05-26	Smart Photonics Holding B.V.	Waveguide structure for a photonic integrated circuit
FR3109944B1	2020-05-11	2023-11-03	Mesquilli Stephane	Antifouling coating, biocide, antiseptic, ecological non-solvent, metalloplastic with lamellar structure
WO2022024641A1 *	2020-08-03	2022-02-10	株式会社京都セミコンダクター	Light receiving element unit

CN112018140A *	2020-08-14	2020-12-01	清华大学	Miniature spectrum chip based on random shape unit
CN112531038*	2020-09-27	2022-09-20	北京工业大学	Preparation method of side-incident SOI (silicon on insulator) based Si/SiGe HPT (high-performance heterojunction bipolar transistor) with photonic crystal structure
CN112420857A *	2020-10-20	2021-02-26	北京工业大学	Photonic crystal SiGe/Si phototransistor detector
CN112038388*	2020-10-29	2022-03-15	西安理工大学	Light-adjustable four-frequency-band terahertz metamaterial absorber based on all-dielectric material
US11538961462	2020-11-17	2022-12-27	GlobalFoundries U.S. Inc.	Photodetector array with diffraction gratings having different pitches
US11482562B2	2020-12-30	2022-10-25	Applied Materials, Inc.	Methods for forming image sensors
FR3120988B1 *	2021-03-23	2023-11-03	St Microelectronics Crolles 2 Sas	Optical device
KR102307779B1 *	2021-03-24	2021-10-01	이상훈	Backside illuminated avalanche photodiode and manufacturing method thereof
CN115036398*	2021-03-09	2022-09-09	南京大学	Method for producing an absorber-emitter structure for solar thermal photovoltaic cells
CN113284948*	2021-05-14	2023-07-05	长春理工大学	Avalanche photodiode structure with high responsivity
CN115700928A *	2021-07-15	2023-02-07	上海新微技术研发中心有限公司	Photodetector and method of manufacturing the same
CN115909838*	2021-10-25	2023-07-04	西安电子科技大学芜湖研究院	Photodiode with strong light absorption capacity and preparation method thereof
US11721780B2 *	2021-11-17	2023-08-08	GlobalFoundries U.S. Inc.	Avalanche photodetectors with a multiple-thickness charge sheet
KR20230089137A *	2021-12-13	2023-06-20	삼성전기주식회사	Multi-layer capacitor
US11848393B2 *	2022-04-11	2024-04-02	Ciena Corporation	Suppression of phototransistor gain in an optical modulator
WO2023211261A1 *	2022-04-28	2023-11-02	Compoundtek Pte. Ltd.	Optical bench apparatus and fabrication method therefor for heterogeneous laser integration
CN114823941B *	2022-04-29	2024-04-02	南京大学	Resonance enhanced photoelectric detector and manufacturing method thereof
CN115224388*	2022-06-17	2023-12-08	浙江大学	Horizontal pull-through germanium-silicon avalanche photodetector

* Cited by examiner, † Cited by third party, ‡ Family to family citation

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US10468543B2	2019-11-05	Microstructure enhanced absorption photosensitive devices
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US8637907B2	2014-01-28	Semiconductor light receiving element and optical communication device
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Priority And Related Applications

Applications Claiming Priority (39)

Application	Filing date	Title
US201462081538P	2014-11-18	
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US62/232,716	2015-09-25	
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Legal Events

Date	Code	Title	Description
2017-11-29	A711	Notification of change in applicant	**Free format text**: JAPANESE INTERMEDIATE CODE: A711 **Effective date**: 20171129
2017-12-15	A521	Request for written amendment filed	**Free format text**: JAPANESE INTERMEDIATE CODE: A821 **Effective date**: 20171129
2017-12-26	A521	Request for written amendment filed	**Free format text**: JAPANESE INTERMEDIATE CODE: A523 **Effective date**: 20171226
2018-01-26	A521	Request for written amendment filed	**Free format text**: JAPANESE INTERMEDIATE CODE: A523 **Effective date**: 20180116
2018-10-18	AA21	Written request for application examination	**Free format text**: JAPANESE INTERMEDIATE CODE: A821 **Effective date**: 20181018
2019-10-15	A977	Report on retrieval	**Free format text**: JAPANESE INTERMEDIATE CODE: A971007 **Effective date**: 20191015
2019-12-03	A131	Notification of reasons for refusal	**Free format text**: JAPANESE INTERMEDIATE CODE: A131 **Effective date**: 20191203
2020-02-27	A601	Written request for extension of time	**Free format text**: JAPANESE INTERMEDIATE CODE: A601 **Effective date**: 20200227
2020-04-27	A521	Request for written amendment filed	**Free format text**: JAPANESE INTERMEDIATE CODE: A523 **Effective date**: 20200427
2020-09-29	A131	Notification of reasons for refusal	**Free format text**: JAPANESE INTERMEDIATE CODE: A131 **Effective date**: 20200929
2020-12-23	A601	Written request for extension of time	**Free format text**: JAPANESE INTERMEDIATE CODE: A601 **Effective date**: 20201223
2021-02-25	A521	Request for written amendment filed	**Free format text**: JAPANESE INTERMEDIATE CODE: A523 **Effective date**: 20210225
2021-03-31	TRDD	Decision of grant or rejection written	
2021-04-06	A01	Written decision to grant a patent or to grant a registration (utility model)	**Free format text**: JAPANESE INTERMEDIATE CODE: A01 **Effective date**: 20210406
2021-04-27	A61	First payment of annual fees (during grant procedure)	**Free format text**: JAPANESE INTERMEDIATE CODE: A61 **Effective date**: 20210423

2021-04-27	R150	Certificate of patent or registration of utility model	**Ref document number**: 6875987 **Country of ref document**: JP **Free format text**: JAPANESE INTERMEDIATE CODE **Ref document number**: 6875987 **Country of ref document**: JP **Free format text**: JAPANESE INTERMEDIATE CODE: R150
2024-05-07	R250	Receipt of annual fees	**Free format text**: JAPANESE INTERMEDIATE CODE: R250

Concepts

machine-extracted

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Name	Image	Sections	Count	Query match
absorption reaction		title,claims,abstract,description	490	0.000
silicon		claims,abstract,description	185	0.000
silicon		claims,abstract,description	124	0.000
silicon		claims,abstract,description	122	0.000
method		claims,abstract,description	66	0.000
semiconductor		claims,abstract,description	49	0.000
reductive effect		claims,abstract,description	15	0.000
optical effect		claims,description	120	0.000
substrate		claims,description	112	0.000
material		claims,description	102	0.000
nitrogen		claims,description	70	0.000
phosphorus		claims,description	68	0.000
fiber		claims,description	40	0.000
processing		claims,description	33	0.000
communication		claims,description	29	0.000
optical fiber		claims,description	29	0.000
process		claims,description	28	0.000
germanium		claims,description	27	0.000
reversible effect		claims,description	27	0.000
etching		claims,description	25	0.000
germanium atom		claims,description	12	0.000
Overgrowth		claims,description	9	0.000
light absorption		claims,description	9	0.000
crystal		claims,description	8	0.000
detection method		claims,description	8	0.000
silicon based material		claims,description	7	0.000
integration		claims,description	6	0.000
metal oxide		claims,description	6	0.000
metal oxides		claims,description	5	0.000
chemical reaction		claims,description	3	0.000

※ complement effect	claims,description	3	0.000
※ benefit	abstract,description	18	0.000
※ packaging method and process	abstract,description	10	0.000

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H01L	31/0232	(2014.01)	H01L	31/02	D	2G065
G01J	1/02	(2006.01)	G01J	1/02	C	4M118
G01J	1/42	(2006.01)	G01J	1/42	H	5F849
G01J	1/04	(2006.01)	G01J	1/04	B	

審査請求 未請求　予備審査請求 未請求　（全 103 頁）　最終頁に続く

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最終頁に続く

(54)【発明の名称】マイクロストラクチャ向上型吸収感光装置

(57)【要約】
【課題】　マイクロストラクチャを使用して半導体におけるフォトンの吸収を向上させる技術を記載する。該マイクロストラクチャは、例えば穴であって、フォトンの吸収を実効的に増加させる。シリコンフォトダイオード及びシリコンアバランシェフォトダイオードに対して吸収向上のためにマイクロストラクチャを使用することは、約９０％以上の量子効率で８５０ｎｍの波長を有するフォトンにおいて１０Ｇｂ／ｓを越える帯域幅となる場合がある。それらの厚さ寸法は、それらがＣＭＯＳ，ＢｉＣＭＯＳ及びその他のエレクトロニクスと同一のＳｉチップ上に便利に集積化させることを可能とさせ、その結果パッケージング上の利点が得られ、容量が減少され、従って一層高速となる。
【解決手段】
【選択図】　図１

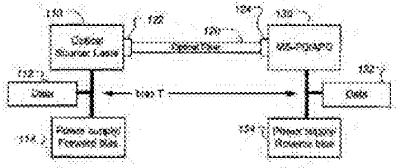


FIG. 1

【特許請求の範囲】
【請求項１】
単一半導体チップ内に形成されているマイクロストラクチャ向上型光吸収を具備する光検知器と電子的プロセッサとの両方を有しているデータ通信用の集積化検知器／プロセッサ回路において、
半導体基板上に形成されており且つデータ通信用に変調された光学ソース信号からのフォトンを吸収し且つそれに対応する出力電気信号を供給する形態とされているフォトン吸収領域を有している光検知器が設けられており、
前記フォトン吸収領域はその中に複数個の穴を有しており、該穴は前記基板へ向けて延在しており且つ複数の該穴において同一のソース信号を同時的に受け取る形態とされており、
電子的プロセッサも前記半導体基板上に形成されており且つ前記フォトン吸収領域と動作上関連されていて前記出力電気信号をそれから受け取り且つ処理済出力へ処理し、それにより該光学ソース信号を受け取り且つ該処理済出力を出力する単一の半導体チップを形成しており、
前記フォトン吸収領域及び前記電子的プロセッサは同じ程度の厚さである夫々の厚さを有しており、及び
カソード領域とアノード領域とが前記フォトン吸収領域と逆バイアス回路とに動作上関連されていて、前記逆バイアス回路は前記カソード領域が前記アノード領域よりも一層正の電圧へ駆動されるように前記カソード領域と前記アノード領域との間に電圧を印加する形態とされている、
集積化検知器／プロセッサ回路。
【請求項２】
該フォトン吸収領域の厚さが０．５乃至５マイクロメートルの範囲内である請求項１記載の集積化検知器／プロセッサ回路。
【請求項３】
該電子的プロセッサが相補的金属酸化物半導体（ＣＭＯＳ）装置、バイポーラ（Ｂｉ）装置、及びＢｉＣＭＯＳ装置の内の少なくとも一つを有している応用特定集積回路（ＡＳＩＣ）を有している請求項１記載の集積化検知器／プロセッサ回路。
【請求項４】
該フォトン吸収領域は、８００ｎｍ乃至９００ｎｍの波長において入射ソース信号を４０％を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項１記載の集積化検知器／プロセッサ回路。
【請求項５】
該フォトン吸収領域は、８００ｎｍ乃至９００ｎｍの波長において入射ソース信号を５０％を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項１記載の集積化検知器／プロセッサ回路。
【請求項６】
該フォトン吸収領域は、８００ｎｍ乃至９００ｎｍの波長において入射ソース信号を６０％を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項１記載の集積化検知器／プロセッサ回路。
【請求項７】
該フォトン吸収領域は、１４００ｎｍ乃至１７００ｎｍの波長において入射ソース信号を４０％を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項１記載の集積化検知器／プロセッサ回路。
【請求項８】
該フォトン吸収領域は、１４００ｎｍ乃至１７００ｎｍの波長において入射ソース信号を５０％を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項１記載の集積化検知器／プロセッサ回路。
【請求項９】

Samsung Exhibit 1090, Page 103 of 786
Samsung v. W&Wsens - IPR2025-00993

該フォトン吸収領域は、１４００ｎｍ乃至１７００ｎｍの波長において入射ソース信号を６０％を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項１記載の集積化検知器／プロセッサ回路。
【請求項１０】
該フォトン吸収領域は、８００ｎｍ乃至９００ｎｍのソース信号波長の少なくとも２０ｎｍの選択した波長スパンに亘って２０％未満だけ変化する吸収百分率において該入射ソース信号を吸収する形態とされている請求項１記載の集積化検知器／プロセッサ回路。
【請求項１１】
該フォトン吸収領域は、１４００ｎｍ乃至１７００ｎｍのソース信号波長の少なくとも２０ｎｍの波長スパンに亘って２０％未満だけ変化する吸収百分率において該入射ソース信号を吸収する形態とされている請求項１記載の集積化検知器／プロセッサ回路。
【請求項１２】
各穴は該基板の表面に平行な断面を有しており且つ該断面の最大寸法は４００ｎｍと２５００ｎｍとの間であり、及び各穴は該複数個の穴の最も近い隣接する穴の中心から３５００ｎｍ未満だけ離隔されている中心を有している請求項１記載の集積化検知器／プロセッサ回路。
【請求項１３】
前記光検知器は、更に、10^{19}／cm^3又はそれを超えて高度にドープされており且つ前記フォトン吸収領域の側面に位置しているＰ層とＮ層とを有しており、及び該フォトン吸収領域は軽度にドープされているか又は意図的にはドープされておらず高々10^{16}／cm^3である請求項１記載の集積化検知器／プロセッサ回路。
【請求項１４】
前記光検知器がアバランシェ光検知器を有している請求項１記載の集積化検知器／プロセッサ回路。
【請求項１５】
該フォトン吸収領域がＳｉを有している請求項１記載の集積化検知器／プロセッサ回路。
【請求項１６】
該フォトン吸収領域がＧｅを有している請求項１記載の集積化検知器／プロセッサ回路。
【請求項１７】
該光検知器が、前記ソース信号を担持するオプチカルファイバーを受け付け且つ該ファイバーの一端部を前記フォトン吸収領域から選択した距離に維持する形態とされているテーパー付き又は段差付きの穴を有している請求項１記載の集積化検知器／プロセッサ回路。
【請求項１８】
更に、該ファイバーの前記端部と該フォトン吸収領域との間にレンズを包含している請求項１７記載の集積化検知器／プロセッサ回路。
【請求項１９】
該光検知器が、該ソース信号の複数回の反射を発生させて前記ソース信号が該フォトン吸収領域を複数回横断する形態とされている反射構造を有している請求項１記載の集積化検知器／プロセッサ回路。
【請求項２０】
該光検知器が、該フォトン吸収領域の２つの対向する側部から該ソース信号を受け取る形態とされている請求項１記載の集積化検知器／プロセッサ回路。
【請求項２１】
前記穴が、該穴の複数のグループにおいて光信号から電気信号への変換において結合共振を発生させてソース信号の吸収を向上させる形態とされている請求項１記載の集積化検知器／プロセッサ回路。
【請求項２２】

Samsung Exhibit 1090, Page 104 of 786
Samsung v. W&Wsens - IPR2025-00993

更に、一つ又はそれ以上の付加的な光検知器が前記半導体基板上に形成されており且つ夫々の付加的なソース信号を受け取り且つそれらに対応する夫々の出力電気信号を供給する夫々のフォトン吸収領域を有しており、及び一つ又はそれ以上の付加的な電子的プロセッサも前記半導体基板上に形成されており且つ前記付加的な光検知器の該夫々のフォトン吸収領域と動作上関連されていてそれから前記夫々の出力電気信号を受け取り且つ処理する請求項１記載の集積化検知器／プロセッサ回路。

【請求項２３】

該複数個の穴は、前記ソース信号の波長を含む波長範囲において、穴は無いがその他は同じ光検知器と比較してフォトンの吸収を向上させる請求項１記載の集積化検知器／プロセッサ回路。

【請求項２４】

該電子的プロセッサは、相互インピーダンス増幅器、信号処理エレクトロニクス、及びルーチングエレクトロニクスからなるグループから選択される一つ又はそれ以上のタイプを包含している請求項１記載の集積化検知器／プロセッサ回路。

【請求項２５】

該光検知器と関連している容量が、そのアノード領域とカソード領域とを従来のボンドパッドへ動作接続させているその他は同じ光検知器と比較して減少されている請求項１記載の集積化検知器／プロセッサ回路。

【請求項２６】

該光検知器は、更に、増倍領域を有しており且つ２より大きな利得を有しており８００乃至９００ｎｍのソース信号波長において１０Ｇｂ／ｓより大きなデータ帯域幅において該ソース信号を検知する形態とされているアバランシェフォトダイオードである請求項１記載の集積化検知器／プロセッサ回路。

【請求項２７】

光学／電子システムにおいて、

光検知器とアクティブ電子回路とが、同一の半導体基板上に構築されており且つ互いに動作上関連されていて単一の集積回路チップを形成しており、

レーザーが、Ｇｂ／ｓのデータレートで変調されてＧｂ／ｓレートで情報を担持する光学ソース信号を発生し、

オプチカルファイバーが、該レーザーと関連していてその入力端において該光学ソース信号を受け取り且つそれをその出力端へ運び、

該光検知器が、該オプチカルファイバーの該出力端と関連していてそれから該光学ソース信号を受け取り且つそれを電気出力信号へ変換させる形態とされており、及び

該アクティブ電子回路が該光検知器と関連していてそれから該出力電気信号を受け取り且つ該電気出力信号を処理して前記処理済電気信号を出力する形態とされている、

システム。

【請求項２８】

該ソース信号及び該電気出力信号の各々が、少なくとも５Ｇｂ／ｓのレートで変調されている請求項２７記載のシステム。

【請求項２９】

該光検知器及び該アクティブ電子回路が、同じ程度の大きさである厚さを有している請求項２７記載のシステム。

【請求項３０】

該光検知器が、該半導体基板へ向かって延在する複数個の穴を包含しているフォトン吸収領域を有しており、複数の穴が同じソース信号を同時的に受け取る形態とされている請求項２７記載のシステム。

【請求項３１】

高度にドープされたＰ層及びＮ層が該フォトン吸収領域の側面に位置しており、及び該フォトン吸収領域は０．１－５．０マイクロメートルの範囲内の厚さを有しており且つ意図的にはドープされていないか又は該Ｐ及びＮ領域と比較して軽度にドープされている請

Samsung Exhibit 1090, Page 105 of 786
Samsung v. W&Wsens - IPR2025-00993

求項２７記載のシステム。
【請求項３２】
該光検知器がバイアスされて電子又は正孔の内の少なくとも一方を該ソース信号が該光検知によって受け取られる方向に沿う方向に移動させる請求項２７記載のシステム。
【請求項３３】
該光検知器及び該アクティブ電子回路の各々がシリコンをベースとしている請求項２７記載のシステム。
【請求項３４】
該光検知器がアバランシェ光検知器である請求項２７記載のシステム。
【請求項３５】
マイクロストラクチャ向上型光吸収を有する光検知器において、
０．５及び５マイクロメートルの間の厚さを持っており且つデータ通信用に変調されたソース信号からフォトンを吸収し且つそれに対応する出力電気信号を供給する形態とされているフォトン吸収領域が設けられており、
前記フォトン吸収領域は複数個の穴を有しており、該複数個の穴は該フォトン吸収領域の該厚さの少なくとも一部を介して延在しており且つ複数の該穴において同じソース信号を同時的に受け取る形態とされており、及び
前記フォトン吸収領域は、８００ｎｍ乃至９００ｎｍ及び１４００ｎｍ乃至１７００ｎｍの範囲の内の少なくとも一つにおける波長において該入射ソース信号を４０％を越えて受け取り且つそれに対応する出力電気信号を供給する形態とされている、
光検知器。
【請求項３６】
該フォトン吸収領域は、８００ｎｍ乃至９００ｎｍの波長において該入射ソース信号を４０％を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項３５記載の光検知器。
【請求項３７】
該フォトン吸収領域は、８００ｎｍ乃至９００ｎｍの波長において該入射ソース信号を５０％を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項３５記載の光検知器。
【請求項３８】
該フォトン吸収領域は、８００ｎｍ乃至９００ｎｍの波長において該入射ソース信号を６０％を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項３５記載の光検知器。
【請求項３９】
該フォトン吸収領域は、１４００ｎｍ乃至１７００ｎｍの波長において該入射ソース信号を４０％を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項３５記載の光検知器。
【請求項４０】
該フォトン吸収領域は、１４００ｎｍ乃至１７００ｎｍの波長において該入射ソース信号を５０％を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項３５記載の光検知器。
【請求項４１】
該フォトン吸収領域は、１４００ｎｍ乃至１７００ｎｍの波長において該入射ソース信号を６０％を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている請求項３５記載の光検知器。
【請求項４２】
該フォトン吸収領域は、８００ｎｍ乃至９００ｎｍのソース信号波長の少なくとも２０ｎｍの波長スパンにわたって２０％未満だけ変化する吸収百分率において該入射ソース信号を吸収する形態とされている請求項３５記載の光検知器。
【請求項４３】

該フォトン吸収領域は、１４００ｎｍ乃至１７００ｎｍのソース信号波長の少なくとも２０ｎｍの波長スパンにわたって２０％未満だけ変化する吸収百分率において該入射ソース信号を吸収する形態とされている請求項３５記載の光検知器。

【請求項４４】

各穴が該基板の上部表面に平行な断面を有しており且つ４００ｎｍと２５００ｎｍとの間の最大寸法を有しており、及び各穴は該複数個の穴の内の最も近くに隣接する穴の中心から３５００ｎｍ未満だけ離隔されている中心を有している請求項３５記載の光検知器。

【請求項４５】

前記光検知器は、更に、10^{19}／cm^3において又はそれを越えて高度にドープされており且つ前記フォトン吸収領域の側面に位置しているＰ層とＮ層とを有しており、及び該フォトン吸収領域は軽度にドープされているか又は意図的にはドープされておらず高々10^{16}／cm^3である請求項３５記載の光検知器。

【請求項４６】

前記光検知器がアバランシェ光検知器を有している請求項３５記載の光検知器。

【請求項４７】

該フォトン吸収領域がＳｉを有している請求項３５記載の光検知器。

【請求項４８】

該フォトン吸収領域がＧｅを有している請求項３５記載の光検知器。

【請求項４９】

該光検知器が、前記ソース信号を担持するオプチカルファイバーを受け付け且つ該ファイバーの一端部を前記フォトン吸収領域から選択した距離に維持する形態とされているテーパー付き又は段差付きの穴を有している請求項３５記載の光検知器。

【請求項５０】

更に、該ファイバーの前記端部と該フォトン吸収領域との間にレンズを包含している請求項４９記載の光検知器。

【請求項５１】

該光検知器が、該ソース信号の複数の反射を発生させて前記ソース信号が該フォトン吸収領域を複数回横断する形態とされている反射構造を有している請求項３５記載の光検知器。

【請求項５２】

該光検知器が、該フォトン吸収領域の２つの対応する側部から該ソース信号を受け取る形態とされている請求項３５記載の光検知器。

【請求項５３】

マイクロストラクチャ向上型光吸収を具備する光検知器において、

カソード領域、

アノード領域、

前記カソード領域が前記アノード領域よりも一層正の電圧へ駆動されるように前記カソード領域と前記アノード領域との間に電圧を印加させる形態とされている逆バイアス回路、

上部表面を持っている基板物質、及び

該カソード領域及び該アノード領域と動作上関連しており且つソース信号からのフォトンを吸収する形態とされておりシリコンから構成されているフォトン吸収領域であって、各々が該上部基板表面と平行であり４００ｎｍと２５００ｎｍとの間の最大寸法を持っている複数個の穴であって各穴が該複数個の穴の最も近い隣接した穴の中心から３５００ｎｍ未満だけ離隔されている中心を持っている該複数個の穴を有している該フォトン吸収領域、

を有している光検知器。

【請求項５４】

該ソース信号が８００ｎｍより大きく且つ１０００ｎｍより小さい波長を持っている請求項５３記載の光検知器。

Samsung Exhibit 1090, Page 107 of 786
Samsung v. W&Wsens - IPR2025-00993

【請求項５５】
該複数個の穴が周期的に離隔されているアレイに配置されている請求項５３記載の光検知器。
【請求項５６】
該周期的に離隔されているアレイが六角形又は正方形の格子パターンを有している請求項５５記載の光検知器。
【請求項５７】
該複数個の穴が、前記ソース信号の波長を含む波長範囲において、穴は無いがその他は同一である光検知器と比較してフォトンの吸収を向上させる請求項５３記載の光検知器。
【請求項５８】
該穴の各々が該上部基板表面と平行である支配的に円形状の断面を持っている請求項５３記載の光検知器。
【請求項５９】
該カソード領域及び該アノード領域が集積回路エレクトロニクスへ動作接続されており、且つ該光検知器及び該集積回路エレクトロニクスが単一のシリコンチップに集積化されている請求項５３記載の光検知器。
【請求項６０】
該集積回路エレクトロニクスが、相互インピーダンス増幅器、信号処理エレクトロニクス、及びルーチングエレクトロニクスからなるグループから選択される一つ又はそれ以上のタイプを包含している請求項５９記載の光検知器。
【請求項６１】
該光検知器と関連している容量が、そのアノード領域とカソード領域とを従来のボンドパッドへ動作接続させているその他は同一の光検知器と比較して、減少されている請求項５９記載の光検知器。
【請求項６２】
更に、シリコンから形成されている増倍領域を有しており、及び
該光検知器が，８５０ｎｍのソース信号波長において５Ｇｂ／ｓよりも大きなデータ帯域幅で該ソース信号を検知する形態とされており、且つ２より大きな利得を有しているアバランシェフォトダイオードである、請求項５３記載の光検知器。
【請求項６３】
前記光検知器が、少なくとも３０％の量子効率で、８５０ｎｍのソース信号波長において２，５Ｇｂ／ｓよりも大きなデータ帯域幅で前記ソース信号を検知する形態とされている請求項５３記載の光検知器。
【請求項６４】
前記光検知器が、少なくとも５０％の量子効率で、８５０ｎｍのソース信号波長において２，５Ｇｂ／ｓよりも大きなデータ帯域幅で前記ソース信号を検知する形態とされている請求項５３記載の光検知器。
【請求項６５】
前記光検知器が，少なくとも３０％の量子効率で、８５０ｎｍのソース信号波長において５Ｇｂ／ｓ以上のデータ帯域幅で前記ソース信号を検知する形態とされている請求項５３記載の光検知器。
【請求項６６】
前記光検知器が、少なくとも５０％の量子効率で，８５０ｎｍのソース信号波長において５Ｇｂ／ｓ以上のデータ帯域幅で前記ソース信号を検知する形態とされている請求項５３記載の光検知器。
【請求項６７】
該複数個の穴がシリコンの一部をエッチング除去することによって形成されている請求項５３記載の光検知器。
【請求項６８】
該光検知器は，該ソース信号の一部が該フォトン吸収領域を１回目に通過し、或る表面

で反射し、且つ、その後に、該光吸収領域を２回目に通過する形態とされている請求項５３記載の光検知器。

【請求項６９】

更に、基板を包含しており、及び

該カソード領域、該吸収領域、及び該アノード領域が該基板の上方に形成されており且つ該光検知器が該基板と反対の該光検知器の側部に面する方向から該ソース信号を受け取る形態とされている、請求項５３記載の光検知器。

【請求項７０】

マイクロストラクチャ向上型光吸収を具備している光検知器において、

カソード領域、

アノード領域、

前記カソード領域が前記アノード領域よりも一層正の電圧へ駆動されるように前記カソード領域と前記アノード領域との間に電圧を印加する形態とされている逆バイアス回路、

上部表面を持っている基板物質、及び

前記カソード領域及び前記アノード領域と動作上関連しており且つソース信号からのフォトンを吸収する形態とされているゲルマニウムを基礎とする物質から構成されているフォトン吸収領域であって、前記ゲルマニウムを基礎とする吸収領域は各々が該上部基板表面と平行で７５０ｎｍと３０００ｎｍとの間の最大寸法を持っている断面を有している複数個の穴を包含しており、且つ各穴は該複数個の穴の内の最も近くに隣接する穴の中心から５０００ｎｍ未満だけ離隔している中心を有している該フォトン吸収領域、

を有している光検知器。

【請求項７１】

該ゲルマニウムを基礎とするフォトン吸収層が、シリコンからなる物質の一つ又はそれ以上の層の上方に、エピタキシャル成長及びエピタキシャル横過剰成長プロセスの内の少なくとも一つによって形成されている請求項７０記載の光検知器。

【請求項７２】

更に、最上シリコン層の上にＧｅの結晶成長を開始させる形態とされているＧｅバッファ層を有している請求項７１記載の光検知器。

【請求項７３】

該アノード領域が、エピタキシャル成長及びエピタキシャル横過剰成長プロセスの内の少なくとも一つによって形成されているＰドープゲルマニウム層を有している請求項７０記載の光検知器。

【請求項７４】

前記光検知器がアバランシェフォトダイオードであり、且つ、更に、シリコンから形成されている増倍領域を有している請求項７０記載の光検知器。

【請求項７５】

該ソース信号が１２００ｎｍよりも大きく且つ１９００ｎｍより小さな波長を有している請求項７０記載の光検知器。

【請求項７６】

該ソース信号が１４００ｎｍより大きな波長を有している請求項７５記載の光検知器。

【請求項７７】

前記光検知器が、少なくとも３０％の量子効率で、１５５０ｎｍのソース信号波長において、２Ｇｂ／ｓよりも大きなデータ帯域幅において、前記ソース信号を検知する形態とされている請求項７０記載の光検知器。

【請求項７８】

前記光検知器が、少なくとも５０％の量子効率で、１５５０ｎｍのソース信号波長において、２Ｇｂ／ｓよりも大きなデータ帯域幅において、前記ソース信号を検知する形態とされている請求項７０記載の光検知器。

【請求項７９】

前記光検知器が、少なくとも３０％の量子効率で、１５５０ｎｍのソース信号波長にお

いて、５Ｇｂ／ｓよりも大きなデータ帯域幅において、前記ソース信号を検知する形態とされている請求項７０記載の光検知器。
【請求項８０】
前記光検知器が、少なくとも５０％の量子効率で、１５５０ｎｍのソース信号波長において、５Ｇｂ／ｓよりも大きなデータ帯域幅において、前記ソース信号を検知する形態とされている請求項７０記載の光検知器。
【発明の詳細な説明】
【技術分野】
【０００１】
本特許出願は以下の仮出願の各々の優先権を主張し且つ引用により本書に取り込むこととする。
【０００２】
米国仮出願番号６２／０８１，５３８号；２０１４年１１月１８日出願
米国仮出願番号６２／０９０，８７９号；２０１４年１２月１１日出願
米国仮出願番号６２／１００，０２５号；２０１５年１月５日出願
米国仮出願番号６２／１１１，５８２号；２０１５年２月３日出願
米国仮出願番号６２／１３９，５１１号；２０１５年３月２７日出願
米国仮出願番号６２／１５３，４４３号；２０１５年４月２７日出願
米国仮出願番号６２／１５４，６７５号；２０１５年４月２９日出願
米国仮出願番号６２／１５７，８７６号；２０１５年５月６日出願
米国仮出願番号６２／１７１，９１５号；２０１５年６月５日出願
米国仮出願番号６２／１７４，４９８号；２０１５年６月１１日出願
米国仮出願番号６２／１７５，８５５号；２０１５年６月１５日出願
米国仮出願番号６２／１８２，６０２号；２０１５年６月２１日出願
米国仮出願番号６２／１８８，８７６号；２０１５年７月６日出願
米国仮出願番号６２／１９７，１２０号；２０１５年７月２７日出願
米国仮出願番号６２／１９９，６０７号；２０１５年７月３１日出願
米国仮出願番号６２／２０５，７１７号；２０１５年８月１５日出願
米国仮出願番号６２／２０９，３１１号；２０１５年８月２４日出願
米国仮出願番号６２／２１３，５５６号；２０１５年９月２日出願
米国仮出願番号６２／２３２，７１６号；２０１５年９月２５日出願
本特許出願は以下の仮及び非仮出願に関連しており，その各々を引用により本書に取り込むこととする。
【０００３】
国際特許出願番号ＰＣＴ／ＵＳ１４／３９２０８；２０１４年５月２２日出願
米国仮出願番号６１／８２６，４４６号；２０１３年５月２２日出願
米国仮出願番号６１／８３４，８７３号；２０１３年６月１３日出願
米国仮出願番号６１／８４３，０２１号；２０１３年７月４日出願
米国仮出願番号６１／９０５，１０９号；２０１３年１１月１５日出願
米国仮出願番号６２／０１７，９１５号；２０１４年６月２７日出願
上に引用した仮及び非仮特許出願の全ては、本書において、「共通に譲渡され組み込まれている出願」として集約的に引用される。
【０００４】
本特許明細書は、大略，感光装置に主に関連する発明を提示する。更に詳細には、幾つかの実施例はマイクロストラクチャ向上型吸収特性を具備している感光装置に関連している。
【背景技術】
【０００５】
オプチカルファイバー通信は、遠隔通信及び大型データセンター内の通信等の適用例において広く使用されている。一層短い光学的波長を使用した場合に関連する減衰損失のた

めに、殆どのオプチカルファイバー通信は８００ｎｍ以上の光学的波長を使用している。一般的に使用される通信窓が８００ｎｍと１６７５ｎｍとの間に存在している。オプチカルファイバー通信システムにおいて使用される光学的受信機の主要な部品は光検知器であって、それは、通常、フォトダイオード（ＰＤ）又はアバランシェフォトダイオード（ＡＰＤ）の形態である。

【０００６】

高品質で低ノイズのＡＰＤはシリコンから構成することが可能である。しかしながら、シリコンは可視光及び近赤外範囲における光を吸収するが、それは一層長い光学的波長において一層透明性となる。シリコンＰＤ及びＡＰＤは、該装置の吸収「Ｉ」領域の厚さを増加させることによって８００ｎｍ以上の光学的波長用とさせることが可能である。しかしながら、適切な量子効率を得るためには、シリコン「Ｉ」領域の厚さが、該装置の最大帯域幅が多くの現在の及び将来の遠隔通信及びデータセンター適用例に対して低すぎるものとなるほど非常に大きくなる。

【０００７】

一層長い波長及び一層高い帯域幅の場合にシリコンＰＤ及びＡＰＤが有している本来的な問題を回避するために、その他の物質が使用される。ゲルマニウム（Ｇｅ）は１７００ｎｍの波長まで赤外を検知するが、比較的高い増倍ノイズ（multiplication noise）を有している。ＩｎＧａＡｓは１６００ｎｍよりも一層長いものまで検知することが可能であり且つＧｅよりも増倍ノイズは少ないが、シリコンよりもかなり一層大きな増倍ノイズを有している。ＩｎＧａＡｓは、最も典型的には基板として且つ増倍層としてＩｎＰが関与するヘテロ構造ダイオードの吸収領域として使用されることが知られている。この物質系は略９００乃至１７００ｎｍの吸収窓と適合性がある。しかしながら、両方のＩｎＧａＡｓ装置は比較的高価であると共にシリコンと比較した場合に比較的高い増倍ノイズを有しており、且つ単一チップとしてＳｉエレクトロニクスと集積化させることは困難である。

【０００８】

光検知器の事業における主要な会社によって公表されている情報（http://files.shareholder.com/downloads/FNSR/0x0x382377/0b3893ea-fb06-417d-ac71-84f2f9084b0d/Finisar Investor Presentation.pdf参照）が１０頁において示していることは、光学的通信装置用の現在の市場は７０億米国ドルを越えており複合年成長率は１２％であることです。８５０ｎｍ波長用に使用されているフォトダイオード（ＰＤ）はＧａＡｓ物質を使用しており、且つ１５５０ｎｍ波長用には、フォトダイオードはＩｎＰ物質をベースとしており、それは高価であると共にＳｉをベースとしたエレクトロニクスと集積化させることは困難である。従って、そこには大きな市場があり且つより良い装置の開発が満たされていない長きに亘る必要性が存在している。今日までのところ、８５０ｎｍ用のＳｉ物質をベースとしたフォトダイオードもアバランシェフォトダイオード（ＡＰＤ）も存在しておらず、且つ上部又は底部照射型でデータレートが５Ｇｂ／ｓ以上であり、本発明者等の知るところによれば市販されている１５５０ｎｍ用のＧｅ・オン・Ｓｉ（Ge on Si）物質をベースとしたフォトダイオードもアバランシェフォトダイオードも存在しない。しかしながら、この様な大きな市場に対してより良い装置を開発しようとする努力が欠如していたわけでもない。例えば、Ｓｉ物質内に製造される共振フォトダイオードに対する提案がなされている（エピタキシャル横過剰成長によって成長された共振キャビティ向上型高速Ｓｉフォトダイオード（Resonant Cavity Enhanced High-Speed Si Photodiodes Grown by Epitaxial Lateral Overgrowth）、Schaub et al.、ＩＥＥＥフォトニクステクノロジーレターズ、１１巻、Ｎｏ．１２、１９９９年１２月）が、それは該市場で認知されるようになったものではない。導波路形態におけるその他の形式の高速フォトダイオードが提案されており、例えば、基準４０ＧＨｚＳｉ／Ｇｅ単一走行キャリア導波路フォトダイオード（Ref. 40 GHz Si/Ge uni-travelling carrier waveguide photodiode）、Piels et al.、ＤＯＩ　１０．１１０９／ＪＬＴ．２０１４．２３１０７８０、ジャーナル・オブ・ライトウエーブ・テクノロジー；モノリシックＧｅ／Ｓｉアバランシェフォトダイオード（Monoli

Samsung Exhibit 1090, Page 111 of 786
Samsung v. W&Wsens - IPR2025-00993

thic Ge/Si Avalanche Photodiodes）、Kang et al.、９７８－１－４２４４－４４０３－８／０９／＄２５．００　著作権２００９ＩＥＥＥ：大断面シリコン・オン・インシュレータ導波路とモノリシックに集積化された高速Ｇｅ光検知器（High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide）、Feng et al.、アプライドフィジックスレターズ９５、２６１１０５（２００９）：doi：１０．１０６３／１．３２７９１２９；におけるものがあり、その場合に、光は端部から光学的導波路内に結合され且つ吸収長は１５５０ｎｍにおけるＧｅの弱い吸収係数を補償するために１００μｍ以上とさせることが可能である。これらの以前に提案されている導波路フォトダイオード構造においては、光は導波路の長さに沿って伝播し且つ光の伝播方向と電界の方向とが支配的に垂直であるようにＰＩＮ導波路を横断して電界が印加される。Ｓｉ内において光は電子／正孔の飽和速度よりも約１０００倍一層速く進行するので、導波路ＰＤは、例えば、２００ミクロンの長さとし且つＰＩＮにおける「Ｉ」は、例えば、２ミクロンとすることが可能であり、且つ１０Ｇｂ／ｓを越える帯域幅を達成することが可能である。この様な光の端部結合は、この特許明細書に記載されるような表面照射と比較してパッケージングにおいてコスト高であり、その場合に、導波路断面の寸法は典型的に数ミクロンであるのと対比して既知の表面照射型フォトダイオード又はアバランシェフォトダイオードの場合には数十ミクロンである。既知の導波路ＰＤ／ＡＰＤは、しばしば、単一モード光学系であるに過ぎず、一方、本特許明細書に記載される表面照射型ＰＤ／ＡＰＤは単一及びマルチモードの両方の光学系で使用することが可能である。更に、既知の導波路フォトダイオードはウエハレベルにおいてテストすることが困難であるが、一方、本特許明細書に記載される表面照射型フォトダイオードはウエハレベルにおいて容易にテストすることが可能である。既知の導波路フォトダイオード／アバランシェフォトダイオードは、殆どが、特別のフォトニック回路において使用されるものであって広く市場で入手可能なものではない。Ｓｉと集積化させることが可能な上部又は底部照射型のＳｉ及びＧｅ・オン・ＳｉのＰＤ／ＡＰＤは、８５０ｎｍ及び１５５０ｎｍの波長において５Ｇｂ／ｓ又はそれ以上のデータレートのものが市販されていることは不知である。対照的に、この特許明細書に記載されている如くＳｉをベースとした物質上のフォトダイオードは、単一Ｓｉチップ上の集積化電子回路とモノリシックに集積化させることが可能であり、その際にパッケージングのコストを著しく減少させる。更に、本特許明細書に記載される８５０ｎｍの公称波長におけるマイクロストラクチャ型ＰＤ／ＡＰＤは支配的に短距離用のものとすることが可能であり、例えば、１メートル未満、及び或る場合には１０メートル未満、及び或る場合には１００メートル未満、及び或る場合には１０００メートル未満の光学的データ伝送の距離とすることが可能である。入射光学ビームのマイクロストラクチャ型ＰＤ／ＡＰＤ方向及びＰＩＮ又はＮＩＰ構造の「Ｉ」領域における電界は支配的に共線状であるか及び／又は略共線状である。この特許明細書はこの様な装置を可能なものとさせ且つ現在のデータセンターをブレード間において及び／又は１個のブレード内において殆ど全てを光学的データ伝送へ変換させるものと予測され、そのことはデータ伝送帯域幅能力を著しく増加させると共に電力消費を著しく減少させるものである。

【０００９】

本書の特許請求の範囲に記載される要旨はいずれか特定の欠点を解消する実施例又は上述したような環境においてのみ動作する実施例に限定されるものではない。そうではなく、この背景は、本書に記載される幾つかの実施例を実施することが可能な一つの例示的な技術分野を例示するために与えれているものである。

【先行技術文献】

【非特許文献】

【００１０】

【非特許文献１】エピタキシャル横過剰成長によって成長された共振キャビティ向上型高速Ｓｉフォトダイオード（Resonant Cavity Enhanced High-Speed Si Photodiodes Grown by Epitaxial Lateral Overgrowth）、Schaub et al.、ＩＥＥＥフォトニクステクノロ

Samsung Exhibit 1090, Page 112 of 786
Samsung v. W&Wsens - IPR2025-00993

ジーレターズ、１１巻、Ｎｏ．１２、１９９９年１２月
【非特許文献２】基準４０ＧＨｚＳｉ／Ｇｅ単一走行キャリア導波路フォトダイオード（Ref. 40 GHz Si/Ge uni-travelling carrier waveguide photodiode）、Piels et al.、ＤＯＩ　１０．１１０９／ＪＬＴ．２０１４．２３１０７８０、ジャーナル・オブ・ライトウエーブ・テクノロジー
【非特許文献３】モノリシックＧｅ／ＳｉアバランシェフォトダイオードMonolithic Ge/Si Avalanche Photodiodes）、Kang et al.、９７８－１－４２４４－４４０３－８／０９／＄２５．００　著作権２００９ＩＥＥＥ
【非特許文献４】大断面シリコン・オン・インシュレータ導波路とモノリシックに集積化された高速Ｇｅ光検知器（High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide）、Feng et al.、アプライドフィジックスレターズ９５、２６１１０５（２００９）
【非特許文献５】doi：１０．１０６３／１．３２７９１２９
【発明の概要】
【発明が解決しようとする課題】
【００１１】
幾つかの実施例によれば、データ通信用の集積化検知器／プロセッサ回路が、マイクロストラクチャ向上型光吸収を具備する光検知器、及び単一の半導体チップに形成されている電子的プロセッサを有している。
【課題を解決するための手段】
【００１２】
該単一チップには，データ通信用に変調された光学的ソース信号からのフォトンを吸収し且つそれに対応する出力電気信号を供給する形態とされているフォトン吸収領域を具備している半導体基板上に形成されている光検知器が設けられており，該フォトン吸収領域は前記基板へ向かってその中を延在している複数個の穴であって該穴の複数において該同一のソース信号を同時的に受け取る形態とされている該複数個の穴を有しており、電子的プロセッサも前記半導体基板上に形成されていて前記フォトン吸収領域と動作上関連していて前記出力電気信号を受け取ってそれを処理済出力へ処理し、それにより該光学的ソース信号を受け取り且つ該処理済出力を出力する単一の半導体チップを形成しており、前記フォトン吸収領域及び前記電子的プロセッサは同じ大きさの程度の夫々の厚さを有しており、且つカソード領域とアノード領域とが前記フォトン吸収領域及び逆バイアス回路と動作上関連しており、該逆バイアス回路は前記カソード領域が前記アノード領域よりも一層正の電圧へ駆動されるように前記カソード領域とアノード領域との間に電圧を印加させる形態とされている。
【００１３】
該フォトン吸収領域の厚さは、好適には、０．５乃至５μｍの範囲内である。該電子的プロセッサは、相補的金属酸化物半導体（ＣＭＯＳ）装置、バイポーラ（ＢＩ）装置、及びＢｉＣＭＯＳ装置の内の少なくとも一つを有している応用特定集積回路（ＡＳＩＣ）とすることが可能である。該フォトン吸収領域は、８００ｎｍ乃至９００ｎｍ、又は１４００ｎｍ乃至１７００ｎｍの波長において入射ソース信号の４０％、又は５０％、又は６０％を越えて吸収し、且つそれに対応する出力電気信号を供給する形態とさせることが可能である。該フォトン吸収領域は、８００ｎｍ乃至９００ｎｍ、又は１４００ｎｍ乃至１７００ｎｍのソース信号波長の少なくとも２０ｎｍの選択した波長範囲に亘って２０％未満だけ変動する吸収百分率において該入射ソース信号を供給する形態とさせることが可能である。
【００１４】
各穴は、４００ｎｍと２５００ｎｍとの間の最大寸法を有しており該基板の表面に対して平行な断面を有することが可能であり、且つ各穴は該複数個の穴の内の最も近い隣接する穴の中心から３５００ｎｍ未満だけ離隔されている中心を有することが可能である。該光検知器は、好適には、更に、10^{19}／ｃｍ^{3}において又はそれを越えて高度にドープ

されており且つ前記フォトン吸収領域の側面に位置しているＰ層及びＮ層を有しており、且つ該フォトン吸収領域は、好適には、軽度にドープされているか又は意図的にドープされておらず高々１０^{16}／ｃｍ^{3}である。該光検知器はアバランシェ光検知器を有することが可能であり、且つ該フォトン吸収領域はＳｉ及びＧｅの内の少なくとも一つを有することが可能である。該光検知器は、前記ソース信号を担持するオプチカルファイバーを受け付け且つ該ファイバーの端部を前記フォトン吸収領域から選択した距離に維持する形態とされているテーパー付き又は段差付きの穴を有することが可能である。該ファイバーの前記端部と該フォトン吸収領域との間にレンズを包含させることが可能である。該光検知器は、更に、該ソース信号の多数回の反射を発生させそれにより前記ソース信号を該フォトン吸収領域を多数回横断させる形態とされている反射構造を有することが可能である。該光検知器は該フォトン吸収領域の２つの反対側から該ソース信号を受け取る形態とさせることが可能であり、且つ前記穴は、該穴の複数のグループにおいて光を電気信号へ変換させる場合の結合共振を発生させてそれによりソース信号吸収を向上させる形態とさせることが可能である。

【００１５】

１個又はそれ以上の付加的な光検知器を前記半導体基板上に形成することが可能であり、それは夫々の付加的なソース信号を受け取り且つそれに対応する夫々の出力電気信号を供給する夫々のフォトン吸収領域を具備しており、又、１個又はそれ以上の付加的な電子的プロセッサを前記半導体基板上に形成し且つ前記夫々の出力電気信号をそれから受け取り且つ処理するために前記付加的な光検知器の夫々のフォトン吸収領域と動作上関連させることも可能である。該複数個の穴は、前記ソース信号の波長を含む複数の波長の範囲において穴が無いがその他は同一の光検知器と比較してフォトンの吸収を向上させる形態とさせることが可能である。該電子的プロセッサは、相互インピーダンス増幅器、信号処理エレクトロニクス、及びルーチングエレクトロニクスからなるグループから選択した１個又はそれ以上のタイプを包含することが可能である。該光検知器と関連する容量は、アノード領域及びカソード領域を従来のボンドパッドへ動作上接続させているその他は同一の光検知器と比較して減少されている。該光検知器は、更に、増倍領域を有することが可能であり、それはアバランシェフォトダイオードをして８００乃至９００ｎｍのソース信号波長において１０ギガビット／ｓよりも大きなデータ帯域幅で該ソース信号を検知する形態とさせ、且つ２よりも大きな利得を具備している。

【００１６】

幾つかの実施例においては、光学的／電子的システムにおいて、光検知器とアクティブ電子回路とが設けられており、それらは同一の半導体基板上に構築されており且つ互いに動作上関連付けられていて単一の集積回路チップを形成しており、Ｇｂ／ｓレートでの情報を担持する該光学的ソース信号を発生させるためにデータのＧｂ／ｓレートで変調されるレーザが設けられており、且つその入力端において該光学的ソース信号を受け取り且つそれをその出力端へ送るために該レーザと関連してオプチカルファイバーが設けられており、その場合に、該光検知器は該光学的ソース信号を受け取るために該オプチカルファイバーの該出力端と関連しており且つそれを電気的出力信号へ変換させる形態とされており、且つ該アクティブ電子回路は該出力電気信号を受け取るために該光検知器と関連しており且つ該電気出力信号を処理し且つ前記処理済の電気信号を出力する形態とされている。該ソース信号及び該電気的出力信号の各々は少なくとも５Ｇｂ／ｓのレートで変調させることが可能である。該光検知器及び該アクティブ電子回路は同じ程度の大きさの厚さを有することが可能である。該光検知器は、該半導体基板へ向かって延在している複数個の穴を包含しているフォトン吸収領域を有することが可能であり、その場合に、複数の穴が同一のソース信号を同時的に受け取る形態とされている。高度にドープしたＰ層及びＮ層が該フォトン吸収領域の側面に位置することが可能であり、且つ該フォトン吸収領域は０．１乃至５．０μｍの範囲内の厚さを有することが可能であり且つ、好適には、意図的にはドープされていないか又はＰ領域及びＮ領域と比較して軽度にドープされている。該光検知器は、該光検知器によって該ソース信号が受け取られる方向に沿う方向において電子又

Samsung Exhibit 1090, Page 114 of 786
Samsung v. W&Wsens - IPR2025-00993

は正孔を誘引させるべくバイアスさせることが可能である。該光検知器及び該アクティブ電子回路の各々はシリコンをベースとしたものとすることが可能である。該光検知器はアバランシェ光検知器とすることが可能である。

【００１７】

幾つかの実施例において、マイクロストラクチャ向上型光吸収を具備している光検知器が、好適には０．５μｍと５μｍとの間の厚さを具備しており且つデータ通信用に変調されたソース信号からフォトンを吸収し且つそれに対応する出力電気信号を供給する形態とされているフォトン吸収領域を有しており、前記フォトン吸収領域は該フォトン吸収領域の厚さの少なくとも一部を介して延在している複数個の穴であって該穴の複数において同一のソース信号を同時的に受け取る形態とされている該複数個の穴を有しており、且つ前記フォトン吸収領域は８００ｎｍ乃至９００ｎｍ及び１４００ｎｍ乃至１７００ｎｍの範囲の内の少なくも一つにおける波長において入射ソース信号の４０％を超えて吸収し且つそれに対応する出力電気信号を供給する形態とされている。該フォトン吸収領域は、８００ｎｍ乃至９００ｎｍ又は１４００ｎｍ乃至１７００ｎｍのソース信号波長の少なくとも２０ｎｍの波長範囲に亘り２０％未満だけ変化する吸収百分率において入射ソース信号を吸収する形態とさせることが可能である。

【００１８】

各穴は、好適には、４００ｎｍと２５００ｎｍとの間の最大寸法を有する該基板の上部表面と平行な断面を有しており、且つ各穴は、好適には、該複数個の穴の内の最も近くに隣接する穴の中心から３５００ｎｍ未満だけ離隔されている中心を有している。該光検知器は、更に、Ｐ層及びＮ層を有しており、それらは、好適には、10^{19}／cm^3での又はそれを越えて高度にドープされており且つ前記フォトン吸収領域の側面に位置しており、且つ該フォトン吸収領域は、好適には、意図的にはドープされていないか又は高々10^{16}／cm^3で軽度にドープされている。該光検知器はアバランシェ光検知器を有することが可能である。該フォトン吸収領域はＳｉ又はＧｅを有することが可能である。該光検知器は、前記ソース信号を担持しているオプチカルファイバーを受け付け且つ該ファイバーの端部を前記フォトン吸収領域から選択された距離に維持する形態とされているテーパー付き又は段差付きの穴を有することが可能であり、且つ該ファイバーの前記端部と該フォトン吸収領域との間にレンズを包含させることが可能である。該光検知器は、該ソース信号の多数回の反射を発生させそれにより該フォトン吸収領域を前記ソース信号で多数回横断させる形態とされている反射構造を有することが可能である。該光検知器は、該フォトン吸収領域の２つの反対側の側部から該ソース信号を受け取る形態とさせることが可能である。

【００１９】

幾つかの実施例において，マイクロストラクチャ向上型光吸収を具備する光検知器は，カソード領域、アノード領域、前記カソード領域が前記アノード領域よりも一層正の電圧へ駆動されるように前記カソード領域と前記アノード領域との間に電圧を印加する形態とされている逆バイアス回路、上部表面を具備している基板物質、及び該カソード領域とアノード領域とに動作上関連しており且つソース信号からフォトンを吸収する形態とされておりシリコンから構成されているフォトン吸収領域、を有しており，前記シリコン吸収領域は各々が４００ｎｍと２５００ｎｍとの間の最大寸法を持っている該上部基板表面と平行な断面を持っている複数個の穴を包含しており、且つ各穴は該複数個の穴の内の最も近くに隣接する穴の中心から３５００ｎｍ未満だけ離隔されている。該ソース信号は８００ｎｍよりも大きく且つ１０００ｎｍよりも小さい波長を有することが可能である。該複数個の穴は、六角形又は正方形の格子パターンを有することが可能な周期的に離隔されたアレイに配列させることが可能である。該複数個の穴は、穴の無いものと比較してフォトンの吸収を向上させるが，その他は、前記ソース信号の波長を含む波長の範囲において同じ光検知器である。該穴の各々は該上部基板表面と平行な支配的に円形状の断面を有することが可能である。該カソード領域及びアノード領域は集積回路エレクトロニクスへ動作接続させることが可能であり、且つ該光検知器及び集積回路エレクトロニクスは単一のシリ

コンチップに集積化させることが可能であり、その場合に、該集積回路エレクトロニクスは相互インピーダンス増幅器、信号処理エレクトロニクス、及びルーチングエレクトロニクスからなるグループから選択される一つ又はそれ以上のタイプを包含することが可能である。該光検知器と関連する容量は、そのアノード領域とカソード領域とを従来のボンドパッドへ動作接続させているその他は同じ光検知器と比較して、減少させることが可能である。該光検知器は、更に、シリコンから形成される増倍領域を有することが可能であり、その場合に、該光検知器は、２より大きいな利得を持っており、８５０ｎｍのソース信号波長において５Ｇｂ／ｓよりも大きなデータ帯域幅において該ソース信号を検知する形態とされているアバランシェフォトダイオードである。該光検知器は、量子効率が少なくとも３０％又は５０％で８５０ｎｍのソース信号波長において２，５Ｇｂ／ｓ以上か又は５Ｇｂ／ｓ以上のデータ帯域幅において前記ソース信号を検知する形態とさせることが可能である。該複数個の穴はシリコンの一部をエッチング除去することによって形成させることが可能である。該光検知器は、該ソース信号の一部が最初に該フォトン吸収領域を通過し、表面から反射し、その後に該フォトン吸収領域を再度通過するような形態とさせることが可能である。該光検知器は、更に、基板を包含することが可能であり、その場合に、該カソード、吸収及びアノード領域は該基板の上方に形成し且つ該光検知器は該基板と反対側の該光検知器の側部に面する方向から該ソース信号を受け取る形態とされる。

【００２０】

幾つかの実施例においては、マイクロストラクチャ向上型光吸収を具備する光検知器は、カソード領域、アノード領域、前記カソード領域が前記アノード領域よりも一層正の電圧へ駆動されるように前記カソード領域とアノード領域との間に電圧を印加する形態とされている逆バイアス回路、上部表面を具備している基板物質、及び該カソード領域及びアノード領域と動作上関連しており且つソース信号からのフォトンを吸収する形態とされておりゲルマニウムをベースとした物質から構成されているフォトン吸収領域、を有しており、前記ゲルマニウムをベースとした吸収領域は各々が７５０ｎｍと３０００ｎｍとの間の最大寸法を持っており該上部基板表面と平行な断面を持っている複数個の穴を包含しており、且つ各穴は該複数個の穴の内の最も近くに隣接する穴の中心から５０００ｎｍ未満だけ離隔されている中心を有している。該ゲルマニウムをベースとしたフォトン吸収層は、シリコンからなる物質の一つ又はそれ以上の層の上にエピタキシャル成長及びエピタキシャル横方向過剰成長（epitaxial lateral overgrowth）プロセスの内の少なくとも一つによって形成させることが可能である。該光検知器は、更に、最上シリコン層の上にＧｅの結晶成長を開始させる形態とされたＧｅバッファー層を有することが可能である。該光検知器のアノード領域は、エピタキシャル成長及びエピタキシャル横方向過剰成長プロセスの内の少なくとも一つによって形成されるＰドープゲルマニウム層を有することが可能である。該光検知器はアバランシェフォトダイオードとすることが可能であり、且つ、更に、シリコンから形成される増倍領域を有することが可能である。該ソース信号は、１２００ｎｍよりも大きく且つ１９００ｎｍよりも小さいか、又は１４００ｎｍよりも大きな波長を有することが可能である。該光検知器は、量子効率が少なくとも３０％か又は５０％で１５５０ｎｍのソース信号波長において２Ｇｂ／ｓ又は５Ｇｂ／ｓよりも大きなデータ帯域幅において前記ソース信号を検知する形態とさせることが可能である。

【００２１】

本書において使用されているように、「及び（and）」、「又は（or）」、及び「及び／又は（and/or）」等の文法上の接続詞は、全て、それらが接続する事例、客体、主体の内の一つ又はそれ以上が発生するか又は存在している場合があることを表すことを意図している。この様に、本書において使用されているように、全ての場合においての用語「又は（or）」は「排他的又は（exclusive or）」の意味ではなく「包括的又は（inclusive or）」の意味を表している。

【００２２】

本書において使用されているように、「１個の穴（hole）」又は「複数の穴（holes）」という用語は一つの物質又は複数の物質の中へ又は貫通している何らかの開口のことを

意味している。一般的に、該開口は、円形、楕円、多角形、及びランダム形状を含む任意の形状及び断面を有することが可能である。

【００２３】

この特許明細書の要旨の上述した及びその他の利点及び特徴を更に明確にさせるために、その実施形態の特定の例を添付図面に例示してある。理解すべきことであるが、これらの図面は単に例示的実施例を図示するに過ぎず、従ってこの特許明細書又は特許請求の範囲を制限するものと考えるべきものではない。本書の要旨を添付図面の使用を介して付加的な特定性及び詳細と共に記載し且つ説明する。

【図面の簡単な説明】

【００２４】

【図１】幾つかの実施例に基づいてマイクロストラクチャ型フォトダイオード／アバランシェフォトダイオードを使用することが可能な光学的データ伝送システムを例示している概略図。

【図２】幾つかの実施例に基づいてマイクロストラクチャ型フォトダイオード（ＭＳ－ＰＤ）及びマイクロストラクチャ型アバランシェフォトダイオード（ＭＳ－ＡＰＤ）と共に包含される波長選択要素を示している概略図。

【図３】幾つかの実施例に基づいてマルチ波長選択要素を具備しているＭＳ－ＰＤ／ＡＰＤを示している概略図。

【図４】（Ａ）乃至（Ｄ）は幾つかの実施例に基づく種々のバンドパスフィルター特性を示している各プロット。

【図５】幾つかの実施例に基づく粗波長分割多重（ＣＷＤＭ）形態を示している概略図。

【図６】（Ａ）及び（Ｂ）は幾つかの実施例に基づくマイクロストラクチャ型フォトダイオードの幾つかの基本的な部分を示している各概略図。

【図７】（Ａ）及び（Ｂ）は幾つかの実施例に基づく底部照射型フォトダイオードの幾つかの基本的な部分を示している各概略図。

【図８】（Ａ）及び（Ｂ）は幾つかの実施例に基づくＭＳ－ＡＰＤ構造の幾つかの基本的な部分を示している各概略図。

【図９】（Ａ）及び（Ｂ）は幾つかの実施例に基づくＩＩＩ－Ｖ又はＧｅのＳＡＧ前後の選択的区域成長（ＳＡＧ）ＡＰＤ構造の側面を示している各概略図。

【図１０】幾つかの実施例に基づくＰＩＮエピタキシャル層を具備する簡単化したマイクロストラクチャ型シリコンフォトダイオードを示している概略図。

【図１１】幾つかの実施例に基づくＰＩＮエピタキシャル層を具備する簡単化したマイクロストラクチャ型シリコンフォトダイオードを示している概略図。

【図１２】（Ａ）乃至（Ｃ）は幾つかの実施例に基づくＰＩＮエピタキシャル層を具備する簡単化したマイクロストラクチャ型シリコンフォトダイオードを示している各概略図。

【図１３】幾つかの実施例に基づくＰ－Ｉ－Ｎドーピングを具備する高コントラストマイクロストラクチャ型フォトダイオード（ＰＤ）に対するエピタキシャル層構造を示している概略図。

【図１４】幾つかの実施例に基づくＰ－Ｉ－Ｎドーピングを具備する高コントラストマイクロストラクチャ型フォトダイオード（ＰＤ）に対するエピタキシャル層構造を示している概略図。

【図１５】幾つかの実施例に基づくＰ－Ｉ－Ｎドーピングを具備する高コントラストマイクロストラクチャ型フォトダイオード（ＰＤ）に対するエピタキシャル層構造を示している概略図。

【図１６】幾つかの実施例に基づく高コントラストマイクロストラクチャ型フォトダイオード（ＰＤ）の製造の幾つかの側面を示している概略図。

【図１７】（Ａ）乃至（Ｄ）は幾つかの実施例に基づく穴配列、間隔、寸法、及びパッシベーション層の例を示している各概略図。

【図１８】幾つかの実施例に基づく高コントラストマイクロストラクチャ型フォトダイオード（ＰＤ）の製造の幾つかの更なる側面を示している概略図。

Samsung Exhibit 1090, Page 117 of 786
Samsung v. W&Wsens - IPR2025-00993

【図１９】幾つかの実施例に基づく高コントラストマイクロストラクチャ型フォトダイオード（ＰＤ）の製造の幾つかの更なる側面を示している概略図。
【図２０】幾つかの実施例に基づく高コントラストマイクロストラクチャ型フォトダイオード（ＰＤ）の製造の幾つかの更なる側面を示している概略図。
【図２１】幾つかのその他の実施例に基づく高コントラストマイクロストラクチャ型フォトダイオード（ＰＤ）の製造の幾つかの側面を示している概略図。
【図２２】（Ａ）及び（Ｂ）は幾つかの実施例に基づく特定のマイクロストラクチャ型ＰＤのシミュレーションの側面を示している各概略図。
【図２３】幾つかの実施例に基づく高コントラストマイクロストラクチャ型ＰＤの或る側面を示している概略図。
【図２４】幾つかの実施例に基づくヘテロエピタキシャルマイクロストラクチャ型ＰＤの或る側面を示している概略図。
【図２５】幾つかの実施例に基づく発光ダイオード（ＬＥＤ）又は垂直表面発光レーザ（ＶＣＳＥＬ）等の光学的発光器用の高コントラスト構造を示している概略図。
【図２６】幾つかの実施例に基づく、例えば、高コントラスト１．３ミクロン波長フォトエミッタ（photo emitter）用の基本構造を示している概略図。
【図２７】幾つかの実施例に基づいてエッチング形成した穴を具備する高コントラストマイクロストラクチャ型フォトエミッタ（ＰＥ）の幾つかの基本的な特徴を示している概略図。
【図２８】幾つかのその他の実施例に基づくＰＥの幾つかの側面を示している概略図。
【図２９】幾つかのその他の実施例に基づくＰＥの幾つかの側面を示している概略図。
【図３０】幾つかのその他の実施例に基づくＰＥの幾つかの側面を示している概略図。
【図３１】幾つかの実施例に基づくシンプルＰＩＮフォトダイオード構造の幾つかの側面を示している概略図。
【図３２】幾つかの実施例に基づくＭＳ－ＰＤ製造の或る側面を示している概略図。
【図３３】幾つかの実施例に基づくＭＳ－ＰＤ製造の或る側面を示している概略図。
【図３４】幾つかの実施例に基づくＭＳ－ＰＤ製造の或る側面を示している概略図。
【図３５】幾つかの実施例に基づくＭＳ－ＰＤ製造の或る側面を示している概略図。
【図３６】幾つかの実施例に基づくＭＳ－ＰＤ製造の或る側面を示している概略図。
【図３７】幾つかのその他の実施例に基づいて少数キャリアーライフタイムを減少させるための一つの技術を示している概略図。
【図３８】（Ａ）乃至（Ｃ）はシミュレーションした幾つかのマイクロストラクチャ型フォトダイオードに対する種々のパラメータを示している各説明図。
【図３９】マイクロストラクチャ型穴フォトダイオードのシミュレーション結果をプロットしたグラフ。
【図４０】幾つかの実施例に基づくＰ－Ｉ－Ｐ－Ｉ－Ｎエピタキシャル構造を具備するマイクロストラクチャ型アバランシェフォトダイオード（ＡＰＤ）を示している概略図。
【図４１】幾つかのその他の実施例に基づくＰ－Ｉ－Ｐ－Ｉ－Ｎエピタキシャル構造を具備するマイクロストラクチャ型アバランシェフォトダイオード（ＡＰＤ）を示している概略図。
【図４２】幾つかの実施例に基づくＧｅ吸収層及びＧｅＰキャッピング層を具備しているマイクロストラクチャ型ＡＰＤを示している概略図。
【図４３】（Ａ）乃至（Ｄ）は幾つかの実施例に基づくマイクロストラクチャ型フォトダイオード及びＡＰＤの分極（偏光）感度を示した各説明図。
【図４４】幾つかの実施例に基づいて相互インピーダンス増幅器及び／又はその他のＡＳＩＣ（応用特定集積回路）と集積化されているＭＳ－ＰＤ／ＡＰＤを示している概略図。
【図４５】幾つかの実施例に基づいて単一シリコンチップ上にＴＩＡ及び／又はその他の信号処理ＩＣを集積化させたＭＳ－ＰＤ／ＡＰＤ用のフリップチップ配置の幾つかの側面を示している概略図。
【図４６】幾つかのその他の実施例に基づいて単一シリコンチップ上にＴＩＡ及び／又は

Samsung Exhibit 1090, Page 118 of 786
Samsung v. W&Wsens - IPR2025-00993

その他の信号処理ＩＣを集積化させたＭＳ－ＰＤ／ＡＰＤ用のフリップチップ配置の幾つかの側面を示している概略図。
【図４７】幾つかのその他の実施例に基づいて単一シリコンチップ上にＴＩＡ及び／又はその他の信号処理ＩＣを集積化させたＭＳ－ＰＤ／ＡＰＤ用のフリップチップ配置の幾つかの側面を示している概略図。
【図４８】幾つかのその他の実施例に基づいて単一シリコンチップ上にＴＩＡ及び／又はその他の信号処理ＩＣを集積化させたＭＳ－ＰＤ／ＡＰＤ用のフリップチップ配置の幾つかの側面を示している概略図。
【図４９】幾つかのその他の実施例に基づいて単一シリコンチップ上にＴＩＡ及び／又はその他の信号処理ＩＣを集積化させたＭＳ－ＰＤ／ＡＰＤ用のフリップチップ配置の幾つかの側面を示している概略図。
【図５０】幾つかのその他の実施例に基づいて単一シリコンチップ上にＴＩＡ及び／又はその他の信号処理ＩＣを集積化させたＭＳ－ＰＤ／ＡＰＤ用のフリップチップ配置の幾つかの側面を示している概略図。
【図５１】幾つかのその他の実施例に基づいて単一シリコンチップ上にＴＩＡ及び／又はその他の信号処理ＩＣを集積化させたＭＳ－ＰＤ／ＡＰＤ用のフリップチップ配置の幾つかの側面を示している概略図。
【図５２】幾つかの実施例に基づいて単一シリコンチップ上にＴＩＡ及び／又はその他の信号処理及びルーチングエレクトロニクスなどのＩＣエレクトロニクスと集積化させたＭＳ－ＰＤ／ＡＰＤのアレイを示している概略図。
【図５３】幾つかの実施例に基づく高データレートＭＳ－ＰＤ用のエピタキシャル構造を示している概略図。
【図５４】幾つかの実施例に基づく高データレートＭＳ－ＰＤ用のエピタキシャル構造を示している概略図。
【図５５】幾つかの実施例に基づく高データレートＭＳ－ＰＤ用のエピタキシャル構造を示している概略図。
【図５６】幾つかの実施例に基づくＭＳ－ＰＤ用のメサ寸法、穴直径、穴周期距離、及び格子パターンを示している表。
【図５７】（Ａ）及び（Ｂ）は幾つかの実施例に基づく六角形及び正方形の格子穴パターンを示している各概略図。
【図５８】幾つかの実施例に基づくシリコンＭＳ－ＰＤ用のエピタキシャル層構造を示している概略図。
【図５９】幾つかの実施例に基づくＭＳ－ＰＤの或る側面を示している概略図。
【図６０】幾つかの実施例に基づくＭＳ－ＰＤの或る側面を示している概略図。
【図６１】幾つかの実施例に基づくＭＳ－ＰＤの或る側面を示している概略図。
【図６２】幾つかの実施例に基づくＭＳ－ＰＤ用のＧｅ・オン・ＳｉのＰＩＮエピタキシャル層構造を示している概略図。
【図６３】幾つかの実施例に基づくＧｅ・オン・ＳｉのＭＳ－ＰＤの或る側面を示している概略図。
【図６４】幾つかの実施例に基づくＧｅ・オン・ＳｉのＭＳ－ＰＤの或る側面を示している概略図。
【図６５】幾つかの実施例に基づくＧｅ・オン・ＳｉのＭＳ－ＰＤの或る側面を示している概略図。
【図６６】幾つかの実施例に基づくＧｅ・オン・ＳｉのＰＤの或る側面を示している概略図。
【図６７】幾つかの実施例に基づくＧｅ・オン・ＳｉのＰＤの或る側面を示している概略図。
【図６８】幾つかの実施例に基づくＭＳ－ＡＰＤの或る側面を示している概略図。
【図６９】幾つかの実施例に基づくＭＳ－ＡＰＤの或る側面を示している概略図。
【図７０】幾つかの実施例に基づくＳｉＯ$_2$層無しのＭＳ－ＡＰＤを示している概略図。

【図７１】幾つかの実施例に基づくＧｅ・オン・Ｓｉマイクロストラクチャ型アバランシェフォトダイオード（ＭＳ－ＡＰＤ）を示している概略図。
【図７２】幾つかの実施例に基づくＧｅ・オン・Ｓｉマイクロストラクチャ型アバランシェフォトダイオード（ＭＳ－ＡＰＤ）を示している概略図。
【図７３】幾つかの実施例に基づくエッチストップ層を具備しているＧｅ・オン・Ｓｉマイクロストラクチャ型アバランシェフォトダイオード（ＭＳ－ＡＰＤ）を示している概略図。
【図７４】幾つかの実施例に基づくＧｅ・オン・Ｓｉマイクロストラクチャ型アバランシェフォトダイオード（ＭＳ－ＡＰＤ）を示している概略図。
【図７５】幾つかの実施例に基づくＭＳ－ＰＤ用の別のＳｉＮＩＰエピタキシャル層構造を示している概略図。
【図７６】（Ａ）乃至（Ｃ）は幾つかの実施例に基づくＭＳ－ＰＤ用の埋込酸化物上のＳｉＮ－Ｉ－Ｐエピタキシャル層を示している各概略図。
【図７７】幾つかの実施例に基づくＰＳｉ基板上のＳｉＮＩＰエピタキシャル層及びＳｉＧｅＢエッチストップ層を具備しているＭＳ－ＰＤを示している概略図。
【図７８】幾つかの実施例に基づくＭＳ－ＰＤ用のＳｉＧｅＢエピタキシャル層構造上のＧｅ・オン・ＳｉのＮＩＰを示している概略図。
【図７９】幾つかの実施例に基づくＭＳ－ＰＤ用のＧｅ・オン・Ｓｉエピタキシャル構造を示している概略図。
【図８０】幾つかの実施例に基づく別のＧｅ・オン・Ｓｉエピタキシャル構造を示している概略図。
【図８１】幾つかの実施例に基づくＧｅ・オン・Ｓｉエピタキシャル構造を示している概略図。
【図８２Ａ】図７９に図示した構造と類似したＧｅ・オン・Ｓｉマイクロストラクチャ型フォトダイオードに関する有限差分時間領域（ＦＤＴＤ）を使用したシミュレーションに関する説明図。
【図８２Ｂ】図７９に図示した構造と類似したＧｅ・オン・Ｓｉマイクロストラクチャ型フォトダイオードに関する有限差分時間領域（ＦＤＴＤ）を使用したシミュレーションに関する説明図。
【図８２Ｃ】図７９に図示した構造と類似したＧｅ・オン・Ｓｉマイクロストラクチャ型フォトダイオードに関する有限差分時間領域（ＦＤＴＤ）を使用したシミュレーションに関する説明図。
【図８３Ａ】図８０における構造と類似したＧｅ・オン・Ｓｉマイクロストラクチャ型フォトダイオードに関する有限差分時間領域（ＦＤＴＤ）を使用したシミュレーションに関する説明図。
【図８３Ｂ】図８０における構造と類似したＧｅ・オン・Ｓｉマイクロストラクチャ型フォトダイオードに関する有限差分時間領域（ＦＤＴＤ）を使用したシミュレーションに関する説明図。
【図８３Ｃ】図８０における構造と類似したＧｅ・オン・Ｓｉマイクロストラクチャ型フォトダイオードに関する有限差分時間領域（ＦＤＴＤ）を使用したシミュレーションに関する説明図。
【図８４Ａ】図７９における構造と類似したＧｅ・オン・Ｓｉマイクロストラクチャ型フォトダイオードに関する有限差分時間領域（ＦＤＴＤ）を使用したシミュレーションの結果を示しているグラフ。
【図８４Ｂ】図７９における構造と類似したＧｅ・オン・Ｓｉマイクロストラクチャ型フォトダイオードに関する有限差分時間領域（ＦＤＴＤ）を使用したシミュレーションの結果を示しているグラフ。
【図８５】幾つかの実施例に基づくマイクロストラクチャ型フォトダイオードチップの概略平面図。
【図８６】幾つかの実施例に基づいて単一チップ上に相互インピーダンス増幅器及び／又

Samsung Exhibit 1090, Page 120 of 786
Samsung v. W&Wsens - IPR2025-00993

はその他のエレクトロニクスを集積化したＭＳ－ＰＤ／ＡＰＤを示している概略平面図。
【図８７】マイクロストラクチャが無い状態の単純なエピタキシャル構造を示している概略図。
【図８８】マイクロストラクチャが無い状態の別の単純なエピタキシャル構造を示している概略図。
【図８９】幾つかの実施例に基づいてＳｉＰエピタキシャル層へマイクロストラクチャ型穴アレイをエッチングした場合の図８７におけるものと同じエピタキシャル構造を示している概略図。
【図９０】幾つかの実施例に基づいてＢＯＸＳｉＯ２層へマイクロストラクチャ型穴アレイをエッチングした場合の図８８におけるものと同じエピタキシャル構造を示している概略図。
【図９１Ａ】図８７－９０に図示した例示的構造に対するシミュレーション結果を示したプロット。
【図９１Ｂ】図８７－９０に図示した例示的構造に対するシミュレーション結果を示したプロット。
【図９２】幾つかの実施例に基づいてシリコン内へ穴をエッチングした場合のシリコン内のマイクロストラクチャ型領域を示している概略図。
【図９３】幾つかの実施例に基づいてテーパー付き穴を具備するＭＳ－ＰＤ構造を示している概略図。
【図９４】幾つかの実施例に基づいて徐々にテーパーが付けられた穴を具備するＭＳ－ＰＤ構造を示している概略図。
【図９５】幾つかの実施例に基づいて異なる直径のマイクロストラクチャ型穴を具備する物質構造を示している概略図。
【図９６】図９５に図示した如く異なる直径のマイクロストラクチャ型穴を具備する物質構造の平面図。
【図９７Ａ】図８２Ａに示した如き層構造を具備するマイクロストラクチャ上に入射する光に対する吸収を示しているグラフ。
【図９７Ｂ】図８２Ａに示した如き層構造を具備するマイクロストラクチャ上に入射する光に対する吸収を示しているグラフ。
【図９８】図８２Ａに示してあり且つ図９７Ａ及び９７Ｂにおいてシミュレーションした構造に対するシミュレーションした吸収を示しているグラフ。
【図９９】幾つかの実施例に基づいて８００乃至１０００ｎｍの波長範囲における動作に対するＳｉアバランシェフォトダイオード用の別の好適なエピタキシャル構造を示している概略図。
【図１００】幾つかの実施例に基づくマイクロストラクチャ型ＡＰＤの幾つかの特徴を示している概略図。
【図１０１】
【図１０２】マイクロストラクチャ型Ｇｅ・オン・ＳｉＡＰＤの幾つかの特徴を示している概略図。
【図１０３】（Ａ）乃至（Ｃ）は、幾つかの実施例に基づいて、マイクロストラクチャ型シリコン及びＧｅ・オン・Ｓｉフォトダイオード及びアバランシェフォトダイオードに対する直径、周期、及びその他のパラメータを示している各説明図。
【図１０４】（Ａ）及び（Ｂ）はマイクロストラクチャ型ＧｅＰ－ＧｅＩ－ＳｉＮ・オン・ＳｉＮ基板フォトダイオードである図８２Ａに示した構造に対する吸収－波長に対してＦＤＴＤ（有限差分時間領域）を使用したシミュレーション結果を示している各グラフ。
【図１０５】（Ａ）及び（Ｂ）は幾つかの実施例に基づく正方形格子穴パターンに対する固有モードを説明するための各説明図。
【図１０６】幾つかの実施例に基づいて互いにオーバーラップして配設された２個の正方形格子を具備しているマイクロストラクチャ型穴を示している概略図。
【図１０７】幾つかの実施例に基づくＧｅ・オン・Ｓｉのエピタキシャル構造を示してい

Samsung Exhibit 1090, Page 121 of 786
Samsung v. W&Wsens - IPR2025-00993

る概略図。
【図１０８】幾つかの実施例に基づくＧｅ・オン・Ｓｉのマイクロストラクチャ型フォトダイオードの基本的な特徴を示している概略図。
【図１０９】（Ａ）及び（Ｂ）は幾つかの実施例に基づいてマイクロストラクチャ型穴アレイに対してマクスウエル方程式を使用したＦＤＴＤシミュレーションの結果を示している各グラフ。
【図１１０】幾つかの実施例に基づいて異なる穴直径及び格子周期を有するマイクロストラクチャ型フォトダイオード／アバランシェフォトダイオードに対する吸収－波長のプロット。
【図１１１Ａ】幾つかの実施例に基づいて２つの格子及び２つの異なる穴直径が使用されている場合の図８２Ａにおけるような構造のＦＤＴＤ方法を使用したシミュレーションを示している概略図。
【図１１１Ｂ】幾つかの実施例に基づいて２つの格子及び２つの異なる穴直径が使用されている場合の図８２Ａにおけるような構造のＦＤＴＤ方法を使用したシミュレーションを示している概略図。
【図１１２】幾つかの実施例に基づいて同じ周期の２つの六角形状格子が結合され且つ互いにインターレースされている場合の別の格子構造を示している概略図。
【図１１３】各セルが固有モードを有しており何らかのフィールド伝播／分布がその固有モードの拡張である場合がある６単位セルを具備している六角形状格子を示している概略図。
【図１１４】幾つかの実施例に基づく穴アレイ及びテクスチャー表面を具備しているＳｉＮＩＰマイクロストラクチャ型フォトダイオードを示している概略図。
【図１１５】波長に対してのＳｉ及びＧｅの吸収係数を示しているグラフ。
【図１１６】幾つかの実施例に基づいてマイクロストラクチャ型穴アレイに起因するＧｅの向上された実効吸収係数を示しているグラフ。
【図１１７】幾つかの実施例に基づいてＳｉマイクロストラクチャ型ＰＤ／ＡＰＤの向上された吸収を示しているグラフ。
【発明を実施するための形態】
【００２５】
好適実施例の幾つかの例の詳細な説明を以下に与える。幾つかの実施例について説明するが、本特許明細書において記載する新たな要旨はここに記載されるいずれか一つの実施例又は幾つかの実施例の組合せに制限されるものではなく、多数の代替物、修正物、及び均等物を包含することを理解すべきである。更に、完全なる理解を与えるために以下の説明においては多数の特定の詳細を記述するが、幾つかの実施例はこれらの詳細の幾つか又は全てが無い状態で実施することが可能である。更に、説明の便宜上、本書に記載する新たな要旨が不必要にぼかされることを回避するために、関連技術において既知である或る技術的物質については詳細に記載していない。本書に記載する特定の実施例の内の一つ又は幾つかの個々の特徴を他の記載する実施例の特徴と結合して使用することが可能であることは明らかである。更に、種々の図面における同様の参照番号及び記号は同様の要素を表している。
【００２６】
幾つかの実施例によれば、半導体物質のバンドギャップの近傍における波長において物質のバルク吸収定数又は吸収を改善するためにマイクロストラクチャが使用される。このことは、光センサーの動作光学的波長及び／又は動作スペクトルを拡張することを可能とする。向上されたバルク吸収定数（即ち、係数）は実効吸収定数（即ち、係数）と呼称される。「実効」という用語が使用される理由は、吸収定数即ち係数は固有の物質特性だからである。しかしながら、共振効果、結合型共振効果、導波効果、プラズモン効果、フィールドエンハンスメント効果、散乱効果、近場及びサブ波長効果、線形及び非線形効果がある場合、実効吸収定数即ち係数はバルク即ち物質吸収定数即ち係数よりも一層大きい場合がある。吸収は吸収係数と吸収長との積に指数的に依存するので、バルク吸収係数を維

持することによって，実効吸収長は，量子効率に比例する同一の吸収を達成するためにＰＤ／ＡＰＤの「１」吸収領域の物理的な長さよりも一層大きなものである場合がある。本書において使用されているように、以下の用語は交換可能に使用されており、即ち、向上された吸収定数、向上された吸収係数、向上された実効吸収定数、向上された実効吸収係数、及び実効吸収定数、及び実効吸収係数、向上された吸収長、実効吸収長、向上された実効吸収長である。向上された吸収即ち実効吸収は，向上された吸収係数及び／又は向上された吸収長のいずれか又は両方に起因する場合がある。

【００２７】

幾つかの実施例によれば、向上された吸収は経路長に関して劇的な効果を有する場合がある。一つのバルク吸収例において，その元の振幅の１／ｅに対して吸収すべきフォトンに対する経路長は１００μｍであり、一方、この特許明細書において記載される幾つかの実施例に基づく向上された吸収の下では、その経路長はその元の振幅の１／ｅへ減衰するための光学振幅に対して１μｍである。等価的に、経路長を１μｍに一定に維持する場合には、向上された吸収係数はバルク吸収係数よりも１００倍大きく及び／又は向上された実効吸収長は実際の物理的長さよりも１００倍大きい。

【００２８】

このことは$A = A_0 e^{-\alpha L}$の関係から理解されるが、尚Ａは入射フォトンフラックスA_0の減衰振幅であり、αは吸収係数であり、Ｌは吸収が行われる経路長である。従って、Ｌを１００倍一層長いものとする代わりに、実効αがバルク吸収係数等の向上されていない吸収係数よりも１００倍一層大きなものであるように実効αを定義することが可能である。例えば、マイクロストラクチャの共振／結合共振／散乱／近場効果が１００倍一層長い経路長の均等性を与え，その場合に該共振／散乱／近場マイクロストラクチャは１ミクロンの長さであるに過ぎない。このことの一層簡単な記述は、共振／結合共振構造内のフォトンはその元の振幅の１／ｅの値に到達する前に５０回の往復を行い、従ってその均等線形長さは結合共振構造の長さの１００倍であるということである。説明の便宜上、共振／結合共振／線形及び非線形フィールドエンハンスメント／散乱／近場効果をここでは集約的に「共振（resonant）」として言及することとし、そのことは、共振、結合共振、導波、散乱、近場、プラズモン、非線形及び線形光学場効果を包含することが可能である。

【００２９】

本書において使用されているように、「マイクロストラクチャ」及び「マイクロストラクチャ型」という用語は、少なくとも一つの寸法がミクロン尺度，サブミクロン尺度，及び／又はサブ波長尺度及び／又は波長尺度である寸法及び種々の形状の柱体、ボイド、穴及びメサのことを意味している。

【００３０】

幾つかの実施例によれば，実効吸収を向上させるための本技術は、シリコン、ゲルマニウム、ＩｎＰとＧａＡｓとＧａＮとＧａＮとＩｎＧａＡｓ等のＩＩＩ―Ｖ物質、及びＩＩＩ－Ｖ物質群の任意の組合せを包含する種々の物質へ適用することが可能である。本明細書において使用されるように、ＩＩＩ－Ｖ物質の「物質群」という用語は、ＧａＡｓ，ＩｎＰ，ＧａＮ、ＩｎＳｂ半導体に対して格子整合しているか又はほぼ格子整合（数％以内）している任意の物質として定義される。例えば、ＩｎＰ物質群はＩｎＧａＡｓ、ＩｎＧａＡｓＰ，ＩｎＡｌＡｓ、ＩｎＡｓを包含することが可能である。幾つかの実施例によれば，マイクロストラクチャの場合，選択区域成長（ＳＡＧ），エピタキシャル横方向過剰成長（ＥＬＯＧ）、ＧｅかＩｎＧａＡｓか又はシリコンマイクロストラクチャにおけるその他のＩＩＩ－Ｖ物質の薄いバッファ層が有るか又は無いエピタキシャル成長（ＥＧ）等の再成長を格子不整合の有害な影響無しに実施することが可能である。何故ならば、シリコン上の格子不整合物質のフットプリントの寸法が小さいからである（約数ミクロン乃至サブミクロン）。このことは、従来のバッファ層（Ｇｅ・オン・Ｓｉ成長の場合における非晶質Ｇｅ等）を使用すること無しにＧｅ及びその他のＩＩＩ－Ｖ物質をシリコンと集積化させることを可能とさせる。複数物質の不均一集積化は，ホモ又はヘテロ構造、結晶性

及び微結晶性及び非晶質半導体の組合せ、炭素等の導体、グラフェン、絶縁体、誘電体、固体、気体、ガラス等の液体、又は半電導性とすることが可能なポリマーとすることが可能である。Ｇｅ及びＩＩＩ－Ｖ物質は、ミクロン尺度より大きな面積からウエハ尺度をカバーする面積を被覆することが可能なＳＯＧ、ＥＬＯＧ，ＥＧ方法を使用するバッファ層と共に又は無しでＳｉ上に成長させることも可能である。

【００３１】

幾つかの実施例によれば、実効屈折率を低下させるために、埋込酸化物（ＢＯＸ）、シリコン・オン・インシュレータ（ＳＯＩ）、シリコン・オン・サファイア（ＳＯＳ）、非晶質半導体等の低密度半導体、ナノワイヤ半導体、ボイド及び穴等の低指数物質が使用される。屈折率は物質の固有の特性である。しかしながら、幾つかの実施例によれば、ボイド、空隙、及び／又は穴（低屈折率物質で充填又は部分的に充填させることが可能）等の構造が光学波長程度の寸法を有している場合には、光学的電磁界が物質屈折率と該構造（低屈折率物質で充填又は部分的に充填させることが可能）とからなる平均屈折率を見ることとなる。この平均は、ここでは、実効屈折率と呼称する。幾つかの実施例によれば、低指数又は低実効指数物質をマイクロストラクチャにおいて使用することは必要ではない。

【００３２】

幾つかの実施例によれば、実効吸収を向上させる技術をシリコン、ゲルマニウム、ＩｎＰやＧａＡｓやＧａＮやＩｎＧａＡｓ等のＩＩＩ－Ｖ物質、及びＩＩＩ－Ｖ物質群の任意の組合せを含む種々の物質へ適用することが可能である。

【００３３】

マイクロストラクチャに起因して、容量も実効容量によって表すことが可能であり、それは、（１）一つの半導体の誘電率と，（２）半導体、誘電体、気体、真空、部分的真空、ガラス又はポリマー（ポリイミド、マイラー、又はその他の有機化合物）等の液体、とすることが可能な別の物質の誘電率との並列容量である。本装置の実効容量は、２つ又はそれ以上とすることが可能な並列コンデンサの容量の結合である。幾つかの実施例によれば、マイクロストラクチャを使用する利点は、その実効容量を半導体等の均一物質の容量よりも著しく低下させることが可能であるということである。ＲＣ時間（抵抗容量）はフォトダイオード及びアバランシェフォトダイオードの帯域幅を決定する基本的な時間の内の一つである。より低い容量は、装置をして、適切に高いデータレート帯域幅を維持しながら一層大きな面積を有することを可能とし、及び／又はＰＤ／ＡＰＤの帯域幅を決定する基本的な時間である電子及び／又は正孔の走行時間（transit time）を減少させるために該装置の厚さを減少させることによってデータレート帯域幅を増加させることを可能とする。

【００３４】

幾つかの実施例によれば，本光センサーはフォトダイオード（ＰＤ）、アバランシェフォトダイオード（ＡＰＤ），光電池（ＰＶ）又は太陽電池，又はフォトンを電子へ変換させる任意のオプトエレクトロニクス装置とすることが可能である。幾つかの実施例によれば、レーザー及び発光ダイオード等の電子／正孔をフォトンへ変換させるエミッター即ち発光体もマイクロストラクチャを使用して実現することが可能である。

【００３５】

幾つかの実施例によれば、向上させた吸収はＡＰＤ／ＰＤを、（１）バルク吸収係数が弱い、例えば、ＱＥ（量子効率）が３０％より大きいか又は５０％より大きく且つデータ帯域幅が３Ｇｂ／ｓよりも大きい状態で約１０００　１／ｃｍ又はそれ以下である場合にＡＰＤ／ＰＤの感度を物質バンドギャップに近いエネルギ（又は波長）を有するフォトンへ拡張させ、（２）一層短い吸収長従って一層短い走行時間に起因して高データレート帯域幅（例えば、１０Ｇｂ／ｓを越える）で動作させ、（３）向上させた吸収で量子効率を増加させ、（４）アバランシェフォトダイオードに対して低過剰ノイズで優れた増倍特性を有するシリコンで製造させ、（５）ＳｉフォトニクスおよびＣＭＯＳプロセスと適合性があるものとさせることを可能とする。幾つかの実施例によれば、ＰＤ／ＡＰＤは、信号処理，信号増幅、メモリ，ＣＰＵ、電気的送信機，光学的導波路、集積化オプティックス、

及び特定適用例のためのその他のＩＣ等のＡＳＩＣ（応用特定集積回路）と集積化させることが可能である。このことはＣＭＯＳファンドリーを使用する大量生産に有益的である。更に、エレクトロニクスと共に又は無しで集積化されている表面（又は底部）照射型ＰＤ／ＡＰＤはウエハレベルプロービングでテストすることが可能であり、更に、単一モード及びマルチモードの両方を取り扱うことが可能である。単一の光学的及び電気的チップはセラミックマルチチップキャリアーの必要性をバイパスし且つ組立及びパッケージングのコストを著しく減少させる。シリコンベンチは必要とされる場合のレンズ、ファイバー等の光学的部品に対する光学的アライメントに関連して使用することも可能である。

【００３６】

幾つかの実施例によれば、シリコンはアバランシェ利得のために使用される。シリコンはアバランシェフォトダイオードに対して過剰ノイズが一層低い。Ｇｅをシリコンと統合させることによって、吸収はＧｅ物質内において行われ且つ電子的利得はシリコン内において発生する。光学的波長、例えば１１００ｎｍ未満、に依存して、シリコンは、マイクロストラクチャの使用と共に、吸収及び電子的利得の両方のために使用することが可能である。

【００３７】

幾つかの実施例によれば、半導体におけるフォトンの吸収はマイクロストラクチャを使用して向上される。該マイクロストラクチャは、共振、結合共振、フィールドエンハンスメント、近場及びサブ波長効果、散乱、プラズモン、線形及び非線形光学的場、フォトニック結晶、与えられた物理的長さに対するフォトンの一層大きな吸収となる実効吸収長を効果的に増加させることが可能であり及び／又は該吸収係数を実効係数へ向上させることが可能な線形及び非線形の両方の効果である近場領域においての高コントラストグレーチングにおける吸収モード又は損失モード等の効果を有することが可能である。

【００３８】

幾つかの実施例によれば、シリコンフォトダイオード及び／又はアバランシェフォトダイオードのための吸収向上のために使用されるマイクロストラクチャは、長さ及び／又は係数の向上に起因して、量子効率が約５０％以上で、幾つかの場合にはＱＥが７０％以上で波長が約８５０ｎｍ（それは現在のデータ通信の好適な波長である）で帯域幅が１０Ｇｂ／ｓ（又は、等価的に、デジタルコーディングフォーマットに依存して、約６．７５ＧＨｚ）を越えているシリコンＰＤ及びＡＰＤとなる場合がある。

【００３９】

シリコン光学的検知器は、物質及び処理技術の成熟性に起因して、非常にロバスト即ち堅牢であり、その表面は表面状態及びキャリアー再結合中心を発生させる場合があるダングリングボンドを取り除くために容易にパッシベーションすることが可能であり、且つ、ＡＰＤ適用例の場合、正孔と電子との間のイオン化比（ｋ係数、シリコンはどのＩＩＩ－Ｖ物質よりも低いｋ係数を有している）が小さいのでノイズが低く、且つこの様な検知器は信号処理用エレクトロニクス及びＳｉフォトニクスとの集積化に対してＣＭＯＳ適合性を有している。

【００４０】

幾つかの実施例によれば、光発生されたキャリアーは、高変調帯域幅（１０Ｇｂ／ｓ帯域幅以上）及び高量子効率のため及び利得が３ｄＢより大きな高電流利得用のＡＰＤのためのＰ－Ｉ－Ｎダイオード（ＰＤ）又はＰ－Ｉ－Ｐ－Ｉ－Ｎダイオード（ＡＰＤ）の吸収用「ｉ」（時々「Ｉ」と言及される）領域における外部逆バイアスでスイープアウト即ち一掃される。

【００４１】

１Ｇｂ／ｓよりも大きな帯域幅を有するマイクロストラクチャ型フォトダイオード及びアバランシェフォトダイオードは通信において使用される。光学信号は、バイナリー（強度）、位相／周波数偏移（コヒーレント、ヘテロダイン通信）、分極（偏光）コーディング（polarization coding）、波長分割多重化等の多波長、及び分極多重化等の技術を使用して光に刻印された情報を有している。該光学信号は、空中及び／又はファイバーを介

Samsung Exhibit 1090, Page 125 of 786
Samsung v. W&Wsens - IPR2025-00993

して走行してマイクロストラクチャフォトダイオード及び／又はアバランシェフォトダイオード上に突き当たり、そこで該光学信号上に刻印されている情報を電気信号として抽出することが可能である。幾つかの場合においては、ヘテロダイン又はホモダインにおけるように、別の一つ又は複数の光学的供給源を混合させることが必要である。

【００４２】

図１は、幾つかの実施例に基づいて、本マイクロストラクチャ型フォトダイオード／アバランシェフォトダイオードを使用することが可能な光学データ伝送システムを例示している概略図である。光学データ伝送システム１００は、光学的供給源（ソース）１１０、空気及び／又はオプチカルファイバー等の伝送媒体１２０、及びマイクロストラクチャ型フォトダイオード／アバランシェフォトダイオードＭＳ－ＰＤ／ＡＰＤから構成されている。幾つかの実施例によれば、光学的供給源１１０はレーザーとすることが可能である。電気データ１１２が、直接的変調のためにレーザー１１０を順方向バイアスしている電源１１４で光学信号上に刻印される。レーザー１１０の出力は、ボールレンズ等の結合器１２２を介してオプチカルファイバー１２０へ結合させることが可能である。該光学信号はファイバー１２０（又は空気）を介して伝播し且つファイバー１２０から例えばレンズ１２４を介して高速マイクロストラクチャフォトダイオード／アバランシェフォトダイオード１３０へ結合させることが可能であり、そこで、該光学信号は電気信号へ変換され且つその結果得られるデータ１３２（データ１１２と一致する）が回復される。該マイクロストラクチャフォトダイオード／アバランシェフォトダイオードは電源１３４を使用して逆バイアスされる。

【００４３】

幾つかの実施例によれば、波長選択要素を該マイクロストラクチャ型フォトダイオード及びマイクロストラクチャ型アバランシェフォトダイオードと集積化させることが可能である。特に、マイクロストラクチャ型フォトダイオード／アバランシェフォトダイオードのアレイを、例えばＣＭＯＳ、ｂｉ－ＣＭＯＳ、バイポーラ装置及び回路を具備している応用特定集積回路を包含することが可能な単一のチップ上に製造させることが可能である。バンドパスフィルター等の波長選択要素は、粗波長分割多重化（ＣＷＤＭ）のために使用することが可能であり、その場合に、例えば、各々が１０－４０Ｇｂ／ｓの変調データを担持している８１０，８２０，８３０，８４０，８５０，８６０，８７０，８８０ｎｍの波長は、単一伝送媒体内において８０－３２０Ｇｂ／ｓの総合データレートを有することが可能である。

【００４４】

波長選択要素の例は、高コントラストサブ波長グレーチング、金属膜又は誘電体膜におけるサブ波長穴からなるアレイ、及びブラッグ反射器におけるような交番する屈折率を有している誘電体層、を包含している。該波長選択要素は、空胴共振器を形成するための多数の高コントラストグレーチングを包含しているバンドパスフィルターとすることが可能である。該要素は、グレーチングと、金属膜又は半金属膜上のサブ波長穴アレイ及び／又はブラッグミラー等のその他の波長選択要素との結合とすることも可能である。

【００４５】

更に、フォトダイオード／アバランシェフォトダイオードのマイクロストラクチャはそれ自身、波長選択性及び吸収長向上の両方とすることが可能であるように高コントラストグレーチング等の反射器を形成することが可能である。特に、該フォトダイオード／アバランシェフォトダイオードのフォトン吸収領域を向上させることが可能である。幾つかの実施例によれば、波長選択性のために共振光学空胴を形成するために、マイクロストラクチャ型フォトダイオード／アバランシェフォトダイオードの上に付加的な高コントラストグレーチングを製造することが可能である。該高コントラストグレーチングの内の一つが該２つの波長選択要素の間で電圧を発生させるように電気的にバイアスさせることが可能である場合には、同調可能なオプチカルファイバーの如く選択された波長を同調させることが可能である。

【００４６】

図２は、幾つかの実施例に基づいて、マイクロストラクチャ型フォトダイオード（ＭＳ－ＰＤ）及びマイクロストラクチャ型アバランシェフォトダイオード（ＭＳ－ＡＰＤ）と共に包含されている波長選択要素を示している概略図である。波長選択要素２２０を使用して、選択波長範囲内の波長のみがＭＳ－ＰＤ／ＡＰＤ１３０上に入射する。幾つかの実施例によれば、その窓は幅を１－２０ｎｍとすることが可能である（例えば、８２０ｎｍの中心波長±５ｎｍで、その場合バンドパスは８２０ｎｍを中心にした１０ｎｍである）。図２に示した場合は、シリコンＭＳ－ＰＤ／ＡＰＤ１３０と集積化させることが可能なシリコンから構成されている高コントラストグレーチング２２０である。幾つかの実施例によれば、マイクロストラクチャ型フォトダイオード／アバランシェフォトダイオード１３０のマイクロストラクチャ特徴部２１０は、該フォトダイオード／アバランシェフォトダイオードの吸収特性を向上させる機能に加えて、それ自身が波長選択器として動作することも可能である。ＭＳ－ＰＤ／ＡＰＤ１３０のマイクロストラクチャ２１０が波長選択器として構成される場合には、高コントラストグレーチング２２０の付加はバンドパスフィルターとして機能することが可能な共振空胴を形成する。

【００４７】

図３は、幾つかの実施例に基づいて、複数個の波長選択要素を具備しているＭＳ－ＰＤ／ＡＰＤを示している概略図である。この場合には、複数個の波長選択要素３２０及び３２２が製造され且つＭＳ－ＰＤ／ＡＰＤ１３０内に集積化されている。波長選択要素３２０及び３２２は、バンドパスフィルターとして機能するデュアル高コントラストグレーチングである。幾つかの実施例によれば、他のものと相対的に一つの波長選択要素へ或る電圧を印加すると、同調可能なバンドパスフィルターを製造することが可能である。

【００４８】

図４（Ａ）乃至（Ｄ）は、幾つかの実施例に基づいて、種々のバンドパスフィルター特性を示しているグラフである。図４（Ａ），（Ｂ），（Ｃ），（Ｄ）におけるプロットは，夫々、中心波長が８２０，８３０，８４０，８５０ｎｍであり、尚「Ｒ」は反射率である。例えば，１０ｎｍの帯域幅の場合の中心波長において、反射率は実際上ゼロであって殆どの光が透過され、一方、その帯域幅の外側においては，反射率は殆ど１００％であり透過は実際上ゼロである。

【００４９】

図５は、幾つかの実施例に基づく、粗波長分割多重化（ＣＷＤＭ）形態を示している概略図である。この場合に，中心波長が８２０，８３０，８４０，８５０ｎｍで各々が１００Ｇｂ／ｓ総合データレートに対して２５Ｇｂ／ｓの変調データレートを有しているような伝送媒体内を４つの波長が伝播する。各波長選択ＭＳ－ＰＤ／ＡＰＤで反射することによりＭＳ－ＰＤ／ＡＰＤ５３０，５３２，５３４，５４６上のバンドパスフィルターによって光学バンドが分離される。各反射の後、その光は反射器５５０を介して次の波長選択ＭＳ－ＰＤ／ＡＰＤへ反射され、全ての光学バンドが指定されたＭＳ－ＰＤ／ＡＰＤによって吸収されるまで、以下同様に行われる。各中心波長は一つのデータチャンネルを担持しており、例えば、８２０ｎｍは２５Ｇｂ／ｓのデータレートにおいてチャンネル１を担持しており，且つ８２０ｎｍにおけるバンドパスフィルターを有するＭＳ－ＰＤ５３０は８２０ｎｍ信号を光学信号の残部から分離し且つ集積化したＣＭＯＳＡＳＩＣ（不図示）によって更なる信号処理を行うために回復されたデータチャンネル１を発生させる。

【００５０】

幾つかの実施例によれば，ＭＳ－ＰＤ／ＡＰＤエピタキシャル層厚さは、エピタキシャル層厚さ及びＣＭＯＳ（相補的金属酸化物半導体）プロセスの構造と適合性があり、従ってＣＭＯＳＡＳＩＣと集積化させることが可能である。対照的に、１．２５Ｇｂ／ｓのデータレートを有する８５０ｎｍにおいての従来のシリコンフォトダイオードはｉ０μｍ厚さよりも大きなエピタキシャル層及び５３％量子効率を有している。従って従来のシリコンフォトダイオードの比較的厚い層はＣＭＯＳプロセスと容易に適合可能なものではない。

【００５１】

幾つかの実施例によれば、該光吸収層は非結晶性のものとすることが可能である。特に、それは、例えば、プラズマエンハンスト化学蒸着（ＰＥＣＶＤ）及び／又はホットワイヤ化学蒸着（ＨＷＣＶＤ）によって付着される水素化非晶質Ｓｉ（ａ－Ｓｉ：Ｈ）とすることが可能である。その層は、典型的に、０．３－３μｍ厚さの程度である。該光吸収領域（即ち、ｐｉｎフォトダイオード構造のｉ領域）を横断して逆バイアスで電圧を印加して光発生されたキャリアーを一掃して高速データ通信適用例のための高効率及び高帯域幅を可能とさせる。該非結晶性層上の層は透明又は半透明の導電性金属又はインジウムすず酸化物等の導電性酸化物とすることが可能である。該上部層はｐｉｎ構造を形成するためにドープした非結晶性物質の薄い層とすることが可能である。

【００５２】

図６（Ａ）及び（Ｂ）は、幾つかの実施例に基づく、マイクロストラクチャ型フォトダイオードの幾つかの基本的な部品を示している概略図である。図６（Ａ）はマイクロストラクチャをエッチングする前の物質構造６００を示しており、且つ図６（Ｂ）はエッチング後のＭＳ－ＰＤ６６０を示している。注意すべきであるが、幾つかの実施例によれば、該マイクロストラクチャは穴６２２であり、且つ幾つかのその他の実施例においては、該マイクロストラクチャは柱体である。幾つかのその他の実施例において、該マイクロストラクチャは穴と柱体との結合である。「Ｉａ」層６０８は、結晶性又は非結晶性Ｎ層上に成長させた非結晶性（例えば、水素化非晶質Ｓｉ（ａ－Ｓｉ：Ｈ））とすることが可能である。Ｐ層６１０は非結晶性及び高度にドープしたＰ又は導電性酸化物又は金属とすることも可能である。Ｎ層６０６も金属又は導電性酸化物とすることが可能である。オーミックコンタクト６２８及び６３０を使用してＰ層とＮ層との間にバイアスを印加させて、水素化キャリアーを一掃する高電界をｉ層６０８内に形成させる。基板６０２は、例えば、非結晶性及び／又は石英等の誘電体、ガラス、セラミック、及び／又は金属等の導体、シリサイド、導電性ポリマーとすることが可能である。幾つかの実施例によれば、「ｉ」層６０８としても知られる「Ｉａ」は０．３乃至３μｍの厚さ範囲を有することが可能である。

【００５３】

図７（Ａ）及び（Ｂ）は、幾つかの実施例に基づく底部照射型フォトダイオードの幾つかの基本的な部品を示している概略図である。図７（Ａ）はマイクロストラクチャをエッチングする前の物質構造７００を示しており、且つ図７（Ｂ）はマイクロストラクチャ（穴７２２等）をエッチングした後の底部照射型ＭＳ－ＰＤ７６０を示している。底部照射型ＰＤ／ＡＰＤの場合、「Ｉａ」即ち「ｉ」領域７０８はａ－Ｓｉ：Ｈ等の非結晶性とすることが可能であり且つ「Ｎ」層７１０も非結晶性とすることが可能であり、一方、「Ｐ」層７０６はＢＯＸ／ＳＯＩ７０４上で結晶性か又は非結晶性とすることが可能であり且つ結晶性又は非結晶性基板７０２とすることが可能である。しかしながら、光学損失を最小とさせるために、基板７０２及びＰ層７０６が結晶性であることが望ましい。何故ならば、それは８００乃至１１００ｎｍの範囲の波長において非晶質シリコンよりも吸収性が少ないからである。「ダブル又はマルチバウンス（bounce）」のＰＤ／ＡＰＤの場合、吸収領域「Ｉａ」層７０８は０．２乃至２μｍの厚さ範囲を有することが可能である。何故ならば、光学信号はＮ金属コンタクト７２６で反射し且つ「Ｉａ」吸収層７０８へ戻るからである。「Ｉａ」層７０８の厚さは減少させることが可能であり、従って、走行時間を減少させ且つフォトダイオード又はアバランシェフォトダイオードの帯域幅を増加させることが可能である。

【００５４】

図８（Ａ）及び（Ｂ）は、幾つかの実施例に基づく、ＭＳ－ＡＰＤ構造の幾つかの基本的な部品を示している概略図である。図８（Ａ）はマイクロストラクチャをエッチングする前の物質構造８００を示しており、且つ図８（Ｂ）はエッチング後のＭＳ－ＡＰＤ８６０を示している。光吸収用の「Ｉａ」領域８０８は結晶性又はａ－Ｓｉ：Ｈなどの非結晶性とすることが可能である。ＰＩＮシリコン（８２０、８１８、及び８０６）の結晶性アバランシェ利得領域をシリコン基板又はＢＯＸ／ＳＯＩ（埋込酸化物／シリコン・オン・

Samsung Exhibit 1090, Page 128 of 786
Samsung v. W&Wsens - IPR2025-00993

インシュレータ）基板８０２上に成長させる。Ｐａ上部層８１０は結晶性又は非結晶性とすることが可能である。ＰＳｉ層８１０とオーミックコンタクトを形成するため及び／又はシート抵抗を減少させるために、透明な金属酸化物層８２６を設けることが可能である。注意すべきことであるが、光学信号は上部表面へ真っ直ぐ（垂直）に来るか、又はそれは
フォトン矢印で示したように角度をもって来る場合がある。マイクロストラクチャ８２２は穴、柱体、又はこれらの組合せとすることが可能である。図８（Ｂ）に示したものは上部照射型ＡＰＤ８６０であるが、幾つかの実施例によれば、ＢＯＸ／ＳＯＩを使用して、基板のバルクを除去することが可能であり、且つ該ＡＰＤは８００－１１００ｎｍの波長範囲で底部から照射させることが可能である。Ｐ層８１０を介してのＰオーミック及びボンド金属８２８とＮ基板８０６を介してのＮオーミック及びボンド金属８３０との間に逆バイアスを印加させる。その逆バイアスは水素化キャリアーを一掃すると共に電子的利得を与える。ＰＤ用の典型的なバイアス電圧は１乃至１０ボルトの逆バイアスであり、且つＡＰＤの場合には、その範囲はほぼ５乃至５０ボルトの逆バイアスである。ここに記載する全てのＰＩＮ、ＰＩＰＩＮ装置における如く、ＰとＮとは交換可能であり、例えば、フォトダイオード及びアバランシェフォトダイオードに対して、ＰＩＮはＮＩＰとすることが可能であり且つＰＩＰＩＮはＮＩＮＩＰとすることが可能である。アノード即ちＰ層はカソードＮ層に関して負にバイアスされる。

【００５５】

図９（Ａ）及び（Ｂ）は、幾つかの実施例に基づいて、ＩＩＩ－Ｖ又はＧｅ物質のＳＡＧ前後の選択区域成長（ＳＡＧ）ＡＰＤ構造の或る側面を示している各概略図である。図９（Ａ）はエッチングした穴９２２（又は柱体周りの区域）を有するＳＩＡＰＤ構造を示している。ＩＩＩ－Ｖ物質又はＧｅの選択区域成長（ＳＡＧ）エピタキシャル成長を実施することが可能であり、図９（Ｂ）に示した如く、その場合には、Ｐａ層９１０及びＩａ層９０８はａ－Ｓｉ：Ｈ等の非結晶性とすることが可能であり、又はそれは結晶性シリコンとすることが可能である。特に、マイクロストラクチャのＩ区域９３４はＩｎＧａＡｓ又はＧｅとすることが可能であり、且つＰ区域９３２はＩｎＧａＡｓとすることが可能である。幾つかの実施例によれば、アバランシェ利得層（Ｐ層９２０及びＩ層９１８）を除去したＰＤ構造で開始して、ＩｎＧａＡｓ又はＧｅを具備するＳＡＧ　ＰＤを製造することが可能である。ＧａＮ，ＺｎＳｅ，ＩｎＰ，ＧａＡｓ等のその他の物質もＳＡＧにおいて使用することが可能である。幾つかの実施例によれば、非晶質Ｇｅ等のその他の非晶質半導体を使用することも可能である。幾つかの実施例によれば、間接遷移を超えるエネルギを有するフォトンの結晶シリコンよりも一層高い吸収係数に起因して非晶質シリコンを使用することが可能である。

【００５６】

図１０は、幾つかの実施例に基づくＰＩＮエピタキシャル層を具備する簡単化したマイクロストラクチャ型シリコンフォトダイオードを示している概略図である。０．２乃至１０μｍの厚さとすることが可能な埋込酸化物層（ＢＯＸ）１００４へ穴１０２２がエッチングされている。この構造１０６０は、シリコンと二酸化シリコンとの間の屈折率において高コントラストを提供しており、そのことは吸収を向上させることが可能である。Ｉ層１００８は０．５乃至５μｍの範囲内の厚さとすることが可能であり、且つＰ層１０１０及びＮ層１００６は０．１乃至５μｍの範囲内の厚さとすることが可能である。吸収の向上は８００乃至９００ｎｍ又はそれ以上の波長範囲において５０％を超えるものとすることが可能である。その向上された吸収は、垂直共振器面発光レーザー等のレーザーを直接的に変調させることによるか、又は光学的変調器がレーザー光を変調させる間接的変調によって発生される光学信号の或る波長範囲に対して最適化させることが可能である。Ｇｂ／ｓでのその変調されたレーザー光が該光学信号である。該光学信号は垂直入射で又は垂直入射に対して或る角度でのいずれかでマイクロストラクチャ型フォトダイオード１０６０上に入射する。マイクロストラクチャ型フォトダイオード１０６０の高速動作のためにＰオーミックコンタクトのアノード１０２８とＮオーミックコンタクトのカソード１０３

Samsung Exhibit 1090, Page 129 of 786
Samsung v. W&Wsens - IPR2025-00993

０との間に逆バイアスを印加させる。図示していないものはシリコン表面上の１０乃至１００ｎｍの厚さのパッシベーション層で、それは、表面再結合において発生するダングリングボンドを減少させるために、例えば、Ｓｉのウエット（蒸気）又はドライ酸化、二酸化シリコンの原子層付着、蒸着、によって成長される。

【００５７】

図１１は、幾つかの実施例に基づくＰＩＮエピタキシャル層を具備している簡単化したマイクロストラクチャ型シリコンフォトダイオードを示している概略図である。ＭＳ－ＰＤ１１６０は、マイクロストラクチャ型穴１１２２がＢＯＸ層１００４へ完全に貫通してエッチングされていないことを除いて、ＭＳ－ＰＤ１０６０と同一である。幾つかの実施例によれば、０．０１乃至２μｍのＮ層１００６を残存させることが可能である。

【００５８】

図１２（Ａ）―（Ｃ）は、幾つかの実施例に基づいて、特定のマイクロストラクチャ型穴パターンのマクスウエル伝播方程式方法の有限差分時間領域（ＦＤＴＤ）を使用するシミュレーションの状況を示している。図１２（Ａ）は六角形穴パターンを示しており、その穴の中心間距離がｘ方向において４９５ｎｍでｙ方向において８６０ｎｍである。図１２（Ｂ）に示してあるように、該穴は２μｍの深さまで完全に貫通してエッチングされており、その穴の直径は上部において３８５ｎｍであり底部において４３０ｎｍである。図１２（Ｃ）は、有限差分時間領域技術を使用したシミュレーションの結果を示しているプロットである。曲線１２１０、１２１２、１２１４は、夫々、吸収率、反射率、及び透過率を示している。この特定の例においては、２μｍの厚さのシリコンの場合、８０５乃至８３０ｎｍの波長範囲の光の６０％を超えるものを吸収させることが可能であることが理解される。穴直径、間隔、エッチング深さを変えることによって、光学信号の特定の波長に対して吸収を最適化させることが可能である。幾つかの実施例によれば、穴直径は２００乃至１８００ｎｍで変化させることが可能であり、間隔は２００乃至３５００ｎｍで変化させることが可能であり、且つ深さは０．１乃至２μｍで変化させることが可能である。

【００５９】

図１３は、幾つかの実施例に基づいて、Ｐ－Ｉ－Ｎドーピングを有する高コントラストマイクロストラクチャ型フォトダイオード（ＰＤ）用のエピタキシャル層構造を示している概略図である。Ｓｉ１３０２におけるＢＯＸ（埋込酸化物）１３０４で開始して、該酸化物層の厚さは０．１乃至１０ミクロン又はそれ以上の範囲であり、薄いＧｅバッファ層１３７０をＮＳｉ１３０２の上に成長させることが可能である。Ｇｅバッファ層１３７０を設けるか又は設けずに、その後のＮ，Ｉ，Ｐ層１３０６，１３０８，１３１０はＧｅ及び／又はＩｎＧａＡｓ，ＩｎＰ，ＩｎＧａＡｓＰ，ＧａＡｓ，ＡｌＧａＡｓ，ＧａＮ，ＩｎＧａＮ，ＡｌＧａＮ等のＩＩＩ－Ｖ物質群とすることが可能である。Ｎ，Ｉ，Ｐ層１３０６，１３０８，１３１０がＳｉである場合、Ｇｅバッファ層１３７０は省略することが可能である。該ＰＤの高速動作のために、該Ｎ層１３０６は０．１乃至５ミクロンの範囲とすることが可能であり、該Ｉ層１３０８は０．２乃至３ミクロンの厚さ範囲とすることが可能であり、且つ該Ｐ層１３１０は０．１乃至２ミクロンの範囲とすることが可能である。最後の層、この例においてはＰ層１３１０，は薄いＩｎＧａＡｓのキャッピングを具備するＩｎＰとＰ層等の複数の層の結合とすることが可能である。

【００６０】

図１４は、幾つかの実施例に基づいて、Ｐ－Ｉ－Ｎドーピングを有する高コントラストマイクロストラクチャ型フォトダイオード（ＰＤ）用のエピタキシャル層構造を示している概略図である。該ＰＩＮヘテロ構造は、Ｇｅバッファ層１４７０がＩ層１４０８とＮ層１４０６との間の界面又はその近くにおけるものとすることが可能であり、その場合にＩ層１４０８及びＰ層１４１０はＧｅ及び／又はＩＩＩ－Ｖ物質群とすることが可能であるということを除いて、図１３のものと同様である。この構造例の利点は、Ｓｉのバンドギャップ未満のフォトンエネルギーの場合に、Ｎ層１４０６においてより少ない数の電子・正孔対が発生され、そこで光発生されたキャリアーはＩ層１４０８内の高電界領域へ拡散

Samsung Exhibit 1090, Page 130 of 786
Samsung v. W&Wsens - IPR2025-00993

することが可能であり、その結果該ＰＤの高速応答における低速成分となる。該Ｇｅバッファ層はヘテロ成長のためには必要ではない場合もある。

【００６１】

図１５は、幾つかの実施例に基づいて、Ｐ－ｉ－Ｎドーピングを有する高コントラストマイクロストラクチャ型フォトダイオード（ＰＤ）用のエピタキシャル層構造を示している概略図である。該ＰＩＮヘテロ構造は、ｉ領域１５０８のみがＧｅ及び／又はＩｎＧａＡｓ，ＩｎＳｂ，ＩｎＧａＡｓＰ，ＩｎＡｓ等のＩＩＩ－Ｖ物質群等の一層低いバンドギャップ物質であることを除いて、図１３及び１４のものと同様である。Ｐ層１５１０及びＮ層１５０６の両方が一層高いバンドギャップ物質から構成されている。幾つかの実施例によれば、Ｐ層１５１０及びＮ層１５０６はフォトンエネルギーよりも一層高いバンドギャップエネルギーを有しており、且つｉ層１５０８はフォトンエネルギーと等しいか又はそれより低いバンドギャップエネルギーを有している。例えば、Ｎ層１５０６はＳｉとすることが可能であり、ｉ層１５０８はＩｎＧａＡｓ及び／又はＧｅとすることが可能であり、且つＰ層１５１０はＳｉ及び／又はＩｎＰとすることが可能である。Ｇｅバッファ層はヘテロ成長のために必要である場合も必要でない場合もある。Ｐ領域及びＮ領域において一層高いバンドギャップ物質を有することの利点は、これらの領域において発生される光キャリアを最小とさせることである。Ｐ領域及びＮ領域において発生される光キャリアは高電界領域へ拡散することが可能であり、その結果短い光学パルスに対してのフォトダイオードの応答における比較的遅い成分となる。したがって、Ｐ領域及びＮ領域において発生される光キャリアを減少させることは「テール効果（tail effect）」、即ちデータを光学的に送信するためのビットストリームにおける如く光学的入力パルス又は１組のパルスに応答してＰＤの電気的パルス出力の下降時間、を減少させる。Ｐ領域及びＮ領域の高ドーピングも、これらの領域において発生された光キャリアが高電界「ｉ」領域へ拡散する前に再結合することが可能であるように、少数キャリア寿命を減少させる。

【００６２】

図１６は、幾つかの実施例に基づいて、高コントラストマイクロストラクチャ型フォトダイオード（ＰＤ）の製造の幾つかの側面を示している概略図である。図１３に図示した例示的構造が、シリコン層１３０２内に埋め込まれている酸化物層１３０４までずーとＰＩＮ層１３１０，１３０８，１３０６を貫通してエッチングされている穴１６２２と共に示されている。ドライ及び／又はウエットエッチを使用することが可能であり、原子層付着によって露出表面へパッシベーション層を付加させることが可能である。この例においては、Ｇｅバッファ層１３７０がＮ層１３０６とＳｉ層１３０２との界面に設けられている。幾つかの実施例によれば、図１４及び１５に示した構造に対して同様の製造方法が使用される。

【００６３】

図１７（Ａ）－（Ｄ）は，幾つかの実施例に基づいて、穴配置、間隔、寸法、及びパッシベーション層の例を示している各概略図である。図１７（Ａ）は２８０ｎｍの間隔でパッシベーション層厚さが５０ｎｍである六角形レイアウトを示している。図１７（Ｂ）は正方形レイアウトを示している。図１７（Ｃ）及び（Ｄ），夫々，テーパー付き及び垂直の穴形状を示している。これらの図示例はシリコン用であるが、寸法を多少修正すれば、該技術はＧｅ及びＩＩＩ－Ｖ物質群に対しても適用可能である。該穴は円形断面を有することが可能であり、又は、幾つかの実施例によれば、たとえば、楕円、矩形等のその他の形状とすることが可能である。

【００６４】

図１８は、幾つかの実施例に基づいて、高コントラストマイクロストラクチャ型フォトダイオード（ＰＤ）の製造の更なる側面を示している概略図である。マイクロストラクチャ型穴１６２２をエッチングし、且つＰオーミックコンタクト層１８２８を付着させ且つアニールさせた後の図１３及び１６に図示した例示的構造を示してある。

【００６５】

図１９は、幾つかの実施例に基づいて、高コントラストマイクロストラクチャ型フォト

ダイオード（ＰＤ）の製造の幾つかの更なる側面を示している概略図である。図１３，１６，１８に図示した例示的構造が示されている。Ｐオーミックコンタクト１８２８を付着させ且つアニールさせた後に、メサをエッチングして物質１９７２を除去してＰＤの容量を画定させることが可能である。該メサの直径は該ＰＤに対して望ましいＲＣ時間に依存して５ミクロンから１００ミクロンを超える範囲とすることが可能である。露出されたＰ，Ｉ，Ｎ領域のパッシベーションを実施して、例えば、ダングリングボンドに起因する漏洩電流を最小とさせる。幾つかの実施例によれば、電気的に半絶縁性又は絶縁性の領域を発生させることによってＰＩＮ構造の容量を画定させるために、メサエッチングの代わりにプロトン衝撃等のイオン注入を使用することも可能である。

【００６６】

図２０は、幾つかの実施例に基づいて、高コントラストマイクロストラクチャ型フォトダイオード（ＰＤ）の製造の幾つかの更なる側面を示している概略図である。図１３，１６，１８，１９に図示した例示的構造が示されている。メサエッチングの後に、Ｎ層１３０６上にリング又は部分的リング形状のＮオーミックコンタクト２０３０を形成する。Ｐ領域１３１０へ電気的バイアスを印加するためにＰオーミックコンタクト１８２８からボンドパッド（不図示）へのメタリゼーションを接続させるために架橋経路が形成されるようにポリイミド等の物質から絶縁層を形成すること等のＰＤを完成させるための付加的な処理ステップは図示していない。又，簡単化のための，Ｎオーミックコンタクト２０３０をＮボンドパッドとの間の接続用金属は図示していない。Ｉ層１３０８内に高電界を形成させるためにＰ及びＮオーミックコンタクト１８２８と２０３０とに逆電気バイアスを印加させる。幾つかの実施例によれば、負の１乃至負の１０ボルトの電圧を印加させることが可能である。

【００６７】

図２１は、幾つかの実施例に基づいて、損失性高コントラストマイクロストラクチャ型フォトダイオード（ＰＤ）の幾つかの側面を示している概略図である。図２１は、光が吸収層１３０８内を２度走行するマイクロストラクチャ型ＰＰＤを示している。このことは、Ｓｉ基板１３０２の一部２１７４を酸化物層１３０４まで除去し且つ該酸化物をＡｕ，Ａｇ，Ａｌ又はＣｕ等の金属反射器２１７６でコーティングすることによって達成される。幾つかの実施例によれば、ブロードバンド又は波長選択性のいずれかのためにブラッグ反射器の形態とすることが可能である。幾つかの実施例によれば、特に、粗波長分割多重化、又は波長分割多重化において使用するために更に波長選択性を与えるためにＰ層１３１０の上部表面上にブラッグ層を包含させることも可能である。

【００６８】

図２２（Ａ）及び（Ｂ）は、幾つかの実施例に基づいて、特定のマイクロストラクチャ型ＰＤのＦＤＴＤ方法を使用するシミュレーションの状況を示している。図２２（Ｂ）は、図２１に図示した如きダブルパウンス構造に対するフォトンの波長に対してのフォトンの吸収のシミュレーション結果を示しているプロットである。該シミュレーションにおいて使用された例示的な厚さは以下の通りであり、即ち、酸化物１３０４は２ミクロン、Ｐシリコン１３１０は３００ｎｍ、ＩＳｉ１３０８は２ミクロン、及びＮシリコン１３０２は３００ｎｍであり、反射器２１７６は１００ｎｍ厚さのＡｕである。図２２（Ａ）に示した如く、六角形マイクロストラクチャ型穴を採用している。図２２（Ａ）に示されている如く、該穴は中心間六角形周期が６００ｎｍであり、穴直径が４８０ｎｍであり、SiO_2パッシベーションが３０ｎｍである。これらの寸法は、波長に対する吸収特性の対応するシミュレーションを有するマイクロストラクチャ型穴に対する単なる一つの例である。図２２（Ｂ）の曲線２２１０（吸収）及び２２１２（反射）から理解することが可能であるように、マイクロストラクチャ型穴の無いＳｉの場合におけるよりも吸収が著しく一層高いものであることが判明した。例えば、８５０ｎｍ波長の近傍において、吸収は７０％よりも一層良い。

【００６９】

図２３は、幾つかの実施例に基づいて、高コントラストマイクロストラクチャ型ＰＤの

Samsung Exhibit 1090, Page 132 of 786
Samsung v. W&Wsens - IPR2025-00993

或る側面を示している概略図である。下部構造は図２０の構造と類似しており、即ち、Ｓｉ基板２３０２、ＳｉＯ２層２３０４、及びＳｉＮ層２３０６である。下部Ｓｉ層２３０８を設けることも可能である。この場合、Ｇｅは上部Ｉ層２３０９及びＰ層２３１０として使用される。Ｐ層２３１０は、Ｇｅ１層２３０９上に成長させることが可能なＩｎＰから構成することも可能である。ＩｎＰＰ層２３１０の利点は、それが０．９乃至２μｍの波長においての吸収性がより低いということである。Ｐ層２３１０はＧｅＩ層２３０９上に成長されるＧａＡｓから構成することも可能である。更に、マイクロストラクチャ穴２３２２、Ｐオーミックコンタクト２３２８、Ｎオーミックコンタクト２３３０も示されている。注意すべきことであるが、光はＰ層２３１０の上部表面上及び／又はＳｉ基板表面２３０２上に入射することが可能である。

【００７０】

図２４は、幾つかの実施例に基づいて、ヘテロエピタキシャルマイクロストラクチャ型ＰＤの状況を示している概略図である。この場合に、Ｉ領域は、Ｇｅ層２４７０によって分離されているＳｉ（下部層２４０８）とＩｎＧａＡｓ（上部Ｉ層２４０９）との複合体とすることが可能である。Ｐ領域２４１０はＩｎＰである。幾つかの実施例によれば、該Ｉ領域は、その全体をバッファＧｅ層２４７０の薄い層の上に成長させたＩｎＧａＡｓとすることが可能である。更に、Ｓｉ基板２４０２、酸化物層２４０４、Ｎ層２４０８、マイクロストラクチャ穴２４２２、Ｐオーミックコンタクト２４２８、及びＮオーミックコンタクト２４３０も示されている。これは、高コントラストマイクロストラクチャ型ＰＤ構造の１例である。それは、更に、図２１における如き金属反射器を組み込むことが可能であり、その場合には、該ＰＤ下側の酸化物層へエッチングすることによってＳｉを除去し且つＡｕ，Ａｇ，Ａｌ又はＣｕ金属層を付着させて光をＩ吸収層へ向けて反射させることが可能である。上述した如くブラッグ反射器を使用することも可能である。光は、この例においては、Ｐ層側からやってくる。光はＳｉ基板側から来ることも可能であり、その場合には、Ｉ層を二度走行させるために反射器が該Ｐ層上に配置される。この様な構成の利点は、Ｉ層を単一走行の場合のものから不変のまま維持しながら、吸収領域を二度又はそれ以上走行させることによって吸収が著しく改善されるということを包含している。吸収領域厚さを、例えば、単一走行ＰＤのものの半分へ減少させることによって、ＰＤの速度が増加する。何故ならば、光発生されたキャリアーに対する走行時間は単一走行ＰＤの距離の半分だけ走行することが必要であるに過ぎないからである。高コントラストマイクロストラクチャとは、該マイクロストラクチャ及び一つの表面界面における空間又は大気及びＳｉＯ２及び／又は別の表面界面におけるバルク半導体物質の間の屈折率差のことを意味している。光は結合型固有セル又は共振器セルの複雑な態様で該マイクロストラクチャと相互作用を行い、その場合に、格子内の各六角形又は正方形セルは、発生する場合がある線形及び非線形の光学的フィールド向上に加えて、その隣接するセル又は共振器と結合されている個別的な共振器として考えることが可能である。光学的損失が存在しないか又は殆ど存在しない場合には、その結合型共振器構造は高いＱ（共振器の品質係数）を有することが可能であり、即ち、光は、例えば、消失する前に１０^{4}乃至１０^{9}回を越えて該マイクロストラクチャ内において繰り返しバウンス即ち跳ね返ることが可能である。しかしながら，弱い吸収に起因する等の光学的損失が或る場合，Ｑは低い場合があり且つ光は１００回未満、又は２０－３０回未満だけ該マイクロストラクチャ内で繰り返し跳ね返る場合がある。ＰＤ／ＡＰＤにおけるマイクロストラクチャは低Ｑ高コントラスト構造又は損失性高コントラスト構造であり、各セルのＱは隣接するセルに結合されている。

【００７１】

図２５は、幾つかの実施例に基づいて、発光ダイオード（ＬＥＤ）又は垂直表面発光レーザー（ＶＣＳＥＬ）等の光学的発光器に対する高コントラスト構造を示している。光学的発光器２５００はヘテロエピタキシャル層構造である。Ｓｉ層２５０６をＳｉ基板２５０２及びＢＯＸ／ＳｉＯ２層２５０４上に形成する。バッファＧｅ層２５７０をＳｉ層２５０６上に形成することが可能であり、続いて層２５１０を形成することが可能であり、該層２５１０はＩｎＡｓ量子ドット２５７２とし、ＧａＡｓ及びＡｌＧａＡｓで被覆させ

Samsung Exhibit 1090, Page 133 of 786
Samsung v. W&Wsens - IPR2025-00993

ることが可能である。更に、「Ｉ」層を約１０００ｎｍ以下の薄いものとすることが可能であり且つ順方向バイアスさせる簡単なＳｉＰＩＮマイクロストラクチャはフォトン射出体とすることが可能である。

【００７２】

図２６は、例えば、幾つかの実施例に基づく、高コントラスト１．３ミクロン波長フォトエミッタ（ＰＥ）用の基本的な構造を示している。１．３ミクロン波長エミッタ用のアクティブ層は、ＩｎＡｓ量子ドット層２５７０（図２５に図示）又は図２６における２６７０をＧａＡｓＰ層２６０４とＮ層２６０６との間に挟み込み、それらをＡｌＧａＡｓＰ層２６０８とＮ層２６０２との間に挟み込み、且つＰＧａＡｓキャッピング層２６１０を最終層として使用して形成される。典型的な厚さは文献中に見出すことが可能である。例えば、AY Liu, S Srinivasan, J Norman, AC Gossard, JE Bowers等のシリコンフォトニクス用量子ドットレーザー（Quantum Dot Lasers For Silicon Photonics）、フォトニクスリサーチ３（５）、Ｂ１－Ｂ９（２０１５）を参照すると良く、この文献を引用により本書に取り込む。更に、量子ドット及び／又は被覆層の複数の層がある場合がある。該マイクロストラクチャは、利得及び光学的フィールドオーバーラップを最適化させるために、ＱＤ層の内の一つ又はそれ以上に定常波ピークが位置されるように構成することが可能である。ＭＳ－ＰＤ／ＡＰＤの場合、該マイクロストラクチャの長さは、特定の波長において、整数個の波長が往復して、例えば、その特定の波長においての吸収の向上を最適化させるようなものとさせることが可能である。更に、単一のマイクロストラクチャ、例えば、単一の穴が、マイクロストラクチャの無い同様の構造のものと比較して、ＰＥ又はＭＳ－ＰＤ／ＡＰＤのいずれかに対して吸収又はエミッションの向上を有することが可能である。

【００７３】

図２７は、幾つかの実施例に基づいて、エッチングした穴を具備する高コントラストマイクロストラクチャ型フォトエミッタ（ＰＥ）構造の幾つかの基本的な特徴を示している概略図である。その物質構造は図２５に示したＰＥ２５００のものと同様である。マイクロストラクチャ穴２７２２はアクティブ層２５１０内にエッチングされている。Ｐ及びＮオーミックコンタクト２７２８及び２７３０を使用して、装置２７００を順方向にバイアスさせ、即ちＮに対してＰを正とさせてアクティブ層２５１０からフォトンを発生させ、該アクティブ層２５１０は、本例においては、１．３ミクロンの波長においてのＩｎＡｓ量子ドット２５７２を有している。可視光から赤外光のその他の波長において光を発生させるために、その他のアクティブ層、被覆層を使用することが可能である。光の波長に依存して、光は上部表面から及び／又は酸化物層２５０４を介して底部表面から射出させることが可能である。マイクロストラクチャ型高コントラストフォトンエミッタの利点は、フォトンが該アクティブ層及び／又はレーザーの場合には利得層と一層長く相互作用を行うことである。何故ならば、該高コントラスト構造は非常に高いＱを有することが可能であり、そのＱは１０^{5}乃至百万以上の範囲に亘り、というのも、該構造は殆ど光学的損失を有するものではなく且つ該量子ドットが光学的利得を与えるからである。該高コントラスト低損失マイクロストラクチャ型フォトエミッタはＬＥＤとして、ＶＣＳＥＬとして、及び／又はレーザー及び／又は高出力ＬＥＤとして動作することが可能である。該ＰＥは順方向バイアスされ、Ｎオーミック即ちＮ層であるカソード２７３０に対してＰオーミック即ちＰ層は正電圧にある。

【００７４】

図２８は、幾つかの実施例に基づいて、ＰＥの幾つかの側面を示している概略図である。ＰＥ２８００は、基板２５０２の一部２８７４が光射出領域下側で酸化物層２５０４へ除去されていることを除いて、図２７に示したＰＥ２７００と同様である。金属及び／又は分散型ブラッグ反射器（ＤＢＲ）２５０４等のブラッグからなる反射器を該酸化物層上に形成してアクティブ層内で発生された光をＰ層２５１０表面へ反射して戻させる。幾つかの実施例によれば、装置２８００はＬＥＤモード及び／又はレーザーモードで動作する。

Samsung Exhibit 1090, Page 134 of 786
Samsung v. W&Wsens - IPR2025-00993

【００７５】
図２９は、幾つかの実施例に基づいて、ＰＥの幾つかの側面を示している概略図である。ＰＥ２９００は，金属とすることが可能であり且つ、所望により，Ｐオーミックコンタクトとしても動作することが可能な反射器２９２８を包含している点を除いて、図２８のＰＥ２８００と同様である。幾つかの実施例によれば、別体のＰオーミックを設けることが可能である。反射器２９２８は分散型ブラッグ反射器及び／又は部分的に金属及び部分的にＤＢＲとすることも可能である。光は酸化物層２５０４の下部表面から且つ一部２８７４が除去されている基板２５０２を介して射出される。フォトエミッタ即ち光射出器２９００は、ＬＥＤ及び／又はＶＣＳＥＬモード等のレーザーモードで動作することが可能である。幾つかの実施例によれば、フォトエミッタ２９００はエッジモードで動作することが可能であり、その場合に光はアクティブ層の面に対して垂直ではなく面内において射出され、射出エッジに沿ってＤＢＲ又は金属等のミラーが存在する場合も存在しない場合もある。

【００７６】
図３０は、幾つかの実施例に基づいて、ＰＥの幾つかの側面を示している概略図である。ＰＥ３０００は図２９のＰＥ２９００と同様であるが、ＶＣＳＥＬ（垂直共振器面発光レーザー）として構成されている。ＰＥ３０００は高コントラストマイクロストラクチャ型穴（又は柱体）を具備しておりＳｉ上にヘテロエピタキシャル成長されている。注意すべきことであるが、簡潔性のために非常に基本的な部品のみが示されているに過ぎない。該高コントラスト構造は反射器２９２８及び３０７６によって挟み込むことが可能である。Ｐ層２５１０は半導体エピタキシーによって成長されたＤＢＲとすることが可能であり、それに続いてＰオーミックメタリゼーション層２９２８を設けることが可能である。幾つかの実施例によれば、ＤＢＲは導電性酸化物又は非導電性酸化物から形成することが可能であり、ＤＢＲ上にＰ金属を設けるか及び／又は図２８における如くその側部上に設けることが可能である。酸化物層２５０４の底部側上のミラー３０７６は金属及び／又は異なる屈折率の誘電体層のＤＢＲとすることが可能である。図示した如き光出力は底部からのものであるが、上部からのものとすることも可能である。

【００７７】
図３１は、幾つかの実施例に基づいて、簡単なＰＩＮフォトダイオード構造の幾つかの側面を示している概略図である。高電界領域外側の領域において発生された光キャリアーに起因する拡散電流を最小とさせるために、「Ｉ」層３１０８、Ｐ及びＮ層３１１０及び３１０６は高度にドープさせ及び／又は縮退的にドープさせて少数キャリアーの寿命を減少させる。Ｎ及びＰドーピングは1×10^{18}乃至8×10^{21}／cm^3以上の範囲とすることが可能である。Ｉ層３１０８は意図的にドープしておらず且つ5×10^{16}／cm^3未満とすることが可能である。更に、酸化物層３１０４とＳｉ基板３１０２とが示されている。前の例におけるように、Ｇｅバッファ層を付加するかしないかに拘わらず、Ｇｅ及び／又はＩＩＩ－Ｖ物質を成長させることが可能であり且つＰ及びＮ層も高度にドープさせるか及び／又は縮退的にドープさせることも可能である。そのドーピングは一様なものであることは必要ではなくグラデーションを有することが可能であり、例えば、エピタキシャル成長期間中に「Ｉ」層内へのドーパントの拡散を最小とさせるために「Ｉ」層界面近くのＰ又はＮ層においてドーピングを減少させる。

【００７８】
Ｐ及びＮ層における少数キャリアーの寿命を減少させることによって、これらの層内の光発生されたキャリアーは拡散し及び／又は高電界「Ｉ」内に移動する前に再結合することが可能であり、該高電界「Ｉ」においては、電子及び／又は正孔が光電流に貢献してフォトダイオード変調型周波数応答の劣化となる場合がある。従って，高電界領域外側で発生されたキャリアーに起因する光電流の寄与を最小とさせることが望ましい。

【００７９】
少数キャリアーの寿命を減少させるその他の方法は、Ｐ及び／又はＮ領域における部分的及び／又は完全なヒアイオン注入等の欠陥を導入することを包含している。導入される

イオンは不活性イオン及び／又は活性イオンとすることが可能であり、部分的な又は完全な熱アニーリングを行うか又は行わないことが可能である。更に、該マイクロストラクチャ型穴（及び／又は柱体）は部分的なパッシベーションを行うか又は行わないものとすることが可能であり、従って、Ｎ及びＰ層の低電界領域はキャリアーシンクとして作用することが可能であり、一方、「Ｉ」層の高電界領域においては、該キャリアーは迅速に一掃される。パッシベーションは「Ｉ」層上において目だって選択的とすることが可能である。

【００８０】

図３２は、幾つかの実施例に基づく、ＭＳ－ＰＤ製造の幾つかの側面を示している概略図である。開始物質構造は図３１の構造３１００に図示した如きものとすることが可能である。簡単なＮＩＰ（Ｎ及びＰはＰ１Ｎに対しては交換可能である）マイクロストラクチャ型フォトダイオードが示されており、その場合に、穴３２２２がＰ層３１０６の上部へエッチングされている。その目的はＮ及び「Ｉ」層の壁をパッシベーションし且つＰ層の壁をパッシベーションせずにおいてそれにより、例えば、７８０乃至９８０ｎｍの波長を有する光で発生されるＰ層内の少数キャリアーの寿命を減少させる。パッシベーションされていないＰ壁上の表面状態は少数キャリアー用の潜在的なシンクとして作用することが可能であり、そこで該キャリアーは再結合される。

【００８１】

図３３は、幾つかの実施例に基づいて、ＭＳ－ＰＤ製造の或る側面を示している概略図である。Ｎ及び「Ｉ」層の穴３２２２の側壁のパッシベーションが示されており、結果的にパッシベーション層３３２４が形成されている。該パッシベーションは熱酸化及び／又はSiO_2の原子層付着を使用して実施することが可能である。５－５０ｎｍ厚さの熱酸化物３３２４を、例えば、該側壁上に成長させることが可能である。その他の厚さのものを成長させることも可能である。熱酸化の後に、穴のエッチングを継続して行い、例えば、Ｐ層３１０６を貫通してSiO_2層３１０４へエッチングすることが可能である。全ての処理ステップが示されているわけではなく、例えば、穴のエッチングを継続する期間中に不図示の熱酸化物によってＮ層を保護することが可能である。

【００８２】

図３４は、幾つかの実施例に基づいて、ＭＳ－ＰＤ製造の側面を示している概略図である。パッシベーションの後に、穴３２２２は区域３４２２で示した如くに更にエッチングされる。注意すべきことであるが、Ｎ及びＰ層は交換させることが可能であり、従ってこの例において示されている如きＮＩＰ構造の代わりに、ＰＩＮ構造とすることも可能である。穴３２２２はSiO_2層３１０４へエッチングさせることが可能であり、及び／又はそれらはＰ層３１０６を介して部分的にのみエッチングさせ、薄いＰ層が残存するようにさせることが可能である。Ｐ層３１０６内の穴３２２２の側部は、この例においては、パッシベーションされておらず、その表面状態が光によって発生される何らかの少数キャリアーをその潜在的なシンクへと引き込んで再結合させることを可能としている。幾つかの実施例によれば、Ｐ層３１０６もパッシベーションさせ及び／又は部分的にパッシベーションさせることが可能である。層３１０６も高度にドープさせることが可能であるので、少数キャリアーの寿命は数十ピコ秒以下である可能性がある。

【００８３】

図３５は、幾つかの実施例に基づいて、ＭＳ－ＰＤの或る側面を示している概略図である。マイクロストラクチャ型ＮＩＰフォトダイオード３５６０は、Ｎ及び「Ｉ」層のパッシベーションされた側壁を具備しているがＰ層の側壁はパッシベーションされていないマイクロストラクチャ穴３２２２を有している。Ｎ及びＰ層の夫々へのオーミックコンタクト３５２８及び３５３０が付加されてフォトダイオード３５６０の高速動作のための逆バイアスを与えている。該フォトダイオードのＮ側上に入射する光は垂直であるか及び／又はＮ層面に対して垂直からずれたもののいずれかである。

【００８４】

図３６は、幾つかの実施例に基づいて、ＭＳ－ＰＤの或る側面を示している概略図であ

る。マイクロストラクチャ型穴フォトダイオード３６６０はＳｉＮＩＰ層を有しており、その場合に、パッシベーションは図３５に示したＰＤ３５６０と同様に側壁上で部分的である。しかしながら、ＰＤ３６６０の場合には、光はＳｉ基板側からオプチカルファイバー３６８０を介してやってくるが、そこではビア３６７２がエッチングされているので自己整合プロセスを可能とさせ、その場合に、ファイバー３６８０は、レンズ３６８２と共に又は無しで、ビア３６７２に沿って光のマイクロストラクチャ型フォトダイオード３６６０内への光学的結合を行うための正しい位置へ案内される。略０．１－１０μｍ厚さの誘電体層３６７６を穴３２２２上方のＮ層３１１０上に位置決めさせることが可能である。誘電体層３６７６上にはＡｇ又はＡｕ（又は任意のその他の適宜の金属又は合金で、例えば、Ａｌ，Ｎｉ，Ｃｒ等）等の金属反射器３６７８及び／又は吸収用「Ｉ」層３１０８へ向けて光を反射させるためにブラッグ反射器（ＢＲ）等の誘電体積層体を設けることが可能である。反射防止コーティング３６７４を設けることも可能である。先の例における如く、Ｇｅバッファ層を付加するか又は付加せずにＧｅ及び／又はＩＩＩ－Ｖ物質を成長させることも可能である。

【００８５】

図３７は、幾つかの実施例に基づいて、少数キャリアーの寿命を減少させるための技術を示している概略図である。この場合には、穴表面をパッシベーションするか又は部分的にパッシベーションする代わりに、表面及びバルクの再結合が使用される。10^{20}／cm^3より大きな高ドーピングは拡散長を例えば０．１μｍ（オーガ（Auger）再結合）未満へ減少させることが可能である。更に、層３７１０及び３７０６内に欠陥３７７０及び３７７２を導入させるためにイオン注入が使用される。半導体内の欠陥はショックリーーリードーホール（Shockley-Read-Hall）再結合プロセスを介して寿命を減少させることも可能である。例えばＸｅ，Ｂｉ，Ｔｉ，Ｃｒ，Ａｒ，Ｎ等のイオンをＮ及び／又はＰ層内に注入させることが可能である。装置動作のために長い少数キャリアーの寿命が望ましい場合の既知の構造と逆に、本書に記載する技術は、ショックリーーリードーホール効果に起因する再結合率を増加させるために、エピタキシャル成長及び／又は金属、非金属及び不活性イオンのイオン注入のいずれかによって欠陥を導入させる。該欠陥に起因して深い及び／又は浅いトラップを形成させることが可能であり、それらは少数キャリアーの寿命を短くさせることが可能である。少数キャリアーの寿命が短いことは、高電界領域「Ｉ」層へ通して光電流に寄与することが可能な拡散電流の寄与を最小とさせるためにＰ及びＮ領域において望ましいものである。該「Ｉ」領域内へ拡散及び／又は走行するこれらの「遅い」拡散電流は、フォトダイオードの光電流時間応答特性に対しての遅い成分に寄与することによってフォトダイオードの時間応答の劣化を発生させる場合がある。

【００８６】

図３８（Ａ）乃至（Ｃ）は、シミュレーションしたマイクロストラクチャ型フォトダイオードに対する種々のパラメータを示している。図３８（Ａ）は穴中心間の距離「ｄ」を有している六角形穴パターンを示している。図３８（Ｂ）は穴中心間の距離「ｄ」を有している正方形穴パターンを示している。図３８（Ｃ）はＦＤＴＤ方法を使用したシミュレーションに対して使用したパラメータの表である。８５０乃至９５０ｎｍ及び、例えば、９８０ｎｍの範囲の光学信号の波長に対して六角形状格子の穴における周期が２０００ｎｍで直径が１３００乃至１５００ｎｍの範囲の複数の穴で２－２．５μｍの厚さのＳｉＯ$_2$層上の２μｍ厚さのシリコン層で９０％より大きな吸収を達成することが可能であることが判明した。更に、波長は７５０－１０００ｎｍの範囲に亘ることが可能である。穴直径は、サブ波長乃至入射光学信号の波長より大きなものとすることが可能であり、１００乃至３０００ｎｍの直径の範囲に亘る。Ｓｉ吸収層の厚さは０．３乃至１０μｍの範囲とすることが可能である。ＳｉＯ$_2$層は０．２乃至１０μｍの範囲に亘ることが可能である。幾つかの実施例によれば、入射フォトンの吸収を最適化させるために複数の穴直径の混合を使用することも可能である。

【００８７】

図３９は、波長に対する吸収に対してのＦＤＴＤを使用するマイクロストラクチャ型穴

Samsung Exhibit 1090, Page 137 of 786
Samsung v. W&Wsens - IPR2025-00993

フォトダイオードのシミュレーション結果をプロットしたグラフである。フォトダイオード吸収「１」層は２μｍ厚さであり、穴直径は１０００乃至１５００ｎｍの範囲にわたるものであった。入射エネルギー波長は８５０乃至９５０ｎｍの範囲であった。３つの曲線３９１０，３９１２，３９１４は、夫々、１０００ｎｍ，１３００ｎｍ，１５００ｎｍの穴直径に対しての吸収のプロットである。このシミュレーションは、１５００ｎｍの穴直径の場合，８５０－８７０ｎｍの波長範囲にわたって９０％より大きな吸収が達成されており、且つ、１３００ｎｍの穴直径の場合、２０００ｎｍの周期での六角形状格子での穴で８７５乃至９５０ｎｍの波長範囲にわたって８０％より大きな吸収を達成することが可能であることを示している。２μｍＳｉは２－２．５μｍＳｉＯ２層の上にある。理解されるように，何らの特徴無しでの従来のシリコン層のものを越えて吸収を向上させるために、入射波長よりも一層大きな穴直径を有することを使用することが可能である。

【００８８】

図４０は、幾つかの実施例に基づいて、Ｐ－Ｉ－Ｐ－Ｉ－Ｎエピタキシャル構造を具備するマイクロストラクチャ型アバランシェフォトダイオード（ＡＰＤ）を示している概略図である。図４０の場合には、ＡＰＤ４０６０の全ての層は、例えば、７８０乃至１０００ｎｍの範囲の光学的通信波長に対してシリコンである。ＡＰＤ４０６０は可視光波長範囲においても動作可能である。データレートは１００Ｍｂ／ｓ乃至５０Ｇｂ／ｓ又はそれ以上の範囲に亘ることが可能である。－４乃至－５０ボルトの電圧範囲でＰ及びＮオーミックコンタクト４０２８及び４０３０間に逆バイアス電圧を印加させる。アバランシェマイクロストラクチャ型フォトダイオード４０６０は以下のようなドーピング及び厚さを有することが可能であり、即ち、例えば，Ｐ層４０１０のドーピングは$1\times10^{18}/cm^3$を越えるもので且つ厚さは０．１－１．０μｍであり、Ｉ層４００８のドーピングは$1\times10^{15}/cm^3$未満であって且つ厚さは０．５－３μｍであり、Ｐ層４０２０のドーピングは$1-3\times10^{17}/cm^3$であって且つ厚さは０．１－０．５μｍであり、Ｉ層４０１８のドーピングは$1\times10^{15}/cm^3$未満であって且つ厚さは０．３－１μｍであり、及びＮ層４００６のドーピングは$1\times10^{19}/cm^3$であって且つ厚さは０．５－３μｍである。幾つかの実施例によれば、上の２つの層４０１０及び４００８はＳｉの代わりにＧｅとすることも可能である。穴４００２はＡＰＤ層を部分的に貫通してエッチングさせるか又は図４０に示されている如くＳｉＯ２層４００４へ完全にエッチングさせることが可能である。

【００８９】

マイクロストラクチャフォトダイオードの場合における如く、ＡＰＤの場合に、光学信号は正面側（エピタキシャル層側）から入射するか又は背面側（基板側）から入射することが可能である。更に，基板内にビアがある場合、反射器をＳｉＯ２上に付着させることが可能であり、その結果、ＡＰＤ構造内において光学信号を２回又は多数回バウンス即ち跳ね返させることとなる。幾つかの実施例によれば，ＰとＮとは交換可能であり，その結果Ｎ－Ｉ－Ｎ－Ｉ－Ｐマイクロストラクチャ型ＡＰＤとなる。

【００９０】

図４１は、幾つかのその他の実施例に基づいて，Ｐ－Ｉ－Ｐ－ＩＮエピタキシャル構造を具備するマイクロストラクチャ型アバランシェフォトダイオード（ＡＰＤ）を示している概略図である。ＡＰＤ４１６０は、複数の穴４１２２（又は柱体）が部分的にエッチングされていることを除いて、図４０に図示したＡＰＤ４０６０と同一である。図４１に示した例においては、穴４１２２はＰ層４０２０内に部分的にエッチングされており及び／又はＰ層４０２０で停止している。幾つかのその他の実施例によれば，穴４１２２は１吸収層４００８内に部分的にエッチングさせることが可能である。

【００９１】

図４２は、幾つかの実施例に基づいて、Ｇｅ吸収層及びＧｅＰキャッピング層を具備しているマイクロストラクチャ型ＡＰＤを示している概略図である。ＡＰＤ４２６０は、上の２つの層がＳｉの代わりにＧｅであるという点を除いて、図４０に図示したＡＰＤ４０６０と同様又は同一である。ＡＰＤ４２６０は、ＰＧｅ層４２１０が$1\times10^{20}/cm$

より大きなドーピングレベルを有することが可能であるという点を除いて、ＡＰＤ４０６０に対して上述した如き同じドーピング及び厚さ範囲を有することが可能である。埋込酸化物（ＢＯＸ）シリコン基板上のＡＰＤ構造Ｐ（Ｇｅ）－Ｉ（Ｇｅ）－Ｐ（Ｓｉ）－Ｉ（Ｓｉ）－Ｎ（Ｓｉ）のエピタキシャル成長の後に、該マイクロストラクチャをエッチングする。該マイクロストラクチャは穴、柱体又はこれら２つの結合とすることが可能である。該エッチングはSiO_2層まで行うことが可能であり、又はSiO_2層４００４に到達する前の深さへ部分的にエッチングすることも可能であり、例えば、穴はＰＳｉ層４０２０まで又はその中へエッチングさせることが可能である。マイクロストラクチャを具備しているＧｅ吸収層４２０８は，１００Ｍｂ／ｓ乃至５０Ｇｂ／ｓ又はそれ以上のデータレートにおいて７８０乃至２０００ｎｍの波長で光学信号が動作することを可能とさせるものと期待されている。該光学信号は上部表面（エピタキシャル表面）から又は底部表面（基板表面）から入射することが可能である。ビア及びSiO_2上に付着させた反射器がある場合には、上部表面から入射する光学信号を、２回目及び／又は多数回にわたり吸収Ｉ（Ｇｅ）層４２０８へ反射させることが可能である。Ｓｉと、空気と、Ｇｅとの間には光学的屈折率差があるので、定常波を確立させることが可能であり、且つ定在波又は固有モードとしても既知の定常波のピーク強度において吸収層を有するべく該構造の厚さを最適化させることが可能である。更に，Ｓｉがトランスペアレント即ち透明である波長において、光学信号が底部表面からＡＰＤ内へ結合することを助けるためにマイクロレンズをＳｉ基板内にエッチングさせることが可能である。底部から入射する光学信号を吸収Ｉ（Ｇｅ）層４２０８へ反射させるためにＰ（Ｇｅ）４２１０上にSiO_2及び反射器を配置させることが可能である。－４乃至－５０ボルトの範囲の逆バイアス電圧をＰ及びＮオーミックコンタクト４０２８と４０３０との間に印加させる。

【００９２】

図４３（Ａ）乃至（Ｄ）は、幾つかの実施例に基づいて、マイクロストラクチャ型フォトダイオード及びＡＰＤの分極感度を示している。図４３（Ａ）はシミュレーション用に使用した幾何学的形状を示している。これらの穴は寸法及び周期において対称的であり、Ｂ又はＡのいずれかに沿っての光学信号の電界分極はＭＳ－ＰＤ／ＡＰＤの吸収特性において５％未満の差を示している。吸収は、入射光からその光の透過及び反射を差し引いたものと等しく，且つ量子効率は吸収に直接的に比例する。穴寸法「ａ」及び「ｂ」が同じでない場合には、ＭＳ－ＰＤ／ＡＰＤは分極感度を示す。図４３（Ｂ）において，曲線４３１０は波長に対しての吸収をプロットしており、その場合、「ａ」及び「ｂ」寸法は両方共１０００ｎｍに等しい。該吸収特性は５％未満の差異を示している。図４３（Ｃ）はａ＝１３００ｎｍでｂ＝８７０ｎｍの場合を示している。曲線４３２０及び４３２２は、Ａ又はＢに沿っての分極が成る場合の吸収値における差異は高々２倍であることを理解することが可能であることを示している。図４３（Ｄ）はａ＝１５００ｎｍでｂ＝６５０ｎｍである場合に対する結果を示している。曲線４３３０及び４３３２は、分極配向（polarization orientation）に起因する吸収差も高々２倍であることを示している。「ａ」、「ｂ」、Ａ及びＢの両方における更なる寸法変化がある場合に、分極配向に起因する吸収差は１０乃至１００倍、又はそれ以上異なる場合がある。分極「不感受性」（分極配向に起因する吸収変化が５％未満の場合）及び分極感受性（分極配向に起因する吸収変化が１０倍又はそれ以上の場合）の両方のフォトダイオード及びＡＰＤが有用である。信号が分極多重化されていない場合、例えば、同じ波長を使用する場合、２つのチャンネルを送信することが可能であり、その場合に一つのチャンネルは一つの分極で且つ別のチャンネルは第１のチャンネルに対して直交している。例えば、各チャンネルは同じ波長において特定の分極において２５Ｇｂ／ｓで送信することが可能である。受信機器において、該信号をデマルチプレクス、即ち脱多重化，させるために分極感受性光検知器を使用する。総合データレートは８５０ｎｍの波長において５０Ｇｂ／ｓである。レーザーの直接変調において、該レーザーのスペクトルは、例えば、ＣＷモードで動作しているレーザーよりも常に一層幅広である。該スペクトルは高々数ナノメートル（例えば，３ｎｍ）だけ広くさせることが可能である。従って、８５０ｎｍにおいて、レーザーが直接的に変調される場合

Samsung Exhibit 1090, Page 139 of 786
Samsung v. W&Wsens - IPR2025-00993

には、高々±約１．５ｗｎｍ広げて中心周波数は８５０ｎｍとすることが可能である。垂直共振器面発光レーザーにおいては、マルチな横モードに起因して、横モードは一層幅広のスペクトルに対して著しく寄与することが可能である。マルチモードシステムにおいては、このことはモード選択損失を減少させるので望ましいことである。

【００９３】

図４４は、幾つかの実施例によれば、データ処理及び／又はルーチングのために相互インピーダンス及び／又は別のＡＳＩＣ（応用特定集積回路）と集積化されているＭＳ－ＰＤ／ＡＰＤを示している。そのプロセスはＣＭＯＳ及び／又はＢｉＣＭＯＳとすることが可能である。ＭＳ－ＰＤ／ＡＰＤ４４２０は電気的リード４４２２を介してエレクトロニクス４４３０（例えば、相互インピーダンス増幅器（ＴＩＡ）及び／又は別のＡＳＩＣ）へ電気的に接続されていることが示されている。その部品は全て単一のシリコン基板４４１０上に集積化されている。マイクロストラクチャ型ＰＤ／ＡＰＤをＩＣエレクトロニクスと集積化させることの一つの利点はパッケージングコストの低下であり、その場合に、２個又はそれ以上の個別的な装置の代わりに、単一のチップが使用され、それは又マルチチップセラミック担体を使用すること無しに回路ボード上に直接的に配置させることも可能である。単一チップ上にＭＳ－ＰＤ／ＡＰＤをエレクトロニクスと集積化させることの別の利点は、オーミックコンタクトへ接続されている比較的大きなボンドパッドを省略することに起因して、潜在的に容量が低くなることである。動作波長は、全てのシリコンマイクロストラクチャ型ＰＤ／ＡＰＤに対して８００－９９０ｎｍの範囲である。動作波長はＧｅマイクロストラクチャ型吸収層を付加した場合には１８００ｎｍへ拡張させることが可能である。１０，２８，５６Ｇｂ／ｓのデータレートでの動作は単独で又はアレイで達成させることが可能である。該データレートは、又、プロトコル及びリンク適用例に依存して１，５，２０，２５，３０，４０Ｇｂ／ｓとすることも可能である。典型的に、マルチモードファイバー及び／又は複数のファイバにわたっての高データレートは１メートル未満から１００メートルを越える長さにわたる距離で使用される。複数のファイバ及びマイクロストラクチャ型ＰＤ／ＡＰＤ（ＭＳ－ＰＤ／ＡＰＤ）のアレイを使用して１００乃至４００Ｇｂ／ｓの総合データレートを与えることが可能である。例えば、単一シリコンチップ上の相互インピーダンス増幅器（ＴＩＡ）及び／又はその他の信号処理／ルーチングＩＣエレクトロニクス等のＩＣエレクトロニクスと集積化されている１０ＭＳ－ＰＤ／ＡＰＤアレイと共に各ファイバーが１０Ｇｂ／ｓで動作している１０ファイバーチャンネルは１００Ｇｂ／ｓの総合データレートを有することが可能である。各チャンネルが５６Ｇｂ／ｓである場合には、該１０チャンネルは５００Ｇｂ／ｓを越える総合データレートを有することが可能である。

【００９４】

図４５は、幾つかの実施例に基づいて、単一シリコンチップ上のＴＩＡ及び／又は別の信号処理ＩＣと集積化されているＭＳ－ＰＤ／ＡＰＤに対するフリップチップ配置の幾つかの側面を示している概略図である。幾つかの実施例によれば、ＴＩＡ及び／その他の信号処理集積回路４５３０はＣＭＯＳ及び／又はＢｉＣＭＯＳプロセスを使用して製造される。半田バンプ４５１２及び４５１４及び／又は同様のバンプ技術を使用してチップ４５１０をＰＣＢ（プリント回路基板）４５５０へ取り付ける。幾つかの実施例によれば、半田バンプ４５１２の幾つか又は全てを使用してチップ４５１０とＰＣＢ４５５０との間の電気的接続を行い、一方、半田バンプ４５１４は物理的マウンティング及び／又は安定化のために使用される。何故ならば、ＭＳ－ＰＤ／ＡＰＤ４５２０とＰＣＢ４５５０との間の直接的な電気的接続は必要ではない場合があるからである。幾つかの実施例によれば、チップ４５１０を、ＰＣＢ４５５０の代わりに、別のチップ又はマルチチップ担体へ取り付ける。チップ４５１０をＰＣＢ４５５０上に直接的にパッケージングすることは、ＰＣＢ上に配置させる前にＰＤ及びＩＣエレクトロニクスを最初にマルチチップセラミック担体上にマウントさせるという既知の従来技術と比較して、高々８０％だけパッケージングコストを減少させる。更に、オプチカルファイバー４５２４からＭＳ－ＰＤ／ＡＰＤ４５２０へ光をフォーカスさせるためにシリコンチップ４５１０上に集積化光学レンズ４５２

Samsung Exhibit 1090, Page 140 of 786
Samsung v. W&Wsens - IPR2025-00993

２を製造させることが可能である。注意すべきことであるが、この構成においては、光信号はＭＳ－ＰＤ／ＡＰＤ４５２０の基板側から入る。Ｓｉ上の集積化レンズ４５２２は、入ってくる光学信号の吸収のためにＧｅマイクロストラクチャを使用することが可能であり動作波長が１１００ｎｍより大きい（例えば、１１００ｎｍ乃至１８００ｎｍ）である場合に、使用することが可能である。

【００９５】

図４６は、幾つかの実施例に基づいて、単一シリコンチップ上にＴＩＡ及び／又は別の信号処理ＩＣと集積化されているＭＳ－ＰＤ／ＡＰＤに対するフリップチップ配置の幾つかの側面を示している概略図である。該チップ及びマウント技術は図４５に図示し且つそれについて説明したものと同様か又は同一である。この場合に、チップ４５１０はビア４６２６を包含しており、そこではＭＳ－ＰＤ／ＡＰＤ４５２０への光学経路における殆ど又は全てのシリコンは除去されている。光を収集し且つそれをＭＳ－ＰＤ／ＡＰＤ４５２０へ指向させるために集積化誘電体レンズ４６２２が設けられている。幾つかの実施例によれば、レンズ４６２２の代わりに光パイプが使用される。ビア４６２６の側壁は光の収集を助けるために誘電体及び／又は金属でコーティングすることが可能である。光学信号がオプチカルファイバー４５２４へ反射して戻ることを減少させるためにレンズ４６２２上に反射防止コーティングを設けることが可能である。更に、ファイバー４５２４又はチップ４５１０を傾斜させてファイバー４５２４へ戻る反射を減少させることが可能である。オプチカルファイバー４５２４は、１Ｇｂ／ｓ未満から６０Ｇｂ／ｓを越える範囲のデータレートでレーザー光源からの光学信号を集積化ＰＤ／ＡＰＤ及びＩＣエレクトロニクス回路４５１０へもたらすために使用される。幾つかの実施例によれば、約１，５，１０，２０，２８，５０，５６Ｇｂ／ｓのデータレートを使用することが可能である。幾つかの実施例によれば、光学信号波長は全シリコンマイクロストラクチャ型ＰＤ／ＡＰＤ（ＭＳ－ＰＤ／ＡＰＤ）に対して８００－９９０ｎｍの範囲にわたる場合があり、且つ吸収層用のマイクロストラクチャ型Ｇｅの場合には、該波長は１８００ｎｍへ拡張させることが可能である。

【００９６】

図４７は、幾つかのその他の実施例に基づいて、単一シリコンチップ上のＴＩＡ及び／又は別の信号処理ＩＣと集積化されているＭＳ－ＰＤ／ＡＰＤ用のフリップチップ配置の幾つかの側面を示している概略図である。そのチップ及びマウント技術は図４５及び４６に図示し且つそれらについて説明したものと同様であるか又は同一である。図４５及び４６におけるように、単一のチップ４５１０は光学的要素と電子的要素との両方を包含している。集積化フレネルレンズ４７２２と共にＭＳ－ＰＤ／ＡＰＤ４５２０への光学経路におけるＳｉの殆ど又は全てを除去するためにチップ４５１０の基板内にビア４６２６が設けられているので、光学信号はオプチカルファイバー４５２４から効率的に収集される。収集された光学信号はＭＳ－ＰＤ／ＡＰＤ４５２０上に入射する。幾つかの実施例によれば、フレネルレンズ４７２２の代わりに、高コントラストグレーチング（ＨＣＧ）が使用される。幾つかの実施例によれば、ＨＣＧはフィルター効果を有することが可能であり、従って特定の光学波長のみをＭＳ－ＰＤ／ＡＰＤへ透過させ、一方その他を反射させることが可能である。この帯域通過特性は単一のファイバーにおいて複数の波長が使用される粗波長分割多重化（ＣＷＤＭ）にとって有用である。

【００９７】

図４８は、幾つかのその他の実施例に基づいて、単一シリコンチップ上のＴＩＡ及び／又は別の信号処理ＩＣと集積化されているＭＳ－ＰＤ／ＡＰＤに対するフリップチップ配置の幾つかの側面を示している概略図である。該チップ及びマウント技術は、図４５－４７に図示し且つそれらについて説明したものと同様であるか又は同一である。ビア４６２６の壁は、光がＭＳ－ＰＤ／ＡＰＤ４５２０へ入射するための光パイプを提供するために誘電体及び／又は金属でコーティングすることが可能である。次いで、オプチカルファイバー４５２４をビア４６２６内へ挿入させることが可能であり、その場合に該ビアはファイバー４５２４をＭＳ－ＰＤ／ＡＰＤ４５２０に対して整合させるためのガイドを提供し

、それによりＭＳ－ＰＤ／ＡＰＤに対するオプチカルファイバーの光学的パッキング及びアライメントを簡単化させて約３０％又はそれ以上のコスト低下を生じさせる。幾つかの実施例によれば、ファイバー４５２４はテーパー付きとさせることも可能であり、及び／又はビア４６２６がファイバー４５２４に対するストップを与えるように複数の直径を有することが可能である。例えば、ビア４６２６にステップ即ち段差を設けてファイバー４５２４の端部をそのステップ上に当接させることが可能であり、それをシリコンへ取り付けることが可能である。このステップ構成は、又、最適な光収集のためのファイバーとＭＳ－ＰＤ／ＡＰＤとの間の精密な距離を与える。幾つかの実施例によれば、ファイバーからＭＳ－ＰＤ／ＡＰＤへの光学信号の転送を最適化させるために、ビア４６２６において、特にファイバー４５２４とＭＳ－ＰＤ／ＡＰＤ４５２０との間の空間において、屈折率整合流体、ゲル及び／又はポリマー及び／又は誘電体バルク又は薄膜を使用することが可能である。

【００９８】

上述した如く、基板側から光が入射する場合（底部照射）、ＭＳ－ＰＤ／ＡＰＤは該ＭＳ－ＰＤ／ＡＰＤ内における光学信号の二重及び／又は多重のバウンス即ち跳ね返りを使用することが可能である。このことは、高い量子効率を達成すると共に吸収層を一層薄くさせることを可能とさせる。一層薄い吸収層は一層高速の走行時間とすることを可能とさせ、それによりＭＳ－ＰＤ／ＡＰＤが一層高いデータレートで動作することを可能とさせる。

【００９９】

図４９は、幾つかのその他の実施例に基づいて、単一シリコンチップ上のＴＩＡ及び／又は別の信号処理ＩＣと集積化されたＭＳ－ＰＤ／ＡＰＤ用のフリップチップ配置の幾つかの側面を示している概略図である。該チップ及びマウント技術は図４５－４８に図示し且つそれらについて説明したものと同様であるか又は同一である。この例においては、ボールレンズ４９２２がビア４６２６内に位置されていて、オプチカルファイバー４５２４からの光を効率的にＭＳ－ＰＤ／ＡＰＤ４５２０へ結合させる。ボールレンズ４９２２はＭＳ－ＰＤ／ＡＰＤ４５２０に対しての該レンズのアライメントのためにビア４６２６内に位置することが可能である。

【０１００】

図５０は、幾つかのその他の実施例に基づいて、単一シリコンチップ上のＴＩＡ及び／又は別の信号処理ＩＣと集積化されたＭＳ－ＰＤ／ＡＰＤ用のフリップチップ配置の幾つかの側面を示している概略図である。該チップ及びマウント技術は図４５－４９に図示し且つそれについて説明したものと同様であるか又は同一である。この例においては、ボールレンズ５０２２がビア４６２６内に位置しており、該ビアにおいてはシリコンの殆ど又は全てがエッチング除去されているので光は殆どが空中及び／又は流体、ゲル、ポリマー、固体等の屈折率整合物質内を走行する。更に、ビア４６２６は、オプチカルファイバー４６２６のボールレンズ５０２２に対しての且つ更にＭＳ－ＰＤ／ＡＰＤ４５２０に対してのアライメントに対するガイド及び／又はストップとして作用する。

【０１０１】

図５１は，幾つかの実施例に基づいて、単一シリコンチップ上のＴＩＡ及び／又は別の信号処理ＩＣと集積化されているＭＳ－ＰＤ／ＡＰＤに対するフリップチップ配置の幾つかの側面を示している概略図である。該チップ及びマウント技術は図４５－５０に図示し且つそれらについて説明したものと同様であるが、ＭＳ－ＰＤ／ＡＰＤ５１２０及びＴＩＡ及び／又はその他の信号処理集積回路５１３０がシリコンチップ５１１０の上部表面上又はその近くにマウントされている点が異なる。金属性導体導管５１３２及び５１３４はＡｌ，Ｃｕ，Ｍｏ，Ｗ，Ｎｉ，ＴｉＮ等から構成することが可能である。導管５１３２はＭＳ－ＰＤ／ＡＰＤ５１２０をＩＣエレクトロニクス５１３０へ接続させている。導管５１３４はＩＣエレクトロニクス５１３０を、半田バンプ等のバンプ技術を使用してＰＣＢ４５５０（又はチップ担体）へのトレースへ接続させており、そのことは、該チップのＰＣＢ及び／又はチップ担体への良好なアライメントを可能とさせる。幾つかの実施例によ

Samsung Exhibit 1090, Page 142 of 786
Samsung v. W&Wsens - IPR2025-00993

れば、ＩＣエレクトロニクスをＰＣＢ上のトレース及び／又はチップ担体へ接続させるために、ワイヤボンディングを使用するその他の方法を使用することも可能である。ファイバー４５２４はＭＳ－ＰＤ／ＡＰＤ５１２０の直ぐ近くに位置され，且つその構成は，ファイバー４５２４の先端部上のボールレンズ、及び／又はファイバーとＭＳ－ＰＤ／ＡＰＤとの間のボールレンズを包含することが可能である。図４５－５０に関して説明した如くに、グレーチング、フレネルレンズ等のその他の光をフォーカスさせる要素を使用することも可能である。幾つかの実施例によれば，上述したＭＳ－ＰＤ／ＡＰＤ構造に示した如く埋込二酸化シリコン（ＢＯＸ，埋込酸化物）等の屈折率の不連続が存在するか及び／又はバルク物質の屈折率に対しての該マイクロストラクチャの実効屈折率における変化が存在している場合には、エピタキシャル表面から照射する光（上部照射型）もＭＳ－ＰＤ／ＡＰＤ５１２０内において光学信号の二重及び／又は多重のバウンス即ち跳ね返りを有する場合がある。ＭＳ－ＰＤ／ＡＰＤ内の光学信号の二重及び／又は多重のバウンスは、量子効率を著しく犠牲にすること無しに一層薄い吸収層及び短い走行時間を可能とさせ、それによりＭＳ－ＰＤ／ＡＰＤの一層高いデータレート動作を可能とさせる。光の二重又は多重のバウンスとは、ＭＳ－ＰＤ／ＡＰＤのパスにおいて吸収されず且つ該ＭＳ－ＰＤ／ＡＰＤ構造から出る光のことを意味しており、これらのフォトンはＭＳ－ＰＤ／ＡＰＤ構造に向けて反射されて戻される。複数の穴及び柱体からなるマイクロストラクチャ内において、光は共振及び／又は結合共振状態となる場合があり，そのことは向上された実効吸収係数及び／又は向上された実効吸収長とさせることが可能である。

【０１０２】

図５２は、単一Ｓｉチップ上にＴＩＡ及び／又はその他の信号処理及びルーチングエレクトロニクス等のＩＣエレクトロニクスと集積化された複数のＭＳ－ＰＤ／ＡＰＤからなるアレイを示している概略図である。アレイは、例えば，ＴＩＡ及び／または信号処理、ルーチング，格納用のＡＳＩＣ等のＩＣエレクトロニクスと集積化された２個乃至１０個を超える数のＭＳ－ＰＤ／ＡＰＤを包含することが可能である。図示例においては、単一のＳｉチップ５２１０上にマウントされている４個のＭＳ－ＰＤ／ＡＰＤ５２２０，５２２２，５２２４，５２２６が示されている。これらのＭＳ－ＰＤ／ＡＰＤ５２２０，５２２２，５２２４，５２２６はＩＣエレクトロニクス５２３０，５２３２，５２３４，５２３６へ夫々接続されている。しかしながら、幾つかの実施例によれば、複数のＭＳ－ＰＤ／ＡＰＤがＳｉチップ上の単一のＩＣエレクトロニクス装置へ接続されているか，または複数のＩＣエレクトロニクス装置が単一のＭＳ－ＰＤ／ＡＰＤへ接続されている。アレイ内の複数のＭＳ－ＰＤ／ＡＰＤは同一のものとすることが可能であり、例えば，マイクロストラクチャの穴直径及び周期は同一の波長、例えば８５０－８７０ｎｍ、に対して最適化される。その他の実施例によれば、アレイ内の各ＭＳ－ＰＤ／ＡＰＤは周波数の異なる帯域に対して最適化させることが可能である。例えば、アレイ内に４個のＭＳ－ＰＤ／ＡＰＤが存在している場合、各ＭＳ－ＰＤ／ＡＰＤの穴直径及び周期を最適化させることによって、該４個のＭＳ－ＰＤ／ＡＰＤは、夫々、８５０－８７０ｎｍ、８７５－８９５ｎｍ、９００－９２０ｎｍ，９２０－９５０ｎｍ（又はその任意の組合せ）において最適化させることが可能である。例えば、Molin et al.、次世代ＷＤＭシステム用の８５０－９５０ｎｍ広帯域ＯＭ４マルチモードファイバー（850-950nm wideband OM4 multimode fiber for next generation WDM systems）、ＯＦＣ（２０１５）、を参照すると良く，それを引用により本書に取り込む。１，５，１０，１６，２０，２５，２８，３２，４０，５６及びそれよりも大きなもの及びそれらの間の全ての範囲のデータレートは，光学的データリンク用の標準及びプロトコル及び適用例に依存して可能である。オプチカルファイバー５２４０，５２４２，５２４４，５２４６は別々のファイバーとすることが可能であり，又は並列フィバーリボンとして設けることが可能である。オプチカルファイバー５２４０，５２４２，５２４４，５２４６は各々が単一帯域の波長及び／又は１００Ｇｂ／ｓ乃至１Ｔｂ／ｓ又はそれ以上の総合データレートを与えるためにＷＤＭ及びＣＷＤＭ用の複数帯域の波長を担持することが可能である。例えば、各々が１０Ｇｂ／ｓである１０個のファイバーチャンネルを有する１０個のＭＳ－ＰＤ／ＡＰＤからなるアレイは１００Ｇｂ

Samsung Exhibit 1090, Page 143 of 786
Samsung v. W&Wsens - IPR2025-00993

／ｓの総合データレートを与える。各々が２５－２８Ｇ／ｂｓにある４個のファイバーチャンネルを有する４ＭＳ－ＰＤ／ＡＰＤアレイは１００Ｇｂ／ｓの総合データレートを与え、各々が５６Ｇｂ／ｓにある２個のファイバーチャンネルを有する２ＭＳ－ＰＤ／ＡＰＤアレイは１００＋Ｇｂ／ｓの総合データレートを与える。各ファイバーチャンネルが複数の波長帯域、例えば８５０－８７０ｎｍ及び８７５－８９５ｎｍ、を担持することが可能であり且つ各波長帯域が２５－２８Ｇｂ／ｓにおいて送信することか可能である場合には、４ファイバーアレイは実効的に２００Ｇｂ／ｓを超える総合データレートを有することが可能である。

【０１０３】

図５３は、幾つかの実施例に基づく、高データレートＭＳ－ＰＤ用のエピタキシャル構造を示している概略図である。図示した構造は１０Ｇｂ／ｓよりも一層大きなものとすることが可能である。穴５３２２がＳｉＯ２ＢＯＸ層５３０４までエッチングするか、又は該穴をＰ層５３０６までエッチングして及び／又は、例えば、Ｐ層５３０６内へ部分的にエッチングさせることが可能である。ドーピング及び厚さは次の通りであり、即ち、Ｓｉ基板５３０２は１５０μｍの厚さであり、ＢＯＸ層５３０４は２－４μｍの厚さであり、Ｐ＋層５３０６は０．２－１μｍの厚さであってドーピングは1×10^{20}／cm^3を越えており、Ｉ層５３０８は１．５－２μｍの厚さであって意図的にはドーピングされておらず（5×10^{15}／cm^3未満），且つＮ＋層５３１０は０．２－０．５μｍの厚さであってドーピングは1×10^{19}／cm^3を越えるものである。Ｎ及びＰ層５３１０及び５３０８の高ドーピングは少数キャリアー寿命を短縮させてＰＤの応答を遅くさせる場合がある拡散電流を最小とさせる。幾つかの実施例によれば，1×10^{20}及び1×10^{19}／cm^3を越える程度の高いドーピングは、少数キャリアー寿命がピコ秒程度であり且つ直列抵抗が減少されるように使用される。

【０１０４】

図５４は、幾つかの実施例に基づく、高データレートＭＳ－ＰＤ用のエピタキシャル構造を示している概略図である。この構造及びドーピングは図５３に図示しかつそれについて説明したものと同様であるか又は同一であるが、穴５４２２がＰ層５３０６の上部までで及び／又はＰ層５３０６内へＴ度入りかけるまでエッチングされていることが異なっている。

【０１０５】

図５５は、幾つかの実施例に基づく、高データレートＭＳ－ＰＤ用のエピタキシャル構造を示している概略図である。この構造及びドーピングは図５３及び５４に図示し且つそれらについて説明したものと同様であるか又は同一であるが、穴５５２２がＰ層５３０６内の少なくとも中間までエッチングされている点が異なっている。

【０１０６】

図５６は、幾つかの実施例に基づいて、ＭＤ－ＰＤに対するメサ寸法、穴直径、穴周期距離、及び格子パターンを示している表である。これらの例においては、該格子は六角形又は正方形とすることが可能である。該穴は円形、楕円、多角形とすることが可能である。該穴は、２０００ｎｍの周期で１３００ｎｍの直径、２０００ｎｍの周期で１５００ｎｍの直径、１０００ｎｍの周期で７００ｎｍの直径、９００ｎｍの周期で６３０ｎｍの直径である。動作波長は８００－９９０ｎｍで且つその物質はＳｉである。厚さが３－１００ｎｍの範囲の薄いパッシベーション層SiO_2を包含させることが可能である。該メサ寸法は、部分的にはＭＳ－ＰＤ（ボンドパッド及びコンタクト金属を除く）の容量を決定し，該ＭＳ－ＰＤのデータレートに依存して，５μｍ、１０μｍ、２０μｍ、２５μｍ、３０μｍ、４０μｍ、５０μｍ、及び８０μｍである。低容量及び短い走行時間は一層高いデータレートのＭＳ－ＰＤとさせる。

【０１０７】

図５７（Ａ）及び（Ｂ）は、幾つかの実施例に基づく、六角形及び正方形の格子穴パターンを示している概略図である。図５７（Ａ）は六角形格子パターンを示しており、且つ図５７（Ｂ）は正方形パターンを示しており，「ｄ」は各場合における周期である。幾つ

かの実施例によれば、これらのレイアウトは図５６に示したＭＳ－ＰＤに対する例示的パラメータに対して使用される。

【０１０８】

図５８は、幾つかの実施例に基づく、シリコンＭＳ－ＰＤ用のエピタキシャル層構造を示している概略図である。この構造の厚さ及びドーピングは以下の通りであり、即ち、Ｓｉ基板５８０２は１５０μｍであり、ＢＯＸ（埋込酸化物）層５８０４は２－４μｍの厚さであり、ＳｉＰ層５８０６は０．２－０．５μｍの厚さでドーピングは2×10^{20}／cm^3を越えており、Ｓｉｉ層５８０８は約１．５－２μｍの厚さで且つ意図的にはドーピングされておらず（5×10^{16}／cm^3未満のバックグラウンドドーピングを有している）、ＳｉＮ層５８１０は約０．２μｍの厚さで且つ2×10^{20}／cm^3を越えてドーピングされている。該Ｐ及びＮ層の高ドーピングは、例えば、1×10^{19}／cm^3を越えるものとすることが可能である。幾つかの実施例によれば、ＳｉＧｅＢ，ＳｉＧｅＣ，ＳｉＧｅＢＣ等の物質から構成されており厚さが５ｎｍ乃至５０ｎｍであるエッチストップ層を、マイクロストラクチャ型穴及び／又はメサのエッチング期間中に処理を助けるために、ＰＳｉ５８０６とＩＳｉ５８０８との間の界面に包含させることが可能である。高度にＰドープされているＳｉＧｅＢが使用される場合，構造はＮ－Ｉ－Ｐとすることが望ましい。Ｐ及びＮ領域の高ドーピングは，シート抵抗を減少させることに加えて、小数キャリアー寿命も減少させ、従ってＰ及びＮ領域において吸収されたフォトンは光電流に対しての寄与は最小とされる。Ｐ及びＮ領域における減少された小数キャリアー寿命は光発生されたキャリアーの高電界「Ｉ」領域への拡散を減少させ、該領域においては、少数キャリアーはアノード及びカソードへ掃引されて光電流に寄与する。

【０１０９】

図５９は、幾つかの実施例に基づく、ＭＳ－ＰＤの或る側面を示している概略図である。厚さ及びドーピングを含むその物質構造は、図５８に図示し且つそれについて説明したものと同様であるか又は同一である。図５９の場合には、層５９１０及び５９０６におけるＰ及びＮドーピングが交換されてＰ－Ｉ－Ｎ配置となっている。注意すべきことであるが、図５８又は５９のいずれかにおいて、その配置はＰ－Ｉ－Ｎ又はＮ－Ｉ－Ｐとすることが可能である。穴５９２２はＳｉＯ２５８０４へエッチングされており，且つＰ及びＮオーミックコンタクト５９２８及び５９３０が、夫々、Ｐ及びＮ層５９１０及び５９０６に対して形成されている。メサをエッチングして感光区域を画定し且つＰＩＮ構造の容量を画定している。メサ直径は、ＭＳ－ＰＤが設計されている（図５６に関して説明した如く）データレートに依存して１０μｍ乃至８０μｍの範囲である。２０－４０Ｇｂ／ｓの場合、該メサの直径は、典型的に、２０－４０μｍである。０．２μｍの厚さで2×10^{20}／cm^3を越えるドーピングＰ層５９１０は、約５０Ω未満のシート抵抗を有することが可能である。０．２μｍの厚さで2×10^{19}／cm^3を越えるドーピングのＮ層５９０６は約３５Ω未満のシート抵抗を与えることが可能である。該Ｐ及びＮ層の高ドーピングも、例えば、1×10^{18}／cm^3とすることも可能である。一層薄いＰ及びＮ層は一層高い百分率の光学パワーが該「Ｉ」層内となり且つ該Ｐ及びＮ層内において一層低い百分率となることを可能とし、それによりＭＳ－ＰＤの量子効率を最大とさせる。説明の便宜上、パッシベーション、ポリイミドブリッジ，ボンドパッド及びその他の処理ステップは図示していない。逆バイアス電圧がＰ及びＮコンタクト間に印加されて該「Ｉ」層内に高電界領域を形成する。電圧は、典型的に、約２－６Ｖの範囲である。図示した場合には，照射は上から垂直に又は垂直からずれた角度においてである。波長は８００－９９０ｎｍの範囲であるが，７８０ｎｍ等のその他の波長を使用することも可能である。公称波長は８５０ｎｍであるが，８１０－８３０，８３０－８５０，８５０，８８０，９３０－９６０，９６０－９９０などの波長を包含することも可能である。

【０１１０】

図６０は、幾つかの実施例に基づく、ＭＳ－ＰＤの或る側面を示している概略図である。物質構造の厚さ及びドーピングを含む該ＭＳ－ＰＤは図５８及び６０に図示し且つそれらについて説明したものと同様であるか又は同一である。この場合に，穴６０２２がＮ層

Samsung Exhibit 1090, Page 145 of 786
Samsung v. W&Wsens - IPR2025-00993

５９０６まで及び／又はその中にエッチングされているが、図５９におけるようにＳｉＯ２層５８０４までずーとエッチングされるものではない。従って、該Ｎ層における吸収は向上されておらず，その結果該「Ｉ」層における光学パワーの百分率を一層高いものとする場合がある。このことは該ＭＳ－ＰＤの量子効率を改善する傾向となる。ＳｉＯ２層５８０４は必要な場合と必要ではない場合とがある。

【０１１１】

図６１は、幾つかの実施例に基づく，ＭＳ－ＰＤの或る側面を示している概略図である。該ＭＳ－ＰＤは、物質構造の厚さ及びドーピングを包含して、図５８－６１に図示し且つそれらについて説明したものと同様であるか又は同一である。この場合に、該ＳｉＭＳ－ＰＤは基板側から照射される（本書においては、背面照射型又は底部照射型とも呼称される）。ビア６１７０がエッチングされてシリコン基板を除去し、且つＳｉＯ２層５８０４まで又は殆ど該ＳｉＯ２層まで又は該ＳｉＯ２層内へ又は該ＳｉＯ２層を貫通してエッチングされる。Ｓｉ基板５８０２を除去して８００－９９０ｎｍの波長範囲における光学損失を最小とさせる。Ｐ層５９１０表面上に反射器６１３２を製造し、それは該反射器６１３２がＰＩＮダイオードを短絡させないようにポリイミド、固体二酸化炭素、又はスピン・オン・ガラス（ＳＯＧ）等の充填プロセス（filler process）を包含することが可能である。注意すべきことであるが、反射器６１３２は正確に平面状であることは必要ではなく、穴を有する領域において凹状とさせることが可能であり、そのことは光波のトラッピングを向上させる場合がある。反射器６１３２は誘電体、ブラッグ反射器、導電性透明金属酸化物、銀，金又はその任意の組合せ等の金属又は合金とすることが可能である。インジウム錫酸化物（ＩＴＯ）を、ブラッグ反射器を形成するために非導電性誘電体と共に、使用することも可能である。金属及び／又は導電性酸化物は、更に、Ｐ層５９１０のシート抵抗を減少させることが可能であり、それにより寄生抵抗を減少させ且つＭＳ－ＰＤの変調型周波数応答（データレート）を改善させる。幾つかの実施例によれば、「Ｉ」層５８０８は反射器を具備する背面照射の場合に一層薄くさせることが可能である。何故ならば、光は量子効率を劣化させること無しに「Ｉ」層を介して少なくとも２回及び多分それ以上の回数走行することが可能であり、しかも同時にＭＳ－ＰＤの変調型周波数（データレート）応答を改善させるからである。その理由は、一層薄い「Ｉ」層の場合に，光発生されたキャリアーの走行時間は一層短いからである。フォトダイオードの周波数応答は、その容量及び抵抗（ＲＣ時間）及び走行時間（transit time）によって決定される。例えば或る高データレートに対して１００又はそれ以上のファクターより一層大きな高い向上された実効吸収長において光学的走行時間が重要となる場合がある。

【０１１２】

図６２は、幾つかの実施例に基づく、ＭＳ－ＰＤ用のＧｅ・オン・ＳｉＰＩＮエピタキシャル層構造を示している。厚さとドーピングとを含む物質構造は、図５８－６２に図示し且つそれらに基づいて説明したものと同様であるか又は同一である。この場合には、２×１０^{18}／ｃｍ^{3}を越えるドーピングを有するＮＳｉ層６２０２は０．２－２μｍの厚さを有することが可能である。Ｇｅ「Ｉ」層６２０８も設けられており、それは意図的にはドーピングされておらず、ドーピングは２×１０^{16}／ｃｍ^{3}未満であり且つ厚さは０．５－２μｍである。ドーピングが２×１０^{19}／ｃｍ^{3}を越える上部ＧｅＰ層６２１０は０．１－０．２μｍの厚さで形成される。幾つかの実施例によれば、Ｓｉ上のＧｅの良好な結晶成長を開始させるためにＮＳｉ層６２０６と「Ｉ」Ｇｅ層６２０８との間の界面において薄いＧｅバッファ層（不図示）を使用することが可能である。ＰおよびＮの高ドーピングも少数キャリアー寿命を減少させ、それにより全体的な光電流に対して寄与する場合がある光電界「Ｉ」領域内へ掃引される場合がある光発生されたキャリアーの拡散を最小とさせる。

【０１１３】

図６３は、幾つかの実施例に基づく、Ｇｅ・オン・ＳｉＭＳ－ＰＤを示している。物質構造の厚さとドーピングとを含んで、該ＭＳ－ＰＤは図５８－６２に図示し且つそれらについて説明したものと同様であるか又は同一である。穴６３２２がＳｉＯ２層５８０４ま

でエッチングされており、又は該穴はＮＳｉ層６２０８までエッチングさせることが可能であり、その場合には、ＳｉＯ２層５８０４は必要である場合と必要ではない場合とがあり、且つ該ＭＳ－ＰＤは上部即ち正面（エピタキシャル表面）から照射される。１１００乃至１８００ｎｍの波長範囲におけるフォトンの吸収は該Ｓｉ領域よりも殆どが該Ｇｅ領域においてである。ＰＧｅ層６２１０を薄く維持することによって、該フォトンの大きな百分率がＧｅ「１」層６２０８において吸収され、それにより量子効率を増加させる。ＧｅとＳｉとの間の高い屈折率差は、該穴をＳｉＮ層６２０６の上部までエッチングさせるに過ぎないことを必要とする場合がある。しかしながら、本例においては、穴６３２２はＳｉＯ２層５８０４までエッチングされている。ＮＳｉ層６２０６は、本例においては、最大で２μｍの厚さとすることが可能であり、且つ５００Ω未満のシート抵抗を与えるために$1\times10^{18}/cm^3$の範囲のドーピングとすることが可能である。８５０ｎｍ動作の場合、又は８００－９９０ｎｍの範囲における波長の場合、薄いＮＳｉ層は該ＩＧｅ領域において吸収されるフォトンの百分率を増加させることが可能である。ドーピングが$2\times10^{18}/cm^3$を越える０．２μｍ厚さのＮＳｉ層は５００Ω未満のシート抵抗を与え且つ少数キャリアー寿命を減少させる。２μｍの厚いＮＳｉ層も８００－９９０ｎｍ又は８００－１８００ｎｍの波長範囲に対して使用することが可能である。何故ならば，８００－９９０ｎｍの範囲における波長に対しては、Ｇｅは２μｍの長さにわたり該フォトンの９０％を越えるものを吸収するからである。従って、該フォトンの５％未満が該ＮＳｉ層に到達する。８５０ｎｍの波長において、１％未満が該ＮＳｉ層へ到達し、且つ９９０ｎｍにおいては３％未満がそれに到達する。

【０１１４】

或る場合には、８００－９９０ｎｍの波長範囲に対して、マイクロストラクチャ型穴は吸収を向上させるために支配的に使用することができない場合があり、寧ろＧｅ層内に部分的に又は完全にエッチングされた穴での容量を減少させるために使用される場合がある。更に、穴が必要ではない場合があり且つバルクＧｅが使用される場合がある。幾つかの実施例によれば、マイクロストラクチャは反射を減少させるためにも使用することが可能である。

【０１１５】

図６４は、幾つかの実施例に基づく，Ｇｅ・オン・ＳｉＭＳ－ＰＤを示している。物質構造の厚さ及びドーピングを含んで、該ＭＳ－ＰＤは図５８－６３に図示し且つそれらについて説明したものと同様のものであるか又は同一のものである。この場合には、穴６４２２がＳｉ層６２０６までエッチングされている。Ｇｅに対する屈折率は約４であり且つＳｉに対する屈折率は約３．４５である。この屈折率における差異は該Ｇｅ領域において十分に向上された吸収を与える場合がある。この場合に、ＳｉＯ２層５８０４は必要でない場合があり且つ該ＭＳ－ＰＤはＢＯＸ層５８０４無しでＳｉウエハ上に成長させる場合がある。１１００－１８００ｎｍの波長範囲に対して、Ｓｉは許容可能に低い光学損失を有しており且つ該吸収の殆どは該Ｇｅ領域においてのものである。上部照射型ＭＳ－ＰＤの場合、該ＰＧｅ層は薄くさせることが可能であり、従って該フォトンのバルクは該ＩＧｅ領域において吸収され、そのことは量子効率を増加させる。該Ｐ層のシート抵抗を更に減少させるためにＰＧｅ層６２１０と関連してＩＴＯ（インジウム錫酸化物）を使用する場合がある。

【０１１６】

図６５は、幾つかの実施例に基づく，Ｇｅ・オン・ＳｉＭＳ－ＰＤを示している。該ＭＳ－ＰＤは、物質構造の厚さ及びドーピングを含んで、図５８－６４に関して図示し且つそれらについて説明したものと同様であるか又は同一である。この場合には、該ＭＳ－ＰＤは背面即ち底部照射型である。この構造は０．２μｍの薄いＮＳｉ層を使用して８００－１８００ｎｍの波長範囲に対して非常に良好である。８００ｎｍにおける波長を有するフォトンの３％未満がＮＳｉ層６２０６において吸収される。更に、１μｍのＧｅの単一パス即ち通過において、９９０ｎｍフォトンの８５％を越えるものが吸収される。ダブルパス即ち二重通過においては、９９０ｎｍフォトンの９５％を越えるものが吸収される。

Samsung Exhibit 1090, Page 147 of 786
Samsung v. W&Wsens - IPR2025-00993

ＧｅＩがＮＳｉ上に成長されている背面照射型ＭＳ－ＰＤにおいては、該ＰＧｅ層上の反射器６５３２と共に、該フォトンの二重及び／又は多重の通過が一層薄いＩ吸収層６２０８を可能とさせ、そのことは光発生された電子及び正孔の走行時間を減少させる。４０Ｇｂ／ｓ又はそれ以上の一層高い帯域幅を有するフォトダイオードを得ることが可能である。穴６３２２はＳｉＯ２層５８０４へエッチングさせることが可能であり、又はＳｉ層６２０６へエッチングさせることが可能である（図６４に示した如く）。マイクロストラクチャ型穴アレイの場合、向上された吸収は１１００－１８００ｎｍの波長において発生することが可能である。例えば、１５５０ｎｍにおいて、１μｍ厚さのバルクＧｅを介してのダブルパス即ち二重通過で、９％未満が吸収され、一方、該Ｇｅ層内にマイクロストラクチャ型穴がある場合には、３０％より大きな吸収を達成することが可能であり、且つ、幾つかの場合においては、５０％より大きな吸収を達成することが可能である。或る場合には、ＧｅＩ層を具備するＭＳ－ＰＤにおける吸収は、１μｍ厚さのＧｅにおける二重通過に対して又は２μｍ厚さのＧｅＭＳ－ＰＤにおける単一通過に対して、１５５０ｎｍにおいて７０％より大きなものを達成することが可能である。

【０１１７】

該ＭＳ－ＰＤは次の層を有することが可能であり、即ち、Ｇｅ（又はＳｉＧｅ）Ｐ層６２１０は約０．１μｍの厚さで２×１０^{19}／ｃｍ^{3}を越えるものへドーピングさせることが可能であり、ＧｅＩ（吸収層）６２０８は０．５－２．０μｍの厚さで意図的にドーピングしないものとすることが可能であり（５×１０^{15}／ｃｍ^{3}未満）、且つ、最後に、ＳｉＮ層６２０６は０．２－０．５μｍの厚さで２×１０^{19}／ｃｍ^{3}を越えるものへドーピングさせることが可能である。更に、Ｓｉ基板を除去するためのビアエッチング期間中、該ＳｉＯ２層は不変のままとさせるか、部分的にエッチングさせるか、又は該ＳｉＯ２を除去するために完全にエッチングさせることが可能である。

【０１１８】

図６６は、幾つかの実施例に基づく、Ｇｅ・オン・ＳｉＰＤを示している概略図である。該ＰＤは、物質構造の厚さ及びドーピングを含めて、図５８－６５に図示し且つそれらについて説明したものと同様である。図６６はフリップチップとして配置されたものを示しているが、該ＰＧｅ層に起因して僅かに劣化するが正面照射型配置とすることも可能である。該ＰＤは、マイクロストラクチャ型穴アレイが無い場合の図６４に示したＭＳ－ＰＤと類似している。８００－１３００ｎｍにおける動作のために図示した如きエピタキシャル構造を具備するＧｅ・オン・Ｓｉフォトダイオードは、特に１３００ｎｍ波長領域に対してのダブルバウンス即ち二重跳ね返りを利用しており尚且つ高いデータレート動作を維持している。該ＰＤはＳｉＧｅＢｉＣＭＯＳと集積化させることが可能である。幾つかの実施例によれば、該ＳｉＯ２層が省略される。半田バンプ技術で、該ＰＤは、例えば図４４－５２に示した如く、その他の実施例に対して上述したと如くに、ＰＣＢ上に直接マウントさせたフリップチップとさせることが可能である。幾つかの実施例によれば、該ＰＤは次の層を有することが可能であり、即ち、約０．１μｍの厚さで２×１０^{20}／ｃｍ^{3}を越えてドープされているＧｅ（又はＳｉＧｅ）Ｐ層６２１０、０．５－２．０μｍの厚さで意図的にはドーピングしていない（５×１０^{15}／ｃｍ^{3}未満）ＧｅＩ（吸収層）６２０８、及び最後に０．２－０．５μｍの厚さで２×１０^{19}／ｃｍ^{3}を越えてドーピングされているＳｉＮ層６２０６である。更に、Ｓｉ基板を除去するためのビア６６７０のエッチング期間中に、ＳｉＯ２層５８０４は不変のままとさせるか（図６５に示した如く）、部分的にエッチングするか、又はＳｉＯ２を除去するために完全にエッチング（図６６に示した如く）させることが可能である。該ＳｉＯ２層が完全にエッチング除去される場合には、反射を最小とするために反射防止層（不図示）を該ＳｉＮ層へ付与することが可能である。

【０１１９】

図６７は、幾つかの実施例に基づく、Ｇｅ・オン・ＳｉＰＤを示している概略図である。該ＰＤは、物質構造の厚さ及びドーピングを含んで、図５８－６６に図示し且つそれらについて説明したものと同様である。この場合には、装置ＰＩＮ接合容量を減少させるた

めにボイド６７２２が形成されている。ボイド６７２２は、或る量だけ容量を減少させるために十分な量の物質を除去するために、該Ｇｅ層内に部分的にエッチングさせることが可能である。該容量減少は、ボイドが無い同様のＧｅ・オン・ＳｉＰＤと同じデータレート帯域幅を維持しながら一層大きな面積のＰＤとすることを可能とする。その一層大きな面積のＰＤは、フォトダイオードに対するオプチカルファイバー及び／又は光源のミスアライメント即ち不整合において一層大きな公差を可能とさせる。データレート帯域幅はＲＣ時間と走行時間とによって決定される。この構造の説明してきた全ての構造との統合は、半田バンプ技術と共にＰＣＢへ直接取り付けることが可能なＴＩＡ等のエレクトロニクスで可能である。幾つかの実施例によれば、この構造に対する動作波長は８００－１３００ｎｍの範囲であり且つデータレートは４０Ｇｂ／ｓを越えるものである。

【０１２０】

注意すべきことであるが、ＢＯＸ構造を使用することは必要ではない。本ＰＤは次のような層を有することが可能であり、即ち、約０．１μｍの厚さで2×10^{18}／cm^3を越えてドーピングされているＧｅＰ層６２１０、０．５－１．０μｍの厚さで意図的にはドーピングしていない（5×10^{15}／cm^3未満）Ｇｅ Ｉ（吸収層）６２０８、及び最後に０．２－０．５μｍの厚さで2×10^{18}／cm^3を越えてドーピングされているＳｉＮ層６２０６、及び２－４μｍの埋込酸化物層５８０４である。

【０１２１】

図６８は、幾つかの実施例に基づく、マイクロストラクチャ型アバランシェフォトダイオード（ＭＳ－ＡＰＤ）の或る側面を示している概略図である。該ＭＳ－ＡＰＤは次の層を有することが可能であり，即ち、約０．１－０．２μｍの厚さで2×10^{19}／cm^3を越えてＰドーピングされているＳｉＰ層６８１０、０．５－２．０μｍの厚さで意図的にはドーピングされていない（5×10^{15}／cm^3未満）ＳｉＩ（吸収層）６８０８、０．２－０．５μｍの厚さで2×10^{19}／cm^3を越えてｎドーピングされているＳｉＮ層６８０６、及びＳｉ基板６８０２上の２－４μｍの厚さの埋込酸化物層６８０４、である。該ＭＳ－ＡＰＤ装置は２つの付加的な層、即ち電荷層及び増倍層、を有している。電荷層６８２０は吸収Ｉ層６８０８の直下である。ＳｉＰ電荷層６８２０は約1.8×10^{17}／cm^3へドーピングされており且つ約０．１μｍの厚さを有している。該電荷層の直下は該ＭＳ－ＡＰＤの増倍層６８１８である。ＳｉＩ層６８１８は意図的にはドーピングされておらず（1×10^{15}／ｃｍ未満）且つ約０．５μｍの厚さを有している。ビア６８７０がシリコン基板内を該SiO_2層までエッチングされており（反射を最小とさせるために反射防止コーティングを適用することが可能）、且つ８００－９９０ｎｍの範囲の波長を有する光が該ビアを介して適用される。該ＭＳ－ＡＰＤの上部表面上の反射器６８３２は吸収用「Ｉ」層６８０８を介してのフォトンの二重／多重通過を与える。一つの利点は一層薄い吸収層であり、それは一層短い走行時間とさせる。従って、該ＭＳ－ＡＰＤのデータレート帯域幅は向上される。マイクロストラクチャ型穴アレイ６８２２はSiO_2層６８０４まで及び／又は殆ど該SiO_2層までエッチングされる。Ｐ及びＮコンタクト６８２８及び６８３０は半田バンプが付与されるべき同一の表面上に示されており、従って、該ＭＳ－ＡＰＤはセラミックマルチチップ担体上及び／又はプリント回路基板上に直接フリップチップマウントさせることが可能である。説明の便宜上、最も基本的な処理ステップのみが示されている。パッシベーション、ボンドパッド、ポリイミド／スピン・オン・ガラス平坦化、反射防止コーティング、等の付加的なステップ又は要素は図示していない。更に、ビア６８７０のエッチング期間中、Ｓｉ基板を除去した後に、該SiO_2層はＭＳ－ＡＰＤ又はＭＳ－ＰＤのいずれかの構造のために部分的にエッチング除去するか又は完全にエッチング除去することが可能である。反射器６８３２が無い場合には、光学信号は上部表面から入射することも可能である。

【０１２２】

図６９は、幾つかの実施例に基づく、マイクロストラクチャ型アバランシェフォトダイオード（ＭＳ－ＡＰＤ）の或る側面を示している概略図である。該ＭＳ－ＡＰＤは、物質構造の厚さ及びドーピングを含んで、図６８に図示し且つそれについて説明したものと同

様である。マイクロストラクチャ型穴アレイ６９２２は、該ＡＰＤ構造の電荷層６８２０、増倍層６８１８、及び／又はＮ層６８０６までエッチングされる。穴６９２２は該ＳｉＯ２層まですーとエッチングされるものではない。光が該ＳｉＯ２までシリコン基板が除去されているビア６９７０を介して照射される。光がＮＳｉ層６８０６上に直接入射するように該ＳｉＯ２層もエッチングすることが可能である。このことは全ての底部照射型ＭＳ－ＰＤ及びＭＳ－ＡＰＤ装置に対して適用可能であり、その場合には反射防止コーティングを直接Ｓｉへ適用することが可能である。８００－９９０ｎｍの範囲の波長の場合、約０．２μｍの薄いＮＳｉ層６８０６が吸収用「Ｉ」層６８０８から離れた領域における吸収を減少させるために好適である。光は上部／正面から入手することも可能であり、その場合には反射器６８３２は除去される。この様な場合には、ビアを省略する場合があり且つ該Ｓｉ「Ｉ」層は３０％を越える量子効率のために１．５－２μｍへ増加させる場合がある。幾つかの場合においては、量子効率は５０％を超えるものであり、幾つかの場合には、７０％を超えるものであり、且つ幾つかの場合には、８０％を超えるものである。該アバランシェの増倍係数即ち利得は２を越えるものとすることが可能である。幾つかの場合には、その利得は５を超えるものである。幾つかの場合には、それは１０を超えるものである。更なる幾つかの場合には、それは１５を超えるものであり、且つ更に幾つかのその他の場合には、該利得は２０を超えるものである。データレート帯域幅は１０Ｇｂ／ｓを超えることが可能である。幾つかの場合には、該帯域幅は１５Ｇｂ／ｓを超えるものであり、且つ幾つかの場合には、３０Ｇｂ／ｓを超えるものである。更に、該ＳｉＯ２層は完全に又は部分的に除去することが可能であり、及び／又はそれはＭＳ－ＰＤ及びＭＳ－ＡＰＤのためにＳｉで充填されているか又はされていないボイドを有することが可能であり、且つ背面／底部照射用に使用されるビアを形成するためのＳｉ基板の除去期間中にＳｉＧｅＢ，ＳｉＧｅＣ又はＳｉＧｅＢＣ等のエッチストップ層を使用することが可能である。

【０１２３】

図７０は、幾つかの実施例に基づき、該ＳｉＯ２層が無いＭＳ－ＡＰＤを示している概略図である。該ＭＳ－ＡＰＤは、物質構造の厚さ及びドーピングを含んで、図６８－６９に図示し且つそれらについて説明したものと同様である。エッチストップ層７０３４はＳｉＧｅ又はＳｉＧｅＣ又はＳｉＧｅＢ（該ＳｉＧｅは約１％のＧｅを有しており且つ$1\times10^{20}/cm^3$を越えてボロンで高度にドープされている）で、且つ厚さは０．１乃至２μｍの範囲である。ＳｉＧｅＢＣはＳｉ基板６８０２上、及び／又はＮＳｉ層６８０６等のＳｉエピタキシャル層上に成長させることが可能である。幾つかの実施例によれば、該ＭＳ－ＡＰＤは次のような厚さ及びドーピングレベルを有しており、即ち、ＳｉＮ層６８０６は０．２乃至１μｍの範囲の厚さ及びドーピングレベルを有しており、ＳｉＮ層６８０６は０．２乃至１μｍの範囲の厚さ及び$2\times10^{19}/cm^3$を越えるものから$2\times10^{20}/cm^3$を越えるものの範囲のドーピングを有しており、ＳｉＩ増倍層６８１８は意図的にはドーピングされておらず（$1\times10^{16}/cm^3$未満）且つ約０．５μｍの厚さを有しており、ＳｉＰ電荷層６８２０は約$1.8\times10^{17}/cm^3$にドーピングされており且つ約０．１μｍの厚さを有しており、ＳｉＩ吸収層６８０８は意図的にはドーピングされたおらず（$5\times10^{15}/cm^3$未満）且つ０．５－１．０μｍの厚さを有しており、且つＳｉＰキャッピング層６８１０は$2\times10^{20}/cm^3$を越えてドーピングされており且つ約０．１μｍの厚さを有している。幾つかの実施例によれば、複数のエッチストップ層を使用することが可能である。例えば、ＳｉＩ増倍層６８１８とＳｉＮ層６８０６との界面に別のエッチストップ層を形成することが可能である。該エッチストップ層の厚さは１ｎｍ乃至１００ｎｍの範囲に亘ることが可能であり、且つ隣接する層の電気的特性と一致させるためにＰ又はＮへドーピングさせるか又は意図的にドーピングしないものとすることが可能である。光学信号の波長は８００乃至９９０ｎｍの範囲にわたることが可能であり且つ背面側から照射される場合には、ＳｉＯ２／Ａｇ等の誘電体から反射器を形成することが可能である。幾つかの実施例によれば、反射器６８３２は、ＳｉＯ２とＨｆＯ２、又はＡｇ，Ａｕ及び／又はＰｔと共にＩＴＯ等の屈折率が異なる２つの誘電

体からなるブラッグ反射器である。反射器６８３２は吸収されなかった信号フォトンを吸収用ＳｉＩ領域６８０８を介して二重及び／又は多重回通過させるべく反射させるために使用される。更に，該装置は正面照射型とすることが可能であり、その場合には反射器６８３２は省略され且つ吸収用ＳｉＩ層６８０８は量子効率を最適化させるために１．５－２μｍへ厚くされる。幾つかの実施例によれば，該正面／上部照射型ＭＳ－ＡＰＤにビアを包含させることも可能である。同様に、或るＭＳ－ＰＤは、該ＳＩＰ電荷層及びＳｉＩ増倍層を省略して、この構造を使用することも可能である。正面及び背面照射型ＭＳ－ＰＤが有益的である場合がある。何故ならば、Ｓｉ基板の除去は屈折率コントラストを改善し且つ該マイクロストラクチャにおいて改善された吸収係数を有しており、そのことは量子効率を改善させるからである。

【０１２４】

該Ｐ及びＮ層の高ドーピングは、シート抵抗を減少させると共に該Ｐ及びＮ層内の少数キャリアーの寿命を減少させて、ＭＳ－ＰＤ／ＡＰＤのデータレート応答（周波数応答とも呼称される）において劣化を発生される場合がある高電界ＳｉＩ吸収層内への少数キャリアーの拡散を減少させる。該マイクロストラクチャ型穴アレイは、該ＳｉＧｅＣ及び／又はＳｉＧｅＢストップ層まで及び／又は穴エッチング期間中及び／又はビアエッチング期間中のいずれかで該ストップ層を超えてエッチングさせることが可能である。該エッチストップ層も該穴エッチングの後又は該ビアエッチング期間中に完全に又は部分的に除去することも可能である。この様に、ＳｉＧｅＣ，ＳｉＧｅＢＣ又はＳｉＧｅＢ層は背面照射型ＭＳ－ＰＤ／ＡＰＤ用の光学系路中には無い。注意すべきことであるが、Ｇｅが約１％（例えば、$Si_{0.99}Ge_{0.01}$）であるＳｉＧｅＢにおいては，そのバンドギャップはほぼＳｉのものと同じである。更に、図６９における如く、該マイクロストラクチャ型穴アレイは、該吸収用ＳｉＩ層に対応する深さへ及び／又は該ＳｉＩ吸収層より大きく且つ部分的にアバランシェ領域内へ入る深さへエッチングさせることが可能である。

【０１２５】

図７１は、幾つかの実施例に基づき、Ｇｅ・オン・Ｓｉマイクロストラクチャ型アバランシェフォトダイオード（ＭＳ－ＡＰＤ）を示している概略図である。該ＭＳ－ＡＰＤは、物質構造の厚さ及びドーピングを含んで、図６８－７０に図示し且つそれらについて説明したものと同様である。ＧｅＩ吸収層７１０８は意図的にはドーピングされておらず（5×10^{15}／cm^3未満）且つ０．５－２．０μｍの厚さを有している。上部ＧｅＰキャッピング層７１１０は2×10^{19}／cm^3を超えてドーピングされており且つ約０．１μｍの厚さを有している。マイクロストラクチャ型穴アレイ７１２２は、ＳｉＰ電荷層６８２０まで又は該ＳｉＰ層直前までエッチングされている。代替的に、穴７１２２はＳｉＰ電荷層６８２０内へ及び／又はＳｉ増倍層６８１８内へエッチングさせることが可能である。ビア６９７０がエッチングされて光学経路からＳｉ基板を除去している。該SiO_2層は不変のままとするか、部分的にエッチングさせるか又は完全に貫通してエッチングさせることが可能であり、又はSiO_2の無いＮＳｉ基板を使用することが可能である。ＳｉＮ層６８０６が露出される場合には、反射を最小とさせるために反射防止層（不図示）を付与することが可能である。波長範囲は、例えば、８００－１８００ｎｍ，１３００－１６００ｎｍ，８１０－８８０ｎｍ，９３０－９９０ｎｍとすることが可能である。穴寸法及び周期は或る波長範囲に対して最適化させることが可能である。ＰＧｅ又はＳｉＧｅ層７１１０上に反射器６８３２を形成することが可能である。該反射器６８３２は誘電体及び金属、ＩＴＯ（インジウム錫酸化物又は同様の透明導電性酸化物）及び金属、ブラッグ反射器のような全誘電体，又はそれらの任意の組合せから構成することが可能である。反射器６８３２は、１回目の通過で吸収されなかったフォトンを２回又は多数回の通過のために吸収用ＧｅＩ層７１０８へ向かって反射させて戻す。単一通過でのフォトダイオードと比較して一層薄いＧｅＩ吸収層７１０８を使用することが可能である。該一層薄いＧｅＩ層は一層短い走行時間とさせ、従って一層高いデータレートとさせる。Ｇｅ・オン・Ｓｉの成長はＧｅバッファ層を使用する場合があり、それはＧｅの高品質結晶成長を開始させるために成長される。例えば、Kang et al.の１．３ＡＥｍ光検知用のエピタキ

シャル的に成長されたＧｅ／Ｓｉアバランシェフォトダイオード（Epitaxially-grown Ge /Si avalanche photodiodes for 1.3μm light detection）、Ｖｏｌ．１６、Ｎｏ．１３／オプティックスエクスプレス（OPTICS EXPRESS）９３６５（２００８）（以後、「Kang et al」と呼称する）を参照すると良く、尚それを引用により本書に取り込む。１２００－１７５０ｎｍの波長範囲の場合、Ｓｉはこれらの波長においては殆ど透明であるからビア７２７０は必要ではない。更に、反射器６８３２が無い場合には、光学信号は上部表面から入射することが可能であり且つＧｅ「ｉ」層７１０８は厚さを約２ミクロンへ増加させることが可能である。

【０１２６】

図７２は、幾つかの実施例に基づく、Ｇｅ・オン・ＳｉマイクロストラクチャＳ型アバランシェフォトダイオード（ＭＳ－ＡＰＤ）を示している概略図である。該ＭＳ－ＡＰＤは、物質構造の厚さ及びドーピングを含んで、図６８－７１に図示し且つそれらについて説明したものと同様である。この場合には、マイクロストラクチャ穴アレイ７２２２がＳｉＯ$_2$層６８０４までエッチングされている。幾つかの実施例によれば、穴７２２２はＳｉＯ$_2$層６８０４の十分の数μｍ内までエッチングされ且つビア７２７０は該ＳｉＯ$_2$層までエッチングされる。該ＳｉＯ$_2$層は該ビアエッチング期間中に不変のままであるか、部分的にエッチングされるか、又は完全に貫通してエッチングさせることが可能である。背面側から入射する光は８００－１８００ｎｍの範囲の波長を有している。例えば６３０－７８０ｎｍなどのその他の波長を使用することも可能である。該Ｓｉ層内において幾らかの光発生されたキャリアーが存在する場合があるが、光発生されたキャリアーのバルクはＧｅｉ層７１０８においてであり、とりわけ８００－１８００ｎｍの波長範囲においてであって、特に１１００－１８００ｎｍの波長範囲においてである。該エピタキシャル構造は図７１に示したものに類似しており、というのも、該ＧｅＰ層上の反射器６８３２が光をＧｅｉ吸収層へ向けて反射して戻すからである。該ＳｉＯ$_2$層の除去は該マイクロストラクチャ型半導体穴間に高い反射指数コントラストを可能とさせ、そのことは該マイクロストラクチャ型穴アレイと空気の光収集特性を改善させることを可能とする。又、ＳｉＯ$_2$－空気界面及びＳｉＯ$_2$－半導体界面において発生する場合がある反射が取り除かれている。正面照射型ＭＳ－ＡＰＤの場合、反射器６８３２は除去され且つＧｅｉ吸収層７１０８が１－２μｍの範囲へ厚くされる。該ビア及びＳｉＯ$_2$の除去は正面側照射型ＭＳ－ＡＰＤのために行うことが可能である。該アバランシェ層、Ｐ電荷及びＩ増倍、を除去することによって、該ＭＳ－ＡＰＤはＭＳ－ＰＤとなる。

【０１２７】

図７３は、幾つかの実施例に基づく、エッチストップ層を具備するＧｅ・オン・Ｓｉマイクロストラクチャ型アバランシェフォトダイオード（ＭＳ－ＡＰＤ）を示している概略図である。該ＭＳ－ＡＰＤは、物質構造の厚さ及びドーピングを含んで、図６８－７２に図示し且つそれらについて説明したものと同様である。ＳｉＧｅ，ＳｉＧｅＣ，ＳｉＧｅＢ，ＳｉＧｅＢＣ等のエッチストップ層７３３４をＳｉウエハ上に成長させる。注意すべきことであるが、Ｓｉ基板（ウエハ）６８０２は、既に、ＮＳｉエピタキシャル層、その後のＡＰＤ層、その他のバッファ層，スペーサ層，又はその他のエッチストップ層等の夫々の層（不図示）をその上に有している場合があり、それらは良好な結晶成長及び処理再現性を促進させるものである。基本的なＡＰＤ層は、厚さが０．２乃至０．５μｍの範囲でドーピングが2×10^{19}／ｃｍ^{3}をこえるものから2×10^{20}／ｃｍ^{3}を越えるものの範囲であるＳｉＮ層６８０６、意図的にはドーピングされておらず且つ厚さが約０．５μｍであるＳｉｉ増倍層６８１８、約１．８$\times10^{17}$／ｃｍ^{3}へドーピングされており且つ厚さが約０．１μｍであるＳｉＰ電荷層６８２０、意図的にはドーピングされておらず且つ厚さが０．５－１．０μｍであるＧｅｉ吸収層７１０８、及びドーピングが2×10^{20}／ｃｍ^{3}を越えており且つ厚さが約０．１μｍであるＧｅ又はＳｉＧｅＰキャッピング層７１１０である。マイクロストラクチャ型穴アレイは特定の波長範囲に対して最適化されている穴直径及び周期でエッチングされている。特定の波長範囲は次のものを包含しており、即ち、８００－８６０，８６０－８８０，８８０－９２０，９２０－９９０

，９９０－１１００，１１００－１３５０，１３５０－１４５０，１４５０－１５５０，１５５０－１６５０，１６５０－１８００ｎｍである。穴及びメサのパッシベーションは説明の便宜上割愛してあるが、Ｋａｎｇ　ｅｔ　ａｌの中にそれらの例が示されている。文献においてはその他のパッシベーション方法が存在している。光はビア７３７０を介して背面側から入射し、その場合は該エッチストップ層を除去することが可能である。光は正面側から入射することも可能であるが、吸収ＧｅＩ層７１０８の厚さは約１－２μｍの範囲に増加される。正面側照射型ＭＳ－ＡＰＤ／ＰＤの場合、例えば、半導体マイクロストラクチャと空気との間の反射指数コントラストを増加させるために該ビアを実現させることも可能である。平坦化層、ブリッジ層、ボンドパッド、及び充填物等のその他の層も説明の便宜上図示していない。

【０１２８】

図７４は、幾つかの実施例に基づく、Ｇｅ・オン・ＳｉマイクロストラクチャＳｉ型アバランシェフォトダイオード（ＭＳ－ＡＰＤ）を示している概略図である。該ＭＳ－ＡＰＤは、物質構造の厚さ及びドーピングを含んで、図６８－７３に図示し且つそれらについて説明したものと同様であるが、Ｐコンタクト層における光キャリアーの吸収を減少させるために該ＧｅＰ層がＳｉＧｅ又はＳｉＧｅＣのＰ層７４１０で置換されている点が異なっている。ＳｉＧｅ及び／又はＳｉＧｅＣはＧｅよりも一層大きなバンドギャップを有しており、従って同じ厚さの場合に吸収係数はＧｅにおける場合よりも一層小さい。例えば、Kolodzey et al.の「Ｓｉ基板上に成長させたＳｉＧｅＣ合金の光学的及び電子的特性（Optical and electronic properties of SiGeC alloys grown on Si substrates）」、ジャーナルオブクリスタルグロス（Journal of Crystal Growth）１５７，３８６－３９１（１９９５）（以後「Ｋｏｌｏｄｚｅｙ　ｅｔ　ａｌ」と呼称する）を参照すると良く、尚それを引用により本書に取り込む。例えば、Ｋｏｌｏｄｚｅｙ　ｅｔ　ａｌから、$Si_{0.98}Ge_{0.02}$の場合、バンドギャップは、Ｓｉが１．１１ｅＶであり且つＧｅが０．６６ｅＶであるのと比較して、１．３ｅＶ（直接）である。ＳｉＧｅ合金はＳｉとＧｅとの間のバンドギャップを与え、従ってＧｅに対してのＳｉの何らかの付加はバンドギャップを増加させ且つ該Ｐ層における吸収を減少させる。幾つかの実施例によれば、このＰ層置換技術はここに示し且つ記載した全てのＭＳ－ＰＤ／ＡＰＤ構造に対して適用される。特に、ＧｅＰ層はＳｉＧｅＰ及び／又はＳｉＧｅＣＰ層で置換される。幾つかの更なる実施例によれば、ここに示し且つ記載した全てのＭＳ－ＰＤ／ＡＰＤにおいて、該ＳｉＰ及びＮ層も完全に又は部分的にＳｉＧｅＣ　Ｐ及びＳｉＧｅＣ　Ｎで置換させることが可能であり、そのことは該ＭＳ－ＰＤ／ＡＰＤのＰ及びＮ領域における光学信号の吸収を減少させる。幾つかの場合には、本発明における光学フォトンの吸収を減少させるために、Ｓｉである該ＡＰＤの増倍領域もＳｉＧｅＣ　Ｉで置換させることが可能である。或る波長１２００－１７５０ｎｍにおいては、Ｓｉは殆ど透明であり、ビア７３７０及びエッチストップ層７３３４のいずれか一方又は両方が必要ではない。この場合には、ＮＳｉ基板を使用してその背面を研磨し且つ反射防止コーティングを行う。

【０１２９】

図７５は、幾つかの実施例に基づく、ＭＳ－ＰＤ用の別のＳｉＮＩＰエピタキシャル層構造を示している概略図である。穴７５２２が約２．３μｍの深さまでエッチングされており且つＳｉＰ層７５０６の前及び／又は後の十分の数ミクロンで終端することが可能である。ドーピング及び厚さはほぼ次の通りであり、即ち、ＳｉＰ基板７５０２、$1\times10^{19}/cm^3$を越えるものとすることも可能であるが$2\times10^{20}/cm^3$を越えるＰドーピングで０．２μｍ（又は０．１－１μｍの範囲）のＳｉＰ層７５０６、意図的にはドーピングされておらずバックグラウンドドーピングが$5\times10^{15}/cm^3$未満であり且つ幾つかの場合には$5\times10^{15}/cm^3$未満であって厚さが約２又は１－２．５μｍの範囲内であるＳｉＩ層７５０８、ドーピングが$2\times10^{19}/cm^3$を越えており且つ厚さが約０．３μｍ又は０．２－０．５μｍの範囲内であるＮＳｉ層７５１０である。Ｎコンタクト７５２８はＳｉＮ層７１５０上にある。Ｐコンタクトは、コンタクト７５３０における如くＳｉＰ基板の上部表面上とすることが可能であり、及び／又はコンタクト７５

３２における如く該基板の底部／背面側上とすることが可能である。ＰＩＮ接合区域、従って容量、を画定するためにメサエッチングが使用される。メサはＰ層７５０６まで及び／又はＰ基板７５０２までエッチングされ且つＰコンタクト７５３０はＳｉＰ層７５０６上及び／又はＳｉＰ基板７５０２背面側７５３２上にデポジット即ち付着させることが可能である。幾つかの実施例によれば、その他の電気的分離を使用することも可能であり、例えば、ＰＩＮ区域を画定するための陽子衝撃（proton bombardment）又はＰＮ接合ドーピング又はトレンチドーピング等のその他のドーピング技術である。この構造において、光は約８００－９９０ｎｍの範囲の波長で正面側から入射する。周期が２０００ｎｍで穴直径が１３００ｎｍ、及び周期が２０００ｎｍで穴直径が１５００ｎｍを六角形及び／又は正方形格子パターンのいずれかで使用することが可能である。幾つかの実施例によれば、穴直径の範囲は約６００ｎｍ乃至１５００ｎｍであり且つ周期の範囲は約９００乃至２５００ｎｍである。

【０１３０】

図７６（Ａ）－（Ｃ）は、幾つかの実施例に基づく、ＭＳ－ＰＤ用の埋込酸化物上のＳｉＮ－ｉ－Ｐエピタキシャル層を示している各概略図である。図７６（Ａ）において、穴７６２２がＳｉＰ層７６０６へエッチングされており、該ＳｉＰ層内へ部分的に及び／又はSiO_2層７６０４へエッチングされている。ドーピング及び厚さはほぼ次の通りであり、即ち、基板７６０２内のＳｉＢＯＸ（埋込酸化物）７６０４、Ｐドーピングが$2\times10^{19}/cm^3$を越えている１μｍ（又は０．１－１μｍの範囲）のＳｉＰ層７６０６、意図的にはドーピングしておらず且つバックグラウンドドーピングが$5\times10^{15}/cm^3$未満であり且つ幾つかの場合には$5\times10^{13}/cm^3$未満であって厚さが２μｍ又は０．５－２．５μｍの範囲であるＳｉＩ層７６０８、及びドーピングが$2\times10^{18}/cm^3$を越えており且つ厚さが例えば０．３μｍ又は０．２－０．５μｍの範囲であるＮＳｉ層７６１０である。Ｎ及びＰコンタクト７６２８及び７６３０は正面側上とすることが可能であり、その場合に、ＰコンタクトはＰ層７６０６に対するメサエッチングの後に形成される。ＳｉＧｅＢ又はＳｉＧｅＣ等のエッチストップ層をＰ層７６０６とＩ層７６０８との間の界面において使用することが可能である。光が背面側から入射し且つ光がＩ層７６０８を介して複数回の通過をすることが可能であるように上部表面ＳｉＮ層７６１０上に反射器が配置される場合には、Ｉ層７６０８は薄くすることが可能であり、例えば０．５－１μｍとすることが可能である。ＰとＮとは交換可能であり、且つ該マイクロストラクチャ型フォトダイオード（ＭＳ－ＰＤ）は、例えば、ＰＩＮとすることが可能である。ＳｉＧｅＢがエッチストップ層として使用される場合には、該ＳｉＧｅＢは高度にＰ型であり且つ該ＮＩＰ構造が好適である。該エッチストップ層は、例えば、０．０５乃至１μｍの厚さとすることが可能であり且つ該ＳｉＰ層を全体的に又は部分的に置換させることが可能である。適切に装置又はエピタキシャル層を修正して、光は正面側から及び／又は背面側から入射することが可能である。波長範囲は約８００－９９０ｎｍである。

【０１３１】

図７６（Ｂ）においては、図７６（Ａ）におけるＰＳｉ層７６０６は、Ｐドーピングが$2\times10^{18}/cm^3$を越えており且つ厚さが０．５μｍ又は０．２－１μｍの範囲である$Si_{0.99}Ge_{0.01}$Ｂ層７６１６で置換されている。その他の全ての層は図７６（Ａ）における通りである。マイクロストラクチャ型穴７６２２がエッチングされ且つ該ＳｉＧｅＢ層において停止するか及び／又は該ＳｉＧｅＢ層を貫通して通過し且つ該SiO_2層において停止するか及び／又は該SiO_2層内に入ることが可能である。該SiO_2層において停止するか又は該SiO_2層内で停止するか又はそれを貫通するビア７６７０をエッチングすることが可能である。ＳｉＮ層及びＳｉＧｅＢＰ層の夫々の上にＮ及びＰオーミックコンタクト７６２８及び７６３０が形成されている。光は上部表面（エピ表面）から及び／又は底部表面（基板表面）からのいずれかから入射することが可能であり、及び該Ｉ吸収層を介して複数回通過させるために誘電体スペーサ層と共に上部か又は底部のいずれかの上に反射器を配置させることが可能である。波長は８００乃至１０００ｎｍの範囲である。説明の便宜上図示していないものは、パッシベーション層、ポリイミド