ブリッジ層、メサ、ボンドメタル等のその他の要素である。

【０１３２】

図７６（Ｃ）においては、約０．１μｍの厚さで且つドーピングが１×１０^{18}／ｃｍ^{3}より大きいＰＳｉ層７６２６がＳｉＯ$_{2}$７６０４上の第１層として付加されており、その上にＰドーピングが１×１０^{18}／ｃｍ^{3}より大きく且つ厚さが約０．３μｍのＳｉ$_{0.94}$Ｇｅ$_{0.06}$Ｂ層７６１６が成長される。図７６（Ａ）及び（Ｂ）における如く、光はビアがエッチングされている上部及び／又は底部表面から入射することが可能である。Ｎ及びＰオーミックコンタクトが該Ｎ及びＰ層の上に夫々配置されている。マイクロストラクチャ型穴アレイ７６２２がＳｉＯ$_{2}$層７６０４を貫通してエッチングされ及び／又はＰ層７６２６内に部分的にエッチングされる。光が底部から入射する場合には、ビア７６７０をシリコン基板７６０２内へ及びＳｉＯ$_{2}$層７６０４内へエッチングし、尚ＳｉＯ$_{2}$層７６０４は部分的に又は完全にエッチングさせることが可能である。１－１０ボルトの逆バイアス電圧を該Ｐ及びＮコンタクトの間に印加させる。

【０１３３】

幾つかの適用例においては、光はＭＳ－ＰＤ／ＡＰＤの上部及び底部から同時的に入射することが可能である。該光は、同一の又は異なる波長、データレート、極性、及びコヒーレント光学通信用の振幅を有することが可能である。光が上部と底部の両方から入射することの利点はビームスプリッターを使用することの必要性が無く且つ光学パワー損失において３ｄＢ節約することが可能であるということである。

【０１３４】

図７７は、幾つかの実施例に基づく、ＳｉＮＩＰエピタキシャル層とＰＳｉ基板上のＳｉＧｅＢエッチストップ層とを具備しているＭＳ－ＰＤを示している概略図である。エッチストップ層７７１６はＳｉ$_{0.94}$Ｇｅ$_{0.06}$Ｂ又はＳｉＧｅにおいて約１％Ｇｅから構成することが可能であり、その場合に、そのバンドギャップは実質的にＳｉと同じであり且つＢドーピングは１×１０^{19}／ｃｍ^{3}を越えるものである。この高度のＰドーピングはＳｉＰ層７７０６を部分的に又は全体的に置換させる場合がある。これらの層及び厚さは次の通りとすることが可能であり、即ち、ＳｉＰ基板７７０２、厚さが０．１－２μｍのＳｉＧｅＢ層７７１６、Ｐドーピングが２×１０^{19}／ｃｍ^{3}を越えている０．２μｍ（又は０．１－１μｍの範囲）のＳｉＰ層７７０６、意図的にはドーピングされておらずバックグラウンドドーピングが５×１０^{15}／ｃｍ^{3}であり且つ幾つかの場合には５×１０^{13}／ｃｍ^{3}未満であって厚さが２μｍ又は０．５－２、５μｍの範囲内であるＳｉ１層７７０８、及びドーピングが２×１０^{18}／ｃｍ^{3}を越えており且つ厚さが０．３μｍ又は０．２－０．５μｍの範囲内であるＮＳｉ層７７１０である。Ｎ及びＰコンタクト７７２８及び７７３０は両方共正面側とすることが可能である。該Ｐコンタクトは、又、コンタクト７７３２におけるように該ＰＳｉの背面側上とすることも可能である。マイクロストラクチャ型穴アレイ７７２２はＳｉＧｅＢのエッチストップ層７７１６へエッチングさせることが可能である。該ＳｉＰ内へ及び／又は該ＳｉＧｅＢ層へメサをエッチングさせて該ＮＩＰ区域、従ってＮＩＰ容量を画定する。Ｐコンタクト７７３０はＰＳｉ層７７０６又はＰＳｉＧｅＢ層７７１６の上に配置させることが可能である。Ｎコンタクト７７２８がＳｉＮ層７７１０上に配置される。該Ｓｉ基板を除去するために、該Ｓｉ及びＳｉＧｅＢに対するものとは異なるエッチングプロセスを使用して、該ＳｉＧｅＢ層まで及び／又は部分的に該ＳｉＧｅＢ層内へビア７７７０をエッチングさせることが可能である。ＳｉＧｅＢ層７７１６もエッチング除去することが可能であり、その場合には、ビア７７７０はＳｉＰ層７７０６まで延在される。更に、ＳｉＰ層７７０６は部分的に又は全体的に該ＳｉＧｅＢ層で置換させることが可能である。そのような場合には、少なくとも０．２乃至０．３μｍのＳｉＧｅＢ層が残存することが望ましい。光は正面及び／又は背面側から入射することが可能である。誘電体が半導体と接触しており厚さが０．５－４μｍの誘電体金属反射器を設けることが可能であり、その場合に、該誘電体はＳＯＧ、ポリイミド、ＳｉＯ$_{2}$、フッ化カルシウム、又は窒化シリコンとすることが可能であり、それに続いて、正面か又は背面側のいずれかの上にＡｇ、Ａｕ、ＡＩ、Ｎｉ等の金属又は合金

を設ける。例えば、該誘電体金属反射器が背面側に配置される場合には、正面側からの光を該吸収用Ｉ層を介して多数回反射させることが可能であり、且つ逆に、該反射器が正面側に配置される場合には、背面側からの光は該吸収用Ｉ層を介して多数回反射させることが可能である。反射器がある場合には、一層薄いＩ層を使用することが可能であり、それは、例えば、１μｍであるか又は反射器が無いＭＳ－ＰＤの厚さの約半分であって、そのことは該ＭＳ－ＰＤに対して一層高いデータレートとさせることが可能である。該ＭＳ－ＰＤの場合に８００－９９０ｎｍの波長範囲を使用することが可能である。幾つかの場合において、該反射器は、単純に、ブラッグミラー等の金属とすることが可能である。更に、光が正面の表面からのみ入射するものであって２回及び／又は多数回の反射が実現されない場合には、ビア７７７０は必要ではない場合がある。

【０１３５】

図７８は、幾つかの実施例に基づく、ＭＳ－ＰＤ用のＳｉＧｅＢエピタキシャル層上のＧｅ・オン・ＳｉＮＩＰを示している概略図である。マイクロストラクチャ型穴アレイ７８２２がＧｅ層７８１０及び７８０８において且つＳｉＰ層７８０６内へ又はそこまでエッチングされている。エッチストップ層７８１６は$Si_{0.99}Ge_{0.01}B$又は約１％のＧｅのＳｉＧｅから構成されており、その場合にバンドギャップはＳｉと実質的に同じであり且つＢドーピングは$1\times10^{20}/cm^3$は越えている。この高度のＢドーピングはＳｉＰ層７８０６を部分的に又は全体的に置換させる場合がある。これらの層及び厚さは次の通りとすることが可能であり、即ち、ＳｉＰ基板７８０２、ＳｉＧｅＢ層７８１６は０．１－２μｍの厚さであり、ＳｉＰ層７８０６は０．２μｍ（又は０．１－１μｍの範囲）でありＰドーピングは$1\times10^{19}/cm^3$であり、Ｇｅ１層７８０８は意図的にドーピングされておらずバックグランドドーピングが$5\times10^{18}/cm^3$未満であって且つ幾つかの場合においては$5\times10^{18}/cm^3$未満であり厚さが２μｍ又は０．５－２．５μｍの範囲であり、且つＮＧｅ層７８１０はドーピングが$2\times10^{18}/cm^3$を越えるものであって厚さが０．２μｍ又は０．２－０．５μｍの範囲内である。Ｎ及びＰコンタクト７８２８及び７８３０の両方を正面側とすることが可能である。該Ｐコンタクトは、コンタクト７８３２における如く、ＰＳｉ基板上の背面側とすることも可能である。数ｎｍのＧｅバッファー層をＳｉ層とＧｅ層との間に成長させることが可能であり、且つその場合のＧｅバッファー層の成長条件は該Ｇｅ１層の成長条件とは異なっている。ビア７８７０をＳｉ基板７８０２内にエッチングして該ＳｉをＳｉＧｅＢ層７８１６まで除去することが可能である。異なるエッチ条件で、ＳｉＧｅＢ層７８１６を部分的に及び／又は全体的にエッチングすることが可能である。光は正面側又は背面側のいずれかから入射することが可能であり、反射器がある場合には、フォトンはＩ吸収層を介して複数回の通過を行い且つ本装置は一層高いデータレート動作のために一層薄い層を使用することが可能である。何故ならば，電子及び正孔の光発生されたキャリアーの走行時間は一層短いからである。波長範囲は８００乃至１８００ｎｍである。穴直径及びアレイ周期は約３０－１００ｎｍに亘る或る波長範囲に対して最適化させることが可能である。光学信号が正面／上部表面から入射する場合にはビア７８７０は必要ではない場合がある。更に、光学信号が１２００－１７５０の範囲内の波長を有している場合には，これらの波長においてシリコンは殆どトランスペアレント即ち透明であるか又は発生する光学損失は非常に低いので底部照射の場合にはビアが必要ではない場合がある。

【０１３６】

図７９は、幾つかの実施例に基づく，ＭＳ－ＰＤ用のＧｅ・オン・Ｓｉエピタキシャル構造を示している概略図である。その物質構造は次の通りであり、即ち、ＳｉＮ基板７９０２（又は代替的にＰＳｉ基板上のＮＩＰ構造）、Ｎドーピングが$2\times10^{19}/cm^3$を越えている０．２μｍ（又は０．１－１μｍの範囲）のＳｉＮ層７９０６、意図的にはドーピングされておらずバックグランドドーピングが$5\times10^{18}/cm^3$未満であり且つ幾つかの場合には$5\times10^{18}/cm^3$未満であって厚さが２μｍ又は厚さ範囲が０．５－２．５μｍであるＧｅ１層７９０８、及びドーピングが$2\times10^{19}/cm^3$であり且つ厚さが０．２μｍ又は０．２－０．５μｍの範囲内であるＰＧｅ層７９１０である。

Ｐ及びＮコンタクト７９２８及び７９３０は両方共正面側とすることが可能である。マイクロストラクチャ型穴アレイ７９２２をＮＳｉ層７９０６までエッチングするか、部分的にその中へエッチングするか、又はそれを貫通してエッチングする。メサエッチングがＰＩＮ区域及び容量を画定する。Ｎコンタクト７９３０及び７９３２を該ＮＳｉ基板の正面側表面上又は背面側表面上のいずれかに該メサエッチングの後に付着させる。パッシベーションは図示されていないが、Ｋａｎｇ　ｅｔ　ａｌ．を使用して、非晶質Ｓｉを露出されたＧｅ表面の側壁上に付着させることが可能であり且つ高温でアニールさせることが可能であり、及び／又はＳｉＧｅを露出されたＧｅの側壁上に付着させ且つアニールして漏洩電流を減少させることが可能である。該ＭＳ－ＰＤ及びＭＳ－ＡＰＤにおけるメサ直径は、データレートに依存して、５μｍ乃至１００μｍの範囲とすることが可能である。幾つかの実施例によれば、該メサ直径範囲は３０Ｇｂ／ｓのデータレートの場合に２０－４０μｍである。更に、高結晶品質を確保するために、ＮＳｉ７９０６とＩＧｅ７９０８との間にバッファＧｅ層を使用することが可能である。例えば、Ｋａｎｇ　ｅｔ　ａｌ．を参照すると良い。正面側から光が入射する場合には、波長は８００－１８００ｎｍの範囲とすることが可能である。好適な範囲においては、該波長は１４５０－１６００ｎｍとすることが可能であり、且つ別の好適な範囲においては、例えば、１２５０－１６００ｎｍとすることが可能である。該ＭＳ－ＰＤ／ＡＰＤはデータ通信波長及び遠隔通信波長の両方をカバーすることが可能である。

【０１３７】

図８０は、幾つかの実施例に基づく、別のＧｅ・オン・Ｓｉエピタキシャル構造を示している概略図である。該ＭＳ－ＰＤは、その物質構造の厚さ及びドーピングを含んで、図７９に図示し且つそれについて説明したものと同様又は同一であるが、それは０．２乃至４μｍの厚さの埋込酸化物層８００４を具備するＳｉＢＯＸウエハ上に成長されることが異なっている。マイクロストラクチャ型穴アレイ８０２２をＮＳｉ層７９０６までエッチングし且つＮＳｉ層７９０６内へ又はそれまで又はＳｉＯ２層８００４までエッチングさせることが可能である。メサエッチングがＰＩＮ容量を画定し且つ該ＭＳ－ＰＤ／ＭＳ－ＡＰＤ用のメサ直径は該ＭＳ－ＰＤ／ＡＰＤのデータレート帯域幅に依存して５－１００μｍの範囲である。２０－５０μｍのメサ直径が２０－３５Ｇｂ／ｓのデータレート帯域幅に対して好適である。光は前部表面又は後部表面から入射することが可能である。１１００ｎｍを越える波長において、Ｓｉの光学損失は非常に低く且つ該Ｓｉ基板は、例えば、レンズ又はグレーチングをエッチングするために使用することが可能である。ＳｉＯ２を全体的に又は部分的に除去するためにビア８０７０をエッチングすることが可能である。ビア８０７０は、光及び／又はファイバーを、例えば、該ＭＳ－ＰＤへ案内するために使用することが可能である。ビア８０７０内に反射器８０７０を付着させることが可能であり、その場合に、正面側からの光が該反射器で跳ね返り且つＩＧｅ吸収領域７９０８を複数回横断するように該ＳｉＯ２は完全には除去しないか又は全く除去することはない。反射器が正面側か又は背面側のいずれかにある場合、ＩＧｅ７９０８は一層薄く、例えば１μｍとすることが可能であり、そのことは電子正孔走行時間を減少させ且つ該ＭＳ－ＰＤ／ＭＳ－ＡＰＤのデータレート帯域幅を増加させる。波長は８００－１８００ｎｍの範囲とすることが可能であり、それはデータ通信及び遠隔通信波長範囲の両方をカバーしている。連続的なＮＳｉ層７９０６の場合、例えば該ＳｉＯ２層が完全にエッチングされている場合には、該ＮＳｉの底部表面へ反射防止コーティングを付与することが可能である。

【０１３８】

図８１は、幾つかの実施例に基づく、Ｇｅ・オン・Ｓｉエピタキシャル構造を示している概略図である。該ＭＳ－ＰＤは、その物質構造の厚さ及びドーピングを含んで、図７９－８０に図示し且つそれらについて説明したものと同様であるか又は同一であるが、ビア８１７０がＳｉＯ２ＢＯＸ層８００４へエッチングされており且つ２－４μｍの厚さ又は０．２－６μｍの範囲の該ＳｉＯ２を部分的にエッチングするか、完全にエッチングするか、又はエッチングしないものとすることが可能であることが異なっている。更に、Ａｇ

，Ａｕ，Ｃｒ，Ａｌ等の物質からなる反射器８１７２を形成することが可能である。該反射器８１７２は、又、ブロードバンド、ナローバンド、又はバスバンドブラッグ反射器とすることが可能である。注意すべきことであるが、反射器８１７２が誘電体である場合には、それは、該ＳｉＯ２層をエッチング除去して、ＮＳｉ層７９０６上に直接的に付着させることも可能である。ＩＧｅ層７９０８を介しての１回目の通過で吸収されなかった正面側から入射する光は、該ＩＧｅ吸収層を介して複数回通過するために該ＩＧｅ層へ反射して戻すことが可能である。該ＩＧｅ層は一層薄く、例えば１μｍ、することが可能であり、そのことは該ＩＧｅ層においての電子及び正孔に対する走行時間を一層短いものとさせる。このことは該ＭＳ－ＰＤ／ＭＳ－ＡＰＤのデータレート帯域幅を増加させる。

【０１３９】

図８２Ａ－８２Ｃは、図７９に図示した構造に類似したＧｅ・オン・Ｓｉマイクロストラクチャ型フォトダイオードに関しての有限差分時間領域（ＦＤＴＤ）を使用してのシミュレーションに関するものである。図８２Ａは、シミュレーションを行ったＧｅ・オン・Ｓｉマイクロストラクチャ型フォトダイオードを示している概略図である。その穴パターンは正方形格子パターンである。穴周期と穴直径との２つの組合せについてシミュレーションを行っており、即ち２５００ｎｍの穴周期と１５００ｎｍの直径、及び２３００ｎｍの穴周期と１３００ｎｍの直径である。図８２Ｂ及び８２Ｃにおいて、水平軸はμｍでの波長であり且つ垂直軸は吸収であってそれは量子効率に直接的に関係している。各場合において、穴の正方形格子パターンをシミュレーションしている。図８２Ｂにおいて、８００ｎｍ乃至１０００ｎｍの範囲の波長を有する光学信号に対して、曲線８２１０は２３００ｎｍの穴周期及び１３００ｎｍの直径に対しての吸収のプロットであり、且つ曲線８２１２は２５００ｎｍの穴周期及び１５００ｎｍの直径に対しての吸収のプロットである。図８２Ｃにおいて、１０００ｎｍ乃至１８００ｎｍの範囲の波長を有する光学信号に対して、曲線８２２０は２３００ｎｍの穴周期及び１３００ｎｍの直径に対しての吸収のプロットであり且つ曲線８２２２は２５００ｎｍの穴周期及び１５００ｎｍの直径に対しての吸収のプロットである。０．８乃至０．９８μｍの波長範囲に対して０．４（フォトンの４０％を吸収）を越えるものから高々０．９（フォトンの９０％を吸収）を越えるものまでの吸収が判別された。０．５より大きな吸収は１．５５μｍに対して見られ且つＧｅの約２μｍの吸収層に対して１．８μｍへ延在している。これはマイクロストラクチャの無い２μｍ厚さの同等のＧｅ層よりも著しく一層大きく、特に１５５０ｎｍ及びそれより一層長い波長においてそうである。

【０１４０】

図８３Ａ－８３Ｃは、図８０における構造に類似したＧｅ・オン・Ｓｉマイクロストラクチャ型フォトダイオードに関して有限差分時間領域（ＦＤＴＤ）を使用したシミュレーションに関するものである。図８３Ａは、上部表面から入射する光でシミュレーションを行ったＧｅ・オン・Ｓｉマイクロストラクチャ型フォトダイオードを示している概略図である。図８３Ｂ及び８３Ｃのグラフにおいて，水平軸はμｍでの波長であり且つ垂直軸は吸収であって，それは２５００ｎｍの周期及び１５００ｎｍの直径（曲線８３１２及び８３２２）と２３００ｎｍの周期及び１３００ｎｍの直径（曲線８３１０及び８３２２）を有する複数の穴の正方形格子に対する量子効率に直接的に関係している。０．７より大きな吸収（フォトンの７０％を吸収）が１．５５μｍに対して見られ且つＧｅの約２μｍの吸収層に対して０．５吸収（フォトンの５０％を吸収）よりも良い状態で１．８μｍへ延在している。このことは、例えば，１６５０ｎｍ及びそれより長い波長において２μｍ厚さを有するＩｎＰと格子整合された同等のＩｎＧａＡｓ層よりも著しく一層大きい。

【０１４１】

図８４Ａ及び８４Ｂは，Ｇｅ・オン・Ｓｉマイクロストラクチャ型フォトダイオードに関して有限差分時間領域（ＦＤＴＤ）を使用したシミュレーションの結果を示している。シミュレーションした構造は図８２Ａに示されている。図８４Ａ及び８４Ｂにおいて、グラフの水平軸はμｍ単位での波長であり且つ垂直軸は吸収であって、それは該穴アレイに対しての正方形及び六角形の両方の格子に対する量子効率に直接関係している。図８４Ａ

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は，２３００ｎｍの周期及び１３００ｎｍの穴直径を有する正方形格子（曲線８４１０）及び六角形格子（曲線８４１２）の両方を示している。０．９（フォトンの９０％を吸収）より大きな吸収が、５０ｎｍ波長スパンにわたって吸収が１０％未満だけ変化している領域と共に１．５５μｍ波長に対して示されている。図８４Ｂは、２５００ｎｍの周期で１５００ｎｍの直径に対しての正方形（曲線８４２０）及び六角形（曲線８４２２）の格子の両方を示しており、それは１．５５μｍにおいて０．７の吸収を示している。全体的に、六角形格子は正方形格子よりも一層良好なフォトン吸収を示している。或る波長範囲においての吸収を改良又は最適化させるために周期及び穴直径、穴形状及び格子のその他の組合せを使用することが可能である。

【０１４２】

図８５は，幾つかの実施例に基づく、縮尺通りではないが，マイクロストラクチャ型フォトダイオードチップの概略平面図を示している。チップ８５６０の近似的な寸法は３５０μｍ×３００μｍ×１５０μｍである。メサエッジ８５６２によって画定されるメサは３０μｍの直径を有している。該メサはＮＩＰ又はＰＩＮ接合容量を画定する。該メサの上部には上部表面８５１０が見えており（例えば、ＮＩＰＭＳ－ＰＤ／ＡＰＤを取るＮ層）、マイクロストラクチャ型穴８５２２も見えている。該メサの外側エッジ近くにはＮオーミックコンタクトリング８５２８（ＮＩＰＭＳ－ＰＤを取る）がある。該メサの外側にはＰオーミックコンタクトリング８５３０がある。Ｎボンドパッド８５８０がブリッジ相互接続８５８２によってＮオーミックコンタクト８５２８へ電気的に接続されている。同様に、Ｐボンドパッド８５９０が相互接続８５９２によってＰオーミックコンタクトへ接続されている。幾つかの実施例によれば、ブリッジ相互接続８５８２と区域８５０６（Ｐ層表面である場合がある）との間の不所望の短絡は、それらの間に付着されたポリイミド等の絶縁体を使用して防止されている。注意すべきことであるが、上述した説明は、Ｎ及びＰ層及びコンタクトが逆にされる場合に、ＰＩＮ配置型ＭＳ－ＰＤ／ＡＰＤに対しても適用可能である。

【０１４３】

幾つかの実施例によれば、ＢＯＸＳｉウエハ上のＮＩＰＭＳ－ＰＤ構造の基本的な製造ステップの簡単な処理フローは、（１）マスクし且つＳｉＯ２層への穴アレイ８５２２をエッチングし、（２）マスクし且つＮ層８５１０上にＮオーミックコンタクト金属リング８５２８を付着させ、（３）マスクし且つ接合容量を画定するメサをエッチングし、Ｐ層８５０６へエッチングし、（４）マスクし且つＳｉＯ２へＰメサをエッチングし、（５）マスクし且つＰ層８５０６上にＰオーミックコンタクト金属８５３０を付着させ、（６）ボンドパッド８５８０によってＮオーミックリング８５２８へのコンタクト用のポリイミドブリッジをマスクし、（７）マスクし且つ夫々Ｐオーミック及びＮオーミックの両方に対してのボンドパッド８５９０及び８５８０を付着させる，ことからなる場合がある。接合及びボンドパッド容量は並列であり，従って、加法型であるので、該ボンドパッドは約１００×１００μｍ^{2}でＮオーミックリング８５２８とコンタクトしている。ＲＣ時定数は全接合、パッド、フリンジ容量によって決定される。上記したプロセスから削除したものは、パッシベーション、アニール、キュア、反射防止、薄層化（thinning），背面側メタリゼーション、ダイシング等である。ＮＩＰ／ＰＩＮメサ直径は１０乃至１００μｍの範囲とすることが可能であり、ＭＳ－ＰＤ／ＡＰＤは従来のＰＤ／ＡＰＤと比較してメサにおける半導体物質はより少ないので、容量はより少なく、従って従来のＰＤ／ＡＰＤと比較して同じデータレート帯域幅に対して一層大きな面積のメサ（又は等価的に一層大きな感光性面積）を有することが可能であり、従ってＭＳ－ＰＤ／ＡＰＤ内への光学信号のアライメントは一層大きな誤差余裕を有しており、そのことはパッケージングにおいて一層コストを低下させることとなる。図５６及び図５７から、正方形穴格子で２０００ｎｍの周期及び１３００ｎｍの直径の穴の場合、その容量は、穴が無いが同じ直径のメサでＩ層の厚さで、フリンジ容量を無視した場合の同等の構造のものよりも約３０％一層少ない。周期が２０００ｎｍで穴直径が１３００ｎｍである六角形格子穴の場合、該ＭＳ－ＰＤの面積は穴が無いＰＤの場合よりも約３５％一層大きい場合がある。その他の格子，周期

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、及び穴直径、吸収向上のためではないが容量減少のための穴、は容量を減少させるため、及び／又は、例えば、ＭＳ－ＰＤ／ＡＰＤ構造における吸収を増加させるか又は最適化させるために使用することも可能である。幾つかの実施例によれば、複数の周期及び／又は複数の穴直径を使用することも可能である。更に、非周期的に離隔させた穴を使用することも可能である。

【０１４４】

図８６は、単一チップ上に相互インピーダンス増幅器及び／又はその他のエレクトロニクスと共に集積化させたＭＳ－ＰＤ／ＡＰＤを示している概略平面図である。単一シリコンチップ８６００上に、ＭＳ－ＰＤ／ＡＰＤ８６６０が相互接続線８６９２を使用してＴＩＡ又はその他のエレクトロニクス８６９０へ接続して示されている。図８５は、更なる信号処理及び送信のために電気信号を他の電子部品へ送信するためにボンドパッドを必要とするスタンドアローンＭＳ－ＰＤ／ＡＰＤを示しているが、図８６は、単一チップに集積化されたＭＳ－ＰＤ／ＡＰＤ及びエレクトロニクスを示している。ボンドパッドは不所望の容量を付加し、且つこの容量は、接合容量と共に、ＭＳ－ＰＤのデータレート帯域幅を計算するために使用される。例えば、２０ＧＨｚ（又は約３０Ｇｂ／ｓ）の帯域幅を有するＲＣ時間は約０．１６ｐＦの容量と５０Ωの負荷抵抗とである。２μｍＩ層を有する３０μｍ直径のＳｉＰＩＮＰＤは、Ｉ層が逆バイアス電圧によって完全に空乏化された状態で３７フェムトファラッド（ｆＦ）の接合容量を有している。このことは、２μｍのポリイミドの上に９０μｍ×９０μｍのボンドパッドを可能とさせて約０．２ｐＦの全容量を与える。該ＭＳ－ＰＤ／ＡＰＤをＴＩＡ及び／又はエレクトロニクスと集積化させるとすると、ボンドパッドは最早使用されることは無く且つ該ＭＳ－ＰＤ／ＡＰＤから該ＴＩＡ及び／又はエレクトロニクスへの送信線の容量を無視すると、該ＭＳ－ＰＤ／ＡＰＤ容量は０．１６ｐＦとなることが可能であり、そのことは、ＭＳ－ＰＤの場合、スタンドアローン装置に対する直径において３０μｍであるのと比較して、直径において約６０μｍの装置となる。この面積における増加は、ＭＳ－ＰＤ／ＡＰＤに対する光学ビームのアライメント誤差における余裕を一層大きなものとさせ且つパッケージングにおけるコストを一層低下させることとなる。寄生容量を含むと、ＭＳ－ＰＤの直径はスタンドアローンＭＳ－ＰＤの３０μｍよりも著しく一層大きく、且つ、例えば、４０μｍよりも大きい場合があり、且つ幾つかの場合においては、直径において５０μｍよりも一層大きい場合がある。

【０１４５】

注意すべきことであるが、本特許明細書に記載されるように、光の波長とほぼ同じ（多かれ少なかれ）直径を有するマイクロストラクチャ型穴アレイ（又は柱体）は、マイクロストラクチャ型穴アレイ（又は柱体）を有することの無い同様の物質のものよりも、フォトンの吸収を向上させる。例えば，ＳｉＰＩＮＰＤが数十Ｇｂ／ｓで動作するためには、Ｉ層の厚さは必ず約２μｍの程度でなければならず、そうでない場合には、光発生されたキャリアである電子及び正孔の走行時間が数十Ｇｂ／ｓのデータレート帯域幅を達成し尚且つ８５０ｎｍ、或る場合には８８０ｎｍ、そして或る場合には９８０ｎｍの公称波長において約２０％を越える、幾つかの場合には４０％を超える十分な量子効率を有するためには長過ぎるものとなる。このことは、単一の周期及び直径で、及び／又は複数の周期及び直径でのいずれかによって、マイクロストラクチャ型穴アレイ（又は柱体）を使用する本書に記載した技術で可能とされる。該穴及び／又は複数の穴（柱体及び／又は複数の柱体）は周期的及び／又は非周期的なものとすることが可能であり、且つ該マイクロストラクチャが吸収及び／又はエミッション（emission）を向上させるためには円形以外の断面形状を有することが可能である。該マイクロストラクチャ型穴アレイ（又は柱体）が存在しない場合には、該２μｍ又はそれ未満の厚さのＳｉ層は９００ｎｍフォトンの約５％を吸収し、一方、マイクロストラクチャ型穴アレイ又は柱体が存在する場合には，２０％を超えて吸収させることが可能であり、幾つかの場合においては、３０％を越えるものである。更に幾つかのその他の場合においては、９００ｎｍ波長のフォトンにおいて４０％、５０％、及び８０％を越えることが可能である

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【０１４６】
このことはＧｅ・オン・Ｓｉの場合でも同じであり、この特許明細書を使用することによって、例えば、１５５０ｎｍ、且つ幾つかの場合においては１６００ｎｍ及び幾つかの場合においては１７００－１８００ｎｍの波長において数十Ｇｂ／ｓデータレート帯域幅を達成することが可能である。
【０１４７】
既知のナノワイヤーフォトダイオードにおいては、数十Ｇｂ／ｓの高データレート帯域幅に対する約２μｍ又はそれ未満の薄い層が同等のバルク層のものを越えるというような吸収の向上は存在しない。例えば、バンドギャップよりも大きな波長における２μｍ長さのＩｎＰナノワイヤーと２μｍバルクＩｎＰとはほぼ同等であり、ＩｎＰナノワイヤーの利点は反射を減少させることのみにある。
【０１４８】
図８７は、何らマイクロストラクチャが存在しない単純なエピタキシャル構造を示している。図８７の構造は、８００－８８０ｎｍの波長範囲を有する入射フォトンの吸収に関して、穴アレイ等のマイクロストラクチャを有する同様のエピタキシャル構造と比較するために使用される。ＦＤＴＤ（有限差分時間領域）を使用するシミュレーション目的のために、Ｐ及びＮコンタクト、メサエッチング、パッシベーション、平坦化、及び完全なフォトダイオードを製造するためのその他のプロセス無しで、マイクロストラクチャを有する構造と有さない構造のみが示される。ケース１におけるエピタキシャル構造は、ドーピングされており且つ約１５０μｍへ薄膜化されたシリコン基板Ｐ８７０２上に成長され、その第１層は約０．２μｍの厚さでボロンを使用して1×10^{20}／cm^3を越えてドーピングされているＳｉＰ層８７０６であり、次いで約２μｍの厚さで意図的にはドーピングされておらず且つドーピングレベルが5×10^{15}／cm^3未満であるＳｉイントリンシック層８７０８であり、次いで約０．３μｍの厚さで燐ドーパントでのドーピングが1×10^{19}／cm^3を越えているＳｉＮ層８７１０である。
【０１４９】
図８８は、何らマイクロストラクチャが存在しない別の単純なエピタキシャル構造を示している。図８８の構造は，８００－８８０ｎｍの波長範囲での入射フォトンの吸収に関して穴アレイ等のマイクロストラクチャを有する同様のエピタキシャル構造と比較するために使用する。ＦＤＴＤ（有限差分時間領域）を使用するシミュレーション目的のために、Ｐ及びＮコンタクト、メサエッチング、パッシベーション、平坦化、及び完全なフォトダイオードを製造するためのその他のプロセス無しで，マイクロストラクチャを有する構造と有さない構造のみが示される。ケース２におけるエピタキシャル構造は、２μｍの埋込酸化物（ＢＯＸ）層８８０４を具備するシリコン基板８８０２上に成長され、該ＢＯＸ層上には約０．１μｍの厚さでボロンを使用したドーピングが1×10^{20}／cm^3を越えているＳｉＰ層８８０６であり、次いでＰドーピングが1×10^{20}／cm^3を越えているＳｉＧｅＢ（$Si_{0.58}Ge_{0.41}B_{0.01}$）層８８１６であり、次いで約２μｍの厚さで意図的にドーピングされておらずドーピングレベルが5×10^{15}／cm^3未満であるＳｉイントリンシック層８８０８であり、次いで約０．３μｍの厚さで燐ドーパントで1×10^{19}／cm^3を越えてドーピングされているＳｉＮ層８８１０である。
ケース１及びケース２の両方に対してフォトンは、シミュレーション研究のために、上部表面即ちＳｉＮエピタキシャル層（８７１０及び８８１０）を有する表面から入射する。
【０１５０】
図８９は、幾つかの実施例に基づいて、マイクロストラクチャ型穴アレイが該ＳｉＰエピタキシャル層までエッチングされていること以外は図８７におけるものと同じエピタキシャル構造を示している。このケース３においては、穴８９２２は１５００ｎｍの直径及び正方形格子アレイにおいて２０００ｎｍの周期を有している。８００－８８０ｎｍの波長を有するフォトンが上部表面即ちＳｉＮエピタキシャル層８７１０上に入射する。該Ｎ及びＰ層／基板は或る適用例においては交換させることが可能であり、その吸収結果はほぼ同じである。

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【０１５１】
図９０は、幾つかの実施例に基づいて、マイクロストラクチャ型穴アレイが該ＢＯＸＳｉＯ２層へエッチングされていること以外図８８におけるものと同じであるエピタキシャル構造を示している。このケース４においては、穴９０２２は１５００ｎｍの直径及び正方形格子アレイにおいて２０００ｎｍの周期を有している。８００－８８０ｎｍの波長を有するフォトンが上部表面即ちＳＩＮエピタキシャル層８８１０上に入射する。該Ｎ及びＰ層／基板は或る適用例においては交換可能であり且つその吸収結果はほぼ同じである。
【０１５２】
更に、該穴は該エッチストップ層ＳｉＧｅＢ８８１６までエッチングさせることが可能である。エッチストップ層８８１６は高度にＰドーピングされており且つＰ層とエッチストップ層とが処理において所望される場合の層構造において使用することが可能であり、このことはフォトダイオード及びアバランシェフォトダイオード構造を包含している。
【０１５３】
図９１Ａ－９１Ｂは、図８７－９０に図示した例示的構造に対するシミュレーションの結果を示しているプロットである。図９１Ａはケース１－４（夫々、図８７－９０）の比較を示しており、その場合に、ＦＤＴＤシミュレーションを使用して８００－９００ｎｍにわたって示した波長に対しての各ケースにおける「Ｉ」Ｓｉイントリンシック層に起因する吸収を計算している。各ケースにおいて、フォトンは上部表面即ちＮＳｉエピタキシャル表面へ入射している（図８７－９０における層８７１０及び８８１０）。該「Ｉ」層以外のその他の層に起因する吸収は包含されていない。曲線９１１０，９１１２，９１１４，９１１６は、ケース１，２，３，４（図８７，８８，８９，９０に示してある）に対する結果を夫々示している。ケース１及び２においては、マイクロストラクチャは存在しておらず、該Ｉ層における吸収は４０％未満である。そのことは、入射フォトンの内の４０％が吸収されたことを意味している。ケース１においては，それは１５％未満であり、且つケース２においては、例えば８０５ｎｍの或る波長において，それは丁度４０％未満とすることが可能であり且つ一層長い波長の８８０ｎｍ及び８５０ｎｍにおいて２０％未満へ減少し且つ８８５ｎｍにおいては１０％未満である。吸収は量子効率に直接比例している。何故ならば、フォトンが吸収され且つ電子及び正孔へ変換されそれらの電子及び正孔が「Ｉ」領域を空乏化させるバイアス電圧の下で該「Ｉ」領域の外へ掃引される前に再結合しない場合には，これらの光発生されＮ及びＰ領域へ夫々掃引された電子及び正孔は光電流に寄与するからである。直径が１５００ｎｍで正方形格子における周期が２０００ｎｍであるマイクロストラクチャ型穴を包含しているケース３及び４において，或る波長においては１００％に近い吸収レベルが見られている。ケース３及び４の両方において、８００乃至９００ｎｍの波長において吸収は４０％よりも大きい。８００－８５０ｎｍの範囲において、それは約７０％よりも大きい吸収である。そして，ケース４においては，８８０乃至９００ｎｍにおいてその吸収は７０％よりも良い。ケース４での８５５ｎｍにおいては、吸収は９５％を越えており、それは１０％未満であるケース２と対比される。マイクロストラクチャの場合における「Ｉ」層においての吸収百分率は、穴直径、周期、及び／又は格子を変化させる、例えば正方形格子から六角形格子へ，ことによって或る波長において高吸収のために増加又は最適化させることが可能である。
【０１５４】
本書に記載する如きマイクロストラクチャを具備するシリコンＰＩＮフォトダイオードの場合に，波長が３００Ｋにおける１．１１ｅＶのシリコンバンドギャップ，即ち約１１１７ｎｍに近づく場合に吸収は必ずしも減少するものではないことが判明した。それと比較して、マイクロストラクチャの無いＰＩＮ（又はＮＩＰ）フォトダイオードの場合、波長が１１１７ｎｍに近づくにつれて吸収は減少する。このことは、光学損失が減少するにつれてマイクロストラクチャの共振及び／又は結合共振のＱ（品質係数）が増加し、従ってフォトンが該マイクロストラクチャ内を行ったり来たりして跳ね返ることによりより多くの時間にわたり滞在し、その結果、波長が１１１７ｎｍに近づく場合でも５０％を超える場合がある吸収となっていることに起因しているものと考えられる。該マイクロストラ

クチャ内の屈折率差は実効指数で表すことが可能である。例えば、該穴はシリコン物質を取り除き且つ、例えば、空気で置換されるので、穴を具備する該領域の実効指数、即ち実効屈折率は、穴が無い場合の該領域の屈折率未満である。単純な評価は屈折率の平均であるが、例えば、該穴が穴を具備する該領域におけるシリコンの半分を除去する場合には、該穴が空気で充填されるものと仮定すると、その実効屈折率は約（１＋３．４４）／２＝２．２２であり、その場合にバルクＳｉの屈折率は１０００ｎｍの波長において約３．４４である。従って、穴を具備しており且つ穴を具備していない該領域は、ほぼ１．２２の屈折率不連続性、即ち約３５％の屈折率変化、を見ることとなる。この屈折率における不連続性は、光学損失が低い場合に１，０００，０００又はそれ以上に近づく場合があるＱを有する高コントラストグレーチングとなる場合がある。このことはマイクロストラクチャ型フォトダイオード及び／又はアバランシェフォトダイオードにおける吸収の向上を説明することが可能である。フォトンが該フォトダイオード／アバランシェフォトダイオードの走行時間及びＲＣ時間である特性時間に近づく時間の間該マイクロストラクチャ内に滞在する場合には、そのことはＰＤ／ＡＰＤのデータレート帯域幅に悪影響を与え始める。しかしながら、データレート帯域幅が低い場合には、一層高いＱを許容することが可能である。該Ｑ係数は、格納されたエネルギー／サイクル当たりのエネルギー損失に比例するものとして定義される。これは該マイクロストラクチャにおける吸収向上に対する蓋然性のある説明である。該マイクロストラクチャは格子から構成されており、従って各々がその組の共振を有しており且つ密接に結合されている多数の単位セル又はセルから構成されている。単一共振器であるのでその共振はシャープなピークや谷であり且つ周期的な波動関数である単一の共振特性のみを示す従来既知の共振フォトダイオードとは異なり、結合共振セルを具備するマイクロストラクチャは、吸収がゆっくりと変化する、例えば、或る波長範囲、例えば５０－１００ｎｍ、に亘って１０％未満だけ変化する波長に対する吸収における領域、及び非周期的な波動関数を有している。該マイクロストラクチャ型ＰＤ／ＡＰＤは複数個の共振の総和を有しており、従って従来既知の共振フォトダイオードと比較してそれほど際立っていないピーク及び谷を有している。非周期的な穴は、又、それ自身が非周期的であり且つ隣接する隣のセルと結合することが可能な共振セルを有することが可能であり、それは吸収及び／又はエミッションを向上させることが可能な結合型共振構造とさせる。

【０１５５】

概算見積もりとして、該特性時間は約２０ＧＨｚ３ｄＢ帯域幅に対して約２０ｐｓである。２０ｐｓにおいて、光はシリコン内を約２０００μｍ走行し、そのことは、光が２μｍマイクロストラクチャ内で約１０００回バウンスすることが可能であり、従って２μｍ厚さの「１」層は同等の光学長において２０００μｍの厚さとすることが可能であることを意味しており、従って、本特許明細書において記載するマイクロストラクチャにおいては、光は一層多くのバウンスを行い且つバルク吸収係数を上回わって向上されており且つ近似的に実効吸収＝バルク吸収×マイクロストラクチャ内のバウンス数として書くことが可能な実効吸収を与えることが可能である。光が該マイクロストラクチャ内において費やす時間は光学的走行時間と呼称され、それは該ＭＳ－ＰＤ／ＡＰＤに対する別の基本的な時間である。これら３つの基本的な時間、即ちＲＣ時間、走行時間、及び光学的走行時間を夫々二乗したものの和は全時間を二乗したものを与える。例えば、Ｔ（全時間）^{2}＝Ｔ（ＲＣ時間）^{2}＋Ｔ（走行時間）^{2}＋Ｔ（光学的走行時間）^{2}であり、２０ＧＨｚの場合には、全時間は２０ｐｓとなる場合があり、且つ簡単化のために、ＲＣ時間、走行時間、及び光学的走行時間は全て同じであると仮定すると、各時間は約１１．５ｐｓに過ぎない場合がある。光学的走行時間に対する１１．５ｐｓは約１０００μｍの等価な光学長へ変換され、即ち、３つの基本的な時間の全てが等しいと仮定した場合に、該光学的走行時間が１１．５ｐｓよりも長い場合にそれがＭＳ－ＰＤの帯域幅を劣化させることを開始する前に、該向上された実効吸収長は１０００μｍ又はほぼ２５０のＱである場合がある。

【０１５６】

図９１Ｂは、マイクロストラクチャ型穴アレイが異なる深さにエッチングされた場合の

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図９０（ケース４）におけるエピタキシャル構造を示している。曲線９１２０は，穴がＳｉＯ２層８８０４へエッチングされた場合の８００乃至９００ｎｍの波長の関数としての「Ｉ」Ｓｉ層における吸収を示している。曲線９１２２は、ＳｉＧｅＢ層８８１６へエッチングした穴について波長に対する吸収を示している。両方の場合に、光は上部表面即ちＳｉＮ表面８８１０から入射する。ピーク及び谷がシフトしているが、８００－９００の範囲における殆どの波長において該ＳｉＯ２層への全体的なエッチングは、該ＳｉＧｅＢ層への穴のエッチングよりも良好である。

【０１５７】

図９２は、幾つかの実施例に基づいて、穴をシリコン内へエッチングした場合のシリコンにおけるマイクロストラクチャ型領域を示している概略図である。その例示的な構造は、ＳｉＰ基板９２０２、ＳｉＰ層９２０６、Ｓｉｉ層９２０８及びＳｉＮ層９２１０を包含しており，それら全ての厚さ及びドーピングレベルは図示した如くである。穴９２２２が約２．３μｍの深さへエッチングされており且つ１５００ｎｍの直径及び正方形格子において２０００ｎｍの周期を有している。概略点線の円９２８０で示した該穴が存在する領域は，実効屈折率ｎ１を有しており、それは１０００ｎｍ波長で３００Ｋにおいて約３．４４であるバルクＳｉの屈折率よりも小さい。これは，該エッチングした領域は空気，真空にあるか、又はシリコンの屈折率よりも低い屈折率を有するポリイミド等の物質で充填されていることを前提としている。該マイクロストラクチャに対して上述した寸法に対して、穴を具備する該領域における実効屈折率は近似的に空気部分０．４４×Ｉ＋Ｓｉ部分０．５６×３．４４によって与えられ，それは約２．３６である。例えば、上部表面９２１０に入射するフォトンは、該マイクロストラクチャ内にトラップされ且つ該２つの屈折率不連続部の間でバウンス即ち跳ね返る。一方の不連続部は空気とマイクロストラクチャとの間の界面であり、そこでの屈折率差は約１．３６であり，且つ他方の不連続部はマイクロストラクチャとシリコンとの間の界面であって、そこでの屈折率差は約１．０７である。この屈折率差は該マイクロストラクチャを損失性高コントラストグレーチングとみなすことを可能としており、そのことは観測される吸収の向上を説明することが可能である。

【０１５８】

図９３は、幾つかの実施例に基づいて，テーパー付き穴を具備するＭＳ－ＰＤ構造を示している概略図である。テーパーの付いた漏斗形状の穴９３２２は実効屈折率ｎ１において次第に変化しており、それは穴の直径において著しい変化が無いが領域１におけるよりも一層小さい直径で、例えば、実効屈折率ｎ２を有している領域に対するものよりも一層小さく、その場合に、単にそこでのシリコン物質がより少ないという事実に起因して、領域１における実効屈折率は領域２における実効屈折率よりも一層小さい。領域１において、表面近くの実効屈折率は６０％又はそれ以上のボイド（空気又は例えばポリイミド等の低屈折率物質）と４０％又はそれ以下のシリコンとすることが可能であり、そのことは該上部表面（この場合にはＳｉＮ層）へ垂直に入射するフォトンに対して一層低い反射とさせる。垂直からずれて入射するフォトンにおいては、その反射は更に低いものとなる場合がある。更なる例として，該表面近くにおいて該穴が９０％又はそれ以上を占有し且つＳｉが１０％又はそれ以下を占有する場合には、垂直入射フォトンに対してのフレネル反射は１％又はそれ以下である場合がある。該穴の直径は深さに関して次第に減少しているので，領域１における実効屈折率は次第に変化する。図示例は漏斗であるが、それは、例えば，単に２つの別個の穴直径でのステップ即ち段差とするか、又は段差が該表面から遠ざかるに従い各段差直径が一層小さくなる複数個の穴直径での複数の段差とすることが可能である。

【０１５９】

図９４は，幾つかの実施例に基づいて、次第にテーパーが付いた穴を具備しているＭＳ－ＰＤ構造を示している概略図である。穴の全長にわたり延在している漸次的漏斗形状を有する穴９４２２で別の形態が図示されている。その実効屈折率も深さの関数として次第に増加する。幾つかの実施例によれば，穴は複数の直径、周期、及び／又は異なる漏斗形

状を有する擬似ランダム又はランダム穴で設けることが可能である。種々の穴パラメータは或る波長帯域において吸収特性を改善するか又は最適化させるために使用することが可能である。幾つかの実施例によれば、穴９４２２は各段差が異なる直径を有している一連の段差を設けることが可能である。これらの段差は均一の間隔とさせるか及び／又は不均一の間隔とさせることが可能である。それらの間隔は、波長の特定の帯域において吸収特性を改善させるか又は最適化させるために、例えば、フィルター又は結合型共振器等を形成するために、四分の一波長、半波長、又は四分の一波長及び半波長の倍数とすることが可能である。光学的発光体の場合、該穴又は柱体の直径におけるこの様な段差は、例えば、利得媒体との光波のオーバーラップを改善させることが可能である。幾つかの実施例によれば、穴９４２２の漏斗形状は任意の形状を有することが可能である。例えば、Ｖ形状とすることが可能であり且つ空気・穴界面においての及び穴・シリコン界面においての実効屈折率は反射及び吸収特性又はエミッション特性における向上のために最適化させることが可能である。

【０１６０】

該マイクロストラクチャ型ＰＤ／ＡＰＤと関連する吸収向上に対する別の説明は、該マイクロストラクチャはメタマテリアルであり且つブロードバンド吸収体として振舞うことが可能である。例えば、G. Dayal et al.「ＩＴＯを接地面として使用した可視透過性のブロードバンド赤外メタマテリアル吸収体（Broadband infrared metamaterial absorber with visible transparency using ITO as ground plane）」、オプティックスエクスプレス（OPTICS EXPRESS）、15104 June 2014、N Lie et al.「赤外完全吸収体及びそのプラズモニックセンサーとしての適用（Infrared Perfect Absorber and Its Application As Plasmonic Sensor）」、ナノレター（Nano Lett.）、2010,10,2342-2348、及びL. Meng et al.「近赤外波長における極性感応性完全吸収体（Polarization-sensitive perfect absorbers at nea-infrared wavelengths）」、オプティックスエクスプレス（OPTICS EXPRESS）、A111 Dec 2012（以後、「Ｍｅｎｇ　ｅｔ　ａｌ．」と呼称）を参照すると良く、これら全ての文献は引用により本書に取り込む。

【０１６１】

例えば、Ｍｅｎｇ　ｅｔ　ａｌ．において、複数の溝がクロスバーパターンで交差される場合、吸収は極性独立性である。長尺溝の代わりに、本書において記載するように、Ｍｅｎｇ　ｅｔ　ａｌ．におけるＡｕはシリコン及び／又はゲルマニウム等の半導体で置換されており、且つ穴／溝はボイドであってそれは空気、気体、真空、ポリイミド、及び／又は該穴を部分的に又は完全に被覆する任意の誘電体とすることが可能である。特に、Ｍｅｎｇ　ｅｔ　ａｌ．の図１１においては、その構造がクロスバーである場合には、Ａｕ基板上に誘電体の正方形アレイが存在している。幾つかの実施例によれば、Ａｕは、半導体及び空気、気体、又は二酸化シリコン、窒化シリコン、フッ化カルシウム、スピン・オン・ガラス、ポリイミド、又はパッシベーション誘電体などの誘電体物質で充填されている穴を具備している誘電体で置換されている。Ｍｅｎｇ　ｅｔ　ａｌ．における図１１も波長に対する吸収を示している。

【０１６２】

高コントラストグレーチングは或るクラスのメタマテリアルと考えることが可能である。このことは、その他の効果と共に、観察された吸収向上を説明することが可能な場合がある。その他の効果は、プラズモン、非線形、サブ波長及び近波長効果、フォトニック結晶、導波、結合型共振、干渉、フィールド向上、及び損失を伴う共振を包含している。

【０１６３】

図９５は、幾つかの実施例に基づいて、異なる直径のマイクロストラクチャ型穴を具備している物質構造を示している概略図である。穴９５２２及び９５２４は異なる直径を有している。周期が近似的に同じである場合には、より小さな直径の穴はより大きな直径の穴よりも除去するシリコン物質は一層少ない。より小さな直径の複数の穴９５２２からなるアレイの実効屈折率は実効屈折率ｎ１であり、且つこれらの穴はＭＳ－ＰＤ／ＡＰＤの中心近くにクラスター即ち集めることが可能である。一層大きな直径の複数の穴９５２４

からなるアレイは実効屈折率n_eを有しており、該一層小さな直径の穴の周りにクラスターすることが可能である（例えば、リング形状パターンで）。一層大きな直径の穴９５２４におけるよりも一層小さな直径の穴９５２２において除去される物質は一層少ないので、例えば、n_1はn_eよりも一層大きい。光はn_1領域内に案内され、従って光が該穴・シリコン（この例においてはＰシリコン）界面と該穴・空気界面との間で行ったり来たりバウンスする場合に、例えば回折に起因して失われる光は最小である。更に、メサエッチングは該Ｎシリコン層及び領域９５３０における「Ｉ」シリコン層の全部ではないにしても殆どを除去する。メサ９５４０がエッチングされてこの例に示した如くＮＩＰ接合の容量を画定する。或る場合には、該ＮＩＰ接合容量を画定するためにイオン注入及び／又は拡散を使用することが可能である。そして、或る場合には、該ＮＳｉ層のみを除去し及び／又は低ドーピング又は反対のドーピングへ変換させることが必要であるに過ぎない。該Ｎ及びＰは交換可能であり、例えば、ＭＳ－ＰＤはＰＩＮとし且つＭＳ－ＡＰＤをＮＩＮＩＰ又はＰＩＰＩＮとすることが可能である。

【０１６４】

図９６は、図９５に図示した如く、異なる直径のマイクロストラクチャ型穴を具備する物質構造の平面図を示している。見えるように、より小さな直径の穴９５２２はより大きな直径の穴９５２４の中にクラスターしている。その結果得られるこのマイクロストラクチャ型フォトダイオード／アバランシェフォトダイオード（ＭＳ－ＰＤ／ＡＰＤ）９６００の中心近くにおける領域間での実効屈折率差は、光が一層高い実効屈折率の領域へより一層案内されるというようなオプチカルファイバーと同様の光案内効果を発生させることとなる。エッチング除去された領域９５３０によって画定されているメサ９５４０も示されており、それは更に光案内効果を与えることが可能である。メサ９５４０は、又、ＮＩＰ接合容量を画定し、且つ単にそのＮ層、「Ｉ」層を介して、又はＰ層まで完全にエッチングさせることも可能である。図示していないものは、オーミックコンタクト金属、ボンド金属、パッシベーション、平坦化、ポリイミド、及びその他の誘電体等である。該ＭＳ－ＰＤ／ＡＰＤの開口数は、幾つかの実施例によれば、クラッディング（一層大きな直径の穴）と比較してコア区域（一層小さな直径の穴）内の穴の直径を調節することによって調節することが可能である。実効屈折率を変更させるためには、穴の密度及び直径が或る領域内のシリコン物質の量を調節するための方法である。

【０１６５】

幾つかの実施例によれば、一層高い屈折率のコアと一層低い屈折率のクラッディングとを有する案内構造は、例えば、回折に起因する光損失を減少させるか又は最小とさせるために、光学的導波路等の光案内器として効果的に動作することが可能である。例えば、周期が２３００ｎｍで穴直径が１５００ｎｍである正方形穴格子は近似的な実効屈折率を２．６３とすることが可能であり、及び周期が２０００ｎｍで穴直径が１５００ｎｍである正方形格子は近似的な実効屈折率を２．３６とすることが可能である。一層高い屈折率はコア側で且つ一層低い屈折率をクラッディング側とすることが可能である。該コアとクラッディングとの間の約１０％の屈折率差は該正方形格子の周期を変えることによって達成することが可能である。その他の組合せとすることも可能である。該クラッディングは六角形格子を有することが可能であり且つ該コアは正方形格子を有することが可能であり、その場合に周期及び直径は同じままでも又は変化するものであっても良い。

【０１６６】

図９７Ａ及び９７Ｂは、図８２Ａに示した如き層構造を具備するマイクロストラクチャ上に入射する光に対する吸収を示しているグラフである。六角形及び正方形の格子アレイ内に穴を１５００ｎｍの直径で且つ夫々２０００及び２５００ｎｍの周期でエッチングしている。曲線９７１２は同一の周期及び穴直径を有する正方形格子に対するものである。その吸収は１．４乃至１．６μｍの波長において８０％を越えており、且つ１．５５μｍにおいては六角形格子に対して９０％を越えている。曲線９７１４は、マイクロストラクチャ型穴無しでの吸収であり、１０％又はそれ未満の吸収を与えており且つ１．５５μｍにおいては数％の吸収に過ぎない。更に、六角形格子の場合、吸収は１４５０ｎｍ乃至１

６００ｎｍの波長範囲に亘り１０％未満だけ変化している。図９７Ａは、又、データ及び通信帯域、Ｓ，Ｃ，Ｌ，Ｕ／ＸＬ、を示している。図８２Ａにおけるような構造の場合、ＭＳ－ＰＤ／ＡＰＤはＳ乃至Ｕ／ＸＬのこれら全ての帯域において使用することが可能である。

【０１６７】

図９７Ｂにおいて、曲線９７２０は，周期が２５００ｎｍの六角形穴格子であり且つ穴直径が１５００ｎｍの場合の波長に対する吸収を示しており、且つ曲線９７２２は同じ周期及び直径の正方形格子に対するものである。それは最適性がより低いものであるが、１．５５μｍ波長においては、その吸収は９０％を越えている。曲線９７１４も参照のために示されている。

【０１６８】

吸収と量子効率とは直接的比例関係にあり、且つ最小の反射での約９０％の吸収は約９０％の量子効率と同等である場合がある。例えば、外部量子効率をＱＥ＝（１－Ｒ）（１－$e^{-\alpha x}$）として定義することが可能であり、尚ＲはＭＳ－ＰＤ／ＡＰＤの表面からの反射であり、αは吸収係数であり、且つｘは吸収長である。吸収は（１－$e^{-\alpha x}$）で与えることが可能であり、それは吸収係数がαで長さがｘにおいて吸収されるフォトンの量である。１．５５μｍ波長での９０％の吸収は吸収係数と吸収長との積へ変換され、αｘは約２．３に等しい。バルク吸収係数が使用される場合には，１．５５μｍ波長において４６０／ｃｍであるから、ｘは約５０μｍである。Ｇｅの物理的長さ２．２μｍと比較して、光は吸収領域を約２３回通過したこととなる。等価的に、物理的な吸収長が２．２μｍである場合には、向上される実効吸収係数は１．５５μｍ波長において約１０４５５／ｃｍであり、一方１．５５μｍ波長においてのバルク吸収係数が約４６０／ｃｍであるのと対比される。このことも向上が約２３倍であることを示している。

【０１６９】

該吸収向上は以下の事項のいずれか又は組合せによって発生させることが可能であり、即ち、フィールド向上、干渉、プラズモン、メタマテリアル吸収体，高コントラストグレーチング、波長及びサブ波長特徴寸法、非線形効果、共振効果、損失を伴う高コントラストグレーチング、遅波、結合波、結合型共振、結合モード，及びフォトニック結晶である（例えば、Krauss, J.「フォトニック結晶導波路における低速光（Slos light in photonic crystal waveguides）」、Phys. D: Appln. Phys. 40 2666-2670(2007)を参照すると良く、それを引用により本書に取り込む）。

【０１７０】

更に、吸収に直接的に比例する量子効率はデータ／遠隔通信波長の範囲に亘って高い。標準的な帯域はＳ（１４６０－１５３０ｎｍ），Ｃ（１５３０－１５６５ｎｍ）、Ｌ（１５６５－１６２５ｎｍ）、及びＵ／ＸＬ（１６２５－１６７５ｎｍ）である。示していないその他の帯域も高い吸収効率を有することが可能であり、例えばＯ（１２６０－１３６０ｎｍ）及びＥ（１３６０－１４６０ｎｍ）等である。単一のマイクロストラクチャ型Ｇｅ・オン・ＳｉＰＤ／ＡＰＤは全体的なデータ／遠隔通信波長スペクトルをカバーすることが可能である。例えば、Casca,「ＯからＬへ：光学的波長帯域の未来（From O to L: The Future of Optical-Wavelength Bands）」、www.broadbandproperties.com、ＢＲＯＡＤＢＡＮＳＤ　ＰＲＯＰＥＲＴＩＥＳ、２００８年６月，を参照すると良く、それを引用により本書に取り込む。

【０１７１】

図９８は、図８２Ａに示してあり且つ図９７Ａ及び９７Ｂにおいてシミュレーションした構造に対するシミュレーションした吸収を示しているグラフである。曲線９８１０及び９８１２は六角形格子及び正方形格子の夫々に対する吸収を示している。各場合において，穴周期は２０００ｎｍであり且つ直径は１５００ｎｍであった。該構造は８５０ｎｍ波長範囲において良く吸収しており、８３０乃至１０００ｎｍの間では８０％より良い吸収であることが理解できる。一つの利点は、単一の装置で、７０％より良い吸収及び／又は量子効率で、波長のカバレージは８００乃至１７００ｎｍ及びそれ以上にわたることが可

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能であることである。この様なＧｅ・オン・ＳｉＭＳ－ＰＤ／ＡＰＤはエレクトロニクスと集積化させることが可能であり、従ってＭＳ－ＰＤ／ＡＰＤと相互インピーダンス増幅器又は信号処理用のその他の集積回路エレクトロニクスとを有する単一チップとすることが可能であり、そのことは組立コストやパッケージングコストを著しく低下させる。

【０１７２】

図９９は、幾つかの実施例に基づいて、８００乃至１０００ｎｍの波長範囲において動作するためのＳｉアバランシェフォトダイオード用の別の好適なエピタキシャル構造を示している。特に、図示した構造は、データ通信の多くが行われる８５０ｎｍ±３０ｎｍ回りで且つ５－４０Ｇｂ／ｓ又はそれ以上のデータレートに対して非常に良く動作することが判明している。吸収を向上させるためにマイクロストラクチャが使用され、それは向上された吸収係数及び／又は向上される吸収長のいずれかとすることが可能である。ＮＳｉ基板９９０２は、装置処理の後に、１５０μｍへ薄くさせることが可能である。エピタキシャル層としては、例えば、厚さが０．１－４μｍの範囲で且つ幾つかの場合においては０．３乃至２μの範囲であり且つドーピングが１×１０^{19}／ｃｍ^{3}を越えているＮコンタクト層であるＮＳｉ層９９０６と、厚さが０．２乃至１μｍの範囲で幾つかの場合には０．５μｍであり且つバックグラウンドドーピングが１×１０^{15}／ｃｍ^{3}未満でありアバランシェ層としても知られる増倍即ち利得層であるＳｉイントリンシック即ち「Ｉ」層９９１８と、厚さが０．０２乃至０．３μｍで幾つかの場合には０．１μｍであり且つドーピングが１－６×１０^{17}／ｃｍ^{3}の範囲であり且ついくつかの場合には１．８×１０^{17}／ｃｍ^{3}である電荷層であるＰＳｉ層９９２０と、厚さが０．３乃至４μｍの範囲で幾つかの場合には２μｍであり且つバックグラウンドドーピングが１×１０^{15}／ｃｍ^{3}未満である吸収層であるＳｉイントリンシック「Ｉ」層９９０８と、厚さが０．１乃至２μｍで幾つかの場合には０．３μｍであり且つドーピングが１×１０^{19}／ｃｍ^{3}より大きくＰコンタクト層であるＰＳｉ層９９１０とである。

【０１７３】

図１００は、幾つかの実施例に基づいて、マイクロストラクチャ型ＡＰＤの幾つかの特徴を示している概略図である。該ＭＳ－ＡＰＤは図９９に図示した物質構造を使用している。マイクロストラクチャ型穴アレイ１００２２はＰＳｉコンタクト層９９２０内へ及び「Ｉ」Ｓｉ吸収層９９１８内へ部分的か又は完全にのいずれかでエッチングされる。光は上部表面即ちＰＳｉ層９９１０から該表面へ垂直に及び／又は該表面に対して垂直からずれて入射する。メサエッチングをＮコンタクト層９９０６まで実施して該装置の容量を画定する。Ｐオーミックコンタクト１００２８及びＮオーミックコンタクト１００３０をＰＳｉコンタクト層９９１０及びＮＳｉコンタクト層９９０６上に夫々形成させる。１０－６０ボルトの逆バイアスを該Ｐ及びＮオーミックコンタクトへ印加させる。Ｎコンタクト（カソード）と相対的に負電圧がＰコンタクト（アノード）へ印加される。簡単化のために示していないものは、パッシベーション層，平坦化層、ブリッジング層、ボンドメタリゼーション層、及びガードリング等の要素である。吸収を向上させたマイクロストラクチャ型フォトダイオードとＳｉアバランシェ即ち利得層との結合は、該マイクロストラクチャ型ＳｉＡＰＤが５Ｇｂ／ｓより大きく且つ幾つかの場合には１０Ｇｂ／ｓよりも大きなデータレートで８００－１０００ｎｍの波長範囲で特に８５０ｎｍ±３０ｎｍにおいて動作することを可能とさせる。その他の場合には、該データレートを増倍係数が２，４，６，８，１０又はそれ以上で１５－４０Ｇｂ／ｓとすることが可能である。Ｓｉマイクロストラクチャ型ＡＰＤの一つの利点は過剰ノイズが低いことであり、それは、例えば、ＧａＡｓ及び／又はＩｎＰをベースとしたＡＰＤよりも一層低い。

【０１７４】

図１０１は、幾つかの実施例に基づいて、８００乃至１７００ｎｍの波長範囲においての動作のためのＧｅ・オン・Ｓｉアバランシェフォトダイオード用の別の好適なエピタキシャル構造を示している。特に、図示した該構造は、遠隔通信の多くが行われる１５５０±２００ｎｍ回りで５－４０Ｇｂ／ｓ又はそれ以上のデータレートに対して良好に動作することが判明している。吸収を向上させるためにマイクロストラクチャを使用することが

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可能であり、それは向上された吸収係数及び／又は向上された吸収長のいずれかとすることが可能である。ＮＳｉ基板１０１０２は装置処理の後に１５０μｍへ薄くさせることが可能である。該エピタキシャル層は、厚さが０．１－４μｍの範囲で幾つかの場合には０．３乃至２μｍであって且つドーピングが1×10^{18}／cm^{3}より大きなＮコンタクト層であるＮＳｉ層１０１０６と、厚さが０．２乃至１μｍの範囲で幾つかの場合には０．５μｍであり且つバックグラウンドドーピングが1×10^{18}／cm^{3}未満であるアバランシェ層としても知られている増倍即ち利得層であるＳｉイントリンシック即ち「ｉ」層１０１１８と、厚さが０．０２乃至０．３μｍの範囲であり幾つかの場合には０．１μｍであり且つドーピングが$1-6\times10^{17}$／cm^{3}で幾つかの場合には1.8×10^{17}／cm^{3}である電荷層であるＰＳｉ層１０１２０と、厚さが０．３乃至４μｍの範囲で幾つかの場合には２μｍであり且つバックグラウンドドーピングが1×10^{18}／cm^{3}未満である吸収層であるＧｅイントリンシック「ｉ」層１０１０８と、厚さが０．１乃至２μｍの範囲で幾つかの場合には０．２μｍであり且つドーピングが1×10^{19}／cm^{3}より大きなＰコンタクト層であるＰＧｅ層１０１１０とである。しばしば、ＳｉとＧｅとの間の界面において、通常のＧｅエピタキシャル成長の前に、低温Ｇｅバッファ層を成長させることが可能である。この点については、例えば、Ｋａｎｇ　ｅｔ　ａｌ．を参照すると良い。

【０１７５】

図１０２は、幾つかの実施例に基づいて、マイクロストラクチャ型Ｇｅ・オン・ＳｉＡＰＤの幾つかの特徴を示している概略図である。該ＭＳ－ＡＰＤは図１０１に図示した物質構造を使用している。マイクロストラクチャ型穴アレイ１０２２２は、図９７Ａにおける如きす法、直径及び六角形格子で、ＰＧｅコンタクト層１０１１０内及び部分的に又は完全に「ｉ」Ｇｅ吸収層１０１０８内にエッチングされている。光は上部表面即ちＰＳｉ層から該表面に対し垂直及び／又は該表面に対して垂直からずれてのいずれかで入射する。Ｎコンタクト層１０１０６に対するメサエッチングが本装置の容量を画定し、且つＰオーミックコンタクト１０２２８及びＮオーミックコンタクト１０２３０がＰＧｅコンタクト層及びＮＳｉコンタクト層の上に夫々形成される。１０－６０ボルトの逆バイアスを該Ｐ及びＮオーミックコンタクトへ印加させる。簡単化のために図示していないものは、パッシベーション層、平坦化層、ブリッジング層、ボンドメタリゼーション層、及びガードリング等である。吸収が向上されているマイクロストラクチャ型Ｇｅフォトダイオードと ＳｉアバランシェＰＤ即ち利得層との結合は、マイクロストラクチャ型Ｇｅ・オン・ＳｉＡＰＤが、２より大きく且つ幾つかの場合には４より大きく且つ更に幾つかの場合には８－１０より大きな増倍係数で５Ｇｂ／ｓより大きく且つ幾つかの場合には１０Ｇｂ／ｓより大きく且つ更に幾つかの場合には１５－４０Ｇｂ／ｓより大きなデータレートで８００－１７００ｎｍで特に１５５０ｎｍ±２００ｎｍの波長範囲において動作することを可能とさせる。Ｇｅ・オン・Ｓｉマイクロストラクチャ型ＡＰＤの一つの利点は過剰ノイズが一層低いことであり、それは、例えば、ＧａＡｓ及び／又はＩｎＰをベースとしたＡＰＤよりも一層低い。

【０１７６】

図１０３（Ａ）－（Ｃ）は、幾つかの実施例に基づいて、マイクロストラクチャ型シリコン及びゲルマニウム・オン・Ｓｉフォトダイオード及びアバランシェフォトダイオードに対する直径、周期、及びその他のパラメータを示している。図１０３（Ａ）は、使用した種々のパラメータを示している表である。幾つかの実施例によれば、六角形及び正方形の両方の格子を使用することが可能である。複数の穴のその他の格子及び／又は非格子配置も可能であるが、図示してはいない。１０，２５，３０，４０，５０，６０，８０μｍのメサす法は５乃至８０を越えるＧｂ／ｓのデータレートをサポートするための容量を達成するために使用される。幾つかの実施例によれば、キャリアーを枯渇させるためにイオン注入又は拡散などの接合容量を画定するその他の方法を使用することが可能である。８００－１０００ｎｍで特に８５０ｎｍ±３０ｎｍの波長範囲におけるＳｉマイクロストラクチャ型ＰＤ及びＡＰＤの動作のための穴直径及び周期は、例えば、六角形及び／又は正

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方形格子のいずれかに対して１３００／２０００，１５００／２０００，７００／１０００，６３０／９００（ｎｍ単位での直径／周期）の範囲にわたることが可能である。Ｇｅ・オン・Ｓｉマイクロストラクチャ型ＰＤ及びＡＰＤの場合，８００－１７００ｎｍで特に１５５０ｎｍ±２００ｎｍの波長範囲における動作に対して、六角形又は正方形のいずれかの格子に対する穴直径と周期との組合せの例は、１３００ｎｍ／２０００ｎｍ、１５００ｎｍ／２０００ｎｍ、１５００ｎｍ／２５００ｎｍ、１３００ｎｍ／２３００ｎｍを包含している。その他の穴直径及び周期とすることも可能である。５０％よりも良好な、及び、幾つかの場合には、７０％又は９０％よりも良好な吸収は、８００－１０００ｎｍ及び８００－１７００ｎｍの波長においてこれらの直径及び周期で達成することが可能である。図１０３（Ｂ）及び（Ｃ）において、「ｄ」は六角形及び正方形の格子パターンに対する周期として示されている。円形状の穴が図示されているが、楕円、矩形，多角形、及び／又はその他の不規則形状等の非円形状の穴も可能である。円形状の穴はＦＤＴＤを使用するシミュレーションの簡単化のために選択されているに過ぎない。

【０１７７】

図１０４（Ａ）及び（Ｂ）は、マイクロストラクチャ型ＧｅＰ－Ｇｅｌ－ＳｉＮ・オン・ＳｉＮ基板フォトダイオードである図８２Ａに示した構造に関して波長に対しての吸収についてＦＤＴＤ（有限差分時間領域）を使用したシミュレーション結果を示しているグラフである。注意すべきことであるが、このシミュレーション結果はマイクロストラクチャ型ＧｅＰＧｅＩＳｉＰＳｉＩＳｉＮＡＰＤへ適用することも可能である。該シミュレーションは六角形格子、１５００ｎｍの穴直径、２０００ｎｍの穴周期を使用しており、その場合に，該穴は該ＳｉＮ層へエッチングされる。このシミュレーションにおいては、波長は１５００ｎｍ±１０ｎｍ（図１０４（Ａ）における曲線１０４１０）を且つ１５５０ｎｍ±１ｎｍ（図１０４（Ｂ）における曲線１０４１２）を中心としている。そのシミュレーションメッシュは０．１ｎｍよりも一層細かく、且つ図１０４（Ｂ）における曲線１０４１２から、吸収は、１５４９乃至１５５１ｎｍ波長にわたって，０．９（９０％吸収）を越える高吸収値及び０．８５（８５％吸収）を越える低吸収値で、１０％未満の変動であることを理解することが可能である。波長に対する吸収におけるこの特性は光学的遠隔通信適用例において重要であり，その場合には、例えば，１５５０ｎｍを中心とした波長変動の２ｎｍ以内の吸収において迅速な変化は存在しない。図１０４（Ａ）における曲線１０４１０は、１５５０ｎｍを中心とする２０ｎｍの波長変動をこえる０．８乃至０．９９の吸収変動を示している。どの２ｎｍの波長変動にわたっても、その吸収変動は１５％未満である。或る場合には、それは５％未満である。粗ＷＤＭに対する波長分割多重化（ＷＤＭ）におけるチャンネル間隔は２ｎｍ又はそれより大きいものとすることが可能であり、一方密ＷＤＭに対しては、チャンネル間隔は０．８、０．４又はそれ未満とすることが可能であり、従って、例えば，１５５０ｎｍにおいて，３個又はそれ以上のチャンネルが２ｎｍ分光幅内に適合することが可能であり、一方粗ＷＤＭに対しては，４ｎｍ又はそれ以上が必要とされる。

【０１７８】

図１０５（Ａ）及び（Ｂ）は、幾つかの実施例に基づいて，正方形格子穴パターンに対する固有モードに関するものである。図１０５（Ａ）は正方形格子配置における単一の単位セル１０５１０を示している。図１０５（Ｂ）は、Ｓｉ（又はＧｅ）物質におけるマイクロストラクチャ型穴の単位セルにおける種々の２Ｄ固有モード（静止モード、定常波モード、共振モード）（マクスウエル方程式を使用するＦＤＴＤシミュレーションから）を示している。波は、例えば、空気／半導体界面とＧｅ／Ｓｉ界面との間を、該マイクロストラクチャ型穴アレイの長さに沿って伝播する。該マイクロストラクチャ型穴がエッチングされている領域によって導波路及び／又は共振器が画定されている。該単位セルにおける半導体及び穴の長さは光学的導波路及び／又は共振器と考えることが可能であり、且つ隣接する単位セルの多くの並列光学的導波路／共振器は結合されて，２Ｄアレイにおける結合された波、結合されたモード、及び／又は結合された共振器となることが可能である。高コントラストグレーチング（ＨＣＧ）、フォトニック結晶、遅波効果及び結合された

導波路／共振器の固有モード、スーパーモード、フィールド向上、線形及び非線形効果、横モード、導波共振モード（guided resonant modes）、ブロッホ（Bloch）モード、及び結合されたブロッホモードの組合せは吸収である（１－ｅ^（－αｘ））に比例する量子効率に対する式における「αｘ」積の観察される向上を発生させることが可能であり、尚αはバルク物質吸収係数であり且つｘは吸収長である。ｘが一定である場合には、αを向上させることが可能であり、αが一定である場合には、ｘを向上させることが可能であり、且つ幾つかの場合には、αとｘの両方を向上させることが可能である。図１０５（Ｂ）は、図１０５（Ａ）における正方形格子の単位セル１０５１０の多くの複雑な固有モードを示している。該正方形格子における各セルはこれらの固有モードの内のいずれか一つ又は複数を有することが可能であり且つ隣接するセルの固有モードと結合することが可能であり、これら全てのセルの大量に結合されたモードはスーパーモードと呼ばれる。この大量の結合は、波長に対して「一層滑らかな」吸収特性となる場合があり、尚一層滑らかとは或る波長範囲，例えば２０ｎｍで或る場合には５０ｎｍで且つ或る場合には１００ｎｍ又はそれ以上、にわたっての吸収特性においての変動が１０％未満であるものとして定義することが可能である。

【０１７９】

図１０６は、幾つかの実施例に基づいて，互いにオーバーラップして配置された２個の正方形格子でのマイクロストラクチャ型穴を示している概略図である。点線の正方形１０６１０は穴直径としてＤ１を有する正方形格子の単位セルを表している。破線の正方形１０６１２は同様の周期であるが穴直径としてＤ２を有している別の正方形格子を表しており、Ｄ１とＤ２とは等しくない。もしもＤ１がＤ２と等しい場合には，それは正方形格子（４５度だけ傾斜）である。又は、等価的に，これら２つの正方形格子の周期が同様のものである場合には，２つの異なる穴直径を有する六角形格子として考えることも可能である。該格子パターンは、２つを越えて異なる穴直径を有することも可能であり、例えば、六角形格子において３つの異なる穴直径を有することが可能である。例えば、複数の穴からなる一つの好適なマイクロストラクチャにおいて、Ｄ１は１３００ｎｍ直径とすることが可能であり且つ該正方形格子は２０００ｎｍの周期を有することが可能である。マイクロストラクチャアレイにおいて一つを越える穴直径を有することの一つの利点は、波長に対する吸収の曲線が更に平坦化されて，吸収における変動が、Ｓｉ内に構成されるマイクロストラクチャ型ＰＤ／ＡＰＤに対する波長において８００－９９０ｎｍにわたり、且つ図１０１におけるようなＧｅ・オン・Ｓｉ内に構成されるマイクロストラクチャ型ＰＤ／ＡＰＤに対する１２５０－１７５０ｎｍの波長に対して、２０％未満とすることが可能であるということである。幾つかの場合において，該変動はこれらの波長範囲に亘っての変動は１０％未満であり，且つ幾つかの場合には，５％未満である。又、全体的な吸収又は等価的に該マイクロストラクチャ型ＰＤ／ＡＰＤの量子効率を改善させることが可能である。

【０１８０】

異なる穴直径を散在させることは吸収に直接比例する量子効率を一層広い範囲の波長、特に、シリコンにおけるマイクロストラクチャ型ＰＤ／ＡＰＤに対して８００－９９０ｎｍで且つＧｅ・オン・Ｓｉにおけるマイクロストラクチャ型ＰＤ／ＡＰＤに対して１０００－１８００ｎｍ、にわたって更に平坦化させることを可能とする。幾つかの実施例によれば、その他の穴直径及び周期とすることも可能である。

【０１８１】

幾つかの実施例によれば、例えば吸収用物質の厚さなどの設計パラメータ内において適切な量子効率を維持するのにバルク吸収係数が不十分である場合に、ＰＤ／ＡＰＤの量子効率を向上させるために使用されるマイクロストラクチャ型穴及び／又は柱体の吸収における改良は、太陽電池、イメージング用センサー、ラディエーション吸収体等のフォトンの吸収を使用するその他の装置へ適用させることが可能である。

【０１８２】

図１０７は、幾つかの実施例に基づく、Ｇｅ・オン・Ｓｉのエピタキシャル構造を示し

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ている概略図である。該構造は図８２Ａに図示したものと同様であるが、Ｎドーピングが１×１０^{19}／ｃｍ^{3}を越えている０．２μｍ（又は０．１－２μｍの範囲）のＳｉＮ層１０７０６上に成長されたバックグラウンドドーピング（Ｎ又はＰのいずれかとすることが可能）が１－５×１０^{14}／ｃｍ^{3}で０．１－０．５μｍ厚さのＳｉＩ層１０７１８が付加されており、次いで意図的にはドーピングされておらずバックグラウンドドーピングが５×１０^{19}／ｃｍ^{3}未満で幾つかの場合には５×１０^{15}／ｃｍ^{3}未満であり且つ厚さが２μｍ又は０．５－２．５μｍの範囲であるＧｅＩ層１０７０８がそれに続いている。ＰＧｅ層１０７１０が最上部でドーピングが１×１０^{19}／ｃｍ^{3}を越えており且つ厚さが０．２μｍ又は０．２－０．５μｍの範囲である。これらの層の全てがＮＳｉ基板１０７０２上に成長される。マイクロストラクチャ型穴アレイ１０７２２は図１０３（Ａ）（Ｃ）に示したパラメータを使用して形成することが可能である。幾つかの実施例によれば、穴直径は１３００－１５００ｎｍであり且つ周期は六角形又は正方形の格子において２０００ｎｍである。その他の実施例によれば、図１０６に示したようなレイアウトが使用される。その様な場合には、複数の直径を有する穴は、例えば、図１０６に示した如く互いに入れ子構造とさせた周期２０００ｎｍの１３００ｎｍ及び１５００ｎｍの正方形格子とすることが可能である。

【０１８３】

ＳｉＩ層１０７１８は、ＧｅＩ層を成長させることを可能とさせるためにＧｅＩ層１０７０８内へのドーパント拡散が減少されるか又は最小とされるようにＳｉにおけるドーパントを低いレベルとさせるために使用される。

【０１８４】

幾つかの実施例によれば、図１０７に示した構造はマイクロストラクチャ型ＰＤ用であり且つ、図１０１における如く、増倍層と電荷層とを付加したマイクロストラクチャ型ＡＰＤ用とすることも可能である。この構造に対する波長範囲は８００－１７００ｎｍで、特に約１５５０ｎｍ±２００ｎｍとすることが可能である。

【０１８５】

付加したＳｉ「Ｉ」層１０７１８は本装置の容量を減少させることにも寄与する。何故ならば、該「Ｉ」層は今や該ＧｅＩ層と該ＳｉＩ層との総和だからである。容量における減少はＰＤ／ＡＰＤの変調帯域幅を増加させることを助ける。該Ｓｉ「Ｉ」層は、幾つかの場合において、その厚さが、例えば０．１乃至３μｍの範囲である場合がある。穴１０７２２は、例えば、該Ｓｉ「Ｉ」層までエッチングすることが可能であり、及び／又は幾つかの場合においては該Ｓｉ「Ｉ」層内へエッチングすることが可能である。

【０１８６】

図１０８は、幾つかの実施例に基づいて、Ｇｅ・オン・Ｓｉのマイクロストラクチャ型フォトダイオードの基本的な特徴を示している概略図である。該構造は図１０７に図示したものと同様であるか又は同一である。該ＭＳ－ＰＤは１３００－１７００ｎｍ及び６００－１３００ｎｍの波長範囲において良好に動作することが判明している。図示した如く、光は穴アレイがエッチングされている上部表面から入射する。幾らかのマイナーチェンジでもって、底部上のＮオーミックコンタクト１０８３２に開口を設け且つＳｉ基板１０７０２の底部を反射防止コーティングでポリッシュした場合には、光は該基板の底部から入射することも可能である。更に、オプチカルファイバーを該マイクロストラクチャ型ＰＤに対してアライメント即ち整合させるためのガイドを与えることが可能であるようにＳｉ基板１０７０２の底部上にピア（不図示）を形成することが可能である。この例においては、穴１０７２２はＳｉＩ層１０７１８までエッチングされる。幾つかの実施例によれば、該穴は該ＳｉＩ層内へ又はそれを通過してエッチングさせるか、又は該ＳｉＩ層まで貫通してエッチングさせないことが可能である。穴アレイは複数の穴寸法及び複数の周期を有することが可能であり、且つ非周期的なものとさせることが可能である。穴直径は５００－１７００ｎｍの範囲とすることが可能であり、且つ周期は１０００－２５００ｎｍの範囲とすることが可能である。幾つかの実施例によれば、穴直径は１３００及び１５００ｎｍで、正方形又は六角形の格子における周期が２０００ｎｍである。更に、１３００

及び１５００ｎｍの穴は、図１０６に示した如くに互いに入れ子とされている周期が２０００ｎｍの正方形格子内のものとすることが可能である。穴直径及び周期は１０－５０ｎｍだけ、且つ幾つかの場合においては５０－１００ｎｍだけ変化する場合がある。図示していないものとしては、パッシベーション層であって、それは該半導体の壁上に２－１００ｎｍの厚さを有する場合がある。パッシベーションは漏洩電流を減少させるために露出されているメサの高電界領域において使用することが可能である。－２乃至－１２ボルトの逆バイアスがＰコンタクト１０８２８とＮコンタクト１０８３０（及び／又は１０８３２）との間に印加される。逆バイアスとは、負電圧がＮ（カソード）コンタクトと相対的なＰ（アノード）へ印加されることを意味している。負記号を付けて又は付けずに示されている電圧は、カソードと相対的にアノードにおいて負であることを意味している。更に、複数の穴は異なる形状を有することが可能であり、必ずしも全てが円形状であることは必要ではない。

【０１８７】

光検知器においてナノワイヤーを使用することは既知である。該ナノワイヤーはＩｎＰであり且つ該光検知器は１４ｐｓ応答時間、又は等価的に、ガウス変換に対する周波数領域において、約３０ＧＨｚ３ｄＢ変調帯域幅に制限されることを示している。V.J. Logeeswaran et al.「非晶質表面上の交差するＩｎＰナノワイヤーで製造された１４ｐｓ半値全幅高速光導電体（A 14-ps full width at half maximum high-speed photoconductor fabricated with intersecting InP nanowires on an amorphous surface）」、アプライドフィジックス（Appl.Phys.）、Ａ９１，１－５（２００８）（以後、「Ｌｏｇｅｅｓｗａｒａｎ　ｅｔ　ａｌ．」という）を参照すると良く、これを引用により本書に取り込む。Ｌｏｇｅｅｓｗａｒａｎ　ｅｔ　ａｌ．においては、入射するフォトンは７８０ｎｍにおいてであり且つ約７８０ｎｍにおけるＩｎＰ吸収係数は約３５０００ｃｍ$^{-1}$であり且つ吸収の向上も吸収長も必要なものではなかった。同様に、別の既知の技術において，８５０ｎｍフォトンがナノワイヤー上に入射され且つ約８５０ｎｍにおけるＧａＡｓの吸収係数は約１２０００ｃｍ$^{-1}$であり、その場合も吸収の向上及び／又は長さが必要なものではなかった。M.A. Seyedi et al.「大活性区域で９ＧＨｚ変調帯域幅での効率的なショットキー状接合ＧａＡｓナノワイヤー光検知器（Efficient Schottky-like junction GaAs nanowire photodetector with 9GHz modulation bandwidth with large active area）」、アプライドフィジックスレターズ（APPLIED PHYSICS LETTERS）、１０５，０４１１０５（２０１４）を参照すると良く、これを引用により本書に取り込む。対照的に、本書に記載する技術によれば、高速フォトダイオード／アバランシェフォトダイオードがｐｓ応答時間及び／又は５Ｇｂ／ｓ又はそれ以上にの変調帯域幅で記載されている。８５０ｎｍにおけるＳｉにおいて、吸収効率は約７００ｃｍ$^{-1}$であり且つ吸収の向上及び／又は吸収長を使用して４０％又はそれより良い量子効率を達成している。同様に，Ｇｅに対して約１５５０ｎｍにおいて，その吸収効率は約４５９ｃｍ$^{-1}$であり、それもまた吸収の向上及び／又は吸収長を使用している。

【０１８８】

例えば、約１０－３０Ｇｂ／ｓにおける動作のための典型的な高速又は高変調帯域幅ＰＤ／ＡＰＤ用の２μｍ厚さの吸収用「Ｉ」層の場合（該「Ｉ」層は該ＰＤ／ＡＰＤの変調帯域幅に依存して０．３－３．５μｍ変化することが可能），８５０ｎｍにおけるフォトンの約１３％が向上無しで吸収される。例えば、本特許出願において記載するマイクロストラクチャ型穴アレイ（又は柱体）によって約１２倍又はそれ以上だけの吸収の向上及び／又は吸収長がある場合には、フォトンの８０％を超えるものを２μｍの物理的な「Ｉ」吸収長において吸収させることが可能である。夫々８５０及び１５５０ｎｍのデータ通信波長及び遠隔通信波長においてＳｉ及びＧｅ等の弱い吸収性（約１０００ｃｍ$^{-1}$又はそれ未満）物質を使用する場合にマイクロストラクチャ型穴及び／又は柱体を付加すると、その吸収即ち吸収係数及び／又は吸収長を、該物質が強く吸収性となり（約２０００ｃｍ$^{-1}$又はそれ以上）且つ該マイクロストラクチャ型ＰＤ／ＡＰＤを高速又は高変調帯域幅データ及び遠隔通信適用例及びシステムのために使用することが可能である点まで向上さ

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せることが可能であることがここで証明された。

【０１８９】

幾つかの場合においては、或る光学的データ／遠隔通信のためには単に約４０％の吸収で十分であり、且つ単に約３倍の吸収の向上及び／又は吸収長が、例えば、８５０ｎｍにおいての２μｍＳｉ「Ｉ」層に対して必要とされるに過ぎず、又は２μｍＧｅ「Ｉ」層に対しての１５５０ｎｍ波長におけるＧｅに対する吸収係数又は吸収長の４、５倍の向上係数が必要であるに過ぎない。一層高い向上係数が可能であり、１０より大きな係数、且つ幾つかの場合においては２０より大きなもの及び幾つかの場合においては４０より大きいものとすることが可能である。半導体バルク物質の吸収係数が一層小さくなるに従い、向上係数は一層大きくなり、１００又はそれ以上となる。

【０１９０】

Ｓｉナノワイヤーの吸収は、Lu Hu, Gang Chen.ナノレターズ（Nano Lett.）「光電池適用例に対するシリコンナノワイヤーアレイにおける光学的吸収の解析（Analysis of Optical Absorption in Silicon Nanowire Arrays for Photovoltaic Applications）」、Ｖｏｌ．７、Ｎｏ．１１，２００７（以後、「Ｈｕ　ｅｔ　ａｌ．」と呼称する）において討論されており、それを引用により本書に取り込む。８５０ｎｍに対応する１．４６ｅＶにおいての吸収は薄いＳｉ膜と比較して向上されず、且つ約２．２５ｅＶの上即ち約５５０ｎｍ又はそれより短い波長の場合には、吸収は薄いＳｉ膜と比較して向上される。Ｈｕ　ｅｔ　ａｌ．は、更に、「一方、低周波数範囲においては、シリコンの吸光係数（extinction coefficient）は小さいために改良を達成することは不可能である」と付け加えている。

【０１９１】

同様の結論は別の刊行物においても到達されており、即ち、Chenxi Lin, Michelle L. Provinelli「光電池適用例に対する大きな格子定数を有するシリコンナノワイヤーアレイにおける光吸収の向上（Optical absorption enhancement in silicon nanowire arrays with a large lattice constant for photovoltaic applications）」、Vol. 17, No. 22／オプティクスエクスプレス（OPTICS EXPRESS）、１９３７１、２００９年１０月２６日（以後、「Ｌｉｎ　ｅｔ　ａｌ．」と呼称する）があり、それも引用により本書に取り込む。Ｌｉｎ　ｅｔ　ａｌ．は約１．５ｅＶにおいての吸収の共振向上を示しており、そのことをＬｉｎ　ｅｔ　ａｌ．はナノ構造において電磁界強度の増大となるガイド共振モード（guides resonance mode）又は遅ブロッホモード（slow Bloch mode）によるものであるとしている。Ｌｉｎ　ｅｔ　ａｌ．は「空中からの入射光を２Ｄ周期的構造の高Ｑ漏洩モードへの結合」と述べている。高Ｑモードのシャープな共振はデータ及び／又は遠隔通信適用例に対するフォトダイオードの使用において望ましいものではない。共振フォトダイオードの特性は、例えば、J. D. Schaub et al.「エピタキシャル横方向過剰成長により成長された共振空胴向上型高速Ｓｉフォトダイオード（Resonant-Cavity-Enhanced High-Speed Si Photodiode Grown by Epitaxial Lateral Overgrowth）」、ＩＥＥＥフォトニクステクノロジーレターズ（IEEE POTONICS TECHNOLOGY LETTERS）、VOL. 11, No. 12,　１９９９年１２月（以後、「Ｊ．Ｄ．Ｓｃｈａｕｂ　ｅｔ　ａｌ．」と呼称する）において討論されており、尚その文献を引用により本書に取り込む。Ｓｃｈａｕｂ　ｅｔ　ａｌ．は約８００ｎｍ波長において高々４０％の量子効率を示している（例えば、Ｓｃｈａｕｂ　ｅｔ　ａｌ．における図３を参照）。しかしながら、そのシャープな共振は望ましいものではない。何故ならば、温度に起因する送信機の波長におけるドリフト（例えば、或るダイオードレーザーに対して０．３ｎｍ／度であり、且つジュール加熱及び環境に起因するレーザー内部温度は、例えば、データセンターにおいて高々８０℃又はそれ以上変化する場合がある）は、例えば、量子効率において著しい変化を発生させる場合がある。シャープな共振を有する従前に既知の共振フォトダイオードも量子効率が最高であるピーク共振波長の点で温度に敏感である場合がある。更に、レーザー源は、しばしば、製造上の変動に起因してレーザー波長において変動を有しており、レーザーをフォトダイオードに対して波長において精密に整合させねばならないことは望ましいことではない。共振フ

ォトダイオードの製造における変動は変化する波長における共振ピークとなる場合もある。このことは、該レーザー源と検知器の波長を整合させることの必要性のために注意深いテスト及び温度安定性を維持することが必要であるので、歩留まりを低下させ且つ光学システムのコストを増加させることとなる。

【０１９２】

最近の文献であるRui Ren, Yong-Xin Guo, Ri-Hong Zhu「太陽エネルギー収穫用楕円シリコンナノワイヤーアレイにおける向上された吸収（Enhanced absorption in elliptical silicon nanowire arrays for solar energy harvesting）」オプチカルエンジニアリング（Optical Engineering）５３（２）、０２７１０２（２０１４年２月）も１．５ｅＶにおいての向上が弱いか又は存在しないが一層高いエネルギーにおける吸収の向上が一層強いという同様の結果を示しており、尚その文献を引用により本書の取り込む。

【０１９３】

Donnelly et al.「光電池適用例用シリコンナノホールアレイのモードに基づく解析（Mode-based analysis of silicon nanohole arrays for photovoltaic applications）」、Ｖｏｌ．２２、Ｎｏ．Ｓ５、オプティックスエクスプレス（OPTICS EXPRESS）、Ａ１３４３　２０１４年８月２５日、（以後「Ｄｏｎｎｅｌｌｙ　ｅｔ　ａｌ．」と呼称する）において、ナノホールが光電池適用例について解析されており、尚その文献を引用により本書に取り込む。太陽のスペクトルは非常に広い（数百ｎｍ）ので、シャープな共振は光電池適用例においては問題ではないが、一方光学的データ／遠隔通信においては、レーザーのスペクトルは非常に狭く、例えば、分布帰還形レーザ、ファブリー・ペローレーザー、垂直共振器面発光レーザー（ＶＣＳＥＬ）等のレーザーのタイプ、及びそれが単一モードであるか又はマルチモードであるか、及びそれが外部変調又は直接変調でのＣＷで動作されるか否かに依存して、１ｎｍよりもかなり小さいものから数ｎｍ、即ち０．０１未満～３ｎｍと狭いものである。Ｄｏｎｎｅｌｌｙ　ｅｔ　ａｌ．は、又、例えば、その図４において８００ｎｍにおいて２０ｎｍの波長スパンに亘って高々７５％又はそれ以上だけの吸収における変動と共に８５０ｎｍ波長領域においてシャープな共振を示している。Ｄｏｎｎｅｌｌｙ　ｅｔ　ａｌ．の図５は、種々のナノホール深さでの５００ｎｍの最適な周期を示しており、又、例えば、８５０ｎｍ波長においてシャープな共振を示しており、その場合に吸収は１０ｎｍ波長スパンに亘って約１００％乃至２０％変化、即ち吸収において約８０％の変化する場合がある。共振導波モード（resonance guided mode）に加えて、該文献は基本モード及び吸収向上を発生させることが可能なチャンネリングモードも包含している。

【０１９４】

量子効率に直接的に比例する吸収におけるリップルが約３０％－４０％、及び幾つかの場合においては２０％以下又は１０％以下はデータ通信適用例及び遠隔通信適用例に対して許容可能なものである。幾つかの場合において、約８５０ｎｍの中心波長、例えば、±５，１０，２０，５０又は１００ｎｍに対して、量子効率のリップルは５％以下が望ましい。

【０１９５】

実験的には、光トラッピング及び向上された吸収はErik Garnett, Peidong Yang「シリコンナノワイヤー太陽電池における光トラッピング（Light Trapping in Silicon Nanowire Solar Cells）」、ナノレター（Nano Lett.）、２０１０，１０，１０８２－１０８７（以後、「Ｇａｒｎｅｔｔ　ｅｔ　ａｌ．」と呼称する）において観察されており、尚該文献を引用により本書に取り込む。Ｇａｒｎｅｔｔ　ｅｔ　ａｌ．の図４は、１１００ｎｍまでの波長において１０％未満で且つ８５０ｎｍ波長において約５％の光透過を示しており、反射を無視することが可能である場合には，吸収はＩ＝Ｔ＋Ｒ＋Ａの式から約９０－９５％であり、尚Ｔは透過で、Ｒは反射で、Ａは吸収であり、全ての光が回収されるものと仮定している。

【０１９６】

別の最近の文献であり引用により本書に取り込むKatherine T. Fountaine, Christian

G. Kendall, Harry A. Atwater「局所化したラジアルモード励起を介しての半導体ナノワイヤーアレイ用の１に近いブロードバンド吸収デザイン（Near-unity broadband absorption design for semiconducting nanowire arrays via localized radial mode excitation）」Ｖｏｌ．２２，Ｎｏ．オプティックスエクスプレス（OPTICS EXPRESS）Ａ９３０，２０１４年５月５日（以後、「Ｆｏｕｎｔａｉｎｅ　ｅｔ　ａｌ．」と呼称する）において，異なる直径を有する３μｍ高さのＳｉ上のＧａＡｓナノワイヤーのシミュレーション結果は、５％の充填率で１に近い吸収を達成することが可能であることを示している。Ｆｏｕｔａｉｎｅ　ｅｔ　ａｌ．の図４を参照すると良い。該シミュレーションの目的は，高効率光電池装置を達成するために物質の使用を減少させることであり、３μｍＧａＡｓナノワイヤーでの５％の充填率は物質の量について平坦状のＧａＡｓ層の１５０ｎｍと等価である。しかしながら、吸収向上の適切な比較は、３μｍＧａＡｓナノワイヤーを３μｍ厚さのＧａＡｓの平坦状の層と比較することである。この場合には、該平坦状ＧａＡｓ３μｍ層は、１．４２ｅＶのバンドギャップ端部又は８７３ｎｍに到達するまでは１の吸収を有し、且つそれは急激に降下し、８８６ｎｍにおいては吸収係数は約２４１／ｃｍであり、その場合に、例えば強い吸収性である８５５ｎｍにおいての約５９１７／ｃｍと比較して弱い吸収性であり、及び３μｍ厚さの層の約７％が８８６ｎｍにおいて吸収され、８５５ｎｍにおいて約８３％の吸収であり，且つ８２７ｎｍにおいて約９９％の吸収である。３μｍＧａＡｓ層をＦｏｕｏｔａｉｎｅ　ｅｔ　ａｌ．の図４と比較すると、何ら吸収の向上は認められない。知覚しうる吸収向上無しでは、バルク層フォトダイオードのものを越えてナノワイヤーフォトダイオードを使用することの利点は無い。この場合には、８００－８５０ｎｍにおけるデータ／遠隔通信用の３μｍＧａＡｓナノワイヤーフォトダイオードよりも一層良いものではないとしても、バルク３μｍＧａＡｓフォトダイオードはほぼ同程度に良く動作する。

【０１９７】

本書に記載する技術によれば，例えばＳｉにおける２μｍマイクロストラクチャ型穴（柱体及び／又は柱体と穴とすることも可能）が，例えば，５Ｇｂ／ｓ以上の高いデータレートのデータ／遠隔通信のための８００－９００ｎｍ波長において２μｍＳｉバルク層フォトダイオードよりも著しく一層吸収性であるように吸収（係数及び／又は長さ）の向上が提供される。

【０１９８】

図１０９（Ａ）及び（Ｂ）は，幾つかの実施例に基づいて、マイクロストラクチャ型穴アレイに対してマクスウエルの式を使用したＦＤＴＤシミュレーションの結果を示しているグラフである。該穴アレイは、２０００ｎｍ周期の六角形格子を有しており且つ２μｍの「Ｉ」厚さのＳｉＮＩＰの図９２に類似したエピタキシャル構造を有しており且つ穴は該Ｉ層を貫通してエッチングされており且つ２つの穴直径（図１０６に示した如く）を有している。図１０９（Ａ）は、１６７０及び１５００ｎｍの穴直径を使用する曲線１０９１０を含む４つのケースについて波長に対する吸収を示しており、一方、図１０９（Ｂ）は、１６７０及び１５００ｎｍの穴直径を使用する曲線１０９１０を含む該４つのケースの内の２つのケースについて誇張した尺度での波長に対する吸収を示している。該シミュレーションは、８４０乃至８６０ｎｍの波長に亘って１０％未満のリップルを示しており，平均吸収は約９０％である。更に、８３５－８７５ｎｍ波長の間の領域は入射フォトンの８０％以上の吸収を有することが可能である。１個を越える穴直径及び／又は周期の付加は該波長に対する吸収の曲線におけるリップルを減少させる。異なる共振モード、異なる穴直径及び／又は周期を有している異なる構造の固有モードの結合は、リップルを減少させ且つ一層広い波長範囲に亘っての吸収の向上を改善させ、且つ約２μｍ厚さのＳｉ物質において８５０ｎｍにおいて８０％よりも大きな量子効率に直接比例する高い吸収効率を達成することに貢献する。幾つかの場合において、８５０ｎｍ±１０ｎｍにおいて９０％より大きなものを達成することが可能である。幾つかの場合において、８５０ｎｍ±１０ｎｍにおいて、７０％、６０％、５０％又は４０％より大きな量子効率を達成することが可能である。

【０１９９】
その他の穴直径も示されており、例えば１３３０及び１５００ｎｍ、１５００及び１５００ｎｍ、１６７０及び１６７０ｎｍは全て周期が２０００ｎｍであり且つリップルは他の場合よりも或る波長範囲において一層良好であり、従って、例えば８５０ｎｍ±１０ｎｍ等の或る波長範囲に対してマイクロストラクチャ型ＰＤ／ＡＰＤを設計する場合に、周期が２０００ｎｍの六角形格子における該１５００ｎｍ穴寸法は、２μｍＳｉ「Ｉ」層においてリップルが１０％未満で８０％より大きな吸収を達成することが可能である。更に、１３３０ｎｍ及び１５００ｎｍの穴、及び、前述した如く、周期が２０００ｎｍの六角形格子での１５００及び１６７０ｎｍ直径の穴もこの性能をほぼ達成することが可能である。従って、９００乃至２０００ｎｍの周期の範囲で６００乃至１７００ｎｍの穴寸法の範囲を使用して２０ｎｍ又はそれ以上のスペクトル範囲での特定の波長範囲を設計することが可能である。その他の直径及び周期を使用することも可能であり、記載した例は、穴直径と周期との或る組合せは、リップルが１０％、２０％、３０％、４０％、５０％未満で吸収を向上させることが可能であることを示している。

【０２００】
該穴直径は波長より大きいものとするか又は波長未満とすることが可能であり、且つ自由空間における該周期は波長よりも一層大きい。サブ波長周期も或る波長以上の周期と関連して使用することが可能である。

【０２０１】
この例は、２０ｎｍ及び幾つかの場合には１０ｎｍ及び幾つかの場合には４０ｎｍ以上の有用なスペクトル範囲で、５Ｇｂ／ｓ、及び幾つかの場合には１０Ｇｂ／ｓ及び幾つかの場合には２０Ｇｂ／ｓ、及び幾つかの場合には３０－４０Ｇｂ／ｓ以上を超えるデータレートで、Ｓｉにおける操作可能な８５０ｎｍＰＤ／ＡＰＤを設計するために、同じ周期で多様な穴直径を使用することが可能であることを示している。例えば８８０ｎｍ波長、９８０ｎｍ波長においての吸収向上を最適化させるために、その他の穴直径及び周期を使用することが可能であり、その場合に、一般的には、波長が一層長くなるに従って穴直径及び／又は周期は対応して一層大きくなる。複数の穴直径及び／又は複数の周期を使用して該マイクロストラクチャ型シリコンＰＤ／ＡＰＤを一層長い波長へ拡張させることが可能であり、例えば、８００から１０００ｎｍの波長で向上される吸収は４０％以上であり、且つ幾つかの場合においては、５０％以上であり、且つ幾つかの場合においては、６０％以上であり、且つ幾つかの場合においては、７０％以上であり、且つ幾つかの場合においては８０％以上であり、且つ或る場合には或る波長において９０％以上である。一層長い波長の場合、例えば１５５０ｎｍでは、該穴及び周期は、例えば、１３００ｎｍ直径及び１５００ｎｍ直径で周期が２３００及び２５００ｎｍとすることが可能であり、その場合には周期が増加している。Ｇｅ・オン・Ｓｉにおける１５５０ｎｍ波長に対するその他の穴直径／周期は、例えば、２３００／３１００（ｎｍ単位）、２０００／３１００（ｎｍ単位）とすることが可能であり、その場合には直径と周期の両方が増加している。

【０２０２】
更に、吸収向上のために山形又は「Ｖ」形状の穴等のその他の形状を使用することも可能である。その他の形状は、「Ｘ」形状、矩形状、三角形状、多角形状、及び／又は所望の吸収向上及びスペクトル幅及び分極感度を達成するための複数の形状の任意の組合せとすることが可能である。

【０２０３】
図１１０は、幾つかの実施例に基づいて、異なる穴直径と格子周期とを有するマイクロストラクチャ型フォトダイオード／アバランシェフォトダイオードに対しての波長に対する吸収のプロットを示している。シミュレーションしたＭＳ－ＰＤ／ＡＰＤは正方形格子を有しておりフォトンは上部表面か又は底部表面のいずれかから入射していた。吸収層はＧｅで約２μｍの厚さである。該構造は図８２Ａに示したものと同様である。該波長に対する吸収の曲線において、例えば曲線１１０１０で表されている周期が２０００ｎｍで穴直径が１５００ｎｍのマイクロストラクチャは、１５００ｎｍから１６５０ｎｍへの波長

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範囲での入射フォトンの良好な吸収特性を示している。該波長に対する吸収の曲線の中で、例えば、曲線１１０１２によって表される周期３０００ｎｍで穴直径２２５０ｎｍのマイクロストラクチャは、例えば、１６５０から１７００ｎｍへの波長範囲で入射フォトンに関して良好な吸収特性を示している。これら２つの穴直径及び格子の組合せは１５００から１７００ｎｍへの波長範囲に対して６０％よりも良い吸収となる場合がある。例えば、５０％よりも良い、幾つかの場合においては４０％よりも良い、及び幾つかの場合においては３０％よりも良い等の良好な吸収特性を達成するために、穴直径／周期のその他の組合せを使用することも可能である。或る波長においては、８０％よりも良いものを達成することが可能であり、例えば、１５５０ｎｍ波長±１０ｎｍ以上である。更に、１６６９ｎｍも８０％吸収効率±波長における数ナノメートルよりも良いものを達成することが可能である。１８７５ｎｍ／２５００ｎｍのその他の穴直径／周期も示されており且つ曲線１１０１４で表されている。

【０２０４】

或る場合においては、穴直径は吸収されるべく該マイクロストラクチャ型ＰＤ／ＡＰＤへ入射する光の波長よりも一層大きいものとすることが可能であり、且つ、幾つかの場合においては、該穴の直径は入射するフォトンの波長とほぼ同じとすることが可能であり、且つ幾つかの場合には、該穴の直径は入射するフォトンの波長よりも小さいものとすることが可能である。同じことが格子の周期についても言うことが出来、その場合に、該周期は検知されるべき光の入射波長よりも一層小さいか、ほぼ同じであるか、及び／又は一層大きいものとすることが可能である。

【０２０５】

図１１１Ａ及び１１１Ｂは、幾つかの実施例に基づいて、図８２Ａに示した構造のＦＤＴＤ方法を使用したシミュレーションを示しており、その場合に、２つの格子及び２つの異なる穴直径を使用している。図１１１Ａは穴パターンを示しており、そこでは１５００ｎｍの穴直径Ｄ１を有する六角形格子が中心において２２５０ｎｍのＤ２と４つの角部においてＤ１とを有する正方形格子とが結合されている。Ｄ１穴は水平方向に３μｍ（ｄ２＝３μｍ）だけ且つ垂直方向に約３．４６μｍだけ離隔されている。該六角形格子は周期が２μｍである（ｄ１＝２μｍ）。図１１１Ｂは波長に対しての吸収のプロットを示している。該２つの格子で２つの異なる穴直径のケース（曲線１１１１０）は、或る幾つかの波長において、吸収が単一格子／穴のマイクロストラクチャ型ＰＤ／ＡＰＤのものよりも一層良好であることを示していることを見ることが可能である。例えば、約１５７０ｎｍ乃至１６００ｎｍ、即ちデータ／遠隔通信波長のＬ帯域、において、曲線１１１１０はかなり一層良好な吸収を示している。このことは、例えば、１５００ｎｍの穴直径での２μｍ周期（曲線１１１１２）と２２５０ｎｍの穴直径での２μｍ周期（曲線１１１１４）とを有する正方形格子と比較される。この結果は、穴直径と周期との異なる組合せで、吸収応答はより少ない共振及び／又はよりシャープでない共振を有することが可能であり且つ又ある波長範囲において吸収応答を最適に調整することが可能であることを示しているだけである。これは単に一つの例であり、所望の量子効率、分極感度、非感受性、波長選択性及び／又は非選択性、例えば、ブロードバンド、リップル／共振減少等を得るために、格子、周期、穴直径及び形状のその他の組合せをシミュレーションすることが可能である。例えば、直径又は最小直径は１００ｎｍから３０００ｎｍの範囲にわたることが可能であり、且つ該周期及び／又は複数の周期は１５０ｎｍから４０００ｎｍの範囲にわたることが可能である。更に、穴パターンは格子ではない場合もあり、例えば複数の穴が非周期的に分布されたり、及び／又は複数の穴の間の間隔がチャープされる場合がある。更に、穴のパターンは周期的である必要が無い場合があるが、該パターンは周期的であるか又は非周期的とすることが可能である。複数の穴をランダムに又は擬似ランダムに分布させることが可能であり、且つ穴直径は周期的、非周期的な態様、ランダムな態様、又は擬似ランダムな態様で変化することが可能である。更に、例えば、周期が同じか、殆ど同じか、或る周期において穴の直径未満である場合には、複数の穴は少なくとも一点で接続させることが可能である。穴のアレイは複数の周期を有することが可能であり、且つ少なくとも

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一つの周期は穴が接触するか及び／又はオーバーラップするようにすることが可能である。

【０２０６】

本書に記載する技術に従って共振セルを隣接する隣の共振セルとの結合を使用して、吸収応答の平滑化が達成され、そのことは単一の共振器を有するのみであり且つその波長に対する吸収においてシャープな共振動作を示す既存の共振フォトダイオードと対比される。本書に記載する技術に基づく共振セルの集団は、制御されたリップルと波長範囲とを有する一層調節された吸収応答となる。更に、本書に記載する技術は、特定の波長において一層最適なＰＤ／ＡＰＤ性能のために特定の波長において特定の吸収特性を調節するために使用することが可能である。

【０２０７】

更に、吸収向上プロセスに参画することの無いその他のマイクロストラクチャ／ナノストラクチャを使用して反射を減少させることが可能であり、例えば、数十ｎｍ乃至数百ｎｍの範囲の寸法（直径等）の表面上のサブ波長の穴又はピット等であり、その場合に、その深さは数十ｎｍ乃至数百ｎｍ又はそれ以上の範囲とすることが可能である。

【０２０８】

図１１２は、幾つかの実施例に基づいて、同じ周期の２つの六角形格子が結合され且つ互いにインターレースされている別の格子構造を示している概略図である。該パターンは同一又は異なる直径の穴を使用することが可能である。図示した如く、該パターンは２つの異なる直径を有しており、例えば、その周期は２０００ｎｍとすることが可能であり、且つＤ１は１５００ｎｍとすることが可能であり且つＤ２は７００ｎｍとすることが可能である。周期及び直径のその他の組合せも可能であり、且つ吸収特性、従って入射フォトン波長に対する量子効率、及び光学的データ／通信通信目的に対して吸収特性が許容可能である波長スパンを調節するため、及びその特定の一つ又は複数の光学システムに対するいかなる特定の適用条件を満足させるために使用される。

【０２０９】

２つの六角形格子の点線によって示した如き単位セルは互いにオーバーラップしており、従ってそれらの固有モードも互いにオーバーラップし、そのことは特定の波長範囲においての吸収特性のリップルを更に減少させることが可能であり且つ該吸収特性におけるリップルが減少される波長範囲を拡張させることも可能である。或る波長範囲内においての吸収特性におけるシャープな変化はフォトダイオード／アバランシェフォトダイオードにおいて望ましいものではない。何故ならば、例えば、入ってくる光学信号波長におけるドリフト及び／又は温度に関してのフォトダイオード吸収特性のドリフトは光学から電気への信号変換において著しい変化をもたらす場合があるからである。５％未満の変化が好適であり、且つ幾つかのその他の場合においては、２ｎｍ，４ｎｍ，１０ｎｍ，２０ｎｍ，４０ｎｍ，６０ｎｍ，１００ｎｍ，又は２５０ｎｍの或る波長範囲内において１０％，２０％，３０％，４０％又は５０％未満であることが好適である。

【０２１０】

図１１３は、６個の単位セルを有している六角形格子を示しており、各セルはその自身の固有モードを有しており、その場合にいかなるフィールド伝播／分布はその固有モードの拡張である場合がある。各セルの固有モードは隣接セルの固有モードと結合させることが可能であり、それにより複合結合型スーパーモードが形成され、そのことは、単なる視覚化の目的のためだけであるが、複数の振り子からなる２Ｄアレイのカップリングとして考えることが可能であり、その場合に、各振り子が弱いスプリング（該弱いスプリングは機械的カップリング機構である）を介してその隣接する全ての振り子に接続されているこの大量に結合された２Ｄアレイの振り子の応答即ち運動は非常に複雑であり且つ単一の振り子の単純な振動運動ではない。該カップリングに加えて、第２の入れ子型の六角形格子を図１１２における如くに付加させることが可能である。更に、円形状又は任意の形状で且つ任意の深さのもので且つ任意の直径のものであり該パラメータの内のいずれもが複数の値を有することが可能な穴を該セル内及び／又は隣接するセルの境界に付加させること

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が可能であり、そのことは該セルの固有モード及び隣接するセルの固有モードとのその結合に影響を与えることが可能である。例えば、説明の便宜上、直径Ｘの複数の穴を図示した如くに付加させることが可能であり、その場合にＸは単一又は複数の値を有することが可能であり且つ該穴はＳｉ又はＧｅ表面において及び該吸収層内に部分的に又は完全にエッチングさせることが可能である。このことは、単に該表面上だけで該吸収層を侵入するものではないものとすることも可能である。幾つかの実施例によれば、該穴は該吸収層内に部分的に又は完全にエッチングさせることが可能である。

【０２１１】

複雑な定在波即ちスーパー固有モードとなる該セルのカップリングは、吸収応答（量子効率に比例）がシャープな応答特徴を有している従来既知の構造における如き共振応答などの単一共振器のものと比較して、一層滑らかな吸収対波長応答を与えることが可能である。

【０２１２】

図１１４は、幾つかの実施例に基づいて、穴アレイとテクスチャー表面とを有するＳｉＮＩＰマイクロストラクチャ型フォトダイオードを示している。テクスチャー表面１１４４０は上部表面上及び／又は穴１１４２２自身内とすることが可能である。テクスチャ付けは垂直からずれた角度において行うことが可能であり、その場合に基板をドライエッチングビーム（方向）に関して傾斜した状態で回転させる（又は静止）ことが可能であり、且つテクスチャーは、例えば、側壁上に部分的にさせることが可能である。幾つかの実施例によれば、テクスチャー１１４４０は入射照射の反射を減少させる。何故ならば、光学的通信リンクにおいて、光学的供給源へ反射して戻される光学信号は望ましいものではなく且つデータ通信システムの信号対ノイズの劣化を発生させる場合がある。マスキングを行うか又は行うこと無しに半導体表面上でドライエッチを実施するブラックシリコン等のテクスチャー付けはフォトンをトラップし反射を減少させることが可能なナノ構造体の森を発生させることが可能である。テクスチャリングが無い場合には、反射は１０％未満であり且ついくつかの場合においては５％未満であり且つ幾つかの場合においては２％未満であり、そのことは、例えば、図３９におけるような波長に対する吸収のプロットにおいてみることが可能であり、その場合に、吸収は或る波長において９０－９５％よりも大きい。１＝Ｔ＋Ｒ＋Ａの式から、尚Ｔは透過光であり、Ｒは反射光であり、Ａは吸収光である。Ａ＝９０－９５％の場合には、Ｔ＋Ｒは５－１０％である。従って、Ｒは１０％以下であり、且つ幾つかの場合には、５％以下である。半導体表面にテクスチャを付加すると、反射を或る波長において１％未満に更に減少させることが可能である。更に、光学信号は垂直からずれた或る角度でマイクロストラクチャ型ＰＤ／ＡＰＤ上に入射することが可能であり、且つ光学データ通信チャンネル内へ反射して戻ることを更に減少させることが可能である。

【０２１３】

図１１５は、波長に対してのＳｉ及びＧｅの吸収係数を示したグラフであり、例えば、http://www.silvaco.com/tech_lib_TCAD/simulationstandard/2010/apr_may_jun/a1/a1.html の図６を参照すると良く、それを引用により本書に取り込む。Ｓｉの場合は８５０ｎｍにおいて且つＧｅの場合には１５５０ｎｍにおいて、両者は約３００／ｃｍ未満の吸収係数を有している。この弱い吸収は、例えば１０Ｇｂ／ｓ帯域幅を超えるデータレートに対して典型的に約２μｍの吸収厚さを有している高速フォトダイオード及び／又はアバランシェフォトダイオードに対して不良な量子効率とさせる。このことは、例えば、Ｓｉの場合は８５０ｎｍの波長でＧｅの場合は１５５０ｎｍの波長に対して、例えば５Ｇｂ／ｓのデータレートを越える高速のフォトダイオードが現在市販されていない理由の一つである。

【０２１４】

図１１６は、幾つかの実施例に基づいて、マイクロストラクチャ型穴アレイに起因するＧｅの向上された実効吸収係数を示しているグラフである。曲線１１６１０は、Ｇｅの２μｍ厚さの層に対して１．２５μｍの穴直径で１．６５μｍの周期を有する六角形格子で

のＧｅに対する向上された吸収係数を示している。比較のために、曲線１１６１２はバルクＧｅ（マイクロストラクチャ型穴無し）の吸収係数を示している。幾つかの実施例によれば、その他のマイクロストラクチャも或る波長帯域に対して最適化させることが可能な向上された実効吸収係数を与えることが可能である。例えば、該マイクロストラクチャは穴又は柱体とすることが可能であり、その間隔は周期的又は非周期的とすることが可能であり、該穴又は柱体は単一又は複数の直径を有することが可能であり、且つその形状は円形状又は非円形状とすることが可能である。先に示した如く、吸収は吸収係数と吸収長との積である。従って、吸収係数をバルク物質の吸収係数（Ｇｅの場合は曲線１１６１２）として維持しながら、吸収長を向上された実効吸収長とさせることが可能であり、即ち、物理的吸収長よりも５，１０，２０又はそれ以上一層長いものとさせることが可能である。図１１６から理解される如く、向上された実効吸収係数は、多くの波長範囲において、Ｇｅにおけるバルク吸収係数よりも１０倍を越えて一層大きい。マイクロストラクチャに起因するＧｅにおける向上された実効吸収係数は、３０％より大きな、４０％より大きな、５０％より大きな、６０％より大きな、７０％より大きな、８０％より大きな、９０％超より大きな量子効率（吸収に直接比例する）で、典型的に、１５５０ｎｍ波長及び一層長い波長においての吸収長が約２μｍ以下である場合には、高速ＰＤ／ＡＰＤの開発を可能とさせる。この様な物質、吸収長、波長、データレート、及び量子効率の組合せはＳｉでもＧｅでも市販されていることが既知ではない。同じことは、例えば、５，１０，２０Ｇｂ／ｓ及びそれより一層早いデータレートに対して吸収長が典型的に約２μｍ以下である場合の高データレート帯域幅において且つ８０５ｎｍ及びそれより長い波長範囲においての動作のためのＳｉマイクロストラクチャ型ＰＤ／ＡＰＤについても言うことが可能である。

【０２１５】

更に、マイクロストラクチャは単一の要素又はセル及び／又は複数の要素又はセルから構成することが可能であり、且つ線形光学フィールド効果、非線形光学フィールド効果、結合モード効果、及び／又は遅波効果の結果である場合がある向上された実効吸収及び／又は向上された実効吸収長を有することが可能である。

【０２１６】

マイクロストラクチャを使用する吸収係数及び／又は吸収長の向上は、吸収係数が一層弱くなる帯域縁部においてＩＩＩ－Ｖ物質、ＧａＡｓ，ＩｎＰ，ＧａＮ等のその他の物質の動作波長を拡張させるために使用することも可能である。例えば、Slawomir S. Piatek, http://www.hamamatsu.com/us/en/community/optical_sensors/tutorials/phsics_of_mppc/indexx.html?utm_source=googleplus&utm_medium=social&utm_campaign=hc-socialにおける図３を参照すると良く、それは１．６μｍ波長の近傍におけるＩｎＧａＡｓに対するものであり、又それを引用により本書に取りこむ。幾つかの実施例によれば、マイクロストラクチャは１．６μｍ近く及びそれより長い動作波長を拡張させるために使用することが可能である。

【０２１７】

更に、吸収の向上のためのマイクロストラクチャの使用は、例えば非晶質Ｓｉ等の非晶質物質へ適用することも可能であり且つ又ポリマー、セラミックス，グラフェン、合金及び酸化物等のその他の物質へ適用することも可能である。更に、音響、マイクロ波、ＵＶ，Ｘ線、及び圧力波等のその他のエネルギー伝播形式を一つの形式のエネルギーから別の形式へ変換させることが可能である。例えば，ピエゾ電気セラミック及び／又は結晶上の略音響波長程度の寸法の構造は、例えば、音響エネルギーから電気的エネルギーへの変換を向上させることが可能である。略音響波長の寸法の構造を使用することは音響吸収を向上させることが可能であり、そのことは、例えば，一層薄いピエゾ電気物質とさせることが可能であり、更にそのことは、例えば，一層高い音響周波数応答を有することを可能とさせる。

【０２１８】

図１１７は、幾つかの実施例に基づいて、Ｓｉマイクロストラクチャ型ＰＤ／ＡＰＤの

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向上された吸収を示しているグラフである。シミュレーションしたＭＳ－ＰＤ／ＡＰＤは六角形格子穴アレイと、２０００ｎｍの周期と、１５００ｎｍの直径と、垂直から、例えば、１０，２０，４０度ずれて入射するフォトンとを有している。図３９は、フォトンが表面に対して垂直に入射する場合の同様の構造に対しての波長に対する向上された吸収のシミュレーションを示している。理解されるように、垂直から１０度ずれてたフォトンは８５０ｎｍの波長においての吸収を著しく変化させるものではなく、該吸収は未だに９０％よりも一層大きい。４０度において，８５０ｎｍにおける吸収は未だに９０％を越えているが、２０度において、吸収は８５０ｎｍにおいて８５％へ減少するようである。全体的に、或る波長においては、マイクロストラクチャに入射するフォトンの入射角度における変化は、例えば，０－４０度の角度範囲にわたって１０％未満の吸収変化を有することが可能である。或る波長範囲において穴直径、周期、非周期的マイクロストラクチャ，を最適化すると、入射フォトンの入射角度に関しての量子効率（吸収に直接比例する）における変化は１０％未満とさせることが可能であり、且つ或る場合には、５％未満、且つ或る場合には、３％未満とさせることが可能である。この特徴はレーザー供給源へ向かって戻される反射光を最小とさせるために重要であり、該レーザー供給源は、オプチカルファイバー及び／又は自由空間及び／又は光学導波路における送信のために電気信号を光学信号へ変換させるために光学変調器が使用される場合に該光学信号を送信するためのデータレートにおいて直接的に又は間接的に変調される。電気信号から光学信号への変換器として発光ダイオード等のレーザーではない供給源を使用することは、該光学供給源へ向かって戻される反射パワーの条件を低下させることとなる。何故ならば、ＬＥＤはコヒーレント性がより低く及び／又はインコヒーレントな光学供給源だからであり、且つ同じ波長における反射は電気信号から光学信号への変換器として完全性においての崩壊の発生はより少ない。

【０２１９】

本特許出願は装置の性質及び動作を説明する上で或る理論に言及しているが，これらの理論は現在の理解に基づくものであって、たとえ将来の進展によりその理論が正しくないものであると証明されたとしても、ここに開示されている装置の実際の動作に影響を与えるものではないことは明らかである。本特許明細書は、又，パラメータの数値範囲に言及しており，この様な範囲からの実質的ではない逸れはここに開示された進歩の精神内のものであることを理解すべきである。

【０２２０】

装置を図示している図面は縮尺通りのものではなく幾分理想化されており、例えば直線は実った角部等であり、一方、実際の装置はそれほど直線的ではないか又は滑らかなものではない壁や幾分丸められている角部を有している場合があり且つ蓋然性があることを理解すべきである。実際に、処理パラメータに依存して、マイクロストラクチャにおける穴又は柱体の壁などの壁は不均一で且つ窪みやへこみ等の表面特徴を具備している粗い表面を有している蓋然性があり，そのことは実際に不所望な反射の減少等の効果を奏することに寄与する場合がある。

【０２２１】

光の検知及び／又は信号処理及びディストリビューション集積回路用の半導体層は，気相エピタキシー、化学蒸着、プラズマエンハンスト化学蒸着、原子層付着、分子ビームエピタキシーなど，及び／又は、例えば、選択的区域エピタキシー、選択的区域エピタキシャルラテラルオーバーエッチ、エピタキシャルラテラル過剰成長、ヘテロエピタキシー，ウエハーボンディング、エピタキシャルリフトオフプロセス、及び成長、ボンディング，リフトオフプロセスの任意の組合せ等の技術を使用してエピタキシャル的に成長させることが可能である。該半導体層に対する好適なプロセスは気相エピタキシー又は化学蒸着である。

【０２２２】

更に、該マイクロストラクチャ穴は吸収用の高電界「Ｉ」領域においてのみとすることが可能であり且つ必ずしも該ＰＤ／ＡＰＤのＮ及びＰ領域内へ及び／又はそれを貫通して

延在するものではない。該穴はその全長にわたってオーバーラップすることが可能であり及び／又は隣接する穴は該穴の長さに沿って部分的にオーバーラップすることが可能である。

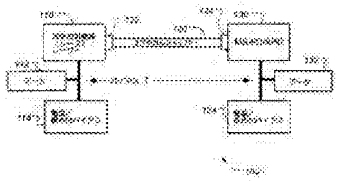
【０２２３】

Ｐ，Ｉ及びＮ領域のドーピングは、しばしば，エピタキシャル成長期間中のドーパントの拡散に一部起因して異なるドーピングレベル領域の間で漸次的な遷移を有している。高ドーピングから低ドーピングへの遷移は、ドーパントタイプ、ドーピングレベル、成長温度及びエピタキシャル付着方法に依存して、１乃至１０００ｎｍ又はそれ以上の距離にわたって発生する場合がある。ＰＩＮ構造は、しばしば、Ｐ＋ＰＰ－ＩＮ－ＮＮ＋であり、その場合に、Ｐ及びＰ－及びＮ及びＮ－は遷移領域であり且つ非常に狭い遷移領域が望ましい。

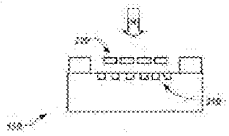
【０２２４】

以上明確性の目的のために幾らか詳細に説明したが、その原理から逸脱すること無しに或る変更及び修正を行うことが可能であることは明らかである。注意すべきことであるが、本書に記載したプロセス及び装置の両方を実施する場合に多くの代替的方法がある。従って、本実施例は例示的なものであって制限的なものではないとして考えるべきであり、且つ本書に記載した業績の内容は本書に記載されている詳細に制限されるべきものではなく、特許請求の範囲及びその均等物内において修正することが可能なものである。

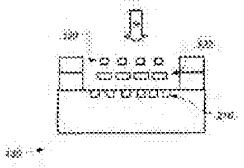
【図１】



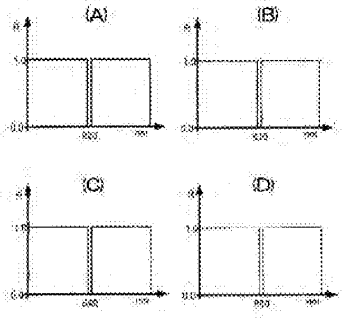
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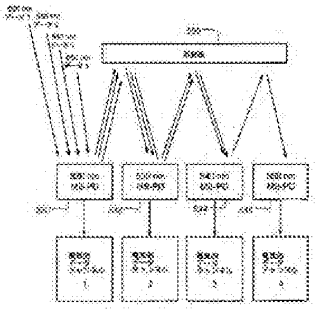
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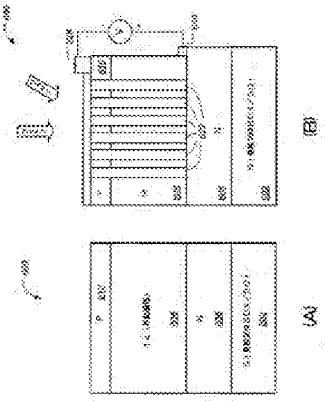
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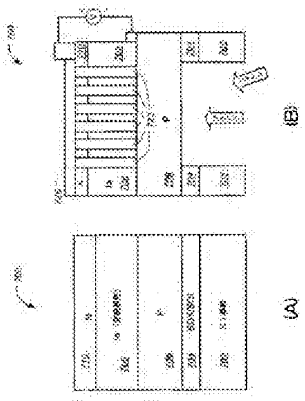
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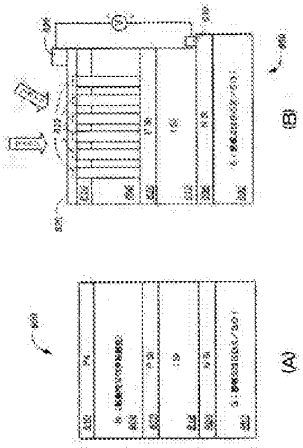
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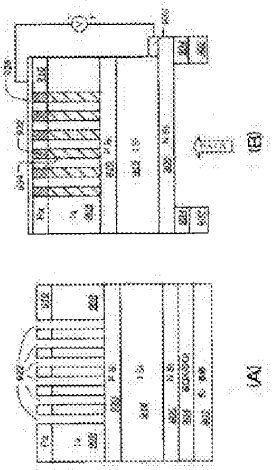
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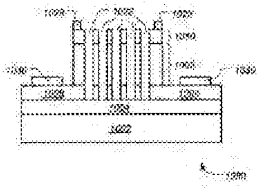
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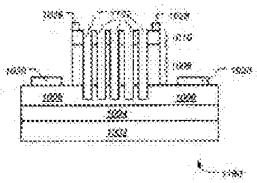
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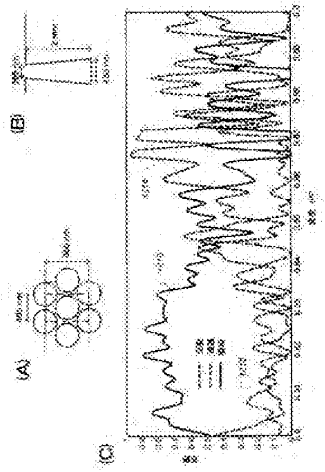
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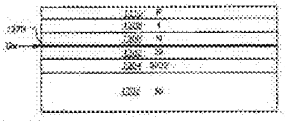
【図１１】



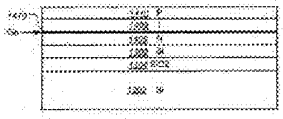
【図１２】



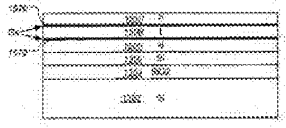
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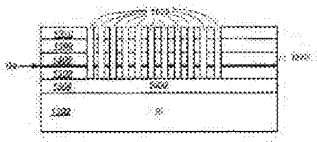
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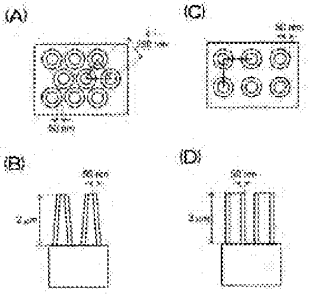
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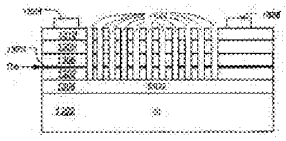
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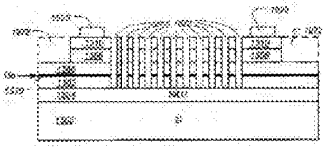
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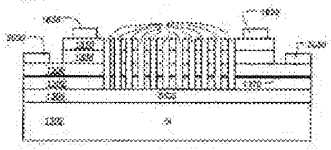
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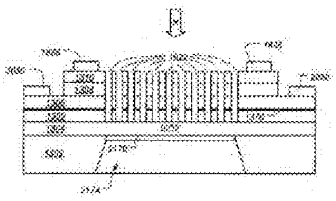
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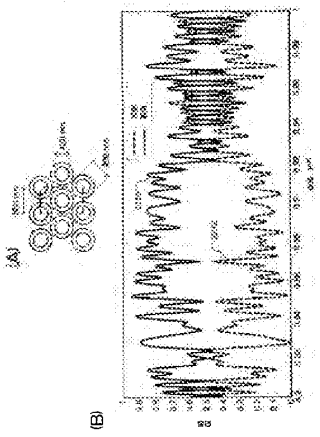
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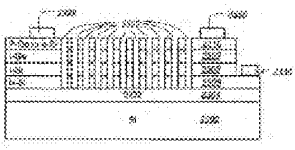
【図２１】



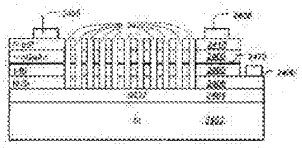
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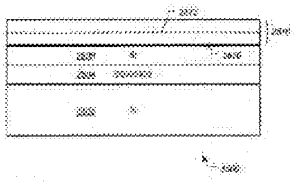
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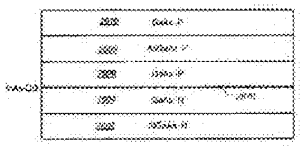
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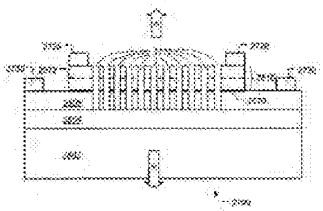
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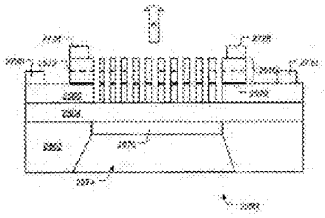
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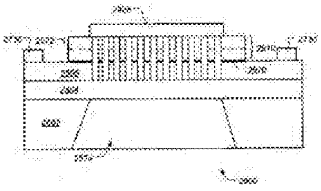
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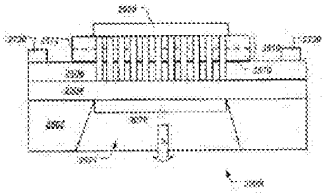
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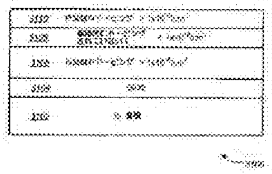
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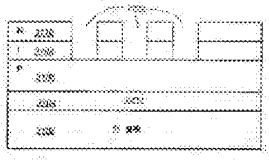
【図３０】



【図３１】



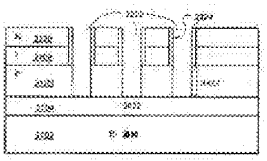
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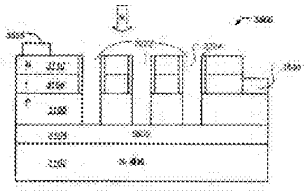
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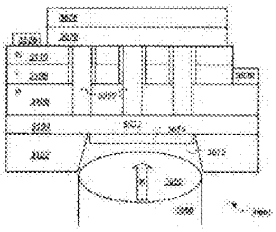
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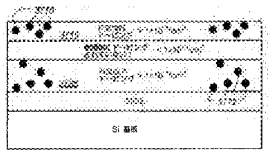
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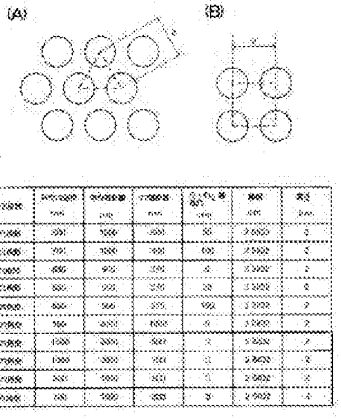
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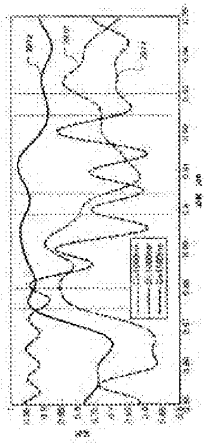
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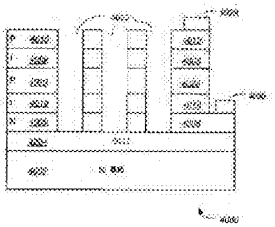
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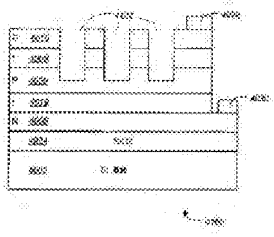
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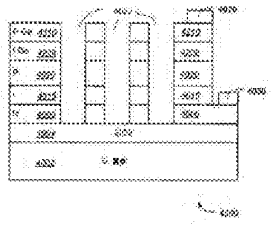
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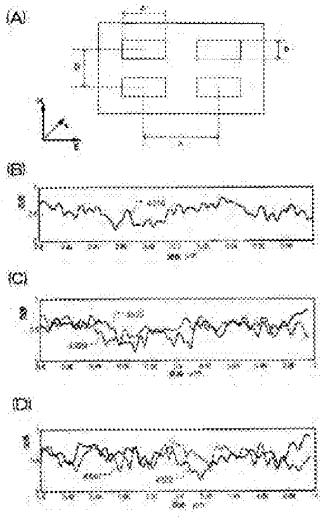
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【図４２】



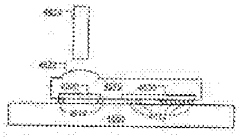
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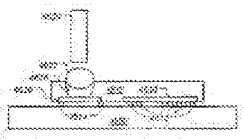
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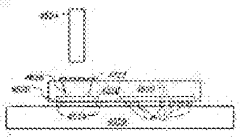
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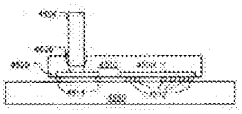
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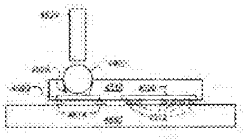
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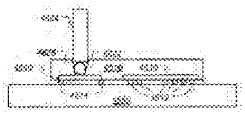
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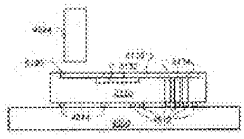
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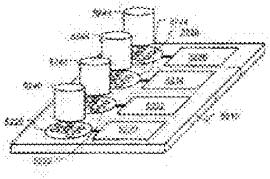
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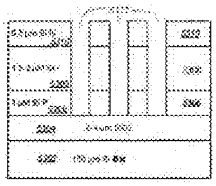
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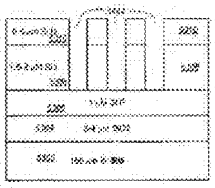
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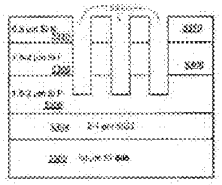
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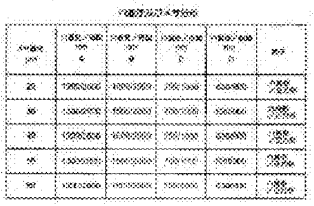
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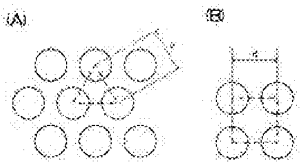
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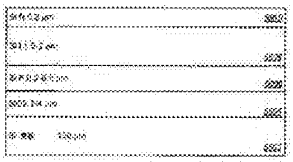
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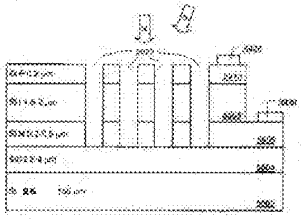
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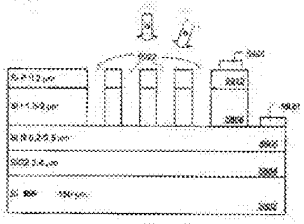
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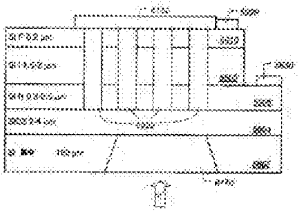
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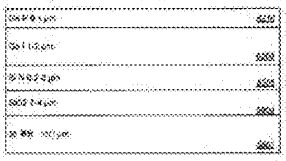
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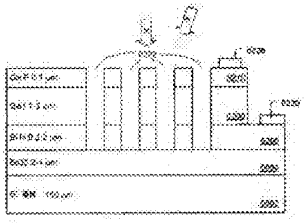
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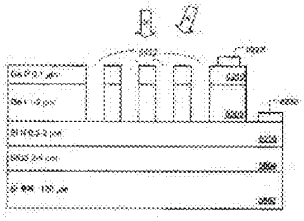
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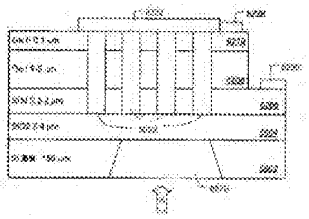
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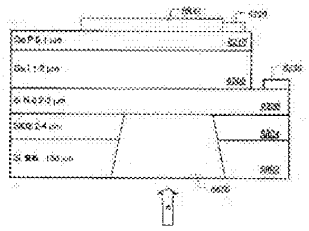
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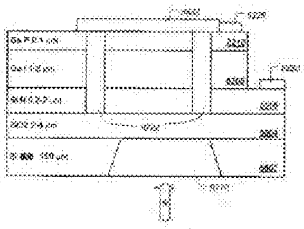
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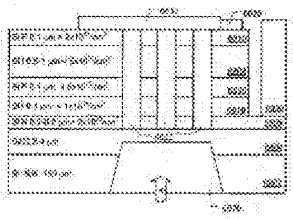
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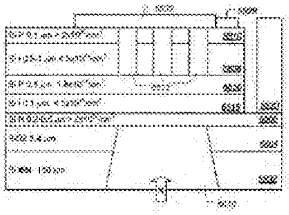
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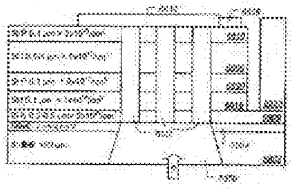
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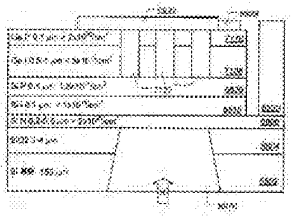
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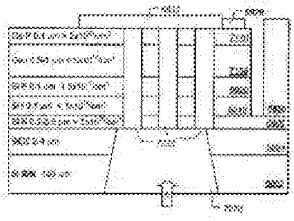
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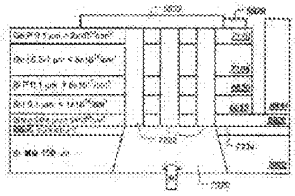
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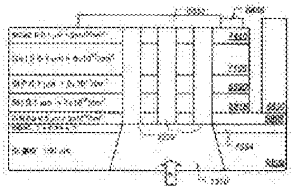
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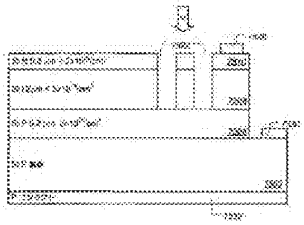
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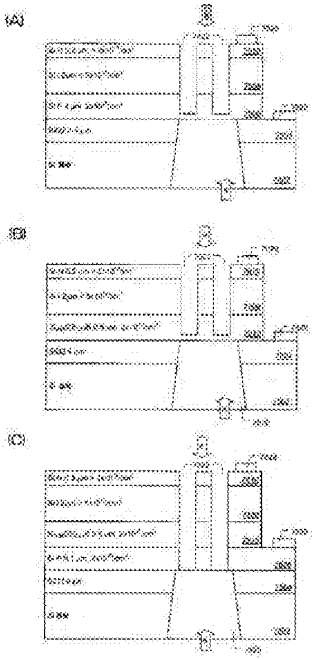
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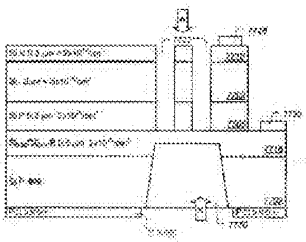
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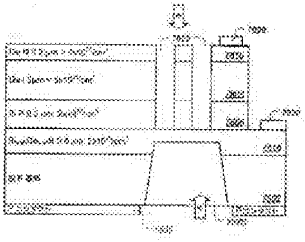
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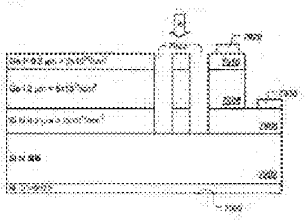
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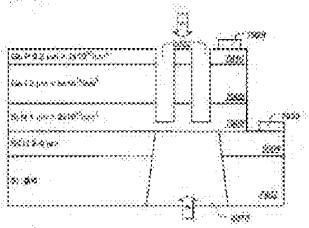
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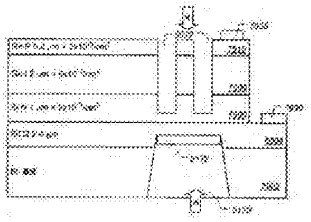
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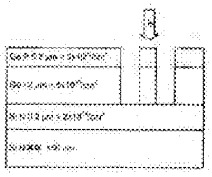
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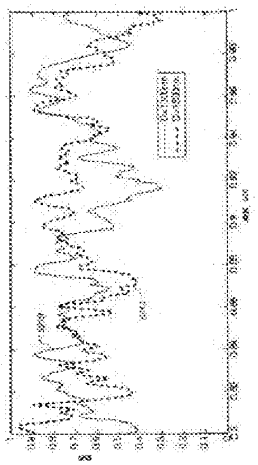
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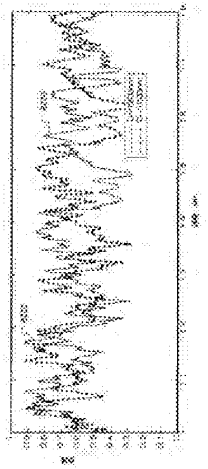
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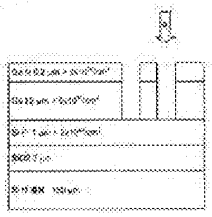
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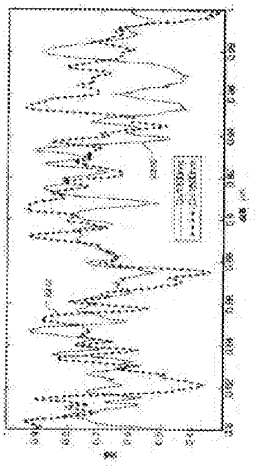
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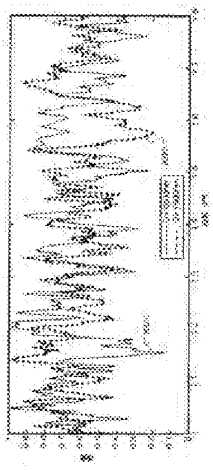
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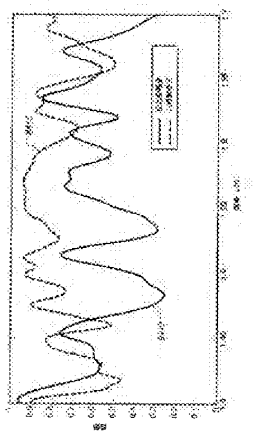
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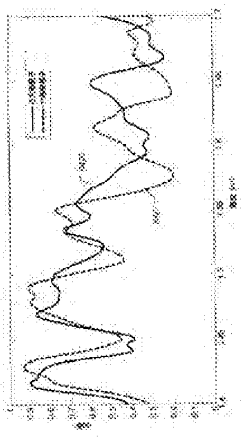
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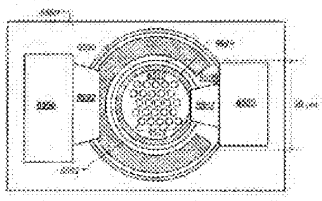
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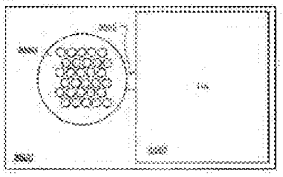
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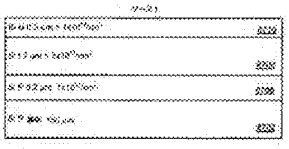
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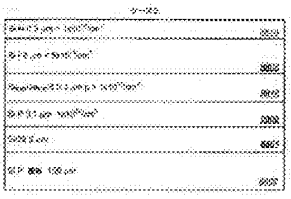
【図８６】



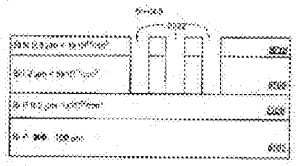
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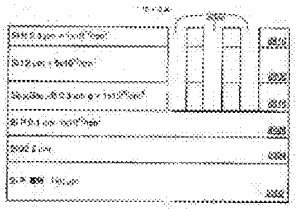
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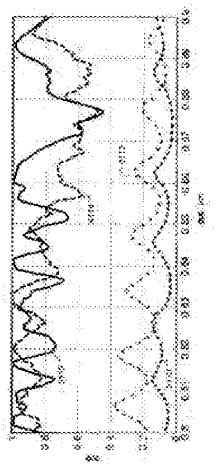
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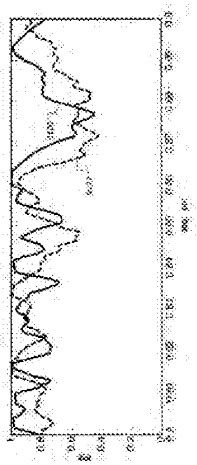
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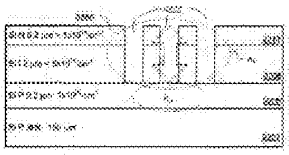
【図９１Ａ】



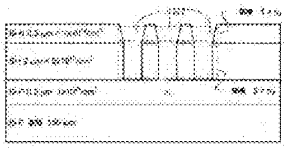
【図９１Ｂ】



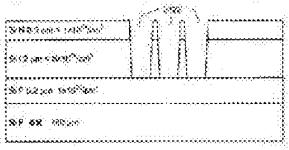
【図９２】



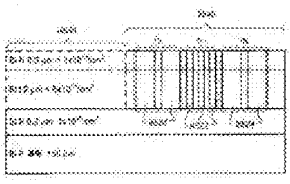
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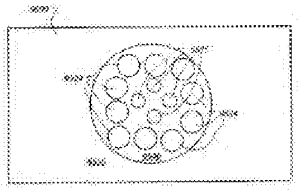
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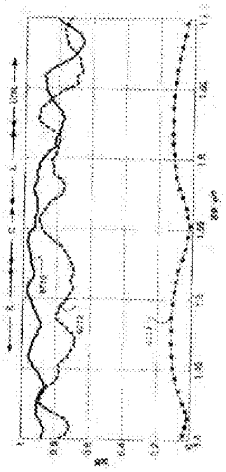
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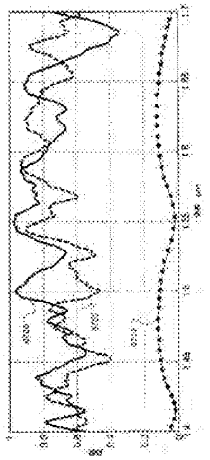
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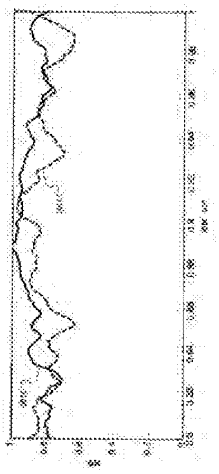
【図９７Ａ】



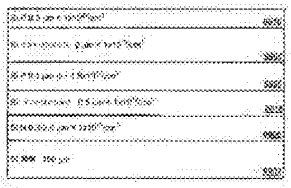
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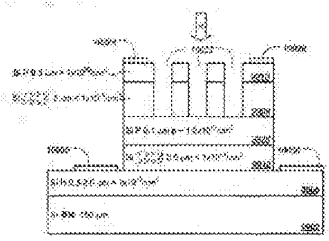
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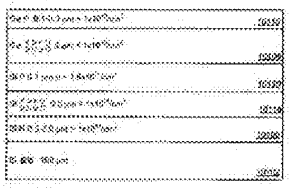
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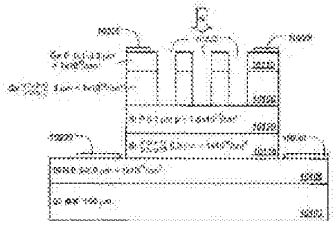
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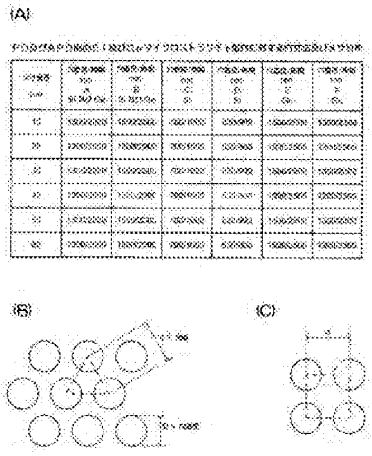
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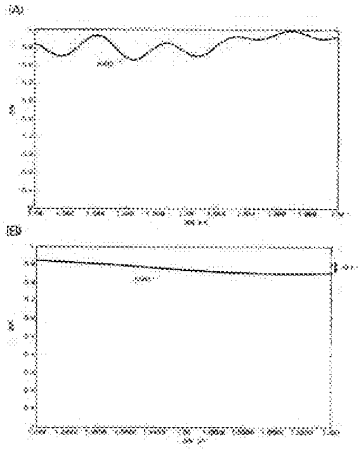
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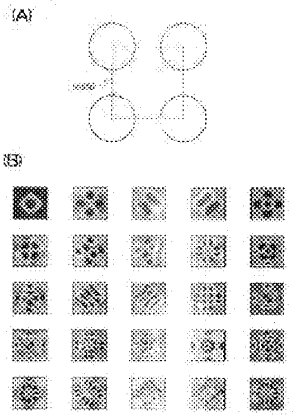
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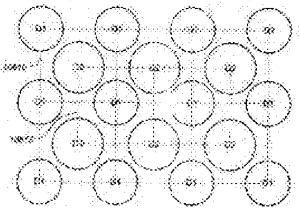
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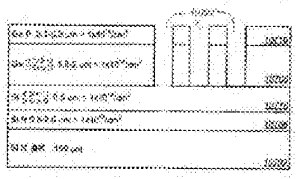
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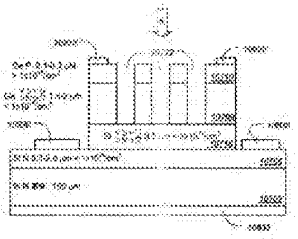
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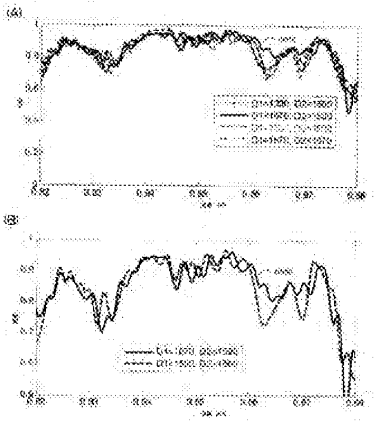
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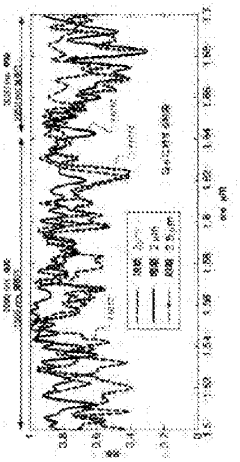
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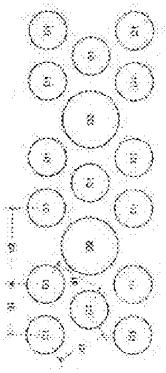
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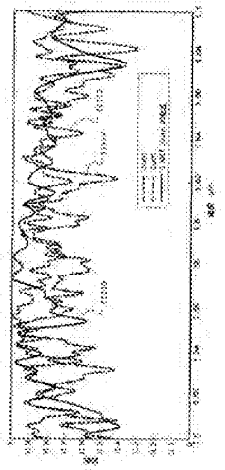
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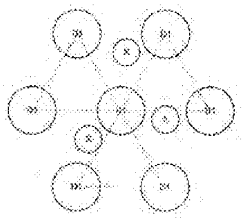
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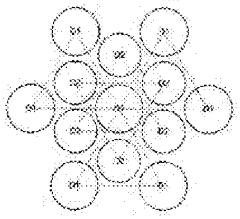
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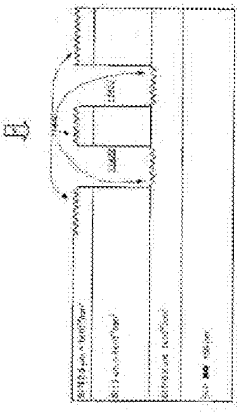
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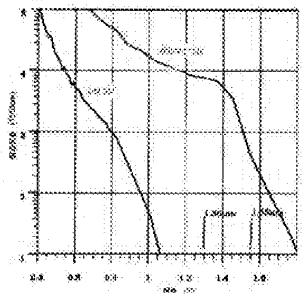
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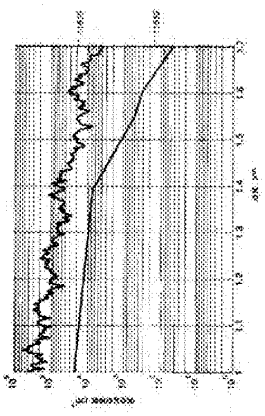
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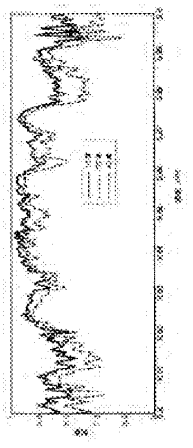
【図１１５】



【図１１６】



【図１１７】



【国際調査報告】

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 15/61120

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 27/148 (2016.01)
CPC - H01L 27/14843; H01L 27/14665; H01L 27/148; H01L 27/15; B82Y 20/00
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8): H01L 27/146 (2016.01)
CPC: H01L 27/14843; H01L 27/14665; H01L 27/148; H01L 27/15; B82Y 20/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
IPC(8): H01L 27/146 (2016.01)
CPC: H01L 27/14843; H01L 27/14665; H01L 27/148; H01L 27/15; B82Y 20/00; USPC: 438/48,60,63,69

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Patbase, Google Web, Google Scholar Search terms used: Photon, absorption, photodetector, photodiode, data, communication, signal, hole, recess, aperture, nanoaperture, bias, circuit, voltage, reverse, substrate, semiconductor, array, monolithic, integrated, processor, microprocessor, dsp, efficiency, rate, percentage, nm, nanometer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 7,977,837 B1 (YAP et al.) 12 July 2011 (12.07.2011), col 9, ln 15-33; col 5, ln 43-64; col 8, ln 42-col 9, ln 15; col 9, ln 30-67, *Figures 14-15*	1-16, 19, 22, 24-26, 35-48, 51, 53-56, 58-60
A		17, 18, 20, 21, 23, 49, 50, 52, 57
Y	US 2012/0141122 A1 (CARUSONE et al.) 07 June 2012 (07.06.2012), para [0005], [0052]	1-16, 19, 22, 24-28, 35-48, 51, 58-61
A		17, 18, 20, 21, 23, 49, 50, 52
Y	US 2013/0009265 A1 (DAUTET et al.) 10 January 2013 (10.01.2013), para [0016], [0027], [0029], [0037]-[0038]	14, 15, 46, 47, 53-56, 58-59
A		57
Y	US 7,348,708 B1 (MASINI et al.) 04 March 2008 (04.03.2008), col 5, ln 20-27; col 7, ln 28-37; col 7, ln 54-col 8, ln 6	18, 48, 70-80
Y	US 2014/0225063 A1 (KLEM et al.) 14 August 2014 (14.08.2014), para [0010], [0052]-[0054], [0059], [0060]	1-16, 19, 22, 24-26, 69
A		17, 18, 20, 21, 23
Y	WO 2013/180690 A1 (HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.) 05 December 2013 (05.12.2013), para [0011], [0042], [0044]	13, 65

☒ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 February 2016	11 MAR 2016
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 15/61120

C (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2014/0167107 A1 (YONEDA et al.) 19 June 2014 (19.06.2014) para [0056]	19, 51, 68
Y	JOSHI et al., "25 Gbps 850 nm photodiode for emerging 100 Gb ethernet applications," SPIE Proceedings Vol 8054, 04 May 2011, (04.05.2011). Abstract [online] <URL: http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=1351039>	26, 62-66
Y	DOSUNMU et al., "Germanium on double-SOI photodetectors for 1550 nm operation," Conference: Lasers and Electro-Optics Society, November 2003, (11.2003), pp. 2, 4-5, 8 [online] <URL: https://www.researchgate.net/publication/224745293>	71-73, 77-80
Y	US 2014/0263975 A1 (NAGANO et al.) 18 September 2014 (18.09.2014), para [0015], [0054]	3
Y	US 2006/0186501 A1 (ISHIMURA) 24 August 2006 (24.08.2006), para [0010], [0039]	28, 61
Y	ACKERT, "10 Gbps silicon waveguide-integrated infrared avalanche photodiode," Optics Express, 12 August 2013, (12.08.2013), Abstract, pp 19535 [online] <URL:https://www.osapublishing.org/view_article.cfm?gotourl=http%3A%2F%2Fwww%2Eosapublishing%2Eorg%2FDirectPDFAccess%2FDDC4EF6B-A4CA-6FBD-9BAB857C67E791AC_260182%2Foe-21-17-19530%2Epdf%3Fda%3D1%26id%3D260182%26seq%3D0%26mobile%3Dno&org=>	26, 62
A	US 4,292,512 A (MILLER et al.) 29 September 1981 (29.09.1981), col 4, in 12-35	17, 18, 49, 50

Form PCT/ISA/210 (continuation of second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 15/61128

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:
This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I: claims 1-26 and 35-80: drawn to an integrated detector/processor circuit for data communication and photodetector with microstructure-enhanced photoabsorption.

Group II: claims 27-34: drawn to an optical/electronic system.

The inventions listed as Groups I and II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

--please see continuation on extra page--

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
1-26, 35-80

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

Form PCT/ISA/210 (continuation of first sheet (2)) (January 2015)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 15/61120

Continuation of Box No. III – Observations where unity of invention is lacking

Special technical features:
Group I requires a photon absorbing region comprising a plurality of holes, not found in the other groups.

Group II requires a laser modulated at Gb/s rates of data to thereby generate the optical source signal carrying information at Gb/s rates; and an optical fiber associated with the laser to receive the optical source signal, not found in the other groups.

Shared Features:
The only technical features shared by Groups I-II that would otherwise unify the groups are an integrated electronic processor circuit and a photodetector formed on a substrate.

However, these shared technical features do not represent a contribution over prior art, because the shared technical features are disclosed by US 2003/0059620 A1 to Yo-Chin 27 March 2003 (27.03.2003), which discloses an integrated electronic processor circuit and a photodetector formed on a substrate (para [0029], [0073] -The integrated circuit detection system can include at least one photodetector. Photodetectors can be selected from photodiodes, avalanche photodiodes, phototransistors, photomultipliers, CCDs, CIDs and hybrid photomultipliers. -Since the anode of the diode is the p-type substrate material, which is common to every circuit on the IC chip, only the cathode is available for monitoring the photocurrent and the photodiode is constrained to operate with a reverse bias.).

As the shared technical features were known in the art at the time of the invention, they cannot be considered special technical features that would otherwise unify the groups.

Groups I and II therefore lack unity under PCT Rule 13 because they do not share a same or corresponding special technical feature.

Form PCT/ISA/210 (extra sheet) (January 2015)

フロントページの続き

(51)Int.Cl.			F I			テーマコード（参考）
G01J	3/36	(2006.01)	G01J	3/36		
H01L	27/144	(2006.01)	H01L	27/144	Z	

(31)優先権主張番号 62/205,717
(32)優先日 平成27年8月15日(2015.8.15)
(33)優先権主張国 米国(US)
(31)優先権主張番号 62/081,538
(32)優先日 平成26年11月18日(2014.11.18)
(33)優先権主張国 米国(US)
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APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
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Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68240468	FILING DATE	09/03/2024
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 6

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV_IDSTransmittal-Final.pdf	1	Transmittal Letter	89 KB
JPA02502326.pdf	13	Foreign Reference	715 KB
JapaneseOfficeActionWithTranslation2020-131831.pdf	21	Non Patent Literature	446 KB
JPA2018508970-.pdf	141	Foreign Reference	17822 KB
309-0015USCIPDIV_1449-Final.pdf	4	Information Disclosure Statement (IDS) Form (SB08)	1010 KB
WO1989005043A1.pdf	20	Foreign Reference	942 KB

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309-0015USCIPDIV_IDSTransmittal-Final.pdf	9DF1BB0D2B4CDAFA4F021BF3603E2A41ADCF7584EC8660811A48D1EDDA47C39C900EEBEB23285F4F77A0991147AA893E97E341DAD9C5497156F5F9960FAB41CE
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JapaneseOfficeActionWithTranslation2020-131831.pdf	6A1743A978363E673A6CCC1EA8F34B72455D16E25180DA5C40A3B71C70681283413025ED5820C4E7F442FB77AF0A8971B114DA31DFE7D6917FF54A2CA972EA76
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309-0015USCIPDIV_1449-Final.pdf	9433C011DAD2F0A119D1A7E02E79DD1C7533D117C8AB9287402383B043C7ADAA2913033C389E0E8780DEE540FAFE311C1F7AB40187BF9C63A26D14FDE6D9C24E
WO1989005043A1.pdf	3D40088EC454A61274BE224417E066CB0F33BD728AAB609B7BBBEEBA3ACA9844EEC41A5FF0BF89326951FE0AA286AD9538DD039FC5027FD2ECD02EB2B804EF62

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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PTO/SB/08a (02-18)
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	Application Number	18822880
	Filing Date	2024-09-03
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIPDIV

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20190001989		2019-01-17	Wang	
	2	20180102442		2018-04-12	Wang	

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	1	8905043	WO		1989-06-01	Santa Barbara Research Center		☐
	2	2018508970	JP		2018-03-29	W&Wsens Devices Inc.		☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	18822880
	Filing Date	2024-09-03
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
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	3	02502326	JP		1990-07-26	Santa Barbara Research Center		☐

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	1	Japanese Office Action for application number 2020-131831, dated October 7, 2024.	☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	18822880
	Filing Date	2024-09-03
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIPDIV

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2024-12-05
Name/Print	Ivan S. Kavrukov	Registration Number	25,161

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Samsung Exhibit 1090, Page 210 of 786
Samsung v. W&Wsens - IPR2025-00993

Infrared radiation detection device

Abstract

translated from Japanese

(57) [Summary] This bulletin contains application data before electronic filing, so abstract data is not recorded.

Classifications

- H01L31/03046 Inorganic materials including, apart from doping materials or other impurities, only AIIIBV compounds including ternary or quaternary compounds, e.g. GaAlAs, InGaAs, InGaAsP

View 4 more classifications

Landscapes

Engineering & Computer Science

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JPH02502326A

Japan

Find Prior Art Similar

Other languages: Japanese

Inventor: アールグレン、ウィリアム・エム、シュルテ、エリック・エフ

Worldwide applications

1988 DE JP WO EP

Application JP1501415A events

1988-10-28 Application filed by サンタ・バーバラ・リサーチ・センター

1990-07-26 Publication of JPH02502326A

1996-08-28 Application granted

1996-08-28 Publication of JP2528192B2

2011-08-28 Anticipated expiration

Status Expired - Lifetime

Info: Patent citations (10), Cited by (5), Similar documents, Priority and Related Applications

External links: Espacenet, Global Dossier, Discuss

Claims (20)

Hide Dependent

translated from Japanese

[Claims] (1) Readout and signal processing circuits are integrated, and silicon, gallium arsenide or a substrate formed of a material selected from the group consisting of or germanium; Mercury/cadmium/tellurium, mercury/zinc/tellurium, mercury/cadmium/selenium mercury, zinc, selenium, mercury, cadmium, sulfur, mercury, zinc, sulfur, lead - Tin/tellurium, lead/tin/selenium, lead/tin/sulfur, indium/arsenic/anti mon, gallium indium antimony, or gallium antimony arsenic a first half grown on said substrate comprising a material selected from the group consisting of a conductor layer; a second semiconductor layer grown on the first semiconductor layer, the readout in the substrate in response to infrared radiation waves received by the first and second semiconductor layers; infrared radiation waves operable to transmit electrical signals to signal processing circuits Monolithic structure for detection (2) a first passivation provided between the base and the first semiconductor layer; 2. The device of claim 1, further comprising a coating layer. (3) a second passivation layer provided between the first passivation layer and the first semiconductor layer; 3. The device of claim 2, comprising a passivation layer of. (4) The first and second passivation layers form the first semiconductor layer. 4. The apparatus of claim 3, including a plurality of nuclear windows operable to control. (5) The nucleation of the first semiconductor layer occurs only within the nucleation window. equipment. (6) a third semiconductor layer provided on the second semiconductor layer; The conductor layer reduces the surface recombination rate of free charge carriers in the second semiconductor layer. 5. The device of claim 4, wherein the device is operable to reduce (7) The first, second and third semiconductor layers are formed by metallic vapor phase epitaxy. 7. The device of claim 6, wherein the device has a length. (8) A layer of antireflection material provided on the third semiconductor layer. equipment. (9) Mercury/cadmium/tellurium, mercury/zinc/tellurium, mercury/cadmium/se Rhenium, mercury/zinc/selenium, mercury/cadmium/sulfur, mercury/zinc/sulfur From the group consisting of yellow, lead/tin/tellurium, lead/tin/selenium, lead/tin/sulfur first and second layers of semiconductor material formed from selected materials as an infrared radiation source; exposed to generating a photocurrent in the first and second layers of semiconductor material; The first and second semiconductor layers are grown thereon and are made of silicon, gallium arsenide or is installed in a substrate formed from a material selected from the group consisting of germanium. sensing the photocurrent by a readout and signal processing circuit How to detect external radiation. (10) the first semiconductor material layer, the second semiconductor material layer and the base 10. The method of claim 9, wherein comprises a monolithic structure. (11) The layer of the first semiconductor material is arranged on the substrate by a first passivation layer. 10. The method of claim 9, wherein the method is isolated from the body. (12) The first passivation layer is half-layered by a second passivation layer. 12. The method of claim 11, wherein the method is separate from the first layer of conductive material. (13) The first and second passivation layers are layers of the first semiconductor material. 13. The nuclear window of claim 12, comprising a plurality of nuclear windows operable to control the formation of the nuclear window. Method. (14) providing a layer of the third semiconductor material on the layer of the second semiconductor material; The surface recombination rate of free charge carriers in the layer of second semiconductor material by 10. The method of claim 9, including the additional step of reducing . (15) The first, second and third semiconductor layers are formed by metallic vapor phase epitaxy. 15. The method of claim 14, wherein: (16) an additional layer of antireflection material that allows infrared radiation to pass through the layer of antireflection material 10. The method of claim 9, comprising the steps of: (17) A readout and signal processing circuit is integrated, and the readout and signal processing circuit is integrated. a substrate formed of a material selected to optimize the properties of the circuit; a first layer grown on said substrate from a material selected to optimize infrared detection; a semiconductor layer of a plurality of passivations provided between the substrate and the layer of first semiconductor material; layer and in response to infrared radiation received by the first and second semiconductor layers. said first operable to transmit an electrical signal to a readout and signal processing circuit; a second semiconductor layer provided on the semiconductor layer; actuated to reduce the surface recombination rate of free charge carriers in the second semiconductor layer; a third semiconductor layer provided on the second semiconductor layer that can be provided on the third semiconductor layer, with a refractive index between the refractive index of the atmosphere and the third semiconductor layer; a monolithic structure for detecting infrared radiation waves comprising an anti-reflection coating having a array of. (18) The plurality

of passivation layers control the growth of the first semiconductor layer. 18. The array of claim 17, comprising a plurality of nuclear windows operable to. (19) One of the nuclear windows is connected to the first semiconductor layer and the readout and signal 19. The array of claim 18, wherein the array enables electrical coupling to and from processing circuitry. (20) The monolithic structure further includes the first and second semiconductor layers and the Contains ohmic contacts to allow electrical coupling to readout and signal processing circuits. 20. The array of claim 19.

Description

translated from Japanese

[Detailed description of the invention] Infrared radiation detection method and device 1. Field of invention The present invention relates to the field of infrared sensing, and in particular to methods and apparatus for detecting infrared radiation.

2. Description of conventional technology Basic infrared detectors have wavelengths from 1 to 30 μm for survey, target investigation and Often used in exploration and tracking imaging systems that detect the presence of electromagnetic radiation be done. These basic detectors to detect infrared radiation are triglycine Temperature sensation like phated and lanthanum-topped lead zirconate titanate crystals Responsive thermoelectric and ferroelectric materials are often used. Such crystals are momentarily in response to an incident infrared radiation wave that causes a potential drop across the attached electrodes. indicates intermediate electrical polarization. Sulfidation where the resistance of the material changes as a function of the incident radiation Photoconductive materials such as lead and mercury, cadmium, and tellurium may be used.

Finally, the intrinsic band-to-band electron-hole excitation is proportional to the incident infrared flux. mercury, cadmium, tellurium, indium, anti Photovoltaic devices such as those constructed from mono or similar materials may be used.

Arrays of such elementary detectors are used to form thermal imaging systems. Good too. In real-time, A thermal imaging system with rotating rhythmic reflectors spans a one-dimensional array of elementary detectors. used to scan the radiation emitted by the source. basic detector When used in this way, the temporal output of the detector produces a two-dimensional representation of the image. may be used as such. Using either observation or scanning arrays In a two-dimensional detection array imaging system capable of A suitable readout such as a charge-coupled device ("CCD") It may be monitored by an integrated circuit. The output from the CCD is time delayed and can be processed by various techniques such as minute or parallel to serial scan conversion. , frame rate, signal-to-noise ratio, etc., are selected according to system requirements. the Other reading devices may also be used.

Although the above detector structures are efficient, they generally have some manufacturing related It has some drawbacks. First, the detector and readout device are configured separately and then A number of such detector structures that are mechanically coupled are formed in a hybrid manner

Because the formation of hybrid structures involves additional processing steps, such structures Monolithic devices (i e. the detector and readout and signal processing circuitry are in one material) The production efficiency tends to be lower compared to other systems (equipment formed in the system). difference Furthermore, there is a possibility that unintended defects may be induced during formation, reducing reliability and impairing properties. High potential. Monolithic detectors eliminate additional processing steps required for hybridization. avoid topography, but use the same material as the infrared detector for the signal processing circuitry. There is a need. This material (e.g. Hg, Cd, Te or InSb) is It is usually better than circuits formed from well-developed silicon or gallium arsenide. According to a preferred embodiment of the present invention, a low characteristic signal processing circuit detects infrared radiation. A method and apparatus are disclosed. The device has integrated readout and signal processing circuits including the base body. Substrate consists of silicon, gallium arsenide and germanium Formed from materials selected from the group. The first semiconductor layer is made of mercury and carbon. Domium/tellurium, mercury ψ zinc/telluride, mercury φ cadmium, selenium, mercury ・ Zinc/Selenium, Mercury/Cadmium/Sulfur, Mercury/Zinc/Sulfur, Lead/Tin/Te Lulu, lead, tin, selenium, lead, tin, sulfur, indium, arsenic, antimony, gas Glue consisting of lithium indium-antimony or gallium antimony arsenic A material selected from the loop is grown on the substrate. Is that the second semiconductor layer? are formed on the first semiconductor layer.

Brief description of the drawing Various advantages of the invention will become apparent to those skilled in the art from the following description and drawings. .

The drawing is a sectional view of a preferred embodiment of a device for detecting infrared radiation according to the invention. .

Description of the preferred embodiment According to a preferred embodiment of the invention, the structure 10 for detecting infrared radiation is indicated by 4 in the figure. Provided as shown. Structure 10 may be used as a single sensing element Alternatively, it may be part of a multi-element video device. Structure IO is silicon, It includes a substrate 12 which may be formed from gallium arsenide or germanium. but It should be understood that other suitable materials may be used. The base 12 is , by reference numeral 14 which converts the output of the semiconductor layer described below into a usable form. including appropriate readout and signal processing circuitry as shown. Readout and signal processing circuits Route 14 is described by Bluzer, N., herein referred to.

and Stehlac, R. ("Buffered Direct Injection of Photocurrents 1nto Cha rge-CoupledDevice', IEEE Transacti ons on Electron Devices.

ED25. n, 2. p. 160, February 1978) You may do so Any other suitable means of processing the output from the semiconductor layer may be used. You may be

A first passivation layer 16 is provided to control the electrical properties of the substrate surface. ing. The first passivation layer 16 has an optimal passivation shape for the substrate 12. selected from materials that provide a Such materials include 5i02 or SiN. include.

However, it should be understood that other suitable materials may be used. Second A passivation layer 18 is deposited on the first passivation layer 16 . No. The passivation layer 18 of No. 2 is made of a material suitable for the infrared active semiconductor layer described below. Provides an ossivation state and prevents nucleation of the infrared active semiconductor layer.

formed from one of a plurality of materials forming a deep surface. Such materials are 5i02 or or ZnS. However, other suitable materials may be used. should be understood. The first and second passivation layers 16 and 18 are It has an ohmic contact 20 and a plurality of nuclear windows 22-26. ohmic contact The child 20 includes a second semiconductor layer and a readout and signal processing circuit 14, which will be described below. Used to make electrical connections between The nuclear window 22 to 26 is the first half. Used to provide seed locations for the core of the conductor layer. Furthermore, the nuclear window 24 enabling electrical coupling between the first semiconductor layer and the readout and signal processing circuitry 14 .

Structure 10 includes a first semiconductor layer for generating a photocurrent in response to incident infrared radiation. 28 and a second semiconductor layer 30. First and second semiconductor layers 28 and 3 0 both include the base and collector layers of the Peter junction photodiode. first The semiconductor layer 28 is made of water having a stoichiometric relationship defined by Hgx-xCcLTe. It is composed of layers of silver, cadmium, and tellurium. The composition value of X is the first semiconductor layer 2 8 is selected to be sensitive to infrared radiation at a particular wavelength in the infrared spectrum. . For example, if the composition value of X is selected to be approximately 0.2, then the first semiconductor layer 28 has a cutoff of about 10 to 12 m at the desired operating temperature (e.g. 77 degrees absolute). It is sensitive to long-wavelength infrared radiation waves that have long wavelengths.

However, the first semiconductor layer 28 is mercury/zinc/tellurium, mercury/cadmium/ Selenium, mercury/cadmium/sulfur, mercury/zinc/sulfur, mercury/zinc/selenium lead, tin, tellurium, lead, tin, selenium, lead, tin, sulfur, indium, arsenic - Antimony, gallium indium antimony, or gallium antimony it should be understood that other suitable materials may also be included, such as be.

The second semiconductor layer 30 has a stoichiometric relationship defined by Hg, 1-cCd, and Te. Contains layers of mercury, cadmium, and tellurium.

The composition value of y is selected to be larger than the composition value X of the first semiconductor layer 28, and is typically has a value of 0.3. However, any other suitable value of y may be selected or mercury, cadmium, tellurium, mercury, zinc, tellurium, mercury, cadmium, selenium um, mercury, zinc, selenium, mercury, cadmium, sulfur, mercury, zinc, sulfur, Lead/tin/telluridum, lead/tin/selenium, lead/tin/sulfur, indium/arsenic/enium Timon, gallium indium antimony or gallium antimony arsenic it should be understood that other suitable materials may be selected, including.

The first semiconductor layer 28 acts as a photodiode base layer while the second semiconductor layer 28 acts as a photodiode base layer. Body layer 30 acts as a photodiode collector layer. However, structure IO The roles of the first and second semiconductor layers 28 and 30 are reversed to increase the collection efficiency of (i.e., the second semiconductor layer 30 becomes the base layer and the first semiconductor layer 30 layer 28 becomes the collector layer). In this case, the composition value of y is approximately 0.2, and the composition value of The closing price is approximately 0.3. However, generally the second semiconductor layer 30 has a narrow barrier. and the first semiconductor layer 28 is a wide bandgap material. . Layers 28 and 30 are doped to have a mixture of opposite types.

That is, the first semiconductor layer 28 is doped p-type, and the second semiconductor layer 28 is doped n-type. and vice versa. However, the same type of heterojunction has also been used Good things should be understood.

When a photon of light in the infrared spectrum is absorbed by device structure 10, an electric charge is generated. Child hole pairs are generated Before the electron-hole pair recombines, the first and second semiconductor When the junction between the body layers 28 and 30 is reached, the first and second semiconductor layers 2 The electric field at the junction between 8 and 30 moves electrons into the n-type semiconductor layer, The holes are moved into the p-type semiconductor layer. This electron hole movement causes the received photon to Generates a photocurrent proportional to the number.

sensing the photocurrent generated in the first and second semiconductor layers 28 and 30; To this end, substrate 12 further includes heavily doped regions 32 and 34. heavily The looped area 32 is connected to the readout and signal processing circuitry 14 through the nuclear window 24 and the first semiconductor layer 28 . Attached to nuclear window 24 The material to be used has a crystal structure and lattice constant similar to HgTe or the semiconductor layer 28. (i.e., HgSe, Hg S, PbTe.

Pb5e, PbS, and Gray Sn can be selected instead). child This provides good ohmic contact between the heavily doped region 32 and the first semiconductor layer 28. I will provide a. Although the same material is deposited in nuclear windows 22 and 26 at the same time, , it is made with respect to the first semiconductor layer 28 only as a nucleation point and not as an ohmic contact. use Furthermore, the heavily doped region 34 is connected to the metallization layer 3B and the ohmic contact. 20 between the readout and signal processing circuit 14 and the second semiconductor layer 30. Provide a bond. Ohmic contacts 20 and 3B can be two different metals. , and the ohmic contact 20 makes good ohmic contact with the heavily doped region 34. metallization layer 36 is selected such as platinum for n-type and gold for p-type. is selected to form a good ohmic contact with the second semiconductor layer 30. metal The chemical layer 36 is also selected to be a material in which the nuclei of the first semiconductor layer 28 are suppressed. There must be.

If the second semiconductor layer 30 acts as the base of the photodiode, the second half Free charge carriers inside the conductor layer 30 are present at the interface with the second semiconductor layer 28. Drift towards them and recombine. As a result of this recombination, free charge carriers become The efficiency collected by passivation layer 16 is reduced second semiconductor layer In order to reduce the rate of recombination of free charge carriers in the second semiconductor layer 3 A third semiconductor layer 38 is provided when 0 acts as the base of a photodiode. It will be done. The third semiconductor layer 38 has H selected such that the composition value of 2 is larger than y. Mercury and cadmium with the stoichiometric relationship defined by g>-*Cd z T e It may be formed from umQ tellurium. However, mercury, cadmium, tellurium , mercury/zinc/tellurium, mercury/cadmium/selenium, mercury/zinc/selenium mercury, cadmium, sulfur, mercury, zinc, sulfur, lead, tin, tellurium, lead, tin, steel Rhenium, lead, tin, sulfur, indium, arsenic, antimony, gallium Mu antimony or other suitable materials such as gallium antimony arsenic It should be understood that may also be used.

Additionally, structure 10 includes an anti-reflective coating 40. Anti-reflection coating 40 is the third semiconductor layer 38 and is used to reduce reflection of incident infrared radiation. anti The anti-radiation coating 40 is made of a material having a refractive index between the refractive index of the atmosphere and the third semiconductor layer 38. formed from. The anti-reflective coating 40 is made of zinc sulfide, zinc selenide or zinc telluride. It may be formed from lead, or other suitable materials may be used. Structure 10 is Also, the first passivation layer 1B and the first and second semiconductor layers 2B and includes a field plate region 42 used to control the relative potential of 30 . Field plate 42 has first and second semiconductor layers 2B and 30 in a first It is provided under the region intersecting the passivation layer 16. field plate Region 42 may be doped into substrate 12 or deposited with metal on the surface of substrate 12. You may wear it.

Control of the potential in the region where layers 28, 30 and 16 intersect is important for device performance. is important. A first passivation is applied to control the potential in this region. Layer 16 is near a flat band potential in first and second semiconductor layers 28 and 30. In order to optimize the photodiode characteristics in current operation, Any deviation from the flat band condition due to the use of the supply potential as used Provides a stable surface potential by using a compensating field region 42 (i.e., the first passivation layer 1B is selected as (selected to passivate the semiconductor layers 28 and 30).

First and second semiconductor layers 28 and 30 are formed on first passivation layer 16. The growth automatically results in a self-passivating buried bond. centre The presence of the field plate region 42 increases the surface voltage in the junction region by gate voltage control. This allows optimization of position.

By giving the above structure, the properties of structure 1o can be determined by signal processing and infrared detection. can be optimized from both perspectives.

The substrate 12 is made of silicon or arsenide on which a signal processing circuit with optimal characteristics can be formed. It may be gallium or germanium.

the first and second semiconductors 2 selected from materials that optimize infrared detection; 8 and 30 are provided on substrate 12 by heteroepitaxial selective region deposition. It will be done. Therefore, this combination of detector structure and substrate 12 is a monolithic heterogeneous Construct an epitaxial focal plane array and associate the hybridized structure with Not affected by shortcomings.

Structure 10 may be formed in the manner described below.

After substrate 12 is formed with readout and signal processing circuitry 14, it is heavily doped. regions 32 and 34 and field plate region 42 are formed. Or is it? Passivation layers 16 and 18 are provided on substrate 12 . then contact The window is a passivation layer covering the heavily doped region 34 by the photorin graph. drilled into the vation layers 18 and 1B. the first metal layer is heavily doped. The ohmic contacts 20 are provided by vacuum evaporation to form the ohmic contacts 20 to the areas 34. Lifted off. A second photolithographic process is then carried out to form the metallization layer 3B. A rough step is executed. The morphology of the metallization layer 36 forms the boundaries of the structure 10 and 2 is selected to be in ohmic contact with the semiconductor layer 30 of No. 2.

Thereafter, nuclear windows 22-26 are opened in passivation layers 16 and 18. A third photolithographic step is used to increase the thickness. Nuclear window 22~ The configuration, dimensions, and spacing of the 26 will depend on the desired detector geometry and the epitome used. Determined by the characteristics of the taxial

growth process. For example, laterally from the nuclear window If the vertical growth occurs at the same rate as the vertical growth, the window will grow as fast as the vertical growth. They should be widely spaced apart. Too many nuclear windows are To provide spatial constraints for the readout and signal processing circuits 14 in 12, The number of windows should also be minimized. Number of nuclear windows 22 to 26 The number and dimensions are determined by the lateral growth rate relative to the vertical growth rate of the first semiconductor layer 28. It can be minimized by maximizing the speed ratio. Furthermore, the second The ratio of the lateral growth rate to the vertical growth rate of the semiconductor layer 30 is also the first and a maximum between the junction between the second semiconductor layers 2g and 3C and the metallization layer 36. should be maximized to give the possible distance of The thickness of the first semiconductor layer 28 is By forming a thinner layer, the number of required nuclear windows 22 to 26 is reduced. be done. By forming the second semiconductor layer 30 even thicker, the metallization layer 36 and The distance between the junction between the first and second semiconductor layers 28 and 30 is greater. This gives more tolerance to variations in lateral growth rate. Ru.

After opening the nuclear windows 22 to 26 in the passivation layers 28 and 30, the remaining The remaining photoresist is removed from passivation layer 16 and substrate 12 is removed from its surface. located in a low temperature metallic vapor phase epitaxial reactor such that in-situ cleaning of surfaces is performed. it will be done. On-site surface cleaning can be done by ultraviolet ozone etching, atomic hydrogen etching or ultraviolet. radiation or other free radicals generated from appropriate reactants in the plasma field. including etching.

The nucleation crystals are located within the nucleation windows 22 to 26 of the passivation layers 16 and 18. grow up. The material from which the passivation layer 18 and the metallization layer 36 are formed is nucleated. To prevent crystal formation, nucleation occurs only in the nucleation windows 22-26. Money The flow of reactants into the gas phase epitaxial reactor is carried out through nuclear windows 22 to 2. The first semiconductor layer 28 is changed to grow a first semiconductor layer 28 that nucleates on the nucleated crystals in 6.

The reactant flow is further varied to grow the second semiconductor layer 30 reaction The final change in the material flow causes the third semiconductor layer 38 to grow. Ru. Finally, a third antireflection layer 40 is applied by vacuum deposition outside the metallic vapor phase reactor. is formed on the semiconductor layer 38 of.

Therefore, the present invention provides that the infrared material is selected to optimize infrared detection, - Infrared signal processing materials can be selected to optimize the power signal processing circuit. It will be appreciated that an apparatus can be provided for detecting radiation. that Therefore, the invention is not limited to the particular embodiments shown. example For example, another suitable region-selective epitaxial growth technique may be used to form the first semiconductor layer. It may also be used for the relative doping of the first and second semiconductor layers; The function they perform (ie base or collector) may also be varied. the Other modifications may occur upon consideration of the specification, drawings, and following claims. This will be made clear to the dealer.

International search report 1""- ^"–"–i'@'PCT/US If/n'17Q5 International Search Report SA 26299

Patent Citations (10)

Publication number	Priority date	Publication date	Assignee	Title
Family To Family Citations				
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US4053919A *	1976-08-18	1977-10-11	The United States Of America As Represented By The Secretary Of The Air Force	High speed infrared detector
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Family To Family Citations				

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* Cited by examiner, † Cited by third party, ‡ Family to family citation

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Priority And Related Applications

Applications Claiming Priority (2)

Application	Filing date	Title
US123842B7A	1987-11-23	
US123,842	1987-11-23	

Concepts

machine-extracted

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Name				Image	Sections	Count	Query match
radiation	title,claims,description	23	0.000				
detection method	title,claims,description	6	0.000				
semiconductor	claims,description	103	0.000				
material	claims,description	50	0.000				
mercury	claims,description	40	0.000				
mercury	claims,description	39	0.000				
passivation	claims,description	31	0.000				
cadmium	claims,description	23	0.000				
tellurium	claims,description	23	0.000				
substrate	claims,description	22	0.000				
cadmium atom	claims,description	21	0.000				
tellurium atom	claims,description	21	0.000				
Sulfur	claims,description	18	0.000				
Zinc	claims,description	18	0.000				
sulfur	claims,description	18	0.000				
sulfur	claims,description	18	0.000				
tin	claims,description	18	0.000				
zinc	claims,description	18	0.000				
zinc	claims,description	18	0.000				
Selenium	claims,description	16	0.000				
selenium	claims,description	16	0.000				
selenium	claims,description	16	0.000				
lead	claims,description	15	0.000				
method	claims,description	15	0.000				
Gallium	claims,description	10	0.000				
gallium	claims,description	10	0.000				
nucleation	claims,description	8	0.000				
nucleation	claims,description	6	0.000				
charge carrier	claims,description	6	0.000				
indium	claims,description	6	0.000				
indium atom	claims,description	6	0.000				
silicon	claims,description	6	0.000				
silicon	claims,description	6	0.000				
AsGa	claims,description	5	0.000				
Gallium arsenide	claims,description	5	0.000				
antimony arsenic	claims,description	5	0.000				
antimony atom	claims,description	5	0.000				
conductor	claims,description	5	0.000				
germanium	claims,description	5	0.000				

germanium atom	claims,description	5	0.000
recombination	claims,description	5	0.000
recombination	claims,description	5	0.000
arsenic	claims,description	4	0.000
biosynthetic process	claims,description	4	0.000
indium antimonide	claims,description	4	0.000
response	claims,description	4	0.000
coating agent	claims,description	3	0.000
coating method	claims,description	3	0.000
coupling	claims,description	3	0.000
coupling process	claims,description	3	0.000
coupling reaction	claims,description	3	0.000
rhenium	claims,description	2	0.000
rhenium atom	claims,description	2	0.000
layer	claims	53	0.000
vapour-phase epitaxy	claims	2	0.000
coating layer	claims	1	0.000

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⑲日本国特許庁（JP）　　⑪特許出願公表

⑫公表特許公報（A）　　平2－502326

⑬公表　平成2年(1990)7月26日

⑤1Int. Cl.⁵	識別記号	庁内整理番号		審査請求 未請求
H 01 L 27/14 31/10				予備審査請求 未請求　部門（区分） 7（2）
		7377－5F	H 01 L 27/14	
		7733－5F	31/10	Z　（全 6 頁）

⑤4発明の名称　赤外線放射検出方法および装置

⑳特　願　平1－501415
⑧6⑳出　願　昭63(1988)10月28日
⑧5翻訳文提出日　平1(1989)7月21日
⑧6国際出願　PCT/US88/03792
⑧7国際公開番号　WO89/05043
⑧7国際公開日　平1(1989)6月1日

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⑧1指定国　DE（広域特許），FR（広域特許），GB（広域特許），IT（広域特許），JP，NL（広域特許）

請求の範囲

（1）読出しおよび信号処理回路が集積されており、シリコン、ヒ化ガリウムまたはゲルマニウムから成るグループから選択された材料で形成された基体と、

水銀・カドミウム・テルル、水銀・亜鉛・テルル、水銀・カドミウム・セレニウム、水銀・亜鉛・セレニウム、水銀・カドミウム・硫黄、水銀・亜鉛・硫黄、鉛・錫・テルル、鉛・錫・セレニウム、鉛・錫・硫黄、インジウム・ヒ素・アンチモン、ガリウム・インジウム・アンチモン、またはガリウム・アンチモン・ヒ素から成るグループから選択された材料から成る前記基体上に成長された第1の半導体層と、

前記第1の半導体層上に成長された第2の半導体層とを含み、前記第1および第2の半導体層が受けた赤外線放射波に応答して前記基体中の前記読出しおよび信号処理回路に電気信号を伝送するように動作可能である赤外線放射波検出用のモノリシック構造。

（2）前記基体と前記第1の半導体層との間に設けられた第1のパッシベイション層を含む請求項1記載の装置。

（3）前記第1のパッシベイション層と第1の半導体層との間に設けられた第2のパッシベイション層を含む請求項2記載の装置。

（4）前記第1および第2のパッシベイション層は、前記第1の半導体層の形成を制御するように動作可能な複数の核ウインドウを含む請求項3記載の装置。

（5）前記第1の半導体層の核化は前記核ウインドウ中でのみ生じる請求項4記載の装置。

（6）前記第2の半導体層上に設けられた第3の半導体層を含み、前記第3の半導体層は前記第2の半導体層中における自由電荷キャリアの表面再結合速度を減少するように動作することができる請求項4記載の装置。

（7）前記第1、第2および第3の半導体層は金属的気相エピタキシによって成長される請求項6記載の装置。

（8）前記第3の半導体層上に設けられた反射防止材料の層を含む請求項1記載の装置。

（9）水銀・カドミウム・テルル、水銀・亜鉛・テルル、水銀・カドミウム・セレニウム、水銀・亜鉛・セレニウム、水銀・カドミウム・硫黄、水銀・亜鉛・硫黄、鉛・錫・テルル、鉛・錫・セレニウム、鉛・錫・硫黄から成るグループから選択された材料から形成された第1および第2の半導体材料の層を赤外線放射源に露出し、

前記半導体材料の第1および第2の層において光電流を発生し、

その上に前記第1および第2の半導体層が成長し、シリコン、ヒ化ガリウムまたはゲルマニウムから成るグループから選択された材料から形成された基体内に設けられた読出しおよび信号処理回路によって前記光電流を感知することを含む赤外線放射を検出する方法。

（10）前記第1の半導体材料の層、前記第2の半導体材料の層および前記基体はモノリシック構造を含む請求項9記載の方法。

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(11) 前記第１の半導体材料の層は第１のパッシベイション層によって前記基体から分離されている請求項９記載の方法。
(12) 前記第１のパッシベイション層は第２のパッシベイション層によって半導体材料の前記第１の層から分離されている請求項11記載の方法。
(13) 前記第１および第２のパッシベイション層は前記第１の半導体材料の層の形成を制御するように動作可能な複数の核ウインドウを含む請求項12記載の方法。
(14) 前記第２の半導体材料の層上に前記第３の半導体材料の層を設けることによって前記第２の半導体材料の層における自由電荷キャリアの表面再結合速度を減少する付加的なステップを含む請求項９記載の方法。
(15) 前記第１、第２および第３の半導体層は金属的気相エピタキシによって形成される請求項14記載の方法。
(16) 赤外線放射に反射防止材料の層を通過させることを可能にする付加的なステップを含む請求項９記載の方法。
(17) 読出しおよび信号処理回路が集積されており、前記読出しおよび信号処理回路の特性を最適化するように選択された材料で形成された基体と、
赤外線検出を最適化するように選択された材料から前記基体上に成長された第１の半導体層と、
前記基体と前記第１の半導体材料の層との間に設けられた複数のパッシベイション層と、
前記第１および第２の半導体層が受けた赤外線放射波に応答して前記基体中の前記読出しおよび信号処理回路に電気信号を伝送するように動作可能な前記第１の半導体層上に設けられた第２の半導体層と、
第２の半導体層における自由電荷キャリアの表面再結合速度を減少するように動作可能な前記第２の半導体層上に設けられた第３の半導体層と、
前記第３の半導体層上に設けられ、大気と第３の半導体層の屈折率の間の屈折率を有する反射防止被覆とを含む赤外線放射波を検出するためのモノリシック構造のアレイ。
(18) 前記複数のパッシベイション層は前記第１の半導体層の成長を制御するように動作可能な複数の核ウインドウを含む請求項17記載のアレイ。
(19) 前記核ウインドウの１つは前記第１の半導体層と前記読出しおよび信号処理回路との間における電気結合を可能にする請求項18記載のアレイ。
(20) 前記モノリシック構造は、さらに前記第１および第２の半導体層と前記読出しおよび信号処理回路との間における電気結合を可能にするオーム接触を含む請求項19記載のアレイ。

明　細　書

赤外線放射検出方法および装置

１．発明の分野

本発明は赤外線感知の分野、特に赤外線放射検出方法および装置に関する。

２．従来技術の説明

基本的な赤外線検出器は、調査、目標捜査および１乃至30μmの波長を有する電磁放射波の存在を感知する探査および追跡映像システムにおいてしばしば使用される。赤外線放射を検出するためにこれらの基本検出器は、トリグリシンサルフェートおよびランタンドープされたジルコン酸チタン酸鉛結晶のような温度感応性熱電気および強誘電材料をしばしば使用する。このような結晶は、結晶に取付けられた電極に対して電位降下をもたらす入射した赤外線放射波に応答して瞬間的な電気偏波を示す。材料の抵抗が入射した放射線の関数として変化する硫化鉛および水銀・カドミウム・テルルのような光導電性材料が使用されてもよい。最後に、固有のバンド・トウ・バンド電子ホール励起が入射した赤外線束に比例する電流または電圧を発生する水銀・カドミウム・テルル、インジウム・アンチモンまたは類似した材料から構成されるような光起電装置が使用されてもよい。

このような基本的検出器のアレイは熱映像システムを形成するために使用されてもよい。実時間において前方観察赤外線（"ＦＬＩＲ"）映像センサのようなプリズム反射鏡を回動する熱映像システムは基本検出器の１次元のアレイにわたってソースによって放出された放射線を走査するために使用される。基本的検出器がこのように使用された場合、検出器の一時的な出力は映像の２次元表示を生成するように使用されてもよい。観察または走査アレイのいずれかを使用することができる２次元検出アレイ映像システムにおいて、基本的検出器は自由電荷キャリアまたは電流を生成し、それは電荷結合装置（"ＣＣＤ"）のような適切な読出し集積回路によって監視されてもよい。ＣＣＤからの出力は時間遅延および積分または並列直列走査変換等の種々の技術によって処理されることが可能であり、フレーム速度、信号・雑音比等のシステム要求にしたがって選択される。その他の読出し装置が使用されてもよい。

上記の検出器構造は能率的であるが、それらは一般的にいくつかの製造に関連する欠点を有する。第１に、検出器および読出し装置が別々に構成され、その後機械的に結合される多数のこのような検出器構造はハイブリッド的に形成される。ハイブリッド構造の形成は付加的な処理ステップを含むため、このような構造はモノリシック装置（すなわち、検出器と読出しおよび信号処理回路が１つの材料のシステム中に形成されている装置）と比較して生産効率が低い傾向がある。さらに、形成中に意図しない欠陥が誘起されて信頼性を低め、特性を損うという可能性が高い。モノリシック検出器はハイブリッド形成に必要な付加的な処理ステップを回避するが、信号処理回路のために赤外線検出器と同一の材料を使用する必要がある。この材料（例えばＨｇ Ｃｄ Ｔｅ またはＩｎ Ｓｂ）

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は製造技術が充分に開発されているシリコンまたはヒ化ガリウムから形成される回路よりも常に低い特性の信号処理回路となる。

発明の要約

本発明の好ましい実施例によると、赤外線放射を検出する方法および装置が開示されている。装置は読出しおよび信号処理回路が集積された基体を含む。基体はシリコン、ヒ化ガリウムおよびゲルマニウムから成るグループから選択された材料から形成されている。第1の半導体の層は水銀・カドミウム・テルル、水銀・亜鉛・テルル、水銀・カドミウム・セレニウム、水銀・亜鉛・セレニウム、水銀・カドミウム・硫黄、水銀・亜鉛・硫黄、鉛・錫・テルル、鉛・錫・セレニウム、鉛・錫・硫黄、インジウム・ヒ素・アンチモン、ガリウム・インジウム・アンチモンまたはガリウム・アンチモン・ヒ素から成るグループから選択された材料から基体上に成長される。第2の半導体の層がそれから第1の半導体の層上に形成される。

図面の簡単な説明

本発明の種々の利点が以下の説明および図面から当業者に明らかになるであろう。

図面は本発明による赤外線放射を検出する装置の好ましい実施例の断面図である。

好ましい実施例の説明

本発明の好ましい実施例によると、赤外線放射を検出する構造10は図中で4で示されるように設けられる。構造10は単一の検出素子として使用されてもよいし、もしくは多数素子の映像装置の一部であってもよい。構造10はシリコン、ヒ化ガリウムまたはゲルマニウムから形成されてもよい基体12を含む。しかしその他の適切な材料が使用されてよいことが理解されるべきである。基体12は、以下に説明される半導体の層の出力を使用可能な形態に変換する符号14によって示された適切な読出しおよび信号処理回路を含む。読出しおよび信号処理回路14は、ここで参照されているBluzer, N.およびStehlac, R.による文献（"Buffered Direct Injection of Photocurrents into Charge-Coupled Device", IEEE Transactions on Electron Devices, ED25, n.2.p.160, 1978年2月）に記載されたものに類似していてもよい。半導体の層からの出力を処理するその他の適切な手段が使用されてもよい。

基体表面の電気特性を制御するために第1のパッシベイション層16が設けられている。第1のパッシベイション層16は基体12に最適なパッシベイション状態を提供する材料から選択される。このような材料はSiO_2またはSiN_4を含む。しかしその他の適切な材料が使用されてよいことが理解されるべきである。第2のパッシベイション層18は第1のパッシベイション層16上に付着される。第2のパッシベイション層18は以下に説明される赤外線能動半導体層に最適なパッシベイション状態を提供し、赤外線能動半導体層の核が発生しない面を形成する複数の材料の1つから形成される。このような材料はSiO_2またはZnSを含んでもよい。しかしその他の適切な材料が使用されてよいことが理解されるべきである。第1および第2のパッシベイション層16および18はオーム接触子20および複数の核ウインドウ22乃至26を有する。オーム接触子20は、以下に説明される第2の半導体層と読出しおよび信号処理回路14との間に電気結合を行うために使用される。核ウインドウ22乃至26は第1の半導体層の核にシード位置を与えるために使用される。さらに核ウインドウ24は第1の半導体層と読出しおよび信号処理回路14との間の電気結合を可能にする。

入射した赤外線に応答して光電流を発生するために構造10は、第1の半導体層28および第2の半導体層30を含む。第1および第2の半導体層28および30は共にベースおよびヘテロ接合フォトダイオードのコレクタ層を含む。第1の半導体層28は$Hg_{1-x}Cd_xTe$で定められた化学量的関係を有する水銀・カドミウム・テルルの層から構成される。xの組成値は、第1の半導体層28が赤外線スペクトル中の特定の波長の赤外線放射に感応するように選択される。例えば、xの組成値が約0.2であるように選択された場合、第1の半導体層28は所望の動作温度（例えば絶対温度77度）で約10乃至12mのカットオフ波長を有する長い波長の赤外線放射波に感応する。しかしながら、第1の半導体層28は水銀・亜鉛・テルル、水銀・カドミウム・セレニウム、水銀・カドミウム・硫黄、水銀・亜鉛・硫黄、水銀・亜鉛・セレニウム、鉛・錫・テルル、鉛・錫・セレニウム、鉛・錫・硫黄、インジウム・ヒ素・アンチモン、ガリウム・インジウム・アンチモン、またはガリウム・アンチモン・ヒ素、のようなその他の適切な材料を含んでもよいことが理解されるべきである。

第2の半導体層30は$Hg_{1-y}Cd_yTe$で定められる化学量的な関係を有する水銀・カドミウム・テルルの層を含む。yの組成値は第1の半導体層28の組成値xよりも大きいように選択され、典型的に0.3の値を有する。しかしながら、その他の適切なyの値が選択され、また水銀・カドミウム・テルル、水銀・亜鉛・テルル、水銀・カドミウム・セレニウム、水銀・亜鉛・セレニウム、水銀・カドミウム・硫黄、水銀・亜鉛・硫黄、鉛・錫・テルル、鉛・錫・セレニウム、鉛・錫・硫黄、インジウム・ヒ素・アンチモン、ガリウム・インジウム・アンチモンまたはガリウム・アンチモン・ヒ素を含むその他の適切な材料が選択されてもよいことが理解されるべきである。

第1の半導体層28はフォトダイオードベース層として動作し、一方第2の半導体層30はフォトダイオードコレクタ層として動作する。しかしながら構造10の収集効率を高めるために第1および第2の半導体層28および30の役割が逆にされてもよい（すなわち第2の半導体層30がベース層になり、第1の半導体層28がコレクタ層になる）。この場合、yの組成値は約0.2であり、xの組成値は約0.3である。しかしながら、一般的には第2の半導体層30は狭いバンドギャップ材料となり、第1の半導体層28は広いバンドギャップ材料となる。層28および30は反対の型の混合物を有するようにドープされる。すなわち第1の半導体層28はp型にドープされ、第2の半導

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体層はn型にドープされ、その逆も可能である。しかしながら、同じ型のヘテロ接合も使用されてよいことが理解されるべきである。

赤外線スペクトルにおける光の光子が装置構造10によって吸収されたとき、電子ホール対が発生される。電子ホール対が再結合する前に第1および第2の半導体層28および30の間の接合部に到達した場合、第1および第2の半導体層28および30の間の接合部における電界は電子をn型半導体層の中に移動させ、ホールをp型半導体層中に移動させる。この電子ホール移動は受光された光子の数に比例する光電流を生成する。

第1および第2の半導体層28および30において発生された光電流を感知するために、基体12はさらに重くドープされた領域32および34を含む。重くドープされた領域32は核ウインドウ24を通して読出しおよび信号処理回路14と第1の半導体層28との間に電気結合を可能にする。核ウインドウ24に付着される材料はHgTeまたは半導体層28に類似した結晶構造および格子定数を有する類似した半金属性の材料であることができる（すなわち、HgSe，HgS，PbTe，PbSe，PbS，およびグレイSnが代わりに選択されることができる）。これは重くドープされた領域32と第1の半導体層28との間に良好なオーム接触を提供する。同一の材料は同時に核ウインドウ22および26中に付着されるが、それは第1の半導体層28に対して、オーム接触ではなく核位置としてのみ作用する。さらに、重くドープされた領域34は金属化層36およびオーム接触子20を通じて読出しおよび信号処理回路14と第2の半導体層30との間に電気結合を提供する。オーム接触子20および36は2つの異なる金属であることができ、オーム接触子20は重くドープされた領域34との良好なオーム接触を生じるように選択され、金属化層36はn型用のプラチナおよびp型用の金のように第2の半導体層30との良好なオーム接触を形成するように選択される。金属化層36はまた第1の半導体層28の核が抑制される材料であるように選択されなければならない。

第2の半導体層30がフォトダイオードのベースとして動作する場合、第2の半導体層30の内部における自由電荷キャリアは第2の半導体層28との境界面に向かってドリフトし再結合する。この再結合の結果、自由電荷キャリアが第1のパッシベイション層16によって収集される効率が減少される。第2の半導体層30中の自由電荷キャリアの再結合の速度を減少するために、第2の半導体層30がフォトダイオードのベースとして動作するとき第3の半導体層38が設けられる。第3の半導体層38はzの組成値がyよりも大きいように選択された$Hg_{1-z}Cd_zTe$で定められた化学量的関係を有する水銀・カドミウム・テルルから形成されてもよい。しかしながら、水銀・カドミウム・テルル、水銀・亜鉛・テルル、水銀・カドミウム・セレニウム、水銀・亜鉛・セレニウム、水銀・カドミウム・硫黄、水銀・亜鉛・硫黄、鉛・錫・テルル、鉛・錫・セレニウム、鉛・錫・硫黄、インジウム・ヒ素・アンチモン、ガリウム・インジウム・アンチモンまたはガリウム・アンチモン・ヒ素のようなその他の適切な材料が使用されてもよいことが理解されるべきである。

さらに構造10は反射防止被覆40を含む。反射防止被覆40は第3の半導体層38上に設けられ、入射した赤外線放射の反射を減少するために使用される。反射防止被覆40は大気と第3の半導体層38の屈折率の間の屈折率を有する材料から形成される。反射防止被覆40は硫化亜鉛、セレン化亜鉛またはテルル化亜鉛から形成されてもよく、その他の適切な材料が使用されてもよい。構造10はまた第1のパッシベイション層16並びに第1および第2の半導体層28および30の相対電位を制御するために使用されるフィールドプレート領域42を含む。フィールドプレート42は第1および第2の半導体層28および30が第1のパッシベイション層16と交差する領域の下に設けられる。フィールドプレート領域42は基体12中にドープされるか、もしくは基体12の表面上に金属を付着させてもよい。

層28，30および16が交差する領域における電位の制御は装置特性にとって重要である。この領域における電位を制御するために、第1のパッシベイション層16は第1および第2の半導体層28および30の中の平坦なバンド電位の近くにおいて、電流動作におけるフォトダイオード特性を最適化するためにゲートが使用されるように供給電位の使用による平坦なバンド状態からの任意の偏差を補償するフィールド領域42を使用することによって安定した表面電位を与えるように選択される（すなわち、第1のパッシベイション層16は第1および第2の半導体層28および30をパッシベイション化するように選択される）。

第1のパッシベイション層16上で第1および第2の半導体層28および30が成長することにより自動的に自己パッシベイション埋設接合がもたらされる。フィールドプレート領域42の存在はゲート電圧制御による接合領域中の表面電位の最適化を可能にする。

上記の構造を与えることによって、構造10の特性は信号処理および赤外線検出の両観点から最適化されることができる。基体12は最適な特性の信号処理回路が形成されることができるシリコン、ヒ化ガリウムまたはゲルマニウムであってよい。それから赤外線検出を最適化する材料から選択された第1および第2の半導体28および30がヘテロエピタキシャル選択領域付着によって基体12上に設けられる。したがって、この検出器構造と基体12との組合せはモノリシックヘテロエピタキシャル焦点平面アレイを構成し、ハイブリッド化された構造に関連した欠点の弊害を受けない。

構造10は以下に説明された方法で形成されることができる。基体12が読出しおよび信号処理回路14と共に形成された後、重くドープされた領域32および34並びにフィールドプレート領域42が形成される。それからパッシベイション層16および18が基体12上に設けられる。それから接触ウインドウはフォトリソグラフによって重くドープされた領域34を覆うパッシベイション層16および18中に開けられる。第1の金属層は、重くドープされた領域34に対するオーム接触子20を形成するために真空蒸着により供給されリフトオフされる。その後、

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金属化層36を形成するために第２のフォトリソグラフステップが実行される。金属化層36の形態は構造10の境界を形成し、第２の半導体層30とオーム接触するように選択される。

その後、パッシベイション層16および18中に核ウインドウ22乃至26を開くために第３のフォトリソグラフステップが使用される。核ウインドウ22乃至26の形態、寸法および間隔は所望の検出器の幾何学形状および使用されるエピタキシャル成長過程の特性によって決定される。例えば、核ウインドウから横方向の成長が垂直方向の成長と同じ速度で生じた場合、ウインドウはそれらと同程度広く離されて位置されているべきである。多過ぎる個数の核ウインドウは基体12中の読出しおよび信号処理回路14に対して空間的な制限を与えるため、核ウインドウの数はまた最小にされるべきである。核ウインドウ22乃至26の個数および寸法は第１の半導体層28の垂直方向の成長速度に対する横方向の成長速度の比率を最大にすることによって最小化されることができる。さらに第２の半導体層30の垂直方向の成長速度に対する横方向の成長速度の比率はまた第１および第２の半導体層28および30の間の接合部と金属化層36との間に最大の可能な距離を与えるように最大にされるべきである。第１の半導体層28を厚い層に形成することによって、要求される核ウインドウ22乃至26の数は減少される。第２の半導体層30をさらに厚く形成することにより、金属化層36と第１および第２の半導体層28および30間の接合部との間の距離がより大きくなるので、横方向の成長速度のバリエーションに対してさらに許容性が与えられる。

パッシベイション層28および30に核ウインドウ22乃至26を開けた後、残りのフォトレジストはパッシベイション層16から除去され、基体12はその表面の現場浄化が行われるように低温金属的気相エピタキシャル反応器中に位置される。現場表面浄化は紫外線オゾンエッチング、原子水素エッチングまたは紫外線またはプラズマフィールド中の適切な反応物から生じたその他の遊離基によるエッチングを含む。

核結晶はパッシベイション層16および18の核ウインドウ22乃至26の中で成長する。パッシベイション層18および金属化層36が形成される材料は核結晶の形成を妨げるため、核結晶は核ウインドウ22乃至26中でのみ生じる。金属的気相エピタキシャル反応器中への反応物の流入は、核ウインドウ22乃至26中の核結晶上で核化する第１の半導体層28を成長させるように変化される。反応物流入はさらに第２の半導体層30を成長させるように変化される。反応物流入における最終変化により第３の半導体層38が成長させられることができる。最後に、反射防止層40が金属的気相反応器の外側で真空蒸着によって第３の半導体層38上に形成される。

したがって、本発明は赤外線検出を最適にするように赤外線材料が選択され、一方信号処理回路を最適化するように信号処理材料が選択されることができる赤外線放射を検出する装置を提供することができることが理解されるであろう。それ故、本発明はここに示された特定の実施例により限定されるものではない。例えば、別の適切な領域選択エピタキシャル成長技術が第１の半導体層を形成するために使用されてもよい。第１および第２の半導体層の相対的ドーピング並びにそれらが実行する作用（すなわちベースまたはコレクタ）も変化されてよい。その他の修正は明細書、図面および以下の請求の範囲の各項を検討することにより当業者に明らかになるであろう。

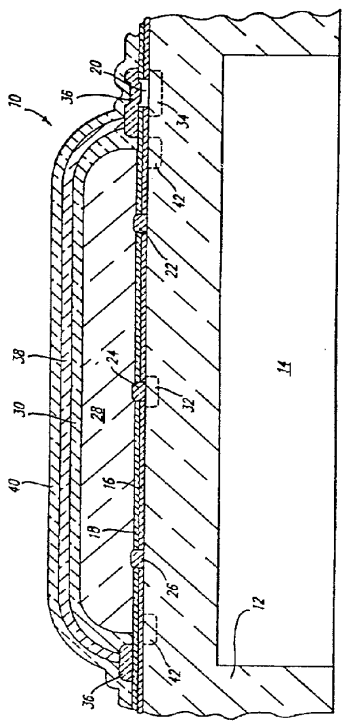


Fig. 1.

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国 際 調 査 報 告

International Application No PCT/US 88/03792

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) *

According to International Patent Classification (IPC) or to both National Classification and IPC

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II. FIELDS SEARCHED

Minimum Documentation Searched *

Classification System	Classification Symbols
IPC4	H 01 L, G 01 J

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched *

III. DOCUMENTS CONSIDERED TO BE RELEVANT *

Category *	Citation of Document, ** with indication, where appropriate, of the relevant passages **	Relevant to Claim No. **
X	US, A, 4559695 (I.M. BAKER) 24 December 1985, see column 3, line 8 - column 6, line 34; abstract; figures 1,6 --	1,17
A		9
X	US, A, 4521798 (I.M. BAKER) 4 June 1985, see column 3, line 6 - column 6, line 34; abstract; figures 1,6 --	1,17
A		9
A	EP, A2, 0137988 (TEXAS INSTRUMENTS INCORPORATED) 24 April 1985, see abstract; figure 1 --	1-3,8,9, 16,17
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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
14th April 1989	28. 04. 89
International Searching Authority: EUROPEAN PATENT OFFICE	Signature of Authorized Officer: P.C.G. VAN DER PUTTEN

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III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	US, A, 4549195 (N. BLUZER) 22 October 1985, see abstract; figures 2,3,5 --	1,9, 17
A	US, A, 4313127 (S.C. SU ET AL) 26 January 1982, see abstract; figure 1 --	1,17
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Form PCT ISA/210 (extra sheet) (January 1985)

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SA 26299

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		US-A- 4521798	04/06/85
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US-A- 4549195	22/10/85	NONE	
US-A- 4313127	26/01/82	NONE	
US-A- 4053919	11/10/77	NONE	

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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(71) Applicant: SANTA BARBARA RESEARCH CENTER [US/US]; 75 Coromar Drive, Goleta, CA 93117 (US).

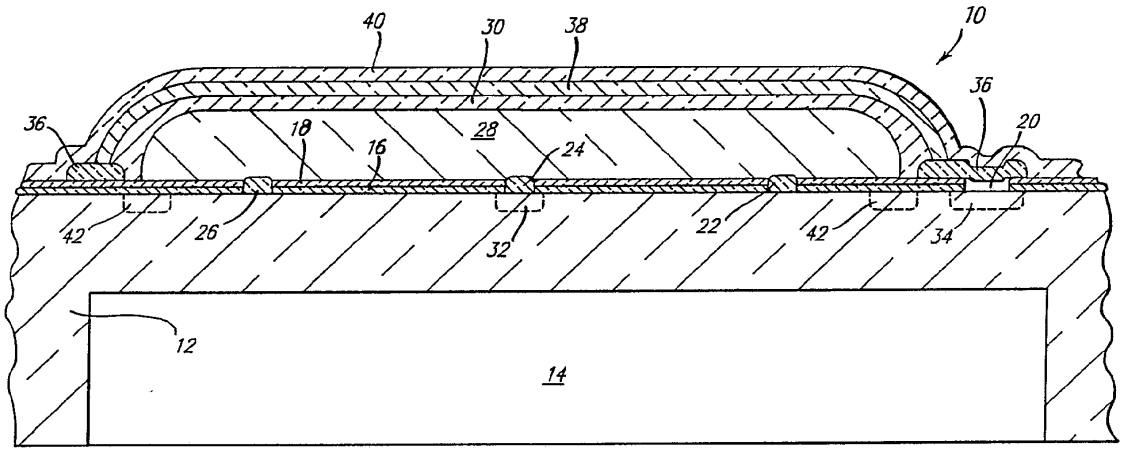
(72) Inventors: AHLGREN, William, L. ; 365 Hillsboro Way, Goleta, CA 93117 (US). SCHULTE, Eric, F. ; 2427 Calle Montilla, Santa Barbara, CA 93117 (US).

(74) Agents: SCHUBERT, William, C. et al.; Hughes Aircraft Company, Post Office Box 45066, Bldg. C1, M/S A-126, Los Angeles, CA 90045-0066 (US).

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(54) Title: METHOD AND APPARATUS FOR DETECTING INFRARED RADIATION



(57) Abstract

A method and apparatus for detecting infrared radiation is disclosed. The apparatus comprises a substrate (12) having readout and signal processing circuits (14) integrated therein. The substrate (12) is formed from a material selected from the group consisting of silicon, gallium arsenide, or germanium. A first semiconductor layer (28) is grown on the substrate (12) from a material selected from the group consisting of mercury-cadmium-telluride, mercury-zinc-telluride, mercury-cadmium-selenide, mercury-zinc-selenide, mercury-cadmium-sulfide, mercury-zinc-sulfide, lead-tin-telluride, lead-tin-selenide, lead-tin-sulfide, indium-arsenide-antimonide, gallium-indium-antimonide, or gallium-antimonide-arsenide. A second semiconductor layer (30) is then grown on the first semiconductor layer (28).

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METHOD AND APPARATUS FOR DETECTING INFRARED RADIATION

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to the field of infrared sensing, and more particularly concerns a method and apparatus for detecting infrared radiation.

2. Description of Related Art

Elemental infrared detectors are often used in surveillance, target seeking, and search and tracking imaging systems to sense the presence of electromagnetic radiation having wavelengths from 1-30 μm. To detect infrared radiation, these elemental detectors often use temperature sensitive pyroelectric and ferroelectric materials such as triglicine sulfate and lanthanum doped lead zirconate titanate crystals. Such crystals exhibit spontaneous electrical polarization in response to incident infrared radiation which creates a potential drop across electrodes attached to the crystals. Photoconductive materials such as lead-sulfide and mercury-cadmium-telluride may also be used in which the resistance of the material changes as a function of incident radiation. Finally, photovoltaic devices such as those fabricated from mercury-cadmium-telluride, indium antimonide, or similar materials may be used in which intrinsic band-to-band electron-hole excitation generates a current or voltage which is proportional to the incident radiation flux.

Arrays of such elemental detectors may be used to form thermal imaging systems. In real-time thermal imaging systems such as forward looking infrared ("FLIR") imaging sensors, oscillating prism

mirrors are used to scan radiation emitted by a source across a one-dimensional array of elemental detectors. When the elemental detectors are used in this manner, the temporal outputs of the detectors may be used to generate a two-dimensional representation of the image. In two-dimensional detector array imaging systems which can utilize either staring or scanning arrays, the elemental detectors produce free charge carriers or currents which may then be monitored by an appropriate readout integrated circuit such as a charge-coupled device ("CCD"). The output from the CCD can be processed by various techniques such as time delay and integration or parallel-to-serial scan conversion, with the choice depending on the system requirements of frame rate, signal-to-noise ratios, etc. Other readout devices may also be used.

While the detector structures described above are effective, they generally have several drawbacks in terms of fabrication. First, many of such detector structures are hybridized in which the detector and the readout device are separately fabricated and then mechanically bonded. Because the formation of hybridized structures involves additional processing steps, such structures tend to have lower yield during production when compared to monolithic devices (i.e., devices in which the detector and the readout and signal processing circuit are fabricated in one material system). In addition, there is a greater likelihood that defects will be unintentionally introduced during fabrication resulting in lower reliability and reduced performance. Monolithic detectors, while avoiding the additional processing steps required for hybridization, suffer from the necessity of using the same material as the infrared detector for the signal processing circuits. This material (e.g., HgCdTe or InSb) invariably leads to lower performance signal processing circuits than circuits formed from silicon or gallium arsenide, for which the fabrication technology is well-developed.

SUMMARY OF THE INVENTION

According to the preferred embodiment of the present invention, a method and apparatus for detecting infrared radiation is disclosed. The apparatus comprises a substrate having readout and signal processing circuits integrated therein. The substrate is formed from material selected from the group consisting of silicon, gallium arsenide, and germanium. A first semiconductor layer is grown on the substrate from a material selected from the group consisting of mercury-cadmium-telluride, mercury-zinc-telluride, mercury-cadmium-selenide, mercury-zinc-selenide, mercury-cadmium-sulfide, mercury-zinc-sulfide, lead-tin-telluride, lead-tin-selenide, lead-tin-sulfide, indium-arsenide-antimonide, gallium-indium-antimonide, or gallium-antimonide-arsenide. A second semiconductor layer is then formed on the first semiconductor layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The various advantages of the present invention will become apparent to one skilled in the art upon reading the following specification and by reference to the following drawing in which:

The FIGURE is a cross-sectional view of the preferred embodiment of the apparatus for detecting infrared radiation according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

According to the preferred embodiment of the present invention, a structure 10 for detecting infrared radiation is provided as shown 4 in the FIGURE. The structure 10 may be used as a single detection element, or be part of a multiple-element imaging device. The structure 10 comprises a substrate 12 which may be made of silicon, gallium arsenide, or germanium, though it is to be understood that other suitable materials may be used. The substrate 12 comprises suitable readout and signal processing circuits, generally designated by the numeral 14, for converting the output of the semiconductor layers described below into useable form. The readout and signal processing circuits 14 may be similar to that disclosed in Bluzer, N., and Stehlac, R., "Buffered Direct Injection of Photocurrents into

Charge-Coupled Devices", IEEE Transactions on Electron Devices, ED 25, n.2 p. 160 February 1978, which is hereby incorporated by reference. It should be understood that other suitable means for processing the output from the semiconductor layers may be used.

To control the electrical properties of the surface of the substrate, a first passivation layer 16 is provided. The first passivation layer 16 is selected from materials which provide optimum passivation for the substrate 12. Such materials may include SiO_2 or SiN_4, though it is to be understood that other suitable materials may be used. A second passivation layer 18 is deposited on the first passivation layer 16. The second passivation layer 18 is formed of one of several materials which provide optimum passivation for the infrared-active semiconductor layers described below and forms a surface on which nucleation of the infrared-active semiconductor layers does not occur. Such materials may include SiO_2 or ZnS, though it is to be understood that other suitable materials may be used. The first and second passivation layers 16 and 18 have a ohmic contact 20 and a plurality of nucleation windows 22-26. The ohmic contact 20 is used for providing electrical communication between the second semiconductor layer described below and the readout and signal processing circuits 14. The nucleation windows 22-26 are used for providing seed locations for nucleation of the first semiconductor layer. In addition, the nucleation window 24 allows electrical communication between the first semiconductor layer and the readout and signal processing circuits 14.

To generate a photocurrent in response to incident radiation, the structure 10 further comprises a first semiconductor layer 28 and a second semiconductor layer 30. The first and second semiconductor layers 28 and 30 together comprise the base and collector layers of a heterojunction photodiode. The first semiconductor layer 28 comprises a layer of mercury-cadmium-telluride having a stoichiometric relationship defined by $Hg_{1-x}Cd_xTe$. The composition value of x is chosen so that the first semiconductor layer 28 is sensitive to infrared radiation of a particular wavelength in the infrared spectrum. For example, if the composition value of x is chosen to be approximately 0.2, the first semiconductor layer 28 will

be sensitive to long wavelength infrared radiation having a cut-off wavelength of approximately 10-12 m at the desired operating temperature (e.g., 77 Kelvin). It is to be understood, however, that the first semiconductor layer 28 may comprise other suitable materials such as mercury-zinc-telluride, mercury-cadmium-selenide, mercury-zinc-selenide, mercury-cadmium-sulfide, mercury-zinc-sulfide, lead-tin-telluride, lead-tin-selenide, lead-tin-sulfide, indium-arsenide-antimonide, gallium-indium-antimonide, or gallium-antimonide-arsenide.

The second semiconductor layer 30 comprises a layer of mercury-cadmium-telluride having a stoichiometric relationship defined by $Hg_{1-y}Cd_yTe$. The composition value of y may be chosen to be larger than the composition value x of the first semiconductor layer 28, and may typically have a value of 0.3. It is to be understood, however, that other suitable values of y may be chosen and other suitable materials may also be chosen including mercury-cadmium-telluride, mercury-zinc-telluride, mercury-cadmium-selenide, mercury-zinc-selenide, mercury-cadmium-sulfide, mercury-zinc-sulfide, lead-tin-telluride, lead-tin-selenide, lead-tin-sulfide, indium-arsenide-antimonide, gallium-indium-antimonide, or gallium-antimonide-arsenide.

The first semiconductor layer 28 acts as a photodiode base layer while the second semiconductor layer 30 acts as a photodiode collector layer. To increase the collection efficiency of the structure 10, however, the roles of the first and second semiconductor layers 28 and 30 may be reversed (i.e., the second semiconductor layer 30 becoming the base layer and the first semiconductor layer 28 the collector layer). In this case, the composition value of y will be approximately 0.2 and the composition value of x will be approximately 0.3. More generally, however, the second semiconductor layer 30 will become the narrow bandgap material and the first semiconductor layer 28 will become the wide bandgap material. The layers 28 and 30 are doped to have impurities of opposite type, i.e., the first semiconductor layer 28 being doped p-type and the second semiconductor layer 30 being doped n-type, or vice-versa. It will be appreciated, however, that isotype heterojunctions may also be employed.

When a photon of light in the infrared spectrum of interest is absorbed by the apparatus structure 10, an electron/hole pair is

generated. If the electron/hole pair arrives at the junction between the first and second semiconductor layers 28 and 30 before recombining, the electric field at the junction between the first and second semiconductor layers 28 and 30 will cause the electron to move into the n-type semiconductor layer and the hole to move into the p-type semiconductor layer. This electron/hole migration produces a photocurrent which is proportional to the number of photons received.

To sense the photocurrent generated in the first and second semiconductor layers 28 and 30, the substrate 12 further comprises the heavily doped regions 32 and 34. The heavily doped region 32 allows electrical communication between the readout and signal processing circuits 14 and the first semiconductor layer 28 through the nucleation window 24. The material deposited in the nucleation window 24 can be HgTe or a similar semi-metallic material with crystal structure and lattice constant similar to the semiconductor layer 28 (thus, HgSe, HgS, PbTe, PbSe, PbS, and grey Sn could be alternative choices). This will provide a better ohmic contact between the heavily doped region 32 and the first semiconductor layer 28. The same material is simultaneously deposited in nucleation windows 22 and 26, but there it serves only as a nucleation site for first semiconductor layer 28, not as an ohmic contact. In addition, the heavily doped region 34 allows electrical communication between the readout and the signal processing circuits 14 and the second semiconductor layer 30 through a metallization layer 36 and the ohmic contact 20. The ohmic contact 20 and 36 can be two different metals, the ohmic contact 20 chosen to make good ohmic contact with the heavily doped region 34, and the metallization layer 36 chosen to make good ohmic contact with the second semiconductor layer 30, such as platinum for n-type and gold for p-type. The metallization layer 36 must also be chosen to be a material on which nucleation of first semiconductor layer 28 is suppressed.

When the second semiconductor layer 30 acts as the base of the photodiode, the free charge carriers in the interior of the second semiconductor layer 30 drift toward the interface with second semiconductor layer 28 and recombine. The result of this recombination is to reduce the efficiency with which free charge

carriers are collected by the first passivation layer 16. To reduce the recombination velocity of the free charge carriers in the second semiconductor layer 30 when the second semiconductor layer 30 acts as the base of the photodiode, a third semiconductor layer 38 is provided. The third semiconductor layer 38 may be fabricated from mercury-cadmium-telluride having a stoichiometric relationship defined by $Hg_{1-z}Cd_zTe$, in which the composition value of z is chosen to be greater than y. It is to be understood, however, that other suitable materials may be used such as mercury-cadmium-telluride, mercury-zinc-telluride, mercury-cadmium-selenide, mercury-zinc-selenide, mercury-cadmium-sulfide, mercury-zinc-sulfide, lead-tin-telluride, lead-tin-selenide, lead-tin-sulfide, indium-arsenide-antimonide, gallium-indium-antimonide, or gallium-antimonide-arsenide.

The structure 10 further includes an anti-reflection coating 40. The anti-reflection coating 40 is located on the third semiconductor layer 38 and is used to reduce the reflection of incident infrared radiation. The anti-reflection coating 40 is manufactured from a material which has an index of refraction between that of air and the third semiconductor layer 38. While the anti-reflection coating 40 may be fabricated from zinc sulfide, zinc selenide, or zinc telluride, other suitable materials may be used. The structure 10 also comprises the field plate regions 42 which are used to control the relative potential of the first and second semiconductor layers 28 and 30 as well as the first passivation layer 16. The field plates 42 are located below the region where the first and second semiconductor layers 28 and 30 intersect the first passivation layer 16. The field plate regions 42 may either be doped regions in the substrate 12 or metal deposited on the surface of the substrate 12.

Control of electrical potential in the region where layers 28, 30 and 16 intersect is essential to device performance. To control the electric potential in this region, the first passivation layer 16 is chosen to provide stable surface potentials, near the flat band potential, in the first and second semiconductor layers 28 and 30 (i.e., the first passivation layer 16 is chosen to passivate the first and second semiconductor layers 28 and 30) and by using the field

plate regions 42 to compensate for any deviation from the flat band condition by the use of an applied potential, in the same way as gates are used to optimize photodiode performance in current practice.

The growth of the first and second semiconductor layers 28 and 30 over the first passivation layer 16 provides automatically a self-passivated buried junction. The existence of field plate region 42 permits optimization of surface potential in the junction region by gate-voltage control.

By providing a structure as described above, the performance of the structure 10 may be optimized both from the signal processing viewpoint as well as from that of infrared detection. The substrate 12 may be silicon, gallium arsenide, or germanium from which signal processing circuits of optimum performance can be fabricated. The first and second semiconductor layers 28 and 30 which are chosen from a material which optimizes infrared detection are then deposited on the substrate by heteroepitaxial selected area deposition. The combination of this detector structure and the substrate 12 thus constitute a monolithic heteroepitaxial focal plane array, and does not suffer from the disadvantages associated with hybridized structures.

The structure 10 may be fabricated in the manner described below. Once the substrate 12 has been formed with the readout and signal processing circuit 14, the heavily doped regions 32 and 34 as well as the field plate regions 42 are formed. The passivation layers 16 and 18 are then deposited on the substrate 12. A contact window is then opened by photolithography in the passivation layers 16 and 18 over the heavily doped region 34. A first layer of metal is applied by vacuum deposition and lift-off so as to form the ohmic contact 20 for the heavily doped region 34. A second photolithographic step is then performed to form the metallization layer 36. The shape of the metallization layer 36 is chosen to form the boundary of the structure 10 and is selected to make ohmic contact with the second semiconductor layer 30.

A third photolithographic step is then used to open the nucleation windows 22-26 in the passivation layers 16 and 18. The shape, size and spacing of the nucleation windows 22-26 are to be

determined by the desired detector geometry and characteristics of the epitaxial growth process used. For example, if the lateral growth from the nucleation window occurs at the same rate as the vertical growth, then the windows should be spaced as far apart as they are wide. The number of nucleation windows should also be minimized as an excessive number of nucleation windows may place spacial constraints on the readout and signal processing circuits 14 in the substrate 12. The number and size of the nucleation windows 22-26 can be minimized by maximizing the ratio of the lateral growth rate to the vertical growth rate of the first semiconductor layer 28. In addition, the ratio of the lateral growth rate to the vertical growth rate of the second semiconductor layer 30 should also be maximized so as to provide the largest possible distance between the junction between the first and second semiconductor layers 28 and 30 and the metallization layer 36. By making the first semiconductor layer 28 a thick layer, the number of nucleation windows 22-26 required is reduced. Making the second semiconductor layer 30 thicker allows more tolerance for lateral growth rate variation since the distance between the metallization layer 36 and the junction between the first and second semiconductor layers 28 and 30 become larger.

After opening the nucleation windows 22-26 in the passivation layers 28 and 30, the remaining photoresist is removed from the passivation layer 16 and the substrate 12 is placed in a low-temperature metallorganic vapor phase epitaxial reactor so that in-situ clean-up of the surface of the substrate 12 can be performed. The in-situ surface clean-up may involve ultraviolet ozone etching, atomic hydrogen etching, or etching by other free radicals generated from suitable reactant sources in an ultraviolet or plasma field.

Nucleation crystals are then grown in the nucleation windows 22-26 of the passivation layers 16 and 18. Because the material from which the passivation layer 18 and the metallization layer 36 are formed resist the formation of nucleation crystals, the nucleation crystals only form in the nucleation windows 22-26. Reactant flow into the metallorganic vapor phase epitaxial reactor is then changed to grow the first semiconductor layer 28 which nucleates on the nucleation crystals in the nucleation windows 22-26. The reactant

flow is then further changed to grow the second semiconductor layer 30. A final change in the reactant flow permits the growth of the third semiconductor layer 38. Finally, the anti-reflection layer 40 is formed on the third semiconductor layer 38 by vacuum evaporation outside the metallorganic vapor phase reactor.

It will therefore be seen that the present invention is able to provide an apparatus for detecting infrared radiation in which the infrared material can be selected to optimize infrared detection, while the signal-processing material may be selected to optimize the signal processing circuits. The present invention should therefore not be judged in accordance with this specific example presented herein. For example, other suitable area selective epitaxial growth techniques may be used for forming the first semiconductor layer. The relative doping of the first and second semiconductor layers may also change, as well as the function which they perform (i.e., base or collector). Other modifications will become apparent to the skilled practictioner upon a study of the specification, drawings and following claims.

CLAIMS

What is Claimed is:

1. A monolithic structure for detecting infrared radiation comprising:

a substrate having readout and signal processing circuits integrated therein, said substrate formed from a material selected from the group consisting of silicon, gallium arsenide, or germanium;

a first semiconductor layer grown on said substrate from a material selected from the group consisting of mercury-cadmium-telluride, mercury-zinc-telluride, mercury-cadmium-selenide, mercury-zinc-selenide, mercury-cadmium-sulfide, mercury-zinc-sulfide, lead-tin-telluride, lead-tin-selenide, lead-tin-sulfide, indium-arsenide-antimonide, gallium-indium-antimonide, or gallium-antimonide-arsenide; and

a second semiconductor layer grown on said first semiconductor layer, said first and second semiconductor layers operable to deliver an electrical signal to said readout and signal processing circuits in said substrate in response to the infrared radiation received by said first and second semiconductor layers.

2. The apparatus of Claim 1, further comprising a first passivation layer disposed between said substrate and said first semiconductor layer.

3. The apparatus of Claim 2, further comprising a second passivation layer disposed between said first passivation layer and said first semiconductor layer.

4. The apparatus of Claim 3, wherein said first and second passivation layers comprises a plurality of nucleation windows operable to control the formation of said first semiconductor layer.

5. The apparatus of Claim 4, wherein nucleation of said first semiconductor layer occurs only in said nucleation windows.

6. The apparatus of Claim 4, further comprising a third semiconductor layer disposed on said second semiconductor layer, said third semiconductor layer operable to reduce the surface recombination velocity of the free charge carriers in said second semiconductor layer.

7. The apparatus of Claim 6, wherein said first, second and third semiconductor layers are grown by metallorganic vapor phase epitaxy.

8. The apparatus of Claim 1, further comprising a layer of anti-reflection material disposed on said third semiconductor layer.

9. A method for detecting infrared radiation comprising:

exposing a first layer and a second layer of semiconductor material to a source of infrared radiation, said first and second semiconductor layers being formed from a material selected from the group consisting of mercury-cadmium-telluride, mercury-zinc-telluride, mercury-cadmium-selenide, mercury-zinc-selenide, mercury-cadmium-sulfide, mercury-zinc-sulfide, lead-tin-telluride, lead-tin-selenide, lead-tin-sulfide;

generating a photocurrent in said first and second layers of semiconductor material; and

sensing said photocurrent by readout and signal processing circuits disposed within a substrate upon which said first and second semiconductor layers are grown, said substrate being formed of a material selected from the group consisting of silicon, gallium arsenide, or germanium.

10. The method of Claim 9, wherein said first layer of semiconductor material, said second layer of semiconductor material and said substrate comprise a monolithic structure.

11. The method of Claim 9, wherein said first layer of semiconductor material is separated from said substrate by a first passivation layer.

12. The method of Claim 11, wherein said first passivation layer is separated from said first layer of semiconductor material by a second passivation layer.

13. The method of Claim 12, wherein said first and second passivation layers comprise a plurality of nucleation windows operable to control formation of said first layer of semiconductor material.

14. The method of Claim 9, comprising the additional step of reducing the surface recombination velocity of free charge carriers in said second layer of semiconductor material by disposing a third layer of semiconductor material on said second layer of semiconductor material.

15. The method of Claim 14, wherein said first, second, and third semiconductor layers are formed by metallorganic vapor phase epitaxy.

16. The method of Claim 9, further comprising the additional step of allowing infrared radiation to pass through a layer of anti-reflection material.

17. An array of monolithic structures for detecting infrared radiation, each of said monolithic structures comprising:

a substrate having readout and signal processing circuits integrated therein, said substrate formed from a material selected to optimize performance of said readout and signal processing circuits;

a first semiconductor layer grown on said substrate from a material selected to optimize infrared detection;

a plurality of passivation layers disposed between said substrate and said first layer of semiconductor material;

a second semiconductor layer disposed on said first semiconductor layer operable to deliver an electrical signal to said readout and signal processing circuits in said substrate in response to the infrared radiation received by said first and second semiconductor layers;

a third semiconductor layer disposed on said second semiconductor layer operable to reduce the surface recombination velocity of the free charge carriers in said second semiconductor layer; and

an anti-reflection coating disposed on the third semiconductor layer, said anti-reflection coating having an index of refraction between that of air and the third semiconductor layer.

18. The array of Claim 17, wherein said plurality of passivation layers comprise a plurality of nucleation windows operable to control the growth of said first semiconductor layer.

19. The array of Claim 18, wherein one of said nucleation windows permits electrical communication between said first semiconductor layer and said readout and signal processing circuits.

20. The array of Claim 19, wherein said monolithic structure further comprises an ohmic contact permitting electrical communication between said first and second semiconductor layers and said read out and signal processing circuits.

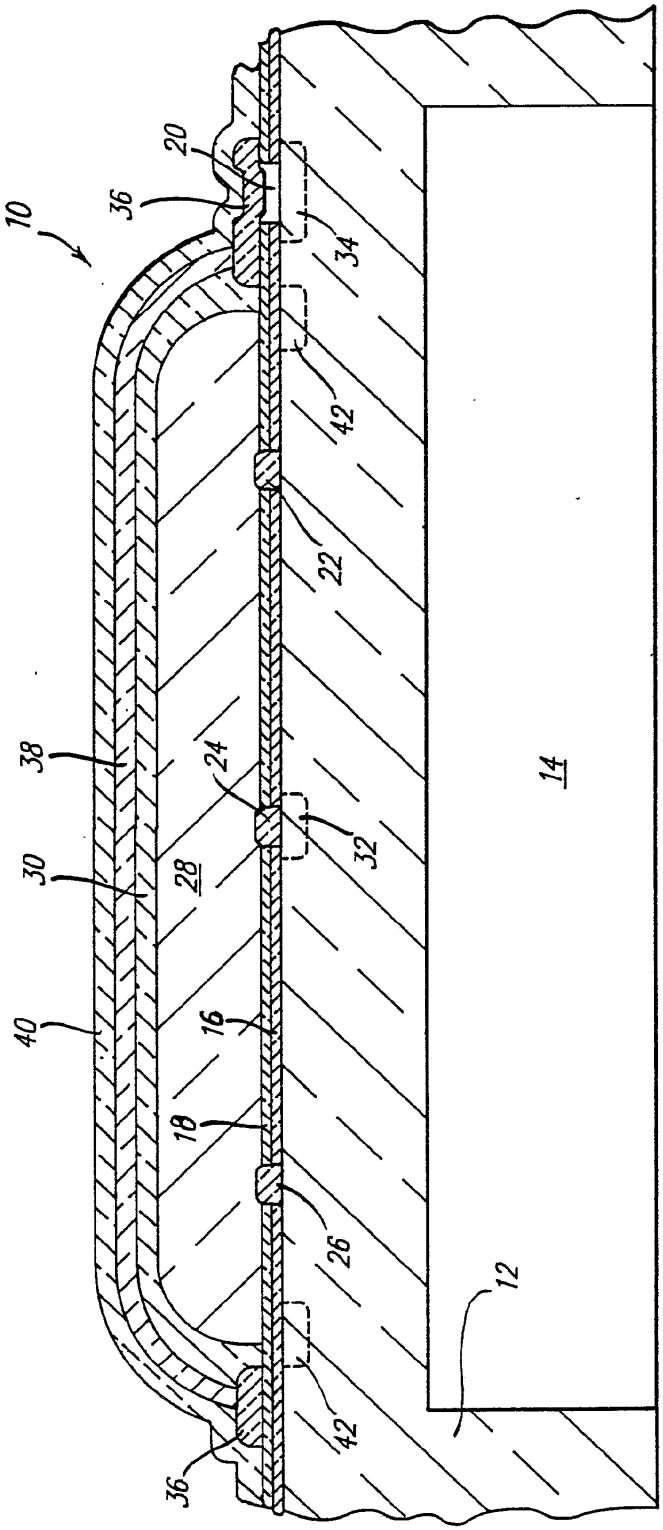


Fig. 1.

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 88/03792

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC4: H 01 L 31/08,27/14, G 01 J 5/20

II. FIELDS SEARCHED

Minimum Documentation Searched [7]	
Classification System	Classification Symbols
IPC4	H 01 L, G 01 J

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	US, A, 4559695 (I.M. BAKER) 24 December 1985, see column 3, line 8 - column 6, line 34; abstract; figures 1,6	1,17
A	--	9
X	US, A, 4521798 (I.M. BAKER) 4 June 1985, see column 3, line 6 - column 6, line 34; abstract; figures 1,6	1,17
A	--	9
A	EP, A2, 0137988 (TEXAS INSTRUMENTS INCORPORATED) 24 April 1985, see abstract; figure 1	1-3,8,9, 16,17
	--	
A	US, A, 4614960 (N. BLUZER) 30 September 1986, see abstract; figures 3,4	1,9, 17
	--	

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
14th April 1989	28. 04. 89
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	P.C.G. VAN DER PUTTEN

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
A	US, A, 4549195 (N. BLUZER) 22 October 1985, see abstract; figures 2,3,5 --	1,9, 17
A	US, A, 4313127 (S.C. SU ET AL) 26 January 1982, see abstract; figure 1 --	1,17
A	US, A, 4053919 (A.M. ANDREWS, II ET AL) 11 October 1977, see abstract; figure 2 --	1,9, 17
A	IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. ED-25, No. 2, February 1978, N. Bluzer et al: "Buffered Direct Injection of Photocurrents into Charge-Coupled Devices ", see page 160 - page 166 cited in the application --	1,9, 17

ANNEX TO THE INTERNATIONAL SEARCH REPORT
ON INTERNATIONAL PATENT APPLICATION NO. PCT/US 88/03792

SA 26299

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report.
The members are as contained in the European Patent Office EDP file on 03/03/89
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 4559695	24/12/85	EP-A-B- 0061803	06/10/82
		GB-A-B- 2095905	06/10/82
		JP-A- 57171226	21/10/82
		US-A- 4521798	04/06/85
US-A- 4521798	04/06/85	EP-A-B- 0061803	06/10/82
		GB-A-B- 2095905	06/10/82
		JP-A- 57171226	21/10/82
		US-A- 4559695	24/12/85
EP-A2- 0137988	24/04/85	US-A- 4447291	08/05/84
		EP-A- 0288792	02/11/88
		JP-A- 60094764	27/05/85
		US-A- 4684812	04/08/87
		US-A- 4686373	11/08/87
US-A- 4614960	30/09/86	NONE	
US-A- 4549195	22/10/85	NONE	
US-A- 4313127	26/01/82	NONE	
US-A- 4053919	11/10/77	NONE	

EPO FORM P0479

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

Attorney Docket No.: 309-0015USCIPDIV **PATENT**
Confirmation No.: 5818

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Shih-Yuan WANG Application No.: 18/822,880 Filed: September 3, 2024 Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	Examiner: EDUARDO A RODELA Art Unit: 2893 **CERTIFICATE OF TRANSMISSION** I hereby certify that this correspondence is being submitted through the USPTO Electronic Filing Service addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 /Mary Ellen Finnegan/ Date: December 5, 2024 Name: Mary Ellen Finnegan

VIA EFS-Web
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

It is respectfully requested that the documents listed on the attached Information Disclosure Citation form PTO/SB/08a be considered by the Patent Examiner in connection with the above-identified application and be made of record therein.

A copy of the non-U.S. patent document is enclosed herewith, in compliance with 37 CFR 1.98.

Independent consideration and acknowledgement of the enclosed document are respectfully requested.

The Commissioner is hereby authorized to charge U.S. PTO Deposit Account 600125 any payment due and to credit any overpayment thereto.

Respectfully submitted,

/Ivan S. Kavrukov/
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Application Number * 18/822,880 *	Application/Control No. 18/822,880	Applicant(s)/Patent under Reexamination WANG et al.	
	Examiner RODELA, EDUARDO A	Art Unit 2893	

Document Code - DISQ	Internal Document - DO NOT MAIL

TERMINAL DISCLAIMER	☑ APPROVED	☐ DISAPPROVED
Date Filed: 22 November 2024	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:

/JEAN PROCTOR/

Technology Center: OPLC

Telephone: (571)272-1040

16 td's

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
18/822,880	**11/22/2024 10:17:10 AM Z ET**	**309-0015USCIPDIV**

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68074993	FILING DATE	09/03/2024
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV_ResponseToFirstOfficeActionDated19Nov2024-Final.pdf	6	Amendment Copy Claims/Response to Suggested Claims	494 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
309-0015USCIPDIV_ResponseToFirstOfficeActionDated19Nov2024-Final.pdf	5F24725AB9DFFD839699EE2DBC51A2C5C44DB3BC415D1991CCEE2CE6808BCB6C616C6869DD7D1F11E150B30BE05205231FC184D2A67088158A39000F92CE5809

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Shih-Yuan WANG et al.
Serial No.:	18/822,880
Examiner:	EDUARDO A RODELA
Group Art Unit	2893
Filing Date:	09/03/2024
For:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
Conf. No.	5818

Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, New York 10001

CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: November 22, 2024

I hereby certify that this correspondence is being transmitted via Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

RESPONSE TO NON-FINAL OFFICE ACTION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the non-final Office Action dated 11/19/2024, please amend the above-identified application as follows:

Amendments to the Claims:

Please rewrite the claims as follows. These amended claims replace all previously filed claims:

1. (currently amended) An integrated structure comprising:

an array of pillars comprising Si, Ge, and/or SiGe alloy semiconductor material, wherein at least some of the pillars are configured to include photodetectors and have respective light-receiving surfaces and respective sides;

wherein at least some of the pillars comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;

one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars, have elongated or other shapes at or parallel to the light-receiving surfaces, extend into the pillars to a depth of 100 to10000 nm, and are filled at least partly with solid dielectric material;

wherein at least some of the holes are elongated along the respective light-receiving surfaces;

side-isolation comprising solid material between at least portions of the sides of at least some of the pillars;

a solid dielectric material forming a base dielectric region for the array;

electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;

wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes.

2. (previously presented) The integrated structure of claim 1, wherein the array is monolithically integrated with Si electronic devices.

3. (canceled) The integrated circuit of claim 1, in which at least some of the holes are elongated along the respective light-receiving surfaces.

4. (currently amended) The integrated structure of claim ~~3~~1, wherein each of at least some of the pillars has a plurality of the elongated holes.

5. (currently amended) The integrated structure of claim ~~3~~1, wherein each of at least some of the pillars has only one of the elongated holes.

6. (currently amended) The integrated structure of claim ~~3~~1, in which the light-receiving surfaces have respective widths, and the elongated holes extend along less than the widths of the light-receiving surfaces of at least some of the pillars in which the holes are fabricated.

7. (currently amended) The integrated structure of claim 6 in which each of at least some of the elongated holes has at least one closed contour remote from respective side edges of the light-receiving surface in which the hole is fabricated.

8. (previously presented) The integrated structure of claim 1, in which the electrical contacts are configured to selectively provide electrical fields across at least some of the photodetectors.

9. (previously presented) The integrated structure of claim 1, in which two or more of the photodetectors share one of the electrical contacts.

10. (previously presented) The integrated structure of claim 1, wherein the array is monolithically integrated with Si electronic devices for signal processing and transmission.

11. (previously presented) The integrated structure of claim 1, wherein the array is monolithically integrated with Si electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors.

12. (previously presented) The integrated structure of claim 1, in which each of at least some of the photodetectors is configured such that the light passes through at least a part of the one of the P-doped region and N-doped region of the photodetector before reaching any part of the other doped region of the photodetector.

13. (previously presented) The integrated structure of claim 1, in which the doped regions of each of at least some of the photodetectors are configured such that the light passes through at least a part of the P-doped region before reaching any part of the N-doped region.

14. (previously presented) An integrated structure comprising:

an array of pillars comprising Si, Ge, and/or alloyed SiGe semiconductor material, wherein at least some of the pillars have respective sides and respective light-receiving surfaces with selected widths and comprise at least one photodetector;

wherein at least some of the pillars comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;

one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars,

wherein each of the holes (i) has an elongated shape extending in length over less than the width of the light-receiving surface in which the hole is fabricated, (ii) has at least one closed contour at the light-receiving surface in which the hole is fabricated, (ii) extends into the pillar in which the hole is fabricated to a depth of 100 to10000 nm, and (iv) is filled at least partly with solid dielectric material;

side-isolation comprising solid material between at least portions of the sides of at least some of the pillars;

a solid dielectric material forming a base dielectric region for the array;

electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;

wherein the presence of the one or more holes increases, by a factor of at least 1.1, absorption of the light by at least some of the photodetectors relative to like photodetectors lacking the holes; and

wherein the array is monolithically integrated with Si electronic devices for signal processing and transmission.

15. (previously presented) The integrated structure of claim 14, in which each of at least some of the pillars has only one of the elongated holes fabricated therein.

16. (previously presented) The integrated structure of claim 14, in which each of at least some of the pillars has at least two of the elongated holes.

17. (previously presented) The integrated structure of claim 14, in which each of at least some of the photodetectors includes at least one of the holes.

REMARKS

Applicant submits that the application is in condition for allowance because claim 1 has been combined with the subject matter of claim 3 (now canceled), which the Office Action stated would be allowable if placed in independent form. Dependent claims 2 and 4-13 claims now depend on amended claim 1 that includes the subject matter of allowable claim 3. The Office Action states that the remaining claims, which are claims 14-17, are allowed.

Applicant believes that the rejected claims patentably differ from the applied references but, for the sake of having the subject application lead to a patent as soon as possible, plans to take up that question in a future divisional application.

Applicant hereby makes of record a brief communication with the Examiner on 11/12/2024 to identify a 2013 priority provisional application and two papers filed in the immediate parent of the subject application, and another brief communication on 11/22/2024 advising the Examiner of the filing of Terminal Disclaimers.

Applicant invites the Examiner to telephone the undersigned if it appears that a call may help advance prosecution.

Please charge any shortfall and credit any overpayments to our Deposit Account number 600125.

Respectfully Submitted,

WISSING MILLER LLP
Attorney for Applicants
By: /Ivan S. Kavrukov/
Ivan S. Kavrukov
Reg. No. 25,161
Tel.: (917) 945-0121

PTO/AIA/26 (04-14)
Approved for use through 11/30/2020. OMB 0651-0031
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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV

In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 11,309,444 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
November 22, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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Privacy Act Statement

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV

In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 11,830,954 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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/Ivan S. Kavrukov/ — Signature
November 22, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV

In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 9,530,905 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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/Ivan S. Kavrukov/ — Signature
November 22, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV

In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

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/Ivan S. Kavrukov/ — Signature
November 22, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

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In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

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Privacy Act Statement

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV

In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 9,818,893 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
November 22, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV

In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 11,121,271 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
November 22, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV

In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 12,087,871 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
November 22, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

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November 22, 2024 — Date

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Attorney of Record — Title
917-945-0121 — Telephone Number

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV

In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 11,621,360 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
November 22, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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Privacy Act Statement

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV

In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 9,525,084 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
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Check either box 1 or 2 below, if appropriate.

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2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
November 22, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV

In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 12,094,903 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
November 22, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV

In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: November 13, 2024

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 11,791,432 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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/Ivan S. Kavrukov/ — Signature
November 22, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV

In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 9,496,435 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
November 22, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV

In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 10,468,543 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
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/Ivan S. Kavrukov/ — Signature
November 22, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0015USCIPDIV

In re Application of: Shih-Yuan WANG

Application No.: 18/822,880

Filed: September 3, 2024

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

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/Ivan S. Kavrukov/ — Signature
November 22, 2024 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
18/822,880	**11/22/2024 09:56:49 AM Z ET**	**309-0015USCIPDIV**

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68074574	FILING DATE	09/03/2024
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 16

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV_TerminalDisclaimer_9496435.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIPDIV_TerminalDisclaimer_9525084.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIPDIV_TerminalDisclaimer_9530905.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIPDIV_TerminalDisclaimer_10446700.pdf	2	Terminal Disclaimer Filed	157 KB
309-0015USCIPDIV_TerminalDis	2	Terminal Disclaimer Filed	157 KB

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309-0015USCIPDIV_TerminalDisclaimer_9818893.pdf	2	Terminal Disclaimer Filed	157 KB
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309-0015USCIPDIV_TerminalDisclaimer_12087871.pdf	2	Terminal Disclaimer Filed	152 KB
309-0015USCIPDIV_TerminalDisclaimer_18113474.pdf	2	Terminal Disclaimer Filed	240 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
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309-0015USCIPDIV_TerminalDisclaimer_18113474.pdf	FA49F2D7A3014A5C6B006FA9D067E0C21E8D548FABB034280A21A8AF1ECB901D8A61B539799C7FC1E7A20761B076E90A49C3A50A5139D473D306CA70FC5F0B20

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
18/822,880	**11/22/2024 09:56:49 AM Z ET**	**309-0015USCIPDIV**

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68074574	AUTHORIZED BY	Ivan Kavrukov
CUSTOMER #	139982	FILING DATE	09/03/2024
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Shih-Yuan WANG

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 2892	**E2024AL057568526**	**Mary Ellen Finnegan**

PRE-AUTHORIZED ACCOUNT	PRE-AUTHORIZED CATEGORY
600125	**37 CFR 1.21 (Miscellaneous fees and charges)**

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2814	STATUTORY DISCLAIMER, INCLUDING TERMINAL DISCLAIMER	170.00	16	2720.00
			TOTAL AMOUNT:	**$2,720.00**

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 18/822,880	Filing Date 09/03/2024	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $40 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $ 192 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	11/22/2024	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 17	Minus	** 20	= 0		x $40 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $ 192 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/VICTORIA JOHNSON/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/822,880	09/03/2024	Shih-Yuan WANG	309-0015USCIPDIV	5818

139982 7590 11/19/2024

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER	
RODELA, EDUARDO A	

ART UNIT	PAPER NUMBER
2893	

NOTIFICATION DATE	DELIVERY MODE
11/19/2024	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

Office Action Summary	**Application No.** 18/822,880	**Applicant(s)** WANG et al.	
	Examiner Eduardo A Rodela	**Art Unit** 2893	**AIA (FITF) Status** Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 10/31/2024.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-17 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☑ Claim(s) 14-17 is/are allowed.

7) ☑ Claim(s) 1-2 and 8-13 is/are rejected.

8) ☑ Claim(s) 3-7 is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 9/3/2024 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

This correspondence is in response to the communications received October 31, 2024. Claims 1-17 are pending. This office action is being examined under an expedited "special" status due to Applicant's Age, see "Petition Decision" document dated October 28, 2024 in the file wrapper.

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Priority

The first instance of pillars having recesses formed therein can be found in provisional application 61/834,873 (dated June 13, 2013), on pg. 39. Therefore, the instant application's effective date is **June 13, 2013**.

Relevant Prior Art

Yu et al. (US 9,515,218) Fig. 8A, shown below. This reference alone cannot be used to reject claim 1, but has similar structures depicting the state of the art at the time of the invention.

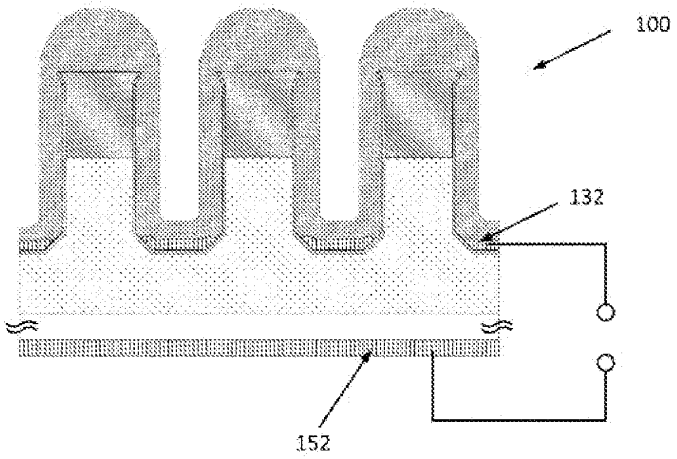


Fig. 8A

Hazeghi et al. (US 2013/0125965) Fig. 1 shown below. This reference alone cannot be used to reject claim 1, but has similar structures depicting the state of the art at the time of the invention.

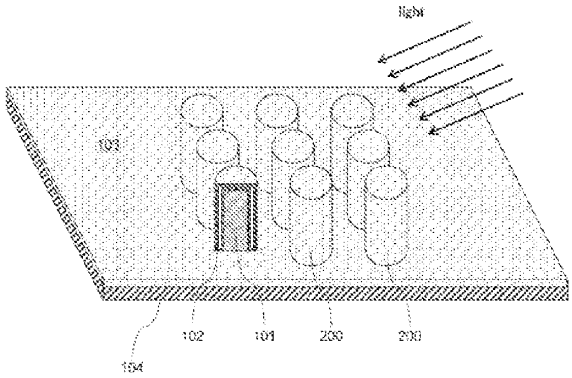
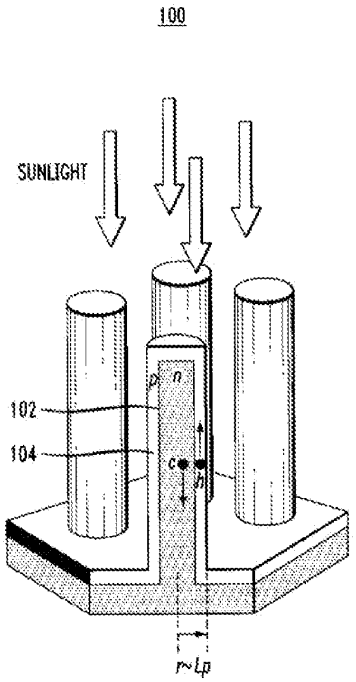


FIG. 1

Graham et al. (US 2012/0196401) Fig. 1, shown below. This reference alone cannot be used to reject claim 1, but has similar structures depicting the state of the art at the time of the invention.

FIG. 1



Lal et al. (US 9,263,519) Fig. 22a shows the specifics about electrical connections, see below. This reference alone cannot be used to reject claim 1, but has similar structures depicting the state of the art at the time of the invention.

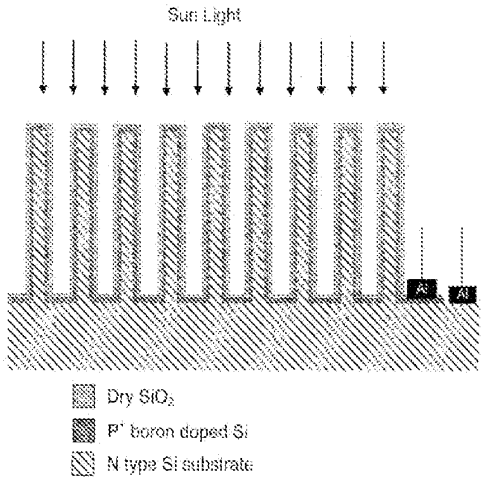


FIG. 22a

Applicant's Claim to Figure Comparison

It is noted that this comparison is merely for the benefit of reviewers of this office action during prosecution, to allow for an understanding of the examiner's interpretation of the Applicant's independent claims as compared to disclosed embodiments in Applicant's Figures. No response or comments are necessary from Applicant.

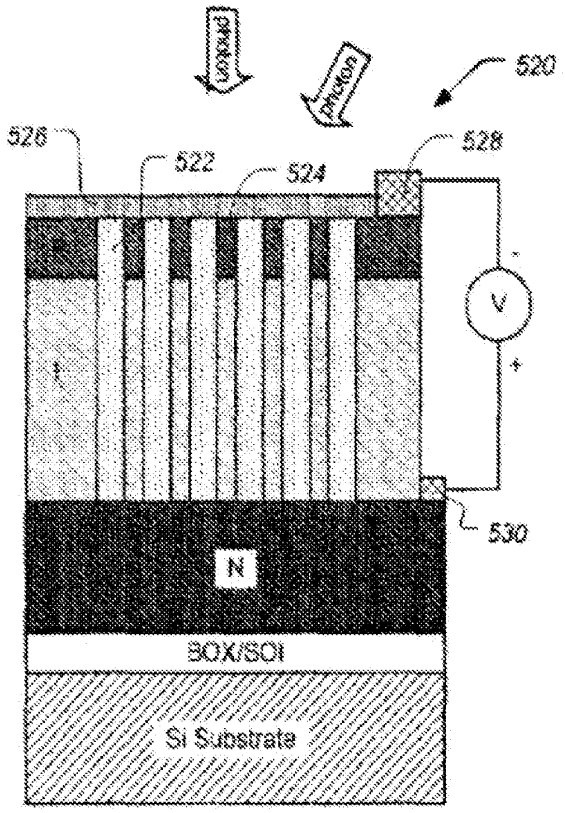


FIG. 5B

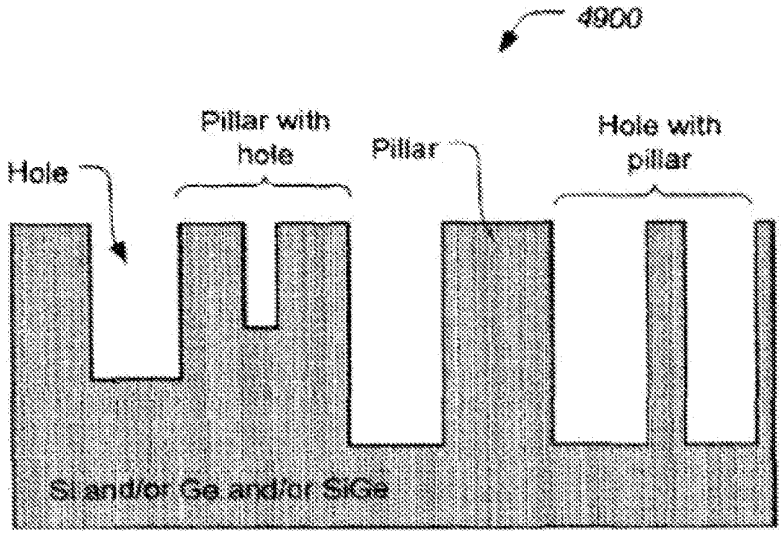


FIG. 49

Regarding claim 1, the Applicant discloses in Figs. 5B and 49, an integrated structure comprising:

an array of pillars ("pillars 524", ¶ 0132) comprising Si, Ge, and/or SiGe alloy semiconductor material, wherein at least some of the pillars are configured to include **photodetectors** and have respective light-receiving surfaces and respective sides ("The PD (and APO) photosensitive area (defined by the P-I-N or P-I-P-I-N junction area)", ¶ 0132);

wherein at least some of the pillars comprise P-doped and N- doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers ("The PD (and APO) photosensitive area (defined by the P-I-N or P-I-P-I-N junction area)", ¶ 0132);

one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars, have elongated or other shapes at or parallel to the light-receiving surfaces, extend into the pillars to a depth of 100 to10000 nm, and are filled at least partly with solid dielectric material;

side-isolation comprising solid material between at least portions of the sides of at least some of the pillars;

a solid dielectric material forming a base dielectric region for the array;

electrical contacts configured to provide electrical pathways coupled electrically to at least some of the **photodetectors**, including for selected reverse-biasing thereof;

wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the **photodetectors** relative to like **photodetectors** lacking said holes.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, 8, 9 and 12 are rejected under 35 U.S.C. 103 as being unpatentable over Yu et al. (US 2011/0309331) in view of Lunev et al. (US 2014/0016660, used to represent the provisional application 61/670,808 whose effective date is July 12, 2012) in view of Counil et al. (US 2010/0116332) in view of Arimoto et al. (US 5,759,292).

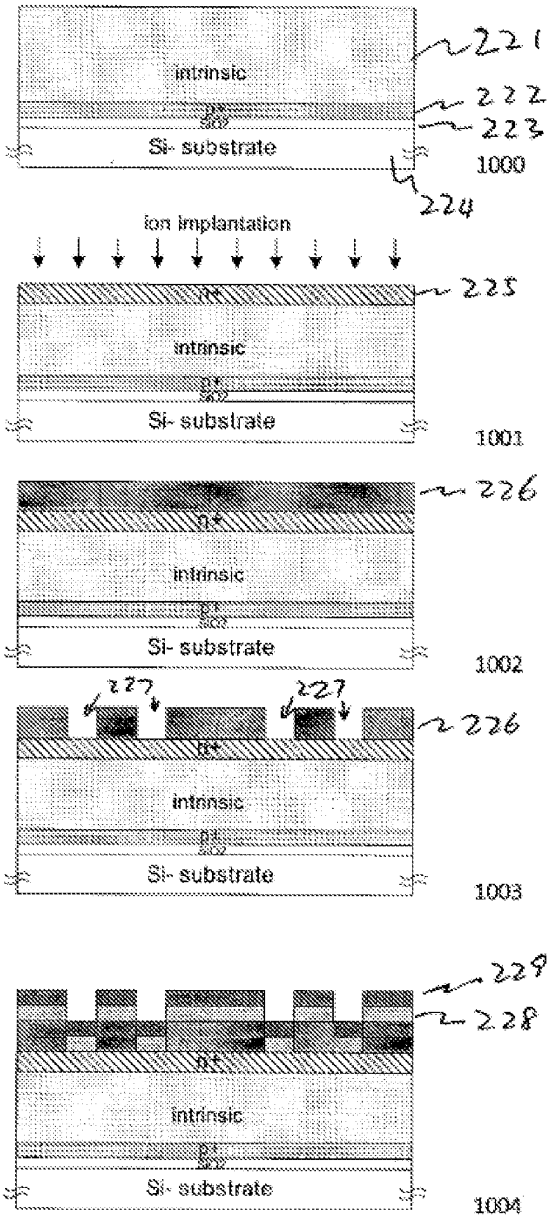
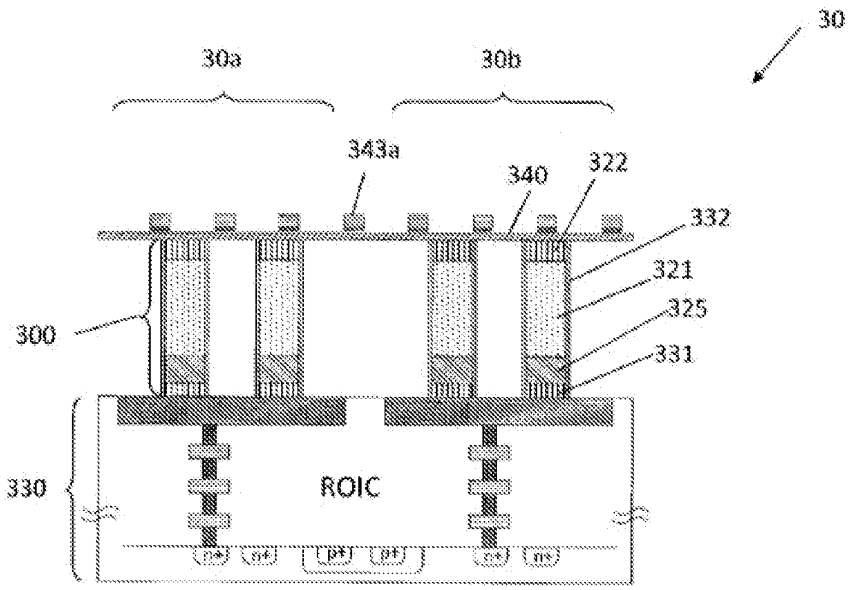

intrinsic
Si- substrate
221
222
223
224
1000
ion implantation
225
1001
226
1002
227
227
226
1003
229
228
1004

Fig. 4



Regarding claim 1, the prior art of Yu discloses in Figs. 4 and 5, an integrated structure comprising:

an array of pillars ("nanowires 300", ¶ 0079) comprising Si, Ge, and/or SiGe alloy semiconductor material ("wherein the silicon substrate 224 comprises an silicon oxide layer 223 thereon and the first heavily doped semiconductor layer 222 (e.g. heavily doped p type silicon) on the silicon oxide layer 223.", ¶ 0050, and layers 221 and 225 are silicon as well, "the second heavily doped semiconductor layer 225 (e.g. heavily doped n type silicon) is fabricated on the layer 221 by a method such as ion implantation and subsequent annealing.", ¶ 0051), wherein at least some of the pillars are configured to include photodetectors (¶ 0025) and have respective light-receiving surfaces and respective sides (top of and side surfaces of nanowires 300);

wherein at least some of the pillars (300/200) comprise P-doped (222, shown to be p-type in Fig. 4) and N- doped (225, shown to be n-type in Fig. 4) regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers (¶ 0005, "An APD is a highly sensitive semiconductor electronic device that exploits the photoelectric effect to convert light to electricity.");

side-isolation (236, Fig. 4 cont'd) comprising solid material between at least portions of the sides of at least some of the pillars ("Space between the nanowires 200 is preferably filled with an oxide layer 236.", ¶ 0048);

a solid dielectric material (part of the base is made up of "SiO2") forming a base dielectric region for the array (array of 300/200 are formed on "SiO2" layer);

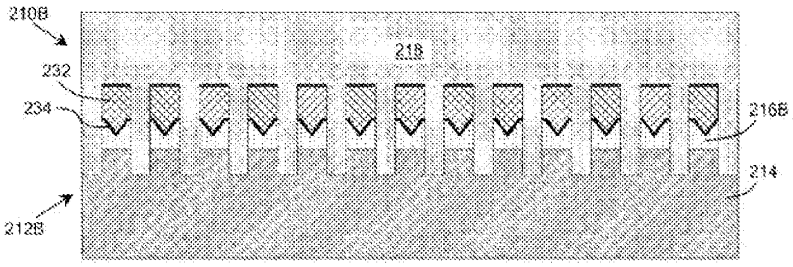
electrical contacts (top electrode is 340, ¶ 0079, and bottom electrode is "The metal silicide layer 231 forms electrical contact to any electrical components of the substrate 230", ¶ 0048) configured to provide electrical pathways coupled electrically to at least some of the photodetectors (noted electrical contact provide electrical signals to pillars 200/300), including for selected reverse-biasing thereof ("By applying a high reverse bias voltage (typically 100-200 V in silicon), APDs show an internal current gain (around 100).", ¶ 0005).

First, Yu does not disclose, "one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars, have elongated or other shapes

at or parallel to the light-receiving surfaces, extend into the pillars to a depth of 100 to10000 nm, and are filled at least partly with solid dielectric material".

Lunev discloses in Fig. 4B (provided below), where pillars are formed with "recesses" in the top surfaces, as disclosed in ¶ 0051, "The conducting layer of the ohmic contact 218 is separated from the corresponding semiconductor contact structure 212A, 212B by a filler material 232 (e.g., silicon dioxide or the like). In FIG. 4B, **a top surface 234 of the top semiconductor layer 216B is roughened or patterned, e.g., by including pyramids, holes**, etched roughness, or the like, which can be configured to scatter light, e.g., generated in the semiconductor contact structure 212B." From ¶ 0075, "As described herein, a device including an ohmic contact described herein can comprise a light emitting device, such as a light emitting diode (LED), a laser diode (LD), a **photodiode**, and/or the like."

FIG. 4B



Counil discloses in ¶ 0016, where texture surface height 'h' can be formed in dimensions between 20nm to 1um, 30nm to 500nm and 50 nm to 200nm.

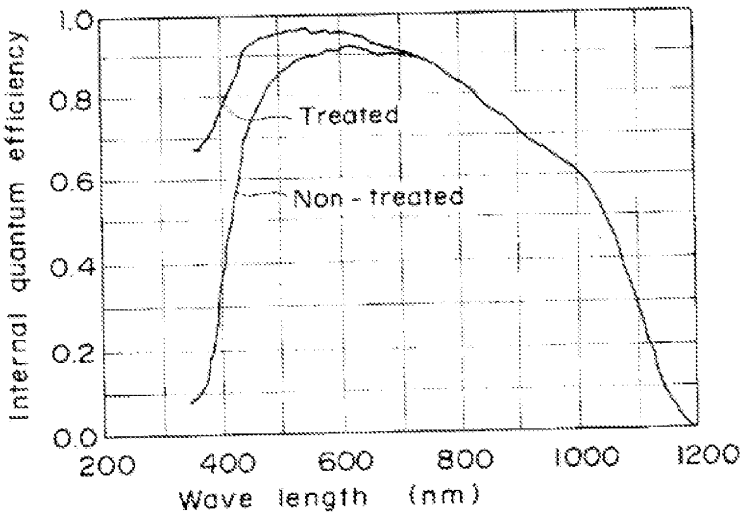
Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was effectively filed to use the "one or more holes that are fabricated as recesses at or under the light-receiving surface of each of at least some of the pillars, have elongated or other

shapes at or parallel to the light-receiving surfaces, extend into the pillars to a depth of 100 to10000 nm, and are filled at least partly with solid dielectric material", as disclosed by Lunev and Counil in the system of Yu, for the purpose of improving the light extraction efficiency. *G. TSM: Teaching, Suggestion, Motivation Test.*

Second, Yu does not disclose, "wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes."

Arimoto shows in Fig. 5 (provided below), where at least 10% efficiency is gained by texturizing the light incident surface.

Fig. 5



Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was effectively filed to use the "wherein the presence of said one or more holes

increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes", as disclosed by Arimoto in the system of Yu, for the purpose of improving the internal quantum efficiency which is to say more light is converted with the textured surface. *G. TSM: Teaching, Suggestion, Motivation Test.*

Regarding claim 2, the prior art of Yu et al. disclose the integrated structure of claim 1, wherein the array is monolithically integrated with Si electronic devices (Yu shows in Fig. 5, where the noted pillars 200/300 are formed in a system that includes devices in a silicon substrate).

Regarding claim 8, the prior art of Yu et al. disclose the integrated structure of claim 1, and Yu discloses, in which the electrical contacts are configured to selectively provide electrical fields across at least some of the photodetectors (top electrode is 340, ¶ 0079, and bottom electrode is "The metal silicide layer 231 forms electrical contact to any electrical components of the substrate 230", ¶ 0048, and these noted electrodes provide access to electrical signal for all of the pillars 200/300).

Regarding claim 9, the prior art of Yu et al. disclose the integrated structure of claim 1, and Yu discloses, in which two or more of the photodetectors share one of the electrical contacts (see Fig. 5, where plural 200/300 share noted electrodes).

Regarding claim 12, the prior art of Yu et al. disclose the integrated structure of claim 1, in which each of at least some of the photodetectors is configured such that the light passes

through at least a part of the one of the P-doped region and N-doped region of the photodetector before reaching any part of the other doped region of the photodetector (the 200/300 above the circuitry below, and thus receive light first from external to the overall device system).

Claims 10 and 11are rejected under 35 U.S.C. 103 as being unpatentable over Yu et al. (US 2011/0309331) in view of Lunev et al. (US 2014/0016660, used to represent the provisional application 61/670,808 whose effective date is July 12, 2012) in view of Counil et al. (US 2010/0116332) in view of Arimoto et al. (US 5,759,292) in view of Martin et al. (US 7,276,749).

Regarding claims 10 and 11, the prior art of Yu et al. disclose the integrated structure of claim 1, and Yu does not specify,

"wherein the array monolithically integrated with Si electronic devices for signal processing and transmission",

"wherein the array is monolithically integrated with Si electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors".

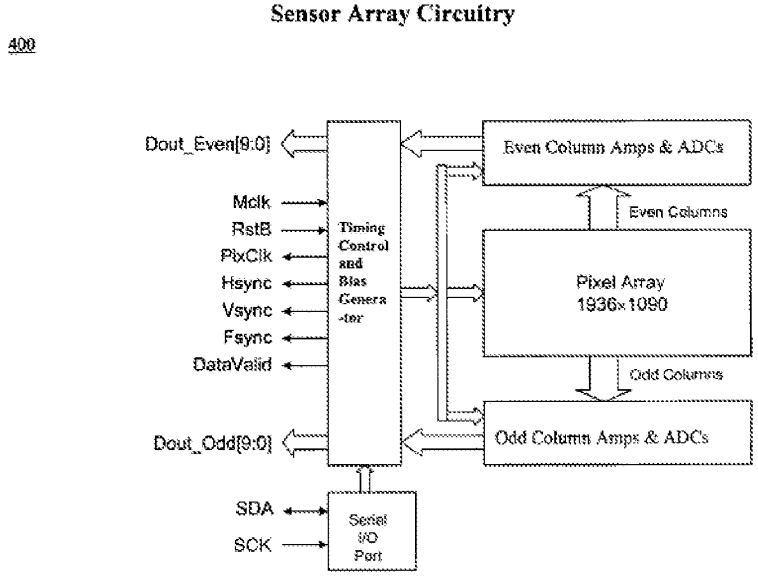


FIG. 1C

Martin discloses in Fig. 1C (provide above), wherein the array monolithically integrated with Si electronic devices for signal processing and transmission (the pixel array is supported by the signal processing elements “Even/Odd Column Amps & ADS’s” and “Timing Control and Bias Generator” and the transmission section “Serial I/O Port”),

wherein the array is monolithically integrated with Si electronic devices (Si devices already shown in ROIC of Yu) for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors (Martin discloses the pixel array is supported by the signal processing elements “Even/Odd Column Amps & ADS’s” and “Timing Control and Bias Generator” and the transmission section “Serial I/O Port”).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was effectively filed to use the,

"wherein the array monolithically integrated with Si electronic devices for signal processing and transmission",

"wherein the array is monolithically integrated with Si electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors", as disclosed by Martin in the system of Yu, for the purpose of providing the necessary device components to make the light signals gathered into usable electrical data signals and for distributing the gathered electrical data. *G. TSM: Teaching, Suggestion, Motivation Test.*

Claim 13 is rejected under 35 U.S.C. 103 as being unpatentable over Yu et al. (US 2011/0309331) in view of Lunev et al. (US 2014/0016660, used to represent the provisional application 61/670,808 whose effective date is July 12, 2012) in view of Counil et al. (US 2010/0116332) in view of Arimoto et al. (US 5,759,292) in view of Kim et al. (US 2011/0297214).

Regarding claim 13, the prior art of Yu et al. disclose the integrated structure of claim 1, and Yu discloses the opposite orientation to, "in which the doped regions of each of at least some of the photodetectors are configured such that the light passes through at least a part of the P-doped region before reaching any part of the N-doped region."

Kim et al. (US 2011/0297214) Fig. 2A (shown below) discloses the limitation of, in which the doped regions of each of at least some of the photodetectors are configured such that

the light passes through at least a part of the P-doped region before reaching any part of the N-doped region (where p-type is above the n-type part of the pillars).

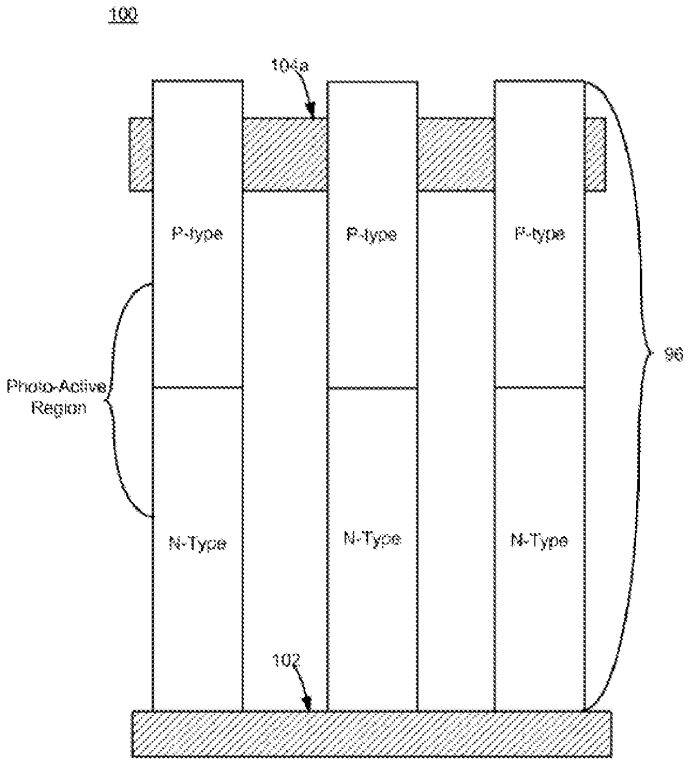


FIGURE 2A

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was effectively filed to use the,

"in which the doped regions of each of at least some of the photodetectors are configured such that the light passes through at least a part of the P-doped region before reaching any part of the N-doped region", as disclosed by Kim in the system of Yu, for the purpose of providing the practical construction of a light converting diode to create electrical signals from light signals. *G. TSM: Teaching, Suggestion, Motivation Test.*

Allowable Subject Matter

Claims 3-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 4-7 are objected to because of their dependency on claim 3.

Claims 14-17 are allowed.

The following is an Examiner's statement of reasons for allowance: The integrated structure as recited in the claims of the instant invention fail to be taught by the prior art cited of interest.

Regarding claim 14, the prior art of Yu et al. (US 2011/0309331) discloses in Figs. 4 and 5, a integrated photoconversion array, but fails to disclose the specific characteristic recited in the claims of the instant invention e.g. the combination of claimed features of an array of pillars comprising Si, Ge, and/or alloyed SiGe semiconductor material, the pillars comprise p-type and n-type doped regions for generating charge carriers, holes in the light receiving surface of at least some of the pillars, the holes are filled with solid dielectric material, side isolation, solid dielectric material forming a base dielectric region for the array, electrical contacts, the presence of holes increases absorption of light by factor of 1.1, and the array is monolithically integrated with electronic devices for signal processing and transmission, in conjunction with the feature of,

"each of the holes has an elongated shape extending in length over less than the width of the light receiving surface in which the hole is fabricated".

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo A Rodela whose telephone number is (571)272-8797. The examiner can normally be reached M-F, 8:30-5:00pm ET.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yara B Green can be reached on (571) 270-3035. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/EDUARDO A RODELA/
Primary Examiner, Art Unit 2893

Notice of References Cited	Application/Control No. 18/822,880	Applicant(s)/Patent Under Reexamination WANG et al.	
	Examiner Eduardo A Rodela	Art Unit 2893	Page 1 of 1

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*	B	US-20130125965-A1	2013-05-23	Hazeghi; Arash	H01L31/18	438/57
*	C	US-20120196401-A1	2012-08-02	Graham; William	H01L31/035227	977/840
*	D	US-9263519-B2	2016-02-16	Lal; Amit	B82Y10/00	1/1
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	J					
	K					
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	18/822,880	WANG et al.
	Examiner	Art Unit
	Eduardo A Rodela	2893

CPC - Searched*		
Symbol	Date	Examiner
H01L31/02019; H01L31/022408; H01L31/02327; H01L31/02363; H01L31/028; H01L31/035281; H01L31/105; H01L31/107; H01L31/0236,02363,0352	11/14/2024	EAR

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PE2E search - see history for complete details	11/14/2024	EAR
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US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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	First Named Inventor	Shih-Yuan WANG
	Art Unit	
	Examiner Name	
	Attorney Docket Number	309-0015USCIPDIV

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	11309444		2022-04-19	Wang et al.	
	2	8558336		2013-10-15	Su	
	3	10411053		2019-09-10	Yokogawa	
	4	10522582		2019-12-31	Maruyama et al.	
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	8	7525170		2009-04-28	Hsu	

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	Examiner Name	
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	10	8357960		2013-01-22	Dutta	
	11	8946675		2015-02-03	Yu	
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	13	11211419		2021-12-28	Wu	
	14	11728457		2023-08-15	Sung	

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	1	20100320444		2010-12-23	Dutta	
	2	20110309331		2011-12-22	Yu et al.	
	3	20180182806		2018-06-28	Jin et al.	

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	First Named Inventor	Shih-Yuan WANG
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	Examiner Name	
	Attorney Docket Number	309-0015USCIPDIV

	4	20110156195		2011-06-30	Tivarus et al.	
	5	20120153127		2012-06-21	Hirigoyen et al.	
	6	20180012918		2018-01-11	Na et al.	
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	10	20160240579		2016-08-18	Sun et al.	
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	13	20200006407		2020-01-02	Yokogawa	
	14	20200006416		2020-01-02	Baba et al.	

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	Art Unit	
	Examiner Name	
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	15	20050145779		2005-07-07	Mochizuki et al.	
	16	20120153416		2012-06-21	Tanaka et al.	

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	5	09040854	EP		1999-09-08	IBM United Kingdom Limited		☐
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	7	103956403	CN		2017-02-15	Suzhou Beipeng Photoelectric Technology Co. Ltd.		☐

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	1	Copy of International Search Report and Written Opinion for PCT/US2020/051733 mailed December 17, 2020.	☐
	2	Copy of Written Opinion of International Search Report for PCT/US2020/051733 dated December 17, 2020.	☐
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	Filing Date	
	First Named Inventor	Shih-Yuan WANG
	Art Unit	
	Examiner Name	
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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2024-09-03
Name/Print	Ivan S. Kavrukov	Registration Number	25,161

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Samsung v. W&Wsens - IPR2025-00993

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L2	3	((("W&W") near3 ("SENS") near3 ("DEVICES") near3 ("INC"))).AS,AANM.	(US-PGPUB; USPAT)	OR	ON	ON	2024/11/08 02:38 PM
L3	862	((("WANG") near3 ("Shih-Yuan")) OR (("WANG") near3 ("Shih-Ping"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2024/11/08 02:39 PM
L5	83304	(H01L31/02019 OR H01L31/022408 OR H01L31/02327 OR H01L31/02363 OR H01L31/028 OR H01L31/035281 OR H01L31/105 OR H01L31/107).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/08 02:40 PM
L6	2267779	(light OR infrared OR "IR") WITH (pillar OR column$2 OR cylinder)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/08 02:41 PM
L7	30593495	(aperture$1 OR gaps OR void OR divot)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO,	OR	ON	ON	2024/11/08 02:59 PM

			RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L9	191	("20050092925"|"20050184354"|"20070092192"|"20070190434"|"20080047604"|"20080218740"|"20080248608"|"20080265449"|"20081012582"|"20090188557"|"20090267049"|"20100029067"|"20100126548"|"20100193768"|"20100197068"|"20100221866"|"20100313941"|"20120193676"|"20120292676"|"20130207222"|"20140001528"|"20150041965"|"20160225631"|"4571559"|"4637129"|"4716449"|"5451767"|"5457327A"|"5625636"|"5757057"|"5886374"|"6027956"|"6177289"|"6667528"|"7115971"|"7397101"|"7495306"|"7601597"|"7674563"|"7772615"|"7795064"|"7893348"|"7898052"|"7972934"|"8114695"|"8129710"|"8436370"|"8357960"|"20050092925"|"20050184354"|"20060218740"|"20070092192"|"20080265449"|"20090188557"|"20100126548"|"20100193766"|"20100197068"|"4637129"|"5457327"|"7115971"|"7397101"|"7501597"|"7674563"|"7795064"|"7893346"|"8129710"). PN.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/08 03:14 PM
L10	101	("20070190434"|"20080047604"|"20080248608"|"20081012582"|"20090267049"|"20100029067"|"20100221866"|"20100313941"|"20120193676"|"20120292676"|"20130207222"|"20140001528"|"20150041965"|"20160225631"|"4571559"|"4716449"|"5451767"|"5625636"|"5757057"|"5886374"|"6027956"|"61	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA,	OR	ON	ON	2024/11/08 03:15 PM

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		77289"|"6667528"|"7495306"|"7772615"|"7898052"|"7972934"|"8114695"|"8357960"|"8436370").PN.	VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L12	1	"20070007621"	(US-PGPUB)	OR	ON	ON	2024/11/12 12:42 PM
L14	31331	H01L31/0236,02363,0352.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/12 04:50 PM
L15	94829	L5 OR L14	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/12 04:51 PM
L16	1103	(@rlpd<="20131115" OR @rlad<="20131115" OR @pd<="20131115" OR @ad<="20131115") AND L15 AND L7 AND L6	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/12 04:52 PM
L17	390	(@rlpd<="20131115"	(US-PGPUB; USPAT;	OR	ON	ON	2024/11/12

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		OR @rlad<="20131115" OR @pd<="20131115" OR @ad<="20131115") AND L15 AND L7 AND L6	USOCR)				04:52 PM
L18	508	("1918848" | "3903427" | "4017332" | "4292512" | "4316048" | "4357415" | "4387265" | "4394571" | "4400221" | "4443890" | "4513168" | "4531055" | "4620237" | "4678772" | "4827335" | "4846556" | "4857973" | "4876586" | "4880613" | "4896941" | "4950625" | "4971928" | "4972244" | "4990988" | "5071490" | "5081049" | "5096520" | "5124543" | "5217911" | "5247349" | "5272518" | "5311047" | "5347147" | "5362972" | "5374841" | "5391896" | "5401968" | "5449626" | "5468652" | "5602661" | "5612780" | "5671914" | "5696863" | "5723945" | "5747796" | "5767507" | "5798535" | "5844290" | "5853446" | "5857053" | "5877492" | "5880495" | "5885881" | "5900623" | "5943463" | "5968528" | "6013871" | "6033582" | "6037243" | "6046466" | "6074892" | "6100551" | "6270548" | "6301420" | "6326649" | "6388243" | "6388648" | "6407439" | "6459034" | "6463204" | "6542231" | "6563995" | "6566723" | "6680216" | "6709929" | "6720594" | "6771314" | "6805139" | "6812473" | "6904187" | "6927145" | "6960526" | "6967120" | "6969899" | "6987258" | "6996147" | "7052927" | "7064372" | "7105428" | "7106938" | "7109517" | "7153720" | "7163659" | "7192533" | "7208783" | "7230286" | "7235475" | "7241434" | "7253017" | "7254151" | "7262400" | "7265328"	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/12 05:05 PM

		| "7272287" | "7285812" | "7306963" | "7307327" | "7311889" | "7326915" | "7330404" | "7335962" | "7336860" | "7339110" | "7358583" | "7381966" | "7388147" | "7416911" | "7446025" | "7462774" | "7471428" | "7491269" | "7507293" | "7521322" | "7524694" | "7582587" | "7582857" | "7598482" | "7622367" | "7626685" | "7646138" | "7646943" | "7647695" | "7649665" | "7655860" | "7663202" | "7692860" | "7704806" | "7713779" | "7719678" | "7719688" | "7732769" | "7732839" | "7736954" | "7740824" | "7790495" | "7872324" | "7888155" | "7902540" | "7948555" | "8030729" | "8035184" | "8049203" | "8063450" | "8067299" | "8067736" | "8084728" | "8093675" | "8118170" | "8143658" | "8154127" | "8193524" | "8208776" | "8212136" | "8212138" | "8222705" | "8242353" | "8269985" | "8274039" | "8299472" | "8330090" | "8384007" | "8455857" | "8471190" | "8514411" | "8546742" | "8748799" | "8766272" | "8791470" | "8810808" | "8835831" | "8866065" | "9000353" | "20020003201" | "20020020846" | "20020021879" | "20020071468" | "20020104821" | "20020109082" | "20020117675" | "20020130311" | "20020172820" | "20030003300" | "20030006363" | "20030077907" | "20030089899" | "20030103744" | "20030132480" | "20030160176" | "20030189202" | "20030227090" |					

		"20040011975" | "20040021062" | "20040026684" | "20040058058" | "20040065362" | "20040075464" | "20040095658" | "20040109666" | "20040114847" | "20040118337" | "20040118377" | "20040122328" | "20040124366" | "20040155247" | "20040156610" | "20040160522" | "20040180461" | "20040213307" | "20040217086" | "20040223681" | "20040241965" | "20040252957" | "20040261840" | "20050009224" | "20050035381" | "20050082676" | "20050087601" | "20050095699" | "20050109388" | "20050116271" | "20050133476" | "20050161662" | "20050164514" | "20050190453" | "20050201704" | "20050218468" | "20050224707" | "20050242409" | "20050284517" | "20060011362" | "20060027071" | "20060038990" | "20060113622" | "20060115230" | "20060121371" | "20060146323" | "20060162766" | "20060180197" | "20060208320" | "20060257071" | "20060260674" | "20060273262" | "20060273389" | "20060284118" | "20070012980" | "20070012985" | "20070023799" | "20070025504" |				

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		"20070029545" | "20070052050" | "20070076481" | "20070082255" | "20070099292" | "20070104441" | "20070107773" | "20070108371" | "20070114622" | "20070120254" | "20070126037" | "20070137697" | "20070138376" | "20070138380" | "20070138459" | "20070139740" | "20070140638" | "20070145512" | "20070148599" | "20070152248" | "20070155025" | "20070164270" | "20070170418" | "20070172623" | "20070172970" | "20070187787" | "20070196239" | "20070200054" | "20070205483" | "20070217754" | "20070228421" | "20070238265" | "20070238285" | "20070241260" | "20070246689" | "20070248958" | "20070272828" | "20070278500" | "20070285378" | "20070290193" | "20070290265" | "20080001498" | "20080006319" | "20080006891" | "20080029701" | "20080036038" | "20080044984" | "20080047601" | "20080047604" | "20080055451" | "20080065451" | "20080073742" | "20080079022" | "20080079076" | "20080083963" | "20080088014" | "20080090401" | "20080092938" |				

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		"20080096308" | "20080108170" | "20080116537" | "20080128760" | "20080137188" | "20080143906" | "20080145965" | "20080149914" | "20080149944" | "20080157253" | "20080166883" | "20080169017" | "20080169019" | "20080173615" | "20080178924" | "20080188029" | "20080191278" | "20080191298" | "20080211945" | "20080218740" | "20080224115" | "20080225140" | "20080233280" | "20080237568" | "20080246020" | "20080246123" | "20080248304" | "20080251780" | "20080258747" | "20080260225" | "20080264478" | "20080266556" | "20080266572" | "20080271783" | "20080277646" | "20080283728" | "20080283883" | "20080297281" | "20080311693" | "20080311712" | "20090001498" | "20090020150" | "20090020687" | "20090032687" | "20090046362" | "20090046749" | "20090050204" | "20090052029" | "20090057650" | "20090072145" | "20090104160" | "20090120498" | "20090121136" | "20090127442" | "20090146198" | "20090151782" | "20090152664" | "20090153961" |				

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		"20090165844" | "20090173976" | "20090179225" | "20090179289" | "20090188552" | "20090189144" | "20090189145" | "20090194160" | "20090199597" | "20090201400" | "20090206405" | "20090211622" | "20090223558" | "20090224245" | "20090224349" | "20090230039" | "20090233445" | "20090242018" | "20090243016" | "20090244514" | "20090260687" | "20090261438" | "20090266418" | "20090266974" | "20090272423" | "20090278998" | "20090289320" | "20090305454" | "20100006817" | "20100019252" | "20100019296" | "20100019355" | "20100025710" | "20100078055" | "20100078056" | "20100090341" | "20100101633" | "20100104494" | "20100110433" | "20100116976" | "20100126573" | "20100127153" | "20100132779" | "20100133986" | "20100136721" | "20100148221" | "20100163714" | "20100163941" | "20100178018" | "20100186809" | "20100187404" | "20100200065" | "20100207103" | "20100218816" | "20100229939" | "20100230653" | "20100237454" | "20100240104" |				

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		"20100244108" | "20100244169" | "20100249877" | "20100258184" | "20100276572" | "20100277607" | "20100282314" | "20100295019" | "20100302440" | "20100304061" | "20100308214" | "20100313952" | "20100319763" | "20100320444" | "20110018424" | "20110036396" | "20110037133" | "20110049572" | "20110050042" | "20110057231" | "20110057234" | "20110057286" | "20110080508" | "20110084212" | "20110127490" | "20110133060" | "20110133160" | "20110135814" | "20110139176" | "20110146771" | "20110147870" | "20110180894" | "20110195577" | "20110220191" | "20110226937" | "20110248315" | "20110249219" | "20110249322" | "20110253982" | "20110272014" | "20110297214" | "20110309237" | "20110309240" | "20110309331" | "20110315988" | "20110316106" | "20120006390" | "20120009714" | "20120014837" | "20120029328" | "20120031454" | "20120060905" | "20120075513" | "20120153124" | "20120192939" | "20120196383" | "20120196401" | "20120240999" |				

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		"20120258563" | "20120280345" | "20120298843" | "20120313078" | "20120318336" | "20120322164" | "20130000704" | "20130020620" | "20130037100" | "20130112256" | "20130125965" | "20130174904" | "20130220406" | "20130341749" | "20140045209" | "20140096816" | "20140117401" | "20150171272").pn. AND (PGPB | USPT | USOC).dbnm.					
L19	1	"9312448".pn.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/13 09:38 AM
L20	385	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L15 AND L7 AND L6	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/13 10:43 AM
L21	38	("6946682" | "7601993" | "7923753" | "8525227" | "8604511" | "8735941" | "8941146" | "8969198" | "9660043" | "20020142548" | "20070187677" | "20080173898" | "20080217625" | "20080258150" | "20090035884" | "20090127575" | "20090212276" | "20100059781" | "20110018024" | "20110143507" | "20110198641" | "20110233520" | "20110233596" | "20120049152" | "20120119189" | "20120235204" | "20120248500" | "20130026519" | "20130320352" | "20140016660" | "20140264454").pn. OR ("9793439").urpn. AND	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/13 10:51 AM

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		(PGPB | USPT | USOC).dbnm.					
L22	36	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L21	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/13 10:52 AM
L23	1	"20110309331"	(US-PGPUB)	OR	ON	ON	2024/11/14 09:38 AM
L24	1	"20140016660"	(US-PGPUB)	OR	ON	ON	2024/11/14 02:11 PM
L25	212	(texture OR recesses OR divots OR holes) WITH surface WITH (diode) WITH (absorb$3 OR absorption OR efficiency) WITH light	(US-PGPUB)	OR	ON	ON	2024/11/14 02:34 PM
L26	277	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L25	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 02:34 PM
L27	1974	(textur$3 OR texturized) WITH (("1" OR "10" OR "20" OR "30 OR "40 OR "50") NEAR (nanometer$1 OR "nm"))	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 03:29 PM
L28	245	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L27 AND L14	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/14 03:30 PM
L29	76	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L27 AND L14	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 03:30 PM
L30	590	(textur$3 OR texturized) WITH surface WITH (increas$3 NEAR	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 04:11 PM

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		(efficiency OR absorb$3 OR absorption))					
L31	78	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND L14	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 04:11 PM
L32	36	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND L14 AND (percent$3 OR "%")	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 04:13 PM
L33	0	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND (L14 SAME (percent$3 OR "%"))	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 04:13 PM
L34	0	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L30 AND (L14 SAME (percent$3 OR "%"))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/14 04:14 PM
L35	7573011	(signal NEAR process$3) AND (output OR transmission)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/11/14 04:36 PM

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L36	244	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND L14 AND L35	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 04:37 PM
L37	4526	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND (cmos NEAR imager) AND L35	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 04:44 PM
L38	747	(@rlpd<="20130613" OR @rlad<="20130613" OR @pd<="20130613" OR @ad<="20130613") AND (cmos NEAR imager) AND ((signal NEAR process$3) AND (output OR transmission)) AND monolithic$4	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2024/11/14 04:44 PM
L39	0	(L2 OR L3 OR L15) AND ((integrated NEAR structure)(array)(pillars)(holes)(p-doped)(n-doped)(light NEAR receiving NEAR surfaces)(visible)(infrared)(wavelengths)(photosensitive NEAR area)(charge NEAR carriers)(holes)(recesses)(side NEAR isolation)(base NEAR dielectric)(electrical NEAR contacts)(factor)(increase)(abosorption)("1.1")).clm.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2024/11/14 05:22 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

Attorney Docket No.: 309-0015USCIPDIV **PATENT**
Confirmation No.: 5818

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Shih-Yuan WANG Application No.: 18/822,880 Filed: September 3, 2024 Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	Examiner: EDUARDO A RODELA Art Unit: 2893 **CERTIFICATE OF TRANSMISSION** I hereby certify that this correspondence is being submitted through the USPTO Electronic Filing Service addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 /Mary Ellen Finnegan/ Date: November 18, 2024 Name: Mary Ellen Finnegan

VIA EFS-Web
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

It is respectfully requested that the documents listed on the attached Information Disclosure Citation form PTO/SB/08a be considered by the Patent Examiner in connection with the above-identified application and be made of record therein.

Independent consideration and acknowledgement of the enclosed document are respectfully requested.

The Commissioner is hereby authorized to charge U.S. PTO Deposit Account 600125 any payment due and to credit any overpayment thereto.

Respectfully submitted,

/Ivan S. Kavrukov/
Ivan S. Kavrukov
Registration No. 25,161
Attorney for Applicant

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001
Attorney's Telephone No.: 917-945-0121
Attorney's E-mail: ikavrukov@wissingmiller.com

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	18822880
	Filing Date	2024-09-03
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIPDIV

U.S.PATENTS Remove

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20080083963		2008-04-10	Hsu	

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	18822880
	Filing Date	2024-09-03
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIPDIV

	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	18822880
	Filing Date	2024-09-03
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2893
	Examiner Name	EDUARDO A RODELA
	Attorney Docket Number	309-0015USCIPDIV

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2024-11-18
Name/Print	Ivan S. Kavrukov	Registration Number	25,161

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Samsung Exhibit 1090, Page 342 of 786
Samsung v. W&Wsens - IPR2025-00993

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
18/822,880	**11/18/2024 01:48:39 PM Z ET**	**309-0015USCIPDIV**

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	68003337	FILING DATE	09/03/2024
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV_IDSTransmittal-Final.pdf	1	Transmittal Letter	446 KB
309-0015USCIPDIV_1449-Final.pdf	4	Information Disclosure Statement (IDS) Form (SB08)	1010 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
309-0015USCIPDIV_IDSTransmittal-Final.pdf	BBBC9ADD8C833A72A2D351F384B1286893606CC11F4FEED79FA801DD068A7381310DF936C33CE4C327CDFA69984DC04D600646B4107A66985EF7FA5DA27DFC39

309-0015USCIPDIV_1449-Final.pdf

BBAB28011A89FD0AE2EC6E41C6EDE85C82FBAB494A37EAD386F1DB469484D4148247AC44C214C24498A14EE398452985EA5068B3F124F216D6F8ED4C1B3E3334

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
18/822,880	**10/31/2024 04:04:48 PM Z ET**	**309-0015USCIPDIV**

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	67799981	FILING DATE	09/03/2024
CUSTOMER #	139982	FIRST NAMED INVENTOR	Shih-Yuan WANG
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV_SecondPreliminary Amendment-Final.pdf	6	Preliminary Amendment	496 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
309-0015USCIPDIV_SecondPreliminary Amendment-Final.pdf	7066265F1E919EC95FE66C4CA20E8B613EE267CF34BB447941B3387A71C6BC77970325D8EA990F3EE087557AEFEC13E6CD085B7B13821A7DF60125EB4A483A2F

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Shih-Yuan WANG et al.
Serial No.:	18/822,880
Examiner:	EDUARDO A RODELA
Group Art Unit	2893
Filing Date:	09/03/2024
For:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
Conf. No.	5818

Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, New York 10001

CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: October 31, 2024

I hereby certify that this correspondence is being transmitted via Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

SECOND PRELIMINARY AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Prior to examination and the issuance of the first Office Action, please amend the above-identified application as follows:

Amendments to the Claims:

Please rewrite the claims as follows. These amended claims replace all previously filed claims:

1. (currently amended) An integrated structure comprising:

an array of pillars comprising ~~SI~~Si, Ge, and/or SiGe alloy semiconductor material, wherein at least some of the pillars are configured ~~as~~ to include photodetectors ~~that~~ and have respective light-receiving surfaces and respective sides;

wherein at least some of the ~~photodetectors~~ pillars comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;

one or more holes that are ~~deliberately formed~~fabricated as recesses at or under the light-receiving surface of each of at least some of the ~~photodetectors~~pillars, have elongated or other shapes at or parallel to the light-receiving surfaces, extend into the ~~photodetectors~~ pillars to a depth of 100 to10000 nm, and are filled at least partly with solid dielectric material;

side-isolation comprising solid material between at least portions of the sides of at least some of the ~~photodetectors~~pillars;

a solid dielectric material forming a base dielectric region for the array;

electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;

wherein the presence of said one or more holes increases by a factor of at least 1.1 the absorption of the light by at least some of the photodetectors relative to like photodetectors lacking said holes.

2. (currently amended) The integrated structure of claim 1, wherein the array ~~of~~ ~~photodetectors~~ is monolithically integrated with ~~SI~~ Si electronic devices.

3. (currently amended) The integrated circuit of claim 1, in which at least some of the holes are elongated along the respective light-receiving surfaces.

4. (currently amended) The integrated structure of claim 3, wherein each of at least some of the ~~photodetectors~~ pillars has a plurality of the elongated holes.

5. (currently amended) The integrated structure of claim 3, wherein each of at least some of the ~~photodetectors~~ pillars has only one of the elongated holes.

6. (currently amended) The integrated structure of claim 3, in which the light-receiving surfaces have respective widths, and the elongated holes extend along less than the widths of the light-receiving surfaces of at least some of the ~~photodetectors~~pillars in which the holes are fabricated.

7. (currently amended) The integrated structure of claim 6 in which each of at least some of the elongated holes has at least one closed contour remote from respective side edges of the light-receiving surface in which the hole is fabricated ~~surfaces of at least some of the photodetectors~~.

8. (previously presented) The integrated structure of claim 1, in which the electrical contacts are configured to selectively provide electrical fields across at least some of the photodetectors.

9. (previously presented) The integrated structure of claim 1, in which two or more of the photodetectors share one of the electrical contacts.

10. (currently amended) The integrated structure of claim 1, wherein the array ~~of~~ ~~photodetectors~~ is monolithically integrated with ~~SI~~ Si electronic devices for signal processing and transmission.

11. (currently amended) The integrated structure of claim 1, wherein the array ~~of photodetectors~~ is monolithically integrated with ~~SI~~ Si electronic devices for transmitting electrical signals related to accumulations of the charge carriers in at least some of the photodetectors.

12. (currently amended) The integrated structure of claim 1, in which each of at least some of the photodetectors is configured ~~the doped regions of each of at least some of the photodetectors are configured~~ such that the light passes through at least a part of the one of the P-doped region and N-doped region of the photodetector before reaching any part of the ~~N-~~ other doped region of the photodetector.

13. (currently amended) The integrated structure of claim 1, in which the doped regions of each of at least some of the photodetectors are configured such that the light passes through at least a part of the ~~N~~P-doped region before reaching any part of the N~~P~~-doped region.

14. (currently amended) An integrated structure comprising:

an array of pillars comprising ~~SI~~Si, Ge, and/or alloyed SiGe semiconductor material, wherein at least some of the pillars ~~are configured as photodetectors that~~ have respective sides and respective light-receiving surfaces with selected widths and comprise at least one photodetector;

wherein at least some of the ~~photodetectors~~ pillars comprise P-doped and N-doped regions and are configured to respond to illumination with light in selected visible and infrared wavelengths by generating electrical charge carriers;

one or more holes that are ~~deliberately formed~~fabricated as recesses at or under the light-receiving surface of each of at least some of the ~~photodetectors~~pillars,

wherein each of the holes (i) has an elongated shape extending in length over less than the width of the light-receiving surface in which the hole is

~~formed~~fabricated, (ii) has at least one closed contour at the light-receiving surface in which the hole is ~~formed~~fabricated, (ii) extends into the ~~photodetector~~ pillar in which the hole is ~~formed~~ fabricated to a depth of 100 to10000 nm, and (iv) is filled at least partly with solid dielectric material;

side-isolation comprising solid material between at least portions of the sides of at least some of the ~~photodetectors~~pillars;

a solid dielectric material forming a base dielectric region for the array;

electrical contacts configured to provide electrical pathways coupled electrically to at least some of the photodetectors, including for selected reverse-biasing thereof;

wherein the presence of the one or more holes increases, by a factor of at least 1.1, absorption of the light by at least some of the photodetectors relative to like photodetectors lacking the holes; and

wherein the array ~~of photodetectors~~ is monolithically integrated with ~~SI~~ Si electronic devices for signal processing and transmission.

15. (currently amended) The integrated structure of claim 14, in which each of at least some of the ~~photodetectors~~ pillars has only one of the elongated holes fabricated therein.

~~15~~ 16. (new) The integrated structure of claim 14, in which each of at least some of the pillars has at least two of the elongated holes.

~~16~~ 17. (new) The integrated structure of claim 14, in which each of at least some of the photodetectors includes at least one of the holes.

REMARKS

This patent application is a divisional of and incorporates by reference parent application Ser. Nos. 18/385,213 filed October 30, 2023, which is expected to issue as U.S. Patent No. 12,087,871 on September 10, 2024, according to Issue Notification dated 08/21/2024.

Applicant submits that the same examples of support discussed in the immediate parent application apply to the claims above, which are entitled to the same 2014 and 2013 filing dates through the same chain of continuing applications as the immediate parent of which the subject application is a division.

Applicant invites the Examiner to telephone the undersigned if it appears that a call may help advance prosecution.

Please charge any shortfall and credit any overpayments to our Deposit Account number 600125.

Respectfully Submitted,

WISSING MILLER LLP
Attorney for Applicants
By: /Ivan S. Kavrukov/
Ivan S. Kavrukov
Reg. No. 25,161
Tel.: (917) 945-0121

REMARKS

This patent application is a divisional of and incorporates by reference parent application Ser. Nos. 18/385,213 filed October 30, 2023, which is expected to issue as U.S. Patent No. 12,087,871 on September 10, 2024, according to Issue Notification dated 08/21/2024.

Applicant submits that the same examples of support discussed in the immediate parent application apply to the claims above, which are entitled to the same 2014 and 2013 filing dates through the same chain of continuing applications as the immediate parent of which the subject application is a division.

Applicant invites the Examiner to telephone the undersigned if it appears that a call may help advance prosecution.

Please charge any shortfall and credit any overpayments to our Deposit Account number 600125.

Respectfully Submitted,

WISSING MILLER LLP
Attorney for Applicants
By: /Ivan S. Kavrukov/
Ivan S. Kavrukov
Reg. No. 25,161
Tel.: (917) 945-0121

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 18/822,880	Filing Date 09/03/2024	☐ To be Mailed

ENTITY: ☐ LARGE ☑ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $40 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $ 192 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	10/31/2024	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 17	Minus	** 20	= 0		x $40 =	0
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $ 192 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/CAROLYN E THOMAS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
18/822,880	09/03/2024	Shih-Yuan WANG	309-0015USCIPDIV	5818

139982 7590 10/28/2024

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER	
CENTRAL, DOCKET	

ART UNIT	PAPER NUMBER
OPAP	

NOTIFICATION DATE	DELIVERY MODE
10/28/2024	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

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Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

In re Application of	:	
WANG et al.	:	
Application No. 18/822,880	:	
Filed: September 3, 2024	:	DECISION ON PETITION
For: MICROSTRUCTURE ENHANCED	:	
ABSORPTION PHOTOSENSITIVE	:	
DEVICES	:	

This is a decision on the petition under 37 CFR 1.102(c)(1), filed September 3, 2024, to make the above-identified application special based on applicant's age as set forth in MPEP § 708.02, Section II.

The petition is **GRANTED**.

A grantable petition to make an application special under 37 CFR 1.102(c)(1) and MPEP § 708.02, Section II: Applicant's Age, must be accompanied by evidence showing that the applicant is 65 years of age, or more, such as applicant's statement or a statement from a registered practitioner that he or she has evidence that the applicant is 65 years of age or older. No fee is required.

The instant petition includes a statement from the registered attorney or agent attesting to having evidence of the joint inventor's age being 65 years of age or more. Accordingly, the above-identified application has been accorded "special" status.

Telephone inquiries concerning this decision should be directed to Paralegal Specialist Lara Willsey at 571-270-1501. All other inquiries concerning the examination or status of the application are accessible in the Patent Center at https://patentcenter.uspto.gov.

/Lara C. Willsey/
Lara C. Willsey
Paralegal Specialist
Office of Petitions

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
18/822,880	09/03/2024	OPAP	992	309-0015USCIPDIV	15	2

CONFIRMATION NO. 5818

REPLACEMENT FILING RECEIPT

139982
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

Date Mailed: 09/20/2024

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Inventor(s)

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping WANG, Los Altos, CA;

Applicant(s)

W&W Sens Devices, Inc., Los Altos, CA;

Power of Attorney: The patent practitioners associated with Customer Number 139982

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and is a CIP of PCT/US2018/057963 10/29/2018

Samsung Exhibit 1090, Page 357 of 786
Samsung v. W&Wsens - IPR2025-00993

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and claims benefit of 62/521,504 06/18/2017

and claims benefit of 62/522,169 06/20/2017
and claims benefit of 62/527,962 06/30/2017
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and claims benefit of 62/540,524 08/02/2017
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and claims benefit of 62/556,426 09/10/2017
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and said 16/042,535 07/23/2018 is a CIP of 15/797,821 10/30/2017 PAT 10,446,700
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and claims benefit of 62/547,728 08/18/2017
and claims benefit of 62/553,844 09/02/2017
and claims benefit of 62/556,426 09/10/2017
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and claims benefit of 62/607,860 12/19/2017
and claims benefit of 62/615,314 01/09/2018
and claims benefit of 62/623,971 01/30/2018
and claims benefit of 62/628,764 02/09/2018
and claims benefit of 62/631,630 02/17/2018
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and claims benefit of 62/646,871 03/22/2018
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and claims benefit of 62/651,087 03/31/2018
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and claims benefit of 62/662,217 04/24/2018
and claims benefit of 62/666,005 05/02/2018
and claims benefit of 62/669,194 05/09/2018
and claims benefit of 62/675,130 05/22/2018
and claims benefit of 62/677,609 05/29/2018
and claims benefit of 62/682,909 06/09/2018
and said 15/309,922 11/09/2016 is a 371 of PCT/US2015/061120 11/17/2015
and is a CON of 14/943,898 11/17/2015 PAT 9,530,905

and is a CON of 14/945,003 11/18/2015 PAT 9,525,084
which claims benefit of 62/232,716 09/25/2015
and claims benefit of 62/213,558 09/02/2015
and claims benefit of 62/209,311 08/24/2015
and claims benefit of 62/205,717 08/15/2015
and claims benefit of 62/199,607 07/31/2015
and claims benefit of 62/197,120 07/27/2015
and claims benefit of 62/188,876 07/06/2015
and claims benefit of 62/182,602 06/21/2015
and claims benefit of 62/175,855 06/15/2015
and claims benefit of 62/174,498 06/11/2015
and claims benefit of 62/171,915 06/05/2015
and claims benefit of 62/157,876 05/06/2015
and claims benefit of 62/154,675 04/29/2015
and claims benefit of 62/153,443 04/27/2015
and claims benefit of 62/139,511 03/27/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/100,025 01/05/2015
and claims benefit of 62/090,879 12/11/2014
and claims benefit of 62/081,538 11/18/2014
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and claims benefit of 62/213,556 09/02/2015
and claims benefit of 62/209,311 08/24/2015
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and said 14/947,718 11/20/2015 is a CON of PCT/US2014/039208 05/22/2014
which claims benefit of 61/826,446 05/22/2013
and claims benefit of 61/843,021 07/04/2013
and claims benefit of 61/905,109 11/15/2013
and claims benefit of 61/834,873 06/13/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the Patent Prosecution Highway program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 09/12/2024

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 18/822,880**

Projected Publication Date: 12/26/2024

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Preliminary Class

136

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

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For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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Samsung v. W&Wsens - IPR2025-00993

community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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OC00000007983380

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and claims benefit of 62/509,093 05/20/2017
and claims benefit of 62/510,249 05/23/2017
and claims benefit of 62/514,889 06/04/2017
and claims benefit of 62/521,504 06/18/2017

and claims benefit of 62/522,169 06/20/2017
and claims benefit of 62/527,962 06/30/2017
and claims benefit of 62/530,281 07/09/2017
and claims benefit of 62/533,078 07/16/2017
and claims benefit of 62/533,603 07/17/2017
and claims benefit of 62/535,801 07/21/2017
and claims benefit of 62/540,524 08/02/2017
and claims benefit of 62/542,243 08/07/2017
and claims benefit of 62/547,728 08/18/2017
and claims benefit of 62/553,844 09/02/2017
and claims benefit of 62/556,426 09/10/2017
and claims benefit of 62/561,869 09/22/2017
and said 16/528,958 08/01/2019 is a CON of 15/797,821 10/30/2017 PAT 10,446,700
and said 16/042,535 07/23/2018 is a CIP of 15/797,821 10/30/2017 PAT 10,446,700
and claims benefit of 62/535,801 07/21/2017
and claims benefit of 62/540,524 08/02/2017
and claims benefit of 62/542,243 08/07/2017
and claims benefit of 62/547,728 08/18/2017
and claims benefit of 62/553,844 09/02/2017
and claims benefit of 62/556,426 09/10/2017
and claims benefit of 62/561,869 09/22/2017
and claims benefit of 62/591,072 11/27/2017
and claims benefit of 62/599,246 12/15/2017
and claims benefit of 62/607,860 12/19/2017
and claims benefit of 62/615,314 01/09/2018
and claims benefit of 62/623,971 01/30/2018
and claims benefit of 62/628,764 02/09/2018
and claims benefit of 62/631,630 02/17/2018
and claims benefit of 62/633,514 02/21/2018
and claims benefit of 62/634,692 02/23/2018
and claims benefit of 62/637,945 03/02/2018
and claims benefit of 62/639,356 03/06/2018
and claims benefit of 62/639,472 03/06/2018
and claims benefit of 62/639,920 03/07/2018
and claims benefit of 62/640,522 03/08/2018
and claims benefit of 62/643,010 03/14/2018
and claims benefit of 62/645,810 03/21/2018
and claims benefit of 62/646,871 03/22/2018
and claims benefit of 62/651,053 03/30/2018
and claims benefit of 62/651,087 03/31/2018
and claims benefit of 62/652,830 04/04/2018
and claims benefit of 62/659,067 04/17/2018
and claims benefit of 62/659,072 04/17/2018
and claims benefit of 62/662,217 04/24/2018
and claims benefit of 62/666,005 05/02/2018
and claims benefit of 62/669,194 05/09/2018
and claims benefit of 62/675,130 05/22/2018
and claims benefit of 62/677,609 05/29/2018
and claims benefit of 62/682,909 06/09/2018
and said 15/309,922 11/09/2016 is a 371 of PCT/US2015/061120 11/17/2015
and is a CON of 14/943,898 11/17/2015 PAT 9,530,905

and is a CON of 14/945,003 11/18/2015 PAT 9,525,084
which claims benefit of 62/232,716 09/25/2015
and claims benefit of 62/213,558 09/02/2015
and claims benefit of 62/209,311 08/24/2015
and claims benefit of 62/205,717 08/15/2015
and claims benefit of 62/199,607 07/31/2015
and claims benefit of 62/197,120 07/27/2015
and claims benefit of 62/188,876 07/06/2015
and claims benefit of 62/182,602 06/21/2015
and claims benefit of 62/175,855 06/15/2015
and claims benefit of 62/174,498 06/11/2015
and claims benefit of 62/171,915 06/05/2015
and claims benefit of 62/157,876 05/06/2015
and claims benefit of 62/154,675 04/29/2015
and claims benefit of 62/153,443 04/27/2015
and claims benefit of 62/139,511 03/27/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/100,025 01/05/2015
and claims benefit of 62/090,879 12/11/2014
and claims benefit of 62/081,538 11/18/2014
and said 14/943,898 11/17/2015 claims benefit of 62/232,716 09/25/2015
and claims benefit of 62/213,556 09/02/2015
and claims benefit of 62/209,311 08/24/2015
and claims benefit of 62/205,717 08/15/2015
and claims benefit of 62/199,607 07/31/2015
and claims benefit of 62/197,120 07/27/2015
and claims benefit of 62/188,876 07/06/2015
and claims benefit of 62/182,602 06/21/2015
and claims benefit of 62/175,855 06/15/2015
and claims benefit of 62/174,498 06/11/2015
and claims benefit of 62/171,915 06/05/2015
and claims benefit of 62/157,876 05/06/2015
and claims benefit of 62/154,675 04/29/2015
and claims benefit of 62/153,443 04/27/2015
and claims benefit of 62/139,511 03/27/2015
and claims benefit of 62/111,582 02/03/2015
and claims benefit of 62/100,025 01/05/2015
and claims benefit of 62/090,879 12/11/2014
and claims benefit of 62/081,583 11/19/2014 ABN
and said 14/947,718 11/20/2015 is a CON of PCT/US2014/039208 05/22/2014
which claims benefit of 61/826,446 05/22/2013
and claims benefit of 61/843,021 07/04/2013
and claims benefit of 61/905,109 11/15/2013
and claims benefit of 61/834,873 06/13/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the Patent Prosecution Highway program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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Samsung v. W&Wsens - IPR2025-00993

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 09/12/2024

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 18/822,880**

Projected Publication Date: 12/26/2024

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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Samsung v. W&Wsens - IPR2025-00993

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 18/822,880

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	64		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	280		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	320		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	15 minus 20 =	* 0	x =	0	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*	x =	0			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			168			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	832		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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Kathi Vidal
Under Secretary of Commerce for Intellectual Property and
Director of the United States Patent and Trademark Office

Derrick Brent
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18822880	09/03/2024

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I20249HL14266827	2054	Non-DOCX Filing Surcharge	$160.00	Deposit Account

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Sale Accounting Date:09/13/2024

Sale Item Reference Number	Effective Date
18822880	09/03/2024

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I20249CG28029412	2081	UTILITY APPL SIZE FEE PER 50 SHEETS >100	$168.00	Deposit Account

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PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
18/822,880	**09/03/2024 03:22:37 PM Z ET**	**309-0015USCIPDIV**

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	67024254	FILING DATE	-
CUSTOMER #	139982	FIRST NAMED INVENTOR	SHIH-PING Wang
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV_PetitionToMakeSpecialBasedOnAge-Final.pdf	2	Petition to make special based on Age/Health	188 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
309-0015USCIPDIV_PetitionToMakeSpecialBasedOnAge-Final.pdf	0076F8C2BE0DC6DFD62872CF3C23801956A97A6EA976B90FF7568BD68A8FD641ECFCD7EF8B96F3B215DAAC3ED09E2E752C920A63AF82A816BE4A90FD76D1C564

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as

described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: PET.OP.AGE
Description: Petition to make special based on age/health

PTO/SB/130 (01-19)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PETITION TO MAKE SPECIAL BASED ON AGE FOR ADVANCEMENT OF EXAMINATION UNDER 37 CFR 1.102(c)(1)

Application Information

Application Number	TBD	Confirmation Number	n/a	Filing Date	TBD
Attorney Docket Number (optional)	309-0015USCIPDIV	Art Unit	n/a	Examiner	n/a
First Named Inventor	Shih-Yuan WANG				
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES				

Attention: Office of Petitions

An application may be made special for advancement of examination upon filing of a petition showing that the applicant is 65 years of age, or more. No fee is required with such a petition. See 37 CFR 1.102(c)(1) and MPEP 708.02 (II).

APPLICANT HEREBY PETITIONS TO MAKE SPECIAL FOR ADVANCEMENT OF EXAMINATION IN THIS APPLICATION UNDER 37 CFR 1.102(c)(1) and MPEP 708.02 (II) ON THE BASIS OF THE APPLICANT'S AGE.

A grantable petition requires one of the following items:

(1) Statement by one named inventor in the application that he/she is 65 years of age, or more; or

(2) Certification by a registered attorney/agent having evidence such as a birth certificate, passport, driver's license, etc. showing one named inventor in the application is 65 years of age, or more.

Name of inventor who is 65 years of age, or older

Given Name	Middle Name	Family Name	Suffix
Shih-Ping		WANG	

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 11.18. Please see 37 CFR 1.4(d) for the format of the signature.

Select (1) or (2):

☐ (1) I am an inventor in this application and I am 65 years of age, or more.

☒ (2) I am an attorney or agent registered to practice before the Patent and Trademark Office, and I certify that I am in possession of evidence, and will retain such in the application file record, showing that the inventor listed above is 65 years of age, or more.

Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2024-09-03
Name	Ivan S. Kavrukov	Registration Number	25,161

This collection of information is required by 37 CFR 1.102(c)(1). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) a petition to make special based on age for advancement of examination. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETED FORMS TO THE CHIEF INFORMATION OFFICER. **Submit completed forms electronically over EFS-Web, or mail to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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THOMSON NATIVE MAT through DFP

SUBJECT OF THE INVENTION

SUBJECT OF THE INVENTION

Improvement in the speed of a response speed can be achieved, and manufacture provides an easy near-infrared-light sensing element.
PROBLEM to be solved
The photoelectric-conversion part 6 which has a photodiode structure of a pin photodiode which forms in 1 surface side of the semiconductor substrate 1, and the i layer 62 which is a drift area| region interposes between the p form area|region 61 and the n form area|region 63, absorbs near infrared light, and an electronic * hole pair generate|occur|produces,
With respect to the wavelength range of the near infrared light of the detection target which injects from the direction which is a slab type|mold photonic crystal which is laminated|stacked on the light-receiving surface of the photoelectric-conversion part 6, and has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and intersects said light-receiving surface
The slab type|mold photonic crystal 7 by which the refractive-index period structure was designed have a resonance peak is provided.

DETAILED DESCRIPTION of the INVENTION

[0001] TECHNICAL FIELD
This invention relates to the near-infrared-light sensing element which detects near infrared light.

DESCRIPTION OF RELATED ART

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[0002] Conventionally, in the optical communication, the near-infrared-light sensing element is used as a light receiving element for receiving a light signal.
As this kind of a near-infrared-light sensing element, the photodiode (pn photodiode, a pin photodiode, an avalanche photo-diode, the Schottky photodiode, etc.) in which the pn junction and the schottky junction were formed is widely used for a semiconductor crystal.
It utilizes that the electric current which the electronic-hole pair generate|occur|produced when the light which has the photon energy more than a band gap injects is isolate|separated, travel|drive| works in a depletion layer (drift), and flows into an external circuit changes,
A light signal is detected as electric current change or voltage change.
As a semiconductor crystal material used for a near-infrared-light sensing element in here, there exists compound-semiconductor crystal|crystallization material (InGaAs, InGaAsP, etc.) other than Si or Ge,
However,
It is properly used by the wavelength range of the light used by an optical communication, the transmission speed request|required, the price, etc.

[0003] By the way, the optical communication is already widely used as a communication network between cities and in a city,
However,
In recent years, the motion which employ|adopts an optical communication also, for example in field|areas, such as SAN(Storage Area Network) which connects a highly efficient server and a router, DVI(Digital Visual Interface) which connects what is called an information appliance and a peripheral device, in-vehicle LAN(Local Area Network), a mobile phone, is activating.
The high-speed optical communication is required also in such a field|area,
Progress of improvement in the speed of transmission speed changes with applicable fields,
It is estimated that the transmission speed of 1Gbps or more is request|required also in either field| area.

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[0004] Improvement in the speed and a lowering of cost of a response speed will be request|required of the photodiode for optical communications used in the above various field|areas from now on.
In here, it is known that the response speed of a photodiode will be fundamentally limited with two elements with the transit time t of the career|carrier (an electron, a hole) which carries out the drift of the inside of a depletion layer to CR time constant of a photodiode.
In order to raise quantum efficiency (light-reception sensitivity) while making CR time constant small when the pin photodiode using Si as a semiconductor crystal material is considered for an example, the wide depletion layer is formed,
Therefore
It becomes impossible for the transit time t of the electron which carries out the drift of the inside of a depletion layer to ignore at the time of a high-speed response.

[0005] For example, in order for quantum efficiency to be 80 % or more by the pin photodiode of Si, a depletion-layer width W of about 30 micrometer is needed,
However,
When cut-off-frequency fc (CR) decided by CR time constant sets the diameter of a light reception to 250 micrometer, the pn-junction area A will become A=4.9*10<-4>cm<2>,
30 micrometer, then junction-capacitance Cj of a pn junction are set to Cj=0.17pF by the depletion-layer width W,
Therefore
It will become fc(CR)=1/(2(pi)CjR)=18GHz when the external resistance R shall be 50 omega|ohm.

[0006] On the other hand, it will become fc(ttr)=0.44/ttr when the frequency from which the amplitude of a photoelectric current becomes 1/2<1/2> of the amplitude of a low-frequency area|region, and electric power becomes 1/2 (-3 dB) is defined as cut-off-frequency f(ttr),
However,
Since saturated-drift-velocity (nu)ds of the electron which carries out the drift of during Si crystal| crystallization is (nu)ds=1*10<7>cm/sec, transit-time ttr of the electron which carries out the drift of the inside of a depletion layer becomes ttr=W/(nu)ds=0.3nsec,
Cut-off-frequency fc(ttr) becomes fc(ttr)=1.5GHz.
As mentioned above, the diameter of a light reception about 250 micrometer and the pin photodiode of Si whose depletion-layer width W is 30 micrometer
Since cut-off-frequency fc (CR) decided from CR time constant was 18GHz, in this pin photodiode, above-mentioned transit-time ttr will limit a cut off frequency,
It understand|indicate|reveals that the 1.5GHz vicinity is a limit of an operating frequency.

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[0007] Here, in order to achieve improvement in the speed of the response speed of a pin photodiode, it is necessary to enlarge a cut off frequency,
Therefore
The drift velocity in a semiconductor crystal should just use compound-semiconductor material, Ge, etc. which are a quick semiconductor crystal material compared with Si,
However,
Like a silicon-semiconductor process, it is not excellent in mass-production property, and since the diameter of a wafer is also small, a lowering of cost is difficult.

[0008] On the other hand, let the photoelectric-conversion part which has a pin photodiode structure of Si be a basic composition in recent years,
Quantum efficiency can be improved though thickness reduction of i layer which is a drift area| region in which a career|carrier carries out a drift in a photoelectric-conversion part is achieved,
The near-infrared-light sensing element which can achieve improvement in the speed by shortening of transit-time ttr of the career|carrier which furthermore carries out the drift of the inside of i layer is proposed (a nonpatent literature 1, 2).

[0009] This kind of near-infrared-light sensing element as shown in FIG. 4
DBR(Distributed Bragg Reflector)152 which consists of laminated film of the 1st SiO2 layer 152a, the Si layer 152b, and the 2nd SiO2 layer 152c, and reflects near infrared light on the 1 surface of the Si board|substrate 151 is provided.
The photoelectric-conversion part 160 which consists of a pin photodiode structure of Si which the i layer 162 interposes between the n<+> area|region 163 and the p<+> area|region 161 is provided on DBR152,
A surface with the light-receiving surface which consists of a surface of air and the p<+> area| region 161 forms the reflective surface which faces DBR152 (each other) on both sides of the photoelectric-conversion part 160 in the thickness direction (vertical direction) of the Si board| substrate 151,
The vertical resonator which consists of Fabry Perot type resonator (Fabry-Perot Resonator) by said reflective surface and DBR152 is formed.
Therefore, even if it makes thickness of the i layer 162 in the photoelectric-conversion part 160 small (it is small about the width of the i layer 162 in other words), a light-reception sensitivity can

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be improved, and the distance of a career|carrier can also be shortened by making thickness of the i layer 162 thin,
Therefore
Improvement in the speed of a response speed can be achieved.
In addition, the p<+> area|region 161 is electrically connected with the p electrode 165 by 1 said surface side of the Si board|substrate 151, and the n<+> area|region 163 is electrically connected with the n electrode 163 by 1 said surface side of the Si board|substrate 151.
M.K. Emsley, et al, Silicon Resonant Cavity Enhanced Photodetector Arrays for Optical Interconnects, Proc. of SPIE Vol.5246,p409-421,2003
M.K. Emsley, et al, Silicon Substrates With Buried Distributed Bragg Reflectors for Resonant Cavity-Enhanced Optoelectronics, IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS,VOL.8,NO.4,p948-955,JULY/AUGUST 2002

DISCLOSURE OF THE INVENTION

PROBLEM TO BE SOLVED BY THE INVENTION

[0010] However,
In order to manufacture the near-infrared-light sensing element of the structure shown in FIG. 4, it is necessary to repeat twice basic process (Hydrogen-ion injection|grouting work is a bonding process, a peeling|exfoliation process, and a surface grinding|polishing process.) required of the hydrogen injection|pouring peel|exfoliating method known as one of the formation methods of an SOI wafer before formation of the photoelectric-conversion part 160,
The manufacture process was complicated and cost reduction was difficult.
Moreover, the manufacturing method of the above-mentioned infrared-light sensing element cannot be applied when employ|adopting semiconductor crystal materials other than Si as a material of the photoelectric-conversion part 160.

[0011] This invention was comprised in view of said reason,
The objective is to be able to achieve improvement in the speed of a response speed, and for manufacture to provide an easy near-infrared-light sensing element.

MEANS TO SOLVE THE PROBLEM

[0012] The photoelectric-conversion part which has a photodiode structure where invention of Claim 1 was formed in 1 surface side of a semiconductor substrate, and the drift area|region was provided

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between p form area|region and n form area|region, absorbs near infrared light, and an electronic * hole pair generate|occur|produces,
With respect to the wavelength range of the near infrared light of the detection target which injects from the direction which is a slab type|mold photonic crystal which is laminated|stacked on the light-receiving surface of a photoelectric-conversion part, or is formed in said light-receiving-surface side in the inside of a photoelectric-conversion part, and has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and intersects said light-receiving surface
The slab type|mold photonic crystal by which the refractive-index period structure was designed have a resonance peak is comprised,
It is characterized by the above-mentioned.

[0013] According to this invention
To 1 surface side of a semiconductor substrate
To the light-receiving surface of the formed photoelectric-conversion part
With respect to the wavelength range of the near infrared light of the detection target which injects from the direction which is a slab type|mold photonic crystal which is laminated|stacked, or is formed in said light-receiving-surface side in the inside of a photoelectric-conversion part, and has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and intersects said light-receiving surface
By providing the slab type|mold photonic crystal by which the refractive-index period structure was designed have a resonance peak
Quantum efficiency can be raised even if it makes thin the thickness of the drift area|region of the photoelectric-conversion part of photodiode structures, such as a pin photodiode and an avalanche photo-diode, without providing a conventional vertical resonator,
Therefore
Can achieve improvement in the speed of a response speed, without making a light-reception sensitivity reduce, and again
The slab type|mold photonic crystal which was laminated|stacked on the photoelectric-conversion part or was formed in said light-receiving-surface side in the inside of a photoelectric-conversion part can be formed using the thin film coating technology, lithography technology, and etching technique which are general semiconductor manufacture process techniques,
Therefore
It can manufacture easily.

[0014] The near-infrared-light reflection part which invention of Claim 2 surrounds said photoelectric-conversion part in 1 said surface side of said semiconductor substrate in invention of Claim 1 by

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two dimensional surface inside parallel to said light-receiving surface, and reflects the near infrared light of said wavelength range in said photoelectric-conversion part side is comprised,
It is characterized by the above-mentioned.

[0015] By providing the near-infrared-light reflection part which surrounds said photoelectric-conversion part by two dimensional surface inside parallel to said light-receiving surface, and reflects the near infrared light of said wavelength range in said photoelectric-conversion part side according to this invention
It can prevent that the near infrared light of said wavelength range that injected on said photoelectric-conversion part through said light-receiving surface leaks to the side of said photoelectric-conversion part,
Therefore
Quantum efficiency can be raised more and a light-reception sensitivity can be raised further.

[0016] In invention of Claim 2, invention of Claim 3 said near-infrared-light reflection part
It is a two dimensional photonic crystal which has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and consists of a two dimensional photonic crystal by which the refractive-index period structure was designed reflect the near infrared light of said wavelength range in said photoelectric-conversion part side,
It is characterized by the above-mentioned.

[0017] According to this invention, said near-infrared-light reflection part can be easily formed using the lithography technology and etching technique which are general semiconductor manufacture process techniques.

[0018] In invention of Claim 1 thru|or Claim 3, the shape of invention of Claim 4 of said p form area|region in two dimensional surface inside with said photoelectric-conversion part parallel to said light-receiving surface and each said n form area|region is comb-shaped,
Said p form area|region and said n form area|region are mutually complex,
The said drift area|region consists of an i layer interposed between said p form area|region and said n form area|region,
It is characterized by the above-mentioned.

[0019] According to this invention
The thickness (width of i layer) of said drift area|region that consists of an i layer which interposes the mask at the time of forming said p form area|region with a spreading|diffusion or an ion implantation and said n form area|region between said p form area|region and said n form area|

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region with relative position accuracy with the mask at the time of forming with a spreading| diffusion or an ion implantation is decided,
Therefore
The precision of the thickness dimension of said drift area|region can be raised.

[0020] ADVANTAGE OF THE INVENTION
Invention of Claim 1 can achieve improvement in the speed of a response speed, and is effective in the ability to manufacture easily.

PREFERRED EMBODIMENT OF THE INVENTION

[0021] (Embodiment 1)
As shown to FIG. 1 (a), (b), the near-infrared-rays sensing element of this embodiment
While the semiconductor layer 3 which consists of a single-crystal Si layer of low concentration (For example, 10<13>-10<16>cm<-3> extent) via the 1st dielectric layer 2 which consists of a SiO2 film|membrane on the 1 surface of the semiconductor substrate 1 which consists of a Si board| substrate is provided
The 2nd dielectric layer 4 which consists of a SiO2 film|membrane is provided on said semiconductor layer 3,
The photoelectric-conversion part 6 which has a photodiode structure of a pin photodiode, absorbs near infrared light, and an electronic * hole pair generate|occur|produces is formed in the center section of the semiconductor layer 3.
In the center section of the 2nd dielectric layer 4, the light-receiving surface of the photoelectric-conversion part 6
With respect to the wavelength range of the near infrared light of the detection target by which injection|incidence (In this embodiment, it injected from the reverse side with the semiconductor substrate 1 side.) is carried out from the direction which is a slab type|mold photonic crystal which has a refractive-index period structure in two dimensional surface inside parallel to (the upper surface in FIG.1(b)), and intersects said light-receiving surface
The slab type|mold photonic crystal 7 by which the refractive-index period structure was designed have a resonance peak is formed.
In addition, in this embodiment, the material of the 1st dielectric layer 2 and the 2nd dielectric layer 4 is SiO2,
The semiconductor crystal material of the photoelectric-conversion part 6 is Si,
Therefore
The refractive index of the semiconductor layer 3 becomes a high value rather than each refractive index of the 1st dielectric layer 2 and the 2nd dielectric layer 4, and in (The refractive index of

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about 1.5 and Si of the refractive index of SiO2 is about 3.4.) and the photoelectric-conversion part 6
The waveguide mode which confines the near infrared light which injected from the light-receiving surface in the photoelectric-conversion part 6 according to a refractive-index difference with the medium of the both sides of the photoelectric-conversion part 6, and waveguides it exists,
Quantum efficiency can be raised.

[0022] In here, the near-infrared-light sensing element of this embodiment is used as a light receiving element of an optical communication,
A 0.8-micrometer belt|band|zone is assumed as a wavelength range of the near infrared light (input-signal light) of a detection target,
Si is employ|adopted as a semiconductor crystal material of the photoelectric-conversion part 6,
Si board|substrate is used as a semiconductor substrate 1.

[0023] The photoelectric-conversion part 6 is with the p form area|region 61 where the shape in two dimensional surface inside parallel to said light-receiving surface consists of a comb-shaped p<+> layer, as shown to FIG.1(b) and (c),
The n form area|region 63 where the shape in two dimensional surface inside parallel to said light-receiving surface consists of a comb-shaped n<+> layer is mutually complex,
In the shape in surface inside parallel to said light-receiving surface, the i layer 62 of an undulation state (the shape of a winding path) is interposing between the p form area|region 61 and the n form area|region 63.
In here, the comb-tooth parts 61b and 63b of multiple (the example of illustration three) which it was equally spaced and were spaced apart are continuously formed in the left-right direction of FIG.1(c) at each of comb bone 61a, 63a with circular arc-shaped p form area|region 61 and n form area|region 63,
In the left-right direction of FIG.1(c), the comb-tooth part 61b of the p form area|region 61 and the comb-tooth part 63b of the n form area|region 63 are alternately located in a line.
In addition, the shape in two dimensional surface inside with the photoelectric-conversion part 6 parallel to said light-receiving surface is formed in circular as a whole.
Moreover, in this embodiment, the i layer 62 is comprising the drift area|region provided between the p form area|region 61 and the n form area|region 63.

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[0024] Moreover, the contact hole is formed in the region to which the near-infrared-light sensing element of this embodiment overlaps with the p form area|region 61 in the 2nd dielectric layer 4,
The contact electrode 8a which consists of a metal material which was embedded at said contact hole and was electrically connected with the p form area|region 61 is electrically connected via Pad 10a and the metal wiring 9a which were formed on the 2nd dielectric layer 4.
Similarly, the contact hole is formed in the region which overlaps with the n form area|region 63 in the 2nd dielectric layer 4,
The contact electrode 8b which consists of a metal material which was embedded at said contact hole and was electrically connected with the n form area|region 63 is electrically connected via Pad 10b and the metal wiring 9b which were formed on the 2nd dielectric layer 4.

[0025] Moreover, the slab type|mold photonic crystal 7 is arranged so that it may have a 2-dimensional period structure by surface inside (Two dimensional surface inside parallel to the light-receiving surface of the photoelectric-conversion part 6 in other words) which many holes 72 orthogonally cross in the thickness direction of slab 71 which consists of a region currently laminated|stacked on the photoelectric-conversion part 6 among the 2nd dielectric layers 4,
The slab type|mold photonic crystal 7 which has said refractive-index period structure by the low-refractive-index medium which consists of air in the high refractive index medium which comprises slab 71, and hole 72 is comprised.
When a unit cell specifically forms hole 72 in each location corresponding to each lattice point of the hypothetical|virtual two dimensional triangular grating|lattice of an equilateral triangle in slab 71, the slab type|mold photonic crystal 7 is formed.
If it paraphrases, hole 72 is arranged by triangular grating|lattice shape in surface inside orthogonally crossed in the thickness direction of slab 71.
In addition, the refractive index of about 1.5 and air of the refractive index of SiO2 which is the material of the 2nd dielectric layer 4 is 1.

[0026] The said refractive-index period structure is designed in design of the slab type|mold photonic crystal 7 have a resonance peak in the wavelength range of the near infrared light of a detection target as mentioned above.
Specifically, a, then Period a should just set period (It is a period of the refractive-index period structure of the slab type|mold photonic crystal 7, and is the distance during the lattice point of a two dimensional triangular grating|lattice.) of the sequence direction of hole 72 in the slab type|

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mold photonic crystal 7 to the half-wave-length extent (For example, 1/2 of the wavelength of an infrared-light) of the infrared-light of said wavelength range, for example.
In addition, about the optical propagation part which is the principal part comprised in the slab type|mold photonic crystal 7 and the photoelectric-conversion part 6 among the near-infrared-light sensing elements of this embodiment
The semiconductor substrate 1 and a reverse side have a refractive-index difference with the air (refractive-index =1) which is a medium of slab type|mold photonic-crystal 7 and slab type|mold photonic-crystal 7 just overhead,
The semiconductor substrate 1 side has the 1st dielectric layer (refractive-index =1.5) 2 and 1st refractive-index difference which are the mediums of photoelectric-conversion part 6 directly under.
When there exist the medium and the above refractive-index differences which said optical propagation part is touching by each of up-and-down both sides (both sides of the thickness direction of the semiconductor substrate 1) in such an optical propagation part
There exist waveguide mode in which the near infrared light which propagates an optical propagation part satisfy|fills the total-reflection conditions of a up-down direction, and is completely

confined in an optical propagation part, and a mode (It calls in-plane resonance mode hereafter) which does not satisfy|fill total-reflection conditions but can be couple|bonded with ambient light. When near infrared light is injected on such an optical propagation part from the exterior, one part near infrared light will couple|bond with in-plane resonance mode,
Any of in-plane resonance mode and waveguide mode, may not couple|bond another one part and it may be permeate|transmitted.
However,
As negate / after couple|bonding with in-plane resonance mode / the near infrared light re-radiated and the near infrared light to permeate|transmit
In this case, all the near infrared light which injected on the optical propagation part couple|bonds with in-plane resonance mode.
Thus, the light couple|bonded with in-plane resonance mode propagates the inside of an optical propagation part according to Q value of a resonance peak,
Therefore
Without providing a vertical resonator like the conventional structure of FIG. 4, in the thickness of the i layer 62 in the photoelectric-conversion part 6, even if thin, near infrared light is efficiently absorbed in the i layer 62.
Moreover, in this embodiment, all the near infrared light of said wavelength range that injects on an optical propagation part couple|bonds with in-plane resonance mode,
Therefore
It is not necessary to provide a reflection layer like DBR at a reverse side separately with the light-receiving surface in the photoelectric-conversion part 6.
In addition, in-plane resonance mode is reported as guided resonances in publication 1 (Shanhui Fan, et al, Analysis of guided resonances in photonic crystal slabs, PHYSICAL REVIEW B, VOLUME 65, 235112).

[0027] By the way, the near-infrared-light sensing element of this embodiment is formed in the middle of the thickness direction what is called using SOI(Silicon On Insulator) board|substrate which has a SiO2 film|membrane,
Si board|substrate of the back side in an SOI board|substrate comprises the semiconductor substrate 1,
The SiO2 film|membrane of an SOI board|substrate comprises the 1st dielectric layer 2,
Si layer of the main surface side of an SOI board|substrate is comprising the semiconductor layer 3.
That is, the photoelectric-conversion part 6 in a near-infrared-light sensing element is formed by introduce|transducing an impurity to the region corresponding to the each of the p form area| region 61 and the n form area|region 63 with a spreading|diffusion or an ion implantation in the

semiconductor layer 3 which consists of a Si layer of the main surface side of an SOI board| substrate,
Therefore
With relative position accuracy with the mask at the time of forming the mask at the time of forming the p form area|region 61 with a spreading|diffusion or an ion implantation, and the n form area| region 63 with a spreading|diffusion or an ion implantation
The thickness (It is the width of the i layer 62,
Comprising:
The distance of a career|carrier) of the i layer 62 which consists of a region interposed between the p form area|region 61 and the n form area|region 63 among the semiconductor layers 3 is decided,
Therefore
The precision of the thickness dimension of the i layer 62 can be raised.

[**0028**] Moreover, after the slab type|mold photonic crystal 7 forms the photoelectric-conversion part 6 in the semiconductor layer 3 which consists of a Si layer of the main surface side of an SOI board| substrate
After forming the 2nd dielectric layer 4 into a film with thin-film formation methods, such as CVD method, to the whole surface of the main surface side of an SOI board|substrate, the resist layer by which the region corresponding to each hole 72 was pierced using the lithography technology is formed on the 2nd dielectric layer 4,
It can form by etching the region corresponding to each hole 72 by the dry etching apparatus among the 2nd dielectric layers 4 by setting said resist layer as a mask.
In addition, not only SiO2 but Si3N4 may be sufficient as the medium which comprises slab 71, for example.

[**0029**] The near-infrared-light sensing element of this embodiment demonstrated above
The slab type|mold photonic crystal 7 by which the refractive-index period structure of two dimensional surface inside parallel to said light-receiving surface was designed have a resonance peak with respect to the wavelength range of the near infrared light of the detection target which is

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laminated|stacked on the light-receiving surface of the photoelectric-conversion part 6, and injects from a reverse side with the photoelectric-conversion part 6 side is provided,
Therefore
Quantum efficiency can be raised even if it makes thin thickness (width) of the i layer 62 of the photoelectric-conversion part 6 of the photodiode structure of a pin photodiode, without providing a vertical resonator like a structure before shown in FIG. 4,
Therefore
Improvement in the speed of a response speed can be achieved without making a light-reception sensitivity reduce.
Moreover, the slab type|mold photonic crystal 7 laminated|stacked on the photoelectric-conversion part 6 can be formed using the thin film coating technology, lithography technology, and etching technique which are general semiconductor manufacture process techniques,
Therefore
It can manufacture easily.

[0030] (Embodiment 2)
The basic composition of the near-infrared-light sensing element of this embodiment is substantially the same as Embodiment 1,
Comprising:
The point currently formed as shown in FIG. 2 in the form where the p form area|region 61 and the i layer 62 in the photoelectric-conversion part 6, and the n form area|region 63 are located in a line with the thickness direction of the semiconductor substrate 1 is different.
In addition, the same code is attached to the same component as Embodiment 1, and description is abbreviate|omitted.

[0031] The p form area|region 61 and the n form area|region 63 of the photoelectric-conversion part 6 in this embodiment are formed in the shape where the shape in two dimensional surface inside parallel to said light-receiving surface notched partial circle as shown in FIG.2(c), (d),
The region interposed between the p form area|region 61 and the n form area|region 63 among the semiconductor layers 3 is comprising the i layer 62.
In addition, the p form area|region 61 and the n form area|region 63 are formed by introduce|transducing an impurity to the region corresponding to the each of the p form area|region 61 and the n form area|region 63 with a spreading|diffusion or an ion implantation in the semiconductor layer 3.

[0032] Moreover, the p form area|region 61 and the n form area|region 63 space apart the near-infrared-light sensing element of this embodiment in the thickness direction of the semiconductor substrate 1, and it is formed,
The n form area|region 63 is formed in the position distant from the 2nd dielectric layer 4,
Therefore
The spreading|diffusion wiring 63c (refer FIG.2(c)) for connecting electrically the n form area|region 63 and the contact electrode 8b is formed in the semiconductor layer 3.
In addition, each contact electrode 8a, 8b are formed in the region which overlaps with each circumference of the p form area|region 61 and the n form area|region 63 in the 2nd dielectric layer 4.

[0033] Thus, without making a light-reception sensitivity reduce, improvement in the speed of a response speed can be achieved, and the near-infrared-light sensing element of this embodiment as well as Embodiment 1 can be manufactured easily.

[0034] (Embodiment 3)
The basic composition of the near-infrared-light sensing element of this embodiment is substantially the same as Embodiment 1,
Comprising:
A point provided with the near-infrared-light reflection part 11 which surrounds the photoelectric-conversion part 6 in 1 said surface side of the semiconductor substrate 1 by two dimensional surface inside parallel to the light-receiving surface of the photoelectric-conversion part 6, and, as shown in FIG. 3, reflects the near infrared light of the wavelength range of a detection target in the photoelectric-conversion part 6 side is different.
In addition, the same code is attached to the same component as Embodiment 1, and description is abbreviate|omitted.

[0035] By the way, the near-infrared-light reflection part 11 in this embodiment is a two dimensional photonic crystal which has a refractive-index period structure in two dimensional surface inside with the near-infrared-light reflection part 11 parallel to said light-receiving surface,
It arranges so that it may have a 2-dimensional period structure by two dimensional surface inside which many holes 11a orthogonally cross in the thickness direction of slab 11b which consists of some semiconductor layers 3,
The two dimensional photonic crystal which has said refractive-index period structure by the low-refractive-index medium which consists of air in the high refractive index medium (here Si) which comprises Slab 11b, and Hole 11a is comprised.
Specifically, when a unit cell forms Hole 11a in Slab 11b at each lattice point of the hypothetical| virtual two dimensional triangular grating|lattice of an equilateral triangle, the two dimensional photonic crystal 11 is formed.
If it paraphrases, Hole 11a is arranged by triangular grating|lattice shape in surface inside orthogonally crossed in the thickness direction of Slab 11b.

[0036] The said refractive-index period structure is designed reflect the near infrared light of the wavelength range of a detection target in the photoelectric-conversion part 6 side as mentioned above in design of the two dimensional photonic crystal 11 in here.
Specifically, b, then Period b should just set period (It is a period of the refractive-index period structure of the two dimensional photonic crystal 11, and is the distance during the lattice point of a two dimensional triangular grating|lattice.) of the sequence direction of hole 11a in the two dimensional photonic crystal 11 to the half-wave-length extent (For example, 1/2 of the wavelength of an infrared-light) of the infrared-light of said wavelength range, for example.

[0037] Thus, in the near-infrared-light sensing element of this embodiment, it can prevent that the near infrared light of said wavelength range that injected on the photoelectric-conversion part 6 through said light-receiving surface leaks to the side of the photoelectric-conversion part 6 by providing the above-mentioned near-infrared-light reflection part 11,
Therefore
Quantum efficiency can be raised more and a light-reception sensitivity can be raised further.
Moreover, it comprises the two dimensional photonic crystal by which the refractive-index period structure was designed so that the near-infrared-light reflection part 11 might be a two dimensional photonic crystal which has a refractive-index period structure in two dimensional surface inside

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parallel to said light-receiving surface and might reflect the near infrared light of said wavelength range in the photoelectric-conversion part 6 side,
Therefore
The near-infrared-light reflection part 11 can be easily formed using the lithography technology and etching technique which are general semiconductor manufacture process techniques.
In addition, in this embodiment, the two dimensional photonic crystal 11 is comprised according to the period structure of two kinds of mediums of Si and air,
However,
It is substantial with the dielectric material (For example, SiO2 etc.) into which a refractive index differs Hole 11a from Si, and it is sufficient to make it form the two dimensional photonic crystal 11 by said dielectric material and Si.
By the way, in each said Embodiment, Si is employ|adopted as a semiconductor crystal material of the photoelectric-conversion part 6,
Si board|substrate is used as a semiconductor substrate 1,
However,
Not only Si but Ge and compound-semiconductor crystal|crystallization material may be sufficient as the semiconductor crystal material of the photoelectric-conversion part 6, for example,
Not only Si board|substrate but Ge board|substrate, a GaAs board|substrate, etc. may be sufficient as the semiconductor substrate 1, for example.
Moreover, in each said Embodiment, the slab type|mold photonic crystal 7 was comprised according to the period structure of two kinds of mediums of SiO2 and air,
However,
It is substantial with the dielectric material into which a refractive index differs the inside of hole 72 from SiO2, and it is sufficient to make it form the slab type|mold photonic crystal 7 by said dielectric material and SiO2.
Or it is good also as a period structure of the medium of 3 or more type,
For example
By forming Si3N4 film|membrane which coat|covers the internal peripheral surface of hole 72 provided at slab 71 which consists of SiO2
It is sufficient to make it comprise the slab type|mold photonic crystal 7 by three kinds such as SiO2, Si3N4, and air.

[0038] Moreover, in each said Embodiment, the slab type|mold photonic crystal 7 is laminated|stacked on the light-receiving surface of the photoelectric-conversion part 6,
However,
Instead of laminating|stacking the slab type|mold photonic crystal 7 on the photoelectric-conversion part 6, it is sufficient to make it form in the light-receiving-surface side in the inside of the photoelectric-conversion part 6.
Moreover, in each said Embodiment, the photoelectric-conversion part 6 has a photodiode structure of a pin photodiode where i layer was provided as a drift area|region 62 between the p form area|region 61 and the n form area|region 63,
However,
As long as the drift area|region is provided between the p form area|region 61 and the n form area|region 63, the photodiode structure of an avalanche photo-diode may be sufficient as the photoelectric-conversion part 6.

[0039] Moreover, to slab 71, the slab type|mold photonic crystal 7 in each said Embodiment is formed, when a unit cell forms hole 72 in each location corresponding to each lattice point of the hypothetical|virtual two dimensional triangular grating|lattice of an equilateral triangle,
However,
Not only an equilateral triangle but a square may be sufficient as a unit cell, for example,
In this case, a unit cell should just form hole 72 in the region corresponding to each lattice point of a square hypothetical|virtual two dimensional tetragonal lattice.
Moreover, in each said Embodiment, in order to form the refractive-index period structure of the slab type|mold photonic crystal 7, many holes 72 are formed in slab 71,
However,
Instead of providing hole 72, it is sufficient to provide holes of another aperture|opening shape, such as a triangular-shaped hole and a rectangular hole, for example.

BRIEF DESCRIPTION OF THE DRAWINGS

[0040]

FIG. 1: Embodiment 1 is shown,
(a) is a schematic plan view,
(b) is the schematic perspective view fractured by A-A' of (a),
(c) is a horizontal sectional view.

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FIG. 2: Embodiment 2 is shown,
(a) is a schematic plan view,
(b) is the schematic perspective view fractured by A-A' of (a),
(c) is a horizontal sectional view,
(d) is an another horizontal sectional view.

FIG. 3: Embodiment 3 is shown,
(a) is a schematic plan view,
(b) is the schematic perspective view fractured by A-A' of (a),
(c) is a horizontal sectional view.

FIG. 4: It is a schematic sectional drawing which shows a prior art example.

DESCRIPTION OF SYMBOLS

[**0041**] One semiconductor substrate
The dielectric layer of 2 1st
Three semiconductor layers
The dielectric layer of 4 2nd
Six photoelectric-conversion parts
Seven slab type|molds photonic crystal
8a,
8b contact electrode
9a,
9b metal wiring
10a,
10b pad
61 P form area|region
62 I layer
63 N form area|region
71 slabs
72 holes

1. 1. The photoelectric-conversion part which has a photodiode structure where formed in 1 surface side of a semiconductor substrate, and the drift area|region was provided between p form area|region and n form area|region, absorbs near infrared light, and an electronic * hole pair generate|occur|produces, With respect to the wavelength range of the near infrared light of the detection target which injects from the direction which is a slab type|mold photonic crystal which is laminated|stacked on the light-receiving

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surface of a photoelectric-conversion part, or is formed in said light-receiving-surface side in the inside of a photoelectric-conversion part, and has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and intersects said light-receiving surface
The slab type|mold photonic crystal by which the refractive-index period structure was designed have a resonance peak is comprised,
The near-infrared-light sensing element characterized by the above-mentioned.

2. 2. The near-infrared-light reflection part which surrounds said photoelectric-conversion part in 1 said surface side of said semiconductor substrate by two dimensional surface inside parallel to said light-receiving surface, and reflects the near infrared light of said wavelength range in said photoelectric-conversion part side is comprised,
The near-infrared-light sensing element of Claim 1 characterized by the above-mentioned.
3. 3. The said near-infrared-light reflection part is a two dimensional photonic crystal which has a refractive-index period structure in two dimensional surface inside parallel to said light-receiving surface, and it consists of a two dimensional photonic crystal by which the refractive-index period structure was designed reflect the near infrared light of said wavelength range in said photoelectric-conversion part side,
The near-infrared-light sensing element of Claim 2 characterized by the above-mentioned.
4. 4. The said photoelectric-conversion part has a comb-shaped shape of said p form area|region in two dimensional surface inside parallel to said light-receiving surface, and each said n form area|region,
Said p form area|region and said n form area|region are mutually complex,
The said drift area|region consists of an i layer interposed between said p form area|region and said n form area|region,
The near-infrared-light sensing element in any one of Claim 1 thru|or Claim 3 characterized by the above-mentioned.

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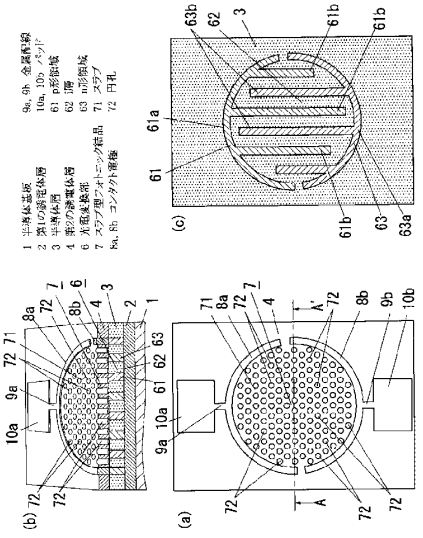
(54)【発明の名称】近赤外光検出素子

(57)【要約】

【課題】応答速度の高速化を図れ且つ製造が容易な近赤外光検出素子を提供する。

【解決手段】半導体基板１の一表面側に形成されｐ形領域６１とｎ形領域６３との間にドリフト領域であるｉ層６２が介在するｐｉｎフォトダイオードのフォトダイオード構造を有し近赤外光を吸収して電子・正孔対が発生する光電変換部６と、光電変換部６の受光面に積層され当該受光面に平行な２次元面内に屈折率周期構造を有するスラブ型フォトニック結晶であって上記受光面に交差する方向から入射される検出対象の近赤外光の波長帯に対して共振ピークを有するように屈折率周期構造が設計されたスラブ型フォトニック結晶７とを備えている。

【選択図】　図１



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【特許請求の範囲】
【請求項１】
半導体基板の一表面側に形成されｐ形領域とｎ形領域との間にドリフト領域が設けられたフォトダイオード構造を有し近赤外光を吸収して電子・正孔対が発生する光電変換部と、光電変換部の受光面に積層され若しくは光電変換部内における前記受光面側に形成され前記受光面に平行な２次元面内に屈折率周期構造を有するスラブ型フォトニック結晶であって前記受光面に交差する方向から入射される検出対象の近赤外光の波長帯に対して共振ピークを有するように屈折率周期構造が設計されたスラブ型フォトニック結晶とを備えてなることを特徴とする近赤外光検出素子。
【請求項２】
前記半導体基板の前記一表面側において前記受光面に平行な２次元面内で前記光電変換部を囲み前記波長帯の近赤外光を前記光電変換部側へ反射する近赤外光反射部を備えてなることを特徴とする請求項１記載の近赤外光検出素子。
【請求項３】
前記近赤外光反射部は、前記受光面に平行な２次元面内に屈折率周期構造を有する２次元フォトニック結晶であって前記波長帯の近赤外光を前記光電変換部側へ反射するように屈折率周期構造が設計された２次元フォトニック結晶からなることを特徴とする請求項２記載の近赤外光検出素子。
【請求項４】
前記光電変換部は、前記受光面に平行な２次元面内における前記ｐ形領域および前記ｎ形領域それぞれの形状が櫛形状であり、前記ｐ形領域と前記ｎ形領域とが互いに入り組んでおり、前記ドリフト領域が前記ｐ形領域と前記ｎ形領域との間に介在するｉ層からなることを特徴とする請求項１ないし請求項３のいずれかに記載の近赤外光検出素子。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、近赤外光を検出する近赤外光検出素子に関するものである。
【背景技術】
【０００２】
従来から、光通信では、光信号を受信するための受光素子として近赤外光検出素子が用いられている。この種の近赤外光検出素子としては、半導体結晶にｐｎ接合やショットキ接合を形成したフォトダイオード（ｐｎフォトダイオード、ｐｉｎフォトダイオード、アバランシェフォトダイオード、ショットキフォトダイオードなど）が広く用いられ、バンドギャップ以上の光子エネルギを有する光が入射された時に発生する電子－正孔対が分離されて空乏層内を走行（ドリフト）し外部回路に流れる電流が変化することを利用して、光信号を電流変化あるいは電圧変化として検出する。ここにおいて、近赤外光検出素子に用いられる半導体結晶材料としては、ＳｉやＧｅの他に、化合物半導体結晶材料（ＩｎＧａＡｓ、ＩｎＧａＡｓＰなど）があるが、光通信で用いられる光の波長帯、要求されている通信速度、価格などにより使い分けられている。
【０００３】
ところで、光通信は、都市間、都市内の通信網として既に広く使われているが、近年では、例えば高性能サーバとルータとをつなぐＳＡＮ（Storage Area Network）、いわゆる情報家電と周辺機器とをつなぐＤＶＩ（Digital Visual Interface）、車載ＬＡＮ（Local Area Network）、携帯電話機などの分野においても光通信を採用する動きが活発化している。このような分野でも高速の光通信が必要とされており、応用分野によって通信速度の高速化の進展は異なるが、いずれの分野においても１Gbps以上の通信速度を要求されることが予測されている。
【０００４】
上述のような各種分野で用いられる光通信用のフォトダイオードには今後、応答速度の高速化や低価格化が要求される。ここにおいて、フォトダイオードの応答速度は基本的に

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はフォトダイオードのＣＲ時定数と、空乏層内をドリフトするキャリア（電子、正孔）の走行時間ｔとの２つの要素で制限されることが知られている。半導体結晶材料としてＳｉを用いたｐｉｎフォトダイオードを例に考えると、ＣＲ時定数を小さくするとともに量子効率（受光感度）を高めるために、広い空乏層が形成されているので、空乏層内をドリフトする電子の走行時間ｔが高速応答時には無視できなくなる。

【０００５】

例えば、Ｓｉのｐｉｎフォトダイオードで量子効率を８０％以上とするためには、３０μｍ程度の空乏層幅Ｗが必要となるが、ＣＲ時定数で決まる遮断周波数$f_c(CR)$は、受光径を２５０μｍとすると、ｐｎ接合面積Ａが$A=4.9\times10^{-4}\ cm^2$となり、空乏層幅Ｗが３０μｍとすればｐｎ接合の接合容量C_jが$C_j=0.17\ pF$となるから、外部抵抗Ｒを５０Ωとすると、$f_c(CR)=1/(2\pi C_j R)=18\ GHz$となる。

【０００６】

一方、光電流の振幅が低周波領域の振幅の$1/2^{1/2}$、すなわち、電力が１／２（－３ｄＢ）になる周波数を遮断周波数$f(t_{tr})$と定義すると、$f_c(t_{tr})=0.44/t_{tr}$となるが、Ｓｉ結晶中をドリフトする電子の飽和ドリフト速度v_{ds}が$v_{ds}=1\times10^7\ cm/sec$であるため、空乏層内をドリフトする電子の走行時間$t_{tr}$が$t_{tr}=W/v_{ds}=0.3\ nsec$となり、遮断周波数$f_c(t_{tr})$は、$f_c(t_{tr})=1.5\ GHz$となる。上述のように、受光径が２５０μｍ、空乏層幅Ｗが３０μｍのＳｉのｐｉｎフォトダイオードについては、ＣＲ時定数から決まる遮断周波数$f_c(CR)$が１８ＧＨｚであったから、このｐｉｎフォトダイオードでは上述の走行時間t_{tr}が遮断周波数を制限することとなり、１．５ＧＨｚ近辺が動作周波数の限界であることが分かる。

【０００７】

ここで、ｐｉｎフォトダイオードの応答速度の高速化を図るには、遮断周波数を大きくする必要があるので、半導体結晶中のドリフト速度がＳｉに比べて速い半導体結晶材料である化合物半導体材料やＧｅなどを用いればよいが、シリコン半導体プロセスほどは量産性に優れておらず、また、ウェハ径も小さいので、低価格化が難しい。

【０００８】

これに対して、近年、Ｓｉのｐｉｎフォトダイオード構造を有する光電変換部を基本構成とし、光電変換部においてキャリアがドリフトするドリフト領域であるｉ層の薄型化を図りながらも量子効率を向上することができ、しかもｉ層中をドリフトするキャリアの走行時間t_{tr}の短縮による高速化を図れる近赤外光検出素子が提案されている（非特許文献１，２）。

【０００９】

この種の近赤外光検出素子は、図４に示すように、Ｓｉ基板１５１の一表面上に第１のSiO_2層１５２ａとＳｉ層１５２ｂと第２のSiO_2層１５２ｃとの積層膜からなり近赤外光を反射するＤＢＲ（Distributed Bragg Reflector）１５２が設けられ、ＤＢＲ１５２上にn^+領域１６３とp^+領域１６１との間にｉ層１６２が介在するＳｉのｐｉｎフォトダイオード構造からなる光電変換部１６０が設けらており、空気とp^+領域１６１の表面からなる受光面との界面がＳｉ基板１５１の厚み方向（縦方向）において光電変換部１６０を挟んでＤＢＲ１５２に対向する反射面を形成し、当該反射面とＤＢＲ１５２とでファブリペロー共振器（Fabry-Perot Resonator）からなる縦型の共振器を形成している。したがって、光電変換部１６０におけるｉ層１６２の厚みを小さく（つまり、ｉ層１６２の幅を小さく）しても受光感度を向上することができ、ｉ層１６２の厚みを薄くすることでキャリアの走行距離も短くできるので、応答速度の高速化を図ることができる。なお、p^+領域１６１はＳｉ基板１５１の上記一表面側でｐ電極１６５と電気的に接続され、n^+領域１６３はＳｉ基板１５１の上記一表面側でｎ電極１６３と電気的に接続されている。

【非特許文献１】M.K.Emsley,et al,「Silicon Resonant Cavity Enhanced Photodetector Arrays for Optical Interconnects」, Proc. of SPIE Vol.5246,p409-421,2003

【非特許文献２】M.K.Emsley,et al,「Silicon Substrates With Buried Distributed Br

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agg Reflectors for Resonant Cavity-Enhanced Optoelectronics」, IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS,VOL.8,NO.4,p948-955,JULY/AUGUST 2002

【発明の開示】

【発明が解決しようとする課題】

【００１０】

しかしながら、図４に示した構成の近赤外光検出素子を製造するには、光電変換部１６０の形成前に、ＳＯＩウェハの形成方法の１つとして知られている水素注入剥離法で必要な基本工程（水素イオン注入工程、貼り合わせ工程、剥離工程、表面研磨工程）を２回繰り返す必要があり、製造プロセスが複雑で低コスト化が難しかった。また、上述の赤外光検出素子の製造方法はＳｉ以外の半導体結晶材料を光電変換部１６０の材料として採用する場合には適用することができない。

【００１１】

本発明は上記事由に鑑みて為されたものであり、その目的は、応答速度の高速化を図れ且つ製造が容易な近赤外光検出素子を提供することにある。

【課題を解決するための手段】

【００１２】

請求項１の発明は、半導体基板の一表面側に形成されｐ形領域とｎ形領域との間にドリフト領域が設けられたフォトダイオード構造を有し近赤外光を吸収して電子・正孔対が発生する光電変換部と、光電変換部の受光面に積層され若しくは光電変換部内における前記受光面側に形成され前記受光面に平行な２次元面内に屈折率周期構造を有するスラブ型フォトニック結晶であって前記受光面に交差する方向から入射される検出対象の近赤外光の波長帯に対して共振ピークを有するように屈折率周期構造が設計されたスラブ型フォトニック結晶とを備えてなることを特徴とする。

【００１３】

この発明によれば、半導体基板の一表面側に形成された光電変換部の受光面に積層され若しくは光電変換部内における前記受光面側に形成され前記受光面に平行な２次元面内に屈折率周期構造を有するスラブ型フォトニック結晶であって前記受光面に交差する方向から入射される検出対象の近赤外光の波長帯に対して共振ピークを有するように屈折率周期構造が設計されたスラブ型フォトニック結晶を備えていることにより、従来のような縦型の共振器を設けることなくｐｉｎフォトダイオードやアバランシェフォトダイオードなどのフォトダイオード構造の光電変換部のドリフト領域の厚さを薄くしても量子効率を高めることができるので、受光感度を低下させることなく応答速度の高速化を図れ、また、光電変換部に積層され若しくは光電変換部内における前記受光面側に形成されたスラブ型フォトニック結晶は一般的な半導体製造プロセス技術である薄膜形成技術とリソグラフィ技術とエッチング技術とを利用して形成することができるので、容易に製造することができる。

【００１４】

請求項２の発明は、請求項１の発明において、前記半導体基板の前記一表面側において前記受光面に平行な２次元面内で前記光電変換部を囲み前記波長帯の近赤外光を前記光電変換部側へ反射する近赤外光反射部を備えてなることを特徴とする。

【００１５】

この発明によれば、前記受光面に平行な２次元面内で前記光電変換部を囲み前記波長帯の近赤外光を前記光電変換部側へ反射する近赤外光反射部を備えていることにより、前記受光面を通して前記光電変換部へ入射された前記波長帯の近赤外光が前記光電変換部の側方へ漏れるのを防止することができるので、量子効率をより高めることができ、受光感度をより一層高めることができる。

【００１６】

請求項３の発明は、請求項２の発明において、前記近赤外光反射部は、前記受光面に平行な２次元面内に屈折率周期構造を有する２次元フォトニック結晶であって前記波長帯の近赤外光を前記光電変換部側へ反射するように屈折率周期構造が設計された２次元フォト

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ニック結晶からなることを特徴とする。

【００１７】

この発明によれば、前記近赤外光反射部を一般的な半導体製造プロセス技術であるリソグラフィ技術とエッチング技術とを利用して容易に形成することができる。

【００１８】

請求項４の発明は、請求項１ないし請求項３の発明において、前記光電変換部は、前記受光面に平行な２次元面内における前記ｐ形領域および前記ｎ形領域それぞれの形状が櫛形状であり、前記ｐ形領域と前記ｎ形領域とが互いに入り組んでおり、前記ドリフト領域が前記ｐ形領域と前記ｎ形領域との間に介在するｉ層からなることを特徴とする。

【００１９】

この発明によれば、前記ｐ形領域を拡散もしくはイオン注入により形成する際のマスクと前記ｎ形領域を拡散もしくはイオン注入により形成する際のマスクとの相対的な位置精度により前記ｐ形領域と前記ｎ形領域との間に介在するｉ層からなる前記ドリフト領域の厚み（ｉ層の幅）が決まるので、前記ドリフト領域の厚み寸法の精度を高めることができる。

【発明の効果】

【００２０】

請求項１の発明は、応答速度の高速化を図れ且つ容易に製造することができるという効果がある。

【発明を実施するための最良の形態】

【００２１】

（実施形態１）

本実施形態の近赤外線検出素子は、図１（ａ），（ｂ）に示すように、Ｓｉ基板からなる半導体基板１の一表面上にSiO_2膜からなる第１の誘電体層２を介して低濃度（例えば、10^{13}～$10^{16}cm^{-3}$程度）の単結晶Ｓｉ層からなる半導体層３が設けられるとともに、当該半導体層３上にSiO_2膜からなる第２の誘電体層４が設けられており、半導体層３の中央部にｐｉｎフォトダイオードのフォトダイオード構造を有し近赤外光を吸収して電子・正孔対が発生する光電変換部６が形成され、第２の誘電体層４の中央部に光電変換部６の受光面（図１（ｂ）における上面）に平行な２次元面内に屈折率周期構造を有するスラブ型フォトニック結晶であって上記受光面に交差する方向から入射（本実施形態では、半導体基板１側とは反対側から入射）される検出対象の近赤外光の波長帯に対して共振ピークを有するように屈折率周期構造が設計されたスラブ型フォトニック結晶７が形成されている。なお、本実施形態では、第１の誘電体層２および第２の誘電体層４の材料がSiO_2であり、光電変換部６の半導体結晶材料がＳｉであるので、第１の誘電体層２および第２の誘電体層４それぞれの屈折率よりも半導体層３の屈折率が高い値となっており（SiO_2の屈折率は１．５程度、Ｓｉの屈折率は３．４程度である）、光電変換部６には、受光面から入射された近赤外光を光電変換部６の両側の媒質との屈折率差により光電変換部６内に閉じ込めて導波する導波モードが存在しており、量子効率を高めることができる。

【００２２】

ここにおいて、本実施形態の近赤外光検出素子は、光通信の受光素子として用いるものであり、検出対象の近赤外光（入力信号光）の波長帯として０．８μｍ帯を想定しており、光電変換部６の半導体結晶材料としてＳｉを採用し、半導体基板１としてＳｉ基板を用いている。

【００２３】

光電変換部６は、図１（ｂ），（ｃ）に示すように、上記受光面に平行な２次元面内における形状が櫛形状のp^+層からなるｐ形領域６１と、上記受光面に平行な２次元面内における形状が櫛形状のn^+層からなるｎ形領域６３とが、互いに入り組んでおり、ｐ形領域６１とｎ形領域６３との間に上記受光面に平行な面内における形状が蛇行状（つづら折れ状）のｉ層６２が介在している。ここにおいて、ｐ形領域６１およびｎ形領域６３は円

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弧状の櫛骨部６１ａ，６３ａそれぞれに、図１（ｃ）の左右方向に等間隔で離間した複数（図示例では、３つ）の櫛歯部６１ｂ，６３ｂが連続して形成されており、図１（ｃ）の左右方向においてｐ形領域６１の櫛歯部６１ｂとｎ形領域６３の櫛歯部６３ｂとが交互に並んでいる。なお、光電変換部６は、上記受光面に平行な２次元面内における形状が、全体として円形状に形成されている。また、本実施形態では、ｉ層６２がｐ形領域６１とｎ形領域６３との間に設けられたドリフト領域を構成している。

【００２４】

また、本実施形態の近赤外光検出素子は、第２の誘電体層４においてｐ形領域６１に重なる部位にコンタクト孔が形成されており、当該コンタクト孔に埋め込まれｐ形領域６１と電気的に接続された金属材料からなるコンタクト電極８ａが、第２の誘電体層４上に形成されたパッド１０ａと金属配線９ａを介して電気的に接続されている。同様に、第２の誘電体層４においてｎ形領域６３に重なる部位にコンタクト孔が形成されており、当該コンタクト孔に埋め込まれｎ形領域６３と電気的に接続された金属材料からなるコンタクト電極８ｂが、第２の誘電体層４上に形成されたパッド１０ｂと金属配線９ｂを介して電気的に接続されている。

【００２５】

また、スラブ型フォトニック結晶７は、多数の円孔７２が、第２の誘電体層４のうち光電変換部６に積層されている部位からなるスラブ７１の厚み方向に直交する面内（つまり、光電変換部６の受光面に平行な２次元面内）で２次元的な周期構造を有するように配列されており、スラブ７１を構成する高屈折率媒質と円孔７２内の空気からなる低屈折率媒質とで上記屈折率周期構造を有するスラブ型フォトニック結晶７を構成している。具体的には、スラブ７１において、単位格子が正三角形の仮想的な２次元三角格子の各格子点に対応する各部位に円孔７２を形成することにより、スラブ型フォトニック結晶７を形成してある。言い換えれば、円孔７２はスラブ７１の厚み方向に直交する面内において三角格子状に配列されている。なお、第２の誘電体層４の材料であるSiO_2の屈折率は１．５程度、空気の屈折率は１である。

【００２６】

スラブ型フォトニック結晶７の設計にあたっては、上述のように検出対象の近赤外光の波長帯に共振ピークを有するように上記屈折率周期構造が設計されている。具体的には、例えば、スラブ型フォトニック結晶７における円孔７２の配列方向の周期（スラブ型フォトニック結晶７の屈折率周期構造の周期であって２次元三角格子の格子点間の距離）をａとすれば、周期ａは上記波長帯の赤外光の半波長程度（例えば、赤外光の波長の２分の１）に設定すればよい。なお、本実施形態の近赤外光検出素子のうちスラブ型フォトニック結晶７と光電変換部６とで構成された主要部である光伝搬部については、半導体基板１と反対側はスラブ型フォトニック結晶７とスラブ型フォトニック結晶７直上の媒質である空気（屈折率＝１）との屈折率差があり、半導体基板１側は光電変換部６直下の媒質である第１の誘電体層（屈折率＝１．５）２と屈折率差がある。このような光伝搬部では、当該光伝搬部が上下両側（半導体基板１の厚み方向の両側）それぞれで接している媒質と上述のような屈折率差があることにより、光伝搬部を伝搬する近赤外光が上下方向の全反射条件を満たして完全に光伝搬部内に閉じ込められる導波モードと、全反射条件を満たさず外部光と結合可能なモード（以下、面内共振モードと呼ぶ）とがある。このような光伝搬部に外部から近赤外光を入射すると、一部の近赤外光が面内共振モードに結合し、別の一部は面内共振モードおよび導波モードのいずれにも結合せず透過する場合もあるが、面内共振モードに結合した後に再放射される近赤外光と透過する近赤外光とが打ち消されるような場合も存在し、この場合には光伝搬部に入射された全ての近赤外光が面内共振モードに結合する。このように面内共振モードに結合した光は、共振ピークのＱ値に応じて光伝搬部内を伝搬していくことになるので、図４の従来構成のような縦型の共振器を設けることなく光電変換部６におけるｉ層６２の厚みを薄くてもｉ層６２にて近赤外光が効率良く吸収されることになる。また、本実施形態では、光伝搬部に入射される上記波長帯の近赤外光の全てが面内共振モードに結合するので、光電変換部６における受光面とは反対側にＤ

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ＢＲのような反射層を別途設ける必要もない。なお、面内共振モードは、刊行物１（Shanhui Fan,et al, 「Analysis of guided resonances in photonic crystal slabs」, PHYSICAL REVIEW B,VOLUME 65,235112）において「guided resonances」として報告されている。

【００２７】

ところで、本実施形態の近赤外光検出素子は、厚み方向の中間にSiO_2膜を有する所謂ＳＯＩ（Silicon On Insulator）基板を用いて形成してあり、ＳＯＩ基板における裏面側のＳｉ基板が半導体基板１を構成し、ＳＯＩ基板のSiO_2膜が第１の誘電体層２を構成し、ＳＯＩ基板の主表面側のＳｉ層が半導体層３を構成している。すなわち、近赤外光検出素子における光電変換部６は、ＳＯＩ基板の主表面側のＳｉ層からなる半導体層３においてｐ形領域６１およびｎ形領域６３それぞれに対応する部位に不純物を拡散もしくはイオン注入によって導入することにより形成されているので、ｐ形領域６１を拡散もしくはイオン注入により形成する際のマスクとｎ形領域６３を拡散もしくはイオン注入により形成する際のマスクとの相対的な位置精度により、半導体層３のうちｐ形領域６１とｎ形領域６３との間に介在する部位からなるｉ層６２の厚さ（ｉ層６２の幅であって、キャリアの走行距離）が決まるので、ｉ層６２の厚み寸法の精度を高めることができる。

【００２８】

また、スラブ型フォトニック結晶７は、ＳＯＩ基板の主表面側のＳｉ層からなる半導体層３に光電変換部６を形成した後で、ＳＯＩ基板の主表面側の全面に第２の誘電体層４を例えばＣＶＤ法などの薄膜形成方法により成膜してから、第２の誘電体層４上にリソグラフィ技術を利用して各円孔７２に対応する部位が開孔されたレジスト層を形成し、当該レジスト層をマスクとして第２の誘電体層４のうち各円孔７２に対応する部位をドライエッチング装置によりエッチングすることによって形成することができる。なお、スラブ７１を構成する媒質はSiO_2に限らず、例えば、Si_3N_4でもよい。

【００２９】

以上説明した本実施形態の近赤外光検出素子は、光電変換部６の受光面に積層され光電変換部６側とは反対側から入射される検出対象の近赤外光の波長帯に対して共振ピークを有するように上記受光面に平行な２次元面内の屈折率周期構造が設計されたスラブ型フォトニック結晶７を備えているので、図４に示した従来構成のような縦型の共振器を設けることなくｐｉｎフォトダイオードのフォトダイオード構造の光電変換部６のｉ層６２の厚み（幅）を薄くしても量子効率を高めることができるので、受光感度を低下させることなく応答速度の高速化を図れる。また、光電変換部６に積層されたスラブ型フォトニック結晶７は一般的な半導体製造プロセス技術である薄膜形成技術とリソグラフィ技術とエッチング技術とを利用して形成することができるので、容易に製造することができる。

【００３０】

（実施形態２）

本実施形態の近赤外光検出素子の基本構成は実施形態１と略同じであって、図２に示すように、光電変換部６におけるｐ形領域６１とｉ層６２とｎ形領域６３とが半導体基板１の厚み方向に並ぶ形で形成されている点が相違する。なお、実施形態１と同様の構成要素には同一の符号を付して説明を省略する。

【００３１】

本実施形態における光電変換部６のｐ形領域６１およびｎ形領域６３は、図２（ｃ），（ｄ）に示すように、上記受光面に平行な２次元面内における形状が円の一部を切り欠いた形状に形成されており、半導体層３のうちｐ形領域６１とｎ形領域６３との間に介在する部位がｉ層６２を構成している。なお、ｐ形領域６１およびｎ形領域６３は、半導体層３においてｐ形領域６１およびｎ形領域６３それぞれに対応する部位に不純物を拡散もしくはイオン注入によって導入することにより形成されている。

【００３２】

また、本実施形態の近赤外光検出素子は、ｐ形領域６１とｎ形領域６３とが半導体基板１の厚み方向に離間して形成されており、ｎ形領域６３が第２の誘電体層４から離れた位

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置に形成されているので、ｎ形領域６３とコンタクト電極８ｂとを電気的に接続するための拡散配線６３ｃ（図２（ｃ）参照）を半導体層３に形成してある。なお、各コンタクト電極８ａ，８ｂは、第２の誘電体層４において、ｐ形領域６１およびｎ形領域６３それぞれの周部に重なる部位に形成されている。

【００３３】

しかして、本実施形態の近赤外光検出素子も、実施形態１と同様に、受光感度を低下させることなく応答速度の高速化を図れ且つ容易に製造することができる。

【００３４】

（実施形態３）

本実施形態の近赤外光検出素子の基本構成は実施形態１と略同じであって、図３に示すように、半導体基板１の上記一表面側において光電変換部６の受光面に平行な２次元面内で光電変換部６を囲み検出対象の波長帯の近赤外光を光電変換部６側へ反射する近赤外光反射部１１を備えている点が相違する。なお、実施形態１と同様の構成要素には同一の符号を付して説明を省略する。

【００３５】

ところで、本実施形態における近赤外光反射部１１は、近赤外光反射部１１が上記受光面に平行な２次元面内に屈折率周期構造を有する２次元フォトニック結晶であり、多数の円孔１１ａが半導体層３の一部からなるスラブ１１ｂの厚み方向に直交する２次元面内で２次元的な周期構造を有するように配列されており、スラブ１１ｂを構成する高屈折率媒質（ここでは、Ｓｉ）と円孔１１ａ内の空気からなる低屈折率媒質とで上記屈折率周期構造を有する２次元フォトニック結晶を構成している。具体的には、スラブ１１ｂに、単位格子が正三角形の仮想的な２次元三角格子の各格子点に円孔１１ａを形成することにより、２次元フォトニック結晶１１を形成してある。言い換えれば、円孔１１ａはスラブ１１ｂの厚み方向に直交する面内において三角格子状に配列されている。

【００３６】

ここにおいて、２次元フォトニック結晶１１の設計にあたっては、上述のように検出対象の波長帯の近赤外光を光電変換部６側へ反射するように上記屈折率周期構造が設計されている。具体的には、例えば、２次元フォトニック結晶１１における円孔１１ａの配列方向の周期（２次元フォトニック結晶１１の屈折率周期構造の周期であって２次元三角格子の格子点間の距離）をｂとすれば、周期ｂは上記波長帯の赤外光の半波長程度（例えば、赤外光の波長の２分の１）に設定すればよい。

【００３７】

しかして、本実施形態の近赤外光検出素子では、上述の近赤外光反射部１１を備えていることにより、上記受光面を通して光電変換部６へ入射された上記波長帯の近赤外光が光電変換部６の側方へ漏れるのを防止することができるので、量子効率をより高めることができ、受光感度をより一層高めることができる。また、近赤外光反射部１１が上記受光面に平行な２次元面内に屈折率周期構造を有する２次元フォトニック結晶であって上記波長帯の近赤外光を光電変換部６側へ反射するように屈折率周期構造が設計された２次元フォトニック結晶により構成されているので、近赤外光反射部１１を一般的な半導体製造プロセス技術であるリソグラフィ技術とエッチング技術とを利用して容易に形成することができる。なお、本実施形態では、２次元フォトニック結晶１１をＳｉと空気との２種類の媒質の周期構造により構成しているが、円孔１１ａをＳｉとは屈折率の異なる誘電体材料（例えば、SiO_2など）により充実して当該誘電体材料とＳｉとで２次元フォトニック結晶１１を形成するようにしてもよい

ところで、上記各実施形態では、光電変換部６の半導体結晶材料としてＳｉを採用し、半導体基板１としてＳｉ基板を用いているが、光電変換部６の半導体結晶材料はＳｉに限らず、例えば、Ｇｅや化合物半導体結晶材料でもよく、半導体基板１もＳｉ基板に限らず、例えば、Ｇｅ基板やＧａＡｓ基板などでもよい。また、上記各実施形態では、スラブ型フォトニック結晶７をSiO_2と空気との２種類の媒質の周期構造により構成していたが、円孔７２内をSiO_2とは屈折率の異なる誘電体材料により充実して当該誘電体材料と

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SiO_2とでスラブ型フォトニック結晶７を形成するようにしてもよいし、あるいは３種類以上の媒質の周期構造としてもよく、例えば、SiO_2からなるスラブ７１に設けた円孔７２の内周面を被覆するSi_3N_4膜を形成することによってSiO_2とSi_3N_4と空気との３種類でスラブ型フォトニック結晶７を構成するようにしてもよい。

【００３８】

また、上記各実施形態では、スラブ型フォトニック結晶７を光電変換部６の受光面に積層してあるが、スラブ型フォトニック結晶７を光電変換部６に積層する代わりに、光電変換部６内における受光面側に形成するようにしてもよい。また、上記各実施形態では、光電変換部６がｐ形領域６１とｎ形領域６３との間にドリフト領域６２としてｉ層が設けられたｐｉｎフォトダイオードのフォトダイオード構造を有しているが、光電変換部６はｐ形領域６１とｎ形領域６３との間にドリフト領域が設けられていればアバランシェフォトダイオードのフォトダイオード構造でもよい。

【００３９】

また、上記各実施形態におけるスラブ型フォトニック結晶７は、スラブ７１に対して、単位格子が正三角形の仮想的な２次元三角格子の各格子点に対応する各部位に円孔７２を形成することにより形成されているが、単位格子は正三角形に限らず、例えば正方形でもよく、この場合には単位格子が正方形の仮想的な２次元正方格子の各格子点に対応する部位に円孔７２を形成すればよい。また、上記各実施形態では、スラブ型フォトニック結晶７の屈折率周期構造を形成するためにスラブ７１に多数の円孔７２を形成してあるが、円孔７２を設ける代わりに、例えば三角形状の孔や四角形状の孔など別の開口形状の孔を設けてもよい。

【図面の簡単な説明】

【００４０】

【図１】実施形態１を示し、（ａ）は概略平面図、（ｂ）は（ａ）のＡ－Ａ’で破断した概略斜視図、（ｃ）は水平断面図である。

【図２】実施形態２を示し、（ａ）は概略平面図、（ｂ）は（ａ）のＡ－Ａ’で破断した概略斜視図、（ｃ）は水平断面図、（ｄ）は他の水平断面図である。

【図３】実施形態３を示し、（ａ）は概略平面図、（ｂ）は（ａ）のＡ－Ａ’で破断した概略斜視図、（ｃ）は水平断面図である。

【図４】従来例を示す概略断面図である。

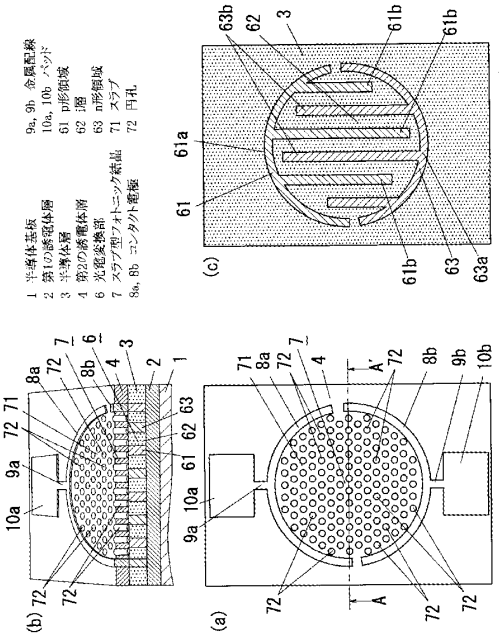
【符号の説明】

【００４１】

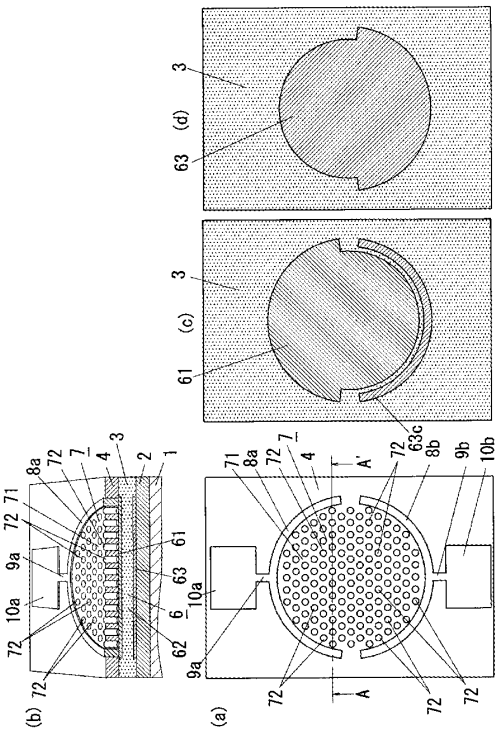
１　半導体基板
２　第１の誘電体層
３　半導体層
４　第２の誘電体層
６　光電変換部
７　スラブ型フォトニック結晶
８ａ，８ｂ　コンタクト電極
９ａ，９ｂ　金属配線
１０ａ，１０ｂ　パッド
６１　ｐ形領域
６２　ｉ層
６３　ｎ形領域
７１　スラブ
７２　円孔

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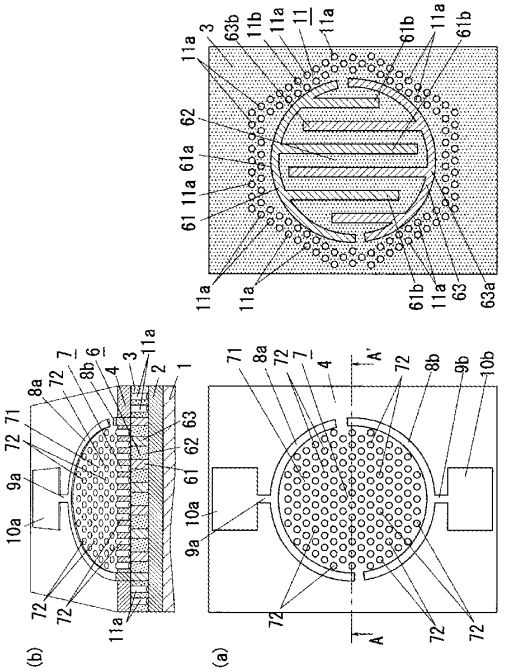
【図１】


1 半導体基板
2 第1の誘電体層
3 半導体層
4 第2の誘電体層
6 光電変換部
7 スライス型フォトニック結晶
8a, 8b コンタクト電極
9a, 9b 金属配線
10a, 10b バンド
61 p形領域
62 i層
63 n形領域
71 スライス
72 円孔
(a)
(b)
(c)

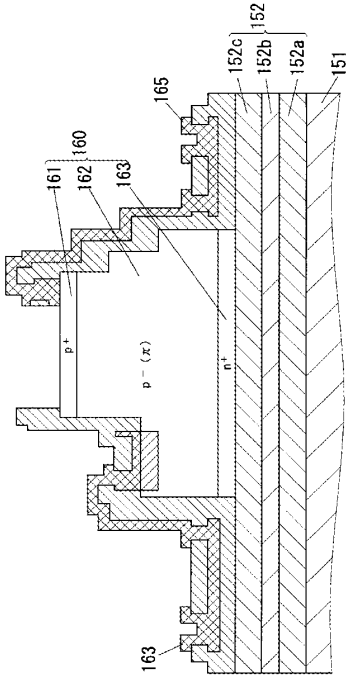
【図２】


(a)
(b)
(c)
(d)

【図３】


(a)
(b)

【図４】


151
152
152a
152b
152c
160
161
162
163
165
p+
p−(π)
n+

Lateral semiconductor photodetector of pin structure

Abstract

PROBLEM TO BE SOLVED: To provide a PIN structure lateral semiconductor photodetector which is improved in sensitivity for detecting light without deteriorating its response speed. SOLUTION: A lateral semiconductor photodetector of PIN structure has interfaces at an I layer 15, a P layer 5, and an N layer, the interfaces are set vertical to the surface of a semiconductor substrate, light impinging on the I layer 15 is converted into a current, and the current is detected. A hole 4 is bored in a light receiving region 2 from a light receiving surface 3 to a certain point as deep as prescribed inside the I layer 15

JP2002314116A

Japan

Find Prior Art Similar

Other languages: Japanese

Inventor: Atsushi Harada, 篤 原田, Tsugio Ide, 次男 井出, Shojiro Kitamura, 庄二郎 北村

Current Assignee : Seiko Epson Corp

Worldwide applications

2001 JP

Application JP2001110168A events

2001-04-09 Application filed by Seiko Epson Corp

2001-04-09 Priority to JP2001110168A

2002-10-25 Publication of JP2002314116A

Status Withdrawn

Info: Cited by (7), Legal events, Similar documents, Priority and Related Applications

External links: Espacenet, Global Dossier, Discuss

Claims (1)

Hide Dependent

translated from Japanese

[Claims] 1. A lateral semiconductor light receiving device wherein an interface between an I-layer, a p-layer, and an n-layer having a PIN structure is formed perpendicular to a surface of a semiconductor substrate, and converts light incident on the I-layer into current and detects the current. A lateral semiconductor light-receiving element having a PIN structure, wherein a hole extending from the light-receiving surface to a predetermined depth of the I-layer is provided in the light-receiving region.

Description

translated from Japanese

DETAILED DESCRIPTION OF THE INVENTION

[0001]

The present invention relates to a lateral semiconductor light receiving device having a PIN structure.

[0002]

2. Description of the Related Art In a vertical photodiode in which a pn junction surface is formed parallel to a semiconductor substrate surface, light is incident on a depletion layer through a p-layer or an n-layer.
In a lateral photodiode in which the n-junction surface is formed perpendicular to the semiconductor substrate surface, light is directly incident on the depletion layer (not through the p-layer or the n-layer). For this reason, lateral photodiodes are better than vertical photodiodes.
This is advantageous in light receiving efficiency.

Conventionally, in a photodiode,
An I layer (intrinsic layer) is provided between a p layer and an n layer to increase the thickness of a depletion layer. In a vertical photodiode having such a PIN structure, the I-layer is formed to have a thickness equal to or more than the absorption length in order to increase the light receiving sensitivity. As a result, a quantum efficiency of 70% or more can be obtained at a wavelength of about 700 nm to 870 nm.

Lateral photodiode having a PIN structure (a photodiode in which an interface between an I-layer, a p-layer, and an n-layer having a PIN structure is formed perpendicular to a semiconductor substrate surface)
For example, after a region having an extremely low impurity concentration forming an I-layer is provided in a surface layer portion of a semiconductor substrate, a p-type impurity and an n-type impurity are added to respective positions of this region at predetermined intervals from an upper surface. To form a p-layer and an n-layer, and leave an I-layer between both layers

Therefore, in the case of a lateral photodiode having a PIN structure, the thickness of the I-layer (depth from the light incident surface)
in order to increase p, it is necessary to form the p-layer and the n-layer deeply. In order to form the p-layer and the n-layer deep while keeping the width of the I-layer (the distance between the p-layer and the n-layer) uniform in the thickness direction of the substrate, the p-layer and the n-layer on the substrate surface must be If is

necessary to increase the distance. When the distance between the p-layer and the n-layer on the substrate surface is increased, the width of the i-layer increases. If the width of the i-layer is large, the movement distance of electrons generated on the p-layer side of the i-layer to reach the electrode of the n-layer increases, and the response speed decreases.

Therefore, in the lateral type photodiode having the PIN structure, as a method for increasing the light receiving sensitivity, simply increasing the thickness of the i-layer (the depth from the light incident surface) cannot be simply employed. Therefore, PIN
As a method for increasing the light receiving sensitivity of the lateral type photodiode having the structure, it is effective to provide an antireflection film on the upper surface of the i-layer to increase the efficiency of incidence on the i-layer.

[0007]

However, a lateral type photodiode having a PIN structure having an antireflection film on the upper surface of the i-layer has a problem that the response speed is low when an element for receiving a high-speed signal is used. There is. SUMMARY OF THE INVENTION The present invention has been made in view of such a problem of the related art, and it is an object of the present invention to improve the light receiving sensitivity without lowering the response speed in a lateral semiconductor light receiving element having a PIN structure.

[0008]

In order to solve the above-mentioned problems, the present invention provides a semiconductor device having an i-layer having a PIN structure in which an interface between a p-layer and an n-layer is formed perpendicular to a semiconductor substrate surface. In a lateral type semiconductor light receiving element for detecting incident light by converting the light into a current, a hole extending from the light receiving surface to a predetermined depth of the i layer (a position shallower than the depths of the p layer and the n layer) is provided in the light receiving region. A lateral type semiconductor light receiving element having a PIN structure is provided.

[0009]

Embodiments of the present invention will be described below. FIG. 1 is a sectional view showing a photodiode corresponding to one embodiment of the present invention. FIG. 2 is a diagram showing an example of a planar shape when the photodiodes of this embodiment are formed in an array. FIG. 1 corresponds to a sectional view taken along line AA of FIG.

This photodiode is a lateral photodiode (semiconductor light receiving element) having a PIN structure formed perpendicular to the substrate surface of a silicon substrate (semiconductor substrate) 1 and has a light receiving region (p layer of i layer 15). A hole 4 extending in a direction perpendicular to the surface of the silicon substrate 1 from the light receiving surface 3 to a predetermined depth of the i-layer 15 is provided in a region (a region between the n-layer 5 and the n-layer 7).

On the upper surfaces of the p layer 5 and the n layer 7, a p electrode 6
And an n electrode 8 are formed. On the lower surface of the silicon substrate 1, a p-electrode 11 is formed. An element protection layer 9 made of a silicon oxide film or the like is provided on the upper surface of the silicon substrate 1 except for the positions of the electrodes 6 and 8 and the hole 4.
is formed with a predetermined thickness. This photodiode can be manufactured, for example, by the following method.

First, n is added to the surface layer of the p-type silicon substrate 1.
A well (a region having an extremely low impurity concentration) 10 is provided.
Next, a p-type impurity is added to one of the two regions of the n-well 10 at a predetermined interval, and an n-type impurity is added to the other, and diffused. As a result, the p layer 5 and the n layer 7 are formed in the n well 10, and the portion between the p layer 5 and the n layer 7 of the n well 10 remains as the i layer 15. Next, after forming the electrodes 6 and 8 on the p-layer 5 and the n-layer 7, the element protection layer 9 is formed.

Next, a focused ion beam processing apparatus (FI
Using B), a portion of the upper surface of the silicon substrate 1 sandwiched between the electrodes 6 and 8 is irradiated with an ion beam, and the element protection layers 9 and i are irradiated.
By etching the layer 15, a hole 4 extending in the thickness direction of the silicon substrate 1 from the light receiving surface 3 to a predetermined depth of the i layer 15 (a position shallower than the depths of the p layer 5 and the n layer 7) is formed.

Here, the dimension of the hole 4 in the direction between the p layer 5 and the n layer 7 is determined between the hole 4 and the p layer 5 and between the hole 4 and the n layer 7. is set to the dimension where exists. When the light receiving surface 3 between each pair of electrodes is large, it is preferable to provide a plurality of holes 4 in the light receiving surface 3 as shown in FIG. In this case, for example, the width W of the electrodes 6 and 8
1 is 1 μm, the interval W2 between the electrodes 6 and 8 is 2 to 4 μm, and the hole 4
is 2 to 4 μm, and the diameter of the hole 4 is 1 μm.

In this photodiode, a power supply is connected between the n-electrode 8 in contact with the upper surface of the n-layer 7 and the p-electrode 11 on the lower surface of the substrate 1 with the n-layer 7 side being positive and a reverse bias voltage applied. Then, by connecting the p-electrode 6 in contact with the upper surface of the p-layer 5 to the output circuit, light incident on the i-layer 15 from the light receiving surface 3 can be converted into a current and detected. Also,
In this photodiode, the light (partially shown by a two-dot chain line in FIG. 1) that has entered the hole 4 from the light receiving surface 3 directly enters the light receiving region 2 from the bottom or side surface of the hole 4 and By being reflected on the side surface, the light is incident on the light receiving region 2 from the bottom surface to the side surface, or is incident on the light receiving region 2 from the side surface toward the opposing side surface. Therefore, the light receiving efficiency in the light receiving region 2 is higher than in the case where there is no hole 4.

If the light receiving surface 3 is simply enlarged without providing the hole 4 in order to increase the light receiving area, it takes a long time for electrons generated on the p layer side of the i layer to reach the electrode of the n layer. As the parasitic capacitance increases, the response speed decreases. In contrast, in this photodiode, By providing the hole 4, the light receiving area is larger by the side surface of the hole 4 than when no hole 4 is provided. Therefore, in this photodiode, electrons generated on the p-layer side of the i-layer are n
The movement time until reaching the electrode of the layer is not longer than when the light receiving surface 3 is the same size and the hole 4 is not provided.
The parasitic capacitance of the photodiode is smaller than that in the case where the light receiving surface 3 has the same size and the hole 4 is not provided. For these reasons, according to this photodiode, the light receiving area can be increased and the light receiving efficiency can be increased without reducing the response speed.

Further, since the photodiode has the hole 4, the intensity of the electric field applied to the peripheral portion of the hole 4 of the i-layer 15 is locally increased. This allows
Since holes and electrons generated by absorbing light in the peripheral portion of the hole 4 of the i-layer 15 can move at high speed through the i-layer 15,
The response speed is faster than the case without the hole 4. Therefore, according to this photodiode, by providing the hole 4, the light receiving efficiency in the light receiving region 2 is increased, the light receiving sensitivity is improved, and the response speed is also increased.

In this embodiment, a lateral type photodiode having a PiN structure is described. However, the lateral type semiconductor light receiving element having a PIN structure of the present invention is not limited to this. It is also applied to the lateral type phototransistor and the like.

[0019]

As described above, according to the lateral semiconductor light receiving device having the PIN structure of the present invention, the light receiving sensitivity can be improved without lowering the response speed.

[Brief description of the drawings]

FIG. 1 is a cross-sectional view showing a photodiode corresponding to an embodiment of the present invention, and is a view corresponding to a cross-sectional view taken along line AA of FIG.

FIG. 2 is a diagram showing an example of a planar shape when the photodiodes of FIG. 1 are formed in an array.

[Explanation of symbols]

REFERENDE SIGNS LIST 1 silicon substrate (semiconductor substrate) 10 n-well 11 p-electrode 15 i-layer 2 light-receiving area 3 light-receiving surface 4 hole 5 p-layer 6 p-electrode 7 n-layer 8 n-electrode 9 element protection layer

---------- Continuing on the front page (72) Inventor Shojiro Kitamura 3-3-5 Yamato, Suwa-shi, Nagano F-term (reference) in Seiko Epson Corporation 5F049 MA04 MB03 NA01 NA03 NA15 PA14 PA20 QA01 QA20 SZ13

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KR100676733B1	2007-02-23	UV detector having NIP Structure
Hinckley et al.	2002	Modelling of device structure effects on electrical crosstalk in back illuminated CMOS compatible photodiodes
JP2000252512A	2000-09-14	Pin photo-diode
KR100424366B1	2004-03-24	A Photodiode With A Diffusion-Layer Of Dispersion-Distribution Pattern And Fabrication Method Thereof And A Substrate And An Electronic Machine Thereby
US8829432B2	2012-10-23	High quantum efficiency optical detectors
US20210234057A1	2021-07-29	Single photon avalanche diode device
JPH10190041A	1998-07-21	Photodiode
JP2020161739A	2020-10-01	Photodetector
JP4951552B2	2012-06-13	Semiconductor photodetection device

Priority And Related Applications

Priority Applications (1)

Application	Priority date	Filing date	Title
JP2001110168A	2001-04-09	2001-04-09	Lateral semiconductor photodetector of pin structure

Applications Claiming Priority (1)

Application	Filing date	Title
JP2001110168A	2001-04-09	Lateral semiconductor photodetector of pin structure

Legal Events

Date	Code	Title	Description
2006-07-01	A300	Withdrawal of application because of no request for examination	**Free format text**: JAPANESE INTERMEDIATE CODE: A300 **Effective date**: 20060701

Concepts

machine-extracted

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Name	Image	Sections	Count	Query match
semiconductor		title,claims,abstract,description	22	0.000
substrate		claims,abstract,description	22	0.000
sensitivity		abstract,description	7	0.000
deteriorative		abstract	1	0.000

Show all concepts from the description section

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審査請求　未請求　請求項の数１　ＯＬ　（全　４　頁）

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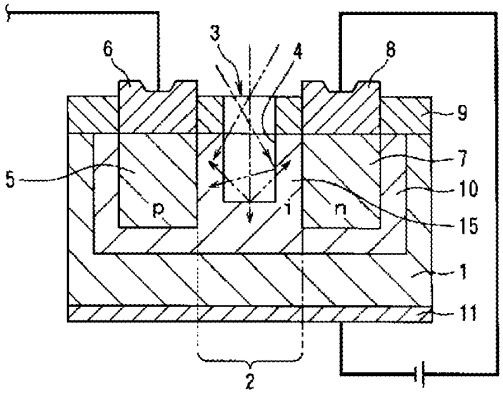
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最終頁に続く

(54)【発明の名称】　ＰＩＮ構造のラテラル型半導体受光素子

(57)【要約】　（修正有）
【課題】応答速度を低下させることなく受光感度を向上させたＰＩＮ構造のラテラル型半導体受光素子を提供する。
【解決手段】ＰＩＮ構造のｉ層１５とｐ層５とｎ層７との界面が半導体基板面に対して垂直に形成され、ｉ層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、受光領域２に、受光面３からｉ層１５の所定深さまで延びる穴４を設けた。



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【特許請求の範囲】

【請求項１】　ＰＩＮ構造のｉ層とｐ層およびｎ層との界面が半導体基板面に対して垂直に形成され、ｉ層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、

受光領域に、受光面からｉ層の所定深さまで延びる穴を設けたことを特徴とするＰＩＮ構造のラテラル型半導体受光素子。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、ＰＩＮ構造のラテラル型半導体受光素子に関する。

【０００２】

【従来の技術】ｐｎ接合面が半導体基板面に対して平行に形成されている縦型フォトダイオードでは、ｐ層またはｎ層を通して空乏層に光が入射されるのに対して、ｐｎ接合面が半導体基板面に対して垂直に形成されているラテラル型フォトダイオードでは、空乏層に直接（ｐ層やｎ層を介さずに）光が入射される。そのため、ラテラル型フォトダイオードは縦型フォトダイオードよりも、受光効率の点で有利である。

【０００３】従来より、フォトダイオードにおいては、ｐ層とｎ層との間にｉ層（真性層）を設けて、空乏層を厚くすることが行われている。このようなＰＩＮ構造を有する縦型フォトダイオードでは、受光感度を高くするために、ｉ層を吸収長以上の厚さに形成することが行われている。これにより、波長７００ｎｍ～８７０ｎｍ前後において、７０％以上の量子効率が得られるようになる。

【０００４】ＰＩＮ構造のラテラル型フォトダイオード（ＰＩＮ構造のｉ層とｐ層およびｎ層との界面が半導体基板面に対して垂直に形成されたフォトダイオード）は、例えば、ｉ層をなす不純物濃度の極めて薄い領域を半導体基板の表層部に設けた後、この領域の所定間隔を開けた各位置に、上面からｐ型不純物及びｎ型不純物をそれぞれ添加して拡散させることによりｐ層及びｎ層を形成し、両層の間をｉ層として残すことによって作製される。

【０００５】そのため、ＰＩＮ構造のラテラル型フォトダイオードの場合にｉ層の厚さ（光入射面からの深さ）を大きくしようとすると、ｐ層及びｎ層を深く形成する必要がある。基板の厚さ方向でｉ層の幅（ｐ層とｎ層との距離）を均一に保持しながら、ｐ層及びｎ層を深く形成するためには、基板表面でのｐ層とｎ層との距離を大きくとる必要がある。基板表面でのｐ層とｎ層との距離を大きくとるとｉ層の幅が大きくなる。ｉ層の幅が大きいと、ｉ層のｐ層側で生じた電子がｎ層の電極に達するまでの移動距離が長くなって、応答速度が遅くなる。

【０００６】したがって、ＰＩＮ構造のラテラル型フォトダイオードでは、受光感度をより高くする方法として、ｉ層の厚さ（光入射面からの深さ）を大きくすることを単純に採用することができない。そのため、ＰＩＮ構造のラテラル型フォトダイオードの受光感度をより高くする方法としては、ｉ層の上面に反射防止膜を設けてｉ層への入射効率を高くすることが有効である。

【０００７】

【発明が解決しようとする課題】しかしながら、ｉ層の上面に反射防止膜を有するＰＩＮ構造のラテラル型フォトダイオードには、高速の信号を受光する素子とした場合に応答速度が低くなるという問題点がある。本発明は、このような従来技術の問題点に着目してなされたものであり、ＰＩＮ構造のラテラル型半導体受光素子において、応答速度を低下させることなく受光感度を向上させることを課題とする。

【０００８】

【課題を解決するための手段】上記課題を解決するために、本発明は、ＰＩＮ構造のｉ層とｐ層およびｎ層との界面が半導体基板面に対して垂直に形成され、ｉ層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、受光領域に、受光面からｉ層の所定深さ（ｐ層およびｎ層の深さより浅い位置）まで延びる穴を設けたことを特徴とするＰＩＮ構造のラテラル型半導体受光素子を提供する。

【０００９】

【発明の実施の形態】以下、本発明の実施形態について説明する。図１は本発明の一実施形態に相当するフォトダイオードを示す断面図である。図２は、この実施形態のフォトダイオードがアレイ状に形成されている場合の平面形状の一例を示す図である。図１は図２のＡ－Ａ線断面図に相当する。

【００１０】このフォトダイオードは、ＰＩＮ構造がシリコン基板（半導体基板）１の基板面に対して垂直に形成されたラテラル型フォトダイオード（半導体受光素子）であり、受光領域（ｉ層１５のｐ層５とｎ層７とで挟まれた領域）２に、受光面３からｉ層１５の所定深さまで、シリコン基板１面に垂直に延びる穴４が設けてある。

【００１１】ｐ層５およびｎ層７の上面には、ｐ電極６およびｎ電極８がそれぞれ形成されている。シリコン基板１の下面にはｐ電極１１が形成されている。また、シリコン基板１の上面の両電極６，８および穴４の位置を除いた部分に、シリコン酸化膜等からなる素子保護層９が所定の厚さで形成されている。このフォトダイオードは、例えば以下の方法で作製できる。

【００１２】先ず、ｐ型のシリコン基板１の表層部にｎウエル（不純物濃度の極めて薄い領域）１０を設ける。次に、ｎウエル１０の所定間隔を開けた２つの領域の一方にｐ型不純物を、他方にｎ型不純物をそれぞれ添加して拡散させる。これにより、ｎウエル１０にｐ層５及びｎ層７が形成され、ｎウエル１０のｐ層５とｎ層７との

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間の部分がｉ層１５として残る。次に、ｐ層５及びｎ層７の上に電極６，８を形成した後、素子保護層９を形成する。

【００１３】次に、集束イオンビーム加工装置（ＦＩＢ）を用い、シリコン基板１上面の両電極６，８で挟まれた部分にイオンビームを照射して、素子保護層９とｉ層１５をエッチングすることにより、受光面３からｉ層１５の所定深さ（ｐ層５およびｎ層７の深さより浅い位置）まで、シリコン基板１の厚さ方向に延びる穴４を開ける。

【００１４】ここで、穴４のｐ層５－ｎ層７間方向の寸法は、穴４とｐ層５との間および穴４とｎ層７との間にそれぞれ所定厚さのｉ層１５が存在する寸法に設定する。また、各電極対間の受光面３が大きい場合には、図２に示すように、受光面３内に複数の穴４を設けることが好ましい。この場合には、例えば、電極６，８の幅Ｗ１を１μｍ、電極６，８の間隔Ｗ２を２～４μｍ、穴４のピッチＫを２～４μｍ、穴４の直径を１μｍとする。

【００１５】このフォトダイオードは、ｎ層７の上面に接触するｎ電極８と基板１の下面のｐ電極１１との間に、ｎ層７側を正として電源を接続して逆バイアス電圧を付与し、ｐ層５の上面に接触するｐ電極６を出力回路に接続することにより、受光面３からｉ層１５に入射された光を電流に変換して検出することができる。また、このフォトダイオードでは、受光面３から穴４内に入射された光（一部を図１に２点鎖線で表示）は、穴４の底面や側面から受光領域２に直接入射するとともに、底面や側面で反射されることで、底面から側面に向かって受光領域２に入射されたり、側面から対向する側面に向かって受光領域２に入射されたりする。そのため、穴４が無い場合よりも受光領域２での受光効率が高くなる。

【００１６】受光面積を大きくするために穴４を設けず単純に受光面３を大きくした場合には、ｉ層のｐ層側で生じた電子がｎ層の電極に達するまでの移動時間が長くなるとともに、寄生容量が大きくなるため、応答速度が遅くなる。これに対して、このフォトダイオードでは、穴４を設けることで、穴４が無い場合よりも穴４の側面の分だけ受光面積が大きくなっている。そのため、このフォトダイオードでは、ｉ層のｐ層側で生じた電子がｎ層の電極に達するまでの移動時間が、受光面３が同じ大きさで穴４を設けない場合よりも長くなることはない。また、このフォトダイオードの寄生容量は、受光面３が同じ大きさで穴４を設けない場合よりも小さくなる。これらのことから、このフォトダイオードによれば、応答速度を遅くすることなく、受光面積を大きくして受光効率を高くすることができる。

【００１７】さらに、このフォトダイオードは、穴４を有することによって、ｉ層１５の穴４の周囲部分に掛かる電界強度が局所的に大きくなっている。これにより、ｉ層１５の穴４の周囲部分で光を吸収して発生した正孔と電子はｉ層１５を高速で移動することができるため、穴４の無い場合と比較して応答速度が速くなる。したがって、このフォトダイオードによれば、穴４を設けることによって、受光領域２での受光効率が高くなって受光感度が向上するとともに、応答速度も高くなる。

【００１８】なお、この実施形態では、ＰＩＮ構造のラテラル型フォトダイオードについて説明しているが、本発明のＰＩＮ構造のラテラル型半導体受光素子はこれに限定されず、ベースとコレクタの部分がＰＩＮ構造になっているラテラル型フォトトランジスタ等にも適用される。

【００１９】

【発明の効果】以上説明したように、本発明のＰＩＮ構造のラテラル型半導体受光素子によれば、応答速度を低下させることなく受光感度を向上させることができる。

【図面の簡単な説明】

【図１】本発明の一実施形態に相当するフォトダイオードを示す断面図であって、図２のＡ－Ａ線断面図に相当する図である。

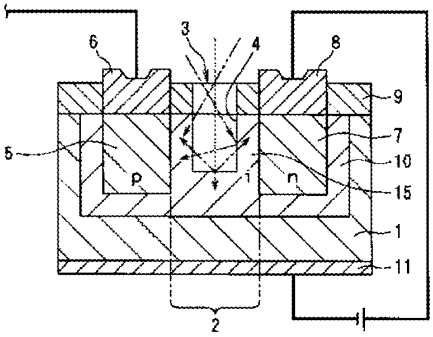
【図２】図１のフォトダイオードがアレイ状に形成されている場合の平面形状の一例を示す図である。

【符号の説明】

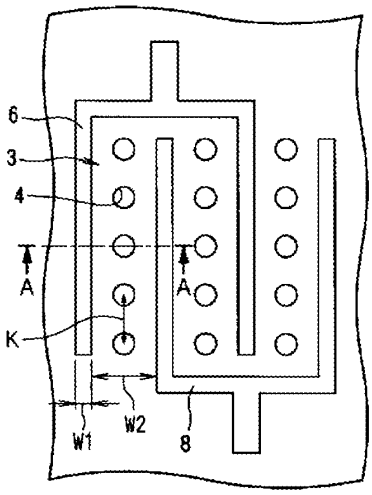
１　シリコン基板（半導体基板）
１０　ｎウエル
１１　ｐ電極
１５　ｉ層
２　受光領域
３　受光面
４　穴
５　ｐ層
６　ｐ電極
７　ｎ層
８　ｎ電極
９　素子保護層

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【図１】



【図２】



フロントページの続き

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Ｆターム(参考)　5F049 MA04 MB03 NA01 NA03 NA15 PA14 PA20 QA01 QA20 SZ13

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIPDIV
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

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Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
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Inventor 2 Remove

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Prefix	Given Name	Middle Name	Family Name	Suffix
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Postal Code	90422	Country	US

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIPDIV
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

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Application Information:

Title of the Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES		
Attorney Docket Number	309-0015USCIPDIV	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	48	**Suggested Figure for Publication (if any)**	5B

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For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

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☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIPDIV
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Division of	18385213	2023-10-30

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18385213	Continuation in part of	17974325	2022-10-26	11830954	2023-11-28

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
18385213	Continuation in part of	18113474	2023-02-23

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18113474	Division of	17707429	2022-03-29	11621360	2023-04-04

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17707429	Continuation in part of	17182954	2021-02-23	11791432	2023-10-17

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17182954	Division of	16528958	2019-08-01	11121271	2021-09-14

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	15797821	2017-10-30	10446700	2019-10-15

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18113474	Continuation in part of	17707429	2022-03-29	11621360	2023-04-04

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIPDIV
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17707429	Division of	17532832	2021-11-22	11309444	2022-04-19
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17532832	Continuation in part of	17182954	2021-02-03	11791432	2023-10-17
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17182954	Division of	16528958	2019-08-01	11121271	2021-09-14
Prior Application Status	Expired			Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
16528958	Continuation in part of	PCTUS1667977	2016-12-21		
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16042535	2018-07-23	10700225	2020-06-30
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16296985	2019-03-08	10468543	2019-10-16
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
18113474	Division of	177077429	2022-03-29	11621360	2023-04-04
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
177077429	Division of	17532831	2021-11-22	11309444	2022-04-19
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17532831	Continuation in part of	17182954	2021-02-23	11791432	2023-10-17
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17182954	Division of	16528958	2019-08-01	11121271	2021-09-14

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIPDIV
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	14947718	2015-11-20	10622498	2020-03-25

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Continuation in part of	PCTUS1667977	2016-12-21

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	15797821	2017-10-20	10446700	2019-09-25

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16042535	2018-07-23	10700225	2020-06-30

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	16296985	2019-03-08	10468543	2019-10-16

Prior Application Status	Abandoned		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Continuation in part of	PCTUS1843289	2018-07-23

Prior Application Status	Abandoned		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Continuation in part of	PCTUS1857963	2018-10-29

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62713455	2018-08-01

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62716310	2018-08-08

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIPDIV
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62717750	2018-08-08
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62719689	2018-08-19
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62724449	2018-08-29
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16528958	Claims benefit of provisional	62733476	2018-09-19

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/737062	2018-09-26
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/750016	2018-10-24
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/770656	2018-09-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/772498	2018-09-28
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/777157	2018-12-09
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/779693	2018-12-14
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/784342	2018-12-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/794330	2019-01-18
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/797141	2019-01-25

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/797263	2019-01-26
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/800371	2019-02-01
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/802171	2019-02-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/802718	2019-02-08
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/805850	2019-02-14
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/808949	2019-02-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/819604	2019-03-17
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/819669	2019-03-17
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/820695	2019-03-19

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/828976	2019-04-03
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/841798	2019-05-01
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/843206	2019-05-03
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/846554	2019-05-10
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/853280	2019-05-28
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/860115	2019-06-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/863231	2019-06-18
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/863852	2019-06-19
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/867186	2019-06-26

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Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/868911	2019-06-29
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/870533	2019-07-03
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/873891	2019-07-13
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/528958	Claims benefit of provisional	62/874418	2019-07-15
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
PCT/US18/57963	Continuation of	15/797821	2017-10-30	10446700	2019-10-15
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/797821	Continuation in part of	14/947718	2015-11-20	10622498	2020-03-25
Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/797821	Continuation in part of	15/309922	2016-11-09	9818893	2017-10-25

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Continuation in part of	PCT/US16/67977	2016-12-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/465734	2017-03-01

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Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/474179	2017-03-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/484474	2017-04-12
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/487606	2017-04-20
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/488998	2017-04-24
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/500581	2017-05-03
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/505974	2017-05-14
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/509093	2017-05-20
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/510249	2017-05-23
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/514889	2017-06-04

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Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/521504	2017-06-18
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/522169	2017-06-20
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/527962	2017-06-30
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/530281	2017-07-19
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/533078	2017-07-16
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/533603	2017-07-17
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/535801	2017-07-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/540524	2017-08-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/542243	2017-08-07

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Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/547728	2017-08-18
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/553844	2017-09-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/556426	2017-09-10
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/797821	Claims benefit of provisional	62/561869	2017-09-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/542243	2017-08-07
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/535801	2017-07-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/540524	2017-08-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/639472	2018-03-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/628764	2018-02-09

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/643010	2018-03-14
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/640522	2018-03-08
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/599246	2017-12-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/645810	2018-03-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/666005	2018-05-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/556426	2017-09-10
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/607860	2017-12-19
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/631630	2018-02-17
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/677609	2018-05-29

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/634692	2018-02-23
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/652830	2018-04-04
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/591072	2017-09-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/639356	2018-03-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/615314	2018-01-09
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/623971	2018-01-30
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/561869	2017-09-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/637945	2018-03-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/651053	2018-03-30

PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/553844	2017-09-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/682909	2018-06-09
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/659072	2018-04-17
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/659067	2018-04-17
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/669194	2018-05-09
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/675130	2018-05-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/547728	2017-08-18
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/651087	2018-03-31
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/646871	2018-03-22

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/662217	2018-04-24
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/639920	2018-03-07
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US18/43289	Claims benefit of provisional	62/633514	2018-02-21
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/296985	Continuation of	15/797821	2017-10-30	10446700	2019-10-15

Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/042535	Continuation in part of	15/797821	2017-10-30	10446700	2019-10-15

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/535801	2017-07-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/540524	2017-08-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/542243	2017-08-07
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/547728	2017-08-18

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/553844	2017-09-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/556426	2017-09-10
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/561869	2017-09-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/591072	2017-11-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/599246	2017-12-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/607860	2017-12-19
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/615314	2018-01-09
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/623971	2018-01-30
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/628764	2018-02-09

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/631630	2018-02-17
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/633514	2018-02-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/634692	2018-02-23
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/637945	2018-03-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/639356	2018-03-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/639472	2018-03-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/639920	2018-03-07
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/640522	2018-03-08
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/643010	2018-03-14

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/645810	2018-03-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/646871	2018-03-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/651053	2018-03-30
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/651087	2018-03-31
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/652830	2018-04-04
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/659067	2018-04-17
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/659072	2018-04-17
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/662217	2018-04-24
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/666005	2018-05-02

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/669194	2018-05-09
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/675130	2018-05-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/677609	2018-05-29
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/042535	Claims benefit of provisional	62/682909	2018-06-09
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/270577	2015-12-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/304907	2016-03-07
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/290391	2016-02-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/334934	2016-05-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/338263	2016-05-18

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/346850	2016-06-07
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/359349	2017-07-07
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/366188	2016-07-25
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/368109	2016-07-28
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/374828	2016-08-13
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/376869	2016-08-18
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/380364	2016-08-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/383391	2016-09-03
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/383479	2016-09-04

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/394222	2016-09-14
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/398607	2016-09-23
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/401126	2016-09-28
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/406999	2016-10-12
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/414671	2016-10-29
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US16/67977	Claims benefit of provisional	62/415339	2016-10-31
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15/309922	a 371 of international	PCT/US15/61120	2015-11-17
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/309922	Continuation of	14/943898	2015-11-17	9530905	2016-12-27
Prior Application Status	Patented				Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/309922	Continuation of	14/945003	2015-11-18	9525084	2016-12-20

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/213558	2015-09-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/199607	2015-07-13
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/188876	2015-07-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/182602	2015-06-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/175855	2015-06-15

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/174498	2015-06-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/111582	2015-02-03
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/100025	2015-01-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/090879	2014-12-11

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/945003	Claims benefit of provisional	62/081538	2014-11-18
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/213556	2015-09-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/199607	2015-07-31
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/188876	2015-07-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/182602	2015-06-21

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/175855	2015-06-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/174498	2015-06-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/111582	2015-02-03
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/100025	2015-01-05

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/090879	2014-12-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/943898	Claims benefit of provisional	62/081538	2014-11-18
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/232716	2015-09-25
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/213556	2015-09-02
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/209311	2015-08-24
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/205717	2015-08-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/199607	2015-07-31
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/197120	2015-07-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/188876	2015-07-06

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/182602	2015-06-21
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/175855	2015-06-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/174498	2015-06-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/171915	2015-06-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/157876	2015-05-06
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/154675	2015-04-29
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/153443	2015-04-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/139511	2015-03-27
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/111582	2015-02-03

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/100025	2015-01-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/090879	2014-12-11
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US15/61120	Claims benefit of provisional	62/081538	2014-11-18
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/947718	Continuation of	PCT/US14/39208	2014-05-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/826446	2013-05-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/843021	2013-07-04
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/905109	2013-11-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/834873	2013-06-13
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
14/892821	a 371 of international	PCT/US14/39208	2014-05-22

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/826446	2013-05-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/843021	2013-07-04
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/905109	2013-11-15
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61/834873	2013-06-13

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	W&W Sens Devices, Inc.		
Mailing Address Information For Applicant:			
Address 1	38 Third Street, Suite 307		
Address 2			
City	Los Altos	**State/Province**	CA
Country	US	Postal Code	94022
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (02-18)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Ivan S. Kavrukov/			Date (YYYY-MM-DD)	2024-09-03
First Name	Ivan S.	Last Name	Kavrukov	Registration Number	25,161

Additional Signature may be generated within this form by selecting the Add button.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0015USCIP
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To: IVAN S. KAVRUKOV
COOPER & DUNHAM LLP
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Date of mailing *(day/month/year)*	17 DEC 2020
Applicant's or agent's file reference: 5176/91538-PCT	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No.: PCT/US 20/51733	International filing date *(day/month/year)*: 21 September 2020 (21.09.2020)
Applicant: W&WSENS DEVICES INC.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46).

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   How? Directly to the International Bureau preferably through ePCT, or on paper to:
   The International Bureau of WIPO, 34, chemin des Colombettes, 1211 Geneva 20, Switzerland

   For more detailed instructions, see the *PCT Applicant's Guide*, International Phase, paragraphs 9.004 – 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:
   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.
   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   The applicant *may* **submit comments on an informal basis on the written opinion of the International Searching Authority** to the International Bureau. These comments will be made available to the public after international publication. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established.

   Shortly after the expiration of **18 months from the priority date, the international application will be published** by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for **entry into the national phase** before those designated Offices. In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months. For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

   Within **22 months from the priority date, the applicant may request that a supplementary international search be carried out** by a different International Searching Authority that offers this service (Rule 45*bis*.1). The procedure for requesting supplementary international search is described in the *PCT Applicant's Guide*, International Phase, paragraphs 8.006-8.032.

Name and mailing address of the ISA/US: Mail Stop PCT, Attn: ISA/US, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450	Authorized officer: Lee Young
Facsimile No. 571-273-8300	Telephone No. PCT Helpdesk: 571-272-4300

Form PCT/ISA/220 (revised January 2020)

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PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference		FOR FURTHER ACTION
6176/91538-PCT		see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US 20/51733	21 September 2020 (21.09.2020)	24 September 2019 (24.09.2019)
Applicant		
W&WSENS DEVICES INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language**, the international search was carried out on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

   ☒ the text is approved as submitted by the applicant.

   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

   ☒ the text is approved as submitted by the applicant.

   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

   a. the figure of the drawings to be published with the abstract is Figure No. 59

   ☒ as suggested by the applicant.

   ☐ as selected by this Authority, because the applicant failed to suggest a figure.

   ☐ as selected by this Authority, because this figure better characterizes the invention.

   b. ☐ none of the figures is to be published with the abstract.

Samsung Exhibit 1090, Page 455 of 786
Samsung v. W&Wsens - IPR2025-00993

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 20/51733

A. CLASSIFICATION OF SUBJECT MATTER
IPC - H01L 27/146, 31/101, 31/102 (2020.01)
CPC - H01L 27/14609, 27/14612, 27/14643, 31/101, 31/102

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2018/0102442 A1 (W&WSENS, DEVICES INC) 12 April 2018 (12.04.2018) entire document; especially Fig. 8; Fig. 45; para [0038], para [0203]-[0248], para [0333]-[0336], para [0469]	1, 2, 6-11, 13-16, 20, 22-32, 34, 35, 37, 39-41

A		3-5, 12, 17-19, 21, 33, 36, 38, 42
Y	US 2011/0156195 A1 (TIVARUS et al.) 30 June 2011 (30.06.2011) entire document; especially Fig. 13; para [0001], [0032], [0062]	1, 2, 6-11, 13-16, 20, 22-32, 34, 35, 37, 39-41

A		3-5, 12, 17-19, 21, 33, 36, 38, 42
Y	US 2012/0153127 A1 (HIRIGOYEN et al.) 21 June 2012 (21.06.2012) entire document; especially Fig. 4; para [0052], [0057]	10

A		17
Y	US 2018/0012918 A1 (ARTILUX CORPORATION) 11 January 2018 (11.01.2018) entire document, especially para [0059]	32
A	US 2019/0166317 A1 (BRILLNICS, INC) 30 May 2019 (30.05.2019) entire document; especially para [0010]-[0012]	3-4, 33
A	US 2012/0012741 A1 (VASYLYEV) 19 January 2012 (19.01.2012) entire document; especially Fig. 10-11; para [0084], [0088]	3, 5, 12

☐ Further documents are listed in the continuation of Box C ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 November 2020	17 DEC 2020
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Lee Young Telephone No. PCT Helpdesk: 571-272-4300

Form PCT/ISA/210 (second sheet) (July 2019)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: IVAN S. KAVRUKOV
COOPER & DUNHAM LLP
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	17 DEC 2020
Applicant's or agent's file reference: 5176/91538-PCT	FOR FURTHER ACTION: See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US 20/51733	21 September 2020 (21.09.2020)	24 September 2019 (24.09.2019)

International Patent Classification (IPC) or both national classification and IPC

IPC - H01L 27/146, 31/101, 31/102 (2020.01)

CPC - H01L 27/14609, 27/14612, 27/14643, 31/101, 31/102

Applicant

W&WSENS DEVICES INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	15 November 2020	Lee Young PCT Help Desk Telephone No. 571-272-4300

Form PCT/ISA/237 (cover sheet) (revised January 2019)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/61733

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(b)).

3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:

   a. ☐ forming part of the international application as filed:

      ☐ in the form of an Annex C/ST.25 text file.

      ☐ on paper or in the form of an image file.

   b. ☐ furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.

   c. ☐ furnished subsequent to the international filing date for the purposes of international search only:

      ☐ in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).

      ☐ on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/61733

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-42	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	3-5, 12, 17-19, 21, 33, 36, 38, 42	YES
	Claims	1, 2, 6-11, 13-16, 20, 22-32, 34, 35, 37, 39-41	NO
Industrial applicability (IA)	Claims	1-42	YES
	Claims	NONE	NO

2. Citations and explanations:

Claims 1, 2, 6-9, 11, 13-16, 20, 22-31, 34, 35, 37, and 39-41 lack an inventive step under PCT Article 33(3) as being obvious over US 2018/0102442 A1 to W&Wsens, Devices Inc. (hereinafter "Wsens") in view of US 2011/0156195 A1 to Tivarus et al. (hereinafter "Tivarus").

Regarding claim 1, Wsens discloses a photosensor wafer of crystalline Si and a CMOS Logic Processor (CLP) wafer stacked on each other for electrical interaction and forming a structure (Fig.8; para [0038]- an integrated combination of a microstructure-enhanced photodetector (MSPD) and an active electronic circuit; para [0203]- Silicon chip 800 can any combination of the following devices: MSPDs; MSAPDs; vertical cavity surface emitting lasers (VCSEL) that are either wafer bonded to the chip and/or have a precision cavity for dropping the VCSEL into as in a silicon platform; CMOS/BICMOS ASICs configured for functions such as signal processing, amplifying, transmission, storage, conditioning, analyzing, and/or configured as laser drivers and/or power amplifiers; Fig.45 shows cmos layer and MSPC layer stacked on each other; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration; para [0469]- the microstructure holes can be very complex, as for example in Berenschot et al, Fabrication of 3D fractal structures using nanoscale anisotropic etching of single crystalline silicon) comprising:
an array of laterally spaced pixels formed in said photosensor wafer (Fig. 20 and 21 shows array of laterally spaced pixels (the structures comprises MSPD 1, MSPD2 or MSPD3) in wafer; Fig. 45 shows a single pixel structure with a CMOS layer; para [0248]- FIG. 21 is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics);
wherein said pixels comprise photosensors each including one or more microstructure holes (4412) extending into said photosensor wafer (Fig. 45 shows holes 4412 extending into the said photo wafer (i Si and/or GeSi layer); para [0333]- microstructure holes 4412; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration) and further including plural N-doped and/or P-doped regions (4482, 4484) of the photosensor wafer configured to interact with light photons impinging on said pixels, including on said holes (Fig. 45; para [0330]- Ion implantation to form region 4482 can be implemented from the bottom surface; para [0333]- a depth etch monitor layer 4466 that can be implanted with ions such as Ar, Ne, Xe, O, and/or N...Also shown are upper ion implanted region 4484; para [0349]-Light and/or optical signal can impinge from the surface with the holes and in some cases light/optical signal can impinge from the substrate side through a via. The optical signal is brought to the MSPD/MSAPD via an optical fiber that can have a lens and is focused onto the surface with a certain numerical aperture such that there may be an angular distribution of light rays that are impinging on the surface of the MSPD/MSAPD.);
one or more active CMOS circuits formed in said CLP wafer (Fig.45; para [0038], [0248], [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration...reinforcement of the MSPD/MSAPD structure and CMOS/BiCMOS IC electronics.); and
electrical interconnects between said pixels and said one or more active CMOS circuits, wherein said interconnects are configured to convey electrical signals between said pixels and said one or more active CMOS circuits (Fig. 21; para [0248]- The MSPDs/MSAPDs (MSPD1, MSPD2, MSPD3, MSPD4, etc.) are connected to the CMOS/BiCMOS electronics with a transmission line 2142...The monolithically integrated chip 2100 can be flipped and the electronics can be solder bumped to external circuits such as on a printed circuit board (PCB) (not shown) for electrical signal transmission and electrical power.).
Wsens fails to discloses respective lenses over said pixels; light photons impinging on said pixels through said lenses; wherein said CLP wafer is at a side of said photosensor wafer that is opposite said lenses.
Tivarus, drawn to a stacked CMOS sensor, discloses respective lenses (1304) over pixels (1204, 1206); light photons impinging on said pixels through said lenses; wherein CLP wafer (1306) is at a side of said photosensor wafer (1300) that is opposite said lenses (1304) (Fig. 13 shows the wafer 1306 is at a side of said photosensor wafer 1300 that is opposite the lenses 1304; para [0001]-more particularly to CMOS image sensors having two separate stacked semiconductor wafers with each wafer including a portion of the electrical circuitry; para [0032]- light 302 from a subject scene is input to an imaging stage 304. Imaging stage 304 can include conventional elements such as a lens; para [0062]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1215, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300; para [0063]- Circuit wafer 1306;). It would have been obvious to a person having ordinary skill in the art to combine the lenses and the stacked structure disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0005]-[0006]).

--see supplemental box

Form PCT/ISA/237 (Box No. V) (revised January 2019)

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/61733

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made.

Claims 27 and 35 lack antecedent basis for terms "said lenses". For purposes of this search, claims 27 and 35 are interpreted as depending from claim 26.

Claim 42 depends on claim 3408 which is not exist. For purposes of this search, claim 42 is interpreted as depending on claim 40.

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/51733

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
Box V.2 - Citations and Explanations:

Regarding claim 2, Wsens in view of Tivarus disclose the structure of claim 1. Tivarus further discloses including respective color filters between said lenses and pixels configured to select respective wavelength ranges (Fig. 13 shows color filters 1302 between lenses 1304 and photodetectors 1202, 1204, 1206, 1208; para [0247]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300.).

Regarding claim 6, Wsens in view of Tivarus disclose the structure of claim 1, Wsens further discloses in which said at least some of said holes in the photosensor wafer are generally cylindrical (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 7, Wsens in view of Tivarus disclose the structure of claim 1, Wsens further discloses in which said at least some of said holes in the photosensor wafer are inverted pyramids (Fig. 24; para [0186]- scanning electron micrographs of holes in the shape of inverted pyramids; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.)

Regarding claim 8, Wsens in view of Tivarus disclose the structure of claim 1, Wsens further discloses in which said at least some of said holes in the photosensor wafer are funnel shaped (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 9, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which said hole of each of at least some of said pixels comprises a cluster of nanoholes (9212) into said photosensor wafer (Fig. 92 shows a cluster of nanoholes 9212, para [0560]- The nano/micro structure holes 9212 can have lateral surface dimensions ranging from 30 nm to 5000 nm or more and spacing between the nano micro structure holes can range from 10 nm to 10000 nm or more. The holes can be shaped as a circle, oval, square, polygon, hourglass, fractal, amoeba, star or a combination of shapes).

Regarding claim 11, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses including light reflectors under said pixels (Fig. 9B; para [0208]- a via 930 can be etched to remove most or all of the substrate to the etch stop layer which can in addition be patterned with nano-micro structures 914 and/or can be coated with dielectric distributed Bragg reflectors.).

Regarding claim 13, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which at least some of said holes differ in shape from one another (Fig. 24 shows the different shape of holes; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.)

Regarding claim 14, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which each of said pixels comprises laterally spaced doped regions (4284) (Fig. 41-42; para [0319]- after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants; para [0330]).

Regarding claim 15, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which each of said pixels comprises vertically spaced doped regions (4260) (Fig. 41-42; para [0319]- A N+ connecting well 4260 formed by ion implantation and/or diffusion can connect the cathode on the surface to the N+ layer/region 4282 and in the case of an N substrate the cathode can be on the bottom of the substrate with or without additional connect wells.; para [0330]).

Regarding claim 16, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which said pixels include Ge regions in said photosensor wafer, configured to extend a response of said pixels to light in a 2 micrometers wavelength range (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer; para [0344]- Operating wavelength range for Si I layer can range from 750 nm to 1070 nm and for GeSi can range from 750 nm to 1350 nm and in some cases 900 nm to 1350 nm and in some cases 1100 nm to 1350 nm and in some cases 1250 nm to 1550 nm and in some cases 1250 nm to 1650 nm and in some cases to 2000 nm depending on the Ge fraction in the GeSi alloy.).

Regarding claim 20, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses including doped Si conformally lining at least some of said holes and hyperdoping over said doped Si lining (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants (it is noted P+ or N+ doping is hyperdoping.)).

Regarding claim 22, Wsens in view of Tivarus disclose the structure of claim 1, further including a first layer of electrically insulating material under said pixels (Fig.4E shows BOX layer under the pixel; para [0215]- buried oxide (BOX) layer of 2000 nm on silicon substrate (Therefore the BOX layer is SiO2, which is an insulating material.)) and a second layer of an electrically insulating material over said active CMOS circuits (para [0442]- entire monolithically integrated MSPD/AMSPD with CMOS and/or SiCMOS electronics chip can be entirely and/or partially hermetically sealed with dielectrics such as silicon oxide, silicon nitride, aluminum oxide, aluminum nitride, polymers such as polyimide, and/or spin-on-glass.).

--see next page

Samsung Exhibit 1090, Page 461 of 786
Samsung v. W&Wsens - IPR2025-00993

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/51733

Supplemental Box

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Regarding claim 23, Wsens in view of Tivarus disclose the structure of claim 22. Wsens further discloses wherein the first and second layers of electrically insulating material are selected from a group consisting of Si Oxide and Si Nitride (*para* Fig.46 shows BOX layer under the pixel; *para* [0215]- buried oxide (BOX) layer of 2000 nm on silicon substrate (Therefore the BOX layer is SiO2, which is an insulating material); [0442]- entire monolithically integrated MSPD/AMSPD with CMOS and/or BiCMOS electronics chip can be entirely and/or partially hermetically sealed with dielectrics such as silicon oxide, silicon nitride, aluminum oxide, aluminum nitride, polymers such as polyimide, and/or spin-on-glass.).

Regarding claim 24, Wsens in view of Tivarus disclose The structure of claim 22. Wsens further discloses wherein one or more additional layers of electrically insulating material are formed on said first and/or second layers of electrically insulating material (Fig. 24 shows a Bragg reflector layer on BOX layer; para [0215]- buried oxide (BOX) layer of 2000 nm on silicon substrate (Therefore the BOX layer is SiO2, which is an insulating materia); para [0255]- Starting with a silicon substrate that can have a buried oxide (BOX) layer and/or buried hole layer (SOH silicon on hole), and/or with or without an etch stop layer; para [0256]- in addition a dielectric Bragg reflector; para [0319]).

Regarding claim 25, Wsens discloses a high-speed photodetector array (HSPA) wafer of crystalline Si and a CMOS Logic Processor (CLP) wafer stacked on each other for electrical interaction and forming a structure (Fig.8; para [0186]- FIGS. 1A-1H are top-view scanning electron micrographs of holes in the shape of inverted pyramids used in a microstructure high speed photodiode (MSPD) and/or a high speed microstructure avalanche photodiode (MSAPD); para [0208]- Arrays of MSPD/MSAPD can be monolithically integrated with CMOS/BiCMOS electronics; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration; para [0489]- the microstructure holes can be very complex, as for example in Berenschot et al, Fabrication of 3D fractal structures using nanoscale anisotropic etching of single crystalline silicon) comprising:
an array of laterally spaced photodetectors formed in said HSPA wafer (Fig. 20 and 21 shows array of laterally spaced pixels (the structures comprises MSPD 1, MSPD2 or MSPD3) in wafer; Fig. 45 shows a single pixel structure with a CMOS layer; para [0248]- FIG. 21 is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics);
wherein each of said photodetectors includes at least one microstructure hole (4412) extending into said HSPA wafer (Fig. 45 shows holes 4412 extending into the said photo wafer (I Si and/or GeSi layer); para [0333]- microstructure holes 4412; *para* [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration) and further includes plural N-doped and/or P-doped regions (4482, 4484) of the HSPA wafer configured to interact with light photons impinging on said photodetector from a first side of the HSPA wafer (Fig. 45; para [0330]- Ion implantation to form region 4482 can be implemented from the bottom surface; para [0333]- a depth etch monitor layer 4466 that can be implanted with ions such as Ar, Ne, Xe, O, and/or N...Also shown are upper ion implanted region 4484; para [0349]-Light and/or optical signal can impinge from the surface with the holes and in some cases light/optical signal can impinge from the substrate side through a via. The optical signal is brought to the MSPD/MSAPD via an optical fiber that can have a lens and is focused onto the surface with a certain numerical aperture such that there may be an angular distribution of light rays that are impinging on the surface of the MSPD/MSAPD.);
one or more active CMOS circuits formed in said CLP wafer (Fig.45; para [0038], [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration...reinforcement of the MSPD/MSAPD structure and CMOS/BiCMOS IC electronics); and
electrical interconnects between said high speed photodetector array and said one or more active CMOS circuits, wherein said interconnects are configured to convey electrical signals between said HSPA and said one or more active CMOS circuits (Fig. 21; para [0248]- The MSPDs/MSAPDs (MSPD1, MSPD2, MSPD3, MSPD4, etc.) are connected to the CMOS/BiCMOS electronics with a transmission line 2142...The monolithically integrated chip 2100 can be flipped and the electronics can be solder bumped to external circuits such as on a printed circuit board (PCB) (not shown) for electrical signal transmission and electrical power).
Wsens fails to disclose wherein said CLP wafer is at a side of said HSPA wafer that is opposite said first side.
Tivarus, drawn to a stacked CMOS sensor, discloses CLP wafer (1306) is at a side of a wafer (1300) that is opposite the first side (Fig. 13 shows the wafer 1306 is at a side of the wafer 1300 that is opposite the side with photodetectors; para [0001]-more particularly to CMOS image sensors having two separate stacked semiconductor wafers with each wafer including a portion of the electrical circuitry; para [0062]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300; para [0063]- Circuit wafer 1306;). It would have been obvious to a person having ordinary skill in the art to combine the stacked structure disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0005]-[0006]).

Regarding claim 26, Wsens in view of Tivarus disclose the structure of claim 25 and the HSPA wafer as discussed above. Tivarus further discloses including an array of lenses (1304) formed over the photodetectors (1204, 1206) on said first side of the wafer (1300) (Fig. 13; para [0062]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300). It would have been obvious to a person having ordinary skill in the art to combine the lenses disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0005]-[0006]).

Regarding claim 27. Wsens in view of Tivarus disclose the structure of claim 26. Wsens further discloses plural holes in pixels in said HSPA wafer (Fig. 45 shows plural holes in a single pixel structure; para [0333]- microstructure holes 4412); said photodetectors and said active CMOS circuits are configured to operate at 56 Gb/s or greater data rates that include 112 Gb/s (para [0218]- With thinner I layer, 50 Gb/s, 60 Gb/s, 80 Gb/s, 100 Gb/s can be achieved). Tivarus further discloses in which each of said lenses overlies each pixel (See Tivarus, Fig. 13; para [0062]- A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300). Therefore the lenses disclosed in Tivarus overlies the holes of Wsens since they overly the substrate of Tivarus and the substrate of Wsens has holes.

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Regarding claim 28, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which at least some of said holes in the HSPA wafer are generally cylindrical (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 29, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which at least some of said holes in the HSPA wafer are inverted pyramids (Fig. 24; para [0186]- scanning electron micrographs of holes in the shape of inverted pyramids; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 30, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which at least some of said holes in the HSPA wafer are funnel shaped (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 31, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses including an array of optical filters (2014, 2016, 2018) formed at said first side of the HSPA wafer over said photodetectors (Fig. 20, para [0246]- Bandpass filters can also be fabricated on the top surface where the microstructured holes for absorption enhancement are etched; para [0247]- Note that some or all of the MSPDs can also be MSAPDs. The MSPDs form an array where each MSPD1, MSPD2, MSPD3, . . . MSPDn has a bandpass filter with its own unique bandpass wavelength. Having a different bandpass wavelength for each of the MSPD in the array allows for the selection of specific wavelengths in a CWDM optical signal).

Regarding claim 34, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which said photodetectors include Ge regions in said HSPA wafer, configured to enhance a response of said photodetectors to light in a wavelength range that includes 1350 nm and / or in a wavelength range that includes1550 nm (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer; para [0344]- Operating wavelength range for SI I layer can range from 750 nm to 1070 nm and for GeSI can range from 750 nm to 1350 nm and in some cases 900 nm to 1350 nm and in some cases 1100 nm to 1350 nm and in some cases 1250 nm to 1550 nm and in some cases 1250 nm to 1650 nm and in some cases to 2000 nm depending on the Ge fraction in the GeSi alloy).

Regarding claim 36, Wsens in view of Tivarus disclose the structure of claim 26. Wsens further discloses plurality of holes in pixels (Fig. 45 shows plurality of holes in a single pixel structure; para [0333]- microstructure holes 4412). Tivarus further discloses in which at least some of said lenses overlies each pixel (See Tivarus, Fig. 13; para [0062]- A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300). Therefore the lenses overlies the holes since they overly the substrate and the substrate of Wsens has holes. Wsens further discloses said photodetector array and said CMOS active circuits are configured to operate at data rates of 56 Gb/s or higher (para [0218]- With thinner I layer, 50 Gb/s, 60 Gb/s, 80 Gb/s, 100 Gb/s can be achieved.)

Regarding claim 37, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses including doped Si conformally lining said holes and hyperdoping over said doped Si lining the holes (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSI layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants (It is noted P+ or N+ doping is hyperdoping.)).

Regarding claim 39, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which said CLP wafer includes clock recovery circuits and transimpedance amplifiers (para [0045]- The additional active electronic circuits can comprise one or more transimpedance amplifiers (TIAs); para [0273]- The CMOS/BiCMOS ASICs can include one or more of the following: TIAs; clock data recovery (CDR) circuitry; equalizers; and limiting amplifiers (LA),), and wherein said HSPA and CLP wafers are configured to operate at aggregated data rates of 400-1000 Gb/s or more (para [0268]- increase the aggregated data rates to greater than 40 Gb/s and in some cases greater than 100 Gb/s and in some cases greater than 1 Tb/s.).

Regarding claim 40, Wsens discloses a monolithic wafer of crystalline Si having a first side and a second side (Fig. 39; para [0325]- and/or polycrystalline silicon layers; para [0488]- the microstructure holes can be very complex, as for example in Berenschot et al, Fabrication of 3D fractal structures using nanoscale anisotropic etching of single crystalline silicon), comprising: an array of laterally spaced photosensor or photodetector pixels formed at said first side of the wafer (Fig. 20 and 21 shows array of laterally spaced pixels (the structures comprises MSPD 1, MSPD2 or MSPD3) in wafer; Fig. 45 shows a single pixel structure with a CMOS layer; para [0248]- FIG. 21 is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics);
wherein each of said pixels includes at least one hole (4412) formed into said first side of the wafer (Fig. 45 shows holes 4412 formed into the said photo wafer (I Si and/or GeSI layer); para [0333]- microstructure holes 4412; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration) and further includes plural N-doped and/or P-doped regions (4482, 4484) of the wafer configured to interact with light photons impinging on said pixels, including on said holes (Fig. 45; para [0330]- Ion implantation to form region 4482 can be implemented from the bottom surface; para [0333]- a depth etch monitor layer 4466 that can be implanted with ions such as Ar, Ne, Xe, O, and/or N.. Also shown are upper ion implanted region 4484; para [0349]-Light and/or optical signal can impinge from the surface with the holes and in some cases light/optical signal can impinge from the substrate side through a via. The optical signal is brought to the MSPD/MSAPD via an optical fiber that can have a lens and is focused onto the surface with a certain numerical aperture such that there may be an angular distribution of light rays that are impinging on the surface of the MSPD/MSAPD.);
CMOS logic processors (para [0038], [0246]- FIG. 21 is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics); and (claim 40 continued)

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(claim 40 continued) electrical interconnects in said wafer configured to convey electrical signals between said pixels and said one or more active CMOS circuits (Fig. 21; para [0248]- The MSPDs/MSAPDs (MSPD1, MSPD2, MSPD3, MSPD4, etc.) are connected to the CMOS/BiCMOS electronics with a transmission line 2142...The monolithically integrated chip 2100 can be flipped and the electronics can be solder bumped to external circuits such as on a printed circuit board (PCB) (not shown) for electrical signal transmission and electrical power). Wsens fails to disclose respective optical lenses over said pixels configured to direct to said pixels and said holes light impinging on said first side of the wafer; CMOS logic processors formed at said second side of the wafer.
Tivarus, drawn to a stacked CMOS sensor, discloses respective optical lenses (1304) over the pixels (1302, 1304) configured to direct to said pixels light impinging on the first side of the wafer (upper side); CMOS logic processors (1306) formed at the second side of the wafer (lower side). (Fig. 13; para [0001]-more particularly to CMOS image sensors having two separate stacked semiconductor wafers with each wafer including a portion of the electrical circuitry; para [0032]- light 302 from a subject scene is input to an imaging stage 304. Imaging stage 304 can include conventional elements such as a lens; para [0062]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300; para [0063]- Circuit wafer 1306;). It would have been obvious to a person having ordinary skill in the art to combine the lenses and the stacked structure disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0005]-[0006]).

Regarding claim 41, Wsens in view of Tivarus disclose the monolithic wafer of claim 40. Wsens further discloses plurality of holes in pixels in the wafer (Fig. 45 shows plurality of holes in a single pixel structure; para [0333]- microstructure holes 4412). Tivarus further discloses in which at least some of said lenses overlies each pixel (See Tivarus, Fig. 13; para [0062]- A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300). Therefore the lenses disclosed by Tivarus overlies the holes disclosed in Wsens since they overly the substrate in Tivarus and the substrate of Wsens has holes.

Claim 10 lacks an inventive step under PCT Article 33(3) as being obvious over Wsens in view of Tivarus and further in view of US 2012/0153127 A1 to Hirigoyen et al. (hereinafter "Hirigoyen").

Regarding claim 10, Wsens in view of Tivarus disclose the structure of claim 1, but fails to discloses further including light blockers between adjacent pixels to reduce crosstalk. Hirigoyen, drawn to image sensor, discloses light blocker (40) between adjacent pixels (S1, S2) to reduce crosstalk (Fig. 4; para [0008], [0052]-isolation region 11.. reduces optical crosstalk thanks to an optical waveguide formed by the differences in refractive indices between the substrate 10, the conductive material 30, and the optical isolator 40. para [0057]- Image sensor IS3 differs from image sensor IS2 in that the color filters F1, F2, F3 and the microlenses L1, L2, L3 are arranged on the backside of the substrate 10...the optical isolator 40 extends entirely through the trench 15). It would have been obvious to a person having ordinary skill in the art to combine the light blockers disclosed by Hirigoyen to the structure disclosed by Wsens to enhance the performance by reducing the corsstalk between pixels (See Hirigoyen, para [0052]).

Claim 32 lacks an inventive step under PCT Article 33(3) as being obvious over Wsens in view of Tivarus and further in view of US 2018/0012916 A1 to Artilux Corporation (hereinafter "Artilux").

Regarding claim 32, Wsens in view of Tivarus disclose the structure of claim 31. Wsens further discloses array of optical filters (para [0241]- each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array). Wsens in view of Tivarus fail to disclose said array of optical filters includes Near InfraRed (NIR) filters to select specific NIR wavelength ranges. Artilux, drawn to image sensor array, discloses NIR filter to select specific NIR wavelength ranges (para [0059]- the optical signal 406 may be filtered by a wavelength filter not shown in this figure, such as an NIR filter in the filter layer). It would have been obvious to a person having ordinary skill to include some of the NIR filters disclosed by Artilux to the array of optical filters to increase the performance of the filter by enabling electing specific NIR wavelength ranges (See Artilux, para [0059]).

Claims 3-6, 12, 17-19, 21, 33, 36, 38, and 42 meet the criteria set forth under PCT Article 33(2)-(3) because the prior art does not teach or fairly suggest the subject matter claimed.

The prior art for claim 3 is exemplified by Wsens, Tivarus, US 2019/0166317 A1 to Brillnics, Inc (hereinafter "Brillnics"), and US 2012/0012741 A1 (Vasylyev).

Regarding claim 3,
Wsens in view of Tivarus disclose the structure of claim 2. Wsens further discloses at least one Near InfraRed (NIR) pixel and an NIR optical filter over said NIR pixel to select specific NIR wavelength ranges (para [0192]- The wavelength range, depending on the percentage of Ge in Si, for 0% Ge can range from 840-960 nm, and with 10% Ge or less in GeSi alloy that is either relaxed or not relaxed, the wavelength can range from 840-990 nm for not relaxed GeSi layer and 840-960 nm for relax, for 20% or less Ge, the wavelength can be extended to 1000 nm and in some cases to 1250 nm for not relaxed GeSi layer and for 40% or less Ge, the wavelength can be extended to 1310 nm (it is noted the wavelengtn of 840-1310 nm is in the NIR wavelength range); para [0241]- each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array.) Wsens in view of Tivarus fail to disclose in which said pixels are configured in a Bayer array and each of at least several pixels in the Bayer array encompasses only a single hole in said photosensor wafer.

Brillnics, drawn to a CMOS sensor, discloses pixels are configured in a Bayer array (para [0068]-when the unit pixel groups are arranged in the Bayer array) that includes at least one Near InfraRed (NIR) pixel (para [0096]- The color pixels in the unit RGB pixel group 200 configured as described above not only have an inherent particular responsibility in a visible range (400 nm to 700 nm), but also have a high responsibility in a near-infrared (NIR) region (800 nm to 1,000 nm)). However, Brillnics otherwise fails to remedy the deficiencies of Wsens and Tivarus.

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Vasylyev, drawn to a light detector, discloses one lenses with one hole (Fig. 10-11; para [0089]- FIG. 10 shows a cone-shape cavity forming light input port 14; para [0084]- Light input ports 14 have the same number as the number of lenses 10 in focusing array 6 disposed on top of photovoltaic layer 4. Light input ports 14 are also distributed over surface 32 in accordance with the distribution of lenses 10 in the lens array so that there is a pairwise optical relationship between each lens 10 and the corresponding light input port 14). However, Vasylyev fails to remedy the deficiencies of Wsens , Tivarus and Brillnics.

None of the prior art discloses each of at least several pixels in the Bayer array encompasses only a single hole in said photosensor wafer. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 3, therefore claim 3 meets the criteria set out in PCT Article 33(2)-(3).

The prior art for claim 4 and 33 is exemplified by Wsens, Tivarus and Brillnics.

Regarding claim 4, Wsens in view of Tivarus disclose the structure of claim 2, but fail to disclose in which said pixels include one or more Bayer arrays at least one of which comprises a Near InfraRed (NIR) pixel, and wherein the at least one NIR pixel in at least one of said one or more Bayer arrays is larger than other pixels therein.

Brillnics, drawn to a CMOS sensor, discloses pixels include one or more Bayer arrays at least one of which comprises a Near InfraRed (NIR) pixel (para [0068]-when the unit pixel groups are arranged in the Bayer array; para [0098]- the photodiode PD22 serving as the second green (Gr) photoelectric conversion part also operate as infrared (NIR) photoelectric conversion parts.). However, Brillnics otherwise fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses wherein the at least one NIR pixel in at least one of said one or more Bayer arrays is larger than other pixels therein. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 4, therefore claim 4 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 33, Wsens in view of Tivarus disclose the structure of claim 32, but fail to disclose wherein said array of photodetectors includes some that are larger than others, and said larger photodetectors are under said NIR filters.

Brillnics, drawn to a CMOS sensor, discloses NIR photodetector are larger (para [0012]-Further, there has been known an infrared (IR, NIR) sensor in which the four pixels in a unit pixel group are replaced with one NIR dedicated pixel having a larger pixel size.). However, Brillnics otherwise fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses wherein said array of photodetectors includes some that are larger than others, and said larger photodetectors are under said NIR filters. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 33, therefore claim 33 meets the criteria set out in PCT Article 33(2)-(3).

The prior art for claim 5 and 12 is exemplified by Wsens, Tivarus and Vasylyev

Regarding claim 5, Wsens in view of Tivarus disclose the structure of claim 1, but fail to disclose in which each of said at least some of said pixels has only a single one of said holes.

Vasylyev, drawn to a light detector, discloses one lenses with one hole (Fig. 10-11; para [0084]- Light input ports 14 have the same number as the number of lenses 10 in focusing array 6 disposed on top of photovoltaic layer 4. Light input ports 14 are also distributed over surface 32 in accordance with the distribution of lenses 10 in the lens array so that there is a pairwise optical relationship between each lens 10 and the corresponding light input port 14; para [0089]- FIG. 10 shows a cone-shape cavity forming light input port 14.). However, Vasylyev fails to remedy the deficiencies of Wsens.

None of the prior art discloses in which each of said at least some of said pixels has only a single one of said holes. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 5, therefore claim 5 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 12, Wsens in view of Tivarus disclose the structure of claim 1, but fail to disclose in which at least some of said pixels have only a single hole each and said single hole is an off-center hole.

Vasylyev, drawn to a light detector, discloses photodetector have only a single hole each (Fig. 10-11; para [0089]- FIG. 10 shows a cone-shape cavity forming light input port 14; para [0084]- Light input ports 14 have the same number as the number of lenses 10 in focusing array 6 disposed on top of photovoltaic layer 4. Light input ports 14 are also distributed over surface 32 in accordance with the distribution of lenses 10 in the lens array so that there is a pairwise optical relationship between each lens 10 and the corresponding light input port 14). However, Vasylyev fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses said single hole is an off-center hole. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 12, therefore claim 12 meets the criteria set out in PCT Article 33(2)-(3).

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The prior art for claim 17 is exemplified by Wsens, Tivarus and Hirigoyen.

Regarding claim 17, Wsens in view of Tivarus disclose the structure of claim 1, but fails to discloses in which said pixels have slanted sidewalls configured to reduce crosstalk between adjacent pixels and improve optical confinement.

Hirigoyen, drawn to image sensor, discloses sidewalls (40) configured to reduce crosstalk between adjacent pixels and improve optical confinement (Fig. 4; para [0052]- isolation region 11.. reduces optical crosstalk thanks to an optical waveguide formed by the differences in refractive indices between the substrate 10, the conductive material 30, and the optical isolator 40. para [0057]- Image sensor IS3 differs from image sensor IS2 in that the color filters F1, F2, F3 and the microlenses L1, L2, L3 are arranged on the backside of the substrate 10...the optical isolator 40 extends entirely through the trench 15). However, Hirigoyen otherwise fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses said pixels have slanted sidewalls configured to reduce crosstalk between adjacent pixels and improve optical confinement. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 17, therefore claim 17 meets the criteria set out in PCT Article 33(2)-(3).

The prior art for claims 18-19, 21, 36, 38 and 42 is exemplified by Wsens and Tivarus.

Regarding claim 18, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which said holes are conformally lined with doped Si (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants). Wsens in view of Tivarus fail to disclose at least some adjacent holes are doped to opposite polarities.

None of the prior art discloses at least some adjacent holes are doped to opposite polarities. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 18, therefore claim 18 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 19, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses graphene (para [0195]- the basic steps consist of etching holes in a device wafer that can include epitaxial layers that can include doped P and/or N and/or I layers, SOI, additional dielectric coatings, metallic layers/fillers, graphene). Wsens in view of Tivarus fail to disclose at least some of said holes are conformally lined with graphene.

None of the prior art discloses at least some of said holes are conformally lined with graphene. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 19, therefore claim 19 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 21, Wsens in view of Tivarus disclose the structure of claim 1, but fail to disclose in which said pixels are in an array in which centrally located pixels are smaller in size that other pixels.

None of the prior art discloses said pixels are in an array in which centrally located pixels are smaller in size that other pixels. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 21, therefore claim 21 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 36, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which said holes are conformally lined with doped Si (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants). Wsens in view of Tivarus fail to disclose adjacent holes are doped to opposite polarities.

None of the prior art discloses adjacent holes are doped to opposite polarities. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 36, therefore claim 36 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 38, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses graphene (para [0195]- the basic steps consist of etching holes in a device wafer that can include epitaxial layers that can include doped P and/or N and/or I layers, SOI, additional dielectric coatings, metallic layers/fillers, graphene). Wsens in view of Tivarus fail to disclose said holes are conformally lined with graphene.

None of the prior art discloses said holes are conformally lined with graphene. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 38, therefore claim 38 meets the criteria set out in PCT Article 33(2)-(3).

--see next page

Samsung Exhibit 1090, Page 466 of 786
Samsung v. W&Wsens - IPR2025-00993

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/61733

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
Box V.2 - Citations and Explanations:

Regarding claim 42. Wsens in view of Tivarus disclose the monolithic wafer of claim 40. Wsens further discloses in which said holes are lined with doped regions of said wafer (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-i-N to N-i-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants). Wsens in view of Tivarus fail to disclose adjacent holes are lined with doped regions of opposite polarities.

None of the prior art discloses adjacent holes are lined with doped regions of opposite polarities. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 42, therefore claim 42 meets the criteria set out in PCT Article 33(2)-(3).

Claims 1-42 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.

SEARCH HISTORY

Application Number	PCT/US 20/51733
Search Conducted By	JQ
Search Approved By	ALK

CPC/IPC Classifications Searched	CPC - H01L 27/14609, 27/14612, 27/14643, 31/101, 31/102 IPC (8)- H01L 27/146, 31/101, 31/102 (2020.01)
Date Conducted	09 November 2020 (09.11.2020)

Documentation Searched	CPC - H01L 27/14609, 27/14612, 27/14643, 31/101, 31/102 IPC (8)- H01L 27/146, 31/101, 31/102 (2020.01)
Search Terms Used	Photosensor/photodetect*/photodiode/hspa Wafer/substrate Crystal/crystalline Si/silicon Cmos/clp Stack~/layer~ Pixel Array/grid Lens/lenses/microlenses Hole/opening/aperture Micro/microstructure/um N/P/dope~ Lines/traces/interconnects
Date Conducted	09 November 2020 (09.11.2020)

Electronic Database Searched	PatBase
Files Searched	Full-text: AU BE BR CA CH CN DE DK EP ES FI FR GB IN JP KR SE TH TW US WO Bibliographic: Europe AT BA BE BG CH CS CY CZ DD DK EE ES FI GE GR HR HU IE IS IT LT LU LV MC MD MT NL NO PL PT RO RS SE SI SK SM TR UA YU Asia EA GC HK ID IL IN KZ MN MY PH RU SG SU TH TJ TW UZ VN North America CA CR CU DO GT HN MX NI PA SV TT South America AR BR CL CO EC PE UY Australasia AU NZ Africa AP DZ EG KE MA MW OA ZA ZM ZW
Date Conducted	09 November 2020 (09.11.2020)
Search Logic:	
Classification Search: 1) IC=(H01L27/146 or H01L31/101 or H01L 31/102) (45716)	

2) CPC=(H01L27/14609 or H01L27/14612 or H01L27/14643 or H01L31/101 or H01L31/102) (9304)
3) 1 or 2 (46498)
4) 3 and FT=(Photosensor? or photodetect* or photodiode? or hspa) (13742)
5) 4 and FT=(wafer or substrate) (11476)
6) 5 and FT=((crystal or crystalline) w3 (Si or silicon)) (1286)
7) 6 and FT=(cmos or clp) (747)
8) 7 and FT=(stack~ or layer~) (733)
9) 8 and FT=(pixel?) (561)
10) 9 and FT=(array or grid) (423)
11) 10 and FT=(lens or lenses or microlenses) (281)
12) 11 and FT=(hole? or opening? or aperture?) (181)
13) 12 and FT=(micro or microstructure or um) (146)
14) 13 and FT=(N or P or doped or doping) (144)
15) 14 and FT=(lines or traces or interconnects) (102)
16) 15 and FT=(color w3 filter?) (57)
17) 16 and FT=("Near InfraRed" or NIR) (26)
18) 16 and FT=(cmos w3 circuit?) (19)
19) 18 not 17 (13)
20) 3 and FT=(cmos or clp) (20106)
21) 20 and FT=((Photosensor? or photodetect* or photodiode? or hspa) w3 (wafer or substrate)) (762)
22) 21 and FT=((array or grid) w3 pixel?) (211)
23) 22 and FT=(lens or lenses or microlenses) (158)
24) 23 and FT=(hole? or opening? or aperture?) (101)
25) 24 and FT=(micro or microstructure or um) (79)
26) 25 and FT=(lines or traces or interconnects) (70)
27) 26 and FT=(color w3 filter?) (49)
28) 27 not (17 or 18) (39)
29) 26 and FT=("Near InfraRed" or NIR) (16)
30) 29 not (17 or 18 or 27) (3)

Search limited only by search terms and not by classifications:
31) FT=((Photosensor? or photodetect* or photodiode? or hspa) w3 (wafer or substrate)) (3738)
32) 31 and FT=(cmos or clp) (1143)
33) 32 and FT=((array or grid) w3 pixel?) (272)
34) 33 and FT=(lens or lenses or microlenses) (205)
35) 34 and FT=(hole? or opening? or aperture?) (126)
36) 35 and FT=(micro or microstructure or um) (98)
37) 36 and FT=(lines or traces or interconnects) (83)
38) 37 and FT=(color w3 filter?) (53)
39) 38 not (17 or 18 or 27 or 29) (4)
40) 37 and FT=("Near InfraRed" or NIR) (20)
41) 40 not (17 or 18 or 27 or 29 or 38) (3)
42) FT=(cmos w3 circuit?) (17544)
43) 42 and FT=((Photosensor? or photodetect* or photodiode? or hspa) w3 (wafer or substrate)) (110)
44) 43 and FT=((array or grid) w3 pixel?) (39)
45) 44 not (17 or 18 or 27 or 29 or 38 or 40) (29)
46) 42 and FT=(Photosensor? or photodetect* or photodiode? or hspa) (1555)
47) 46 and FT=((crystal or crystalline) w3 (Si or silicon)) (443)
48) 47 and FT=((array or grid) w3 pixel?) (64)
49) 48 not (17 or 18 or 27 or 29 or 38 or 40 or 44) (42)

F/B search:
50) PN=(us2018102442 or us2017250211) (2)
51) CTB 50 or CTF 50 (269)
52) 51 not (17 or 18 or 27 or 29 or 38 or 40 or 44 or 48) (265)
53) 52 and FT=(cmos w3 circuit?) (13)

Electronic Database Searched	Google
Files Searched	Google Patents
Date Conducted	09 November 2020 (09.11.2020)

Search Logic:

photosensor cmos logic processor
About 12,000 results

photosensor cmos logic processor wafer
About 3,810 results

photosensor cmos logic processor wafer array pixels
About 2,760 results

photosensor cmos logic processor wafer array pixels lenses
About 2,090 results

photosensor cmos logic processor wafer array pixels lenses n-doped
About 802 results

photosensor cmos logic processor wafer array pixels lenses p-doped
About 1,850 results

photosensor cmos circuits wafer array pixels lenses
About 4,400 results

photosensor cmos circuits wafer array pixels lenses NIR
About 1,270 results

Electronic Database Searched	Google
Files Searched	Google Scholar
Date Conducted	09 November 2020 (09.11.2020)

Search Logic:

photosensor cmos logic processor
About 20,000 results

photosensor cmos logic processor wafer
About 5,410 results

photosensor cmos logic processor wafer array pixels
About 3,250 results

photosensor cmos logic processor wafer array pixels lenses
About 1,980 results

photosensor cmos logic processor wafer array pixels lenses n-doped
About 157 results

photosensor cmos logic processor wafer array pixels lenses p-doped
About 145 results

photosensor cmos circuits wafer array pixels lenses
About 6,740 results

photosensor cmos circuits wafer array pixels lenses NIR
About 1,120 results

Supplemental SAO searching:

Electronic Database Searched	PatBase
Files Searched	Full-text: AU BE BR CA CH CN DE DK EP ES FI FR GB IN JP KR SE TH TW US WO Bibliographic: (Europe) AT BA BE BG CH CS CY CZ DD DK EE ES FI GE GR HR HU IE IS IT LT LU LV MC MD MT NL NO PL PT RO RS SE SI SK SM TR UA YU (Asia) EA GC HK ID IL IN KZ MN MY PH RU SG SU TH TJ TW UZ VN (North America) CA CR CU DO GT HN MX NI PA SV TT (South America) AR BR CL CO EC PE UY (Australasia) AU NZ (Africa) AP DZ EG KE MA MW OA ZA ZM ZW
Date Conducted	20 November 2020 (20.11.2020)
Search Logic:	
Search 1:	(photosens* or photodetect*) (Results 567476)
Search 2:	1 and (wafer or substrate or chip) (Results 212373)
Search 3:	2 and (si or silicon) (Results 111160)
Search 4:	3 and (CMOS) (Results 15125)
Search 5:	4 and (pixel%) (Results 9352)
Search 6:	5 and (dope or doped or doping) (Results 4083)
Search 7:	6 and (lens or lenses or microlenses) (Results 2208)
Search 8:	7 and ((connect* or interconnect*) near pixel%) (Results 813)
Search 9:	8 and (holes OR microholes) (Results 481)
Search 10:	8 and (holes OR microholes or nanohole%) (Results 481)
Search 11:	10 and ((holes OR microholes or nanohole%) near (lens or lenses or microlenses)) (Results 3)
Search 12:	10 and ((holes OR microholes or nanohole%) near (pixel%)) (Results 40)
Search 13:	10 and Bayer (Results 103)
Search 14:	13 and (IR or NIR or infrared or (infra%red) or (infra_red)) (Results 86)
Search 15:	10 and (((holes OR microholes or nanohole%) near (pixel%)) near (one or single)) (Results 8)
Search 16:	10 and (((wall% or sidewall%) near pixel%) near (angle~ or slant~)) (Results 2)

Search 17:	10 and ((hole% or microhole%) near dope~) (Results 18)

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To: IVAN S. KAVRUKOV
WISSING MILLER LLP
434 WEST 33RD STREET, 7TH FLOOR
NEW YORK, NY 10001

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Date of mailing *(day/month/year)*	DEC 06 2021
Applicant's or agent's file reference: 309-0013PCT	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No.: PCT/US 21/50717	International filing date *(day/month/year)*: 16 September 2021 (16.09.2021)
Applicant: W&WSENS DEVICES, INC.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   How? Directly to the International Bureau preferably through ePCT, or on paper to:
   The International Bureau of WIPO, 34, chemin des Colombettes, 1211 Geneva 20, Switzerland

   For more detailed instructions, see the *PCT Applicant's Guide*, International Phase, paragraphs 9.004 – 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:
   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.
   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   The applicant may **submit comments on an informal basis on the written opinion of the International Searching Authority** to the International Bureau. These comments will be made available to the public after international publication. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established.

   Shortly after the expiration of **18 months from the priority date, the international application will be published** by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for **entry into the national phase** before those designated Offices. In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months. For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

   Within **22 months from the priority date, the applicant may request that a supplementary international search be carried out** by a different International Searching Authority that offers this service (Rule 45*bis*.1). The procedure for requesting supplementary international search is described in the *PCT Applicant's Guide*, International Phase, paragraphs 8.006-8.032.

Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Kari Rodriquez Telephone No. PCT Helpdesk: 571-272-4300

Form PCT/ISA/220 (revised January 2020)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference		FOR FURTHER ACTION
309-0013PCT		see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US 21/50717	16 September 2021 (16.09.2021)	21 September 2020 (21.09.2020)
Applicant W&WSENS DEVICES, INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the title,

☒ the text is approved as submitted by the applicant.

☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

☒ the text is approved as submitted by the applicant.

☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

a. the figure of the **drawings** to be published with the abstract is Figure No. 25

☒ as suggested by the applicant.

☐ as selected by this Authority, because the applicant failed to suggest a figure.

☐ as selected by this Authority, because this figure better characterizes the invention.

b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 21/50717

A. CLASSIFICATION OF SUBJECT MATTER

IPC - G01S 7/4865; G01S 17/894; G01S 13/08; G01J 1/42; G02B 6/42; G02F 1/16762 (2021.01)

CPC - G01S 7/4865; G01S 17/894; G01S 13/08; G01J 1/42; G02B 6/42; G02F 1/16762; H04N 5/36965; H01G 9/2045

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2018/0102442 A1 (W&WSENS, DEVICES INC.) 12 April 2018 (12.04.2018) entire document, especially: para [0031], [0223], [0241], [0263], [0456], [0549]	1-22
A	US 2016/0240579 A1 (OMNIVISION TECHNOLOGIES INC.) 18 August 2016 (18.08.2016) entire document, especially: para [0002], [0020], [0023], [0024], [0034], [0038]	1-22
A	US 2017/0141153 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING CO., LTD.) 18 May 2017 (18.05.2017) entire document, especially: [0015]-[0019], [0023], [0024], [0055]	1-22

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
08 November 2021	DEC 06 2021
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Kari Rodriquez Telephone No. PCT Helpdesk: 571-272-4300

Form PCT/ISA/210 (second sheet) (July 2019)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: IVAN S. KAVRUKOV
WISSING MILLER LLP
434 WEST 33RD STREET, 7TH FLOOR
NEW YORK, NY 10001

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	DEC 06 2021
Applicant's or agent's file reference 309-0013PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US 21/50717	16 September 2021 (16.09.2021)	21 September 2020 (21.09.2020)

International Patent Classification (IPC) or both national classification and IPC

IPC - G01S 7/4865; G01S 17/894; G01S 13/08; G01J 1/42; G02B 6/42; G02F 1/16762 (2021.01)

CPC - G01S 7/4865; G01S 17/894; G01S 13/08; G01J 1/42; G02B 6/42; G02F 1/16762; H04N 5/36965; H01G 9/2045

Applicant W&WSENS DEVICES, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	08 November 2021	Kari Rodriquez PCT Help Desk Telephone No. 571-272-4300

Form PCT/ISA/237 (cover sheet) (revised January 2019)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 21/50717

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(b)).

3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:

a. ☐ forming part of the international application as filed:

☐ in the form of an Annex C/ST.25 text file.

☐ on paper or in the form of an image file.

b. ☐ furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.

c. ☐ furnished subsequent to the international filing date for the purposes of international search only:

☐ in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).

☐ on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 21/50717

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-22	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	1-22	YES
	Claims	NONE	NO
Industrial applicability (IA)	Claims	1-22	YES
	Claims	NONE	NO

2. Citations and explanations:
Claims 1-22 meet the criteria set out in PCT Article 33(2)-(3) because the prior art does not teach or fairly suggest the subject matter claimed.

The prior art for claim 1-22 is exemplified by US 2018/0102442 A1 to W&WSens, Devices Inc. (hereinafer 'W&WSens'), US 2016/0240579 A1 to Omnivision Technologies Inc. (hereinafter 'Omnivision'), and US 2017/0141153 A1 to Taiwan Semiconductor Manufacturing Co. Ltd. (hereinafter 'Taiwan').

Regarding Claim 1,
W&WSens discloses a microstructure enhanced absorption photosensitive device (para [0031]- This patent specification relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics.) comprising: a CMOS ASIC wafer (120) (para [0223]- FIG. 14 is a cross section schematic of a MSPD monolithically integrated with CMOS/BiCMOS electronics in a single chip, according to some embodiments. The chip can include multiple MSPD (and/or MSAPD) with single and/or multiple CMOS/BiCMOS electronic application specific integrated circuits.) the CMOS ASIC wafer is configured to process signals (para [0203]- CMOS/BiCMOS ASICs configured for functions such as signal processing, amplifying, transmission, storage, conditioning, analyzing, and/or configured as laser drivers and/or power amplifiers);
a semiconductor material (102) in which an array is formed (para [0241]- MSPD/MSAPD arrays can be fabricated over the holes either in the oxide and/or in the silicon such that each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array.);
wherein a region of undoped or low-doped Si (FIG. 24; element "I Si"; para [0263]- In the case of integration with CMOS/BiCMOS electronics, the I layer can be low doped and/or undoped) between said doped Si regions (see arrangement of elements of "P Si and/or GeSi and /or Ge", "I Si" and "N Si and/or Bragg reflecctor layers of Si/GeSi"), and a single microhole (2540) (FIG. 24, 2412; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.);
wherein a region of undoped or low-doped Ge or an alloy (FIG. 24; element "I Si and/or GeSi and /or Ge"; para [0263]- In the case of integration with CMOS/BiCMOS electronics, the I layer can be low doped and/or undoped) thereof between said doped regions of Ge or an alloy thereof (see arrangement of elements of "P Si and/or GeSi and /or Ge", "I Si and/or GeSi and /or Ge" and "N Si and/or GeSi and /or Ge");
deep trench (FIG. 89, element 8970; para [0549]- In some cases, instead of a highly doped connecting well, a deep trench with oxide 8970 on its sidewalls and the center can have conducting silicide 8972 and/or metal as shown in FIG. 89);
and connecting electrodes (para [0456]- In some cases a metal connecting electrode can be formed from the surface to the P+ substrate via a trench (not shown) and in some cases a TSV (not shown) can be formed to the bottom anode metal).
W&WSens fails to disclose a CMOS image sensor wafer (CIS) stacked to each other, the CMOS ASIC wafer is configured to receive the signals that the CIS wafer produces, wherein the CIS wafer comprises: an array of both Si pixels and Ge pixels; each Si pixel comprises an upper and a lower region of Si doped to opposite polarities and the microhole extending into the Si pixel; each Ge pixel comprises an upper and a lower region of Ge or an alloy thereof doped to opposite polarities and and a single microhole extending into the Ge pixel; wherein the deep trench is a trench isolation between adjacent Si pixels and Ge pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes in the Si and Ge pixels; and pixel electrodes coupled to said Si and Ge pixels, wherein connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Omnivision discloses a microstructure enhanced absorption photosensitive device (para [0002]-This invention is related to image sensors; para [0020]- each of the plurality of visible light pixels includes a photosensitive element, such as for example a photodiode, to receive a portion of light, and pixel support circuitry to generate a signal representative of an intensity of the received portion of light.) comprising:
a CMOS ASIC wafer (para [0034]- Digital counter 480 may be implemented using CMOS circuitry disposed on the ASIC die fabricated using a standard CMOS process of the stacked die system) and a CMOS image sensor wafer (CIS) (FIG. 2, image sensor 200) stacked to each other (para [0024]- Since stacked 3D color image sensor 200 includes a sensor die stacked with an ASIC die in a stacked chip scheme) such that signals that the CIS wafer produces (para [0023]- In one example, each of the plurality of visible light pixels 211 includes a photosensitive element such as a photodiode to receive a portion of light, as well as pixel support circuitry to generate a signal representative of an intensity of the received portion of light.), wherein the CIS wafer comprises:
a semiconductor material (FIG. 5, semiconductor layer 510) in which an array is formed of Si pixels (para [0020]- For instance, in one example, an imaging system includes an image pixel array having a plurality of visible light pixels, and a plurality of silicon photon avalanche diode (SPAD) pixels). (claim 1 continued)
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Supplemental Box

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(claim 1 continued)
Omnivision fails to disclose the CMOS ASIC wafer is configured to receive and process signals, and wherein an array is formed of both Si pixels and Ge pixels; wherein each Si pixel comprises an upper and a lower region of Si doped to opposite polarities and a region of undoped or low-doped Si between said doped Si regions, and a single microhole extending into the Si pixel; wherein each Ge pixel comprises an upper and a lower region of Ge or an alloy thereof doped to opposite polarities and a region of undoped or low-doped Ge or an alloy thereof between said doped regions of Ge or an alloy thereof, and a single microhole extending into the Ge pixel; deep trench insulation between adjacent Si pixels and Ge pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes in the Si and Ge pixels; and pixel electrodes coupled to said Si and Ge pixels, connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Taiwan discloses a microstructure enhanced absorption photosensitive device (para [0017]- The present application is directed to a CMOS image sensor with elemental silicon and silicon germanium for long-wavelength pixel sensors; By arranging the photodetector in the silicon germanium layer, the photodetector advantageously has good sensitivity to and absorption of long-wavelength radiation, such as, for example, infrared radiation) comprising: a CMOS image sensor wafer (CIS) (FIG.1, 100; para [0018]- With reference to FIG. 1, a cross-sectional view 100 of some embodiments of a CMOS image sensor with a semiconductor stack 102 of silicon and silicon germanium is provided.), wherein the CIS wafer comprises:
a semiconductor material in which an array is formed of both Si pixels and Ge pixels (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer; para [0016]- Another solution is to use silicon germanium in place of elemental silicon for the semiconductor layer);
wherein each Si pixel comprises an upper (FIG.2A, upper silicon layer 104; para [0023]- an upper silicon layer 104 a of the pair is arranged over and directly abuts the silicon germanium layer 106 a.) and a lower region of Si (FIG.2A, lower silicon layer 204; para [0023]- Further, in some embodiments, a lower silicon layer 204 of the pair is arranged over and directly abuts the semiconductor substrate 202) doped (para [0023]- The semiconductor stack 102 a is doped with p- or n-type dopants, and comprises a pair of silicon layers 104 a, 204);
wherein each Ge pixel comprises a region of Ge or an alloy thereof doped (para [0023]- The semiconductor stack 102 a is doped with p- or n-type dopants, and comprises a pair of silicon layers 104 a, 204 and a silicon germanium layer 106 a arranged between the silicon layers 104 a, 204);
deep trench insulation (FIG. 1, deep trench isolation 112; para [0024]- The isolation region 112 is, for example, a shallow trench isolation (STI) region, a deep trench isolation (DTI) region, or an implant isolation region.) between adjacent Si pixels and Ge pixels (para [0055]- The isolation region 112 is configured to isolate the pixel sensors 110, 502, 504 and is, for example, a STI or DTI region; para [0016]- Another solution is to use silicon germanium in place of elemental silicon for the semiconductor layer.) in said array (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer) and an electrically and optically isolating material in said deep trench insulation (para [0061]- In some embodiments, the process for forming the isolation region 112 comprises filling the trench with a dielectric material, such as silicon dioxide.) in the Si and Ge pixels (para [0055]- The isolation region 112 is configured to isolate the pixel sensors 110, 502, 504 and is, for example, a STI or DTI region; para [0019]- The pixel sensor 110 comprises a photodetector 114 at least partially buried in the silicon germanium layer 106, and one or more pixel transistors arranged on the upper surface 108 of the silicon layer 104.);
and pixel electrodes coupled to said Si and Ge pixels (Claim 21- wherein the transistor further comprises a gate electrode, a gate dielectric layer, and an additional source/drain region, wherein the gate dielectric layer spaces the gate electrode over the surface of the silicon layer; para [0017]- A photodetector is at least partially buried in the silicon germanium layer and a transistor is arranged on a surface of the elemental silicon layer with a source/drain region electrically coupled to the photodetector);

Taiwan fails to discloses a CMOS ASIC wafer and a CMOS image sensor wafer (CIS) stacked to each other such that the CMOS ASIC wafer is configured to receive and process signals that the CIS wafer produces, wherein a region of Si to opposite polarities and a region of undoped or low-doped Si between said doped Si regions, and a single microhole extending into the Si pixel, wherein an upper and lower region of Ge or an alloy thereof to opposite polarities and a region of undoped or low-doped Ge or an alloy thereof between said doped regions of Ge or an alloy thereof, and a single microhole extending into the Ge pixel; an electrically and optically isolating material in said microholes; connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

None of the prior art discloses, the CMOS ASIC wafer is configured to receive signals; a region of Si to opposite polarities and the microhole extending into the Si pixel; an upper and a lower region of Ge or an alloy thereof to opposite polarities and a single microhole extending into the Ge pixel; an electrically and optically isolating material in said microholes; wherein connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular elements as required by claim 1, therefore claim 1 meets the criteria set out in PCT Article 33(2)-(3).

Claims 2-13 depend from claim 1, and therefore, meet the criteria set out in PCT Article 33(2)-(3) as well.

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In case the space in any of the preceding boxes is not sufficient.
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Regarding Claim 14,
W&WSens discloses a method (para [0031]- This patent specification relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics; para [0061]- According to some embodiments, a method of making a microstructure-enhanced photodetector (MSPD) configured to convert an optical input that at least some of the time has a cross-section that is essentially continuous spatially to an electrical output) comprising:
a CMOS ASIC wafer (120) (para [0223]- FIG. 14 is a cross section schematic of a MSPD monolithically integrated with CMOS/BiCMOS electronics in a single chip, according to some embodiments. The chip can include multiple MSPD (and/or MSAPD) with single and/or multiple CMOS/BiCMOS electronic application specific integrated circuits.) such that the CMOS ASIC wafer is configured to process signals (para [0203]- CMOS/BiCMOS ASICs configured for functions such as signal processing, amplifying, transmission, storage, conditioning, analyzing, and/or configured as laser drivers and/or power amplifiers);
forming a semiconductor material (102) by fabricating an array of pixels (2530 and/or 2532) therein (para [0241]- MSPD/MSAPD arrays can be fabricated over the holes either in the oxide and/or in the silicon such that each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array.)
forming a region of undoped or low-doped semiconductor material (FIG. 24; element "I Si and/or GeSi and /or Ge"; para [0263]- In the case of integration with CMOS/BiCMOS electronics, the I layer can be low doped and/or undoped) between said doped regions (see arrangement of elements of "P Si and/or GeSi and/or Ge", "I Si and/or GeSi and/or Ge" and "N Si and/or GeSi and/or Ge"), and a single microhole (2540) (FIG. 24, 2412; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.);
forming deep trench (FIG. 89, element 8970; para [0549]- In some cases, instead of a highly doped connecting well, a deep trench with oxide 8970 on its sidewalls and the center can have conducting silicide 8972 and/or metal as shown in FIG. 89);
and forming connecting electrodes (para [0456]- In some cases a metal connecting electrode can be formed from the surface to the P+ substrate via a trench (not shown) and in some cases a TSV (not shown) can be formed to the bottom anode metal).
W&WSens fails to disclose stacking and bonding to each other a CMOS image sensor wafer (CIS) (110), and the CMOS ASIC wafer is configured to receive the signals that the CIS wafer produces; forming at each pixel an upper and a lower region of semiconductor material doped to opposite polarities (2534, 2536), wherein the microhole (2540) extending into the pixel; wherein the deep trench is a trench isolation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes in the pixels; and forming pixel electrodes (154) coupled to said pixels, wherein connecting electrodes (152) coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Omnivision discloses a method (para [0002]-This invention is related to image sensors; para [0027]- In the example, the sensor die and ASIC die are stacked and coupled together during fabrication in a stacked chip scheme) comprising:
stacking and bonding (para [0024]- Since stacked 3D color image sensor 200 includes a sensor die stacked with an ASIC die in a stacked chip scheme; para [0038]- FIG. 5 includes a first device die 506, a second device die 508 and a bonding interface 507 at which first device die 506 is bonded to second device die 508.) to each other a CMOS ASIC wafer (para [0034]- Digital counter 480 may be implemented using CMOS circuitry disposed on the ASIC die fabricated using a standard CMOS process of the stacked die system) and a CMOS image sensor wafer (CIS) (FIG. 2, image sensor 200; para [0024]- Since stacked 3D color image sensor 200 includes a sensor die stacked with an ASIC die in a stacked chip scheme) such signals that the CIS wafer produces (para [0023]- In one example, each of the plurality of visible light pixels 211 includes a photosensitive element such as a photodiode to receive a portion of light, as well as pixel support circuitry to generate a signal representative of an intensity of the received portion of light.);
forming the CIS wafer in a semiconductor material (FIG. 5, semiconductor layer 510) by fabricating an array of pixels therein (para [0020]- For instance, in one example, an imaging system includes an image pixel array having a plurality of visible light pixels, and a plurality of silicon photon avalanche diode (SPAD) pixels; para [0038]- The illustrated example shows a plurality of visible light pixels, 502A, 502B, 502C and 502D, as well as a plurality of SPAD pixels 503A and 503B).
Omnivision fails to disclose the CMOS ASIC wafer is configured to receive and process signals; forming at each pixel an upper and a lower region of semiconductor material doped to opposite polarities and a region of undoped or low-doped semiconductor material between said doped regions, and a single microhole extending into the pixel; wherein the deep trench insulation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes in the pixels; forming deep trench insulation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes in the pixels; and forming pixel electrodes coupled to said pixels, connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Taiwan discloses a method (para [0056]- With reference to FIGS. 6-12, a series of cross-sectional views of some embodiments of a method for manufacturing a CMOS image sensor with silicon and silicon germanium is provided.) comprising:
a CMOS image sensor wafer (CIS) (FIG.1, 100; para [0018]- With reference to FIG. 1, a cross-sectional view 100 of some embodiments of a CMOS image sensor with a semiconductor stack 102 of silicon and silicon germanium is provided.);
forming the CIS wafer in a semiconductor material by fabricating an array of pixels therein (para [0015]- Some complementary metal-oxide -semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer);
forming at each pixel an upper (FIG.2A, upper silicon layer 104; para [0023]- an upper silicon layer 104 a of the pair is arranged over and directly abuts the silicon germanium layer 106 a.) and a lower region of semiconductor material (FIG.2A, lower silicon layer 204; para [0023]- Further, in some embodiments, a lower silicon layer 204 of the pair is arranged over and directly abuts the semiconductor substrate 202) doped (para [0023]- The semiconductor stack 102 a is doped with p- or n-type dopants, and comprises a pair of silicon layers 104 a, 204) to opposite polarities and a region of undoped or low-doped semiconductor material between said doped regions, and a single microhole extending into the pixel; (claim 14 continued)

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(claim 14 continued) forming deep trench insulation (FIG. 1, deep trench isolation 112; para [0024]- The isolation region 112 is, for example, a shallow trench isolation (STI) region, a deep trench isolation (DTI) region, or an implant isolation region.) between adjacent pixels (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer) in said array (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer) and an electrically and optically isolating material in said deep trench insulation in the pixels (para [0061]- In some embodiments, the process for forming the isolation region 112 comprises filling the trench with a dielectric material, such as silicon dioxide.;para [0055]- The isolation region 112 is configured to isolate the pixel sensors 110, 502, 504 and is, for example, a STI or DTI region); and forming pixel electrodes coupled to said pixels (Claim 21- wherein the transistor further comprises a gate electrode, a gate dielectric layer, and an additional source/drain region, wherein the gate dielectric layer spaces the gate electrode over the surface of the silicon layer).
Taiwan fails to disclose stacking and bonding to each other a CMOS ASIC wafer and a CMOS image sensor wafer (CIS) such that the CMOS ASIC wafer is configured to receive and process signals that the CIS wafer produces; forming a region to opposite polarities and a region of undoped or low-doped semiconductor material between said doped region; optically isolating material in said microholes; connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

None of the prior art discloses, the CMOS ASIC wafer is configured to receive signals; a region to opposite polarities and the microhole extending into the pixel; optically isolating material in said microholes in the pixels; connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular steps as required by claim 14, therefore claim 14 meets the criteria set out in PCT Article 33(2)-(3).

Claim 15 depends from claim 14, and therefore, meet the criteria set out in PCT Article 33(2)-(3) as well.

Regarding Claim 16,
W&WSens discloses a microstructure enhanced absorption photosensitive device (para [0031]- This patent specification relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics.) comprising: a CMOS ASIC wafer (para [0223]- FIG. 14 is a cross section schematic of a MSPD monolithically integrated with CMOS/BiCMOS electronics in a single chip, according to some embodiments. The chip can include multiple MSPD (and/or MSAPD) with single and/or multiple CMOS/BiCMOS electronic application specific integrated circuits.) the CMOS ASIC wafer is configured to process signals (para [0203]- CMOS/BiCMOS ASICs configured for functions such as signal processing, amplifying, transmission, storage, conditioning, analyzing, and/or configured as laser drivers and/or power amplifiers);
a layer in which an array of pixels is formed (para [0241]- MSPD/MSAPD arrays can be fabricated over the holes either in the oxide and/or in the silicon such that each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array);
wherein a region of undoped or low-doped semiconductor material (FIG. 24; element "I Si and/or GeSi and /or Ge"; para [0263]- In the case of integration with CMOS/BiCMOS electronics, the I layer can be low doped and/or undoped) between said doped regions (see arrangement of elements of "P Si and/or GeSi and /or Ge", "I Si and/or GeSi and /or Ge" and "N Si and/or GeSi and /or Ge"), and a single microhole (2540) (FIG. 24, 2412; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.);
deep trench (FIG. 89, element 8970; para [0549]- In some cases, instead of a highly doped connecting well, a deep trench with oxide 8970 on its sidewalls and the center can have conducting silicide 8972 and/or metal as shown in FIG. 89);
and connecting electrodes (para [0456]- In some cases a metal connecting electrode can be formed from the surface to the P+ substrate via a trench (not shown) and in some cases a TSV (not shown) can be formed to the bottom anode metal).
W&WSens fails to disclose a CMOS image sensor wafer (CIS) (110) stacked to each other, the CMOS ASIC wafer is configured to receive the signals that the CIS wafer produces, wherein each pixel comprises an upper and a lower region of semiconductor material doped to opposite polarities (2534, 2536), and the microhole extending into the pixel; wherein the deep trench is a trench isolation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes; and pixel electrodes (154) coupled to said pixels, wherein connecting electrodes (152) coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Omnivision discloses a microstructure enhanced absorption photosensitive device (para [0002]-This invention is related to image sensors; para [0020]- each of the plurality of visible light pixels includes a photosensitive element, such as for example a photodiode, to receive a portion of light, and pixel support circuitry to generate a signal representative of an intensity of the received portion of light.) comprising:
a CMOS ASIC wafer (para [0034]- Digital counter 480 may be implemented using CMOS circuitry disposed on the ASIC die fabricated using a standard CMOS process of the stacked die system) and a CMOS image sensor wafer (CIS) (FIG. 2, image sensor 200) stacked to each other (para [0024]- Since stacked 3D color image sensor 200 includes a sensor die stacked with an ASIC die in a stacked chip scheme) such that signals that the CIS wafer produces (para [0023]- In one example, each of the plurality of visible light pixels 211 includes a photosensitive element such as a photodiode to receive a portion of light, as well as pixel support circuitry to generate a signal representative of an intensity of the received portion of light.), wherein the CIS wafer comprises:
a layer (FIG. 5, semiconductor layer 510) in which an array of pixels is formed (para [0020]- For instance, in one example, an imaging system includes an image pixel array having a plurality of visible light pixels, and a plurality of silicon photon avalanche diode (SPAD) pixels; para [0038]- The illustrated example shows a plurality of visible light pixels, 502A, 502B, 502C and 502D, as well as a plurality of SPAD pixels 503A and 503B); (claim 16 continued)

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(claim 16 continued) Omnivision fails to disclose the CMOS ASIC wafer is configured to receive and process signals; wherein each pixel comprises an upper and a lower region of semiconductor material doped to opposite polarities, a region of undoped or low-doped semiconductor material between said doped regions, and a single microhole extending into the pixel; wherein the deep trench insulation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes; deep trench insulation between adjacent pixels in said array and an electrically and optically isolating material in said deep trench insulation and in said microholes; and pixel electrodes coupled to said pixels, connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

Taiwan discloses a microstructure enhanced absorption photosensitive device (para [0017]- The present application is directed to a CMOS image sensor with elemental silicon and silicon germanium for long-wavelength pixel sensors; By arranging the photodetector in the silicon germanium layer, the photodetector advantageously has good sensitivity to and absorption of long-wavelength radiation, such as, for example, infrared radiation) comprising: a CMOS image sensor wafer (CIS) (FIG.1, 100; para [0018]- With reference to FIG. 1, a cross-sectional view 100 of some embodiments of a CMOS image sensor with a semiconductor stack 102 of silicon and silicon germanium is provided.), wherein the CIS wafer comprises:
a layer in which an array of pixels is formed (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer);
wherein each pixel comprises an upper (FIG.2A, upper silicon layer 104; para [0023]- an upper silicon layer 104 a of the pair is arranged over and directly abuts the silicon germanium layer 106 a.) and a lower region of semiconductor material (FIG.2A, lower silicon layer 204; para [0023]- Further, in some embodiments, a lower silicon layer 204 of the pair is arranged over and directly abuts the semiconductor substrate 202) doped (para [0023]- The semiconductor stack 102 a is doped with p- or n-type dopants, and comprises a pair of silicon layers 104 a, 204);
deep trench insulation (FIG. 1, deep trench isolation 112; para [0024]- The isolation region 112 is, for example, a shallow trench isolation (STI) region, a deep trench isolation (DTI) region, or an implant isolation region.) between adjacent pixels (para [0055]- The isolation region 112 is configured to isolate the pixel sensors 110, 502, 504 and is, for example, a STI or DTI region) in said array (para [0015]- Some complementary metal-oxide-semiconductor (CMOS) image sensors comprise a semiconductor layer of elemental silicon and an array of pixel sensors arranged in the semiconductor layer) and an electrically and optically isolating material in said deep trench insulation (para [0061]- In some embodiments, the process for forming the isolation region 112 comprises filling the trench with a dielectric material, such as silicon dioxide);
and pixel electrodes coupled to said pixels (Claim 21- wherein the transistor further comprises a gate electrode, a gate dielectric layer, and an additional source/drain region, wherein the gate dielectric layer spaces the gate electrode over the surface of the silicon layer);
Taiwan fails to disclose a CMOS ASIC wafer and a CMOS image sensor wafer (CIS) stacked to each other such that the CMOS ASIC wafer is configured to receive and process signals that the CIS wafer produces, wherein a region of semiconductor material to opposite polarities and a region of undoped or low-doped semiconductor material between said doped regions, and a single microhole extending into the pixel; an electrically and optically isolating material in said microholes; connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer.

None of the prior art discloses, the CMOS ASIC wafer is configured to receive signals; a region of semiconductor material to opposite polarities and the microhole extending into the pixel; an electrically and optically isolating material in said microholes; wherein connecting electrodes coupled to at least some of the pixel electrodes, and bonding electrodes coupled to at least some of the connected electrodes, configured to convey electrical signals between said pixels and said CMOS ASIC wafer. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular elements as required by claim 16, therefore claim 16 meets the criteria set out in PCT Article 33(2)-(3).

Claims 17-22 depend from claim 16, and therefore, meet the criteria set out in PCT Article 33(2)-(3) as well.

Claims 1-22 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used by industry.

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PATENT AND TRADEMARK OFFICE

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
18/822,880	**09/03/2024 02:21:44 PM Z ET**	**309-0015USCIPDIV**

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	67016011	AUTHORIZED BY	Ivan Kavrukov
CUSTOMER #	139982	FILING DATE	-
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	SHIH-PING Wang

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 2892	**E202493E23339898**	**Mary Ellen Finnegan**

PRE-AUTHORIZED ACCOUNT	PRE-AUTHORIZED CATEGORY
600125	**37 CFR 1.21 (Miscellaneous fees and charges)**

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
2111	UTILITY PATENT APPL. SEARCH FEE	280.00	1	280.00
4011	BASIC FILING FEE- UTILITY	64.00	1	64.00
2311	EXAMINATION OF ORIGINAL PATENT APPLICATION	320.00	1	320.00
			TOTAL AMOUNT:	**$664.00**

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	
	Filing Date	
	First Named Inventor	Shih-Yuan WANG
	Art Unit	
	Examiner Name	
	Attorney Docket Number	309-0015USCIPDIV

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	3	10411053		2019-09-10	Yokogawa	
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	Application Number	
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	First Named Inventor	Shih-Yuan WANG
	Art Unit	
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	Attorney Docket Number	309-0015USCIPDIV

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	1	20100320444		2010-12-23	Dutta	
	2	20110309331		2011-12-22	Yu et al.	
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	1	20080101301	KR		2008-11-21	Dongbu Hitek Co. Ltd.		☐
	2	2002314116	JP		2002-10-25	Seiko Epson Corp.		☐
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Name/Print	Ivan S. Kavrukov	Registration Number	25,161

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Application Number	TBD
Filing Date	TBD
First Named Inventor	Shih-Yuan WANG
Title	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
Art Unit	N/A
Examiner Name	N/A
Attorney Docket Number	309-0015USCIPDIV

SIGNATURE of Applicant or Patent Practitioner

Signature	/Ivan S. Kavrukov/	Date (Optional)	
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Name	SHIHPING WANG		
Title	PRESIDENT CEO		

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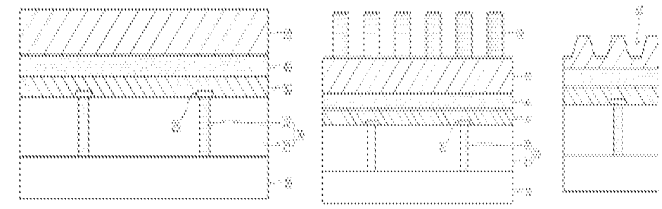
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Image sensor and method for manufacturing thereof

Abstract

An image sensor and a manufacturing method thereof are provided to improve condensing rate and simplify its process while adopting a vertical photodiode of which resolution and sensitivity are improved. A CMOS(Complementary Metal Oxide Silicon) circuit is formed at a semiconductor circuit, and a metallic wiring layer which includes a metal wire and an inter insulation film is formed at a semiconductor substrate. A first conductivity type conductive layer is formed at the metallic wiring layer, and an intrinsic layer is formed at the first conductivity type conductive layer. A second conductivity type conductive layer(51) is formed at the intrinsic layer is formed at the intrinsic layer. At one or more than one layer of those three layers, the first conductivity conductive layer, the intrinsic layer and the second conductivity conductive layer, a concavo-convex part is formed.

Images (14)



KR20080101301A

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Worldwide applications

2007 KR

Application KR1020070047886A events

2007-05-17 Application filed by 주식회사 동부하이텍

2007-05-17 Priority to KR1020070047886A

2008-11-21 Publication of KR20080101301A

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Classifications

H01L27/14607 Geometry of the photosensitive area

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Claims (10)

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translated from Korean

A semiconductor substrate on which a CMOS circuit is formed; A metal wiring layer including a metal wiring and an interlayer insulating film formed on the semiconductor substrate; A first conductivity type conductive layer formed on the metal wiring layer; An intrinsic layer formed on the first conductivity type conductive layer; And A second conductivity type conductive layer formed on the intrinsic layer, At least one of the first conductive type conductive layer, the intrinsic layer and the second conductive type conductive layer is an image sensor, characterized in that at least one uneven portion is formed on the upper surface. The method of claim 1, At least one trench is formed in any one of the first conductive conductive layer, the intrinsic layer and the second conductive conductive layer formed on the metal wiring. The method of claim 1, And an upper electrode and a color filter array formed on the second conductive conductive layer. The method of claim 1, And an adhesive layer formed between the upper electrode and the

color filter array. The method of claim 4, wherein The adhesive layer is an image sensor, characterized in that formed of a thermal resin. Forming a metal wiring layer including a metal wiring and an interlayer insulating film on the semiconductor substrate on which the CMOS circuit is formed; Forming a first conductivity type conductive layer on the metallization layer; Forming an intrinsic layer on the first conductivity type conductive layer; And Forming a second conductivity type conductive layer on the intrinsic layer; At least one uneven portion is formed on an upper surface of any one of the first conductive conductive layer, the intrinsic layer, and the second conductive conductive layer. The method of claim 6, Forming the uneven portion on the upper surface of any one of the first conductive conductive layer, the intrinsic layer and the second conductive conductive layer formed on the metal wiring, Forming at least one mask pattern on any one of the first conductivity type conductive layer and the intrinsic layer; And forming at least one trench on an upper surface of any one of the first conductive type conductive layer, the intrinsic layer, and the second conductive type conductive layer by using the mask pattern as an etching mask. The method of claim 7, wherein The trench is a method of manufacturing an image sensor, characterized in that formed by a dry etching method or a wet etching method. The method of claim 6, Forming an upper electrode on the second conductive conductive layer; And And forming a color filter array on the upper electrode. The method of claim 1, Forming an adhesive layer formed of a thermal resin on the upper electrode.

Description

translated from Korean

Image sensor and method for manufacturing thereof

1 to 5A are diagrams illustrating a manufacturing process of the image sensor of the first embodiment.

6 to 9 are diagrams illustrating a manufacturing process of the image sensor of the second embodiment.

10 to 13 are diagrams illustrating a manufacturing process of the image sensor of the third embodiment.

The embodiment discloses an image sensor and a method of manufacturing the same.

An image sensor is a semiconductor device that converts an optical image into an electrical signal, and is classified into a charge coupled device (CCD) image sensor and a complementary metal oxide silicon (CMOS) image sensor (CIS). do.

CCD image sensor has complex driving method, high power consumption, multi-stage photo process, and manufacturing process has complicated disadvantage. Therefore, as a next generation image sensor to overcome the disadvantage of the charge coupling device, Morse image sensor is attracting attention.

The CMOS image sensor implements an image by sequentially detecting an electrical signal of each unit pixel by a switching method by forming a photodiode and a MOS transistor in the unit pixel.

This CMOS image sensor is simpler to drive than the CCD image sensor, which is widely used as a conventional image sensor, and can realize various scanning methods, and can integrate signal processing onto a single chip, thereby miniaturizing the product. The use of compatible CMOS technology reduces manufacturing costs and lowers power consumption.

The CMOS image sensor according to the related art may be divided into a photo diode region (not shown) that receives a light signal and converts the light signal into an electrical signal, and a transistor region (not shown) that processes the electrical signal.

However, the CMOS image sensor according to the related art has a structure in which a photodiode and a transistor are horizontally disposed on a semiconductor substrate.

Of course, although the disadvantages of the CCD image sensor have been solved by the horizontal CMOS image sensor according to the prior art, there are still problems in the horizontal CMOS image sensor according to the prior art.

That is, according to the horizontal CMOS image sensor according to the prior art, the photodiode and the transistor are formed adjacent to each other horizontally on the substrate. Accordingly, there is a need for an additional area for forming a photodiode, thereby reducing the fill factor area and limiting the possibility of resolution.

In addition, according to the horizontal CMOS image sensor according to the prior art there is a problem that it is very difficult to achieve the optimization for the process of manufacturing the photodiode and transistor at the same time. That is, in a fast transistor process, a shallow junction is required for low sheet resistance, but such a shallow junction may not be suitable for a photodiode.

In addition, according to the horizontal CMOS image sensor according to the prior art, the size of the unit pixel is increased or decreased to maintain the sensor sensitivity of the image sensor as additional on-chip functions are added to the image sensor. Should be.

However, when the pixel size is increased, the resolution of the image sensor is reduced, and the area of the photodiode decreases in the sensor sensitivity of the image sensor.

The embodiment provides an image sensor and a method of manufacturing the same that can provide new integration of transistor circuits and photodiodes.

The present invention also provides an image sensor and a method of manufacturing the same, in which resolution and sensor sensitivity can be improved together.

In addition, to provide an image sensor and a method of manufacturing the same that can achieve a light condensation rate and simplify the process while employing a vertical photodiode.

An image sensor according to an embodiment includes a semiconductor substrate on which a CMOS circuit is formed; A metal wiring layer including a metal wiring and an interlayer insulating film formed on the semiconductor substrate; A first conductivity type conductive layer formed on the metal wiring layer; An intrinsic layer formed on the first conductivity type conductive layer; And a second conductive conductive layer formed on the intrinsic layer, wherein any one of the first conductive conductive layer, the intrinsic layer, and the second conductive conductive layer has at least one uneven portion formed thereon. It includes.

In addition, the manufacturing method of the image sensor according to the embodiment comprises the steps of: forming a metal wiring layer including a metal wiring and an interlayer insulating film on the semiconductor substrate on which the CMOS circuit is formed; Forming a first conductivity type conductive layer on the metallization layer; Forming an intrinsic layer on the first conductivity type conductive layer; And forming a second conductive conductive layer on the intrinsic layer, and forming an uneven portion on an upper surface of any one of the first conductive conductive layer, the intrinsic layer, and the second conductive conductive layer. Steps.

Hereinafter, an image sensor and a method of manufacturing the same according to an embodiment will be described in detail with reference to the accompanying drawings.

In the description of the embodiments, where described as being formed "on / over" of each layer, the on / over may be directly or through another layer (indirectly) includes everything formed.

In the drawings, the thickness or size of each layer is exaggerated, omitted, or schematically illustrated for convenience and clarity of description. In addition, the size of each component does not necessarily reflect the actual size.

In addition, the same code | symbol was used about the same part in description of each Example.

<First Embodiment>

5A is a cross-sectional view of the image sensor according to the first embodiment.

5A, the image sensor of the embodiment includes a semiconductor substrate 10 on which a CMOS circuit is formed; A metal wiring layer 20 including a metal wiring 22 and an interlayer insulating film 21 formed on the semiconductor substrate 10; A first conductivity type conductive layer 30 formed on the metal wiring layer 20; An intrinsic layer 40 formed on the first conductivity type conductive layer 30; And a second conductivity type conductive layer 51 having an uneven portion 53 formed on an upper surface of the intrinsic layer 40.

The lower electrode 25 may be formed on the metal line 22.

An upper electrode 60 and a color filter array 80 may be formed on the second conductive conductive layer 51.

In addition, an adhesive layer 70 may be formed between the upper electrode 60 and the color filter array 80. For example, the adhesive layer 70 is formed of a thermal resin.

A plurality of trenches 52 may be formed in the second conductive conductive layer 51 so that the upper surface of the second conductive conductive layer 51 may have an uneven portion 53 having a plurality of uneven shapes. .

Alternatively, as illustrated in FIG. 5B, one uneven portion 53b may be formed in the second conductive conductive layer 51b connected to the metal wire 22 to form one pixel.

As shown in FIGS. 5A and 5B, the photodiode formed on the metal wire 25 connected to the CMOS circuit (not shown) is formed to have at least one uneven portion.

Therefore, since the photodiode having at least one uneven portion is formed in one pixel including the CMOS circuit and the photodiode, the area of the photodiode can be increased to increase the light sensing efficiency.

An image sensor according to an embodiment may provide vertical integration of a transistor circuit and a photodiode.

In addition, the fill factor can be approached to 100% by vertical integration of the transistor circuit and the photodiode.

In addition, the vertical integration can provide higher sensitivity at the same pixel size than the prior art.

In addition, each unit pixel can implement a more complex circuit without reducing the sensitivity.

In addition, the surface of the photodiode formed in the unit pixel is formed in a dome shape, so that the surface area per unit pixel is increased, so that the light receiving region of the photodiode is enlarged, thereby increasing the light efficiency.

In addition, the surface of the photodiode formed in the unit pixel is formed in the shape of a dome such as a micro lens to maximize the light collecting rate.

In addition, since the photodiode is formed in a shape similar to a lens, a separate microlens forming process may not be performed, thereby simplifying the process.

A method of manufacturing the image sensor of the first embodiment will be described with reference to FIGS. 1 to 5A.

Referring to FIG. 1, a metal wiring layer 20 including a metal wiring 22 and an interlayer insulating film 21 is formed on a semiconductor substrate 10 on which a CMOS circuit (not shown) is formed.

Although not illustrated, an isolation layer (not shown) defining an active region and a field region is formed in the semiconductor substrate 10, and the photoelectric charges received by the photodiodes connected to a photodiode described later to form a unit pixel are used as electrical signals. A CMOS circuit (not shown) may be formed of a transistor structure for changing the circuit into a transistor.

Although not shown, the metal wiring layer 20 may be formed of a plurality of layers to connect the power line or the signal line to the CMOS circuit.

The metal wiring layer 20 is formed of a plurality of metal wirings 22 formed through the interlayer insulating film 21 and the interlayer insulating film 21 on the semiconductor substrate 10.

For example, the interlayer insulating film 21 may be formed of an oxide film, and the metal wire 22 may be formed of various conductive materials including metal, alloy, or silicide, that is, aluminum, copper, cobalt, or tungsten. .

The lower electrode 25 may be formed on the metal wiring layer 20 to be electrically connected to the metal wiring 22. For example, the lower electrode 25 may be formed of metals such as Cr, Ti, TiW, and Ta. Of course, the lower electrode 25 may not be formed.

A metal pixel 22 connected to the CMOS circuit of the semiconductor substrate 10 may be formed on the interlayer insulating layer 21, and then a photodiode may be formed on the metal wiring layer 20 to form a unit pixel.

The photodiode is formed on the metal wiring layer 220 to receive and receive light incident from the outside to convert and store in an electrical form. In this embodiment, a pin diode is used.

The pin diode is formed of a structure in which an n-type amorphous silicon layer, an intrinsic amorphous silicon layer, and a p-type amorphous silicon layer are bonded to each other. The performance of the photodiode is determined by the efficiency of converting it into electrical form by receiving external light and the total charge capacitance. The existing photodiode is depleted when heterojunction of PN, NP, NPN, PNP, etc. Although the charge is generated and stored in the region, the fin diode is a photodiode having a structure in which an intrinsic amorphous silicon layer, which is a pure semiconductor, is bonded between a p-type silicon layer and an n-type silicon layer. All of the intrinsic amorphous silicon layers formed therebetween become depletion regions, which is advantageous for generation and storage of charges.

As described above, in the exemplary embodiment, a pin diode is used as the photodiode, and the pin diode may have a structure of P-I-N or N-I-P. Particularly, in the embodiment, a pin structure having a PIN structure is used as an example, and the n-type amorphous silicon layer includes a first conductive type conductive layer 30 and the intrinsic amorphous silicon layer. In this case, the intrinsic layer 40 and the p-type amorphous silicon layer are referred to as a second conductivity type conductive layer 50.

A method of forming the photodiode using the pin diode will be described below.

A first conductivity type conductive layer 30 is formed on the metal wiring layer 20. The first conductivity type conductive layer 30 may serve as the N layer of the P-I-N diode employed in the present embodiment. That is, the first conductivity type conductive layer 30 may be an N type conductivity type conductive layer, but is not limited thereto.

The first conductivity type conductive layer 30 may be formed using n-doped amorphous silicon doped with N-type impurities, but is not limited thereto.

That is, the first conductivity type conductive layer 30 is a-Si: H, a-SiGe: H, a-SiC, a-SiN: H a- by adding germanium, carbon, nitrogen or oxygen to amorphous silicon. SiO: H or the like.

In addition, the first conductivity type conductive layer 30 may be formed by chemical vapor deposition (CVD), in particular, PECVD. For example, the first conductive conductive layer 30 may be formed of amorphous silicon by PECVD by mixing PH_3, P_2H_5, and the like with silane gas (SiH_4).

Next, an intrinsic layer 40 is formed on the first conductivity type conductive layer 30. The intrinsic layer 40 may serve as an I layer employed in the embodiment.

The intrinsic layer 40 may be formed using intrinsic amorphous silicon. The intrinsic layer 40 may be formed by chemical vapor deposition (CVD), in particular, PECVD. For example, the intrinsic layer 40 may be formed of amorphous silicon by PECVD using silane gas (SiH_4).

In addition, the intrinsic layer 40 is preferably formed to a thickness of about 10 to 1,000 times the thickness of the first conductive type conductive layer 30. This is because the thicker the intrinsic layer 40 is, the more the depletion region of the photodiode increases, which is advantageous for storing and generating a large amount of photocharges.

Next, a second conductivity type conductive layer 50 is formed on the intrinsic layer 40.

The second conductivity type conductive layer 50 may serve as a P layer of the P-I-N diode employed in the embodiment. That is, the second conductivity type conductive layer 50 may be a P type conductivity type conductive layer, but is not limited thereto.

For example, the second conductivity type conductive layer 50 may be formed using P-doped amorphous silicon, but is not limited thereto.

The second conductivity type conductive layer 50 may be formed by chemical vapor deposition (CVD), in particular, PECVD. For example, the second conductivity type conductive layer 50 may be formed of amorphous silicon by PECVD by mixing a gas such as BH_3 or B_2H_6 with silane gas (SiH_4).

As described above, since the circuit region formed on the semiconductor substrate 10 and the photodiode are vertically formed, the fill factor of the photodiode may approach 100%.

Referring to FIG. 2, a mask pattern 100 is formed on the second conductive conductive layer 50.

The mask pattern 100 is to form the second conductive conductive layer 50 in the form of irregularities. The mask pattern 100 is formed by applying and patterning a photoresist film.

At least one mask pattern 100 may be formed on the second conductive conductive layer 50 so that the upper surface of the second conductive conductive layer 50 has a step difference.

Referring to FIG. 3, the trench 52 is formed by etching the second conductive conductive layer 50 using the mask pattern 100 as an etch mask. Then, the concave-convex portion 53 of the concave-convex shape is formed on the upper surface of the second conductivity type conductive layer 51 by the trench 52.

The second conductive conductive layer 51 may be etched by a dry or wet etching process. In particular, the etching of the second conductivity type conductive layer 51 proceeds so that the intrinsic layer 40 under the second conductivity type conductive layer 51 is not exposed.

As described above, since the uneven portion 53 is formed on the upper surface of the second conductive conductive layer 51, the surface area of the second conductive conductive layer 51 is increased, and thus the light receiving area of the photodiode is increased. This can be extended to improve the light detection rate of the image sensor.

In addition, at least one convex dome-shaped lens is formed in one pixel by the concave-convex portion 53 of the second conductivity type conductive layer 51 to increase the light efficiency of the photodiode.

Referring to FIG. 4, the upper electrode 60 is formed on the second conductive type conductive layer 51 on which the uneven portion 52 is formed.

The upper electrode 60 may be formed of a transparent electrode having good light transmittance and high conductivity. For example, the upper electrode 60 may be formed of indium tin oxide (ITO) or cardium tin oxide (CTO).

By the shape of the uneven portion 53, the upper electrode 60 may also be formed in the uneven shape having a step.

Referring to FIG. 5A, an adhesive layer 70 and a color filter 80 are formed on the upper electrode 60.

The adhesive layer 70 is to improve the adhesion between the upper electrode 60 and the color filter 80. The adhesive layer 70 is formed by depositing a thermal resin on the upper electrode 60 and then performing a planarization process. To form.

In addition, a color filter 80 is formed on the adhesive layer 70.

In the image sensor formed as described above, photodiodes having a plurality of dome shapes may be formed in one pixel, thereby improving light condensation.

Alternatively, as illustrated in FIG. 5B, one uneven portion 53b may be formed in the second conductive conductive layer 51b formed on the metal wiring 22.

As a result, the light receiving area is extended by the uneven shape of the photodiode, thereby increasing the photosensitive index.

Second Embodiment

9 is a sectional view of an image sensor according to a second embodiment.

The image sensor of the embodiment with reference to FIG. 9 includes: a semiconductor substrate 10 on which a CMOS circuit is formed; A metal wiring layer 20 including a plurality of metal wirings 22 and an interlayer insulating film 21 formed on the semiconductor substrate 10; A first conductivity type conductive layer 31 having at least one uneven portion 33 formed on an upper surface of the metal wiring layer 20; An intrinsic layer 40 formed on the first conductivity type conductive layer 31; And a second conductivity type conductive layer 50 formed on the intrinsic layer 40.

At least one trench 32 may be formed in the first conductive conductive layer 31 so that one or more uneven portions 33 may be formed on an upper surface of the first conductive conductive layer 31.

The lower electrode 25 may be formed on the metal line 22.

An upper electrode 60 and a color filter array 80 may be formed on the second conductive conductive layer 50.

In addition, an adhesive layer 70 may be formed between the upper electrode 60 and the color filter array 80. For example, the adhesive layer 70 is formed of a thermal resin.

A manufacturing process of the image sensor of the second embodiment will be described with reference to FIGS. 6 to 9.

Referring to FIG. 6, a metal wiring layer 20 and a lower electrode 25 are formed on the semiconductor substrate 10.

Since the semiconductor substrate 10, the metallization layer 20, and the lower electrode 25 are the same as in the above-described first embodiment, description thereof will be omitted.

After forming the metal wiring 22 connected to the CMOS circuit of the semiconductor substrate 10 on the interlayer insulating film 21, a photodiode is formed on the metal wiring layer 20.

The photodiode is formed on the metal wiring layer 220 to receive and receive light incident from the outside to convert and store in an electrical form. In this embodiment, a pin diode is used. Since the photodiode used in the second embodiment is the same as the first embodiment, a detailed description thereof will be omitted and only the process sequence will be described.

A method of forming the photodiode using the pin diode will be described below.

After forming the first conductive conductive layer 30 on the metal wiring layer 20, at least one mask pattern 100 is formed on the first conductive conductive layer 30.

The mask pattern 100 is for forming the first conductivity type conductive layer 30 in the form of irregularities. The mask pattern 100 is formed by coating and patterning a photoresist film. At least one mask pattern 100 may be formed on the first conductivity type conductive layer 30 so that the upper surface of the first conductivity type conductive layer 30 has a step difference.

Referring to FIG. 7, the trench 32 is formed by etching the first conductive conductive layer 30 using the mask pattern 100 as an etch mask. Then, the concave-convex portion 33 having the concave-convex shape is formed on the upper surface of the first conductivity type conductive layer 31 by the trench 32.

The first conductive conductive layer 31 may be etched by a dry or wet etching process. In particular, the etching of the first conductivity type conductive layer 31 proceeds so that the metal wiring layer 20 positioned under the first conductivity type conductive layer 31 is not exposed.

Referring to FIG. 8, an intrinsic layer 40 and a second conductive conductive layer 50 are sequentially formed on the first conductive conductive layer 30.

Then, the intrinsic layer 40 formed along the upper surface of the first conductivity type conductive layer 31 has a stepped upper surface by the uneven portion 33 of the first conductivity type conductive layer 31. The second conductive conductive layer 50 has a stepped upper surface by the intrinsic layer 40.

Therefore, the surface of the photodiode including the first conductive conductive layer 31, the intrinsic layer 40, and the second conductive conductive layer 50 is formed in an uneven shape to improve the light sensing rate due to the increase of the surface area. it becomes possible.

In addition, since the photodiode has a shape such as a convex lens, it is possible to improve the light collecting rate.

In addition, the photodiode may have at least one uneven portion per pixel to increase the light detection rate of the photodiode.

Referring to FIG. 9, an upper electrode 60 is formed on the second conductive conductive layer 50.

The upper electrode 60 may be formed of a transparent electrode having good light transmittance and high conductivity. For example, the upper electrode 60 may be formed of indium tin oxide (ITO) or cardium tin oxide (CTO).

The adhesive layer 70 and the color filter 80 are formed on the upper electrode 60.

The adhesive layer 70 is to improve the adhesion between the upper electrode 60 and the color filter 80. The adhesive layer 70 is formed by depositing a thermal resin on the upper electrode 60 and then performing a planarization process. To form.

In addition, a color filter 80 is formed on the adhesive layer 70.

Third Embodiment

13 is a sectional view of an image sensor according to a third embodiment.

The image sensor of the embodiment with reference to FIG. 13 includes a semiconductor substrate 10 having a CMOS circuit formed thereon; A metal wiring layer 20 including a plurality of metal wirings 22 and an interlayer insulating film 21 formed on the semiconductor substrate 10; A first conductivity type conductive layer 30 formed on the metal wiring layer 20; An intrinsic layer 41 having at least one uneven portion 43 formed on an upper surface of the first conductive conductive layer 30; And a second conductivity type conductive layer 50 formed on the intrinsic layer 41.

At least one trench 42 may be formed in the intrinsic layer 41, and at least one uneven portion 43 may be formed on an upper surface of the intrinsic layer 41.

The lower electrode 25 may be formed on the metal line 22.

An upper electrode 60 and a color filter array 80 may be formed on the second conductive conductive layer 50.

In addition, an adhesive layer 70 may be formed between the upper electrode 60 and the color filter array 80. For example, the adhesive layer 70 is formed of a thermal resin.

A manufacturing process of the image sensor of the second embodiment will be described with reference to FIGS. 10 to 13.

Referring to FIG. 10, a metal wiring layer 20 and a lower electrode 25 are formed on the semiconductor substrate 10.

Since the semiconductor substrate 10, the metallization layer 20, and the lower electrode 25 are the same as those of the first embodiment described above, description thereof will be omitted.

After forming the metal wiring 22 connected to the CMOS circuit of the semiconductor substrate 10 on the interlayer insulating film 21, a photodiode is formed on the metal wiring layer 20.

The photodiode is formed on the metal wiring layer 220 to receive and receive light incident from the outside to convert and store in an electrical form. In this embodiment, a pin diode is used. Since the photodiode used in the second embodiment is the same as the first embodiment, a detailed description thereof will be omitted and only the process sequence will be described.

A method of forming the photodiode using the pin diode will be described below.

The first conductivity type conductive layer 30 and the intrinsic layer 40 are sequentially formed on the metal wiring layer 20.

The mask pattern 100 is formed on the intrinsic layer 40.

The mask pattern 100 is for forming the intrinsic layer 40 in the form of irregularities. The mask pattern 100 is formed by applying and patterning a photoresist film. At least one mask pattern 100 may be formed on the intrinsic layer 40 so that the upper surface of the intrinsic layer 41 has a step.

Referring to FIG. 11, the trench 42 is formed by etching the intrinsic layer 40 using the mask pattern 100 as an etch mask. Then, the uneven portions 43 having the uneven shape are formed on the upper surface of the intrinsic layer 41 by the trench 42.

The intrinsic layer 41 may be etched by a dry or wet etching process. In particular, the etching of the intrinsic layer 41 proceeds so that the first conductivity type conductive layer 30 positioned below the intrinsic layer 41 is not exposed.

Referring to FIG. 12, a second conductivity type conductive layer 50 is formed on the intrinsic layer 41.

Then, in the second conductive type conductive layer 50 formed along the upper surface of the intrinsic layer 41, the upper surface is stepped by the uneven portion 43 of the intrinsic layer 41.

Therefore, the surface of the photodiode including the first conductive conductive layer 30, the intrinsic layer 41, and the second conductive conductive layer 50 is formed in an uneven shape to improve the light sensing rate due to the increase of the surface area. It becomes possible.

In addition, since the photodiode has a shape such as a convex lens, it is possible to improve the light collecting rate.

Referring to FIG. 9, an upper electrode 60 is formed on the second conductive conductive layer 50.

The upper electrode 60 may be formed of a transparent electrode having good light transmittance and high conductivity. For example, the upper electrode 60 may be formed of indium tin oxide (ITO) or cardium tin oxide (CTO).

The adhesive layer 70 and the color filter 80 are formed on the upper electrode 60.

The adhesive layer 70 is to improve the adhesion between the upper electrode 60 and the color filter 80. The adhesive layer 70 is formed by depositing a thermal resin on the upper electrode 60 and then performing a planarization process. To form.

In addition, a color filter 80 is formed on the adhesive layer 70.

The embodiments described above are not limited to the above-described embodiments and drawings, and it is to be understood that various changes, modifications, and changes can be made without departing from the technical spirit of the present embodiments. It will be obvious to those who have it.

According to the image sensor and the manufacturing method thereof according to the embodiment, it is possible to provide vertical integration of the transistor circuit and the photodiode.

In addition, the fill factor can be approached to 100% by vertical integration of the transistor circuit and the photodiode.

In addition, the vertical integration can provide higher sensitivity at the same pixel size than the prior art.

In addition, each unit pixel can implement a more complex circuit without reducing the sensitivity.

In addition, by adopting a vertical photodiode, insulation between unit pixels is secured, thereby preventing crosstalk between pixels and the like, thereby improving reliability of the image sensor.

In addition, in implementing the unit pixel of the photodiode, the light sensing ratio may be improved by increasing the surface area of the photodiode in the unit pixel.

In addition, the photodiode corresponding to the unit pixel may have a lens shape such as a convex lens, thereby improving the light condensing ratio.

Cited By (2)

Publication number	Priority date	Publication date	Assignee	Title
CN109723127A *	2017-10-30	2019-05-07	上海箩寰技术有限公司	Photodiode and forming method thereof, imaging sensor, fingerprint imaging mould group
US20210242354A1 *	2015-11-17	2021-08-05	W&Wsens Devices, Inc.	Microstructure enhanced absorption photosensitive devices

Family To Family Citations

* Cited by examiner, † Cited by third party, ‡ Family to family citation

Similar Documents

Publication	Publication Date	Title
KR100851756B1	2008-08-11	Image sensor and method for manufacturing therof
KR100894391B1	2009-04-20	Image Sensor and Method for Manufacturing Thereof
KR100935771B1	2010-01-06	Image Sensor and Method for Manufacturing Thereof
KR100872719B1	2008-12-05	Image Sensor and Method for Manufacturing thereof
KR100913019B1	2009-08-20	Image Sensor and Method for Manufacturing Thereof
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KR100872990B1	2008-12-08	Image Sensor and Method for Fabrication of the Same
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KR100871973B1	2008-12-08	Image Sensor and Method for Manufacturing thereof
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KR20080101301A	2008-11-21	Image sensor and method for manufacturing thereof
KR100924412B1	2009-10-29	Image Sensor and Method for Manufacturing Thereof
KR100935768B1	2010-01-06	Method for Manufacturing of Image Sensor
KR20090044117A	2009-05-07	Image sensor and method for manufacturing thereof

Priority And Related Applications

Priority Applications (1)

Application	Priority date	Filing date	Title
KR1020070047886A	2007-05-17	2007-05-17	Image sensor and method for manufacturing thereof

Applications Claiming Priority (1)

Application	Filing date	Title
KR1020070047886A	2007-05-17	Image sensor and method for manufacturing thereof

Legal Events

Date	Code	Title	Description
2007-05-17	A201	Request for examination	
2008-04-15	E902	Notification of reason for refusal	
2008-10-20	E601	Decision to refuse application	

Concepts

machine-extracted

Download Filter table

Name	Image	Sections	Count	Query match
manufacturing process		title,claims,abstract,description	20	0.000
metal		claims,abstract,description	53	0.000
metal		claims,abstract,description	53	0.000
semiconductor		claims,abstract,description	28	0.000
substrate		claims,abstract,description	26	0.000
layer		claims,description	228	0.000
adhesive		claims,description	21	0.000
adhesive		claims,description	21	0.000
interlayer		claims,description	14	0.000

resin	claims,description	8	0.000
resin	claims,description	8	0.000
etching	claims,description	7	0.000
dry etching	claims,description	4	0.000
metallisation	claims,description	4	0.000
wet etching	claims,description	4	0.000
method	abstract,description	16	0.000
sensitivity	abstract,description	8	0.000
silicon	abstract,description	4	0.000
silicon	abstract,description	4	0.000
complement	abstract,description	2	0.000
insulation	abstract,description	2	0.000
metal oxide	abstract,description	2	0.000
metal oxides	abstract,description	2	0.000

Show all concepts from the description section

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(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

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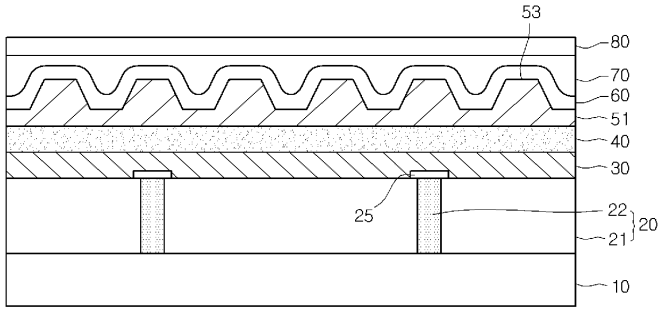
전체 청구항 수 : 총 10 항

(54) 이미지 센서 및 그의 제조방법

(57) 요 약

실시예는 이미지 센서에 관한 것으로, 씨모스 회로가 형성된 반도체 기판; 상기 반도체 기판 상에 형성된 금속배선 및 층간절연막을 포함하는 금속배선층; 상기 금속배선층 상에 형성된 제1 도전형 전도층; 상기 제1 도전형 전도층 상에 형성된 진성층; 및 상기 진성층 상에 상부 표면에 적어도 하나 이상의 요철부가 형성된 제2 도전형 전도층을 포함한다.

대 표 도 - 도5a



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특허청구의 범위

청구항 1

씨모스 회로가 형성된 반도체 기판;

상기 반도체 기판 상에 형성된 금속배선 및 층간절연막을 포함하는 금속배선층;

상기 금속배선층 상에 형성된 제1 도전형 전도층;

상기 제1 도전형 전도층 상에 형성된 진성층; 및

상기 진성층 상에 형성된 제2 도전형 전도층을 포함하며,

상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층은 그 상부 표면에 적어도 하나 이상의 요철부가 형성된 것을 특징으로 하는 이미지 센서.

청구항 2

제1항에 있어서,

상기 금속배선 상에 형성된 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층에는 적어도 하나 이상의 트렌치가 형성된 것을 포함하는 이미지 센서.

청구항 3

제1항에 있어서,

상기 제2 도전형 전도층 상부에는 상부전극 및 컬러필터 어레이가 형성된 것을 포함하는 이미지 센서.

청구항 4

제1항에 있어서,

상기 상부전극과 컬러필터 어레이 사이에는 접착층이 형성된 것을 포함하는 이미지 센서.

청구항 5

제4항에 있어서,

상기 접착층은 열 수지로 형성된 것을 특징으로 하는 이미지 센서.

청구항 6

씨모스 회로가 형성된 반도체 기판 상에 금속배선 및 층간절연막을 포함하는 금속배선층을 형성하는 단계;

상기 금속배선층 상에 제1 도전형 전도층을 형성하는 단계;

상기 제1 도전형 전도층 상에 진성층을 형성하는 단계; 및

상기 진성층 상에 제2 도전형 전도층을 형성하는 단계를 포함하며,

상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층의 상부 표면에는 적어도 하나 이상의 요철부가 형성되는 단계를 포함하는 이미지 센서의 제조방법.

청구항 7

제6항에 있어서,

상기 금속배선 상에 형성된 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층의 상부표면에 요철부를 형성하는 단계는,

상기 제1 도전형 전도층, 진성층 중 어느 하나의 층 상에 적어도 하나 이상의 마스크 패턴을 형성하는 단계;

상기 마스크 패턴을 식각 마스크로 하여 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의

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층 상부 표면에 적어도 하나 이상의 트렌치를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 8

제7항에 있어서,

상기 트렌치는 건식식각 또는 습식식각 방법으로 형성된 것을 특징으로 하는 이미지 센서의 제조방법.

청구항 9

제6항에 있어서,

상기 제2 도전형 전도층 상에 상부전극을 형성하는 단계; 및

상기 상부전극 상에 컬러필터 어레이를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 10

제1항에 있어서,

상기 상부전극 상에 열 수지로 형성된 접착층을 형성하는 단계를 포함하는 이미지 센서의 제조방법.

명 세 서

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

<4> 실시예는 이미지 센서 및 그의 제조방법을 개시한다.

<5> 이미지 센서는 광학적 영상(Optical Image)을 전기 신호로 변환시키는 반도체 소자로서, 크게 전하결합소자(charge coupled device:CCD) 이미지 센서와 씨모스(Complementary Metal Oxide Silicon:CMOS) 이미지 센서(CIS)로 구분된다.

<6> CCD 이미지 센서는 구동방식이 복잡하고, 전력소비가 클 뿐만 아니라, 다단계의 포토공정이 요구되므로 제조공정이 복잡한 단점을 갖고 있으므로, 최근에는 상기 전하결합소자의 단점을 극복하기 위한 차세대 이미지 센서로서 씨모스 이미지 센서가 주목을 받고 있다.

<7> 씨모스 이미지 센서는 단위 화소 내에 포토다이오드와 모스트랜지스터를 형성시킴으로써 스위칭 방식으로 각 단위 화소의 전기적 신호를 순차적으로 검출하여 영상을 구현한다.

<8> 이러한 씨모스 이미지 센서는 종래 이미지 센서로 널리 사용되고 있는 CCD 이미지 센서에 비하여 구동방식이 간편하고 다양한 스캐닝 방식의 구현이 가능하며, 신호처리를 단일칩에 집적할 수 있어 제품의 소형화가 가능할 뿐만 아니라, 호환성의 씨모스 기술을 사용하므로 제조단가를 낮출 수 있고,전력 소모 또한 낮다는 장점을 지니고 있다.

<9> 종래기술에 의한 씨모스 이미지 센서는 빛 신호를 받아서 전기신호로 바꾸어 주는 포토다이오드(Photo diode) 영역(미도시)과 이 전기 신호를 처리하는 트랜지스터 영역(미도시)으로 구분할 수 있다.

<10> 그런데 종래기술에 따른 씨모스 이미지 센서는 포토다이오드와 트랜지스터가 반도체 기판에 수평으로 배치되는 구조이다.

<11> 물론, 종래기술에 의한 수평형 씨모스 이미지 센서에 의해 CCD 이미지 센서의 단점이 해결되기는 하였으나, 종래기술에 의한 수평형 씨모스 이미지 센서에는 여전히 문제점들이 있다.

<12> 즉, 종래기술에 의한 수평형 씨모스 이미지 센서에 의하면 포토다이오드와 트랜지스터가 기판 상에 상호 수평으로 인접하여 형성된다. 이에 따라, 포토다이오드 형성을 위한 추가적인 영역이 요구되며, 이에 의해 필 팩터(fill factor) 영역을 감소시키고 레졸루션(Resolution)의 가능성을 제한하는 문제가 있다.

<13> 또한, 종래기술에 의한 수평형 씨모스 이미지 센서에 의하면 포토다이오드와 트랜지스터를 동시에 제조하는 공

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정에 대한 최적화를 달성하는 점이 매우 어려운 문제가 있다. 즉, 신속한 트랜지스터 공정에서는 작은 면저항(low sheet resistance)을 위해 샐로우 정션(shllow junction)이 요구되나, 포토다이오드에는 이러한 샐로우 정션(shllow junction)이 적절하지 않을 수 있다.

<14> 또한, 종래기술에 의한 수평형 씨모스 이미지 센서에 의하면 추가적인 온칩(on-chip) 기능들이 이미지 센서에 부가되면서 단위화소의 크기가 이미지 센서의 센서티버티(sensitivity)를 유지하기 위해 증가되거나 또는 감소되어야 한다.

<15> 그런데, 픽셀사이즈가 증가되면 이미지 센서의 레졸루션(Resolution)이 감소하게 되며, 또한 포토다이오드의 면적이 이미지 센서의 센서티버티(sensitivity)가 감소하는 문제가 발생한다.

발명이 이루고자 하는 기술적 과제

<16> 실시예는 트랜지스터 회로와 포토다이오드의 새로운 집적을 제공할 수 있는 이미지 센서 및 그의 제조방법을 제공한다.

<17> 또한, 레졸루션(Resolution)과 센서티버티(sensitivity)가 함께 개선될 수 있는 이미지 센서 및 그의 제조방법을 제공한다.

<18> 또한, 수직형의 포토다이오드를 채용하면서 집광률 향상과 동시에 공정 단순화를 이룰 수 있는 이미지 센서 및 그의 제조방법을 제공하고자 한다.

발명의 구성 및 작용

<19> 실시예에 따른 이미지 센서는, 씨모스 회로가 형성된 반도체 기판; 상기 반도체 기판 상에 형성된 금속배선 및 층간절연막을 포함하는 금속배선층; 상기 금속배선층 상에 형성된 제1 도전형 전도층; 상기 제1 도전형 전도층 상에 형성된 진성층; 및 상기 진성층 상에 형성된 제2 도전형 전도층을 포함하고, 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층은 그 상부 표면에 적어도 하나 이상의 요철부가 형성된 것을 포함한다.

<20> 또한, 실시예에 따른 이미지 센서의 제조방법은, 씨모스 회로가 형성된 반도체 기판 상에 금속배선 및 층간절연막을 포함하는 금속배선층을 형성하는 단계; 상기 금속배선층 상에 제1 도전형 전도층을 형성하는 단계; 상기 제1 도전형 전도층 상에 진성층을 형성하는 단계; 및 상기 진성층 상에 제2 도전형 전도층을 형성하는 단계를 포함하며, 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층의 상부 표면에 요철부를 형성하는 단계를 포함한다.

<21> 이하, 실시예에 따른 이미지 센서 및 그의 제조방법을 첨부된 도면을 참조하여 상세히 설명한다.

<22> 실시예의 설명에 있어서, 각 층의 "상/위(on/over)"에 형성되는 것으로 기재되는 경우에 있어, 상/위(on/over)는 직접(directly)와 또는 다른 층을 개재하여(indirectly) 형성되는 것을 모두 포함한다.

<23> 도면에서 각층의 두께나 크기는 설명의 편의 및 명확성을 위하여 과장되거나 생략되거나 또는 개략적으로 도시되었다. 또한 각 구성요소의 크기는 실제크기를 전적으로 반영하는 것은 아니다.

<24> 또한, 각 실시예의 설명에 있어서 동일한 부분에 대하여 동일한 부호를 사용하였다.

<25> <제1 실시예>

<26> 도 5a는 제1 실시예에 따른 이미지 센서의 단면도이다.

<27> 도 5a를 참조하여, 실시예의 이미지 센서는, 씨모스 회로가 형성된 반도체 기판(10); 상기 반도체 기판(10) 상에 형성된 금속배선(22) 및 층간절연막(21)을 포함하는 금속배선층(20); 상기 금속배선층(20) 상에 형성된 제1 도전형 전도층(30); 상기 제1 도전형 전도층(30) 상에 형성된 진성층(40); 및 상기 진성층(40) 상에 상부표면에 요철부(53)가 형성된 제2 도전형 전도층(51)을 포함한다.

<28> 상기 금속배선(22) 상부에는 하부전극(25)이 형성될 수 있다.

<29> 상기 제2 도전형 전도층(51) 상부에는 상부전극(60) 및 컬러필터 어레이(80)가 형성될 수 있다.

<30> 또한, 상기 상부전극(60)과 컬러필터 어레이(80) 사이에는 접착층(70)이 형성될 수 있다. 예를 들어 상기 접착층(70)은 열 수지(thermal resin)로 형성된다.

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<31> 상기 제2 도전형 전도층(51)에는 복수개의 트렌치(52)가 형성되어 상기 제2 도전형 전도층(51)의 상부표면은 복수개의 요철형상을 갖는 요철부(53)가 형성될 수 있다.

<32> 또는, 도 5b에 도시된 바와 같이 상기 금속배선(22)과 연결되어 하나의 픽셀을 이루는 상기 제2 도전형 전도층(51b)에는 하나의 요철부(53b)가 형성될 수 있다.

<33> 도 5a 및 도 5b에 도시된 바와 같이, 씨모스 회로(미도시)와 연결되는 금속배선(25) 상에 형성된 포토다이오드가 적어도 하나 이상의 요철부를 가지도록 형성된다.

<34> 따라서, 씨모스 회로와 포토다이오드로 이루어지는 하나의 픽셀에 적어도 하나 이상의 요철부를 갖는 포토다이오드가 형성되므로써 상기 포토다이오드의 면적이 증가되어 광감지 효율을 증가시킬 수 있다.

<35> 실시예에 따른 이미지 센서는 트랜지스터 회로와 포토다이오드의 수직형 집적을 제공할 수 있다.

<36> 또한, 트랜지스터 회로와 포토다이오드의 수직형 집적에 의해 필 팩터(fill factor)를 100%에 근접시킬 수 있다.

<37> 또한, 수직형 집적에 의해 종래기술보다 같은 픽셀 사이즈에서 높은 센서티비티(sensitivity)를 제공할 수 있다.

<38> 또한, 각 단위 픽셀은 센서티비티(sentivity)의 감소없이 보다 복잡한 회로를 구현할 수 있다.

<39> 또한, 단위 픽셀 내에 형성된 포토다이오드의 표면이 돔 형태로 형성되어 단위 픽셀 당 표면적이 증가하여 포토다이오드의 수광영역이 확대되어 광효율을 증가지시킬 수 있다.

<40> 또한, 단위 픽셀 내에 형성된 포토다이오드의 표면이 마이크로렌즈와 같은 돔형태로 형성되어 집광율을 극대화 시킬 수 있다.

<41> 또한, 상기 포토다이오드의 형태가 렌즈와 유사한 형태로 형성되어 별도의 마이크로렌즈 형성공정을 진행하지 않아도 되므로 공정을 단순화 시킬 수 있다.

<42> 도 1 내지 도 5a를 참조하여 제1 실시예의 이미지 센서의 제조방법을 설명한다.

<43> 도 1을 참조하여, 씨모스 회로(미도시)가 형성된 반도체 기판(10) 상에는 금속배선(22) 및 층간절연막(21)을 포함하는 금속배선층(20)이 형성되어 있다.

<44> 도시하지는 않았지만, 상기 반도체 기판(10)에는 액티브 영역 및 필드 영역을 정의하는 소자분리막(미도시)이 형성되어 있으며, 단위 픽셀을 형성하기 위해 후술되는 포토다이오드에 연결되어 수광된 광전하를 전기신호로 변화시키기 위한 트랜지스터 구조물로 이루어진 씨모스 회로(미도시)가 형성되어 있을 수 있다.

<45> 도시하지는 않았지만, 상기 금속배선층(20)은 전원라인 또는 신호라인과 씨모스 회로를 접속시키기 위해 복수의 층으로 형성될 수 있다.

<46> 상기 금속배선층(20)은 반도체 기판(10) 상에 층간절연막(21)과 상기 층간절연막(21)을 관통하여 형성되는 복수의 금속배선(22)으로 형성되어 있다.

<47> 예를 들어, 상기 층간절연막(21)은 산화막으로 형성될 수 있으며, 상기 금속배선(22)은 금속, 합금 또는 실리사이드를 포함한 다양한 전도성 물질, 즉 알루미늄, 구리, 코발트 또는 텅스텐 등으로 형성할 수 있다.

<48> 상기 금속배선층(20) 상에 상기 금속배선(22)과 전기적으로 연결되는 하부전극(25)을 형성할 수도 있다. 예를 들어, 상기 하부전극(25)은 Cr, Ti, TiW 및 Ta과 같은 금속으로 형성할 수 있다. 물론 상기 하부전극(25)은 형성되지 않을 수 있다.

<49> 상기 층간절연막(21)에 상기 반도체 기판(10)의 씨모스 회로와 연결되는 금속배선(22)을 형성한 후 상기 금속배선층(20) 상부로 포토다이오드를 형성하여 단위픽셀을 형성할 수 있다.

<50> 상기 포토다이오드는 금속배선층(220) 상부에 형성되어 외부에서 입사되는 빛을 받아 전기적 형태로 전환 및 보관하기 위한 것으로 실시예에서는 핀 다이오드(PIN diode)를 사용한다.

<51> 상기 핀 다이오드는 n형 비정질 실리콘층(n-type amorphous silicon), 진성 비정질 실리콘층(intrinsic amorphous silicon), p형 비정질 실리콘층(p-type amorphous silicon)이 접합된 구조로 형성되는 것이다. 포토다이오드의 성능은 외부의 빛을 받아 전기적 형태로 전환하는 효율과 총 보관 가능 전기량(charge capacitanc

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e)에 따라 결정되는 것으로 기존의 포토다이오드는 P-N, N-P, N-P-N, P-N-P 등의 이종접합시 생성되는 공핍영역(Depletion region)에 전하를 생성 및 보관하였으나, 상기 핀 다이오드는 p형 실리콘층과 n형 실리콘층 사이에 순수한 반도체인 진성 비정질 실리콘층이 접합된 구조의 광 다이오드로서, 상기 p형과 n형 사이에 형성되는 진성 비정질 실리콘층이 모두 공핍영역이 되어 전하의 생성 및 보관에 유리하게 된다.

<52> 이와 같이 실시예에서는 포토다이오드로서 핀 다이오드를 사용하며 핀 다이오드의 구조는 P-I-N 또는 N-I-P의 구조로 형성될 수 있다. 특히, 실시예에서는 P-I-N 구조의 핀 다이오드가 사용되는 것을 예로 하며, 상기 n형 비정질 실리콘층(n-type amorphous silicon)은 제1 도전형 전도층(30), 상기 진성 비정질 실리콘층(intrinsic amorphous silicon)은 진성층(40), 상기 p형 비정질 실리콘층(p-type amorphous silicon)은 제2 도전형 전도층(50)이라 칭하도록 한다.

<53> 상기 핀 다이오드를 이용한 포토다이오드를 형성하는 방법에 대하여 설명하면 다음과 같다.

<54> 상기 금속배선층(20) 상에 제1 도전형 전도층(30)을 형성한다. 상기 제1 도전형 전도층(30)은 본 실시에에서 채용하는 P-I-N 다이오드의 N층의 역할을 할 수 있다. 즉, 상기 제1 도전형 전도층(30)은 N타입 도전형 전도층 일 수 있으나 이에 한정되는 것은 아니다.

<55> 상기 제1 도전형 전도층(30)은 N형 불순물이 도핑된 비정질 실리질 실리콘(n-doped amorphous silicon)을 이용하여 형성될 수 있으나, 이에 한정되는 것은 아니다.

<56> 즉, 상기 제1 도전형 전도층(30)은 비정질 실리콘에 게르마늄, 탄소,질소 또는 산소 등을 첨가하여 a-Si:H, a-SiGe:H, a-SiC, a-SiN:H a-SiO:H 등으로 형성될 수도 있다.

<57> 또한, 상기 제1 도전형 전도층(30)은 화학기상증착(CVD) 특히, PECVD 등에 의해 형성될 수 있다. 예를 들어, 상기 제1 도전형 전도층(30)은 실란가스(SiH_4)에 PH_3, P_2H_5 등을 혼합하여 PECVD에 의해 비정질 실리콘으로 형성될 수 있다.

<58> 그 다음, 상기 제1 도전형 전도층(30) 상으로 진성층(intrinsic layer)(40)을 형성한다. 상기 진성층(40)은 실시예에서 채용하는 I층의 역할을 할 수 있다.

<59> 상기 진성층(40)은 비정질 실리콘(intrinsic amorphous silicon)을 이용하여 형성될 수 있다. 상기 진성층(40)은 화학기상증착(CVD) 특히, PECVD 등에 의해 형성될 수 있다. 예를 들어, 상기 진성층(40)은 실란가스(SiH_4) 등을 이용하여 PECVD에 의해 비정질 실리콘으로 형성될 수 있다.

<60> 또한, 상기 진성층(40)은 상기 제1 도전형 전도층(30)의 두께 보다 약 10~1,000배 정도의 두꺼운 두께로 형성하는 것이 바람직하다. 이는 상기 진성층(40)의 두께가 두꺼울수록 포토다이오드의 공핍영역이 늘어나 많은 양의 광전하를 보관 및 생성하기에 유리하기 때문이다.

<61> 그 다음, 상기 진성층(40) 상으로 제2 도전형 전도층(50)을 형성한다.

<62> 상기 제2 도전형 전도층(50)은 실시예에서 채용하는 P-I-N 다이오드의 P층의 역할을 할 수 있다. 즉, 상기 제2 도전형 전도층(50)은 P 타입 도전형 전도층일 수 있으나 이에 한정되는 것은 아니다.

<63> 예를 들어, 상기 제2 도전형 전도층(50)은 P 도핑된 비정질 실리콘(p-doped amorphous silicon)을 이용하여 형성될 수 있으나, 이에 한정되는 것은 아니다.

<64> 상기 제2 도전형 전도층(50)은 화학기상증착(CVD) 특히, PECVD 등에 의해 형성될 수 있다. 예를 들어, 상기 제2 도전형 전도층(50)은 실란가스(SiH_4)에 BH_3 또는 B_2H_6 등의 가스를 혼합하여 PECVD에 의해 비정질 실리콘으로 형성될 수 있다.

<65> 상기와 같이 반도체 기판(10)에 형성된 회로영역과 포토다이오드가 수직형으로 형성됨으로써 포토다이오드의 필팩터(fill factor)를 100%에 근접시킬 수 있다.

<66> 도 2를 참조하여, 상기 제2 도전형 전도층(50) 상부로 마스크 패턴(100)을 형성한다.

<67> 상기 마스크 패턴(100)은 상기 제2 도전형 전도층(50)을 요철형태로 형성하기 위한 것으로, 포토레지스트 필름을 도포하고 패터닝하여 형성한다.

<68> 상기 마스크 패턴(100)은 상기 제2 도전형 전도층(50) 상에 적어도 하나 이상 형성되어 상기 제2 도전형 전도층(50)의 상부 표면이 단차를 가지도록 형성할 수 있다.

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<69> 도 3을 참조하여, 상기 마스크 패턴(100)을 식각마스크로 하여 상기 제2 도전형 전도층(50)을 식각하여 트렌치(52)를 형성한다. 그러면 상기 트렌치(52)에 의해 상기 제2 도전형 전도층(51)의 상부 표면은 요철형태의 요철부(53)가 형성된다.

<70> 상기 제2 도전형 전도층(51)의 식각은 건식 또는 습식식각 공정으로 진행될 수 있다. 특히, 상기 제2 도전형 전도층(51)의 식각은 상기 제2 도전형 전도층(51) 하부에 위치한 진성층(40)이 노출되지 않도록 진행한다.

<71> 상기와 같이, 상기 제2 도전형 전도층(51)의 상부 표면에 요철부(53)가 형성됨으로써 상기 제2 도전형 전도층(51)의 표면적은 증가하게 되고, 이로 인해 포토다이오드의 수광영역이 확장되어 이미지 센서의 광감지율을 향상시킬 수 있다.

<72> 또한, 상기 제2 도전형 전도층(51)의 요철부(53)에 의하여 하나의 픽셀 내에 볼록한 돔 형상의 렌즈가 적어도 하나 이상 형성되어 포토다이오드의 광 효율을 증가시킬 수 있다.

<73> 도 4를 참조하여, 상기 요철부(52)가 형성된 제2 도전형 전도층(51)의 상부로 상부전극(60)을 형성한다.

<74> 상기 상부전극(60)은 빛의 투과성이 좋고 전도성이 높은 투명전극으로 형성될 수 있다. 예를 들어, 상기 상부전극(60)은 ITO(indium tin oxide) 또는 CTO(cardium tin oxide) 등으로 형성될 수 있다.

<75> 상기 요철부(53)의 형태에 의하여 상기 상부전극(60)도 단차를 가지는 요철형태로 형성될 수 있다.

<76> 도 5a를 참조하여, 상기 상부전극(60) 상으로 접착층(70) 및 컬러필터(80)를 형성한다.

<77> 상기 접착층(70)은 상기 상부전극(60)과 컬러필터(80)의 접착력을 향상시키기 위한 것으로, 상기 상부전극(60) 상으로 열 수지(thermal resin)를 증착하여 형성한 후 평탄화 공정을 진행하여 형성한다.

<78> 그리고, 상기 접착층(70)의 상부로 컬러필터(80)를 형성한다.

<79> 상기와 같이 형성된 이미지 센서는 하나의 픽셀 내에 복수의 돔형태를 갖는 포토다이오드가 형성되어 집광율을 향상시킬 수 있다.

<80> 또는 도 5b에 도시된 바와 같이, 상기 금속배선(22) 상에 형성된 제2 도전형 전도층(51b)에 하나의 요철부(53b)가 형성될 수 있다.

<81> 그러면 상기 포토다이오드의 요철형태에 의하여 수광면적이 확장되어 감광지율을 높일 수 있다.

<82> <제2 실시예>

<83> 도 9는 제2 실시예에 따른 이미지 센서의 단면도이다.

<84> 도 9를 참조하여 실시예의 이미지 센서는, 씨모스 회로가 형성된 반도체 기판(10); 상기 반도체 기판(10) 상에 형성된 복수의 금속배선(22) 및 층간절연막(21)을 포함하는 금속배선층(20); 상기 금속배선층(20) 상에 상부표면에 적어도 하나 이상의 요철부(33)가 형성된 제1 도전형 전도층(31); 상기 제1 도전형 전도층(31) 상에 형성된 진성층(40); 및 상기 진성층(40) 상에 형성된 제2 도전형 전도층(50)을 포함한다.

<85> 상기 제1 도전형 전도층(31)에는 적어도 하나 이상의 트렌치(32)가 형성되어 상기 제1 도전형 전도층(31)의 상부표면은 하나 이상의 요철부(33)가 형성될 수 있다.

<86> 상기 금속배선(22) 상부에는 하부전극(25)이 형성될 수 있다.

<87> 상기 제2 도전형 전도층(50) 상부에는 상부전극(60) 및 컬러필터 어레이(80)가 형성될 수 있다.

<88> 또한, 상기 상부전극(60)과 컬러필터 어레이(80) 사이에는 접착층(70)이 형성될 수 있다. 예를 들어 상기 접착층(70)은 열 수지(thermal resin)로 형성된다

<89> 도 6 내지 도 9를 참조하여 제2 실시예의 이미지 센서의 제조공정을 설명한다.

<90> 도 6을 참조하여, 반도체 기판(10) 상에는 금속배선층(20) 및 하부전극(25)이 형성되어 있다.

<91> 상기 반도체 기판(10), 금속배선층(20) 및 하부전극(25)은 상술된 제1 실시예와 동일하므로 이에 대한 설명은 생략하기로 한다.

<92> 상기 층간절연막(21)에 상기 반도체 기판(10)의 씨모스 회로와 연결되는 금속배선(22)을 형성한 후 상기 금속배선층(20) 상부로 포토다이오드를 형성한다.

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<93> 상기 포토다이오드는 금속배선층(220) 상부에 형성되어 외부에서 입사되는 빛을 받아 전기적 형태로 전환 및 보관하기 위한 것으로 실시예에서는 핀 다이오드(PIN diode)를 사용한다. 제2 실시예에서 사용되는 포토다이오드는 제1 실시예와 동일하므로 이에 대한 구체적은 설명은 생략하고 공정순서에 대해서만 설명하도록 한다.

<94> 상기 핀 다이오드를 이용한 포토다이오드를 형성하는 방법에 대하여 설명하면 다음과 같다.

<95> 상기 금속배선층(20) 상에 제1 도전형 전도층(30)을 형성한 후, 상기 제1 도전형 전도층(30) 상부로 적어도 하나 이상의 마스크 패턴(100)을 형성한다.

<96> 상기 마스크 패턴(100)은 상기 제1 도전형 전도층(30)을 요철형태로 형성하기 위한 것으로, 포토레지스트 필름을 도포하고 패터닝하여 형성한다. 상기 마스크 패턴(100)은 상기 제1 도전형 전도층(30) 상에 적어도 하나 이상 형성되어 상기 제1 도전형 전도층(30)의 상부 표면이 단차를 가지도록 형성할 수 있다.

<97> 도 7을 참조하여, 상기 마스크 패턴(100)을 식각마스크로 하여 상기 제1 도전형 전도층(30)을 식각하여 트렌치(32)를 형성한다. 그러면 상기 트렌치(32)에 의해 상기 제1 도전형 전도층(31)의 상부 표면에는 요철형태의 요철부(33)가 형성된다.

<98> 상기 제1 도전형 전도층(31)의 식각은 건식 또는 습식식각 공정으로 진행될 수 있다. 특히, 상기 제1 도전형 전도층(31)의 식각은 상기 제1 도전형 전도층(31) 하부에 위치한 금속배선층(20)이 노출되지 않도록 진행한다.

<99> 도 8을 참조하여, 상기 제1 도전형 전도층(30) 상으로 진성층(intrinsic layer)(40) 및 제2 도전형 전도층(50)을 순차적으로 형성한다.

<100> 그러면, 상기 제1 도전형 전도층(31)의 상부 표면을 따라 형성되는 상기 진성층(40)은 상기 제1 도전형 전도층(31)의 요철부(33)에 의해 상부 표면이 단차를 가지게 되고, 상기 제2 도전형 전도층(50)은 상기 진성층(40)에 의해 상부 표면이 단차를 가지게 된다.

<101> 따라서, 상기 제1 도전형 전도층(31), 진성층(40) 및 제2 도전형 전도층(50)으로 이루어지는 포토다이오드의 표면은 요철형태로 형성되어 표면적 증가로 인하여 광감지율을 향상시킬 수 있게 된다.

<102> 또한, 상기 포토다이오드의 형태가 볼록렌즈와 같은 형태를 가지게 되므로 집광율을 향상시킬 수 있게 된다.

<103> 또한, 상기 포토다이오드는 하나의 픽셀당 적어도 하나 이상의 요철부가 형성되어 포토다이오드의 광감지율을 높일 수 있다.

<104> 도 9를 참조하여, 상기 제2 도전형 전도층(50)의 상부로 상부전극(60)을 형성한다.

<105> 상기 상부전극(60)은 빛의 투과성이 좋고 전도성이 높은 투명전극으로 형성될 수 있다. 예를 들어, 상기 상부전극(60)은 ITO(indium tin oxide) 또는 CTO(cardium tin oxide) 등으로 형성될 수 있다.

<106> 그리고, 상기 상부전극(60) 상으로 접착층(70) 및 컬러필터(80)를 형성한다.

<107> 상기 접착층(70)은 상기 상부전극(60)과 컬러필터(80)의 접착력을 향상시키기 위한 것으로, 상기 상부전극(60) 상으로 열 수지(thermal resin)를 증착하여 형성한 후 평탄화 공정을 진행하여 형성한다.

<108> 그리고, 상기 접착층(70)의 상부로 컬러필터(80)를 형성한다.

<109> <제3 실시예>

<110> 도 13은 제3 실시예에 따른 이미지 센서의 단면도이다.

<111> 도 13을 참조하여 실시예의 이미지 센서는, 씨모스 회로가 형성된 반도체 기판(10); 상기 반도체 기판(10) 상에 형성된 복수의 금속배선(22) 및 층간절연막(21)을 포함하는 금속배선층(20); 상기 금속배선층(20) 상에 형성된 제1 도전형 전도층(30); 상기 제1 도전형 전도층(30) 상에 상부표면에 적어도 하나 이상의 요철부(43)가 형성된 진성층(41); 및 상기 진성층(41) 상에 형성된 제2 도전형 전도층(50)을 포함한다.

<112> 상기 진성층(41)에는 적어도 하나 이상의 트렌치(42)가 형성되어 상기 진성층(41)의 상부표면은 적어도 하나 이상의 요철부(43)가 형성될 수 있다.

<113> 상기 금속배선(22) 상부에는 하부전극(25)이 형성될 수 있다.

<114> 상기 제2 도전형 전도층(50) 상부에는 상부전극(60) 및 컬러필터 어레이(80)가 형성될 수 있다.

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<115> 또한, 상기 상부전극(60)과 컬러필터 어레이(80) 사이에는 접착층(70)이 형성될 수 있다. 예를 들어 상기 접착층(70)은 열 수지(thermal resin)로 형성된다

<116> 도 10 내지 도 13을 참조하여 제2 실시예의 이미지 센서의 제조공정을 설명한다.

<117> 도 10을 참조하여, 반도체 기판(10) 상에는 금속배선층(20) 및 하부전극(25)이 형성되어 있다.

<118> 상기 반도체 기판(10), 금속배선층(20) 및 하부전극(25)은 상술된 제1 실시예와 동일하므로 이에 대한 설명은 생략하기로 한다.

<119> 상기 층간절연막(21)에 상기 반도체 기판(10)의 씨모스 회로와 연결되는 금속배선(22)을 형성한 후 상기 금속배선층(20) 상부로 포토다이오드를 형성한다.

<120> 상기 포토다이오드는 금속배선층(220) 상부에 형성되어 외부에서 입사되는 빛을 받아 전기적 형태로 전환 및 보관하기 위한 것으로 실시예에서는 핀 다이오드(PIN diode)를 사용한다. 제2 실시예에서 사용되는 포토다이오드는 제1 실시예와 동일하므로 이에 대한 구체적은 설명은 생략하고 공정순서에 대해서만 설명하도록 한다.

<121> 상기 핀 다이오드를 이용한 포토다이오드를 형성하는 방법에 대하여 설명하면 다음과 같다.

<122> 상기 금속배선층(20) 상에 제1 도전형 전도층(30) 및 진성층(40)을 순차적으로 형성한다.

<123> 상기 진성층(40) 상으로 상부로 마스크 패턴(100)을 형성한다.

<124> 상기 마스크 패턴(100)은 상기 진성층(40)을 요철형태로 형성하기 위한 것으로, 포토레지스트 필름을 도포하고 패터닝하여 형성한다. 상기 마스크 패턴(100)은 상기 진성층(40) 상에 적어도 하나 이상 형성되어 상기 진성층(41)의 상부 표면이 단차를 가지도록 형성할 수 있다.

<125> 도 11을 참조하여, 상기 마스크 패턴(100)을 식각마스크로 하여 상기 진성층(40)을 식각하여 트렌치(42)를 형성한다. 그러면 상기 트렌치(42)에 의해 상기 진성층(41)의 상부 표면에는 요철형태의 요철부(43)가 형성된다.

<126> 상기 진성층(41)의 식각은 건식 또는 습식식각 공정으로 진행될 수 있다. 특히, 상기 진성층(41)의 식각은 상기 진성층(41) 하부에 위치한 제1 도전형 전도층(30)이 노출되지 않도록 진행한다.

<127> 도 12를 참조하여, 상기 진성층(41) 상으로 제2 도전형 전도층(50)을 형성한다.

<128> 그러면, 상기 진성층(41)의 상부 표면을 따라 형성되는 상기 제2 도전형 전도층(50)은 상기 진성층(41)의 요철부(43)에 의해 상부 표면이 단차를 가지게 된다.

<129> 따라서, 상기 제1 도전형 전도층(30), 진성층(41) 및 제2 도전형 전도층(50)으로 이루어지는 포토다이오드의 표면은 요철형태로 형성되어 표면적 증가로 인하여 광감지율을 향상시킬 수 있게 된다.

<130> 또한, 상기 포토다이오드의 형태가 볼록렌즈와 같은 형태를 가지게 되므로 집광율을 향상시킬 수 있게 된다.

<131> 도 9를 참조하여, 상기 제2 도전형 전도층(50)의 상부로 상부전극(60)을 형성한다.

<132> 상기 상부전극(60)은 빛의 투과성이 좋고 전도성이 높은 투명전극으로 형성될 수 있다. 예를 들어, 상기 상부전극(60)은 ITO(indium tin oxide) 또는 CTO(cardium tin oxide) 등으로 형성될 수 있다.

<133> 그리고, 상기 상부전극(60) 상으로 접착층(70) 및 컬러필터(80)를 형성한다.

<134> 상기 접착층(70)은 상기 상부전극(60)과 컬러필터(80)의 접착력을 향상시키기 위한 것으로, 상기 상부전극(60) 상으로 열 수지(thermal resin)를 증착하여 형성한 후 평탄화 공정을 진행하여 형성한다.

<135> 그리고, 상기 접착층(70)의 상부로 컬러필터(80)를 형성한다.

<136> 이상에서 설명한 실시예는 전술한 실시예 및 도면에 한정되는 것이 아니고, 본 실시예의 기술적 사상을 벗어나지 않는 범위 내에서 여러 가지 치환, 변형 및 변경할 수 있다는 것은 본 실시예가 속하는 기술 분야에서 통상의 지식을 가진자에게 있어 명백할 것이다.

발명의 효과

<137> 실시예에 따른 이미지 센서 및 그의 제조방법에 의하면 트랜지스터 회로와 포토다이오드의 수직형 집적을 제공할 수 있다.

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<138> 또한, 트랜지스터 회로와 포토다이오드의 수직형 집적에 의해 필 팩터(fill factor)를 100%에 근접시킬 수 있다.

<139> 또한, 수직형 집적에 의해 종래기술보다 같은 픽셀 사이즈에서 높은 센서티비티(sensitivity)를 제공할 수 있다.

<140> 또한, 각 단위 픽셀은 센서티비티(sentivity)의 감소없이 보다 복잡한 회로를 구현할 수 있다.

<141> 또한, 수직형 포토다이오드를 채용하면서 단위 픽셀 간의 절연성을 확보함으로써 픽셀간의 크로스토크 등을 방지하여 이미지 센서의 신뢰성을 향상시킬 수 있다.

<142> 또한, 포토다이오드의 단위픽셀을 구현함에 있어 단위 픽셀 내의 포토다이오드의 표면적을 증가시켜 광감지율을 향상시킬 수 있다.

<143> 또한, 상기 단위픽셀에 해당하는 포토다이오드가 볼록렌즈와 같은 렌즈형태를 가지게 되어 집광율을 향상시킬 수 있다.

도면의 간단한 설명

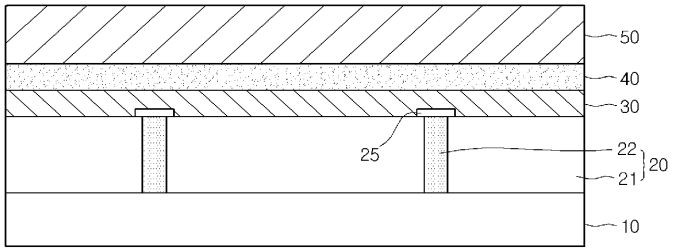
<1> 도 1 내지 도 5a는 제1 실시예의 이미지 센서의 제조 공정을 나타내는 도면이다.

<2> 도 6 내지 도 9는 제2 실시예의 이미지 센서의 제조 공정을 나타내는 도면이다.

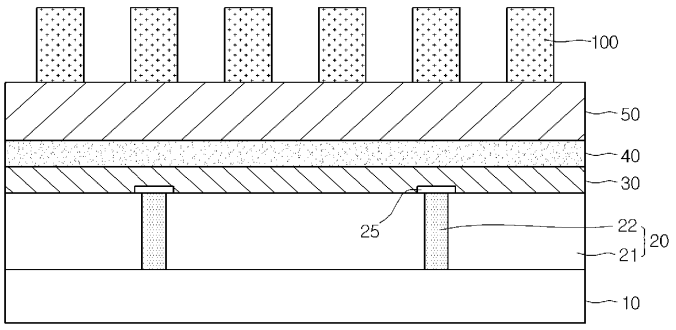
<3> 도 10 내지 도 13은 제3 실시예의 이미지 센서의 제조 공정을 나타내는 도면이다.

도면

도면1

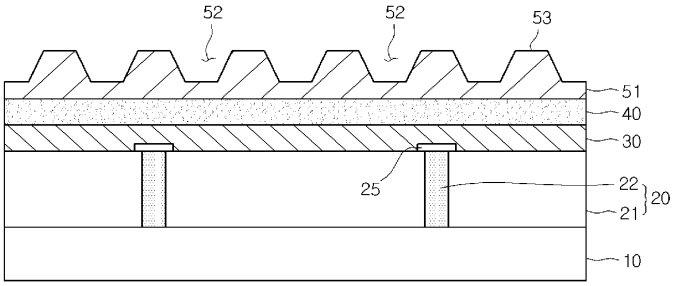


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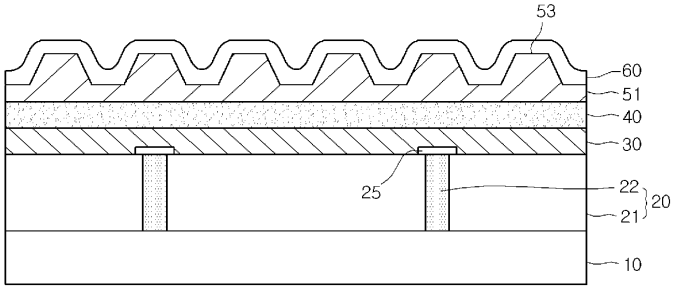


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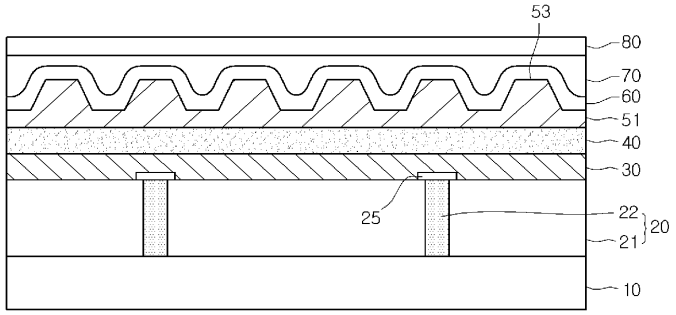
도면3



도면4

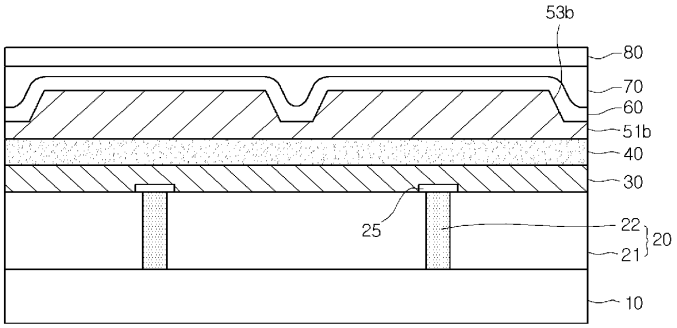


도면5

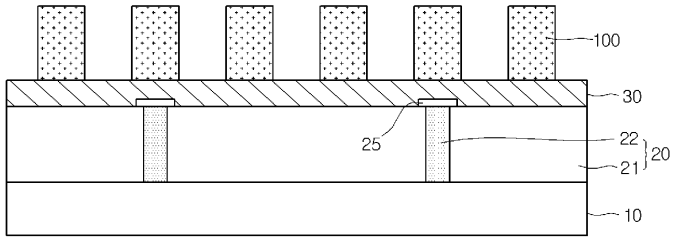


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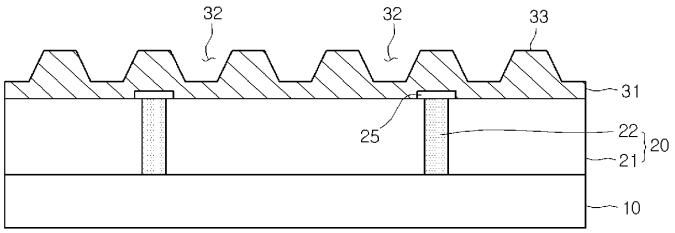
도면5



도면6

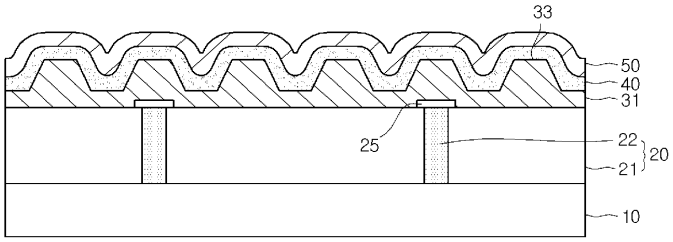


도면7

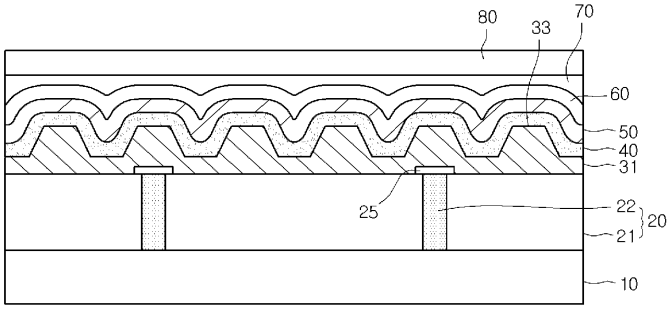


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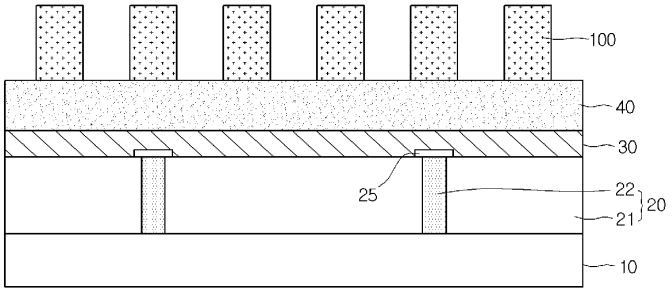
도면8



도면9

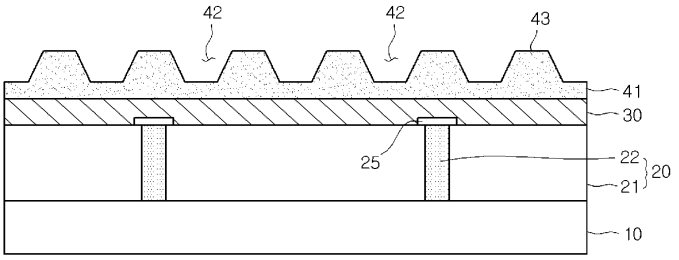


도면10

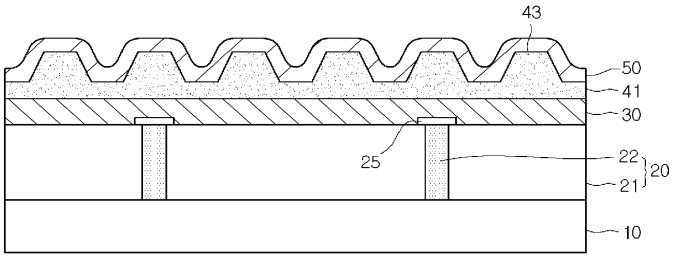


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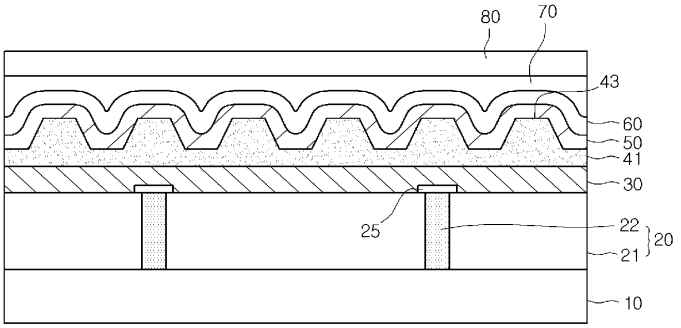
도면11



도면12



도면13



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Attorney Docket No.: 309-0015USCIPDIV **PATENT**
Confirmation No.: TBD

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Shih-Yuan WANG Application No.: TBD Filed: TBD Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	Examiner: N/A Art Unit: N/A
	CERTIFICATE OF TRANSMISSION I hereby certify that this correspondence is being submitted through the USPTO Electronic Filing Service addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 /Mary Ellen Finnegan/ Date: September 3, 2024 Name: Mary Ellen Finnegan

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Alexandria, VA 22313-1450

SIR:

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

It is respectfully requested that the documents listed on the attached Information Disclosure Citation form PTO/SB/08a be considered by the Patent Examiner in connection with the above-identified application and be made of record therein.

A copy of the non-U.S. patent document is enclosed herewith, in compliance with 37 CFR 1.98.

Independent consideration and acknowledgement of the enclosed document are respectfully requested.

The Commissioner is hereby authorized to charge U.S. PTO Deposit Account 600125 any payment due and to credit any overpayment thereto.

Respectfully submitted,

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18/822,880	**09/03/2024 02:21:44 PM Z ET**	**309-0015USCIPDIV**

Title of Invention

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	5818	FILED BY	Mary Ellen Finnegan
PATENT CENTER #	67016011	FILING DATE	-
CUSTOMER #	139982	FIRST NAMED INVENTOR	SHIH-PING Wang
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Ivan Kavrukov

Documents

TOTAL DOCUMENTS: 27

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
309-0015USCIPDIV_ADS--Final.pdf	37	Application Data Sheet	9377 KB
Warning: This is not a USPTO supplied ADS fillable form. Data in the form cannot be automatically loaded to other USPTO systems.			
309-0015USCIPDIV_TransmittalOfPowerOfAttorney-Signed.pdf	2	Power of Attorney	649 KB
309-0015USCIP_Figures_FINAL.pdf	48	Drawings-only black and white line drawings	18638 KB
309-0015USCIP_Declaration_Shih-YuanWANG-signed.pdf	2	Oath or Declaration filed	176 KB

309-0015USCIP_Declaration_ShihPingWANG-signed.pdf	1	Oath or Declaration filed	361 KB
309-0015USCIPDIV_IDSTransmittal-Signed.pdf	1	Transmittal Letter	446 KB
309-0015USCIPDIV_1449.pdf	7	Information Disclosure Statement (IDS) Form (SB08)	1012 KB
KR20080101301A.pdf	26	Foreign Reference	782 KB
JP2002314116.pdf	8	Foreign Reference	3578 KB
WO0103255.pdf	69	Foreign Reference	9889 KB
WO2019018846A3.pdf	3	Foreign Reference	148 KB
EP0940854B1.pdf	26	Foreign Reference	380 KB
JP2007013065.pdf	30	Foreign Reference	10154 KB
CN103956403B.pdf	17	Foreign Reference	4311 KB
ISR_WrittenOpinionPCTUS2150717-12-17-2020.pdf	19	Non Patent Literature	24213 KB
Nanoelectronic_and_Nanophotonic_Interconnect.pdf	18	Non Patent Literature	2566 KB
ISR_WrittenOpinionPCTUS2150717.pdf	10	Non Patent Literature	749 KB
BFLevine_GBSi_HighQuantumEfficiencyMonolithically.pdf	3	Non Patent Literature	1040 KB
YangGAO_PhotonTrappingMicrostructures.pdf	9	Non Patent Literature	2485 KB
DEVINE_SingleMicroholePixelCMOSImageSensors.pdf	7	Non Patent Literature	1222 KB
HAN_DeepTrenchIsolationInvertedPyramidArrayStructuresUsedEnhanceOpticalEfficiencyPhotodiodeCMOS.pdf	14	Non Patent Literature	10939 KB
PARKSamsungPixelTechnologyImprovingQuantum.pdf	4	Non Patent Literature	2089 KB
YOKOGAWA_Sony3NanophotonicsContributionsStateOfTheArtCMOSImageSensors.pdf	4	Non Patent Literature	1408 KB

YOKOGAWA_SonySensitivityEnhancementCMOSImageSensorDiffractiveLightTrappingPixels.pdf	9	Non Patent Literature	2680 KB
309-0015USCIPDIV_PreliminaryAmendment_FINAL.pdf	7	Preliminary Amendment	510 KB
309-0015USCIPDIV_Specification---Final-APP.TEXT.docx	87	Application body structured text document	150 KB

Warning: The document submitted appears to have portions not written in English language. Please review and revise. Bookmarks were found and have been removed.

309-0015USCIPDIV_Specification---Final.pdf	87	Auxiliary PDF of Application	449 KB

Digest

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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

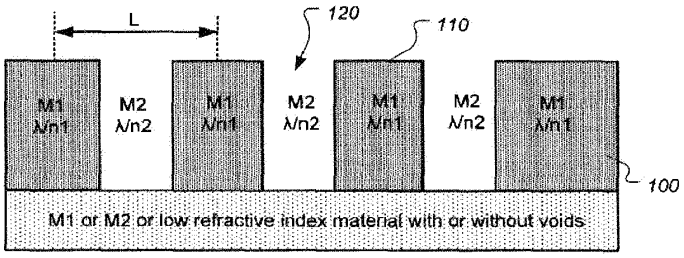


FIG. 1

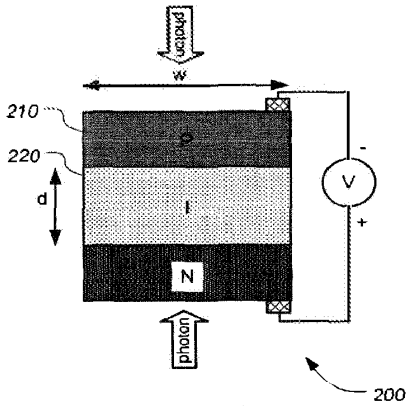


FIG. 2
(prior art)

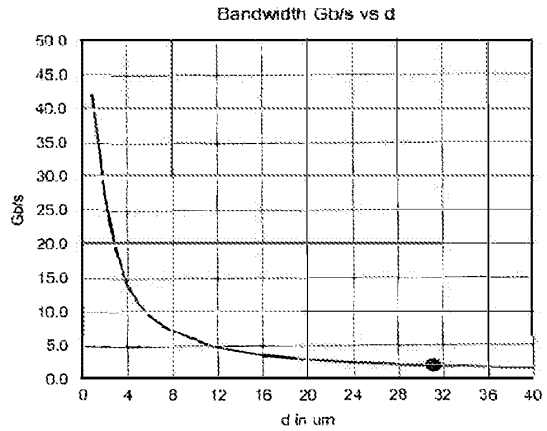


FIG. 3A
(prior art)

310

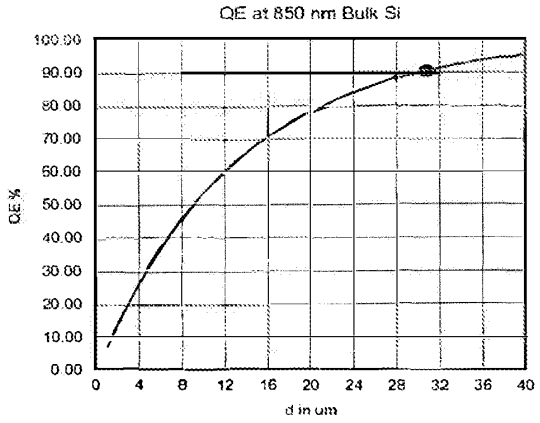


FIG. 3B
(prior art)

312

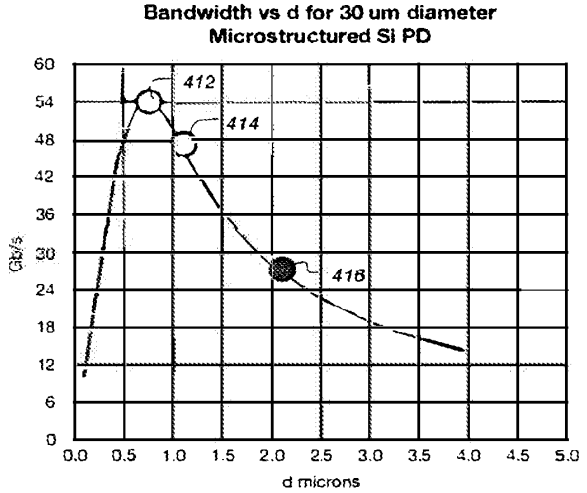


FIG. 4A

410

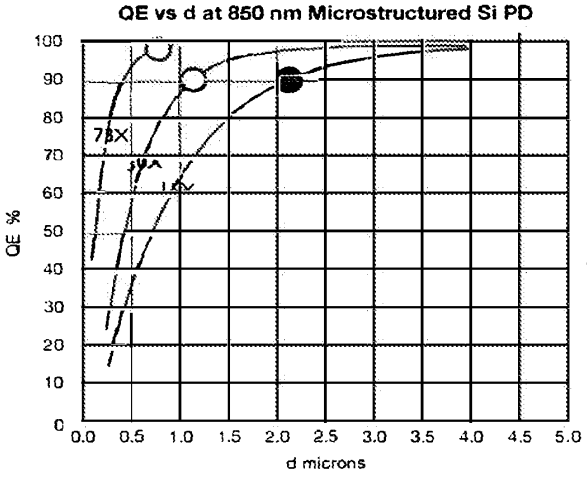


FIG. 4B

420

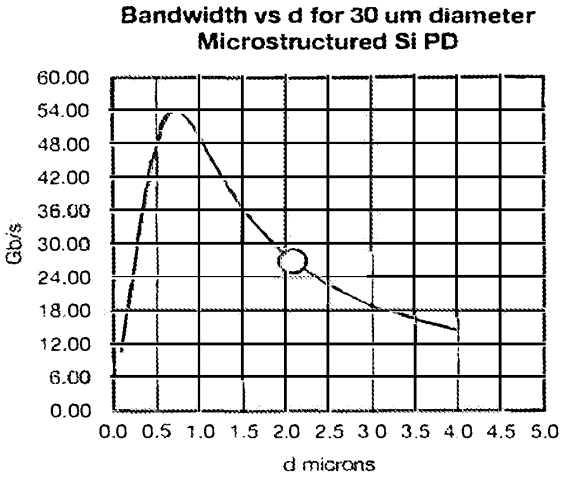


FIG. 4C

430

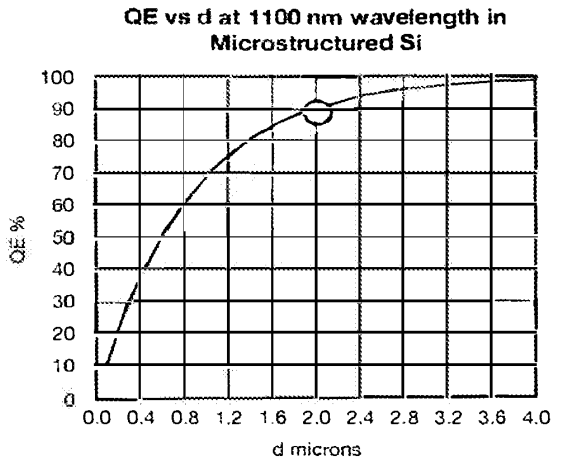


FIG. 4D

440

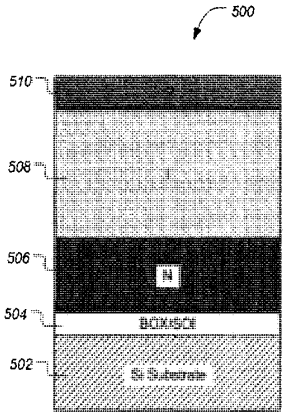

500
510
508
506
504
502
N
BOX/SOI
Si Substrate

FIG. 5A

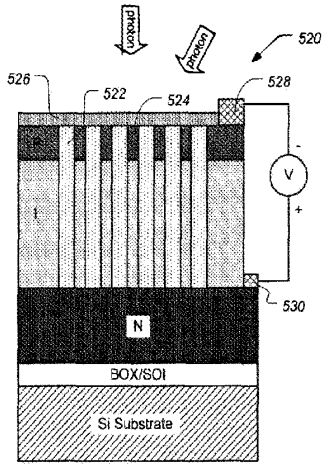

photon
photon
520
526
522
524
528
P
I
N
V
-
+
530
BOX/SOI
Si Substrate

FIG. 5B

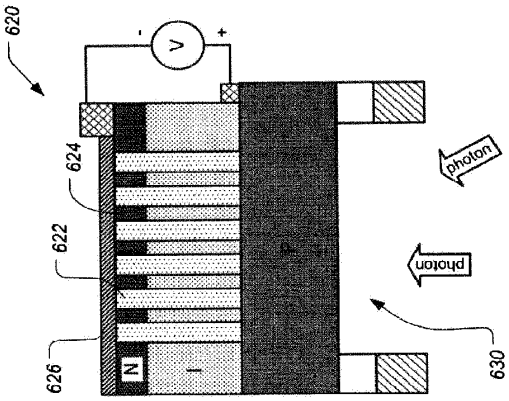

620
-
V
+
624
622
626
N
I
P
photon
photon
630

FIG. 6B

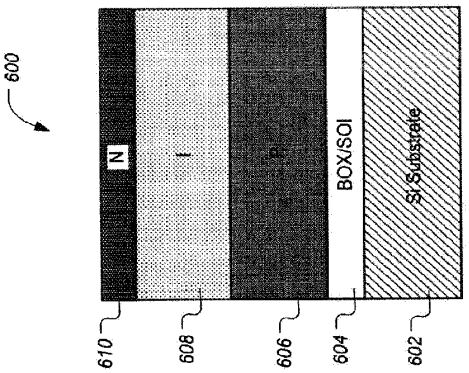

600
N
I
P
BOX/SOI
Si Substrate
610
608
606
604
602

FIG. 6A

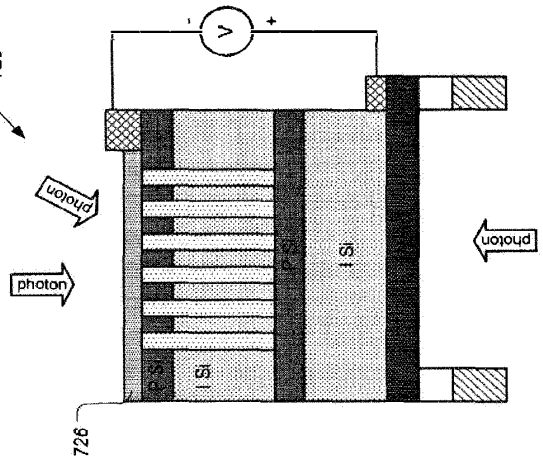

720
V
-
+
photon
photon
photon
726
Si
Si
SiO2
Si

FIG. 7B

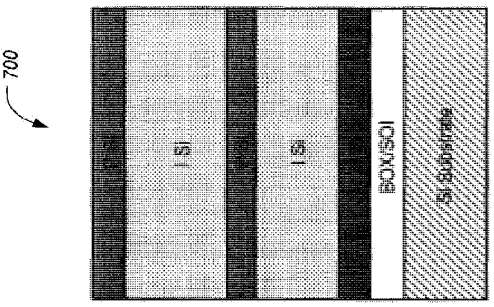

700
Si
Si
BOX/SOI
Si substrate

FIG. 7A

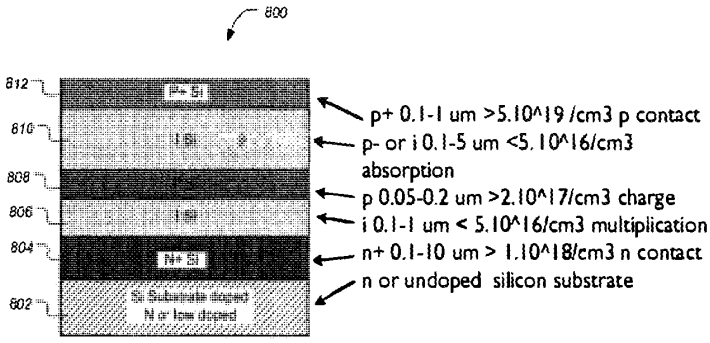


FIG. 8

309-05151/SCIP

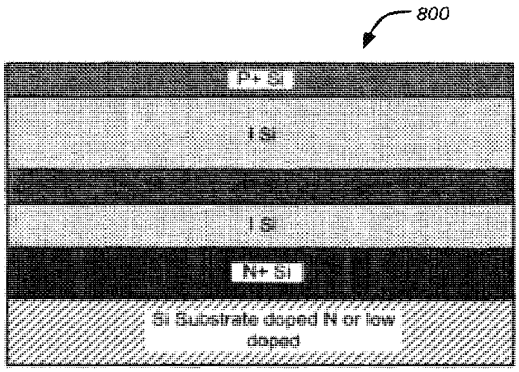

800
P+ Si
I Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9A

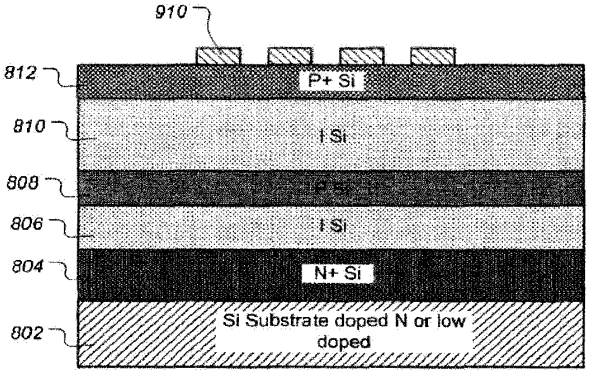

910
812
810
808
806
804
802
P+ Si
I Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9B

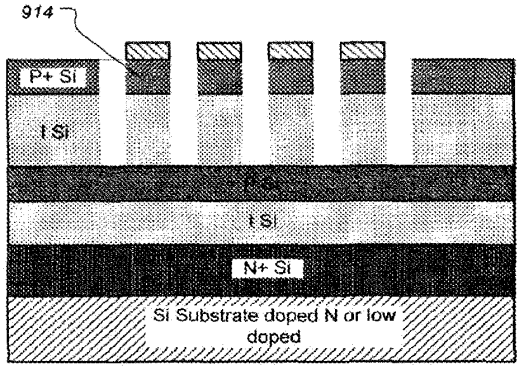

914
P+ Si
I Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9C

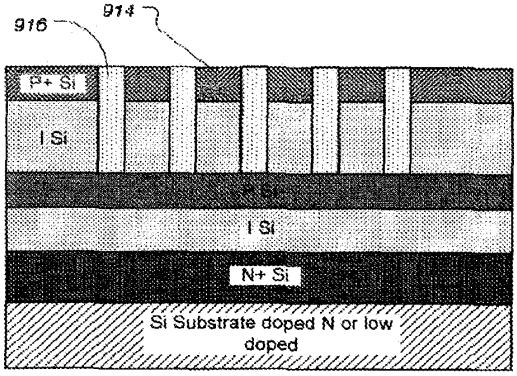

916
914
P+ Si
I Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9D

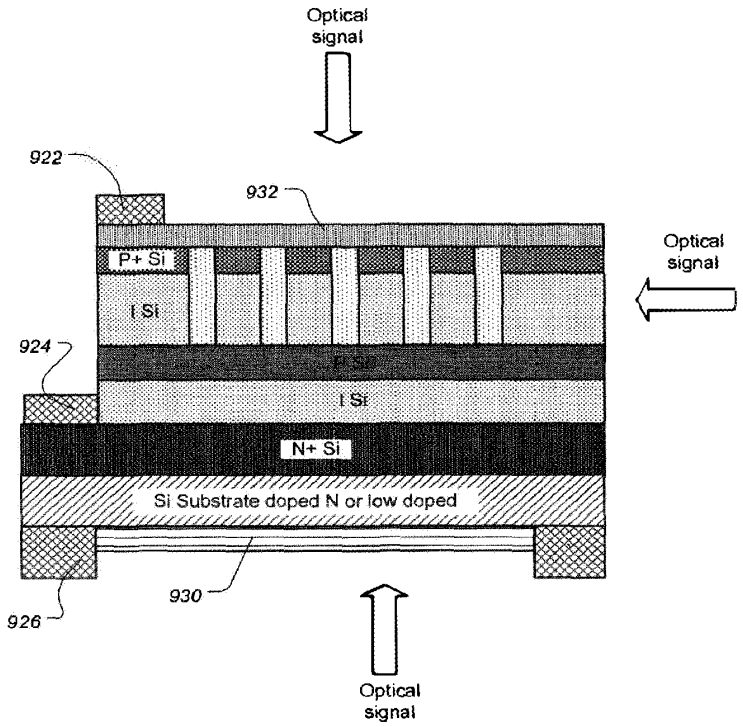

Optical signal
922
932
P+ Si
I Si
Optical signal
924
P+ Si
I Si
N+ Si
Si Substrate doped N or low doped
930
926
Optical signal

FIG. 9E

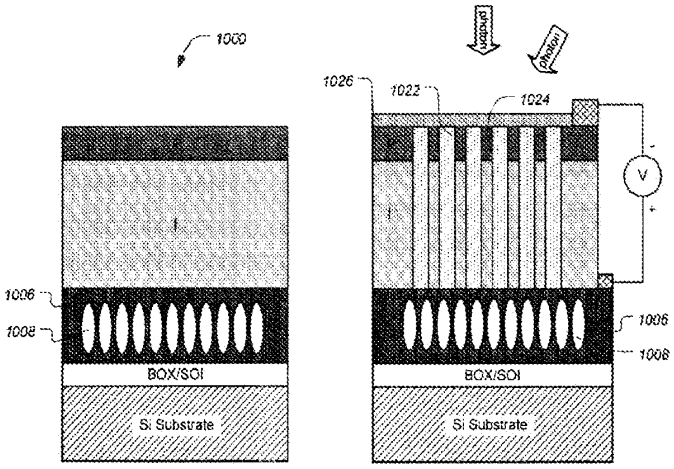


FIG. 10A FIG. 10B

309-0015USCIP

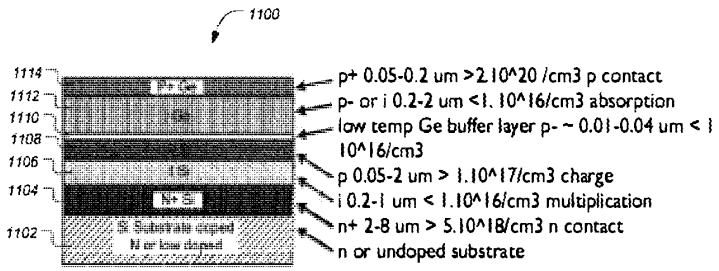

1100
1114
1112
1110
1108
1106
1104
1102
p+ 0.05-0.2 um >2.10^20 /cm3 p contact
p- or i 0.2-2 um <1. 10^16/cm3 absorption
low temp Ge buffer layer p- ~ 0.01-0.04 um < 1 10^16/cm3
p 0.05-2 um > 1.10^17/cm3 charge
i 0.2-1 um < 1.10^16/cm3 multiplication
n+ 2-8 um > 5.10^18/cm3 n contact
n or undoped substrate

FIG. 11A

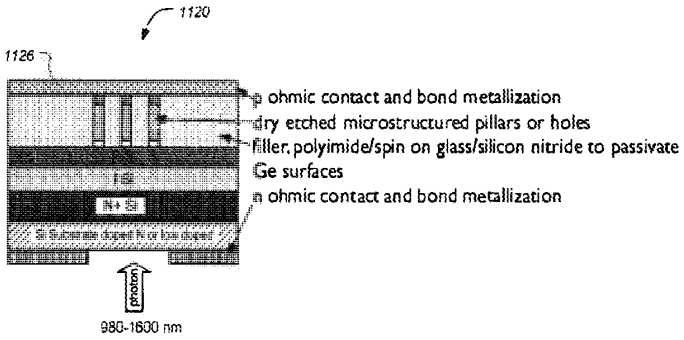

1120
1126
p ohmic contact and bond metallization
dry etched microstructured pillars or holes
filler, polyimide/spin on glass/silicon nitride to passivate
Ge surfaces
n ohmic contact and bond metallization
photon
980-1600 nm

FIG. 11B

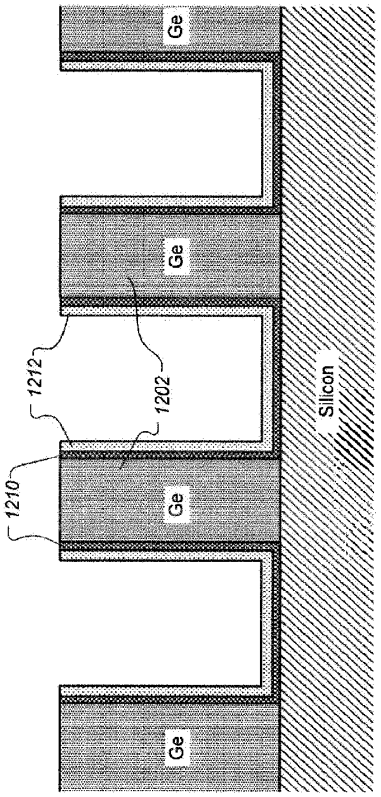


FIG. 12

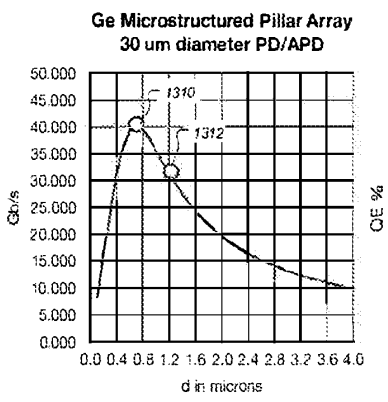


FIG. 13A

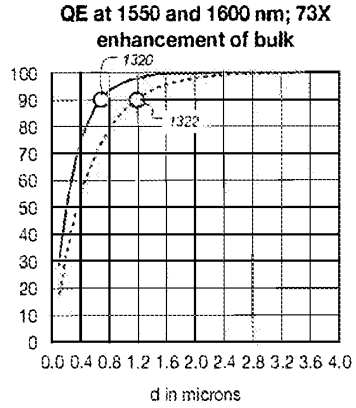


FIG. 13B

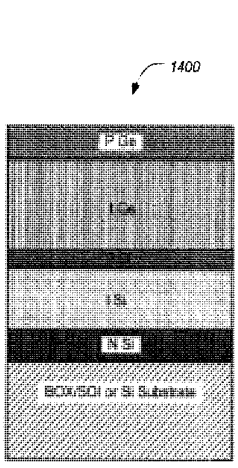


FIG. 14A

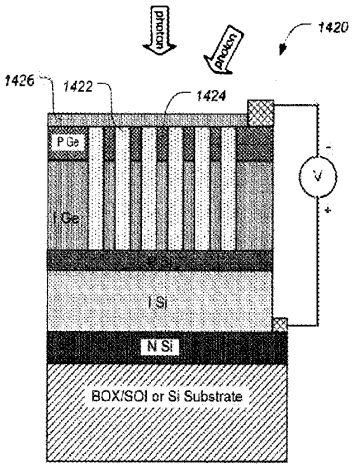


FIG. 14B

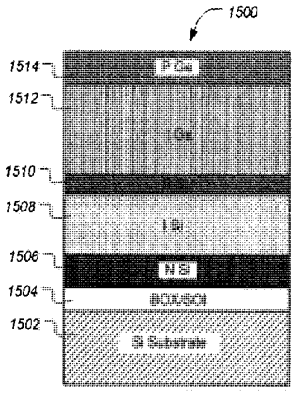


FIG. 15A

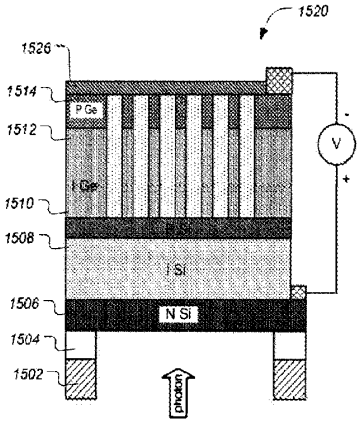


FIG. 15B

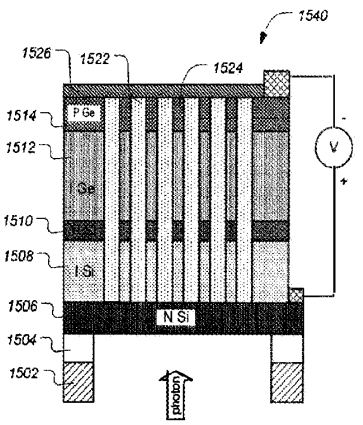


FIG. 15C

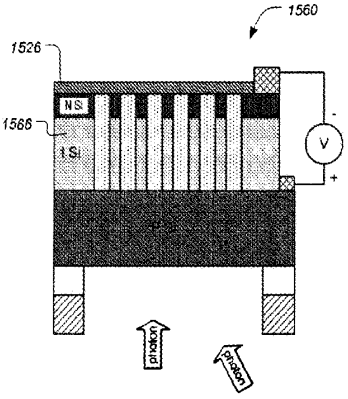


FIG. 15D

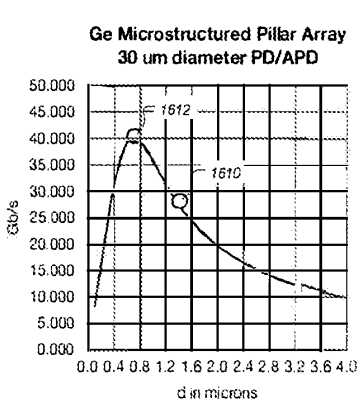


FIG. 16A

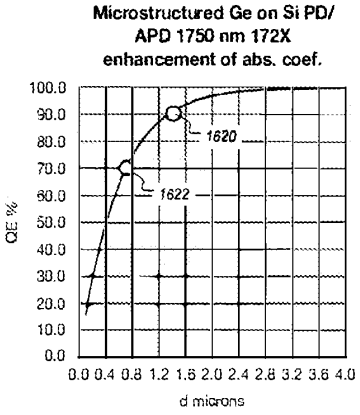


FIG. 16B

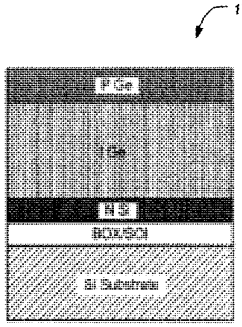


FIG. 17A

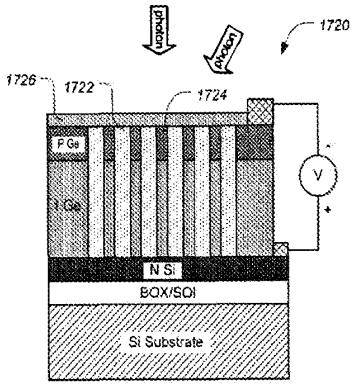


FIG. 17B

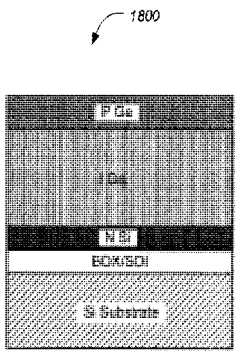


FIG. 18A

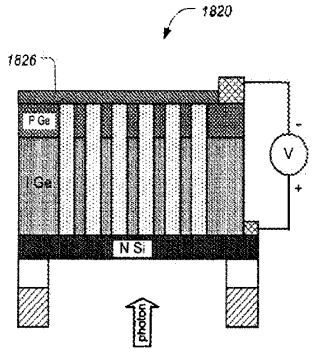


FIG. 18B

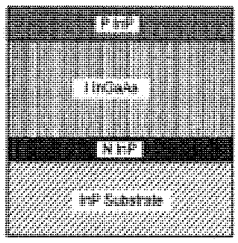


FIG. 19A

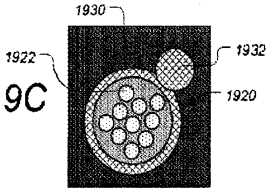


FIG. 19C

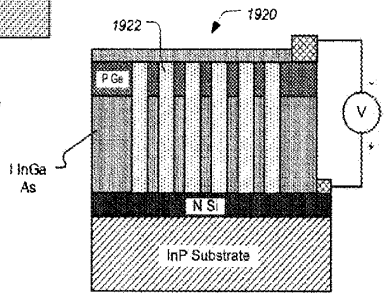


FIG. 19B

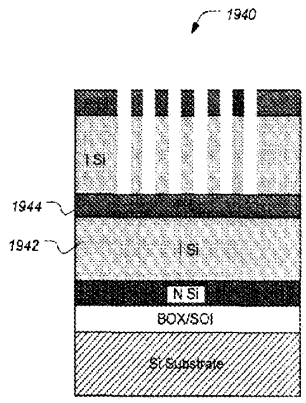


FIG. 19D

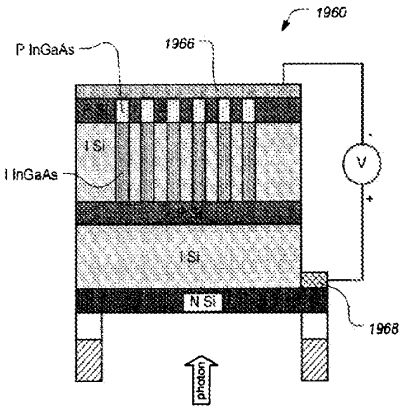


FIG. 19E