

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS
AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG
AUSTIN SEMICONDUCTOR LLC,

Petitioner

v.

W&WSENS DEVICES INC.,

Patent Owner

Case IPR2025-00994
Patent No. 11,621,360

**DECLARATION OF MICHAEL LEBBY, PH.D.,
IN SUPPORT OF PETITION FOR INTER PARTES REVIEW OF
UNITED STATES PATENT NO. 11,621,360**

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i.	[1d]: “one or more deliberately formed in-pillar holes with solid dielectric therein;”	149
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I. INTRODUCTION

1. I, Michael Lebby, Ph.D., have been retained as an independent expert by Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor LLC (“Petitioner” or “Samsung”) in connection with an *inter partes* review (IPR) of U.S. Patent No. 11,621,360 (“the ’360 Patent”) (Ex. 1001). I have prepared this declaration in connection with Samsung’s Petition for *Inter Partes* Review.

2. Specifically, this document contains my opinions about the technology in claims 1, 3, 5, 6, 8, and 9 (“Challenged Claims”) of the ’360 Patent and the grounds against these claims that have been asserted by Samsung. I was not asked to provide any opinions about the ’360 Patent that are not expressed herein.

II. SUMMARY OF OPINIONS

3. This declaration considers claims 1, 3, 5, 6, 8, and 9 of the ’360 Patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for these opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

4. Based on my experience, knowledge of the art at the time of the applicable priority date (I was told to assume a priority date of May 22, 2013), it is

my opinion that claims 1, 3, 5, 6, 8, and 9 of the '360 Patent would have been obvious based on the asserted grounds discussed below.

5. I am being compensated for my time at my normal hourly rate. My compensation is in no way contingent upon the nature of my findings, the presentation of my findings in testimony, or the outcome of this proceeding.

III. QUALIFICATIONS AND BACKGROUND

6. I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below. A copy of my curriculum vitae is attached as Appendix A to this declaration.

7. Based on my education, research, and work experience, I am knowledgeable about the subject matter of the '360 Patent and the related prior art.

8. In what follows, I provide a short summary of my qualifications.

9. I am an engineer with a Ph.D. in Electrical and Electronic Engineering and have worked extensively with optoelectronics, photonics, electrical and electronic circuits, optical systems, as well as integrated circuit semiconductors for both optoelectronic and electronic solutions. Overall, I have approximately 40 years of experience working in industry to develop new electronic, photonic, display, and optics-based products, which I have taken from research to manufacturing.

10. I received a Bachelor of Engineering degree in Electrical and Electronic Engineering in 1984 from the University of Bradford, United Kingdom. I received a Ph.D. in Electrical and Electronic Engineering in 1987 from the University of Bradford, United Kingdom. I also received a second doctorate degree: a Doctor of Engineering degree (D.Eng) in electrical and electronic engineering in 2004 from the University of Bradford, United Kingdom.

11. I am currently Chief Executive Officer (CEO) and Chief Technology Officer (CTO) of GenusTechnik Inc., which is my consulting company, through which I engage in my expert witness work.

12. I recently retired in late 2024 as Chairman and CEO of Lightwave Logic Inc. (NASDAQ: LWLG), where I served as a Director of the Board of Directors since 2015.

13. I am a named inventor on over 225 U.S. utility patents. My work has also led to me either being an inventor or co-inventor in subjects such as: semiconductors, electronics, optics, displays, high frequency optical and electronic products such as lasers and LEDs, as well as photonic integrated circuits. I am the author of more than 60 publications.

14. I am a Fellow grade of three professional organizations: IEEE (Institute of Electrical and Electronic Engineers), NAI (National Academy of Inventors), and Optica (Optical Society of America).

15. As described in this Section, and further detailed in my *curriculum vitae* (Appendix A) over the course of my 40-year career in electronics and optoelectronics, I have worked in nearly every aspect of the electronic, semiconductor, and optoelectronics business, ranging from wafers to components, to modules, displays, optics, connectors and cable technology. At the wafer level, I have experience in epitaxial wafer growth (compound semiconductors). I also have experience in electrical and optoelectronic device and circuit design, using modeling and simulation, electrical and optoelectronic device and component fabrication, testing, and qualification, implementation of devices such as laser diodes, light emitting diodes, photodetectors etc., into packages, connectors, and panels, both hermetic and non-hermetic, as well as analysis of package/panel materials such as plastics (including plastic housings such as resin-packaged lead frame housings), optical plastics, metallic-based packages, semiconductor-based packages, and ceramic-based packages for fiber optics, displays, and data-communications industries. I have also designed device packages (through-pin, surface mount, flip-chip, and various combinations thereof) for printed circuit board mounting as well as electrical and optical components for various industrial and environmental applications. Many of the designed components were implemented into technology applications both as manufactured products as well as components for testing, characterization and analysis of qualified products for

volume scaling. The components were designed to work at both at optical and RF frequencies that include both optical and RF wireless as well as fiber-optics based applications. I have also worked in commercially based industrial research-and-development laboratories to bring new high-performance optoelectronic- and photonic-based technologies from the research proof-of-concept phase through prototyping up to and including qualified manufacturing for volume release. This has included both transfer of as well as the design of optics and optical systems for various commercial systems.

16. I have been both an entrepreneur (*e.g.*, Ignis Optics Inc, One Chip Photonics, Lightwave Logic Inc.), as well as an intrapreneur (*e.g.*, Motorola, Intel, TE Connectivity (previously Tyco Electronics), AT&T Bell Labs), creating innovative new high technology programs, both as venture backed start-ups as well as corporate funded divisions. I have built these entities to develop optical, electronic, optoelectronics, and photonics technology from the laboratory and fabrication clean room to production factories.

17. My career started in the late 1970s at the Ministry of Defense in the United Kingdom where I spent time at a number of their R&D facilities including Malvern (RSRE – Royal Signals and Radar Establishment). There, I worked on electronic and optoelectronic semiconductor device design, as well as basic and high frequency telecommunications and data-communications electronics for

module, cable, connector, and circuit implementation. My research work in electronics then took me to AT&T Bell Laboratories in 1985, where I pursued research in novel electronic and optoelectronic semiconductor material systems that included laser diodes, LEDs, photodetectors, optical waveguides, optics, and standard electronic devices as well as the processing and fabrication for such devices. The devices researched at Bell Labs became in part the subject of my Ph.D. thesis for which I was granted a doctoral degree in 1987.

18. I moved to Motorola in 1989 to further develop my skills in consumer commercial application of technology and focused on optoelectronics, and semiconductor engineering and development. I became a Research and Development Manager in Motorola, until I left the company in 1998. During my time at Motorola, I worked on many photonic, electronic, and optical technology projects that included projection, display, optics, LEDs, OLEDs, laser diodes, phosphors, cameras, as well as the packaging and reliability of mobile product prototypes. At that time, I was particularly interested in miniaturization of electronics, optics, and optoelectronics, and worked on novel optical designs that included portable heads-up displays, optical heads for storage, and various light-based prototypes as well as advanced prototypes of futuristic communications and consumer hardware and cameras.

19. The research work at Motorola also included work on displays and in particular, miniature displays, arrays, imagers, projection systems, and optics for pagers, clam-shell phones, and head-mounted displays that included mounting onto eyeglasses (similar in concept to Google glass™) as well as techniques for electrical and optical connections in these applications.

20. I also initiated Motorola's work in optical interconnect (Optobus™) technology, that incorporated both transfer and injection molded optical parts and included the design of electrical and optical connector technology. This project involved the research and development of a multi-channel electronic IC chip for parallel optical interconnects as well as optical simulations of performance.

21. I was one of Motorola's most prolific inventors, having over 150 issued utility patents as an inventor or a co-inventor by the late 1990s. Many of the photonics and optical prototypes with which I was involved were subject to reliability and stress testing as well as optical measurement analysis. These consumer products all were driven using standard electronic ICs and electronic signaling where I had a role in design and simulation of these circuits.

22. Between 1998 and 1999, I worked as the Director of Technology/ BD (Fiber Optics) for Tyco Electronics (previously AMP). I joined Tyco Electronics as a business development director and director of advanced technology for the telecommunications and data-communications industries. I was responsible for

growing the optical and optoelectronic technology business through external interactions that included mergers, acquisitions, strategic alliances, and technical strategic planning as well as leading new technology projects.

23. In 1999, I left Tyco and started employment at Intel. At Intel, I was involved heavily in photonic technology, especially technology that supported silicon photonic device platforms with different types of displays and optical systems. As a culmination of this work, I was one of Intel's founders of its silicon photonics division in the year 2000, and worked to set up a fabrication facility in South San Jose, California, USA. The work involved integrating silicon FET electronics with optoelectronics and optics onto the same silicon semiconductor wafer. This included CMOS detectors and arrays. I was also part of Intel Capital's optical investment team, and participated in over 30 photonics investment projects into photonics, optics, and optoelectronics. My focus included optical devices, packaging and modules for optical storage, consumer applications such as displays, cameras, projection, communications, and sensing. The technologies that I investigated included lasers, LEDs, optics, LCDs, optical waveguides, cameras, imagers, and optical displays.

24. At the end of 2000, I left Intel and raised venture capital funding for a company called Ignis Optics Inc. The main goal of the company was to design and manufacture, in high volume, very high-performance optoelectronic modules.

These fiber optic transceiver modules have the capability of transmitting and receiving optical signals that are controlled using programmable electronics and packaged optoelectronics chips, such as laser diodes, optical lenses, and photodetectors.

25. In 2005, I took up employment for a trade association, based in Washington, D.C., called IEEE Optoelectronics Industry Development Association (OIDA). As head of this trade association, and with electronics, photonics and optics manufacturers that included manufacturers of projection displays, optical systems, fiber optics, display, cameras, sensing, defense, aerospace, LED lighting, and automotive vendors as members, I was responsible, in part, for industry-based technology roadmaps; and I implemented common industry roadmap methodologies with common features such as “Red Brick Walls” and transferred them into technology roadmaps for the industry in which displays, optics, optical sensors, telecommunications cables, fiber-optic cables, fiber, cameras, and their associated technology platforms, were featured. OIDA roadmaps featured purple brick walls, to show differentiation from the semiconductor industry.

26. In 2010, I became the General Manager and CTO of Translucent, Inc., a high-tech start-up company which developed and manufactured silicon and rare earth oxide based epitaxial semiconductor wafers. I patented a number of

optoelectronic and electronic device designs using rare earth oxides and phosphors while employed at Translucent.

27. Throughout my career, I have also had an active role in a number of technical professional organizations, including, among others, IEEE Components, Packaging, and Manufacturing Technology (CPMT), IEEE Electronic Components and Technology Conferences (ECTC); IEEE TC-10 (Technical Committee on Optoelectronics), and IEEE Optoelectronics Industry Development Association (OIDA). Through these organizations, I have consistently been a part of committees, events, and workshops relating to semiconductor, optoelectronics, electronics, and packaging technology.

28. I also serve as a Technical Expert/Consultant for the European Commission. In my work at the European Commission, I review and advise on general optics, photonics, electronics, telecommunications, semiconductors, optoelectronics, imaging, sensing, cameras, display (*e.g.*, LCD, LED, OLED, etc.), and related Information and Communications Technology (ICT).

29. A full list of my patents and journal publications in addition to my academic and industrial experience is further detailed in my curriculum vitae, which is attached to this declaration as Appendix A.

IV. MATERIALS CONSIDERED

30. In forming my opinions, I have analyzed the materials listed in the Table below. My opinions are based on my experience, knowledge of the relevant art, the documents identified in the Table below, as well as the documents directly cited to in this declaration.

Exhibit	Description
Ex. 1001	U.S. Patent No. 11,621,360 B2 to Wang et al. (“’360 Patent”)
Ex. 1003	Prosecution History of the ’360 Patent (downloaded from Patent Center)
Ex. 1004	U.S. Patent Application Publication No. 2012/0049044 A1 to Kuboi (“ <i>Kuboi</i> ”)
Ex. 1005	U.S. Patent Application Publication No. 2012/0033119 to Shinohara (“ <i>Shinohara</i> ”)
Ex. 1006	European Patent Application EP 2172974 A1 to NXP B.V. (“ <i>NXP</i> ”)
Ex. 1007	U.S. Patent Application Publication No. 2008/0259981 A1 to Wang et al. (“ <i>Wang</i> ”)
Ex. 1010	Zhihong Huang et al., <i>Microstructured silicon photodetector</i> , Applied Physics Letter, Vol. 89 (2006), pp. 033506-1 to -3.
Ex. 1011	Richard A. Myers et al., <i>Enhancing near-infrared avalanche photodiode performance by femtosecond laser microstructuring</i> , Applied Optics, Vol. 45, No. 35 (Dec. 2006), pp. 8825-31.
Ex. 1012	Abbas El Gamal et al., <i>CMOS Image Sensors</i> , IEEE Circuits & Devices Magazine (2005), pp. 6-20.
Ex. 1013	Eric R. Fossum, <i>CMOS Image Sensors: Electronic Camera-On-A-Chip</i> , IEEE Transactions on Electron Devices, Vol. 44, No. 10 (Oct. 1997), pp. 1689-98.
Ex. 1014	Sunetra Mendis et al., <i>CMOS Active Pixel Image Sensor</i> , IEEE Transactions on Electron Devices, Vol. 41, No. 3 (Mar. 1994), pp. 452-53.

Exhibit	Description
Ex. 1015	Renato Turchetta et al., <i>Introduction to CMOS Image Sensors</i> , Molecular Expressions™ Optical Microscopy Primer: Digital Imaging in Optical Microscopy - Introduction to CMOS Image Sensors (July 16, 2004), pp. 1-9, <i>available at</i> https://web.archive.org/web/20120508153832/https://micro.magnet.fsu.edu/primer/digitalimaging/cmosimagesensors.html
Ex. 1020	John P. Uyemura, <i>CMOS Logic Circuit Design</i> (Kluwer Academic Publishers 2002), pp. 64, 74-102, 315-17, 458-60.
Ex. 1021	Khalil Jumah Tawfiq Haram, <i>Organic Solar Cells Based on High Dielectric Constant Materials: An Approach to Increase Efficiency</i> (June 2013) (Ph.D. dissertation, Western Michigan University), pp. 1-122.
Ex. 1022	P. Kalugasalam et al., <i>Dielectric and AC Conduction Studies of Lead Phthalocyanine Thin Film</i> , Chalcogenide Letters, Vol. 6, No. 9 (Sept. 2009), pp. 469-76.
Ex. 1028	Leonard Rubin et al., <i>Ion Implantation in Silicon Technology</i> , Industrial Physicist, 9(3), (Jun/July 2003), pp. 12-15.
Ex. 1029	Jurgen Michel et al., <i>Advances in fully CMOS integrated photonic devices</i> , Proceedings of SPIE, Vol. 6477 (2007), pp. 64770P-1 to -11 ("Michel").
Ex. 1030	Mark Beals et al., <i>Process Flow Innovations for Photonic Device Integration in CMOS</i> , Proceedings of SPIE, Vol. 6898 (2008), pp. 689804-1 to -14 ("Beals").
Ex. 1034	Matthew Saucedo, <i>Porphyrin Thin Film Dielectrics</i> , SUNFEST Technical Report TR-CST01NOV04, Center for Sensor Technologies, Univ. of Pennsylvania, Philadelphia, PA (2004), pp. 181-98.
Ex. 1035	N. Venkatramaiah et al., <i>Spectroscopic and dielectric studies of meso-tetrakis(p-sulfonatophenyl) porphyrin doped hybrid borate glasses</i> , Journal of Alloys and Compounds, Vol. 509 (2011), pp. 2797-803.
Ex. 1036	Tom J. Savenije, <i>Photogeneration and transport of charge carriers in a porphyrin p/n heterojunction</i> , Physical Review B, Vol. 55, No. 15 (Apr. 1997), pp. 9685-92.

Exhibit	Description
Ex. 1037	Ümit Salan et al., <i>Synthesis, characterization, electrical and dielectric permittivity measurements of 2,9,16,23-tetra(4-ferrocenylimino-3-nitrophenoxy)phthalocyanines</i> , Journal of Porphyrins and Phthalocyanines, Vol. 10 (2006), pp. 1263-70.
Ex. 1038	Teresa M. Figueira-Duarte et al., <i>Pyrene-Based Materials for Organic Electronics</i> , Chemical Reviews, Vol. 111 (2011), pp. 7260-314.
Ex. 1050	U.S. Patent Application Publication No. 2012/0153124 A1 to Yu et al. (“Yu”)
Ex. 1051	International Patent Publication No. WO 2011/085297 A1 to Han et al. (“Han”)
Ex. 1052	Japanese Patent Publication No. JP 2007-129024A
Ex. 1053	Certified English Language Translation of Japanese Patent Publication No. JP 2007-129024A to Hasegawa (“Hasegawa”)
Ex. 1055	U.S. Patent No. 7,646,943 B1 to Wober (“’943 Patent”)
Ex. 1056	U. S. Patent No. 8,274,122 B2 to Shimotsusa
Ex. 1057	U. S. Patent No. 8,378,339 B2 to Nomura et al.
Ex. 1058	Richard Rhoad et al., <i>Geometry for Enjoyment and Challenge</i> (Houghton Mifflin 1997), pp. 234-238.
Ex. 1059	U.S. Patent Application Publication No. 2008/0157141 A1 to Han
Ex. 1060	U. S. Patent No. 8,390,036 B2 to Goto
Ex. 1061	H. H. Li, <i>Refractive Index of Silicon and Germanium and Its Wavelength and Temperature Derivatives</i> , J. Phys. Chem. Ref. Data, Vol. 9, No. 3 (1980), pp. 561-658.
Ex. 1062	Rei Kitamura et al., <i>Optical constants of silica glass from extreme ultraviolet to far infrared at near room temperature</i> , Applied Optics, Vol. 46, No. 33 (November 20, 2007), pp. 8118-33.
Ex. 1063	S.M. Sze et al., <i>Semiconductor Devices Physics and Technology</i> (John Wiley & Sons, Inc. 3d ed. 2012), pp. 6-9, 205-10, 325-30, 392-406, 416-17, 466-67.
Ex. 1067	<i>Electrical Engineering Dictionary</i> - CRCnetBase (Phillip A. Laplante editor-in-chief, CRCPress LLC 2000), pp. 1-10.

Exhibit	Description
Ex. 1068	P.A. Lane et al., <i>Electroabsorption studies of phthalocynine/perylene solar cells</i> , Solar Energy Materials & Solar Cells, Vol. 63, (2000), pp. 3-13.
Ex. 1069	Martin A. Green, <i>Self-consistent optical parameters of intrinsic silicon at 300K including temperature coefficients</i> , Solar Energy Materials & Solar Cells, Vol. 92, (2008), pp. 1305-10.
Ex. 1070	Horst Zimmerman, <i>Integrated Silicon Optoelectronics</i> (Springer. 2d ed. 2010), pp. 1-7.
Ex. 1071	M.M. El-Nahas et al., <i>Structural and optical properties of Ni (II) tetraphenyl porphyrin thin films</i> , Eur. Phys. J. Appl. Phys. (2012), Vol. 57, pp. 30201-p1 to 30201-p13.
Ex. 1072	M.M. El-Nahas et al., <i>Structural and optical properties of thermally evaporated zinc phthalocyanine thin films</i> , Proc. 2 nd Saudi Sci. Conf. (March 2004), pp. 277-293.
Ex. 1073	M.E. Azim-Araghi et al., <i>Electrical and optical properties of an organic semiconductor metal-free phthalocyanine (C₃₂H₁₈N₈)</i> , Eur. Phys. J. Appl. Phys. (2012), Vol. 58, pp. 30201-p1 to 30201-p6.
Ex. 1074	<i>W&Wsens Devices Inc. v. Samsung Electronics Co. Ltd. et al.</i> , Case No. 2:24-cv-00854, Excerpts from Plaintiff's Infringement Contentions (Jan. 7, 2025)

V. LEGAL STANDARDS

31. I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Petitioner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

32. I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art can “anticipate” a claim. Second, I have been informed that the prior art can render a claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated and would not have been obvious by the prior art at the effective filing date of the patent.

33. I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

34. I have been asked to provide my opinions as to whether the cited prior art teaches or renders obvious claims 1, 3, 5, 6, 8, and 9 of the '360 Patent from the perspective of a person of ordinary skill in the art at the '360 Patent's earliest claimed priority date (May 22, 2013), as described in more detail below.

35. I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means “more likely than not.”

36. For purposes of this declaration, I have been asked to provide my opinions on issues regarding unpatentability. I have been informed of the following legal standards, which I have applied in forming my opinions.

A. Level of Ordinary Skill

37. I have been informed a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

38. I have been instructed to assume a person of ordinary skill in the art is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Prior Art

39. I have been advised and understand the information used to evaluate whether an invention was new and not obvious when made is generally referred to as “prior art.” I understand that prior art includes patents and printed publications that existed before the earliest claimed priority date or the earliest filing date of the patent (which I have been informed is also called the “effective filing date”). I have been informed and understand that a patent or published patent application is prior art if it was filed before the earliest filing date of the claimed invention and that a printed publication is prior art if it was publicly available before the earliest filing date.

C. Anticipation

40. I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if it is not novel, including if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

D. Obviousness

41. I have been informed that under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

42. I have been informed that a proper obviousness analysis includes the following:

- a. Determining the scope and content of the prior art;
- b. Ascertaining the differences between the prior art and the claims at issue;

- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of non-obviousness (if available). I am not aware of any evidence of secondary considerations that would support a determination of non-obviousness of the claimed subject matter in the '360 Patent.

43. I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Petitioner instructed me to assume that the date of invention for the Challenged Claims is May 22, 2013. My opinions would not change if I assumed a later date of invention.

44. I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

45. I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that

the prior art contain an express suggestion to combine known elements to achieve the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

46. In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;

- d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—but not “absolute predictability” of success—in achieving the claimed invention by combining prior art references.

47. I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation is likely to have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or

market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

48. I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

49. I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to

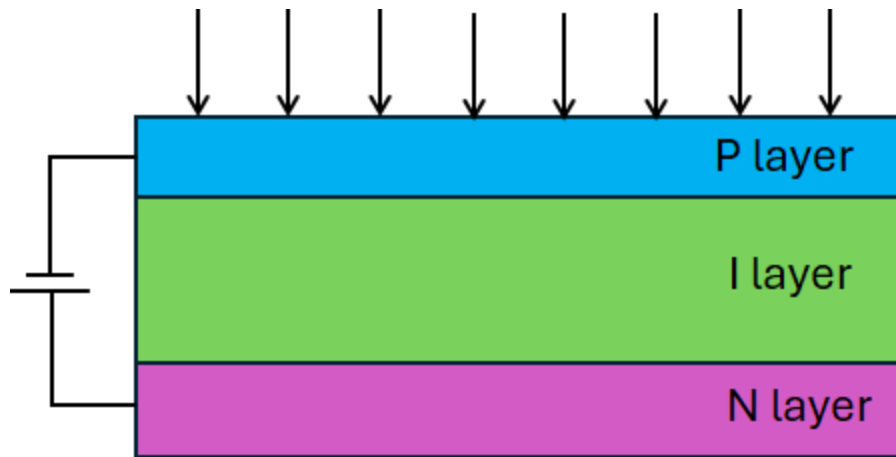
combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

50. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

VI. TECHNOLOGY BACKGROUND

A. Photodetectors

51. A photodetector is a semiconductor device that transforms photons into electrical signals, enabling electrical circuits to detect and measure incident light. Various types of photodetectors exist, including photodiodes and avalanche photodiodes. A PiN photodetector is a specific type of photodiode characterized by an **intrinsic (undoped) layer** positioned between highly doped **P-type** and **N-type** semiconductor layers (hence the name “**PiN**”):



52. When light enters the photodetector, the intrinsic layer absorbs photons, generating electron-hole pairs. Applying a negative bias across the photodetector causes the separated electrons to move towards the N-type layer and the holes towards the P-type layer, producing a measurable photocurrent.

B. Microstructure-Enhanced Photodetectors

53. Conventional silicon photodetectors exhibit high responsivity at wavelengths of light less than about 850 nm. Ex. 1010, 1. The prior art recognized that tailoring silicon's microstructure extends photodetector operability to longer wavelengths. For instance, etching a silicon photodetector surface to create micron-sized pillars was known to enhance a photodetector's responsiveness at longer wavelengths. Ex. 1010, 1-2; Ex. 1011, 1-6. The images below illustrate photodiodes with laser-etched microstructures designed to enhance their responsiveness at longer wavelengths.

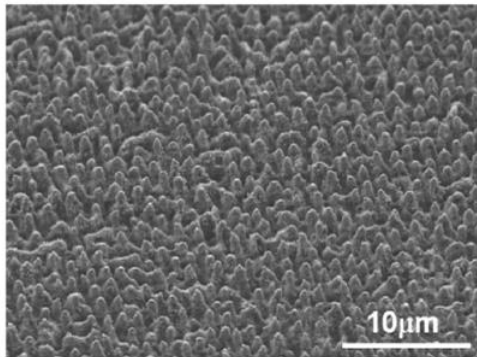


FIG. 1. Scanning electron micrographs of microstructured Si surface.

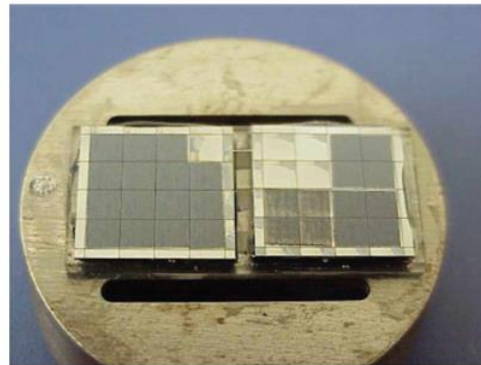


Fig. 1. (Color online) Picture of two microstructured APD arrays prior to packaging. Structuring was performed with an 800 nm fs laser operating at a fluence of 3.5 kJ/m^2 in an atmosphere of SF_6 . The array on the right had four different structured regions with a pulse number ranging from 0 to 300. The shiny area is the bare silicon.

Ex. 1010, 1 (left); Ex. 1011, 2 (right)

54. Photodetectors featuring microstructures enhanced by etched holes were widely known and utilized well before the purported invention. For example, *NXP* (Ex. 1006) discloses a single-chip device 1300 where a silicon **PiN** photodiode is integrated with CMOS signal processing circuitry (not shown in Figure 13 below) on the same **substrate 102**. *NXP*, ¶¶[15], [32], [42], [85].

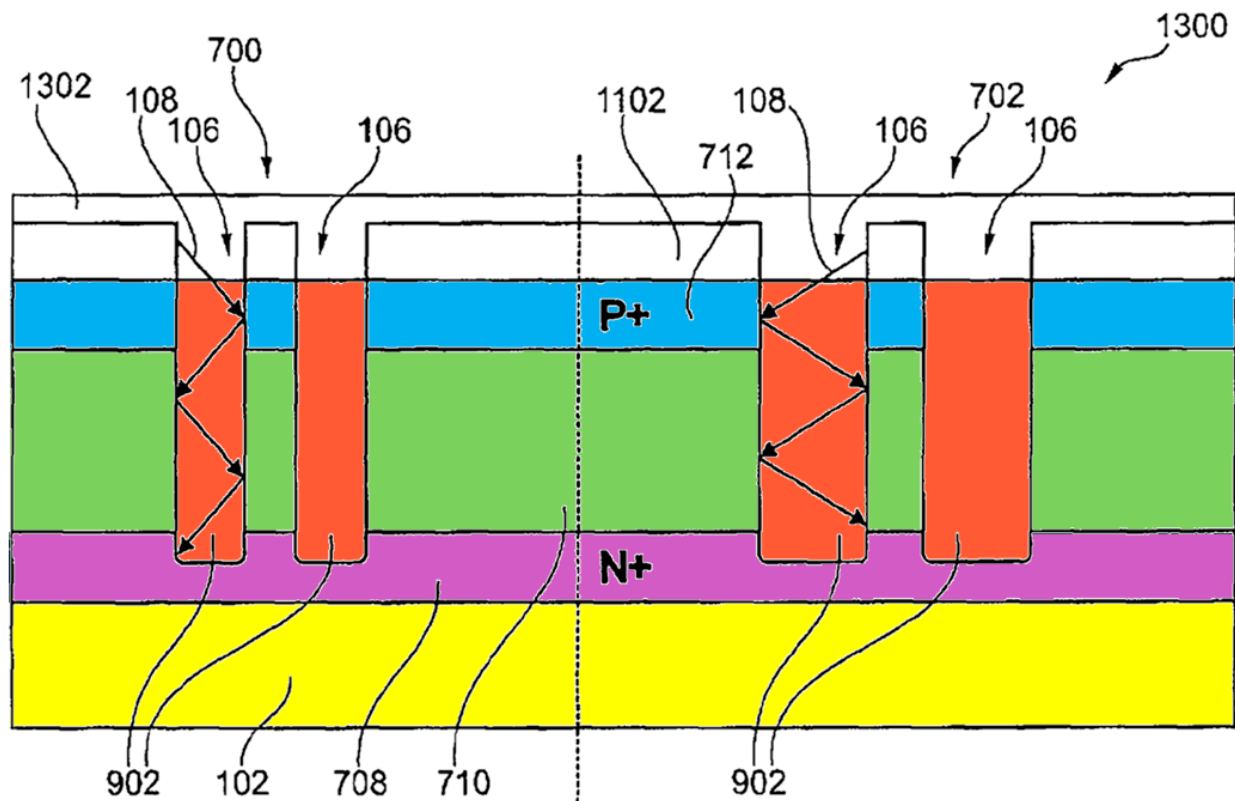


Fig. 13

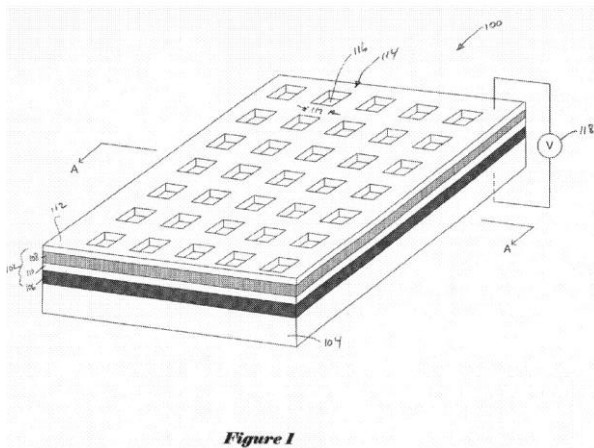
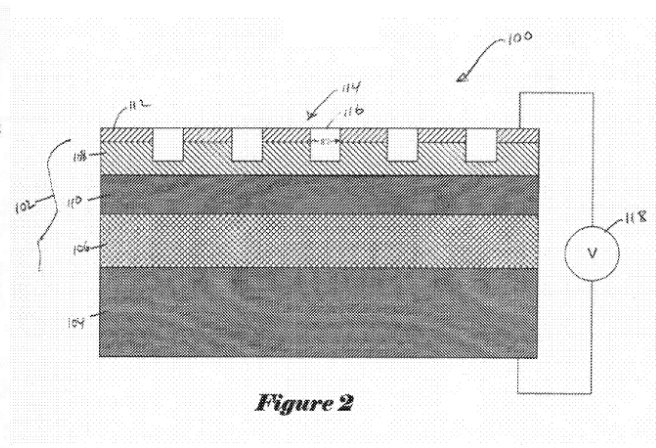
NXP, Fig. 13.¹

55. The **PiN** photodiode above includes an **intrinsic layer** 710 disposed between an **N⁺ layer** 708 and a **P⁺ layer** 712 and holes or **pores** 106 formed on the **PiN** layers by etching. *NXP*, ¶¶[77]-[78]. *NXP* discloses that **pores** 106 increase the photodiode's quantum efficiency. *NXP*, ¶¶[13], [38]. Quantum efficiency is a

¹ I have added color and colored annotations in figures throughout my declaration to illustrate claimed features disclosed in the '360 Patent as well as in the prior art references.

measure of how effectively the photodiode converts incoming optical energy into electrical signals. *See* Ex. 1012, 4; Ex. 1013, 4.

56. As another example, *Wang* (Ex. 1007) discloses a photonic device 100 comprising a PiN structure with a stacked p-semiconductor region 108, intrinsic semiconductor region 110, and an n-semiconductor region 106. *See Wang*, ¶[28], Figs. 1-2. A thin doped region 112 overlays the surface of the p-region 108, and a periodic array of holes or recesses 116 extends into the PiN structure through the overlying region 112. *Wang*, ¶¶[29]-[32].



Wang, Figs. 1, 2.

C. Photodetectors and Processing Circuitry on a Single Substrate

57. The integration of photodetectors and signal processing circuitry on a single substrate to form a single-chip device was known long before the purported invention date of the '360 Patent. Ex. 1012, 1-14; Ex. 1013, 1-8; Ex. 1014, 1-2. For instance, *NXP* teaches that integrating signal processing circuitry and the

photodiode on the same substrate “may be more reliable than a discrete solution” and result in a smaller package, which is advantageous for mobile applications. *NXP*, ¶¶[16], [32], [37].

58. Beginning in the late 1980s, advancements in CMOS technology enabled the fabrication of both photodetectors and signal processing electronics on the same substrate. Ex. 1012, 2-3, 10. For example, researchers at NASA’s Jet Propulsion Laboratory developed the CMOS active pixel sensor (“APS”), which integrated a photodiode, amplifier, and signal processing circuitry within each pixel of an image sensor. Ex. 1012, 2-3. This allowed for on-chip conversion of light to electrical signals and immediate processing. Ex. 1012, 2-3; Ex. 1013, 4. This CMOS APS is shown below:

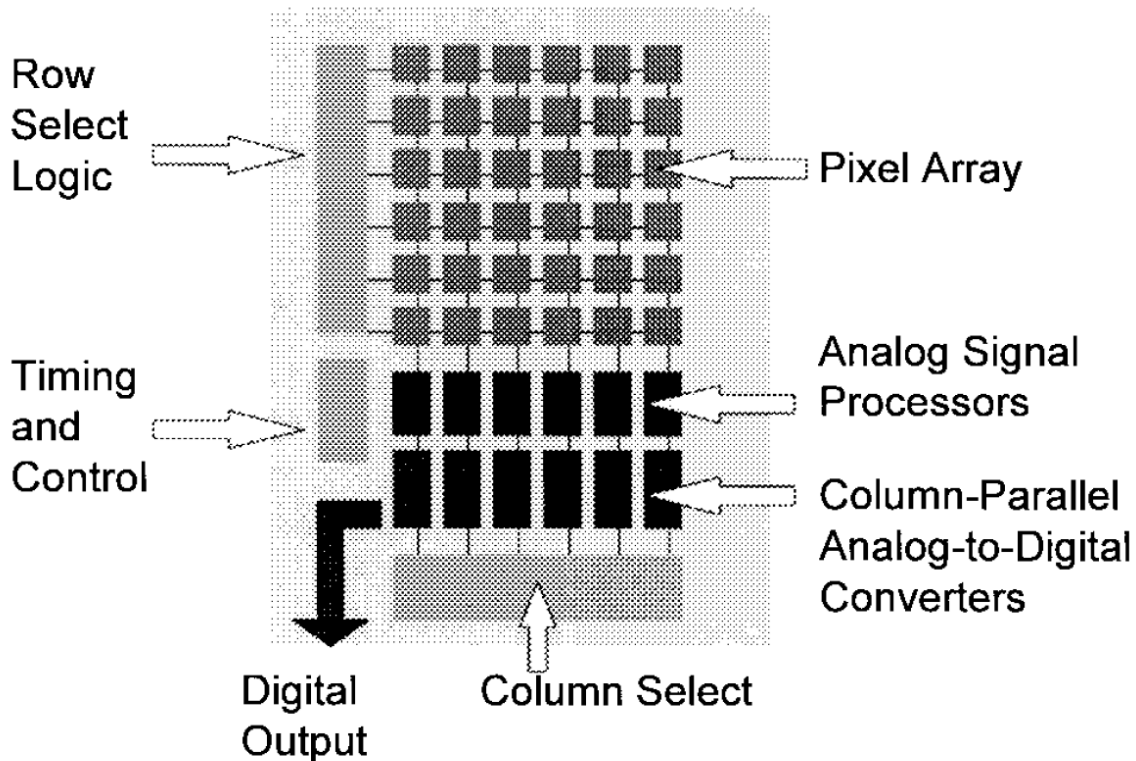
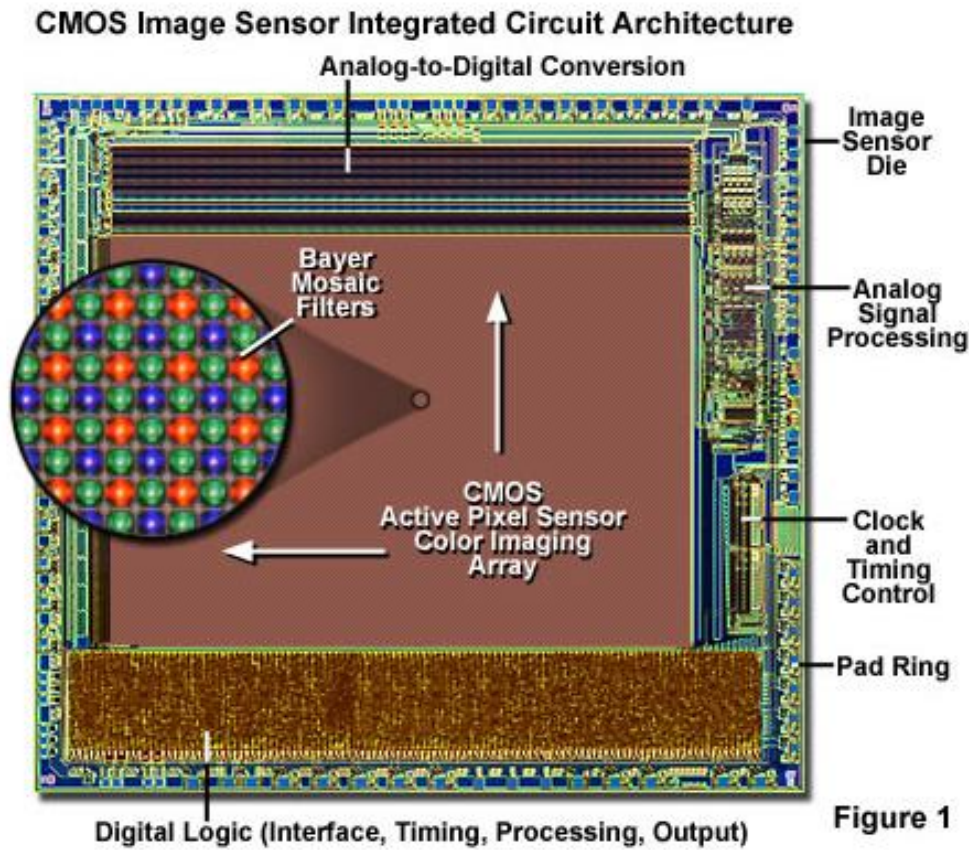


Fig. 2. CMOS APS integrates timing and control, ADC, and other circuitry on the same chip.

Ex. 1013, 3.

59. The integration of the photodiode and processing circuitry on the same chip reduced power consumption, lowered manufacturing costs, and allowed for smaller, more efficient imaging devices. Ex. 1012, 3, 10, 12; Ex. 1013, 8.

60. By the early 2000s, APS technology was prevalent in consumer electronics such as digital cameras, smartphones, and webcams. Ex. 1012, 1-3; Ex. 1015, 9. An image of a CMOS APS image sensor die is shown below.

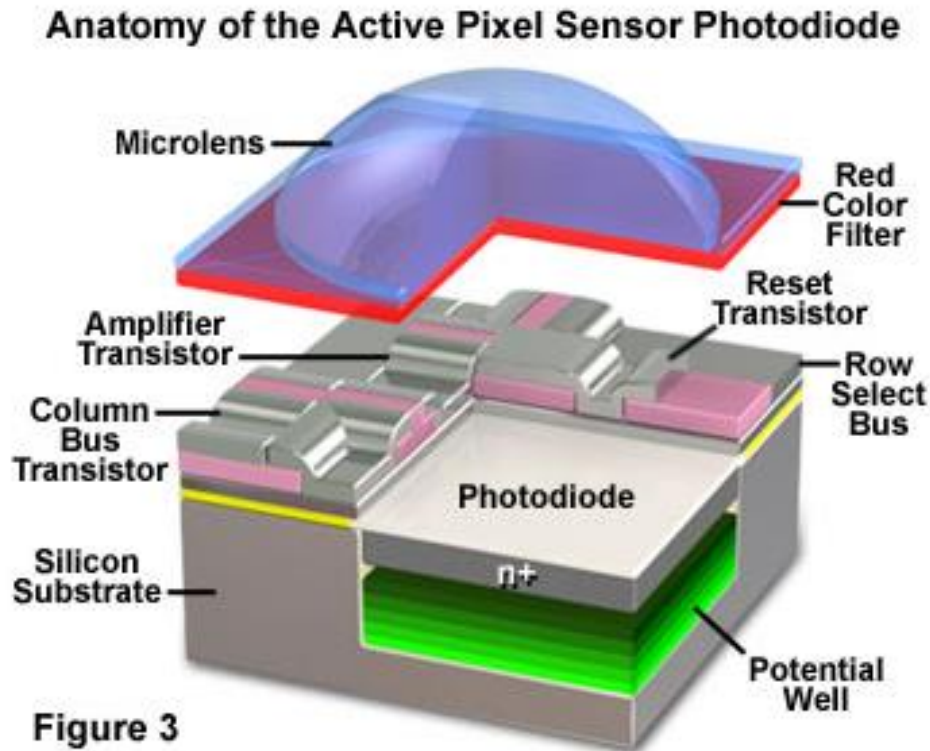


Ex. 1015, 1.

61. This image sensor die includes an array of photodiodes (640 x 480 pixels) located in the large reddish-brown central area of the chip and analog signal processing circuitry to collect and interpret the signals generated by the photodiode array. Ex. 1015, 2-3, Fig. 1.

62. A three-dimensional cutaway drawing of the above image sensor is shown below, illustrating a single photodiode and associated transistors that process the signals produced by the photodiode on a single substrate.

Ex. 1015, 3-5.



Ex. 1015, 3.

63. To focus the incident light on the photodiode, the photodiode is positioned beneath a microlens and a color filter to capture color information from the incident light. Ex. 1015, 3-4, Fig. 3.

64. Well before the purported invention date of the '360 Patent, numerous published references disclosed single-chip devices integrating photodetectors and signal processing circuitry on a single substrate. For example, *Kuboi* (Ex. 1004), discussed below, describes such a device. *Infra* VIII.A. *Shinohara* (Ex. 1005) discloses a similar single-chip device incorporating photodetectors and signal processing circuitry. See *Shinohara*, Figs. 1-2, ¶¶[51]-[63]; *infra* VIII.B.

FIG. 1

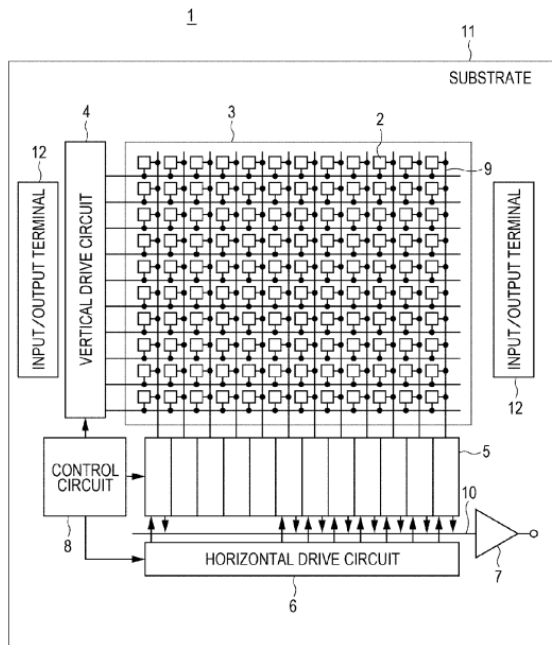
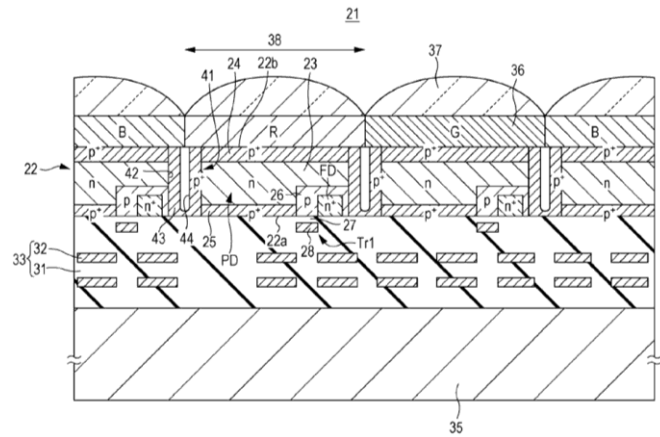


FIG. 2



Shinohara, Figs. 1, 2.

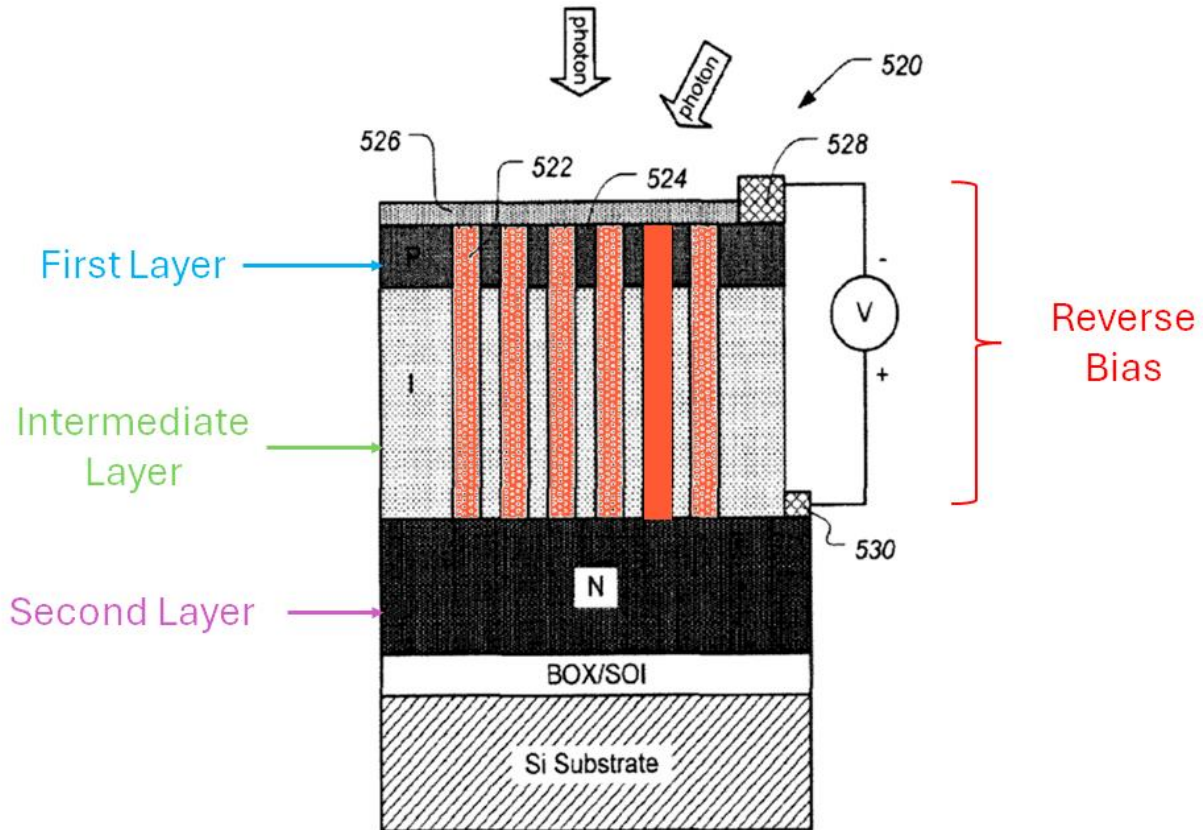
65. Like Kuboi's imaging device 201 (see Kuboi, Fig. 5, ¶¶[48]-[54]), Shinohara's imaging device 1 features a pixel region 3 with a two-dimensional pixel array 2 and a peripheral circuit portion integrated on the same semiconductor substrate 11. See Shinohara, ¶[51]; see *infra* VIII.A. In Shinohara, each pixel 2 contains a photoelectric conversion portion and four pixel transistors, similar to Kuboi. Shinohara, ¶[51]; see Kuboi, ¶[48]; see *infra* VIII.A. Additionally, akin to Kuboi, Shinohara's peripheral circuit portion includes various logic circuits, such as a vertical drive circuit 4, a column signal processing circuit 5, a horizontal drive circuit 6, an output circuit 7, and a control circuit 8. Shinohara, ¶[52]; see Kuboi, ¶[49]; see *infra* VIII.A. In Shinohara's imaging device 1, the photodiode-based

photoelectric conversion portion and pixel transistors are formed on a single semiconductor substrate (substrate 22), along with the logic circuits of the peripheral circuit portion. *See Shinohara*, ¶¶[3]-[4], [58], [81].

VII. THE '360 PATENT

A. Alleged Invention of the '360 Patent

66. The '360 Patent describes a photodetector that includes microstructures to enhance photoabsorption. '360 Patent, 2:31-32, 2:58-62, 3:57-64, 17:13-19. The photodetectors of the '360 Patent include a silicon substrate that has a first layer (P^+ layer), a very low doped N or P layer called the intermediate layer (or I layer), and a second layer (N^+ layer), and further includes holes etched in one or more of the PIN layers. '360 Patent, 15:45-47, 15:64-16:24, 17:35-40. The '360 Patent also discloses the photodetector can be operated in a reverse-bias mode, in which a negative voltage is applied to the anode (P^+ layer) and a positive voltage is applied to the cathode (N^+ layer). '360 Patent, 16:28-31; *see also* '360 Patent, 11:32-38. Figure 5B (below) illustrates the photodetector of the '360 Patent:

**FIG. 5B**

'360 Patent, Fig. 5B.

67. The '360 Patent discloses that optical signals or light can impinge on the light-receiving surface of the photodetector either perpendicular (normal) to the light-receiving surface or at an angle relative to the normal. '360 Patent, 16:36-37. The '360 Patent discloses that one of the causes of enhancement of the absorption coefficient of the incident light includes high contrast grating (HCG) effects. '360 Patent, 11:39-44. The '360 Patent explains that its microstructured pillar-hole-void array can enhance the absorption coefficient of the incident light relative to the bulk absorption coefficient by a factor of 1.1 to over 100 because of the HCG

effect. '360 Patent, 12:36-42. According to the '360 Patent, its photodetector can be integrated with ASIC (application-specific integrated circuits) such as signal processing, signal amplification, optical waveguides, integrated optics, and other integrated circuits for specific applications. '360 Patent, 10:9-13.

B. Prosecution History

68. Applicant filed U.S. Application No. 17/707,429 (“the '429 Application”) with 69 application claims. Ex. 1003, 438-47. Subsequently, Applicant filed a Preliminary Amendment that replaced the previously filed applications claims with new application claims 1-30. Ex. 1003, 329-35. Applicant filed a second preliminary amendment to correct a typographical error in application claim 29. Ex. 1003, 289-97.

69. The Examiner issued one non-final office action objecting to certain application claims and rejecting all application claims 1-30 on the ground of nonstatutory double patenting over claims of U. S. Patent No. 11,309,444. Ex. 1003, 205-07. The Examiner also rejected application claims 1-30 under 35 U.S.C. § 112. Ex. 1003, 207-20. In response, Applicant canceled application claims 1-30 and presented new application claims 31-50. Ex. 1003, 158-62. The Examiner allowed application claims 31-50 stating that the cited prior art failed to anticipate or render obvious “a photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar holes

comprising a laterally extending array of pillars with specific structures and characteristics” as recited in the independent claims. Ex. 1003, 105. However, as I explain in detail below, *Kuboi* or *Yu* in view of *Shinohara* discloses the very features the Examiner found patentable.

C. Claim Construction

70. I have been instructed that the “intrinsic record” includes the patent itself, including the claims, description, and figures (Ex. 1001), and the patent’s prosecution history (Ex. 1003)—i.e., the record of proceedings at the U.S. Patent and Trademark Office (“Patent Office”) concerning the patent. I understand that, like the claims and written description, the prosecution history provides evidence to a person of ordinary skill in the art of how the inventor intended his patent to be understood, and how the Patent Office understood the patent. I understand that the inventor is permitted to apply a special definition to the terms or to limit the scope of claim terms in his patent claims, which may differ from the term’s plain and ordinary meaning. That special definition or limitation on scope may be provided in the patent’s written description, the patent’s prosecution history, or both.

71. I understand that claim interpretation may also be informed by “extrinsic evidence” (that is, evidence outside of the patent record itself). I have been informed that extrinsic evidence may include dictionaries, technical treatises,

and other materials evidencing the meaning of a claim term and the understanding held by a person of ordinary skill in the art (POSITA) in the relevant time period.

72. I have been asked for purposes of this declaration to apply the plain and ordinary meaning of the claim terms as they would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the '360 Patent. Based on my review of the materials and my personal knowledge and experience, I have considered each term of the '360 Patent as it would have been understood by a person of ordinary skill in the art at the earliest claimed priority date of the '360 Patent (May 22, 2013).

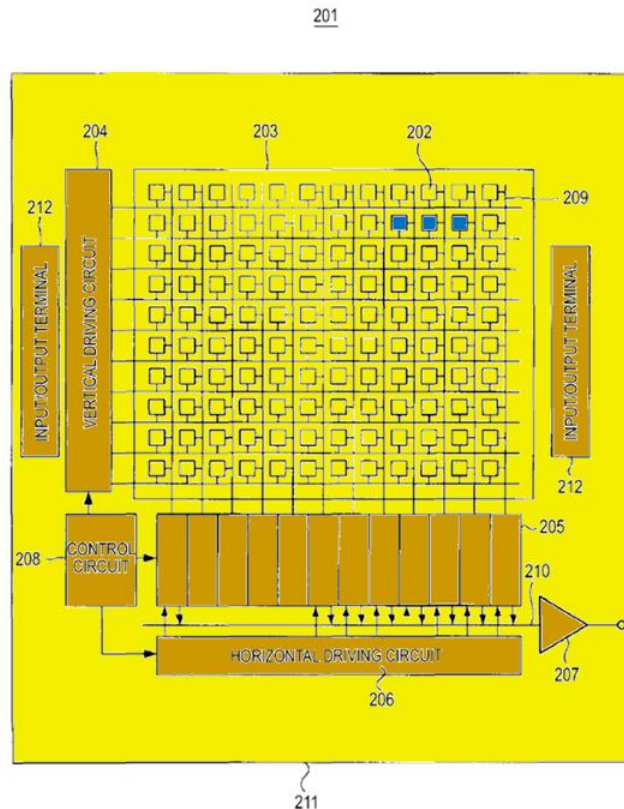
VIII. SUMMARY OF THE PRIOR ART

A. *Kuboi*

73. *Kuboi* is titled Solid-State Imaging Device, Manufacturing Method Thereof, and Electronic Apparatus, was filed on August 19, 2011, and published as U.S. Patent Application Publication No. 2012/0049044 (Ex. 1004) on March 1, 2012. I understand that *Kuboi* is prior art to the '360 Patent.

74. *Kuboi* discloses a complementary metal oxide semiconductor (CMOS) imaging device 201 that includes a pixel region 203 and a peripheral circuit portion formed on a single semiconductor substrate 211. *Kuboi*, ¶[48], Fig. 15. *Kuboi*'s imaging device is illustrated below.

FIG. 15



Kuboi, Fig. 15.

75. According to *Kuboi*, and as shown in the above figure, pixel region 203 of substrate 211 includes a number of pixels 202 that are arranged in a two-dimensional array. *Kuboi*, ¶[48]. Each pixel 202 contains one photoelectric conversion portion (or a photodiode) and four pixel transistors. *Kuboi*, ¶[48]. *Kuboi* also discloses that the peripheral circuit portion includes logic circuits (such as a vertical driving circuit 204, column signal processing circuits 205, horizontal driving circuit 206, output circuit 207, and control circuit 208), which process the pixel's electrical signals and then output the processed electrical signals. *Kuboi*, ¶¶[49]-[54]. *Kuboi* discloses that the pixels and peripheral circuit portion are

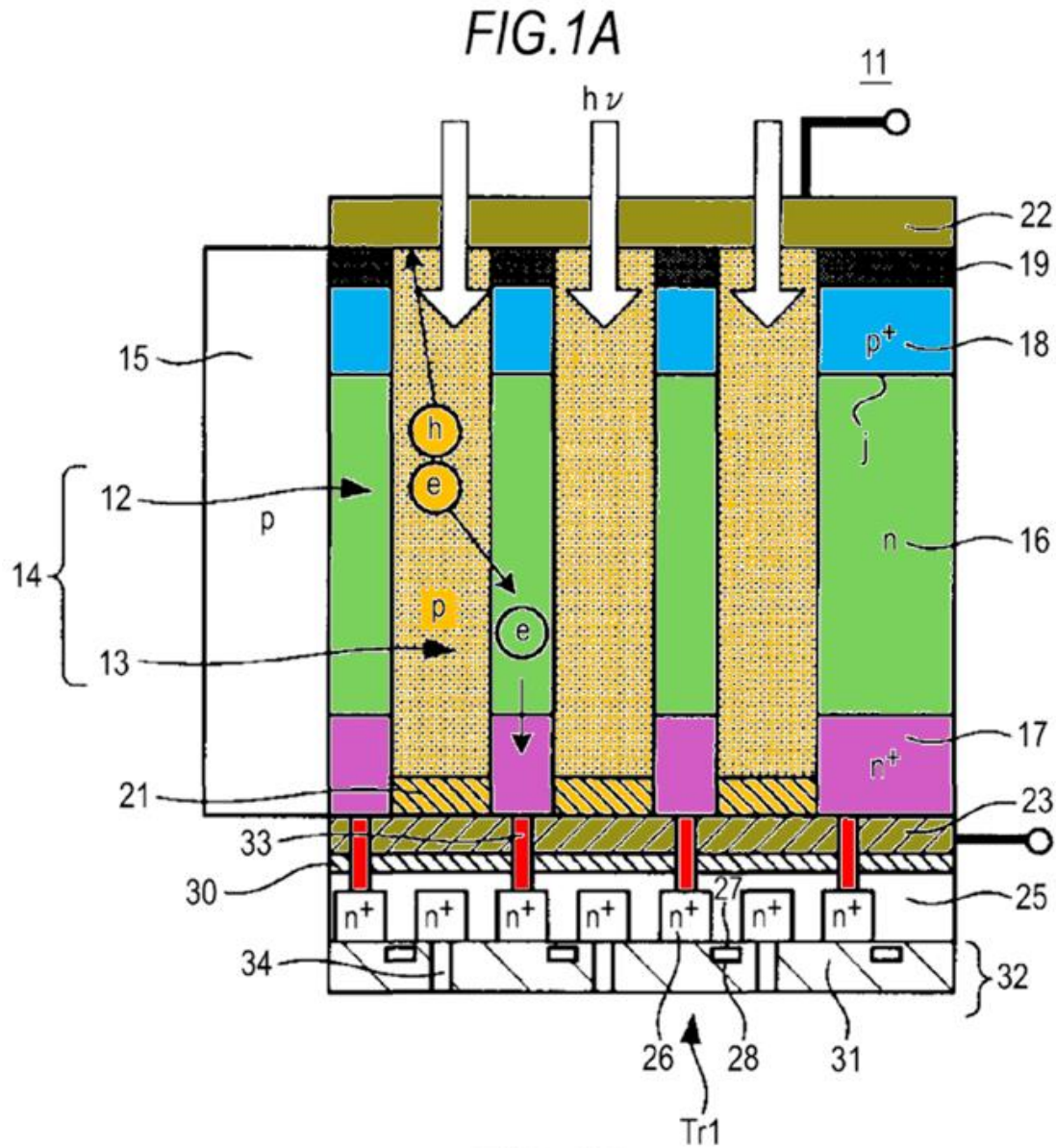
fabricated on one single substrate, the pixel transistors are fabricated on another substrate, and then two substrates are bonded together. *Kuboi*, ¶¶[62], [70], [78].

76. *Kuboi* describes photoelectric conversion portions suitable for use in the imaging device 201 shown in Figure 15. *Kuboi*, ¶[48]. For example, *Kuboi* discloses a basic pixel configuration for its imaging device with reference to Figures 1A/1B. *Kuboi*, ¶[55]. Similarly, *Kuboi* discloses a pixel configuration with reference to Figures 6A/6B, and explains that the disclosed red and green pixels 53R and 53G of Figures 6A/6B have a structure that is the same as the basic configuration of Figures 1A/1B. *Kuboi*, ¶¶[90], [95], [69]. *Kuboi* explains that Figure 13 includes pixels 53R, 53G, and 53B, having configurations that are the same as the pixels of Figures 1A/1B. *Kuboi*, ¶[181]. Similarly, *Kuboi* describes its Figure 15 as being applicable to all of *Kuboi*'s pixel configurations. *Kuboi*, ¶¶[34], [48]. With reference to its Figures 4A-4F, *Kuboi* discloses a method of manufacturing the basic pixel configuration of Figures 1A/1B. *Kuboi*, ¶¶[69]-[76].

77. In my opinion, based on *Kuboi*'s disclosure, a person of ordinary skill in the art would have recognized that the different pixels described by *Kuboi* and illustrated in its Figures 1A/1B, 6A/6B, 13, and 15 all disclose the pixel configuration of the same imaging device 201. Further, in my opinion, Figures 4A-4F of *Kuboi* and the associated description disclose methods of manufacturing that same pixel configuration. Accordingly, throughout this

declaration, references to disclosures associated with Figures 1A/1B, 4A-4F, 6A/6B, 13, and 15 are deemed to be representative of the pixel configuration of the same imaging device 201. In addition, in my opinion, a person of ordinary skill in the art would have found it obvious to combine the elements illustrated and disclosed with Figures 1A/1B, 4A-4F, 6A/6B, 13, and 15.

78. *Kuboi* discloses that pixel 11, including photoelectric conversion portion 14, can be utilized in imaging device 201. *Kuboi*, ¶¶[48], [55]. Figure 1A of *Kuboi*, illustrating a photoelectric conversion portion 14 in a pixel 11, is shown below. *Kuboi*, ¶¶[48], [55]-[56].

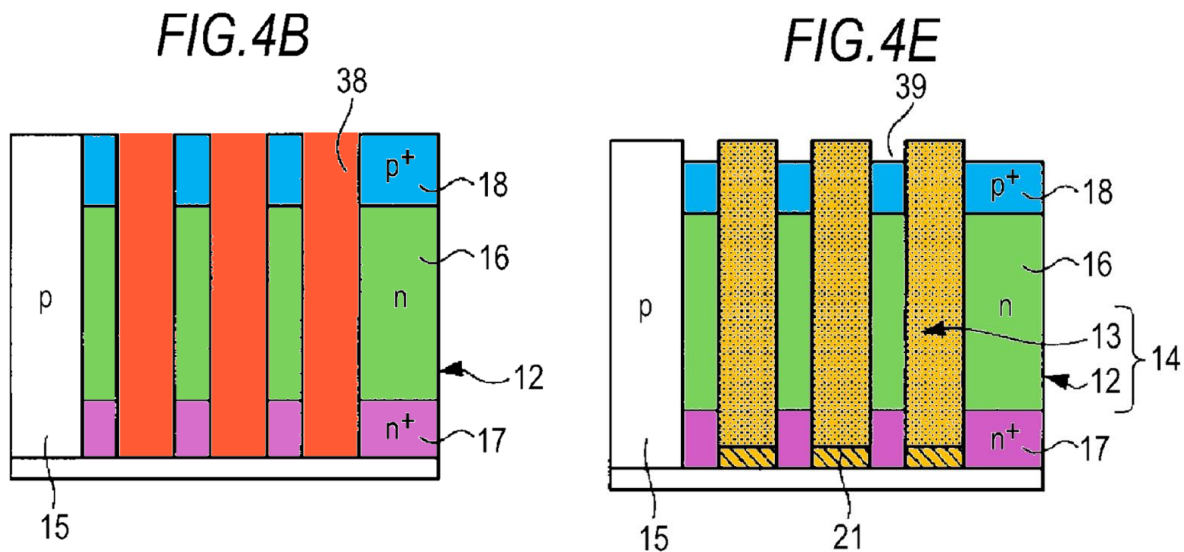


Kuboi, Fig. 1A.

79. Kuboi discloses that **photoelectric conversion portion 14** comprises a silicon semiconductor layer 12 that includes multiple embedded **organic material layers 13**. Kuboi, ¶[55]. Kuboi's silicon semiconductor layer 12 is implanted with different impurities (or doped) to form an **n-type semiconductor (or**

“intermediate”) region 16 with a p⁺ type semiconductor region 18 on one side and an n⁺-type semiconductor region 17 on the opposite side (i.e., stacked PIN regions). *Kuboi*, ¶¶[56], [71]. *Kuboi* discloses that the doping of layer 12 is such that region 18 and region 17 have a higher concentration of impurities than region 16. *Kuboi*, ¶[56].

80. *Kuboi* explains that after forming regions 18, 16, and 17, vertical holes 38 extending from p⁺ type region 18 to n⁺-type region 17 are etched into the PIN regions (illustrated in *Kuboi*’s Figure 4B, below, left). *Kuboi*, ¶¶[71]-[72]. *Kuboi* further discloses that after forming holes 38, the organic material that forms photoelectric conversion films 13 is deposited in holes 38 (illustrated in *Kuboi*’s Figure 4E, below, right). *Kuboi*, ¶¶[72]-[73].



Kuboi, Figs. 4B (left), 4E (right).

81. According to *Kuboi*, a metal shielding film 19 is applied to the surface of region 18 such that only holes 38 containing films 13 are exposed to incident light ($h\nu$). *Kuboi*, ¶¶[59], [72], [73], [76], Figs. 1A, 4F. Further, *Kuboi* discloses that an upper electrode 22 and a lower electrode 23 are formed on opposite sides of the PIN regions. *Kuboi*, ¶[60]. *Kuboi* discloses that a reverse bias is applied to electrodes 22 and 23. *Kuboi*, ¶[64]. Specifically, *Kuboi* discloses that a “necessary voltage is applied between the upper electrode 22 and the lower electrode 23 so that the upper electrode 22 has the negative potential, and the lower electrode 23 has the positive potential.” *Kuboi*, ¶[64].

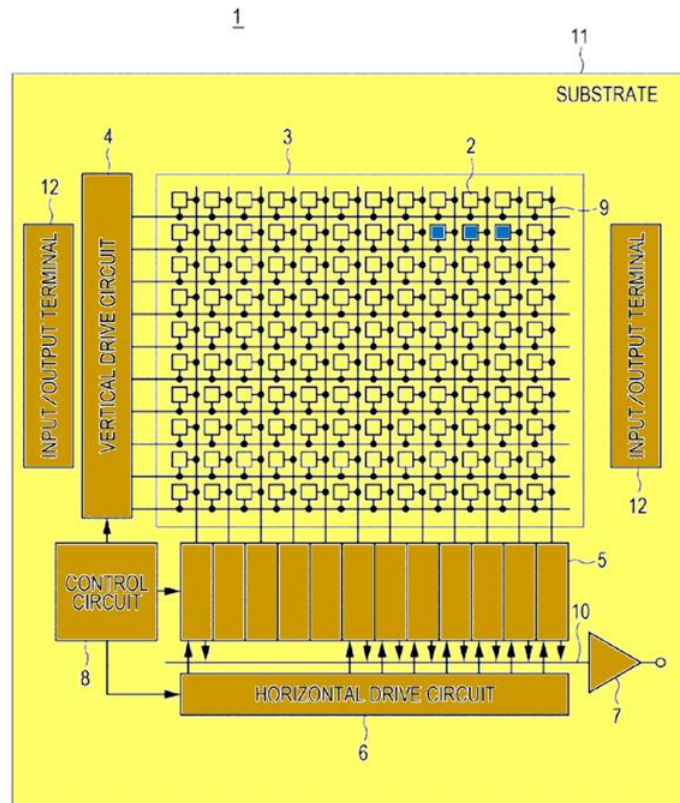
82. *Kuboi* explains that photoelectric conversion of the incident light ($h\nu$) occurs within films 13 (inside holes 38) and results in generation of electron-hole pairs. *Kuboi*, ¶[64]. *Kuboi* discloses that the generated electrons move from the photoelectric conversion film 13 toward the depleted semiconductor layer 12 into a charge accumulation region 26 of the transfer transistor (Tr1) of the corresponding pixel 11 (via conductors 33). *Kuboi*, ¶¶[62], [64], [73]. *Kuboi* also discloses that the holes move toward upper electrode 22 through photoelectric conversion film 13. *Kuboi*, ¶[64]. *Kuboi* explains that after initial signal processing (e.g., amplification) by the pixel transistors, the electrical signals from the pixel 11 are sent to the peripheral circuit portions for further processing. *Kuboi*, ¶¶[48]-[49], [61]-[62].

B. *Shinohara*

83. *Shinohara* is titled Solid-State Imaging Device, Manufacturing Method Thereof, and Electronic Apparatus, was filed on August 2, 2011, and published as U.S. Patent Application Publication No. 2012/0033119 on February 9, 2012. I understand that *Shinohara* is prior art to the '360 Patent.

84. *Shinohara* discloses “a solid-state imaging device which suppresses the generation of white spots and dark current and the occurrence of color mixture and which improves the sensitivity.” *Shinohara*, ¶¶[13], [51]. Specifically, *Shinohara* discloses a solid-state imaging device 1 that includes a pixel region (so-called imaging region) 3 and a peripheral circuit portion. *Shinohara*, ¶[51]. *Shinohara* explains that in its pixel region, a plurality of pixels 2 are arranged in a semiconductor substrate 11, such as a silicon substrate, in a two-dimensional matrix. *Shinohara*, ¶[51]. *Shinohara* also discloses that each of its pixels 2 includes a photoelectric portion. *Shinohara*, ¶[51]. Further, *Shinohara* discloses that the peripheral circuit portion includes logic circuits, such as a vertical drive circuit 4, a column signal processing circuit 5, a horizontal drive circuit 6, an output circuit 7, and a control circuit 8. *Shinohara*, ¶[52]. *Shinohara*'s imaging device including these features is illustrated below:

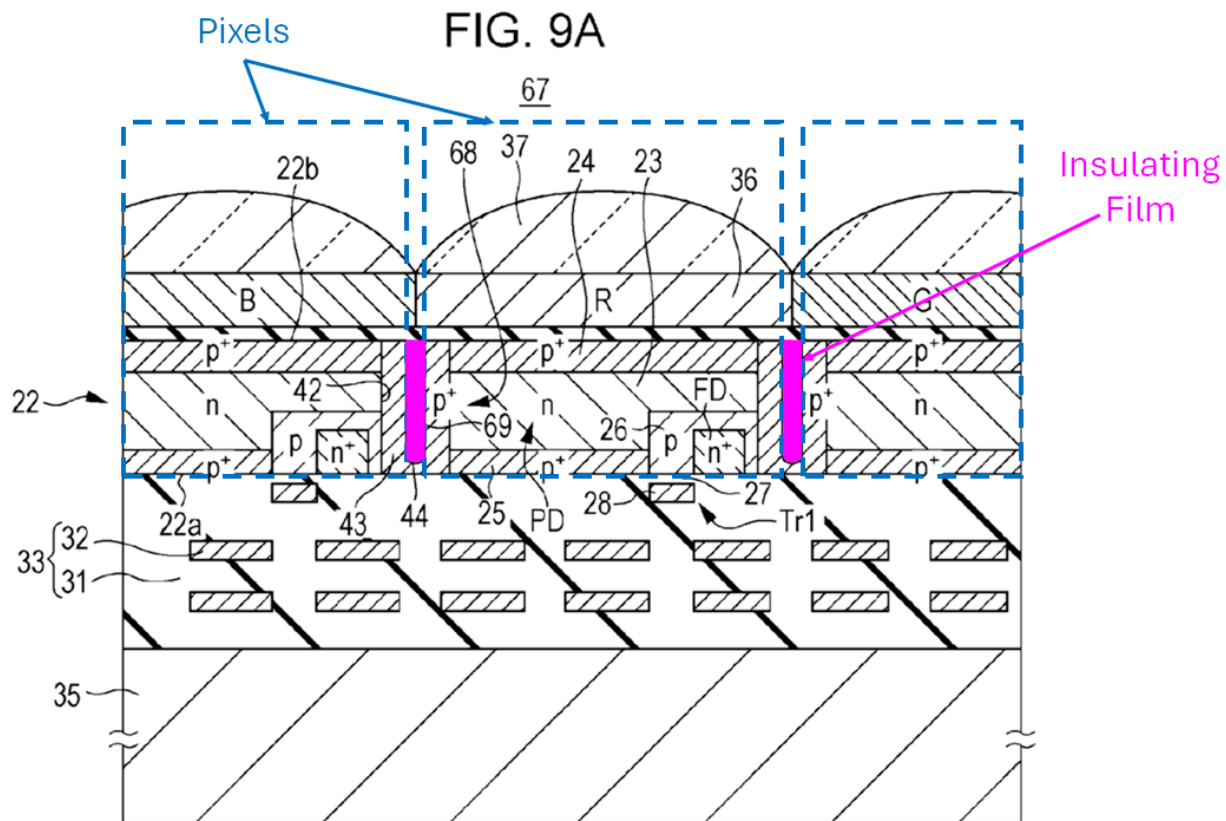
FIG. 1

*Shinohara*, Fig. 1.

85. *Shinohara* discloses that its photodiode PD includes a first conductivity type that functions as both photoelectric conversion and charge storage. *Shinohara*, ¶[58]. *Shinohara* explains that the first conductivity type can be an n-type charge storage region 23. *Shinohara*, ¶[58]. *Shinohara* discloses that its PD also includes second conductivity types, for example, p-type semiconductor regions 25 and 24. *Shinohara*, ¶[58].

86. Further, *Shinohara* discloses that its imaging device includes an element isolation region 68 for isolating pixels and that the element isolation region includes the p-type semiconductor layer 43 provided in trench 42 by an

epitaxial growth. *Shinohara*, ¶[90]. *Shinohara* discloses that an **insulating film 69** is filled in the void 44 inside this p-type semiconductor layer 43. *Shinohara*, ¶[90]. *Shinohara* explains that **insulating film 69** may include a silicon oxide film or a silicon nitride film. *Shinohara*, ¶[91]. *Shinohara*'s imaging device including these features is illustrated below:



Shinohara, Fig. 9A.

87. *Shinohara* also discloses a method for manufacturing the imaging device on a p-type silicon semiconductor substrate 22. *Shinohara*, ¶[68]. For example, *Shinohara* discloses forming an n-type semiconductor region 52, in a region corresponding to the pixel region, by ion-implanting an n-type impurity 51.

Shinohara, ¶[69]. *Shinohara* discloses forming a trench 42 corresponding to the element isolation region and filling trench 42 with a p-type semiconductor region by epitaxial growth so as to form void 44 in trench 42. *Shinohara*, ¶[71].

Shinohara also discloses filling void 44 with an insulating film 69. *Shinohara*, ¶[91].

88. *Shinohara* discloses forming the p-type semiconductor well region 26 in a part of the n-type semiconductor region 52 at a surface side corresponding to each pixel isolated by the element isolation region 41. *Shinohara*, ¶[81]. Further, *Shinohara* discloses forming the floating diffusion portion FD in the p-type semiconductor well region 26 by an n-type semiconductor region. *Shinohara*, ¶[81]. *Shinohara* also discloses, forming the transfer gate electrode 28, transfer transistor Tr1, and other pixel transistors such as a reset transistor Tr2, an amplification transistor Tr3, and a selection transistor Tr4, in the p-type semiconductor well region 26. *Shinohara*, ¶[81].

89. *Shinohara* discloses forming the multilayer wiring layer 33 with a plurality of layers of the wires 32 disposed with at least one interlayer insulating film 31 on the surface of the semiconductor substrate 22. *Shinohara*, ¶[82]. Subsequently, the rear surface 22b of the semiconductor substrate 22 is formed as a light-receiving surface, and the p-type semiconductor region 24 which forms the photodiode PD is formed in the rear surface 22b. *Shinohara*, ¶[85]. In my opinion,

a person of ordinary skill in the art would have understood from *Shinohara's* disclosure that the pixel region, the multilayer wiring, and the pixel transistors in *Shinohara's* imaging device are monolithically formed on a single substrate.

C. Yu

90. *Yu* is titled Vertically Structured Passive Pixel Arrays and Methods for Fabricating the Same, was filed on December 21, 2010, and published as U.S. Patent Application Publication No. 2012/0153124 (Ex. 1050) on June 21, 2012. I understand that *Yu* is prior art to the '360 Patent.

91. *Yu* discloses an image sensor that includes **pixels** having at least one nanopillar adapted to convert light to electrical signals. *Yu*, Abstract, ¶[48]. According to *Yu*, the “image sensor and the control circuit can be formed as an integrated circuit or chip.” *Yu*, ¶[115].

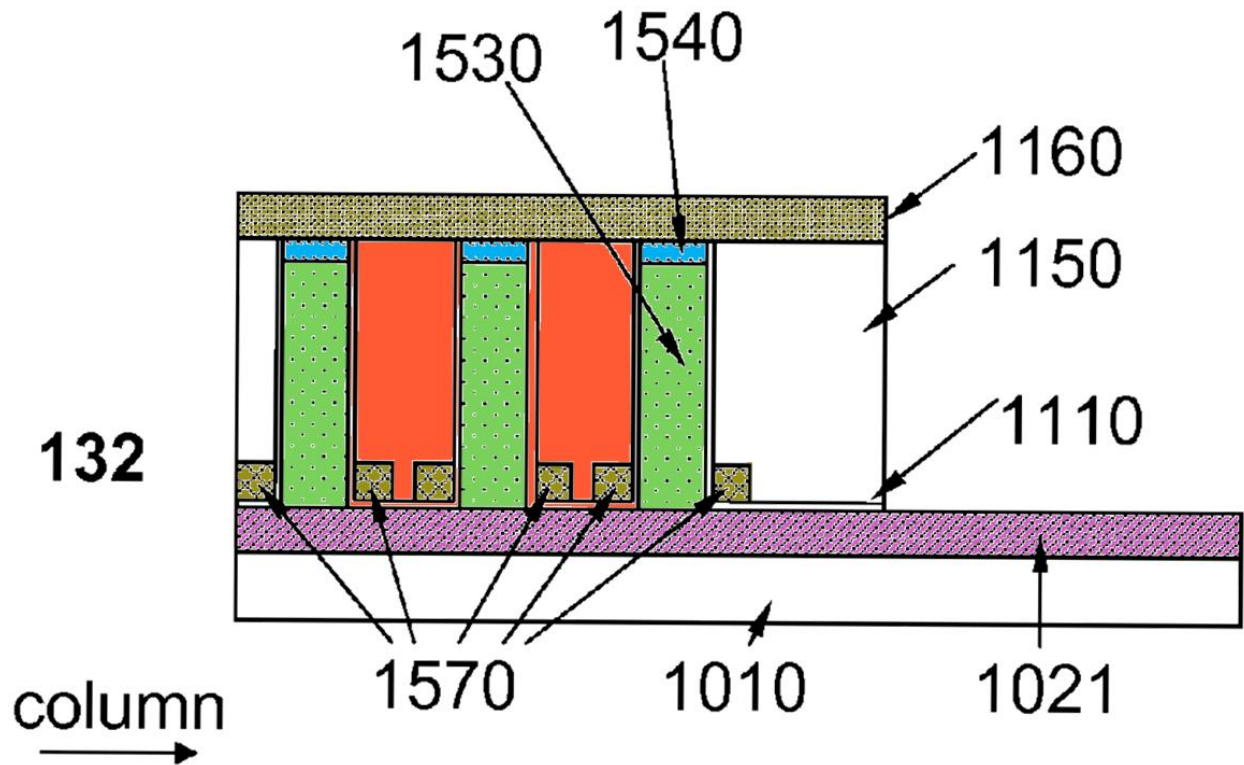
92. *Yu* discloses that the image sensor's **pixels** may include different size nanopillars. *Yu*, ¶[124]. For example, *Yu* discloses a three-nanopillar pixel and a four-nanopillar pixel. *Yu*, ¶¶[130], [124]; Figs. 7A-7B. *Yu* further discloses that “the pixels are organized into a plurality of ‘rows’” and the “pixels can be organized into a plurality of ‘columns.’” *Yu*, ¶¶[51], [9], [17], [25], [48].

93. *Yu* discloses that “the nanopillars and the substrate can comprise suitable semiconductor materials and/or metals such as Si.” *Yu*, ¶¶[55], [27]. *Yu* discloses that its “substrate has an oxide layer 1010, a **heavily doped layer (HDL)**

1020 on the layer 1010 and an **epi layer 1030** on the HDL layer 1020.” *Yu*, ¶[62].

Yu explains that the “substrate can have the following doping profiles: (i) the HDL layer 1020 is p⁺ (i.e. heavily doped to p type), the **epi layer 1030** is p⁻ (i.e. lightly doped to p type); [and] (ii) the HDL layer 1020 [is] p⁺, the **epi layer 1030** is i (i.e.,] intrinsic).” *Yu*, ¶[62]. *Yu* further explains that the “epi layer 1030 can be about 3000 to 10000 nm thick.” *Yu*, ¶[62]. *Yu* discloses that “a **junction layer 1040** is formed on the epi layer 1030,” and that “**junction layer 1040** is of the opposite conduction type as the HDL layer 1020, i.e.,] if the HDL 1020 is p type, the **junction layer 1040** is n type.” *Yu*, ¶[63]. *Yu* discloses that “the exposed portion of the junction layer 1040 and the portion of the epi layer 1030 directly therebelow are deep etched until the HDL layer 1020 directly below the exposed portion of the junction layer 1040 is exposed, to form nanopillars 1500.” *Yu*, ¶¶[68], [76]. The deep etching produces **holes** between adjacent nanopillars.

94. *Yu* explains that a “portion of the **metal layer 1140** deposited around the lower end of the nanopillars 1500 forms the gate electrodes and gate lines 1570.” *Yu*, ¶[85]. Further, *Yu* discloses that “a **transparent conductive layer (TCL) 1160**, such as ITO or aluminum doped zinc oxide (AZO) is deposited by a suitable technique such sputtering.” *Yu*, ¶¶[89], [27], [53]. These features of *Yu*’s pixel are illustrated below, including holes (shown in orange).



Yu, Fig. 1, step 132.

95. *Yu* also discloses “a silicon-on-insulator (SOI)-type substrate or silicon-on-glass (SG)-type substrate.” *Yu*, ¶¶[62], [15], [102].

IX. LEVEL OF ORDINARY SKILL IN THE ART

96. In rendering the opinions set forth in this declaration, I have been asked to consider the '360 Patent's claims and the prior art through the eyes of a person of ordinary skill in the art (which I may also refer to as “one skilled in the art,” “skilled artisan,” “POSITA,” or similar variation). I have considered factors such as the educational level and years of experience of those working in the pertinent art, the types of problems encountered in the art, the teachings of the

prior art, patents and publications of other persons or companies, and the sophistication of the technology.

97. Taking the factors described in the Legal Standards – Level of Ordinary Skill section into consideration, it is my opinion that a person of ordinary skill in the art pertinent to the '360 Patent (May 22, 2013) would have had at least a master's degree in electrical engineering or a similar field and at least five years of experience working with semiconductor systems and semiconductor dice. Additional relevant work experience can compensate for less education, and *vice versa*.

98. As I discussed in the Qualifications and Background section, I received a Ph.D. in Electrical and Electronic Engineering in 1987 and a Doctor of Engineering degree (D.Eng) in electrical and electronic engineering in 2004, both well before the earliest priority date, May 22, 2013, of the '360 Patent. As I also discussed there, I have over 40 years of experience in working with semiconductor systems and semiconductor dice. I also have additional work experience in imaging devices, photonics, and optics, as outlined in the Qualifications and Background section. Accordingly, I was at least a person of ordinary skill in the art as of May 22, 2013.

X. GROUNDS OF UNPATENTABILITY

99. Based on my review of the materials set forth above, including my application of the knowledge of a person of ordinary skill in the art, it is my opinion that claims 1, 3, 5, 6, 8, and 9 of the '360 Patent would have been obvious to one of ordinary skill in the art.

100. In particular, it is my opinion that claims 1, 3, 5, 6, 8, and 9 of the '360 Patent would have been obvious to a person of ordinary skill in the art based on the prior art shown below:

Ground	Claims	Basis	Prior Art
1	1, 3, 5, and 6	§103	<i>Kuboi and Shinohara</i>
2	1, 8, and 9	§103	<i>Yu</i>
3	1, 8, and 9	§103	<i>Yu and Shinohara</i>

XI. THE CHALLENGED CLAIMS ARE UNPATENTABLE OVER THE PRIOR ART

101. In my opinion, claims 1, 3, 5, 6, 8, and 9 of the '360 Patent would have been obvious to one skilled in the art as of the earliest priority date (May 22, 2013) of the '360 Patent.

A. Claims 1, 3, and 5-6 are Obvious Over *Kuboi* and *Shinohara* (Ground 1)

1. Independent Claim 1

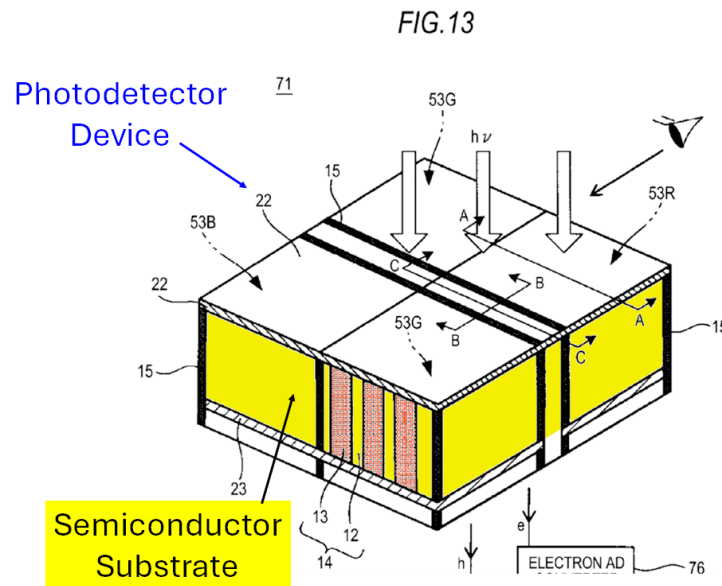
- a. [1pre]: “A photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar holes comprising:”

102. In my opinion, to the extent the preamble limits the scope of claim 1, *Kuboi* discloses the preamble.

103. For example, *Kuboi*'s imaging device is a photodetector device that includes photoelectric conversion portions formed on a silicon substrate. *Kuboi*, Abstract, ¶¶[11]-[13], [55], [181]. *Kuboi*'s “imaging device includes: pixels each including a hybrid photoelectric conversion.” *Kuboi*, Abstract. Specifically, *Kuboi*'s imaging device includes a pixel region in which a group of red, blue, green, and green pixels are arranged in a two-dimensional array.” *Kuboi*, ¶[181]. *Kuboi* explains that “respective pixels 53R, 53G, and 53B include the hybrid photoelectric conversion portion 14.” *Kuboi*, ¶[181]. In my opinion, *Kuboi*'s imaging device is a photodetector because it includes a hybrid photoelectric conversion portion in its pixels that generates electron-hole pairs when light is incident on the hybrid photoelectric conversion portion. *Kuboi*, ¶[64].

104. *Kuboi* also explains that its “hybrid photoelectric conversion portion 14 includes a semiconductor layer 12 formed of silicon and a plurality of organic material layers 13 embedded in the semiconductor layer 12.” *Kuboi*,

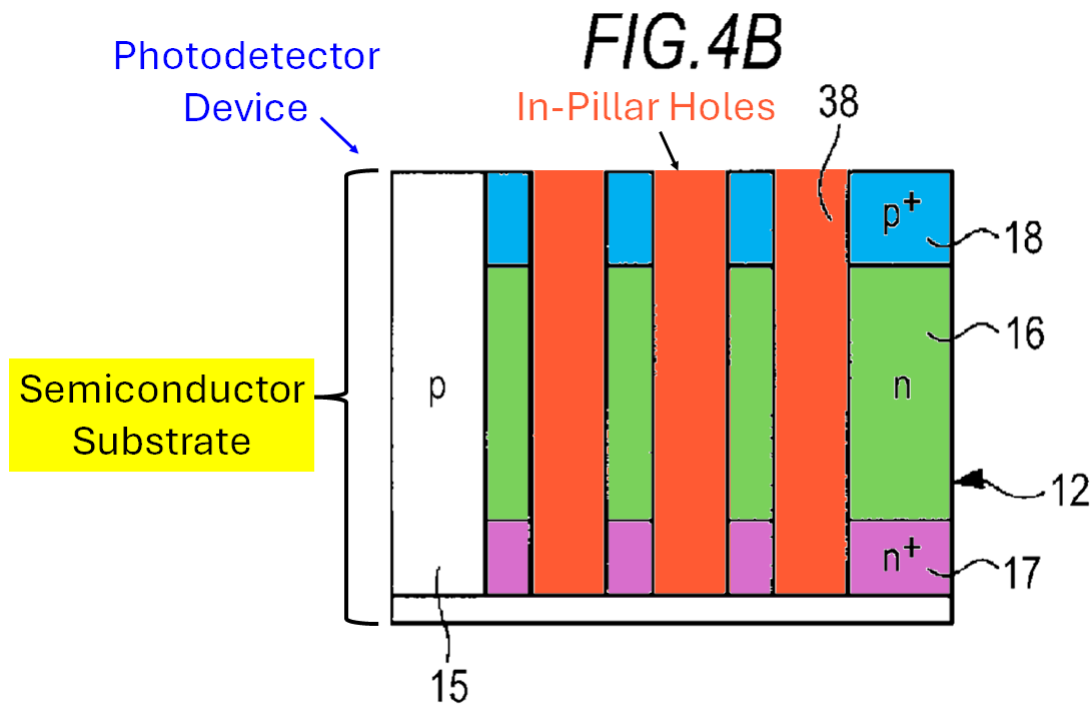
¶¶[55], [181]. In my opinion, therefore, *Kuboi*'s photodetector device is formed in or on a semiconductor substrate (i.e., layer 12 of Figure 13 or layer 211 of Figure 15) because *Kuboi* expressly discloses forming its photoelectric conversion portion in a semiconductor layer formed of silicon. *Kuboi*'s photodetector device formed in or on a semiconductor substrate is illustrated below:



Kuboi, Fig. 13.

105. *Kuboi* also discloses an exemplary pixel manufacturing method in which “element separation region 15” and doped semiconductor regions, including “n⁺-type semiconductor region 17 (corresponding to the front surface side), a n-type semiconductor region 16 (corresponding to an intermediate region), and a p⁺-type semiconductor region [18] (corresponding to the rear surface side) are formed” in a semiconductor substrate. *Kuboi*, ¶[71]. Further, *Kuboi* discloses that “holes 38 are formed at necessary intervals” and that each hole 38 such as a trench

or a via extends from the p⁺-type semiconductor region 18 to the n⁺-type semiconductor region. *Kuboi*, ¶[72]. In my opinion, therefore, *Kuboi*'s photodetector device includes deliberately formed in-pillar holes. I further explain why holes 38 are deliberately formed in its semiconductor substrate in more detail with reference to claim [1d]. *Infra* XI.A.1.i. A portion of *Kuboi*'s photodetector device showing the in-pillar holes formed in a semiconductor substrate is illustrated below:

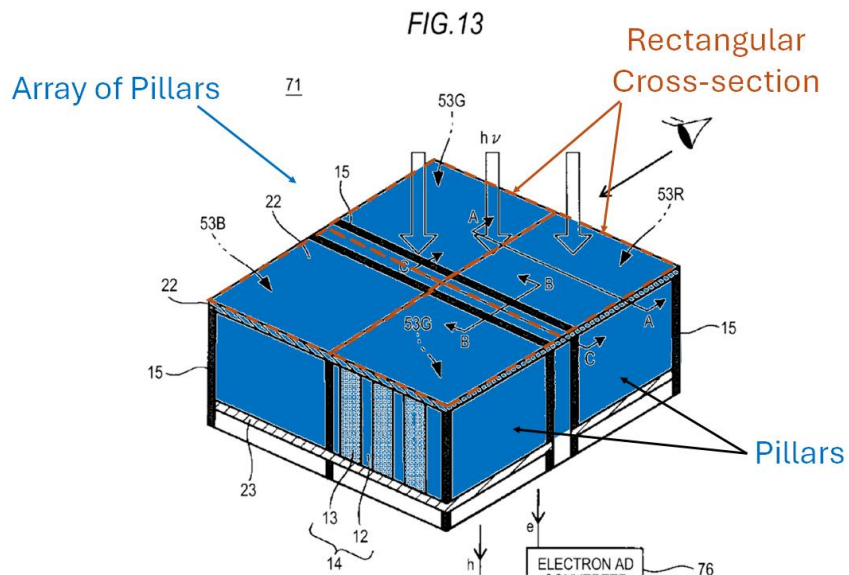


Kuboi, Fig. 4B.

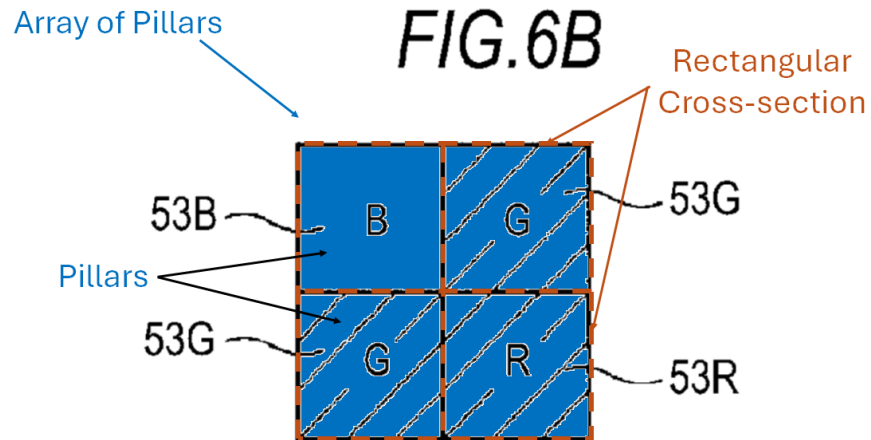
- b. [1a]: “a laterally extending array of pillars that have rectangular cross-sections in a horizontal plane;”

106. In my opinion, *Kuboi* discloses this limitation.

107. For example, *Kuboi* discloses that its imaging device includes “red, blue, green, and green **pixels** ... arranged in a two-dimensional array.” *Kuboi*, ¶¶[181], [90]. In my opinion, *Kuboi*’s **array of pixels** arranged in two-dimensional array form an **array of pillars**. The figures below illustrate a perspective view and a horizontal plan view of a 2-row by 2-column array of *Kuboi*’s pixels. In my opinion, the figures illustrate that each of *Kuboi*’s **pixels** (or **pillars**) has a **rectangular cross-section** and is bounded by **sides of a rectangle**.

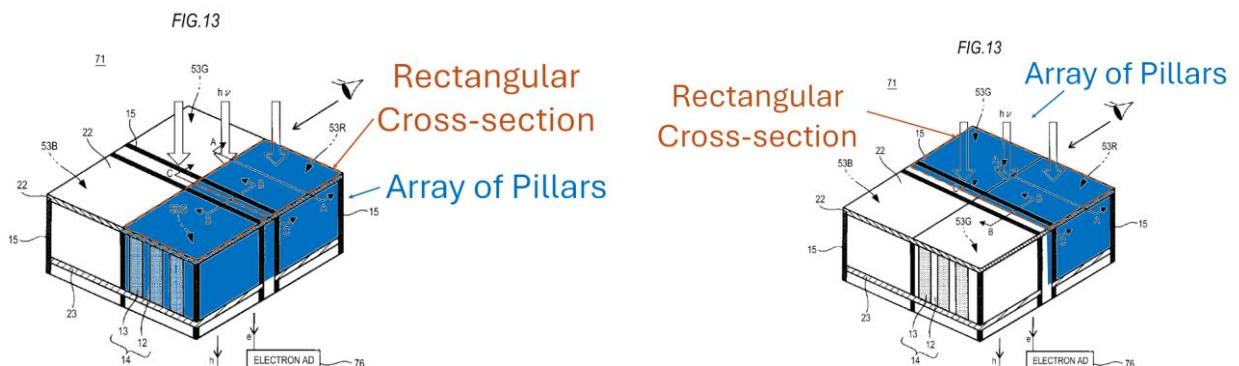


Kuboi, Fig. 13 (perspective view).

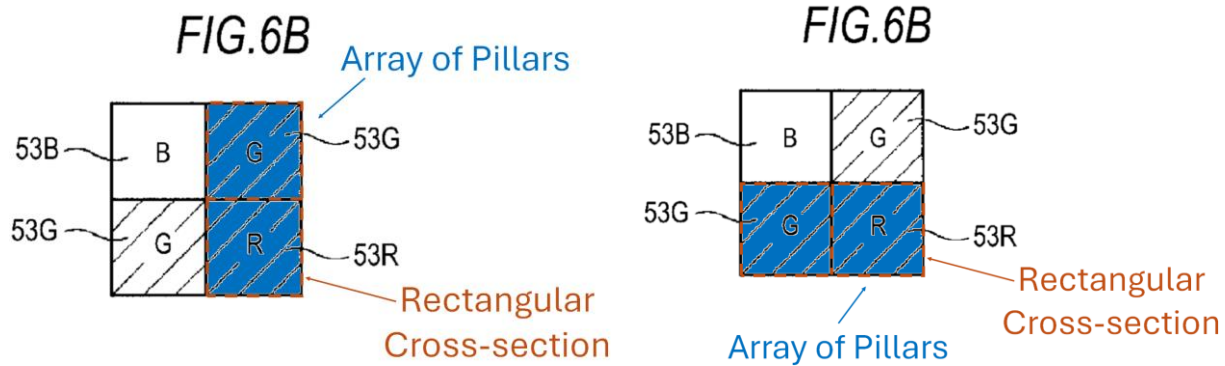


Kuboi, Fig. 6B (horizontal plane view).

108. I note that although pixels 53B, 53G, 53G, and 53R are illustrated as forming a 2-row by 2-column **array of pillars**, one skilled in the art would understand that a subset of these pixels may also form a 2-row by 1-column or a 1-row by 2-column **array of pillars**. These configurations are illustrated in perspective view and horizontal plan view in the figures below.



Kuboi, Fig. 13 (2x1 array, left; 1x2 array, right, perspective views).



Kuboi, Fig. 6B (2x1 array, left; 1x2 array, right, horizontal plan views).

109. To the extent *Kuboi*'s pixels have a square shape, a square is a particular type of rectangle that has sides of equal length. Ex. 1058, 17 ("A square is a parallelogram that is both a rectangle and a rhombus."), 23. In my opinion, therefore, *Kuboi* discloses a laterally extending **array of pixels** (i.e., **array of pillars**) in which **each pillar** has a **rectangular cross-section** in a horizontal plane.

- c. [1b.1]: "wherein said **array of pillars** comprises: a **first doped semiconductor material**; an **intermediate semiconductor material**; and **solid dielectric** between at least portions of **sidewalls** of adjacent **pillars** of said **array of pillars**;"

110. In my opinion, the *Kuboi-Shinohara* combination renders this limitation obvious.

111. *Kuboi* discloses an imaging device that includes "a pixel region 52 in which a **group of pixels** made up of a blue (B) pixel 53B, a red (R) pixel 53R, a green (G) pixel 53G, and a green (G) pixel 53G are arranged in a two-dimensional array." *Kuboi*, ¶[90]. *Kuboi* discloses that in blue pixel 53B (i.e., a **pillar**), "a **p⁺**

type semiconductor region 18, an n-type semiconductor region 16, and a n⁺-type semiconductor region 17 are formed in that order from the light incident surface of the semiconductor layer 12 toward the opposite surface.” *Kuboi*, ¶[91]; *see also* *Kuboi*, ¶¶[71], [181]. *Kuboi* further discloses that in red pixel 53R (i.e., pillar) and green pixels 53G (i.e., pillars), “the same p⁺-type semiconductor region 18, n-type semiconductor region 16, and n⁺-type semiconductor region 17 are formed.” *Kuboi*, ¶[91].

112. *Kuboi* discloses that semiconductor layer 12, which is formed of silicon, is implanted with impurities. *Kuboi*, ¶[56]. Specifically, implanting impurities in *Kuboi*’s semiconductor layer 12 forms “a n⁺-type semiconductor region 17 having higher concentration [of impurities] than the n-type semiconductor region 16.” *Kuboi*, ¶[56]. Similarly, implanting impurities in *Kuboi*’s semiconductor layer 12 forms “a semiconductor region 18 of second conductivity type (for example, p⁺ type) having higher concentration [of impurities] than the n-type semiconductor region 16.” *Kuboi*, ¶[56]; *see also* *Kuboi*, ¶¶[111], [151], [7].

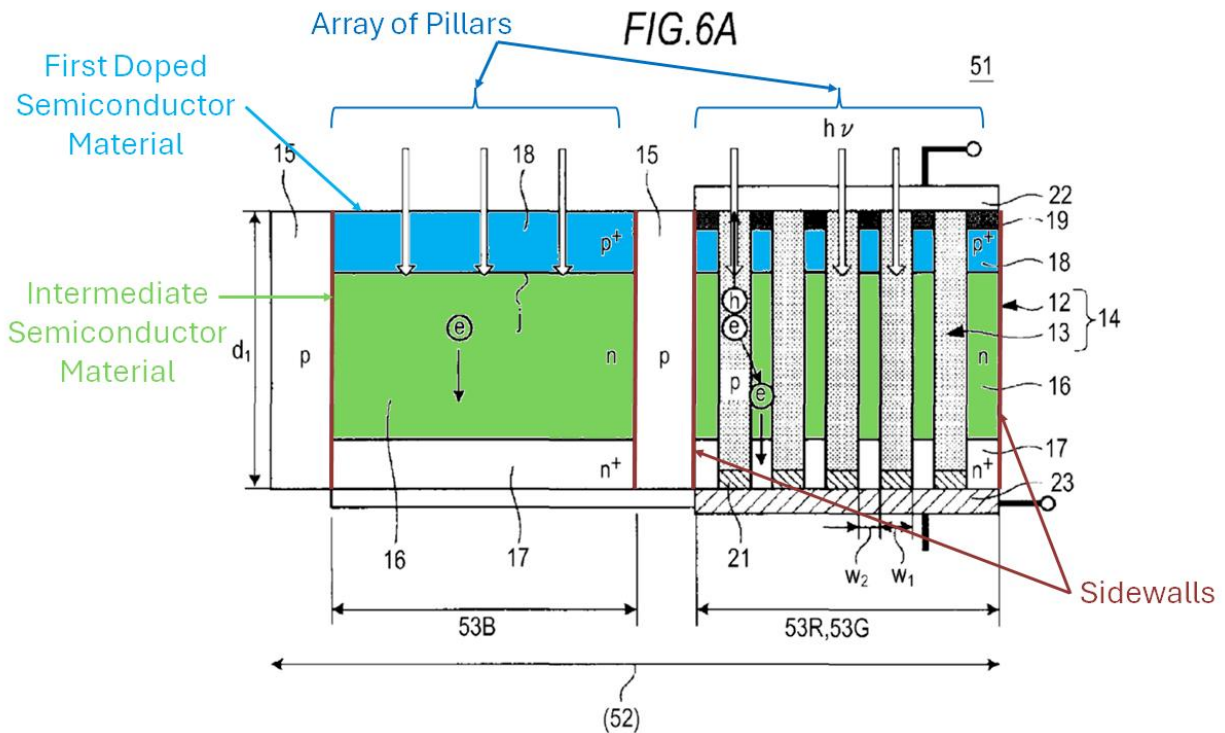
113. In my opinion, one skilled in the art would have understood that the process of implanting impurities into silicon material is known as “doping,” and as a result, region 18 is a “first doped semiconductor material,” as claimed. This is supported by other prior art that would have been known to one skilled in the art.

114. For example, doping of semiconductors by implanting impurities has been well known in semiconductor fabrication since at least the early 1960s, and doping has been a major element of semiconductor manufacturing since then and even today. Ex. 1063, 4 (noting use of diffusion using diffusion techniques to alter the type of conductivity in silicon patented in 1952, and development of ion implantation for doping semiconductors in 1958). Ex. 1067 defines “doping” as “the process of introducing impurity atoms into pure silicon to change its electrical properties.” Ex. 1067, 4. Similarly, Ex. 1063 discloses: “Impurity doping is the introduction of controlled amounts of impurity dopants into semiconductor materials.” Ex. 1063, 37. And Ex. 1020 explains: “A doped region is simply a section of the silicon into which impurity atoms have been purposely added to alter the electrical properties.” Ex. 1020, 4. Therefore, in my opinion, *Kuboi*’s **region 18** is a “**first doped semiconductor material**,” as claimed because it is formed by adding impurity atoms to *Kuboi*’s semiconductor layer 12. Moreover, because *Kuboi*’s **region 16** is located between *Kuboi*’s **p⁺-type semiconductor region 18** and n⁺-type semiconductor region 17, as illustrated in the *Kuboi*’s Figure 6A, *Kuboi*’s **region 16** is an “**intermediate semiconductor region**,” as claimed.

115. According to *Kuboi*, its pixels 11 are “separated by an element separation region 15 formed in the semiconductor layer.” *Kuboi*, ¶[55]. *Kuboi* explains that “[i]n this example, the element separation region 15 is formed by a p-

type semiconductor region.” *Kuboi*, ¶[55]. Thus, while *Kuboi* contemplates forming element separation region 15 by a semiconductor (*Kuboi*, ¶¶[91], [56], [71], [182]), *Kuboi* leaves open the possibility that element separation region 15 may be made of other materials such as solid dielectric materials. *Kuboi*, ¶[55]. Each of *Kuboi*’s pixels 53B, 53R, and 53G also have **sidewalls** adjacent to the element separation region.

116. *Kuboi*’s **first doped semiconductor material** (i.e., **region 18**), **intermediate semiconductor material** (i.e., **region 16**), and **sidewalls** are illustrated below:



Kuboi, Fig. 6A.

117. To the extent the Patent Owner argues that *Kuboi* does not disclose or suggest that *Kuboi*'s element separation region 15 includes a solid dielectric, in my opinion, *Shinohara* discloses this limitation.

118. *Shinohara* discloses an "imaging device" in which "a plurality of unit pixels each having a photodiode PD functioning as a photoelectric conversion portion and a plurality of pixel transistors is regularly arranged in a two-dimensional matrix." *Shinohara*, ¶[58]. *Shinohara* further discloses that its photodiode PD includes "a first conductivity type functioning as both photoelectric conversion and charge storage, i.e., an n-type charge storage region 23," and "second conductivity types," namely "p-type semiconductor regions 25 and 24." *Shinohara*, ¶[58]. *Shinohara*'s region 24 is similar to *Kuboi*'s p-type region 18. In my opinion, therefore, *Shinohara*'s region 24 corresponds to the claimed "first doped region." Likewise, *Shinohara*'s region 23 is similar to *Kuboi*'s n-type intermediate semiconductor material region 16. In my opinion, therefore, *Shinohara*'s region 23 corresponds to the claimed "intermediate semiconductor material."

119. *Shinohara* further discloses that in its imaging device, "an element isolation region 68 for isolating pixels is formed such that the p-type semiconductor layer 43 is provided in the trench 42 by an epitaxial growth, and an insulating film 69 is filled in the void 44 inside this p-type semiconductor

layer 43.” *Shinohara*, ¶[90]. *Shinohara* discloses that insulating film 69 may include “a silicon oxide film or a silicon nitride film.” *Shinohara*, ¶[91].

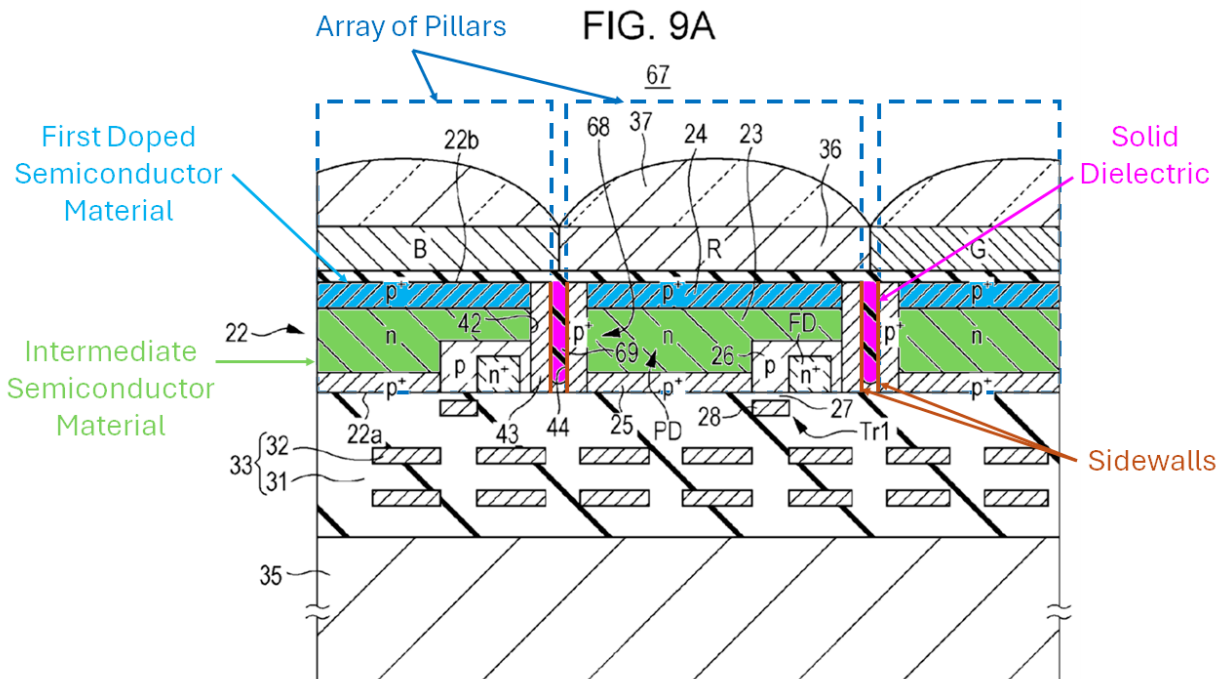
120. In my opinion, a person of ordinary skill in the art would have understood that silicon oxide and silicon nitride films are dielectric materials. This is supported by other prior art that would have been known to one skilled in the art. Ex. 1020, 34 (“Classically, silicon dioxide (generically called oxide here) has served as the insulating dielectric.”); Ex. 1020, 35 (disclosing silicon nitride as “an insulator”); Ex. 1063, 20 (disclosing “[d]ielectric layers such as silicon dioxide and silicon nitride”).

121. In my opinion, one skilled in the art would have further understood that *Shinohara*’s silicon dioxide or silicon nitride film would be made of solid material. This is because thermal oxides like silicon dioxide are formed during semiconductor fabrication processes by oxidizing the solid silicon material. Ex. 1063, 20-21 (disclosing “thermal oxidation” by supplying oxygen for oxidizing solid silicon wafers in a furnace). One skilled in the art would also understand that an insulating film formed by oxidation of silicon would have an amorphous structure, which is characteristic of a solid material. Ex. 1063, 23 (“When silicon is thermally oxidized, the silicon dioxide structure is amorphous.”).

122. Similarly, a skilled artisan would recognize that in semiconductor fabrication silicon nitride is deposited via a chemical vapor deposition (CVD)

process. Ex. 1063, 33. Further, one skilled in the art would have understood that such CVD deposition of silicon nitride would produce a solid layer of silicon nitride. Ex. 1063, 30 (“Chemical vapor deposition (CVD) is a method of forming a thin solid film on a substrate.”).

123. In my opinion, therefore, *Shinohara*’s imaging device includes an array of pixels (i.e., array of pillars) with silicon dioxide or silicon nitride film (i.e., solid dielectrics) disposed between portions (i.e., at least part of the height) of sidewalls of adjacent pillars (i.e., adjacent pixels B and R or adjacent pixels R and G). These features are illustrated below:



Shinohara, Fig. 9A.

124. As I explain below, in my opinion, one skilled in the art would have found it obvious to implement *Shinohara*'s solid dielectric (i.e., insulating film 69) in *Kuboi*'s p-type isolation region. This would have resulted in modifying *Kuboi*'s imaging device to include a "solid dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars," as claimed.

i. Motivation to modify *Kuboi*'s imaging device in view of *Shinohara*'s teaching of a solid dielectric insulating film

125. In my opinion, a person of ordinary skill in the art would have been motivated to implement *Shinohara*'s solid dielectric insulating film in *Kuboi*'s pixel isolation region.

126. Initially, I note that *Kuboi* and *Shinohara* are analogous art to the '360 Patent because, like the '360 Patent, both *Kuboi* and *Shinohara* aim to improve the light absorption efficiency of their respective imaging devices. The '360 Patent is directed to techniques for enhancing photon absorption. '360 Patent, Abstract. Similarly, *Kuboi* discloses a solid-state imaging device in which "the light absorption efficiency in the photoelectric conversion portions of the pixels increases, and the charge mobility increases." *Kuboi*, ¶[16]; see also *Kuboi*, ¶[9]. Likewise, *Shinohara* discloses a solid-state imaging device that improves sensitivity by improving a pixel's light absorption, thereby reducing leakage of

charge into an adjacent pixel. *Shinohara*, ¶¶[12]-[13]. Thus, in my opinion, both *Kuboi* and *Shinohara* are analogous art to the '360 Patent.

127. *Kuboi* discloses that in its imaging device, adjacent pixels are separated by an element separation region formed of p-type semiconductor. *Kuboi*, ¶¶[55], [71], [91]. Like *Kuboi*, *Shinohara* also discloses that adjacent pixels in *Shinohara*'s imaging device are separated by an isolation region made of p-type semiconductor. *Shinohara*, ¶[60]. *Shinohara* discloses, however, that its element isolation region may include a void. *Shinohara*, ¶[60]. *Shinohara* also discloses the void in the p-type element isolation region can be filled with an insulating film made of solid dielectric material, such as silicon oxide or silicon nitride. *Shinohara*, ¶¶[90]-[91].

128. *Shinohara* discloses that filling the void in the element isolation region with the insulating film provides several benefits. First, *Shinohara* discloses that by filling the void in the element isolation region, "adjacent pixels are further electrically insulated from each other, thereby suppressing the leakage of photoelectrically converted charge into an adjacent pixel." *Shinohara*, ¶[94]. Second, *Shinohara* explains that because the insulating film has a refractive index different from that of the p-type semiconductor, any "inclined incident light is reflected at the interface between the silicon and the insulating film and does not leak outside from the pixel." *Shinohara*, ¶[94]. *Shinohara* explains that avoiding

leakage of light into an adjacent pixel “prevent[s] color mixture.” *Shinohara*, ¶[94]. Thus, *Shinohara* outlines the benefits of using a solid dielectric material in the element isolation region between adjacent pixels.

129. In my opinion, one skilled in the art would have understood that including *Shinohara*’s solid dielectric insulating film in *Kuboi*’s element isolation region would improve *Kuboi*’s imaging device by providing benefits similar to those outlined by *Shinohara*. Particularly, one skilled in the art would have recognized that adding *Shinohara*’s insulating film into *Kuboi*’s element separation region would ensure that light incident on a particular pixel does not inadvertently leak into and generate electrical charge in a neighboring pixel of *Kuboi*’s imaging device. A skilled artisan would also have recognized that implementing *Shinohara*’s insulating film in *Kuboi*’s element separation region would help light incident at an angle on a pixel to be reflected back into that same pixel, allowing more light to be absorbed by that pixel. A skilled artisan would have understood that such improved light absorption would also improve the efficiency of *Kuboi*’s modified imaging device.

130. In my opinion, a skilled artisan would therefore have been motivated to implement *Shinohara*’s insulating film in *Kuboi*’s imaging device to realize the benefits of this configuration outlined by *Shinohara*. Furthermore, in my opinion, modifying *Kuboi*’s element separation region in this manner would have involved

nothing more than the use of a known technique (namely inserting an insulating film in the element separation region), to improve a similar device (namely *Kuboi's* imaging device), in the same way (namely, by improving electrical insulation between adjacent pixels and minimizing light leakage between adjacent pixels).

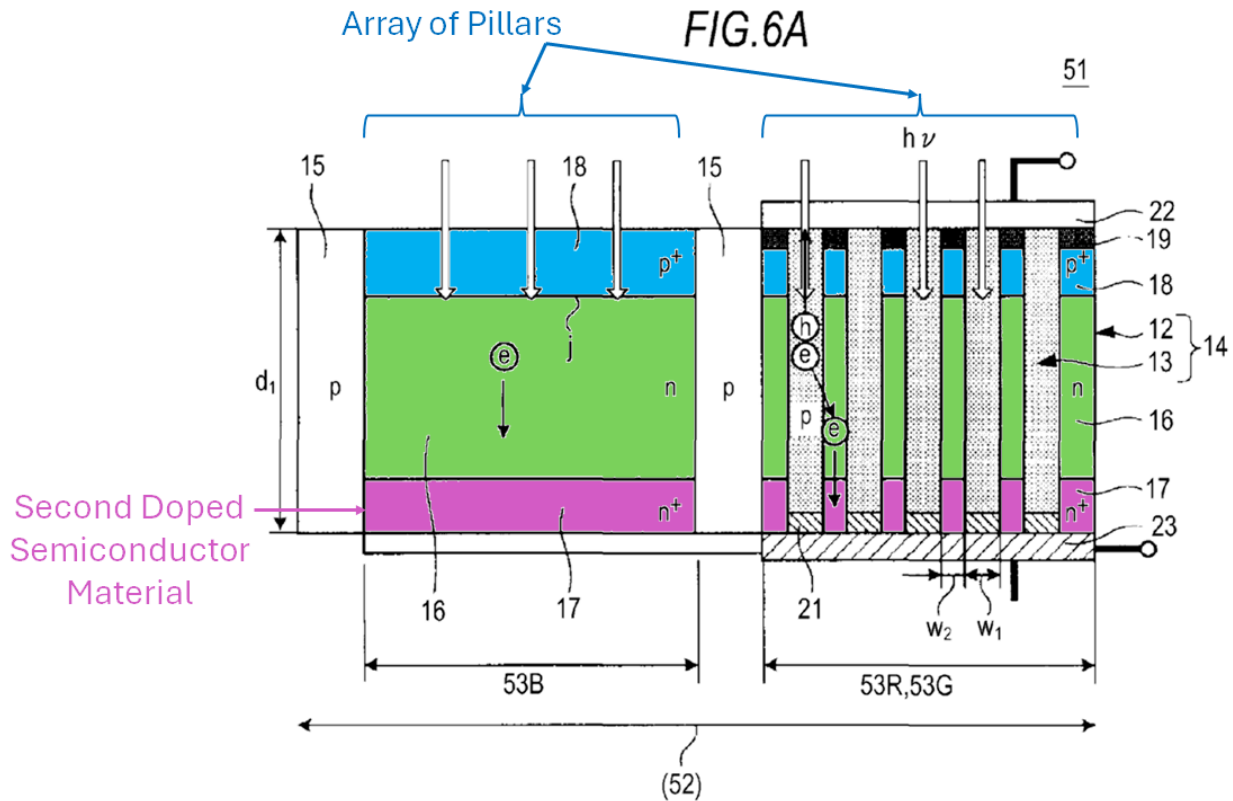
131. It is also my opinion that a person of ordinary skill in the art would have had a reasonable expectation of success in implementing *Shinohara's* teachings in *Kuboi's* imaging device. Both *Kuboi* and *Shinohara* disclose similar imaging devices with adjacent pixels separated by an element separation or element isolation region. Moreover, *Shinohara* discloses a method of manufacturing the element isolation region with an insulting film disposed in the element isolation region. In my opinion, based on these disclosures, it would have been well within the skill level of a person of ordinary skill in the art to implement *Shinohara's* insulating film into *Kuboi's* element separation region. Further, in my opinion, a skilled artisan would have had a reasonable expectation of success because implementing *Shinohara's* insulating film in *Kuboi's* element separation region merely requires combining well-known prior elements and manufacturing methods taught by *Shinohara*.

132. Therefore, it is my opinion that the combination of *Kuboi* and *Shinohara* renders claim [1b.1] obvious.

d. [1b.2]: “a second doped semiconductor material; wherein:”

133. In my opinion, *Kuboi* discloses this limitation.

134. *Kuboi* discloses that in its blue pixel 53B, region 18, region 16, and region 17 “are formed in that order.” *Kuboi*, ¶[91]; see also *Kuboi*, ¶¶[71], [181]. Further, *Kuboi* discloses that, in its red pixel 53R and green pixels 53G, “the same” region 18, region 16, and region 17 “are formed.” *Kuboi*, ¶[91]; see also *Kuboi*, ¶¶[71], [181]. As I discussed for claim [1b.1], *Kuboi*’s region 17 is formed by implanting semiconductor layer 12 with impurities. *Kuboi*, ¶¶[55]-[56]; *supra* XI.A.1.c. As I also explained for claim [1b.1], “the process of introducing impurity atoms into pure silicon” results in a doped semiconductor material. Ex. 1067, 4; Ex. 1063, 37; Ex. 1020, 4; *supra* XI.A.1.c. Thus, because *Kuboi*’s region 17 is formed by implanting impurities in semiconductor layer 12, *Kuboi*’s region 17 is the claimed “second doped semiconductor material.” *Kuboi*’s photodetector device with the “second doped semiconductor material” (i.e., region 17) is illustrated below.



Kuboi, Fig. 6A.

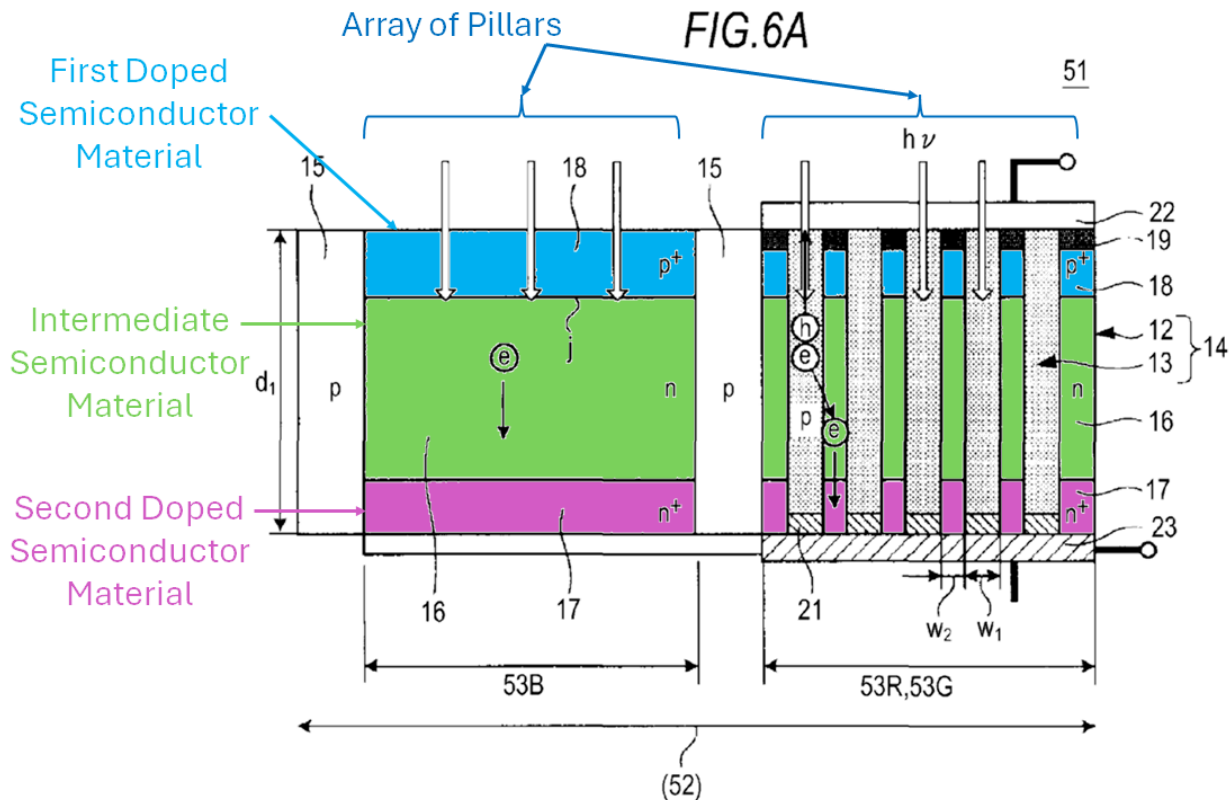
- e. [1c.1]: “the **intermediate semiconductor material** is between said **first** and **second** doped semiconductor materials;”

135. In my opinion, *Kuboi* discloses this limitation.

136. As I discussed for claims [1b.1] and [1b.2], *Kuboi* discloses that region 18, region 16, and region 17 “are formed in that order from the light incident surface of the semiconductor layer 12 toward the opposite surface.”

Kuboi, ¶¶[91], [55]-[56], [71], [181]; *supra* XI.A.1.c ([1b.1]), XI.A.1.d ([1b.2]). In my opinion, because layers 18, 16, and 17 are formed “in that order,” *Kuboi* discloses that its intermediate semiconductor material (region 16) is located

between its first doped semiconductor material (region 18) and its second doped semiconductor material (region 17). This arrangement of *Kuboi's* regions 18, 16, and 17 is illustrated below:



Kuboi, Fig. 6A.

- f. [1c.2]: “the **first** and **second** doped semiconductor materials are doped to opposite semiconductor types;”**

137. In my opinion, *Kuboi* discloses this limitation.

138. As I discussed for claims [1b.1], [1b.2] and [1c.1], *Kuboi* discloses that region 18, region 16, and region 17 are formed in its semiconductor layer 12. *Kuboi*, ¶¶[91], [55]-[56], [71], [181]; *supra* XI.A.1.c ([1b.1]), XI.A.1.d ([1b.2]),

XI.A.1.e ([1c.1]). Further, as I discussed for claim [1b.1], *Kuboi*'s p⁺-type semiconductor region 18 is the claimed first doped semiconductor material. *Supra* XI.A.1.c ([1b.1]). Similarly, as I discussed for claim [1b.2], *Kuboi*'s n⁺-type semiconductor region 17 is the claimed second doped semiconductor material. *Supra* XI.A.1.d ([1b.2]). In my opinion, one skilled in the art would have understood that *Kuboi* discloses that its first and second doped semiconductor materials are doped to opposite semiconductor types because *Kuboi*'s first doped semiconductor material is a p⁺-type semiconductor region 18 and because *Kuboi*'s second doped semiconductor material is the oppositely doped n⁺-type semiconductor region 17. *Yu*, ¶[63] (stating that a p type semiconductor region is of an opposite conductivity compared to a n type semiconductor region).

- g. [1c.3]: “the intermediate semiconductor material is less doped than at least one of the first and second doped semiconductor materials and the degree of doping is the same or different for different positions in the intermediate semiconductor material; and”

139. In my opinion, *Kuboi* discloses this limitation.

140. *Kuboi* discloses that “semiconductor layer 12 is implanted with impurities.” *Kuboi*, ¶[56]. As I discussed for claim [1b.1], one skilled in the art would have understood that the process of implanting impurities into silicon material is known as “doping.” *Supra* XI.A.1.c. *Kuboi* also discloses that semiconductor layer 12 includes “n⁺-type semiconductor region 17 having higher

concentration [of impurities] than the **n-type semiconductor region 16**.” *Kuboi*, ¶[56]. Similarly, *Kuboi* discloses that semiconductor layer 12 includes “a **semiconductor region 18** of second conductivity type (for example, **p⁺ type**) having higher concentration [of impurities] than **n-type semiconductor region 16**.” *Kuboi*, ¶[56]. Further, as I discussed for claim [1b.1], *Kuboi*’s **p⁺-type semiconductor region 18** is the claimed **first doped semiconductor material**. *Supra* XI.A.1.c ([1b.1]). Similarly, as I discussed for claim [1b.2], *Kuboi*’s **n⁺-type semiconductor region 17** is the claimed **second doped semiconductor material**. *Supra* XI.A.1.d ([1b.2]).

141. Thus, *Kuboi* discloses that both the first and second doped semiconductor materials (i.e., **region 17** and **region 18**) have a higher doping concentration than the intermediate semiconductor material (i.e., **region 16**). In my opinion, one skilled in the art would have understood these disclosures to mean that *Kuboi*’s intermediate semiconductor material (i.e., **region 16**) is less doped than *Kuboi*’s first and second doped semiconductor materials (**region 17** and **region 18**).

142. *Kuboi* does not expressly describe the degree of doping at different positions in the **n-type region 16** (“**intermediate layer**”). However, in my opinion, one skilled in the art would have understood that the degree of doping would either

be the same or different at different positions in **n-type region 16** as no other possibilities exist.

143. In *Kuboi*, the silicon semiconductor layer 12 is “implanted with impurities” in the **n-type region 16**. *Kuboi*, ¶¶[55]-[56], [71], Fig. 4. In my opinion, a person of ordinary skill would have understood that “[d]iffusion and ion implantation are the two key methods of impurity doping” in CMOS technology. Ex. 1063, 37. In both methods, the doping concentration varies progressively with depth into the semiconductor. *Kuboi* employs “ion implantation” for implanting impurities in semiconductor layer 12. *Kuboi*, ¶¶[7], [134].

144. In the ion implantation process, which was developed and refined in the 1960s for silicon semiconductor processing and is still used today, the dopant ions are implanted into the semiconductor by means of an ion beam. Ex. 1063, 4. “The doping concentration has a peak distribution inside the semiconductor and the profile of the dopant distribution is determined mainly by the ion mass and the implanted-ion energy.” Ex. 1063, 37. Specifically, during ion implantation, dopant ions are propelled to high velocities and embedded into the silicon wafer as shown in the figure below. Ex. 1020, 4. Through collisions with silicon atoms, the ions lose energy and settle within the wafer. Ex. 1020, 4. This is illustrated in the figure below.

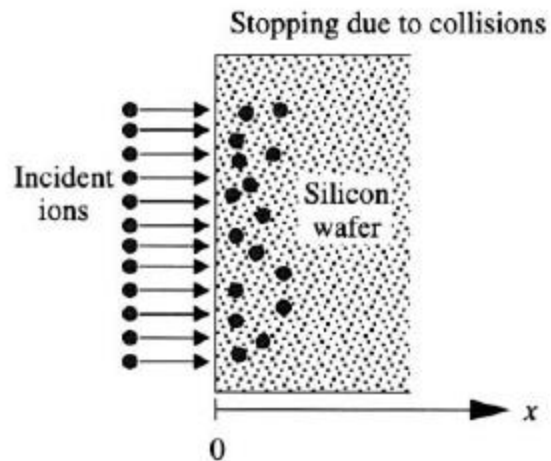


Figure 2.3 The ion stopping process

Ex. 1020, 4.

145. In ion implantation, the dopant concentration varies with wafer depth (x in the figure above) and can be approximated by a Gaussian distribution.

Ex. 1020, 4. The figure below illustrates the dopant concentration as a function of depth when ion implantation is employed for doping.

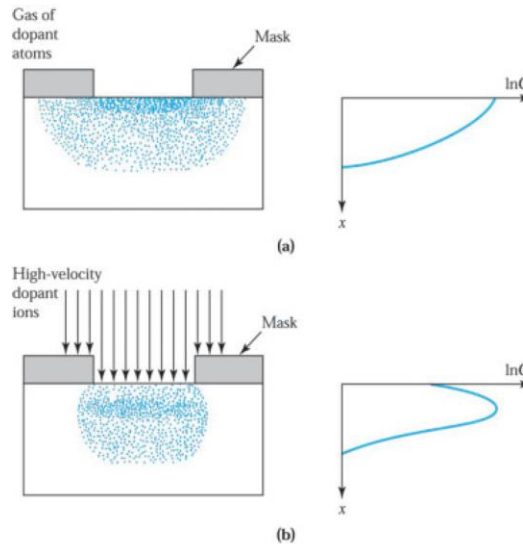


Fig. 1 Comparison of (a) diffusion and (b) ion-implantation techniques for selective introduction of dopants into the semiconductor substrate.

Ex. 1063, 38.

146. The figure above illustrates how dopant concentration varies with depth (x) in a semiconductor substrate after ion implantation. Ex. 1063, 37-38. Based on the figure above, the dopant concentration at the same depth (in a direction perpendicular to x in the figure on the right above) would be the same. A similar dopant distribution pattern occurs when an n-type dopant is introduced into *Kuboi*'s silicon semiconductor layer 12 via ion implantation, to form **n-type region 16** (“**intermediate layer**”). Typically, arsenic (As) and phosphorus (P) serve as dopants for n-type regions. Ex. 1020, 4 (“Arsenic (As) and phosphorus (P) are used for n-type regions”); Ex. 1063, 38 (explains that “arsenic and phosphorus are used extensively as n-type dopants”). The figure below visually represents the

dopant concentration profile as a function of depth when a silicon substrate undergoes implantation with arsenic (As) and phosphorus (P). *See* Ex. 1028, 1.

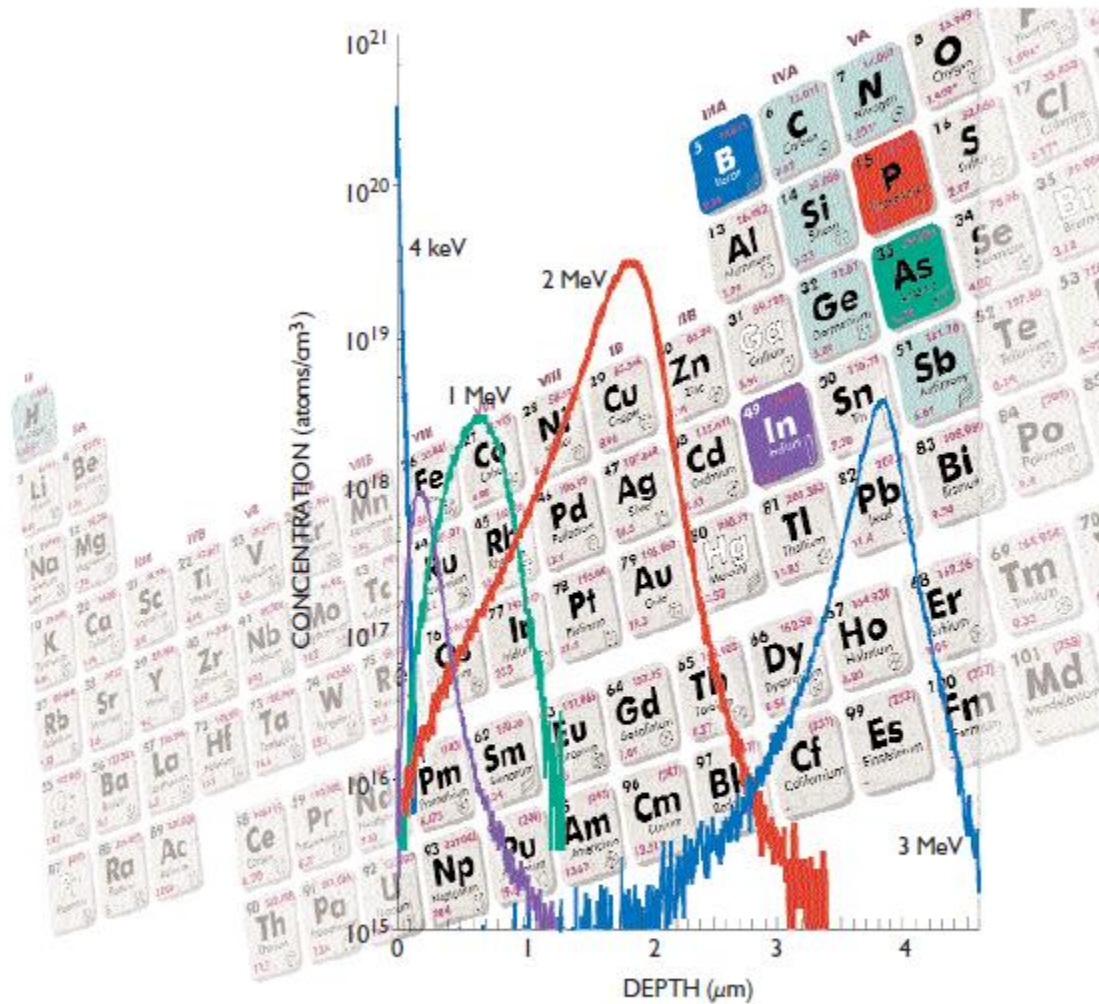
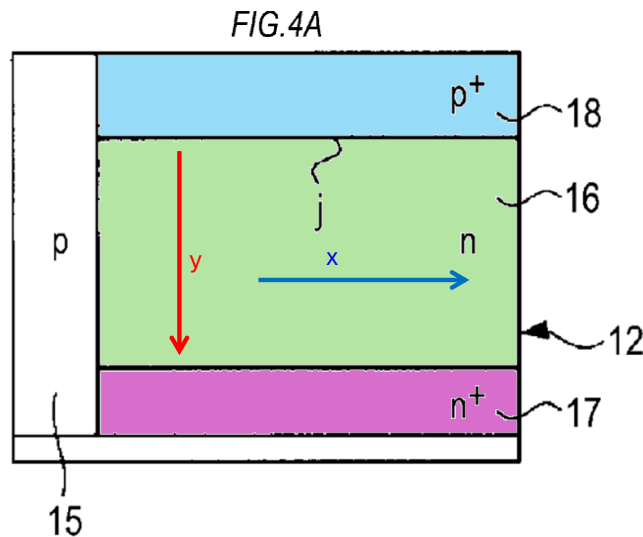


Figure 1. Some of the most commonly implanted species highlighted on the periodic table, along with typical concentration-versus-depth traces for various implant energies.

Ex. 1028, 1.

147. The **red curve** in the figure above illustrates how the concentration of phosphorus (**P**) atoms changes with depth when silicon undergoes ion implantation doping. *See* Ex. 1028, 1. The **green curve** illustrates that a similar distribution

pattern occurs when arsenic (As) is used as the dopant. *See* Ex. 1028, 1. A person of ordinary skill in the art would understand that the degree of doping, or the dopant concentration, would vary in a similar manner in *Kuboi's* n-type region 16 (“intermediate layer”). I have illustrated the variation of dopant concentration that may occur in *Kuboi's* n-type region 16 (“intermediate layer”) below:



Kuboi, Fig. 4A.

148. In other words, one skilled in the art would have understood that the degree of doping will be different at different positions along the depth (along line *y* in the figure above) of *Kuboi's* n-type region 16, and the degree of doping will be the same for different positions along the width (along line *x* in the figure above) of *Kuboi's* n-type region 16.

149. A person of ordinary skill in the art would have thus recognized that “the degree of doping is the same or different for different positions in the **intermediate semiconductor material**” of *Kuboi* as claimed.

h. [1c.4]: “each of the first and second doped semiconductor materials and said intermediate semiconductor material comprises Si;”

150. In my opinion, *Kuboi* discloses this limitation.

151. *Kuboi* discloses that pixel 11 includes “semiconductor layer 12 formed of silicon.” *Kuboi*, ¶¶[55], [70]-[71], [91], [108], [181]. Moreover, as I discussed for claim [1c.3], semiconductor layer 12 includes “**n⁺-type semiconductor region 17** having higher concentration [of impurities] than the **n-type semiconductor region 16**” and “a **semiconductor region 18** of second conductivity type (for example, **p⁺ type**) having higher concentration [of impurities] than **n-type semiconductor region 16**.” *Kuboi*, ¶[56]; *supra* XI.A.1.g ([1c.3]).

152. As I also discussed for claim [1b.1], *Kuboi*’s **p⁺-type semiconductor region 18** is the claimed **first doped semiconductor material** and *Kuboi*’s **n-type semiconductor region 16** is the claimed **intermediate semiconductor material**. *Supra* XI.A.1.c ([1b.1]). Similarly, as I discussed for claim [1b.2], *Kuboi*’s **n⁺-type semiconductor region 17** is the claimed **second doped semiconductor material**. *Supra* XI.A.1.d ([1b.2]).

153. In my opinion, because *Kuboi*'s semiconductor region 18 (i.e., first doped semiconductor material), semiconductor region 16 (i.e., intermediate semiconductor material) and semiconductor region 17 (i.e., second doped semiconductor material) are each created by implanting impurities into silicon, each of these regions will comprise silicon. *Kuboi*, ¶[3] (“an impurity-implanted crystalline silicon layer”); *see also Kuboi*, ¶¶[7], [56], [66]. That is each of *Kuboi*'s “first and second doped semiconductor materials and said intermediate semiconductor material” comprises silicon (i.e. Si) as claimed.

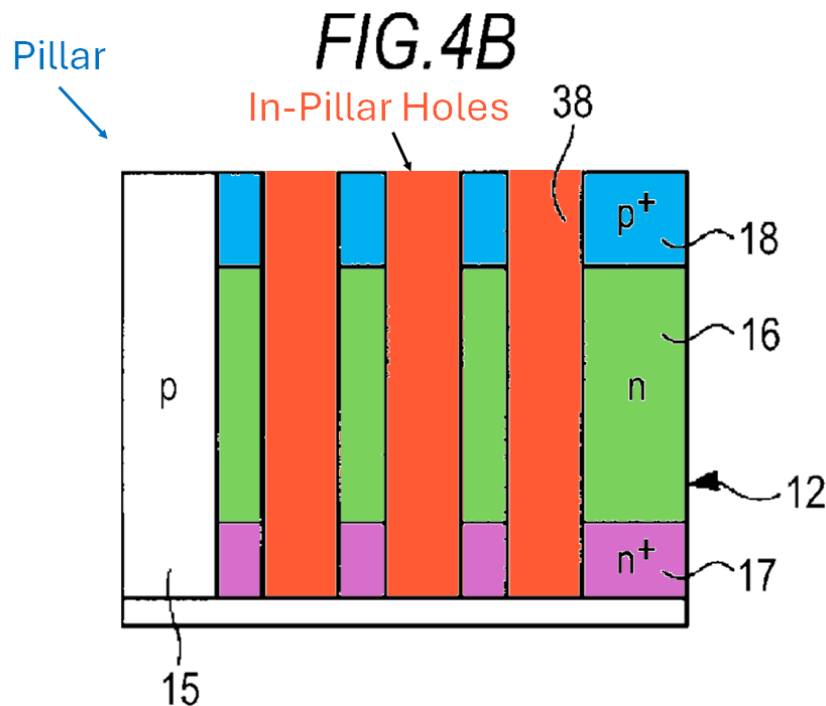
i. [1d]: “one or more deliberately formed in-pillar holes with solid dielectric therein;”

154. In my opinion, *Kuboi* discloses this limitation.

155. *Kuboi* discloses that “hole 38 such as a trench or a via extending from the p⁺-type semiconductor region 18 to the n⁺-type semiconductor region is formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching.” *Kuboi*, ¶¶[72], [13]-[14], [67], [95]. *Kuboi* further discloses that a “plurality of vertical holes 38 are formed at necessary intervals” and “holes 38 are formed in a stripe shape.” *Kuboi*, ¶[72]. Additionally, *Kuboi* discloses that the holes 38 may be dry-etched “using a CCP (Capacitive Coupled Plasma) etching apparatus” or other apparatuses. *Kuboi*, ¶¶[72], [95]. In my opinion, because holes 38 are formed using a CCP apparatus, one skilled in the art would have

understood that these **holes 38** are deliberately formed in *Kuboi*'s semiconductor layer 12.

156. Furthermore, as I discussed for claim [1a], each **pixel** of *Kuboi* is a **pillar**. *Supra* XI.A.1.b. Thus, *Kuboi*'s **holes 38** are **in-pillar holes** because they are formed in a semiconductor layer 12 corresponding to a **pixel** (i.e., **pillar**) of *Kuboi*'s imaging device. *Kuboi*, ¶[72]. The **in-pillar holes** formed in *Kuboi*'s **pixel** (i.e., **pillar**) are illustrated below:



Kuboi, Fig. 4B.

157. *Kuboi* also discloses that “an **electron blocking film 21** having a thickness of several tens of nm, for example is formed on the bottom portions of the vertical holes 38.” *Kuboi*, ¶¶[73], [91]. *Kuboi* explains that “**film 21** is formed

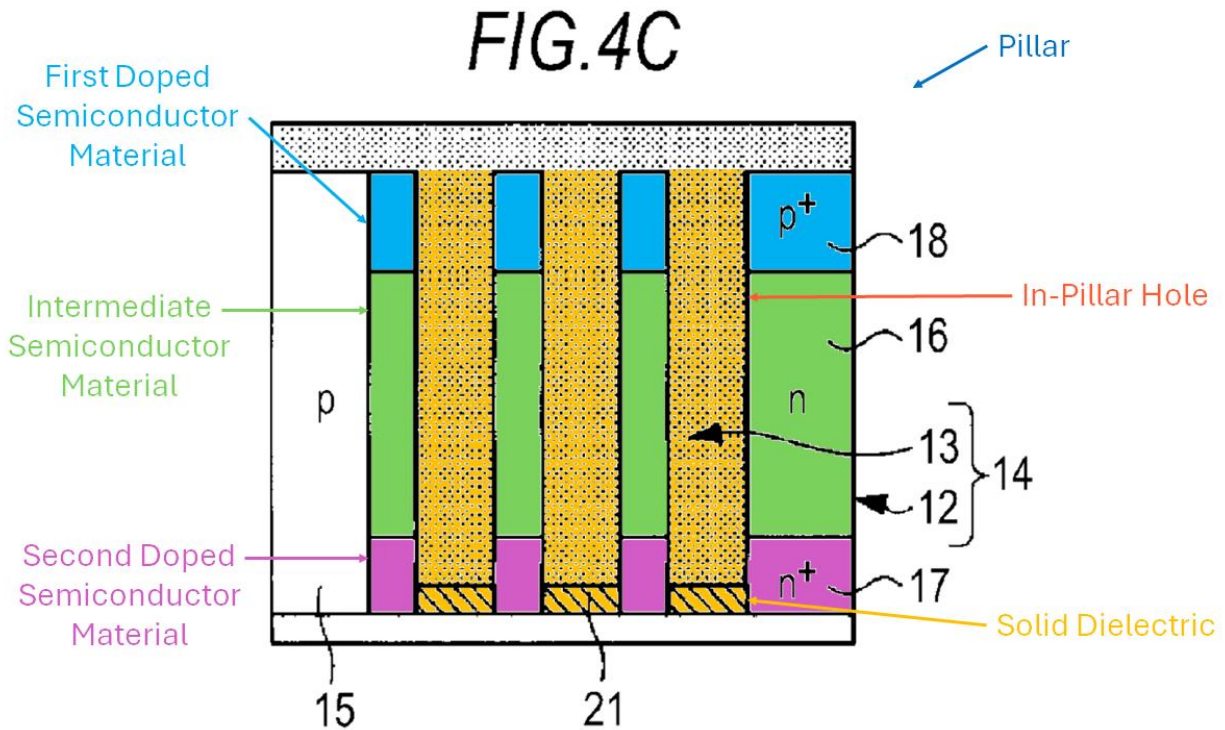
by an insulating film such as, for example, a silicon nitride (Si_3N_4) film [or] a silicon [oxide] (SiO_2) film.” *Kuboi*, ¶[73]. As I explained for claim [1b.1], one skilled in the art would have understood that silicon nitride (Si_3N_4) and silicon oxide (SiO_2) are solid dielectrics. *Supra* XI.A.1.c; Ex. 1020, 34-35; Ex. 1063, 20-21, 23, 30, 33.

158. *Kuboi* also discloses that an organic material is deposited to fill portions of the **holes**, thereby forming organic **photoelectric conversion films 13** embedded within the hole. *Kuboi*, ¶¶[73], [58], [85], Fig. 4C. *Kuboi* discloses that as the p-type organic material is sensitive to a visible light region, “perylene-based compounds, phthalocyanine compounds, quinacridone compounds, porphyrin compounds, merocyanine compounds, and the like can be used, for example.” *Kuboi*, ¶[58]. This is consistent with the description in the ’360 Patent indicating that its microstructured pillar and hole arrays can include “polymer, glass, oxides, nitrides, . . . organic conducting and non conducting polymers.” ’360 Patent, 49:67-50:5.

159. In my opinion, one skilled in the art would have understood that phthalocyanine compounds, perylene-based compounds, and porphyrin compounds function as dielectric materials. Various prior art references examine their dielectric properties and behavior in optoelectronic devices. For instance, Exhibit 1021 discusses the dielectric characteristics of phthalocyanine and perylene

compounds used in organic solar cells. Ex. 1021, 3, 17, 47, 52-56. Additionally, Exhibit 1022, 1-4, 7, explores the dielectric behavior of phthalocyanine compounds, noting that their dielectric constant decreases with increasing frequency and rises with increasing temperature. Exhibit 1034, 4-11, presents experimental studies on porphyrin as a dielectric material, while Exhibit 1035, 1-6, details dielectric investigations of porphyrin compounds used in optical devices. Exhibit 1036, 1-6, discusses the measurement of photocurrents generated by illuminating a porphyrin compound, alongside its dielectric property evaluations. Exhibit 1037, 2, explains that the dielectric properties of phthalocyanine compounds increase with temperature and decrease with frequency. Lastly, Exhibit 1038, 1-5, describes perylene compounds as organic dielectric materials with “high photoluminescence efficiency,” employed in solar cells.

160. Thus, both **electron blocking film 21** and **photoelectric conversion film 13** together entirely fill the **holes** of photoelectric conversion portion 14 and are dielectric materials. *Kuboi*’s deliberately formed **in-pillar holes** filled with **solid dielectric material** are illustrated below.



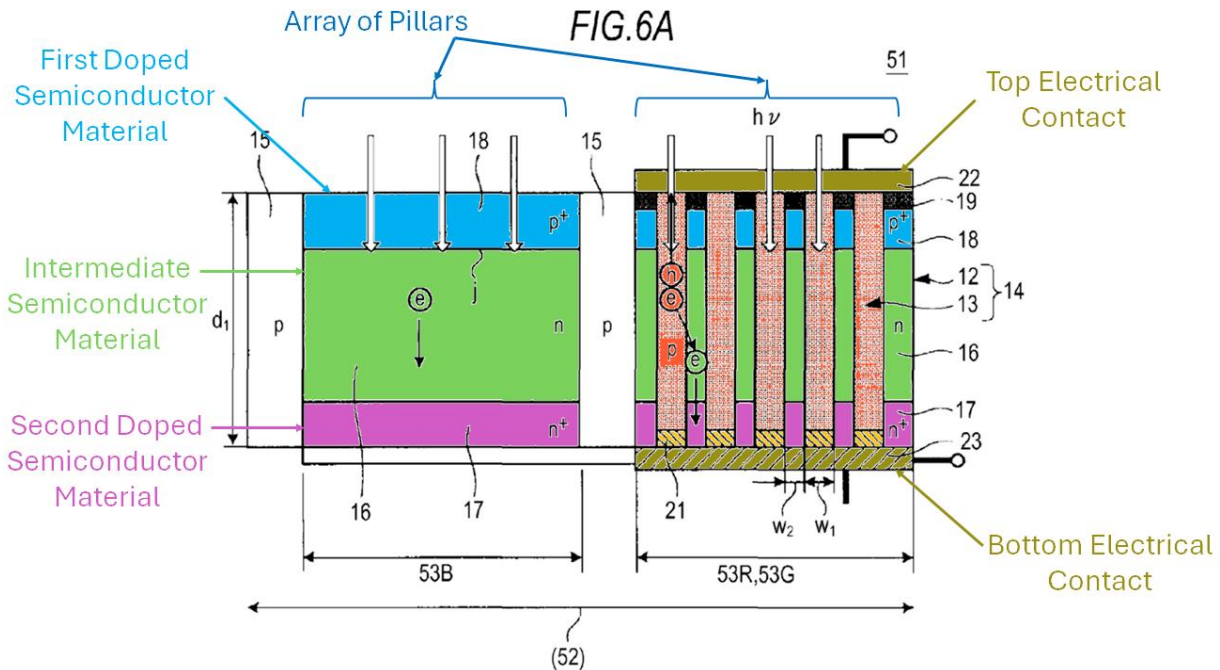
Kuboi, Fig. 4C.

- j. [1e]: “**top and bottom electrical contacts** electrically coupled with said **array of pillars**, wherein said **photodetector device** is configured to respond to **light photons** incident on said **array of pillars** by **photo-generated charge carriers** therein; and”

161. In my opinion, *Kuboi* discloses this limitation.

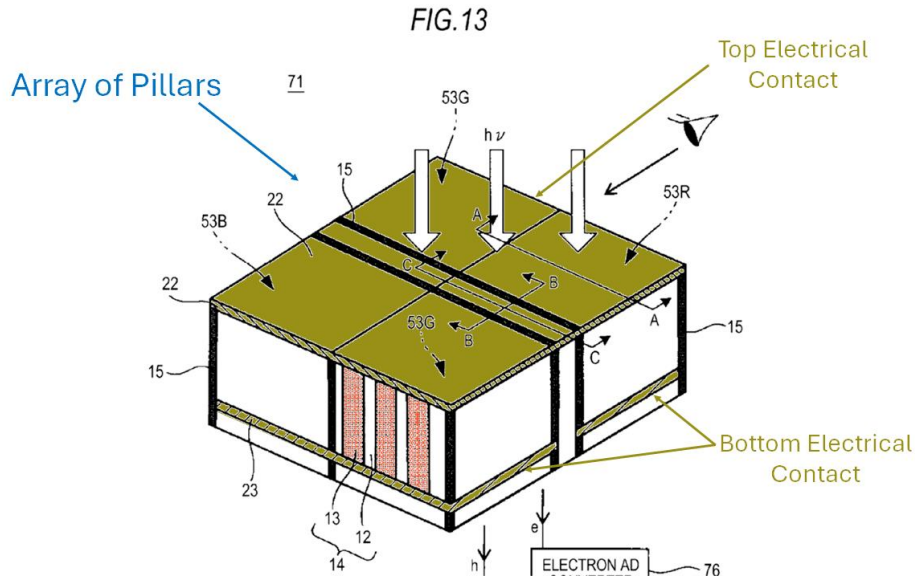
162. *Kuboi* discloses that a “pair of **electrodes 22 and 23** is formed on the entire rear and fro[nt] surfaces of the semiconductor layer 12.” *Kuboi*, ¶¶[60], [77], [93], [103]. *Kuboi* explains that “**upper electrode 22** on the rear surface side is formed by a transparent electrode formed of a transparent conductive film.” *Kuboi*, ¶[60]. *Kuboi* further explains that “**lower electrode 23** is formed of metal exhibiting

ohmic properties.” *Kuboi*, ¶[60]. *Kuboi*’s **electrodes** (i.e., “**electrical contacts**”) are illustrated in the figure below:



Kuboi, Fig. 6A.

163. *Kuboi*’s **electrodes** (i.e., “**electrical contacts**”) are also illustrated in the figure below, which shows a perspective view of *Kuboi*’s imaging device.

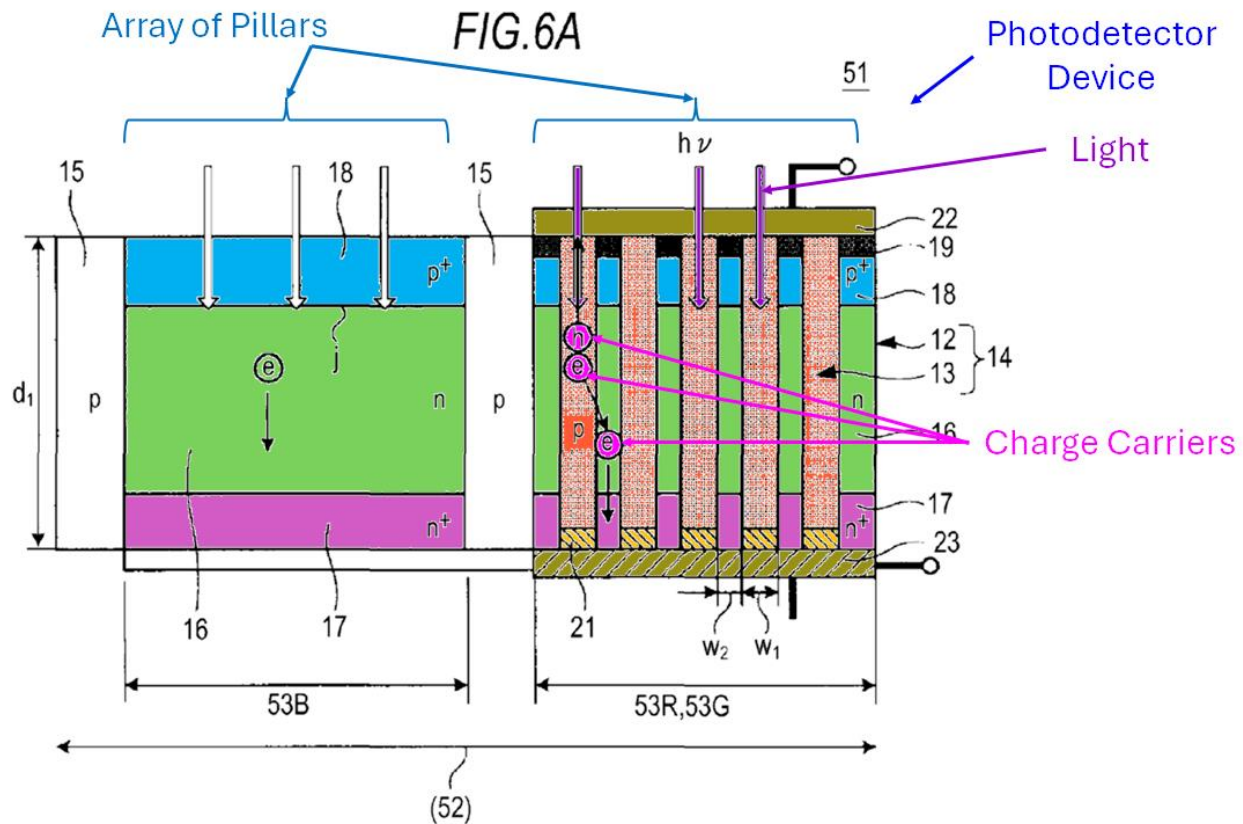


Kuboi, Fig. 13.

164. *Kuboi* discloses that pixel 11 “is configured to include a hybrid photoelectric conversion portion 14 and a plurality of pixel transistors.” *Kuboi*, ¶[55]. According to *Kuboi*, “hybrid photoelectric conversion portion 14 includes a semiconductor layer 12 formed of silicon and a plurality of organic material layers 13 embedded in the semiconductor layer 12.” *Kuboi*, ¶¶[55], [91], [181]. *Kuboi* discloses that “an organic photoelectric conversion film 13 is deposited so as to be embedded in the vertical holes 38.” *Kuboi*, ¶¶[73], [91]. *Kuboi* explains that “[l]ight hv passes through the on-chip microlens to enter the p-type organic photoelectric conversion film 13, in which the light is subjected to photoelectric conversion, whereby electron-hole pairs are generated.” *Kuboi*, ¶[64].

165. In my opinion, because the photoelectric conversion film generates **electron-hole pairs** when subjected to light, the charge carriers are photo-generated.

Furthermore, because the photoelectric conversion film 13 is embedded in **pixels** (i.e., **pillars**) of **imaging device** (i.e., **photodetector device**), *Kuboi's photodetector device* is configured to generate **electron-hole pairs** (i.e., **charge carriers**) when subjected to **light $h\nu$** (**light photons** incident on said **array of pillars**). *Kuboi*, ¶¶[107], [64]. The figure below illustrates generation of **charge carriers** in *Kuboi's photodetector device*.



Kuboi, Fig. 6A.

166. *Kuboi* also discloses that a “necessary voltage is applied between the upper electrode 22 and the lower electrode 23.” *Kuboi*, ¶[64]. *Kuboi* explains that **electrons e** from the electron-hole pairs “move from the organic photoelectric

conversion film 13 ... toward the semiconductor layer 12 depleted by the applied bias voltage.” *Kuboi*, ¶[64]. In my opinion, one skilled in the art would have understood that because the bias voltage applied by the upper electrode 22 and the lower electrode 23 depletes semiconductor layer 12, electrodes 22 and 23 (i.e., *Kuboi*’s electrical contacts) would be electrically coupled with semiconductor layer 12. Furthermore, because each pixel (i.e., pillar) of *Kuboi* includes semiconductor layer 12, electrodes 22 and 23 (i.e., *Kuboi*’s electrical contacts) would also be electrically coupled to *Kuboi*’s pixels (i.e., pillars).

167. As another example, *Kuboi* also discloses that “hole h moves toward the upper electrode 22 through the organic photoelectric conversion film 13 and is discharged through the upper electrode 22.” *Kuboi*, ¶[64]. Because the holes generated in *Kuboi*’s pixels (i.e., pillars) move through and are discharged by electrodes 22, electrodes 22 are electrically coupled with *Kuboi*’s array of pillars.

k. [1f]: “a base dielectric region that is below the array of pillars and comprises substantially solid dielectric material;”

168. In my opinion, *Kuboi* alone or in combination with *Shinohara* renders this limitation obvious.

169. *Kuboi* discloses a “CMOS solid-state imaging device” in which “pixel transistors constituting one pixel are formed in a semiconductor region 25 formed of silicon which is disposed on the front surface side of the semiconductor

layer 12, namely under the lower electrode 23 with an insulating film 30 disposed therebetween.” *Kuboi*, ¶¶[55], [61], [69]. *Kuboi* also discloses a semiconductor substrate on which the semiconductor region 25 having pixel transistors, the multilayer wiring layer 32, and the lower electrode 23 are formed. *Kuboi*, ¶[69]. *Kuboi* explains that multilayer wiring layer 32 includes a plurality of layers of wiring with an interlayer insulating film 31 disposed therebetween. *Kuboi*, ¶[62]. In my opinion, insulating film 30 and/or insulating interlayer film 31 constitutes the claimed base dielectric region because they are located below *Kuboi*’s pixels (i.e., pillars).

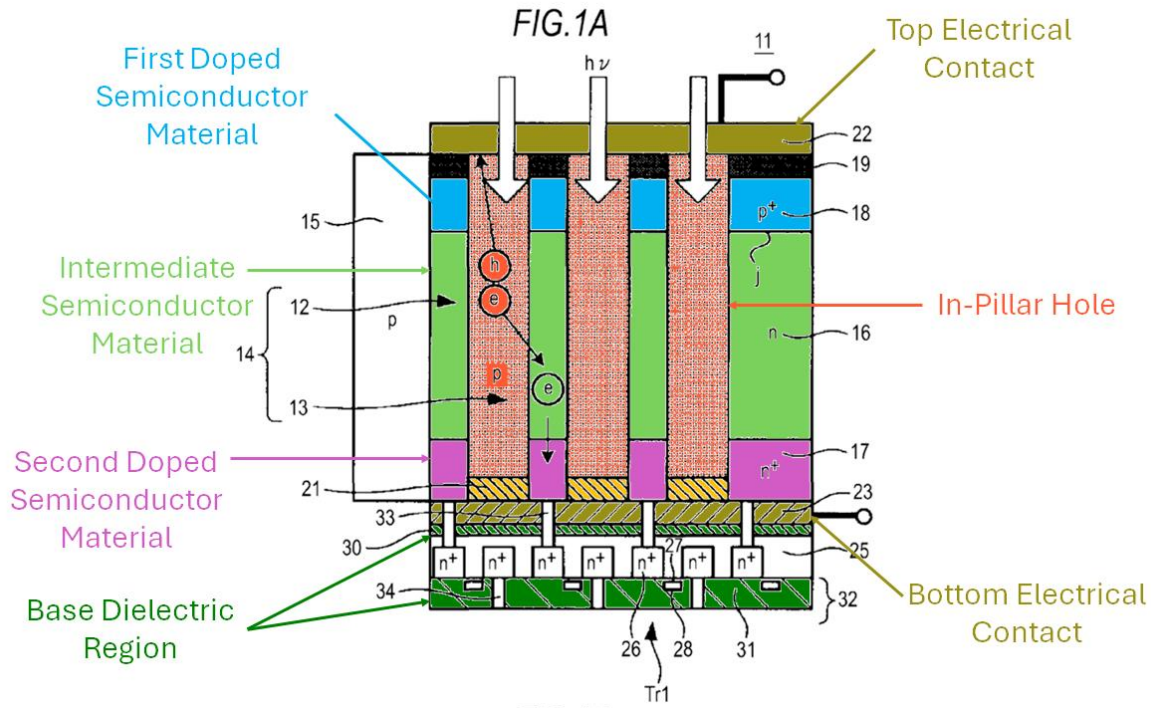
170. *Kuboi* does not disclose the material for its insulating films 30 or 31. In my opinion, one skilled in the art would have understood that *Kuboi*’s insulating film 30 that insulates lower electrode 23 from the pixel transistors and is part of a CMOS device would constitute a film of silicon oxide or silicon nitride, or at least would have found this configuration obvious, there being a motivation for it and a reasonable expectation of success in achieving it. This is because silicon oxide or silicon nitride films can be fabricated using standard silicon fabrication processes. Ex. 1063, 20 (stating that “thermal oxidation . . . is a key process in modern silicon integrated-circuit technology.”). Moreover, silicon oxide or silicon nitride provide good barriers to impurity and moisture diffusion. Ex. 1063, 4 (“[A]n oxide layer can prevent most impurity atoms from diffusing through it.”), 5, 34 (“The plasma-

deposited nitride provides excellent scratch protection, serves as a moisture barrier, and prevents sodium diffusion.”).

171. Similarly, one skilled in the art would have understood that *Kuboi*’s interlayer **insulating film 31** that insulates wiring layers from each other would constitute a film of silicon oxide or silicon nitride, or at least would have found this configuration obvious, there being a motivation for it and a reasonable expectation of success in achieving it. This is supported by other prior art that would have been known to one skilled in the art. Ex. 1059, ¶¶[13], [14] (disclosing “a method of manufacturing a CMOS device” in which “first insulating film 102 may be composed of silicon oxide film (SiO_2) or an aluminum oxide film”); Ex. 1020, 34 (“Classically, silicon dioxide (generically called oxide here) has served as the insulating dielectric.”); Ex. 1020, 35 (disclosing silicon nitride as “an insulator”); Ex. 1060, 26:9-14 (disclosing that “it is preferable that the material of the interlayer insulating film used for the multi-layer wiring of the lower layer is used so as to form the film, from the viewpoint of reliability and manufacturing cost” and that “silicon oxide, silicon nitride, silicon nitride oxide or laminated films thereof are generally used”); Ex. 1063, 20 (disclosing that many different kinds of thin films, including thermal oxides, are used to fabricated discrete devices and integrated circuits), 34 (“The plasma-deposited nitride provides excellent scratch protection, serves as a moisture barrier, and prevents sodium

diffusion.”). One skilled in the art would have also understood that both silicon dioxide and silicon nitride are dielectric or insulating materials. Ex. 1063, 20 (“Dielectric layers such as silicon dioxide and silicon nitride are used for insulation between conducting layers.”).

172. As I also explained above, in my opinion, one skilled in the art would have further understood that *Kuboi*’s insulating films 30 or 31 made of silicon dioxide or silicon nitride would be made of solid material. *Supra* XI.A.1.c; Ex. 1063, 20-21, 23, 30, 33; Ex. 1020, 34-35. In my opinion, therefore, a skilled artisan would have understood that *Kuboi*’s insulating films 30 or 31 are formed of a solid dielectric material (e.g., amorphous silicon dioxide. *Kuboi*’s insulating films 30 and/or 31 (i.e., base dielectric region) disposed below *Kuboi*’s pixel (i.e., pillar) is illustrated below:

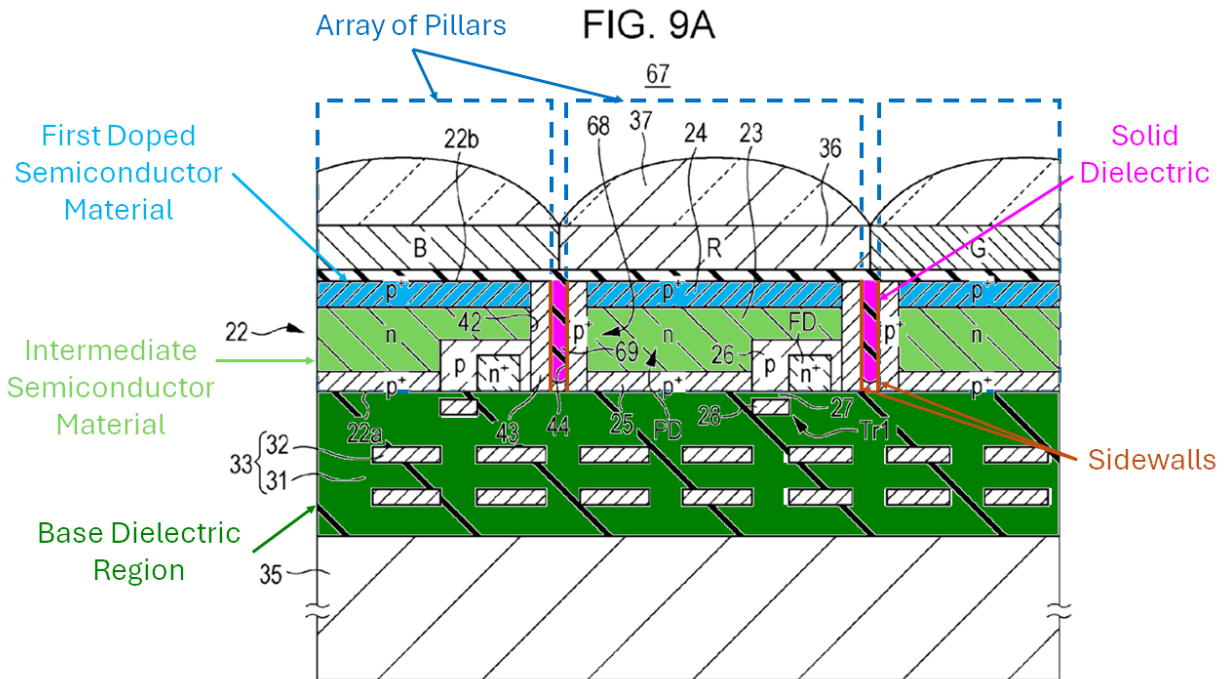


Kuboi, Fig. 1A.

173. Although Figure 1A illustrates only one pixel, as discussed for claim [1a], *Kuboi*'s imaging device includes a plurality of pixels (i.e., 53R and 53G) arranged as an array of pixels. *Supra* XI.A.1.b. *Kuboi* discloses that pixels 53R and 53G have structures similar to the Figure 1A pixel. *Kuboi* ¶[90]. In my opinion, therefore, Figure 1A's base dielectric region is a base dielectric region for *Kuboi*'s array of pixels.

174. In my opinion, *Shinohara* also discloses "a base dielectric region that is below the array of pillars and comprises substantially solid dielectric material," as claimed. For example, *Shinohara* discloses a CMOS solid-state imaging device. *Shinohara*, Abstract, ¶¶[51], [90]. With respect to its CMOS solid-state imaging

device, *Shinohara* discloses forming multilayer wiring layer 33, including wires 32 and interlayer insulating film 31, on the same substrate 22 on which pixels B, R, G are formed. *Shinohara*, ¶[82]; *see also Shinohara*, ¶¶[68]-[89]. As I discussed above, in my opinion, one skilled in the art would have understood that an interlayer insulating film 31 in *Shinohara*'s CMOS solid-state device would be made of materials such as silicon oxide or silicon nitride. Ex. 1020, 24-25; Ex. 1059, ¶¶[13], [14]; Ex. 1060, 26:9-14; Ex. 1063, 4-5. In my opinion, as I discussed above, a skilled artisan would have understood that *Shinohara*'s insulating film 31 made of silicon oxide or nitride would be a solid material. *Supra* XI.A.1.c; Ex. 1063, 20-21, 23, 30, 33; Ex. 1020, 34-35. *Shinohara*'s **base dielectric region** disposed below *Shinohara*'s **array of pillars** is illustrated below.



Shinohara, Fig. 9A.

175. As I explain below for claim [1i], one skilled in the art would have found it obvious to modify *Kuboi* in view of *Shinohara*, resulting in an imaging device (*Kuboi-Shinohara* device²) in which the array of pillars (i.e., pixel region) is monolithically integrated with electronic circuits that include active elements for signal processing and transmission. *Infra* XI.A.1.n. In my opinion, one skilled in the art would have also understood that because the wiring layer of the

² I refer to *Kuboi*'s imaging device modified using one or more of *Shinohara*'s teachings as the *Kuboi-Shinohara* device in this declaration.

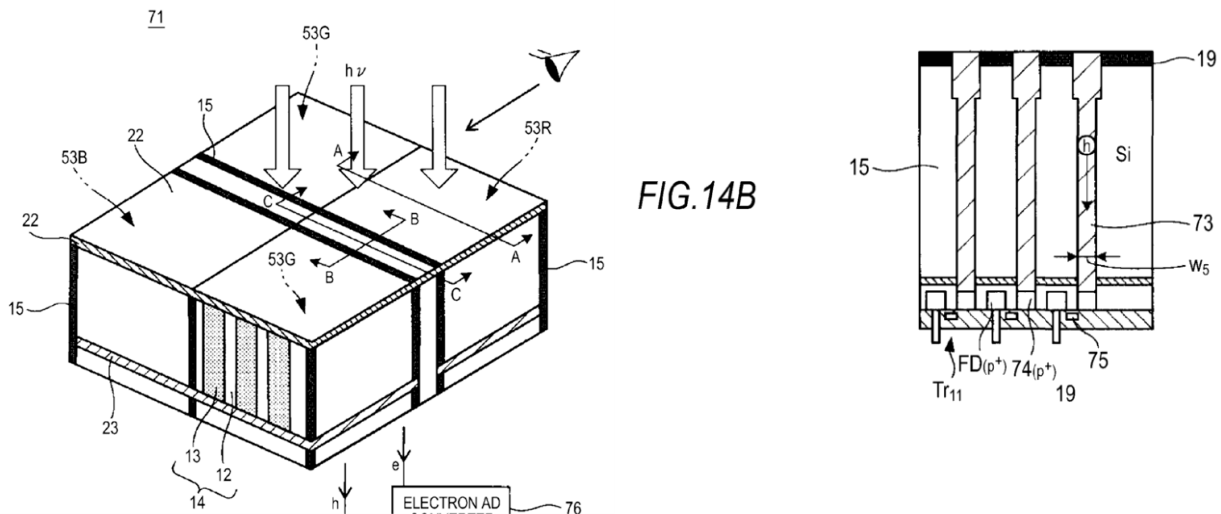
Kuboi-Shinohara device would include the **base dielectric region**, monolithically integrating *Kuboi*'s **pixels**, electronic circuits, and active elements, as taught by *Shinohara*, would have resulted in a wiring layer having a **base dielectric region** (i.e. **insulating film 30 and/or 31**) disposed below the **array of pillars** in the *Kuboi-Shinohara* device. Further, in my opinion, a skilled artisan would have had a reasonable expectation of success in obtaining a **base dielectric region** in the *Kuboi-Shinohara* device. This is because *Shinohara* already discloses a method of forming a monolithically integrated imaging device having a **base dielectric region** (**insulating film 30**) disposed below the **array of pillars**. *Shinohara*, Fig. 9A.

- I. **[1g]: “wherein the **pillars** of said **array of pillars**: are laterally spaced center to center by no more than 10,000 nanometers; and have up-down lengths of said **intermediate semiconductor material** in the range of 100-5000 nanometers;”**

176. In my opinion, *Kuboi* renders this limitation obvious.

177. As I explained for claim [1a], *Kuboi*'s **pixels 11** constitute the claimed **pillars** forming the **array of pillars**. *Supra* XI.A.1.b. *Kuboi* also discloses that Figures 6A/6B “show a solid-state imaging device.” *Kuboi*, ¶[90]. *Kuboi* explains that “a blue (B) pixel 53B, a red (R) pixel 53R, a green (G) pixel 53G, and a green (G) pixel 53G are arranged in a two-dimensional array.” *Kuboi*, ¶[90]. Further, *Kuboi* discloses that, “[i]n the present embodiment, one pixel has an area of 1.4 μm by 1.4 μm .” *Kuboi*, ¶[94]. *Kuboi* also discloses that “FIG. 13 is a perspective view

FIG. 14B

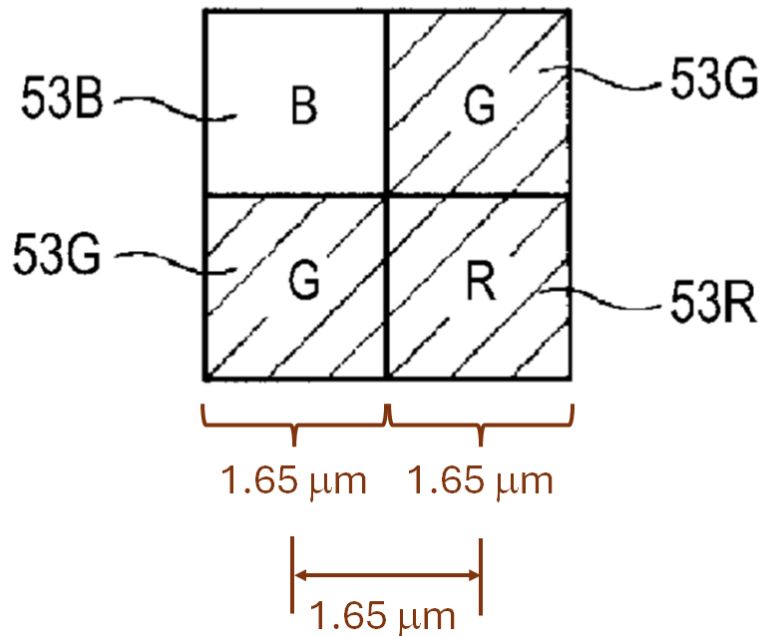


Kuboi, Figs. 13, 14B.

178. Referencing Figure 14B, *Kuboi* explains that “in the element separation region 15 between the pixels neighboring each other in the vertical direction of the pixel region, wiring layers 73 are formed so as to be provided for the movement of holes h of the electron-hole pairs.” *Kuboi*, ¶[182]. In my opinion, one skilled in the art reading *Kuboi*’s disclosure would have understood from Figure 14B that the wiring layers are formed in the element separation region 15 between *Kuboi*’s pixels. See *Kuboi*, Fig. 13 (illustrating that cross-section B-B cuts across element separation region 15). *Kuboi* already discloses forming the wiring

layers in the p-type semiconductor layer in the element separation region. *Kuboi*, Fig. 14B, ¶[182]. As I also discussed, *Shinohara* discloses forming wiring layers in an insulating film. *Shinohara*, ¶[82], Fig. 9A; *supra* XI.A.1.k. Therefore, in my opinion, one skilled in the art would have understood that it would be possible to form the wiring layers 73 in the *Kuboi-Shinohara* device that includes *Shinohara*'s dielectric region disposed in *Kuboi*'s element separation region 15 (*infra* XI.A.1.c, claim [1b.1]). Further, in my opinion, one skilled in the art would have understood that such wiring layers would pass through the dielectric region in the *Kuboi-Shinohara* device, or would pass through portions of *Kuboi*'s p-type element separation region disposed on either side of the dielectric region in the *Kuboi-Shinohara* device.

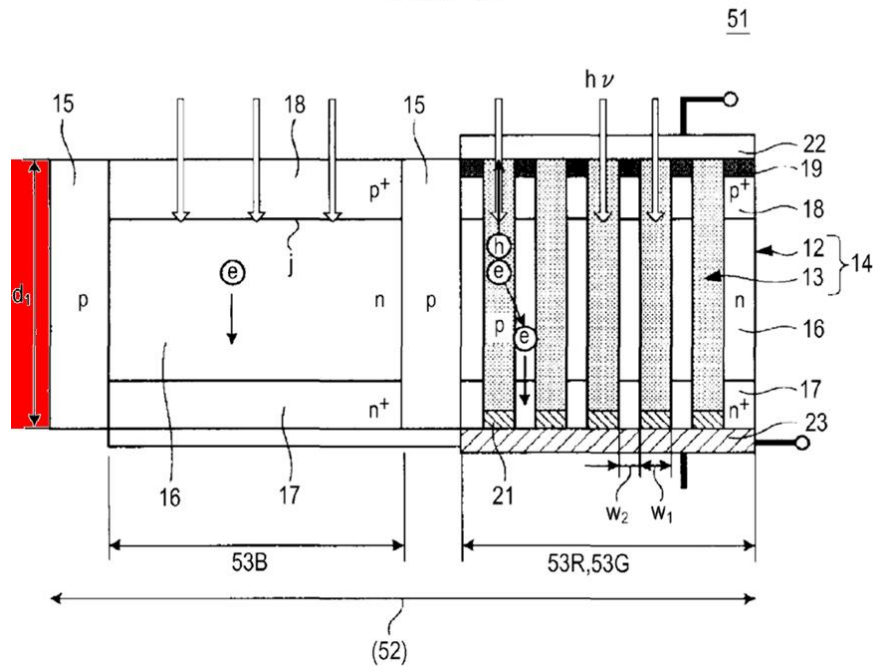
179. *Kuboi* further explains that “[t]he pixel including the wiring layer has an area of 1.65 μm by 1.65 μm .” *Kuboi*, ¶[185]. In my opinion, one skilled in the art would have understood this disclosure to mean that *Kuboi*'s pixel including the element separation region 15 with the wiring layers 73 has a width of 1.65 μm . As illustrated in the figure below, because adjoining pixels (i.e., pillars) of *Kuboi* each have a width of 1.65 μm , the pitch or center-to-center distance between adjacently abutting pillars would also be 1.65 μm .

FIG. 6B*Kuboi*, Fig. 6B.

180. A center-to-center distance of 1.65 μm (or 1650 nm) is “no more than 10,000 nanometers,” as claimed. In my opinion, therefore, *Kuboi* discloses or at least suggests that the **pillars** of *Kuboi*’s **array of pillars** are laterally spaced center to center by no more than 10,000 nanometers.

181. *Kuboi* also discloses that thickness **d₁** of the semiconductor layer 12 “is set to about 1.4 μm.” *Kuboi*, ¶[94]. Thickness **d₁** of *Kuboi*’s **pixels** (i.e., **pillars**) is illustrated below:

FIG. 6A



Kuboi, Fig. 6A.

182. As illustrated in the above figure, **region 16** occupies a portion of thickness **d₁**. Therefore, in my opinion, one skilled in the art would have understood that the up-down length of **region 16** (i.e., **intermediate semiconductor material**) would be less than 1400 nanometers to accommodate regions 17 and 18 within the thickness **d₁**. In my opinion, one skilled in the art would have also understood that because *Kuboi*'s substrate includes **region 16** (e.g., *Kuboi*, ¶[71]), the thickness of **region 16** would be greater than 0 nm. A skilled artisan would, therefore, have understood that **region 16** would have a thickness ranging between some number greater than 0 nm and a number less than 1400 nm.

183. One skilled in the art would have also understood that the intrinsic layer thickness in a PiN diode should be sized sufficiently large to maximize the absorption of photons. Ex. 1063, 17 (“The p-i-n structure is designed so that almost complete optical absorption occurs over the i-layer.”). Moreover, one skilled in the art would have understood that although a thinner intrinsic layer improves response time, it is desirable to make the intrinsic layer thicker to maximize the quantity of absorbed photons. Ex. 1063, 17. In my opinion, therefore, one skilled in the art would have found it obvious that *Kuboi*’s region 16 (i.e., intermediate semiconductor material) would have occupied a majority of the 1400 nm thickness of *Kuboi*’s pixel. Thus, a skilled artisan would have found it obvious that the thickness of *Kuboi*’s region 16 (i.e., intermediate semiconductor material) would have fallen within the claimed 100 to 5000 nm thickness range. One skilled in the art would have had a reasonable expectation of success in forming *Kuboi*’s region 16 in this manner because *Kuboi* already discloses a method of forming a pixel having three differently doped regions in a substrate of thickness of 1400 nm.

184. Further, in my opinion, although *Kuboi*’s figures are not to scale, one skilled in the art would have understood from Fig. 6A that *Kuboi*’s n-doped layer (i.e., *Kuboi*’s intermediate semiconductor material) would occupy about 50% if not more of the thickness d_1 . Thus, a skilled artisan would have understood *Kuboi*’s

intermediate semiconductor material to have a thickness of around 700 nm, which falls within the claimed range of 100-5000 nm.

185. I note that at a minimum, *Kuboi*'s disclosed thickness range of between 0 and 1400 nanometer for its intermediate semiconductor material overlaps with the claimed range of 100-5000 nanometers. I also note that *Kuboi*'s imaging device formed with an intermediate semiconductor material having a thickness selected between 100 to 1400 nanometers would satisfy the claimed thickness range. In my opinion, one skilled in the art would not have considered a thickness less than 100 nanometers for the intermediate semiconductor material because a photodetector with smaller than 100 nanometers intermediate semiconductor material thickness would have a slow response time. One skilled in the art would have understood that faster response times for *Kuboi*'s photodetectors would be desirable to improve the performance of *Kuboi*'s imaging device.

186. Moreover, the '360 Patent fails to disclose that the claimed range is critical to the claimed photodetector device's operation. Therefore, because of the substantial overlap in the thickness range disclosed by *Kuboi* and the claimed thickness range, in my opinion, *Kuboi* renders the claimed thickness range 100 to 5000 nanometers obvious. Further, in my opinion, one skilled in the art would have a reasonable expectation of success in forming *Kuboi*'s device with an intermediate

semiconductor material having a thickness in the 100 to 5000 nanometers range because *Kuboi* already discloses an imaging device that can have an intermediate semiconductor material thickness in the 100 to 1400 nanometer range.

- m. [1h]: “wherein at least said pillars, in-pillar holes, and solid dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars increase photon absorption of said device of incident light by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said one or more in-pillar holes;”

187. In my opinion, *Kuboi* discloses or at least renders this limitation obvious in view of the knowledge of a person of ordinary skill in the art.

188. First, a skilled artisan would have found claim [1h] disclosed in view of the skilled artisan’s knowledge of the state of the art before the priority date of the ’360 Patent. In my opinion, the skilled artisan would have understood that the intensity I_d of light at a depth “d” in a material is governed by the Lambert-Beer expression $I_d = I_0 e^{-\alpha d}$, where I_0 is the intensity of incident light and α is the absorption coefficient of the material. Ex. 1070, 23. A skilled artisan would have also understood that the amount of incident light entering a material would be $I_0 \times A$, where A is the cross-sectional area available for light to enter the material (i.e., area of light incidence). Ex. 1070, 25. Further, the skilled artisan would have understood that the amount of light exiting the material of depth d would be $(I_0 e^{-\alpha d}) \times A$. Ex. 1070, 25. A skilled artisan would, therefore, have understood that the

amount of incident light absorbed by a material of depth d (P_{abs}) would be

$I_0 (1 - e^{-\alpha d}) \times A$, based on the Lambert-Beer expression. Ex. 1070, 23-25.

189. *Kuboi* discloses that the organic photoelectric conversion film 13 in the red pixel 53R which is sensitive to the red light wavelength band can include “phthalocyanine compounds.” *Kuboi*, ¶[92]. Red light wavelengths range between about 620 to 750 nm. *Yu*, ¶[23]. Further, *Kuboi* discloses that the organic photoelectric conversion film 13 in the green pixel 53G which is sensitive to the green light wavelength band can include “porphyrin compounds.” *Kuboi*, ¶[92]. Green light wavelengths range between about 495 to 570 nm. *Yu*, ¶[23]. *Kuboi* also discloses “the organic photoelectric conversion film has a greater optical absorption coefficient than silicon.” *Kuboi*, ¶[4], [12], [92]. As I explain below, the higher absorption coefficient of *Kuboi*’s organic photoelectric conversion film provides a greater than 10% increase in light absorption over a comparable device that does not include in-pillar holes.

190. Ex. 1068 provides a graph showing the absorption coefficients for phthalocyanine compounds (i.e., organic compounds in *Kuboi*’s red pixels) over a range of wavelengths. Ex. 1068, 3, Fig. 1. Ex. 1071 similarly provides a graph showing the absorption coefficients for porphyrin compounds (i.e., organic compounds in *Kuboi*’s green pixels) over a range of wavelengths. Ex. 1071, 7, Fig. 6. I have reproduced these graphs below.

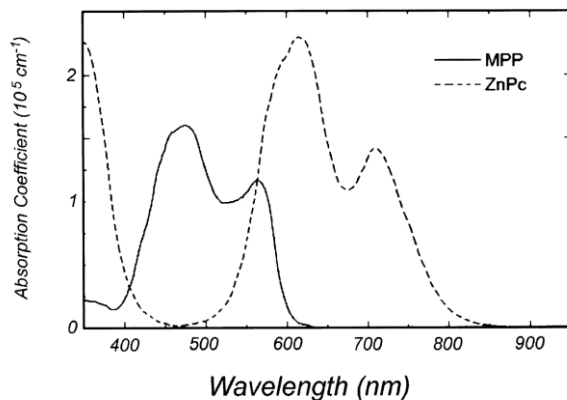


Fig. 1. The absorption spectra of ZnPc (dashed line) and MPP (solid line).

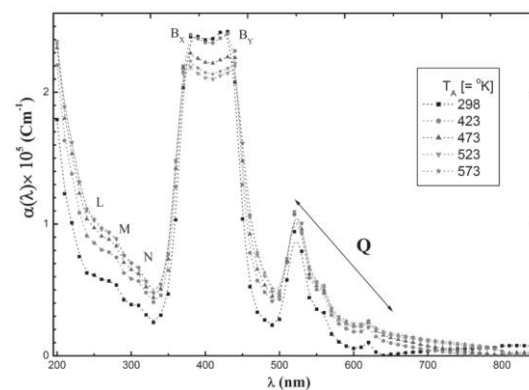


Fig. 6. (Color online) The optical absorption coefficient, $\alpha(\lambda)$, versus wavelength, λ , for as-deposited and annealed NiTPP thin films.

Ex. 1068, 3.

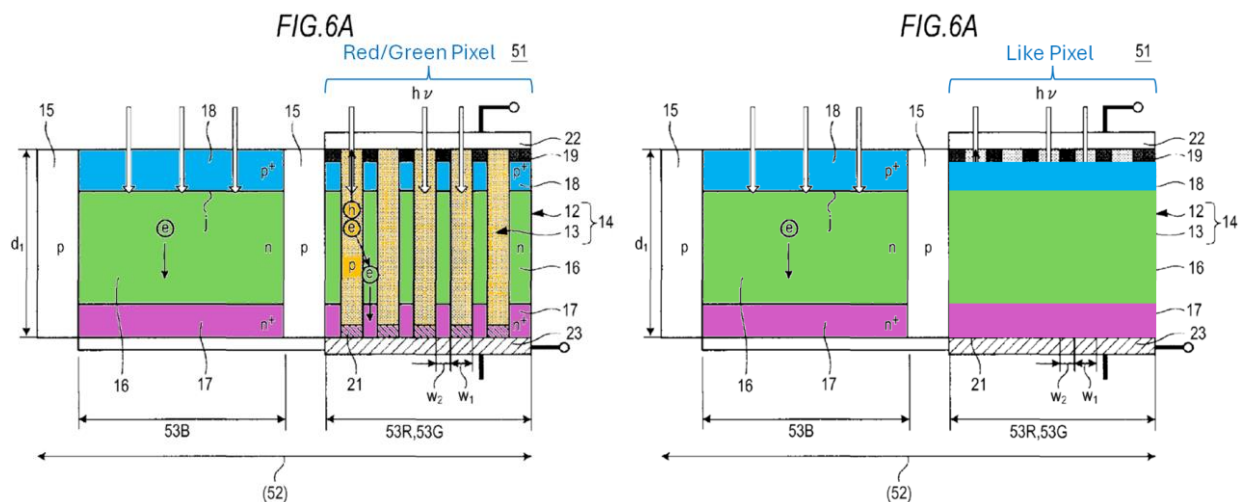
Ex. 1071, 5.

191. Ex. 1069 provides a table of the absorption coefficients of silicon. In Table A below, I have listed the absorption coefficients for the phthalocyanine and porphyrin organic materials which I extracted from the above figures and compared them with the absorption coefficient for silicon for the green and red light wavelength ranges. As seen from the table below, the absorption coefficient of the porphyrin organic materials is greater than silicon in the green light wavelength range of 510 to 580 nm. Similarly, the absorption coefficient of the phthalocyanine organic materials is at least ten times greater than silicon for the red light wavelength range of 620 to 750 nm.

Table A			
Wavelength (nm)	Absorption coefficient α (cm⁻¹)		
	Silicon (Ex. 1068)	Porphyrin (Ex. 1071)	Phthalocyanine (Ex. 1068)
490	12600	22000	
500	11100	27000	
510	9700	57600	
520	8800	93400	
530	7850	79000	
540	7050	44000	
550	6390	35000	
560	5780	31400	
570	5320	15800	
580	4880	10000	
620	3520		228000
630	3280		216000
640	3030		188000
650	2790		147000
660	2570		122000
670	2390		111000
680	2200		110000
690	2040		120000
700	1890		133000
710	1780		142000
720	1680		135000
730	1540		119600
740	1420		101000
750	1310		83000

192. Claim [1h] recites an “increase [in] photon absorption of said device of incident light by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a *like* device lacking said one or more in-

pillar holes” (emphases added). Below I have illustrated the structure of *Kuboi*’s red or green pixels 53R or 53G (left) and the structure of a *like* pixel (right) that does not have the in-pillar holes. As is apparent from the below figures, the *like* pixel would include silicon in place of the organic film in pixel portions corresponding to the *Kuboi*’s in-pillar holes. Further, as illustrated in the figures below, both *Kuboi*’s 53R or 53G pixel and the *like* pixel include *Kuboi*’s light shielding film 19. Thus, light is incident over the same area, defined by the openings in the light shielding film, at the light-receiving surface for both cases.

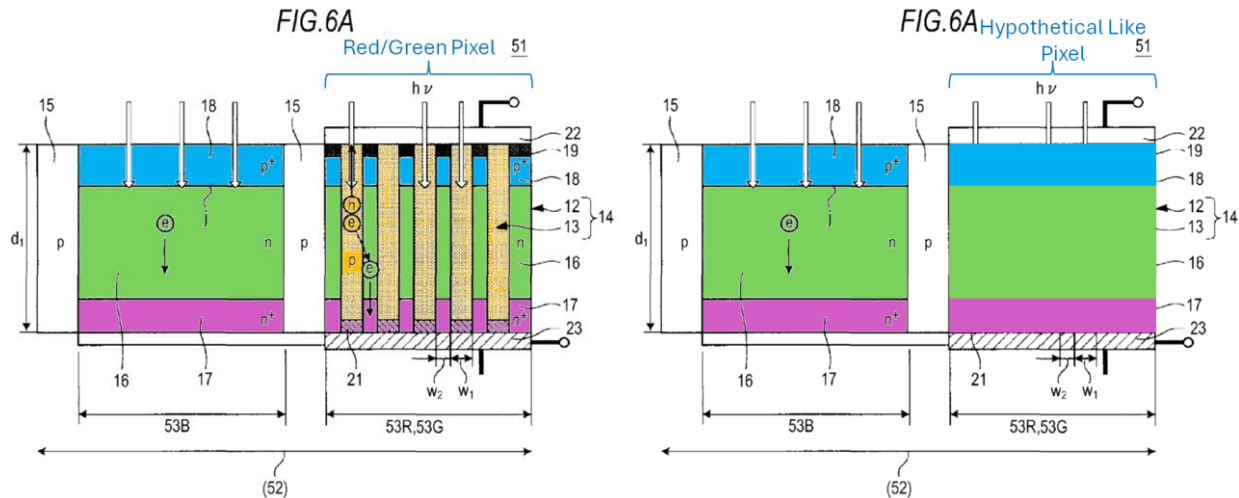


Kuboi, Fig. 6A (53R/53G pixel with organic material in the in-pillar holes)

Kuboi, Fig. 6A (*Like* pixel without in-pillar holes)

193. It is instructive to also consider a configuration in which a *hypothetical like* pixel does not include the in-pillar holes and the light shielding film. Below I have illustrated the structure of *Kuboi*’s red or green pixels 53R or

53G (left) and the structure of the *hypothetical like* pixel (right) that does not have the in-pillar holes and also does not include the light shielding film.



Kuboi, Fig. 6A (53R/53G pixel with organic material in the in-pillar holes)

Kuboi, Fig. 6A (Hypothetical pixel without in-pillar holes and no light shield)

194. As I discussed above, *Kuboi* discloses a hole width of 200 nm, at least five in-pillar holes in its red and green pixels, and a 1.4 μm by 1.4 μm pixel area. *Supra* XI.A.1.1; *Kuboi*, ¶[94]. Thus, the area of the organic film on which light is incident in *Kuboi*'s red or green pixels (53R or 53G), as defined by the openings in the light shielding film, is about 1.4 μm^2 (i.e., $5 \times 0.2 \mu\text{m} \times 1.4 \mu\text{m}$). In contrast, the area on which light would be incident on a *hypothetical like* pixel that does not have the light shielding film is about 1.96 μm^2 (i.e., $1.4 \mu\text{m} \times 1.4 \mu\text{m}$). Thus, the

area on which light is incident in *Kuboi*'s green and red pixels is about 71% of the total pixel area over which light is incident on the *hypothetical light* pixel.

195. As I discussed above, *Kuboi* discloses in-pillar holes filled with the organic material and having a depth of 1.4 μm . *Supra* XI.A.1.1; *Kuboi*, ¶[94].

Table B below shows the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for a *like* pixel (second column) for the green light wavelength range of 490-580 nm. In the table, $P_{\text{abs-organic}}$ is the amount of light absorbed in porphyrin organic material (for green pixel 53G), $P_{\text{abs-silicon}}$ is the amount of light absorbed by a *like* pixel having no in-pillar holes, and both $P_{\text{abs-organic}}$ and $P_{\text{abs-silicon}}$ are obtained using the Lambert-Beer expression. The ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for the *hypothetical like* pixel (Table B, third column) is obtained by scaling the values of $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for the *like* pixel (Table B, second column) by 71% to account for the smaller area of light incidence on the organic material in the green pixel as compared to the area of light incidence on the *hypothetical like* pixel.

Table B		
Wavelength (nm)	$P_{\text{abs-organic}} / P_{\text{abs-silicon}}$	
	<i>Like Pixel</i>	<i>Hypothetical Like Pixel (without light shielding film)</i>
490	1.2	0.8
500	1.2	0.9
510	1.3	1.0
520	1.4	1.0
530	1.5	1.1
540	1.6	1.1
550	1.7	1.2
560	1.8	1.3
570	1.7	1.2
580	1.5	1.1

196. The ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ in Table B is illustrated in chart form in Figure A below. As illustrated in Figure A, the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ is greater than or equal to 1.1 (shown by the dashed black line) for the entire green light wavelength range for the *like* pixel. That is, the amount of light absorbed by *Kuboi's* green pixel with in-pillar holes filled with porphyrin organic material is at least 1.1 times that absorbed by a *like* pixel without in-pillar holes. Furthermore, the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ is greater than or equal to 1.1 (shown by the dashed black line) for the 540-570 nm wavelength range for the *hypothetical like* pixel.

That is, the amount of light absorbed by *Kuboi's* green pixel with in-pillar holes filled with porphyrin organic material is at least 1.1 times that absorbed by a *hypothetical like* pixel without in-pillar holes and without the light shielding film for the 540-570 nm wavelength range.

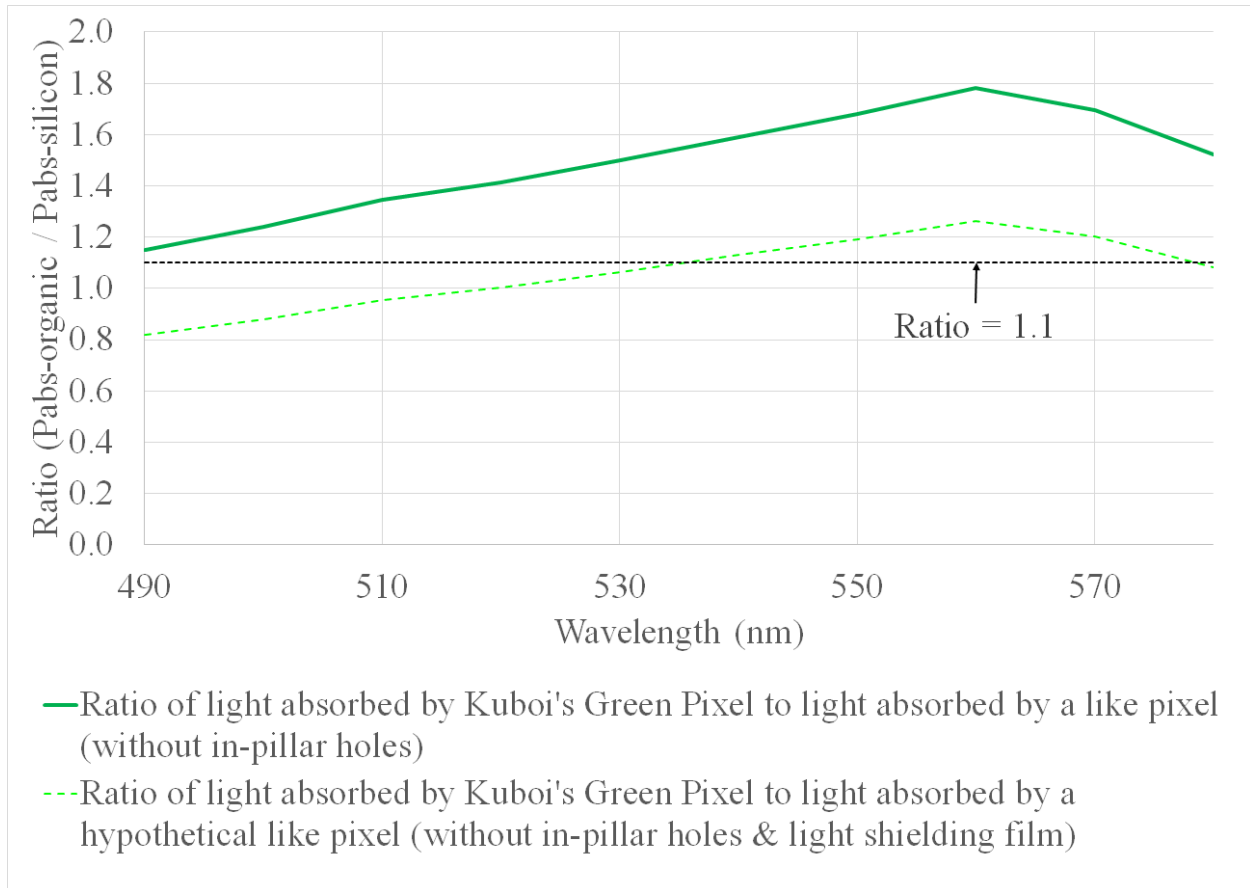


Figure A

197. Table C below shows the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for a *like* pixel (second column) for the red light wavelength range of 620-780 nm. In the table, $P_{\text{abs-organic}}$ is the amount of light absorbed in phthalocyanine organic material (for red pixel 53R) and is obtained using the Lambert-Beer expression. The ratio

$P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for the *hypothetical like* pixel (Table C, third column) is obtained by scaling the values of $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for the *like* pixel (Table C, second column) by 71% to account for the smaller area of light incidence on the organic material in the red pixel as compared to the area of light incidence on the hypothetical pixel.

Table C		
Wavelength (nm)	$P_{\text{abs-organic}} / P_{\text{abs-silicon}}$	
	<i>Like Pixel</i>	<i>Hypothetical Like Pixel</i> (without light shielding film)
620	2.6	1.8
630	2.7	1.9
640	2.9	2.1
650	3.1	2.2
660	3.3	2.3
670	3.5	2.5
680	3.8	2.7
690	4.0	2.9
700	4.3	3.1
710	4.5	3.2
720	4.8	3.4
730	5.2	3.7
740	5.5	3.9
750	6.0	4.2
760	6.5	4.6
770	7.0	5.0
780	7.4	5.2

198. The ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ in Table C for the *like* pixel is illustrated in chart form in Figure B below. As illustrated in Figure B (and in Table C, column two), the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ is greater than or equal to 1.1 (shown by the

dashed black line) for the entire red light wavelength range for the *like* pixel. That is, the amount of light absorbed by *Kuboi's* red pixel with in-pillar holes filled with phthalocyanine organic material is at least 1.1 times that absorbed by a *like* pixel without in-pillar holes. Furthermore, the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ is greater than or equal to 1.1 (shown by the dashed black line) for the entire red light wavelength range for the *hypothetical like* pixel. That is, the amount of light absorbed by *Kuboi's* red pixel with in-pillar holes filled with phthalocyanine organic material is at least 1.1 times that absorbed by a *hypothetical like* pixel without in-pillar holes and without the light shielding film.

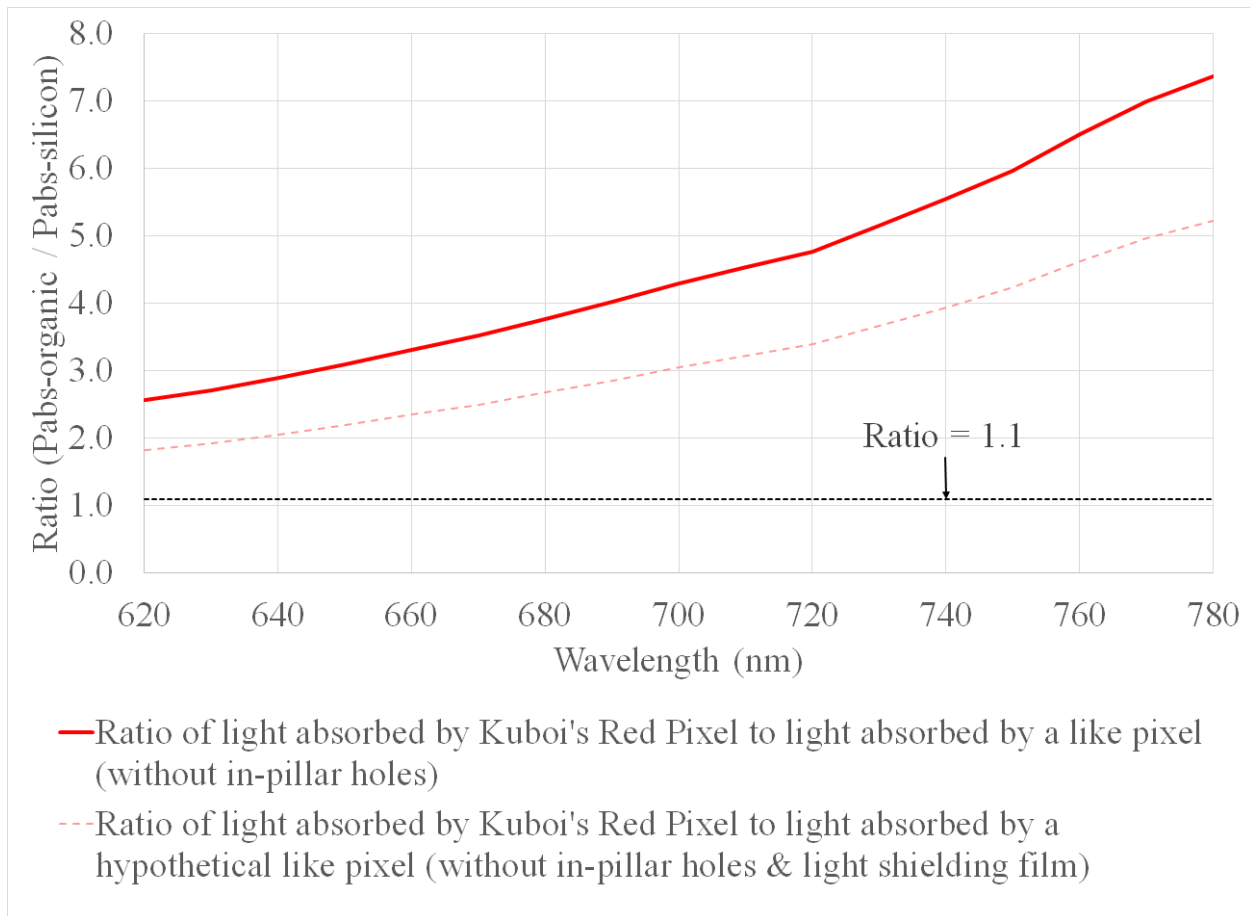


Figure B.

199. In my opinion, therefore, one skilled in the art would have understood that *Kuboi's* photodetectors with organic material in its in-pillar holes would increase photon absorption in *Kuboi's* device by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a *like* device lacking said one or more in-pillar holes.

200. Second, in my opinion, a POSITA would have also found [1h] disclosed based on Patent Owner's statements in the '360 Patent. The Patent

Owner represents in the '360 Patent that an imaging device having the structure disclosed in *Kuboi* would improve photon absorption by at least 10%.

201. The '360 Patent details the cause or causes of the enhancement of the absorption coefficient. Specifically, the '360 Patent explains:

The cause or causes of the enhancement of the absorption coefficient are believed to include one or more of the following: an increase in optical field concentration, resonance effects, constructive and destructive optical interferences (amplitude and phase) effects, scattering, and *high contrast grating (HCG) effects*. See, e.g. Chang-Hasnain et al, High contrast gratings for integrated optoelectronics, *Advances in Optics and Photonics* 4, 379-440 (2012), hereinafter "Chang-Hasnain." The HCG effects are at the near-wavelength regime (See, Chang-Hasnain) where the optical wavelength in the material of the grating and the optical wavelength in the surrounding material of the grating is the range of the period of the grating.

'360 Patent, 11:39-51 (emphasis added). A skilled artisan would have understood from the above-excerpted disclosure that one cause of enhancement of photon absorption is due to effects produced by a high contrast grating (HCG).

202. The '360 Patent further explains that "[t]he period of the 3D pillar/hole microstructured array can be seen as a 3D high contrast grating, whose

period of the grating Λ can lie between λ/n_1 where n_1 is the optical refractive index of material M_1 and λ/n_2 where n_2 is the optical refractive index of material M_2 .” ’360 Patent, 12:1-5. Further, “[i]f $n_1 > n_2$ then $\lambda/n_1 < \Lambda < \lambda/n_2$.” ’360 Patent, 12:5-11. A skilled artisan would have understood from this disclosure that a structure that includes holes in the pillars of an imaging device would behave like a HCG if the pitch between the holes satisfies the condition $\lambda/n_1 < \Lambda < \lambda/n_2$, when $n_1 > n_2$.

203. The ’360 Patent confirms this, explaining that the HCG effect may explain the high absorption coefficient of semiconductors with in-pillar holes that satisfy the relationship $\lambda/n_1 < \Lambda < \lambda/n_2$. Specifically, the ’360 Patent states:

The HCG effect that may explain the high enhancement of the absorption coefficient of the bulk material is that a single or multiple HCG layer (or a single microstructured pillar/hole array layer) due to its resonance effects and/or due to a varying of the microstructured pillar/hole period spacing, the optical signal resonating in the HCG/microstructured pillar-hole array can be directed to propagate in the plane of the HCG/microstructured pillar-hole array rather than normal to the surface. Together with resonance and in-plane propagation this can greatly increase the absorption path length in the HCG/microstructured pillar-hole array.

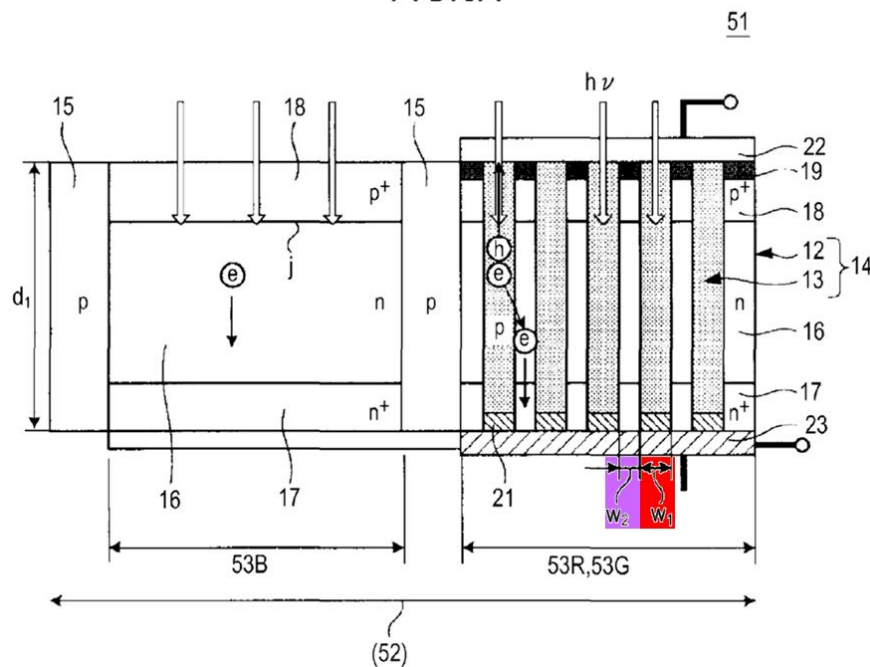
'360 Patent, 12:22-32. The '360 Patent goes on to say that “[u]sing the phenomenon of near-wavelength and also deep-wavelength where the HCG period is much less than the optical wavelength, and the diffraction regime where the HCG period is greater than the optical wavelength (See, Chang-Hasnain) the microstructured pillar-hole-void array can have enhanced absorption coefficient over the bulk absorption coefficient by a factor of 1.1 to over 100.” '360 Patent, 12:36-42.

204. One skilled in the art would have understood these disclosures of the '360 Patent as representations made by Patent Owner that a microstructured pillar hole array having microstructure period Λ (i.e., pitch of the holes) and satisfying the relationship $\lambda/n_1 < \Lambda < \lambda/n_2$ forms a high contrast grating (HCG). In my opinion, one skilled in the art would have further understood the Patent Owner as representing that if the microstructured pillar hole array forms an HCG, then the physical phenomenon of near-wavelength and deep-wavelength would result in an enhanced absorption coefficient of 1.1 to 100 times the bulk absorption coefficient associated with a structure that does not have the microstructured pillar hole array.

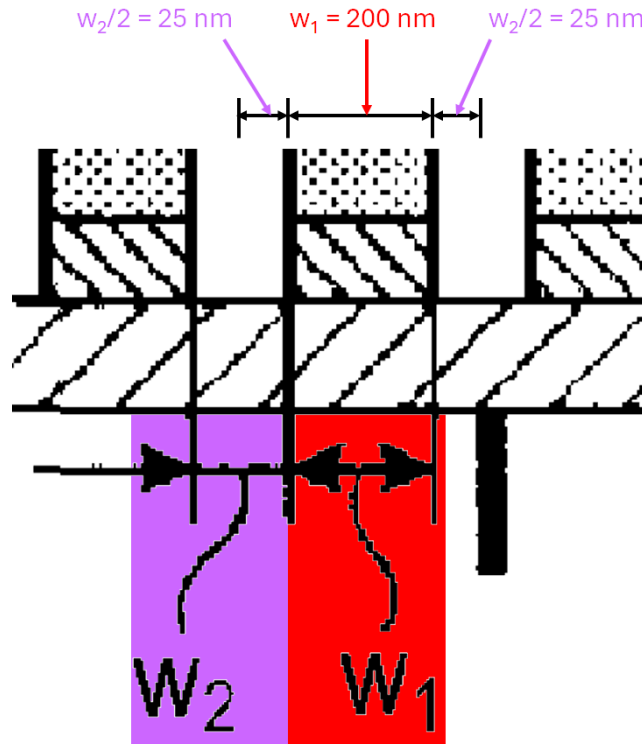
205. As I have discussed, *Kuboi* discloses an imaging device that has an array of pillars with in-pillar holes. *Supra*, XI.A.1.a, XI.A.1.b, XI.A.1.i. Furthermore, *Kuboi* discloses a microstructured pillar hole array where the period Λ or center-to-center distance between holes is about 250 nanometers. For

example, *Kuboi* discloses that the width w_1 of photoelectric conversion films 13 is 200 nm and width w_2 of semiconductor layer 12 between the photoelectric conversion films is 50 nm. *Kuboi*, ¶[94]. *Kuboi*'s Figure 6A, below, illustrates these dimensions. Additionally, I have provided a magnified view of Figure 6A to illustrate that the period Λ or center-to-center distance between holes in that figure would be 250 nm. Specifically, the period Λ would be $w_2/2 + w_1 + w_2/2 = 25 \text{ nm} + 200 \text{ nm} + 25 \text{ nm} = 250 \text{ nm}$.

FIG. 6A



Kuboi, Fig. 6A.



Kuboi, Fig. 6A (cropped and magnified).

206. One skilled in the art would have understood that visible light has a wavelength range of 400-700 nm and infrared light has a wavelength range of 750 nm to 1000 μm or even up to 2000 μm . Ex. 1012, 4 (disclosing wavelengths “typically in the 400-700 nm range of visible light”); Yu, ¶[23] (disclosing “IR light (light of wavelengths from about 0.78 to about 1000 microns)”). Further, one skilled in the art would have understood that the refractive index n_1 of silicon ranges between about 3.0 to 5.9 (Ex. 1056, 9:43-46, Fig. 4) and varies with wavelength. Ex. 1061, 48. For example, the refractive index n_1 of silicon is about

5.8 for light of wavelength 400 nm, 3.7 for light of wavelength 700-750 nm, and about 3.5 for light of wavelength 1000 nm. Ex. 1061, 48.

207. *Kuboi* discloses the organic photoelectric conversion films in its in-pillar holes may include materials such as “perylene-based compounds, phthalocyanine compounds, quinacridone compounds, porphyrin compounds, merocyanine compounds.” *Kuboi*, ¶[58]. One skilled in the art would have understood that the refractive index n_2 of such organic materials ranges between 1.5 and 3.0. Ex. 1057, 86:35-48 (disclosing porphyrin compounds as photoelectric conversion material), 142:18-25 (disclosing refractive index of the photoelectric conversion material); Ex. 1071, 6, Fig. 5 (disclosing refractive index of porphyrin compounds ranging from 1.5 to 2.8 for wavelengths of 400-700 nm); Ex. 1072, 13, Fig. 7 (disclosing refractive index of phthalocyanine compounds ranging from 1.5 to 2.8 for wavelengths of 400-700 nm); Ex. 1073, Abstract (disclosing refractive index of phthalocyanine compounds ranging from 2.03 to 2.48).

208. Below, I have provided Table D showing calculated values of λ/n_1 and λ/n_2 for *Kuboi*'s green pixels with porphyrin for visible light wavelengths 400 nm and 700 nm, and near infrared wavelengths of greater than 700 nm wavelength. I obtained values of λ/n_1 and λ/n_2 in Table D, using values of n_1 of silicon for different wavelengths from Ex. 1061, page 48, Table A-1, and values of n_2 of porphyrin compounds at different wavelengths from Ex. 1071, Fig. 5. As seen

from the values in Table D, *Kuboi's* hole pitch of 250 nm falls in the range λ/n_1 to λ/n_2 for at least part of the visible light spectrum (400-700 nm wavelengths) and at least part of the near infrared light spectrum (>700 nm wavelengths). For example, for the 550 nm green light wavelength, λ/n_1 ($550/4.5 = 123$) $< \Lambda$ (250 nm) $< \lambda/n_2$ ($550/2.0 = 275$).

Table D				
λ (nm)	n_1 (Silicon)	n_2 (Porphyrin)	λ/n_1(nm)	λ/n_2 (nm)
400	5.8	1.7	68	235
550	4.5	2.0	123	275
700	3.7	1.6	188	438
750	3.7	1.8	203	417

209. Below, I have provided Table E showing calculated values of λ/n_1 and λ/n_2 for *Kuboi's* red pixels with porphyrin for visible light wavelengths 400 nm and 700 nm, and near infrared wavelengths of greater than 700 nm wavelength. I obtained values of λ/n_1 and λ/n_2 in Table E, using values of n_1 of silicon for different wavelengths from Ex. 1061, page 48, Table A-1, and values of n_2 of phthalocyanine compounds at different wavelengths from Ex. 1072, page 13, Fig. 5. As seen from the values in Table E, *Kuboi's* hole pitch of 250 nm falls in the range λ/n_1 to λ/n_2 for at least part of the visible light spectrum (400-700 nm wavelengths) and at least part of the near infrared light spectrum (>700 nm

wavelengths). For example, for the 650 nm red light wavelength, λ/n_1 ($650/3.9 = 168$) $< \Lambda$ (250 nm) $< \lambda/n_2$ ($650/2.1 = 302$)

Table E				
λ (nm)	n_1 (Silicon)	n_2 (Phthalocyanine)	λ/n_1(nm)	λ/n_2 (nm)
400	5.8	1.9	68	211
650	3.9	2.1	168	302
700	3.8	1.8	186	389
750	3.7	2.3	203	326

210. In my opinion, therefore, one skilled in the art would have understood that the stated period of *Kuboi*'s in-pillar hole array falls within the λ/n_1 to λ/n_2 range for "selected visible and infrared wavelength ranges."

211. Further, one skilled in the art would have understood based on Patent Owner's representations that because the pitch of *Kuboi*'s in-pillar hole array falls within the λ/n_1 to λ/n_2 range, *Kuboi*'s in-pillar hole structure would form a HCG. One skilled in the art would have also understood based on Patent Owner's representations that such an HCG would produce an enhanced absorption coefficient of 1.1 to 100 times the bulk absorption coefficient based on the near-wavelength and deep-wavelength phenomena. In my opinion, therefore, one skilled in the art would have understood that *Kuboi*'s in-pillar holes would increase photon absorption in *Kuboi*'s device by at least 1.1 times at selected visible and

infrared wavelength ranges of said incident light compared to a like device lacking said one or more in-pillar holes.

212. Third, in my opinion, one skilled in the art would have found that Patent Owner's representations were consistent with those of other prior art teachings. For example, according to *Han* (Ex. 1051), "[t]o obtain the same ultimate efficiency as a standard 300 micrometer crystalline silicon wafer, nanohole arrays require less silicon by mass." *Han*, Abstract, 2:4-5. *Han* discloses that "nanoholes can be sized to substantially trap incident light." *Han*, 3:2-3. As shown in Figure 4 of *Han* below, the ultimate efficiency for a device having a semiconductor thickness of about 1.4 μm without nanoholes is approximately 0.12, whereas the ultimate efficiency for a similar device having nanoholes is approximately 0.22. *Han*, Fig. 4. In my opinion, based on a skilled artisan's knowledge of the state of the art before the '360 Patent's priority date, the skilled artisan would have understood that nanohole depths of 1.4 μm would increase light absorption by a factor of 1.8 ($0.22/0.12 = 1.8$), which is significantly higher than a factor of 1.1.

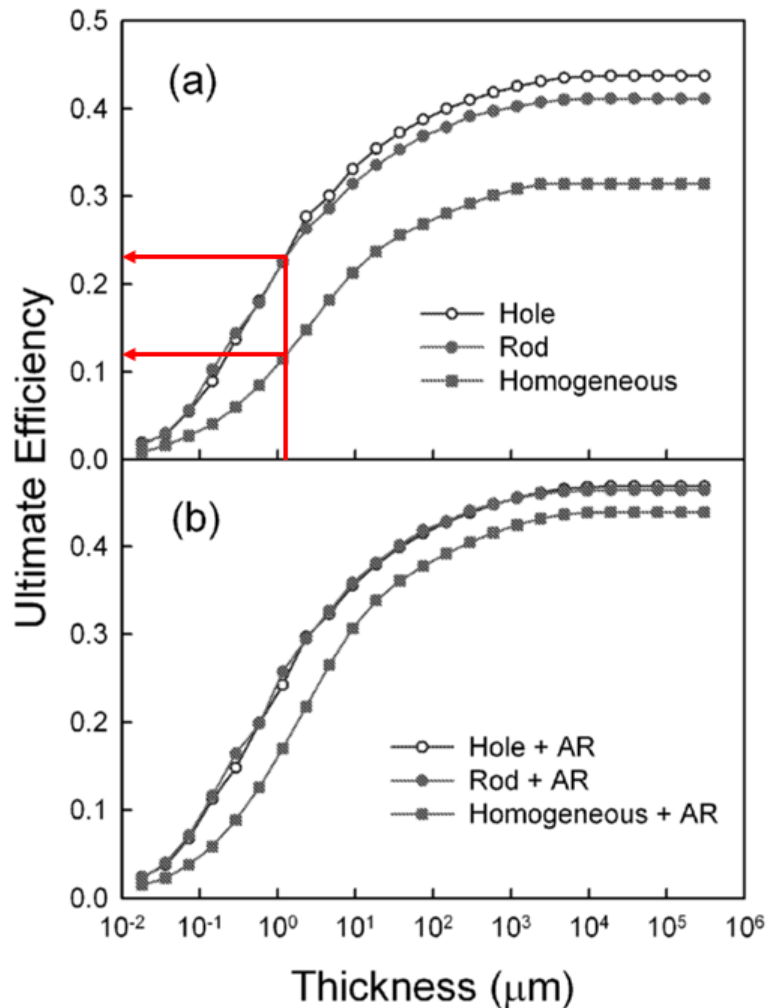


FIG. 4

Han, Fig. 4.

213. In my opinion, based on a skilled artisan's knowledge of the state of the art before the '360 Patent's priority date, the skilled artisan would have understood that *Kuboi*'s in-pillar $1.4 \mu\text{m}$ hole depth would increase photon absorption in *Kuboi*'s device by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said one or more in-pillar holes, and even if not readily understood, a POSITA would have

found such a result not only obvious but also one having a reasonable expectation of success in achieving this increase because *Kuboi* discloses forming nanoholes of 1.4 μm depth.

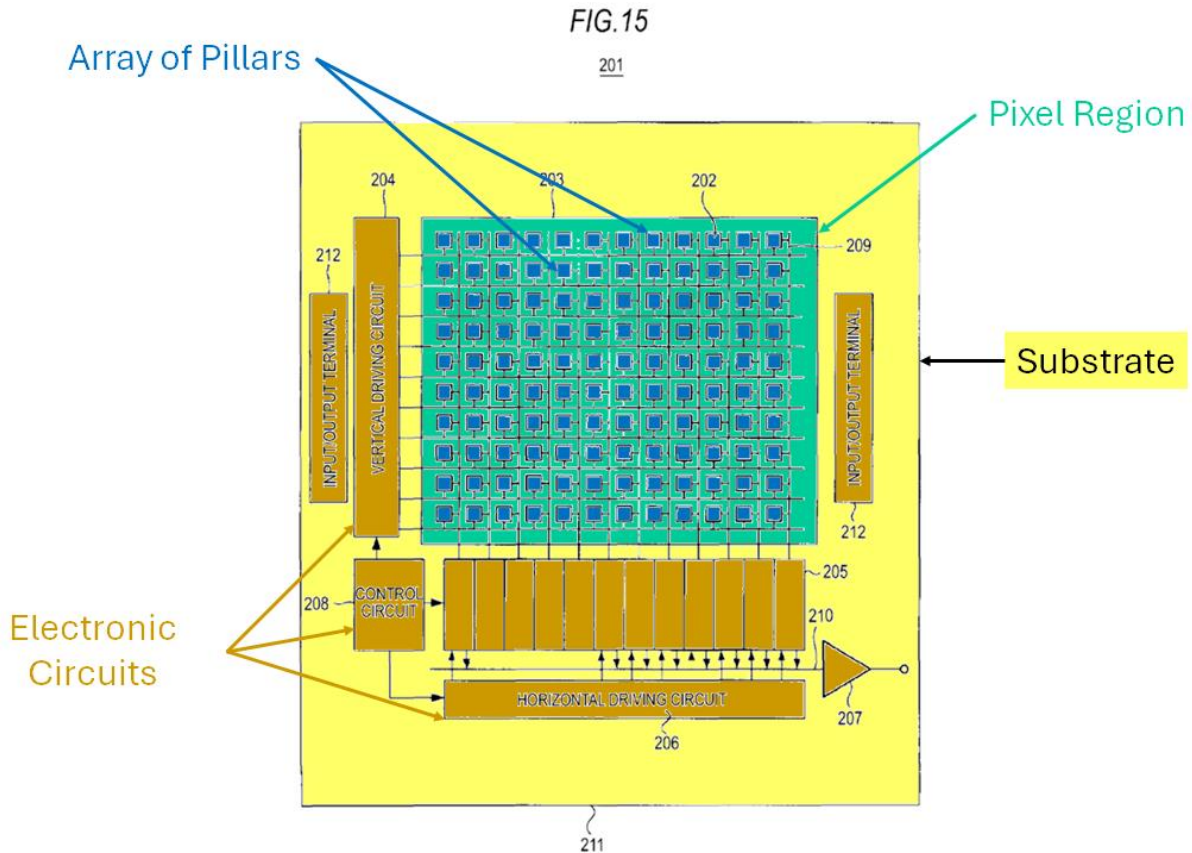
- n. [1i]: “wherein said **array of pillars** is monolithically integrated in or on said **semiconductor substrate** with **electronic circuits** that include active elements for signal processing and transmission.”

214. In my opinion, *Kuboi* discloses this limitation. Alternatively, in my opinion, the *Kuboi-Shinohara* combination renders this limitation obvious.

i. ***Kuboi* discloses this limitation.**

215. *Kuboi* discloses “a simplified exemplary configuration of a CMOS solid-state imaging device.” *Kuboi*, ¶[48]. *Kuboi*’s imaging device 201 “include[s] a **pixel region** (so-called ... imaging region) 203 and a **peripheral circuit portion** which are provided on a **semiconductor substrate 211** (i.e., a silicon substrate).” *Kuboi*, ¶[48]. *Kuboi* teaches that “**a pixel and logical circuit portion may be created in advance** and be bonded to the semiconductor substrate on which the semiconductor region 25 having the pixel transistors, the multilayer wiring layer 32, the lower electrode 23, and the like are formed.” *Kuboi*, ¶[78] (emphasis added). In my opinion, one skilled in the art would have understood *Kuboi* as teaching formation of the **pixel region** (including the **array of pillars**) and the **logical circuit portion** (including **vertical driving circuit 204, column signal processing circuits 205, horizontal driving circuit 206, output circuit 207, control**

circuit 208) in or on the same substrate. *Kuboi*, ¶¶[48]-[49]. *Kuboi*'s single-chip device is shown below:



Kuboi, Fig. 15.

216. *Kuboi* discloses a manufacturing method that forms the pixel region and the logical circuit portion on the same substrate. For example, *Kuboi* discloses a method of forming the pixel region by first forming an element separation region 15 on a silicon semiconductor layer 12. *Kuboi*, ¶[71]. *Kuboi* further discloses that “n⁺-type semiconductor region 17 (corresponding to the front surface side), a n-type semiconductor region 16 (corresponding to an intermediate region), and a p⁺-type semiconductor region 19 (corresponding to the rear surface side) are

formed in that order” in the region corresponding to one pixel divided by the element separation region 15. *Kuboi*, ¶[71]. *Kuboi* also discloses that subsequently “a vertical hole 38 such as a trench or a via extending from the p⁺-type semiconductor region 18 to the n⁺-type semiconductor region is formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching.” *Kuboi*, ¶[72]. *Kuboi* explains that a plurality of such holes are formed at necessary intervals. *Kuboi*, ¶[72]. *Kuboi* discloses forming electron blocking film 21 on the bottom of the vertical holes 38 and depositing an organic photoelectric conversion film 13 in the vertical holes 38. *Kuboi*, ¶[73]. *Kuboi* discloses forming an upper electrode on the upper surface of semiconductor layer 12 and a lower electrode on its lower surface. *Kuboi*, ¶[77]. Further, *Kuboi* discloses that “the pixel and logical circuit portion may be created in advance” on substrate 12. *Kuboi*, ¶¶[78], [48]-[49]. In my opinion, one skilled in the art would have understood from these disclosures that *Kuboi*’s manufacturing method would result in monolithically integrating the array of pillars (i.e., pixel region) with electronic circuits that include active elements for signal processing and transmission (i.e., control circuit 208 and output circuit 207).

ii. The *Kuboi-Shinohara* combination renders this limitation obvious.

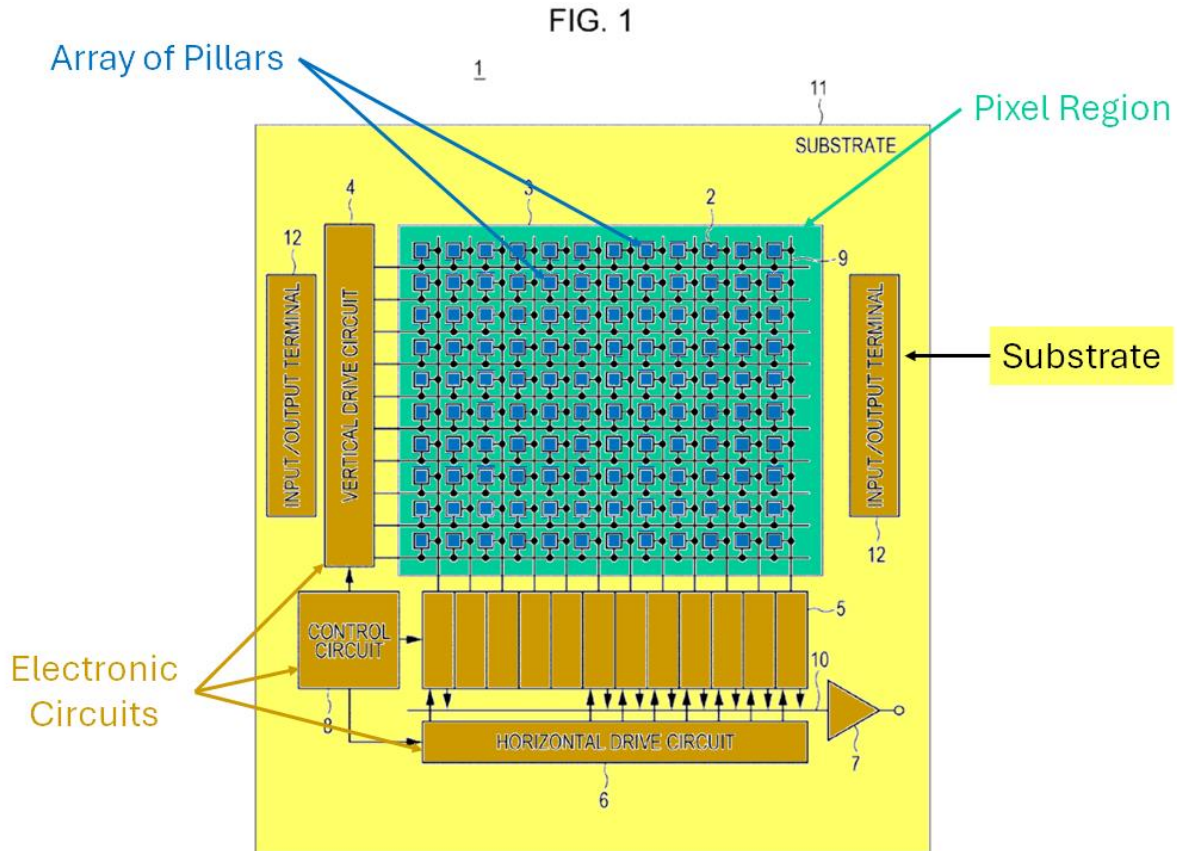
217. To the extent the Patent Owner argues that *Kuboi* does not disclose monolithic integration, the *Kuboi-Shinohara* combination renders claim [1i] obvious.

218. Referring to its Figure 1, *Shinohara* discloses “a MOS solid-state imaging device” that “includes a pixel region (so-called imaging region) 3 in which a plurality of pixels 2 each having a photoelectric conversion portion is regularly arranged in a semiconductor substrate 11, such as a silicon substrate, in a two-dimensional matrix and a peripheral circuit portion.” *Shinohara*, ¶[51]. *Shinohara* also discloses that its “peripheral circuit portion includes so-called logic circuits, such as a vertical drive circuit 4, a column signal processing circuit 5, a horizontal drive circuit 6, an output circuit 7, and a control circuit 8.” *Shinohara*, ¶[52].

219. *Shinohara* discloses a method for manufacturing the imaging device on a “p-type silicon semiconductor substrate 22.” *Shinohara*, ¶[68]. *Shinohara* teaches forming the photodiodes and the separation regions between the photodiodes on the imaging device on a “p-type silicon semiconductor.” *Shinohara*, ¶¶[68]-[82]. According to *Shinohara*, “the floating diffusion portion,” “transfer gate electrode,” “transfer transistor,” “reset transistor,” “amplification transistor,” and “selection transistor” are each “formed in the other part of the p-

type semiconductor well region” of the substrate. *Shinohara*, ¶[81]. As a result, “the pixel region in which the pixels are arranged in a two-dimensional matrix is formed.” *Shinohara*, ¶[81]. *Shinohara* discloses that “the peripheral circuit portion (not shown) by CMOS transistors is formed in the periphery of the pixel region.” *Shinohara*, ¶[81]. *Shinohara* also discloses that “the multilayer wiring layer 33 in which a plurality of layers of the wires 32 is disposed with at least one interlayer insulating film 31 provided therebetween is formed on the surface of the semiconductor substrate 22.” *Shinohara*, ¶[82]

220. Thus, *Shinohara* discloses forming the pixel region (i.e., including [array of pillars](#)), the peripheral circuit portion, the floating diffusion portion, the transfer gate electrode, transistors (i.e., transfer transistor, reset transistor, amplification transistor, and selection transistor), and multilayer wiring layer 33 (i.e. [electronic circuits](#)) on the same substrate 22. In my opinion, one skilled in the art would have understood that *Shinohara* discloses monolithically integrating its pixel region, and the peripheral circuit portion including various electronic circuits and transistors on the same substrate. *Shinohara*’s imaging device with these features is illustrated below.



Shinohara, Fig. 1.

221. In my opinion, one skilled in the art would have found it obvious to combine *Shinohara*'s teachings with *Kuboi*, resulting in an imaging device in which *Kuboi*'s array of pillars (i.e., pixel region) is monolithically integrated with electronic circuits that include active elements for signal processing and transmission.

iii. Motivation to modify *Kuboi*'s imaging device in view of *Shinohara*'s teaching of monolithic integration

222. As discussed above, both *Kuboi* and *Shinohara* are analogous art to the '360 Patent. *Supra* XI.A.1.c.i. In my opinion, one skilled in the art would have been motivated to combine the teachings of *Kuboi* and *Shinohara*.

223. In particular, one skilled in the art would have understood that including the pixel region, peripheral circuit portion, pixel transistors, and wiring layer on the same substrate would provide several advantages. For example, monolithically integrating the pixel region and electronic circuits for signal processing and transmission on the same substrate reduces noise and attenuation of the photoelectric signal generated by the pixel region particularly by shortening the signal travel path in the monolithically integrated imaging device. This is supported by other prior art that would have been known to one skilled in the art.

224. For example, *Hasegawa* (Ex. 1053) discloses that “from the viewpoint of curtailing attenuation of the photo-electrical conversion signals and suppressing the superimposition of noise, the length of wiring between the light-receiving parts and the amplifier is configured to be as short as possible.” *Hasegawa*, ¶[9]. *Hasegawa* explains: “Based on this viewpoint, and from the viewpoint of reducing the manufacturing cost of the photodetector, it would be ideal to form the circuits—such as the light-receiving parts, each of which has the PIN photodiode

structure, and the amplifier—on the same semiconductor chip.” *Hasegawa*, ¶[9].

Similarly, *Michel* (Ex. 1029) discloses that “complete integration of photonic devices into a CMOS process flow will enable low cost photonic functionality within electronic circuits.” *Michel*, Abstract. *Beals* (Ex. 1030) discloses that drivers for manufacturing monolithic electronic photonic integrated circuits include “increasing demand for high frequency mixed signal processing, ability to operate at high bandwidths in chip-to-chip as well as within the chip for multicore applications with greater power efficiency and lower manufacturing cost.” *Beals*, 2. And *NXP* teaches that integrating signal processing circuitry and the photodiode on the same substrate “may be more reliable than a discrete solution” and result in a smaller package, which is advantageous for mobile applications. *NXP*, ¶¶[16], [32], [37].

225. In my opinion, one skilled in the art would have been motivated to use *Shinohara*’s monolithic integration method to manufacture and further improve *Kuboi*’s imaging device to achieve the above-identified benefits such as high bandwidth, low manufacturing cost, and a smaller package size. In my opinion, one skilled in the art would have found that using *Shinohara*’s monolithic integration in *Kuboi* would involve nothing more than the use of a known technique (namely forming the pixel region and all associated electronic circuitry on the same substrate), to improve a similar device (namely *Kuboi*’s imaging

device), in the same way (namely, by improving manufacturing reliability, reducing manufacturing cost and package size, reducing signal attenuation, reducing noise, and improving high-bandwidth performance) of *Kuboi*'s device.

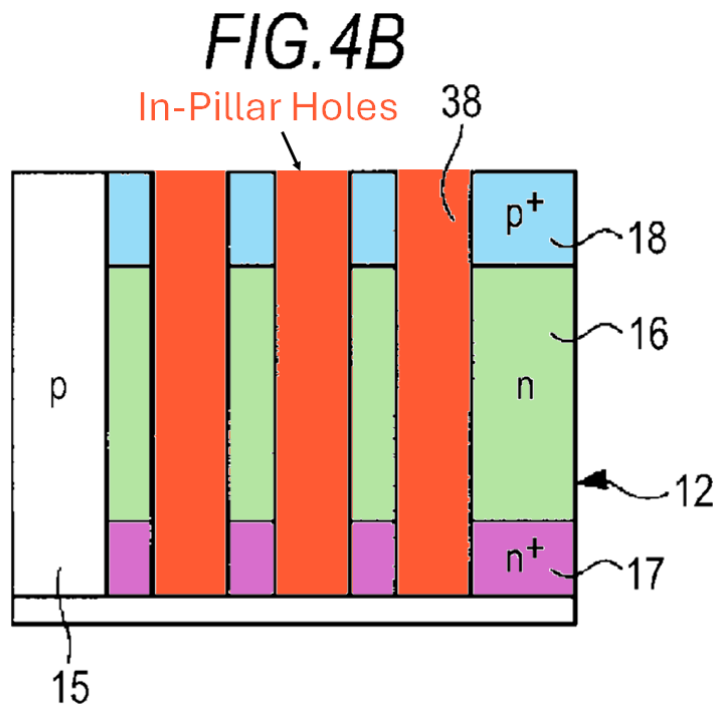
226. *Kuboi* and *Shinohara* disclose similar imaging devices that include a pixel region and a peripheral circuit portion. Both *Kuboi* and *Shinohara* provide extensive disclosure regarding methods of manufacturing their respective imaging devices. In my opinion, therefore, manufacturing *Kuboi*'s pixel region and associated electronic circuitry, including *Kuboi*'s pixel transistors, using *Shinohara*'s monolithic integration techniques would have been well within the skill level of a person of ordinary skill in the art. Further, in my opinion, a skilled artisan would have had a reasonable expectation of success in implementing *Shinohara*'s teachings for manufacturing *Kuboi*'s imaging device because it merely requires combining well-known prior elements and manufacturing methods taught by *Shinohara*.

227. To summarize, in my opinion, *Kuboi* alone discloses the limitations of claim [1i]. Alternatively, in my opinion, the combination of the teachings of *Kuboi* and *Shinohara* disclose and render obvious the limitations of claim [1i].

2. Claim 3: "The photodetector device of claim 1, in which each of said pillars has a plurality of said one or more in-pillar holes."

228. In my opinion, *Kuboi* discloses this additional limitation.

229. As I discussed for claim [1d], *Kuboi* discloses that **holes 38** extending from **region 18** to **region 17** are “formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching.” *Kuboi*, ¶¶[72], [13]-[14], [67], [95]; *supra* VI.A.7.i. *Kuboi* further discloses that “**holes 38** are formed at necessary intervals” and “in a stripe shape.” *Kuboi*, ¶[72]; *supra* VI.A.7.i. The plurality of **in-pillar holes** (e.g., more than one **in-pillar hole**) in *Kuboi*’s **pillar** (i.e. **pixel**) are illustrated below:

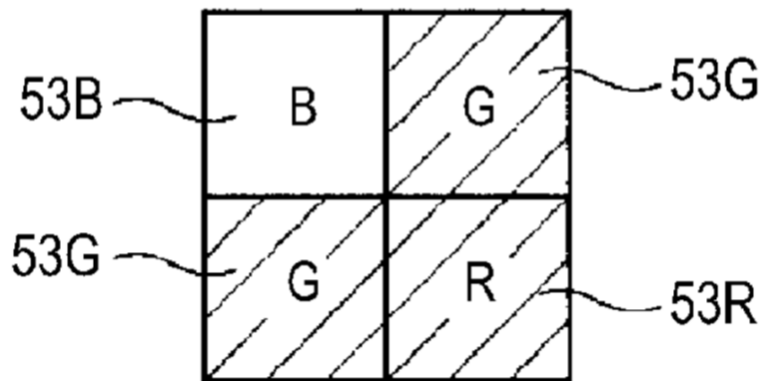


Kuboi, Fig. 4B.

230. Although only one pillar (or pixel) has been described above, *Kuboi* uses the same structure for a plurality of pixels. For example, *Kuboi*’s “imaging device” includes “primary color filters ... and a pixel region 52 in which a group of

pixels made up of a blue (B) pixel 53B, a red (R) pixel 53R, a green (G) pixel 53G, and a green (G) pixel 53G are arranged in a two-dimensional array,” as shown below. *Kuboi*, ¶[90].

FIG. 6B



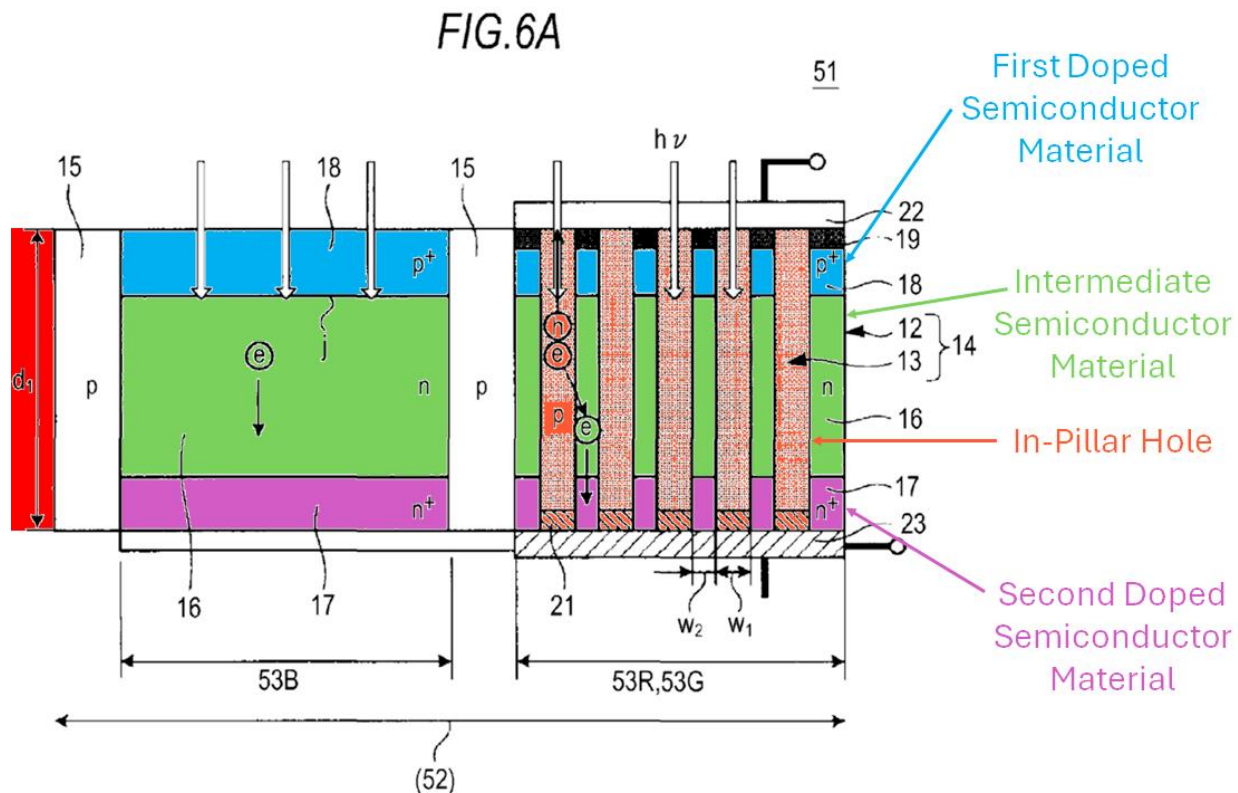
Kuboi, Fig. 6B.

231. *Kuboi* discloses that “[t]he processes of manufacturing the red and green pixels in the solid-state imaging device 51 of the first embodiment are the same as those illustrated in FIGS. 4A to 4F.” *Kuboi*, ¶[95]. As I discussed for claim [1a], *Kuboi*’s pillar arrays may include a 2-column, 1-row array; or a 1-column, 2-row array. *Supra* XI.A.1.b. In my opinion, one skilled in the art would have thus understood that *Kuboi* discloses a plurality of pixels (i.e., 53G, 53R) forming an array of pillars (2-column, 1-row; or 1-column, 2-row) and each pillar (i.e., each pixel 53G or 53R) in these arrays of pillars includes a plurality of in-pillar holes 38 (as illustrated in Figure 4B).

3. Claim 5: “The photodetector device of claim 1, in which said one or more in-pillar holes extend to a depth in a range of 100-10,000 nanometers.”

232. In my opinion, *Kuboi* discloses this additional limitation.

233. *Kuboi* discloses that holes 38 extending from region 18 to region 17 “[are] formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching.” *Kuboi*, ¶¶[72], [13]-[14], [67], [95]; *supra* VI.A.7.i. Furthermore, referencing Figures 6A/6B, *Kuboi* discloses that the thickness d_1 of semiconductor layer 12 is “set to about 1.4 μm .” *Kuboi*, ¶[94]. *Kuboi*’s in-pillar holes extending through thickness d_1 of semiconductor layer 12 are illustrated below:



Kuboi, Fig. 6A.

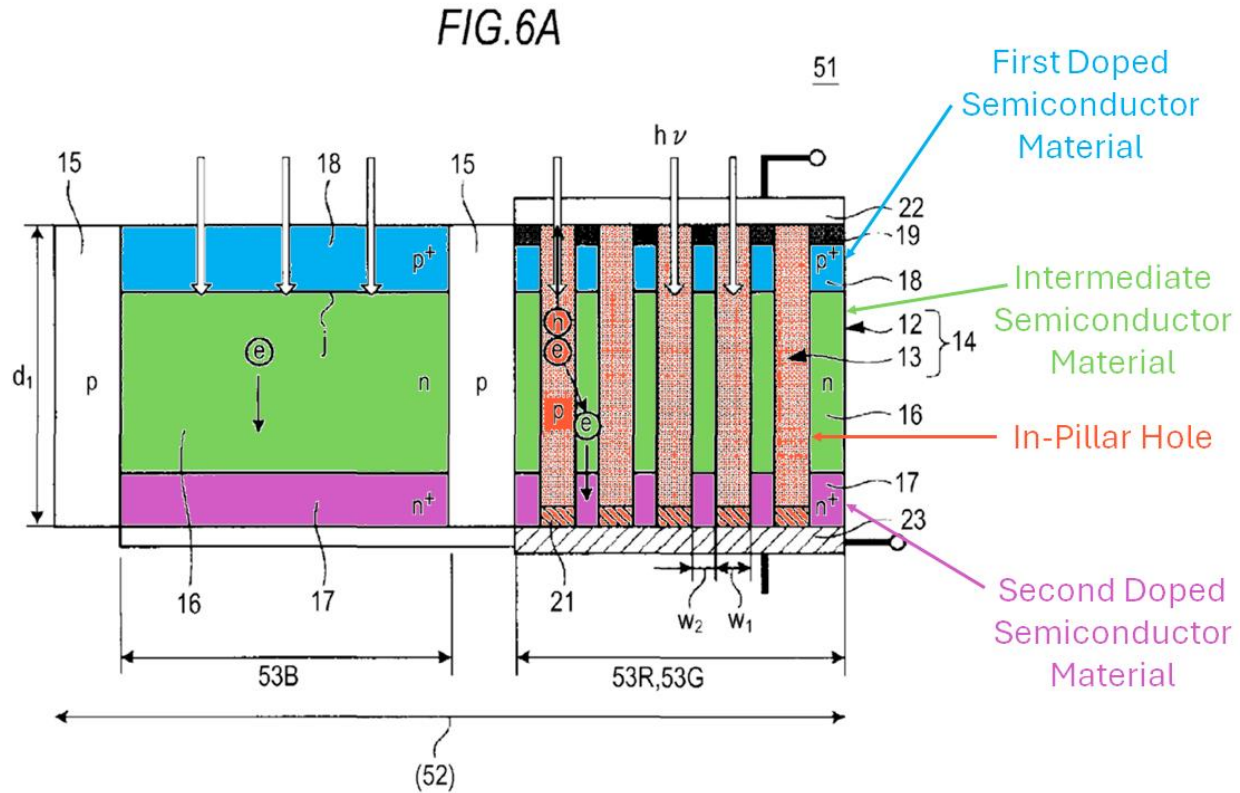
234. Because the depth of **each hole** is equal to the thickness **d₁** of the semiconductor layer, in my opinion, one skilled in the art would have understood that *Kuboi*'s in-pillar holes have a depth **d₁**. As discussed above, *Kuboi* discloses that depth **d₁** is 1.4 μm (i.e., 1400 nanometers), which falls within the claimed range of 100-10,000 nanometers. In my opinion, therefore, *Kuboi* discloses that the **one or more in-pillar holes** in its photodetector device extend to a depth in the claimed range of 100-10,000 nanometers.

4. Claim 6: “The photodetector device of claim 1, in which said one or more **in-pillar holes extend into said **intermediate semiconductor material**.”**

235. In my opinion, *Kuboi* discloses this additional limitation.

236. *Kuboi* discloses that **region 18**, **region 16**, and **region 17** “are formed in that order from the light incident surface of the semiconductor layer 12.” *Kuboi*, ¶¶[91], [55]-[56], [71], [181]; *supra* XI.A.1.d ([1b.2]). Further, *Kuboi* discloses that **hole 38** extending from **region 18** to **region 17** “is formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching.” *Kuboi*, ¶[72]. As I discussed for claim [1c.1], *Kuboi*'s intermediate semiconductor material (i.e., **region 16**) is disposed between **region 18** and **region 17**. *Supra* XI.A.1.e. In my opinion, one skilled in the art would understand that because **holes 38** extend from **region 18** to **region 17**, through **region 16**, *Kuboi*'s one or more **in-pillar holes**

extend into intermediate semiconductor material. Kuboi's in-pillar holes extending into the intermediate semiconductor material are illustrated below.



Kuboi, Fig. 6A.

B. Claims 1, 8, and 9 are Obvious Over *Yu* (Ground 2) or Obvious Over *Yu* and *Shinohara* (Ground 3)

1. Independent Claim 1

- a. [1pre]:³ “A photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar holes comprising:”

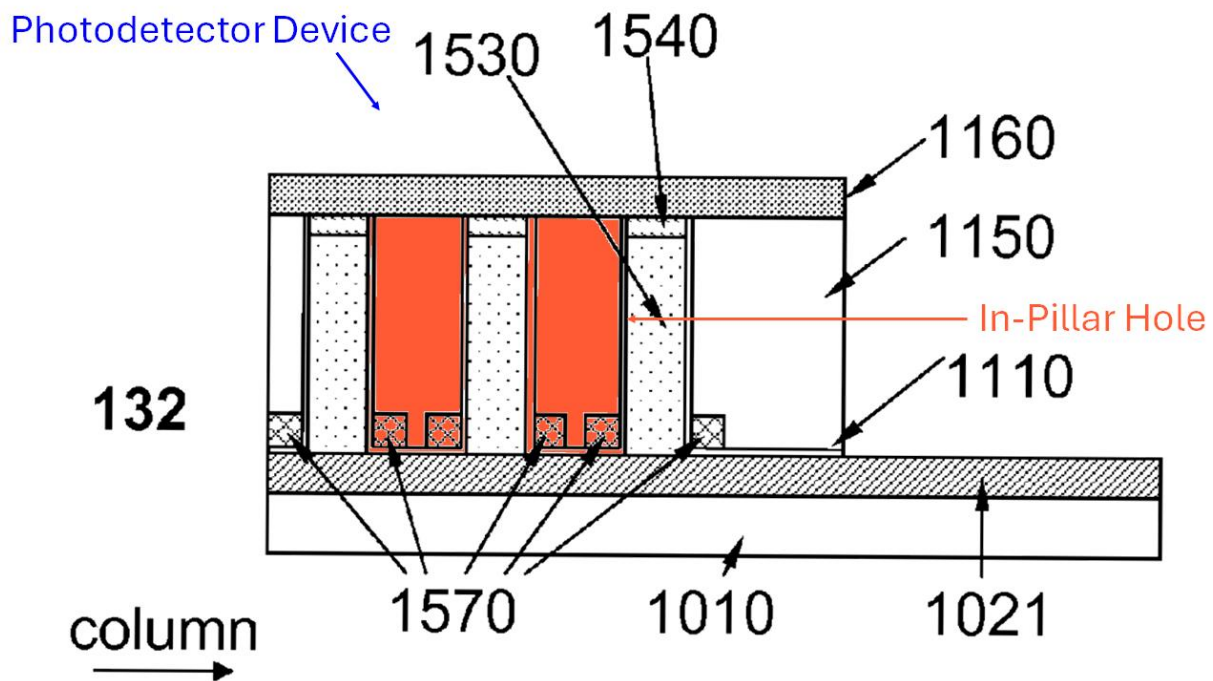
237. In my opinion, to the extent the preamble limits the scope of claim 1, *Yu* discloses the preamble.

238. For example, *Yu*’s image sensor is a photodetector device formed in or on a semiconductor substrate that includes nanopillars adapted to convert light impinging thereon to electrical signals. *Yu*, Abstract, ¶¶[7], [17], [48], [52]. *Yu* discloses starting with a silicon-on-insulator (SOI)-type substrate. *Yu*, ¶[62].

239. *Yu* also discloses that its image sensor has pixels that include at least one nanopillar, which convert light impinging thereon to electrical signals. *Yu*, Abstract, ¶[48]. In my opinion, *Yu*’s image sensor is a photodetector device because the nanopillars in *Yu*’s image sensor convert light to electrical signals. *Yu* also discloses that “the nanopillars and the substrate can comprise suitable

³ My mapping of the claims to *Yu*, including the terms “in-pillar holes” (and a plurality thereof) and “array of pillars,” is based on how Patent Owner maps the same claims to Petitioner’s accused products in litigation. Ex. 1074.

semiconductor materials.” *Yu*, ¶[55]. In my opinion, because *Yu*’s nanopillars and substrate comprise semiconductor materials, *Yu*’s image sensor (i.e., photodetector device) is formed in or on a semiconductor substrate. As I explain for claim [1d] (*infra* XI.B.1.i), *Yu*’s image sensor (i.e., photodetector device) includes deliberately formed in-pillar holes. *Yu*’s image sensor (i.e., photodetector device) with in-pillar holes is illustrated below:



Yu, Fig. 1, step 132.

- b. [1a]: “a laterally extending array of pillars that have rectangular cross-sections in a horizontal plane;”

240. In my opinion, *Yu* discloses this limitation.

241. *Yu*'s image sensor has pixels that include at least one nanopillar. *Yu*, Abstract. *Yu* discloses that "the pixels are organized into a plurality of 'rows'" and the "pixels can be organized into a plurality of 'columns.'" *Yu*, ¶¶[51], [9] ("image sensor can comprise first, second, third and fourth pixels"), [17], [25], [48]. In my opinion, each of *Yu*'s pixels is a **pillar**. Further, one skilled in the art would have understood that *Yu* discloses a laterally extending **array of pillars** because *Yu*'s pixels can be organized into rows and columns.

242. *Yu* discloses that "each pixel has at least one nanopillar, which comprises a p-n or p-i-n junction extending in the length direction of the nanopillar." *Yu*, ¶[52]. *Yu* further discloses "an exemplary three-nanopillar pixel and an exemplary four-nanopillar pixel" that "may be incorporated into the image sensor." *Yu*, ¶¶[130-[132], Figs. 7A-7B. In my opinion, each of *Yu*'s pixels is a **pillar**, and as shown below, each **pillar** in *Yu*'s image sensor has a **rectangular cross-section** in a horizontal plane. An exemplary pixel (i.e., pillar) with multiple nanopillars is illustrated below:

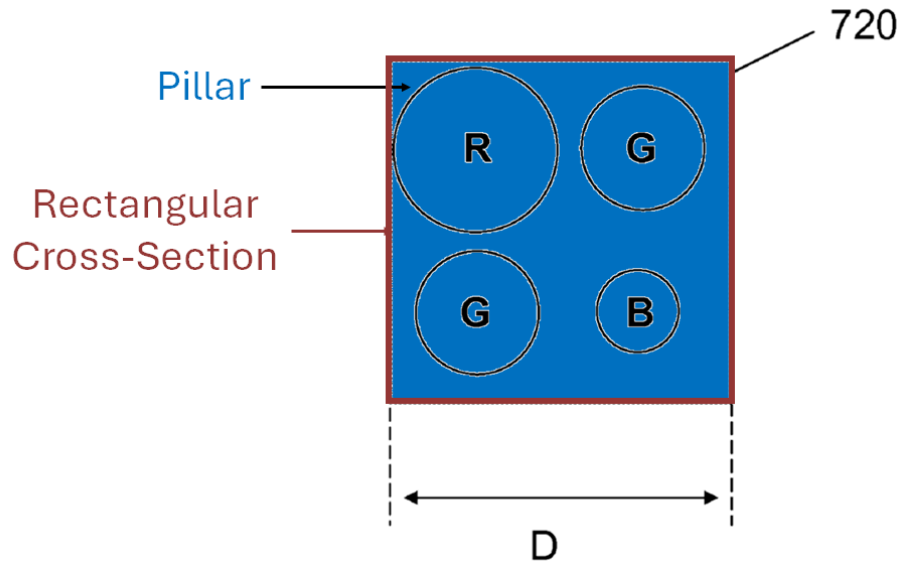


FIG. 7B

Yu, Fig. 7B.

243. In my opinion, one skilled in the art would have understood that the “nanopillars” disclosed in *Yu* are not the claimed pillars. Rather, a skilled artisan would have understood that *Yu*’s pixel is the claimed **pillar** and that each such **pixel** (i.e. **pillar**) may have more than one nanopillars. In my opinion, therefore, one skilled in the art would have understood that *Yu* discloses an array of **pixels** (i.e., **pillars**) arranged in an array of rows and columns and further that each such **pixel** or **pillar** has a **rectangular cross-section**.

244. Further in my opinion, to the extent Patent Owner argues that *Yu*’s pixels have a square shape, a square is nothing but a particular type of rectangle that has sides of equal length. Ex. 1058, 17, 23. In my opinion, therefore, *Yu*

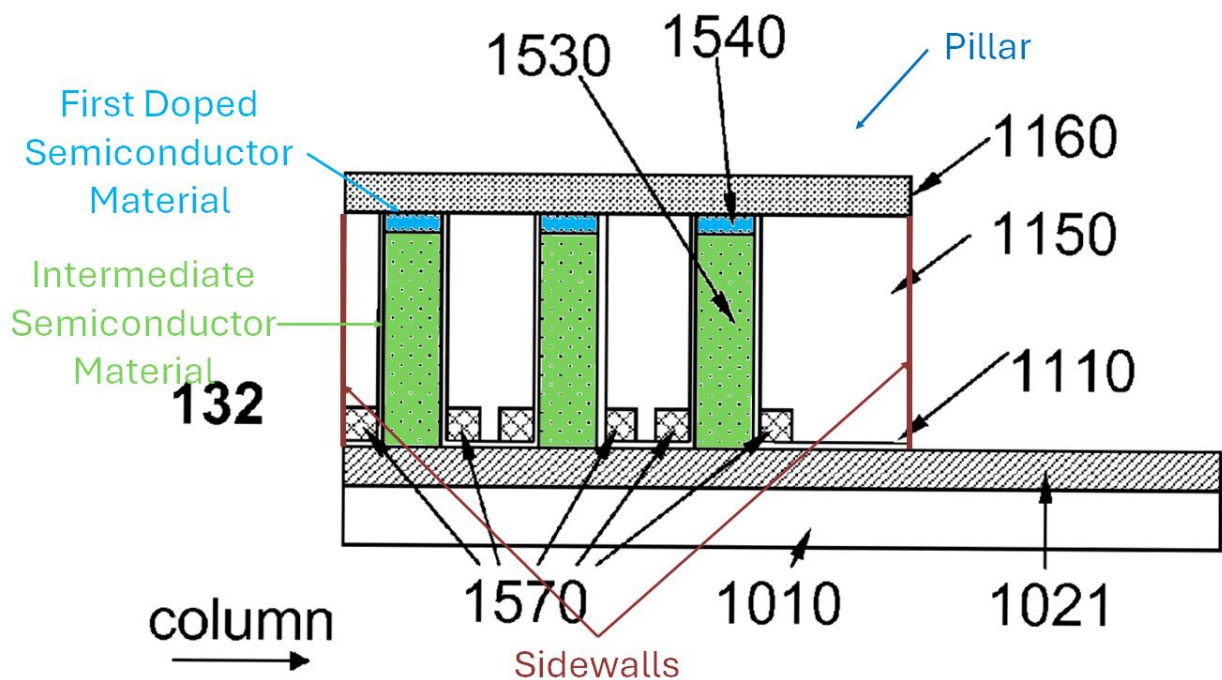
discloses an array of **pixels** (i.e., **pillars**) arranged in an array of rows and columns and further that each such **pixel** or **pillar** has a **rectangular cross-section**.

- c. [1b.1]: “wherein said **array of pillars** comprises: a **first doped semiconductor material**; an **intermediate semiconductor material**; and **solid dielectric** between at least portions of **sidewalls** of adjacent **pillars** of said **array of pillars**;

245. In my opinion, *Yu* discloses this limitation.

246. As I discussed for claim [1a], *Yu* discloses an **array of pillars**, each of which has multiple nanopillars. *Supra* XI.B.1.b. As I also discussed for claim [1pre], *Yu*’s “nanopillars and the substrate can comprise suitable semiconductor materials and/or metals such as Si.” *Yu*, ¶¶[55], [27]; *supra* XI.B.1.a. *Yu* discloses that its “substrate has an oxide layer 1010, a heavily doped layer (HDL) 1020 on the layer 1010 and an **epi layer 1030** on the HDL layer 1020.” *Yu*, ¶[62]. *Yu* explains that the “substrate can have the following doping profiles: (i) the HDL layer 1020 is p⁺ (i.e., [] heavily doped to p type), the **epi layer 1030** is p[−] (i.e., [] lightly doped to p type); [and] (ii) the HDL layer 1020 [is] p⁺, the **epi layer 1030** is i (i.e., [] intrinsic). *Yu*, ¶[62]. *Yu* also discloses that “**junction layer 1040** is formed on the epi layer 1030” and that “**junction layer 1040** is of the opposite conduction type as the HDL layer 1020, i.e., [] if the HDL 1020 is p type, the **junction layer 1040** is n type.” *Yu*, ¶[63]. Because *Yu*’s **epi layer 1030** is located between *Yu*’s **junction layer 1040** and *Yu*’s HDL 1020, in my opinion, *Yu*’s **epi layer 1030** is the

intermediate semiconductor material. Yu's pillars also include sidewalls defining the outer boundaries of the pillars as shown in the figure below, which also illustrates Yu's pillar including the intrinsic epi layer 1530 (i.e., "intermediate semiconductor material"), and junction layer 1540, "which is part of the junction layer 1040" (Yu, ¶[68], i.e., "first doped semiconductor material").



Yu, Fig. 1, step 132.

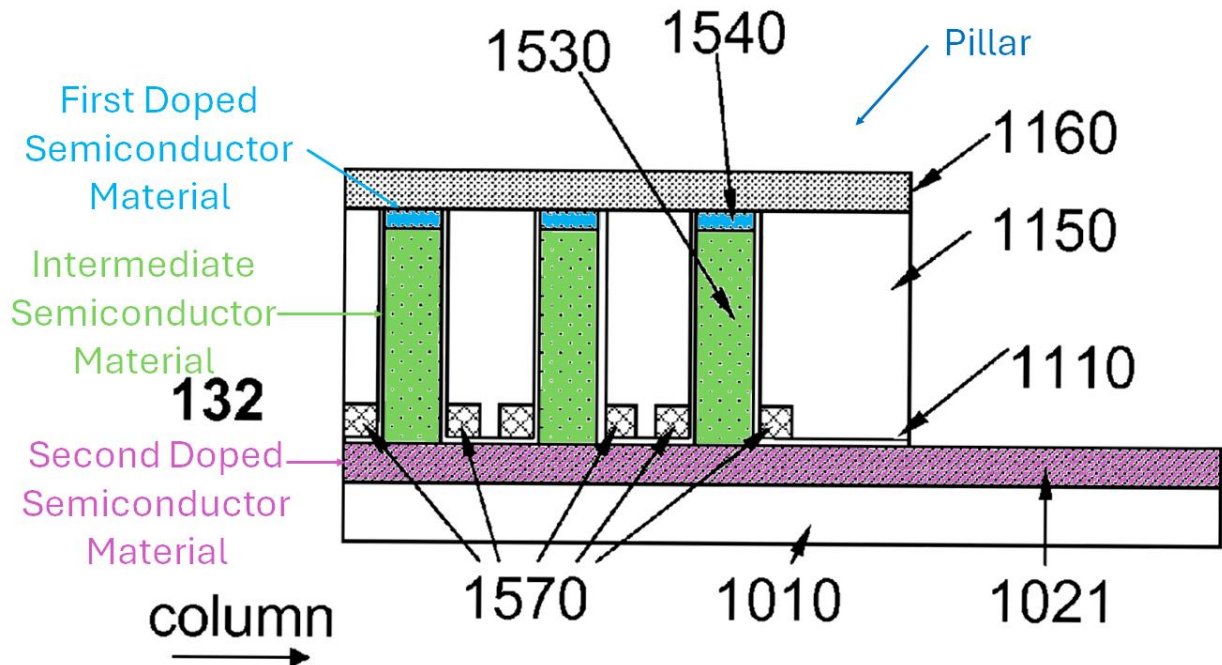
247. Yu explains that a cladding may surround some or all pixels of the image sensor, and that the cladding may be formed from silicon nitride. Yu, ¶[133]. As I explained above, silicon nitride is a solid dielectric material. *Supra* XI.A.1.c; Ex. 1063, 20, 33; Ex. 1020, 35. In my opinion, therefore, one skilled in the art

would have understood that the silicon nitride cladding on the sidewalls is a “solid dielectric,” as claimed. Further, one skilled in the art would have understood that *Yu*’s solid dielectric cladding would also be positioned between sidewalls of adjacent pixels, because the cladding surrounds each of the pixels (or pillars).

d. [1b.2]: “a second doped semiconductor material; wherein:”

248. In my opinion, *Yu* discloses this limitation.

249. As I discussed for claim [1b.1], *Yu* discloses that its “nanopillars and the substrate can comprise suitable semiconductor materials and/or metals such as Si.” *Yu*, ¶¶[55], [27]; *supra* XI.B.1.c. As I also discussed there, *Yu*’s “substrate has an oxide layer 1010, a heavily doped layer (HDL) 1020 on the layer 1010 and an epi layer 1030 on the HDL layer 1020.” *Yu*, ¶[62]; *supra* XI.B.1.c. *Yu* further discloses that “the HDL layer 1020 is p⁺ (i.e., heavily doped to p type).” *Yu*, ¶[62]. *Yu* explains that HDL layer 1020 is segmented into readout lines 1021. *Yu*, ¶[76]. In my opinion, because HDL layer 1020 is heavily doped and is part of *Yu*’s substrate, which is a semiconductor material, HDL layer 1020 is a doped semiconductor material. Further, in my opinion, *Yu*’s HDL layer 1020 is the claimed “second doped semiconductor material.” *Yu*’s photodetector device (i.e., image sensor) with the “second doped semiconductor material” (i.e., HDL layer 1020) is illustrated below.



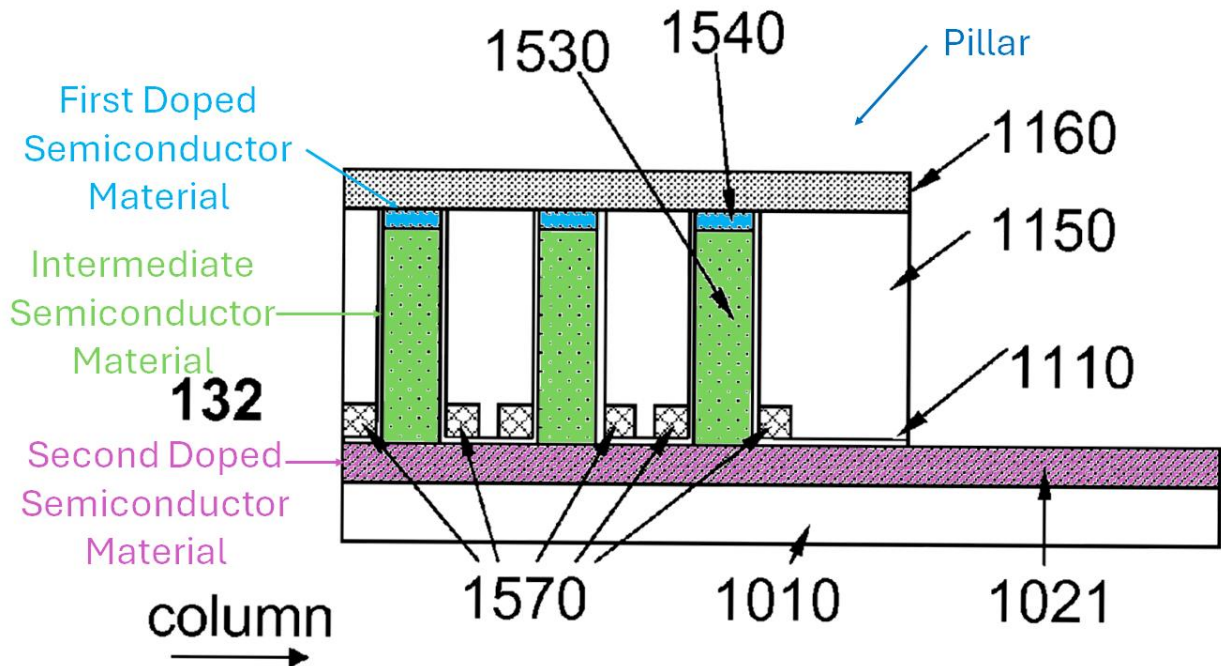
Yu, Fig. 1, step 132.

- e. [1c.1]: “the **intermediate semiconductor material** is between said **first** and **second** doped semiconductor materials;”

250. In my opinion, *Yu* discloses this limitation.

251. *Yu* discloses that its “substrate has an oxide layer 1010, a heavily doped layer (HDL) 1020 on the layer 1010 and an epi layer 1030 on the HDL layer 1020.” *Yu*, ¶[62]. *Yu* also discloses that “junction layer 1040 is formed on the epi layer 1030.” *Yu*, ¶[63]. In my opinion, one skilled in the art would understand that because the epi layer is formed on the HDL layer and because the junction layer is formed on the epi layer, *Yu*’s **epi layer** (i.e., **intermediate semiconductor material**) is between the **junction layer 1540**, “which is part of the **junction layer 1040**” (*Yu*, ¶[68], i.e., **first doped semiconductor material**) and the **HDL** (i.e., **second doped**

semiconductor material). Yu's photodetector device (i.e., image sensor) in which the intermediate semiconductor material is between said first and second doped semiconductor materials is illustrated below.



Yu, Fig. 1, step 132.

- f. [1c.2]: “the first and second doped semiconductor materials are doped to opposite semiconductor types;”

252. In my opinion, Yu discloses this limitation.

253. As I discussed for claims [1b.1], [1b.2] and [1c.1], Yu discloses that “first doped semiconductor material” (i.e., junction layer 1040), “intermediate semiconductor material” (i.e., intrinsic epi layer 1530), and “second doped semiconductor material” (i.e., HDL layer 1020) are formed in Yu's substrate. Yu, ¶¶[27], [55], [62], [63], [68]; *supra* XI.A.1.c ([1b.1]), XI.A.1.d ([1b.2]), XI.A.1.e

([1c.1]). *Yu* discloses that “junction layer 1040 is of the opposite conduction type as the HDL layer 1020, i.e., [] if the HDL 1020 is p type, the junction layer 1040 is n type.” *Yu*, ¶[63]; *see also Yu*, ¶[62]. In my opinion, one skilled in the art would have understood opposite conduction types, namely p type and n type, as referring to semiconductor materials that are oppositely doped. Therefore, in my opinion, *Yu* discloses that its p type first doped semiconductor material (i.e., junction layer 1040) is oppositely doped relative to its n type second doped semiconductor material (i.e., HDL layer).

- g. [1c.3]: “the intermediate semiconductor material is less doped than at least one of the first and second doped semiconductor materials and the degree of doping is the same or different for different positions in the intermediate semiconductor material; and”

254. In my opinion, *Yu* discloses this limitation.

255. *Yu* discloses that its “substrate can have the following doping profiles: (i) the HDL layer 1020 is p+ (i.e., [] heavily doped to p type)”; and (ii) “the epi layer 1030 is p− (i.e. lightly doped to p type).” *Yu*, ¶[62]. *Yu*’s intermediate semiconductor material (i.e., epi layer) is doped less (lightly doped p type) than the second doped semiconductor material (i.e., HDL layer, highly doped p type). In my opinion, one skilled in the art would have understood that because *Yu*’s epi layer is lightly doped to p type and because *Yu*’s HDL layer is heavily doped to p type,

Yu's intermediate semiconductor material (i.e., epi layer) is less doped than *Yu*'s second doped semiconductor material (i.e., HDL layer).

256. *Yu* does not expressly describe the degree of doping at different positions in the epi layer (“intermediate semiconductor material”). However, in my opinion, a person of ordinary skill would have understood that the degree of doping would either be the same or different at different positions in epi layer as no other possibilities exist.

257. As I explained above, diffusion and ion implantation are the two key methods of doping semiconductors. Ex. 1063, 37; *supra* XI.A.1.g. As I also explained there, in both methods the doping concentration varies progressively with depth into the semiconductor. *supra* XI.A.1.g; Ex. 1063, 37-38; Ex. 1020, 4; Ex. 1028, 1. Therefore, in my opinion, a skilled artisan would have understood that the doping concentration in *Yu*'s epi layer would vary with depth. In my opinion, therefore, a skilled artisan would have found it obvious that the degree of doping is the same or different for different positions in *Yu*'s “intermediate semiconductor material” (i.e., epi layer).

- h. [1c.4]: “each of the first and second doped semiconductor materials and said intermediate semiconductor material comprises Si;”

258. In my opinion, *Yu* discloses this limitation.

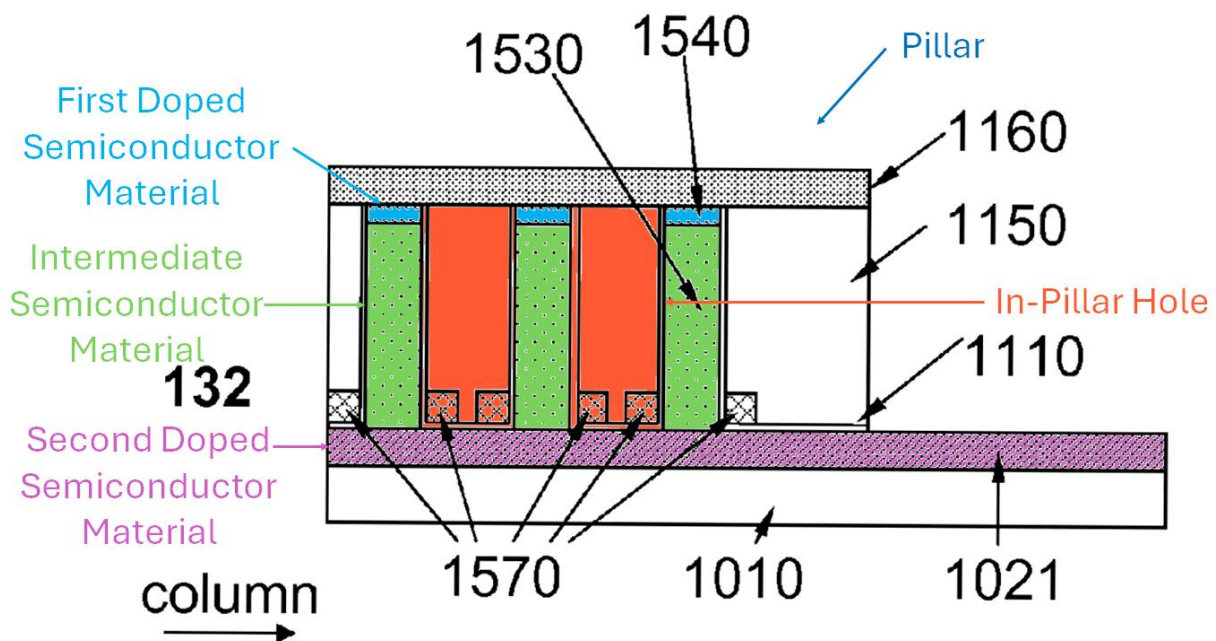
259. As I discussed for claim [1pre], *Yu*'s "nanopillars and the substrate can comprise suitable semiconductor materials and/or metals such as Si." *Yu*, ¶[55]; *supra* XI.B.1.a. *Yu* also discloses that "junction layer 1040, the epi layer 1030[,] and the HDL layer 1020 form a p-i-n, p-n, n-i-p, or n-p junction, depending on the doping profile." *Yu*, ¶[63]. In my opinion, because *Yu*'s first and second doped semiconductor materials and the intermediate semiconductor material are created in silicon nanopillars by doping, each region comprises silicon (Si). Specifically, in my opinion, *Yu*'s first doped semiconductor material (i.e., junction layer 1040), intermediate semiconductor material (i.e., epi layer), and its second doped semiconductor material (i.e., HDL layer) that are all formed in a silicon substrate comprise Si.

i. [1d]: "one or more deliberately formed in-pillar holes with solid dielectric therein;"

260. In my opinion, *Yu* discloses this limitation.

261. *Yu* discloses starting with a silicon-on-insulator (SOI)-type substrate. *Yu*, ¶[62]. *Yu* discloses forming an oxide layer, a heavily doped layer (HDL) on the oxide layer, and forming an epi layer on the HDL layer. *Yu*, ¶[62]. *Yu* also discloses forming a junction layer on the epi layer. *Yu*, ¶[63]. According to *Yu*, "the exposed portion of the junction layer 1040 and the portion of the epi layer 1030 directly therebelow are deep etched until the HDL layer 1020 directly below the exposed portion of the junction layer 1040 is exposed, to form nanopillars 1500."

Yu, ¶¶[68], [76]. In my opinion, one skilled in the art would have understood that the spaces between nanopillars are the **in-pillar holes** because they are formed by etching *Yu*'s semiconductor substrate. One skilled in the art would have also understood that the **in-pillar holes** formed in *Yu*'s substrate are deliberately formed because they are formed by a purposeful deep-etch process. *Yu*'s **photodetector device** (i.e., **image sensor**) with the deliberately formed **in-pillar holes** is illustrated below. As illustrated above, there are a plurality of (i.e., two) **in-pillar holes** in each **pillar**.



Yu, Fig. 1, step 132.

262. *Yu* also discloses that the “space between the nanopillars 1500 is filled by an **oxide** or a polymer 1150 such as **silicon oxide** or polyimide.” *Yu*, ¶[87]. As I explained above, **silicon oxide** is a **solid dielectric**. *Supra* XI.A.1.c; Ex. 1020, 34-

35; Ex. 1063, 20-21, 23. In my opinion, therefore, *Yu* discloses that *Yu*'s **in-pillar holes** are filled with **solid dielectric**.

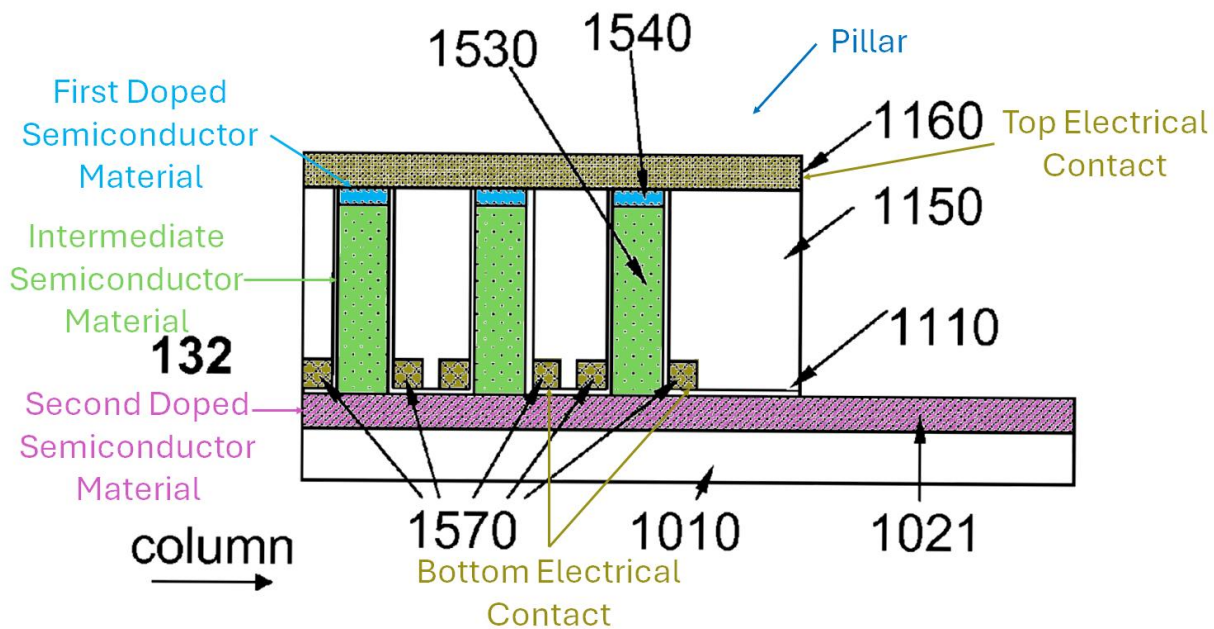
- j. [1e]: “**top and bottom electrical contacts** electrically coupled with said **array of pillars**, wherein said **photodetector device** is configured to respond to **light photons** incident on said **array of pillars** by **photo-generated charge carriers** therein; and”

263. In my opinion, *Yu* discloses this limitation.

264. *Yu* discloses that during formation of its image sensor, “a **metal layer 1140** is deposited” and that the “portion of the **metal layer 1140** deposited around the lower end of the nanopillars 1500 forms the gate electrodes and gate lines 1570.” *Yu*, ¶[85]. In my opinion, this **metal layer 1140** forms the **bottom electrical contacts** for *Yu*'s photodetector device. *Yu* discloses that its “image sensor can comprise first, second, third and fourth pixels.” *Yu*, ¶¶[9], [25], [51]. *Yu* also discloses that its pixels include at least one nanopillar. *Yu*, Abstract. *Yu* further discloses “a first **gate line** electrically connected to the gate electrodes of the first and third pixels and a second **gate line** electrically connected to the gate electrodes of the second and fourth pixels.” *Yu*, ¶¶[9], [25], [51]. One skilled in the art would have understood from these disclosures that *Yu*'s gate lines are connected to its nanopillars, which are included in *Yu*'s pillars. In my opinion, therefore, one skilled in the art would have also understood that *Yu*'s **bottom electrical contacts** (i.e., **gate lines**) are connected to *Yu*'s array of **pillars**.

265. *Yu* also discloses that “a transparent conductive layer (TCL) 1160, such as ITO or aluminum doped zinc oxide (AZO)[,] is deposited.” *Yu*, ¶¶[89], [27], [53]. In my opinion, the TCL layer is the image sensor’s top electrical contact. Because layer 1160 is deposited on *Yu*’s image sensor including a plurality of nanopillars, which are part of *Yu*’s pillars, *Yu*’s top electrical contact (i.e., TCL) is electrically connected to *Yu*’s array of pillars.

266. *Yu*’s top and bottom electric contacts are illustrated below.



Yu, Fig. 1, step 132.

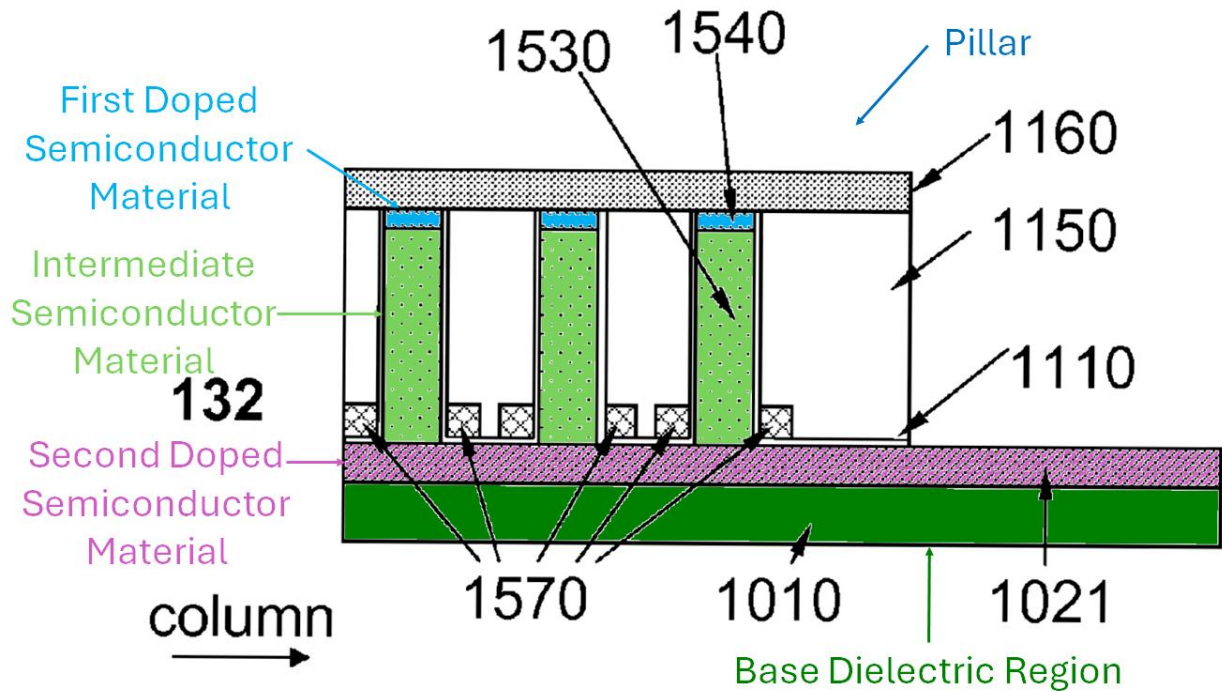
267. *Yu* discloses that its “image sensor can have large number of nanopillars.” *Yu*, ¶[60]. As I discussed for claim [1a], these nanopillars are arranged in an array of pillars. *Supra* XI.B.1.b. *Yu* also discloses that its “nanopillar [] can convert light impinging thereon to electrical signals.” *Yu*, ¶¶[48],

[17]. One skilled in the art would have understood that light impinging on *Yu*'s nanopillars would also impinge on *Yu*'s pillars. Thus, *Yu*'s image sensor (i.e., photodetector device) is configured to convert light photons (i.e., impinging light) incident on said array of pillars into electrical signals (i.e., photo-generated charge carriers).

- k. [1f]: “a base dielectric region that is below the array of pillars and comprises substantially solid dielectric material;”

268. In my opinion, *Yu* discloses this limitation.

269. *Yu* discloses “a silicon-on-insulator (SOI)-type substrate or silicon-on-glass (SG)-type substrate is provided.” *Yu*, ¶¶[62], [15], [102]. *Yu* explains that the “substrate has an oxide layer 1010.” *Yu*, ¶¶[62], [102]. In my opinion, one skilled in the art would have understood that oxide layer 1010 in *Yu*'s substrate is the base dielectric layer. This is for two reasons. First, as I discussed above, an oxide layer is a dielectric layer. *Supra* XI.A.1.c; Ex. 1020, 34-35; Ex. 1063, 20-21, 23. Second, as shown in the figure below, *Yu*'s oxide layer is disposed below *Yu*'s pillars. Therefore, in my opinion, the oxide layer 1010 in *Yu*'s substrate is the base dielectric layer.



Yu, Fig. 1, step 132.

270. Further, as discussed above, a skilled artisan would have understood that oxide layer 1010 is a solid because such a layer would be formed by oxidizing solid semiconductor materials using standard silicon fabrication processes, or at least would have found this configuration obvious, there being a motivation for it and a reasonable expectation of success in achieving it. *Supra* XI.A.1.k; Ex. 1020, 34; Ex. 1063, 20-21. In my opinion, therefore, one skilled in the art would have understood that *Yu*'s base dielectric layer (i.e., **oxide layer 1010**) is formed of a solid dielectric material.

- I. [1g]: “wherein the **pillars** of said **array of pillars**: are laterally spaced center to center by no more than 10,000 nanometers; and have up-down lengths of said **intermediate semiconductor material** in the range of 100-5000 nanometers;”

271. In my opinion, *Yu* renders this limitation obvious.

272. *Yu* discloses that it “is related to U.S. patent application Ser. No. 12/204,686 (granted as U.S. Pat. No. 7,646,943)” (“’943 Patent,” Ex. 1055), and that the ’943 Patent and other applications are “incorporated by reference in their entirety.” *Yu*, ¶[1]. The ’943 Patent discloses that “each pixel containing an image sensor of the embodiments disclosed herein could be as small as 1 micron or less in pitch.” ’943 Patent, 10:50-54.

273. As explained for [1pre] and [1a], *Yu*’s **pixels** constitute the claimed **pillars** forming the **array of pillars**. *Supra* XI.B.1.a, XI.B.1.b. Further, because the ’943 Patent is incorporated by reference, *Yu* also discloses a pixel pitch—which is the same as the pitch between *Yu*’s pillars—of 1 μm or less.

274. In my opinion, one skilled in the art would have found it obvious to implement the ’943 Patent’s pixel pitch dimensions in *Yu*’s photodetector device. This is because pixel pitch of the order of 1 μm was well known in the art. As I explained above, one skilled in the art would have understood *Kuboi* as disclosing a pixel pitch of 1.65 μm , which is of the same order of magnitude as the pixel pitch disclosed by the ’943 Patent. *Supra* XI.A.1.1; *Kuboi*, ¶[185]. Similarly, Ex. 1012

discloses a pixel pitch of 2 μm for CMOS image sensors, which is also of the order of 1 μm . Ex. 1012, 2; Ex. 1013 (disclosing pixel sizes and pitch of 3 to 4 μm).

275. One skilled in the art would have understood that there is an increasing “demand for miniature electronic imaging devices, such as surveillance and telephone cameras.” Ex. 1015, 8. One skilled in the art would have also been aware of the desire to reduce pixel size and pixel pitch to reduce cost and mass of the optical components. Ex. 1013, 2. Moreover, one skilled in the art would have understood that reducing the pixel pitch would help to reduce the size of the image sensor, which would help reduce the cost and mass of the sensor, while meeting the demand for miniature imaging devices. *See* Ex. 1015, 8; Ex. 1012, 6 (disclosing that in mobile imaging applications, it was desirable to have small pixels to increase spatial resolution without increasing the areas of the sensor).

276. In my opinion, therefore, one skilled in the art would have found it obvious to implement a pixel pitch of the order of 1 μm as disclosed by the '943 Patent in *Yu*'s photodetector device to provide an image sensor of smaller size, reduced mass, and having increased spatial resolution. In my opinion, a skilled artisan would have had a reasonable expectation of success in doing so because photodetector devices with pixel pitch values of the order of 1 μm were well-known in the art.

277. A pixel pitch of 1 μm is equivalent to 1,000 nm, which corresponds to [pillars](#) “laterally spaced center to center by no more than 10,000 nanometers,” as claimed.

278. As I discussed for claim [1c.1], *Yu*’s [epi layer](#) is the claimed [intermediate semiconductor material](#). *Supra* XI.B.1.e. Furthermore, *Yu* discloses that its “[epi layer 1030](#) can be about 3000 to 10000 nm thick.” *Yu*, ¶[62]. Thus, the thickness range disclosed by *Yu* (i.e., 3000 to 10000 nm) partially overlaps with the claimed range of 100 to 5000 nm. One skilled in the art would have understood that any of *Yu*’s photodetector devices having an [epi layer 1030](#) with a thickness of 3000 to 5000 nm would fall within the claimed thickness range.

279. Moreover, the ’360 Patent fails to disclose that the claimed range is critical to the claimed photodetector device’s operation. In my opinion, therefore, one skilled in the art would have understood that *Yu* renders the claimed range obvious because at least some of *Yu*’s photodetector devices would have an [intermediate semiconductor material](#) of thickness falling within the claimed range of 100-5000 nm. In my opinion, one skilled in the art would have had a reasonable expectation of success in forming a photodetector device having an [epi layer 1030](#) (i.e., [intermediate semiconductor material](#)) with a thickness in the claimed range of 100-5000 nm because *Yu* already discloses devices having [epi layer 1030](#) with a thickness ranging between 3000-5000 nm, which fall within the claimed range.

- m. [1h]: “wherein at least said **pillars**, **in-pillar holes**, and **solid dielectric** between at least portions of **sidewalls** of adjacent **pillars** of said **array of pillars** increase photon absorption of said device of incident light by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said one or more **in-pillar holes**;

280. In my opinion, *Yu* discloses or at least renders this limitation obvious in view of the knowledge of a person of ordinary skill in the art.

281. As I explain below, one skilled in the art would have found this limitation disclosed based on Patent Owner’s statements in the ’360 Patent. The Patent Owner represents in the ’360 Patent that an imaging device having the structure disclosed in *Yu* would improve photon absorption by at least 10%.

282. *Yu* discloses minimum feature size of 50 nm when etching the in-pillar holes. *Yu*, ¶[65]. In my opinion, one skilled in the art would have understood from this disclosure that *Yu* discloses spacing between its nanopillars is of the order of 50 nm. *Yu* also discloses that more preferably its nanopillars have dimensions of 90-150 nm. *Yu*, ¶[57]. Thus, *Yu* discloses that preferably the period Λ or center-to-center distance between its in-pillar holes ranges between about 140-200 nm.

283. As I discussed above, one skilled in the art would have understood that visible light has a wavelength range of 400-700 nm and infrared light has a wavelength range of 750 nm to 1000 μm or even 2000 μm . *Supra* XI.A.1.m.

Further, as I discussed above, one skilled in the art would have understood that the refractive index n_1 of silicon ranges between about 3.0 to 5.9 (Ex. 1056, 9:43-46, Fig. 4) and varies with wavelength. Ex. 1061, 48; *supra* XI.A.1.m. For example, the refractive index n_1 of silicon is about 5.8 for light of wavelength 400 nm, 3.7 for light of wavelength 700-750 nm, and about 3.5 for light of wavelength 1000 nm. Ex. 1061, 49; *supra* XI.A.1.m. One skilled in the art would also have understood that the refractive index n_2 of silicon dioxide in *Yu*'s nanopillars would be about 1.5 for the wavelength range of 400 nm to 1000 nm. Ex. 1062, 6, Fig. 1; Ex. 1056, 9:43-46, Fig. 4.

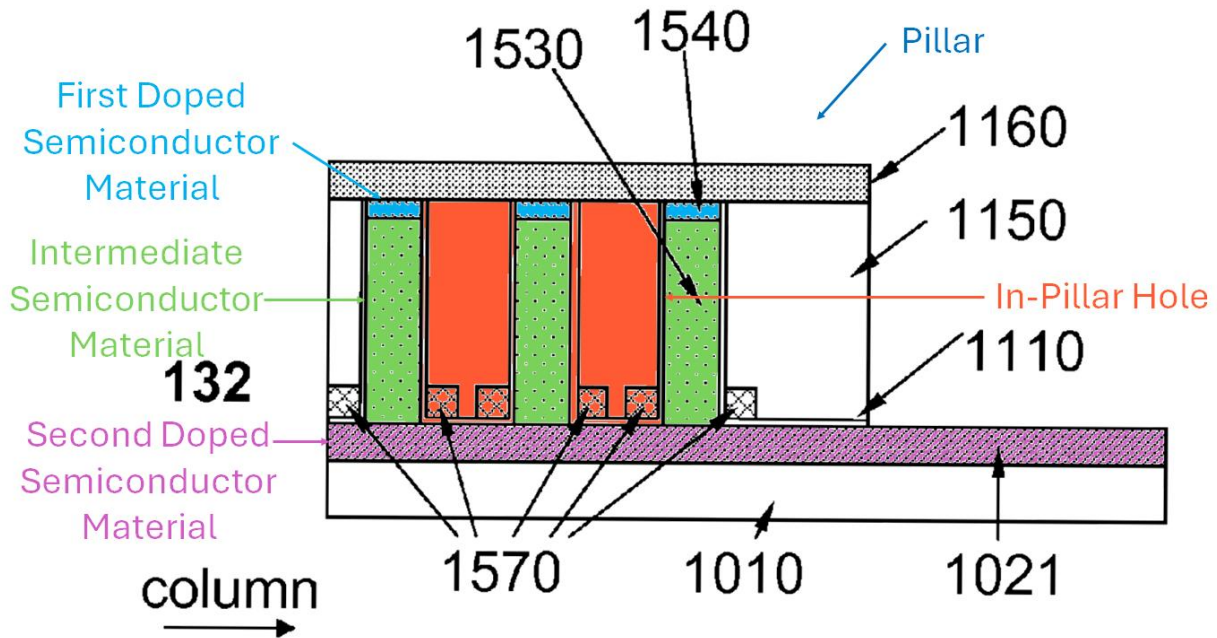
284. Below, I have provided a table (Table F) showing calculated values of λ/n_1 and λ/n_2 for visible light wavelengths of 400 nm and 700 nm, and near infrared wavelengths of 750 nm and 1000 nm.

285. I obtained values of λ/n_1 and λ/n_2 in Table F, using values of n_1 of silicon for different wavelengths from Ex. 1061, page 48, Table A-1, and values of n_2 of 1.5. As seen from the values in Table F, *Yu*'s hole pitch of 140-200 nm falls within the range λ/n_1 to λ/n_2 for at least a portion of the visible light spectrum. For example, for the 550 nm green light wavelength, λ/n_1 ($550/4.5 = 123$) $< \Lambda$ (140-200 nm) $< \lambda/n_2$ ($550/1.5 = 367$). Similarly, for example, for the 650 nm red light wavelength, λ/n_1 ($650/3.9 = 168$) $< \Lambda$ (200 nm) $< \lambda/n_2$ ($650/1.5 = 467$).

Table F				
λ (nm)	n_1 (Silicon)	n_2 (Dielectric)	λ/n_1(nm)	λ/n_2 (nm)
400	5.8	1.5	68	267
550	4.5	1.5	123	367
650	3.9	1.5	168	433
700	3.8	1.5	184	467

286. Thus, the stated period of *Yu*'s in-pillar hole array falls within the λ/n_1 to λ/n_2 range for "selected visible and infrared wavelength ranges." Further, in my opinion, based on Patent Owner's representations, *Yu*'s in-pillar hole structure would form a HCG. And, based on those same representations, in my opinion, such an HCG would produce an enhanced absorption coefficient of 1.1 to 100 times the bulk absorption coefficient based on the near-wavelength and deep-wavelength phenomena. In my opinion, therefore, one skilled in the art would have understood that consistent with Patent Owner's representations, *Yu*'s in-pillar holes increase photon absorption in *Yu*'s device by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said one or more in-pillar holes.

287. As I explain in detail below, in my opinion, one skilled in the art would have found Patent Owner's representations were consistent with those of other prior art teachings. *Yu*'s pixel with in-pillar holes is illustrated below.



Yu, Fig. 1, step 132.

288. Yu discloses that “**epi layer 1030** can be about 3000 to 10000 nm thick.” Yu, ¶[62]. Yu also discloses that “the thickness of the **junction layer 1040** is from 10 to 200 nm.” Yu, ¶[63]. Thus, one skilled in the art would have understood that each **in-pillar hole** of Yu has a depth ranging between 3,010-10,200 nm.

289. As I discussed above, Han discloses that “[t]o obtain the same ultimate efficiency as a standard 300 micrometer crystalline silicon wafer, nanohole arrays require less silicon by mass.” Han, Abstract, 2:4-5; *supra* XI.A.1.m. Han discloses that “nanoholes can be sized to substantially trap incident light.” Han, 3:2-3; *supra* XI.A.1.m. As shown in Figure 4 of Han below the ultimate efficiency for a device having a semiconductor thickness of about 3,010 nm (3.01 μm) without nanoholes is approximately 0.15, whereas the ultimate

efficiency for a similar device with nanoholes of 3,010 nm (3.01 μm) depth is approximately 0.27. In my opinion, before the earliest priority date of the '360 Patent, one skilled in the art would have understood that *Yu*'s nanohole depths of 3,010 nm (3.01 μm) would increase light absorption by a factor of 1.8 ($0.27/0.15 = 1.8$), which is significantly higher than a factor of 1.1.

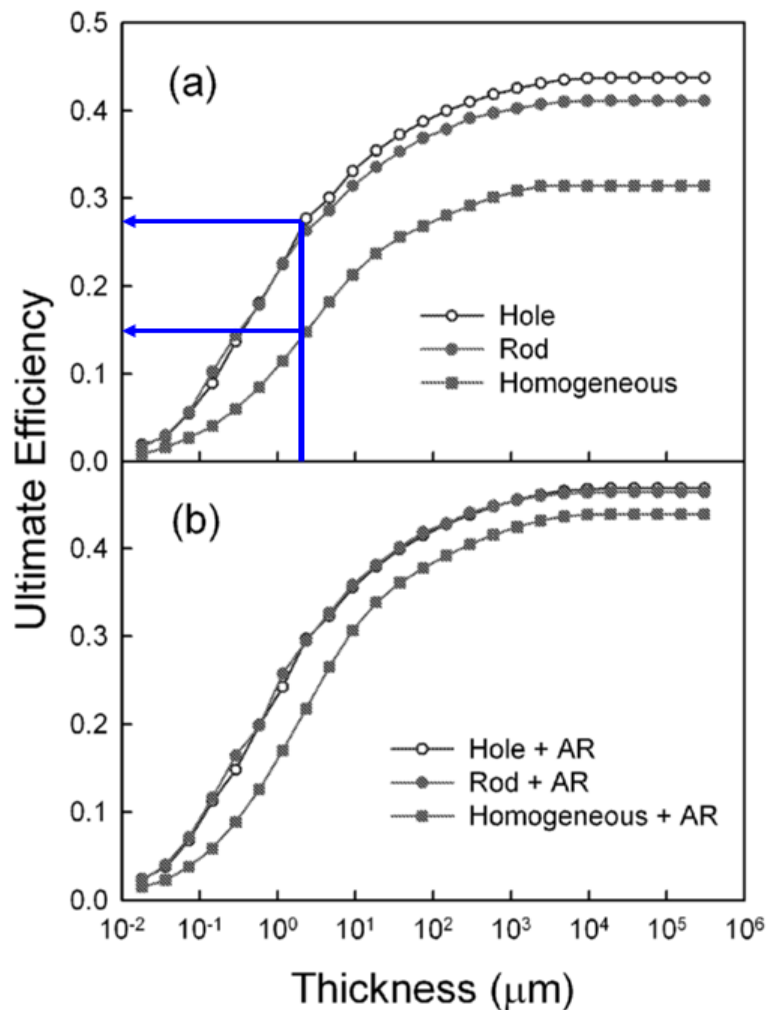


FIG. 4

290. Similarly, as shown in Figure 4 of *Han* below the ultimate efficiency for a device having a semiconductor thickness of about 10,200 nm (10.2 μm) is

approximately 0.22, whereas the ultimate efficiency for a similar device having a semiconductor with nanoholes of 10,200 nm (10.2 μm) depth is approximately 0.33. In my opinion, before the earliest priority date of the '360 Patent, one skilled in the art would have understood that *Yu*'s nanohole depths of 10,200 nm (10.2 μm) would increase light absorption by a factor of 1.5 ($0.33/0.22 = 1.5$), which is significantly higher than a factor of 1.1.

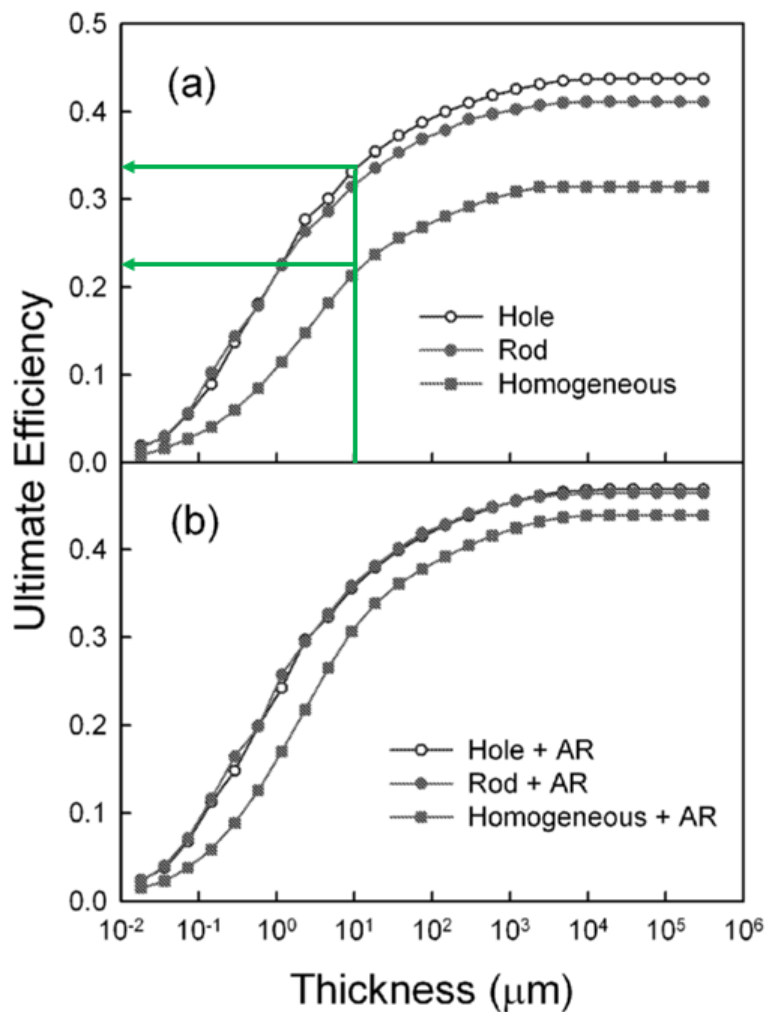


FIG. 4

Han, Fig. 4.

291. In my opinion, based on a skilled artisan's knowledge of the state of the art before the earliest priority date of the '360 Patent, the skilled artisan would have understood that *Yu*'s in-pillar holes of 3,010-10,200 nm would increase photon absorption in *Yu*'s device by at least 1.1 times compared to a like device that did not include the in-pillar holes, and even if not readily understood, a POSITA would have found such a result not only obvious but also one having a reasonable expectation of success in achieving this increase because *Yu* already discloses forming in-pillar holes ranging in depth from 3,010-10,200 nm.

- n. [1i]: “wherein said **array of pillars** is monolithically integrated in or on said **semiconductor substrate** with **electronic circuits that include active elements for signal processing and transmission.**”

292. In my opinion, *Yu* discloses this limitation.

293. *Yu* discloses an apparatus comprising the image sensor and a control circuit that includes a decoder, a transimpedance amplifier, a multiplexer circuit, and other readout circuitry components. *Yu*, ¶[115]. *Yu* also discloses that its control circuit can comprise other components such as an analog-to-digital converter, an exposure controller, and a bias voltage circuit. *Yu*, ¶[115]. One skilled in the art would have understood that at least the transimpedance amplifier and analog-to-digital convertor would include circuit elements for signal processing. One skilled in the art would have also understood that the readout circuitry components would include circuit elements for transmission of the signal.

In my opinion, therefore, *Yu*'s control circuit includes elements for signal processing and transmission.

294. *Yu* also discloses that the “image sensor and the control circuit can be formed as an integrated circuit or chip.” *Yu*, ¶[115]. In my opinion, one skilled in the art would have understood that forming the image sensor and control circuit as an “integrated circuit” indicates that *Yu*'s pixels (part of the image sensor) are monolithically integrated with the control circuit on the same chip or substrate. Ex. 1067, 6 (defining integrated circuit as “an assembly of miniature electronic components simultaneously produced in batch processing, on or within a single substrate, that performs an electronic circuit function” or “many transistors, resistors, capacitors, etc., fabricated and connected together to make a circuit on one monolithic slab of semiconductor material.”

295. To the extent Patent Owner argues that *Yu* does not disclose monolithic integration, the *Yu-Shinohara* combination renders obvious [1i].

296. As discussed above, *Shinohara* discloses forming a pixel region, a peripheral circuit portion, pixel transistors, and a wiring layer on the same substrate. *Shinohara*, ¶¶[68]-[82]; *supra* VIII.B, XI.A.1.n.iii. In my opinion, one skilled in the art would have found it obvious to combine *Shinohara*'s teachings with *Yu*, resulting in an imaging device in which *Yu*'s image sensor (i.e., pixel region) is monolithically integrated with its control circuit that includes active

elements for signal processing and transmission for at least reasons similar to those discussed with respect to the *Kuboi-Shinohara* combination (*supra* XI.A.1.n.iii) and for the additional reasons discussed below.

i. Motivation to modify *Yu*'s image sensor in view of *Shinohara*'s teaching of monolithic integration

297. As discussed above, *Shinohara* is analogous art to the '360 Patent. *Supra* XI.A.1.c.i. *Yu* is also analogous art to the '360 Patent. Like the '360 Patent and *Shinohara*, *Yu* discloses an image sensor having a plurality of pixels. *Yu*, Abstract, ¶¶[7], [17], [48], [52]. *Yu* is analogous art to the '360 Patent because, like the '360 Patent, *Yu*'s image sensor also includes features to improve light absorption. *Yu*, ¶[133].

298. *Shinohara* discloses forming a pixel region, a peripheral circuit portion, pixel transistors, and a wiring layer on the same substrate. *Shinohara*, ¶¶[68]-[82]; *supra* XI.A.1.n.iii. As I discussed above, one skilled in the art would have understood that *Shinohara*'s monolithic integration lowers manufacturing costs, reduces package size, allows high bandwidth operation, improves power efficiency, and enables high-frequency mixed-signal processing. *Supra* XI.A.1.n.iii; *Hasegawa*, ¶[9]; *Michel*, Abstract; *Beals*, 2; *NXP*, ¶¶[16], [32], [37]. In my opinion, one skilled in the art, therefore, would have been motivated to use *Shinohara*'s teaching of monolithic integration to manufacture and further improve

Yu's imaging device and achieve the above-identified benefits such as high bandwidth and low manufacturing cost and package size. In my opinion, one skilled in the art would have found that that using *Shinohara*'s monolithic integration in *Yu* would involve nothing more than the use of a known technique (namely forming *Yu*'s image sensor and all associated electronic circuitry on the same substrate as taught by *Shinohara*), to improve a similar device (namely *Yu*'s imaging device), in the same way (namely, by improving manufacturing reliability, reducing manufacturing cost and package size, reducing signal attenuation, reducing noise, and improving high-bandwidth performance) of *Yu*'s device.

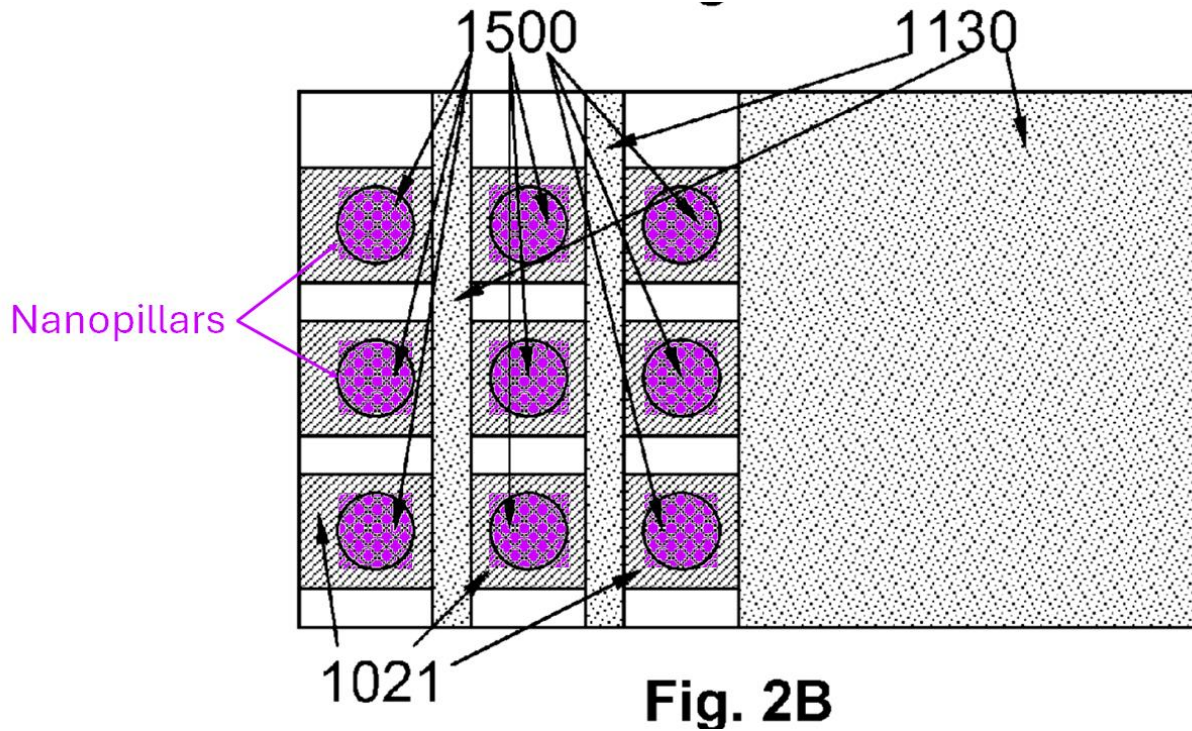
299. *Yu* and *Shinohara* disclose imaging devices that include a pixel region (or image sensor) and a peripheral circuit portion (or control circuit). In my opinion, therefore, manufacturing *Yu*'s image sensor and control circuit, using *Shinohara*'s monolithic integration techniques would have been well within the skill level of a person of ordinary skill in the art. Further, in my opinion, a skilled artisan would have had a reasonable expectation of success in implementing *Shinohara*'s teachings for manufacturing *Yu*'s imaging device because it merely requires combining well-known prior elements and manufacturing methods taught by *Shinohara*.

300. To summarize, in my opinion, *Yu* alone discloses the limitations of claim [1i]. Alternatively, in my opinion, the combination of the teachings of *Yu* and *Shinohara* discloses and renders obvious the limitations of claim [1i].

2. Claim 8: “The photodetector device of claim 1, in which each of said pillars has at least two of said one or more in-pillar holes that partly overlap.”

301. In my opinion, *Yu* discloses this additional limitation.

302. *Yu* discloses that “the exposed portion of the junction layer 1040 and the portion of the epi layer 1030 directly therebelow are deep etched until the HDL layer 1020 directly below the exposed portion of the junction layer 1040 is exposed, to form nanopillars 1500.” *Yu*, ¶[68]. *Yu* also discloses that “nanopillars can have any suitable cross-sectional shape such as a circle, a square, [or] a hexagon.” *Yu*, ¶[57]. *Yu* discloses a plan view or top view of its image sensor. *Yu*, ¶[42]. Figure 2B illustrates this plan view. Below, I have illustrated Figure 2B for the configuration where each nanopillar has a generally square or rectangular cross-sectional shape. *Yu*, ¶[57].



Yu, Fig. 2B.

303. In my opinion, one skilled in the art would have understood that *Yu*'s square- or rectangular-shaped nanopillars, as illustrated above, would be formed by deep etching a substrate (*Yu*, ¶¶[68], [76]), to form trenches oriented generally perpendicular to each other. One skilled in the art would have arrived at this conclusion based on *Yu*'s own disclosures. For example, after forming a junction layer on the epi layer, *Yu* discloses applying a layer of resist 1050 on the junction layer 1040. *Yu*, ¶[64]. *Yu* further discloses performing lithography to create a pattern of openings in which the junction layer 1040 is exposed. *Yu*, ¶[65]. *Yu* explains that the openings are preferably dots, squares, or circles in shape and correspond to the shapes and locations of the nanopillars. *Yu*, ¶[65]. Further, *Yu*

discloses depositing a mask layer 1060 and then the mask layer 1060 and resist layer 1050 are removed such that mask layer 1060 is retained in the openings. *Yu*, ¶¶[66]-[67]. The figure below discloses this configuration.

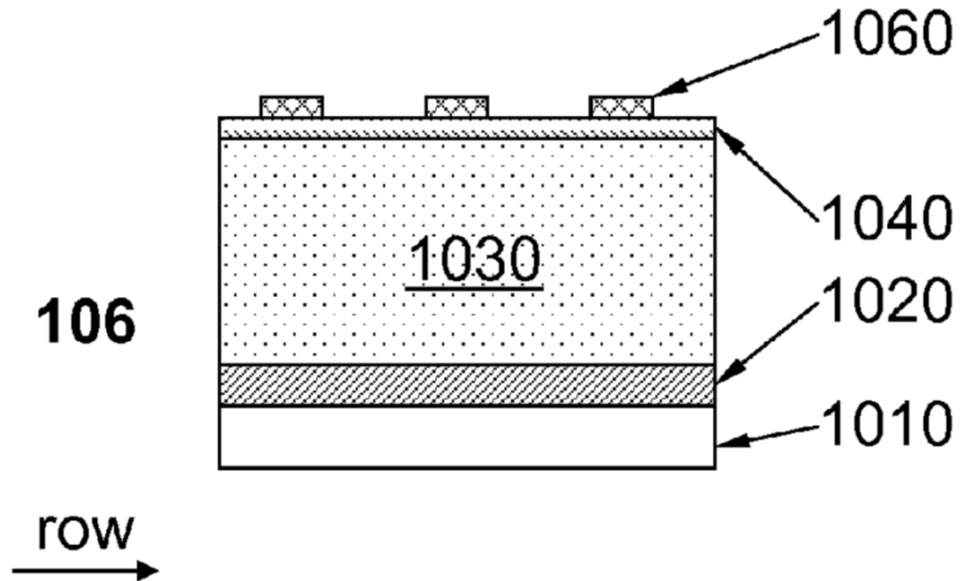
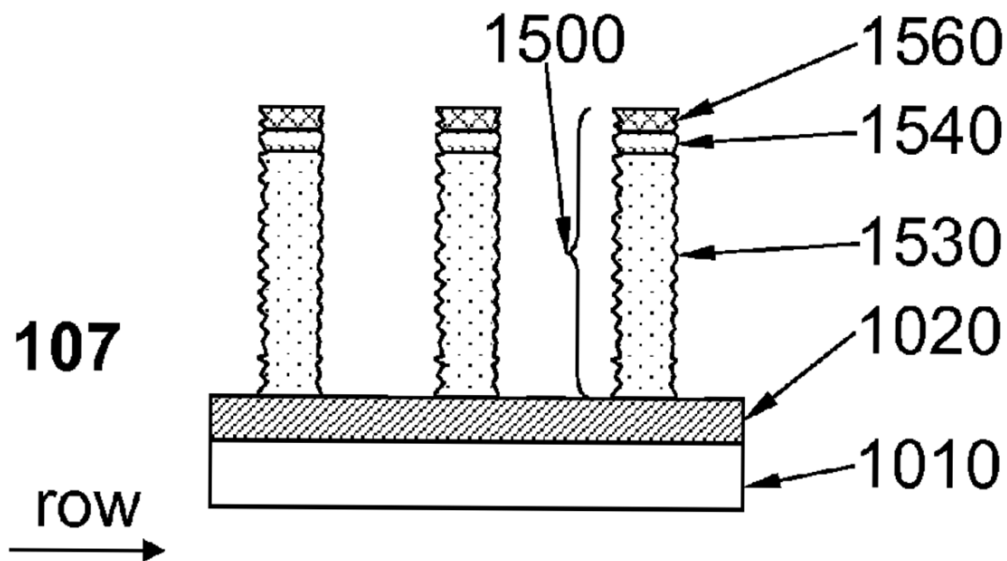


Fig. 1

Yu, Fig. 1, step 106.

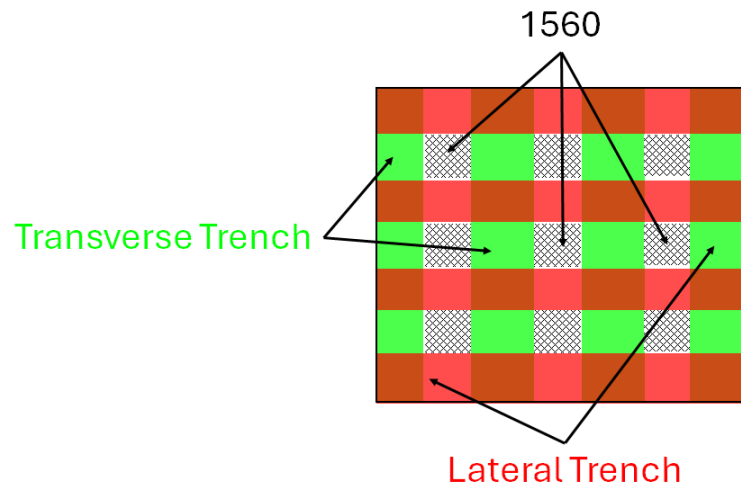
304. *Yu* further discloses that in step 107, “the exposed portion of the junction layer 1040 and the portion of the epi layer 1030 directly therebelow are deep etched until the HDL layer 1020 directly below the exposed portion of the junction layer 1040 is exposed, to form nanopillars 1500.” *Yu*, ¶[68]. *Yu* explains that each nanopillar 1500 now has a mask layer 1560 which is part of the mask layer 1060. *Yu*, ¶[68]. This configuration is illustrated below.



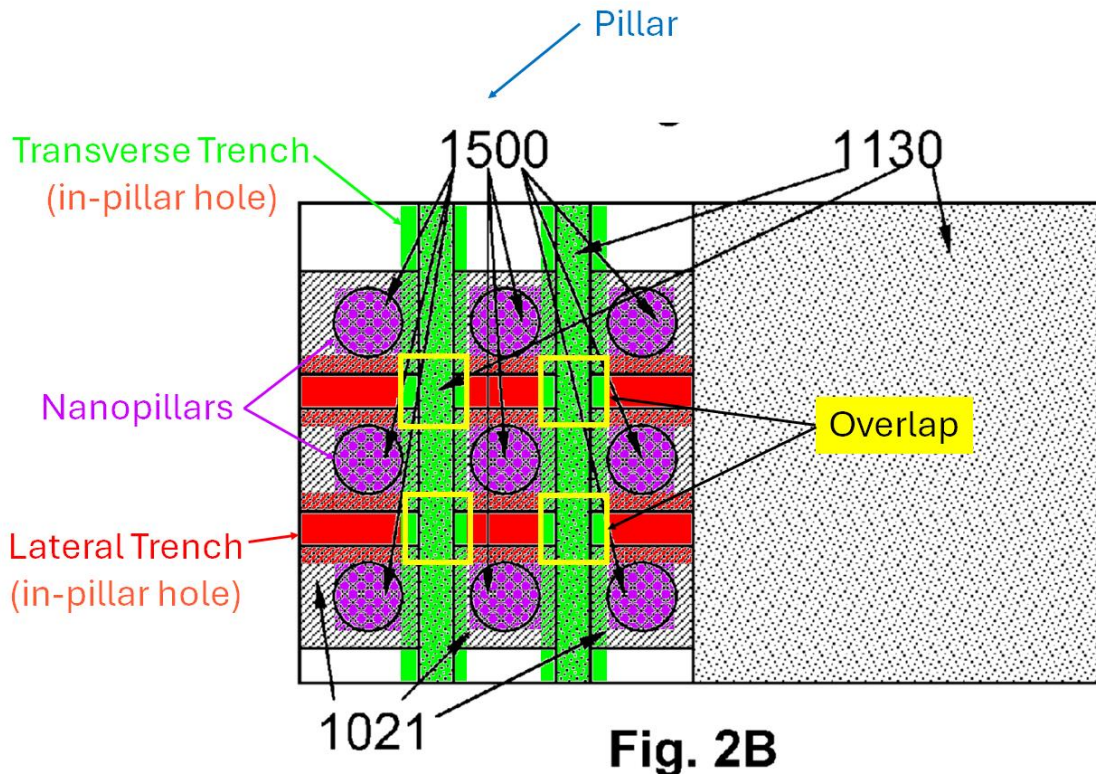
Yu, Fig. 1, step 107.

305. In my opinion, one skilled in the art would have understood that the above figures illustrating steps 106 and 107 are cross-sectional views. In my opinion, one skilled in the art would also have understood that when the openings in which the junction layer 1040 have square shapes, and when the semiconductor material around those openings are deep etched as disclosed by *Yu*, such etching would produce a plurality of **trenches in a lateral direction**, and a plurality of **trenches in a transverse direction** extending across the **trenches in the lateral direction**, leaving square shaped nanopillars as disclosed by *Yu*. I have illustrated a cartoon showing a top view that would correspond to step 107 above, to show how the mask layer 1560 allows for formation of the square nanopillars formed by etching of the **trenches in the lateral direction** and the **trenches in the transverse**

direction. As seen in the figure below, the mask layer 1560 prevents etching of the semiconductor layer in the portions covered by the mask layer. Other portions of the semiconductor layer are etched into the **trenches in the lateral direction** and the **trenches in the transverse direction** forming nanopillars having square cross-sections defined by the mask layer 1560.



306. I have illustrated similar trenches (or **in-pillar holes**) including a plurality of **trenches in a lateral direction** and a plurality of **trenches in a transverse direction** in Figure 2B below.



Yu, Fig. 2B.

307. In my opinion, one skilled in the art would have also understood that the **trenches in the lateral direction** and the **trenches in the transverse direction** formed in the deep etching step would overlap at their intersection portions. This is illustrated by the **yellow rectangles** in the above figure, showing where the **trenches** (or **in-pillar holes**) **in the lateral direction** partly **overlap** with the **trenches** (or **in-pillar holes**) **in the transverse direction**. In my opinion, therefore, Yu discloses the additional limitations of claim 8.

3. **Claim 9: “The photodetector device of claim 1, in which said second doped semiconductor material comprises a laterally continuous region coupled to a plurality of said pillars.”**

308. In my opinion, Yu discloses this additional limitation.

309. As I discussed for claim [1b.2], the HDL disposed on *Yu*'s substrate's oxide layer constitutes the claimed second doped semiconductor material. *Supra* XI.B.1.d. *Yu* also discloses that HDL layer 1020 is segmented into readout lines. *Yu*, ¶[76]. Further, *Yu* discloses that its "image sensor can comprise first, second, third[,] and fourth pixels, a first readout line electrically connected to the first and second pixels, [and] a second readout line electrically connected to the third and fourth pixels." *Yu*, ¶[9], [25], [51].

310. As I discussed for claim [1a], each pixel in *Yu*'s image sensor corresponds to a claimed pillar. *Supra* XI.B.1.b. In my opinion, one skilled in the art would have understood that the first readout line must be continuous to be connected to two pixels. Similarly, one skilled in the art would have understood that the second readout line must be continuous to be connect to two pixels. Further, in my opinion, each readout line must extend laterally between the two pixels to be connected to two pixels. In my opinion, because the first and second readout lines each extend between and are connected to at least two pixels, *Yu*'s first or second readout line (i.e., second doped semiconductor material) is laterally continuous and is connected to more than one pillar (i.e., to more than one pixel).

XII. CONCLUSION

311. For the reasons set forth above, it is my opinion that one skilled in the art would have found claims 1, 3, 5, 6, 8, and 9 of the '360 Patent obvious over the

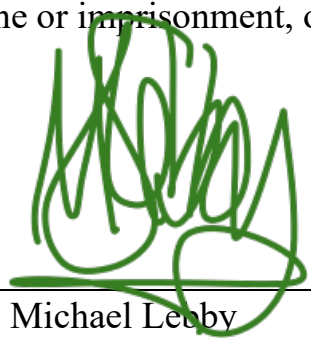
prior art. My opinion would remain the same even if the level of skill in the art was slightly lower (e.g., requiring only a bachelor's degree instead of a master's degree).

XIII. DECLARATION

312. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

313. I declare that all statements made herein of my knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001.

Date: June 18, 2025

By: 
Michael Leiby