UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/707,429	04/04/2023	11621360	309-0011USDIVCIP2	1214

139982 7590 03/15/2023

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site http://pair.uspto.gov for additional inventors):

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping WANG, Los Altos, CA;

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

W&WSENS DEVICES, INC., Los Altos, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17707429
Filing Date	2022-03-29
First Named Inventor	Shih-Yuan WANG
Art Unit	
Examiner Name	Eduardo A. Rodela
Attorney Docket Number	309-0011USDIVCIP2

Change(s) applied to document,6
/J.E.B./
11/3/2022

	20180102442		2018-04-12	Wang, et al.

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Copy of International Search Report and Written Opinion for PCT/US2020/051733 mailed December 17, 2020.	
	2	Copy of Written Opinion of International Search Report for PCT/US2020/051733 dated December 17, 2020.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/Hoang-Quan Ho/	Date Considered	06/16/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

EFS Web 2.1.18

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/707,429	03/29/2022	Shih-Yuan WANG	309-0011USDIVCIP2	1214

139982 7590 02/28/2023

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER
HO, HOANG QUAN TRAN

ART UNIT	PAPER NUMBER
2818	

NOTIFICATION DATE	DELIVERY MODE
02/28/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Wissing Miller LLP
Industrious at Hudson Yards 31 Hudson Yards, 11th Floor
New York, NY 10001

In re Application of W&WSENS DEVICES, INC.
Application No.: 17/707,429
Filing Date: 29 March 2022
Attorney Docket No.: 309-0011USDIVCIP2
For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

DECISION ON PETITION UNDER 37 CFR 1.78(e)

TThis is a decision on the petition under 37 CFR 1.182 to expedite the concurrently filed petition under 37 CFR 1.78(e), filed 05 January 2023, to accept an unintentionally delayed claim under 35 U.S.C. 120 for the benefit of priority to one or more prior-filed nonprovisional or international applications.

Applicants seek to change the relationship between non-provisional application 15/797,821 and 14/947,718 from a continuation-in-part of to a continuation. Applicants provide an Application Data Sheet, in compliance with 37 C.F.R. 1.76, which reflects this benefit claim.

MPEP 211.03 states that "[a] petition under 37 CFR 1.78 and the surcharge would not be required for correcting a timely submitted benefit claim for the following situations:_(A) Changing the relationship of the applications (e.g., changing from "continuation" or "divisional" to " continuation-in-part" or from "continuation-in-part" to "continuation" or "divisional"). . ." Accordingly, a petition is not required to change the relationship of the application from one recognized relationship to another.

Although the petition is not required to change the relationship, a filing receipt that reflects the benefit claim within the ADS cannot be issued at this time. MPEP 211.01(b), Section II. states, " Benefit Claims to Multiple Prior Applications", "Sometimes a pending application is one of a series of applications wherein the pending application is not copending with the first filed application but is copending with an intermediate application entitled to the benefit of the filing date of the first application. . . . Appropriate references must be made in each intermediate application in the chain of prior applications." Before the petition can be granted, each intermediate application must be amended to include an appropriate reference to the application.

In the present case, prior intermediate application 17/532,831 and 17/182,954 do not contain a proper benefit claim as indicated in the ADS in the present application. While applicant has filed petitions under 37 CFR 1.78 in each application, the applications have been dismissed. Until a petition under 37 CFR 1.78 has been granted in the intermediate applications and a proper benefit claim is recognized to all the applications, the benefit claim in the present application cannot be recognized and filing receipt cannot be issued.

For the reasons above, the petition under 37 CFR 1.78(e) is **DISMISSED AS MOOT.**

Applicant is advised that the inclusion of a prior-filed application on any filing receipt should not be construed as meaning that the present application is necessarily entitled to the benefit of the prior-filed application. In order for an application to be entitled to the benefit of the prior-filed application, all other requirements under 35 U.S.C. 120 and 37 CFR 1.78 must be met.

This matter is being referred to the Office of Publications for appropriate action.

/ANISH GUPTA/
ANISH GUPTA
PCT Legal Examiner
International Patent Legal Administration
(571)272-0965

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

139982 7590 11/02/2022

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Mary Ellen Finnegan	(Typed or printed name)
/Mary Ellen Finnegan/	(Signature)
February 1, 2023	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/707,429	03/29/2022	Shih-Yuan WANG	309-0011USDIVCIP2	1214

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	02/02/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
HO, HOANG QUAN TRAN	2818	257-431000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Wissing Miller LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: W&W Sens Devices, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Los Altos, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 600125

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Ivan S. Kavrukov/ Date February 1, 2023

Typed or printed name Ivan S. Kavrukov Registration No. 25,161

Samsung Exhibit 1003, Page 6 of 516

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Shih-Yuan WANG
Serial No.:	17/707,429
Filing Date:	March 29, 2022
Art Unit:	2818
Confirmation No.:	1214
Examiner:	Tran Quan Hoang Ho
For:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

31 Hudson Yards, 11th Floor
New York, New York 10001

CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: February 1, 2023

I hereby certify that this correspondence is being transmitted via Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL LETTER ACCOMPANYING ISSUE FEE PAYMENT

Submitted herewith for filing in the U.S. Patent and Trademark Office are the following:

☒ Part B – Issue Fee Transmittal;
☒ Payment by credit card and Authorization to charge Deposit Account 600125 in payment of any fee deficiencies;

Applicant Comments to Examiner's Statement of Reasons for Allowance

The applicant recognizes that in accordance with M.P.E.P. § 1302.14, the Examiner's reasons for allowance need not set forth all of the details as to why the claims are allowed. In the above identified application, the applicant does not concede that the examiner's stated reasons for allowance are the only reasons for which the claims are allowable. In particular, the applicant does not concede

that all of the recited limitations are necessary to distinguish the prior art of record or to satisfy the requirements of 35 U.S.C. § 112. In addition, the dependent claims are allowable on their own merits, and are allowable on the basis of a sub-combination of the recited features of the dependent claims and their respective base claims.

If there are any questions regarding this submission, the Examiner is encouraged to contact the undersigned via telephone at (917) 945-0121. I hereby authorize the USPTO to communicate any subject matter of this application by electronic mail at [wmdocket@wissingmiller.com]. I understand that a copy of these communications will be made of record in the application file.

By: /Ivan S. Kavrukov/
Ivan S. Kavrukov
Reg. No. 25,161
Tel. (917) 945-0121

Date: February 1, 2023
Address: (associated with Customer Number: 139982)
31 Hudson Yards, 11th Floor
New York, New York 10001
Attorney's Telephone No.: (917) 945-0121

Electronic Acknowledgement Receipt

EFS ID:	47465100
Application Number:	17707429
International Application Number:	
Confirmation Number:	1214
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	139982
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	309-0011USDIVCIP2
Receipt Date:	01-FEB-2023
Filing Date:	29-MAR-2022
Time Stamp:	17:48:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$600
RAM confirmation Number	E202321H49244565
Deposit Account	600125
Authorized User	Mary Ellen Finnegan
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	309-0011USDIVCIP2_Issue_Fee - Ltr_WithStatementOfAllowance-signed.pdf	513402 9e0e4f2a66848b420cc8b6901a480d39ce4116cc	no	2
Warnings:					
Information:					
2	Issue Fee Payment (PTO-85B)	309-0011USDIVCIP2_IssueFeeTransmit.pdf	141580 734bd807c56a545df7d2959a2a666e12f7ee4e50	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	38134 069b82151082389fc7ce9f82581bba8360f359aa	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	693116		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Patent Application Fee Transmittal

Application Number:	17707429
Filing Date:	29-Mar-2022
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Attorney Docket Number:	309-0011USDIVCIP2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	2501	1	600	600

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**600**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Shih-Yuan WANG
Serial No.:	17/707,429
Filing Date:	March 29, 2022
Art Unit:	2818
Confirmation No.:	1214
Examiner:	HOANG QUAN TRAN HO
For:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, New York 10001

CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: January 5, 2023

I hereby certify that this correspondence is being transmitted via Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

STATEMENT ACCOMPANYING PETITION

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits a Petition under 37 CFR §1.78 to Accept an Unintentionally Delayed Claim Under 35 U.S.C. 119(e) for the Benefit of Prior-Filed Provisional Applications. Applicant has already received the benefit claim and is only changing the continuity type from "continuation" to --continuation-in-part-- of one of the benefit claims. Attached is a corrected

Application Data Sheet correcting the continuity type of a benefit claim.

The entire delay between the date the benefit claim was due under section 37 CFR 1.78 (a)(4) and the date the benefit claim was filed was unintentional and due to a clerical error.

The Office is hereby authorized to charge any other fees that may be required in connection herewith and to credit any overpayment to our Deposit Account No. 600125.

Respectfully Submitted,

WISSING MILLER LLP

Attorney for Applicants

By: /Ivan S. Kavrukov/

Ivan S. Kavrukov
Reg. No. 25,161
Tel: (917) 945-0121

Doc Code: PET.OP
Document Description: Petition for Review by the Office of Petitions

PTO/SB/445 (09-22)
Approved for use through 05/31/2024. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION TO ACCEPT AN UNINTENTIONALLY DELAYED CLAIM UNDER 35 U.S.C. 119(e) (37 CFR 1.78(c)) AND/OR TO ACCEPT AN UNINTENTIONALLY DELAYED CLAIM UNDER 35 U.S.C. 120, 121, 365(c), or 386(c) (37 CFR 1.78(e)) FOR THE BENEFIT OF A PRIOR-FILED APPLICATION

First named inventor: Shih-Yuan WANG

Application No.: 17/707,429 Art Unit: 2818

Filed: March 29, 2022 Examiner: HOANG QUAN TRAN HO

Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Attention: Office of Petitions
Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
FAX 571-273-8300

When filing via USPTO's patent electronic filing systems, use Doc Code PET.PCT (Petition for review by the PCT Legal Office) for applications filed under 35 U.S.C. 371 and/or if the reference to the prior-filed application(s) includes an international application or an international design application. In all other instances, use Doc Code PET.OP (Petition for review by the Office of Petitions).

NOTE: If information or assistance is needed in completing this form, please contact the Office of Petitions at 571-272-3282.

APPLICANT HEREBY PETITIONS FOR ACCEPTANCE OF AN UNINTENTIONALLY DELAYED BENEFIT CLAIM TO A PRIOR-FILED APPLICATION UNDER 37 CFR 1.78(c) AND/OR 37 CFR 1.78(e).

NOTE: For a petition under 37 CFR 1.78(e), the above-identified application must have been filed during the pendency of the prior application or during the pendency of an intermediate application similarly entitled to the benefit of the filing date of the prior application. For a petition under 37 CFR 1.78(c), the above-identified application must have been filed within 12 months of the filing date of the provisional application or be entitled to claim the benefit under 35 U.S.C. 120, 121, or 365(c) of an application that was filed within 12 months of the filing date of the provisional application, except as provided in 37 CFR 1.78(b).

NOTE: A grantable petition requires the following items:

(1) the reference required by 35 U.S.C. 119(e) and 37 CFR 1.78(a)(3) to the prior-filed provisional application and/or the reference required by 35 U.S.C. 120 and 37 CFR 1.78(d)(2) to the prior-filed nonprovisional application, international application designating the United States, or international design application designating the United States, unless previously submitted;
(2) the petition fee set forth in 37 CFR 1.17(m); and
(3) a statement that the entire delay between the date the benefit claim was due under 37 CFR 1.78(d)(3) and/or 37 CFR 1.78(a)(4) and the date the benefit claim was filed was unintentional. The Director may require additional information where there is a question as to whether the delay was unintentional.

1. The required reference to the prior-filed application:

☑ The above-identified application was filed on or after September 16, 2012, and the reference is either set forth in the attached corrected application data sheet (ADS) or in a corrected ADS that was previously submitted.

☐ The above-identified application was filed prior to September 16, 2012, and the reference is either (1) set forth in a supplemental ADS, (2) set forth in the attached amendment to the first sentence(s) of the specification, or (3) set forth in a supplemental ADS or amendment to the first sentence(s) of the specification that was previously submitted. See 37 CFR 1.78(h).

Reminder: Any ADS which corrects or updates the information of record must comply with 37 CFR 1.76(c)(2) (or for applications filed prior to September 16, 2012, pre-AIA 37 CFR 1.76(c)).

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0032. Public burden for this form is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PETITION TO ACCEPT AN UNINTENTIONALLY DELAYED CLAIM UNDER 35 U.S.C. 119(e) (37 CFR 1.78(c)) AND/OR TO ACCEPT AN UNINTENTIONALLY DELAYED CLAIM UNDER 35 U.S.C. 120, 121, 365(c), or 386(c) (37 CFR 1.78(e)) FOR THE BENEFIT OF A PRIOR-FILED APPLICATION

2. Petition fee (37 CFR 1.17(m)):

☐ Other than a small or micro entity (undiscounted) fee $ _____ (Fee Code 1454).

☐ Small entity fee $ _____ (Fee Code 2454). Applicant asserts small entity status. See 37 CFR 1.27.

☐ Micro entity fee $ _____ (Fee Code 3454). Applicant has established or is establishing micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

3. Statement: The entire delay between the date the benefit claim was due under 37 CFR 1.78(d)(3) and/or 37 CFR 1.78(a)(4) and the date the benefit claim was filed was unintentional.

Petitioner is reminded that a change in circumstance or a delay resulting from a deliberately chosen course of action does not become an "unintentional" delay because, for example:

- the applicant does not consider any patent to be of sufficient value to justify the financial expense of obtaining the patent; or
- the applicant remains interested in eventually obtaining a patent, but simply seeks to defer patent fees and patent prosecution expenses.

NOTE: Where the petition under 37 CFR 1.78(c) and/or 37 CFR 1.78(e) is filed more than two years after the date the priority or benefit claim was due, the United States Patent and Trademark Office requires an additional explanation of the circumstances surrounding the delay that establishes the entire delay was unintentional. This requirement is in addition to the requirement to provide a statement that the entire delay was unintentional. See *Clarification of the Practice for Requiring Additional Information in Petitions Filed in Patent Applications and Patents Based on Unintentional Delay*, 85 FR 12222 (March 2, 2020). See MPEP 711.03(c)(II)(C)-(F) for additional guidance on the information required to establish that the entire delay was unintentional.

☐ Because this petition under 37 CFR 1.78(c) and/or 37 CFR 1.78(e) is being filed more than two years after the date the priority or benefit claim was due, additional explanation of the circumstances surrounding the delay that establishes the entire delay was unintentional is enclosed herewith.

PTO/SB/445 (09-22)
Approved for use through 05/31/2024. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PETITION TO ACCEPT AN UNINTENTIONALLY DELAYED CLAIM UNDER 35 U.S.C. 119(e) (37 CFR 1.78(c)) AND/OR TO ACCEPT AN UNINTENTIONALLY DELAYED CLAIM UNDER 35 U.S.C. 120, 121, 365(c), or 386(c) (37 CFR 1.78(e)) FOR THE BENEFIT OF A PRIOR-FILED APPLICATION

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

/Ivan S. Kavrukov/
Signature*

January 5, 2022
Date

Ivan S. Kavrukov
Typed or Printed Name

25,161
Registration Number, if applicable

Wissing Miller LLP
Address

(917) 945-0121
Telephone Number

31 Hudson Yards, 11th Floor , New York, New York 10001
Address

* This petition must be signed in accordance with 37 CFR 1.33. Please see 37 CFR 1.4(d) for the signature requirements. Submit multiple forms if more than one signature is required.

Enclosures:

- [x] Application Data Sheet (see instructions starting on page 4)
- [ ] Fee (along with supporting documentation, if required)
- [ ] Other: _____

CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)]

I hereby certify that this correspondence is being:

- [ ] Deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Petition, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.
- [x] Transmitted by electronic filing (EFS-Web or Patent Center) or by facsimile on the date shown below to the United States Patent and Trademark Office at 571-273-8300.

January 5, 2023
Date

/Mary Ellen Finnegan/
Signature

Mary Ellen Finnegan
Typed or printed name of person signing certificate

Instructions for Petition to Accept an Unintentionally Delayed Claim under 35 U.S.C. 119(e) (37 CFR 1.78(c)) and/or to Accept an Unintentionally Delayed Claim under 35 U.S.C. 120, 121, 365(c), or 386(c) (37 CFR 1.78(e)) for the Benefit of a Prior-Filed Application

(Not to be Submitted to the USPTO)

When filing electronically via EFS-Web or Patent Center, use Doc Code PET.PCT (Petition for review by the PCT Legal Office) for applications filed under 35 U.S.C. 371 and/or if the reference to the prior-filed application(s) includes an international application or an international design application. In all other instances, use Doc Code PET.OP (Petition for review by the Office of Petitions).

1. The reference required to the prior-filed application:

a. For applications filed on or after September 16, 2012, the reference must be set forth in a corrected application data sheet (ADS). See 37 CFR 1.76.

Note: Any ADS filed after the filing of the application is considered a corrected (or updated) ADS even if an ADS was not previously submitted. A corrected ADS must identify the information that is being changed with underlining for insertions and strike-through or brackets for text removed. In general, the identification of the information being changed should be made relative to the most recent filing receipt. For example, where the most recent filing receipt for the application shows no benefit claim, the entire benefit claim must be shown with underlining in the corrected ADS. In addition, if the ADS identified an incorrect provisional application number and the most recent filing receipt included the incorrect provisional application number, the corrected ADS should identify the incorrect provisional application number being deleted with strike-through or brackets, and should identify the correct provisional application number being added with underlining. For more information regarding a corrected ADS in an application filed on or after September 16, 2012, see MPEP 601.05(a), subsection II.

A corrected ADS may include all of the section headings listed in 37 CFR 1.76(b) with all appropriate data for each heading or only those sections (including the section headings) containing changed or updated information. See 37 CFR 1.76(c)(2). A corrected ADS must identify the application by application number and be properly signed.

Use of the corrected Web-based ADS is recommended for registered users of EFS-Web or Patent Center because it will pre-populate with information of record; applicants can then type in the desired changes, and the system will create a PDF version with the appropriate strike-through and underlining. For more information, see the "Quick Start Guide for Corrected Web-based Application Data Sheet (Corrected Web ADS)" available at https://www.uspto.gov/patents-application-process/applying-online/efsweb-guidance-and-resources.

Applicants may also use Form PTO/AIA/14, which may be printed and marked up to comply with 37 CFR 1.76(c).

Instructions for Petition to Accept an Unintentionally Delayed Claim under 35 U.S.C. 119(e) (37 CFR 1.78(c)) and/or to Accept an Unintentionally Delayed Claim under 35 U.S.C. 120, 121, 365(c), or 386(c) (37 CFR 1.78(e)) for the Benefit of a Prior-Filed Application

(Not to be Submitted to the USPTO)

b. For applications filed before September 16, 2012, the reference to the prior-filed application may be made in a supplemental ADS in compliance with pre-AIA 37 CFR 1.76(c) or in an amendment in the first sentence(s) of the specification following the title. See 37 CFR 1.78(h).

Note: For applications filed before September 16, 2012, any ADS submitted after the filing date of the application is a supplemental ADS, regardless of whether an original ADS was submitted with the application papers on filing. Supplemental ADS papers must be labeled Supplemental ADS or Supplemental Application Data Sheet, include each of the seven section headings listed in pre-AIA 37 CFR 1.76(b) with all appropriate data for the section heading, and identify the information that is being changed. See pre-AIA 37 CFR 1.76(c). A supplemental ADS must also identify the application by application number and be properly signed. For more information regarding a supplemental ADS in an application filed before September 16, 2012, see MPEP 601.05(b), subsection II.

2. Petition fee:

The petition fee is set forth in 37 CFR 1.17(m) and must be included with the petition. Petitioner is advised to refer to the current fee schedule at https://www.uspto.gov/learning-and-resources/fees-and-payment/uspto-fee-schedule.

3. Statement:

37 CFR 1.78(c) and 37 CFR 1.78(e) require a statement that the entire delay between the date the benefit claim was due and the date the benefit claim was filed was unintentional. The required statement(s) is included in this form.

Note: the Director may require additional information where there is a question whether the delay was unintentional.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	17707429
Filing Date:	29-Mar-2022
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Attorney Docket Number:	309-0011USDIVCIP2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
PETITION FEE - 37 CFR 1.17(F)(GROUP I)	2462	1	168	168
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**168**

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shih-Yuan		WANG	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Palo Alto	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	766 Encina Grande Dr.		
Address 2			
City	Palo Alto	State/Province	CA
Postal Code	94306	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shih-Ping		WANG	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Los Altos	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	38 3rd Street, Suite #307		
Address 2			
City	Los Altos	State/Province	CA
Postal Code	94022	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

☐ An Address is being provided for the correspondence Information of this application.			
Customer Number	23432		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES		
Attorney Docket Number	309-0011USDIVCIP2	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	47	**Suggested Figure for Publication (if any)**	5B

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	23432		

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Division of	17532831	2021-11-22
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
17532831	Continuation in part of	17182954	2021-02-23
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17182954	Division of	16528958	2019-08-01	11121271	2021-09-04
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	15797821	2017-10-30	10446700	2019-10-15
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15797821	~~Continuation of~~ Continuation in part	14947718	2015-11-20	10622498	2020-04-14
Prior Application Status	Pending				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
14947718	Continuation of	PCT/US14/39208	2014-05-22		
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
PCT/US14/39208	Claims benefit of provisional	61826446	2013-05-22		
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
PCT/US14/39208	Claims benefit of provisional	61834873	2013-06-13		
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
PCT/US14/39208	Claims benefit of provisional	61843021	2013-07-04		
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
PCT/US14/39208	Claims benefit of provisional	61905109	2013-11-15		

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	W&WSENS DEVICES, INC.

Mailing Address Information For Applicant:

Address 1	38 THIRD STREET		
Address 2	SUITE 307		
City	LOS ALTOS	**State/Province**	CA
Country	US	Postal Code	94022
Phone Number		Fax Number	

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Email Address	

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/Ivan S. Kavrukov/			Date (YYYY-MM-DD)	~~2022-03-29~~ 2023-01-0
First Name	Ivan	Last Name	Kavrukov	Registration Number	25161

Additional Signature may be generated within this form by selecting the Add button.

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent C o o p eration Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Shih-Yuan WANG
Serial No.:	17/707,429
Filing Date:	March 29, 2022
Art Unit:	2818
Confirmation No.:	1214
Examiner:	HOANG QUAN TRAN HO
For:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, New York 10001

CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: January 5, 2023

I hereby certify that this correspondence is being transmitted via Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

PETITION TO EXPEDITE

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits a Petition, Statement Accompanying the Petition, and a Corrected Application Data Sheet. Applicant asks that the Petition be expedited since the Issue Fee for this application is due February 2, 2022.

The Office is hereby authorized to charge any other fees that may be required in connection herewith and to credit any overpayment to our Deposit Account No. 600125.

Respectfully Submitted,

WISSING MILLER LLP

Attorney for Applicants

By: /Ivan S. Kavrukov/

Ivan S. Kavrukov
Reg. No. 25,161
Tel: (917) 945-0121

Electronic Acknowledgement Receipt

EFS ID:	47324511
Application Number:	17707429
International Application Number:	
Confirmation Number:	1214
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	139982
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	309-0011USDIVCIP2
Receipt Date:	05-JAN-2023
Filing Date:	29-MAR-2022
Time Stamp:	15:45:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$168
RAM confirmation Number	E202315F46002786
Deposit Account	600125
Authorized User	Mary Ellen Finnegan

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Petition for review by the Office of Petitions	309-0011USDIVCIP2_Petition.pdf	285054 f53184dc09eea41d6c965255aafe06797f0c6eb6	no	6
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	309-0011USDIV2-Statement_Accompanying_Petition-signed.pdf	460275 72edecfaef681c0f012ee99551b9ec232053bcc9	no	2
Warnings:					
Information:					
3	Miscellaneous Incoming Letter	309-0011USDIV2-PetitionToExpedite-signed.pdf	458936 cb667ad3aaff86cc2595165ca0ad302bd39fe97b	no	2
Warnings:					
Information:					
4	Application Data Sheet	309-0011USDIVCIP2_CorrectedADS_signed_01-05-2023.pdf	2601743 815080b3f42c499ef1979fef8ab5748809767df2	no	8
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
5	Fee Worksheet (SB06)	fee-info.pdf	38399 279ac684c3f86a24d9ea3ea9b807db1c6c605293	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3844407		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Receipt date: 10/24/2022

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17707429
Filing Date	2022-03-29
First Named Inventor	Shih-Yuan WANG
Art Unit	2818
Examiner Name	Tran Quan Hoang Ho
Attorney Docket Number	309-0011USDIVCIP2

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	11309444		2022-04-19	Wang et al.	

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20100320444		2010-12-23	Dutta	
	2	20110309331		2011-12-22	Yu et al.	
	3	20180182806		2018-06-28	Jin et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	20080101301	KR		2008-11-21	Dongbu Hitek Co. Ltd.		☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

Receipt date: 10/24/2022

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(**Not for submission under 37 CFR 1.99)**

Application Number	17707429
Filing Date	2022-03-29
First Named Inventor	Shih-Yuan WANG
Art Unit	2818
Examiner Name	Tran Quan Hoang Ho
Attorney Docket Number	309-0011USDIVCIP2

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/Hoang-Quan Ho/	Date Considered	11/15/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/707,429	03/29/2022	Shih-Yuan WANG	309-0011USDIVCIP2	1214

139982 7590 11/18/2022

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER
HO, HOANG QUAN TRAN

ART UNIT	PAPER NUMBER
2818	

NOTIFICATION DATE	DELIVERY MODE
11/18/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

Supplemental ***Notice of Allowability***	**Application No.** 17/707,429	**Applicant(s)** WANG et al.	
	Examiner Hoang-Quan Ho	**Art Unit** 2818	**AIA (FITF) Status** Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to IDS filed on 10/24/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☐ The allowed claim(s) is/are _____ . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10/24/2022.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☑ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☑ Other Detailed Action.

/Hoang-Quan Ho/
Primary Examiner, Art Unit 2818

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on October 24, 2022 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in an interview with Ivan Kavrukov on November 15, 2022.

The application has been amended as follows:

Claim 31: At line 10, replace "material);" with --material;--.

Claim 35: At line 1, replace "in which in which" with --in which-- and at line 2, replace "the range" with --a range--.

Claim 44: At line 1, replace "in which in which" with --in which-- and at line 2, replace "the range" with --a range--.

Claim 49: At lines 2 and 3, replace "the 100-2,000 nm range" with --a range of 100-2,000 nm--.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Quan Ho whose telephone number is (571)272-8711. The examiner can normally be reached Monday - Friday, 10 AM - 6 PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hoang-Quan Ho
Primary Patent Examiner
Art Unit 2818

/Hoang-Quan Ho/
Primary Examiner, Art Unit 2818

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/707,429	WANG et al.
	Examiner	**Art Unit**
	Hoang-Quan Ho	2818

CPC						
Symbol					**Type**	**Version**
H01L	/	31	/	035272	F	2013-01-01
H01L	/	31	/	035281	I	2013-01-01
H01L	/	31	/	075	I	2013-01-01
H01L	/	31	/	105	I	2013-01-01
G02B	/	6	/	136	I	2013-01-01
H01L	/	31	/	0284	I	2013-01-01
H01L	/	31	/	035227	I	2013-01-01
H01L	/	31	/	022475	I	2013-01-01
H01L	/	31	/	035209	I	2013-01-01
H01L	/	31	/	0312	I	2013-01-01
H01L	/	31	/	036	I	2013-01-01
H01L	/	31	/	077	I	2013-01-01
H01L	/	31	/	1808	I	2013-01-01
H01L	/	31	/	1812	I	2013-01-01
H01L	/	31	/	1075	I	2013-01-01
H01L	/	31	/	028	I	2013-01-01
H01L	/	31	/	1055	I	2013-01-01
H01L	/	31	/	107	I	2013-01-01
H01L	/	31	/	054	I	2014-12-01
G02B	/	6	/	122	I	2013-01-01
H01L	/	23	/	66	I	2013-01-01
H01L	/	31	/	02005	I	2013-01-01
H01L	/	31	/	02019	I	2013-01-01
H01L	/	31	/	022408	I	2013-01-01
H01L	/	31	/	02327	I	2013-01-01
H01L	/	31	/	02363	I	2013-01-01
H01L	/	31	/	024	I	2013-01-01
H01L	/	31	/	0304	I	2013-01-01
H01L	/	31	/	03046	I	2013-01-01
H01L	/	31	/	0745	I	2013-01-01
H01L	/	31	/	1804	I	2013-01-01

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/Hoang-Quan Ho/ Primary Examiner, Art Unit 2818	22 October 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5B

U.S. Patent and Trademark Office — Part of Paper No.: 20221022

Samsung Exhibit 1003, Page 42 of 516

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/707,429	WANG et al.
	Examiner	**Art Unit**
	Hoang-Quan Ho	2818

CPC						
Symbol					**Type**	**Version**
H01L	/	31	/	184	I	2013-01-01
H01L	/	31	/	1844	I	2013-01-01
H01L	/	31	/	02016	I	2013-01-01
G02B	/	2006	/	12176	A	2013-01-01
Y02E	/	10	/	52	A	2013-01-01
Y02E	/	10	/	548	A	2013-01-01
G02B	/	2006	/	12097	A	2013-01-01
H01L	/	2223	/	6627	A	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/Hoang-Quan Ho/ Primary Examiner, Art Unit 2818	22 October 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5B

U.S. Patent and Trademark Office — Part of Paper No.: 20221022

Samsung Exhibit 1003, Page 43 of 516

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/707,429	WANG et al.
	Examiner	**Art Unit**
	Hoang-Quan Ho	2818

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H01L31/0352	/	31	/	0352
H01L31/075	/	31	/	075
H01L31/105	/	31	/	105
H01L31/028	/	31	/	028
H01L31/0224	/	31	/	0224
H01L31/107	/	31	/	107
H01L31/02	/	31	/	02
H01L31/0236	/	31	/	0236

NON-CLAIMED				
G02B6/136	/	6	/	136
H01L31/0312	/	31	/	0312
H01L31/036	/	31	/	036
H01L31/077	/	31	/	077
H01L31/18	/	31	/	18
H01L31/054	/	31	/	054
G02B6/122	/	6	/	122
H01L23/66	/	23	/	66
H01L31/0232	/	31	/	0232
H01L31/024	/	31	/	024
H01L31/0304	/	31	/	0304
H01L31/0745	/	31	/	0745

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/Hoang-Quan Ho/ Primary Examiner, Art Unit 2818	22 October 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5B

U.S. Patent and Trademark Office — Part of Paper No.: 20221022

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/707,429	WANG et al.
	Examiner	**Art Unit**
	Hoang-Quan Ho	2818

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10		19		28	7	37	16	46				
	2		11		20		29	8	38	17	47				
	3		12		21		30	9	39	18	48				
	4		13		22	1	31	10	40	19	49				
	5		14		23	2	32	11	41	20	50				
	6		15		24	3	33	12	42						
	7		16		25	4	34	13	43						
	8		17		26	5	35	14	44						
	9		18		27	6	36	15	45						

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/Hoang-Quan Ho/ Primary Examiner, Art Unit 2818 (Primary Examiner)	22 October 2022 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 5B

U.S. Patent and Trademark Office Part of Paper No.: 20221022

Samsung Exhibit 1003, Page 45 of 516

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	2	"17707429"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/15 03:24 PM
L2	6	("20110156195"|"20120012741"|"20120153127"|"20180012918"|"20180102442"|"20190166317").PN.	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/15 03:25 PM
L3	28	(W&WSENS DEVICES).as,aanm.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	WITH	ON	ON	2022/06/15 03:26 PM
L4	1385	(Shih-Yuan WANG).in.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT;	WITH	ON	ON	2022/06/15 03:26 PM

Samsung Exhibit 1003, Page 46 of 516

			IBM_TDB)				
L5	457	(Shih-Ping WANG).in.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	WITH	ON	ON	2022/06/15 03:26 PM
L7	285723	(H01L31/035272 OR G02B6/122 OR G02B6/136 OR H01L23/66 OR H01L31/02005 OR H01L31/02016 OR H01L31/02019 OR H01L31/022408 OR H01L31/022475 OR H01L31/02327 OR H01L31/02363 OR H01L31/024 OR H01L31/028 OR H01L31/0284 OR H01L31/0304 OR H01L31/03046 OR H01L31/0312 OR H01L31/035209 OR H01L31/035227 OR H01L31/035281 OR H01L31/036 OR H01L31/054 OR H01L31/0745 OR H01L31/075 OR H01L31/077 OR H01L31/105 OR H01L31/1055 OR H01L31/107 OR H01L31/1075 OR H01L31/1804 OR H01L31/1808 OR H01L31/1812 OR H01L31/184 OR H01L31/1844 OR G02B2006/12097 OR G02B2006/12176 OR H01L2223/6627 OR Y02E10/52 OR Y02E10/548).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/15 03:32 PM
L8	51993616	pillar column mesa post	(US-PGPUB; USPAT;	OR	ON	ON	2022/06/15

		rod	USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				06:42 PM
L9	1	"11309444".pn.	(USPAT)	AND	ON	ON	2022/06/15 06:44 PM
L10	30838630	dielectric insulat$3 oxide	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/15 08:20 PM
L11	48494892	spac$3 pitch	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/15 08:22 PM
L12	14061155	pin! (p ADJ i ADJ n)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS,	OR	ON	ON	2022/06/15 08:23 PM

			IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L13	15	(3 OR 4 OR 5) 7 (8 near5 10) (8 near5 11)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/15 08:24 PM
L14	655	7 (8 near5 10) (8 near5 11)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/15 08:45 PM
L15	52161205	pillar column mesa post rod nanowire nanorod	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/15 08:53 PM

L16	28	(3 OR 4 OR 5) 7 (15 near5 10) (15 near5 11)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/15 08:54 PM
L17	1064	7 (15 near5 10) (15 near5 11)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/15 08:56 PM
L18	20	("2011/0309331").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2022/06/15 10:46 PM
L19	10899934	infrared ir!	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/15 10:54 PM
L20	385	7 (15 near5 10) (15 near5 11) 19	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	AND	ON	ON	2022/06/15 11:01 PM

			EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L21	12	("7525170" | "9000492" | "10411053" | "10522582" | "20050145779" | "20120153416" | "20150349206" | "20160240579" | "20170141153" | "20180102442" | "20200006407" | "20200006416").pn. OR ("11309444").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2022/06/16 08:12 PM
L22	31	(Artificial Intelligence) More like doc: US-11309444-B1 Text: (JP-2020537816-A OR US-20180102442-A1 OR US-9496435-B2 OR US-20220102563-A1 OR CN-105556680-B OR US-20160126381-A1 OR US-10622498-B2 OR US-20190288132-A1 OR US-20210242354-A1 OR WO-2014190189-A9 OR WO-2014190189-A2 OR EP-3000134-A2 OR US-20160254407-A1 OR JP-2016526295-A OR EP-3000134-B1 OR US-9818893-B2 OR US-20170194522-A1 OR JP-6602751-B2 OR KR-102358584-B1 OR US-20210313483-A1).did.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/16 08:13 PM
L24	10	("11309444" "11121271" "10446700" "10622498" "10468543" "9496435" "9530905" "10700225" "9525084"	(USPAT)	OR	ON	ON	2022/06/17 04:37 PM

Samsung Exhibit 1003, Page 51 of 516

		"9818893").pn.					
L25	2	17/532831	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/17 04:39 PM
L26	2	17/182954	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/17 04:40 PM
L27	4	L1	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/10/14 04:47 PM
L28	33	(Artificial Intelligence) More like doc: US-20220246775-A1 Text: (US-20220102563-A1 OR EP-3000134-A2 OR US-20160254407-A1 OR KR-20160039150-A OR WO-2014190189-A2 OR KR-20220019844-A OR WO-2014190189-A9 OR EP-3000134-B1 OR US-20160126381-A1 OR US-10622498-B2 OR US-11309444-B1 OR US-20170194522-A1 OR JP-2016526295-A OR US-9818893-B2 OR US-9496435-B2 OR JP-6602751-B2 OR KR-102358584-B1 OR US-20190288132-A1 OR CN-105556680-A OR US-20150001410-A1).did.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/10/14 04:47 PM
L29	0	("2022/0246775").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2022/10/14 05:01 PM
L30	2	("8835905").pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	AND	ON	ON	2022/10/14 08:05 PM

			EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L31	2	("20110309331").pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/10/14 08:07 PM
L32	16	L13	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/10/14 10:09 PM
L33	671	L14	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO;	AND	ON	ON	2022/10/14 10:10 PM

Samsung Exhibit 1003, Page 53 of 516

			JPO; DERWENT; IBM_TDB)				
L34	29	L16	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/10/14 10:21 PM
L35	1087	L17	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/10/14 10:22 PM
L36	392	L20	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/10/14 10:22 PM
L37	20	"2009088071"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB,	AND	ON	ON	2022/10/22 04:02 PM

Samsung Exhibit 1003, Page 54 of 516

			HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L38	12	"2011083693"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/10/22 04:03 PM
L39	1	("20080218740").pn.	(US-PGPUB)	AND	ON	ON	2022/10/22 04:07 PM
L40	1	("7977637").pn.	(USPAT)	AND	ON	ON	2022/10/22 04:15 PM
L41	1	("20120141122").pn.	(US-PGPUB)	AND	ON	ON	2022/10/22 04:16 PM
L42	50	"2014190189"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/10/22 04:33 PM
L43	1	("7251386").pn.	(USPAT)	AND	ON	ON	2022/10/22 05:04 PM
L44	9	"2002314116"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	AND	ON	ON	2022/10/22 06:11 PM

			EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	47695	(H01L31/035272 OR G02B6/122 OR G02B6/136 OR H01L23/66 OR H01L31/02005 OR H01L31/02016 OR H01L31/02019 OR H01L31/022408 OR H01L31/022475 OR H01L31/02327 OR H01L31/02363 OR H01L31/024 OR H01L31/028 OR H01L31/0284 OR H01L31/0304 OR H01L31/03046 OR H01L31/0312 OR H01L31/035209 OR H01L31/035227 OR H01L31/035281 OR H01L31/036 OR H01L31/054 OR H01L31/0745 OR H01L31/075 OR H01L31/077 OR H01L31/105 OR H01L31/1055 OR H01L31/107 OR H01L31/1075 OR H01L31/1804 OR H01L31/1808 OR H01L31/1812 OR H01L31/184 OR H01L31/1844 OR G02B2006/12097 OR G02B2006/12176 OR H01L2223/6627 OR Y02E10/52 OR Y02E10/548).cpc.	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/16 07:56 PM
N2	1014266	(pillar column mesa post rod nanowire	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/16 07:56 PM

		nanorod).clm.					
N3	1506210	(dielectric insulat$3 oxide).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/16 07:58 PM
N4	2514245	(spac$3 pitch).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/16 08:10 PM
N5	196222	(infrared ir!).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/16 08:10 PM
N6	5	N1 (N2 near5 N3) (N2 near5 N4) N5	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/16 08:11 PM
N7	5	N6	(US-PGPUB; USPAT)	AND	ON	ON	2022/10/21 05:41 PM

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/707,429	WANG et al.
	Examiner	Art Unit
	Hoang-Quan Ho	2818

CPC - Searched*		
Symbol	Date	Examiner
H01L31/035272 or G02B6/122 or G02B6/136 or H01L23/66 or H01L31/02005 or H01L31/02016 or H01L31/02019 or H01L31/022408 or H01L31/022475 or H01L31/02327 or H01L31/02363 or H01L31/024 or H01L31/028 or H01L31/0284 or H01L31/0304 or H01L31/03046 or H01L31/0312 or H01L31/035209 or H01L31/035227 or H01L31/035281 or H01L31/036 or H01L31/054 or H01L31/0745 or H01L31/075 or H01L31/077 or H01L31/105 or H01L31/1055 or H01L31/107 or H01L31/1075 or H01L31/1804 or H01L31/1808 or H01L31/1812 or H01L31/184 or H01L31/1844 or G02B2006/12097 or G02B2006/12176 or H01L2223/6627 or Y02E10/52 or Y02E10/548	06/15/2022	HQH
H01L31/035272 or G02B6/122 or G02B6/136 or H01L23/66 or H01L31/02005 or H01L31/02016 or H01L31/02019 or H01L31/022408 or H01L31/022475 or H01L31/02327 or H01L31/02363 or H01L31/024 or H01L31/028 or H01L31/0284 or H01L31/0304 or H01L31/03046 or H01L31/0312 or H01L31/035209 or H01L31/035227 or H01L31/035281 or H01L31/036 or H01L31/054 or H01L31/0745 or H01L31/075 or H01L31/077 or H01L31/105 or H01L31/1055 or H01L31/107 or H01L31/1075 or H01L31/1804 or H01L31/1808 or H01L31/1812 or H01L31/184 or H01L31/1844 or G02B2006/12097 or G02B2006/12176 or H01L2223/6627 or Y02E10/52 or Y02E10/548	10/14/2022	HQH

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/707,429	WANG et al.
	Examiner	Art Unit
	Hoang-Quan Ho	2818

Search Notes		
Search Notes	**Date**	**Examiner**
See Search history.	06/17/2022	HQH
See Google Scholar search history.	06/16/2022	HQH
See Search history.	10/22/2022	HQH
See Global Dossier search.	10/22/2022	HQH

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
H01L	31/035272,02005,02016,02019,022408,022475,02327,02363,024,028,0284,0304,03046,0312,035209,035227,035281,036,054,0745,075,077,105,1055,107,1075,1804,1808,1812,184,1844	06/16/2022	HQH
G02B	6/122,136	06/16/2022	HQH
H01L	23/66	06/16/2022	HQH
H01L	2223/6627	06/16/2022	HQH
G02B	2006/12097,12176	06/16/2022	HQH
Y02E	10/52,548	06/16/2022	HQH
H01L	31/035272,02005,02016,02019,022408,022475,02327,02363,024,028,0284,0304,03046,0312,035209,035227,035281,036,054,0745,075,077,105,1055,107,1075,1804,1808,1812,184,1844	10/22/2022	HQH
G02B	6/122,136	10/22/2022	HQH
H01L	23/66	10/22/2022	HQH
H01L	2223/6627	10/22/2022	HQH
G02B	2006/12097,12176	10/22/2022	HQH
H01L	10/52,548	10/22/2022	HQH

Bibliographic Data

Application No: 17/707,429

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /Hoang-Quan Ho/ Examiner's Signature | Initials

Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
03/29/2022	257	2818	309-0011USDIVCIP2
RULE			

APPLICANTS

W&WSENS DEVICES, INC., Los Altos, CA,

INVENTORS

Shih-Yuan WANG, Palo Alto, CA, UNITED STATES

Shih-Ping WANG, Los Altos, CA, UNITED STATES

CONTINUING DATA

This application is a DIV of 17532831 11/22/2021 PAT 11309444

17532831 is a CIP of 17182954 02/23/2021

17182954 is a DIV of 16528958 08/01/2019 PAT 11121271

16528958 is a CIP of 15797821 10/30/2017 PAT 10446700

15797821 is a CON of 14947718 11/20/2015 PAT 10622498

14947718 is a CON of PCT/US14/39208 05/22/2014

PCT/US14/39208 has PRO of 61905109 11/15/2013

PCT/US14/39208 has PRO of 61843021 07/04/2013

PCT/US14/39208 has PRO of 61834873 06/13/2013

PCT/US14/39208 has PRO of 61826446 05/22/2013

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

04/06/2022

** SMALL ENTITY **

STATE OR COUNTRY

UNITED STATES

ADDRESS

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001
UNITED STATES

FILING FEE RECEIVED

$1,330

Global Dossier

Office

US

Type

Application

17707429

★ 0 1

US 17707429 107 Members in Patent Family (104 currently shown)

« ()

IP Office Type

- All IP5 Offices
  - EPO
  - SIPO
  - KIPO
  - JPO
  - USPTO
- Non-IP5 Offices

	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
()	US	13384621	1) Han, Kyung Soo	SYSTEM AND METHOD FOR PROVIDING A CONSTANT OUTPUT FROM A VARIABLE FLOW INPUT	07/20/2010	US 13384621 US PCT/US10/42519 US 12226943	US 20120115662 A1 () US 8388481 B2 ()	05/10/2012 03/05/2013

Most Recent Documents

Date	Document Description ()	Options
02/13/2013	Issue Notification ()	•••
01/31/2013	Issue Fee Payment (PTO-85B) ()	•••
01/31/2013	Fee Worksheet (SB06) ()	•••

Office Actions

Date	Document Description ()
12/18/2012	Notice of Allowance and Fees Due (PTOL-85) ()
11/02/2012	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
()	US	PCT/US10/42519	1) HAN, Kyung-Soo,	A SYSTEM AND METHOD FOR PROVIDING A CONSTANT OUTPUT FROM A VARIABLE FLOW INPUT	07/20/2010	US 12226943	WO 2011011358 A2 () WO 2011011358 A3 ()	01/27/2011 04/28/2011

Most Recent Documents

Date	Document Description ()	Options
01/24/2012	Notification of Transmittal of Copies of International Preliminary Report on Patentability Chapter I ()	•••
01/24/2012	International Preliminary Report on Patentability Chapter I ()	•••
01/20/2012	Written Opinion of the International Search Authority ()	•••

Office Actions

Date	Document Description ()
01/24/2012	International Preliminary Report on Patentability Chapte
01/20/2012	Written Opinion of the International Search Authority ()
03/10/2011	International Search Report ()

All Documents | Classification and Citation | View All Office Actions

	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
()	US	13425501	1) Han, Kyung Soo	INFINITELY VARIABLE MOTION CONTROL (IVMC) FOR GENERATORS, TRANSMISSIONS AND PUMPS/COMPRESSORS	03/21/2012	US 13425501 US 61466056 US PCT/US10/42519 US 13384621	US 20120243991 A1 () US 8641570 B2 ()	09/27/2012 02/04/2014

Most Recent Documents

Date	Document Description ()	Options
01/15/2014	Issue Notification ()	•••
01/02/2014	Filing Receipt ()	•••
01/01/2014	Issue Fee Payment (PTO-85B) ()	•••

Office Actions

Date	Document Description ()
10/04/2013	Notice of Allowance and Fees Due (PTOL-85) ()
08/30/2013	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	13568288	1) Han, Kyung Soo	INFINITELY VARIABLE MOTION CONTROL (IVMC) FOR RIVER TURBINES	08/07/2012	US 61523846 US 13425501 US PCT/US10/42519 US 13384621 US 13568288 US 61521408	US 20120299301 A1 () US 8485933 B2 ()	11/29/2012 07/16/2013

Most Recent Documents

Date	Document Description ()	Options
08/30/2021	ePetition Request Form ()	•••
08/30/2021	Fee Worksheet (SB06) ()	•••
08/30/2021	ePetition Grant Letter ()	•••

Office Actions

Date	Document Description ()
04/19/2013	Notice of Allowance and Fees Due (PTOL-85) ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	13915785	1) Han, Kyung Soo	INFINITELY VARIABLE MOTION CONTROL (IVMC) FOR A TRANSMISSION WITH A DIFFERENTIAL	06/12/2013	US 61523846 US 13425501 US PCT/US10/42519 US 13568288 US 61521408 US 13915785	US 20130274056 A1 () US 8702552 B2 ()	10/17/2013 04/22/2014

Most Recent Documents

Date	Document Description ()	Options
04/02/2014	Issue Notification ()	•••
03/18/2014	Miscellaneous Incoming Letter ()	•••
03/18/2014	Electronic Filing System(EFS) Acknowledgment Receipt ()	•••

Office Actions

Date	Document Description ()
01/23/2014	Notice of Allowance and Fees Due (PTOL-85) ()
11/19/2013	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	14096171	1) Han, Kyung Soo	INFINITELY VARIABLE MOTION CONTROL (IVMC) FOR GENERATORS, TRANSMISSIONS AND PUMPS/COMPRESSORS	12/04/2013	US 13425501 US 61466056 US PCT/US10/42519 US 13384621 US 12226943 US 14096171	US 20140094338 A1 () US 9017208 B2 ()	04/03/2014 04/28/2015

Most Recent Documents

Date	Document Description ()	Options
04/08/2015	Issue Notification ()	•••
03/31/2015	Issue Fee Payment (PTO-85B) ()	•••
03/31/2015	Fee Worksheet (SB06) ()	•••

Office Actions

Date	Document Description ()
01/22/2015	Notice of Allowance and Fees Due (PTOL-85) ()
10/08/2014	Final Rejection ()
08/18/2014	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	14155401	1) Han, Kyung Soo	INFINITELY VARIABLE DIRECTION CONTROL	01/15/2014	US 61523846 US 13425501 US PCT/US10/42519 US 13384621 US 13915785 US 14155401 US 13568288 US 61521408	US 20140141927 A1 () US 8986149 B2 ()	05/22/2014 03/24/2015

Most Recent Documents

Date	Document Description ()	Options
03/04/2015	Issue Notification ()	•••
02/03/2015	Issue Fee Payment (PTO-85B) ()	•••
02/03/2015	Fee Worksheet (SB06) ()	•••

Office Actions

Date	Document Description ()
01/30/2015	Notice of Allowance and Fees Due (PTOL-85) ()
11/19/2014	Final Rejection ()
08/04/2014	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	14155404	1) Han, Kyung Soo	INFINITELY VARIABLE PUMPS AND COMPRESSORS	01/15/2014	US 61523846 US 13425501 US PCT/US10/42519 US 13384621 US 13915785 US 13568288 US 14155404 US 61521408	US 20140137676 A1 () US 8992370 B2 ()	05/22/2014 03/31/2015

Most Recent Documents

Date	Document Description ()	Options
03/11/2015	Issue Notification ()	•••
02/19/2015	Issue Fee Payment (PTO-85B) ()	•••
02/19/2015	Fee Worksheet (SB06) ()	•••

Office Actions

Date	Document Description ()
02/02/2015	Notice of Allowance and Fees Due (PTOL-85) ()
11/03/2014	Final Rejection ()
07/23/2014	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	14225658	1) Han, Kyung Soo	ONE-STROKE INTERNAL COMBUSTION ENGINE	03/26/2014	US 61805584 US 14225658 US 61825560	US 20140290616 A1 () US 9169772 B2 ()	10/02/2014 10/27/2015

Most Recent Documents

Date	Document Description ()	Options
08/28/2021	ePetition Request Form ()	•••
08/28/2021	Fee Worksheet (SB06) ()	•••
08/28/2021	ePetition Grant Letter ()	•••

Office Actions

Date	Document Description ()
06/19/2015	Notice of Allowance and Fees Due (PTOL-85) ()
03/13/2015	Final Rejection ()
10/02/2014	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	14255377	1) Han, Kyung Soo	RUN-OF-THE-RIVER OR OCEAN CURRENT TURBINE	04/17/2014	US 13425501 US PCT/US10/42519 US 13384621 US 12226943 US 14255377 US 13915785 US 13568288	US 20140241855 A1 () US 9151269 B2 ()	08/28/2014 10/06/2015

Most Recent Documents

Date	Document Description ()	Options
11/25/2019	ePetition Request Form ()	•••
11/25/2019	Fee Worksheet (SB06) ()	•••
11/25/2019	ePetition Grant Letter ()	•••

Office Actions

Date	Document Description ()
05/22/2015	Notice of Allowance and Fees Due (PTOL-85) ()
03/03/2015	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	PCT/US14/34859	1) HAN, Kyung, Soo, 2) DIFFERENTIAL DYNAMICS CORPORATION,	ONE-STROKE INTERNAL COMBUSTION ENGINE	04/22/2014	US 14225658 US 61825560	WO 2014189640 A1 ()	11/27/2014

Most Recent Documents

Date	Document Description ()	Options
11/24/2015	Notification of Transmittal of Copies of International Preliminary Report on Patentability Chapter I ()	•••
11/24/2015	International Preliminary Report on Patentability Chapter I ()	•••
11/21/2015	Written Opinion of the International Search Authority ()	•••

Office Actions

Date	Document Description ()
11/24/2015	International Preliminary Report on Patentability Chapter
11/21/2015	Written Opinion of the International Search Authority ()
11/27/2014	International Search Report ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
KR	20157035202	1) DIFFERENTIAL DYNAMICS CORPORATION,	ONE-STROKE INTERNAL COMBUSTION ENGINE	04/22/2014	US 14225658 US PCT/US14/34859 US 61825560	KR 20160009043 A ()	01/25/2016

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
CN	201480029108	1) DIFFERENTIAL DYNAMICS CORP, 2) HAN KYUNG SOO,	One-stroke internal combustion engine	04/22/2014	US 14225658 US PCT/US14/34859 US 61825560	CN 105247189 A ()	01/13/2016
JP	2016515334	1) An alder, ***, *, 2) Differential Dynamics Corporation, 3) YOSHIKAWA, Toshio, 4) ICHIKAWA, Kanna,	1 stroke internal combustion engine {ONE-STROKE INTERNAL COMBUSTION ENGINE}.	04/22/2014	US 14225658 US PCT/US14/34859 US 61825560	JP 2016522346 A ()	07/28/2016
EP	14801886	1) HAN, Kyung Soo,	ONE-STROKE INTERNAL COMBUSTION ENGINE	04/22/2014	US 14225658 US PCT/US14/34859 US 61825560	EP 2999866 A1 () EP 2999866 A4 ()	03/30/2016 04/26/2017
KR	20167000606	1) DIFFERENTIAL DYNAMICS CORPORATION,	RUN-OF-THE-RIVER OR OCEAN CURRENT TURBINE	04/25/2014	US 14255377 US PCT/US14/35487 US 14096171 US 13915785	KR 20160017086 A () KR 101874213 B1 ()	02/15/2016 07/03/2018

Most Recent Documents

Date	Document Description ()	Options
12/11/2015	[Patent Application] Paper according to the Article 203 of Patent Act (TRANSLATED) ()	•••
12/11/2015	[Patent Application] Paper according to the Article 203 of Patent Act (ORIGINAL) ()	•••

All Documents | Classification and Citation

Most Recent Documents

Date	Document Description ()	Options
05/02/2017	First Office Action(PCT) (TRANSLATED) ()	•••
05/02/2017	First Office Action(PCT) (ORIGINAL) ()	•••
04/20/2017	First search (ORIGINAL) ()	•••

Office Actions

Date	Document Description ()
05/02/2017	First Office Action(PCT) (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

Most Recent Documents

Date	Document Description ()	Options
01/18/2019	Trial and Appeal Decision (TRANSLATED) ()	•••
01/18/2019	Trial and Appeal Decision (ORIGINAL) ()	•••
12/11/2018	Notice of Concluding of Proceedings (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
08/15/2017	Decision of Refusal (TRANSLATED) ()
11/01/2016	Notice of Reasons for Refusal (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

Most Recent Documents

Date	Document Description ()	Options
04/05/2018	Refund of fees ()	•••
11/28/2017	Application deemed to be withdrawn (no declaration of maintenance of the application/non-reply to the Written Opinion) ()	•••
04/11/2017	Invitation to declare maintenance of the application and to correct deficiencies in the Written Opinion/amend application ()	•••

Office Actions

Date	Document Description ()
03/24/2017	European search opinion ()
12/08/2015	Copy of the international preliminary report on patentab

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	PCT/US14/35487	1) HAN, Kyung, Soo, 2) DIFFERENTIAL DYNAMICS CORPORATION,	RUN-OF-THE-RIVER OR OCEAN CURRENT TURBINE	04/25/2014	US 14255377 US 14096171 US 13915785	WO 2014200622 A1 ()	12/18/2014

Most Recent Documents

Date	Document Description ()	Options
03/29/2018	Written Decision on Registration (TRANSLATED) ()	•••
03/29/2018	Written Decision on Registration (ORIGINAL) ()	•••
10/30/2017	Written Opinion (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
03/29/2018	Written Decision on Registration (TRANSLATED) ()
08/28/2017	Request for the Submission of an Opinion (TRANSLATED
10/29/2016	Request for the Submission of an Opinion (TRANSLATED

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
EP	14810755	1) HAN, Kyung Soo,	RUN-OF-THE-RIVER OR OCEAN CURRENT TURBINE	04/25/2014	US 14255377 US PCT/US14/35487 US 14096171 US 13915785	EP 3008330 A1 () EP 3008330 A4 () EP 3008330 B1 ()	04/20/2016 08/16/2017 02/05/2020

Most Recent Documents

Date	Document Description ()	Options
06/07/2016	Notification Concerning Submission Or Transmittal Of Priority Document ()	•••
12/15/2015	Notification of Transmittal of Copies of International Preliminary Report on Patentability Chapter I ()	•••
12/15/2015	International Preliminary Report on Patentability Chapter I ()	•••

Office Actions

Date	Document Description ()
12/15/2015	International Preliminary Report on Patentability Chapte
12/12/2015	Written Opinion of the International Search Authority ()
12/18/2014	International Search Report ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
CN	201480031843	1) Korean Powered Company,	Radial or ocean turbine	04/25/2014	US 14255377 US PCT/US14/35487 US 14096171 US 13915785	CN 105264220 A () CN 105264220 B ()	01/20/2016 03/23/2018

Most Recent Documents

Date	Document Description ()	Options
12/09/2020	Communication regarding the expiry of opposition period ()	•••
02/17/2020	Transmission of the certificate for a European patent pursuant to Rule 74 EPC ()	•••
01/10/2020	Decision to grant a European patent ()	•••

Office Actions

Date	Document Description ()
12/09/2020	Communication regarding the expiry of opposition peric
01/10/2020	Decision to grant a European patent ()
09/25/2019	Communication about intention to grant a European pat

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
JP	2016519502	1) An alder, ***, *, 2) Differential Dynamics Corporation, 3) YOSHIKAWA, Toshio, 4) ICHIKAWA, Kanna,	The water stream or ocean current turbine {RUN. sub. -- OF. sub. -- THE- RIVER OR OCEAN CURRENT TURBINE }.	04/25/2014	US 14255377 US PCT/US14/35487 US 14096171 US 13915785	JP 2016529431 A () JP 6260805 B2 ()	09/23/2016 01/17/2018

Most Recent Documents

Date	Document Description ()	Options
11/27/2017	Claims (ORIGINAL) ()	•••
11/24/2017	Claims (ORIGINAL) ()	•••
08/11/2017	Claims (ORIGINAL) ()	•••

Office Actions

Date	Document Description ()
03/13/2017	Nth Office Action (TRANSLATED) ()
10/21/2016	First Office Action(PCT) (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

Samsung Exhibit 1003, Page 66 of 516

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
KR	20227003296	1) WANG, Shih-Yuan,	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	05/22/2014	US 61834873 US 61826446 KR 20157033316 US 61843021 US PCT/US14/39208 US 61905109	KR 20220019844 A ()	02/17/2022

Most Recent Documents

Date	Document Description ()	Options
11/07/2017	Decision to Grant a Patent (TRANSLATED) ()	•••
11/07/2017	Decision to Grant a Patent (ORIGINAL) ()	•••
09/19/2017	Written Opinion (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
11/07/2017	Decision to Grant a Patent (TRANSLATED) ()
06/20/2017	Notice of Reasons for Refusal (TRANSLATED) ()
01/10/2017	Notice of Reasons for Refusal (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
JP	2016515097	1) One and See -***, 2) One and See -**, 3) KOBASHI, Masaaki,	The microstructure enhanced absorption photosensitive device	05/22/2014	US 61834873 US 61826446 US 61843021 US PCT/US14/39208 US 61905109	JP 2016526295 A () JP 6602751 B2 ()	09/01/2016 11/06/2019

Most Recent Documents

Date	Document Description ()	Options
07/08/2022	Written Opinion (TRANSLATED) ()	•••
07/08/2022	Written Opinion (ORIGINAL) ()	•••
07/08/2022	Amendment including Specification etc. (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
05/11/2022	Request for the Submission of an Opinion (TRANSLATED

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	PCT/US14/39208	1) WANG, Shih-Yuan, 2) WANG, Shih-Ping,	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	05/22/2014	US 61834873 US 61826446 US 61843021 US 61905109	WO 2014190189 A2 () WO 2014190189 A3 () WO 2014190189 A9 ()	11/27/2014 01/22/2015 01/07/2016

Most Recent Documents

Date	Document Description ()	Options
09/10/2019	Decision to Grant a Patent (TRANSLATED) ()	•••
09/10/2019	Decision to Grant a Patent (ORIGINAL) ()	•••
08/18/2019	Written Amendment (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
09/10/2019	Decision to Grant a Patent (TRANSLATED) ()
07/23/2019	Notice of Reasons for Refusal (TRANSLATED) ()
01/08/2019	Notice of Reasons for Refusal (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
CN	201480035698	1) Chinese aqua,	Microstructure Enhanced Absorption Photosensitive Device	05/22/2014	US 61834873 US 61826446 US 61843021 US PCT/US14/39208 US 61905109	CN 105556680 A () CN 105556680 B ()	05/04/2016 12/22/2017

Most Recent Documents

Date	Document Description ()	Options
01/07/2016	Published International Application ()	•••
12/29/2015	Notification Concerning the Transmittal of Copy of International Application as Published (to the applicant) ()	•••
12/17/2015	Application Body ()	•••

Office Actions

Date	Document Description ()
11/24/2015	International Preliminary Report on Patentability Chapte
11/22/2015	Written Opinion of the International Search Authority ()
12/09/2014	International Search Report ()

All Documents | Classification and Citation | View All Office Actions

Samsung Exhibit 1003, Page 67 of 516

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
EP	14801543	1) Wang, Shih-Yuan,	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	05/22/2014	US 61834873 US 61826446 US 61843021 US PCT/US14/39208 US 61905109	EP 3000134 A2 () EP 3000134 A4 () EP 3000134 B1 ()	03/30/2016 01/04/2017 03/10/2021

Most Recent Documents

Date	Document Description ()	Options
10/17/2017	Claims (ORIGINAL) ()	•••
07/14/2017	Claims (ORIGINAL) ()	•••
05/04/2017	Nth Office Action (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
05/04/2017	Nth Office Action (TRANSLATED) ()
11/28/2016	First Office Action(PCT) (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
KR	20157033316	1) WANG, Shih-Yuan,	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	05/22/2014	US 61834873 US 61826446 US 61843021 US PCT/US14/39208 US 61905109	KR 20160039150 A () KR 102358584 B1 ()	04/08/2016 02/04/2022

Most Recent Documents

Date	Document Description ()	Options
01/14/2022	Communication regarding the expiry of opposition period ()	•••
03/22/2021	Transmission of the certificate for a European patent pursuant to Rule 74 EPC ()	•••
02/11/2021	Decision to grant a European patent ()	•••

Office Actions

Date	Document Description ()
01/14/2022	Communication regarding the expiry of opposition peric
02/11/2021	Decision to grant a European patent ()
11/26/2020	Communication about intention to grant a European pat

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	14892821	1) WANG, Shih-Yuan 2) WANG, Shih-Ping	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	05/22/2014	US 61834873 US 61826446 US 61843021 US 14892821 US PCT/US14/39208 US 61905109	US 20160126381 A1 () US 9496435 B2 ()	05/05/2016 11/15/2016

Most Recent Documents

Date	Document Description ()	Options
01/29/2022	Amendment including Specification etc. (TRANSLATED) ()	•••
01/29/2022	Amendment including Specification etc. (ORIGINAL) ()	•••
01/27/2022	Divisional Application for International Patent (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
10/26/2021	Written Decision on Registration (TRANSLATED) ()
04/29/2021	Request for the Submission of an Opinion (TRANSLATED
10/22/2020	Request for the Submission of an Opinion (TRANSLATED

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	14668315	1) Han, Kyung Soo	THREE VARIABLE AND FOUR VARIABLE TRANSGEAR ASSEMBLIES	03/25/2015	US 13425501 US 61805584 US 61466056 US PCT/US10/42519 US 13384621 US 12226943 US 14668315 US 14096171 US 61825560 US 14225658	US 20150204421 A1 () US 9303733 B2 ()	07/23/2015 04/05/2016

Most Recent Documents

Date	Document Description ()	Options
11/17/2020	Communication - Re: Power of Attorney (PTOL-308) ()	•••
11/17/2020	Communication - Re: Power of Attorney (PTOL-308) ()	•••
11/10/2020	Power of Attorney ()	•••

Office Actions

Date	Document Description ()
09/14/2016	Notice of Allowance and Fees Due (PTOL-85) ()

All Documents | Classification and Citation | View All Office Actions

()	Office ()	Application ()	Applicant	Title ()	App. Date ()	Priority #	Pub. # ()	Pub. Date	A
()	US	PCT/US15/25121	1) HAN, Kyung, Soo, 2) DIFFERENTIAL DYNAMICS CORPORATION,	THREE, FOUR, FIVE AND N VARIABLE TRANSGEAR ASSEMBLIES	04/09/2015	US 14668315 US 14255377 US PCT/US14/35487 US PCT/US14/34859	WO 2015160623 A1 ()	10/22/2015	

Most Recent Documents

Date	Document Description ()	Options
10/18/2016	Notification of Transmittal of Copies of International Preliminary Report on Patentability Chapter I ()	•••
10/18/2016	International Preliminary Report on Patentability Chapter I ()	•••
10/17/2016	Written Opinion of the International Search Authority ()	•••

Office Actions

Date	Document Description ()
10/18/2016	International Preliminary Report on Patentability Chapte
10/17/2016	Written Opinion of the International Search Authority ()
10/22/2015	International Search Report ()

All Documents | Classification and Citation | View All Office Actions

()	Office ()	Application ()	Applicant	Title ()	App. Date ()	Priority #	Pub. # ()	Pub. Date	A
()	US	14829354	1) Han, Kyung Soo	ADJUSTABLE ASSEMBLY OF ROTOR AND STATOR AND APPLICATIONS THEREOF WITH A VARIABLE POWER GENERATOR	08/18/2015	US 61523846 US 13425501 US PCT/US10/42519 US 14255377 US 14829354 US 13915785 US 13568288 US 62039096 US 61521408	US 20150357951 A1 () US 9490736 B2 ()	12/10/2015 11/08/2016	

Most Recent Documents

Date	Document Description ()	Options
10/19/2016	Issue Notification ()	•••
10/15/2016	Specification ()	•••
10/11/2016	Issue Fee Payment (PTO-85B) ()	•••

Office Actions

Date	Document Description ()
07/14/2016	Notice of Allowance and Fees Due (PTOL-85) ()
05/09/2016	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

()	Office ()	Application ()	Applicant	Title ()	App. Date ()	Priority #	Pub. # ()	Pub. Date	A
()	US	14838867	1) Han, Kyung Soo	MARINE HYDROKINETIC TURBINE	08/28/2015	US 61523846 US 13425501 US PCT/US10/42519 US 13384621 US 14838867 US 14255377 US 14829354 US 13915785 US 13568288 US 62039096 US 61521408	US 20160010620 A1 () US 9476401 B2 ()	01/14/2016 10/25/2016	

Most Recent Documents

Date	Document Description ()	Options
10/05/2016	Issue Notification ()	•••
09/29/2016	List of References cited by applicant and considered by examiner ()	•••
09/29/2016	List of References cited by applicant and considered by examiner ()	•••

Office Actions

Date	Document Description ()
07/20/2016	Notice of Allowance and Fees Due (PTOL-85) ()
07/01/2016	Notice of Allowance and Fees Due (PTOL-85) ()
05/06/2016	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	14860962	1) Han, Kyung Soo	ONE-STROKE INTERNAL COMBUSTION ENGINE	09/22/2015	US 61805584 US 14225658 US 14860962 US 61825560	US 20160025001 A1 () US 9371775 B2 ()	01/28/2016 06/21/2016

Most Recent Documents

Date	Document Description ()	Options
06/01/2016	Issue Notification ()	•••
05/24/2016	Issue Fee Payment (PTO-85B) ()	•••
05/24/2016	Fee Worksheet (SB06) ()	•••

Office Actions

Date	Document Description ()
05/05/2016	Notice of Allowance and Fees Due (PTOL-85) ()
01/13/2016	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	14943898	1) WANG, Shih-Yuan 2) WANG, Shih-Ping	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	11/17/2015	US 62182602 US 62213556 US 62157876 US 14943898 US 62139511 US 62197120 US 62188876 US 62153443 US 62154675 US 62081538 US 62175855 US 62174498 US 62232716 US 62090879 US 62171915 US 62199607 US 62100025 US 62209311 US 62205717 US 62111582	US 20160307939 A1 () US 9530905 B2 ()	10/20/2016 12/27/2016

Most Recent Documents

Date	Document Description ()	Options
11/17/2020	Communication - Re: Power of Attorney (PTOL-308) ()	•••
11/17/2020	Communication - Re: Power of Attorney (PTOL-308) ()	•••
11/10/2020	Power of Attorney ()	•••

Office Actions

Date	Document Description ()
11/03/2016	Notice of Allowance and Fees Due (PTOL-85) ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	15309922	1) WANG, Shih-Yuan 2) WANG, Shih-Ping	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	11/17/2015	US 62182602 US 62213556 US 62157876 US 14943898 US 62139511 US 62197120 US 62188876 US 62153443 US 62154675 US 62081538 US 62175855 US 62174498 US PCT/US15/61120 US 15309922 US 62232716 US 14945003 US 62090879 US 62171915 US 62199607 US 62100025 US 62209311 US 62205717 US 62111582	US 20170194522 A1 () US 9818893 B2 ()	07/06/2017 11/14/2017

()	Office ()	Application ()	Applicant	Title ()	App. Date ()	Priority #	Pub. # ()	Pub. Date	A

Most Recent Documents

Date	Document Description ()	Options
11/17/2020	Communication - Re: Power of Attorney (PTOL-308) ()	•••
11/17/2020	Communication - Re: Power of Attorney (PTOL-308) ()	•••
11/10/2020	Power of Attorney ()	•••

Office Actions

Date	Document Description ()
06/30/2017	Notice of Allowance and Fees Due (PTOL-85) ()

All Documents | Classification and Citation | View All Office Actions

()	EP	15861593	1) Wang, Shih-Yuan,	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	11/17/2015	US 62182602 US 62213556 US 62157876 US 62139511 US 62197120 US 62188876 US 62153443 US 62154675 US 62081538 US 62175855 US 62174498 US PCT/US15/61120 US 62232716 US 62090879 US 62171915 US 62199607 US 62100025 US 62209311 US 62205717 US 62111582	EP 3221895 A1 () EP 3221895 A4 ()	09/27/2017 08/15/2018

Most Recent Documents

Date	Document Description ()	Options
01/12/2022	Letter accompanying subsequently filed items ()	•••
01/12/2022	Reply to communication from the Examining Division ()	•••
01/12/2022	Claims ()	•••

Office Actions

Date	Document Description ()
07/02/2021	Annex to the communication ()
07/16/2018	European search opinion ()
06/07/2017	Copy of the international preliminary report on patentab

All Documents | Classification and Citation | View All Office Actions

()	CN	201580056778	1) Chinese aqua,	Photosensitive Device with Microstructure Enhanced Absorption	11/17/2015	US 62182602 US 62213556 US 62157876 US 62139511 US 62197120 US 62188876 US 62153443 US 62154675 US 62081538 US 62175855 US 62174498 US PCT/US15/61120 US 62232716 US 62090879 US 62171915 US 62199607 US 62100025 US 62209311 US 62205717 US 62111582	CN 107078145 A () CN 107078145 B ()	08/18/2017 05/07/2019

Most Recent Documents

Date	Document Description ()	Options
01/29/2019	Notification to Grant Patent Right for Invention(PCT) (TRANSLATED) ()	•••
01/29/2019	Notification to Grant Patent Right for Invention(PCT) (ORIGINAL) ()	•••
08/31/2018	Claims (ORIGINAL) ()	•••

Office Actions

Date	Document Description ()
01/29/2019	Notification to Grant Patent Right for Invention(PCT) (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

Samsung Exhibit 1003, Page 71 of 516

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	PCT/US15/61120	1) WANG, Shih-Yuan, 2) WANG, Shih-Ping,	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	11/17/2015	US 62182602 US 62213556 US 62157876 US 62139511 US 62197120 US 62188876 US 62153443 US 62154675 US 62081538 US 62175855 US 62174498 US 62232716 US 62090879 US 62171915 US 62199607 US 62100025 US 62209311 US 62205717 US 62111582	WO 2016081476 A1 ()	05/26/2016

Most Recent Documents

Date	Document Description ()	Options
05/23/2017	Notification of Transmittal of Copies of International Preliminary Report on Patentability Chapter I ()	•••
05/23/2017	International Preliminary Report on Patentability Chapter I ()	•••
03/14/2017	Notice Informing The Applicant Of The Communication Of The International Application (To Designated Offices Which Do Not Apply The 30 Month Time Limit Under Article 22(1)) ()	•••

Office Actions

Date	Document Description ()
05/23/2017	International Preliminary Report on Patentability Chapte
05/26/2016	International Search Report ()
05/26/2016	Written Opinion of the International Search Authority ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
JP	2017526132	1) W and W sense Debye seeds and Inc., 2) KOBASHI, Masaaki,	The microstructure enhanced absorption photosensitive device	11/17/2015	US 62182602 US 62213556 US 62157876 US 62139511 US 62197120 US 62188876 US 62153443 US 62154675 US 62081538 US 62175855 US 62174498 US PCT/US15/61120 US 62232716 US 62090879 US 62171915 US 62199607 US 62100025 US 62209311 US 62205717 US 62111582	JP 2018508970 A () JP 6875987 B2 ()	03/29/2018 05/26/2021

Most Recent Documents

Date	Document Description ()	Options
04/06/2021	Decision to Grant a Patent (TRANSLATED) ()	•••
04/06/2021	Decision to Grant a Patent (ORIGINAL) ()	•••
02/25/2021	Written Amendment (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
04/06/2021	Decision to Grant a Patent (TRANSLATED) ()
09/29/2020	Notice of Reasons for Refusal (TRANSLATED) ()
12/03/2019	Notice of Reasons for Refusal (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	14945003	1) WANG, Shih-Yuan 2) Wang, Shih-Ping	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	11/18/2015	US 62182602 US 62213556 US 62157876 US 62139511 US 62197120 US 62188876 US 62153443 US 62154675 US 62081538 US 62175855 US 62174498 US 62232716 US 14945003 US 62090879 US 62171915 US 62199607 US 62100025 US 62209311 US 62205717 US 62111582	US 20160308075 A1 () US 9525084 B2 ()	10/20/2016 12/20/2016

Most Recent Documents

Date	Document Description ()	Options
11/17/2020	Communication - Re: Power of Attorney (PTOL-308) ()	•••
11/17/2020	Communication - Re: Power of Attorney (PTOL-308) ()	•••
11/10/2020	Power of Attorney ()	•••

Office Actions

Date	Document Description ()
10/17/2016	Notice of Allowance and Fees Due (PTOL-85) ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	14947718	1) WANG, Shih-Yuan 2) WANG, Shih-Ping	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	11/20/2015	US 61834873 US 61826446 US 14947718 US 61843021 US PCT/US14/39208 US 61905109	US 20160254407 A1 () US 10622498 B2 ()	09/01/2016 04/14/2020

Most Recent Documents

Date	Document Description ()	Options
11/17/2020	Communication - Re: Power of Attorney (PTOL-308) ()	•••
11/17/2020	Communication - Re: Power of Attorney (PTOL-308) ()	•••
11/10/2020	Power of Attorney ()	•••

Office Actions

Date	Document Description ()
01/03/2020	Notice of Allowance and Fees Due (PTOL-85) ()
12/10/2019	Notice of Allowance and Fees Due (PTOL-85) ()
09/24/2019	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	15011772	1) Han, Kyung Soo	THREE VARIABLE AND FOUR VARIABLE TRANSGEAR ASSEMBLIES	02/01/2016	US 13425501 US 61805584 US 61466056 US PCT/US10/42519 US 13384621 US 12226943 US 14668315 US 15011772 US 14096171 US 61825560 US 14225658	US 20160169353 A1 () US 9506534 B2 ()	06/16/2016 11/29/2016

Most Recent Documents

Date	Document Description ()	Options
11/09/2016	Issue Notification ()	•••
10/28/2016	Issue Fee Payment (PTO-85B) ()	•••
10/28/2016	Fee Worksheet (SB06) ()	•••

Office Actions

Date	Document Description ()
09/02/2016	Notice of Allowance and Fees Due (PTOL-85) ()
07/25/2016	Final Rejection ()
04/11/2016	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	15140295	1) NATHENSON, REBECCA WINDT 2) GOODWIN, Joshua Stephen 3) KESSMAN, Rosalina T. 4) OBEROI, Yukte 5) MANETAKIS, Allison	SYSTEM AND METHODS FOR LEVERAGING CUSTOMER AND COMPANY DATA TO GENERATE RECOMMENDATIONS AND OTHER FORMS OF INTERACTIONS WITH CUSTOMERS	04/27/2016	US 15140295 US 62154975	US 20170236131 A1 ()	08/17/2017

Most Recent Documents

Date	Document Description ()	Options
04/21/2020	Abandonment ()	•••
04/16/2020	Letter Express Abandonment of the application ()	•••
04/16/2020	Electronic Filing System(EFS) Acknowledgment Receipt ()	•••

Office Actions

Date	Document Description ()
12/10/2019	Final Rejection ()
04/16/2019	Non-Final Rejection ()
11/27/2018	Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	15267655	1) Han, Kyung Soo	RENEWABLE ENERGY MARINE HYDROKINETIC OR WIND TURBINE	09/16/2016	US 61523846 US 13425501 US PCT/US10/42519 US 13384621 US 14838867 US 14255377 US 14829354 US 13915785 US 13568288 US 62039096 US 61521408 US 15267655	US 20170030326 A1 () US 9912209 B2 ()	02/02/2017 03/06/2018

Most Recent Documents

Date	Document Description ()	Options
02/14/2018	Issue Notification ()	•••
02/01/2018	List of References cited by applicant and considered by examiner ()	•••
01/23/2018	Issue Fee Payment (PTO-85B) ()	•••

Office Actions

Date	Document Description ()
10/24/2017	Notice of Allowance and Fees Due (PTOL-85) ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
EP	16880012	1) W&WSENS Devices, Inc.,	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	12/21/2016	US 62366188 US 62376869 US 62401126 US 62334934 US 62359349 US 62398607 US 62346850 US 62368109 US 62290391 US 62374828 US 62394222 US 62414671 US 62380364 US 62383391 US PCT/US16/67977 US 62270577 US 62383479 US 62415339 US 62338263 US 62406999 US 62304907	EP 3411906 A1 () EP 3411906 A4 ()	12/12/2018 10/09/2019

Samsung Exhibit 1003, Page 74 of 516

()	Office ()	Application ()	Applicant	Title ()	App. Date ()	Priority #	Pub. # ()	Pub. Date	A

Most Recent Documents

Date	Document Description ()	Options
04/05/2022	Letter accompanying subsequently filed items ()	•••
04/05/2022	Reply to communication from the Examining Division ()	•••
04/05/2022	Claims ()	•••

Office Actions

Date	Document Description ()
11/25/2021	Annex to the communication ()
09/09/2019	European search opinion ()
07/16/2018	Copy of the international preliminary report on patentab

All Documents | Classification and Citation | View All Office Actions

()	Office	Application	Applicant	Title	App. Date	Priority #	Pub. # ()	Pub. Date	A
()	CN	201680082229	1) Vent and Vassens Devices Inc.,	Microstructure Enhanced Absorption Photosensitive Device	12/21/2016	US 62366188 US 62376869 US 62401126 US 62334934 US 62359349 US 62398607 US 62346850 US 62368109 US 62290391 US 62374828 US 62394222 US 62414671 US 62380364 US 62383391 US PCT/US16/67977 US 62270577 US 62383479 US 62415339 US 62338263 US 62406999 US 62304907	CN 109155340 A ()	01/04/2019	

Most Recent Documents

Date	Document Description ()	Options
04/18/2022	Nth Office Action (TRANSLATED) ()	•••
04/18/2022	Nth Office Action (ORIGINAL) ()	•••
06/23/2021	First Office Action(PCT) (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
04/18/2022	Nth Office Action (TRANSLATED) ()
06/23/2021	First Office Action(PCT) (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

()	Office	Application	Applicant	Title	App. Date	Priority #	Pub. # ()	Pub. Date	A
()	US	PCT/US16/67977	1) W&WSENS DEVICES, INC.,	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	12/21/2016	US 62366188 US 62376869 US 62401126 US 62334934 US 62359349 US 62398607 US 62346850 US 62368109 US 62290391 US 62394222 US 62414671 US 62380364 US 62383391 US 62270577 US 62383479 US 62415339 US 62338263 US 62406999 US 62304907	WO 2017112747 A1 ()	06/29/2017	

Most Recent Documents

Date	Document Description ()	Options
06/26/2018	Notification of Transmittal of Copies of International Preliminary Report on Patentability Chapter I ()	•••
06/26/2018	International Preliminary Report on Patentability Chapter I ()	•••
04/17/2018	Notice Informing The Applicant Of The Communication Of The International Application (To Designated Offices Which Do Not Apply The 30 Month Time Limit Under Article 22(1)) ()	•••

Office Actions

Date	Document Description ()
06/26/2018	International Preliminary Report on Patentability Chapte
06/29/2017	International Search Report ()
06/29/2017	Written Opinion of the International Search Authority ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	15675346	1) NIPPES, JOSEPH TIMOTHY	LEAD SERVICE WATER PIPE LINE REMOVAL APPARATUS AND METHOD	08/11/2017	US 62374828 US 15675346	US 20180045334 A1 ()	02/15/2018

Most Recent Documents

Date	Document Description ()	Options
01/09/2019	Abandonment ()	•••
06/04/2018	Non-Final Rejection ()	•••
06/04/2018	Search information including classification, databases and other search related notes ()	•••

Office Actions

Date	Document Description ()
06/04/2018	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	15707138	1) Han, Kyung Soo	COMMUTATOR-LESS AND BRUSH-LESS DIRECT CURRENT GENERATOR AND APPLICATIONS FOR GENERATING POWER TO AN ELECTRIC POWER SYSTEM	09/18/2017	US 61523846 US 13425501 US 15707138 US PCT/US10/42519 US 13915785 US 62039096 US 61521408 US 13384621 US 14838867 US 14255377 US 14829354 US 62409549 US 13568288 US 15267655	US 20180038340 A1 () US 10378506 B2 ()	02/08/2018 08/13/2019

Most Recent Documents

Date	Document Description ()	Options
09/03/2019	Mail returned to USPTO as undelivered ()	•••
09/03/2019	Artifact sheet indicating an item has been filed which cannot be scanned ()	•••
07/24/2019	Issue Notification ()	•••

Office Actions

Date	Document Description ()
05/20/2019	Notice of Allowance and Fees Due (PTOL-85) ()
09/24/2018	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	15797821	1) WANG, Shih-Yuan 2) WANG, Shih-Ping 3) Islam, M. Saif	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	10/30/2017	US 61826446 US 62182602 US 62157876 US 14943898 US 62188876 US 62175855 US 15797821 US 62174498 US 61834873 US 14947718 US 62270577 US 62232716 US 14945003 US 62415339 US 62199607 US 15309922 US 62100025 US 62209311 US PCT/US14/39208 US 62213556 US 62139511 US 62197120 US 62153443 US 62154675 US 61843021 US 62081538 US 61905109 US PCT/US15/61120 US PCT/US16/67977 US 62090879 US 62171915 US 62205717 US 62111582	US 20180102442 A1 () US 10446700 B2 ()	04/12/2018 10/15/2019

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	15883927	1) Han, Kyung Soo	CONTROL APPARATUS AND METHOD FOR VARIABLE RENEWABLE ENERGY	01/30/2018	US 15707138 US 14838867 US 62487101 US 15883927 US 62520884 US 62409549 US 15267655	US 20180195582 A1 () US 10670116 B2 ()	07/12/2018 06/02/2020

Most Recent Documents

Date	Document Description ()	Options
11/24/2020	Certificate of Correction - Post Issue Communication ()	•••
11/17/2020	Communication - Re: Power of Attorney (PTOL-308) ()	•••
11/17/2020	Communication - Re: Power of Attorney (PTOL-308) ()	•••

Office Actions

Date	Document Description ()
05/07/2019	Notice of Allowance and Fees Due (PTOL-85) ()
03/26/2019	Non-Final Rejection ()
02/06/2019	Notice of Allowance and Fees Due (PTOL-85) ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	16001019	1) Damphousse, Kurt P. 2) Logan, Stephen D. 3) Macdonald, John 4) Martz, Kenneth	UPSET PROTRUSION JOINING AND FORGING GUN THEREFOR	06/06/2018	US 62522187 US 16001019	US 20180361463 A1 () US 10807148 B2 ()	12/20/2018 10/20/2020

Most Recent Documents

Date	Document Description ()	Options
09/30/2020	Issue Notification ()	•••
09/16/2020	Issue Fee Payment (PTO-85B) ()	•••
09/16/2020	Fee Worksheet (SB06) ()	•••

Office Actions

Date	Document Description ()
07/23/2020	Notice of Allowance and Fees Due (PTOL-85) ()
03/27/2020	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
CN	PCT/CN2018/091383	1) SUNSTONE SCIENTIFIC LIMITED.,	PARAFFIN SHIELD COATING FOR MICROSCOPE SLIDE	06/15/2018	US 62520169 US 62520319	WO 2018228508 A1 ()	12/20/2018

Most Recent Documents

Date	Document Description ()	Options
12/17/2019	Notification of Transmittal of Copies of International Preliminary Report on Patentability Chapter I ()	•••
12/17/2019	International Preliminary Report on Patentability Chapter I ()	•••
10/08/2019	Notice Informing The Applicant Of The Communication Of The International Application (To Designated Offices Which Do Not Apply The 30 Month Time Limit Under Article 22(1)) ()	•••

Office Actions

Date	Document Description ()
12/17/2019	International Preliminary Report on Patentability Chapte
12/20/2018	International Search Report ()
12/20/2018	Written Opinion of the International Search Authority ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
JP	2020519173	1) Shenzhen PR S Limited, 2) Patent business corporation Hokuto patent firm,	The process recording of slides for immunohistochemical staining.	06/15/2018	US 62520169 US 62520178 US 62539281 CN 2018091686 US 62520187 US 62520319	JP 2020523614 A ()	08/06/2020

()	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date	
()	JP	2020519174	1) Shenzhen PR S Limited, 2) Patent business corporation Hokuto patent firm,	The process records the special staining.	06/15/2018	US 62520169 CN 2018091687 US 62520178 US 62520334 US 62520341	JP 2020523615 A ()	08/06/2020	

Most Recent Documents

Date	Document Description ()	Options
10/17/2022	Written Opinion (TRANSLATED) ()	•••
10/17/2022	Written Opinion (ORIGINAL) ()	•••
08/17/2022	Request for Extension of Time Limits (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
05/17/2022	Notice of Reasons for Refusal (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

()	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date	
()	JP	2020519171	1) Shenzhen PR S Limited, 2) Patent business corporation Hokuto patent firm,	Process for the preparation of microscope slides with paraffin PROTECTIVE COATING	06/15/2018	US 62520169 CN 2018091383 US 62520319	JP 2020523613 A ()	08/06/2020	

Most Recent Documents

Date	Document Description ()	Options
08/10/2022	Written Amendment (TRANSLATED) ()	•••
08/10/2022	Written Amendment (ORIGINAL) ()	•••
08/10/2022	Written Opinion (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
05/10/2022	Notice of Reasons for Refusal (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

()	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date	
()	JP	2020519172	1) Shenzhen PR S Limited, 2) Patent business corporation Hokuto patent firm,	A microscope slide with a black and white target integrated.	06/15/2018	CN 2018091685 US 62520178	JP 2020523646 A ()	08/06/2020	

Most Recent Documents

Date	Document Description ()	Options
07/25/2022	Written Opinion (TRANSLATED) ()	•••
07/25/2022	Written Opinion (ORIGINAL) ()	•••
07/25/2022	Written Amendment (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
04/26/2022	Notice of Reasons for Refusal (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

()	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date	
()	JP	2020519175	1) Shenzhen PR S Limited, 2) Patent business corporation Hokuto patent firm,	The method of extrapolation of the IHC antigen imaging	06/15/2018	CN 2018091689 US 62520187 US 62520319	JP 2020523616 A ()	08/06/2020	

Most Recent Documents

Date	Document Description ()	Options
09/07/2022	Written Opinion (TRANSLATED) ()	•••
09/07/2022	Written Opinion (ORIGINAL) ()	•••
09/07/2022	Written Amendment (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
06/07/2022	Notice of Reasons for Refusal (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

Samsung Exhibit 1003, Page 78 of 516

()	Office ()	Application ()	Applicant	Title ()	App. Date ()	Priority #	Pub. # ()	Pub. Date	A
()	KR	20207001301	1) SHENZHEN PRS LIMITED,	METHOD FOR IHC ANTIGEN IMAGING SCALE EXTRAPOLATION	06/15/2018	CN 2018091689 US 62520187 US 62520319	KR 20200041861 A () KR 102342988 B1 ()	04/22/2020 12/27/2021	

Most Recent Documents

Date	Document Description ()	Options
08/17/2022	Written Amendment (TRANSLATED) ()	•••
08/17/2022	Written Amendment (ORIGINAL) ()	•••
08/17/2022	Written Opinion (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
05/17/2022	Notice of Reasons for Refusal (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

()	Office ()	Application ()	Applicant	Title ()	App. Date ()	Priority #	Pub. # ()	Pub. Date	A
()	CN	201880039196	1) Shenzhen Novo Experimental Devices Ltd.,	Process recording slides for immunohistochemical staining	06/15/2018	US 62520169 US 62520178 US 62539281 CN 2018091686 US 62520187 US 62520319	CN 110741302 A () CN 110741302 B ()	01/31/2020 11/16/2021	

Most Recent Documents

Date	Document Description ()	Options
09/26/2021	Written Decision on Registration (TRANSLATED) ()	•••
09/26/2021	Written Decision on Registration (ORIGINAL) ()	•••
06/23/2021	Amendment to Bibliographic Information (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
09/26/2021	Written Decision on Registration (TRANSLATED) ()
01/19/2021	Request for the Submission of an Opinion (TRANSLATED

All Documents | Classification and Citation | View All Office Actions

()	Office ()	Application ()	Applicant	Title ()	App. Date ()	Priority #	Pub. # ()	Pub. Date	A
()	CN	201880040066	1) Shenzhen Novo Experimental Devices Ltd.,	Process recording slides for specific staining	06/15/2018	US 62520169 CN 2018091687 US 62520178 US 62520334 US 62520341	CN 110753869 A () CN 110753869 B ()	02/04/2020 05/17/2022	

Most Recent Documents

Date	Document Description ()	Options
09/10/2021	Notification to Grant Patent Right for Invention(PCT) (TRANSLATED) ()	•••
09/10/2021	Notification to Grant Patent Right for Invention(PCT) (ORIGINAL) ()	•••
09/01/2021	Supplementary search (ORIGINAL) ()	•••

Office Actions

Date	Document Description ()
09/10/2021	Notification to Grant Patent Right for Invention(PCT) (TRANSLATED) ()
03/30/2021	First Office Action(PCT) (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

()	Office ()	Application ()	Applicant	Title ()	App. Date ()	Priority #	Pub. # ()	Pub. Date	A
()	CN	201880039119	1) Shenzhen Novo Experimental Devices Ltd.,	Paraffin Barrier Coating Layer for Microscope Slides	06/15/2018	US 62520169 CN 2018091383 US 62520319	CN 110741301 A () CN 110741301 B ()	01/31/2020 11/05/2021	

Most Recent Documents

Date	Document Description ()	Options
01/28/2022	Notification to Grant Patent Right for Invention(PCT) (TRANSLATED) ()	•••
01/28/2022	Notification to Grant Patent Right for Invention(PCT) (ORIGINAL) ()	•••
10/08/2021	Nth Office Action (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
01/28/2022	Notification to Grant Patent Right for Invention(PCT) (TRANSLATED) ()
10/08/2021	Nth Office Action (TRANSLATED) ()
04/01/2021	First Office Action(PCT) (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
CN	201880038946 Refresh Dossier ()			06/15/2018	CN 2018091689 US 62520187 US 62520319	CN 110753846 A ()	02/04/2020
EP	18818678	1) Shenzhen PRS Limited,	PROCESS RECORD SLIDE FOR SPECIAL STAINING	06/15/2018	US 62520169 CN 2018091687 US 62520178 US 62520334 US 62520341	EP 3639080 A1 () EP 3639080 A4 ()	04/22/2020 04/14/2021

Most Recent Documents

Date	Document Description ()
08/19/2021	Notification to Grant Patent Right for Invention(PCT) (TRANSLATED) ()
08/19/2021	Notification to Grant Patent Right for Invention(PCT) (ORIGINAL) ()
08/12/2021	Supplementary search (ORIGINAL) ()

Office Actions

Date	Document Description ()
08/19/2021	Notification to Grant Patent Right for Invention(PCT) (TRANSLATED) ()
03/23/2021	First Office Action(PCT) (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

Most Recent Documents

Date	Document Description ()
07/06/2022	Notice on debiting of fees ()
10/01/2021	Letter accompanying subsequently filed items ()
10/01/2021	Amended claims filed after receipt of (European) search report ()

Office Actions

Date	Document Description ()
03/15/2021	European search opinion ()
01/03/2020	Copy of the international preliminary report on patentab

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
CN	201880039127	1) Shenzhen Novo Experimental Devices Ltd.,	Microscope Slides Integrated Black and White Targets	06/15/2018	CN 2018091685 US 62520178	CN 110770553 A ()	02/07/2020

Most Recent Documents

Date	Document Description ()
12/03/2021	Nth Office Action (TRANSLATED) ()
12/03/2021	Nth Office Action (ORIGINAL) ()
04/25/2021	First Office Action(PCT) (TRANSLATED) ()

Office Actions

Date	Document Description ()
12/03/2021	Nth Office Action (TRANSLATED) ()
04/25/2021	First Office Action(PCT) (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
EP	18816945	1) Shenzhen PRS Limited,	METHOD FOR IHC ANTIGEN IMAGING SCALE EXTRAPOLATION	06/15/2018	CN 2018091689 US 62520187 US 62520319	EP 3639031 A1 () EP 3639031 A4 ()	04/22/2020 05/05/2021

Most Recent Documents

Date	Document Description ()
07/06/2022	Notice on debiting of fees ()
10/29/2021	Letter accompanying subsequently filed items ()
10/29/2021	Amendments received before examination ()

Office Actions

Date	Document Description ()
04/01/2021	European search opinion ()
01/03/2020	Copy of the international preliminary report on patentab

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
EP	18817800	1) Shenzhen PRS Limited,	PARAFFIN SHIELD COATING FOR MICROSCOPE SLIDE	06/15/2018	US 62520169 CN 2018091383 US 62520319	EP 3639078 A1 () EP 3639078 A4 ()	04/22/2020 03/31/2021

Samsung Exhibit 1003, Page 80 of 516

	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
⊟	EP	18817809	1) Shenzhen PRS Limited,	MICROSCOPE SLIDE WITH INTEGRATED BLACK AND WHITE TARGET	06/15/2018	CN 2018091685 US 62520178	EP 3638995 A1 EP 3638995 A4	04/22/2020 03/31/2021

Most Recent Documents

Date	Document Description	Options
07/06/2022	Notice on debiting of fees	•••
10/04/2021	Letter accompanying subsequently filed items	•••
10/04/2021	Amended claims filed after receipt of (European) search report	•••

Office Actions

Date	Document Description
03/03/2021	European search opinion
01/03/2020	Copy of the international preliminary report on patentab

All Documents | Classification and Citation | View All Office Actions

	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
⊟	EP	18817809	1) Shenzhen PRS Limited,	MICROSCOPE SLIDE WITH INTEGRATED BLACK AND WHITE TARGET	06/15/2018	CN 2018091685 US 62520178	EP 3638995 A1 EP 3638995 A4	04/22/2020 03/31/2021

Most Recent Documents

Date	Document Description	Options
07/06/2022	Notice on debiting of fees	•••
09/13/2021	Letter accompanying subsequently filed items	•••
09/13/2021	Amendments received before examination	•••

Office Actions

Date	Document Description
02/26/2021	European search opinion
01/03/2020	Copy of the international preliminary report on patentab

All Documents | Classification and Citation | View All Office Actions

	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
⊟	KR	20207001292	1) SHENZHEN PRS LIMITED,	MICROSCOPE SLIDE WITH INTEGRATED BLACK AND WHITE TARGET	06/15/2018	CN 2018091685 US 62520178	KR 20200040746 A	04/20/2020

Most Recent Documents

Date	Document Description	Options
09/21/2022	Request for Extension of Designated Period (TRANSLATED)	•••
09/21/2022	Request for Extension of Designated Period (ORIGINAL)	•••
07/27/2022	Request for the Submission of an Opinion (TRANSLATED)	•••

Office Actions

Date	Document Description
05/24/2021	Request for the Submission of an Opinion (TRANSLATED

All Documents | Classification and Citation | View All Office Actions

	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
⊟	CN	PCT/CN2018/091685	1) SUNSTONE SCIENTIFIC LIMITED.,	MICROSCOPE SLIDE WITH INTEGRATED BLACK AND WHITE TARGET	06/15/2018	US 62520178	WO 2018228574 A1	12/20/2018

Most Recent Documents

Date	Document Description	Options
12/17/2019	Notification of Transmittal of Copies of International Preliminary Report on Patentability Chapter I	•••
12/17/2019	International Preliminary Report on Patentability Chapter I	•••
10/08/2019	Notice Informing The Applicant Of The Communication Of The International Application (To Designated Offices Which Do Not Apply The 30 Month Time Limit Under Article 22(1))	•••

Office Actions

Date	Document Description
12/17/2019	International Preliminary Report on Patentability Chapte
12/20/2018	International Search Report
12/20/2018	Written Opinion of the International Search Authority

All Documents | Classification and Citation | View All Office Actions

	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
⊟	EP	18817810	1) Shenzhen PRS Limited,	PROCESS RECORD SLIDE FOR IMMUNOHISTOCHEMICAL STAINING	06/15/2018	US 62520169 US 62520178 US 62539281 CN 2018091686 US 62520187 US 62520319	EP 3639079 A1 EP 3639079 A4	04/22/2020 02/24/2021

Most Recent Documents

Date	Document Description	Options
07/06/2022	Notice on debiting of fees	•••
08/09/2021	Letter accompanying subsequently filed items	•••
08/09/2021	Amendments received before examination	•••

Office Actions

Date	Document Description
01/22/2021	European search opinion
01/03/2020	Copy of the international preliminary report on patentab

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
CN	PCT/CN2018/091689	1) SUNSTONE SCIENTIFIC LIMITED,,	METHOD FOR IHC ANTIGEN IMAGING SCALE EXTRAPOLATION	06/15/2018	US 62520187 US 62520319	WO 2018228577 A1 ()	12/20/2018

Most Recent Documents

Date	Document Description ()	Options
12/17/2019	Notification of Transmittal of Copies of International Preliminary Report on Patentability Chapter I ()	•••
12/17/2019	International Preliminary Report on Patentability Chapter I ()	•••
10/08/2019	Notice Informing The Applicant Of The Communication Of The International Application (To Designated Offices Which Do Not Apply The 30 Month Time Limit Under Article 22(1)) ()	•••

Office Actions

Date	Document Description ()
12/17/2019	International Preliminary Report on Patentability Chapte
12/20/2018	International Search Report ()
12/20/2018	Written Opinion of the International Search Authority ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
CN	PCT/CN2018/091687	1) SUNSTONE SCIENTIFIC LIMITED,,	PROCESS RECORD SLIDE FOR SPECIAL STAINING	06/15/2018	US 62520169 US 62520178 US 62520334 US 62520341	WO 2018228576 A1 ()	12/20/2018

Most Recent Documents

Date	Document Description ()	Options
12/17/2019	Notification of Transmittal of Copies of International Preliminary Report on Patentability Chapter I ()	•••
12/17/2019	International Preliminary Report on Patentability Chapter I ()	•••
10/08/2019	Notice Informing The Applicant Of The Communication Of The International Application (To Designated Offices Which Do Not Apply The 30 Month Time Limit Under Article 22(1)) ()	•••

Office Actions

Date	Document Description ()
12/17/2019	International Preliminary Report on Patentability Chapte
12/20/2018	International Search Report ()
12/20/2018	Written Opinion of the International Search Authority ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
CN	PCT/CN2018/091686	1) SUNSTONE SCIENTIFIC LIMITED,,	PROCESS RECORD SLIDE FOR IMMUNOHISTOCHEMICAL STAINING	06/15/2018	US 62520169 US 62520178 US 62539281 US 62520187 US 62520319	WO 2018228575 A1 ()	12/20/2018

Most Recent Documents

Date	Document Description ()	Options
12/17/2019	Notification of Transmittal of Copies of International Preliminary Report on Patentability Chapter I ()	•••
12/17/2019	International Preliminary Report on Patentability Chapter I ()	•••
10/08/2019	Notice Informing The Applicant Of The Communication Of The International Application (To Designated Offices Which Do Not Apply The 30 Month Time Limit Under Article 22(1)) ()	•••

Office Actions

Date	Document Description ()
12/17/2019	International Preliminary Report on Patentability Chapte
12/20/2018	International Search Report ()
12/20/2018	Written Opinion of the International Search Authority ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
KR	20207001297	1) SHENZHEN PRS LIMITED,	PROCESS RECORD SLIDE FOR SPECIAL STAINING	06/15/2018	US 62520169 CN 2018091687 US 62520178 US 62520334 US 62520341	KR 20200040748 A () KR 102378095 B1 ()	04/20/2020 03/23/2022

Most Recent Documents

Date	Document Description ()	Options
12/28/2021	Written Decision on Registration (TRANSLATED) ()	•••
12/28/2021	Written Decision on Registration (ORIGINAL) ()	•••
08/11/2021	Written Opinion (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
12/28/2021	Written Decision on Registration (TRANSLATED) ()
05/28/2021	Request for the Submission of an Opinion (TRANSLATED

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
KR	20207001295	1) SHENZHEN PRS LIMITED,	PROCESS RECORD SLIDE FOR IMMUNOHISTOCHEMICAL STAINING	06/15/2018	US 62520169 US 62520178 US 62539281 CN 2018091686 US 62520187 US 62520319	KR 20200040747 A () KR 102342993 B1 ()	04/20/2020 12/27/2021

Samsung Exhibit 1003, Page 82 of 516

()	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
()	KR	20207001289	1) SHENZHEN PRS LIMITED,	PARAFFIN SHIELD COATING FOR MICROSCOPE SLIDE	06/15/2018	US 62520169 CN 2018091383 US 62520319	KR 20200036849 A () KR 102368836 B1 ()	04/07/2020 02/28/2022

Most Recent Documents

Date	Document Description ()	Options
11/26/2021	Written Decision on Registration (TRANSLATED) ()	•••
11/26/2021	Written Decision on Registration (ORIGINAL) ()	•••
07/22/2021	Written Opinion (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
11/26/2021	Written Decision on Registration (TRANSLATED) ()
04/30/2021	Request for the Submission of an Opinion (TRANSLATED
10/30/2020	Request for the Submission of an Opinion (TRANSLATED

All Documents | Classification and Citation | View All Office Actions

()	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
()	US	PCT/US18/43289	1) W&WSENS, DEVICES INC.,	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	07/23/2018	US 62669194 US 62633514 US 62659067 US 62645810 US 62615314 US 62628764 US 62631630 US 62556426 US 62623971 US 62542243 US 62591072 US 62651087 US 62639920 US 62634692 US 62640522 US 62639356 US 62607860 US 62547728 US 62599246 US 62659072 US 62662217 US 62675130 US 62651053 US 62561869 US 62639472 US 62535801 US 62677609 US 62637945 US 62540524 US 62646871 US 62652830 US 62666005 US 62682909 US 62553844 US 62643010	WO 2019018846 A2 () WO 2019018846 A3 ()	01/24/2019 03/28/2019

Most Recent Documents

Date	Document Description ()	Options
01/21/2020	Notification of Transmittal of Copies of International Preliminary Report on Patentability Chapter I ()	•••
01/21/2020	International Preliminary Report on Patentability Chapter I ()	•••
11/12/2019	Notice Informing The Applicant Of The Communication Of The International Application (To Designated Offices Which Do Not Apply The 30 Month Time Limit Under Article 22(1)) ()	•••

Office Actions

Date	Document Description ()
01/21/2020	International Preliminary Report on Patentability Chapte
02/25/2019	International Search Report ()
01/24/2019	Written Opinion of the International Search Authority ()

All Documents | Classification and Citation | View All Office Actions

	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
	EP	18835833	1) W&WSENS Devices, Inc.,	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	07/23/2018	US 62669194 US 62633514 US 62659067 US 62645810 US 62615314 US 62628764 US 62631630 US 62556426 US 62623971 US 62542243 US 62591072 US 62651087 US 62639920 US 62634692 US 62640522 US PCT/US18/43289 US 62639356 US 62607860 US 62547728 US 62599246 US 62659072 US 62662217 US 62675130 US 62651053 US 62561869 US 62639472 US 62535801 US 62677609 US 62637945 US 62540524 US 62646871 US 62652830 US 62666005 US 62682909 US 62553844 US 62643010	EP 3656000 A2 EP 3656000 A4	05/27/2020 08/04/2021

Most Recent Documents

Date	Document Description	Options
01/31/2022	Letter accompanying subsequently filed items	•••
01/31/2022	Amended claims filed after receipt of (European) search report	•••
01/31/2022	Amended claims with annotations	•••

Office Actions

Date	Document Description
07/01/2021	European search opinion
02/03/2020	Copy of the international preliminary report on patentab

All Documents | Classification and Citation | View All Office Actions

	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
()	JP	2020502957	1) W and W sense Debye seeds and Inc., 2) KOBASHI, Masaaki,	The microstructure enhanced absorption photosensitive device	07/23/2018	US 62669194 US 62633514 US 62659067 US 62645810 US 62615314 US 62628764 US 62631630 US 62556426 US 62623971 US 62542243 US 62591072 US 62651087 US 62639920 US 62634692 US 62640522 US PCT/US18/43289 US 62639356 US 62607860 US 62547728 US 62599246 US 62659072 US 62662217 US 62675130 US 62651053 US 62561869 US 62639472 US 62535801 US 62677609 US 62637945 US 62540524 US 62646871 US 62652830 US 62666005 US 62682909 US 62553844 US 62643010	JP 2020537816 A ()	12/24/2020

Most Recent Documents

Date	Document Description ()	Options
10/11/2022	Written Amendment (TRANSLATED) ()	•••
10/11/2022	Written Amendment (ORIGINAL) ()	•••
10/11/2022	Written Opinion (TRANSLATED) ()	•••

Office Actions

Date	Document Description ()
04/12/2022	Notice of Reasons for Refusal (TRANSLATED) ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
CN	201880061391 Refresh Dossier ()			07/23/2018	US 62669194 US 62633514 US 62659067 US 62645810 US 62615314 US 62628764 US 62631630 US 62556426 US 62623971 US 62542243 US 62591072 US 62651087 US 62639920 US 62634692 US 62640522 US PCT/US18/43289 US 62639356 US 62607860 US 62547728 US 62599246 US 62659072 US 62662217 US 62675130 US 62651053 US 62561869 US 62639472 US 62535801 US 62677609 US 62637945 US 62540524 US 62646871 US 62652830 US 62666005 US 62682909 US 62553844 US 62643010	CN 111133590 A ()	05/08/2020
US	16042535	1) WANG, Shih-Yuan 2) WANG, Shih-Ping	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	07/23/2018	US 61826446 US 62182602 US 62157876 US 14943898 US 62188876 US 62175855 US 15797821 US 62174498 US 61834873 US 14947718 US 62270577 US 62232716 US 14945003 US 62415339 US 62199607 US 15309922 US 62100025 US 62209311 US PCT/US14/39208 US 62213556 US 62139511 US 62197120 US 62153443 US 62154675 US 61843021 US 62081538 US 61905109 US PCT/US15/61120 US 16042535 US PCT/US16/67977 US 62090879 US 62171915 US 62205717 US 62111582	US 20190019899 A1 () US 10700225 B2 ()	01/17/2019 06/30/2020

Most Recent Documents

Date	Document Description ()	Options
11/17/2020	Communication - Re: Power of Attorney (PTOL-308) ()	...
11/17/2020	Communication - Re: Power of Attorney (PTOL-308) ()	...
11/10/2020	Power of Attorney ()	...

Office Actions

Date	Document Description ()
05/19/2020	Notice of Allowance and Fees Due (PTOL-85) ()
02/27/2020	Notice of Allowance and Fees Due (PTOL-85) ()
10/08/2019	Notice of Allowance and Fees Due (PTOL-85) ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	16121073	1) NIPPES, JOSEPH TIMOTHY	LEAD SERVICE WATER PIPE LINE REMOVAL APPARATUS AND METHOD	09/04/2018	US 16121073 US 15675346	US 20190049041 A1 () US 10550961 B2 ()	02/14/2019 02/04/2020

Most Recent Documents

Date	Document Description ()	Options
04/13/2020	Change of Address via Patent Application Information Retrieval (PAIR) ()	•••
04/13/2020	Change of Address via Patent Application Information Retrieval (PAIR) ()	•••
04/13/2020	Change of Address via Patent Application Information Retrieval (PAIR) ()	•••

Office Actions

Date	Document Description ()
10/07/2019	Notice of Allowance and Fees Due (PTOL-85) ()
07/31/2019	Final Rejection ()
05/20/2019	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	16134595	1) Han, Kyung Soo	RIVER AND TIDAL TURBINE WITH POWER CONTROL	09/18/2018	US 15707138 US 14838867 US 16134595 US 62487101 US 15883927 US 62520884 US 62409549 US 15267655	US 20190048845 A1 () US 10982645 B2 ()	02/14/2019 04/20/2021

Most Recent Documents

Date	Document Description ()	Options
03/31/2021	Issue Notification ()	•••
03/24/2021	Specification ()	•••
03/24/2021	List of References cited by applicant and considered by examiner ()	•••

Office Actions

Date	Document Description ()
12/07/2020	Notice of Allowance and Fees Due (PTOL-85) ()
07/09/2020	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	PCT/US18/57963	1) W&WSENS DEVICES INC.,	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	10/29/2018	US 15797821	WO 2019089437 A1 ()	05/09/2019

Most Recent Documents

Date	Document Description ()	Options
04/30/2020	International Preliminary Report on Patentability Chapter II (IPEA/409) ()	•••
02/25/2020	Notice Informing The Applicant Of The Communication Of The International Application (To Designated Offices Which Do Not Apply The 30 Month Time Limit Under Article 22(1)) ()	•••
05/21/2019	Notice Informing The Applicant Of The Communication Of The International Application (To Designated Offices Which Do Not Apply The 30 Month Time Limit Under Article 22(1)) ()	•••

Office Actions

Date	Document Description ()
04/30/2020	International Preliminary Report on Patentability Chapter (IPEA/409) ()
05/09/2019	International Search Report ()
05/09/2019	Written Opinion of the International Search Authority ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	16233365	1) Han, Kyung Soo	Expandable Power Marine Hydrokinetic Turbines, Pumps, Compressors and Transmissions	12/27/2018	US 16134595 US 16233365	US 20200088156 A1 () US 10947956 B2 ()	03/19/2020 03/16/2021

Most Recent Documents

Date	Document Description ()	Options
02/24/2021	Issue Notification ()	•••
02/10/2021	Issue Fee Payment (PTO-85B) ()	•••
02/10/2021	Fee Worksheet (SB06) ()	•••

Office Actions

Date	Document Description ()
01/08/2021	Notice of Allowance and Fees Due (PTOL-85) ()
06/11/2020	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

	Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
⊟	US	16296985	1) WANG, Shih-Yuan 2) WANG, Shih-Ping 3) ISLAM, M. Saif	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	03/08/2019	US 62366188 US 61826446 US 62376869 US 62488998 US 62157876 US 14943898 US 62188876 US 62368109 US 62154975 US 62290391 US 62175855 US 15797821 US 62174498 US 61834873 US 62270577 US 62232716 US 62383479 US 62338263 US 62199607 US 62484474 US 15309922 US 62100025 US 62209311 US PCT/US14/39208 US 62213556 US 62398607 US 62139511 US 62197120 US 62153443 US 62154675 US 62530281 US 61843021 US 62527962 US 62533078 US 62533603 US 62465734 US 62540524 US 62090879 US 62553844 US 62111582 US 62510249 US 62182602 US 62334934 US 62522169 US 62359349 US 62346850 US 16296985 US 62380364 US 14947718 US 62556426 US 62542243 US 14945003 US 62415339 US 62509093 US 62401126 US 62547728 US 62474179 US 62374828 US 62521507 US 62081538 US 62394222 US 62414671 US 62487606 US 62505974 US 62561869 US PCT/US15/61120 US 62383391 US PCT/US16/67977 US 62535801 US 62514889 US 62171915 US 62406999 US 62500581 US 62304907 US 62205717	US 20190288132 A1 US 10468543 B2	09/19/2019 11/05/2019

()	Office ()	Application ()	Applicant	Title ()	App. Date ()	Priority #	Pub. # ()	Pub. Date	A
⊟ ()	US	16528958	1) WANG, Shih-Yuan 2) WANG, Shih-Ping	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	08/01/2019	US 62797141 US 62376869 US 62488998 US 62633514 US 62188876 US 15797821 US 62174498 US 62863231 US 62591072 US 62794330 US 62797263 US 62800371 US 62484474 US 62100025 US 62808949 US 62860115 US 62213556 US 62659072 US 62819604 US 62154675 US 62841798 US 62651053 US 16528958 US 16042535 US 62873891 US 62090879 US 62652830 US 62553844 US 62779693 US 62182602 US 62669194 US 62784342 US 62819669 US 62359349 US 62346850 US 62659067 US 62615314 US PCT/US18/57963 US 62380364 US 62556426 US 62542243 US 62639920 US 14945003 US 62640522 US PCT/US18/43289 US 62547728 US 62599246 US 62374828 US 62394222 US 62724449 US 62414671 US 62505974 US 62561869 US 62868911 US PCT/US15/61120 US 62383391 US PCT/US16/67977 US 62677609 US 62867186 US 62171915 US 62406999 US 62646871 US 62846554 US 62366188 US 61826446 US 62802171 US 62750016 US 62157876 US 62870533 US 14943898 US 62368109 US 62719689	US 20200028000 A1 () US 11121271 B2 ()	01/23/2020 09/14/2021	

Most Recent Documents

Date	Document Description ()	Options
11/17/2020	Communication - Re: Power of Attorney (PTOL-308) ()	•••
11/10/2020	Power of Attorney ()	•••
11/10/2020	Electronic Filing System(EFS) Acknowledgment Receipt ()	•••

Office Actions

Date	Document Description ()
10/03/2019	Notice of Allowance and Fees Due (PTOL-85) ()
08/15/2019	Notice of Allowance and Fees Due (PTOL-85) ()

All Documents | Classification and Citation | View All Office Actions

()	Office ()	Application ()	Applicant	Title ()	App. Date ()	Priority #	Pub. # ()	Pub. Date
						US 62290391		
						US 62175855		
						US 61834873		
						US 62628764		
						US 62828976		
						US 62853280		
						US 62802718		
						US 62623971		
						US 62270577		
						US 62651087		
						US 62232716		
						US 62383479		
						US 62338263		
						US 62634692		
						US 62199607		
						US 15309922		
						US 62639356		
						US 62209311		
						US 62607860		
						US PCT/US14/39208		
						US 62805850		
						US 62398607		
						US 62139511		
						US 62197120		
						US 62737062		
						US 62843206		
						US 62153443		
						US 62530281		
						US 62772498		
						US 62777157		
						US 61843021		
						US 62675130		
						US 62527962		
						US 62533078		
						US 61905109		
						US 62874418		
						US 62533603		
						US 62820695		
						US 62639472		
						US 62770656		
						US 62465734		
						US 62540524		
						US 62682909		
						US 62643010		
						US 62111582		
						US 62510249		
						US 62863852		
						US 62334934		
						US 62522169		
						US 62645810		
						US 62717750		
						US 16296985		
						US 14947718		
						US 62631630		
						US 62415339		
						US 62509093		
						US 62401126		
						US 62474179		
						US 62662217		
						US 62081538		
						US 62713455		
						US 62487606		
						US 62733476		
						US 62535801		
						US 62514889		
						US 62637945		
						US 62716310		
						US 62521504		
						US 62500581		
						US 62666005		
						US 62304907		
						US 62205717		

Most Recent Documents

Date	Document Description ()	Options
08/25/2021	Issue Notification ()	...
08/13/2021	List of References cited by applicant and considered by examiner ()	...
08/09/2021	Transmittal Letter ()	...

Office Actions

Date	Document Description ()
05/12/2021	Notice of Allowance and Fees Due (PTOL-85) ()
01/25/2021	Notice of Allowance and Fees Due (PTOL-85) ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	16701741	1) Han, Kyung Soo	Concentric Wing Turbines	12/03/2019	US 62779693 US 16701741 US 16233365	US 20200191120 A1 () US 10815968 B2 ()	06/18/2020 10/27/2020

Most Recent Documents

Date	Document Description ()	Options
10/07/2020	Issue Notification ()	•••
09/14/2020	Issue Fee Payment (PTO-85B) ()	•••
09/14/2020	Fee Worksheet (SB06) ()	•••

Office Actions

Date	Document Description ()
07/28/2020	Notice of Allowance and Fees Due (PTOL-85) ()
06/09/2020	Final Rejection ()
01/30/2020	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	16691145	1) Han, Kyung Soo	Speed Converter-Controlled River Turbines	12/11/2019	US 15707138 US 14838867 US 16691145 US 16134595 US 16233365 US 62487101 US 15883927 US 62520884 US 62409549 US 62779683 US 15267655	US 20200095974 A1 () US 10941749 B2 ()	03/26/2020 03/09/2021

Most Recent Documents

Date	Document Description ()	Options
02/17/2021	Issue Notification ()	•••
01/26/2021	Specification ()	•••
01/15/2021	Post Allowance Communication - Incoming ()	•••

Office Actions

Date	Document Description ()
11/25/2020	Notice of Allowance and Fees Due (PTOL-85) ()
07/02/2020	Final Rejection ()
02/24/2020	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	16715715	1) HUSHER, Frederick Knute 2) SHUM, Jee Jong	PARAFFIN SHIELD COATING FOR MICROSCOPE SLIDE	12/16/2019	US 62522169 CN 2018091383 US 62520319 US 62520169 CN 2018091685 US 62520341 CN 2018091686 CN 2018091687 US 62520334 US 62520187 US 16715715 US 62520178 US 62539281 CN 2018091689 US 62522187	US 20200192072 A1 ()	06/18/2020

Most Recent Documents

Date	Document Description ()	Options
10/07/2022	Final Rejection ()	•••
10/07/2022	List of references cited by examiner ()	•••
10/07/2022	Search information including classification, databases and other search related notes ()	•••

Office Actions

Date	Document Description ()
10/07/2022	Final Rejection ()
06/15/2022	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	16717118	1) NIPPES, JOSEPH TIMOTHY	LEAD SERVICE WATER PIPE LINE REMOVAL APPARATUS AND METHOD	12/17/2019	US 16121073 US 16717118	US 20200116277 A1 () US 10895332 B2 ()	04/16/2020 01/19/2021

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
EP	19903644	1) Differential Dynamics Corporation,	SCALABLE AND EFFICIENT MECHANICAL SPEED CONVERTER-CONTROLLED WIND AND HYDROKINETIC TURBINES	12/23/2019	US 16691145 US 16233365 US 16701741 US PCT/US19/68418	EP 3853504 A1 () EP 3853504 A4 ()	07/28/2021 11/03/2021

Most Recent Documents

Date	Document Description ()	Options
07/25/2022	Communication of amended entries concerning the representative ()	•••
05/02/2022	Letter accompanying subsequently filed items ()	•••
05/02/2022	Amended claims filed after receipt of (European) search report ()	•••

Office Actions

Date	Document Description ()
10/04/2021	European search opinion ()
07/05/2021	Copy of the international preliminary examination report
07/02/2020	Copy of the international preliminary report on patentab

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	PCT/US19/68418	1) DIFFERENTIAL DYNAMICS CORPORATION, 2) HAN, Kyung Soo,	SCALABLE AND EFFICIENT MECHANICAL SPEED CONVERTER-CONTROLLED WIND AND HYDROKINETIC TURBINES	12/23/2019	US 16701741 US 16691145 US 16233365	WO 2020139863 A1 ()	07/02/2020

Most Recent Documents

Date	Document Description ()	Options
06/28/2021	IP424 ()	•••
06/28/2021	International Preliminary Report on Patentability Chapter II (IPEA/409) ()	•••
06/27/2021	A34AM ()	•••

Office Actions

Date	Document Description ()
06/28/2021	International Preliminary Report on Patentability Chapte (IPEA/409) ()
06/27/2021	International Preliminary Report on Patentability Chapte (IPEA/409)(replaced) ()
07/02/2020	International Search Report ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
JP	2020131831	1) W and W sense Debye seeds and Inc., 2) KOBASHI, Masaaki,	The microstructure enhanced absorption photosensitive device	08/03/2020	US 16528958	JP 2021027358 A ()	02/22/2021

Most Recent Documents

Date	Document Description ()	Options
08/03/2020	Abstract (TRANSLATED) ()	•••
08/03/2020	Abstract (ORIGINAL) ()	•••
08/03/2020	Request for a Patent (TRANSLATED) ()	•••

All Documents | Classification and Citation

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
CN	202010766983	1) Vent and Vassens Devices Inc.,	Microstructure Enhanced Absorption Photosensitive Device	08/03/2020	US 16528958	CN 112582387 A ()	03/30/2021

()	Office ()	Application ()	Applicant	Title ()	App. Date ()	Priority #	Pub. # ()	Pub. Date	A

Most Recent Documents

Date	Document Description ()	Options
08/03/2020	Certified Copy of Priority Document (ORIGINAL) ()	•••

All Documents | Classification and Citation

()	EP	20189156	1) W&WSENS Devices, Inc.,	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	08/03/2020	US 16528958	EP 3772104 A1 ()	02/03/2021

Most Recent Documents

Date	Document Description ()	Options
08/03/2021	Letter accompanying subsequently filed items ()	•••
08/03/2021	Amendments received before examination ()	•••
08/03/2021	Amended claims filed after receipt of (European) search report ()	•••

Office Actions

Date	Document Description ()
12/04/2020	European search opinion ()

All Documents | Classification and Citation | View All Office Actions

()	US	17012426	1) Han, Kyung Soo	VOLTAGE CONVERTER-CONTROLLED DAMLESS HYDROKINETIC RIVER TURBINES	09/04/2020	US 15707138 US 62520884 US 17012426 US 63063522 US 14838867 US 16691145 US 16134595 US 16233365 US 62487101 US 15883927 US 16701741 US 62409549 US 15267655	US 20210180559 A1 () US 11111898 B2 ()	06/17/2021 09/07/2021

Most Recent Documents

Date	Document Description ()	Options
08/18/2021	Issue Notification ()	•••
08/09/2021	Claims ()	•••
08/04/2021	Issue Fee Payment (PTO-85B) ()	•••

Office Actions

Date	Document Description ()
07/16/2021	Notice of Allowance and Fees Due (PTOL-85) ()
07/06/2021	Notice of Allowance and Fees Due (PTOL-85) ()
05/04/2021	Ex Parte Quayle Action ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
EP	20868204	1) W&WSENS Devices, Inc.,	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	09/21/2020	US 63009928 US 63039941 US 63034961 US 62957779 US 63026591 US 63039945 US 62937813 US 63051896 US 63038079 US 63054192 US 62969624 US 62985171 US 62993414 US 62968093 US 63034964 US 62950888 US 62943146 US 63041997 US PCT/US20/51733 US 63016160 US 63019208 US 63050044 US 63011217 US 62978736 US 62905065 US 62981979 US 62925183 US 62975726 US 62964094 US 63033153 US 63048641 US 62914028 US 62994758 US 63043709 US 63005152	EP 4059055 A1 ()	09/21/2022

Most Recent Documents

Date	Document Description ()	Options
08/24/2022	Notification on forthcoming publication of bibliographic data ()	•••
08/03/2022	Communication regarding possible amendment of the application/payment of claims fee ()	•••
07/29/2022	Request for further processing allowed ()	•••

Office Actions

Date	Document Description ()
04/11/2022	Copy of the international preliminary report on patentab

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	17434382	1) WANG, Shih-Yuan 2) Wang, Shih-Ping	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	09/21/2020	US 62905065 US PCT/US20/51733	US 20220149098 A1 ()	05/12/2022

Most Recent Documents

Date	Document Description ()	Options
08/16/2022	Information Disclosure Statement (IDS) Form (SB08) ()	•••
08/16/2022	Foreign Reference ()	•••
08/16/2022	Electronic Filing System(EFS) Acknowledgment Receipt ()	•••

All Documents | Classification and Citation

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	PCT/US20/51733	1) W&WSENS DEVICES INC.,	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	09/21/2020	US 63009928 US 63039941 US 63034961 US 62957779 US 63026591 US 63039945 US 62937813 US 63051896 US 63038079 US 63054192 US 62969624 US 62985171 US 62993414 US 62968093 US 63034964 US 62950888 US 62943146 US 63041997 US 63016160 US 63019208 US 63050044 US 63011217 US 62978736 US 62905065 US 62981979 US 62925183 US 62975726 US 62964094 US 63033153 US 63048641 US 62914028 US 62994758 US 63043709 US 63005152	WO 2021061543 A1 ()	04/01/2021

Most Recent Documents

Date	Document Description ()	Options
03/29/2022	Notification of Transmittal of Copies of International Preliminary Report on Patentability Chapter I ()	•••
03/29/2022	International Preliminary Report on Patentability Chapter I ()	•••
01/18/2022	Notice Informing The Applicant Of The Communication Of The International Application (To Designated Offices Which Do Not Apply The 30 Month Time Limit Under Article 22(1)) ()	•••

Office Actions

Date	Document Description ()
03/29/2022	International Preliminary Report on Patentability Chapte
04/01/2021	International Search Report ()
04/01/2021	Written Opinion of the International Search Authority ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	17182954	1) WANG, Shih-Yuan 2) Wang, Shih-Ping	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	02/23/2021	US PCT/US15/61120 US 15309922 US 15797821 US 17182954 US 16528958	US 20210242354 A1 ()	08/05/2021

Most Recent Documents

Date	Document Description ()	Options
10/21/2022	Information Disclosure Statement (IDS) Form (SB08) ()	•••
10/21/2022	Electronic Filing System(EFS) Acknowledgment Receipt ()	•••
10/21/2022	Transmittal Letter ()	•••

Office Actions

Date	Document Description ()
09/14/2022	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

Samsung Exhibit 1003, Page 95 of 516

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	PCT/US21/50717	1) W&WSENS DEVICES, INC.,	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	09/16/2021	US 63241414 US 17182954 US 63160799 US 63194059 US 63125349 US 63110345 US 63143004 US 63236195 US 63117449 US 63141948 US 63079409 US PCT/US20/51733 US 63223508 US 63136101 US 63157703 US 63174008 US 63218855 US 63083705 US 63116387 US 63161915 US 63192971 US 63154598 US 63175026 US 63090669 US 63167007 US 63104358 US 63228491 US 63208358 US 63128702 US 63172078	WO 2022061016 A1 ()	03/24/2022

Most Recent Documents

Date	Document Description ()	Options
04/12/2022	Notice Informing The Applicant Of The Communication Of The International Application (To Designated Offices Which Do Not Apply The 30 Month Time Limit Under Article 22(1)) ()	•••
03/24/2022	Application Body ()	•••
03/24/2022	Applicant Correspondence ()	•••

Office Actions

Date	Document Description ()
03/24/2022	International Search Report ()
03/24/2022	Written Opinion of the International Search Authority ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	17532831	1) WANG, Shih-Yuan 2) WANG, Shih-Ping	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	11/22/2021	US 17532831 US 14947718 US 15797821 US 17182954 US 16528958	US 20220102563 A1 () US 11309444 B1 ()	03/31/2022 04/19/2022

Most Recent Documents

Date	Document Description ()	Options
10/17/2022	Petition decision routed to the Office of Patent Application Processing(OPAP) to act on the decision or continue prosecution ()	•••
06/13/2022	Request for Certificate of Correction ()	•••
06/13/2022	Transmittal Letter ()	•••

Office Actions

Date	Document Description ()
03/23/2022	Notice of Allowance and Fees Due (PTOL-85) ()
03/04/2022	Notice of Allowance and Fees Due (PTOL-85) ()
02/22/2022	Notice of Allowance and Fees Due (PTOL-85) ()

All Documents | Classification and Citation | View All Office Actions

Office	Application	Applicant	Title	App. Date	Priority #	Pub. #	Pub. Date
US	17707429	1) WANG, Shih-Yuan 2) WANG, Shih-Ping	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	03/29/2022	US 61834873 US 61826446 US 14947718 US 17182954 US 17532831 US 17707429 US 61843021 US 15797821 US PCT/US14/39208 US 61905109 US 16528958	US 20220246775 A1 ()	08/04/2022

()	Office ()	Application ()	Applicant	Title ()	App. Date ()	Priority #	Pub. # ()	Pub. Date

Most Recent Documents

Date	Document Description ()	Options
09/26/2022	Electronic Filing System(EFS) Acknowledgment Receipt ()	•••
09/26/2022	Supplemental Response or Supplemental Amendment ()	•••
09/26/2022	Claims ()	•••

Office Actions

Date	Document Description ()
06/24/2022	Non-Final Rejection ()

All Documents | Classification and Citation | View All Office Actions

(http://www.uspto.gov/)

BROWSE BY TOPIC

ABOUT THIS SITE

USPTO BACKGROUND

FEDERAL GOVERNMENT

Receipt date: 08/16/2022

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17707429
Filing Date	2022-03-29
First Named Inventor	Shih-Yuan WANG
Art Unit	2818
Examiner Name	Tran Quan Hoang Ho
Attorney Docket Number	309-0011USDIVCIP2

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2002314116	JP		2002-10-25	Seiko Epson Corp.		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

Receipt date: 08/16/2022

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17707429
	Filing Date	2022-03-29
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2818
	Examiner Name	Tran Quan Hoang Ho
	Attorney Docket Number	309-0011USDIVCIP2

	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/Hoang-Quan Ho/	Date Considered	10/14/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

139982 7590 11/02/2022

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER	
HO, HOANG QUAN TRAN	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/02/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/707,429	03/29/2022	Shih-Yuan WANG	309-0011USDIVCIP2	1214

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	02/02/2023

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

139982 7590 11/02/2022
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/707,429	03/29/2022	Shih-Yuan WANG	309-0011USDIVCIP2	1214

TITLE OF INVENTION: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$600	$0.00	$0.00	$600	02/02/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
HO, HOANG QUAN TRAN	2818	257-431000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Samsung Exhibit 1003, Page 101 of 516

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/707,429	03/29/2022	Shih-Yuan WANG	309-0011USDIVCIP2	1214

139982 7590 11/02/2022

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER	
HO, HOANG QUAN TRAN	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/02/2022

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/707,429	Applicant(s) WANG et al.	
	Examiner Hoang-Quan Ho	Art Unit 2818	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to reply filed on 09/26/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 31-50 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some* c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 08/16/2022.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/Hoang-Quan Ho/
Primary Examiner, Art Unit 2818

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Response to Amendment

Applicant's amendment to the claims, filed on September 26, 2022, is acknowledged. Amendment is entered.

Response to Arguments/Remarks

Applicant's response filed on September 26, 2022 is acknowledged and is answered as follows.

Applicant's remarks, with respect to claim objections, double patenting, and claim rejections have been fully considered and are persuasive. Therefore, the objections, double patenting, and rejections have been rendered moot.

Allowable Subject Matter

Claims 31 - 50 are allowed.

The following is an examiner's statement of reasons for allowance:

In view of the instant patent application's record of prosecution as a whole, applicant's amendments to the claims, applicant's submitted responses that were found persuasive, and the cited prior art taken singularly or in combination, especially when all limitations were considered within the claimed specific combination, failed to anticipate or render obvious:

- a photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar holes comprising a laterally extending array of pillars with specific structures and characteristics, *inter alia*, as found in claim 31; claims depending on claim 31 inherit the allowance
- a photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar holes comprising an array of pillars with specific structures and characteristics, *inter alia*, as found in claim 40; claims depending on claim 40 inherit the allowance

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Quan Ho whose telephone number is (571)272-8711. The examiner can normally be reached Monday - Friday, 10 AM - 6 PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To

file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hoang-Quan Ho
Primary Patent Examiner
Art Unit 2818

/Hoang-Quan Ho/
Primary Examiner, Art Unit 2818

Electronic Acknowledgement Receipt

EFS ID:	46880411
Application Number:	17707429
International Application Number:	
Confirmation Number:	1214
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	139982
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	309-0011USDIVCIP2
Receipt Date:	24-OCT-2022
Filing Date:	29-MAR-2022
Time Stamp:	16:38:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	309-0011USDIVCIP2_SIDSTransmittal-signed.pdf	474229 c8deea25578f45ae219c5d9209b2ca39b917bf5e	no	1

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	309-0011USDIVCIP2_1449-signed.pdf	1266256 6f70b3cea4b6768d500ca7c1f6ad1f07b95f6985	no	4
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Foreign Reference	KR20080101301.pdf	6748562 12bc15ed7fa89d60be424bac841a39fb41242aaf	no	26
Warnings:					
Information:					
			Total Files Size (in bytes):	8489047	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17707429
Filing Date	2022-03-29
First Named Inventor	Shih-Yuan WANG
Art Unit	2818
Examiner Name	Tran Quan Hoang Ho
Attorney Docket Number	309-0011USDIVCIP2

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	11309444		2022-04-19	Wang et al.	

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20100320444		2010-12-23	Dutta	
	2	20110309331		2011-12-22	Yu et al.	
	3	20180182806		2018-06-28	Jin et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	20080101301	KR		2008-11-21	Dongbu Hitek Co. Ltd.		☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17707429
Filing Date	2022-03-29
First Named Inventor	Shih-Yuan WANG
Art Unit	2818
Examiner Name	Tran Quan Hoang Ho
Attorney Docket Number	309-0011USDIVCIP2

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17707429
	Filing Date	2022-03-29
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2818
	Examiner Name	Tran Quan Hoang Ho
	Attorney Docket Number	309-0011USDIVCIP2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2022-10-24
Name/Print	Ivan S. Kavrukov	Registration Number	25,161

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Shih-Yuan WANG Application No.: 17/707,429 Filed: March 29, 2022 Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	Examiner: Tran Quan Hoang Ho Art Unit: 2818 **CERTIFICATE OF TRANSMISSION** I hereby certify that this correspondence is being submitted through the USPTO Electronic Filing Service addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 /Mary Ellen Finnegan/ Date: October 24, 2022 Name: Mary Ellen Finnegan

VIA EFS-Web
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

TRANSMITTAL OF SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

It is respectfully requested that the documents listed on the attached Supplemental Information Disclosure Citation form PTO/SB/08a be considered by the Patent Examiner in connection with the above-identified application and be made of record therein.

A copy of the non-U.S. patent document is enclosed herewith, in compliance with 37 CFR 1.98.

Independent consideration and acknowledgement of the enclosed document are respectfully requested.

The Commissioner is hereby authorized to charge U.S. PTO Deposit Account 600125 any payment due and to credit any overpayment thereto.

Respectfully submitted,

/Ivan S. Kavrukov/
Ivan S. Kavrukov
Registration No. 25,161
Attorney for Applicant

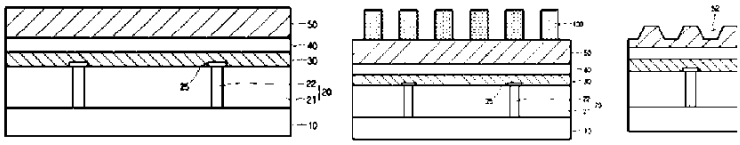
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001
Attorney's Telephone No.: 917-945-0121
Attorney's E-mail: ikavrukov@wissingmiller.com

Image sensor and method for manufacturing thereof

Abstract

An image sensor and a manufacturing method thereof are provided to improve condensing rate and simplify its process while adopting a vertical photodiode of which resolution and sensitivity are improved. A CMOS(Complementary Metal Oxide Silicon) circuit is formed at a semiconductor circuit, and a metallic wiring layer which includes a metal wire and an inter insulation film is formed at a semiconductor substrate. A first conductivity type conductive layer is formed at the metallic wiring layer, and an intrinsic layer is formed at the first conductivity type conductive layer. A second conductivity type conductive layer(51) is formed at the intrinsic layer is formed at the intrinsic layer. At one or more than one layer of those three layers, the first conductivity conductive layer, the intrinsic layer and the second conductivity conductive layer, a concavo-convex part is formed.

Images (14)



KR20080101301A
South Korea

Download PDF Find Prior Art Similar

Other languages: Korean

Inventor: 심천만

Worldwide applications

2007 KR

Application KR1020070047886A events

2007-05-17 Application filed by 주식회사 동부하이텍

2007-05-17 Priority to KR1020070047886A

2008-11-21 Publication of KR20080101301A

Info: Cited by (2), Legal events, Similar documents, Priority and Related Applications

External links: Espacenet, Global Dossier, Discuss

Classifications

- H01L27/14607 Geometry of the photosensitive area

View 4 more classifications

Claims (10)

Hide Dependent
translated from Korean

A semiconductor substrate on which a CMOS circuit is formed; A metal wiring layer including a metal wiring and an interlayer insulating film formed on the semiconductor substrate; A first conductivity type conductive layer formed on the metal wiring layer; An intrinsic layer formed on the first conductivity type conductive layer; And A second conductivity type conductive layer formed on the intrinsic layer, At least one of the first conductive type conductive layer, the intrinsic layer and the second conductive type conductive layer is an image sensor, characterized in that at least one uneven portion is formed on the upper surface. The method of claim 1, At least one trench is formed in any one of the first conductive conductive layer, the intrinsic layer and the second conductive conductive layer formed on the metal wiring. The method of claim 1, And an upper electrode and a color filter array formed on the second conductive conductive layer. The method of claim 1, And an adhesive layer formed between the upper electrode and the

color filter array. The method of claim 4, wherein The adhesive layer is an image sensor, characterized in that formed of a thermal resin. Forming a metal wiring layer including a metal wiring and an interlayer insulating film on the semiconductor substrate on which the CMOS circuit is formed; Forming a first conductivity type conductive layer on the metallization layer; Forming an intrinsic layer on the first conductivity type conductive layer; And Forming a second conductivity type conductive layer on the intrinsic layer, At least one uneven portion is formed on an upper surface of any one of the first conductive conductive layer, the intrinsic layer, and the second conductive conductive layer. The method of claim 6, Forming the uneven portion on the upper surface of any one of the first conductive conductive layer, the intrinsic layer and the second conductive conductive layer formed on the metal wiring, Forming at least one mask pattern on any one of the first conductivity type conductive layer and the intrinsic layer; And forming at least one trench on an upper surface of any one of the first conductive type conductive layer, the intrinsic layer, and the second conductive type conductive layer by using the mask pattern as an etching mask. The method of claim 7, wherein The trench is a method of manufacturing an image sensor, characterized in that formed by a dry etching method or a wet etching method. The method of claim 6, Forming an upper electrode on the second conductive conductive layer; And And forming a color filter array on the upper electrode. The method of claim 1, Forming an adhesive layer formed of a thermal resin on the upper electrode.

Description translated from Korean

Image sensor and method for manufacturing thereof

1 to 5A are diagrams illustrating a manufacturing process of the image sensor of the first embodiment.

6 to 9 are diagrams illustrating a manufacturing process of the image sensor of the second embodiment.

10 to 13 are diagrams illustrating a manufacturing process of the image sensor of the third embodiment.

The embodiment discloses an image sensor and a method of manufacturing the same.

An image sensor is a semiconductor device that converts an optical image into an electrical signal, and is classified into a charge coupled device (CCD) image sensor and a complementary metal oxide silicon (CMOS) image sensor (CIS). do.

CCD image sensor has complex driving method, high power consumption, multi-stage photo process, and manufacturing process has complicated disadvantage. Therefore, as a next generation image sensor to overcome the disadvantage of the charge coupling device, Morse image sensor is attracting attention.

The CMOS image sensor implements an image by sequentially detecting an electrical signal of each unit pixel by a switching method by forming a photodiode and a MOS transistor in the unit pixel.

This CMOS image sensor is simpler to drive than the CCD image sensor, which is widely used as a conventional image sensor, and can realize various scanning methods, and can integrate signal processing onto a single chip, thereby miniaturizing the product. The use of compatible CMOS technology reduces manufacturing costs and lowers power consumption.

The CMOS image sensor according to the related art may be divided into a photo diode region (not shown) that receives a light signal and converts the light signal into an electrical signal, and a transistor region (not shown) that processes the electrical signal.

However, the CMOS image sensor according to the related art has a structure in which a photodiode and a transistor are horizontally disposed on a semiconductor substrate.

Of course, although the disadvantages of the CCD image sensor have been solved by the horizontal CMOS image sensor according to the prior art, there are still problems in the horizontal CMOS image sensor according to the prior art.

That is, according to the horizontal CMOS image sensor according to the prior art, the photodiode and the transistor are formed adjacent to each other horizontally on the substrate. Accordingly, there is a need for an additional area for forming a photodiode, thereby reducing the fill factor area and limiting the possibility of resolution.

In addition, according to the horizontal CMOS image sensor according to the prior art there is a problem that it is very difficult to achieve the optimization for the process of manufacturing the photodiode and transistor at the same time. That is, in a fast transistor process, a shallow junction is required for low sheet resistance, but such a shallow junction may not be suitable for a photodiode.

In addition, according to the horizontal CMOS image sensor according to the prior art, the size of the unit pixel is increased or decreased to maintain the sensor sensitivity of the image sensor as additional on-chip functions are added to the image sensor. Should be.

However, when the pixel size is increased, the resolution of the image sensor is reduced, and the area of the photodiode decreases in the sensor sensitivity of the image sensor.

The embodiment provides an image sensor and a method of manufacturing the same that can provide new integration of transistor circuits and photodiodes.

The present invention also provides an image sensor and a method of manufacturing the same, in which resolution and sensor sensitivity can be improved together.

In addition, to provide an image sensor and a method of manufacturing the same that can achieve a light condensation rate and simplify the process while employing a vertical photodiode.

An image sensor according to an embodiment includes a semiconductor substrate on which a CMOS circuit is formed; A metal wiring layer including a metal wiring and an interlayer insulating film formed on the semiconductor substrate; A first conductivity type conductive layer formed on the metal wiring layer; An intrinsic layer formed on the first conductivity type conductive layer; And a second conductive conductive layer formed on the intrinsic layer, wherein any one of the first conductive conductive layer, the intrinsic layer, and the second conductive conductive layer has at least one uneven portion formed thereon. It includes.

In addition, the manufacturing method of the image sensor according to the embodiment comprises the steps of: forming a metal wiring layer including a metal wiring and an interlayer insulating film on the semiconductor substrate on which the CMOS circuit is formed; Forming a first conductivity type conductive layer on the metallization layer; Forming an intrinsic layer on the first conductivity type conductive layer; And forming a second conductive conductive layer on the intrinsic layer, and forming an uneven portion on an upper surface of any one of the first conductive conductive layer, the intrinsic layer, and the second conductive conductive layer. Steps.

Hereinafter, an image sensor and a method of manufacturing the same according to an embodiment will be described in detail with reference to the accompanying drawings.

In the description of the embodiments, where described as being formed "on / over" of each layer, the on / over may be directly or through another layer (indirectly) includes everything formed.

In the drawings, the thickness or size of each layer is exaggerated, omitted, or schematically illustrated for convenience and clarity of description. In addition, the size of each component does not necessarily reflect the actual size.

In addition, the same code | symbol was used about the same part in description of each Example.

<First Embodiment>

5A is a cross-sectional view of the image sensor according to the first embodiment.

5A, the image sensor of the embodiment includes a semiconductor substrate 10 on which a CMOS circuit is formed; A metal wiring layer 20 including a metal wiring 22 and an interlayer insulating film 21 formed on the semiconductor substrate 10; A first conductivity type conductive layer 30 formed on the metal wiring layer 20; An intrinsic layer 40 formed on the first conductivity type conductive layer 30; And a second conductivity type conductive layer 51 having an uneven portion 53 formed on an upper surface of the intrinsic layer 40.

The lower electrode 25 may be formed on the metal line 22.

An upper electrode 60 and a color filter array 80 may be formed on the second conductive conductive layer 51.

In addition, an adhesive layer 70 may be formed between the upper electrode 60 and the color filter array 80. For example, the adhesive layer 70 is formed of a thermal resin.

A plurality of trenches 52 may be formed in the second conductive conductive layer 51 so that the upper surface of the second conductive conductive layer 51 may have an uneven portion 53 having a plurality of uneven shapes. .

Alternatively, as illustrated in FIG. 5B, one uneven portion 53b may be formed in the second conductive conductive layer 51b connected to the metal wire 22 to form one pixel.

As shown in FIGS. 5A and 5B, the photodiode formed on the metal wire 25 connected to the CMOS circuit (not shown) is formed to have at least one uneven portion.

Therefore, since the photodiode having at least one uneven portion is formed in one pixel including the CMOS circuit and the photodiode, the area of the photodiode can be increased to increase the light sensing efficiency.

An image sensor according to an embodiment may provide vertical integration of a transistor circuit and a photodiode.

In addition, the fill factor can be approached to 100% by vertical integration of the transistor circuit and the photodiode.

In addition, the vertical integration can provide higher sensitivity at the same pixel size than the prior art.

In addition, each unit pixel can implement a more complex circuit without reducing the sensitivity.

In addition, the surface of the photodiode formed in the unit pixel is formed in a dome shape, so that the surface area per unit pixel is increased, so that the light receiving region of the photodiode is enlarged, thereby increasing the light efficiency.

In addition, the surface of the photodiode formed in the unit pixel is formed in the shape of a dome such as a micro lens to maximize the light collecting rate.

In addition, since the photodiode is formed in a shape similar to a lens, a separate microlens forming process may not be performed, thereby simplifying the process.

A method of manufacturing the image sensor of the first embodiment will be described with reference to FIGS. 1 to 5A.

Referring to FIG. 1, a metal wiring layer 20 including a metal wiring 22 and an interlayer insulating film 21 is formed on a semiconductor substrate 10 on which a CMOS circuit (not shown) is formed.

Although not illustrated, an isolation layer (not shown) defining an active region and a field region is formed in the semiconductor substrate 10, and the photoelectric charges received by the photodiodes connected to a photodiode described later to form a unit pixel are used as electrical signals. A CMOS circuit (not shown) may be formed of a transistor structure for changing the circuit into a transistor.

Although not shown, the metal wiring layer 20 may be formed of a plurality of layers to connect the power line or the signal line to the CMOS circuit.

The metal wiring layer 20 is formed of a plurality of metal wirings 22 formed through the interlayer insulating film 21 and the interlayer insulating film 21 on the semiconductor substrate 10.

For example, the interlayer insulating film 21 may be formed of an oxide film, and the metal wire 22 may be formed of various conductive materials including metal, alloy, or silicide, that is, aluminum, copper, cobalt, or tungsten. .

The lower electrode 25 may be formed on the metal wiring layer 20 to be electrically connected to the metal wiring 22. For example, the lower electrode 25 may be formed of metals such as Cr, Ti, TiW, and Ta. Of course, the lower electrode 25 may not be formed.

A metal pixel 22 connected to the CMOS circuit of the semiconductor substrate 10 may be formed on the interlayer insulating layer 21, and then a photodiode may be formed on the metal wiring layer 20 to form a unit pixel.

The photodiode is formed on the metal wiring layer 220 to receive and receive light incident from the outside to convert and store in an electrical form. In this embodiment, a pin diode is used.

The pin diode is formed of a structure in which an n-type amorphous silicon layer, an intrinsic amorphous silicon layer, and a p-type amorphous silicon layer are bonded to each other. The performance of the photodiode is determined by the efficiency of converting it into electrical form by receiving external light and the total charge capacitance. The existing photodiode is depleted when heterojunction of PN, NP, NPN, PNP, etc. Although the charge is generated and stored in the region, the fin diode is a photodiode having a structure in which an intrinsic amorphous silicon layer, which is a pure semiconductor, is bonded between a p-type silicon layer and an n-type silicon layer. All of the intrinsic amorphous silicon layers formed therebetween become depletion regions, which is advantageous for generation and storage of charges.

As described above, in the exemplary embodiment, a pin diode is used as the photodiode, and the pin diode may have a structure of P-I-N or N-I-P. Particularly, in the embodiment, a pin structure having a PIN structure is used as an example, and the n-type amorphous silicon layer includes a first conductive type conductive layer 30 and the intrinsic amorphous silicon layer. In this case, the intrinsic layer 40 and the p-type amorphous silicon layer are referred to as a second conductivity type conductive layer 50.

A method of forming the photodiode using the pin diode will be described below.

A first conductivity type conductive layer 30 is formed on the metal wiring layer 20. The first conductivity type conductive layer 30 may serve as the N layer of the P-I-N diode employed in the present embodiment. That is, the first conductivity type conductive layer 30 may be an N type conductivity type conductive layer, but is not limited thereto.

The first conductivity type conductive layer 30 may be formed using n-doped amorphous silicon doped with N-type impurities, but is not limited thereto.

That is, the first conductivity type conductive layer 30 is a-Si: H, a-SiGe: H, a-SiC, a-SiN: H a- by adding germanium, carbon, nitrogen or oxygen to amorphous silicon. SiO: H or the like.

In addition, the first conductivity type conductive layer 30 may be formed by chemical vapor deposition (CVD), in particular, PECVD. For example, the first conductive conductive layer 30 may be formed of amorphous silicon by PECVD by mixing PH_3, P_2H_5, and the like with silane gas (SiH_4).

Next, an intrinsic layer 40 is formed on the first conductivity type conductive layer 30. The intrinsic layer 40 may serve as an I layer employed in the embodiment.

The intrinsic layer 40 may be formed using intrinsic amorphous silicon. The intrinsic layer 40 may be formed by chemical vapor deposition (CVD), in particular, PECVD. For example, the intrinsic layer 40 may be formed of amorphous silicon by PECVD using silane gas (SiH_4).

In addition, the intrinsic layer 40 is preferably formed to a thickness of about 10 to 1,000 times the thickness of the first conductive type conductive layer 30. This is because the thicker the intrinsic layer 40 is, the more the depletion region of the photodiode increases, which is advantageous for storing and generating a large amount of photocharges.

Next, a second conductivity type conductive layer 50 is formed on the intrinsic layer 40.

The second conductivity type conductive layer 50 may serve as a P layer of the P-I-N diode employed in the embodiment. That is, the second conductivity type conductive layer 50 may be a P type conductivity type conductive layer, but is not limited thereto.

For example, the second conductivity type conductive layer 50 may be formed using P-doped amorphous silicon, but is not limited thereto.

The second conductivity type conductive layer 50 may be formed by chemical vapor deposition (CVD), in particular, PECVD. For example, the second conductivity type conductive layer 50 may be formed of amorphous silicon by PECVD by mixing a gas such as BH_3 or B_2H_6 with silane gas (SiH_4).

As described above, since the circuit region formed on the semiconductor substrate 10 and the photodiode are vertically formed, the fill factor of the photodiode may approach 100%.

Referring to FIG. 2, a mask pattern 100 is formed on the second conductive conductive layer 50.

The mask pattern 100 is to form the second conductive conductive layer 50 in the form of irregularities. The mask pattern 100 is formed by applying and patterning a photoresist film.

At least one mask pattern 100 may be formed on the second conductive conductive layer 50 so that the upper surface of the second conductive conductive layer 50 has a step difference.

Referring to FIG. 3, the trench 52 is formed by etching the second conductive conductive layer 50 using the mask pattern 100 as an etch mask. Then, the concave-convex portion 53 of the concave-convex shape is formed on the upper surface of the second conductivity type conductive layer 51 by the trench 52.

The second conductive conductive layer 51 may be etched by a dry or wet etching process. In particular, the etching of the second conductivity type conductive layer 51 proceeds so that the intrinsic layer 40 under the second conductivity type conductive layer 51 is not exposed.

As described above, since the uneven portion 53 is formed on the upper surface of the second conductive conductive layer 51, the surface area of the second conductive conductive layer 51 is increased, and thus the light receiving area of the photodiode is increased. This can be extended to improve the light detection rate of the image sensor.

In addition, at least one convex dome-shaped lens is formed in one pixel by the concave-convex portion 53 of the second conductivity type conductive layer 51 to increase the light efficiency of the photodiode.

Referring to FIG. 4, the upper electrode 60 is formed on the second conductive type conductive layer 51 on which the uneven portion 52 is formed.

The upper electrode 60 may be formed of a transparent electrode having good light transmittance and high conductivity. For example, the upper electrode 60 may be formed of indium tin oxide (ITO) or cardium tin oxide (CTO).

By the shape of the uneven portion 53, the upper electrode 60 may also be formed in the uneven shape having a step.

Referring to FIG. 5A, an adhesive layer 70 and a color filter 80 are formed on the upper electrode 60.

The adhesive layer 70 is to improve the adhesion between the upper electrode 60 and the color filter 80. The adhesive layer 70 is formed by depositing a thermal resin on the upper electrode 60 and then performing a planarization process. To form.

In addition, a color filter 80 is formed on the adhesive layer 70.

In the image sensor formed as described above, photodiodes having a plurality of dome shapes may be formed in one pixel, thereby improving light condensation.

Alternatively, as illustrated in FIG. 5B, one uneven portion 53b may be formed in the second conductive conductive layer 51b formed on the metal wiring 22.

As a result, the light receiving area is extended by the uneven shape of the photodiode, thereby increasing the photosensitive index.

Second Embodiment

9 is a sectional view of an image sensor according to a second embodiment.

The image sensor of the embodiment with reference to FIG. 9 includes: a semiconductor substrate 10 on which a CMOS circuit is formed; A metal wiring layer 20 including a plurality of metal wirings 22 and an interlayer insulating film 21 formed on the semiconductor substrate 10; A first conductivity type conductive layer 31 having at least one uneven portion 33 formed on an upper surface of the metal wiring layer 20; An intrinsic layer 40 formed on the first conductivity type conductive layer 31; And a second conductivity type conductive layer 50 formed on the intrinsic layer 40.

At least one trench 32 may be formed in the first conductive conductive layer 31 so that one or more uneven portions 33 may be formed on an upper surface of the first conductive conductive layer 31.

The lower electrode 25 may be formed on the metal line 22.

An upper electrode 60 and a color filter array 80 may be formed on the second conductive conductive layer 50.

In addition, an adhesive layer 70 may be formed between the upper electrode 60 and the color filter array 80. For example, the adhesive layer 70 is formed of a thermal resin.

A manufacturing process of the image sensor of the second embodiment will be described with reference to FIGS. 6 to 9.

Referring to FIG. 6, a metal wiring layer 20 and a lower electrode 25 are formed on the semiconductor substrate 10.

Since the semiconductor substrate 10, the metallization layer 20, and the lower electrode 25 are the same as in the above-described first embodiment, description thereof will be omitted.

After forming the metal wiring 22 connected to the CMOS circuit of the semiconductor substrate 10 on the interlayer insulating film 21, a photodiode is formed on the metal wiring layer 20.

The photodiode is formed on the metal wiring layer 220 to receive and receive light incident from the outside to convert and store in an electrical form. In this embodiment, a pin diode is used. Since the photodiode used in the second embodiment is the same as the first embodiment, a detailed description thereof will be omitted and only the process sequence will be described.

A method of forming the photodiode using the pin diode will be described below.

After forming the first conductive conductive layer 30 on the metal wiring layer 20, at least one mask pattern 100 is formed on the first conductive conductive layer 30.

The mask pattern 100 is for forming the first conductivity type conductive layer 30 in the form of irregularities. The mask pattern 100 is formed by coating and patterning a photoresist film. At least one mask pattern 100 may be formed on the first conductivity type conductive layer 30 so that the upper surface of the first conductivity type conductive layer 30 has a step difference.

Referring to FIG. 7, the trench 32 is formed by etching the first conductive conductive layer 30 using the mask pattern 100 as an etch mask. Then, the concave-convex portion 33 having the concave-convex shape is formed on the upper surface of the first conductivity type conductive layer 31 by the trench 32.

The first conductive conductive layer 31 may be etched by a dry or wet etching process. In particular, the etching of the first conductivity type conductive layer 31 proceeds so that the metal wiring layer 20 positioned under the first conductivity type conductive layer 31 is not exposed.

Referring to FIG. 8, an intrinsic layer 40 and a second conductive conductive layer 50 are sequentially formed on the first conductive conductive layer 30.

Then, the intrinsic layer 40 formed along the upper surface of the first conductivity type conductive layer 31 has a stepped upper surface by the uneven portion 33 of the first conductivity type conductive layer 31. The second conductive conductive layer 50 has a stepped upper surface by the intrinsic layer 40.

Therefore, the surface of the photodiode including the first conductive conductive layer 31, the intrinsic layer 40, and the second conductive conductive layer 50 is formed in an uneven shape to improve the light sensing rate due to the increase of the surface area. It becomes possible.

In addition, since the photodiode has a shape such as a convex lens, it is possible to improve the light collecting rate.

In addition, the photodiode may have at least one uneven portion per pixel to increase the light detection rate of the photodiode.

Referring to FIG. 9, an upper electrode 60 is formed on the second conductive conductive layer 50.

The upper electrode 60 may be formed of a transparent electrode having good light transmittance and high conductivity. For example, the upper electrode 60 may be formed of indium tin oxide (ITO) or cardium tin oxide (CTO).

The adhesive layer 70 and the color filter 80 are formed on the upper electrode 60.

The adhesive layer 70 is to improve the adhesion between the upper electrode 60 and the color filter 80. The adhesive layer 70 is formed by depositing a thermal resin on the upper electrode 60 and then performing a planarization process. To form.

In addition, a color filter 80 is formed on the adhesive layer 70.

Third Embodiment

13 is a sectional view of an image sensor according to a third embodiment.

The image sensor of the embodiment with reference to FIG. 13 includes a semiconductor substrate 10 having a CMOS circuit formed thereon; A metal wiring layer 20 including a plurality of metal wirings 22 and an interlayer insulating film 21 formed on the semiconductor substrate 10; A first conductivity type conductive layer 30 formed on the metal wiring layer 20; An intrinsic layer 41 having at least one uneven portion 43 formed on an upper surface of the first conductive conductive layer 30; And a second conductivity type conductive layer 50 formed on the intrinsic layer 41.

At least one trench 42 may be formed in the intrinsic layer 41, and at least one uneven portion 43 may be formed on an upper surface of the intrinsic layer 41.

The lower electrode 25 may be formed on the metal line 22.

An upper electrode 60 and a color filter array 80 may be formed on the second conductive conductive layer 50.

In addition, an adhesive layer 70 may be formed between the upper electrode 60 and the color filter array 80. For example, the adhesive layer 70 is formed of a thermal resin.

A manufacturing process of the image sensor of the second embodiment will be described with reference to FIGS. 10 to 13.

Referring to FIG. 10, a metal wiring layer 20 and a lower electrode 25 are formed on the semiconductor substrate 10.

Since the semiconductor substrate 10, the metallization layer 20, and the lower electrode 25 are the same as those of the first embodiment described above, description thereof will be omitted.

After forming the metal wiring 22 connected to the CMOS circuit of the semiconductor substrate 10 on the interlayer insulating film 21, a photodiode is formed on the metal wiring layer 20.

The photodiode is formed on the metal wiring layer 220 to receive and receive light incident from the outside to convert and store in an electrical form. In this embodiment, a pin diode is used. Since the photodiode used in the second embodiment is the same as the first embodiment, a detailed description thereof will be omitted and only the process sequence will be described.

A method of forming the photodiode using the pin diode will be described below.

The first conductivity type conductive layer 30 and the intrinsic layer 40 are sequentially formed on the metal wiring layer 20.

The mask pattern 100 is formed on the intrinsic layer 40.

The mask pattern 100 is for forming the intrinsic layer 40 in the form of irregularities. The mask pattern 100 is formed by applying and patterning a photoresist film. At least one mask pattern 100 may be formed on the intrinsic layer 40 so that the upper surface of the intrinsic layer 41 has a step.

Referring to FIG. 11, the trench 42 is formed by etching the intrinsic layer 40 using the mask pattern 100 as an etch mask. Then, the uneven portions 43 having the uneven shape are formed on the upper surface of the intrinsic layer 41 by the trench 42.

The intrinsic layer 41 may be etched by a dry or wet etching process. In particular, the etching of the intrinsic layer 41 proceeds so that the first conductivity type conductive layer 30 positioned below the intrinsic layer 41 is not exposed.

Referring to FIG. 12, a second conductivity type conductive layer 50 is formed on the intrinsic layer 41.

Then, in the second conductive type conductive layer 50 formed along the upper surface of the intrinsic layer 41, the upper surface is stepped by the uneven portion 43 of the intrinsic layer 41.

Therefore, the surface of the photodiode including the first conductive conductive layer 30, the intrinsic layer 41, and the second conductive conductive layer 50 is formed in an uneven shape to improve the light sensing rate due to the increase of the surface area. It becomes possible.

In addition, since the photodiode has a shape such as a convex lens, it is possible to improve the light collecting rate.

Referring to FIG. 9, an upper electrode 60 is formed on the second conductive conductive layer 50.

The upper electrode 60 may be formed of a transparent electrode having good light transmittance and high conductivity. For example, the upper electrode 60 may be formed of indium tin oxide (ITO) or cardium tin oxide (CTO).

The adhesive layer 70 and the color filter 80 are formed on the upper electrode 60.

The adhesive layer 70 is to improve the adhesion between the upper electrode 60 and the color filter 80. The adhesive layer 70 is formed by depositing a thermal resin on the upper electrode 60 and then performing a planarization process. To form.

In addition, a color filter 80 is formed on the adhesive layer 70.

The embodiments described above are not limited to the above-described embodiments and drawings, and it is to be understood that various changes, modifications, and changes can be made without departing from the technical spirit of the present embodiments. It will be obvious to those who have it.

According to the image sensor and the manufacturing method thereof according to the embodiment, it is possible to provide vertical integration of the transistor circuit and the photodiode.

In addition, the fill factor can be approached to 100% by vertical integration of the transistor circuit and the photodiode.

In addition, the vertical integration can provide higher sensitivity at the same pixel size than the prior art.

In addition, each unit pixel can implement a more complex circuit without reducing the sensitivity.

In addition, by adopting a vertical photodiode, insulation between unit pixels is secured, thereby preventing crosstalk between pixels and the like, thereby improving reliability of the image sensor.

In addition, in implementing the unit pixel of the photodiode, the light sensing ratio may be improved by increasing the surface area of the photodiode in the unit pixel.

In addition, the photodiode corresponding to the unit pixel may have a lens shape such as a convex lens, thereby improving the light condensing ratio.

Cited By (2)

Publication number	Priority date	Publication date	Assignee	Title
CN109728127A *	2017-10-30	2019-05-07	上海箩箕技术有限公司	Photodiode and forming method thereof, imaging sensor, fingerprint imaging mould group
US20210242354A1 *	2015-11-17	2021-08-05	W&Wsens Devices, Inc.	Microstructure enhanced absorption photosensitive devices

Family To Family Citations

* Cited by examiner, † Cited by third party, ‡ Family to family citation

Similar Documents

Publication	Publication Date	Title
KR100851756B1	2008-08-11	Image sensor and method for manufacturing therof
KR100894391B1	2009-04-20	Image Sensor and Method for Manufacturing Thereof
KR100935771B1	2010-01-06	Image Sensor and Method for Manufacturing Thereof
KR100872719B1	2008-12-05	Image Sensor and Method for Manufacturing thereof
KR100913019B1	2009-08-20	Image Sensor and Method for Manufacturing Thereof
KR100868651B1	2008-11-12	Image sensor and method for manufacturing thereof
US7968366B2	2011-06-28	Image sensor and method for manufacturing the same
KR100881276B1	2009-02-05	Image sensor and method for manufacturing thereof
KR100837556B1	2008-06-12	Image sensor and method for manufacturing thereof
KR100866255B1	2008-10-30	Image sensor and method for manufacturing thereof
KR100872990B1	2008-12-08	Image Sensor and Method for Fabrication of the Same
KR100851758B1	2008-08-11	Image sensor and method for manufacturing thereof
KR100871973B1	2008-12-08	Image Sensor and Method for Manufacturing thereof
KR100884204B1	2009-02-18	Image Sensor and Method for Manufacturing thereof
KR100997312B1	2010-11-29	Image Sensor and Method for Manufactruingg thereof
KR20080101301A	2008-11-21	Image sensor and method for manufacturing thereof
KR100924412B1	2009-10-29	Image Sensor and Method for Manufacturing Thereof
KR100935768B1	2010-01-06	Method for Manufacturing of Image Sensor
KR20090044117A	2009-05-07	Image sensor and method for manufacturing thereof

Priority And Related Applications

Priority Applications (1)

Application	Priority date	Filing date	Title
KR1020070047886A	2007-05-17	2007-05-17	Image sensor and method for manufacturing thereof

Applications Claiming Priority (1)

Application	Filing date	Title
KR1020070047886A	2007-05-17	Image sensor and method for manufacturing thereof

Legal Events

Date	Code	Title	Description
2007-05-17	A201	Request for examination	
2008-04-15	E902	Notification of reason for refusal	
2008-10-20	E601	Decision to refuse application	

Concepts

machine-extracted

Download Filter table

Name	Image	Sections	Count	Query match
manufacturing process		title,claims,abstract,description	20	0.000
metal		claims,abstract,description	53	0.000
metal		claims,abstract,description	53	0.000
semiconductor		claims,abstract,description	28	0.000
substrate		claims,abstract,description	26	0.000
layer		claims,description	228	0.000
adhesive		claims,description	21	0.000
adhesive		claims,description	21	0.000
interlayer		claims,description	14	0.000

resin	claims,description	8	0.000
resin	claims,description	8	0.000
etching	claims,description	7	0.000
dry etching	claims,description	4	0.000
metallisation	claims,description	4	0.000
wet etching	claims,description	4	0.000
method	abstract,description	16	0.000
sensitivity	abstract,description	8	0.000
silicon	abstract,description	4	0.000
silicon	abstract,description	4	0.000
complement	abstract,description	2	0.000
insulation	abstract,description	2	0.000
metal oxide	abstract,description	2	0.000
metal oxides	abstract,description	2	0.000

Show all concepts from the description section

Data provided by IFI CLAIMS Patent Services

About Send Feedback Public Datasets Terms Privacy Policy

(19) 대한민국특허청(KR)
(12) 공개특허공보(A)

(11) 공개번호 10-2008-0101301
(43) 공개일자 2008년11월21일

(51) Int. Cl.
H01L 27/146 (2006.01)
(21) 출원번호 10-2007-0047886
(22) 출원일자 2007년05월17일
심사청구일자 2007년05월17일

(71) 출원인
주식회사 동부하이텍
서울특별시 강남구 대치동 891-10
(72) 발명자
심천만
서울 영등포구 신길7동 1967
(74) 대리인
허용록

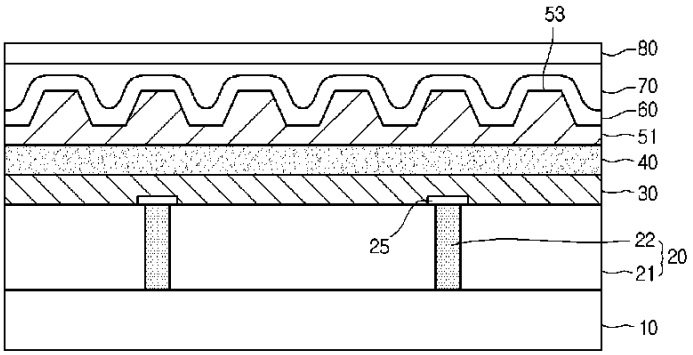
전체 청구항 수 : 총 10 항

(54) 이미지 센서 및 그의 제조방법

(57) 요 약

실시예는 이미지 센서에 관한 것으로, 씨모스 회로가 형성된 반도체 기판; 상기 반도체 기판 상에 형성된 금속배선 및 층간절연막을 포함하는 금속배선층; 상기 금속배선층 상에 형성된 제1 도전형 전도층; 상기 제1 도전형 전도층 상에 형성된 진성층; 및 상기 진성층 상에 상부 표면에 적어도 하나 이상의 요철부가 형성된 제2 도전형 전도층을 포함한다.

대 표 도 - 도5a



Samsung Exhibit 1003, Page 127 of 516

특허청구의 범위

청구항 1

씨모스 회로가 형성된 반도체 기판;

상기 반도체 기판 상에 형성된 금속배선 및 층간절연막을 포함하는 금속배선층;

상기 금속배선층 상에 형성된 제1 도전형 전도층;

상기 제1 도전형 전도층 상에 형성된 진성층; 및

상기 진성층 상에 형성된 제2 도전형 전도층을 포함하며,

상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층은 그 상부 표면에 적어도 하나 이상의 요철부가 형성된 것을 특징으로 하는 이미지 센서.

청구항 2

제1항에 있어서,

상기 금속배선 상에 형성된 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층에는 적어도 하나 이상의 트렌치가 형성된 것을 포함하는 이미지 센서.

청구항 3

제1항에 있어서,

상기 제2 도전형 전도층 상부에는 상부전극 및 컬러필터 어레이가 형성된 것을 포함하는 이미지 센서.

청구항 4

제1항에 있어서,

상기 상부전극과 컬러필터 어레이 사이에는 접착층이 형성된 것을 포함하는 이미지 센서.

청구항 5

제4항에 있어서,

상기 접착층은 열 수지로 형성된 것을 특징으로 하는 이미지 센서.

청구항 6

씨모스 회로가 형성된 반도체 기판 상에 금속배선 및 층간절연막을 포함하는 금속배선층을 형성하는 단계;

상기 금속배선층 상에 제1 도전형 전도층을 형성하는 단계;

상기 제1 도전형 전도층 상에 진성층을 형성하는 단계; 및

상기 진성층 상에 제2 도전형 전도층을 형성하는 단계를 포함하며,

상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층의 상부 표면에는 적어도 하나 이상의 요철부가 형성되는 단계를 포함하는 이미지 센서의 제조방법.

청구항 7

제6항에 있어서,

상기 금속배선 상에 형성된 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층의 상부표면에 요철부를 형성하는 단계는,

상기 제1 도전형 전도층, 진성층 중 어느 하나의 층 상에 적어도 하나 이상의 마스크 패턴을 형성하는 단계;

상기 마스크 패턴을 식각 마스크로 하여 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의

Samsung Exhibit 1003, Page 128 of 516

층 상부 표면에 적어도 하나 이상의 트렌치를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 8

제7항에 있어서,

상기 트렌치는 건식식각 또는 습식식각 방법으로 형성된 것을 특징으로 하는 이미지 센서의 제조방법.

청구항 9

제6항에 있어서,

상기 제2 도전형 전도층 상에 상부전극을 형성하는 단계; 및

상기 상부전극 상에 컬러필터 어레이를 형성하는 단계를 포함하는 이미지 센서의 제조방법.

청구항 10

제1항에 있어서,

상기 상부전극 상에 열 수지로 형성된 접착층을 형성하는 단계를 포함하는 이미지 센서의 제조방법.

명 세 서

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

<4> 실시예는 이미지 센서 및 그의 제조방법을 개시한다.

<5> 이미지 센서는 광학적 영상(Optical Image)을 전기 신호로 변환시키는 반도체 소자로서, 크게 전하결합소자(charge coupled device:CCD) 이미지 센서와 씨모스(Complementary Metal Oxide Silicon:CMOS) 이미지 센서(CIS)로 구분된다.

<6> CCD 이미지 센서는 구동방식이 복잡하고, 전력소비가 클 뿐만 아니라, 다단계의 포토공정이 요구되므로 제조공정이 복잡한 단점을 갖고 있으므로, 최근에는 상기 전하결합소자의 단점을 극복하기 위한 차세대 이미지 센서로서 씨모스 이미지 센서가 주목을 받고 있다.

<7> 씨모스 이미지 센서는 단위 화소 내에 포토다이오드와 모스트랜지스터를 형성시킴으로써 스위칭 방식으로 각 단위 화소의 전기적 신호를 순차적으로 검출하여 영상을 구현한다.

<8> 이러한 씨모스 이미지 센서는 종래 이미지 센서로 널리 사용되고 있는 CCD 이미지 센서에 비하여 구동방식이 간편하고 다양한 스캐닝 방식의 구현이 가능하며, 신호처리를 단일칩에 집적할 수 있어 제품의 소형화가 가능할 뿐만 아니라, 호환성의 씨모스 기술을 사용하므로 제조단가를 낮출 수 있고,전력 소모 또한 낮다는 장점을 지니고 있다.

<9> 종래기술에 의한 씨모스 이미지 센서는 빛 신호를 받아서 전기신호로 바꾸어 주는 포토다이오드(Photo diode) 영역(미도시)과 이 전기 신호를 처리하는 트랜지스터 영역(미도시)으로 구분할 수 있다.

<10> 그런데 종래기술에 따른 씨모스 이미지 센서는 포토다이오드와 트랜지스터가 반도체 기판에 수평으로 배치되는 구조이다.

<11> 물론, 종래기술에 의한 수평형 씨모스 이미지 센서에 의해 CCD 이미지 센서의 단점이 해결되기는 하였으나, 종래기술에 의한 수평형 씨모스 이미지 센서에는 여전히 문제점들이 있다.

<12> 즉, 종래기술에 의한 수평형 씨모스 이미지 센서에 의하면 포토다이오드와 트랜지스터가 기판 상에 상호 수평으로 인접하여 형성된다. 이에 따라, 포토다이오드 형성을 위한 추가적인 영역이 요구되며, 이에 의해 필 팩터(fill factor) 영역을 감소시키고 레졸루션(Resolution)의 가능성을 제한하는 문제가 있다.

<13> 또한, 종래기술에 의한 수평형 씨모스 이미지 센서에 의하면 포토다이오드와 트랜지스터를 동시에 제조하는 공

Samsung Exhibit 1003, Page 129 of 516

정에 대한 최적화를 달성하는 점이 매우 어려운 문제가 있다. 즉, 신속한 트랜지스터 공정에서는 작은 면저항(low sheet resistance)을 위해 샐로우 정션(shllow junction)이 요구되나, 포토다이오드에는 이러한 샐로우 정션(shllow junction)이 적절하지 않을 수 있다.

<14> 또한, 종래기술에 의한 수평형 씨모스 이미지 센서에 의하면 추가적인 온칩(on-chip) 기능들이 이미지 센서에 부가되면서 단위화소의 크기가 이미지 센서의 센서티버티(sensitivity)를 유지하기 위해 증가되거나 또는 감소되어야 한다.

<15> 그런데, 픽셀사이즈가 증가되면 이미지 센서의 레졸루션(Resolution)이 감소하게 되며, 또한 포토다이오드의 면적이 이미지 센서의 센서티버티(sensitivity)가 감소하는 문제가 발생한다.

발명이 이루고자 하는 기술적 과제

<16> 실시예는 트랜지스터 회로와 포토다이오드의 새로운 집적을 제공할 수 있는 이미지 센서 및 그의 제조방법을 제공한다.

<17> 또한, 레졸루션(Resolution)과 센서티버티(sensitivity)가 함께 개선될 수 있는 이미지 센서 및 그의 제조방법을 제공한다.

<18> 또한, 수직형의 포토다이오드를 채용하면서 집광률 향상과 동시에 공정 단순화를 이룰 수 있는 이미지 센서 및 그의 제조방법을 제공하고자 한다.

발명의 구성 및 작용

<19> 실시예에 따른 이미지 센서는, 씨모스 회로가 형성된 반도체 기판; 상기 반도체 기판 상에 형성된 금속배선 및 층간절연막을 포함하는 금속배선층; 상기 금속배선층 상에 형성된 제1 도전형 전도층; 상기 제1 도전형 전도층 상에 형성된 진성층; 및 상기 진성층 상에 형성된 제2 도전형 전도층을 포함하고, 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층은 그 상부 표면에 적어도 하나 이상의 요철부가 형성된 것을 포함한다.

<20> 또한, 실시예에 따른 이미지 센서의 제조방법은, 씨모스 회로가 형성된 반도체 기판 상에 금속배선 및 층간절연막을 포함하는 금속배선층을 형성하는 단계; 상기 금속배선층 상에 제1 도전형 전도층을 형성하는 단계; 상기 제1 도전형 전도층 상에 진성층을 형성하는 단계; 및 상기 진성층 상에 제2 도전형 전도층을 형성하는 단계를 포함하며, 상기 제1 도전형 전도층, 진성층 및 제2 도전형 전도층 중 어느 하나의 층의 상부 표면에 요철부를 형성하는 단계를 포함한다.

<21> 이하, 실시예에 따른 이미지 센서 및 그의 제조방법을 첨부된 도면을 참조하여 상세히 설명한다.

<22> 실시예의 설명에 있어서, 각 층의 "상/위(on/over)"에 형성되는 것으로 기재되는 경우에 있어, 상/위(on/over)는 직접(directly)와 또는 다른 층을 개재하여(indirectly) 형성되는 것을 모두 포함한다.

<23> 도면에서 각층의 두께나 크기는 설명의 편의 및 명확성을 위하여 과장되거나 생략되거나 또는 개략적으로 도시되었다. 또한 각 구성요소의 크기는 실제크기를 전적으로 반영하는 것은 아니다.

<24> 또한, 각 실시예의 설명에 있어서 동일한 부분에 대하여 동일한 부호를 사용하였다.

<25> <제1 실시예>

<26> 도 5a는 제1 실시예에 따른 이미지 센서의 단면도이다.

<27> 도 5a를 참조하여, 실시예의 이미지 센서는, 씨모스 회로가 형성된 반도체 기판(10); 상기 반도체 기판(10) 상에 형성된 금속배선(22) 및 층간절연막(21)을 포함하는 금속배선층(20); 상기 금속배선층(20) 상에 형성된 제1 도전형 전도층(30); 상기 제1 도전형 전도층(30) 상에 형성된 진성층(40); 및 상기 진성층(40) 상에 상부표면에 요철부(53)가 형성된 제2 도전형 전도층(51)을 포함한다.

<28> 상기 금속배선(22) 상부에는 하부전극(25)이 형성될 수 있다.

<29> 상기 제2 도전형 전도층(51) 상부에는 상부전극(60) 및 컬러필터 어레이(80)가 형성될 수 있다.

<30> 또한, 상기 상부전극(60)과 컬러필터 어레이(80) 사이에는 접착층(70)이 형성될 수 있다. 예를 들어 상기 접착층(70)은 열 수지(thermal resin)로 형성된다.

Samsung Exhibit 1003, Page 130 of 516

<31> 상기 제2 도전형 전도층(51)에는 복수개의 트렌치(52)가 형성되어 상기 제2 도전형 전도층(51)의 상부표면은 복수개의 요철형상을 갖는 요철부(53)가 형성될 수 있다.

<32> 또는, 도 5b에 도시된 바와 같이 상기 금속배선(22)과 연결되어 하나의 픽셀을 이루는 상기 제2 도전형 전도층(51b)에는 하나의 요철부(53b)가 형성될 수 있다.

<33> 도 5a 및 도 5b에 도시된 바와 같이, 씨모스 회로(미도시)와 연결되는 금속배선(25) 상에 형성된 포토다이오드가 적어도 하나 이상의 요철부를 가지도록 형성된다.

<34> 따라서, 씨모스 회로와 포토다이오드로 이루어지는 하나의 픽셀에 적어도 하나 이상의 요철부를 갖는 포토다이오드가 형성되므로써 상기 포토다이오드의 면적이 증가되어 광감지 효율을 증가시킬 수 있다.

<35> 실시예에 따른 이미지 센서는 트랜지스터 회로와 포토다이오드의 수직형 집적을 제공할 수 있다.

<36> 또한, 트랜지스터 회로와 포토다이오드의 수직형 집적에 의해 필 팩터(fill factor)를 100%에 근접시킬 수 있다.

<37> 또한, 수직형 집적에 의해 종래기술보다 같은 픽셀 사이즈에서 높은 센서티비티(sensitivity)를 제공할 수 있다.

<38> 또한, 각 단위 픽셀은 센서티비티(sentivity)의 감소없이 보다 복잡한 회로를 구현할 수 있다.

<39> 또한, 단위 픽셀 내에 형성된 포토다이오드의 표면이 돔 형태로 형성되어 단위 픽셀 당 표면적이 증가하여 포토다이오드의 수광영역이 확대되어 광효율을 증가시킬 수 있다.

<40> 또한, 단위 픽셀 내에 형성된 포토다이오드의 표면이 마이크로렌즈와 같은 돔형태로 형성되어 집광율을 극대화시킬 수 있다.

<41> 또한, 상기 포토다이오드의 형태가 렌즈와 유사한 형태로 형성되어 별도의 마이크로렌즈 형성공정을 진행하지 않아도 되므로 공정을 단순화 시킬 수 있다.

<42> 도 1 내지 도 5a를 참조하여 제1 실시예의 이미지 센서의 제조방법을 설명한다.

<43> 도 1을 참조하여, 씨모스 회로(미도시)가 형성된 반도체 기판(10) 상에는 금속배선(22) 및 층간절연막(21)을 포함하는 금속배선층(20)이 형성되어 있다.

<44> 도시하지는 않았지만, 상기 반도체 기판(10)에는 액티브 영역 및 필드 영역을 정의하는 소자분리막(미도시)이 형성되어 있으며, 단위 픽셀을 형성하기 위해 후술되는 포토다이오드에 연결되어 수광된 광전하를 전기신호로 변화시키기 위한 트랜지스터 구조물로 이루어진 씨모스 회로(미도시)가 형성되어 있을 수 있다.

<45> 도시하지는 않았지만, 상기 금속배선층(20)은 전원라인 또는 신호라인과 씨모스 회로를 접속시키기 위해 복수의 층으로 형성될 수 있다.

<46> 상기 금속배선층(20)은 반도체 기판(10) 상에 층간절연막(21)과 상기 층간절연막(21)을 관통하여 형성되는 복수의 금속배선(22)으로 형성되어 있다.

<47> 예를 들어, 상기 층간절연막(21)은 산화막으로 형성될 수 있으며, 상기 금속배선(22)은 금속, 합금 또는 실리사이드를 포함한 다양한 전도성 물질, 즉 알루미늄, 구리, 코발트 또는 텅스텐 등으로 형성할 수 있다.

<48> 상기 금속배선층(20) 상에 상기 금속배선(22)과 전기적으로 연결되는 하부전극(25)을 형성할 수도 있다. 예를 들어, 상기 하부전극(25)은 Cr, Ti, TiW 및 Ta과 같은 금속으로 형성할 수 있다. 물론 상기 하부전극(25)은 형성되지 않을 수 있다.

<49> 상기 층간절연막(21)에 상기 반도체 기판(10)의 씨모스 회로와 연결되는 금속배선(22)을 형성한 후 상기 금속배선층(20) 상부로 포토다이오드를 형성하여 단위픽셀을 형성할 수 있다.

<50> 상기 포토다이오드는 금속배선층(220) 상부에 형성되어 외부에서 입사되는 빛을 받아 전기적 형태로 전환 및 보관하기 위한 것으로 실시예에서는 핀 다이오드(PIN diode)를 사용한다.

<51> 상기 핀 다이오드는 n형 비정질 실리콘층(n-type amorphous silicon), 진성 비정질 실리콘층(intrinsic amorphous silicon), p형 비정질 실리콘층(p-type amorphous silicon)이 접합된 구조로 형성되는 것이다. 포토다이오드의 성능은 외부의 빛을 받아 전기적 형태로 전환하는 효율과 충 보관 가능 전기량(charge capacitanc

Samsung Exhibit 1003, Page 131 of 516

e)에 따라 결정되는 것으로 기존의 포토다이오드는 P-N, N-P, N-P-N, P-N-P 등의 이종접합시 생성되는 공핍영역(Depletion region)에 전하를 생성 및 보관하였으나, 상기 핀 다이오드는 p형 실리콘층과 n형 실리콘층 사이에 순수한 반도체인 진성 비정질 실리콘층이 접합된 구조의 광 다이오드로서, 상기 p형과 n형 사이에 형성되는 진성 비정질 실리콘층이 모두 공핍영역이 되어 전하의 생성 및 보관에 유리하게 된다.

<52> 이와 같이 실시예에서는 포토다이오드로서 핀 다이오드를 사용하며 핀 다이오드의 구조는 P-I-N 또는 N-I-P의 구조로 형성될 수 있다. 특히, 실시예에서는 P-I-N 구조의 핀 다이오드가 사용되는 것을 예로 하며, 상기 n형 비정질 실리콘층(n-type amorphous silicon)은 제1 도전형 전도층(30), 상기 진성 비정질 실리콘층(intrinsic amorphous silicon)은 진성층(40), 상기 p형 비정질 실리콘층(p-type amorphous silicon)은 제2 도전형 전도층(50)이라 칭하도록 한다.

<53> 상기 핀 다이오드를 이용한 포토다이오드를 형성하는 방법에 대하여 설명하면 다음과 같다.

<54> 상기 금속배선층(20) 상에 제1 도전형 전도층(30)을 형성한다. 상기 제1 도전형 전도층(30)은 본 실시예에서 채용하는 P-I-N 다이오드의 N층의 역할을 할 수 있다. 즉, 상기 제1 도전형 전도층(30)은 N타입 도전형 전도층 일 수 있으나 이에 한정되는 것은 아니다.

<55> 상기 제1 도전형 전도층(30)은 N형 불순물이 도핑된 비정질 실리질 실리콘(n-doped amorphous silicon)을 이용하여 형성될 수 있으나, 이에 한정되는 것은 아니다.

<56> 즉, 상기 제1 도전형 전도층(30)은 비정질 실리콘에 게르마늄, 탄소,질소 또는 산소 등을 첨가하여 a-Si:H, a-SiGe:H, a-SiC, a-SiN:H a-SiO:H 등으로 형성될 수도 있다.

<57> 또한, 상기 제1 도전형 전도층(30)은 화학기상증착(CVD) 특히, PECVD 등에 의해 형성될 수 있다. 예를 들어, 상기 제1 도전형 전도층(30)은 실란가스(SiH_4)에 PH_3, P_2H_5 등을 혼합하여 PECVD에 의해 비정질 실리콘으로 형성될 수 있다.

<58> 그 다음, 상기 제1 도전형 전도층(30) 상으로 진성층(intrinsic layer)(40)을 형성한다. 상기 진성층(40)은 실시예에서 채용하는 I층의 역할을 할 수 있다.

<59> 상기 진성층(40)은 비정질 실리콘(intrinsic amorphous silicon)을 이용하여 형성될 수 있다. 상기 진성층(40)은 화학기상증착(CVD) 특히, PECVD 등에 의해 형성될 수 있다. 예를 들어, 상기 진성층(40)은 실란가스(SiH_4) 등을 이용하여 PECVD에 의해 비정질 실리콘으로 형성될 수 있다.

<60> 또한, 상기 진성층(40)은 상기 제1 도전형 전도층(30)의 두께 보다 약 10~1,000배 정도의 두꺼운 두께로 형성하는 것이 바람직하다. 이는 상기 진성층(40)의 두께가 두꺼울수록 포토다이오드의 공핍영역이 늘어나 많은 양의 광전하를 보관 및 생성하기에 유리하기 때문이다.

<61> 그 다음, 상기 진성층(40) 상으로 제2 도전형 전도층(50)을 형성한다.

<62> 상기 제2 도전형 전도층(50)은 실시예에서 채용하는 P-I-N 다이오드의 P층의 역할을 할 수 있다. 즉, 상기 제2 도전형 전도층(50)은 P 타입 도전형 전도층일 수 있으나 이에 한정되는 것은 아니다.

<63> 예를 들어, 상기 제2 도전형 전도층(50)은 P 도핑된 비정질 실리콘(p-doped amorphous silicon)을 이용하여 형성될 수 있으나, 이에 한정되는 것은 아니다.

<64> 상기 제2 도전형 전도층(50)은 화학기상증착(CVD) 특히, PECVD 등에 의해 형성될 수 있다. 예를 들어, 상기 제2 도전형 전도층(50)은 실란가스(SiH_4)에 BH_3 또는 B_2H_6 등의 가스를 혼합하여 PECVD에 의해 비정질 실리콘으로 형성될 수 있다.

<65> 상기와 같이 반도체 기판(10)에 형성된 회로영역과 포토다이오드가 수직형으로 형성됨으로써 포토다이오드의 필 팩터(fill factor)를 100%에 근접시킬 수 있다.

<66> 도 2를 참조하여, 상기 제2 도전형 전도층(50) 상부로 마스크 패턴(100)을 형성한다.

<67> 상기 마스크 패턴(100)은 상기 제2 도전형 전도층(50)을 요철형태로 형성하기 위한 것으로, 포토레지스트 필름을 도포하고 패터닝하여 형성한다.

<68> 상기 마스크 패턴(100)은 상기 제2 도전형 전도층(50) 상에 적어도 하나 이상 형성되어 상기 제2 도전형 전도층(50)의 상부 표면이 단차를 가지도록 형성할 수 있다.

Samsung Exhibit 1003, Page 132 of 516

<69> 도 3을 참조하여, 상기 마스크 패턴(100)을 식각마스크로 하여 상기 제2 도전형 전도층(50)을 식각하여 트렌치(52)를 형성한다. 그러면 상기 트렌치(52)에 의해 상기 제2 도전형 전도층(51)의 상부 표면은 요철형태의 요철부(53)가 형성된다.

<70> 상기 제2 도전형 전도층(51)의 식각은 건식 또는 습식식각 공정으로 진행될 수 있다. 특히, 상기 제2 도전형 전도층(51)의 식각은 상기 제2 도전형 전도층(51) 하부에 위치한 진성층(40)이 노출되지 않도록 진행한다.

<71> 상기와 같이, 상기 제2 도전형 전도층(51)의 상부 표면에 요철부(53)가 형성됨으로써 상기 제2 도전형 전도층(51)의 표면적은 증가하게 되고, 이로 인해 포토다이오드의 수광영역이 확장되어 이미지 센서의 광감지율을 향상시킬 수 있다.

<72> 또한, 상기 제2 도전형 전도층(51)의 요철부(53)에 의하여 하나의 픽셀 내에 볼록한 돔 형상의 렌즈가 적어도 하나 이상 형성되어 포토다이오드의 광 효율을 증가시킬 수 있다.

<73> 도 4를 참조하여, 상기 요철부(52)가 형성된 제2 도전형 전도층(51)의 상부로 상부전극(60)을 형성한다.

<74> 상기 상부전극(60)은 빛의 투과성이 좋고 전도성이 높은 투명전극으로 형성될 수 있다. 예를 들어, 상기 상부전극(60)은 ITO(indium tin oxide) 또는 CTO(cardium tin oxide) 등으로 형성될 수 있다.

<75> 상기 요철부(53)의 형태에 의하여 상기 상부전극(60)도 단차를 가지는 요철형태로 형성될 수 있다.

<76> 도 5a를 참조하여, 상기 상부전극(60) 상으로 접착층(70) 및 컬러필터(80)를 형성한다.

<77> 상기 접착층(70)은 상기 상부전극(60)과 컬러필터(80)의 접착력을 향상시키기 위한 것으로, 상기 상부전극(60) 상으로 열 수지(thermal resin)를 증착하여 형성한 후 평탄화 공정을 진행하여 형성한다.

<78> 그리고, 상기 접착층(70)의 상부로 컬러필터(80)를 형성한다.

<79> 상기와 같이 형성된 이미지 센서는 하나의 픽셀 내에 복수의 돔형태를 갖는 포토다이오드가 형성되어 집광율을 향상시킬 수 있다.

<80> 또는 도 5b에 도시된 바와 같이, 상기 금속배선(22) 상에 형성된 제2 도전형 전도층(51b)에 하나의 요철부(53b)가 형성될 수 있다.

<81> 그러면 상기 포토다이오드의 요철형태에 의하여 수광면적이 확장되어 감광지율을 높일 수 있다.

<82> <제2 실시예>

<83> 도 9는 제2 실시예에 따른 이미지 센서의 단면도이다.

<84> 도 9를 참조하여 실시예의 이미지 센서는, 씨모스 회로가 형성된 반도체 기판(10); 상기 반도체 기판(10) 상에 형성된 복수의 금속배선(22) 및 층간절연막(21)을 포함하는 금속배선층(20); 상기 금속배선층(20) 상에 상부표면에 적어도 하나 이상의 요철부(33)가 형성된 제1 도전형 전도층(31); 상기 제1 도전형 전도층(31) 상에 형성된 진성층(40); 및 상기 진성층(40) 상에 형성된 제2 도전형 전도층(50)을 포함한다.

<85> 상기 제1 도전형 전도층(31)에는 적어도 하나 이상의 트렌치(32)가 형성되어 상기 제1 도전형 전도층(31)의 상부표면은 하나 이상의 요철부(33)가 형성될 수 있다.

<86> 상기 금속배선(22) 상부에는 하부전극(25)이 형성될 수 있다.

<87> 상기 제2 도전형 전도층(50) 상부에는 상부전극(60) 및 컬러필터 어레이(80)가 형성될 수 있다.

<88> 또한, 상기 상부전극(60)과 컬러필터 어레이(80) 사이에는 접착층(70)이 형성될 수 있다. 예를 들어 상기 접착층(70)은 열 수지(thermal resin)로 형성된다

<89> 도 6 내지 도 9를 참조하여 제2 실시예의 이미지 센서의 제조공정을 설명한다.

<90> 도 6을 참조하여, 반도체 기판(10) 상에는 금속배선층(20) 및 하부전극(25)이 형성되어 있다.

<91> 상기 반도체 기판(10), 금속배선층(20) 및 하부전극(25)은 상술된 제1 실시예와 동일하므로 이에 대한 설명은 생략하기로 한다.

<92> 상기 층간절연막(21)에 상기 반도체 기판(10)의 씨모스 회로와 연결되는 금속배선(22)을 형성한 후 상기 금속배선층(20) 상부로 포토다이오드를 형성한다.

Samsung Exhibit 1003, Page 133 of 516

<93> 상기 포토다이오드는 금속배선층(220) 상부에 형성되어 외부에서 입사되는 빛을 받아 전기적 형태로 전환 및 보관하기 위한 것으로 실시예에서는 핀 다이오드(PIN diode)를 사용한다. 제2 실시예에서 사용되는 포토다이오드는 제1 실시예와 동일하므로 이에 대한 구체적은 설명은 생략하고 공정순서에 대해서만 설명하도록 한다.

<94> 상기 핀 다이오드를 이용한 포토다이오드를 형성하는 방법에 대하여 설명하면 다음과 같다.

<95> 상기 금속배선층(20) 상에 제1 도전형 전도층(30)을 형성한 후, 상기 제1 도전형 전도층(30) 상부로 적어도 하나 이상의 마스크 패턴(100)을 형성한다.

<96> 상기 마스크 패턴(100)은 상기 제1 도전형 전도층(30)을 요철형태로 형성하기 위한 것으로, 포트레지스트 필름을 도포하고 패터닝하여 형성한다. 상기 마스크 패턴(100)은 상기 제1 도전형 전도층(30) 상에 적어도 하나 이상 형성되어 상기 제1 도전형 전도층(30)의 상부 표면이 단차를 가지도록 형성할 수 있다.

<97> 도 7을 참조하여, 상기 마스크 패턴(100)을 식각마스크로 하여 상기 제1 도전형 전도층(30)을 식각하여 트렌치(32)를 형성한다. 그러면 상기 트렌치(32)에 의해 상기 제1 도전형 전도층(31)의 상부 표면에는 요철형태의 요철부(33)가 형성된다.

<98> 상기 제1 도전형 전도층(31)의 식각은 건식 또는 습식식각 공정으로 진행될 수 있다. 특히, 상기 제1 도전형 전도층(31)의 식각은 상기 제1 도전형 전도층(31) 하부에 위치한 금속배선층(20)이 노출되지 않도록 진행한다.

<99> 도 8을 참조하여, 상기 제1 도전형 전도층(30) 상으로 진성층(intrinsic layer)(40) 및 제2 도전형 전도층(50)을 순차적으로 형성한다.

<100> 그러면, 상기 제1 도전형 전도층(31)의 상부 표면을 따라 형성되는 상기 진성층(40)은 상기 제1 도전형 전도층(31)의 요철부(33)에 의해 상부 표면이 단차를 가지게 되고, 상기 제2 도전형 전도층(50)은 상기 진성층(40)에 의해 상부 표면이 단차를 가지게 된다.

<101> 따라서, 상기 제1 도전형 전도층(31), 진성층(40) 및 제2 도전형 전도층(50)으로 이루어지는 포토다이오드의 표면은 요철형태로 형성되어 표면적 증가로 인하여 광감지율을 향상시킬 수 있게 된다.

<102> 또한, 상기 포토다이오드의 형태가 볼록렌즈와 같은 형태를 가지게 되므로 집광율을 향상시킬 수 있게 된다.

<103> 또한, 상기 포토다이오드는 하나의 픽셀당 적어도 하나 이상의 요철부가 형성되어 포토다이오드의 광감지율을 높일 수 있다.

<104> 도 9를 참조하여, 상기 제2 도전형 전도층(50)의 상부로 상부전극(60)을 형성한다.

<105> 상기 상부전극(60)은 빛의 투과성이 좋고 전도성이 높은 투명전극으로 형성될 수 있다. 예를 들어, 상기 상부전극(60)은 ITO(indium tin oxide) 또는 CTO(cardium tin oxide) 등으로 형성될 수 있다.

<106> 그리고, 상기 상부전극(60) 상으로 접착층(70) 및 컬러필터(80)를 형성한다.

<107> 상기 접착층(70)은 상기 상부전극(60)과 컬러필터(80)의 접착력을 향상시키기 위한 것으로, 상기 상부전극(60) 상으로 열 수지(thermal resin)를 증착하여 형성한 후 평탄화 공정을 진행하여 형성한다.

<108> 그리고, 상기 접착층(70)의 상부로 컬러필터(80)를 형성한다.

<109> <제3 실시예>

<110> 도 13은 제3 실시예에 따른 이미지 센서의 단면도이다.

<111> 도 13을 참조하여 실시예의 이미지 센서는, 씨모스 회로가 형성된 반도체 기판(10); 상기 반도체 기판(10) 상에 형성된 복수의 금속배선(22) 및 층간절연막(21)을 포함하는 금속배선층(20); 상기 금속배선층(20) 상에 형성된 제1 도전형 전도층(30); 상기 제1 도전형 전도층(30) 상에 상부표면에 적어도 하나 이상의 요철부(43)가 형성된 진성층(41); 및 상기 진성층(41) 상에 형성된 제2 도전형 전도층(50)을 포함한다.

<112> 상기 진성층(41)에는 적어도 하나 이상의 트렌치(42)가 형성되어 상기 진성층(41)의 상부표면은 적어도 하나 이상의 요철부(43)가 형성될 수 있다.

<113> 상기 금속배선(22) 상부에는 하부전극(25)이 형성될 수 있다.

<114> 상기 제2 도전형 전도층(50) 상부에는 상부전극(60) 및 컬러필터 어레이(80)가 형성될 수 있다.

Samsung Exhibit 1003, Page 134 of 516

<115> 또한, 상기 상부전극(60)과 컬러필터 어레이(80) 사이에는 접착층(70)이 형성될 수 있다. 예를 들어 상기 접착층(70)은 열 수지(thermal resin)로 형성된다

<116> 도 10 내지 도 13을 참조하여 제2 실시예의 이미지 센서의 제조공정을 설명한다.

<117> 도 10을 참조하여, 반도체 기판(10) 상에는 금속배선층(20) 및 하부전극(25)이 형성되어 있다.

<118> 상기 반도체 기판(10), 금속배선층(20) 및 하부전극(25)은 상술된 제1 실시예와 동일하므로 이에 대한 설명은 생략하기로 한다.

<119> 상기 층간절연막(21)에 상기 반도체 기판(10)의 씨모스 회로와 연결되는 금속배선(22)을 형성한 후 상기 금속배선층(20) 상부로 포토다이오드를 형성한다.

<120> 상기 포토다이오드는 금속배선층(220) 상부에 형성되어 외부에서 입사되는 빛을 받아 전기적 형태로 전환 및 보관하기 위한 것으로 실시예에서는 핀 다이오드(PIN diode)를 사용한다. 제2 실시예에서 사용되는 포토다이오드는 제1 실시예와 동일하므로 이에 대한 구체적은 설명은 생략하고 공정순서에 대해서만 설명하도록 한다.

<121> 상기 핀 다이오드를 이용한 포토다이오드를 형성하는 방법에 대하여 설명하면 다음과 같다.

<122> 상기 금속배선층(20) 상에 제1 도전형 전도층(30) 및 진성층(40)을 순차적으로 형성한다.

<123> 상기 진성층(40) 상으로 상부로 마스크 패턴(100)을 형성한다.

<124> 상기 마스크 패턴(100)은 상기 진성층(40)을 요철형태로 형성하기 위한 것으로, 포토레지스트 필름을 도포하고 패터닝하여 형성한다. 상기 마스크 패턴(100)은 상기 진성층(40) 상에 적어도 하나 이상 형성되어 상기 진성층(41)의 상부 표면이 단차를 가지도록 형성할 수 있다.

<125> 도 11을 참조하여, 상기 마스크 패턴(100)을 식각마스크로 하여 상기 진성층(40)을 식각하여 트렌치(42)를 형성한다. 그러면 상기 트렌치(42)에 의해 상기 진성층(41)의 상부 표면에는 요철형태의 요철부(43)가 형성된다.

<126> 상기 진성층(41)의 식각은 건식 또는 습식식각 공정으로 진행될 수 있다. 특히, 상기 진성층(41)의 식각은 상기 진성층(41) 하부에 위치한 제1 도전형 전도층(30)이 노출되지 않도록 진행한다.

<127> 도 12를 참조하여, 상기 진성층(41) 상으로 제2 도전형 전도층(50)을 형성한다.

<128> 그러면, 상기 진성층(41)의 상부 표면을 따라 형성되는 상기 제2 도전형 전도층(50)은 상기 진성층(41)의 요철부(43)에 의해 상부 표면이 단차를 가지게 된다.

<129> 따라서, 상기 제1 도전형 전도층(30), 진성층(41) 및 제2 도전형 전도층(50)으로 이루어지는 포토다이오드의 표면은 요철형태로 형성되어 표면적 증가로 인하여 광감지율을 향상시킬 수 있게 된다.

<130> 또한, 상기 포토다이오드의 형태가 볼록렌즈와 같은 형태를 가지게 되므로 집광율을 향상시킬 수 있게 된다.

<131> 도 9를 참조하여, 상기 제2 도전형 전도층(50)의 상부로 상부전극(60)을 형성한다.

<132> 상기 상부전극(60)은 빛의 투과성이 좋고 전도성이 높은 투명전극으로 형성될 수 있다. 예를 들어, 상기 상부전극(60)은 ITO(indium tin oxide) 또는 CTO(cardium tin oxide) 등으로 형성될 수 있다.

<133> 그리고, 상기 상부전극(60) 상으로 접착층(70) 및 컬러필터(80)를 형성한다.

<134> 상기 접착층(70)은 상기 상부전극(60)과 컬러필터(80)의 접착력을 향상시키기 위한 것으로, 상기 상부전극(60) 상으로 열 수지(thermal resin)를 증착하여 형성한 후 평탄화 공정을 진행하여 형성한다.

<135> 그리고, 상기 접착층(70)의 상부로 컬러필터(80)를 형성한다.

<136> 이상에서 설명한 실시예는 전술한 실시예 및 도면에 한정되는 것이 아니고, 본 실시예의 기술적 사상을 벗어나지 않는 범위 내에서 여러 가지 치환, 변형 및 변경할 수 있다는 것은 본 실시예가 속하는 기술 분야에서 통상의 지식을 가진자에게 있어 명백할 것이다.

발명의 효과

<137> 실시예에 따른 이미지 센서 및 그의 제조방법에 의하면 트랜지스터 회로와 포토다이오드의 수직형 집적을 제공할 수 있다.

Samsung Exhibit 1003, Page 135 of 516

<138> 또한, 트랜지스터 회로와 포토다이오드의 수직형 집적에 의해 필 팩터(fill factor)를 100%에 근접시킬 수 있다.

<139> 또한, 수직형 집적에 의해 종래기술보다 같은 픽셀 사이즈에서 높은 센서티비티(sensitivity)를 제공할 수 있다.

<140> 또한, 각 단위 픽셀은 센서티비티(sentivity)의 감소없이 보다 복잡한 회로를 구현할 수 있다.

<141> 또한, 수직형 포토다이오드를 채용하면서 단위 픽셀 간의 절연성을 확보함으로써 픽셀간의 크로스토크 등을 방지하여 이미지 센서의 신뢰성을 향상시킬 수 있다.

<142> 또한, 포토다이오드의 단위픽셀을 구현함에 있어 단위 픽셀 내의 포토다이오드의 표면적을 증가시켜 광감지율을 향상시킬 수 있다.

<143> 또한, 상기 단위픽셀에 해당하는 포토다이오드가 볼록렌즈와 같은 렌즈형태를 가지게 되어 집광율을 향상시킬 수 있다.

도면의 간단한 설명

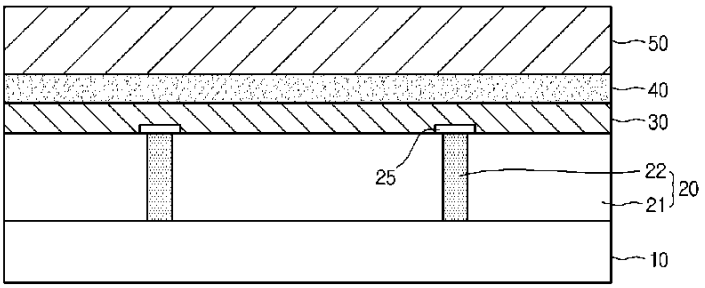
<1> 도 1 내지 도 5a는 제1 실시예의 이미지 센서의 제조 공정을 나타내는 도면이다.

<2> 도 6 내지 도 9는 제2 실시예의 이미지 센서의 제조 공정을 나타내는 도면이다.

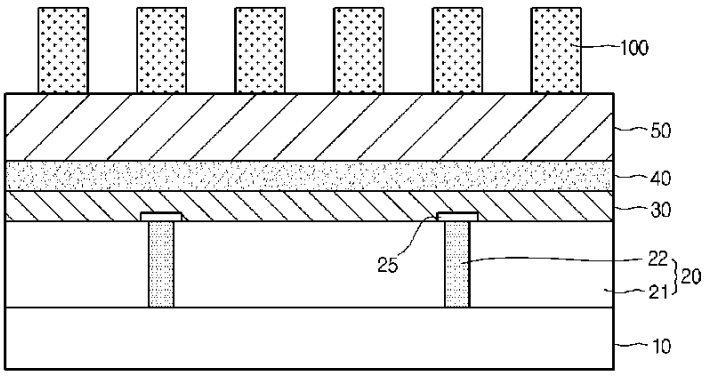
<3> 도 10 내지 도 13은 제3 실시예의 이미지 센서의 제조 공정을 나타내는 도면이다.

도면

도면1

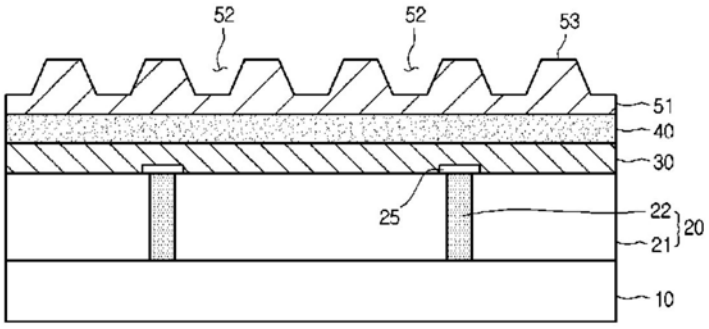


도면2

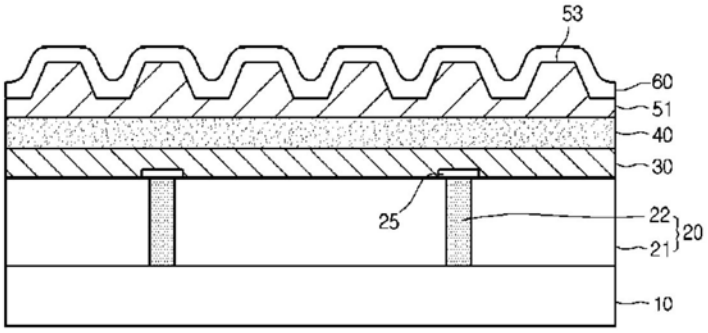


Samsung Exhibit 1003, Page 136 of 516

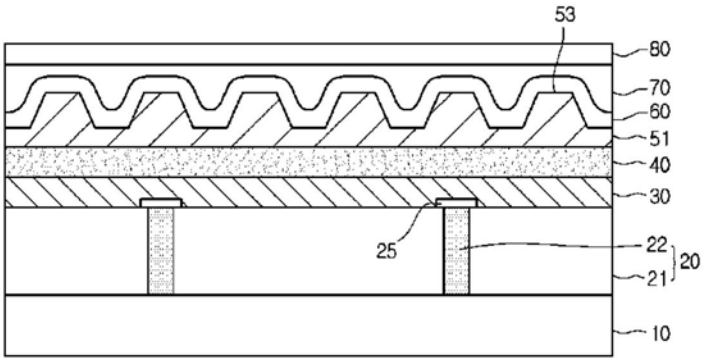
도면3



도면4

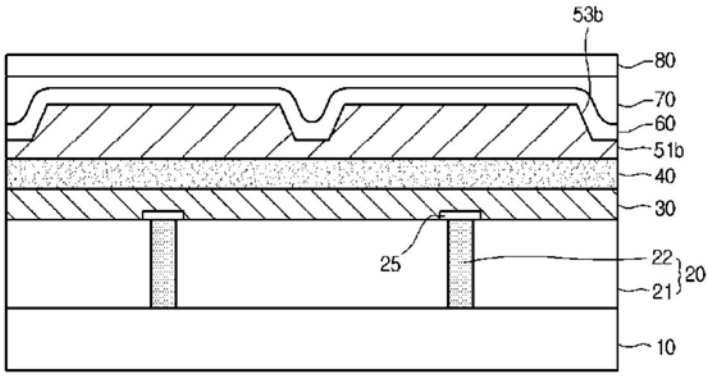


도면5a

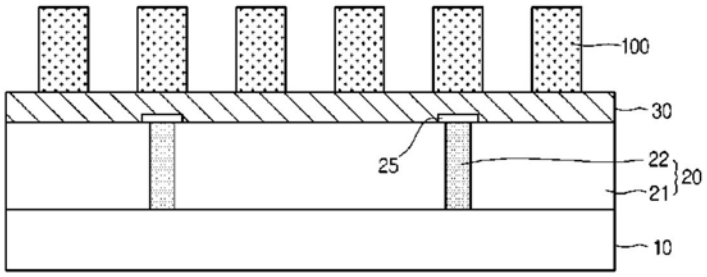


Samsung Exhibit 1003, Page 137 of 516

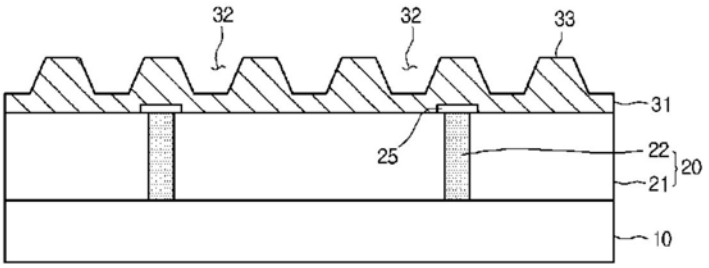
도면5b


53b
80
70
60
51b
40
30
25
22
21
20
10

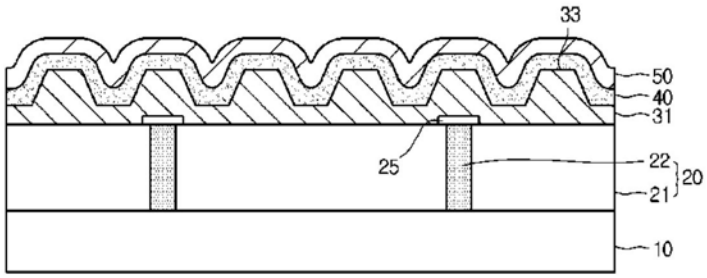
도면6


100
30
25
22
21
20
10

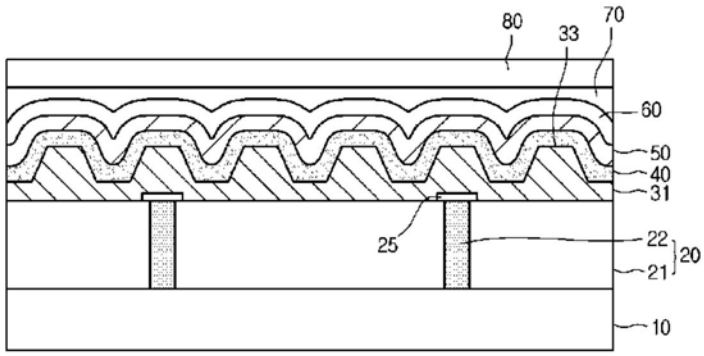
도면7


32
32
33
31
25
22
21
20
10

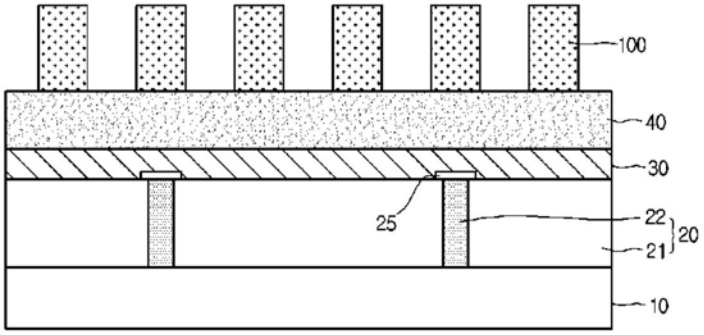
도면8



도면9

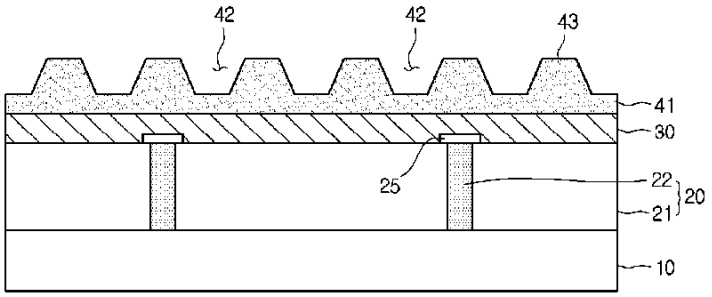


도면10

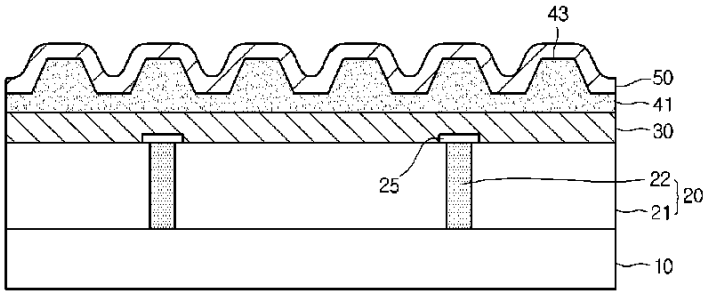


Samsung Exhibit 1003, Page 139 of 516

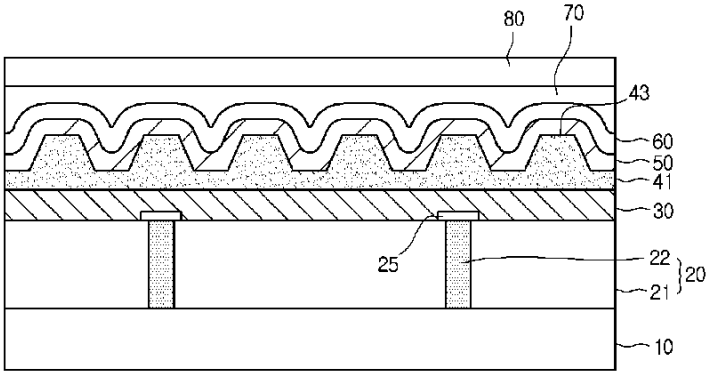
도면11



도면12



도면13



Samsung Exhibit 1003, Page 140 of 516

Electronic Acknowledgement Receipt

EFS ID:	46692503
Application Number:	17707429
International Application Number:	
Confirmation Number:	1214
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	139982
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	309-0011USDIVCIP2
Receipt Date:	26-SEP-2022
Filing Date:	29-MAR-2022
Time Stamp:	14:42:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Supplemental Response or Supplemental Amendment	309-0011USDIVCIP2_SupplementalROA.pdf	575034 3e93e89f244dc960eba844e8f8046b55ff893f45	no	14

Warnings:

Information:	
Total Files Size (in bytes):	575034

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

Applicant appreciates the Examiner's thorough review of the claims and the helpful suggestions for clarifications.

Claim Objections

Claims 1-30 are canceled. Claims 31-50 are pending. Applicant believes that the new claims avoid the informalities that the Office Action pointed out regarding the canceled claims.

The total number of claims is reduced from 30 to 20 and the number of independent claims from 4 to 2.

Double Patenting

When filing the subject application, Applicant submitted a Terminal Disclaimer over parent application Ser. No. 17/532,831 and any patent issuing therefrom. The parent application became Patent 11,309,444 B1 on which the double patenting rejection is based. Applicant believes no additional Terminal Disclaimer is needed but will submit one should the Examiner require it.

35 USC §112 Issues

Applicant submits that claims 31-50 are supported by the original specification and, accordingly, the Section 112 issues that the Office Action raised regarding now canceled claims need not be discussed.

Claims 31-39 are supported mainly by the example of Figs. 5A and 5B. For the Examiner's convenience, this paper attaches a version of these claims indicating examples of support in figures and paragraphs of the ultimate parent U.S. application Ser. No. 14/947,718 filed November 20, 2015.

Claims 40-50 are supported mainly by the example of Figs. 7A and 7B. For the Examiner's convenience, this paper attaches a version of claim 40 indicating examples of support in figures and paragraphs of the ultimate parent. Claims 41-48 are like claims

depending on claim 31 except that they depend on claim 40 so examples of support are not duplicated. Examples of support are indicated for claims 49 and 50.

Applicant notes that the original specification explains in paragraph 0071 that "individual features of one or several of the specific embodiments described herein can be used in combination with features or [sic, of] other described embodiments," and that the identified examples of support are just that – examples – and other support can be found in other figures and paragraphs in the original application.

If the Examiner finds that further clarifications may help or that a phone call may otherwise help expedite prosecution, Application invites the Examiner to telephone the undersigned representative.

If a petition for an extension of time is required to make this response timely, this paper should be taken as such a petition. The Patent Office is hereby authorized to charge any required fees in connection with this paper, and to credit any overpayment, to our Deposit Account No. 600125.

Respectfully Submitted,

WISSING MILLER LLP
Attorney for Applicants

By: /Ivan S. Kavrukov/
Ivan S. Kavrukov
Reg. No. 25,161
Tel.: (917) 945-0121

Attachment: Claims with indicated examples of support in ultimate parent U.S. application Ser. No. 14/947,718 filed November 20, 2015.

Attachment: Claims 31-50 with inserted non-limiting examples of support in the ultimate parent U.S. application Ser. No. 14/947,718 filed November 20, 2015:

31. A photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar holes comprising:

a laterally extending array of pillars that have rectangular cross-sections in a horizontal plane (¶132: "the shape of the pillars can be … rectangle") and are elongated in an up-down direction (Fig. 5B);

wherein said array of pillars comprises:

a first doped semiconductor material (510);

an intermediate semiconductor material (I-layer 508); and

solid dielectric (522) between at least portions of sidewalls of adjacent pillars of said array of pillars;

a second doped semiconductor material (506);

wherein:

the intermediate semiconductor material is between said first and second doped semiconductor materials;

the first and second doped semiconductor materials are doped to opposite semiconductor types (P, N);

the intermediate semiconductor material is less doped than at least one of the first and second doped semiconductor materials and the degree of doping is the same or different for different positions in the intermediate semiconductor material; and

each of the first and second doped semiconductor materials and said intermediate semiconductor material comprises Si (Fig. 5B);

one or more deliberately formed in-pillar holes with solid dielectric therein (Fig. 49 – "pillar with hole;" ¶122: "Planerization (filler step) using . . . dielectrics");

top and bottom electrical contacts (526, 528, 530) electrically coupled with said array of pillars, wherein said photodetector device is

configured to respond to light photons incident on said array of pillars by photo-generated charge carriers therein; and

a base dielectric region (504) that is below the array of pillars and comprises substantially solid dielectric material;

wherein the pillars of said array of pillars:

are laterally spaced center to center by no more than 10,000 nanometers (Figs. 43-46: "C-C 100-10,000 nm"); and

have up-down lengths of said intermediate semiconductor material in the range of 100-5000 nanometers (¶ 115: "from 0.1 to 5 micrometers");

wherein at least said pillars, in-pillar holes, and solid dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars increase photon absorption of said device of incident light by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said one or more in-pillar holes (¶97);and

wherein said array of pillars is monolithically integrated in or on said semiconductor substrate with electronic circuits that include active elements for signal processing and transmission (Provisional 61/834,873 filed June 13, 2013 and incorporated by reference in subject application in ¶ 0001: See sentence bridging pages 1 and 2: "the detector array can be monolithically integrated with Si electronic devices such as bipolar transistors, CMOS . . . (ASIC) for signal processing, storage, signal conditioning, and transmission;" see also ¶ 82 of the subject application).

32. The photodetector device of claim 31, in which the top electrical contact is a transparent, laterally continuous region that is electrically coupled to a plurality of said pillars (¶ 146: "transparent conducting oxide").

33. The photodetector device of claim 31, in which each of said pillars has a plurality of said one or more in-pillar holes (¶ 232: "hole(s) can exist in a pillar").

34. The photodetector device of claim 31, in which each of said pillars has only one of said one or more in-pillar holes (Fig. 49: "Pillar with hole").

35. The photodetector device of claim 31, in which in which said one or more in-pillar holes extend to a depth in the range of 100-10,000 nanometers (¶ 231: "the holes have … depths ranging from 1 to 10 microns.").

36. The photodetector device of claim 31, in which said one or more in-pillar holes extend into said intermediate semiconductor material (¶ 198: "The microstructured holes 2722 (or space around pillars) … can be partially into the 'I' layer.").

37. The photodetector device of claim 31, in which said one or more in-pillar holes are pyramid-shaped (¶ 234: "holes … shapes such as pyramids").

38. The photodetector device of claim 31, in which each of said pillars has at least two of said one or more in-pillar holes that partly overlap (Fig. 46 shows examples of partly overlapping holes).

39. The photodetector device of claim 31, in which said second doped semiconductor material comprises a laterally continuous region coupled to a plurality of said pillars (Fig. 5B).

40. A photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar holes comprising:

an array of pillars that have rectangular cross-sections in a horizontal plane (Fig. 7B);

wherein said array of pillars comprises at least:

a first doped semiconductor material (Figs. 7A-B: top P);

a first intermediate semiconductor material (Figs. 7A-B: upper I Si); and

solid dielectric between at least portions of sidewalls of adjacent pillars;

a second doped semiconductor material (Figs. 7A-B: lower P);

wherein the first intermediate material is between the first and second doped semiconductor materials (Fig. 7B);

a third doped semiconductor material (Figs. 7A-B: N);

wherein said first and second semiconductor materials (Figs. 7A-B: upper and lower P) are doped to a first semiconductor type and the third semiconductor material is doped to a second semiconductor type (Figs. 7A-B: N);

a second intermediate semiconductor material (Figs. 7A-B: lower I Si) between the second and third doped semiconductor materials;

wherein the first and second intermediate semiconductor materials are doped less than at least one of the first, second, and third doped semiconductor materials or are undoped;

one or more deliberately formed in-pillar holes with solid dielectric therein (Fig. 49 – "Pillar with hole;" ¶122: "Planerization (filler step) using . . . dielectrics");

first and second electrical contacts that are electrically coupled with said array of pillars and are configured for operation of said device as an avalanche photodetector responding to light incident on the array of pillars by multiplying photogenerated charge carriers therein, with a multiplication gain greater than two (¶ 0009: "gain greater than 2"); and

a base dielectric region that is under the array of pillars and comprises substantially solid dielectric material (Fig. 7A-B: Si substrate);

wherein said pillars of said array of pillars:

are spaced from each other center to center by no more than 10,000 nanometers (Figs. 43-46: "C-C 100-10,000 nm); and

have an up-down dimension of said first intermediate semiconductor material that is less than 5000 nanometers (Fig. 8: region 810 thickness 0.1 – 5 um);

wherein at least said pillars, in-pillar holes, and dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars increase photon absorption of said device of incident light by a factor of at least 1.1, at least at selected wavelength of said incident light that include visible and infrared light compared to a like device lacking said one or more in-pillar holes (¶ 0097); and

wherein said array of pillars is monolithically integrated in or on said semiconductor substrate with electronic circuits including active elements for signal processing and transmission (Provisional 61/834,873 filed June 13, 2013 and incorporated by reference in subject application in ¶ 0001: See sentence bridging pages 1 and 2: "the detector array can be monolithically integrated with Si electronic devices such as bipolar transistors, CMOS . . . (ASIC) for signal processing, storage, signal conditioning, and transmission;" see also ¶ 82 of the subject application).

41. The photodetector device of claim 40, in which the top electrical contact is a transparent, laterally continuous region that is electrically coupled to a plurality of said pillars.

42. The photodetector device of claim 40, in which each of said pillars has a plurality of said one or more in-pillar holes.

43. The photodetector device of claim 40, in which each of said pillars has only one of said one or more in-pillar holes.

44. The photodetector device of claim 40, in which in which said one or more in-pillar holes extend to a depth in the range of 100-10,000 nanometers.

45. The photodetector device of claim 40, in which said one or more in-pillar holes extend into said first intermediate semiconductor material.

46. The photodetector device of claim 40, in which said one or more in-pillar holes are pyramid-shaped.

47. The photodetector device of claim 40, in which each of said pillars has at least two of said one or more in-pillar holes that partly overlap.

48. The photodetector device of claim 40, in which said third doped semiconductor material comprises a laterally continuous region coupled to a plurality of said pillars.

49. The photodetector device of claim 40, in which said second intermediate semiconductor material has a thickness in the 100-2,000 nm range (¶ 124: layer 806 is 0.1-2 μm).

50. The photodetector device of claim 40, in which said solid dielectric between at least portions of sidewalls of adjacent pillars extends down to said second intermediate semiconductor material (Fig. 15C).

Amendments to the claims:

Please rewrite the claims as follows. These amended claims replace all previously filed claims:

Claims 1-30 (canceled)

31. (previously presented) A photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar holes comprising:

a laterally extending array of pillars that have rectangular cross-sections in a horizontal plane;

wherein said array of pillars comprises:

a first doped semiconductor material;

an intermediate semiconductor material; and

solid dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars;

a second doped semiconductor material);

wherein:

the intermediate semiconductor material is between said first and second doped semiconductor materials;

the first and second doped semiconductor materials are doped to opposite semiconductor types;

the intermediate semiconductor material is less doped than at least one of the first and second doped semiconductor materials and the degree of doping is the same or different for different positions in the intermediate semiconductor material; and

each of the first and second doped semiconductor materials and said intermediate semiconductor material comprises Si;

one or more deliberately formed in-pillar holes with solid dielectric therein;

top and bottom electrical contacts electrically coupled with said array of pillars, wherein said photodetector device is configured to respond

to light photons incident on said array of pillars by photo-generated charge carriers therein; and

a base dielectric region that is below the array of pillars and comprises substantially solid dielectric material;

wherein the pillars of said array of pillars:

are laterally spaced center to center by no more than 10,000 nanometers; and

have up-down lengths of said intermediate semiconductor material in the range of 100-5000 nanometers;

wherein at least said pillars, in-pillar holes, and solid dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars increase photon absorption of said device of incident light by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said one or more in-pillar holes;

wherein said array of pillars is monolithically integrated in or on said semiconductor substrate with electronic circuits that include active elements for signal processing and transmission.

32. (previously presented) The photodetector device of claim 31, in which the top electrical contact is a transparent, laterally continuous region that is electrically coupled to a plurality of said pillars.

33. (previously presented) The photodetector device of claim 31, in which each of said pillars has a plurality of said one or more in-pillar holes.

34. (previously presented) The photodetector device of claim 31, in which each of said pillars has only one of said one or more in-pillar holes.

35. (previously presented) The photodetector device of claim 31, in which in which said one or more in-pillar holes extend to a depth in the range of 100-10,000 nanometers.

36. (previously presented) The photodetector device of claim 31, in which said one or more in-pillar holes extend into said intermediate semiconductor material.

37. (previously presented) The photodetector device of claim 31, in which said one or more in-pillar holes are pyramid-shaped.

38. (previously presented) The photodetector device of claim 31, in which each of said pillars has at least two of said one or more in-pillar holes that partly overlap.

39. (previously presented) The photodetector device of claim 31, in which said second doped semiconductor material comprises a laterally continuous region coupled to a plurality of said pillars.

40. (previously presented) A photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar holes comprising:

an array of pillars that have rectangular cross-sections in a horizontal plane;

wherein said array of pillars comprises at least:

a first doped semiconductor material;

a first intermediate semiconductor material; and

solid dielectric between at least portions of sidewalls of adjacent pillars;

a second doped semiconductor material;

wherein the first intermediate material is between the first and second doped semiconductor materials;

a third doped semiconductor material;

wherein said first and second semiconductor materials are doped to a first semiconductor type and the third semiconductor material is doped to a second semiconductor type;

a second intermediate semiconductor material between the second and third doped semiconductor materials;

wherein the first and second intermediate semiconductor materials are doped less than at least one of the first, second, and third doped semiconductor materials or are undoped;

one or more deliberately formed in-pillar holes with solid dielectric therein;

first and second electrical contacts that are electrically coupled with said array of pillars and are configured for operation of said device as an avalanche photodetector responding to light incident on the array of pillars by multiplying photogenerated charge carriers therein, with a multiplication gain greater than two; and

a base dielectric region that is under the array of pillars and comprises substantially solid dielectric material;

wherein said pillars of said array of pillars:

are spaced from each other center to center by no more than 10,000 nanometers; and

have an up-down dimension of said first intermediate semiconductor material that is less than 5000 nanometers;

wherein at least said pillars, in-pillar holes, and dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars increase photon absorption of said device of incident light by a factor of at least 1.1, at least at selected wavelength of said incident light that include visible and infrared light compared to a like device lacking said one or more in-pillar holes; and

wherein said array of pillars is monolithically integrated in or on said semiconductor substrate with electronic circuits including active elements for signal processing and transmission.

41. (previously presented) The photodetector device of claim 40, in which the top electrical contact is a transparent, laterally continuous region that is electrically coupled to a plurality of said pillars.

42. (previously presented) The photodetector device of claim 40, in which each of said pillars has a plurality of said one or more in-pillar holes.

43. (previously presented) The photodetector device of claim 40, in which each of said pillars has only one of said one or more in-pillar holes.

44. (previously presented) The photodetector device of claim 40, in which in which said one or more in-pillar holes extend to a depth in the range of 100-10,000 nanometers.

45. (previously presented) The photodetector device of claim 40, in which said one or more in-pillar holes extend into said first intermediate semiconductor material.

46. (previously presented) The photodetector device of claim 40, in which said one or more in-pillar holes are pyramid-shaped.

47. (previously presented) The photodetector device of claim 40, in which each of said pillars has at least two of said one or more in-pillar holes that partly overlap.

48. (currently amended) The photodetector device of claim 40~~31~~, in which said second doped semiconductor material comprises a laterally continuous region coupled to a plurality of said pillars.

49. (currently amended) The photodetector device of claim 40~~31~~, in which said second intermediate semiconductor material has a thickness in the 100-2,000 nm range.

50. (currently amended) The photodetector device of claim 40~~31~~, in which said solid dielectric between at least portions of sidewalls of adjacent pillars extends down to said second intermediate semiconductor material.

THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Shih-Yuan WANG et al.
Serial No.:	17/707,429
Examiner:	Ho, Hoang Quan Tran
Group Art Unit	2818
Filing Date:	March 29, 2022
For:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
Conf. No.	1214

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: September 26, 2022

I hereby certify that this correspondence is being transmitted via Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

SUPPLEMENTAL RESPONSE TO NON-FINAL OFFICE ACTION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In further response to the Non-Final Office Action dated June 24, 2022, and following the Response filed September 23, 2022, Applicant submits the following Supplemental Response that: (1) corrects the dependency of claims 48-50; and (2) notes that in the Appendix, the references are to paragraphs of the ultimate parent U.S. patent application Ser. No. 14/947,718 filed November 20, 2015. In other respects, the claims and remarks are the same as in the Response filed September 23, 2022, except for claim status notation.

THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Shih-Yuan WANG et al.
Serial No.:	17/707,429
Examiner:	Ho, Hoang Quan Tran
Group Art Unit	2818
Filing Date:	March 29, 2022
For:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
Conf. No.	1214

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: September 23, 2022

I hereby certify that this correspondence is being transmitted via Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

RESPONSE TO NON-FINAL OFFICE ACTION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the Non-Final Office Action dated June 24, 2022, Applicant submits the following Amendments and Remarks. Amendments to the Claims begin at page 2. Remarks begin at page 5.

Amendments to the claims:

Please rewrite the claims as follows. These amended claims replace all previously filed claims:

Claims 1-30 (canceled)

31. (new) A photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar holes comprising:

a laterally extending array of pillars that have rectangular cross-sections in a horizontal plane;

wherein said array of pillars comprises:

a first doped semiconductor material;

an intermediate semiconductor material; and

solid dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars;

a second doped semiconductor material);

wherein:

the intermediate semiconductor material is between said first and second doped semiconductor materials;

the first and second doped semiconductor materials are doped to opposite semiconductor types;

the intermediate semiconductor material is less doped than at least one of the first and second doped semiconductor materials and the degree of doping is the same or different for different positions in the intermediate semiconductor material; and

each of the first and second doped semiconductor materials and said intermediate semiconductor material comprises Si;

one or more deliberately formed in-pillar holes with solid dielectric therein;

top and bottom electrical contacts electrically coupled with said array of pillars, wherein said photodetector device is configured to respond

to light photons incident on said array of pillars by photo-generated charge carriers therein; and

a base dielectric region that is below the array of pillars and comprises substantially solid dielectric material;

wherein the pillars of said array of pillars:

are laterally spaced center to center by no more than 10,000 nanometers; and

have up-down lengths of said intermediate semiconductor material in the range of 100-5000 nanometers;

wherein at least said pillars, in-pillar holes, and solid dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars increase photon absorption of said device of incident light by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said one or more in-pillar holes;

wherein said array of pillars is monolithically integrated in or on said semiconductor substrate with electronic circuits that include active elements for signal processing and transmission.

32. (new) The photodetector device of claim 31, in which the top electrical contact is a transparent, laterally continuous region that is electrically coupled to a plurality of said pillars.

33. (new) The photodetector device of claim 31, in which each of said pillars has a plurality of said one or more in-pillar holes.

34. (new) The photodetector device of claim 31, in which each of said pillars has only one of said one or more in-pillar holes.

35. (new) The photodetector device of claim 31, in which in which said one or more in-pillar holes extend to a depth in the range of 100-10,000 nanometers.

36. (new) The photodetector device of claim 31, in which said one or more in-pillar holes extend into said intermediate semiconductor material.

37. (new) The photodetector device of claim 31, in which said one or more in-pillar holes are pyramid-shaped.

38. (new) The photodetector device of claim 31, in which each of said pillars has at least two of said one or more in-pillar holes that partly overlap.

39. (new) The photodetector device of claim 31, in which said second doped semiconductor material comprises a laterally continuous region coupled to a plurality of said pillars.

40. (new) A photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar holes comprising:

an array of pillars that have rectangular cross-sections in a horizontal plane;

wherein said array of pillars comprises at least:

a first doped semiconductor material;

a first intermediate semiconductor material; and

solid dielectric between at least portions of sidewalls of adjacent pillars;

a second doped semiconductor material;

wherein the first intermediate material is between the first and second doped semiconductor materials;

a third doped semiconductor material;

wherein said first and second semiconductor materials are doped to a first semiconductor type and the third semiconductor material is doped to a second semiconductor type;

a second intermediate semiconductor material between the second and third doped semiconductor materials;

wherein the first and second intermediate semiconductor materials are doped less than at least one of the first, second, and third doped semiconductor materials or are undoped;

one or more deliberately formed in-pillar holes with solid dielectric therein;

first and second electrical contacts that are electrically coupled with said array of pillars and are configured for operation of said device as an avalanche photodetector responding to light incident on the array of pillars by multiplying photogenerated charge carriers therein, with a multiplication gain greater than two; and

a base dielectric region that is under the array of pillars and comprises substantially solid dielectric material;

wherein said pillars of said array of pillars:

are spaced from each other center to center by no more than 10,000 nanometers; and

have an up-down dimension of said first intermediate semiconductor material that is less than 5000 nanometers;

wherein at least said pillars, in-pillar holes, and dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars increase photon absorption of said device of incident light by a factor of at least 1.1, at least at selected wavelength of said incident light that include visible and infrared light compared to a like device lacking said one or more in-pillar holes; and

wherein said array of pillars is monolithically integrated in or on said semiconductor substrate with electronic circuits including active elements for signal processing and transmission.

41. (new) The photodetector device of claim 40, in which the top electrical contact is a transparent, laterally continuous region that is electrically coupled to a plurality of said pillars.

42. (new) The photodetector device of claim 40, in which each of said pillars has a plurality of said one or more in-pillar holes.

43. (new) The photodetector device of claim 40, in which each of said pillars has only one of said one or more in-pillar holes.

44. (new) The photodetector device of claim 40, in which in which said one or more in-pillar holes extend to a depth in the range of 100-10,000 nanometers.

45. (new) The photodetector device of claim 40, in which said one or more in-pillar holes extend into said first intermediate semiconductor material.

46. (new) The photodetector device of claim 40, in which said one or more in-pillar holes are pyramid-shaped.

47. (new) The photodetector device of claim 40, in which each of said pillars has at least two of said one or more in-pillar holes that partly overlap.

48. (new) The photodetector device of claim 31, in which said second doped semiconductor material comprises a laterally continuous region coupled to a plurality of said pillars.

49. (new) The photodetector device of claim 31, in which said second intermediate semiconductor material has a thickness in the 100-2,000 nm range.

50. (new) The photodetector device of claim 31, in which said solid dielectric between at least portions of sidewalls of adjacent pillars extends down to said second intermediate semiconductor material.

REMARKS

Applicant appreciates the Examiner's thorough review of the claim and the helpful suggestions for clarifications.

Claim Objections

This paper cancels original claims 1-30 and adds new claims 31-50. Applicant believes that the new claims avoid the informalities that the Office Action pointed out regarding the canceled claims.

This paper reduces the total number of claims from 30 to 20 and the number of independent claims from 4 to 2.

Double Patenting

When filing the subject application, Applicant submitted a Terminal Disclaimer over parent application Ser. No. 17/532,831 and any patent issuing therefrom. The parent application became Patent 11,309,444 B1 on which the double patenting rejection is based. Applicant believes no additional Terminal Disclaimer is needed but will submit one should the Examiner require it.

35 USC §112 Issues

Applicant submits that new claims 31-50 are supported by the original specification and, accordingly, the Section 112 issues that the Office Action raised regarding now canceled claims need not be discussed.

Claims 31-39 are supported mainly by the example of Figs. 5A and 5B. For the Examiner's convenience, this paper attaches a version of these claims indicating examples of support in figures and paragraphs of the original application.

Claims 40-50 are supported mainly by the example of Figs. 7A and 7B. For the Examiner's convenience, this paper attaches a version of claim 40 indicating examples of support in figures and paragraphs of the original application. Claims 41-48 are like claims depending on claim 31 except that they depend on claim 41 so examples of support are not duplicated. Examples of support are indicated for claims 49 and 50.

Applicant notes that the original specification explains in paragraph 0071 that "individual features of one or several of the specific embodiments described herein can be used in combination with features or [sic, of] other described embodiments," and that the identified examples of support are just that – examples – and other support can be found in other figures and paragraphs in the original application.

If the Examiner finds that further clarifications may help or that a phone call may otherwise help expedite prosecution, Application invites the Examiner to telephone the undersigned representative.

If a petition for an extension of time is required to make this response timely, this paper should be taken as such a petition. The Patent Office is hereby authorized to charge any required fees in connection with this paper, and to credit any overpayment, to our Deposit Account No. 600125.

Respectfully Submitted,

WISSING MILLER LLP
Attorney for Applicants

By: /Ivan S. Kavrukov/
Ivan S. Kavrukov
Reg. No. 25,161
Tel.: (917) 945-0121

Attachment: Claims with indicated examples of support.

Attachment: Claims 31-50 with inserted non-limiting examples of support in the original application:

31.(new) A photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar holes comprising:

a laterally extending array of pillars that have rectangular cross-sections in a horizontal plane (¶132: "the shape of the pillars can be … rectangle") and are elongated in an up-down direction (Fig. 5B);

wherein said array of pillars comprises:

a first doped semiconductor material (510);

an intermediate semiconductor material (I-layer 508); and

solid dielectric (522) between at least portions of sidewalls of adjacent pillars of said array of pillars;

a second doped semiconductor material (506);

wherein:

the intermediate semiconductor material is between said first and second doped semiconductor materials;

the first and second doped semiconductor materials are doped to opposite semiconductor types (P, N);

the intermediate semiconductor material is less doped than at least one of the first and second doped semiconductor materials and the degree of doping is the same or different for different positions in the intermediate semiconductor material; and

each of the first and second doped semiconductor materials and said intermediate semiconductor material comprises Si (Fig. 5B);

one or more deliberately formed in-pillar holes with solid dielectric therein (Fig. 49 – "pillar with hole;" ¶122: "Planerization (filler step) using . . . dielectrics");

top and bottom electrical contacts (526, 528, 530) electrically coupled with said array of pillars, wherein said photodetector device is

configured to respond to light photons incident on said array of pillars by photo-generated charge carriers therein; and

a base dielectric region (504) that is below the array of pillars and comprises substantially solid dielectric material;

wherein the pillars of said array of pillars:

are laterally spaced center to center by no more than 10,000 nanometers (Figs. 43-46: "C-C 100-10,000 nm"); and

have up-down lengths of said intermediate semiconductor material in the range of 100-5000 nanometers (¶ 115: "from 0.1 to 5 micrometers");

wherein at least said pillars, in-pillar holes, and solid dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars increase photon absorption of said device of incident light by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said one or more in-pillar holes (¶97);and

wherein said array of pillars is monolithically integrated in or on said semiconductor substrate with electronic circuits that include active elements for signal processing and transmission (Provisional 61/834,873 filed June 13, 2013 and incorporated by reference in subject application in ¶ 0001: See sentence bridging pages 1 and 2: "the detector array can be monolithically integrated with Si electronic devices such as bipolar transistors, CMOS . . . (ASIC) for signal processing, storage, signal conditioning, and transmission;" see also ¶ 82 of the subject application).

32. (new) The photodetector device of claim 31, in which the top electrical contact is a transparent, laterally continuous region that is electrically coupled to a plurality of said pillars (¶ 146: "transparent conducting oxide").

33. (new) The photodetector device of claim 31, in which each of said pillars has a plurality of said one or more in-pillar holes (¶ 232: "hole(s) can exist in a pillar").

34. (new) The photodetector device of claim 31, in which each of said pillars has only one of said one or more in-pillar holes (Fig. 49: "Pillar with hole").

35. (new) The photodetector device of claim 31, in which in which said one or more in-pillar holes extend to a depth in the range of 100-10,000 nanometers (¶ 231: "the holes have … depths ranging from 1 to 10 microns.").

36. (new) The photodetector device of claim 31, in which said one or more in-pillar holes extend into said intermediate semiconductor material (¶ 198: "The microstructured holes 2722 (or space around pillars) … can be partially into the 'I' layer.").

37. (new) The photodetector device of claim 31, in which said one or more in-pillar holes are pyramid-shaped (¶ 234: "holes … shapes such as pyramids").

38. (new) The photodetector device of claim 31, in which each of said pillars has at least two of said one or more in-pillar holes that partly overlap (Fig. 46 shows examples of partly overlapping holes).

39. (new) The photodetector device of claim 31, in which said second doped semiconductor material comprises a laterally continuous region coupled to a plurality of said pillars (Fig. 5B).

40. (new) A photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar holes comprising:

an array of pillars that have rectangular cross-sections in a horizontal plane (Fig. 7B);

wherein said array of pillars comprises at least:

a first doped semiconductor material (Figs. 7A-B: top P);

a first intermediate semiconductor material (Figs. 7A-B: upper I Si); and

solid dielectric between at least portions of sidewalls of adjacent pillars;

a second doped semiconductor material (Figs. 7A-B: lower P);

wherein the first intermediate material is between the first and second doped semiconductor materials (Fig. 7B);

a third doped semiconductor material (Figs. 7A-B: N);

wherein said first and second semiconductor materials (Figs. 7A-B: upper and lower P) are doped to a first semiconductor type and the third semiconductor material is doped to a second semiconductor type (Figs. 7A-B: N);

a second intermediate semiconductor material (Figs. 7A-B: lower I Si) between the second and third doped semiconductor materials;

wherein the first and second intermediate semiconductor materials are doped less than at least one of the first, second, and third doped semiconductor materials or are undoped;

one or more deliberately formed in-pillar holes with solid dielectric therein (Fig. 49 – "Pillar with hole;" ¶122: "Planerization (filler step) using . . . dielectrics");

first and second electrical contacts that are electrically coupled with said array of pillars and are configured for operation of said device as an avalanche photodetector responding to light incident on the array of pillars by multiplying photogenerated charge carriers therein, with a multiplication gain greater than two (¶ 0009: "gain greater than 2"); and

a base dielectric region that is under the array of pillars and comprises substantially solid dielectric material (Fig. 7A-B: Si substrate);

wherein said pillars of said array of pillars:

are spaced from each other center to center by no more than 10,000 nanometers (Figs. 43-46: "C-C 100-10,000 nm); and

have an up-down dimension of said first intermediate semiconductor material that is less than 5000 nanometers (Fig. 8: region 810 thickness 0.1 – 5 um);

wherein at least said pillars, in-pillar holes, and dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars increase photon absorption of said device of incident light by a factor of at least 1.1, at least at selected wavelength of said incident light that include visible and infrared light compared to a like device lacking said one or more in-pillar holes (¶ 0097); and

wherein said array of pillars is monolithically integrated in or on said semiconductor substrate with electronic circuits including active elements for signal processing and transmission (Provisional 61/834,873 filed June 13, 2013 and incorporated by reference in subject application in ¶ 0001: See sentence bridging pages 1 and 2: "the detector array can be monolithically integrated with Si electronic devices such as bipolar transistors, CMOS . . . (ASIC) for signal processing, storage, signal conditioning, and transmission;" see also ¶ 82 of the subject application).

41. (new) The photodetector device of claim 40, in which the top electrical contact is a transparent, laterally continuous region that is electrically coupled to a plurality of said pillars.

42. (new) The photodetector device of claim 40, in which each of said pillars has a plurality of said one or more in-pillar holes.

43. (new) The photodetector device of claim 40, in which each of said pillars has only one of said one or more in-pillar holes.

44. (new) The photodetector device of claim 40, in which in which said one or more in-pillar holes extend to a depth in the range of 100-10,000 nanometers.

45. (new) The photodetector device of claim 40, in which said one or more in-pillar holes extend into said first intermediate semiconductor material.

46. (new) The photodetector device of claim 40, in which said one or more in-pillar holes are pyramid-shaped.

47. (new) The photodetector device of claim 40, in which each of said pillars has at least two of said one or more in-pillar holes that partly overlap.

48. (new) The photodetector device of claim 31, in which said third doped semiconductor material comprises a laterally continuous region coupled to a plurality of said pillars.

49. (new) The photodetector device of claim 31, in which said second intermediate semiconductor material has a thickness in the 100-2,000 nm range (¶ 124: layer 806 is 0.1-2 μm).

50. (new) The photodetector device of claim 31, in which said solid dielectric between at least portions of sidewalls of adjacent pillars extends down to said second intermediate semiconductor material (Fig. 15C).

Electronic Acknowledgement Receipt

EFS ID:	46684411
Application Number:	17707429
International Application Number:	
Confirmation Number:	1214
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	139982
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	309-0011USDIVCIP2
Receipt Date:	23-SEP-2022
Filing Date:	29-MAR-2022
Time Stamp:	16:29:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment Copy Claims/Response to Suggested Claims	309-0011USDIVCIP2_ResponseToNonFinalOfficeAction-signed.pdf	577777 b8059319ec52a2d7c986c9cf608da254e4c3e5fd	no	14

Warnings:

Information:	
Total Files Size (in bytes):	577777

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Shih-Yuan WANG Application No.: 17/707,429 Filed: March 29, 2022 Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	Examiner: Tran Quan Hoang Ho Art Unit: 2818 **CERTIFICATE OF TRANSMISSION** I hereby certify that this correspondence is being submitted through the USPTO Electronic Filing Service addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 /Mary Ellen Finnegan/ Date: April 13, 2022 Name: Mary Ellen Finnegan

VIA EFS-Web
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

It is respectfully requested that the documents listed on the attached Information Disclosure Citation form PTO/SB/08a be considered by the Patent Examiner in connection with the above-identified application and be made of record therein.

A copy of the non-U.S. patent document is enclosed herewith, in compliance with 37 CFR 1.98.

Independent consideration and acknowledgement of the enclosed document are respectfully requested.

The Commissioner is hereby authorized to charge U.S. PTO Deposit Account 600125 any payment due and to credit any overpayment thereto.

Respectfully submitted,

/Ivan S. Kavrukov/
Ivan S. Kavrukov
Registration No. 25,161
Attorney for Applicant

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001
Attorney's Telephone No.: 917-945-0121
Attorney's E-mail: ikavrukov@wissingmiller.com

Electronic Acknowledgement Receipt

EFS ID:	46423371
Application Number:	17707429
International Application Number:	
Confirmation Number:	1214
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	139982
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	309-0011USDIVCIP2
Receipt Date:	16-AUG-2022
Filing Date:	29-MAR-2022
Time Stamp:	16:31:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$130
RAM confirmation Number	E20228FG32112554
Deposit Account	600125
Authorized User	Mary Ellen Finnegan

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	309-0011USDIVCIP2_IDSTransmittal-signed.pdf	474206 06c254f8830049fccb3eb70ad8dfcd9e587ae37e	no	1
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	309-0011USDIVCIP2_1449-signed.pdf	1247224 f0a9f2af59bc4c33c6675288c44cc3ef797e032f	no	4
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Foreign Reference	JP2002314116_FINAL.pdf	3664015 d91cced44bea24b8de96d6d3813966b16ad9dbc8	no	8
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	38065 54a54c8339ad1ab81a08a4bd0fef0e0d5c3c6a57	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	5423510		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Patent Application Fee Transmittal

Application Number:	17707429
Filing Date:	29-Mar-2022
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Attorney Docket Number:	309-0011USDIVCIP2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	2806	1	130	130
		Total in USD ($)		**130**

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17707429
Filing Date	2022-03-29
First Named Inventor	Shih-Yuan WANG
Art Unit	2818
Examiner Name	Tran Quan Hoang Ho
Attorney Docket Number	309-0011USDIVCIP2

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	2002314116	JP		2002-10-25	Seiko Epson Corp.		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17707429
	Filing Date	2022-03-29
	First Named Inventor	Shih-Yuan WANG
	Art Unit	2818
	Examiner Name	Tran Quan Hoang Ho
	Attorney Docket Number	309-0011USDIVCIP2

	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17707429
Filing Date	2022-03-29
First Named Inventor	Shih-Yuan WANG
Art Unit	2818
Examiner Name	Tran Quan Hoang Ho
Attorney Docket Number	309-0011USDIVCIP2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2022-08-16
Name/Print	Ivan S. Kavrukov	Registration Number	25,161

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Lateral semiconductor photodetector of pin structure

Abstract

PROBLEM TO BE SOLVED: To provide a PIN structure lateral semiconductor photodetector which is improved in sensitivity for detecting light without deteriorating its response speed. SOLUTION: A lateral semiconductor photodetector of PIN structure has interfaces at an I layer 15, a P layer 5, and an N layer, the interfaces are set vertical to the surface of a semiconductor substrate, light impinging on the I layer 15 is converted into a current, and the current is detected. A hole 4 is bored in a light receiving region 2 from a light receiving surface 3 to a certain point as deep as prescribed inside the I layer 15

JP2002314116A

Japan

Find Prior Art Similar

Other languages: Japanese

Inventor: Atsushi Harada, 篤 原田, Tsugio Ide, 次男 井出, Shojiro Kitamura, 翼二郎 北村

Current Assignee : Seiko Epson Corp

Worldwide applications

2001 JP

Application JP2001110168A events

2001-04-09 Application filed by Seiko Epson Corp

2001-04-09 Priority to JP2001110168A

2002-10-25 Publication of JP2002314116A

Status Withdrawn

Info: Cited by (7), Legal events, Similar documents, Priority and Related Applications

External links: Espacenet, Global Dossier, Discuss

Claims (1)

Hide Dependent ^
translated from Japanese

[Claims] 1. A lateral semiconductor light receiving device wherein an interface between an I-layer, a p-layer, and an n-layer having a PIN structure is formed perpendicular to a surface of a semiconductor substrate, and converts light incident on the I-layer into current and detects the current. A lateral semiconductor light-receiving element having a PIN structure, wherein a hole extending from the light-receiving surface to a predetermined depth of the I-layer is provided in the light-receiving region.

Description

translated from Japanese

DETAILED DESCRIPTION OF THE INVENTION

[0001]

The present invention relates to a lateral semiconductor light receiving device having a PIN structure.

[0002]

2. Description of the Related Art In a vertical photodiode in which a pn junction surface is formed parallel to a semiconductor substrate surface, light is incident on a depletion layer through a p-layer or an n-layer.
In a lateral photodiode in which the n-junction surface is formed perpendicular to the semiconductor substrate surface, light is directly incident on the depletion layer (not through the p-layer or the n-layer). For this reason, lateral photodiodes are better than vertical photodiodes.
This is advantageous in light receiving efficiency.

Conventionally, in a photodiode,
An I layer (intrinsic layer) is provided between a p layer and an n layer to increase the thickness of a depletion layer. In a vertical photodiode having such a PIN structure, the I-layer is formed to have a thickness equal to or more than the absorption length in order to increase the light receiving sensitivity. As a result, a quantum efficiency of 70% or more can be obtained at a wavelength of about 700 nm to 870 nm.

Lateral photodiode having a PIN structure (a photodiode in which an interface between an I-layer, a p-layer, and an n-layer having a PIN structure is formed perpendicular to a semiconductor substrate surface)
For example, after a region having an extremely low impurity concentration forming an I-layer is provided in a surface layer portion of a semiconductor substrate, a p-type impurity and an n-type impurity are added to respective positions of this region at predetermined intervals from an upper surface. To form a p-layer and an n-layer, and leave an I-layer between both layers

Therefore, in the case of a lateral photodiode having a PIN structure, the thickness of the I-layer (depth from the light incident surface)
In order to increase p, it is necessary to form the p-layer and the n-layer deeply. In order to form the p-layer and the n-layer deep while keeping the width of the I-layer (the distance between the p-layer and the n-layer) uniform in the thickness direction of the substrate, the p-layer and the n-layer on the substrate surface must be li is

necessary to increase the distance. When the distance between the p-layer and the n-layer on the substrate surface is increased, the width of the I-layer increases. If the width of the I-layer is large, the movement distance of electrons generated on the p-layer side of the I-layer to reach the electrode of the n-layer increases, and the response speed decreases.

Therefore, in the lateral type photodiode having the PIN structure, as a method for increasing the light receiving sensitivity, simply increasing the thickness of the I-layer (the depth from the light incident surface) cannot be simply employed. Therefore, PIN
As a method for increasing the light receiving sensitivity of the lateral type photodiode having the structure, it is effective to provide an antireflection film on the upper surface of the I-layer to increase the efficiency of incidence on the I-layer.

[0007]

However, a lateral type photodiode having a PIN structure having an antireflection film on the upper surface of the I-layer has a problem that the response speed is low when an element for receiving a high-speed signal is used. There is. SUMMARY OF THE INVENTION The present invention has been made in view of such a problem of the related art, and it is an object of the present invention to improve the light receiving sensitivity without lowering the response speed in a lateral semiconductor light receiving element having a PIN structure.

[0008]

In order to solve the above-mentioned problems, the present invention provides a semiconductor device having an I-layer having a PIN structure in which an interface between a p-layer and an n-layer is formed perpendicular to a semiconductor substrate surface. In a lateral type semiconductor light receiving element for detecting incident light by converting the light into a current, a hole extending from the light receiving surface to a predetermined depth of the i layer (a position shallower than the depths of the p layer and the n layer) is provided in the light receiving region. A lateral type semiconductor light receiving element having a PIN structure is provided.

[0009]

Embodiments of the present invention will be described below. FIG. 1 is a sectional view showing a photodiode corresponding to one embodiment of the present invention. FIG. 2 is a diagram showing an example of a planar shape when the photodiodes of this embodiment are formed in an array. FIG. 1 corresponds to a sectional view taken along line AA of FIG.

This photodiode is a lateral photodiode (semiconductor light receiving element) having a PIN structure formed perpendicular to the substrate surface of a silicon substrate (semiconductor substrate) 1 and has a light receiving region (p layer of i layer 15). A hole 4 extending in a direction perpendicular to the surface of the silicon substrate 1 from the light receiving surface 3 to a predetermined depth of the I-layer 15 is provided in a region (a region between the n-layer 5 and the n-layer 7).

On the upper surfaces of the p layer 5 and the n layer 7, a p electrode 6
And an n electrode 8 are formed. On the lower surface of the silicon substrate 1, a p-electrode 11 is formed. An element protection layer 9 made of a silicon oxide film or the like is provided on the upper surface of the silicon substrate 1 except for the positions of the electrodes 6 and 8 and the hole 4.
is formed with a predetermined thickness. This photodiode can be manufactured, for example, by the following method.

First, n is added to the surface layer of the p-type silicon substrate 1.
A well (a region having an extremely low impurity concentration) 10 is provided.
Next, a p-type impurity is added to one of the two regions of the n-well 10 at a predetermined interval, and an n-type impurity is added to the other, and diffused. As a result, the p layer 5 and the n layer 7 are formed in the n well 10, and the portion between the p layer 5 and the n layer 7 of the n well 10 remains as the I layer 15. Next, after forming the electrodes 6 and 8 on the p-layer 5 and the n-layer 7, the element protection layer 9 is formed.

Next, a focused ion beam processing apparatus (FI
Using B), a portion of the upper surface of the silicon substrate 1 sandwiched between the electrodes 6 and 8 is irradiated with an ion beam, and the element protection layers 9 and I are irradiated.
By etching the layer 15, a hole 4 extending in the thickness direction of the silicon substrate 1 from the light receiving surface 3 to a predetermined depth of the i layer 15 (a position shallower than the depths of the p layer 5 and the n layer 7) is formed.

Here, the dimension of the hole 4 in the direction between the p layer 5 and the n layer 7 is determined between the hole 4 and the p layer 5 and between the hole 4 and the n layer 7. is set to the dimension where exists. When the light receiving surface 3 between each pair of electrodes is large, it is preferable to provide a plurality of holes 4 in the light receiving surface 3 as shown in FIG. in this case, for example, the width W of the electrodes 6 and 8
1 is 1 μm, the interval W2 between the electrodes 6 and 8 is 2 to 4 μm, and the hole 4
is 2 to 4 μm, and the diameter of the hole 4 is 1 μm.

In this photodiode, a power supply is connected between the n-electrode 8 in contact with the upper surface of the n-layer 7 and the p-electrode 11 on the lower surface of the substrate 1 with the n-layer 7 side being positive and a reverse bias voltage applied. Then, by connecting the p-electrode 6 in contact with the upper surface of the p-layer 5 to the output circuit, light incident on the I-layer 15 from the light receiving surface 3 can be converted into a current and detected. Also,
In this photodiode, the light (partially shown by a two-dot chain line in FIG. 1) that has entered the hole 4 from the light receiving surface 3 directly enters the light receiving region 2 from the bottom or side surface of the hole 4 and By being reflected on the side surface, the light is incident on the light receiving region 2 from the bottom surface to the side surface, or is incident on the light receiving region 2 from the side surface toward the opposing side surface. Therefore, the light receiving efficiency in the light receiving region 2 is higher than in the case where there is no hole 4.

If the light receiving surface 3 is simply enlarged without providing the hole 4 in order to increase the light receiving area, it takes a long time for electrons generated on the p layer side of the I layer to reach the electrode of the n layer. As the parasitic capacitance increases, the response speed decreases. In contrast, in this photodiode, By providing the hole 4, the light receiving area is larger by the side surface of the hole 4 than when no hole 4 is provided. Therefore, in this photodiode, electrons generated on the p-layer side of the I-layer are n
The movement time until reaching the electrode of the layer is not longer than when the light receiving surface 3 is the same size and the hole 4 is not provided.
The parasitic capacitance of the photodiode is smaller than that in the case where the light receiving surface 3 has the same size and the hole 4 is not provided. For these reasons, according to this photodiode, the light receiving area can be increased and the light receiving efficiency can be increased without reducing the response speed.

Further, since the photodiode has the hole 4, the intensity of the electric field applied to the peripheral portion of the hole 4 of the I-layer 15 is locally increased. This allows
Since holes and electrons generated by absorbing light in the peripheral portion of the hole 4 of the I-layer 15 can move at high speed through the I-layer 15,
The response speed is faster than the case without the hole 4. Therefore, according to this photodiode, by providing the hole 4, the light receiving efficiency in the light receiving region 2 is increased, the light receiving sensitivity is improved, and the response speed is also increased.

in this embodiment, a lateral type photodiode having a PIN structure is described. However, the lateral type semiconductor light receiving element having a PIN structure of the present invention is not limited to this. It is also applied to the lateral type phototransistor and the like.

[0019]

As described above, according to the lateral semiconductor light receiving device having the PIN structure of the present invention, the light receiving sensitivity can be improved without lowering the response speed.

[Brief description of the drawings]

FIG. 1 is a cross-sectional view showing a photodiode corresponding to an embodiment of the present invention, and is a view corresponding to a cross-sectional view taken along line AA of FIG.

FIG. 2 is a diagram showing an example of a planar shape when the photodiodes of FIG. 1 are formed in an array.

[Explanation of symbols]

REFERENCE SIGNS LIST 1 silicon substrate (semiconductor substrate) 10 n-well 11 p-electrode 15 I-layer 2 light-receiving area 3 light-receiving surface 4 hole 5 p-layer 6 p-electrode 7 n-layer 8 n-electrode 9 element protection layer

---------- Continuing on the front page (72) Inventor Shojiro Kitamura 3-3-5 Yamato, Suwa-shi, Nagano F-term (reference) in Seiko Epson Corporation 5F049 MA04 MB03 NA01 NA03 NA15 PA14 PA20 QA01 QA20 SZ13

Cited By (7)

Publication number	Priority date	Publication date	Assignee	Title
WO2006129427A1 *	2005-05-31	2006-12-07	Sharp Kabushiki Kaisha	Light sensor and display device
JP2007214405A *	2006-02-10	2007-08-23	Epson Imaging Devices Corp	Light receiving apparatus, electro-optical apparatus, and electronic appliance
JP2009130278A *	2007-11-27	2009-06-11	Hitachi Displays Ltd	Optical sensor device and image display device
US7936648B2	2004-06-23	2011-05-03	Lg Electronics Inc.	Method and apparatus for overwriting data on recording medium and the recording medium
JP2011238942A *	2002-12-18	2011-11-24	Noblepeak Vision Corp	Semiconductor device having reduced defect of active region, and unique contact scheme
JP2015056651A *	2013-09-13	2015-03-23	株式会社東芝	Light receiving element and optically coupled insulating device
JP2020537816A *	2017-07-21	2020-12-24	ダブリュアンドダブリュセンスデバイシーズ、インコーポレイテッドW&Wsens Devices, Inc.	Microstructure improved absorption photosensitizer

Family To Family Citations

* Cited by examiner, † Cited by third party, ‡ Family to family citation

Similar Documents

Publication	Publication Date	Title
US8916945B2	2014-12-23	Semiconductor light-detecting element
EP2403012B1	2019-03-27	Photodiode and photodiode array
US7576371B1	2009-08-18	Structures and methods to improve the crosstalk between adjacent pixels of back-illuminated photodiode arrays
US20220005848A1	2022-01-06	Photodetector
US20130001729A1	2013-01-03	High Fill-Factor Laser-Treated Semiconductor Device on Bulk Material with Single Side Contact Scheme
JP3912024B2	2007-05-09	PIN type lateral type semiconductor photo detector
JP2006060183A	2006-03-02	Semiconductor light receiving device and ultraviolet sensor
JP2002314118A	2002-10-25	Photodetector
JP4522531B2	2010-08-11	Semiconductor energy detector
KR960009395B1	1996-04-21	Photo-sensing device
US10636993B2	2020-04-28	Tilted photodetector cell
JP2002314118A	2002-10-25	Lateral semiconductor photodetector of pin structure

US6798001B2	2004-09-28	Semiconductor device having photo diode with sensitivity to light of different wavelengths
JP2773990B2	1998-07-09	Light detection device
US6809981B1	2004-10-26	Short-wavelength photodiode of enhanced sensitivity with low leak current and method of manufacturing photodiode
JP2000252512A5	2005-11-24	
KR100676783B1	2007-02-23	UV detector having NIP Structure
Hinckley et al.	2002	Modelling of device structure effects on electrical crosstalk in back illuminated CMOS compatible photodiodes
JP2000252512A	2000-09-14	Pin photo-diode
KR100424366B1	2004-03-24	A Photodiode With A Diffusion-Layer Of Dispersion-Distribution Pattern And Fabrication Method Thereof And A Substrate And An Electronic Machine Thereby
US8829423282	2012-10-23	High quantum efficiency optical detectors
US20210234057A1	2021-07-29	Single photon avalanche diode device
JPH10190041A	1998-07-21	Photodiode
JP2020161739A	2020-10-01	Photodetector
JP4951552B2	2012-06-13	Semiconductor photodetection device

Priority And Related Applications

Priority Applications (1)

Application	Priority date	Filing date	Title
JP2001110168A	2001-04-09	2001-04-09	Lateral semiconductor photodetector of pin structure

Applications Claiming Priority (1)

Application	Filing date	Title
JP2001110168A	2001-04-09	Lateral semiconductor photodetector of pin structure

Legal Events

Date	Code	Title	Description
2008-07-01	A300	Withdrawal of application because of no request for examination	**Free format text**: JAPANESE INTERMEDIATE CODE: A300 **Effective date**: 20080701

Concepts

machine-extracted

Download Filter table

Name	Image	Sections	Count	Query match
semiconductor		title,claims,abstract,description	22	0.000
substrate		claims,abstract,description	22	0.000
sensitivity		abstract,description	7	0.000
deteriorative		abstract	1	0.000

Show all concepts from the description section

Data provided by IFI CLAIMS Patent Services

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号
特開2002－314116
（P2002－314116A）
(43)公開日　平成14年10月25日(2002.10.25)

(51)Int.Cl.⁷	識別記号	ＦＩ	ﾃｰﾏｺｰﾄﾞ(参考)
Ｈ０１Ｌ　31/10		Ｈ０１Ｌ　31/10	Ａ　５Ｆ０４９

審査請求　未請求　請求項の数１　ＯＬ　（全　４　頁）

(21)出願番号　特願2001－110168(P2001－110168)

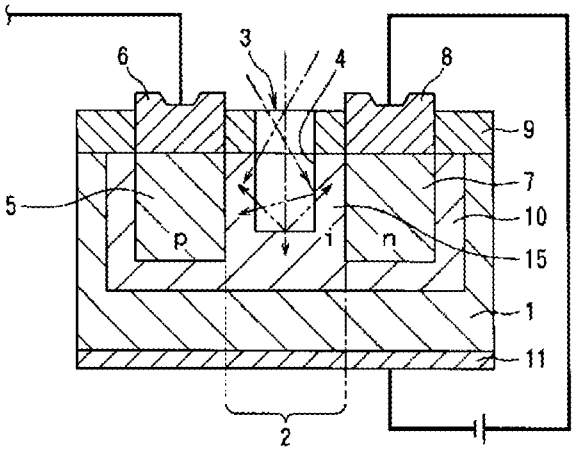
(22)出願日　平成13年４月９日(2001.4.9)

(71)出願人　000002369
セイコーエプソン株式会社
東京都新宿区西新宿２丁目４番１号
(72)発明者　原田　篤
長野県諏訪市大和３丁目３番５号　セイコーエプソン株式会社内
(72)発明者　井出　次男
長野県諏訪市大和３丁目３番５号　セイコーエプソン株式会社内
(74)代理人　100095728
弁理士　上柳　雅誉　（外１名）

最終頁に続く

(54)【発明の名称】　ＰＩＮ構造のラテラル型半導体受光素子

(57)【要約】　（修正有）
【課題】応答速度を低下させることなく受光感度を向上させたＰＩＮ構造のラテラル型半導体受光素子を提供する。
【解決手段】ＰＩＮ構造のｉ層１５とｐ層５とｎ層７との界面が半導体基板面に対して垂直に形成され、ｉ層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、受光領域２に、受光面３からｉ層１５の所定深さまで延びる穴４を設けた。



1

【特許請求の範囲】

【請求項１】　ＰＩＮ構造のｉ層とｐ層およびｎ層との界面が半導体基板面に対して垂直に形成され、ｉ層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、

受光領域に、受光面からｉ層の所定深さまで延びる穴を設けたことを特徴とするＰＩＮ構造のラテラル型半導体受光素子。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、ＰＩＮ構造のラテラル型半導体受光素子に関する。

【０００２】

【従来の技術】ｐｎ接合面が半導体基板面に対して平行に形成されている縦型フォトダイオードでは、ｐ層またはｎ層を通して空乏層に光が入射されるのに対して、ｐｎ接合面が半導体基板面に対して垂直に形成されているラテラル型フォトダイオードでは、空乏層に直接（ｐ層やｎ層を介さずに）光が入射される。そのため、ラテラル型フォトダイオードは縦型フォトダイオードよりも、受光効率の点で有利である。

【０００３】従来より、フォトダイオードにおいては、ｐ層とｎ層との間にｉ層（真性層）を設けて、空乏層を厚くすることが行われている。このようなＰＩＮ構造を有する縦型フォトダイオードでは、受光感度を高くするために、ｉ層を吸収長以上の厚さに形成することが行われている。これにより、波長７００ｎｍ～８７０ｎｍ前後において、７０％以上の量子効率が得られるようになる。

【０００４】ＰＩＮ構造のラテラル型フォトダイオード（ＰＩＮ構造のｉ層とｐ層およびｎ層との界面が半導体基板面に対して垂直に形成されたフォトダイオード）は、例えば、ｉ層をなす不純物濃度の極めて薄い領域を半導体基板の表層部に設けた後、この領域の所定間隔を開けた各位置に、上面からｐ型不純物及びｎ型不純物をそれぞれ添加して拡散させることによりｐ層及びｎ層を形成し、両層の間をｉ層として残すことによって作製される。

【０００５】そのため、ＰＩＮ構造のラテラル型フォトダイオードの場合にｉ層の厚さ（光入射面からの深さ）を大きくしようとすると、ｐ層及びｎ層を深く形成する必要がある。基板の厚さ方向でｉ層の幅（ｐ層とｎ層との距離）を均一に保持しながら、ｐ層及びｎ層を深く形成するためには、基板表面でのｐ層とｎ層との距離を大きくとる必要がある。基板表面でのｐ層とｎ層との距離を大きくとるとｉ層の幅が大きくなる。ｉ層の幅が大きいと、ｉ層のｐ層側で生じた電子がｎ層の電極に達するまでの移動距離が長くなって、応答速度が遅くなる。

【０００６】したがって、ＰＩＮ構造のラテラル型フォトダイオードでは、受光感度をより高くする方法として、ｉ層の厚さ（光入射面からの深さ）を大きくすることを単純に採用することができない。そのため、ＰＩＮ構造のラテラル型フォトダイオードの受光感度をより高くする方法としては、ｉ層の上面に反射防止膜を設けてｉ層への入射効率を高くすることが有効である。

2

【０００７】

【発明が解決しようとする課題】しかしながら、ｉ層の上面に反射防止膜を有するＰＩＮ構造のラテラル型フォトダイオードには、高速の信号を受光する素子とした場合に応答速度が低くなるという問題点がある。本発明は、このような従来技術の問題点に着目してなされたものであり、ＰＩＮ構造のラテラル型半導体受光素子において、応答速度を低下させることなく受光感度を向上させることを課題とする。

【０００８】

【課題を解決するための手段】上記課題を解決するために、本発明は、ＰＩＮ構造のｉ層とｐ層およびｎ層との界面が半導体基板面に対して垂直に形成され、ｉ層に入射された光を電流に変換して検出するラテラル型半導体受光素子において、受光領域に、受光面からｉ層の所定深さ（ｐ層およびｎ層の深さより浅い位置）まで延びる穴を設けたことを特徴とするＰＩＮ構造のラテラル型半導体受光素子を提供する。

【０００９】

【発明の実施の形態】以下、本発明の実施形態について説明する。図１は本発明の一実施形態に相当するフォトダイオードを示す断面図である。図２は、この実施形態のフォトダイオードがアレイ状に形成されている場合の平面形状の一例を示す図である。図１は図２のＡ－Ａ線断面図に相当する。

【００１０】このフォトダイオードは、ＰＩＮ構造がシリコン基板（半導体基板）１の基板面に対して垂直に形成されたラテラル型フォトダイオード（半導体受光素子）であり、受光領域（ｉ層１５のｐ層５とｎ層７とで挟まれた領域）２に、受光面３からｉ層１５の所定深さまで、シリコン基板１面に垂直に延びる穴４が設けてある。

【００１１】ｐ層５およびｎ層７の上面には、ｐ電極６およびｎ電極８がそれぞれ形成されている。シリコン基板１の下面にはｐ電極１１が形成されている。また、シリコン基板１の上面の両電極６，８および穴４の位置を除いた部分に、シリコン酸化膜等からなる素子保護層９が所定の厚さで形成されている。このフォトダイオードは、例えば以下の方法で作製できる。

【００１２】先ず、ｐ型のシリコン基板１の表層部にｎウエル（不純物濃度の極めて薄い領域）１０を設ける。次に、ｎウエル１０の所定間隔を開けた２つの領域の一方にｐ型不純物を、他方にｎ型不純物をそれぞれ添加して拡散させる。これにより、ｎウエル１０にｐ層５及びｎ層７が形成され、ｎウエル１０のｐ層５とｎ層７との

間の部分がｉ層１５として残る。次に、ｐ層５及びｎ層７の上に電極６，８を形成した後、素子保護層９を形成する。

【００１３】次に、集束イオンビーム加工装置（ＦＩＢ）を用い、シリコン基板１上面の両電極６，８で挟まれた部分にイオンビームを照射して、素子保護層９とｉ層１５をエッチングすることにより、受光面３からｉ層１５の所定深さ（ｐ層５およびｎ層７の深さより浅い位置）まで、シリコン基板１の厚さ方向に延びる穴４を開ける。

【００１４】ここで、穴４のｐ層５－ｎ層７間方向の寸法は、穴４とｐ層５との間および穴４とｎ層７との間にそれぞれ所定厚さのｉ層１５が存在する寸法に設定する。また、各電極対間の受光面３が大きい場合には、図２に示すように、受光面３内に複数の穴４を設けることが好ましい。この場合には、例えば、電極６，８の幅Ｗ１を１μｍ、電極６，８の間隔Ｗ２を２～４μｍ、穴４のピッチＫを２～４μｍ、穴４の直径を１μｍとする。

【００１５】このフォトダイオードは、ｎ層７の上面に接触するｎ電極８と基板１の下面のｐ電極１１との間に、ｎ層７側を正として電源を接続して逆バイアス電圧を付与し、ｐ層５の上面に接触するｐ電極６を出力回路に接続することにより、受光面３からｉ層１５に入射された光を電流に変換して検出することができる。また、このフォトダイオードでは、受光面３から穴４内に入射された光（一部を図１に２点鎖線で表示）は、穴４の底面や側面から受光領域２に直接入射するとともに、底面や側面で反射されることで、底面から側面に向かって受光領域２に入射されたり、側面から対向する側面に向かって受光領域２に入射されたりする。そのため、穴４が無い場合よりも受光領域２での受光効率が高くなる。

【００１６】受光面積を大きくするために穴４を設けず単純に受光面３を大きくした場合には、ｉ層のｐ層側で生じた電子がｎ層の電極に達するまでの移動時間が長くなるとともに、寄生容量が大きくなるため、応答速度が遅くなる。これに対して、このフォトダイオードでは、穴４を設けることで、穴４が無い場合よりも穴４の側面の分だけ受光面積が大きくなっている。そのため、このフォトダイオードでは、ｉ層のｐ層側で生じた電子がｎ層の電極に達するまでの移動時間が、受光面３が同じ大きさで穴４を設けない場合よりも長くなることはない。また、このフォトダイオードの寄生容量は、受光面３が同じ大きさで穴４を設けない場合よりも小さくなる。これらのことから、このフォトダイオードによれば、応答速度を遅くすることなく、受光面積を大きくして受光効率を高くすることができる。

【００１７】さらに、このフォトダイオードは、穴４を有することによって、ｉ層１５の穴４の周囲部分に掛かる電界強度が局所的に大きくなっている。これにより、ｉ層１５の穴４の周囲部分で光を吸収して発生した正孔と電子はｉ層１５を高速で移動することができるため、穴４の無い場合と比較して応答速度が速くなる。したがって、このフォトダイオードによれば、穴４を設けることによって、受光領域２での受光効率が高くなって受光感度が向上するとともに、応答速度も高くなる。

【００１８】なお、この実施形態では、ＰＩＮ構造のラテラル型フォトダイオードについて説明しているが、本発明のＰＩＮ構造のラテラル型半導体受光素子はこれに限定されず、ベースとコレクタの部分がＰＩＮ構造になっているラテラル型フォトトランジスタ等にも適用される。

【００１９】

【発明の効果】以上説明したように、本発明のＰＩＮ構造のラテラル型半導体受光素子によれば、応答速度を低下させることなく受光感度を向上させることができる。

【図面の簡単な説明】

【図１】本発明の一実施形態に相当するフォトダイオードを示す断面図であって、図２のＡ－Ａ線断面図に相当する図である。

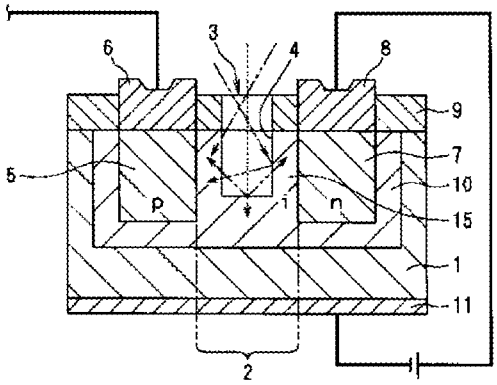
【図２】図１のフォトダイオードがアレイ状に形成されている場合の平面形状の一例を示す図である。

【符号の説明】

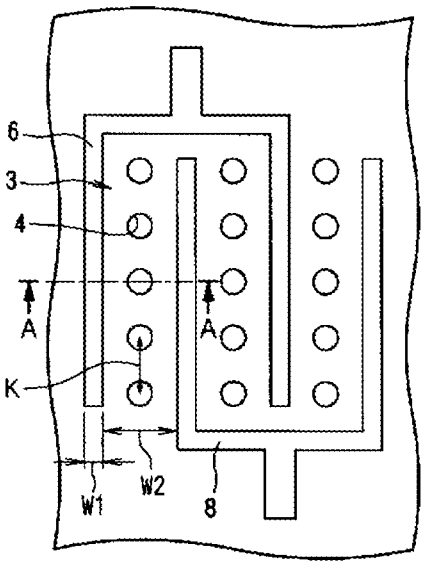
１　シリコン基板（半導体基板）
１０　ｎウエル
１１　ｐ電極
１５　ｉ層
２　受光領域
３　受光面
４　穴
５　ｐ層
６　ｐ電極
７　ｎ層
８　ｎ電極
９　素子保護層

Samsung Exhibit 1003, Page 189 of 516

【図１】



【図２】



フロントページの続き

(72)発明者　北村　昇二郎
長野県諏訪市大和３丁目３番５号　セイコーエプソン株式会社内

Ｆターム(参考)　5F049 MA04 MB03 NA01 NA03 NA15 PA14 PA20 QA01 QA20 SZ13

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/707,429	03/29/2022	Shih-Yuan WANG	309-0011USDIVCIP2

CONFIRMATION NO. 1214

139982
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

PUBLICATION NOTICE

OC000000135621187

Title:MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Publication No.US-2022-0246775-A1
Publication Date:08/04/2022

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	2	"17707429"	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/15 03:24 PM
L2	6	("20110156195"|"20120012741"|"20120153127"|"20180012918"|"20180102442"|"20190166317").PN.	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/15 03:25 PM
L3	28	(W&WSENS DEVICES).as,aanm.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	WITH	ON	ON	2022/06/15 03:26 PM
L4	1385	(Shih-Yuan WANG).in.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT;	WITH	ON	ON	2022/06/15 03:26 PM

Samsung Exhibit 1003, Page 192 of 516

			IBM_TDB)				
L5	457	(Shih-Ping WANG).in.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	WITH	ON	ON	2022/06/15 03:26 PM
L7	285723	(H01L31/035272 OR G02B6/122 OR G02B6/136 OR H01L23/66 OR H01L31/02005 OR H01L31/02016 OR H01L31/02019 OR H01L31/022408 OR H01L31/022475 OR H01L31/02327 OR H01L31/02363 OR H01L31/024 OR H01L31/028 OR H01L31/0284 OR H01L31/0304 OR H01L31/03046 OR H01L31/0312 OR H01L31/035209 OR H01L31/035227 OR H01L31/035281 OR H01L31/036 OR H01L31/054 OR H01L31/0745 OR H01L31/075 OR H01L31/077 OR H01L31/105 OR H01L31/1055 OR H01L31/107 OR H01L31/1075 OR H01L31/1804 OR H01L31/1808 OR H01L31/1812 OR H01L31/184 OR H01L31/1844 OR G02B2006/12097 OR G02B2006/12176 OR H01L2223/6627 OR Y02E10/52 OR Y02E10/548).cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/15 03:32 PM
L8	51993616	pillar column mesa post	(US-PGPUB; USPAT;	OR	ON	ON	2022/06/15

Samsung Exhibit 1003, Page 193 of 516

		rod	USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				06:42 PM
L9	1	"11309444".pn.	(USPAT)	AND	ON	ON	2022/06/15 06:44 PM
L10	30838630	dielectric insulat$3 oxide	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/15 08:20 PM
L11	48494892	spac$3 pitch	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/15 08:22 PM
L12	14061155	pin! (p ADJ i ADJ n)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS,	OR	ON	ON	2022/06/15 08:23 PM

			IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L13	15	(3 OR 4 OR 5) 7 (8 near5 10) (8 near5 11)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/15 08:24 PM
L14	655	7 (8 near5 10) (8 near5 11)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/15 08:45 PM
L15	52161205	pillar column mesa post rod nanowire nanorod	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/15 08:53 PM

Samsung Exhibit 1003, Page 195 of 516

L16	28	(3 OR 4 OR 5) 7 (15 near5 10) (15 near5 11)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/15 08:54 PM
L17	1064	7 (15 near5 10) (15 near5 11)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/15 08:56 PM
L18	20	("2011/0309331").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2022/06/15 10:46 PM
L19	10899934	infrared ir!	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/06/15 10:54 PM
L20	385	7 (15 near5 10) (15 near5 11) 19	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	AND	ON	ON	2022/06/15 11:01 PM

			EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L21	12	("7525170" | "9000492" | "10411053" | "10522582" | "20050145779" | "20120153416" | "20150349206" | "20160240579" | "20170141153" | "20180102442" | "20200006407" | "20200006416").pn. OR ("11309444").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	AND	ON	ON	2022/06/16 08:12 PM
L22	31	(Artificial Intelligence) More Like: US-11309444-B1 Text: (JP-2020537816-A OR US-20180102442-A1 OR US-9496435-B2 OR US-20220102563-A1 OR CN-105556680-B OR US-20160126381-A1 OR US-10622498-B2 OR US-20190288132-A1 OR US-20210242354-A1 OR WO-2014190189-A9 OR WO-2014190189-A2 OR EP-3000134-A2 OR US-20160254407-A1 OR JP-2016526295-A OR EP-3000134-B1 OR US-9818893-B2 OR US-20170194522-A1 OR JP-6602751-B2 OR KR-102358584-B1 OR US-20210313483-A1).did.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	AND	ON	ON	2022/06/16 08:13 PM
L24	10	("11309444" "11121271" "10446700" "10622498" "10468543" "9496435" "9530905" "10700225" "9525084"	(USPAT)	OR	ON	ON	2022/06/17 04:37 PM

Samsung Exhibit 1003, Page 197 of 516

		"9818893").pn.					
L25	2	17/532831	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/17 04:39 PM
L26	2	17/182954	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/17 04:40 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	47695	(H01L31/035272 OR G02B6/122 OR G02B6/136 OR H01L23/66 OR H01L31/02005 OR H01L31/02016 OR H01L31/02019 OR H01L31/022408 OR H01L31/022475 OR H01L31/02327 OR H01L31/02363 OR H01L31/024 OR H01L31/028 OR H01L31/0284 OR H01L31/0304 OR H01L31/03046 OR H01L31/0312 OR H01L31/035209 OR H01L31/035227 OR H01L31/035281 OR H01L31/036 OR H01L31/054 OR H01L31/0745 OR H01L31/075 OR H01L31/077 OR H01L31/105 OR H01L31/1055 OR H01L31/107 OR H01L31/1075 OR H01L31/1804 OR H01L31/1808 OR H01L31/1812 OR H01L31/184 OR H01L31/1844 OR G02B2006/12097 OR G02B2006/12176 OR H01L2223/6627 OR Y02E10/52 OR Y02E10/548).cpc.	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/16 07:56 PM
N2	1014266	(pillar column mesa post rod nanowire nanorod).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/16 07:56 PM
N3	1506210	(dielectric insulat$3 oxide).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/16 07:58 PM
N4	2514245	(spac$3 pitch).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/16

Samsung Exhibit 1003, Page 198 of 516

							08:10 PM
N5	196222	(infrared ir!).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/06/16 08:10 PM
N6	5	N1 (N2 near5 N3) (N2 near5 N4) N5	(US-PGPUB; USPAT)	AND	ON	ON	2022/06/16 08:11 PM

Skin effect photon-trapping enhancement in infrared photodiodes

H Ge, R Xie, Y Chen, P Wang, Q Li, Y Gu, J Guo... - Optics ..., 2021 - opg.optica.org

... The preparation process of the **dielectric-filled** structure is ... We found that the optical properties of the **dielectric-filled** structure ... The quantum efficiency of the **dielectric-filled** structure is ...

☆ Save 99 Cite Cited by 3 Related articles All 4 versions »

SiGe quantum dots over Si pillars for visible to near-infrared broadband photodetection

WT Lai, PH Liao, AP Homyk... - IEEE Photonics ..., 2013 - ieeexplore.ieee.org

... SiGe QD/Si **pillar photodiodes** (Fig. 2(a)) suggests SiGe QDs over Si ... flatness of the Si **pillars** by taking **full** advantage of the ... quantum dots in the gate **dielectrics**," Appl. Phys. Lett., vol. ...

☆ Save 99 Cite Cited by 14 Related articles All 6 versions

Silicon nitride light pipes for image sensors

T Tut, P Duane, NY Winnie, M Wober... - ... Devices: Infrared ..., 2010 - spiedigitallibrary.org

... of silicon nitride **pillars**, and the fabrication of **photodiodes**. ... **dielectric** region between the microlenses and **photodiodes** of a ... Because of the demanding nature of **filling** a cylindrical hole ...

☆ Save 99 Cite Cited by 4 Related articles All 6 versions

HgCdTe mid-Infrared photo response enhanced by monolithically integrated meta-lenses

F Li, J Deng, J Zhou, Z Chu, Y Yu, X Dai, H Guo... - Scientific reports, 2020 - nature.com

... For the inter-**pillar** distance to be 2 μm in our design, the ... In this work, we propose to monolithically integrate a **dielectric** ... on **full** meta-lens simulation with the center-to-center ...

☆ Save 99 Cite Cited by 22 Related articles All 8 versions »

Tunable visible and near-IR emission from sub-10 nm etched single-crystal Si nanopillars

SS Walavalkar, CE Hofmann, AP Homyk, MD Henry... - Nano ..., 2010 - ACS Publications

... **dielectric** layer into the nanocrystals where they recombine. ... in **pillar** size while the y error bars show the **full** width half-... a narrower size distribution of silicon **pillar** cores, an effect we ...

☆ Save 99 Cite Cited by 105 Related articles All 12 versions »

New concepts in infrared photodetector designs

P Martyniuk, J Antoszewski, M Martyniuk... - Applied Physics ..., 2014 - aip.scitation.org

... of electrons, and low **dielectric** constant. The extremely small ... to the **photodiodes** for passive **IR** imaging applications and is ... structures with **pillars** and holes of varying volume **fill** factors. ...

☆ Save 99 Cite Cited by 227 Related articles All 2 versions »

Ultrafast all-optical tuning of direct-gap semiconductor metasurfaces

MR Shcherbakov, S Liu, VV Zubyuk, A Vaskin... - Nature ..., 2017 - nature.com

... The **pillars** are situated on a bulk GaAs substrate that we ... (Avesta ASP-**IR**) coupled to an InGaAs **photodiode**; the spectral ... For the complex **dielectric** permittivity function of GaAs we used ...

☆ Save 99 Cite Cited by 248 Related articles All 20 versions

Nature-inspired chiral metasurfaces for circular polarization detection and full-Stokes polarimetric measurements

A Basiri, X Chen, J Bai, P Amrollahi... - Light: Science & ..., 2019 - nature.com

... We choose **dielectric** metasurfaces composed of silicon ... adjusting the **pillar** height and the silicon volume **filling** factor (... fabricated, we used FTIR with an **infrared** microscope to build the ...

☆ Save 99 Cite Cited by 81 Related articles All 14 versions »

HOT infrared photodetectors

P Martyniuk, A Rogalski - Opto-Electronics Review, 2013 - degruyter.com

... of electrons, and low **dielectric** constant. The extremely small ... structures with **pillars** and holes of varying volume **fill** factors. ... of HgCdTe **photodiodes** operated in a long wavelength **IR** ...

☆ Save 99 Cite Cited by 104 Related articles All 9 versions »

Metalens array for InGaAs/InP avalanche photodiodes at optical-communication wavelengths

H Zhang, Y Zhao, Q Li, Y Tian, W Ding, Z Lin… - Optics …, 2022 - Elsevier

… The **dielectric** metalens composed of high refractive index … nm, is taken as the height h of the **pillar** in this work, which can … For **infrared** APDs, one of the key figure of merit is detectivity D …

☆ Save 99 Cite Cited by 1 Related articles All 2 versions

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/707,429	03/29/2022	Shih-Yuan WANG	309-0011USDIVCIP2	1214

139982 7590 06/24/2022

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER
HO, HOANG QUAN TRAN

ART UNIT	PAPER NUMBER
2818	

NOTIFICATION DATE	DELIVERY MODE
06/24/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

Office Action Summary	Application No. 17/707,429	Applicant(s) WANG et al.	
	Examiner Hoang-Quan Ho	Art Unit 2818	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 31 March 2022.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-30 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-30 is/are rejected.

8) ☑ Claim(s) 1,5,7-8,23,27 and 30 is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 29 March 2022 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 04/13/2022,04/28/2022.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

The drawings were received on March 29, 2022. These drawings are accepted.

Terminal Disclaimer

The eleven terminal disclaimers filed on March 29, 2022 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of the indicated patents/applications have been reviewed and are accepted. The terminal disclaimers have been recorded.

Information Disclosure Statement

The information disclosure statements (IDS) submitted on April 13, 2022 and April 28, 2022 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Objections

Claims 1, 5, 7, 8, 23, 27, and 30 are objected to because of the following informalities:

Claim 1: in line 20, "wherein said pillars;" should be "wherein said pillars:" to allow the following limitations to associate with said pillars.

Claim 5: in lines 1 and 2, "said second undoped or low-doped region" is inconsistent with claim 2 "second undoped or low-doped semiconductor region", for which claim 5 depends from claim 2.

Claim 7: in line 1, "In" should be "in" since "In" is found in the middle of the claim and is not the starting word of the claim which requires a capital letter.

Claim 8: in lines 1 and 2, "first and second doped regions" is inconsistent with claim 1 "first doped semiconductor region" and "second doped semiconductor region", for which claim 8 depends from claim 1 indirectly.

Claim 8: in line 3, "first and second undoped or low-doped regions" is inconsistent with claim 1 "first undoped or low-doped semiconductor region" and claim 2 "second undoped or low-doped semiconductor region", for which claim 8 depends from claims 1 and 2.

Claim 23: in lines 1 and 2, "first and second doped regions" is inconsistent with claim 1 "first doped semiconductor region" and "second doped semiconductor region", for which claim 23 depends from claim 1.

Claim 23: in line 3, "first undoped or low-doped regions" is inconsistent with claim 1 "first undoped or low-doped semiconductor region", for which claim 23 depends from claim 1.

Claim 27: in line 17, "wherein said pillars;" should be "wherein said pillars:" to allow the following limitations to associate with said pillars.

Claim 30: in line 21, "wherein said pillars;" should be "wherein said pillars:" to allow the following limitations to associate with said pillars.

Appropriate corrections are required.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 *et seq.* for applications not subject

to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1 - 30 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1 - 30 of U.S. Patent No. 11,309,444 B1. Although the claims at issue are not identical, they are not patentably distinct from each other because claims 1, 27, and 30 of the application broadly overlaps with claim 1 of the patent, among other claims of the patent. It is noted that the application's claims recite device operations (e.g., avalanche photodiode), but these do not structurally define over the same, if not similar structure of the patent's claimed device. Claim 30 of the application recites reverse-bias from an external source in the range of -5 to -50 volts, however such claimed voltage range is obvious when the patent's claim requires a reverse bias from an external source to operate the device. Claims 2 - 26 depend from claim 1 directly/indirectly and inherit the double patenting rejection from claim 1. Claims 28 and 29 depend from claim 27 and inherit the double patenting rejection from claim 27.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable

> any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of 35 U.S.C. 112(b):

> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 - 30 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-AIA 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 1 recites the following subject matter in ll. 6 - 15, emphasis added:

> wherein each pillar comprises:
> a first doped semiconductor region;
> ...
> one or more deliberately formed, solid dielectric-filled, in-pillar holes extending into the pillar;
> a top electrical contact; and
> a bottom electrical contact;

In applicant's submitted TABLE on March 29, 2022, support for claim 1 subject matter is described on pp. 12 - 14. Specifically, on pg. 12, "each pillar" is referred to in fig. 5B as each 524 or fig. 15C as each 1524. On pg. 13, a top electrical contact is referred to in fig. 5B as 528 and/or 526 or in fig. 15C as top contact connected to source V. Furthermore, on pg. 13, a bottom electrical contact is

referred to in fig. 5B as 530 or in fig. 15C as bottom contact connected to source V. In fig. 5B, a plurality of pillars 524 share a top electrical contact 526 while a single pillar 524 makes electrical contact with 526 & 528. However, only a single pillar connects with a bottom electrical contact 530 as seen in fig. 5B. This is also similar in fig. 15 C. Therefore, claim 1 does not have support from figs. 5B and 15C that each pillar comprises its own and top and bottom electrical contacts. Claims 2 - 26 depend from claim 1 directly/indirectly and inherit the issue of claim 1.

Claim 1 recites the limitation "10-10,000 nanometers" in line 21. In applicant's submitted TABLE on March 29, 2022, support for claim 1 subject matter is described on pp. 12 - 14. Specifically, on pg. 14, support for the claimed limitation is found in figs. 43 - 46 with the description of "C-C 100-10,000 nm." Therefore, claim 1 does not have support from figs. 43 - 46 for a range of 10-10,000 nm. Claims 2 - 26 depend from claim 1 directly/indirectly and inherit the issue of claim 1.

Claim 2 recites the following subject matter in ll. 1 - 8, emphasis added:

> The device of claim 1, in which each of said pillars further includes:
> a second undoped or low-doped semiconductor regions under the second doped semiconductor regions of said pillars;
> third doped semiconductor regions under the second undoped or low-doped semiconductor regions and above said base dielectric; and
> wherein said top and bottom electrical contacts are configured to provide reverse- bias from an external source in the range of -5 to -50 Volts sufficient for operations of said device as an avalanche photodiode.

In applicant's submitted TABLE on March 29, 2022, support for claim 2 subject matter is described on pp. 15 and 16. Specifically, on pg. 14, support for the claimed limitation is found in fig. 15C for regions 1508 and 1506, for each pillar 1524 (*id.* pg. 12). The preamble of claim 2 establishes that in the claim body, each pillar includes plurality of regions 1508 and 1506, and top and bottom electrical contacts per pillars. However, fig. 15C shows that each pillar 1524 comprises a second undoped or low-doped semiconductor region 1508, each pillar shares a third doped semiconductor region 1506, each pillar shares a top contact connected to source V, and each pillar shares a bottom contact connected to source V. Therefore, claim 2 does not have support from fig. 15C that each pillar includes plurality of

second undoped or low-doped semiconductor regions, plurality of third doped semiconductor regions, and top and bottom electrical contacts, of pillars. Claim 2 contains the limitation "operations of said device". Support for the claimed limitation is found in fig. 15C and ¶ 169 only describes an operation of the device as an avalanche photodiode and provides no additional details that there are multiple operations of the device beyond an avalanche photodiode. Therefore, claim 2 does not have support from fig. 15C and ¶ 169 for "operations". Claims 3 - 15 depends from claim 2, do not remedy the issue of claim 2, and inherit the issue of claim 2.

Claim 27 recites the following subject matter in ll. 4 - 12, emphasis added:

wherein each pillar comprises:
a first doped semiconductor region;
...
one or more deliberately formed, solid dielectric-filled, in-pillar holes extending into the pillar;
a first electrical contact; and
a second electrical contact;

In applicant's submitted TABLE on March 29, 2022, support for claim 27 subject matter is described on pp. 21 - 13. Specifically, on pg. 21, "each pillar" is referred to in fig. 5B as each 524 or fig. 15C as each 1524. On pg. 22, a first electrical contact is referred to in fig. 5B as 528 and/or 526 or in fig. 15C as top contact connected to source V. Furthermore, on pg. 22, a second electrical contact is referred to in fig. 5B as 530 or in fig. 15C as bottom contact connected to source V. In fig. 5B, a plurality of pillars 524 share a top electrical contact 526 while a single pillar 524 makes electrical contact with 526 & 528. However, only a single pillar connects with a second electrical contact 530 as seen in fig. 5B. This is also similar in fig. 15 C. Therefore, claim 27 does not have support from figs. 5B and 15C that each pillar comprises its own and first and second electrical contacts. Claims 28 and 29 depend from claim 27 and inherit the issue of claim 27.

Claim 29 recites the limitation "operations of said device". In applicant's submitted TABLE on March 29, 2022, support for claim 29 subject matter is described on pp. 23 and 24. Specifically, on pg.

24, support for the claimed limitation is found in fig. 15C and ¶ 169 only describes an operation of the device as an avalanche photodiode and provides no additional details that there are multiple operations of the device beyond an avalanche photodiode. Therefore, claim 29 does not have support from fig. 15C and ¶ 169 for "operations".

Claim 30 recites the following subject matter in ll. 5 - 16, emphasis added:

wherein each pillar comprises:
a first doped semiconductor region;
...
one or more deliberately formed, solid dielectric-filled, in-pillar holes extending selected distances into the pillar;
a first electrical contact; and
a second electrical contact;

In applicant's submitted TABLE on March 29, 2022, support for claim 30 subject matter is described on pp. 24 - 46. Specifically, on pg. 24, "each pillar" is referred to in fig. 15C as each 1524. On pg. 25, a first electrical contact is referred to in fig. 15C as top electrical contact connected to source V. Furthermore, on pg. 25, a second electrical contact is referred to in fig. 15C as bottom electrical contact connected to source V. In fig. 15C, a single pillar 1524 connects to a top electrical contact and a bottom electrical contact connected to source V. Therefore, claim 30 does not have support from fig. 15C that each pillar comprises its own and first and second electrical contacts.

Claims 1 - 30 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor (or for applications subject to pre-AIA 35 U.S.C. 112, the applicant), regards as the invention.

Claim 1 recites the limitation "said pillar" in line 18. There is insufficient antecedent basis for this limitation in the claim. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear which pillar the limitation is referring to from the array of pillars. Claims 2 -

26 depend from claim 1 directly/indirectly, do not remedy the issue of claim 1, and inherit the issue of claim 1.

Claim 1 recites the limitation "said pillars" in line 20. There is insufficient antecedent basis for this limitation in the claim. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 6 of claim 1. Claims 2 - 26 depend from claim 1 directly/indirectly, do not remedy the issue of claim 1, and inherit the issue of claim 1.

Claim 1 recites the limitation "said pillars" in line 24. There is insufficient antecedent basis for this limitation in the claim. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 6 of claim 1. Claims 2 - 26 depend from claim 1 directly/indirectly, do not remedy the issue of claim 1, and inherit the issue of claim 1.

Claim 2 recites the limitation "each of said pillars" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 2 depends from claim 1. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 6 of claim 1. Claims 3 - 15 depends from claim 2, do not remedy the issue of claim 2, and inherit the issue of claim 2.

Claim 2 recites the limitation "said pillars" in line 3. There is insufficient antecedent basis for this limitation in the claim. Claim 2 depends from claim 1. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by

"each pillar" in line 6 of claim 1. Claims 3 - 15 depends from claim 2, do not remedy the issue of claim 2, and inherit the issue of claim 2.

Claim 2 recites the limitation "an external source" in line 7. Claim 2 depends from claim 1. Claim 1 recites "an external source" in line 17. It is unclear whether the limitation "an external source" recited in claim 2 was intended to relate back to "an external source" of claim 1 or to set forth an additional external source. Claims 3 - 15 depends from claim 2, do not remedy the issue of claim 2, and inherit the issue of claim 2.

Claim 3 recites the limitation "said pillars" in line 1 and again in line 2. There is insufficient antecedent basis for this limitation in the claim. Claim 3 depends from claim 2. Claim 2 recites "each of said pillars" in line 1. Claim 2 depends from claim 1. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 6 of claim 1.

Claim 4 recites the limitation "said pillars" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claim 4 depends from claim 2. Claim 2 recites "each of said pillars" in line 1. Claim 2 depends from claim 1. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 6 of claim 1.

Claim 5 recites the limitation "said second undoped or low-doped region" in lines 1 and 2. There is insufficient antecedent basis for this limitation in the claim. Claim 5 depends from claim 2. Claim 2 recites "each of said pillars". Claim 2 depends from claim 1. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear which pillar out of the array of pillars that

includes a "second undoped or low-doped semiconductor region" that claim 5 is referring to from claims 1 and 2.

Claim 6 recites the limitation "the same polarity" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claim 6 depends from claim 2. Claim 2 depends from claim 1. Both claims 1 and 2 do not declare "a polarity" for claim 6 to refer back to. Prior to the limitation in claim 6, claim 6 does not declare "a polarity" for each first and second doped semiconductor regions.

Claim 6 recites the limitations "the first and second doped semiconductor regions" and "the third doped semiconductor region" in lines 1 - 3. There are insufficient antecedent bases for these limitations in the claim. Claim 6 depends from claim 2. Claim 2 recites "each of said pillars". Claim 2 depends from claim 1. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear which pillar out of the array of pillars that the limitations of claim 6 is referring to from claims 1 and 2.

Claim 7 recites the limitation "said first undoped or low-doped semiconductor regions" in line 2. There is insufficient antecedent basis for this limitation in the claim. It is unclear how "each of" in line 1 of claim 7 is referring to a plurality of first undoped or low-doped semiconductor regions. Claim 7 depends from claim 2. Claim 2 recites "each of said pillars". Claim 2 depends from claim 1. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear which pillars are being referred to from the array of pillars that the limitations of claim 7 is referring to from claims 1 and 2.

Claim 7 recites the limitations "said second undoped or low-doped semiconductor region" and "said third doped semiconductor region" in lines 3 and 4, emphasis added. There are insufficient antecedent bases for these limitations in the claim. Claim 7 depends from claim 2. Claim 2 declared "second undoped or low- doped semiconductor regions" and "third doped semiconductor regions", emphasis added. It is unclear which second undoped or low-doped semiconductor region out of the

second undoped or low-doped semiconductor regions and which third doped semiconductor region out of third doped semiconductor regions are referring to in claim 2.

Claim 9 recites the limitation "at least said first and second doped semiconductor regions and said first and second undoped or low-doped semiconductor regions" in lines 2 and 3. There is insufficient antecedent basis for this limitation in the claim. It is unclear which first and second doped semiconductor regions and first and which second undoped or low-doped semiconductor regions of the array of pillars claim 9 is referring to.

Claim 10 recites the limitation "each of said pillars" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 10 depends from claim 1 indirectly. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 6 of claim 1.

Claim 11 recites the limitation "each of said pillars" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 11 depends from claim 1 indirectly. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 6 of claim 1.

Claim 12 recites the limitation "said one or more in-pillar holes" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 12 depends from claim 1 indirectly. Claim 1 recites "array of pillars" in line 3, "each pillar" from the array of pillars in line 6, and each pillar comprises "one or more deliberately formed, solid dielectric-filled, in-pillar holes" in line 12. It is unclear which pillar out of the array of pillars the limitation is referring to in claim 1.

Claim 13 recites the limitations "said one or more in-pillar holes" in line 1 and "said first undoped or low-doped semiconductor region" in line 2. There are insufficient antecedent bases for

these limitations in the claim. Claim 13 depends from claim 1 indirectly. Claim 1 recites "array of pillars" in line 3, "each pillar" from the array of pillars in line 6, and each pillar comprises "first undoped or low-doped semiconductor region" in line 8 and "one or more deliberately formed, solid dielectric-filled, in-pillar holes" in line 12. It is unclear which pillar out of the array of pillars the limitations are referring to in claim 1.

Claim 14 recites the limitation "said one or more in-pillar holes" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 14 depends from claim 1 indirectly. Claim 1 recites "array of pillars" in line 3, "each pillar" from the array of pillars in line 6, and each pillar comprises "one or more deliberately formed, solid dielectric-filled, in-pillar holes" in line 12. It is unclear which pillar out of the array of pillars the limitation is referring to in claim 1.

Claim 15 recites the limitation "the gain" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 15 depends from claim 2. Claim 2 depends from claim 1. Claims 1 and 2 do not declare "a gain" for claim 15 to refer to.

Claim 16 recites the limitation "said one or more in-pillar holes" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 16 depends from claim 1 indirectly. Claim 1 recites "array of pillars" in line 3, "each pillar" from the array of pillars in line 6, and each pillar comprises "one or more deliberately formed, solid dielectric-filled, in-pillar holes" in line 12. It is unclear which pillar out of the array of pillars the limitation is referring to in claim 1.

Claim 17 recites the limitations "the first doped semiconductor region and the second doped semiconductor region" in lines 1 and 2. There are insufficient antecedent bases for these limitations in the claim. Claim 17 depends from claim 1. Claim 1 recites "array of pillars" in line 3, "each pillar" from the array of pillars in line 6, and each pillar comprises "a first doped semiconductor region" in line 7 and "a second doped semiconductor region" in line 10. It is unclear which pillar out of the array of pillars the limitations are referring to in claim 1.

Claim 18 recites the limitation "the second doped semiconductor region " in line 3. There is insufficient antecedent basis for this limitation in the claim. Claim 18 depends from claim 1. Claim 1 recites "array of pillars" in line 3, "each pillar" from the array of pillars in line 6, and each pillar comprises "a second doped semiconductor region" in line 10. It is unclear which pillar out of the array of pillars the limitation is referring to in claim 1.

Claim 19 recites the limitation "each of said pillars" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 19 depends from claim 1. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 6 of claim 1.

Claim 20 recites the limitation "each of said pillars" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 20 depends from claim 1. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 6 of claim 1.

Claim 21 recites the limitations "said one or more in-pillar holes" in line 1 and "said first undoped or low-doped semiconductor region". There are insufficient antecedent bases for these limitations in the claim. Claim 21 depends from claim 1. Claim 1 recites "array of pillars" in line 3, "each pillar" from the array of pillars in line 6, and each pillar comprises "a first undoped or low-doped semiconductor region" in line 8 and "one or more deliberately formed, solid dielectric-filled, in-pillar holes" in line 12. It is unclear which pillar out of the array of pillars the limitations are referring to in claim 1.

Claim 22 recites the limitation "each of said pillars" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 22 depends from claim 1. Claim 1 recites "array of pillars" in

line 3 and "each pillar" from the array of pillars in line 6. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 6 of claim 1.

Claim 23 recites the limitation "the first undoped or low-doped regions". There is insufficient antecedent basis for this limitation in the claim. Claim 23 depends from claim 1. Claim 1 recites "array of pillars" in line 3, "each pillar" from the array of pillars in line 6, and each pillar comprises "a first undoped or low-doped semiconductor region" in line 8. It is unclear which pillars out of the array of pillars the limitation is referring to in claim 1.

Claim 24 recites the limitation "said pillars" in lines 2 and 3. There is insufficient antecedent basis for this limitation in the claim. Claim 24 depends from claim 1. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 6 of claim 1.

Claim 25 recites the limitation "said second doped semiconductor regions of said pillars" in lines 1 and 2. There is insufficient antecedent basis for this limitation in the claim. Claim 25 depends from claim 1. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6, where each pillar comprises "second doped semiconductor region" in line 10. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 6 of claim 1.

Claim 25 recites the limitation "said pillar" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claim 25 depends from claim 1. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 6 of claim 1.

Claim 26 recites the limitation "the first doped semiconductor region" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 26 depends from claim 1. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6, where each pillar comprises "first doped semiconductor region" in line 7. It is unclear which pillar out of the array of pillars the limitation is referring to in claim 1.

Claim 26 recites the limitation "the first undoped or low-doped semiconductor region" in line 2. There is insufficient antecedent basis for this limitation in the claim. Claim 26 depends from claim 1. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6, where each pillar comprises "a first undoped or low-doped semiconductor region" in line 8. It is unclear which pillar out of the array of pillars the limitation is referring to in claim 1.

Claim 26 recites the limitation "the second doped semiconductor region" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 26 depends from claim 1. Claim 1 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 6, where each pillar comprises "a second doped semiconductor region" in line 10. It is unclear which pillar out of the array of pillars the limitation is referring to in claim 1.

Claim 27 recites the limitation "said pillar" in line 15. There is insufficient antecedent basis for this limitation in the claim. Claim 27 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 4. It is unclear which pillar the limitation is referring to from the array of pillars. Claims 28 and 29 depend from claim 27, do not remedy the issue of claim 27, and inherit the issue of claim 27.

Claim 27 recites the limitation "said pillars" in line 17. There is insufficient antecedent basis for this limitation in the claim. Claim 27 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 4. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 4 of claim 27.

Claims 28 and 29 depend from claim 27, do not remedy the issue of claim 27, and inherit the issue of claim 27.

Claim 28 recites the limitation "each of said pillars" in line 1. There is insufficient antecedent basis for this limitation in the claim. Claim 28 depends from claim 27. Claim 27 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 4. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 4 of claim 27.

Claim 29 recites the limitation "an external source" in line 7. Claim 29 depends from claim 27. Claim 27 recites "an external source" in line 14. It is unclear whether the limitation "an external source" recited in claim 29 was intended to relate back to "an external source" of claim 27 or to set forth an additional external source.

Claim 30 recites the limitation "said pillars" in line 21. There is insufficient antecedent basis for this limitation in the claim. Claim 30 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 5. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 5 of claim 30.

Claim 30 recites the limitation "said pillars" in line 26. There is insufficient antecedent basis for this limitation in the claim. Claim 30 recites "array of pillars" in line 3 and "each pillar" from the array of pillars in line 5. It is unclear if the limitation is referring to the "array of pillars" in line 3 or the limitation is referring to a subset of pillars from the array of pillars established by "each pillar" in line 5 of claim 30.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Quan Ho whose telephone number is (571)272-8711. The examiner can normally be reached Monday - Friday, 10 AM - 6 PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hoang-Quan Ho
Primary Patent Examiner
Art Unit 2818

/Hoang-Quan Ho/
Primary Examiner, Art Unit 2818

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17707429
Filing Date	2022-03-29
First Named Inventor	Shih-Yuan WANG
Art Unit	
Examiner Name	~~Eduardo A. Rodela~~
Attorney Docket Number	309-0011USDIVCIP2

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17707429
	Filing Date	2022-03-29
	First Named Inventor	Shih-Yuan WANG
	Art Unit	
	Examiner Name	~~Eduardo A. Rodela~~
	Attorney Docket Number	309-0011USDIVCIP2

	1	M. S. Ünlü, M. K. Emsley, O. I. Dosunmu, P. Muller, and Y. Leblebici, "High-speed Si resonant cavity enhanced photodetectors and arrays," J. Vac. Sci. Technol. Vac. Surf. Films, vol. 22, no. 3, p. 781, 2004, doi: 10.1116/1.1647591.	☐
	2	E. Garnett and P. Yang, "Light Trapping in Silicon Nanowire Solar Cells," Nano Lett., vol. 10, no. 3, pp. 1082–1087, Mar. 2010, doi: 10.1021/nl100161z.	☐
	3	D. R. Kim, C. H. Lee, P. M. Rao, I. S. Cho, and X. Zheng, "Hybrid Si Microwire and Planar Solar Cells: Passivation and Characterization," Nano Lett., vol. 11, no. 7, pp. 2704–2708, Jul. 2011, doi: 10.1021/nl2009636.	☐
	4	T. J. Kempa et al., "Coaxial multishell nanowires with high-quality electronic interfaces and tunable optical cavities for ultrathin photovoltaics," Proc. Natl. Acad. Sci., vol. 109, no. 5, pp. 1407–1412, Jan. 2012, doi: 10.1073/pnas.1120415109.	☐
	5	S. Jeong, M. D. McGehee, and Y. Cui, "All-back-contact ultra-thin silicon nanocone solar cells with 13.7% power conversion efficiency," Nat. Commun., vol. 4, no. 1, p. 2950, Dec. 2013, doi: 10.1038/ncomms3950.	☐
	6	H. Lin et al., "Developing controllable anisotropic wet etching to achieve silicon nanorods, nanopencils and nanocones for efficient photon trapping," J. Mater. Chem. A, vol. 1, no. 34, p. 9942, 2013, doi: 10.1039/c3ta11889d	☐
	7	S.-F. Leung et al., "Efficient Photon Capturing with Ordered Three-Dimensional Nanowell Arrays," Nano Lett., vol. 12, no. 7, pp. 3682–3689, Jul. 2012, doi: 10.1021/nl3014567.	☐
	8	JJ. L. Donnelly et al., "Mode-based analysis of silicon nanohole arrays for photovoltaic applications," Opt. Express, vol. 22, no. S5, p. A1343, Aug. 2014, doi: 10.1364/OE.22.0A1343.	☐
	9	P. Spinelli, M. A. Verschuuren, and A. Polman, "Broadband omnidirectional antireflection coating based on subwavelength surface Mie resonators," Nat. Commun., vol. 3, no. 1, p. 692, Jan. 2012, doi: 10.1038/ncomms1691.	☐
	10	S. E. Han and G. Chen, "Toward the Lambertian Limit of Light Trapping in Thin Nanostructured Silicon Solar Cells," Nano Lett., vol. 10, no. 11, pp. 4692–4696, Nov. 2010, doi: 10.1021/nl1029804.	☐
	11	S.-F. Leung et al., "Light Management with Nanostructures for Optoelectronic Devices," J. Phys. Chem. Lett., vol. 5, no. 8, pp. 1479–1495, Apr. 2014, doi: 10.1021/jz500306f.	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17707429
	Filing Date	2022-03-29
	First Named Inventor	Shih-Yuan WANG
	Art Unit	
	Examiner Name	~~Eduardo A. Rodela~~
	Attorney Docket Number	309-0011USDIVCIP2

	12	Y. Yao et al., "Broadband light management using low-Q whispering gallery modes in spherical nanoshells," Nat. Commun., vol. 3, no. 1, p. 664, Jan. 2012, doi: 10.1038/ncomms1664.	☐
	13	K. J. Yu et al., "Light Trapping in Ultrathin Monocrystalline Silicon Solar Cells," Adv. Energy Mater., vol. 3, no. 11, pp. 1401–1406, Nov. 2013, doi: 10.1002/aenm.201300542.	☐
	14	J. Zhu, C.-M. Hsu, Z. Yu, S. Fan, and Y. Cui, "Nanodome Solar Cells with Efficient Light Management and Self-Cleaning," Nano Lett., vol. 10, no. 6, pp. 1979–1984, Jun. 2010, doi: 10.1021/nl9034237.	☐
	15	J. Vaillant, A. Crocherie, F. Hirigoyen, A. Cadien, and J. Pond, "Uniform illumination and rigorous electromagnetic simulations applied to CMOS image sensors," p. 10, 2007.	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/Hoang-Quan Ho/	Date Considered	06/16/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/707,429	WANG et al.
	Examiner	Art Unit
	Hoang-Quan Ho	2818

CPC - Searched*		
Symbol	Date	Examiner
H01L31/035272 or G02B6/122 or G02B6/136 or H01L23/66 or H01L31/02005 or H01L31/02016 or H01L31/02019 or H01L31/022408 or H01L31/022475 or H01L31/02327 or H01L31/02363 or H01L31/024 or H01L31/028 or H01L31/0284 or H01L31/0304 or H01L31/03046 or H01L31/0312 or H01L31/035209 or H01L31/035227 or H01L31/035281 or H01L31/036 or H01L31/054 or H01L31/0745 or H01L31/075 or H01L31/077 or H01L31/105 or H01L31/1055 or H01L31/107 or H01L31/1075 or H01L31/1804 or H01L31/1808 or H01L31/1812 or H01L31/184 or H01L31/1844 or G02B2006/12097 or G02B2006/12176 or H01L2223/6627 or Y02E10/52 or Y02E10/548	06/15/2022	HQH

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
See Search history.	06/17/2022	HQH
See Google Scholar search history.	06/16/2022	HQH

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/707,429	WANG et al.
	Examiner	Art Unit
	Hoang-Quan Ho	2818

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

Notice of References Cited	Application/Control No. 17/707,429	Applicant(s)/Patent Under Reexamination WANG et al.	
	Examiner Hoang-Quan Ho	Art Unit 2818	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20100320444-A1	12-2010	DUTTA; ACHYUT KUMAR	H01L31/068	257/21
*	B	US-20110309331-A1	12-2011	Yu; Young-June	H01L31/028	438/73
*	C	US-11309444-B1	04-2022	Wang; Shih-Yuan	H01L31/035209	1/1
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17707429
Filing Date	2022-03-29
First Named Inventor	Shih-Yuan WANG
Art Unit	
Examiner Name	~~Eduardo A. Rodela~~
Attorney Docket Number	309-0011USDIVCIP2

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20110156195		2011-06-30	Tivarus et al.	
	2	20120153127		2012-06-21	Hirigoyen et al.	
	3	20180012918		2018-01-11	Na et al.	
	4	20190166317		2019-05-30	Tanaka et al.	
	5	20120012741		2012-01-19	Vasylyev	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17707429
	Filing Date	2022-03-29
	First Named Inventor	Shih-Yuan WANG
	Art Unit	
	Examiner Name	Eduardo A. Rodela
	Attorney Docket Number	309-0011USDIVCIP2

	6	20180102442		2018-04-12				

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Copy of International Search Report and Written Opinion for PCT/US2020/051733 mailed December 17, 2020.	
	2	Copy of Written Opinion of International Search Report for PCT/US2020/051733 dated December 17, 2020.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/Hoang-Quan Ho/	Date Considered	06/16/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.H./

Application Number * 17/707,429 *	Application/Control No. 17/707,429	Applicant(s)/Patent under Reexamination WANG et al.	
	Examiner HO, HOANG QUAN TRAN	Art Unit 2818	

Document Code - DISQ	Internal Document - DO NOT MAIL

TERMINAL DISCLAIMER	☑ APPROVED	☐ DISAPPROVED
Date Filed: 29 March 2022	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:

11/Tds all approved.
/LAWANA R HIXON/

Technology Center: OPLC

Telephone: (571)272-6074

_____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/707,429	03/29/2022	Shih-Yuan WANG	309-0011USDIVCIP2	1214

139982 7590 05/26/2022

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

EXAMINER	
CENTRAL, DOCKET	

ART UNIT	PAPER NUMBER
OPAP	

NOTIFICATION DATE	DELIVERY MODE
05/26/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

WMDocket@wissingmiller.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

In re Application of	:	
Wang, et al.	:	
Application No. 17/707,429	:	
Filed: 29 Mar 2022	:	DECISION ON PETITION
For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	:	

This is a decision on the petition under 37 CFR 1.102(c)(1), filed March 29, 2022, to make the above-identified application special based on applicant's age as set forth in MPEP § 708.02, Section II.

The petition is **GRANTED**.

A grantable petition to make an application special under 37 CFR 1.102(c)(1) and MPEP § 708.02, Section II: Applicant's Age, must be accompanied by evidence showing that the applicant is 65 years of age, or more, such as applicant's statement or a statement from a registered practitioner that he or she has evidence that the applicant is 65 years of age or older. No fee is required.

The instant petition includes a statement from a registered practitioner that he or she has evidence that an inventor is 65 years of age or older. Accordingly, the above-identified application has been accorded "special" status.

All other inquiries concerning either the examination or status of the application should be directed to the Technology Center.

Telephone inquiries concerning this decision should be directed to Paralegal Specialist Selena Hamilton at 571-272-8825.

/LIANA S WALSH/
Lead Paralegal Specialist, OPET

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/707,429	03/29/2022	OPAP	1540	309-0011USDIVCIP2	30	3

CONFIRMATION NO. 1214

CORRECTED FILING RECEIPT

139982
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

OC000000133492979

Date Mailed: 04/29/2022

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping WANG, Los Altos, CA;

Applicant(s)

W&WSENS DEVICES, INC., Los Altos, CA;

Power of Attorney: The patent practitioners associated with Customer Number 139982

Domestic Priority data as claimed by applicant

This application is a DIV of 17/532,831 11/22/2021 PAT 11309444
which is a CIP of 17/182,954 02/23/2021
which is a DIV of 16/528,958 08/01/2019 PAT 11121271
which is a CIP of 15/797,821 10/30/2017 PAT 10446700
which is a CON of 14/947,718 11/20/2015 PAT 10622498
which is a CON of PCT/US14/39208 05/22/2014
which claims benefit of 61/826,446 05/22/2013
and claims benefit of 61/834,873 06/13/2013
and claims benefit of 61/843,021 07/04/2013
and claims benefit of 61/905,109 11/15/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/06/2022
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/707,429**
Projected Publication Date: 08/04/2022
Non-Publication Request: No
Early Publication Request: No
**** SMALL ENTITY ****
Title

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor

community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17707429
Filing Date	2022-03-29
First Named Inventor	Shih-Yuan WANG
Art Unit	
Examiner Name	Eduardo A. Rodela
Attorney Docket Number	309-0011USDIVCIP2

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17707429
	Filing Date	2022-03-29
	First Named Inventor	Shih-Yuan WANG
	Art Unit	
	Examiner Name	Eduardo A. Rodela
	Attorney Docket Number	309-0011USDIVCIP2

	1	M. S. Ünlü, M. K. Emsley, O. I. Dosunmu, P. Muller, and Y. Leblebici, "High-speed Si resonant cavity enhanced photodetectors and arrays," J. Vac. Sci. Technol. Vac. Surf. Films, vol. 22, no. 3, p. 781, 2004, doi: 10.1116/1.1647591.	☐
	2	E. Garnett and P. Yang, "Light Trapping in Silicon Nanowire Solar Cells," Nano Lett., vol. 10, no. 3, pp. 1082–1087, Mar. 2010, doi: 10.1021/nl100161z.	☐
	3	D. R. Kim, C. H. Lee, P. M. Rao, I. S. Cho, and X. Zheng, "Hybrid Si Microwire and Planar Solar Cells: Passivation and Characterization," Nano Lett., vol. 11, no. 7, pp. 2704–2708, Jul. 2011, doi: 10.1021/nl2009636.	☐
	4	T. J. Kempa et al., "Coaxial multishell nanowires with high-quality electronic interfaces and tunable optical cavities for ultrathin photovoltaics," Proc. Natl. Acad. Sci., vol. 109, no. 5, pp. 1407–1412, Jan. 2012, doi: 10.1073/pnas.1120415109.	☐
	5	S. Jeong, M. D. McGehee, and Y. Cui, "All-back-contact ultra-thin silicon nanocone solar cells with 13.7% power conversion efficiency," Nat. Commun., vol. 4, no. 1, p. 2950, Dec. 2013, doi: 10.1038/ncomms3950.	☐
	6	H. Lin et al., "Developing controllable anisotropic wet etching to achieve silicon nanorods, nanopencils and nanocones for efficient photon trapping," J. Mater. Chem. A, vol. 1, no. 34, p. 9942, 2013, doi: 10.1039/c3ta11889d	☐
	7	S.-F. Leung et al., "Efficient Photon Capturing with Ordered Three-Dimensional Nanowell Arrays," Nano Lett., vol. 12, no. 7, pp. 3682–3689, Jul. 2012, doi: 10.1021/nl3014567.	☐
	8	JJ. L. Donnelly et al., "Mode-based analysis of silicon nanohole arrays for photovoltaic applications," Opt. Express, vol. 22, no. S5, p. A1343, Aug. 2014, doi: 10.1364/OE.22.0A1343.	☐
	9	P. Spinelli, M. A. Verschuuren, and A. Polman, "Broadband omnidirectional antireflection coating based on subwavelength surface Mie resonators," Nat. Commun., vol. 3, no. 1, p. 692, Jan. 2012, doi: 10.1038/ncomms1691.	☐
	10	S. E. Han and G. Chen, "Toward the Lambertian Limit of Light Trapping in Thin Nanostructured Silicon Solar Cells," Nano Lett., vol. 10, no. 11, pp. 4692–4696, Nov. 2010, doi: 10.1021/nl1029804.	☐
	11	S.-F. Leung et al., "Light Management with Nanostructures for Optoelectronic Devices," J. Phys. Chem. Lett., vol. 5, no. 8, pp. 1479–1495, Apr. 2014, doi: 10.1021/jz500306f.	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17707429
	Filing Date	2022-03-29
	First Named Inventor	Shih-Yuan WANG
	Art Unit	
	Examiner Name	Eduardo A. Rodela
	Attorney Docket Number	309-0011USDIVCIP2

	12	Y. Yao et al., "Broadband light management using low-Q whispering gallery modes in spherical nanoshells," Nat. Commun., vol. 3, no. 1, p. 664, Jan. 2012, doi: 10.1038/ncomms1664.	☐
	13	K. J. Yu et al., "Light Trapping in Ultrathin Monocrystalline Silicon Solar Cells," Adv. Energy Mater., vol. 3, no. 11, pp. 1401–1406, Nov. 2013, doi: 10.1002/aenm.201300542.	☐
	14	J. Zhu, C.-M. Hsu, Z. Yu, S. Fan, and Y. Cui, "Nanodome Solar Cells with Efficient Light Management and Self-Cleaning," Nano Lett., vol. 10, no. 6, pp. 1979–1984, Jun. 2010, doi: 10.1021/nl9034237.	☐
	15	J. Vaillant, A. Crocherie, F. Hirigoyen, A. Cadien, and J. Pond, "Uniform illumination and rigorous electromagnetic simulations applied to CMOS image sensors," p. 10, 2007.	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17707429
Filing Date	2022-03-29
First Named Inventor	Shih-Yuan WANG
Art Unit	
Examiner Name	Eduardo A. Rodela
Attorney Docket Number	309-0011USDIVCIP2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2022-04-28
Name/Print	Ivan S. Kavrukov	Registration Number	25,161

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	45585111
Application Number:	17707429
International Application Number:	
Confirmation Number:	1214
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	139982
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	309-0011USDIVCIP2
Receipt Date:	28-APR-2022
Filing Date:	29-MAR-2022
Time Stamp:	12:34:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	309-0011USDIVCIP2_IDSTransmittal-signed.pdf	473749 4c4a00cb507a641ea4604b244857ba83eb78b5c2	no	1

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	309-0011USDIVCIP2_1449_04-28-2022-signed.pdf	918815 a95cd7d9f2484aeedb44f87d6e142152335f1a9	no	5
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Non Patent Literature	Unlu_High-speedSiResonantCavityEnhancedPhotodetectorsAndArrays.pdf	563868 7e5ee52abebd20ec5d6037b2ce30759aba76f77e	no	7
Warnings:					
Information:					
4	Non Patent Literature	Garnett_Light_Trapping_In_SiliconNanowireSolarCells.pdf	3158107 55a672c978c40fb303c4badc22084d388ea5af0c	no	6
Warnings:					
Information:					
5	Non Patent Literature	Kim_HybridSi_Microwire-And_PlanarSolarCells.pdf	4349805 6226d59e3be47f368047e2dbfa2362693aab4770	no	5
Warnings:					
Information:					
6	Non Patent Literature	Kempa_CoaxialMultishellNanowiresHighQuality.pdf	1193150 4fede540b8f837fce6035d4a9dbf8a226a480960	no	6
Warnings:					
Information:					
7	Non Patent Literature	Jeong_All-back-contactUltra-thinSiliconNanoconeSolarCellsPowerConversionEfficiency.pdf	881313 fac1a361d32e4f918a2e7f42799aabda39bf4aa4	no	7
Warnings:					
Information:					
8	Non Patent Literature	DevelopingControllableAnisotropicWetEtchingAchieveSiliconNanorodsNanopencils.pdf	454493 3c7c8a4280d32a36a73659d69c880aff60f85e5a	no	5
Warnings:					
Information:					

9	Non Patent Literature	EfficientPhotonCapturingOrderedThree-DimensionalNanowellArrays.pdf	1562563 2c5f879c25c0847e96af19aee47d6c41555ff7b3	no	8
Warnings:					
Information:					
10	Non Patent Literature	BroadbandOmnidirectionalAntireflection.pdf	712326 f4c7029cabdd52e18e5c3900418688cc48b67cdb	no	5
Warnings:					
Information:					
11	Non Patent Literature	EON_TowardLambertianLimitLightTrapping.pdf	2136013 0ca1f5ecd8c6034e210559c9b326cbaf45c0dec3	no	5
Warnings:					
Information:					
12	Non Patent Literature	LightManagementNanostructuresOptoelectronicDevices.pdf	1814707 a9e280108db19b987fcd0c15391d0ed4bbbe6d84	no	17
Warnings:					
Information:					
13	Non Patent Literature	Yu_AdvancedEnergyMaterials2013.pdf	1650338 c1e0e122892f6bf5a5927d118bd5eda8117da3aa	no	6
Warnings:					
Information:					
14	Non Patent Literature	Zhu_NanodomeSolarCellsEfficientLightManagement.pdf	477468 8293378c988f639984a6b89862b4e8ad0dcc4881	no	6
Warnings:					
Information:					
15	Non Patent Literature	Donnelly_Mode-basedAnalysis.pdf	5359629 09cc61b4d04e5332d2bb1dc47f55d495de32f150	no	12
Warnings:					
Information:					

16	Non Patent Literature	Yao__BroadbandLightManagementUsingLow-Q.pdf	4880379 3aa834d7bb1efa00e2b1ef8ad30781bcc090e08a	no	8
Warnings:					
Information:					
17	Non Patent Literature	Vaillant__UniformIlluminationiGorousElectromagneticSimulations.pdf	4546814 5c6a5db3778dedaa1656fec1eebb668b1fff7677	no	10
Warnings:					
Information:					
		Total Files Size (in bytes):	35133537		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Shih-Yuan WANG Application No.: 17/707,429 Filed: March 29, 2022 Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	Examiner: n/a Art Unit: n/a **CERTIFICATE OF TRANSMISSION** I hereby certify that this correspondence is being submitted through the USPTO Electronic Filing Service addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 /Mary Ellen Finnegan/ Date: April 28, 2022 Name: Mary Ellen Finnegan

VIA EFS-Web
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

It is respectfully requested that the documents listed on the attached Information Disclosure Citation form PTO/SB/08a be considered by the Patent Examiner in connection with the above-identified application and be made of record therein.

Independent consideration and acknowledgement of the enclosed document are respectfully requested.

The Commissioner is hereby authorized to charge U.S. PTO Deposit Account 600125 any payment due and to credit any overpayment thereto.

Respectfully submitted,

/Ivan S. Kavrukov/
Ivan S. Kavrukov
Registration No. 25,161
Attorney for Applicant

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001
Attorney's Telephone No.: 917-945-0121
Attorney's E-mail: ikavrukov@wissingmiller.com

Electronic Acknowledgement Receipt

EFS ID:	45566053
Application Number:	17707429
International Application Number:	
Confirmation Number:	1214
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	139982
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	309-0011USDIVCIP2
Receipt Date:	26-APR-2022
Filing Date:	29-MAR-2022
Time Stamp:	15:39:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	309-0011USDIVCIP2_Response RegardingCorrectedADS_Filing Receipt-signed.pdf	479037 71e9337c5a106b83cf78dcee07318569ed02bbad	no	2

Warnings:

Information:					
2	Application Data Sheet	309-0011USDIVCIP2_Corrected ADS_04-26-2022_FINAL.pdf	1507208 42039d370661e5cc2e33b5ef25ed39d04d7c493d	no	8
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
			Total Files Size (in bytes):	1986245	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shih-Yuan		WANG	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Palo Alto	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	766 Encina Grande Dr.
Address 2	

City	Palo Alto	State/Province	CA
Postal Code	94306	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shih-Ping		WANG	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Los Altos	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	38 3rd Street, Suite #307
Address 2	

City	Los Altos	State/Province	CA
Postal Code	94022	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	23432		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES		
Attorney Docket Number	309-0011USDIVCIP2	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	47	**Suggested Figure for Publication (if any)**	5B

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	23432		

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Division of	17532831	2021-11-22
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
17532831	Continuation in part of	17182954	2021-02-23
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17182954	Division of	16528958	2019-08-01	11121271	2021-09-04

Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	15797821	2017-10-30	10446700	2019-10-15

Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15797821	Continuation of	14947718	2015-11-20	10622498	2020-04-14

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
14947718	Continuation of	PCT/US14/39208	2014-05-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61826446	~~2013-05-05~~ 2013-05-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61834873	2013-06-13
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	~~61834821~~ 61/843,021	2013-07-04
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61905109	2013-11-15

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	W&WSENS DEVICES, INC.

Mailing Address Information For Applicant:

Address 1	38 THIRD STREET		
Address 2	SUITE 307		
City	LOS ALTOS	**State/Province**	CA
Country	US	Postal Code	94022
Phone Number		Fax Number	

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Email Address	

Additional Applicant Data may be generated within this form by selecting the Add button.

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/Ivan S. Kavrukov/			Date (YYYY-MM-DD)	~~2022-03-20~~ 2022-04-2
First Name	Ivan	Last Name	Kavrukov	Registration Number	25161

Additional Signature may be generated within this form by selecting the Add button.

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent C o o p eration Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor:	Shih-Yuan WANG
Serial No.:	17/707,429
Filing Date:	March 29, 2022
Examiner:	TBD
Art Unit:	TBD
Confirmation No.:	1214
For:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: April 26, 2022

I hereby certify that this correspondence is being transmitted via Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

COMMUNICATION REGARDING CORRECTION OF APPLICATION DATA SHEET AND CORRECTED FILING RECIEPT

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits a Corrected Application Data Sheet to correct an error in the priority application number and filing date.

The Application Data Sheet that was originally filed on March 29, 2022, had the incorrect filing date as May 5, 2013, for Provisional Application Number 61/826,446. The correct filing date is May 22, 2013.

In addition, the Application Data Sheet originally filed on March 29, 2022, inadvertently transposed the Serial Number for Provisional Application Number as 61/834,021, filed July 4, 2013. The Provisional Application Number should have read 61/843,021, filed July 4, 2013. Submitted herewith is a Corrected ADS with changes marked to show the correct application number and filing date for each Provisional Application mentioned above.

Correction of the ADS and issuance of a corrected Filing Receipt is earnestly solicited.

No fee is required. Nevertheless, the Office is hereby authorized to charge any other fees that may be required in connection herewith and to credit any overpayment to our Deposit Account No. 600125.

Respectfully Submitted,

WISSING MILLER LLP

Attorney for Applicants

By: /Ivan S. Kavrukov/

Ivan S. Kavrukov
Reg. No. 25,161
Tel.: (917) 945-0121

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/707,429	03/29/2022	OPAP	1540	309-0011USDIVCIP2	30	3

CONFIRMATION NO. 1214

CORRECTED FILING RECEIPT

139982
Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

OC000000133374525

Date Mailed: 04/25/2022

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping WANG, Los Altos, CA;

Applicant(s)

W&WSENS DEVICES, INC., Los Altos, CA;

Power of Attorney: The patent practitioners associated with Customer Number 139982

Domestic Priority data as claimed by applicant

This application is a DIV of 17/532,831 11/22/2021 PAT 11309444
which is a CIP of 17/182,954 02/23/2021
which is a DIV of 16/528,958 08/01/2019 PAT 11121271
which is a CIP of 15/797,821 10/30/2017 PAT 10446700
which is a CON of 14/947,718 11/20/2015 PAT 10622498
which is a CON of PCT/US14/39208 05/22/2014
which claims benefit of 61/826,446 05/22/2013 *
and claims benefit of 61/834,873 06/13/2013
and claims benefit of 61/834,021 06/12/2013 *
and claims benefit of 61/905,109 11/15/2013
(*)Data provided by applicant is not consistent with PTO records.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/06/2022
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/707,429**
Projected Publication Date: 07/14/2022
Non-Publication Request: No
Early Publication Request: No
**** SMALL ENTITY ****
Title

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign

patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Shih-Yuan WANG Application No.: 17/707,429 Filed: March 29, 2022 Title: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	Examiner: n/a Art Unit: n/a **CERTIFICATE OF TRANSMISSION** I hereby certify that this correspondence is being submitted through the USPTO Electronic Filing Service addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 /Mary Ellen Finnegan/ Date: April 13, 2022 Name: Mary Ellen Finnegan

VIA EFS-Web
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT

It is respectfully requested that the documents listed on the attached Information Disclosure Citation form PTO/SB/08a be considered by the Patent Examiner in connection with the above-identified application and be made of record therein.

Independent consideration and acknowledgement of the enclosed document are respectfully requested.

The Commissioner is hereby authorized to charge U.S. PTO Deposit Account 600125 any payment due and to credit any overpayment thereto.

Respectfully submitted,

/Ivan S. Kavrukov/
Ivan S. Kavrukov
Registration No. 25,161
Attorney for Applicant

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001
Attorney's Telephone No.: 917-945-0121
Attorney's E-mail: ikavrukov@wissingmiller.com

Electronic Acknowledgement Receipt

EFS ID:	45468588
Application Number:	17707429
International Application Number:	
Confirmation Number:	1214
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	309-0011USDIVCIP2
Receipt Date:	13-APR-2022
Filing Date:	29-MAR-2022
Time Stamp:	17:20:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	309-0011USDIVCIP2_IDSTransmittal-signed.pdf	89727 b27a4240101297a8bb8ddc8c4b52e7118f86a17a	no	1

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	309-0011USDIVCIP2_1449.pdf	1034610 558f26b275d8759118c0da1fc149bc845e040979	no	4
Warnings:					
Information:					
3	Non Patent Literature	PCTUS2051733_SearchReport.pdf	102640 54ac1b55149a8eea612b73f11a543fd80b4bca18	no	2
Warnings:					
Information:					
4	Non Patent Literature	PCTUS2051733_WrittenOpinion.pdf	807956 18fe8c300e7c435d09577b4679fadf03d8b529f0	no	11
Warnings:					
Information:					
			Total Files Size (in bytes):	2034933	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: IVAN S. KAVRUKOV
COOPER & DUNHAM LLP
30 ROCKEFELLER PLAZA
NEW YORK, NY 10112

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	17 DEC 2020
Applicant's or agent's file reference 5176/91538-PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US 20/51733	21 September 2020 (21.09.2020)	24 September 2019 (24.09.2019)

International Patent Classification (IPC) or both national classification and IPC

IPC - H01L 27/146, 31/101, 31/102 (2020.01)

CPC - H01L 27/14609, 27/14612, 27/14643, 31/101, 31/102

Applicant

W&WSENS DEVICES INC:

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	15 November 2020	Lee Young PCT Help Desk Telephone No. 571-272-4300

Form PCT/ISA/237 (cover sheet) (revised January 2019)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/51733

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

☒ the international application in the language in which it was filed.

☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(b)).

3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:

a. ☐ forming part of the international application as filed:

☐ in the form of an Annex C/ST.25 text file.

☐ on paper or in the form of an image file.

b. ☐ furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.

c. ☐ furnished subsequent to the international filing date for the purposes of international search only:

☐ in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).

☐ on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/51733

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-42	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	3-5, 12, 17-19, 21, 33, 36, 38, 42	YES
	Claims	1, 2, 6-11, 13-16, 20, 22-32, 34, 35, 37, 39-41	NO
Industrial applicability (IA)	Claims	1-42	YES
	Claims	NONE	NO

2. Citations and explanations:
Claims 1, 2, 6-9, 11, 13-16, 20, 22-31, 34, 35, 37, and 39-41 lack an inventive step under PCT Article 33(3) as being obvious over US 2018/0102442 A1 to W&Wsens, Devices Inc. (hereinafter "Wsens") in view of US 2011/0156195 A1 to Tivarus et al. (hereinafter "Tivarus").

Regarding claim 1, Wsens discloses a photosensor wafer of crystalline Si and a CMOS Logic Processor (CLP) wafer stacked on each other for electrical interaction and forming a structure (Fig.8; para [0038]- an integrated combination of a microstructure-enhanced photodetector (MSPD) and an active electronic circuit; para [0203]- Silicon chip 800 can any combination of the following devices: MSPDs; MSAPDs; vertical cavity surface emitting lasers (VCSEL) that are either wafer bonded to the chip and/or have a precision cavity for dropping the VCSEL into as in a silicon platform; CMOS/BiCMOS ASICs configured for functions such as signal processing, amplifying, transmission, storage, conditioning, analyzing, and/or configured as laser drivers and/or power amplifiers; Fig.45 shows cmos layer and MSPC layer stacked on each other; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration; para [0489]- the microstructure holes can be very complex, as for example in Berenschot et al, Fabrication of 3D fractal structures using nanoscale anisotropic etching of single crystalline silicon) comprising:
an array of laterally spaced pixels formed in said photosensor wafer (Fig. 20 and 21 shows array of laterally spaced pixels (the structures comprises MSPD 1, MSPD2 or MSPD3) in wafer; Fig. 45 shows a single pixel structure with a CMOS layer; para [0248]- FIG. 21 is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics);
wherein said pixels comprise photosensors each including one or more microstructure holes (4412) extending into said photosensor wafer (Fig. 45 shows holes 4412 extending into the said photo wafer (I Si and/or GeSi layer); para [0333]- microstructure holes 4412; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration) and further including plural N-doped and/or P-doped regions (4482, 4484) of the photosensor wafer configured to interact with light photons impinging on said pixels, including on said holes (Fig. 45; para [0330]- Ion implantation to form region 4482 can be implemented from the bottom surface; para [0333]- a depth etch monitor layer 4466 that can be implanted with ions such as Ar, Ne, Xe, O, and/or N...Also shown are upper ion implanted region 4484; para [0349]-Light and/or optical signal can impinge from the surface with the holes and in some cases light/optical signal can impinge from the substrate side through a via. The optical signal is brought to the MSPD/MSAPD via an optical fiber that can have a lens and is focused onto the surface with a certain numerical aperture such that there may be an angular distribution of light rays that are impinging on the surface of the MSPD/MSAPD.);
one or more active CMOS circuits formed in said CLP wafer (Fig.45; para [0038], [0248], [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration...reinforcement of the MSPD/MSAPD structure and CMOS/BiCMOS IC electronics.); and
electrical interconnects between said pixels and said one or more active CMOS circuits, wherein said interconnects are configured to convey electrical signals between said pixels and said one or more active CMOS circuits (Fig. 21; para [0248]- The MSPDs/MSAPDs (MSPD1, MSPD2, MSPD3, MSPD4, etc.) are connected to the CMOS/BiCMOS electronics with a transmission line 2142...The monolithically integrated chip 2100 can be flipped and the electronics can be solder bumped to external circuits such as on a printed circuit board (PCB) (not shown) for electrical signal transmission and electrical power.).
Wsens fails to discloses respective lenses over said pixels; light photons impinging on said pixels through said lenses; wherein said CLP wafer is at a side of said photosensor wafer that is opposite said lenses.
Tivarus, drawn to a stacked CMOS sensor, discloses respective lenses (1304) over pixels (1204, 1206); light photons impinging on said pixels through said lenses; wherein CLP wafer (1306) is at a side of said photosensor wafer (1300) that is opposite said lenses (1304) (Fig. 13 shows the wafer 1306 is at a side of said photosensor wafer 1300 that is opposite the lenses 1304; para [0001]-more particularly to CMOS image sensors having two separate stacked semiconductor wafers with each wafer including a portion of the electrical circuitry; para [0032]- light 302 from a subject scene is input to an imaging stage 304. Imaging stage 304 can include conventional elements such as a lens; para [0062]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300; para [0063]- Circuit wafer 1306;). It would have been obvious to a person having ordinary skill in the art to combine the lenses and the stacked structure disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0005]-[0006]).

--see supplemental box

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/51733

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

Claims 27 and 35 lack antecedent basis for terms "said lenses". For purposes of this search, claims 27 and 35 are interpreted as depending from claim 26.

Claim 42 depends on claim 3408 which is not exist. For purposes of this search, claim 42 is interpreted as depending on claim 40.

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/51733

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
Box V.2 - Citations and Explanations:

Regarding claim 2, Wsens in view of Tivarus disclose the structure of claim 1. Tivarus further discloses including respective color filters between said lenses and pixels configured to select respective wavelength ranges (Fig. 13 shows color filters 1302 between lenses 1304 and photodetectors 1202, 1204, 1206, 1208; para [0247]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300.).

Regarding claim 6, Wsens in view of Tivarus disclose the structure of claim 1, Wsens further discloses in which said at least some of said holes in the photosensor wafer are generally cylindrical (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 7, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which said at least some of said holes in the photosensor wafer are inverted pyramids (Fig. 24; para [0186]- scanning electron micrographs of holes in the shape of inverted pyramids; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.)

Regarding claim 8, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which said at least some of said holes in the photosensor wafer are funnel shaped (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 9, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which said hole of each of at least some of said pixels comprises a cluster of nanoholes (9212) into said photosensor wafer (Fig. 92 shows a cluster of nanoholes 9212, para [0560]- The nano/micro structure holes 9212 can have lateral surface dimensions ranging from 30 nm to 5000 nm or more and spacing between the nano micro structure holes can range from 10 nm to 10000 nm or more. The holes can be shaped as a circle, oval, square, polygon, hourglass, fractal, amoeba, star or a combination of shapes).

Regarding claim 11, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses including light reflectors under said pixels (Fig. 9B; para [0208]- a via 930 can be etched to remove most or all of the substrate to the etch stop layer which can in addition be patterned with nano-micro structures 914 and/or can be coated with dielectric distributed Bragg reflectors.).

Regarding claim 13, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which at least some of said holes differ in shape from one another (Fig. 24 shows the different shape of holes; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 14, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which each of said pixels comprises laterally spaced doped regions (4284) (Fig. 41-42; para [0319]- after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants; para [0330]).

Regarding claim 15, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which each of said pixels comprises vertically spaced doped regions (4260) (Fig. 41-42; para [0319]- A N+ connecting well 4260 formed by ion implantation and/or diffusion can connect the cathode on the surface to the N+ layer/region 4282 and in the case of an N substrate the cathode can be on the bottom of the substrate with or without additional connect wells.; para [0330]).

Regarding claim 16, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which said pixels include Ge regions in said photosensor wafer, configured to extend a response of said pixels to light in a 2 micrometers wavelength range (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer; para [0344]- Operating wavelength range for Si I layer can range from 750 nm to 1070 nm and for GeSi can range from 750 nm to 1350 nm and in some cases 900 nm to 1350 nm and in some cases 1100 nm to 1350 nm and in some cases 1250 nm to 1550 nm and in some cases 1250 nm to 1650 nm and in some cases to 2000 nm depending on the Ge fraction in the GeSi alloy.).

Regarding claim 20, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses including doped Si conformally lining at least some of said holes and hyperdoping over said doped Si lining (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants (It is noted P+ or N+ doping is hyperdoping.)).

Regarding claim 22, Wsens in view of Tivarus disclose the structure of claim 1, further including a first layer of electrically insulating material under said pixels (Fig.46 shows BOX layer under the pixel; para [0215]- buried oxide (BOX) layer of 2000 nm on silicon substrate (Therefore the BOX layer is SiO2, which is an insulating material.)) and a second layer of an electrically insulating material over said active CMOS circuits (para [0442]- entire monolithically integrated MSPD/AMSPD with CMOS and/or BiCMOS electronics chip can be entirely and/or partially hermetically sealed with dielectrics such as silicon oxide, silicon nitride, aluminum oxide, aluminum nitride, polymers such as polyimide, and/or spin-on-glass.).

--see next page

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/51733

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
Box V.2 - Citations and Explanations:

Regarding claim 23, Wsens in view of Tivarus disclose the structure of claim 22. Wsens further discloses wherein the first and second layers of electrically insulating material are selected from a group consisting of Si Oxide and Si Nitride (para Fig.46 shows BOX layer under the pixel; para [0215]- buried oxide (BOX) layer of 2000 nm on silicon substrate (Therefore the BOX layer is SiO2, which is an insulating material); [0442]- entire monolithically integrated MSPD/AMSPD with CMOS and/or BiCMOS electronics chip can be entirely and/or partially hermetically sealed with dielectrics such as silicon oxide, silicon nitride, aluminum oxide, aluminum nitride, polymers such as polyimide, and/or spin-on-glass.).

Regarding claim 24, Wsens in view of Tivarus disclose The structure of claim 22. Wsens further discloses wherein one or more additional layers of electrically insulating material are formed on said first and/or second layers of electrically insulating material (Fig. 24 shows a Bragg reflector layer on BOX layer; para [0215]- buried oxide (BOX) layer of 2000 nm on silicon substrate (Therefore the BOX layer is SiO2, which is an insulating materia); para [0255]- Starting with a silicon substrate that can have a buried oxide (BOX) layer and/or buried hole layer (SOH silicon on hole), and/or with or without an etch stop layer; para [0256]- in addition a dielectric Bragg reflector; para [0319]).

Regarding claim 25, Wsens discloses a high-speed photodetector array (HSPA) wafer of crystalline Si and a CMOS Logic Processor (CLP) wafer stacked on each other for electrical interaction and forming a structure (Fig.8; para [0186]- FIGS. 1A-1H are top-view scanning electron micrographs of holes in the shape of inverted pyramids used in a microstructure high speed photodiode (MSPD) and/or a high speed microstructure avalanche photodiode (MSAPD); para [0209]- Arrays of MSPD/MSAPD can be monolithically integrated with CMOS/BiCMOS electronics; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration; para [0489]- the microstructure holes can be very complex, as for example in Berenschot et al, Fabrication of 3D fractal structures using nanoscale anisotropic etching of single crystalline silicon) comprising:
an array of laterally spaced photodetectors formed in said HSPA wafer (Fig. 20 and 21 shows array of laterally spaced pixels (the structures comprises MSPD 1, MSPD2 or MSPD3) in wafer; Fig. 45 shows a single pixel structure with a CMOS layer; para [0248]- FIG. 21 is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics);
wherein each of said photodetectors includes at least one microstructure hole (4412) extending into said HSPA wafer (Fig. 45 shows holes 4412 extending into the said photo wafer (I Si and/or GeSi layer); para [0333]- microstructure holes 4412; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration) and further includes plural N-doped and/or P-doped regions (4482, 4484) of the HSPA wafer configured to interact with light photons impinging on said photodetector from a first side of the HSPA wafer (Fig. 45; para [0330]- Ion implantation to form region 4482 can be implemented from the bottom surface; para [0333]- a depth etch monitor layer 4466 that can be implanted with ions such as Ar, Ne, Xe, O, and/or N...Also shown are upper ion implanted region 4484; para [0349]-Light and/or optical signal can impinge from the surface with the holes and in some cases light/optical signal can impinge from the substrate side through a via. The optical signal is brought to the MSPD/MSAPD via an optical fiber that can have a lens and is focused onto the surface with a certain numerical aperture such that there may be an angular distribution of light rays that are impinging on the surface of the MSPD/MSAPD.);
one or more active CMOS circuits formed in said CLP wafer (Fig.45; para [0038], [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration...reinforcement of the MSPD/MSAPD structure and CMOS/BiCMOS IC electronics); and
electrical interconnects between said high speed photodetector array and said one or more active CMOS circuits, wherein said interconnects are configured to convey electrical signals between said HSPA and said one or more active CMOS circuits (Fig. 21; para [0248]- The MSPDs/MSAPDs (MSPD1, MSPD2, MSPD3, MSPD4, etc.) are connected to the CMOS/BiCMOS electronics with a transmission line 2142...The monolithically integrated chip 2100 can be flipped and the electronics can be solder bumped to external circuits such as on a printed circuit board (PCB) (not shown) for electrical signal transmission and electrical power).
Wsens fails to disclose wherein said CLP wafer is at a side of said HSPA wafer that is opposite said first side.
Tivarus, drawn to a stacked CMOS sensor, discloses CLP wafer (1306) is at a side of a wafer (1300) that is opposite the first side (Fig. 13 shows the wafer 1306 is at a side of the wafer 1300 that is opposite the side with photodetectors; para [0001]-more particularly to CMOS image sensors having two separate stacked semiconductor wafers with each wafer including a portion of the electrical circuitry; para [0062]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300; para [0063]- Circuit wafer 1306;). It would have been obvious to a person having ordinary skill in the art to combine the stacked structure disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0005]-[0006]).

Regarding claim 26, Wsens in view of Tivarus disclose the structure of claim 25 and the HSPA wafer as discussed above. Tivarus further discloses including an array of lenses (1304) formed over the photodetectors (1204, 1206) on said first side of the wafer (1300) (Fig. 13; para [0062]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300). It would have been obvious to a person having ordinary skill in the art to combine the lenses disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0005]-[0006]).

Regarding claim 27, Wsens in view of Tivarus disclose the structure of claim 26. Wsens further discloses plural holes in pixels in said HSPA wafer (Fig. 45 shows plural holes in a single pixel structure; para [0333]- microstructure holes 4412); said photodetectors and said active CMOS circuits are configured to operate at 56 Gb/s or greater data rates that include 112 Gb/s (para [0218]- With thinner I layer, 50 Gb/s, 60 Gb/s, 80 Gb/s, 100 Gb/s can be achieved). Tivarus further discloses in which each of said lenses overlies each pixel (See Tivarus, Fig. 13; para [0062]- A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300). Therefore the lenses disclosed in Tivarus overlies the holes of Wsens since they overly the substrate of Tivarus and the substrate of Wsens has holes.

--see next page

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/51733

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
Box V.2 - Citations and Explanations:

Regarding claim 28, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which at least some of said holes in the HSPA wafer are generally cylindrical (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 29, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which at least some of said holes in the HSPA wafer are inverted pyramids (Fig. 24; para [0186]- scanning electron micrographs of holes in the shape of inverted pyramids; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 30, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which at least some of said holes in the HSPA wafer are funnel shaped (Fig. 24; para [0255]- Microstructure holes 2412 in general can have any shape, and in some cases are pyramidal, funnel shaped, cylindrical, polygonal, and/or a combination of shapes.).

Regarding claim 31, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses including an array of optical filters (2014, 2016, 2018) formed at said first side of the HSPA wafer over said photodetectors (Fig. 20; para [0246]- Bandpass filters can also be fabricated on the top surface where the microstructured holes for absorption enhancement are etched; para [0247]- Note that some or all of the MSPDs can also be MSAPDs. The MSPDs form an array where each MSPD1, MSPD2, MSPD3, . . . MSPDn has a bandpass filter with its own unique bandpass wavelength. Having a different bandpass wavelength for each of the MSPD in the array allows for the selection of specific wavelengths in a CWDM optical signal).

Regarding claim 34, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which said photodetectors include Ge regions in said HSPA wafer, configured to enhance a response of said photodetectors to light in a wavelength range that includes 1350 nm and / or in a wavelength range that includes1550 nm (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer; para [0344]- Operating wavelength range for Si I layer can range from 750 nm to 1070 nm and for GeSi can range from 750 nm to 1350 nm and in some cases 900 nm to 1350 nm and in some cases 1100 nm to 1350 nm and in some cases 1250 nm to 1550 nm and in some cases 1250 nm to 1650 nm and in some cases to 2000 nm depending on the Ge fraction in the GeSi alloy).

Regarding claim 35, Wsens in view of Tivarus disclose the structure of claim 26. Wsens further discloses plurality of holes in pixels (Fig. 45 shows plurality of holes in a single pixel structure; para [0333]- microstructure holes 4412). Tivarus further discloses in which at least some of said lenses overlies each pixel (See Tivarus, Fig. 13; para [0062]- A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300). Therefore the lenses overlies the holes since they overly the substrate and the substrate of Wsens has holes. Wsens further discloses said photodetector array and said CMOS active circuits are configured to operate at data rates of 56 Gb/s or higher (para [0218]- With thinner I layer, 50 Gb/s, 60 Gb/s, 80 Gb/s, 100 Gb/s can be achieved.)

Regarding claim 37, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses including doped Si conformally lining said holes and hyperdoping over said doped Si lining the holes (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants (It is noted P+ or N+ doping is hyperdoping.)).

Regarding claim 39, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which said CLP wafer includes clock recovery circuits and transimpedance amplifiers (para [0045]- The additional active electronic circuits can comprise one or more transimpedance amplifiers (TIAs); para [0273]- The CMOS/BiCMOS ASICs can include one or more of the following: TIAs; clock data recovery (CDR) circuitry; equalizers; and limiting amplifiers (LA),), and wherein said HSPA and CLP wafers are configured to operate at aggregated data rates of 400-1000 Gb/s or more (para [0268]- increase the aggregated data rates to greater than 40 Gb/s and in some cases greater than 100 Gb/s and in some cases greater than 1 Tb/s.).

Regarding claim 40, Wsens discloses a monolithic wafer of crystalline Si having a first side and a second side (Fig. 39; para [0325]- and/or polycrystalline silicon layers; para [0489]- the microstructure holes can be very complex, as for example in Berenschot et al, Fabrication of 3D fractal structures using nanoscale anisotropic etching of single crystalline silicon), comprising: an array of laterally spaced photosensor or photodetector pixels formed at said first side of the wafer (Fig. 20 and 21 shows array of laterally spaced pixels (the structures comprises MSPD 1, MSPD2 or MSPD3) in wafer; Fig. 45 shows a single pixel structure with a CMOS layer; para [0248]- FIG. 21 is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics);
wherein each of said pixels includes at least one hole (4412) formed into said first side of the wafer (Fig. 45 shows holes 4412 formed into the said photo wafer (I Si and/or GeSi layer); para [0333]- microstructure holes 4412; para [0336]- FIG. 45 is a cross section view as in FIGS. 44A-44C illustrating some further aspects of MSPD-ASIC monolithic integration) and further includes plural N-doped and/or P-doped regions (4482, 4484) of the wafer configured to interact with light photons impinging on said pixels, including on said holes (Fig. 45; para [0330]- Ion implantation to form region 4482 can be implemented from the bottom surface; para [0333]- a depth etch monitor layer 4466 that can be implanted with ions such as Ar, Ne, Xe, O, and/or N...Also shown are upper ion implanted region 4484; para [0349]-Light and/or optical signal can impinge from the surface with the holes and in some cases light/optical signal can impinge from the substrate side through a via. The optical signal is brought to the MSPD/MSAPD via an optical fiber that can have a lens and is focused onto the surface with a certain numerical aperture such that there may be an angular distribution of light rays that are impinging on the surface of the MSPD/MSAPD.);
CMOS logic processors (para [0038], [0248]- FIG. 21 is a simple schematic diagram showing MSPD/MSAPD arrays monolithically integrated with CMOS and/or BiCMOS electronics); and (claim 40 continued)

--see next page

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/51733

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
Box V.2 - Citations and Explanations:

(claim 40 continued) electrical interconnects in said wafer configured to convey electrical signals between said pixels and said one or more active CMOS circuits (Fig. 21; para [0248]- The MSPDs/MSAPDs (MSPD1, MSPD2, MSPD3, MSPD4, etc.) are connected to the CMOS/BiCMOS electronics with a transmission line 2142...The monolithically integrated chip 2100 can be flipped and the electronics can be solder bumped to external circuits such as on a printed circuit board (PCB) (not shown) for electrical signal transmission and electrical power). Wsens fails to disclose respective optical lenses over said pixels configured to direct to said pixels and said holes light impinging on said first side of the wafer; CMOS logic processors formed at said second side of the wafer.
Tivarus, drawn to a stacked CMOS sensor, discloses respective optical lenses (1304) over the pixels (1202, 1204) configured to direct to said pixels light impinging on the first side of the wafer (upper side); CMOS logic processors (1306) formed at the second side of the wafer (lower side). (Fig. 13; para [0001]-more particularly to CMOS image sensors having two separate stacked semiconductor wafers with each wafer including a portion of the electrical circuitry; para [0032]- light 302 from a subject scene is input to an imaging stage 304. Imaging stage 304 can include conventional elements such as a lens; para [0062]- Sensor wafer 1300 includes photodetectors 1202, 1204, 1206, 1208, transfer gates 1214, 1216, and charge-to-voltage conversion regions 1218. A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300; para [0063]- Circuit wafer 1306;). It would have been obvious to a person having ordinary skill in the art to combine the lenses and the stacked structure disclosed by Tivarus to the structure disclosed by Wsens for higher image resolutions and more reliable fabrication process (See Tivarus, para [0005]-[0006]).

Regarding claim 41, Wsens in view of Tivarus disclose the monolithic wafer of claim 40. Wsens further discloses plurality of holes in pixels in the wafer (Fig. 45 shows plurality of holes in a single pixel structure; para [0333]- microstructure holes 4412). Tivarus further discloses in which at least some of said lenses overlies each pixel (See Tivarus, Fig. 13; para [0062]- A color filter array (CFA) 1302 and microlenses 1304 are disposed on a surface of sensor wafer 1300). Therefore the lenses disclosed by Tivarus overlies the holes disclosed in Wsens since they overly the substrate in Tivarus and the substrate of Wsens has holes.

Claim 10 lacks an inventive step under PCT Article 33(3) as being obvious over Wsens in view of Tivarus and further in view of US 2012/0153127 A1 to Hirigoyen et al. (hereinafter "Hirigoyen").

Regarding claim 10, Wsens in view of Tivarus disclose the structure of claim 1, but fails to discloses further including light blockers between adjacent pixels to reduce crosstalk. Hirigoyen, drawn to image sensor, discloses light blocker (40) between adjacent pixels (S1, S2) to reduce crosstalk (Fig. 4; para [0008], [0052]-Isolation region I1.. reduces optical crosstalk thanks to an optical waveguide formed by the differences in refractive indices between the substrate 10, the conductive material 30, and the optical isolator 40. para [0057]- Image sensor IS3 differs from image sensor IS2 in that the color filters F1, F2, F3 and the microlenses L1, L2, L3 are arranged on the backside of the substrate 10...the optical isolator 40 extends entirely through the trench 15). It would have been obvious to a person having ordinary skill in the art to combine the light blockers disclosed by Hirigoyen to the structure disclosed by Wsens to enhance the performance by reducing the corsstalk between pixels (See Hirigoyen, para [0052]).

Claim 32 lacks an inventive step under PCT Article 33(3) as being obvious over Wsens in view of Tivarus and further in view of US 2018/0012918 A1 to Artilux Corporation (hereinafter "Artilux").

Regarding claim 32, Wsens in view of Tivarus disclose the structure of claim 31. Wsens further discloses array of optical filters (para [0241]- each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array). Wsens in view of Tivarus fail to disclose said array of optical filters includes Near InfraRed (NIR) filters to select specific NIR wavelength ranges. Artilux, drawn to image sensor array, discloses NIR filter to select specific NIR wavelength ranges (para [0059]- the optical signal 406 may be filtered by a wavelength filter not shown in this figure, such as an NIR filter in the filter layer). It would have been obvious to a person having ordinary skill to include some of the NIR filters disclosed by Artilux to the array of optical filters to increase the performance of the filter by enabling electing specific NIR wavelength ranges (See Artilux, para [0059]).

Claims 3-5, 12, 17-19, 21, 33, 36, 38, and 42 meet the criteria set forth under PCT Article 33(2)-(3) because the prior art does not teach or fairly suggest the subject matter claimed.

The prior art for claim 3 is exemplified by Wsens, Tivarus, US 2019/0166317 A1 to Brillnics, Inc (hereinafter "Brillnics"), and US 2012/0012741 A1 (Vasylyev).

Regarding claim 3,
Wsens in view of Tivarus disclose the structure of claim 2. Wsens further discloses at least one Near InfraRed (NIR) pixel and an NIR optical filter over said NIR pixel to select specific NIR wavelength ranges (para [0192]- The wavelength range, depending on the percentage of Ge in Si, for 0% Ge can range from 840-960 nm, and with 10% Ge or less in GeSi alloy that is either relaxed or not relaxed, the wavelength can range from 840-990 nm for not relaxed GeSi layer and 840-960 nm for relax, for 20% or less Ge, the wavelength can be extended to 1000 nm and in some cases to 1250 nm for not relaxed GeSi layer and for 40% or less Ge, the wavelength can be extended to 1310 nm (It is noted the wavelength of 840-1310 nm is in the NIR wavelength range); para [0241]- each MSPD/MSAPD in an array can have a distinct bandpass filter associated with the array or with each or two or more individual MSPD/MSAPD in the array.) Wsens in view of Tivarus fail to disclose in which said pixels are configured in a Bayer array and each of at least several pixels in the Bayer array encompasses only a single hole in said photosensor wafer.

Brillnics, drawn to a CMOS sensor, discloses pixels are configured in a Bayer array (para [0068]-when the unit pixel groups are arranged in the Bayer array) that includes at least one Near InfraRed (NIR) pixel (para [0096]- The color pixels in the unit RGB pixel group 200 configured as described above not only have an inherent particular responsibility in a visible range (400 nm to 700 nm), but also have a high responsibility in a near-infrared (NIR) region (800 nm to 1,000 nm).). However, Brillnics otherwise fails to remedy the deficiencies of Wsens and Tivarus.

--see next page

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/51733

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
Box V.2 - Citations and Explanations:

Vasylyev, drawn to a light detector, discloses one lenses with one hole (Fig. 10-11; para [0089]- FIG. 10 shows a cone-shape cavity forming light input port 14; para [0084]- Light input ports 14 have the same number as the number of lenses 10 in focusing array 6 disposed on top of photovoltaic layer 4. Light input ports 14 are also distributed over surface 32 in accordance with the distribution of lenses 10 in the lens array so that there is a pairwise optical relationship between each lens 10 and the corresponding light input port 14). However, Vasylyev fails to remedy the deficiencies of Wsens , Tivarus and Brillnics.

None of the prior art discloses each of at least several pixels in the Bayer array encompasses only a single hole in said photosensor wafer. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 3, therefore claim 3 meets the criteria set out in PCT Article 33(2)-(3).

The prior art for claim 4 and 33 is exemplified by Wsens, Tivarus and Brillnics.

Regarding claim 4, Wsens in view of Tivarus disclose the structure of claim 2, but fail to disclose in which said pixels include one or more Bayer arrays at least one of which comprises a Near InfraRed (NIR) pixel, and wherein the at least one NIR pixel in at least one of said one or more Bayer arrays is larger than other pixels therein.

Brillnics, drawn to a CMOS sensor, discloses pixels include one or more Bayer arrays at least one of which comprises a Near InfraRed (NIR) pixel (para [0068]-when the unit pixel groups are arranged in the Bayer array; para [0098]- the photodiode PD22 serving as the second green (Gr) photoelectric conversion part also operate as infrared (NIR) photoelectric conversion parts.). However, Brillnics otherwise fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses wherein the at least one NIR pixel in at least one of said one or more Bayer arrays is larger than other pixels therein. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 4, therefore claim 4 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 33, Wsens in view of Tivarus disclose the structure of claim 32, but fail to disclose wherein said array of photodetectors includes some that are larger than others, and said larger photodetectors are under said NIR filters.

Brillnics, drawn to a CMOS sensor, discloses NIR photodetector are larger (para [0012]-Further, there has been known an infrared (IR, NIR) sensor in which the four pixels in a unit pixel group are replaced with one NIR dedicated pixel having a larger pixel size.). However, Brillnics otherwise fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses wherein said array of photodetectors includes some that are larger than others, and said larger photodetectors are under said NIR filters. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 33, therefore claim 33 meets the criteria set out in PCT Article 33(2)-(3).

The prior art for claim 5 and 12 is exemplified by Wsens, Tivarus and Vasylyev

Regarding claim 5, Wsens in view of Tivarus disclose the structure of claim 1, but fail to disclose in which each of said at least some of said pixels has only a single one of said holes.

Vasylyev, drawn to a light detector, discloses one lenses with one hole (Fig. 10-11; para [0084]- Light input ports 14 have the same number as the number of lenses 10 in focusing array 6 disposed on top of photovoltaic layer 4. Light input ports 14 are also distributed over surface 32 in accordance with the distribution of lenses 10 in the lens array so that there is a pairwise optical relationship between each lens 10 and the corresponding light input port 14; para [0089]- FIG. 10 shows a cone-shape cavity forming light input port 14.). However, Vasylyev fails to remedy the deficiencies of Wsens.

None of the prior art discloses in which each of said at least some of said pixels has only a single one of said holes. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 5, therefore claim 5 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 12, Wsens in view of Tivarus disclose the structure of claim 1, but fail to disclose in which at least some of said pixels have only a single hole each and said single hole is an off-center hole.

Vasylyev, drawn to a light detector, discloses photodetector have only a single hole each (Fig. 10-11; para [0089]- FIG. 10 shows a cone-shape cavity forming light input port 14; para [0084]- Light input ports 14 have the same number as the number of lenses 10 in focusing array 6 disposed on top of photovoltaic layer 4. Light input ports 14 are also distributed over surface 32 in accordance with the distribution of lenses 10 in the lens array so that there is a pairwise optical relationship between each lens 10 and the corresponding light input port 14). However, Vasylyev fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses said single hole is an off-center hole. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 12, therefore claim 12 meets the criteria set out in PCT Article 33(2)-(3).

--see next page

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/51733

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
Box V.2 - Citations and Explanations;

The prior art for claim 17 is exemplified by Wsens, Tivarus and Hirigoyen.

Regarding claim 17, Wsens in view of Tivarus disclose the structure of claim 1, but fails to discloses in which said pixels have slanted sidewalls configured to reduce crosstalk between adjacent pixels and improve optical confinement.

Hirigoyen, drawn to image sensor, discloses sidewalls (40) configured to reduce crosstalk between adjacent pixels and improve optical confinement (Fig. 4; para [0052]- Isolation region I1.. reduces optical crosstalk thanks to an optical waveguide formed by the differences in refractive indices between the substrate 10, the conductive material 30, and the optical isolator 40. para [0057]- Image sensor IS3 differs from image sensor IS2 in that the color filters F1, F2, F3 and the microlenses L1, L2, L3 are arranged on the backside of the substrate 10...the optical isolator 40 extends entirely through the trench 15). However, Hirigoyen otherwise fails to remedy the deficiencies of Wsens and Tivarus.

None of the prior art discloses said pixels have slanted sidewalls configured to reduce crosstalk between adjacent pixels and improve optical confinement. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 17, therefore claim 17 meets the criteria set out in PCT Article 33(2)-(3).

The prior art for claims 18-19, 21, 36, 38 and 42 is exemplified by Wsens and Tivarus.

Regarding claim 18, Wsens in view of Tivarus disclose the structure of claim 1. Wsens further discloses in which said holes are conformally lined with doped Si (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants). Wsens in view of Tivarus fail to disclose at least some adjacent holes are doped to opposite polarities.

None of the prior art discloses at least some adjacent holes are doped to opposite polarities. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 18, therefore claim 18 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 19, Wsens in view of Tivarus disclose the structure of claim 1. Wsens furhter discloses graphene (para [0195]- the basic steps consist of etching holes in a device wafer that can include epitaxial layers that can include doped P and/or N and/or I layers, SOI, additional dielectric coatings, metallic layers/fillers, graphene). Wsens in view of Tivarus fail to disclose at least some of said holes are conformally lined with graphene.

None of the prior art discloses at least some of said holes are conformally lined with graphene. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 19, therefore claim 19 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 21, Wsens in view of Tivarus disclose the structure of claim 1, but fail to disclose in which said pixels are in an array in which centrally located pixels are smaller in size that other pixels.

None of the prior art discloses said pixels are in an array in which centrally located pixels are smaller in size that other pixels. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 21, therefore claim 21 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 36, Wsens in view of Tivarus disclose the structure of claim 25. Wsens further discloses in which said holes are conformally lined with doped Si (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants). Wsens in view of Tivarus fail to disclose adjacent holes are doped to opposite polarities.

None of the prior art discloses adjacent holes are doped to opposite polarities. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 36, therefore claim 36 meets the criteria set out in PCT Article 33(2)-(3).

Regarding claim 38, Wsens in view of Tivarus disclose the structure of claim 25. Wsens furhter discloses graphene (para [0195]- the basic steps consist of etching holes in a device wafer that can include epitaxial layers that can include doped P and/or N and/or I layers, SOI, additional dielectric coatings, metallic layers/fillers, graphene). Wsens in view of Tivarus fail to disclose said holes are conformally lined with graphene.

None of the prior art discloses said holes are conformally lined with graphene. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 38, therefore claim 38 meets the criteria set out in PCT Article 33(2)-(3).

--see next page

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 20/51733

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
Box V.2 - Citations and Explanations:

Regarding claim 42, Wsens in view of Tivarus disclose the monolithic wafer of claim 40. Wsens further discloses in which said holes are lined with doped regions of said wafer (Fig. 42; para [0319]- The microstructure holes 4212 can be etched first partially into the low doped and/or undoped I Si and/or GeSi layer...after the microstructure hole etch, the P+ (or N+ with P and N interchanged from a P-I-N to N-I-P) layer 4284 can be formed conformally to the microstructure holes 4212 by ion implantation of the P (or N) type ions and/or by diffusion of P or N type dopants). Wsens in view of Tivarus fail to disclose adjacent holes are lined with doped regions of opposite polarities.

None of the prior art discloses adjacent holes are lined with doped regions of opposite polarities. Further, the prior art whether taken alone or combination, fails to disclose or suggest the particular arrangement of these parts as required by claim 42, therefore claim 42 meets the criteria set out In PCT Article 33(2)-(3).

Claims 1-42 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference		FOR FURTHER ACTION
5176/91538-PCT		see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/US 20/51733	21 September 2020 (21.09.2020)	24 September 2019 (24.09.2019)
Applicant		
W&WSENS DEVICES INC.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed.
      ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 59
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figures is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (July 2019)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 20/51733

A. CLASSIFICATION OF SUBJECT MATTER
IPC - H01L 27/146, 31/101, 31/102 (2020.01)
CPC - H01L 27/14609, 27/14612, 27/14643, 31/101, 31/102

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2018/0102442 A1 (W&WSENS, DEVICES INC) 12 April 2018 (12.04.2018) entire document; especially Fig. 8; Fig. 45; para [0038], para [0203-[0248], para [0333]-[0336], para [0489]	1, 2, 6-11, 13-16, 20, 22-32, 34, 35, 37, 39-41

A		3-5, 12, 17-19, 21, 33, 36, 38, 42
Y	US 2011/0156195 A1 (TIVARUS et al.) 30 June 2011 (30.06.2011) entire document; especially Fig. 13; para [0001], [0032], [0062]	1, 2, 6-11, 13-16, 20, 22-32, 34, 35, 37, 39-41

A		3-5, 12, 17-19, 21, 33, 36, 38, 42
Y	US 2012/0153127 A1 (HIRIGOYEN et al.) 21 June 2012 (21.06.2012) entire document; especially Fig. 4; para [0052], [0057]	10

A		17
Y	US 2018/0012918 A1 (ARTILUX CORPORATION) 11 January 2018 (11.01.2018) entire document, especially para [0059]	32
A	US 2019/0166317 A1 (BRILLNICS, INC) 30 May 2019 (30.05.2019) entire document; especially para [0010]-[0012]	3-4, 33
A	US 2012/0012741 A1 (VASYLYEV) 19 January 2012 (19.01.2012) entire document; especially Fig. 10-11; para [0084], [0089]	3, 5, 12

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 November 2020	17 DEC 2020
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Lee Young Telephone No. PCT Helpdesk: 571-272-4300

Form PCT/ISA/210 (second sheet) (July 2019)

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17707429
Filing Date	2022-03-29
First Named Inventor	Shih-Yuan WANG
Art Unit	
Examiner Name	Eduardo A. Rodela
Attorney Docket Number	309-0011USDIVCIP2

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20110156195		2011-06-30	Tivarus et al.	
	2	20120153127		2012-06-21	Hirigoyen et al.	
	3	20180012918		2018-01-11	Na et al.	
	4	20190166317		2019-05-30	Tanaka et al.	
	5	20120012741		2012-01-19	Vasylyev	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17707429
	Filing Date	2022-03-29
	First Named Inventor	Shih-Yuan WANG
	Art Unit	
	Examiner Name	Eduardo A. Rodela
	Attorney Docket Number	309-0011USDIVCIP2

	6	20180102442		2018-04-12				

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Copy of International Search Report and Written Opinion for PCT/US2020/051733 mailed December 17, 2020.	
	2	Copy of Written Opinion of International Search Report for PCT/US2020/051733 dated December 17, 2020.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17707429
Filing Date	2022-03-29
First Named Inventor	Shih-Yuan WANG
Art Unit	
Examiner Name	Eduardo A. Rodela
Attorney Docket Number	309-0011USDIVCIP2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	2022-04-13
Name/Print	Ivan S. Kavrukov	Registration Number	25,161

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/707,429	03/29/2022		1540	309-0011USDIVCIP2	30	3

CONFIRMATION NO. 1214

FILING RECEIPT

23432
Gary J. Gershik; John P. White;
Christopher C. Dunham; Paul Teng
90 PARK AVENUE, 21st Fl
NEW YORK, NY 10016

OC000000132993856

Date Mailed: 04/07/2022

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Shih-Yuan WANG, Palo Alto, CA;
Shih-Ping WANG, Los Altos, CA;

Applicant(s)

W&WSENS DEVICES, INC., Los Altos, CA;

Power of Attorney: The patent practitioners associated with Customer Number 139982

Domestic Priority data as claimed by applicant

This application is a DIV of 17/532,831 11/22/2021 PAT 11309444
which is a CIP of 17/182,954 02/23/2021
which is a DIV of 16/528,958 08/01/2019 PAT 11121271
which is a CIP of 15/797,821 10/30/2017 PAT 10446700
which is a CON of 14/947,718 11/20/2015 PAT 10622498
which is a CON of PCT/US14/39208 05/22/2014
which claims benefit of 61/826,446 05/22/2013 *
and claims benefit of 61/834,873 06/13/2013
and claims benefit of 61/834,021 06/12/2013 *
and claims benefit of 61/905,109 11/15/2013
(*)Data provided by applicant is not consistent with PTO records.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: No

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/06/2022

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/707,429**

Projected Publication Date: 07/14/2022

Non-Publication Request: No

Early Publication Request: No
**** SMALL ENTITY ****
Title

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign

patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/707,429

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	80		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	350		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	400		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	30 minus 20 =	* 10	x 50 =	500	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*	x 240 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			210			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	1540		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.



United States Patent and Trademark Office

Office of the Chief Financial Officer

Document Code:WFEE

User :C41739

Sale Accounting Date:04/01/2022

Sale Item Reference Number	Effective Date
17707429	03/29/2022

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I202241C43293608	2081	UTILITY APPL SIZE FEE PER 50 SHEETS >100	$210.00	Deposit Account

REMARKS

Applicant submits that the claims submitted in this paper are supported by the disclosure of the parent application and do not raise new matter issues. The only change is making claim 29 depend on claim 27 rather than on claim 28.

If the Examiner finds that a telephone discussion might advance prosecution, the Examiner is respectfully requested to call the undersigned applicant's representative.

The Patent Office is hereby authorized to charge any required fees in connection with this paper, and to credit any overpayment, to our Deposit Account No. 600125.

Respectfully Submitted,

WISSING MILLER LLP
Attorney for Applicants

By: /Ivan S. Kavrukov/
Ivan S. Kavrukov
Reg. No. 25,161
Tel.: (917) 945-0121

AMENDMENTS TO THE CLAIMS:

1. (Previously presented) A semiconductor device with deliberately formed in-pillar holes comprising:

a laterally extending array of pillars that have rectangular cross-sections in a horizontal plane and are elongated in an up-down direction;

pillar-separating dielectric between sidewalls of adjacent pillars;

wherein each pillar comprises:

a first doped semiconductor region;

a first undoped or low-doped semiconductor region below the first doped semiconductor region;

a second doped semiconductor region below the first undoped or low-doped semiconductor region;

one or more deliberately formed, solid dielectric-filled, in-pillar holes extending into the pillar;

a top electrical contact; and

a bottom electrical contact;

wherein said top and bottom electrical contacts are configured to provide reverse-bias from an external source for operation of said device to convert light photons incident on said pillar to electrons;

a base dielectric below the array of pillars;

wherein said pillars;

are laterally spaced center to center by 10-10,000 nanometers; and

have up-down lengths of said first undoped or low-doped semiconductor regions in the range of 100-5000 nanometers;

wherein said pillars, in-pillar holes, and pillar-separating dielectric:

increase photon absorption of said device of incident light compared to a like device lacking said one or more in-pillar holes; and

facilitate operation of said device with infrared incident light; and

wherein said device is CMOS compatible for mass production using CMOS foundries.

2. (Previously presented) The device of claim 1, in which each of said pillars further includes:
   a second undoped or low-doped semiconductor regions under the second doped semiconductor regions of said pillars;
   third doped semiconductor regions under the second undoped or low-doped semiconductor regions and above said base dielectric; and
   wherein said top and bottom electrical contacts are configured to provide reverse-bias from an external source in the range of -5 to -50 Volts sufficient for operations of said device as an avalanche photodiode.

3. (Previously presented) The device of claim 2, in which said third doped semiconductor regions of said pillars form a laterally continuous region coupled to a plurality of said pillars.

4. (Previously presented) The device of claim 2, in which the top electrical contact is a transparent, laterally continuous region that is electrically coupled to a plurality of said pillars.

5. (Previously presented) The device of claim 2, in which said second undoped or low-doped region has a thickness in the 100-2,000 nanometers range.

6. (Previously presented) The device of claim 2, in which the first and second doped semiconductor regions are doped to the same polarity and the third doped semiconductor region is doped to an opposite polarity.

7. (Previously presented) The device of claim 2, In which each of said first doped semiconductor region and said first undoped or low-doped semiconductor regions is a Ge region and each of said second doped semiconductor region, said second undoped or low-doped semiconductor region, and said third doped semiconductor region is an Si region.

8. (Previously presented) The device of claim 2, in which at least one of the first and second doped regions and first and second undoped or low-doped regions is an SiGe region.

9. (Previously presented) The device of claim 2, in which said pillar-separating dielectric is along sidewalls of at least said first and second doped semiconductor regions and said first and second undoped or low-doped semiconductor regions.

10. (Previously presented) The device of claim 2, in which each of said pillars has a plurality of said one or more in-pillar holes.

11. (Previously presented) The device of claim 2, in which each of said pillars has only one of said one or more in-pillar holes.

12. (Previously presented) The device of claim 2, in which said one or more in-pillar holes extend to a depth in the range of 100-10,000 nanometers.

13. (Previously presented) The device of claim 2, in which said one or more in-pillar holes extend into said first undoped or low-doped semiconductor region.

14. (Previously presented) The device of claim 2, in which said one or more in-pillar holes are pyramid-shaped.

15. (Previously presented) The device of claim 2, in which the gain of said device operating as an avalanche photodiode is greater than two.

16. (Previously presented) The device of claim 1, in which said one or more in-pillar holes are pyramid-shaped.

17. (Previously presented) The device of claim 1, in which the first doped semiconductor region and the second doped semiconductor region are doped to opposite polarities.

18. (Previously presented) The device of claim 1, in which each of the first doped semiconductor region and the first undoped or low-doped semiconductor region is a Ge region and the second doped semiconductor region is an Si region.

19. (Previously presented) The device of claim 1, in which each of said pillars has a plurality of said one or more in-pillar holes.

20. (Previously presented) The device of claim 1, in which each of said pillars has only one of said one or more in-pillar holes.

21. (Previously presented) The device of claim 1, in which said one or more in-pillar holes extend into said first undoped or low-doped semiconductor region.

22. (Previously presented) The device of claim 1, in which each of said pillars has at least two of said one or more in-pillar holes and said at least two of said in-pillar holes partly overlap.

23. (Previously presented) The device of claim 1, in which at least one of the first and second doped regions and the first undoped or low-doped regions is an SiGe region.

24. (Previously presented) The device of claim 1, in which the top electrical contact is a transparent, laterally continuous region that is electrically coupled to a plurality of said pillars.

25. (Previously presented) The device of claim 1, in which said second doped semiconductor regions of said pillars form a laterally continuous region coupled to a plurality of said pillars.

26. (Previously presented) The device of claim 1, in which the first doped semiconductor region is an amorphous Si region, the first undoped or low-doped semiconductor region is a crystalline Ge region, and the second doped semiconductor region is a crystalline Si region.

27. (Previously presented) A semiconductor device with deliberately formed in-pillar holes comprising:

an array of pillars that have rectangular cross-sections in a horizontal plane;

wherein each pillar comprises:

a first doped semiconductor region;

a second doped semiconductor region;

a first undoped or low-doped semiconductor region between the first and second doped semiconductor regions;

one or more deliberately formed, solid dielectric-filled, in-pillar holes extending into the pillar;

a first electrical contact; and

a second electrical contact;

wherein said first and second electrical contacts are configured to provide reverse-bias from an external source for operation of said device to convert light photons incident on said pillar to electrons;

a base dielectric under the array of pillars;

wherein said pillars;

are spaced from each other center to center by less than 10,000 nanometers;

increase photon absorption of said device of incident light compared to a like device lacking said one or more in-pillar holes; and

wherein said device is CMOS compatible for mass production using CMOS foundries.

28. (Previously presented) The device of claim 27, in which each of said pillars has only one of said one or more in-pillar holes.

29. (Currently Amended) The device of claim ~~28~~ 27, in which each of said pillars further includes:

a third doped semiconductor region over said base dielectric;

a second undoped or low-doped semiconductor region between the second and third doped semiconductor regions; and

wherein said first and second electrical contacts are configured to provide reverse-bias from an external source in the range of -5 to -50 Volts sufficient for operations of said device as an avalanche photodiode.

30. (Previously presented) A semiconductor device with deliberately formed in-pillar holes comprising:

an array of pillars that have rectangular cross-sections in a horizontal plane;

pillar-separating dielectric between sidewalls of adjacent pillars;

wherein each pillar comprises:

a first doped semiconductor region;

a second doped semiconductor region;

a third doped semiconductor region;

a first undoped or low-doped semiconductor region between of the first and second doped semiconductor regions;

a second undoped or low-doped semiconductor region between the second and third doped semiconductor regions;

one or more deliberately formed, solid dielectric-filled, in-pillar holes extending selected distances into the pillar;

a first electrical contact; and

a second electrical contact;

wherein said first and second electrical contacts are configured to provide reverse-bias from an external source in the range of -5 to -50 Volts for operation of said device as an avalanche photodiode with a gain greater than two;

a base dielectric under the array of pillars;

wherein said pillars;

are spaced from each other center to center by less than 10,000 nanometers; and

have a dimension of said first undoped or low-doped semiconductor regions that is less than 5000 nanometers;

wherein said pillars, in-pillar holes, and pillar-separating dielectric:

increase photon absorption of said device of incident light compared to a like device lacking said one or more in-pillar holes; and

facilitate operation of said device with infrared incident light; and

wherein said device is CMOS compatible for mass production using CMOS foundries.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Shih-Yuan WANG et al.

Serial No.: 17/707,429

Filing Date: March 29, 2022

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Conf. No. 1214

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: March 31, 2022

I hereby certify that this correspondence is being transmitted via Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

SECOND PRELIMINARY AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Prior to examination and the issuance of the first Office Action, please amend the above-identified application as follows:

Amendments to the claims start on page 2. (The only change is making claim 29 depend on claim 27 rather than on claim 28.)

Remarks start on page 9.

Electronic Acknowledgement Receipt

EFS ID:	45367509
Application Number:	17707429
International Application Number:	
Confirmation Number:	1214
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	309-0011USDIVCIP2
Receipt Date:	31-MAR-2022
Filing Date:	
Time Stamp:	15:50:28
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Preliminary Amendment	309-0011USDIVCIP2_SecondPreliminaryAmendment_FINAL.pdf	505804 09d7d52107a9a4e3d737f7099a646e9db83110dc	no	9

Warnings:

Information:	
Total Files Size (in bytes):	505804

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/26 (04-14)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0011USCIP2

In re Application of: Shih-Yuan WANG

Application No.: 17/707,429

Filed: March 29, 2022

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 10,700,225 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
March 29, 2022 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	17707429
Filing Date:	
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Attorney Docket Number:	309-0011USDIVCIP2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
STATUTORY OR TERMINAL DISCLAIMER	2814	11	170	1870
		Total in USD ($)		**1870**

PTO/AIA/25 (04-13)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION	Docket Number (Optional) 309-0011USDIVCIP2

In re Application of: Shih-Yuan WANG

Application No.: 17/707,429

Filed: March 29, 2022

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending **reference** Application Number 17/532,831, filed, November 22, 2021, as the term of any patent granted on said **reference** application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending **reference** application. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the **reference** application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term of any patent granted on said **reference** application, "as the term of any patent granted on said **reference** application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending **reference** application," in the event that: any such patent granted on the pending **reference** application expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

Ivan S. Kavrukov	March 29, 2022
Signature	Date
/Ivan S. Kavrukov/	
Typed or printed name	
Attorney of Record	917-945-0121
Title	Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) is included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	45347829
Application Number:	17707429
International Application Number:	
Confirmation Number:	1214
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	23432
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	309-0011USDIVCIP2
Receipt Date:	29-MAR-2022
Filing Date:	
Time Stamp:	18:03:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1870
RAM confirmation Number	E20223SI04232616
Deposit Account	600125
Authorized User	Mary Ellen Finnegan

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Petition to make special based on Age/ Health	309-0011USDIVCIP2_PetitionToMakeSpecialBasedOnAge.pdf	193085 6958d2c46c943437038228650d353bdf86769daa	no	2
Warnings:					
Information:					
2	Terminal Disclaimer Filed	309-0011USDIVCIP2_TerminalDisclaimer_9496435.pdf	165491 72cdbe5040ed76e05b25b1812632c51260125df4	no	2
Warnings:					
Information:					
3	Terminal Disclaimer Filed	309-0011USDIVCIP2_TerminalDisclaimer_9525084.pdf	165876 a390921954c7f3928da21cc372bacb28166c1c97	no	2
Warnings:					
Information:					
4	Terminal Disclaimer Filed	309-0011USDIVCIP2_TerminalDisclaimer_9530905.pdf	165289 2453b044a516b3205db26b0eef0aac8f297cd4ff	no	2
Warnings:					
Information:					
5	Terminal Disclaimer Filed	309-0011USDIVCIP2_TerminalDisclaimer_9818893.pdf	155596 7fef77e90bd7c5fca311cb102b101de2dab5c216	no	2
Warnings:					
Information:					
6	Terminal Disclaimer Filed	309-0011USDIVCIP2_TerminalDisclaimer_10446700.pdf	155599 7c8be4cca9cf180fd6666dfed2f0a49940802b75	no	2
Warnings:					
Information:					

7	Terminal Disclaimer Filed	309-0011USDIVCIP2_TerminalDisclaimer_10468543.pdf	155597 db5f58e5c3a143624251adf458615a8171624841	no	2
Warnings:					
Information:					
8	Terminal Disclaimer Filed	309-0011USDIVCIP2_TerminalDisclaimer_10622498.pdf	155595 9a16837a49ac86fbc9258effa0d934e09a774860	no	2
Warnings:					
Information:					
9	Terminal Disclaimer Filed	309-0011USDIVCIP2_TerminalDisclaimer_11121271.pdf	155653 263ae453804dd59925952faf9c1174051604bed0	no	2
Warnings:					
Information:					
10	Terminal Disclaimer Filed	309-0011USDIVCIP2_TerminalDisclaimer_17182954.pdf	240854 5a25c841646773090733a61df6c32582f178c073	no	2
Warnings:					
Information:					
11	Preliminary Amendment	309-0011USDIVCIP2_PreliminaryAmendment_FINAL.pdf	675257 8d20b45d40abdde79fd310a8210e09a94de58812	no	26
Warnings:					
Information:					
12	Terminal Disclaimer Filed	309-0011USDIVCIP2_TerminalDisclaimer_10700225.pdf	160519 c40e87aaf9133eb852dbe568391ecf7f6a7418ae	no	2
Warnings:					
Information:					
13	Terminal Disclaimer Filed	309-0011USDIVCIP2_TerminalDisclaimer_17532831.pdf	246271 3e8af15d22b16d965606f860a37ef88e4e16f78d	no	2
Warnings:					
Information:					

14	Fee Worksheet (SB06)	fee-info.pdf	38111 24f6dffcbdc0feb9fce7d701306a8c8489c509cc	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	2828793

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Amendments to the specification:

Please replace paragraphs [0001] with the following:

[0001] This application is a DIV of 17/532,831 filed 11/22/2021, which is a CIP of 17/182,954 filed 02/23/2021, which is a DIV of 16/528,958 filed 08/01/2019 now PAT 11,121,271, which is a CIP of 15/797,821 filed 10/30/2017 now PAT 10446700, which is a continuation of 14/947,718 filed 11/20/2015, which is a CONT of PCT/US14/39208 filed 05/22/2014, which claims priority to 61/826,446 filed 05/05/2013 and claims priority to 61/834,873 filed 06/13/2013 and claims priority to 61/834,021 filed 07/04/2013 and claim priority to 61/905,109 filed 11/15/2013.

Said 16/528,958 additionally is a CIP of 16/296,985 filed 03/8/2019 now Pat 10468543, a CIP of 16/042,535 filed 07/23/2018 now Pat 10700225, a CIP of PCT/US18/ 57963 filed 10/29/2018, and a CIP of PCT/US18/43289 filed 07/23/2018.

Said 15/797,821 additionally is CIP of PCT/US16/67977 filed 12/21/2016, and a CIP of 15/309,922 filed 11/9/2016 now PAT 9,818,893.

Said 16/296,985 is a CONT of said 15/797,821.

Said 15/309,922 is Nat'l Stage of PCT/US15/61120 filed 11/17/2015, CONT of 14/943,898 filed 11/17/2015 now PAT 9,530,905, and a CONT of 14/945,003 filed 11/18/2015 now PAT 9,525,084.

14/892,821 filed 11/20/2015 is Nat'l Stage of said PCT/US14/39208.

This application incorporates by reference the entire contents of each of the patents and patent application identified above and of the respective priority applications to which they claim priority, and claims priority to each of said patent applications, patents, and priority applications.

APPENDIX A -- Partial chain of parent applications

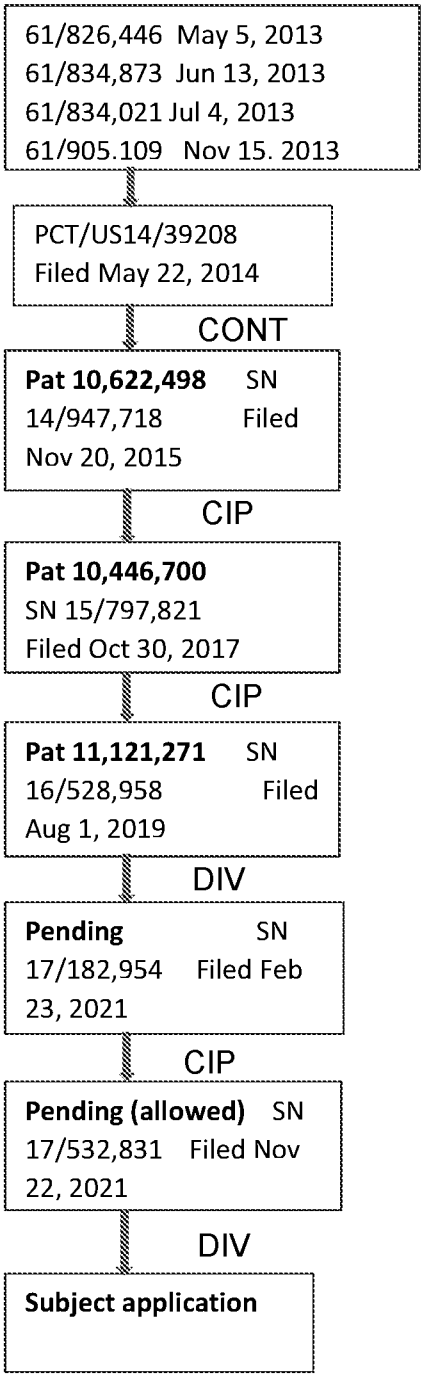


TABLE (pointing to non-limiting examples of support for claim elements)

Claims in division of SN 17/532,831	**Examples of support in SN 14/947,718 filed Nov 15, 2015 and claiming priority to PCT/ US14/39208 filed May 22, 2014 and claiming priority to U.S. Provisional filed May 22, Jun 13, July 5, and Nov 15, 2013**
1. A semiconductor device with deliberately formed in-pillar holes comprising:	¶81 ("... the photosensor can be ... optoelectronic device that converts photons to electrons.) ¶71 ("... individual features of one or several of the specific embodiments described herein can be used in combination with specific features or [sic, of] other described embodiments.)
a laterally extending array of pillars that have rectangular cross-sections in a horizontal plane and are elongated in an up-down direction;	Figs. 5A-B: Pillars 524 are elongated in up-down direction when the device is oriented as in Fig. 5B. ¶232 ("... for example a rectangular pillar ... .") ¶132 ("... the shape of the pillars can be ... rectangle ... .") Fig. 46: one of the illustrates shapes is a rectangle (square). ¶228 ("Fig. 46 shows a microstructured pillar ... rectangle ... .") Fig. 15C: pillars 1524.
pillar-separating dielectric between sidewalls of adjacent pillars;	Figs. 5A-B: regions around pillars 524. Fig. 15C: dielectric 1522. ¶127 ("... a filler 916 is used to fill or partially fill the space between the Si pillars 914 ... .") ¶146 "The sidewalls of the microstructure patterns (pillars or holes) are passivated with dielectric ...."
wherein each pillar comprises:	Fig. 5B: Each of pillars 524. Fig. 15C: each of pillars 1524.
a first doped semiconductor region;	Figs. 5A-B: region 510. ¶114-115. Fig. 15C: region 1514.
a first undoped or low-doped semiconductor region below the first doped semiconductor region;	Figs. 5A-B: region 508. ¶114-115. Fig. 15C: region 1512.

a second doped semiconductor region below the first undoped or low-doped semiconductor region;	Figs. 5A-B: region 506. ¶114-115. Fig. 15C: region 1510.
one or more deliberately formed, solid dielectric-filled, in-pillar holes extending into the pillar;	Fig. 49: "Pillar with hole." ¶232 ("… in addition, hole(s) can exist in a pillar … .") ¶122: "…passivating the sidewalls of the of the microstructure patterns (pillars or holes with thermal oxide …. Planarization (filler step) using … (PECVD) of dielectrics …." ¶146: "…using polyimide or spin-on glass to partially fill the holes …."
a top electrical contact; and	Fig. 5B: top contact 528 and/or 526. Fig. 15C: top contact connected to source V.
a bottom electrical contact;	Fig. 5B: bottom contact 530. Fig. 15C: bottom contact connected to source V.
wherein said top and bottom electrical contacts are configured to provide reverse-bias from an external source for operation of said device to convert light photons incident on said pillar to electrons;	Fig. 5B: voltage source V. ¶116 ("The PD 520 is operated in a reverse-bias mode, with negative voltage on the anode (P^+ layer 510 via P-ohmic and bond contact metal 528) and positive voltage on the cathode (N^+ layer 506 via N-ohmic bond contact metal 530 … .") Fig. 15C: Voltage source V.
a base dielectric below the array of pillars;	Fig. 5B: region 504 labeled "BOX/SOI." Fig. 15C: substrate 1502 (with dielectric 1504). ¶152: "… the substrate 1502 can include a BOX or SOI layer 1502."
wherein said pillars;	Fig. 5B: Pillars 524. Fig. 15C: pillars 1524.

are laterally spaced center to center by 10-10,000 nanometers; and	Figs. 43-46: "C-C 100-10,000 nm."

have up-down lengths of said first undoped or low-doped semiconductor regions in the range of 100-5000 nanometers;	¶115 ("… I high field absorption region 508 with … thickness ranging approximately from 0.1 to 5 micrometers …")
wherein said pillars, in-pillar holes, and pillar-separating dielectric:	Fig. 5B, pillars 524; Fig. 49 "Pillar with hole;" regions 524 or 1522. ¶146 "The sidewalls of the microstructure patterns (pillars or holes) are passivated with dielectric …."
increase photon absorption of said device of incident light compared to a like device lacking said one or more in-pillar holes; and	¶97 ("… enhanced absorption coefficient over the bulk absorption coefficient … .") Fig. 3B shows QE (roughly absorption) of a conventional photodetector (without microstructures) at 850 nm incident light (infrared); Fig. 4B shows that absorption at the same incident wavelength is increased for a device with microstructures; and Fig. 4D shows increased absorption at 1100 nm wavelength.
facilitate operation of said device with infrared incident light; and	Increased absorption at 850 nm and 1100 nm light (compare Fig. 3B with Figs. 4B and 4D) facilitates operation with infrared incident light.
wherein said device is CMOS compatible for mass production using CMOS foundries.	¶82 (… advantageous for mass production using CMOS foundries.)
2. The device of claim 1, in which each of said pillars further includes:	
a second undoped or low-doped semiconductor regions under the second doped semiconductor regions of said pillars;	Fig. 15C: region 1508.
third doped semiconductor regions under the second undoped or low-doped semiconductor regions and above said base dielectric; and	Fig. 15C: region 1506.

wherein said top and bottom electrical contacts are configured to provide reverse-bias from an external source in the range of -5 to -50 Volts sufficient for operations of said device as an avalanche photodiode.	Fig. 15C: voltage source V. ¶169: "... reverse bias of -5 to -50 volts ..."
3. The device of claim 2, in which said third doped semiconductor regions of said pillars form a laterally continuous region coupled to a plurality of said pillars.	Fig. 15C: region 1506. See also the doped P-SI region in Fig. 14B.
4. The device of claim 2, in which the top electrical contact is a transparent, laterally continuous region that is electrically coupled to a plurality of said pillars.	Fig. 15C: region 1526. ¶146: "...transparent conducting oxide ..."
5. The device of claim 2, in which said second undoped or low-doped region has a thickness in the 100-2,000 nanometers range.	¶124: "...electronic gain layer of the APD) with thickness ranging approximately from 0.1 to 2.0 μm ..."
6. The device of claim 2, in which the first and second doped semiconductor regions are doped to the same polarity and the third doped semiconductor region is doped to an opposite polarity.	Fig. 15C: regions 1514 and 1510 are doped to P-type polarity and region 1506 is doped to N-type polarity.

7. The device of claim 2, In which each of said first doped semiconductor region and said first undoped or low-doped semiconductor regions is a Ge region and each of said second doped semiconductor region, said second undoped or low-doped semiconductor region, and said third doped semiconductor region is an Si region.	Fig. 15C: regions 1514 and 1512 are Ge regions while regions 1510 and 1508 are Si regions.
8. The device of claim 2, in which at least one of the first and second doped regions and first and second undoped or low-doped regions is an SiGe region.	¶¶ 143, 233: "... the microstructures pillar . . . can be fabricated in ... SiGe ..."
9. The device of claim 2, in which said pillar-separating dielectric is along sidewalls of at least said first and second doped semiconductor regions and said first and second undoped or low-doped semiconductor regions.	Fig. 15C: dielectric 1522 is at the sides of regions 1514, 1512, 1510, and 1508.
10. The device of claim 2, in which each of said pillars has a plurality of said one or more in-pillar holes.	Fig. 49; ¶ 232: "... hole(s) can exist in a pillar ..."
11. The device of claim 2, in which each of said pillars has only one of said one or more in-pillar holes.	Fig. 49: "Pillar with hole."
12. The device of claim 2, in which said one or more in-pillar holes extend to a depth in the range of 100-10,000 nanometers.	¶ 231: "... the holes have ... depths ranging from 0.1 to 10 microns."
13. The device of claim 2, in which said one or more in-pillar holes extend	¶ 198: "The microstructured holes 2722 (or space around pillars) ... can be partially into the 'I' layer."

into said first undoped or low-doped semiconductor region.	
14. The device of claim 2, in which said one or more in-pillar holes are pyramid-shaped.	¶234 ("... holes ... shapes such as pyramids ...")
15. The device of claim 2, in which the gain of said device operating as an avalanche photodiode is greater than two.	¶ 9: "... at wavelengths of 850 nanometers ... a gain greater than 2..." ¶ 10: "... at source signal wavelengths of 1750 nanometers ... a gain of greater than 2."
16. The device of claim 1, in which said one or more in-pillar holes are pyramid-shaped.	¶234 ("... holes ... shapes such as pyramids ...")
17. The device of claim 1, in which the first doped semiconductor region and the second doped semiconductor region are doped to opposite polarities.	Figs. 5A-B: region 510 and 506 are doped to opposite polarities.
18. The device of claim 1, in which each of the first doped semiconductor region and the first undoped or low-doped semiconductor region is a Ge region and the second doped semiconductor region is an Si region.	Fig. 15C: regions 1514 and 1512 are Ge regions while region 1510 is Si region.
19. The device of claim 1, in which each of said pillars has a plurality of said one or more in-pillar holes.	Fig. 49; ¶ 232: "... hole(s) can exist in a pillar ..."
20. The device of claim 1, in which each of said pillars has only one of said one or more in-pillar holes.	Fig. 49: "Pillar with hole."

21. The device of claim 1, in which said one or more in-pillar holes extend into said first undoped or low-doped semiconductor region.	¶ 198: "The microstructured holes 2722 (or space around pillars) … can be partially into the 'I' layer."
22. The device of claim 1, in which each of said pillars has at least two of said one or more in-pillar holes and said at least two of said in-pillar holes partly overlap.	Fig. 46 shows examples of partly overlapping holes.
23. The device of claim 1, in which at least one of the first and second doped regions and the first undoped or low-doped regions is an SiGe alloy region.	¶¶ 143, 233: "… the microstructures pillar . . . can be fabricated in … SiGe …"
24. The device of claim 1, in which the top electrical contact is a transparent, laterally continuous region that is electrically coupled to a plurality of said pillars.	Fig. 15C: region 1526. ¶146: "…transparent conducting oxide …"
25. The device of claim 1, in which said second doped semiconductor regions of said pillars form a laterally continuous region coupled to a plurality of said pillars.	Figs. 5A-B: region 506. See also the doped P-SI region in Fig. 14B.

26. The device of claim 1, in which the first doped semiconductor region is an amorphous Si region, the first undoped or low-doped semiconductor region is a crystalline Ge region, and the second doped semiconductor region is a crystalline Si region.	¶ 98: "… photodiodes and avalanche photodiodes operating in reverse bias mode … can be homo or heterojunction, crystalline or amorphous or any combination thereof." ¶ 247: "The microstructures can be within each other such as pillar(s) in hole(s), hole(s) in pillar(s) and void(s) can be in the pillar, and buried and or embedded in any layer of the semiconductor heterogeneous or homogeneous. The material used includes semiconductors such as Si, Ge, GeSi, Ge on Si, and the III-V group material family of InP, GaN, InGaAsP, GaAs, and other semiconductors such as ZnO, CdTe, CuInGaSe (CIGS), amorphous Si, or any amorphous semiconductor and or microcrystalline and crystalline semiconductor. The material can be a combination of amorphous, microcrystalline, crystalline heterogeneous and or homogeneous."

27. A semiconductor device with deliberately formed in-pillar holes comprising:	Figs. 5A-B; Fig. 15C. ¶71 ("… individual features of one or several embodiments described herein can be used in combination with specific features or [sic, of] other described embodiments.)
an array of pillars that have rectangular cross-sections in a horizontal plane;	Figs. 5A-B: Pillars 524 when the device is oriented as in Fig. 5B. Fig. 15C: pillars 1524. ¶132 ("… the shape of the pillars can be … rectangle … .") ¶228 ("Fig. 46 shows a microstructured pillar … rectangle … .") ¶232 ("Fig. 49 shows … for example a rectangular pillar … .") Fig. 46: one of the illustrated shapes is a rectangle (square).
pillar-separating dielectric between sidewalls of adjacent pillars;	Fig. 15C: dielectric 1522. ¶198 ("… space around pillars … .") Fig. 46: space surrounding the closed shapes, one example of which is a rectangular pillar. ¶127 ("… a filler 916 is used to fill or partially fill the space between the Si pillars 914 … .")
wherein each pillar comprises:	Figs. 5B, 15C: each of pillars 524 1524.
a first doped semiconductor region;	Figs. 5A-B; region 510. See ¶114-115 Fig. 15C: region 1514.
a second doped semiconductor region;	Figs. 5A-B: region 506. See ¶114-115 Fig. 15C: region 1510.
a first undoped or low-doped semiconductor region between the first and second doped semiconductor regions;	Figs. 5A-B: region 508. See ¶114-115 Fig. 15C: region 1512.

one or more deliberately formed, solid dielectric-filled, in-pillar holes extending into the pillar;	Fig. 49 shows "Pillar with hole." ¶232 ("…hole(s) can exist in a pillar …") ¶122: "…passivating the sidewalls of the of the microstructure patterns (pillars or holes with thermal oxide …. Planarization (filler step) using … (PECVD) of dielectrics …."
a first electrical contact; and	Fig. 5B: top contact 528 and/or 526. Fig. 15C: top contact connected to source V.
a second electrical contact;	Fig. 5B: bottom contact 530. Fig. 15C: bottom contact connected to source V.
wherein said first and second electrical contacts are configured to provide reverse-bias from an external source for operation of said device to convert light photons incident on said pillar to electrons;	Fig. 5B: voltage source V. Fig. 15C: Voltage source V. ¶116 ("The PD 520 is operated in a reverse-bias mode, with negative voltage on the anode (P^+ layer 510 via P-ohmic and bond contact metal 528) and positive voltage on the cathode (N^+ layer 506 via N-ohmic bond contact metal 530 … .") ¶81 ("… the photosensor can be … optoelectronic device that converts photons to electrons.)
a base dielectric under the array of pillars;	Fig. 5B: region 504 labeled "BOX/SOI." Fig. 15C: dielectric 1504.
wherein said pillars;	Fig. 5B: Pillars 524. Fig. 15C: pillars 1524.
are spaced from each other center to center by less than 10,000 nanometers;	Figs. 43-46: each shows C-C spacing 100-10,000 nm.
have a dimension of said first undoped or low-doped semiconductor regions that is less than 5000 nanometers;	¶115 ("… I high field absorption region 508 with … thickness ranging approximately from 0.1 to 5 micrometers … .")

increase photon absorption of said device of incident light compared to a like device lacking said one or more in-pillar holes; and	¶97 ("... enhanced absorption coefficient over the bulk absorption coefficient ... .") Fig. 3B shows QE (roughly absorption) of a conventional photodetector (without microstructures) at 850 nm incident light (infrared) and Fig. 4B shows that absorption at the same incident wavelength is increased for a device with microstructures.
facilitate operation of said device with infrared incident light; and	Fig. 3B shows QE (roughly absorption) of a conventional photodetector (without microstructures) at 850 nm incident light (infrared) and Fig. 4B shows that absorption at the same incident wavelength is increased for a device with microstructures. ¶ 9: ". . . at wavelengths of 850 nanometers . . . a gain greater than 2. . .." ¶ 10: ". . . at source signal wavelengths of 1750 nanometers . . . a gain of greater than 2."
wherein said device is CMOS compatible for mass production using CMOS foundries.	¶82 (... advantageous for mass production using CMOS foundries.)
28. The device of claim 27, in which each of said pillars has only one of said one or more in-pillar holes.	Fig. 49: "Pillar with hole."
29. The device of claim 28, in which each of said pillars further includes:	Fig. 15C: region 1508.
a third doped semiconductor region over said base dielectric;	Fig. 15C: region 1506.
a second undoped or low-doped semiconductor region between the second and third doped semiconductor regions; and	Fig. 15C: region 1508.

wherein said first and second electrical contacts are configured to provide reverse-bias from an external source in the range of -5 to -50 Volts sufficient for operations of said device as an avalanche photodiode.	Fig. 15C: voltage source V. ¶169: ". . . reverse bias of -5 to -50 volts is applied . . . ."
30. A semiconductor device with deliberately formed in-pillar holes comprising:	Fig. 15C ¶71 ("… individual features of one or several of the specific embodiments described herein can be used in combination with features or [sic, of] other described embodiments.)
an array of pillars that have rectangular cross-sections in a horizontal plane;	¶132 ("… the shape of the pillars can be … rectangle … .") Fig. 46: one of the illustrates shapes is a rectangle (square). ¶228 ("Fig. 46 shows a microstructured pillar … rectangle … .") ¶232 ("Fig. 49 shows … for example a rectangular pillar … .") Fig. 15C: pillars 1524.
pillar-separating dielectric between sidewalls of adjacent pillars;	Fig. 15C: dielectric 1522. ¶198 ("The microstructured … space around pillars … .") Fig. 46: the space surrounding the closed shapes, one example of which is a rectangular pillar. ¶127 ("… a filler 916 is used to fill or partially fill the space between the Si pillars 914 … .")
wherein each pillar comprises:	Fig. 15C: Each of pillars 1524.
a first doped semiconductor region;	Fig. 15C: region 1514.
a second doped semiconductor region;	Fig. 15C: region 1510.
a third doped semiconductor region;	Fig. 15C: region 1506.

a first undoped or low-doped semiconductor region between of the first and second doped semiconductor regions;	Fig. 15C: region 1512.
a second undoped or low-doped semiconductor region between the second and third doped semiconductor regions;	Fig. 15C: region 1508.
one or more deliberately formed, solid dielectric-filled, in-pillar holes extending selected distances into the pillar;	Fig. 49 shows "Pillar with hole." ¶232 ("… in addition, hole(s) can exist in a pillar … .") ¶122: "…passivating the sidewalls of the of the microstructure patterns (pillars or holes with thermal oxide …. planarization (filler step) using … (PECVD) of dielectrics …."
a first electrical contact; and	Fig. 15C: top electrical contact connected to voltage source V.
a second electrical contact;	Fig. 15C: bottom electrical contact connected to voltage source V.
wherein said first and second electrical contacts are configured to provide reverse-bias from an external source in the range of -5 to -50 Volts for operation of said device as an avalanche photodiode with a gain greater than two;	Fig. 15C: voltage source V. ¶169: ". . . reverse bias of -5 to -50 volts is applied . . . ."¶81 ("… the photosensor can be … optoelectronic device that converts photons to electrons.)
a base dielectric under the array of pillars;	Fig. 15C: region 1504. ¶152: ". . . the substrate 1502 can include a BOX or SOI layer 1502."

wherein said pillars;	Fig. 15C: pillars 1524.
are spaced from each other center to center by less than 10,000 nanometers; and	Figs. 43-46: each shows C-C spacing 100-10,000 nm.
have a dimension of said first undoped or low-doped semiconductor regions that is less than 5000 nanometers;	¶115 ("... I high field absorption region ... thickness ranging approximately from 0.1 to 5 micrometers ... .")
wherein said pillars, in-pillar holes, and pillar-separating dielectric:	Fig. 15C: pillars 1524, in-pillar holes (Fig. 49), an pillar- separating dielectric 1522:
increase photon absorption of said device of incident light compared to a like device lacking said one or more in-pillar holes; and	¶97 ("... enhanced absorption coefficient over the bulk absorption coefficient ... .") Fig. 3B shows QE (roughly absorption) of a conventional photodetector (without microstructures) at 850 nm incident light (infrared) and Fig. 4B shows that absorption at the same incident wavelength is increased for a device with microstructures.
facilitate operation of said device with infrared incident light; and	Fig. 3B shows QE (roughly absorption) of a conventional photodetector (without microstructures) at 850 nm incident light (infrared) and Fig. 4B shows that absorption at the same incident wavelength is increased for a device with microstructures. ¶ 9: ". . . at wavelengths of 850 nanometers . . . a gain greater than 2. . .." ¶ 10: ". . . at source signal wavelengths of 1750 nanometers . . . a gain of greater than 2."
wherein said device is CMOS compatible for mass production using CMOS foundries.	¶82: "... advantageous for mass production using CMOS foundries."

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor: Shih-Yuan WANG et al.

Serial No.: 17/707,429 Group Art Unit: 2863

Filing Date: March 29, 2022 Examiner: RODELA, EDUARDO A

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

Wissing Miller LLP
Industrious at Hudson Yards
31 Hudson Yards, 11th Floor
New York, NY 10001

CERTIFICATE OF ELECTRONIC FILING

Date of Transmission: March 29, 2022

I hereby certify that this correspondence is being transmitted via Electronic Filing Services on the date indicated above.

Mary Ellen Finnegan
(Typed or printed name of person signing transmittal)

/Mary Ellen Finnegan/
(Signature of person signing transmittal)

PRELIMINARY AMENDMENT

Amendments to the specification start at page 2.

A Listing of the Claims starts at page 3.

Remarks start on page 10.

APPENDIX A is at page 11.

TABLE starts at page 12.

REMARKS

This application claims ultimate priority to the 2014 filing date of PCT/US14/39208 and the provisional applications filed in 2013 to which it claims priority.

APPENDIX A hereto (page 11 hereof) is a simplified chart of an unbroken chain to the 2014 and 2013 dates. The full listing of related applications is in amended paragraph [0001] submitted in this Preliminary Amendment.

The text and drawings of this application (other than amended paragraph [0001]) are as in the PCT application incorporated by reference in the intermediate applications. Consideration of the claims of and listed references in the related patents/applications identified in amended paragraph [0001] is respectfully requested, per MPEP 609.02.

Applicant attaches hereto a **TABLE** (starting at page 12 hereof) pointing to non-limiting examples of support for the current claims in the PCT application filed in 2014.

Applicant is concurrently filing a Request for Expedited Examination Based on Age and Terminal Disclaimers to the related patents and applications listed in the TABLE and plans to request a pre-examination interview.

If a petition for an extension of time is required to make a response timely, this paper should be taken as such a petition. The Patent Office is hereby authorized to charge any required fees in connection with this paper, and to credit any overpayment, to our Deposit Account No. 600125.

Respectfully submitted,

/Ivan S. Kavrukov/ Attorney Reg. No. 25,161

Address: (associated with Customer Number: 139982)

Phone: (917) 945-0121

Attachments:

- **APPENDIX A (Partial chain of parent applications); and**
- **TABLE (pointing to non-limiting examples of support for claim elements).**

LISTING OF CLAIMS:

The following claims replace all previously pending claims in this patent application:

1. A semiconductor device with deliberately formed in-pillar holes comprising:
    a laterally extending array of pillars that have rectangular cross-sections in a horizontal plane and are elongated in an up-down direction;
    pillar-separating dielectric between sidewalls of adjacent pillars;
    wherein each pillar comprises:
        a first doped semiconductor region;
        a first undoped or low-doped semiconductor region below the first doped semiconductor region;
        a second doped semiconductor region below the first undoped or low-doped semiconductor region;
        one or more deliberately formed, solid dielectric-filled, in-pillar holes extending into the pillar;
        a top electrical contact; and
        a bottom electrical contact;
    wherein said top and bottom electrical contacts are configured to provide reverse-bias from an external source for operation of said device to convert light photons incident on said pillar to electrons;
    a base dielectric below the array of pillars;
    wherein said pillars;
        are laterally spaced center to center by 10-10,000 nanometers; and
        have up-down lengths of said first undoped or low-doped semiconductor regions in the range of 100-5000 nanometers;
    wherein said pillars, in-pillar holes, and pillar-separating dielectric:
        increase photon absorption of said device of incident light compared to a like device lacking said one or more in-pillar holes; and
        facilitate operation of said device with infrared incident light; and

wherein said device is CMOS compatible for mass production using CMOS foundries.

2. The device of claim 1, in which each of said pillars further includes:
   a second undoped or low-doped semiconductor regions under the second doped semiconductor regions of said pillars;
   third doped semiconductor regions under the second undoped or low-doped semiconductor regions and above said base dielectric; and
   wherein said top and bottom electrical contacts are configured to provide reverse-bias from an external source in the range of -5 to -50 Volts sufficient for operations of said device as an avalanche photodiode.

3. The device of claim 2, in which said third doped semiconductor regions of said pillars form a laterally continuous region coupled to a plurality of said pillars.

4. The device of claim 2, in which the top electrical contact is a transparent, laterally continuous region that is electrically coupled to a plurality of said pillars.

5. The device of claim 2, in which said second undoped or low-doped region has a thickness in the 100-2,000 nanometers range.

6. The device of claim 2, in which the first and second doped semiconductor regions are doped to the same polarity and the third doped semiconductor region is doped to an opposite polarity.

7. The device of claim 2, In which each of said first doped semiconductor region and said first undoped or low-doped semiconductor regions is a Ge region and each of said second doped semiconductor region, said second undoped or low-doped semiconductor region, and said third doped semiconductor region is an Si region.

8. The device of claim 2, in which at least one of the first and second doped regions and first and second undoped or low-doped regions is an SiGe region.

9. The device of claim 2, in which said pillar-separating dielectric is along sidewalls of at least said first and second doped semiconductor regions and said first and second undoped or low-doped semiconductor regions.

10. The device of claim 2, in which each of said pillars has a plurality of said one or more in-pillar holes.

11. The device of claim 2, in which each of said pillars has only one of said one or more in-pillar holes.

12. The device of claim 2, in which said one or more in-pillar holes extend to a depth in the range of 100-10,000 nanometers.

13. The device of claim 2, in which said one or more in-pillar holes extend into said first undoped or low-doped semiconductor region.

14. The device of claim 2, in which said one or more in-pillar holes are pyramid-shaped.

15. The device of claim 2, in which the gain of said device operating as an avalanche photodiode is greater than two.

16. The device of claim 1, in which said one or more in-pillar holes are pyramid-shaped.

17. The device of claim 1, in which the first doped semiconductor region and the second doped semiconductor region are doped to opposite polarities.

18. The device of claim 1, in which each of the first doped semiconductor region and the first undoped or low-doped semiconductor region is a Ge region and the second doped semiconductor region is an Si region.

19. The device of claim 1, in which each of said pillars has a plurality of said one or more in-pillar holes.

20. The device of claim 1, in which each of said pillars has only one of said one or more in-pillar holes.

21. The device of claim 1, in which said one or more in-pillar holes extend into said first undoped or low-doped semiconductor region.

22. The device of claim 1, in which each of said pillars has at least two of said one or more in-pillar holes and said at least two of said in-pillar holes partly overlap.

23. The device of claim 1, in which at least one of the first and second doped regions and the first undoped or low-doped regions is an SiGe region.

24. The device of claim 1, in which the top electrical contact is a transparent, laterally continuous region that is electrically coupled to a plurality of said pillars.

25. The device of claim 1, in which said second doped semiconductor regions of said pillars form a laterally continuous region coupled to a plurality of said pillars.

26. The device of claim 1, in which the first doped semiconductor region is an amorphous Si region, the first undoped or low-doped semiconductor region is a crystalline Ge region, and the second doped semiconductor region is a crystalline Si region.

27. A semiconductor device with deliberately formed in-pillar holes comprising:

an array of pillars that have rectangular cross-sections in a horizontal plane;

wherein each pillar comprises:

a first doped semiconductor region;

a second doped semiconductor region;

a first undoped or low-doped semiconductor region between the first and second doped semiconductor regions;

one or more deliberately formed, solid dielectric-filled, in-pillar holes extending into the pillar;

a first electrical contact; and

a second electrical contact;

wherein said first and second electrical contacts are configured to provide reverse-bias from an external source for operation of said device to convert light photons incident on said pillar to electrons;

a base dielectric under the array of pillars;

wherein said pillars;

are spaced from each other center to center by less than 10,000 nanometers;

increase photon absorption of said device of incident light compared to a like device lacking said one or more in-pillar holes; and

wherein said device is CMOS compatible for mass production using CMOS foundries.

28. The device of claim 27, in which each of said pillars has only one of said one or more in-pillar holes.

29. The device of claim 28, in which each of said pillars further includes:

a third doped semiconductor region over said base dielectric;

a second undoped or low-doped semiconductor region between the second and third doped semiconductor regions; and

wherein said first and second electrical contacts are configured to provide reverse-bias from an external source in the range of -5 to -50 Volts sufficient for operations of said device as an avalanche photodiode.

30. A semiconductor device with deliberately formed in-pillar holes comprising:

an array of pillars that have rectangular cross-sections in a horizontal plane;

pillar-separating dielectric between sidewalls of adjacent pillars;

wherein each pillar comprises:

a first doped semiconductor region;

a second doped semiconductor region;

a third doped semiconductor region;

a first undoped or low-doped semiconductor region between of the first and second doped semiconductor regions;

a second undoped or low-doped semiconductor region between the second and third doped semiconductor regions;

one or more deliberately formed, solid dielectric-filled, in-pillar holes extending selected distances into the pillar;

a first electrical contact; and

a second electrical contact;

wherein said first and second electrical contacts are configured to provide reverse-bias from an external source in the range of -5 to -50 Volts for operation of said device as an avalanche photodiode with a gain greater than two;

a base dielectric under the array of pillars;

wherein said pillars;

are spaced from each other center to center by less than 10,000 nanometers; and

have a dimension of said first undoped or low-doped semiconductor regions that is less than 5000 nanometers;

wherein said pillars, in-pillar holes, and pillar-separating dielectric:

increase photon absorption of said device of incident light compared to a like device lacking said one or more in-pillar holes; and

facilitate operation of said device with infrared incident light; and

wherein said device is CMOS compatible for mass production using CMOS foundries.

PTO/AIA/26 (04-14)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0011USDIVCIP2

In re Application of: Shih-Yuan WANG

Application No.: 17/707,429

Filed: March 29, 2022

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 9,818,893 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
March 29, 2022 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/26 (04-14)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0011USDIVCIP2

In re Application of: Shih-Yuan WANG

Application No.: 17/707,429

Filed: March 29, 2022

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 9,530,905 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
March 29, 2022 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/26 (04-14)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0011USDIVCIP2

In re Application of: Shih-Yuan WANG

Application No.: 17/707,429

Filed: March 29, 2022

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 10,622,498 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
March 29, 2022 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
914-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc code: PET.OP.AGE
Description: Petition to make special based on age/health

PTO/SB/130 (01-19)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number

PETITION TO MAKE SPECIAL BASED ON AGE FOR ADVANCEMENT OF EXAMINATION UNDER 37 CFR 1.102(c)(1)

Application Information

Application Number	17/707,429	Confirmation Number	1214	Filing Date	March 14, 2022
Attorney Docket Number (optional)	309-0011USDIVCIP2	Art Unit	n/a	Examiner	n/a
First Named Inventor	Shih-Yuan WANG				
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES				

Attention: Office of Petitions

An application may be made special for advancement of examination upon filing of a petition showing that the applicant is 65 years of age, or more. No fee is required with such a petition. See 37 CFR 1.102(c)(1) and MPEP 708.02 (II).

APPLICANT HEREBY PETITIONS TO MAKE SPECIAL FOR ADVANCEMENT OF EXAMINATION IN THIS APPLICATION UNDER 37 CFR 1.102(c)(1) and MPEP 708.02 (II) ON THE BASIS OF THE APPLICANT'S AGE.

A grantable petition requires one of the following items:

(1) Statement by one named inventor in the application that he/she is 65 years of age, or more; or

(2) Certification by a registered attorney/agent having evidence such as a birth certificate, passport, driver's license, etc. showing one named inventor in the application is 65 years of age, or more.

Name of inventor who is 65 years of age, or older

Given Name	Middle Name	Family Name	Suffix
Shih-Ping		WANG	

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 11.18. Please see 37 CFR 1.4(d) for the format of the signature.

Select (1) or (2):

☐ (1) I am an inventor in this application and I am 65 years of age, or more.

☒ (2) I am an attorney or agent registered to practice before the Patent and Trademark Office, and I certify that I am in possession of evidence, and will retain such in the application file record, showing that the inventor listed above is 65 years of age, or more.

Signature	/Ivan S. Kavrukov/	Date (YYYY-MM-DD)	March 29, 2022
Name	Ivan S. Kavrukov	Registration Number	25,161

This collection of information is required by 37 CFR 1.102(c)(1). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) a petition to make special based on age for advancement of examination. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETED FORMS TO THE CHIEF INFORMATION OFFICER. **Submit completed forms electronically over EFS-Web, or mail to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/25 (04-13)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION	Docket Number (Optional) 309-0011USCIPDIV2

In re Application of: Shih-Yuan WANG

Application No.: 17/707,429

Filed: March 29, 2022

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending **reference** Application Number 17/182,954, filed, February 23, 2021, as the term of any patent granted on said **reference** application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending **reference** application. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the **reference** application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term of any patent granted on said **reference** application, "as the term of any patent granted on said **reference** application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending **reference** application," in the event that: any such patent granted on the pending **reference** application expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/	March 29, 2022
Signature	Date
Ivan S. Kavrukov	
Typed or printed name	
Attorney of Record	917-945-0121
Title	Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) is included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/26 (04-14)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0011USDIVCIP2

In re Application of: Shih-Yuan WANG

Application No.: 17/707,429

Filed: March 29, 2022

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 9,496,435 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
March 29, 2021 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/26 (04-14)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0011USDIVCIP2

In re Application of: Shih-Yuan WANG

Application No.: 17/707,429

Filed: March 29, 2022

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 10,446,700 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
March 29, 2022 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/26 (04-14)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0011USDIVCIP2

In re Application of: Shih-Yuan WANG

Application No.: 17/707,429

Filed: March 29, 2022

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 11,121,271 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
March 29, 2022 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/26 (04-14)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0011USDIVCIP2

In re Application of: Shih-Yuan WANG

Application No.: 17/707,429

Filed: March 29, 2022

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 9,525,084 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
March 29, 2022 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/26 (04-14)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) 309-0011USDIVCIP2

In re Application of: Shih-Yuan WANG

Application No.: 17/707,429

Filed: March 29, 2022

For: MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

The applicant, W&WSENS DEVICES, INC., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 10,468,543 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 25,161

/Ivan S. Kavrukov/ — Signature
March 29, 2022 — Date

Ivan S. Kavrukov — Typed or printed name

Attorney of Record — Title
917-945-0121 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ABSTRACT

Techniques for enhancing the absorption of photons in semiconductors with the use of microstructures are described. The microstructures, such as pillars and/or holes, effectively increase the effective absorption length resulting in a greater absorption of the photons. Using microstructures for absorption enhancement for silicon photodiodes and silicon avalanche photodiodes can result in bandwidths in excess of 10 Gb/s at photons with wavelengths of 850 nm, and with quantum efficiencies of approximately 90% or more.

MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

REFERENCE TO RELATED APPLICATIONS

[0001] This patent application claims the priority of and incorporates by reference each of the following applications:

U.S. Prov. Ser. No. 61/826,446 filed May 22, 2013;

U.S. Prov. Ser. No. 61/834,873 filed June 13, 2013;

U.S. Prov. Ser. No. 61/843,021 filed July 4, 2013; and

U.S. Prov. Ser. No. 61/905,109 filed November 15, 2013;

The above-referenced provisional patent applications are collectively referenced herein as "the commonly assigned incorporated applications."

FIELD

[0002] The present invention generally relates mainly to photosensitive devices. More particularly, some embodiments relate to photosensitive devices having microstructure enhanced absorption characteristics.

BACKGROUND

[0003] Fiber-optic communication is widely used in applications such as telecommunications and communication within large data centers. Because of attenuation losses associated with using shorter optical wavelengths most fiber-optic communication uses optical wavelengths of 800 nm and longer. Commonly used transmission windows exist between 1260 nm and 1675 nm. A main component of optical receivers used in fiber-optic communication system is the photo detector, usually in the form of a photodiode (PD) or avalanche photodiode (APD).

[0004] High-quality low-noise APDs can be made from silicon. However, while silicon will absorb light in the visible and near infrared range, it becomes more transparent at longer optical wavelengths. Silicon PDs and APDs can be made for optical wavelengths of 800 nm and longer by increasing the thickness of the absorption "I" region of the device. FIG. 2 is a cross section of a conventional PIN photodiode 200, where "d" is the length of the absorption "I" region 220. FIGs. 3A and 3B show bandwidth and quantum efficiency a conventional silicon photodiode

with a 30-micron diameter at 850 nm optical wavelength. As can be seen, in order to obtain a quantum efficiency of 90% the thickness "d" of the "I" region is over 30 microns. This leads to a maximum bandwidth of less than 2.5 Gb/s, which is too low for many current and future telecom and data center applications.

[0005] To avoid the inherent problem that silicon PDs and APDs have with longer wavelengths and higher bandwidths, other materials are used. Germanium (Ge) detects infrared out to a wavelength of 1700 nm, but has relatively high multiplication noise. InGaAs can detect out to longer than 1600 nm, and has less multiplication noise than Ge but still has far greater noise than silicon. InGaAs is known to be used as the absorption region of a heterostructure diode, most typically involving InP as a substrate and as a multiplication layer. This material system is compatible with an absorption window of roughly 900 to 1700 nm. However both InGaAs and Ge devices are relatively expensive and have relatively high multiplication noise when compared with silicon.

[0006] The subject matter claimed herein is not limited to embodiments that solve any specific disadvantages or that operate only in environments such as those described above. Rather, this background is only provided to illustrate one exemplary technology area where some embodiments described herein may be practiced.

SUMMARY

[0007] According to some embodiments, a photodetector with microstructure-enhanced photoabsorption is described. The photodetector (e.g. photodiode or avalanche photodiode) includes: a cathode region; an anode region; reverse biasing circuitry configured to apply a voltage between the cathode and anode regions such that the cathode region is driven to a more positive voltage than the anode region; and a microstructure-enhanced photon absorbing semiconductor region configured to absorb photons from a source signal. The absorbing region includes a plurality of microstructures that are dimensioned and positioned to increase absorption of photons at a range of wavelengths that includes a wavelength of the source signal. According to some embodiments the microstructures have at least one dimension that is equal to or shorter than a longest signal wavelength. According to some embodiments the microstructures

are pillars, holes and/or voids. The microstructures can be arranged into a periodically-spaced array, a non-periodically-spaced array, a randomly-spaced array or a multiperiodically-spaced array. According to some embodiments the microstructures have a major longitudinal axis that is normal to the upper surface of the underlying substrate material. According to some other embodiments, the microstructures have major longitudinal axes that are not parallel to one another. According to some embodiments, the microstructures are oriented so as to reduce sensitivity to any single direction of the source signal.

[0008] According to some embodiments, the microstructures increase absorption at least in part by forming an absorbing mode high contrast grating that makes use of resonance effects, scattering effects, near field effects, sub-wavelength effects, and/or interference effects.

[0009] According to some embodiments, the absorbing region and the microstructures are formed of silicon. According to some embodiments, a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 5 gigabits per second, at wavelengths of 850 nanometers with a quantum efficiency of at least 60%. According to some embodiments, a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 10 gigabits per second, at signal wavelengths of 850 nanometers with a quantum efficiency of at least 60%. According to some embodiments a silicon avalanche photodiode is provided that can detect source signals at a data bandwidth of greater than 5 gigabits per second, at wavelengths of 850 nanometers, while having a gain of greater than 2. According to some embodiments a silicon APD has a multiplication region with microstructures that extend into the P multiplication layer, N multiplication layer and/or charge layer. According to some embodiments a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 1 gigabit per second, at wavelengths of 980 nanometers with a quantum efficiency of at least 40%. According to some embodiments a silicon photodiode is provided that can detect source signals at a data bandwidth of greater than 0.5 gigabits per second, at wavelengths of 1000 nanometers with a quantum efficiency of at least 30%. According to some embodiments, the microstructures effectively reduce

capacitance of the photodetector when compared to a microstructure-free device having a similar photon absorbing length.

[0010] According to some embodiments, the absorbing semiconductor region and the microstructures are formed of silicon and germanium. According to some embodiments, the microstructures are formed by etching away portions of silicon and using a selective area growth process to grow germanium in the etched away portions. According to some embodiments, the absorbing semiconductor region and the microstructures are formed of germanium. According to some embodiments, the photo detector is configured to receive the source signal from the substrate-side. The anode region can include a germanium P layer formed by an epitaxial lateral overgrowth process. The device can be configured such that the source signal to passes through the absorbing region a first time, reflects from a surface and thereafter passes through the absorbing region a second time. The device can also be configured to receive the source signal the top-side and the anode region can be made of a silicon P layer. According to some embodiments, a avalanche photodiode is provided that detects source signals at a data bandwidth of greater than 1 gigabit per second, at source signal wavelengths of 1750 nanometers or shorter, and having a gain of greater than 2. According to some embodiments, the absorbing semiconductor region and the microstructures are formed of III-V family material(s) such as InP, GaAs, InGaAs, GaN, InGaN, InGaAsP, AlGaAs, AlGaN, GaP, InSb or InAs.

[0011] According to some embodiments, the microstructures include voids buried within the absorbing semiconductor region. According to some embodiments, voids are buried in a layer of material so as to effectively lower the refractive index at the signal wavelength(s) and as well as lower the capacitance of the layer of material.

[0012] According to some embodiments, a photovoltaic device is described that includes a semiconductor material having a plurality of voids buried therein. The semiconductor material being configured to convert solar radiation into direct current electricity. According to some embodiments, the voids are microstructured voids and are configured to enhance absorption of the semiconductor material thereby increasing conversion efficiency of the device. According to some embodiments, the voids are sized and/or spaced apart by less than 3 microns, and

are configured to alter an effective refractive index of the semiconductor material near a surface, for example to reduce reflection of incident sunlight from the device and/or increase internal reflections within the semiconductor material.

[0013] According to some embodiments a glass material is described in which the glass has a plurality of buried voids dimensioned between 0.01 microns to 1000 microns. In some examples the glass forms a part of a photovoltaic device. According to some embodiments, the buried voids are filled with a material gel, polymer and gas. The buried voids can provide flexibility of the glass material, and/or increased resistance of the glass material to physical damage and/or damage propagation.

[0014] According to some embodiments, a microwave transmission line structure is described that includes: a semiconductor substrate material having a plurality of high-density dielectric-filled voids configured to reduce a dielectric constant of the semiconductor substrate material; and a plurality of metallic microwave transmission lines, least one of which is positioned above the semiconductor substrate material. According to some embodiments, the dielectric-filled voids are filled a material such as: nitrogen, argon, vacuum, air, helium, polymer, metal oxides, silicon dioxide, silicon nitride, calcium fluoride, or zinc oxide. According to some embodiments, the voids are further configured to reduce dispersion and reduce loss associated with the microwave transmission lines at least in part by reducing current loop flow and/or eddy currents.

[0015] According to some embodiments, an optical waveguide structure is described that includes: an optical mode region; and a supporting semiconductor material adjacent to the optical mode region. The supporting material includes a plurality of microstructured voids that are configured to alter an effective index of refraction of the supporting material based on the size, shape, density, etc. of the microstructured voids.

[0016] According to some embodiments, a heat exchanger system is described that includes: a heat generating device; a heat sink configured to dissipate heat to a surrounding medium; and an intermediate material mounted between the heat generating device and the heat sink. The intermediate material includes a plurality of buried voids configured to effect thermal conductivity of the intermediate material. According to some embodiments, some of the buried voids are filled with

thermally conductive material and others are filled with a thermally isolating material. The two types of voids being positioned to conduct heat from the heat generating device to the heat sink and to reduce thermal cross talk with other heat sensitive devices mounted on the intermediate material.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] To further clarify the above and other advantages and features of the subject matter of this patent specification, specific examples of embodiments thereof are illustrated in the appended drawings. It should be appreciated that these drawings depict only illustrative embodiments and are therefore not to be considered limiting of the scope of this patent specification or the appended claims. The subject matter hereof will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

[0018] FIG. 1 is schematic side cross section of three dimensional micro structures that enhance bulk absorption coefficient in photo sensitive devices, according to some embodiments;

[0019] FIG. 2 is a cross section diagram showing aspects of a typical structure of a conventional PIN photodiode**;**

[0020] FIGs. 3A and 3B a plots showing bandwidth and quantum efficiency (QE), respectively, of a bulk conventional silicon photodiode versus “d” in microns;

[0021] FIGs. 4A-4D are graphs showing the enhancement of bulk absorption coefficient vs bandwidth and QE for a microstructured Si photodetector, according to some embodiments;

[0022] FIGs. 5A and 5B are cross sections showing aspects of a top illuminated microstructered PIN silicon photodiode, according to some embodiments;

[0023] FIGs. 6A and 6B are cross sections showing aspects of a bottom illuminated microstructered NIP silicon photodiode, according to some embodiments;

[0024] FIGs. 7A and 7B are cross sections showing aspects of a microstructered avalanche photodiode, according to some embodiments;

[0025] FIG. 8 is a cross section showing a silicon epitaxial structure for a high-speed high-efficiency microstructured APD, according to some embodiments;

[0026] FIGs. 9A-9E are a series of cross sections showing some basic microstructure processing steps, for a high-speed APD, according to some embodiments;

[0027] FIGs. 10A-10B are cross sections showing aspects of a top illuminated microstructered photo diodes, avalanche photo diodes and/or photovoltaics (PV) with microstructured voids in N-Si, according to some embodiments;

[0028] FIGs. 11A and 11B are cross sections showing aspects of an heteroepitaxial APD structure of Ge on Si, according to some embodiments;

[0029] FIG. 12 is a cross section illustrating aspects of a passivation method for Ge surfaces on microstructures, according to some embodiments;

[0030] FIGs. 13A and 13B are graphs showing the effects of mictrostructure enhancement of Ge bulk absorption coefficient for photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments;

[0031] FIGs. 14A-14B are cross sections showing aspects of a top-illuminated Ge on Si avalanche photodiode having microstructured pillars/holes, according to some embodiments;

[0032] FIGs. 15A-15D are cross sections illustrating aspects of bottom-illuminated Ge on Si avalanche photodiodes having microstructured pillars/holes, according to some embodiments;

[0033] FIGs. 16A and 16B are graphs comparing single pass and double pass photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments;

[0034] FIGs. 17A-17B are cross sections showing aspects of a top-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 700 to 1800 nm, according to some embodiments;

[0035] FIGs. 18A-18B are cross sections showing aspects of a bottom-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 1200 to 1800 nm, according to some embodiments;

[0036] FIGs. 19A-19C are diagrams illustrating how mictrostructures can reduce capacitance of a photodiode such that a larger area photo diode can be fabricated with the same bandwidth and QE, according to some embodiments;

[0037] FIGs. 19D-19E are cross sections showing aspects of fabricating an APD device having a III-V absorbing layer grown on a P-I-N silicon multiplication layer, according to some embodiments;

[0038] FIG. 20 shows bulk layers without a final P-Si layer for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments;

[0039] FIG. 21 is a cross section showing etching of microstructured pillars and/or holes for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments;

[0040] FIG. 22 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after the Ge "I" layer is grown in the etched region and planarized, according to some embodiments;

[0041] FIG. 23 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after I-Ge regrowth and planarization, and a cap layer of P-Si, according to some embodiments;

[0042] FIGs. 24A - 24B are cross sections showing aspects of a microstructured APD with buried/embedded I-Ge absorbing microstructures in I-Si microstructures, according to some embodiments;

[0043] FIGS. 25A - 25C are cross sections showing aspects of a photodiode having buried/embedded Ge microstructures in a Si microstuctured pillar and/or hole array, according to some embodiments;

[0044] FIGs. 25D - 25E are cross sections showing aspects of a forward biased device such as a vertical cavity surface emitting laser (VCSEL), according to some embodiments;

[0045] FIG. 26 is a cross section showing starting epitaxial layers in which mictrostructured voids are fabricated, according to some embodiments;

[0046] FIG. 27 is a cross section showing microstructured holes/pillars etched into the I-Si layer, according to some embodiments;

[0047] FIG. 28 is a cross section showing microstructured voids buried or embedded in Si with a Si capping P^+ anode layer 2826, according to some embodiments;

[0048] FIG. 29 is a cross section showing Bragg reflectors formed on the P-Si surface to provide a highly reflective mirror, according to some embodiments;

[0049] FIG. 30 shows an example of a PIN PD/PV structure with microstructured voids to enhance absorption, reduce bulk refractive index, reduce capacitance and increase mechanical flexibility of large sheets of PV on semiconductor material, according to some embodiments;

[0050] Fig. 31 is a cross section showing regrown I-Ge with a buried/embedded voids, according to some embodiments;

[0051] Fig. 32 is a cross section showing a device having buried microstructured voids in I-Si with regrown I-Ge and capped by a epitaxial layer, according to some embodiments;

[0052] FIG. 33 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some embodiments;

[0053] FIG. 34 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some other embodiments;

[0054] Fig. 35 shows the basic epitaxial structure for a conventional Si PV/PD diode on N Si substrate;

[0055] FIG. 36 shows microstructured voids incorporated into an N-Si layer, according to some embodiments;

[0056] FIG. 37 is a cross section showing etched Si microstructured pillars/holes with regrown Ge covering the Si, according to some embodiments;

[0057] FIG. 38 is a cross section showing microstructured Si pillars/holes with Ge regrowth on an N-Si layer having embedded microstructured voids, according to some embodiments;

[0058] FIG. 39 is a cross section showing partial coverage I-Ge on microstructured Si pillars/holes, according to some embodiments;

[0059] FIG. 40 is a cross section sowing the basic components for the a microstructured Si-Ge pillar hole array PD/PV and/or APD, according to some embodiments;

[0060] FIGs. 41A-41B are cross sections showing aspects of a microstructured pillar/hole array device above a N-Si layer having buried microstructured voids, according to some embodiments;

[0061] FIGs. 42A-42D are cross sections showing aspects of an APD with microstructured pillar/hole arrays above an N-Si layer having buried microstructured voids, according to some embodiments;

[0062] FIGs. 43-46 are top views illustrating various dimensions, spacings and shapes for microstructured elements, according to some embodiments;

[0063] FIGs. 47-48 are cross sections showing microstructured pillar and hole arrays having varying lengths and depths, according to some embodiments;

[0064] FIG. 49 shows shows a microstructured surface having a combination of both pillars and holes, according to some embodiments;

[0065] FIG. 50 is a cross section of an optical ridge waveguide, according to some embodiments;

[0066] FIG. 51 is a cross section of a buried optical waveguide in silicon using voids, according to some embodiments;

[0067] FIGs. 52 and 53 are a cross section and top view, respectively, of a ridge waveguide integrated with a microstructured PD/APD, according to some embodiments;

[0068] FIGs. 54A and 54B show a microwave transmission line on Si with voids, according to some embodiments;

[0069] FIG. 55 is a cross section of voids for thermal conduction and thermal isolation of heat producing ICs and light emitters, according to some embodiments; and

[0070] FIG. 56 is a cross section showing a distribution of voids to increase lateral path length for increasing lateral electrical resistivity and decrease lateral thermal conduction, according to some embodiments.

DETAILED DESCRIPTION

[0071] A detailed description of examples of preferred embodiments is provided below. While several embodiments are described, it should be understood that the new subject matter described in this patent specification is not limited to any one embodiment or combination of embodiments described herein, but instead encompasses numerous alternatives, modifications, and equivalents. In addition, while numerous specific details are set forth in the following description in order to provide a thorough understanding, some embodiments can be practiced without some or all of these details. Moreover, for the purpose of clarity, certain technical material that is known in the related art has not been described in detail

in order to avoid unnecessarily obscuring the new subject matter described herein. It should be clear that individual features of one or several of the specific embodiments described herein can be used in combination with features or other described embodiments. Further, like reference numbers and designations in the various drawings indicate like elements.

[0072] According to some embodiments, microstructures are used to enhance the bulk absorption constant (also referred to as absorption coefficient) to achieve high quantum efficiency (QE) while maintaining an absorption length suitable for high data rate applications. As used herein, “QE” refers to internal quantum efficiency (IQE). IQE is equal to external quantum efficiency (EQE) in cases where reflection and transmission are negligible.

[0073] According to some embodiments, microstructures are used to improve bulk absorption constant at wavelengths in the proximity of the semiconductor material's band gap. This allows for extending the operating optical wavelengths and/or operating spectrum of the photosensor. The enhanced bulk absorption constant (or coefficient) is called the effective absorption constant (or coefficient). The term "effective" is used since absorption constant or coefficient is an inherent material property. However, with resonance effects, plasmonic effects, field enhancement effects, scattering effects, near field and sub wavelength effects, the effective absorption constant or coefficient can be greater than the bulk or material absorption constant or coefficient. As used herein, the following terms are used interchangeably: enhanced absorption constant, enhanced absorption coefficient; enhanced effective absorption constant; enhanced effective absorption coefficient; enhanced absorption; enhanced effective absorption; and effective absorption constant; and effective absorption coefficient.

[0074] According to some embodiments, enhanced absorption can also have drastic effects on path length. In one bulk absorption example, the path length for the photons to be absorbed to 1/e of its original amplitude is, for example 100 micrometers (μm), whereas under enhanced absorption according to some embodiments, the path length is 1 micrometer for the optical amplitude to decay to 1/e of its original amplitude. Equivalently, if path length is kept constant to one micrometer then the enhanced absorption coefficient is 100 times greater than the bulk absorption coefficient.

[0075] This is seen by the relationship $A = A_0 e^{-\alpha L}$ where A is the decaying amplitude of the incident photon flux A_0 and α is the absorption coefficient and L the path length for absorption to take place. So, rather than have L be 100 times longer, an effective α can be defined such that it is 100 times greater than a non enhanced absorption coefficient such as the bulk absorption coefficient. The resonance/scattering/near field effects of microstructures for example gives the equivalence of the path length that is 100 times longer where the resonant/scattering/near field microstructure is just one micron long. To put it another way, in a very simplistic view, the photons in the resonant structures make 50 round trips before reaching the 1/e value of its original amplitude, so the equivalent linear length is 100 times the length of the resonant structure. For simplicity, resonance/scattering/near field effects will collectively be referred to herein as “resonant” which can include, resonant, scattering, near field, plasmonic, nonlinear and linear optical effects.

[0076] As used herein the terms "microstructures" and “microstructured” refer to: pillars, voids, holes and mesas, of various shapes and sizes having at least one dimension in the micrometer scale, submicrometer scale, and/or sub-wavelength scale.

[0077] According to some embodiments, properties of the microstructures can also be explained as the absorption mode of high contrast grating (HCG) being used to enhance the effective absorption constant/coefficient or enhanced absorption. Conventionally, HCG uses material that is transparent at the optical wavelength of interest. In contrast, according to some embodiments, at least one of the microstructures is absorbing or weakly absorbing at the optical wavelength of interest. According to some embodiments a low-Q absorbing mode HCG enhances absorption (e.g. Q values in the range of 2-200).

[0078] According to some embodiments, a low index material is used such as buried oxide (BOX), silicon on insulator (SOI), silicon on sapphire (SOS), low-density semiconductors such as amorphous semiconductor, nanowire semiconductors, voids and holes to lower the effective refractive index. Refractive index is an inherent property of a material. However, according to some embodiments, when structures such as voids, air gaps, and/or holes (which can be filled with low index material, and/or regrowth) have dimensions on the order of the

optical wavelength, the optical electromagnetic field will see an average refractive index consisting of the material refractive index and the structures (which can be filled by a low refractive index material). This average is referred to herein as the effective refractive index. According to some embodiments, a low index or effective low index material need not be used in the microstructures.

[0079] According to some embodiments, the techniques for enhancing effective absorption can be applied to various materials including: silicon, germanium, III-V material such as InP, GaAs, GaN, InGaAs, and any combination of the III-V material family. As used herein, the term "material family" of a III-V material is defined as any material that is lattice matched or approximately lattice matched (within a few percent) to GaAs, InP, GaN, InSb semiconductors. For example, the InP material family can include InGaAs, InGaAsP, InAlAs. According to some embodiments, in the case of microstructures, regrowth such as selective area growth (SAG) of Ge, InGaAs, or other III-V material in silicon microstructures can be carried out without the detrimental effects of lattice mismatch since the dimension of the footprint of the lattice mismatched material on silicon is small (approximately a few micrometers to sub-micrometers). This allows Ge and other III-V materials to be integrated with silicon without the use of a conventional buffer layer (such as amorphous Ge in the case of Ge on Si growth). The heterogeneous integration of materials can be homo or hetero structures, combination of crystalline and microcrystalline and amorphous semiconductor, conductor such as carbon, graphene, insulator, dielectrics, solid, gaseous, liquid such as glass or polymer that can be semiconducting.

[0080] Due to the microstructures, the capacitance can also be represented by an effective capacitance which is a parallel capacitance of (1) the dielectric constant of one semiconductor, and (2) the dielectric constant of another material, which can be a semiconductor, dielectric, gas, vacuum, partial vacuum, liquid such as glass or polymer (polyimide, mylar, or other organic compound). The effective capacitance of the device is the combination of the capacitance of the parallel capacitors, which can be two or more. An advantage of the use of microstructure according to some embodiments, is that the effective capacitance can be significantly lower than the capacitance of a homogeneous material such as a semiconductor. The lower capacitance allows a device to have a larger area while

still maintaining suitably high data rate bandwidth, and/or increase the data rate bandwidth by reducing the thickness of the device to reduce the transit time.

[0081] According to some embodiments, the photosensor can be a photodiode (PD), avalanche photodiode (APD), photovoltaic (PV) or solar cell, or any optoelectronic device that converts photons to electrons. According to some embodiments, emitters such as lasers and light emitting diodes that convert electrons/holes to photons can also be implemented using microstructures.

[0082] According to some embodiments, the enhanced absorption allows the APD/PD to: (1) extend the sensitivity of the APD/PD to photons with energies (or wavelength) closer to the material band gap with QE greater than 60% and data bandwidth greater than 3 Gb/s; (2) operate at a high data rate bandwidth (e.g. >10 Gb/s), due to shorter absorption length therefore shorter transit time; (3) increase quantum efficiency with enhanced absorption; (4) be manufactured of silicon which has superior APD properties with low excess noise; (5) be compatible with Si Photonics and CMOS processes. According to some embodiments, the PD/APD can be integrated with ASIC (application specific integrated circuits) such as signal processing, signal amplification, memory, cpu, electrical transmitter, optical waveguides, integrated optics, and other ICs for specific applications. This is advantageous for mass production using CMOS foundries.

[0083] According to some embodiments, microstructures such as voids are used to reduce effective refractive index to create resonant structures to enhance the absorption. In microstructures where selective area growth are used to integrate Ge or III-V material with silicon, voids can be made in the silicon microstructure such that the absorbing region is a resonant structure to enhance the effective absorption coefficient by 2 to over 100 times.

[0084] According to some embodiments, silicon is used for avalanche gain. Silicon has the lowest excess noise for an avalanche photodiode. By integrating Ge and/or III-V material with silicon, the absorption takes place in Ge and/or III-V material and the electronic gain occurs in silicon. Depending on the optical wavelengths, for example shorter than 1100 nm, silicon may be used for both absorption and electronic gain with the use of microstructures.

[0085] According to some embodiments, microstructures such as buried voids can reduce lateral electrical and thermal conductivity. In situations where

directional conductivity of electrical or thermal (phonons) is preferred, voids can be used to confine the flow of electrical current and/or heat.

[0086] According to some embodiments, the absorption of photons in semiconductors is enhanced with the use of microstructures. The microstructures can have effects such as resonance, field enhancement, near field and sub wavelength effects, scattering, plasmonics, photonic crystal, absorption mode in high contrast grating at the near field regime, which are both linear and non linear effects that can effectively increase the effective absorption length resulting in a greater absorption of the photons for a given length.

[0087] According to some embodiments, microstructures used for absorption enhancement for silicon photodiodes and silicon avalanche photodiodes can result in silicon PD and APD with bandwidths in excess of 10 Gb/s (or equivalently 6.75 GHz approximately depending of the digital coding format) at photons with wavelengths of 850 nm approximately (which is the current datacom preferred wavelength) with quantum efficiencies of approximately 90% or more.

[0088] Silicon optical detectors are very robust due to the maturity of the material and processing techniques, the surfaces can be easily passivated to eliminate dangling bonds that can cause surface states and carrier recombination centers, they have excellent carrier lifetimes due to low defects and high material purity, and for APD applications, the noise is low due to the small ionization ratio between holes and electrons (k factor, silicon have the lowest k factor than any III-V material) and such detectors are CMOS compatible for integration with electronics for signal processing and with Si photonics.

[0089] According to some embodiments, other material such as germanium, III-V, a-Si (amorphous silicon) may also be used singly or together with other materials such that a multiple bandgap in parallel can be fabricated with enhanced absorption.

[0090] According to some embodiments, microstructures and voids are used to reduce the effective refractive index and capacitance to achieve the absorption mode high contrast grating effect and to reduce the effective capacitance of the device for lower RC time constants.

[0091] In addition, according to some embodiments, microstructures buried in the semiconductor can reduce lateral electrical and thermal conduction. Microwave

transmission lines are possible for example where high-density voids are buried in Si to reduce the dielectric constant and also eddy currents in the semiconductor resulting in low loss and dispersion. Voids can also be used for thermal isolation and to improve thermal conductivity by filling the voids with thermal conductors. This is useful in thermal management of components on a silicon substrate.

[0092] The enhancement using nanowires (Garnett et al, Light trapping in silicon nanowire solar cells, Nano Letters, 2010, 10, 1082-1087; Kelzenberg et al, Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications, Nature Materials, vol. 9, March 2010, 239-244) and nanoholes (Lin et al, Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications, Proceeding of SPIE, Vol. 7772, 77721G-1, 2010) have been reported. Nanowire is known to be used for light trapping in photovoltaic applications where the photogenerated carriers diffuse to the anode or cathode of a P-N junction with zero external bias operating at DC (direct current).

[0093] According to some embodiments, the photogenerated carriers are swept out with an external reverse bias in the absorbing "i" region of a P-I-N diode (PD) or P-I-P-I-N diode (APD) for high modulation bandwidth (greater than or equal to 10 Gb/s bandwidth) and high quantum efficiency and for APD for high current gain, with gain greater than 3 dB.

[0094] The cause or causes of the enhancement of the absorption coefficient are believed to include one or more of the following: an increase in optical field concentration, resonance effects, constructive and destructive optical interferences (amplitude and phase) effects, scattering, and high contrast grating (HCG) effects. See, e.g. Chang-Hasnain et al, High contrast gratings for integrated optoelectronics, Advances in Optics and Photonics 4, 379–440 (2012), hereinafter "Chang-Hasnain." The HCG effects are at the near-wavelength regime (See, Chang-Hasnain) where the optical wavelength in the material of the grating and the optical wavelength in the surrounding material of the grating is the range of the period of the grating.

[0095] FIG. 1 is schematic side cross section of three dimensional micro structures that enhance bulk absorption coefficient in photo sensitive devices, according to some embodiments. Microstructured pillars 110 and/or holes 120 are etched into the "I" Si layer 100. The optical wavelength in material M_1 is λ/n_1 where

n_1 is the refractive index of M_1 and the optical wavelength in material M_2 is given by λ/n_2 where n_2 is the refractive index of material M_2. The center to center distance L of the structures 110 can be between λ/n_1 and λ/n_2 or approximately 100-2000 nm, which is referred to as the near-wavelength regime. The diffraction regime is where L (one cycle) is greater than the wavelength, while the subwavelength regime is where L is less than the wavelength. The cross section of FIG. 1 shows the 3D (dimension) microstructured pillar/hole array, which enhances the bulk film absorption coefficient by factors of 1.5 to over 100. The period of the 3D pillar/hole microstructured array can be seen as a 3D high contrast grating, whose period of the grating Λ can lie between λ/n_1 where n_1 is the optical refractive index of material M_1 and λ/n_2 where n_2 is the optical refractive index of material M_2. If $n_1 > n_2$ then $\lambda/n_1 < \Lambda < \lambda/n_2$ where λ is the optical wavelength of the light to be absorbed by the microstructured pillar/hole array typically in the "I" region of a P-I-N PD or for APD, the absorbing "**I**" region P-**I**-P-I-N where the second "I" region is the multiplication region, or the wavelength of the optical signal to be detected by the PD and APD. At this near-wavelength regime of the 3D HCG microstructured pillar/hole array, the resonance Q (quality factor, or proportional to the ratio of the energy stored in the resonator/energy losses per cycle; where it is the optical cycle, the optical frequency impinging on the resonator or in the resonator) can be as high as 10^7 (see, Chang-Hasnain) if the HCG has minimal absorption loss as is known**.** In addition, in most cases the ratio of the index of the HCG to the surrounding material index need only be approximately 1.1 to observe the effects of the HCG.

[0096] The HCG effect that may explain the high enhancement of the absorption coefficient of the bulk material is that a single or multiple HCG layer (or a single microstructured pillar/hole array layer) due to its resonance effects and/or due to a varying of the microstructured pillar/hole period spacing, the optical signal resonating in the HCG/microstructured pillar-hole array can be directed to propagate in the plane of the HCG/microstructured pillar-hole array rather than normal to the surface. Together with resonance and in-plane propagation this can greatly increase the absorption path length in the HCG/microstructured pillar-hole array. According to some embodiments, the absorbing HCG mode is operated with a reverse voltage bias for PD/APD and a built-in bias (zero applied bias) in photovoltaic devices.

[0097] Using the phenomenon of near-wavelength and also deep-wavelength where the HCG period is much less than the optical wavelength, and the diffraction regime where the HCG period is greater than the optical wavelength (See, Chang-Hasnain) the microstructured pillar-hole-void array can have enhanced absorption coefficient over the bulk absorption coefficient by a factor of 1.1 to over 100.

[0098] According to some embodiments, the HCG effect is also used in the absorbing mode or lossy mode or low Q of 1-10000 (compared with known HCG that are in the non-absorbing mode or non-lossy mode to achieve high Q of greater than 1,000,000 and high reflectivity), in both buried/embedded (not fully buried) Ge microstructures in Si and buried/embedded void microstr Fig. 49: "Pillar with hole structures in either Ge or Si to improve the quantum efficiency (QE) and operating wavelength range of Si (400-1100 nm) and Ge (400 to 1800 nm) and Ge on Si photodiodes and avalanche photodiodes operated in a reverse bias mode of the pn, pin, pinip junctions (p and n can be switched for certain device configurations) that can be homo or heterojuction, crystalline or amorphous or any combinations thereof. In addition, the substrate can be on SOI or BOX or voids to reduce the index of refraction or effective index of refraction and the dielectric constant or effective dielectric constant (a dielectric with many voids can be represented as an effective dielectric constant, or equivalently effective capacitance).

[0099] Known silicon photodetectors have been limited to wavelength ranges of 200 to 1000 nm due to indirect bandgap of 1.1 eV. In particular, near the band gap wavelengths of 800-1000 nm, the frequency response of the silicon photodetector to a modulated optical signal at Gb/s rate is limited to 1.5 Gb/s approximately or less due to the weak absorption constant of Si at those wavelengths which are approximately 760 cm^{-1} at 850 nm and 67 cm^{-1} and 63 cm^{-1} at 980 and 1000 nm respectively, resulting in long absorption lengths of material, 30 microns or more, which results in low frequency response for the PD/APD. The wavelengths 850 nm is of interest since this is the standard wavelength for short distance (few meters to a few kilometers) multimode fiber optical datacommunication.

[00100] The amount of incident photons absorbed is approximately given by $\eta=1-e^{-\alpha L}$ where η (also the quantum efficiency if reflection off the surface of the PD is negligible) is the amount absorbed and "α" is α the absorption constant and "L" is the length length of the absorber. Using this equation and the absorption constant

of Si at 850 nm, 90% of the incident photons are absorbed at a depth of approximately 30 μm. Known high speed photodetectors typically have an absorption region of approximately 2 μm in length. The reason for this is that transit time and RC time of the photodiode need to be considered to have a bandwidth of 20 GHz (or approximately 30 Gb/s) or more and still have an external quantum efficiency of 80-90% or better.

[00101] Efficiency and bandwidth (transit and RC time): At a field strength of $6 \bullet 10^4$ V/cm the electron drift velocity is $1 \bullet 10^7$ cm/s at a temperature of 300 K. The 3 dB bandwidth of the photodetector due to transit time is given by: f(3dB)=0.45/t(transit) where t(transit) is the transit time for the carriers to cross the depleted high field region. FIG. 2 is a cross section diagram showing aspects of a typical structure of a PIN photodiode structure. Assuming negligible photocarriers generated in the P region 210 of the PIN 200 and mostly generated in the "i" region 220, the transit time is determined by the electron drift velocity and "d" (the high field "i" region). The PIN 200 is reversed biased (e.g. between -4 and -25 V). The "i" region 220 is fully depleted in this case. The RC time of the PIN structure 200 is determined by the capacitance, which is the ratio of the area ($\pi w^2/4$) of the PIN 220 to d.

[00102] According to conventional techniques, a 30 μm thick absorption layer ('i") to achieve 90% absorption for Si at 850 nm wavelength will give a transit time limited 3dB bandwidth of 1.5 GHz (approximately 2.2 Gb/s) which is too low for many current applications. Many current applications are in the 10-20 Gb/s range and in the near future 40 Gb/s. A d of 2 μm or less is desirable for current high-speed photodiodes in optical datacom applications to give over 30 Gb/s bandwidth.

[00103] RC time is another time to consider in photodiodes (applies to both APD and PD). The 3 dB bandwidth due to RC time is given by $f(RC)= 1/(2\pi RC)$; where C is the capacitance of the photodiode and R is the load resistance which is typically 50 ohms (and occasionally 25 ohms). Capacitance in the case of a conventional PIN structure photodiode with the "i" region fully depleted by the reverse bias, is just a parallel plate capacitance given by $\varepsilon A/d$ where ε is the dielectric constant of the material (multiplied by vacuum permittivity of $8.854 \bullet 10^{-14}$ farads/cm) which is 11.9 for Si, A is the area of the capacitor ($\pi(w/2)^2$), and d is the depleted "i" (i and I are used herein interchangeably). The f(RC) becomes larger

as d increases since the capacitance is decreasing with increasing d and a fixed area, where the diode diameter for example is 30 μm (diameters of high frequency PD/APD range from 5 to 60 μm). Diameter of diode for calculating the RC time is the total capacitive area of the diode that includes the photosensitive area and any metallization that may contribute to the overall capacitance.

[00104] The overall frequency bandwidth of the photodiode is a sum of the squares of the transit time and the RC time. This is given by the equation:

$$f=1/(2\pi(RC)^2+(\tau/2.4)^2)^{1/2}).$$

[00105] FIGs. 3A and 3B are plots showing bandwidth and QE, respectively, of a bulk conventional Silicon photodiode versus "d" in microns. From plots 310 and 312 in FIGs. 3A and 3B, for the combined f(3dB) of the transit time and RC time and the quantum efficiency η (assuming negligible reflection losses) we see that for bulk silicon to reach 10 Gb/s, the quantum efficiency (QE) is less than 40%, for a 30 μm diameter PD, which is too low for most datacom applications.

[00106] According to some embodiments, to overcome the relatively weak absorption of semiconductors with radiation energies near the bandgap and indirect bandgap semiconductors, for example Si at 850-1100 nm, a microstructured array is used that is etched into silicon that is grown by conventional methods epitaxially such as chemical vapor deposition (CVD) or metal organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), molecular beam epitaxy (MBE). Note that according to some embodiments, non semiconductors can be used: such as polymers, glass, ceramics, hybrid material such as transition metal oxides, hydrides, chlorides, sulfides embedded with semiconductor, metal, carbon nanoparticles and or atoms, which may or may not have a bandgap. The microstructured array of silicon consists of pillars of Si and/or holes in Si. See, Garnett and Yang, *Light Trapping in Silicon Nanowire Solar Cells, Nano Lett. 2010, 10, 1082–1087* (hereinafter "Garnett et al.") that experimentally demonstrates that an ordered array of silicon nanowires increased the optical path length of the incident optical radiation by 73 times greater than that of bulk silicon.

[00107] According to some embodiments, as described earlier, the concept of effective absorption coefficient is introduced. The effective absorption coefficient of the ordered array of Si nanowires is 73X that of bulk silicon; bulk α for Si is 760 /cm

and nanowire Si α is 5.548×10^4 /cm at 850 nm which is higher than direct bandgap III-V material.

[00108] It should be noted that the microstructures can also be epitaxially grown using methods such as VLS (vapor liquid solid epitaxial grown) nanowires or microwires (some nanowires have the largest dimension, such as the diameter, in the micron range, so that it can be called a microwire) with or without catalysts, or using a dielectric mask for selective area growth (SAG) epitaxy.

[00109] The nanowire array described in Garnett et al. has a diameter of the nanowire of approximately 390 nm using an array of beads of 530 nm as a dry etch mask. Roughly 1/2 of the Si material is etched away; the effective capacitance for the nanowire array is less than that of the bulk. The effective capacitance can be estimated as two parallel capacitors, one with Si and another with polyimide (filler) whose dielectric constants are 11.9 and 3.4 respectively. The area of each capacitor will be 1/2 that of a 30 μm diameter parallel plate.

[00110] With the effective capacitance lower, the overall 3dB bandwidth for a 30 μm diameter device is significantly higher. FIGs. 4A-4D are graphs showing the enhancement of bulk absorption coefficient vs bandwidth and QE for a microstructured Si photodetector, according to some embodiments. FIGs. 4A and 4B shows the bandwidth (plot 410) and quantum efficiency (plot 420) of a microstructured Si photodiode (PD) or avalanche photodiode (APD) at 850 nm wavelength photons impinging on the PD/APD either single or double pass. With an effective absorption coefficient (EAC) of 73X (412), 30X (414) or 15X (416) over bulk absorption coefficient (BAC), the bandwidth and QE are 54 Gb/s, 98%; 49 Gb/s 90%, 28 Gb/s 90% respectively for a 30 micrometer diameter PD/APD for example. At 1100nm, shown in plots 430 and 440 of FIGs. 4C and 4D, with enhancement, for example, of 172X QE of 90% and bandwidths of 26 Gb/s can be attained using Si microstructured PD/APD. Both PD and APD operate at a reverse bias of -2 to -50 volts range. APDs in general will have less bandwidth than PDs for the same geometry due to the added multiplication layer of the APD. In addition, APDs have a gain-bandwidth product. For simplicity, APD and PD are shown to be approximately the same.

[00111] According to some embodiments, a combination of low capacitance due to the gaps between the microstructured pillars and the enhanced absorption

allows the silicon photodiode and avalanche photodiode to operate at bandwidths greater than 10 Gb/s with high quantum efficiencies (> 90%) at 850 nm wavelength. This has not been demonstrated by conventional silicon PD/APD at these wavelengths. 850 nm is chosen as the nominal wavelength, but according to some embodiments, wavelengths can have values from 700 to 1100 nm.

[00112] According to some embodiments, the weak absorption in the bulk can be taken advantage of for photodetector applications since this will allow light at 850 nm and longer to pass through Si substrate and epitaxial layers toward the microstructured silicon with minimal optical loss and minimal photocurrent outside of the high field region, which can diffuse to the i-region and can cause the photodetector to have a degradation in frequency response.

[00113] According to some embodiments, the techniques described herein are applied to other semiconductors, polymers, organic films, glass, dielectrics, hybrid material such as glass, dielectrics, polymers embedded with nanoparticles of metal, semiconductors. According to some embodiments, one or more of the following are used: Ge, III-V material family such as InP, GaAs, GaN, InGaN; II-VI material family such as ZnSe, and also heterostucture material such as III-V grown on Si, Ge grown on Si. For example, for Ge on Si, microstructures are fabricated on the Ge to increase absorption which allows a shorter length of Ge to be used resulting in higher speed due to lower effective capacitance and shorter transit time for the carriers.

[00114] FIGs. 5A and 5B are cross sections showing aspects of a top illuminated microstructered PIN silicon photodiode, according to some embodiments. FIG. 5A shows the starting basic material structure 500. In FIG. 5B, silicon epitaxial structure is shown for a high-speed high efficiency microstructured photodiode 520. The photophoto diode 520 in FIG. 5B is designed for top illumination. According to some embodiments, BOX/SOI layer 504 may not be used. FIGs. 6A-B, *infra* show an example for bottom illumination. Note that with minor modifications the n and p doping can be switched and the direction of illumination may also be affected. Acccording to some embodiments, the illumination can be either perpendicular to the surface of the PD/APD or at an angle off perpendicular to the surface. According to some embodiments, in integrated structures where the optical signal is guided in an optical waveguide, the

microstructured absorption region can also be illuminated edge wise, directly into the microstructures or evanescently coupled to the microstructured i region.

[00115] FIG. 5B shows a microstructured pillar and or hole PD 520 in silicon with the starting material 500 consisting of a P-I-N Si layer grown on an Si substrate 502 that can be N doped or low doped in which case an extra N^+ layer is first grown on the substrate to minimize series resistance. The dimensions and doping of the layers can range as follows; N^+ cathode contact layer 506 (or a thin layer on top of 506, between 506 and 508) with N doping of greater than 5. $10^{17}/cm^3$, and thickness ranging approximately from 0.1 to 10 micrometers or more; N layer 506 with N doping greater than 5. $10^{17}/cm^3$, and thickness ranging approximately from 0.1 to 10 micrometers or more; I high field absorption region 508 with background doping of less than $5x10^{16}/cm^3$ and thickness ranging approximately from 0.1 to 5 micrometers depending on applications; and P^+ anode layer 510 with P doping greater than 5. $10^{18}/cm^3$ and thickness ranging approximately from 0.1 to 5 micrometers or more. The PD (and APD) photosensitive area (defined by the P-I-N or P-I-P-I-N junction area) is nominally 30 micrometers (10-80 micrometers in diameter are possible ranges) in diameter for 20 Gb/s or more bandwidth operation. According to some embodiments, the area can be larger for lower bandwidth or smaller for higher bandwidth operation. The Si microstructures of arrays of holes 522 and/or pillars 524 shown in FIG. 5B, which can be random, patterned or pseudo-random, are for enhancing the bulk absorption coefficient of Si to detect photons with wavelengths from 300-1100 nm. In the case of datacom applications, according to some embodiments, the optical signal wavelengths range from 750-1100 nm. A transparent conducting oxide and P-ohmic layer 526 is also provided.

[00116] The PD 520 is operated in a reverse bias mode, with negative voltage on the anode (P^+ layer 510 via P-ohmic and bond contact metal 528) and positive voltage on the cathode (N^+ layer 506 with N-ohmic bond contact metal 530) ranging from -1 to -20 volts. According to some embodiments, the PD structure 520 shown in Fig. 5B (and PD structure 620 in FIG. 6B, *infra*) can also be used for photovoltaic (PV) operation without any external bias.

[00117] As shown in FIG. 5B, the optical signal can impinge normal to the surface or at an angle off normal. In certain cases, optical signal coming in at an

angle off normal can have a higher QE and can also be at a certain rotation about the axis normal to the surface. This is to avoid the bald spot effect where some photons travelling normal to the surface can "see" bald spots whereas for photons illuminating at an angle off normal to the surface, the bald spots are hidden by other microstructures. This is not the case in near field optics where the spacing of the microstructures are of the order of the optical wavelength or subwavelength, the bald spots are not a significant issue.

[00118] FIGs. 6A and 6B are cross sections showing aspects of a bottom illuminated microstructered NIP silicon photodiode, according to some embodiments. The optical signal impinges on the photodiode 620 from the substrate side or bottom. The substrate 602 can be thinned to 10 microns or less by etching for example a via and stopping at the P layer or the photodiode can be fabricated on a BOX (buried oxide) or silicon on insulator (SOI) silicon wafer and the etch via can stop at the BOX layer 604 which can also be selectively etched to the silicon layer 606, the via 630 is as wide or wider as the photosensitive area of the photodiode 620. An antireflection layer (not shown) is applied to the silicon remaining layer 606 or the BOX layer 604 (the BOX layer 604 can be designed as a part of the antireflection layer for example) to minimize reflection (the BOX layer 604 can also be selectively etched off such that antireflection layer can be applied to the silicon P layer 606 to minimize multiple reflections). The back illuminated photodiode 620 has the advantage that a reflector 626 can be applied on the N layer 610 to reflect any light not absorbed on the first pass, in effect doubling the length of the "I" layer 608. The QE can be increased due to the extra length. In addition the reflector 626 on the N layer 610 can be smooth of textured to scatter (non-specular or diffused reflection) the light (optical signal) to optimize absorption by the microstructures (arrays of pillars 624 or holes 622). Since the length of the "I" region is effectively doubled, the transit time can effectively be reduce since only half of "I" is needed.

[00119] Bottom illuminated PDs such as PD 620 in FIG. 6B are also sometimes referred to back/substrate illuminated PDs, and top illuminated PDs such as PD 520 in FIG. 5B are also sometimes referred to front/surface illuminated PDs.

[00120] According to some embodiments, the basic structure of a microstructured Si photodiode such as shown in in FIGs. 5A, 5B, 6A and 6B, is

fabricated from a bulk thin film epitaxially grown silicon with a P-I-N structure on a silicon wafer which can be doped N type or not intentionally doped or low doped N type Si substrate with (100) orientation or other orientation such as (111).

[00121] According to some embodiments, the basic layer structures (such as layers 502, 504, 506, 508 and 510 of structure 500 of FIG. 5A, and layers 602, 604, 606, 608 and 610 in structure 600 of FIG. 6A) are all grown epitaxially using one or more of the following methods: chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), plasma enhanced chemical vapor deposition (PECVD), molecular beam epitaxy (MBE), atomic layer deposition (ALD), pulsed laser deposition (PLD) on Si substrate of either P or N or low doped or undoped) or BOX/SOI substrates.

[00122] Processing details have been left out for simplicity. According to some embodiments the following basic steps are carried out: first (for pillars, not necessary for holes), depositing the p ohmic contact metal layer using e-beam, thermal or sputtering deposition; second, photolithographically (or imprint lithography) defining the microstructure pattern either pillars or holes and forming the etch mask for either dry or wet etching; third, etching of microstructure patterns on the P and I layers partially or fully and can extend into the N layer; fourth, passivating the sidewalls of the microstructure patterns (pillars or holes) with thermal oxide to minimize surface recombination of the photogenerated carriers via surface states due to dangling bonds and other surface imperfections (other passivation techniques may also be applied such as ALD (atomic layer deposition) of Si oxides and Si nitrides); fifth, planarization (filler step) using either spin on glass, polyimide, or plasma enhanced chemical vapor deposition (PECVD) of dielectrics such as Si oxides and Si nitrides; sixth, etch back to expose the P layer or P ohmic metal layer (polyimide or spin-on glass may partially fill the holes or space between the pillars/microstructures); and seventh, ohmic and/or bond contacts formed on the P and N layers. In the case of top illuminated photodetectors, where the optical signal enters on the epitaxial surface where the microstructure patterns are fabricated, a transparent conducting oxide is deposited to connect all the P ohmic metal layers (for pillars). In the case where the microstructures are holes or voids the transparent conducting oxide layer is not used, according to some embodiments. A voltage bias is applied between the P

layer (anode) and the N layer (cathode) of -1 to -20 V, and the photodiode is operated in a reverse bias mode to deplete as much as possible the "I" layer, preferably the entire I layer.

[00123] FIGs. 7A and 7B are cross sections showing aspects of a microstructered avalanche photodiode, according to some embodiments. As in the Si microstructured photodiodes shown in FIGs. 5A, 5B, 6A and 6B, the epitaxial layers 700 for the APD 720 are grown first followed by microstructure processing. The microstructured avalanche photodiode 720 can be illuminated (e.g. with 300-1100 nm) from the top with transparent metal oxide P ohmic contact 726, or the P ohmic contact 726 can be a mirror to reflect the photons illuminating from the bottom (e.g. with 950-1100 nm) to have a double pass absorption. The double pass absorption greatly improves the RC time and the Transit time of the APD for a higher frequency response.

[00124] FIG. 8 is a cross section showing a silicon epitaxial structure for a high-speed high-efficiency microstructured APD, according to some embodiments. Layers 800 are shown prior to microstructure processing. With minor modifications, the n and p doping can be switched and the direction of illumination may also be affected. Starting with a N silicon substrate 802 (or low doped or silicon on sapphire or a BOX /SOI wafer depending on the application and packaging considerations), an N^+ layer 804 (N ohmic contact layer) is formed with doping concentration of greater than 10^{18} cm^{-3} (typically phosphorous) with layer thickness ranging approximately from 0.1 to 10 µm. A non-intentionally doped layer "i" 806 or a P^- (very low doping level P layer) has a doping concentration less than $5x10^{16}$ cm^{-3} (this is the multiplication or electronic gain layer of the APD) with thickness ranging approximately from 0.1 to 2.0 µm depending on gain and bandwidth of the APD. A P charge layer 808 is grown with an approximate thickness 0.05-0.2 µm and doping concentration of greater than $2x10^{17}$ cm^{-3}. An absorption layer 810 is grown (P^- or "i") ("I" and "i" are used interchangeably herein) with doping less than $5x10^{16}$ cm^{-3} with thickness ranging approximately from 0.1 to 5 µm. Finally a P^+ contact layer 812 is grown with doping greater than $5x10^{19}$ cm^{-3} with layer thickness ranging approximately from 0.1 to 1.0 µm. According to some embodiments, all layers 800 are grown epitaxially using CVD or MOCVD reactors.

Doping and thickness are approximate and are adjusted depending on applications.

[00125] For best noise performance of the Si APD, photogenerated electrons should dominate in the multiplication process; i.e. holes diffuse/drift toward p (anode) and electrons diffuse/drift toward the n (cathode) with reverse bias. The Si layers 800 are grown epitaxially using chemical vapor deposition, plasma enhanced chemical vapor deposition, molecular beam epitaxy, atomic layer deposition (can be a combination of these methods to generate the optimal layer structure in doping and interface quality) on doped or undoped substrates. The total length for the electrons to transit range from approximately 0.25 to 7.2 microns. This can be, for example, 0.5 μm for absorption, 0.1 μm for charge, 0.5 μm for multiplication, with a total of 1.1 μm for the APD layer structure 800 shown. According to some embodiments, for higher QE, the absorption region can be lengthened to one μm for a total transit length of 1.6 μm for example. Other layer thickness and doping concentrations can be adjusted to optimize device characteristics for different wavelength, integration with CMOS, application requirements, operating conditions such as bias voltage, gain and noise.

[00126] Also, the APD can be illuminated with modulated optical signal from the bottom, where using BOX or SOI, the bulk of the substrate can be removed to minimize optical losses and thus can use the double pass of the photons in the enhanced absorbing microstructured layer.

[00127] FIGs. 9A-9E are a series of cross sections showing some basic microstructure processing steps, for a high-speed APD, according to some embodiments. FIG. 9A shows the high speed APD epi structure 800 as described with respect to FIG. 8. In FIG. 9B, as in the PD process, a P-ohmic metallization or dielectric mask 910 can be deposited first on the P layer 812 for the microstructured pillars. In the case of holes and/or voids this step may not be carried out. Dry etch mask 910 is deposited on the surface using photolithography, metal/dielectric deposition techniques and wet/dry etching. In FIG. 9C, according to some embodiments, reactive ion etching (RIE) or deep reactive ion etching (DRIE), wet etching using chemicals and oxidation of the Si are used to generate the microstructured pillars 914. Native silicon oxide for surface passivation can be provided by thermal oxidation (which is preferred in some cases), electrochemical

anodization, and/or plasma enhanced chemical vapor deposition. According to some embodiments, the thermal oxidation of the pillars 914 can also be used to fine tune the diameter of the pillar since the oxide is created from the Si material. Thermal oxidation also smooths the surface which is favorable for electrical properties. In FIG. 9D a filler 916 is used to fill or partially fill the space between the Si pillars 914 to support subsequent contact layers to be deposited. The filler 916 can be spin on glass, polyimide, dielectric such as silicon nitride, or silicon oxide, that can be deposited for example using plasma enhanced chemical vapor deposition. Once the contacts are made the fillers can be left in place or removed by dissolving the filler with an etchant or solvent. Removing the filler has an advantage of further reducing the capacitance of the device since air has a dielectric constant of 1. The reduction of the capacitance allows the device to operate at higher bandwidth due to reduction of the RC time. In FIG. 9E, the anode and cathode ohmic contact metallizations 922, 924 and 926 are made. Depending on the direction of illumination, transparent conducting oxide TCO 932 (such as indium tin oxide ITO) can be used. In the case of top illumination, a dry etch can be used to expose the pillars if they are buried in the filler. The TCO 932 can then be used to contact the P^+ silicon pillars at the tip or the P ohmic metallization 922. Ohmic contact metallization is then applied to the cathode (N^+) layer either on the surface (924) or bottom (926) depending on integration topology.

[00128] In the case of the optical signal coming from the substrate side (the bottom), the wafer is thinned. If the thinning is carried out by etching it can include a buried silicon dioxide layer such as silicon on insulator, SOI/BOX, such that the oxide layer can act as an etch stop layer. The wafer can be thinned first by chemical mechanical polishing to 100 μm followed by a via etch to the oxide layer which can be selectively etched off, such that the optical signal only need to traverse a few micrometers of Si bulk material. Anti-reflection coating 930 is applied to the Si surface to minimize reflection loss. Ohmic metallization is applied to the N^+ layer followed by bond metal 924. On the microstructured pillars, ohmic metallization is applied to the P^+ tips (if its not applied already in the preliminary steps), followed by bond metal 922. According to some embodiments, an advantage of the optical signal entering from the substrate surface (i.e. the bottom)

is that the light will bounce and travel twice within the pillar structures, thus increasing the quantum efficiency. According to some other embodiments, the pillars can be made shorter to improve the transit time.

[00129] According to some embodiments, the optical signal can also enter from the edge as shown FIG. 52, *infra*, either in a guided mode or in free space. In the edge application, TCO 932 and solid anode ohmic contacts may not be used and wafer thinning may not be carried out. Cathode ohmic contacts can instead complete the structure. According to some embodiments, in edge approach, the pillars are arranged such that their density is not uniform to optimize the capture of the optical radiation. It can be arranged in a V pattern for example to reduce optical reflection.

[00130] Not shown in FIGS. 9A-9D are mesa etching steps used to define the diameter of the APD 920. According to some embodiments, other methods such as ion implantation may also be used. Note that the microstructures themselves provide good confinement of current in the vertical direction and not in the lateral direction. Other known processing steps that are not shown for sake of simplicity include: thermal oxidation passivation of exposed surfaces; adding guard rings; thinning of the wafer; adding anti-reflection coatings; annealing of ohmic contacts; and creating via holes for removal of filler.

[00131] Taking advantage of low absorption constant of bulk Si. High speed photodiodes made with III-V material often are constructed such than the photocarriers are generated only in the i layer of a PiN structure to minimize the photogenerated carriers outside of the high field region that can cause degradation to the frequency response of the device. This can be done easily in III-V material since there are many ternary and quaternary material such as InGaAsP, InGaAs, InAs, that are lattice matched to InP and the bandgap of these alloys can be changed by altering the composition such that the P+ anode 812 and P charge 808 layers are mostly transparent and the i layer is absorbing. However it is not easy for silicon since there are no materials that are lattice matched to silicon. Germanium can be grown on silicon but with the addition of a buffer layer to accommodate for the lattice mismatch.

[00132] According to some embodiments, a method to overcome this issue in silicon is to take advantage of the low absorption constant of silicon at radiation

near the bandgap of silicon. According to some embodiments, the wafer can be thinned to the insulator of an SOI structure and the 850 nm optical signal will only traverse 1-2 μm of bulk silicon losing approximately 10% or less of the incident radiation. The rest of the radiation continues to the microstructured pillar silicon where the absorption is stronger possibly due to resonance effects. According to some embodiments, the shape of the pillars can be circular, oval, rectangle, chevron, hexagon, double-circle, crescent, star, or any shape to optimize absorption and collection efficiency. The pillar diameter range from 50-1200 nm (smallest dimension can be 50 and largest dimension 1200 nm) and can be spaced uniformly or non-uniformly, periodic or aperiodic, chirped, or a pattern either locally or globally to optimize APD/PD performance and applications. The spacing of the pillars can be 20-2000 nm. The microstructured pillars can be 100 to 10000 nm in length that is optimized for bandwidth and efficiency for a particular wavelength near the silicon bandgap for example 850, 880, 980, 1000 nm.

[00133] According to some embodiments, multiple dimensions (both structure and spacing) of the microstructures within a single PD/APD can broaden the resonance bandwidth of the microstructures such that the enhanced absorption coefficient is over a broader optical spectrum.

[00134] The substrate becomes less absorbing as the wavelength approaches 1100 nm (1.1 eV Si indirect bandgap).

[00135] According to some embodiments, the microstructured pillars/holes/voids can have orientations that are not perpendicular to the surface of the silicon substrate. Other orientations off perpendicular or with multiple orientations or even random or pseudo-random are possible to optimize the QE with respect to the directivity of the optical signal. In multiple and/or random or pseudo random orientations of the microstructures, the device become less sensitive to the direction of light illumination which is beneficial in PV applications. In certain applications, antenna like high directivity of the PD/APD may be desirable to avoid cross talk for example from other optical signal sources or to further improve its QE.

[00136] According to some embodiments, microstructured hole arrays, instead of pillar arrays, are used as light traps in silicon. Microstructure hole arrays have similar properties as microstructured pillars. See e.g. Lin et al, Optical absorption

enhancement in silicon nanowire and nanohole arrays for photovoltaic applications, Next Generation (Nano) Photonic and Cell Technologies for Solar Energy Conversion, edited by Loucas Tsakalakos, Proc. of SPIE Vol. 7772, 77721G (2010). According to some embodiments, instead of etching microstructured pillar arrays as described herein, microstructured hole arrays are etched using RIE/DRIE and similar processing for the pillars, including thermal oxidation for surface passivation, deep ion implantation for electrical isolation, confinement of optical fields and reduction of capacitance. In the case of the hole arrays, it is possible that the filler need not extend the entire length of the hole. For example, if the surface tension of the filler is high, only partial filling of the holes with filler will be possible and provide support for subsequent layers of TCO, metal, oxide, silicide, alloys to name a few that may be necessary to complete the device structure. According to some embodiments, in the case of microstructured holes, fillers are not used in the PD/APD/PV devices since the surface is contiguous rather than consisting of islands as in the case of microstructured pillars.

[00137] According to some embodiments, the microstructured holes can have diameters of 50-3000 nm and can be a square, hexagon, oval, rectangle, chevron, double-hole, with the smallest dimension at 50 nm to the largest dimension of 3000 nm approximately. The spacing between holes (adjacent edges) can be regular or irregular or a pattern at 20-2000 nm. The depth (or length) of the hole can be 100 to 10000 nm and can be uniform depth or non-uniform depth. Dimensions are chosen for optimal absorption, quantum efficiency, bandwidth and radiation collection efficiency for a particular wavelength and application.

[00138] As discussed earlier, to optimize High Contrast Grating in the Absorption regime of this invention, it may be desirable to have the microstructured enhanced absorption structures on materials of a lower refractive index such as BOX or SOI where the silicon dioxide refractive index is lower than that of Si, Ge or III-V/II-VI material. According to some embodiments, the effective refractive index can be made lower than the refractive index of the microstructures with the inclusion of voids in the substrate. FIGs. 10A-10B are cross sections showing aspects of a top illuminated microstructered photo diodes, avalanche photo diodes and/or photovoltaics (PV) with microstructured voids in N-Si, according to some embodiments. Voids can be included in the substrate or as a microstructure for

enhancing absorption coefficient as will be discussed *infra*. Refractive index in the optical spectrum of Si, Ge, III-V material typically range from 3-3.6, by using silicon dioxide such as SOI and voids that are 50% of the material in volume, the refractive index or effective refractive index can be reduced to approximately 0.5 that of the bulk semiconductors. By adjusting the ratio of the volume of the voids to the material (Si for example) the effective refractive index can also be adjusted from a few percent to more than 90% that of the bulk material. The voids can be filled with other material such that it is not just air, gas or vacuum, but a dielectric such as glass, polymer, dielectric, oxide, or amorphous semiconductor that can be optically and/or electrically passive and or active with optical and/or electrical gain for example.

[00139] FIG. 10A shows the layers 1000 including N-Si layer 1006 which contains microstructured voids 1008 that effectively reduce the refractive index of the N-Si layer 1006 as described. FIG. 10B shows a top illuminated PD/APD/PV 1020 that includes microstructured pillars 1024 and/or holes 1022, as well as transparent conducting oxide layer 1026. Microstructered voids 1008 can be random or patterned. The microstructered voids 1008 can be used reflect photons back to the absorbing "I" region if the voids 1008 are patterned to have HCG effects at wavelenghs where loss is low such as 950-1100 nm. According to some embodiments, BOX or SOI substrates can also be used together with voids or without voids or without BOX/SOI.

[00140] According to some embodiments, the microstructuring techniques described herein are also applied to heteroepitaxial material (III-V on Si, Ge on Si, or II-VI on Si). Ge (bandgap 0.66 eV at 300K) having much smaller bandgap than Si, can be used for detecting optical signals at 850 and 1300 nm. Using the techniques described herein, Ge devices can also be made to detect optical signal with wavelength at 1550-1600 nm which can than replace III-V material based photodetectors. According to some embodiments, microstructures are grown such as nano/microwires or etched from bulk material with or without lithographic masking.

[00141] Ge thin film can be grown epitaxially on Si. See, e.g. Kang et al, Epitaxially-grown Ge/Si avalanche photodiodes for 1.3μm light detection, 23 June 2008 / Vol. 16, No. 13 / OPTICS EXPRESS 9365 (hereinafter "Kang et al."), where

an APD was fabricated for 1310 nm wavelength operation for a 30 μm diameter device. The QE of the device with a 1 μm Ge absorption length is only 56% whereas by using microstructured pillars/holes/voids according to embodiments described herein, QE of approximately 90% or greater can be achieved at 1300-1600 nm wavelength with bandwidths of approximately 30 Gb/s or greater for a 30 micrometer diameter PD/APD. Such devices can find useful applications in datacenters, local area networks, and in metro and long distance optical data/telecommunications. According to some embodiments, integration on silicon is used which results in significant cost reduction in manufacturing and packaging. In comparison, in Kang et al. a 30 μm diameter APD was only able to reach approximately 15 Gb/s bandwidth at 1310 nm and cannot extend the wavelength due to low absorption of the bulk material without sacrificing a significant reduction in bandwidth.

[00142] FIGs. 11A and 11B are cross sections showing aspects of an heteroepitaxial APD structure of Ge on Si, according to some embodiments. Layers 1100 and APD device 1120 show a possible heteroepitaxial APD structure of Ge on Si (as opposed to descriptions, *supra*, of homoepitaxial APD/PD structure where only silicon is used with different doping concentrations). Similar processing methods as in the homoepitaxial Si APD are used to fabricate microstructured pillar/hole arrays. According to some embodiments, the absorption constant of bulk Ge is enhanced by greater than 70X, for example 73-172X. According to some embodiments, APDs and PDs with bandwidths in excess of 30 Gb/s can be achieved in devices with an active diameter of 30 μm or less at wavelengths to 1750 nm and QE of approximately 90% or greater. This is a significant improvement over existing Ge on Si APD with illumination normal or off normal to the surface of the substrates.

[00143] According to some embodiments, the microstructured pillar and hole (and variations thereof) arrays can be fabricated in Si, Ge, Ge on Si, SiGe on Si, SiGe on Ge; it can be any combination of Si,Ge and SiGe.

[00144] At longer wavelengths 1200-1800 nm, Ge (germanium) photodiodes are often used since Ge has a bandgap of 0.66 eV (whereas Si has a bandgap of 1.1 eV). However, for high bandwidth applications (greater or equal to 20 Gb/s) Ge photodiodes are only good to 1350 nm due to the fact that for transit times to be

approximately 30 picosec (electron saturated drift velocity is $6x10^6$ cm/s at $1x10^4$ V/cm in order to have a bandwidth of approximately 20 Gb/s ($f(3dB)=0.44/\tau$ where τ is the transit time through the "I" region) the length of the absorption region or the "I" region is limited to approximately 2 microns. At this length, the QE at 1550 and 1600 nm is less than 10%, which is not generally acceptable for optical receivers for datacom and telecom applications. In a waveguide configuration, the length of the absorption region can be 50-100 microns and still achieve 20 Gb/s or higher with QE equal or greater than 90%. The waveguide Ge on Si photodiode structure have been reported by other research groups however such waveguide photodiodes have excess optical losses due to waveguide losses and coupling loss (coupling of optical signal to the optical waveguide) which can be as high as 3 dB or half of the optical signal is lost. The "free-space" coupling (where the optical signal is directed to the PD/APD using elements such as lens, diffraction elements, light pipes, optical waveguides to name a few) of optical signal to the microstructured photodiode and avalanche photodiode have much less optical losses, typically a few percent or less. One of the reason is the large area of the microstructured PD/APD which is 30 microns in diameter as compared to waveguide photodiodes its dimensions are a few microns, typically 1-2 microns. Not only is coupling loss high in waveguide PD/APD, it often uses active alignment which requires that the waveguide PD/APD is turned on to monitor the coupling of the optical signal into the waveguide PD/APD. This active alignment is slow and time consuming which adds cost to the packaging of the waveguide PD/APD in any optical receiver module. In contrast, the large area microstructured PD/APD, according to some embodiments, uses only passive alignment where it is aligned without turning on the microstructured PD/APD. Such alignment is much faster and easier which reduces the cost of a microstructured PD/APD in any optical receiver module. It should be noted that with the effective capacitance of the microstructured PD/APD significantly lower than bulk PD/APD by 10 to 80% or more, the area of the microstructured PD/APD can be correspondingly larger by 10 to 80% or more.

[00145] In FIG. 11B, a microstructured Ge on Si pillars/holes APD structure 1120 with bottom illumination is shown. Epitaxial layers for an APD Ge on Si are used where the optical absorption to generate electron-hole pairs takes place in Ge

and the gain/multiplication of the electrical charged carriers takes place in Si. The epitaxially grown layers are similar to Ge on Si bulk (thin film) APD with the following layer compositions ranges (shown in FIG. 11A). N is undoped, or low doped (20 ohms-cm) Si substrate 1102, which can also be SOI or BOX, to allow removal of the Si substrate for bottom illumination and/or to reduce the refractive index. If SOI or BOX substrates are used, the N ohmic contact and bond metal will be on the N^+ -Si surface adjacent to the multiplication I region. N^+ contact layer 1104 which can be 2-8 microns, $N^+ > 5.10^{18}\ cm^{-3}$. I multiplication layer (or gain layer) 1106 which can be undoped (not intentionally doped), 0.2-1.0 microns thick and $I < 1.10^{16}\ cm^{-3}$. P charge layer 1108 having a thickness of 0.05-0.2 microns and P ~ 1-6. $10^{17}\ cm^{-3}$. P^- low temp Ge buffer layer 1110 having a thickness of ~ 0.01-0.04 microns and $P^- \sim < 1. 10^{16}\ cm^{-3}$. I or P^- absorption layer 1112 having a thickness of 0.2- 2.0 microns, and I (or P^-) $<1. 10^{16}\ cm^{-3}$. Finally, P^+ contact layer 1114 has a thickness of 0.05- 0.2 microns, and $P^+ > 2. 10^{20}\ cm^{-3}$, approximately.

[00146] Starting with a wafer with all the layers 1100 grown for APD operation, the processing details are left out for simplicity. The basic steps involve first, depositing the p ohmic contact metal layer 1126 using e-beam, thermal or sputtering deposition. The microstructure pattern of either pillars or holes is photolithographically, using positive or negative or image reversal photoresist methods depending on pillars or holes, defined to form the etch mask for either dry or wet etching. According to some embodiments imprint lithography can be used. The microstructure patterns are etched on the P^+ and I (or P^-) and P Ge layers 1114, 1112 and 1110, respectively, partially or fully to the P Si layer 1108 (e.g. using fluorine, chlorine, bromine based gases such as SF_6, CF_4, BCl_2, Cl_2, for selective dry etching using RIE and DRIE). The selectivity of the etch between Ge and Si can be as high as 70, so as to etch Ge 70 times faster than Si by adjusting gases mixtures, pressure, temperature and bias, and power. The sidewalls of the microstructure patterns (pillars or holes) are passivated with dielectric or SiGe and gradually reducing the Ge content such that Si remains on the surface (using for example atomic layer deposition ALD) and subsequently using thermal oxidation to minimize surface recombination of the photogenerated carriers via surface states due to dangling bonds and other surface imperfections. According to some embodiments, other passivation techniques may also be applied such as ALD of

Si oxides and Si nitrides. Planarization is performed using either spin on glass, polyimide, or PECVD deposition of dielectrics such as Si oxides and Si nitrides. An etch back is performed to expose the P layer. For microstructured holes and pillars, it may not be necessary to planarize completely, by using polyimide or spin-on glass to partially fill the holes and spaces between pillars. Ohmic and/or bond contacts are formed on the P and N layers. For top illuminated photodetectors, where the optical signal enters on the epitaxial surface where the microstructure patterns are fabricated, a transparent conducting oxide 1126 (the transparent conducting oxide may not be used in the case of microstructured holes) is deposited to connect all the P ohmic metal layers (for pillars). A voltage bias is applied between the P^+ Ge layer 1114 (anode) and the N^+ Si layer 1104 (cathode) of -2 to -45 V. The APD 1120 is operated in a reverse bias mode to deplete as much as possible both of the "I" layers. Many detailed processing steps are left out such as annealing, surface preparations, deposition of ohmic contacts, bond metal, RIE, DRIE, wet etching, masks for etching, mask removal, antireflection coatings, mirrors such as Bragg reflectors on the microstructured layers, to name a few. Ohmic contact metallization to P and N semiconductors and bond metallizations are well known in the art and details are not mentioned here. Also, holes are used in electron-hole pairs as charged electrical carriers and holes as in a physical void such as the microstructured holes. From context it should be understood if "hole" refers to a charged electrical particle or a physical void.

[00147] According to some embodiments, Ge surfaces of the microstructured pillars or holes and any Ge surfaces exposed to an electric field, where electric current can flow and/or where electric charges are formed are passivated to reduce current leakage, minimize surface states that can be a potential sink or recombination centers for carriers, especially photogenerated carriers of electrons and holes (as in Si, thermal oxide or rapid thermal exidation, to create SiO_2 and SiO_x used to passivate any silicon surfaces that can cause excessive leakage current or recombination centers for photogenerated carriers, or a carrier sink) and GeO_xN_y which is a native Ge oxynitride that is formed in two stages, where the Ge microstructured pillars and/or holes are first exposed to oxygen and then to ammonia ambient in a rapid thermal annealer to form the Ge oxynitride passivation layer. These passivation methods are well known in the art.

[00148] FIG. 12 is a cross section illustrating aspects of a passivation method for Ge surfaces on microstructures, according to some embodiments. Shown are microstructured Ge pillars 1202 (or holes) for a PD and/or APD. On the Ge surfaces is conformally epitaxially grown SiGe layer 1210. Gradually, the Ge content is reduced within layer 1210 until only Si is exposed on the surface. Thermal oxidation of Si is then used to passivate the exposed Si surfaces, forming SiO2 layer 1212, to minimize leakage current and surface states that can be a potential sink for carriers, especially photogenerated carriers (electrons and holes) that can degrade QE.

[00149] FIGs. 13A and 13B are graphs showing the effects of mictrostructure enhancement of Ge bulk absorption coefficient for photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments. According to some embodiments, a 73x enhancement of bulk absorption coefficient is gained in PD/APD devices having microstructured pillars/holes at 1550 and 1600 nm. FIG. 13A shows the bandwidth verses "d" or the length of the "I" layer for 1550 nm (point 1310) and for 1600 nm (point 1312) Note that APDs have both a Ge "I" layer and an Si "I" layer; whereas for PDs have just a Ge "I" layer. FIG. 13B shows QE verses "d" or "I" layer length for 1550 nm (point 1320) and 1600 nm (point 1322). It can be seen that for a 30 micron diameter active region PD/APD bandwidths of 40 and 31 Gb/s can be attained at 1550 nm and 1600 nm optical wavelength respectively with 90% QE. This result was not achievable with bulk Ge photodiodes and avalanche photodiodes of conventional design.

[00150] The separation of using Ge microstructures to absorb the light generating e-h (electron-hole) pairs and using Si for the avalanche multiplication of the carriers, preferably electrons, results in an APD with very low noise due to the fact that the ionization ratio (defined as hole ionization rate/electron ionization rate) for electrons injected into the multiplication region (gain region which is a function of applied reversed bias voltage) is lower than in III-V material family. This result in a low excess noise factor leads advantageously to a high signal to noise ratio (S/N).

[00151] FIGs. 14A-14B are cross sections showing aspects of a top-illuminated Ge on Si avalanche photodiode having microstructured pillars/holes, according to some embodiments. FIG. 14A shows the bulk layers 1400. In FIG. 14B, top

illuminated microstructured Ge on Si APD 1420 is shown with a semitransparent conductive oxide 1426 connecting the P-ohmics on the Ge microsturctured pillars 1424 (holes 1422) as described *supra*. Both top and bottom illuminated microstructured Ge on Si share similar epitaxial structures. The processing steps for top and bottom illuminated microstructured APDs are similar. The main differences are that the transparent conductive oxide for top illuminated APD (or PD) is replaced with an opaque ohmic/bond metallization that can act as a mirror to reflect the optical signal back toward the absorption I layer. According to some embodiments, the mirror can also consist of Bragg reflectors either wafer bond to the microstructure or epitaxially or vacuum deposited such as dielectric or conductive metal dielectrics to enhance the reflectivity to greater than 90% of the optical signal. In addition, bottom illuminated PD/APD may require a window or via where most of the Si substrate is removed to reduce optical losses depending on the wavelength of the optical signal.

[00152] FIGs. 15A-15C are cross sections illustrating aspects of bottom-illuminated Ge on Si avalanche photodiodes having microstructured pillars/holes, according to some embodiments. FIG. 15A shows the bulk layers 1500 prior to forming the microstructures (pillars and/or holes). FIG. 15B shows a Ge on Si microstructured APD 1520 with the optical signal illuminating from the bottom (substrate side) for wavelengths from 1200-1800 nm. Note that Si is basically transparent at these wavelengths. According to some embodiments, to further reduce optical losses, the Si wafer can be thinned just at the area of illumination, for example through a via of 50-500 microns in diameter and thinned to the N^+ layer of the Si; or the Si substrate 1502 can include a BOX or SOI layer 1502. The Si substrate 1502 can then be thinned selectively to the BOX or insulator layer 1502 which can be etched away selectively. According to some embodiments, an anti reflection layer (not shown) can be added to minimize reflection. The advantage of this arrangement is that the optical signal will have a double bounce, reflecting off the metallization 1526 on the Ge P^+ layer 1514 and traversing the Ge "I" absorber region 1512 once again. For example, as shown in FIGs. 13A and 13B, keeping the same absorption length, Ge "I" length, the QE for both 1550 and 1600 nm would be approximately 90% or higher for a Si substrate side (bottom) illumination by the optical signal assuming negligible reflection loss. According to some

embodiments, the Ge "I" absorption length can be further shortened to increase the bandwidth and still maintain acceptable QE.

[00153] For Ge epitaxially grown on Si, it is known that the bulk absorption coefficient is greater than that of Ge bulk by itself (not grown on Si); at 1750 nm the Ge on Si absorption coefficient is approximately 100 cm^{-1}. According to some embodiments, this can be enhanced by the microstructured pillars and/or holes by 172 times. The resulting enhanced Ge on Si microstructured pillar and/or holes absorption coefficient can be about 1.72. 10^4 cm^{-1}.

[00154] FIG. 15C shows an APD 1540 in which the microstructure extends all the way to the N cathode layer 1506 to further reduce capacitance and refractive index. In this case, the absorbing i layer 1512 is microstructured as is the charge layer 1510 and the i multiplication layer 1508. According to some embodiments, the microstructures can also be formed partially into the charge and multiplication layers 1510 and 1508. Additionally, according to some embodiments, the microstructures in the absorbing layer 1512 and the multiplication layer 1508 need not be the same. In FIG. 15D, photons may generate electron hole pairs in the multiplication region which may contribute to added gain but also may contribute to excess noise. According to some embodiments, the absorption and multiplication region using the microstructure APD is combined in one region without the use of the charge layer. This is possible due to enhanced absorption: the length of absorption and multiplication can be of the order of one micron or less allowing reasonable avalanche voltage.

[00155] FIG. 15D shows a microstructered APD 1560 where the absorption and multiplication region are a single region 1566, pillars or holes, according to some embodiments. This is enabled by the microstructure enhancing the absorption coefficient so that less than one micron of the absorbing microstructure length is needed to achieve QE of approximately 90% or more and avalanche multiplication can also occur in this length of material. For example, if 0.5 μm of microstructured Si shown in Fig.15D is the thickness of layer 1566, a back illuminated APD 1560 allows a double bounce of the optical signal reflecting off the N ohmic contact and bond metallization resulting in an effective length of one micron of absorption length. The Si APD 1560 can operate at 0.5 μm multiplication length resulting in gain of 3 dB or more with a reverse bias ranging from -5 to -50 volts. According to

some embodiments, the structure shown in FIG. 15D can be applied to other material systems such as Ge, Ge on Si, III-V, and III-V on Si or not on Si.

[00156] FIGs. 16A and 16B are graphs comparing single pass and double pass photodiodes and/or avalanche photodiodes based on Ge on Si, according to some embodiments. Points 1610 and 1620 show the bandwidth and QE values for single pass with d of approximately 1.4 microns and points 1612 and 1622 show the bandwidth and QE values for a thinner d of approximately 0.7 microns single pass. For double pass the device will have points 1612 for bandwidth and point 1622 for QE. At 1750 nm optical signal wavelength, using absorption coefficient data of 100/cm for Ge on Si and with, for example, 172 times (172X) enhancement factor due to the microstructured Ge on Si photodiode/avalanche photodiode structures, a bandwidth of 27 Gb/s and a QE of approximately as high as 90% can be attained with an "l" (also "d") length of approximately 1.4 microns for a single pass (top illuminated - where the optical signal illuminates the top Ge microstructured side). As mentioned earlier, for photodiodes the "l" or "d" is the absorption length, whereas for avalanche photodiodes the "l" is the combined absorption length and the multiplication length. For example, for an APD to achieve 27 Gb/s the total "l" length needs to be limited to 1.4 microns. A double pass arrangement can be used such that for example the absorption length is 0.9 microns and the multiplication is 0.5 microns, making the absorption length effectively 1.8 microns to achieve QE above 90%. However, if we instead have the optical signal illuminate from the bottom Si substrate side, the Si substrate and Si layers are basically transparent and have minimal optical losses (approximately 1-3 dB/cm) at optical radiation energies that are below the bandgap of Si (1.1 eV or 1127 nm wavelength at 300K) for example for radiation from 1200-1800 nm wavelengths. The advantage of illuminating from the Si substrate side (bottom) is that the optical signal can have a double pass at the Ge "l" absorbing region if the metallization on the P^+ contact layer is reflective which it should be since it is metallic composing of Au, Al, Ag, Cr, Zn, Ti, Ta, Ge, or a combination of these metals and semiconductors. Bragg reflectors consisting of material with alternating refractive indices from oxides, nitrides, chlorides, semiconductors, either wafer bonded to the microstructures or deposited on the microstructures can also be incorporated. Reflectivity can be greater than 90%. With double pass, as shown in

FIGs. 16A and 16B, a bandwidth of 40 Gb/s can be attained with a QE approximately as high as 90% or more.

[00157] FIGs. 17A-17B are cross sections showing aspects of a top-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 700 to 1800 nm, according to some embodiments. FIG. 17A shows the bulk layers 1700. In FIG. 17B, Ge on Si microstructured pillars 1724 and/or holes 1722 are in a configuration for photodiode 1720. This is essentially a P-I-N structure where the "P" and "I" are Ge with microstructured pillars 1724 and/or holes 1722 to enhance the bulk absorption coefficient of Ge grown on Si. The increase in the absorption coefficient of Ge grown on Si (Ge on Si) could be due to the stress build in the Ge epitaxial layer due to lattice mismatch with the Si host substrate that it is grown on. Optical signal as in the case for Ge on Si APD can be illuminated from either the microstructured side (as in FIG. 17B) or the substrate side (as in FIG. 18B).

[00158] FIGs. 18A-18B are cross sections showing aspects of a bottom-illuminated Ge on Si photodiode structure having microstructured pillars/holes for applications with signal wavelengths ranging from 1200 to 1800 nm, according to some embodiments. FIG. 18A shows the bulk layers 1800. FIG. 18B shows photo diode 1820 configured for signal illumination from the Si substrate side (bottom illumination) with photo energies that are less than the Si bandgap of 1.1 eV at 300K. The corresponding wavelength range is 1200 to 1800 nm. Ohmic contact 1826 can also act as a mirror such that the light makes a double pass of the Ge absorbing microstructures where the metal contact layer on the P Ge can reflect the optical signal back toward the Ge "I" absorbing layer.

[00159] It should be noted that in all the discussions of the P-I-N structures, according to some embodiments the P and N are interchanged such as with an N-I-P structure formed on a P substrate or on a low doped P substrate or undoped substrate. According to some embodiments, the N and P for the APD structures are also interchanged and the substrate can be P, low doped P or undoped. However, in an Si multiplication layer, to achieve the lowest noise and the best S/N, electrons are injected into the multiplication region as dominantly as possible since the ionization rate of electrons is higher than the ionization rate of holes in Si; the ionization ratio for Si can range from 0.06 to 0.002 where as compared to Ge

and InGaAs it is 0.9 and 0.45 respectively. This is why in many of the embodiments described herein the enhanced absorption is in Ge microstructures and the gain or multiplication which is dependent on the field strength and therefore on the applied reverse bias voltage which for the described devices can range from -10 to -60 V, is in Si.

[00160] According to some embodiments, the microstructured pillars and or holes for Si and Ge on Si photodiodes (PD) and avalanche photodiodes (APD) are used to replace relatively expensive III-V photodiodes. The Si microstructured pillars and holes PD/APD can operate from 500 to 1100 nm at bandwidths of 20 Gb/s or higher and QE of 90% or higher. In particular, the datacom wavelengths of 730-980 nm. The microstructured pillars and or holes on Ge epitaxially grown on Si PD and APD can operate from 500-1800 nm with bandwidths of 20 Gb/s or more and QE of 90% or more. In particular, the telecom wavelengths of 1250-1600 nm and possibly to 1750 nm. The techniques described herein thus extends the wavelengths, bandwidth and QE of conventional Si and Ge on Si free space coupled photodiodes and avalanche photodiodes.

[00161] According to some embodiments, the microstructured pillars can also be fabricated using VLS (vapor-liquid-solid epitaxy) growth of Ge nanowires on an Si substrate. Others have demonstrated the growth of vertical Ge nanowires on Si (111) orientation for example, with Au nanoparticles as catalysts for the VLS epitaxial growth using chemical vapor deposition (CVD) or metal organic chemical vapor deposition (MOCVD). Crystal orientations other than (111), or with materials with multiple orientations such as in polycrystalline may be used. Materials such as Si, Ge, III-V, glass, quartz, metal, to name a few can also be used as substrates. According to some embodiments, a thin Ge buffer layer of approximately 2nm on Si (111) substrate is formed together with Au nanoparticles as catalysts for VLS growth in a CVD reactor. The Au catalyst can be deposited using a lithography mask to expose photoresist that is coated on the Si substrate. The Au is evaporated onto the Si substrate with patterned photoresist. Using standard processing methods such as lift-off, the Au pattern is left behind on the Si substrate which is then the catalyst for Ge VLS growth on Si substrates. According to some embodiments, it can also be grown using selective area growth where a dielectric

mask is deposited on the Si substrate with a pattern of voids that allow Ge to grow in the void using CVD.

[00162] The microstructure of pillars and holes on the surface of a bulk photodiode not only enhance the absorption coefficient by factors ranging from 10-200 over the absorption coefficient of bulk material (material without any microstructured features and grown on lattice matched substrates so that stress due to lattice mismatch is minimal) but also significantly reduce the capacitance of devices such as PDs and APDs. The reduction in capacitance allows the PD or APD to have a shorter absorption length, which in turns result in a faster transit time for the photogenerated carriers to be swept out of the high field region. The absorption region typically is depleted as much as possible by the reverse bias voltage that is applied externally with an electric field strength approaching 10,000 V/cm or higher. If the microstructured pillars or holes can result in removing half or more of the semiconductor material, which for silicon has a dielectric constant of 11.9 and germanium have a dielectric constant of 16, replacing the removed material with either air (dielectric constant of 1) or polyimide (dielectric constant of 3.5) or other dielectrics with low dielectric constants, then the overall capacitance can be estimated to be the sum of the capacitance due to the total area occupied by the semiconductor and the capacitance due to the area occupied by air or polyimide. C(total)=C(semiconductor)+C(air or polyimide) where C= $\varepsilon A/d$ where ε is the dielectric constant times the free space permittivity ($8.854\ 10^{-14}$ farads/cm), A is the area occuped by the semiconductor or air/polyimide and d is the length of the "I" region which can be the absorbing region or the absorbing and multiplication region as in the case for APD. From the equation for C(total), the more semiconductor material which has a high dielectric constant removed and replaced by low dielectric material such as air/polyimide/ SiOx/spin on glass the lower the overall capacitance and the faster the RC time. This reduction of capacitance for PD and APD invention can be extended to other PD and APD such as those of III-V material, microstructures can be fabricated on its surfaces and extend into and pass the optical signal absorbing regions to remove half or more of the semiconductor material to reduce its capacitance and can effectively make a larger area PD/APD and have the same bandwidth as before etching microstructures on the device. The larger area allows for easier coupling of the optical signal to the

photodetector. A simple formula for the increase in radius for example by replacing semiconductor material with low dielectric material is: $r=(\varepsilon_1/((\varepsilon_1-\varepsilon_2)x+\varepsilon_2)))^{1/2} r_o$ where x is the fraction of semiconductor area left, ε_1 is the dielectric constant of the semiconductor, ε_2 is the low dielectric material such as air or polyimide or spin on glass, and r_o is the radius of the active area of the PD/APD before etching microstructured pillars and or holes. As an example, for a 20 micron diameter Ge photodiode with $\varepsilon_1=16$ and for simplicity $\varepsilon_2=1$ (air) and x=.5 (half of the semiconductor material is removed in the microstructured pillar or holes), the increase in the new radius with the same capacitance as the non-microstructured Ge PD is 13 microns or a diameter of 26 microns which is significantly larger than 20 microns and can significantly reduce the cost of coupling the optical signal into the microstructured large area photodetector. This reduces the cost of passive packaging of the optical receiver module and increase the yield.

[00163] FIGs. 19A, 19B and 19C are diagrams illustrating how mictrostructures can reduce capacitance of a photodiode such that a larger area photo diode can be fabricated with the same bandwidth and QE, according to some embodiments. FIG. 19A shows the bulk layers 1900 in an InP-InGaAs-InP structure. In FIG. 19B, the InP-InGaAs-InP layers with microstructured holes 1922 effectively reduce the capacitance of the photodiode 1920 to allow a larger area photodiode to be fabricated with the same bandwidth and QE. FIG. 19C is a top view showing PD 1920. The microstructured holes 1922 can be 100-1000 nm in diameter with depth of 0.1 to 3 microns. Also visible in FIG. 19C is contact ring 1930 and bond pad 1932. According to some embodiments, a complementary microstructured pillars can also be fabricated. According to some embodiments, the sidewalls of InP and InGaAs can be passivated with SiOx, SiNx (silicon oxide and silicon nitride via ALD or PECVD), polyimide or spin-on-glass that can be spun on using standard processing methods. The absorption coefficient of the bulk material can be enhanced by up to two orders of magnitude or more.

[00164] According to some embodiments, III-V material such as InP, InGaAs, InGaAsP, InAs, InSb, GaSb, InGaSb on Si, Ge on Si, is epitaxially grown in a sub micrometer selective area growth (SAG) or vapor liquid solid (VLS) (See, e.g. Sarkar et al, Heteroepitaxial growth dynamics of InP nanowires on silicon, Journal of Nanophotonics, Vol. 2, 021775 (12 February 2008); Roest, et al, Position-

controlled epitaxial III–V nanowires on silicon, Nanotechnology 17 (2006) S271–S275) heteroepitaxy using metal organic vapor epitaxy with or without catalyst which can consists of Au, Cu, Al, Ti, W, Fe, Cr to name a few. Also for vertical oriented microwires grown on silicon, wafers with surface orientation (111) are selected. It is not necessary that the microwires be normal to the surface, it can be off normal and even have a mixture of orientations.

[00165] In VLS growth, the silicon wafer that has the layer structure for APD or PD just prior to heteroepitaxial growth is photolithographically (or e-beam or nanoimprint lithographically) patterned with aperture ranging from 10-5000 nm, and spaced between 10-3000 nm. An Au deposition (e-beam, or thermal evaporation) follows with thickness of 0.1-10 nm, followed by a lift-off, VLS epitaxial growth in a MOCVD reactor.

[00166] For SAG growth (See, e.g. Chu et al, Wurtzite InP nanowire arrays grown by selective area MOCVD, Phys. Status Solidi C 7, No. 10, 2494 – 2497 (2010)), a 50 nm SiN_x is PECVD (or sputtered or ALD) deposited on a (111) oriented Si wafer with the necessary APD or PD epitaxial layers grown on it ready for heteroepitaxial growth. Using lithography (photo, e-beam or nanoimprint) apertures are defined with dimensions ranging from 10-5000 nm and spaced between 10-10000 nm followed by dry etching (RIE) to open a via to the silicon surface. The wafer is then ready for SAG of Ge, III-V microwires in a MOCVD reactor.

[00167] Detailed processes such as surface treatments, surface preparations, annealing, plasma etching, are not described for simplicity. These processes can be found in the literature.

[00168] FIGs. 19D and 19E are cross sections showing aspects of fabricating an APD device having a III-V absorbing layer grown on a P-I-N silicon multiplication layer, according to some embodiments. In FIG. 19D, a Si APD structure 1940 is etched as shown for v epitaxial growth of the III-V material. In FIG. 19E a III-V absorbing layer is grown on P-I-N silicon multiplication layer for APD device 1960. As in the III-V on Si for a PD device, the III-V nanowires or microwires can be grown on Si using VLS process with or without catalyst. Since the footprint of the nano/microwires on Si is of the order of a micron, defects due to stress from lattice mismatch are not a significant issue and high quality III-V nano/microwires can be

grown on Si. According to some embodiments, SAG is used for fabricating III-V microstructures on Si electronic gain layers.

[00169] From FIGs. 19D and 19E it can be seen that the InGaAs on Si APD 1960 starts with a Si APD structure 1940 where microstructures of holes or pillars are etched to the charge layer 1944 or just before the charge layer 1944. According to some embodiments, the microstructure holes and/or pillars can be etched into the multiplication layer 1942. Then using a process, for example SAG, with or without silicon oxide on the Si microstructure's sidewalls, I-InGaAs is grown, ending with P-InGaAs at the surface. Surface growth can use a process such as epitaxial lateral overgrowth (ELOG) to form a continuous P-InGaAs film of high quality. P ohmic alloy and bond metal 1966 are formed and annealed on the P-InGaAs. The back side processing consist of thinning the Si wafer using for example a BOX layer for selective etch stop and removing the BOX layer. Anti reflection can be coated on the backside silicon to reduce reflection. N ohmic 1968 is fabricated on the N Si layer. The optical signal is illuminated from the bottom. A reverse bias of -5 to -50 volts is applied to the cathode and anode. As mentioned earlier, the small footprint of the InGaAs on Si microstructure of the order of 10 square microns allows for high quality InGaAs material to be grown where lattice mismatch causing crystal defects are not significant.

[00170] According to some embodiments, the integration of Ge, III-V with Si PDs, PVs (See, FIG. 25C, *infra*.) and APDs allow the absorption spectrum of Ge and III-V material on a mature Si electronic platform. It allows integration of III-V with Si CMOS ICs for example for photodetector, optical light source such as light emitting diodes (LED) and laser diodes (LD) and III-V electronics such as transistors.

[00171] Multiple absorbing material and voids as microstructures. According to some embodiments, the microstructured pilllars and/or holes are regrown with Ge such that both Si and Ge are microstructured to enhance the bulk absorption coefficient. According to some embodiments, voids can also be buried or embedded to generate a buried/embedded microstructure such that the surface is more planar. The microstructured voids can also enhance the absorption coefficient, by being patterned so as to enhance reflection and also to reduce the effective refractive index of a material (e.g. Si), reduce the weight of the device,

and increase mechanical flexibility. The microstructured voids can be random, pseudo-random or patterned typically with dimension and spacing that are approximately the order of a wavelength or subwavelength. According to some embodiments, instead of combining Ge with Si, others combinations can be used for example III-V with Si or other semiconductor material, polymers, or other non semiconductor absorbers, which can significantly broaden the absorption spectrum over that of a single absorber.

[00172] The enhancement using nanowires (See, e.g. Garnett et al, Light trapping in silicon nanowire solar cells, Nano Letters, 2010, 10, 1082-1087; Kelzenberg et al, Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications, Nature Materials, vol. 9, March 2010, 239-244) and nanoholes (See, e.g. Lin et al, Optical absorption enhancement in silicon nanowire and nanohole arrays for photovoltaic applications, Proceeding of SPIE, Vol. 7772, 77721G-1, 2010) have been reported by various groups. The known use of nanowire for light trapping are for photovoltaic applications where the photogenerated carriers diffuse to the anode or cathode of a P-N junction with zero external bias, operating at DC (direct current). According to many of the embodiments described herein, the photogenerated carriers are swept out with an external reverse bias in the absorbing “i” region of a P-I-N diode (PD) or P-I-P-I-N diode (APD) for high modulation bandwidth (e.g. greater than or equal to 10 Gb/s bandwidth) and high quantum efficiency and for APD for high current gain (e.g. gain greater than 3 dB). In addition, according to some embodiments, multiple absorbing materials can be used to broaden the absorption spectrum. The multiple absorbing materials are connected in parallel as current sources whereas in known technology the absorbing materials are connected in series. In addition, the use of voids as microstructures to enhance the absorption of the material according to many embodiments described herein allows the surface to be more planar and simplify processing since fillers may be avoided. Also, the more planar surface allows the epitaxial growth of semiconductor Bragg reflectors to enhance reflection for double or multiple pass absorption in the I absorption layer of the PD/APD. According to some embodiments, Dielectric Bragg reflectors can also be used in a more planar surface since the surface can be highly N or P doped and the ohmic contact can be made on the periphery such as a ring ohmic contact and the

dielectric Bragg reflectors deposited on the photosensitive area such as shown in FIG. 29, *infra*. Chemical mechanical polishing (CMP) can be used to smooth the surface of the epitaxial layer with buried voids.

[00173] Further aspects of fabricating devices having microstructured Ge that is buried or embedded in Si microstructure will now be described. FIG. 20 shows bulk layers without a final P-Si layer for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments. The final P-Si layer, according to some embodiment will be the last layer grown in the epitaxial structure where the first layer grown is the layer adjacent to the substrate, followed by the second layer that is adjacent to the first layer, and so forth to the last layer grown. Shown in FIG. 20 is P-I-N PD structure 2000 and a P-I-P-I-N APD structure 2020 both without the final P-Si layer. In many of the embodiments described herein, N can refer to N (mid N type doping of 5. 10^{16} cm^{-3} to 8. 10^{17} cm^{-3}, low N doping less than 1. 10^{17} cm^{-3}, and high N doping greater than 5. 10^{17} cm^{-3}, with the same for P doping. I (or i) doping is commonly defined as intrinsic, or not intentionally doped or low doping back ground doping of less than 5. 10^{16} cm^{-3}. The "I" region is configured such that the field of a P-I-N junction is developed across the "I" region usually with an external reverse bias. In PD and APD applications, the absorbing material is in the "I" region so that the photogenerated carriers can be quickly sweep to anode (P) and cathode (N) layers. For APDs, the carriers (electrons in most cases shown here, since this gives the lowest noise APD) are swept to the second "I" region for multiplication (current gain) before transiting to the cathode layer). In the Figures herein, P-I-N, P-I-P-I-N structures are shown and the top P layer(s) that are in contact to external circuits are referred to as the anode and the N layer(s) that are in contact to external circuits are referred tp as the cathode; the layers can be interchanged from P to N and N to P with P or low dope substrates to also fabricate PD's and APD's.

[00174] FIG. 21 is a cross section showing etching of microstructured pillars and/or holes for devices having microstructured Ge buried or embedded in an Si microstructure, according to some embodiments. The microstructure pillars 2104 and/or holes 2102 are etched into the I-Si layer, partially or entirely or to/into the N (PD structure) or P (APD structure) Si layer. The etching process can be one of the following: wet chemical etching, dry etching using reactive ion etching (RIE), a

deep reactive ion etching (DRIE), ion milling, and/or focused ion beam milling. The etching can be isotropic or anisotropic or a combination of isotropic and anisotropic. As shown in FIGs. 22 and 23, *infra*, Ge is then regrown in the etched region (i.e. the area around the pillars and on the sidewalls of the pillars in the case of pillars, or area in the holes, sidewalls of the holes in the case of holes) isotropically, anisotropically, or by selective area growth (SAG) where a dielectric layer such as SiOx, SiNx, cover area where regrowth of Ge is not desired which in some embodiments can include the sidewalls. During etching if a dielectric mask material such as SiOx, SiNx, SiCx is used and left in place during epitaxial growth, the epitaxy layers may not grow on the dielectric mask in a crystalline film and may be amorphous in nature or may not grow on the dielectric layer other than some dendrites. Note that the isotropic or anisotropic growth rate often depends on the crystal plane it is growing on and any etched structures may expose multiple crystal planes resulting in different growth rates at those planes that can lead to anisotropic growth in the etched regions with 3D microstructures.

[00175] Growth of Ge on Si is well documented in the literature where a thin buffer Ge layer is first epitaxially grown at a lower temperature followed by a higher temperature Ge epitaxial growth using chemical vapor deposition (CVD), molecular beam epitaxy (MBE), atomc layer deposition (ALD), low pressure -CVD, and or a combination of growth techniques, for example the thin Ge buffer layer can be grown by MBE and the high quality thicker Ge film grown by CVD. The thin Ge buffer layer is to allow lattice mismatch stress to be accommodated between Si and Ge, (see, e.g. Feng et al, High-speed Ge photodetector monolithically integrated with large cross-section silicon-on-insulator waveguide, APPLIED PHYSICS LETTERS 95, 261105 ,2009).

[00176] The Ge regrowth may have voids or non-planarities and, where useful, the surface can be planarized using polishing such as chemical mechanical polishing (CMP) or etching. FIG. 22 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after the Ge "I" layer is grown in the etched region and planarized, according to some embodiments. Note that according to some embodiments, planarization is not needed and is omitted. After the Ge "I" layer 2202 is grown and planarized, a P^+ Ge capping layer 2204 is grown to complete the P-I-N structure of a PD or P-I-P-I-

N structure of an APD. Optical signal or photons with wavelengths ranging from 400 to 1800 nm can illuminate the PD/APD 2220 from the anode (top) side (P^+ side) 2202 and optical signal or photons with wavelength ranges 950-1800 from the substrate side (bottom) since Si is mostly non-absorbing at these wavelengths. According to some embodiments, it is advantageous to configure the device 2220 for illumination from the substrate side since this will allow a double bounce of the optical signal or photons within the absorbing Ge microstructures embedded in Si. Shown in these figures are only the basic epitaxial layer structures. Structures and layers not shown for simplicity include: anti-reflection coatings, passivations, ohmic metals, bond metallization, any metal interconnect to CMOS, via's for electrical connectivity, arrays of PD/APD for multichannel optical interconnects, to name a few. Optical signal/photons can illuminate either normal to the surface or at any angle off normal, including rotation angles for optimal PD/APD performances; optimizing QE and bandwidth of the PD/APD.

[00177] FIG. 23 is a cross section showing a device having microstructured Ge buried or embedded in an Si microstructure, after I-Ge regrowth and planarization, and a cap layer of P-Si, according to some embodiments. In the case of FIG. 23, the buried Ge microstructures 2302 are capped with a P^+ Si layer 2304. The Si P^+ cap layer (anode) 2304 has low optical loss at optical wavelengths of 950-1800 nm and therefore generates minimal photocarriers that are not in the high field "I" region of the PD/APD 2320 and contribute minimal diffusion photocurrent which can lead to a degradation of the frequency response of the PD/APD 2320 and the QE of the PD/APD.

[00178] Some dimension doping ranges for the buried or embedded Ge and capping layers shown in FIGs. 20-23 will now be provided in greater detail, according to some embodiments. The dimension of the microstructured Ge (e.g. 2202 and/or 2302) can range in depth from 0.1 to 5 micrometers, have a lateral dimension range from 10-5000 nm, and a spacing between adjacent microstructure structures (the structures can be identical or non-identical) in contact (overlapping) to 5000 nm. The "I" doping for both Ge (2202 and/or 2302) and Si (2104) is less than or equal to 5. $10^{16}/cm^3$. "I" is often called intrinsic or not intentionally doped and can have either a p or n background doping, the doping level is low enough that a reverse bias voltage of -2 to -45 volts can fully deplete the "I" region of

mobile holes or electrons (carriers). The capping layer, Si (2304) or Ge(2204) thickness can range from 0.1 to 5 μm with doping level greater than or equal to 6. $10^{17}/cm^3$. These parameters can be adjusted to other values, but the goals are to increase or optimize the QE and bandwidth of the PD/APD for a given application. Series resistance, photogenerated diffusion current, ohmic contacts, capacitance, transit time, depletion of the "I" absorption region all contribute to the performance of the PD/APD. In addition for double/multiple bounce within the "I" region for optical signal illuminating from the bottom substrate side, a reflective metal or dielectric stack such as a Bragg refelctor/mirror consisting of alternating dielectric layers of different refractive indices or HCG can be used to reflect the optical signal back into the microstructured absorbing region at the top anode side. With the Si cap layer as in FIG. 23, the optical signal can illuminate the Si P^+ cap layer (anode) 2304 and, since Si has minimal losses at 1100-1800 nm (below bandgap radiation), it can also have double bounce of the optical signal within the microstructured buried/embedded Ge 2302 by providing a reflector such as a Bragg reflector epitaxially grown at the Si N^+ layer or at the Si substrate to reflect the light back into the absorption region.

[00179] According to some embodiments, all the discussions of microstructured layers herein, light can additionally impinge from top and bottom surfaces, as well as on the sides of the microstructures, either directly or from scattering, near field effects, interferences, or resonance, which can vastly improve the QE of the microstructured photosensors since photogenerated carriers are generated directly in the high field absorbing "I" ("I") layer(s).

[00180] According to some embodiments, dopant choices for Si and Ge (group 4 elements) include the following: (1) for donors (n-type) from group 5 elements - antimony, phosphorus, and arsenic; and (2) for acceptors (p-type) from group 3 elements - boron, aluminum, and gallium.

[00181] It is also noted that in the structure shown in FIG. 23, the I-Ge microstructures 2302 buried in Si 2104 are completely surrounded by Si which has a lower refractive index than Ge. At 1000-2000 nm wavelength range, the refractive index of Si is approximately 3.49 and for Ge is 4.1. The index ratio of Ge/Si is 1.17 so according to Chang-Hasnain reference, HCG effects will exist. The resonance and field concentration in the absorbing Ge microstructures can further enhance

the absorption coefficient from that of the bulk absorption coefficient value anywhere from greater than 1X to several orders of magnitude. The index difference also causes light to be confined and concentrated in the high index material, in this example, Ge; further improving QE.

[00182] The silicon (Si) microstructure can detect photons with wavelength ranging from 300-1100 nm and the germanium (Ge) microstructure can detect photons with wavelengths ranging from 300-1800 nm. According to some embodiments, for high bandwidth and high QE, the shorter wavelengths, 300-600 nm, may generate photocarriers outside the "I" region resulting in a diffusion current that can result in non-optimal bandwidth and or QE. Where bandwidth is not an issue, the degradations may not be very significant.

[00183] FIGs. 24A and 24B are cross sections showing aspects of a microstructured APD with buried/embedded I-Ge absorbing microstructures in I-Si microstructures, according to some embodiments. FIG. 24A shows the bulk layers 2400. In FIG. 24B, the etched pillars 2424 and/or holes 2422 are filled with I-Ge (intrinsic-Ge, non-intentionally doped or undoped or low doped Ge) and finished with a capping layer 2426 of P^+ Ge or Si to complete the anode of the APD 2420. The microstructured Ge 2422 is buried/embedded in Si 2412. Optical signal of wavelength 950-1800 nm (or photons from 300-1800nm where the shorter wavelengths, 300-900 nm, may not have as high a bandwidth) can illuminate the APD 2420 from either top or bottom at various angles to the normal and/or normal to the surface. According to some embodiments, the starting layers prior to the I-Ge regrowth into the etched regions can also include the P^+ Si layer 2426, such as shown in FIG. 7 with layer 726, *supra*. In the case shown in FIG. 24B, the starting layer was removed to minimize P dopant diffusion during I-Ge regrowth. The buried or embedded Ge microstructure in Si microstructure allows the APD (or PD) 2420 to operate in two regimes. A first regime is at wavelengths where Si is low loss and Ge is absorbing or high loss (950-1800 nm). In this Si low loss regime, the Ge microstructures 2422 with a Si P^+ anode cap layer 2426 is completely buried in Si which has a lower refractive index than Ge. The Ge microstructure arrays can have HCG low Q with Q ranging from 1 to 3000 approximately (or other resonant, scattering, near field, linear and non-linear optical effects) or high enhancement of the absorption coefficient. A second regime is where both Si and

Ge are absorbing, 300-945 nm, and both Si microstructures 2424 and Ge microstructures 2422 work in parallel (parallel current generators) absorbing the photons with enhancement of the absorption coefficients of both Si and Ge. This is particularly advantageous for examples in photovoltaic applications.

[00184] FIGS. 25A - 25C are cross sections showing aspects of a photodiode having buried/embedded Ge microstructures in a Si microstuctured pillar and/or hole array, according to some embodiments. Starting with a Si PD epitaxial layer structure 2500 with or without the P layer 2526, microstructures of holes 2522 and/or pillars 2524 are etched into the Si P layer 2526 and I layer 2512 and can extend into the N layer 2510. Regrowth of Ge 2522 (or III-V material such as InGaAs, InAs, InSb, GaN, InGaN to name a few) using a process such as SAG with our without silicon oxide on the sidewalls of the Si microstructure 2524 or using a process such as VLS with or without catalysts, the I-Ge layer 2522 is grown followed by P Ge 2526 (or a P-Si layer which may be more suitable for top illuminated devices) at the surface where a process such as ELOG can be used to form a contiunous P-Ge film. P ohmic alloy, annealed, followed by bond metallization completes the contact 2528 for the anode. The back side processing as discussed earlier is deposited on the silicon surface to reduce reflection. See, e.g. FIGs. 19A-19C, *supra*, where the silicon is thinned and etched to the BOX layer selectively. The BOX layer is etched selectively and an anti reflection N ohmic alloy is formed on the N-Si layer, annealed and followed by bond metallization, which completes the cathode contact. Reverse bias of -2 to - 10 volts is applied between the anode and cathode for high bandwidth PD applications. In PV applications, 0 bias is applied.

[00185] According to some embodiments, the dimensions and doping are similar to the Si microstructured PD shown in FIGs. 5A-5B, *supra*, with the I-Ge doping level less than 5. 10^{16} cm^{-3}, and dimensions ranging in thickness of 0.1 to 5 micrometers, and lateral dimension of the microstructure ranging from 10 to 5000 nm with adjacent structures that can touch/overlap to 5000 nm separation. Optical signal/photons can either illuminate from the anode top side or cathode bottom side with wavelength range of 300-1800 nm and normal to the surface or at an angle to normal which can also include rotation. For bottom side illumination, the Si is thinned down to a few micrometers thickness for illumination at wavelength

ranges of 300-900 nm. Only the basic layers are shown for simplicity. For example, the following structures are not shown: isolation mesa or diffusion or ion implantation, passivation, anti-reflection, ohmic metal, guard rings (e.g. for an APD). Both Si microstructures and Ge microstructures can detect the optical signal/photons in parallel for wavelengths where both are absorbing, 300-1100 nm, and only the Ge microstructure at wavelength ranges 900-1800 nm. The cap layer 2526 and 2546 in FIGs. 25B and 25C respectively can be either P^+ Si or P^+ Ge. For broad modulation bandwidth (sometimes just referred to as bandwidth) of greater than 10 Gb/s (gigabits per second), P^+ Si cap layer is preferred for wavelengths ranges from 950 to 1800 nm, since at these wavelengths Si has low optical losses (also referred to low loss). According to some embodiments, the structure shown in FIGs. 25B and 25C can also be use for photovoltaic applications where no external bias is purposely applied in the reverse direction.

[00186] According to some embodiments, for all the structures shown, the P and N can be interchanged to form for example N-I-P structures for the PD and PV (photovoltaic) and N-I-N-I-P structures for the APD.

[00187] The regrowth of Ge microstructures in Si also have applications in photovoltaic devices where the device is operated without external reverse bias. The P-I-N PD structure for example with Ge microstructures embedded or buried in Si microstructures effectively have two bandgaps, Si bandgap and Ge bandgap that is exposed to the solar radiation. The combination of two bandgaps widen the absorption spectrum of the photovoltaic device and therefore can collect a broader spectrum of the solar energy. The two bandgaps can have a higher QE and or short circuit current over that of single bandgap photovoltaic devices or multiple devices connected in series. The microstructures also have enhanced absorption that can further improve the QE and or short circuit current of the photovoltaic device. The solar spectrum at AM 0 and AM 1.0, with a photovoltaic device with a spectrum width of 300-1800 nm, at least approximately 90% of the solar spectrum is captured. In addition, in the PV device with Ge and Si microstructures are adjacent laterally to each other (i.e. in parallel) rather than being vertically adjacent (i.e. in series) as in prior art PVs. This allows the Si and Ge to be exposed to solar photons equally and are parallel current generators that are additive; $I_{Si} + I_{Ge} = I_{total}$

where I_S is the photocurrent generated by the Si microstructures and I_{Ge} is the photocurrent generated by the Ge microstructure and I_{total} is the total photocurrent.

[00188] Although according to some embodiments the use of Si and Ge are described, according to some other embodiments, other materials are used. According to some embodiments, Si is used with an InP microstructure embedded or buried. According to some embodiments, more than two materials are used such as Si, Ge, InGaAs, InP, GaAS, GaN, InGaN, InSb, to name a few. The microstructures, in addition to pillars and holes, can be embedded and or buried to use the effects of HCG to enhance the absorption coefficient over that of bulk absorption coefficient to further improve QE and minimize the use of material in order to reduce cost of manufacturing.

[00189] FIG. 25C is a cross section showing grown Ge, InP, InGaAs to name a few, within silicon microstructures. SAG can be used where the sidewalls of the microstructures are oxidized or coated with a conformal dielectric and where the oxide/dielectric is removed at the bottom of the microstructure surface where it is approximately parallel to the silicon substrate where it can provide crystalline information for the growth of Ge, InP, InGaAs microstructures. The area where the Ge, InP, InGaAs will epitaxially grow with or without catalysts using various growth methods such as VLS, MOCVD, CVD to name a few, is approximately 100 square microns or less; more typically around 0.3-3 square microns. Because of the small area, crystalline defects due to lattice mismatch are not significant. The sidewalls with the silicon dioxide that can be thermally grown or deposited using ALD, provide an electrical insulation between the Si and the Ge, InP, InGaAs SAG grown layer. It should be noted that SAG growth can continue until the Ge or InP or InGaAs (to name a few) can merge above the silicon microstructure and with lateral over growth (LOG) epitaxial process, the microstructures of Ge or InP or InGaAs can form a continuous epitaxial thin film layer that can be doped P type for the anode layer.

[00190] FIGs. 25D and 25E are cross sections showing aspects of a forward biased device such as a vertical cavity surface emitting laser (VCSEL), according to some embodiments. VCSEL 2562 can also be fabricated using similar processing as described *supra* for the PDs, PVs and/or APDs. Starting with a Si PIN structure 2562, Si microstructure hole(s) 2564 are etched through I-Si layer

2566 to the N-Si layer 2568. According to some embodiments, the etching of hole 2564 can extend into the N-Si layer 2568. An SAG process is followed with or without silicon oxide on the Si microstructure sidewalls (oxide 2570 is shown). First, a GaAs/AlGaAs distributed Bragg reflector 2572 (DBR) all N type is grown, follow by N-GaAs 2574, The active layer 2576 is undoped InGaAs/GaAs multiple quantum well (MQW) of 1-5 wells, followed by P-GaAs 2578 to the surface and using ELOG which can form a continuous film at the surface of the I-Si 2566. Dielectric DBR 2582 on the P-GaAs 2580 completes the optical cavity. P ohmic alloy with anneal and bond metal 2584 on P-GaAs 2580 completes the anode contact and N ohmic alloy with anneal and bond metal 2582 on N-Si 2568 completes the cathode contact. Forward bias of 1 to 20 volts to the anode and cathode will result 1200-1300 nm light to be emitted from the VCSEL 2560.

[00191] The design and growth of VCSELs at 1200-1300 nm and other wavelengths are known. See, e.g. "High-performance 1200-nm InGaAs and 1300-nm InGaAsN quantum-well lasers by metalorganic chemical vapor deposition", Tansu et el; Selected Topics in Quantum Electronics, IEEE Journal of (Volume: 9, Issue: 5), 2003.

[00192] According to some embodiments, longer wavelength are selected when embedding InGaAs, InGaAsN and other III-V material, because at wavelengths greater than 1000 nm silicon is mostly transparent and does not introduce excess additional optical losses. Accordingly, Si is a good heat sink for the VCSEL 2560. According to some embodiments, the GaAs/AlGaAs DBR 2572 is replaced with a silicon/air or a dielectric DBR on the bottom by thinning the Si wafer and etching to the BOX layer, removing the BOX layer and depositing a dielectric DBR. Design of DBR, dielectric and semiconductors are well known. The silicon/air DBR will require further processing, using sacrificial layers such as Ge that can later be selectively etched away via etch trenches.

[00193] According to some embodiments, an LED is fabricated by applying minor variations, including removing the DBRs and adding multiple Si microstructures. The LED can use MQW or just a simple heterojunction of P-GaAs/ I-InGaAs/N-GaAs for example. Other semiconductors can also be used such as InGaAsN, InGaAsP, GaAsN, to name a few. The substrate can be another material such as sapphire, SOI, insulator on Si (IOS), ceramic, glass, quartz, GaN,

crystalline or non-crystalline. Addtionally, other material for blue/UV LEDs such as GaN, AlGaN, GaInN, AlN, can be grown using epitaxial reactors and methods of fabrication described above.

[00194] According to some embodiments, voids are formed, that are buried or embedded in Si or Ge on Si or Ge. As used herein "buried" refers to cases when the void is beneath the surface, and "embedded" refers to cases when the void can intersect or be slightly above the surface. As described *supra*, during regrowth of Ge on a microstructured Si with pillar and/or hole arrays, voids can develop due to the fact that growth rate during epitaxial growth often depends on the crystal orientation of the surface. Since etching microstructured pillars and/or holes in Si can expose different surface orientation of the side walls, asymmetric growth rate of Ge on these different Si surface orientation can result in void formation. According to some embodiments, the void formation is exploited to generate a buried and/or embedded microstructured void arrays that can behave as HCG and or light trapping structures that concentrate the optical field and/or resonance through interference of the optical field (amplitude and phase), scattering, near field, linear and non-linear optical effects to enhance the bulk film absorption coefficient by one to several orders of magnitude. In addition, the voids can be used to reduce the effective refractive index of a material (e.g. Si with voids) since the optical field sees an average or effective refractive index. At dimensions on the order of a wavelength or less, the refractive index of voids and Si, for example, can be approximated with an effective refractive index which is the average of the volume occupied by Si and the volume occupied by the void. For example, if Si occupies 1/2 the volume and voids occupy 1/2 volume, the Si index is 3.49 and the void is 1.0 (for air), then the average effective index is approximately 2.25.

[00195] The voids also reduce capacitance of the device if the voids are generated in the "I" region, as discussed *supra*; where the space between microstructured pillars or the microstructured holes can reduce the capacitance of the P-I-N PD diode or the P-I-P-I-N APD diode. The voids according to some embodiments are either buried (buried holes) or embedded (space between pillars) and the total capacitance is approximately the capacitance of the total area occupied by the voids plus the capacitance of the total area occupied by the semiconductor. In the case where the voids do not occupy the full thickness of the

"I" layer (i.e. only occupy part of the thickness), then the effective dielectric constant can be estimated by taking into account a volume that contains both the void and the semiconductor extending through the thickness of the "I" layer, the volume of the void and the volume of the semiconductor in a given volume; for example if the voids occupy 1/2 of a given volume of the thickness of the "I" layer and the semiconductor material occupies 1/2, and if the semiconductor material is Si with dielectric constant of 11.9, then the average effective dielectric constant is approximately 6.5, where the void is assumed to be air with dielectric constant of 1 for that given volume. The total area occupied by this effective dielectric constant, consisting of both voids and semiconductor material, is used in the capacitance calculation plus the area occupied only by semiconductor in the "I" region to give the total capacitance of the P-I-N or P-I-P-I-N diode. Reduction of capacitance leads to a reduction in RC time constant for the diode which improves the bandwidth of the PD and APD.

[00196] Although buried voids in semiconductor material are known, such voids are conventionally regarded as detrimental and as such are to be avoided. According to some embodiments, such voids are intentionally created and form useful features in the semiconductor material.

[00197] FIG. 26 is a cross section showing starting epitaxial layers in which mictrostructured voids are fabricated, according to some embodiments. To generate voids in PD, PV and APD structures start with a structure 2600. The starting material can be a Si PD or APD structure with or without the Si P^+ anode layer. Details of the layers are not shown for simplicity.

[00198] FIG. 27 is a cross section showing microstructured holes/pillars etched into the I-Si layer, according to some embodiments. The microsctured holes 2722 (or space around pillars) are etched into the Si "I" layer and can extend pass the "I" layer or can be partially into the "I" layer. Wet and/or dry etching can be used or a combination of wet chemical and dry etching (RIE, DRIE for example) where the wet etching can be used to remove damage due to dry etching or wet etching in combination with dry etching and oxidation to form a certain shape or surface smoothness. As shown in FIG. 27, the etch can be isotropic or anisotropic, the sidewall can have negative or positive slope (slope defined with respect to the plane of the substrate). For anisotropic etching both negative and positive slope

can exist at the same time for an etched feature such as a pillar or hole. Anisotropic epitaxial growth can result in void formation, with the shape of the void being determined by many factors including: side wall slope, crystal orientations of the side wall, growth conditions, pressure, temperature, flow rate, growth technique (CVD, MBE, ALD or a combination of growth methods), surface preparation, and surface oxidation. According to some embodiments, surface oxide, partial oxide or other dielectric 2726 can be intentionally deposited on the side walls, which can also influence the regrowth of Si or Ge (or any other semiconductor such as InP, GaAs, InGaAs, GaN, InGaN, to name a few) and can be used to form voids.

[00199] FIG. 28 is a cross section showing microstructured voids buried or embedded in Si with a Si capping P^+ anode layer 2826, according to some embodiments. The buried voids 2800 can be uniformly spaced, or with chirped spacing, or any complex patterns with a combination of periodic and aperiodic spacing or it can be random or pseudo-random. The buried voids 2800 can have a length ranging approximately from 0.1 to 10 micrometers and lateral dimension ranging from 10-5000 nm. The voids can also be overlapping one another. Although FIG. 28 shows buried voids in Si, according to some embodiments buried voids can be formed in Ge. For example, in a Ge epitaxial layer on Si, or any other semiconductors, such as InP, GaAs, InGaAs, GaN, InGaN, InGaAsP, and other semiconductors in the III-V material family. The voids can be non-uniform is size and shape within the void and adjacent voids. The voids may also have non-uniform spacing and/or orientation. However, with proper process control uniformity in size and shape, patterning, random and pseudo-random placements of the voids can be attained. For simplicity the voids are shown to be uniform.

[00200] FIG. 29 is a cross section showing Bragg reflectors formed on the P-Si surface to provide a highly reflective mirror, according to some embodiments. With a more planar surface, high reflectivity Bragg reflectors 2900 may be deposited or grown using dielectrics or semiconductors on the P silicon layer 2826 surface. The ohmic contact and the bond metallization 2902 can be on the peripheral in a ring configuration as shown in FIG. 29. Optical signal illuminating from the bottom will have a double/multiple pass through the absorbing I region thereby improving QE and the bandwidth of the PD/APD. In PV where bandwidth is not an issue, then the QE will be improved. According to some embodiments,

Bragg reflectors 2900 can be configured for wavelength selectivity so as to reflect the optical signal back into the absorbing I region.

[00201] According to some embodiments, voids are not only in the I region but are also formed in the P and/or N region of a PIN PD or PV, in the P charge region, in the I multiplication region and/or the P anode and N cathode region of an APD. According to some embodiments, voids can also be formed in the substrate. The density, shape and material (voids can be filled with different material from vacuum, gas, helium to dielectrics with or without doping with rare earth elements for optical gain for example, carbon/graphene/diamond,copper, ceramics for thermal conductivity for example) of the voids in each layer can be different or the same, or different/same within the same layer.

[00202] According to some embodiments, voids are also used to make the material more mechanically flexible and bend and or conform to different surface contours. For example, in PV applications where large sheets of the device are fabricated, the sheets can conform to contours in for example the roof, or the sheets of semiconductor PV can be rolled for compactness in storage prior to deployment. According to some embodiments, voids sized between 0.01 microns and 1000 microns are introduced into semiconductor and/or glass material for use with photo voltaics for purposes of increasing flexibility and/or resistance to physical damage and/or damage propagation.

[00203] High-density voids in semiconductors are also resistant to crack propagation since the crack will terminate at a boundary, in this case the boundary of the void. This is advantageous for large devices such as solar cells where if an object such as hail or stone strikes the solar cell, only the point of contact will be damaged and perhaps a small adjacent area (5-50% of the diameter of impact for example) where the damages are localized to area of impact and cracks will not propagate across the entire cell. A device may survive such small damage events with minimal degraded performance without taking the entire solar panel down.

[00204] According to some embodiments, the voids are also formed in other materials also such as glass, ceramics, polymers, metal, plastics, to name a few, to avoid crack propagation in case of foreign object impacts since cracks will terminate at a boundary, in this case the boundary at the void.

[00205] FIG. 30 shows an example of a PIN PD/PV structure 3000 with microstructured voids to enhance absorption, reduce bulk refractive index, reduce capacitance and increase mechanical flexibility of large sheets of PV on semiconductor material, according to some embodiments. The Si substrate is removed leaving only the BOX/SOI layers together with the PIN epitaxially grown layers. Ohmic contacts, bond metallizations, antireflection coatings, passivations, are not shown for simplicity. In addition to PV, the techniques are also applicable to PD, APD, light emitters such as light emitting diodes and diode lasers, and to electronic integrated circuits such as CMOS and ASIC (application specific integrated circuits) where voids can not only make the material more flexible and lighter but also as mentioned earlier more resistant to cracking. The voids, according to some embodiments can be filled with a gel that can repair impact damage and seal exposed cracked edges to prevent further deterioration due to moisture for example to the semiconducting surfaces. The gel can be spin on glass for example. According to some embodiments, the voids can be filled with material to enhance thermal conductivity for example, reduction of optical or microwave losses by removing the silicon and replacing with material that is not lossy such as Ar, He, Xe, N_2, Ne gas, or vacuum for example. The voids can have different sizes and shapes and densities and can be random, pseudo random, aperiodic, periodic, chirped, single or multiple patterns. The voids can also be in a single layer or in multiple layers of the device. Fig. 30, for example, shows the voids in P-Si layer 3002, I-Si layer 3004, and N-Si layers 3006 and 3008. According to some embodiments the index of refraction near the uppermost surface can be altered to more effectively index "match" with surrounding air so as to reduce reflections of incident light. For example, in PV applications near surface voids can be used to index match such that less incident sunlight is reflected from the PV surface. According to some embodiments, the index of refraction at lower surfaces can be altered so as to increase internal reflections that may, for examples, increase the number of passes light makes through an absorbing region.

[00206] According to some embodiments, random voids can also be generated by dry etching/electrochemical etching the surface of the semiconductor without any mask. Generating semiconductor nanowires followed by epitaxial regowth on these random nanowires will result in buried voids. As discussed in Frajtag et al,

Growing thin films that contain embedded voids, 23 June 2011, SPIE Newsroom; DOI: 10.1117/2.1201105.003750, this method can be used in GaN light emitting diodes to minimize defect formation due to lattice mismatch of the GaN epitaxial layer with the substrate which can be sapphire, Si, SOI, IOS to name a few. The random formation of semiconductor nanowires by dry etching of the surface of the semiconductor (which can be Si, Ge, III-V material family such as InP, GaAs, InGaAs, InGaAsP, GaN, InGaN, InSb, to name a few) without any mask and subsequently regrowing on the nanowires epitaxially using CVD for example, to form random buried voids can also be used to reduce the effective refractive index of the semiconductor and reduce the effective capacitance of the P-I-N, P-I-P-I-N diodes if the voids are formed in the "I" absorption layer and/or P, N layers, and/or charge, multiplication layers of the PD, APD, in any combination to optimize the performance of the device in bandwidth, QE, and energy consumption.

[00207] Fig. 31 is a cross section showing regrown I-Ge with a buried/embedded voids, according to some embodiments. The regrowth of Ge 3104 epitaxially on Si microstructured pillars and/or holes results in voids 3102 in the Ge layer that can be intrinsic or non-intentionally doped or low doped using the method shown in FIGs. 27-28, *supra*. In addition, selective masking with dielectric such as SiOx, SiNx for example can be used to generate nanowires only in the selected areas such as the Ge regrowth, for example, and with additional regrowth of Ge, random voids can be buried only in the selected Ge areas. The random voids can be combined with patterned voids to optimize a device performance in terms of bandwidths, quantum efficiencies and power consumption. The microstructures shown in FIG. 31 combine the Ge microstructure and void microstructure to enhance to bulk absorption coefficient and reduce the effective capacitance of the diode.

[00208] Fig. 32 is a cross section showing a device having buried microstructured voids in I-Si with regrown I-Ge and capped by an epitaxial layer, according to some embodiments. As can be seen in FIG. 32, the buried/embedded microstructure voids 3202 can be in I-Si layer 3200 while the Ge microstructure 3104 is also buried/embedded in Si layer 3200 using a few additional processing steps. First the voids 3202 are buried/embedded as in FIG. 28 with or without the P-Si anode layer 3226. Microstructures are then again

etched into the I-Si layer 3200 with the voids and then Ge 3104 is regrown resulting in a microstructure with voids 3202 in the Si layer 3200 and a Ge microstructure 3104 to enhance the bulk absorption coefficient and reduce the capacitance of the diode. Not shown is that the microstructured voids can also be buried/embedded entirely in Ge for Ge on Si layers, such that in Fig. 28, if the I-Si layer 3200 is replaced with I-Ge followed by a P^+ Ge capping anode layer 3226.

[00209] The buried/embedded microstructure voids is an inverse HCG structure with absorption, or a lossy HCG structure, and can have resonance, constructive and destructive optical interference effects of both phase and amplitude that can result in the enhancement of the bulk absorption coefficient. The period of the microstructure pillar, hole, void, buried/embedded Ge arrays can fall in the near-wavelength regime of the HCG effect or it can fall in the subwavelength regime where the grating period is much less than a wavelength and the diffraction regime where the period is greater than a wavelength. The HCG characteristics of the microstructure array and the input optical signal can be coupled to in-plane optical modes. The microstructured arrays can also behave as a lens to mode match the incoming optical signal. Good coupling efficiency also improves the overall QE of the PD/APD. According to some embodiments, a lossy HCG is provided where the absorbing region is a part of or included in the HCG structure (other effects such as scattering, near field, plasmonic, resonance, linear and non-linear optical effects to name a few, can also play a significant role in absorption enhancements), and where Si can be the HCG for photon energies that are below the Si bandgap and the Ge microstructures are buried or embedded within the Si that is absorbing to the photons with wavelength ranging from 950-1800 nm (where Si has relatively low optical losses).

[00210] According to some embodiments, the microstructures of holes, pillars, and voids can be arranged in any pattern or no pattern in the active area, including any parts of the P-I-N structure of a PD or P-I-P-I-N structure of an APD; the active area includes the absorbing “I” region and the P and N regions. According to some embodiments, to simplify manufacturing and to improve yield, the microstructures can extend outside the active areas of a PD/APD if it does not interfere with the PD/APD operations and performance. FIG. 33 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some

embodiments. The microstructure array 3300 consists of pillars, holes, and/or voids, and buried/embedded Ge in Si or Si in Ge or any combination of multiple semiconductors, can be distributed over the entire active area 3302 of the photodiode or avalanche photodiode or just partially for example in the center where the optical intensity is the highest. The active area can be defined as any area that contributes to the generation of electrical signal upon illumination with optical signal, or in the case of a PV, the generation of electricity upon illumination with photons. In FIG. 33, the active area 3302 is commonly the area within the metal ohmic contact/bond metal ring 3304. The distribution of the array 3300 can be non uniform, non periodic, non uniform is size of the microstructure, or in shape.

[00211] FIG. 34 is a top view showing distribution of microstructured pillars, holes and/or buried voids in an PD/APD, according to some other embodiments. In FIG. 34, the QE is optimized at the center of the active area where the optical intensity is the highest and away from the center, more semiconductor material is removed in the microstructure pattern to reduce the capacitance of the active area in order to decrease the RC (resistance, capacitance) time constant to achieve higher bandwidth for the PD/APD and or to increase the active area to allow passive alignment of the optical signal to the PD/APD thereby reducing the cost of packaging and assembly. Microstructured pillars/holes/buried voids 3400 near the center of the PD/APD optimize QE while the microstructured pillars/holes/buried voids 3410 at the periphery of active area 3402 minimize capacitance while still maintaining good QE.

[00212] Buried voids in the N (or P if P and N are switched) part of the P-I-N or P-I-P-I-N diode structure can reduce the effective refractive index of the semiconductor in the N layer. This is useful in increasing the refractive index contrast for HCG structures (to include other possible optical effects that may be significant in absorption enhancements such as scattering, plasmonic, near field, linear and non-linear optical effects to name a few), for example in Si the refractive index is approximately 3.5 (for wavelengths 950-1800 nm) and if half of the volume of the material is air, then the effective refractive index (1/2 air and 1/2 Si) would be approximately 1.8 for the air-Si composite material. Any semiconductor microstructures of pillars or holes fabricated on top of this composite air-Si material will have a index contrast of, for example Si pillars on the composite air-Si layer,

approximately 2. The high index contrast would enhance the performance of the HCG. According to some embodiments, this is used to enhance the lossy HCG performance (where loss can be as high or higher than - 1 dB/cm) and enhance the absorption coefficient with its resonance, light concentration and in-plane light coupling effects to name a few. There is an advantage in having the voids in the N and or N^+ layers since it will have a minimal effect on the electrical properties and characteristics of the diode since once electrons are swept into the N and or N^+ layer, they are majority carriers.

[00213] The microstructured voids in the N and or N^+ layer can be patterned, non-patterned or random or pseudo-random, and can be defined using lithography, masking and etching or just etching followed by a regrowth of Si, or Ge or any other material. The voids can range in length approximately from 0.01 to 10 micrometers and lateral dimensions can range approximately from 10-5000 nm with spacing between adjacent voids ranging approximately from overlapping to 5000 nm.

[00214] Fig. 35 shows the basic epitaxial structure 3500 for a conventional Si PV/PD diode on N Si substrate. FIG. 36 shows the structure of FIG. 35 with microstructured voids incorporated into the N-Si layer, according to some embodiments. The doping and thickness of the layers are dependent of the applications. For high bandwidth PD applications the "I" Si thickness ranges from 0.1 to 3 micrometers whereas for PV applications the "I" Si thickness ranges from 1 to 20 micrometers with doping range of intrinsic or not intentionally doped, background doping of $< 5.\ 10^{16}\ cm^{-3}$. Device size to define the area of the capacitance for high bandwidth PD (for circular apertures) ranges from 5 to 100 micrometer diameter whereas for PV, the lateral dimension can range from 0.1 to > 50 cm (centimeters) limited only by the size of the wafer or substrate. The doping ranges and layer thicknesses for non "I" layers are similar for PV, PD and APD; P or P^+ layer thickness ranges 0.1 to 3 micrometers P doping $> 5.\ 10^{18}\ cm^{-3}$, N or N^+ layer(s) thickness ranges of 0.1 to 10 micrometers N doping $> 1.\ 10^{17}\ cm^{-3}$. The Si substrate can be N doped, low N doped or undoped.

[00215] After growing the N/N^+ layer(s) on the Si substrate, microstructures of pillars and or holes and or nanowires are etched into the N/N^+ layer(s) 3604 and followed by a N/N^+ layer(s) regrowth resulting in buried voids 3622 as shown in Fig.

36. The regrowth surface may or may not need further planarization such as using chemical mechanical polishing (CMP). Some applications may have more optimal performance with a non-planar surface, for example PV that can couple sun light in multiple angles with minimal reflections (a rough surface reflect less light).

Subsequent "I" Si layer 3606 and P/P^+ layer 3608 are grown on the N/N^+ layer(s) 3604 with the buried voids 3622. In addition to reducing the effective refractive index, at wavelengths where Si has low loss (approximately -1 dB/cm or less), 950-1800 nm, the buried voids 3622 can be patterned into a reversed HCG and behave as a very reflective (close to 100% reflectivity) broad spectrum mirror for any photons illuminating from the top (P side) and not absorbed in the "I" microstructured pillar/hole region on the first pass, the photons can be reflected back toward the absorbing "I" region. In addition, with the voids, the substrate may be more flexible and lightweight such that it can be more adaptable to contoured surfaces and/or for use where weight is an issue such as a solar panel, or for mobility.

[00216] FIG. 37 is a cross section showing etched Si microstructured pillars/holes with regrown Ge covering the Si, according to some embodiments. The starting structure is the same as layers 3500 in FIG. 35. The Si microstructure pillar and/or hole arrays are etched with a depth ranging from 0.1 to 10 micrometers and subsequently regrown with a I-Ge layer 3702 of thickness 0.01 to 4 micrometers including according to some embodiments a 1-10 nm low temperature buffer Ge layer to account for lattice mismatch between the Si and Ge. Note that the Ge buffer may not be included for pillar hole lateral dimensions of approximately 1000 nm or less since the lattice mismatch strain at that small area may not be significant to cause extensive defects to form. The lateral dimensions of the microstructured pillars 3704 and holes 3706 range from 10 to 5000 nm and spacing of adjacent elements from overlapping to 5000 nm. The P/P^+ Si layer 3708 is left on in FIG. 37 as it may be useful in making good P ohmic contact with the ohmic metals of Ti, W, Al silicide that are 1-50 nm thick to be semitransparent or transparent transition metal silicide.

[00217] FIG. 38 is a cross section showing microstructured Si pillars/holes with Ge regrowth on an N-Si layer having embedded microstructured voids, according to some embodiments. The structure shown in FIG. 38 is similar in starting

material as shown in FIG. 36. The buried voids 3822 in the N/N^+ layer 3804 act to reduce the effective refractive index of layer 3804. The voids spacing and lateral dimensions can be subwavelength ($< \lambda$) or even deep subwavelength ($<< \lambda$) to minimize optical scattering loss such as Rayleigh scattering which is proportional to λ^{-4} where λ is the wavelength. The wavelength of interest range from 300 to 1800 nm.

[00218] FIG. 39 is a cross section showing partial coverage I-Ge on microstructured Si pillars/holes, according to some embodiments. In the variation of the microstructure shown in FIG. 39, instead of regrowing I-Ge over the entire Si microstructured pillars and holes, it is only grown on part of the Si microstructures. Part of the Si microstructure is without I-Ge and the other part has regrown I-Ge. The partial regrowth of Ge can be accomplished by partially covering the Si microstructure with a dielectric such as SiOx or SiNx by directional deposition such as electron beam evaporation deposition, or directional laser ablation deposition or other directional methods such as ion milling to remove native oxide of Si selectively or ALD thin layer of oxides/nitrides and removing selectively and directionally with ion beam milling. Once the Si microstructure is partially coated with an oxide or nitride (or other dielectric such as CaFx, TaOx, TiOx, to name a few) Ge epitaxial regrowth will predominantly occur where there is lattice information such as a Si surface. The I-Ge regrowth 3902 thickness can range from 0.1 to 4 micrometers or more. The Si microstructure of pillars 3904 or holes 3906 can have a depth of 0.1 to 10 micrometers and a lateral dimension of 10 to 5000 nm and spacing between adjacent microstructures of overlapping to 5000 nm. Both Si and Ge microstructures are exposed to photons with wavelengths ranging from 300-1800 nm from photons impinging from the anode surface and impinging on the sidewalls of the microstructure directly, scattered, near field, resonance, HCG effect, linear and non-linear optical effects, and with enhanced absorption coefficient. Both Si and Ge will generate photocurrent due to the incident photons. The Si current generator and Ge current generator are in parallel and the total photocurrent generated by this PD/PV is the sum of the Si and Ge photocurrent generators. The buried voids 3922 reduce the refractive index of the N/N^+ layer 3914 and improve the index contrast of the microstructure and the substrate thus improving the performance of the lossy HCG for enhancing the absorption

coefficient. The voids 3922 in the Si 3914 can also behave as a good reflector to reflect photons back toward the "I" absorbing layer for a double pass (for photons illuminating from the top side). BOX or SOI 3912 can also be used in addition with the buried voids or without the buried voids, as the refractive index of SiO_2 is approximately 1.54, roughly half that of silicon at infrared and near infrared wavelengths.

[00219] FIG. 40 is a cross section showing the basic components for a microstructured Si-Ge pillar hole array PD/PV and/or APD, according to some embodiments. Note that the APD multiplication layers are not shown for simplicity. Only the very basic parts of the device is shown. After processing steps shown in FIG. 39 are completed, surface passivation is carried out using thermal oxide or ALD or PECVD or CVD deposition of oxide or nitride to passivate or SiGe as a passivation layer on Ge. A filler 4002 is spun on or deposited such as spin-on-glass, or SiOx, SiNx by PECVD or CVD. Using RIE to etch back to expose either the Ge or P/P^+ Si (during i-Ge epitaxial growth, the P dopant in the P/P^+ Si may diffuse into the Ge layer to also result in a P/P^+ Ge layer). Ge and or Si P- ohmic material may be Al, W, AuGe, Au, Au/Ti and Al, TiN, Pt, transition metal-silicide respectively; ohmic contacts to P and N semiconductors are well known in the literature and art and these are only a few examples of possible ohmic contacts. A transparent conducting oxide (TCO) 4004 such as indium tin oxide (ITO) may be used to further reduce the series resistance of the anode. For microstructured holes, since the P/P^+ layers are contiguous, TCO 4004 may not be used and only a perimeter (ring for circular apertured PD/APD/PV) border ohmic contact and metallization 4006 may be used instead to reduce series resistance of the ohmic contact, such as Al, Au/Ti. Cu, to name a few. Anti-reflection layers are not shown for simplicity. N ohmic material can be used on the substrate or on the N/N^+ layer together with metallization. Al, Pt, transition metal silicide, followed with Al or Au deposition (e-beam, sputter, thermal evaporation) on the ohmic contacts reduce series resistance. Ohmic contacts normally use an annealing process that is well known in the art. Bond and/or connecting metallization 4006 is deposited (using standard processing methods) to complete the PD/APD/PV device. Sunlight/optical signal is illuminated from the top (anode) of the device normal to the surface or at any angle off normal and may be rotated to optimize the QE. At wavelengths where

Si is low loss (950-1800 nm or more) the buried voids can both reduce the effective refractive index of Si and act as a reflector to reflect photons that are not absorbed back toward the absorbing region. The surface of the N/N^+ layer 3914 can be non-planar to help diffuse the reflected photons to optimize its absorption in the microstructured Si and Ge array. A contact pad 4008 can be provided, for example, on the side of layer 3914 as shown. Although many of the embodiments show the microstructures of Si and Ge, Si, Ge are normal to the surface (vertically aligned) and straight, according to some other embodiments if the N/N^+ surface is non-planar, subsequent layers may also be non-planar. Etching (wet chemical or dry RIE, DRIE) may result in microstructures that are off normal and not straight (with bends) which may further improve the absorption of photons. Due to the non-planar topology of the surface, the microstructures may have various orientations depending on the orientation of the crystal within the same device. The different orientations of the microstructures are advantageous to capturing photons that may be illuminating the surface of the device at different angles, for example for PV as the sun changes position in the sky and for PD/APD for applications where multiple optical signal may illuminate the PD/APD from different angles/directions.

[00220] Microstructured Si pillar and/or hole arrays/pattern/random PD shown in FIG. 5, *supra*, can also have buried voids in the N/N^+ layers as shown in FIG. 10 to both reduce the refractive index of Si so that the microstuctures of Si pillars/holes are more optimized as lossy HCG by increasing the refractive index contrast and also as a HCG reflector in Si for wavelengths where Si has low loss, 950-1100 nm for this application as a wide bandwidth (> 5 Gb/s) PD or as a PV.

[00221] The Si substrate in all the embodiments described herein can be either Si with doping, not intentionally doped, low doping, or buried oxide (BOX) or silicon on insulator (SOI) where the silicon layers again can be doped, heavily doped, lightly doped or not intentionally doped. The BOX and SOI layers allow the removal of the all or almost all of the Si substrate to reduce optical losses, increase mechanical flexibility and also the refractive index of SiO_2 in BOX and SOI have refractive index of approximately 1.54 in the infrared and near infrared wavelengths which is roughly half of silicon refractive index. The low index of SiO_2 also improves the performance of HCG, or the silicon dioxide layer can be removed for bottom illuminated PD/APD/PV.

[00222] FIGs. 41A-41B are cross sections showing aspects of a microstructured pillar/hole array device above a N-Si layer having buried microstructured voids, according to some embodiments. The bulk layers 4100 shown in FIG. 41A include I-Si layer 4112 and N-Si layer 4110. Microstructured voids 4102 are formed in the N-Si layer 4110 using techniques such as described herein *supra*. The structures in FIGs. 41A and 41B are a version of the PDs/PVs shown in FIGs. 25A-B but with buried voids 4102 in the N/N^+ layer 4110 to improve the refractive index contrast for lossy HCG (microstructures of Si and Ge) and to provide a reflector low loss HCG for photons. Pillars 4124 and/or holes 4122 arrays are formed in I-Si layer 4112. I-Ge is regrown in the etch region 4122 resulting in a buried/embedded Ge "I" layer with microstructure voids 4102 in the N Si layer 4110 to reduce the effective refractive index of Si and/or to reflect photons entering from the anode surface at wavelength where Si is low loss (950-1800 nm). Cap layer 4126 can be P-GE or P-Si regrowth. In the case of bottom illumination, an anti-reflection coating 4130 may be provided.

[00223] FIGs. 42A-42D are cross sections showing aspects of an APD with microstructured pillar/hole arrays above an N-Si layer having buried microstructured voids, according to some embodiments. The APDs shown in FIGs. 42A-42D are versions of the APD shown in FIGs. 24A and 24B, *supra*, except that buried voids 4202 are included in the N/N^+ layer 4210 to improve the refractive index contrast for lossy HCG (microstructures of Si and Ge) and to provide a reflector low loss HCG for photons. According to some embodiments, BOX/SOI Si wafers can also be used with or without buried voids to improve refractive index contrast for optimal HCG lossy operation. Only the basic structures are shown for simplicity. Electrical isolation, passivations, ohmic metallization, anneal, anti reflections, bond/interconnect metallization, guard rings, to name a few are not shown. FIG. 42A shows the bulk layers 4200, which include N-Si layer 4206, I-Si layers 4208 and 4212 and P-Si layer 4210. Microstructured voids 4202 are formed in the N-Si layer 4206 using techniques such as described herein *supra*. As in the case of FIG. 41B, I-Ge is regrowth in the etched area 4222. The voids 4202 are to reduce the effective index of the N-Si since the optical field will be an average effective refractive index composing of air and Si. If the voids 4202 are patterned for HCG effect, photons can be reflected that are not absorbed in the first pass

through the "I" absorbing region 4212 for photons illuminating the APD 4220 from the top or anode surface. The APD can also be illuminated from the bottom or cathode side.

[00224] FIGs. 42C and 42D show another variation of an APD 4230 in which voids 4204 are formed in the I-Si multiplication layer 4208 as well as in N^+ layer 4206 to reduce the effective refractive index and capacitance of those layers. Note that the elongated nature of the microstructured voids will have a minimal effect on charged carrier transport in the semiconductor materials. According to some embodiments, voids of various shapes and densities can be formed in the P anode, N cathode, P charge, and/or I multiplication layers of the APD in addition to the absorbing I layer. The addition of voids in the I multiplication layer 4208 and the I absorption layer 4212 can reduce the effective capacitance resulting in a short RC time constant for the device. The voids 4204 in the multiplication I Si layer 4208 also reduce the effective refractive index, which is helpful in enhancing the absorption coefficient in a HCG absorbing mode.

[00225] Epitaxial growth/regrowth/overgrowth/selective area growth/epitaxial lateral over growth of Si, Ge, SiGe, III-V such as InP, GaAs, GaN, InGaN, InGaAs, InGaAsP, InSb, heteroepitaxy, homoepitaxy, heterogeneous epitaxy to name a few, using chemical vapor deposition (CVD), metallic organic chemical vapor deposition (MOCVD), atomic layer deposition (ALD), molecular beam epitaxy (MBE), gas source molecular beam epitaxy (GSMBE) plasma enhanced chemical vapor deposition (PECVD), laser ablation deposition (LAD) to name a few, are well known in the art.

[00226] According to some embodiments, material other than Si and Ge on Si are used. For example, the techniques described herein can be applied to all combinations of Si, Ge, III-V and II-VI material families and substrates.

[00227] FIGs. 43-46 are top views illustrating various dimensions, spacings and shapes for microstructured elements, according to some embodiments. FIG. 43 shows a microstructured pillar and/or hole array 4300 (also applicable to embedded or buried voids) that is uniformly spaced with a fixed diameter ranging from 100-5000 nm and a spacing ranging from 100-10000 nm. The pillars and or holes can be formed in or using: Si, Ge, SiGe, or other materials such as III-V or II-VI material family. Examples includes: GaAs, InP, InGaAs, InGaAsN, InGaAsP,

InAs, GaN, InGaN, ZnTe, CdS, ZnSe, and HgTe. According to some embodiments, the microstructures can also be formed in or using absorbing polymers, glass, and/or ceramics.

[00228] FIG. 44 shows a microstructured pillar and/or hole array 4400 having a fixed diameter but with non-uniform spacing such as aperiodic or a mixture of periodic and aperiodic or random/pseudo random spacing or a mixture of random/pseudo random, periodic and aperiodic. According to some embodiments, the arrays can also be uniformly spaced periodic but with varying diameter. FIG. 45 shows a microstructured pillar and/or hole array 4500 having both variable diameters (ranging from 100 nm to 5000 nm) and variable spacing (ranging from 100 nm to 10000 nm). According to some embodiments, the variations can be random/pseudo random, or a pattern or a mixture of patterns or any combinations thereof. FIG. 46 shows a microstructured pillar and/or hole array 4600 having various shapes such as oval, circular, rectangle, doublets, triplets, and stars. In general, any shape that can be generated using a photolithographic mask, or e-beam direct write or that can be generated with a mold for imprint lithography, can be used. The pillar/hole arrays can also have a combination of different shapes and spacings, as well as variations in the depth of the microstructured holes or lengths of the microstructured pillars/mesas. The variations can be periodic, aperiodic, or random (or a mixture of periodic, aperiodic and random) within a single array.

[00229] According to some embodiments, for some applications an array dimension of Si or Ge or III-V microstructured pillars or holes of length 2 μm approximately (or depth of 2 μm approximately) with diameter of pillar/hole of 390 nm approximately and center to center spacing of 1060 nm approximately has been found to be suitable for enhancement of the absorption coefficient of greater than 50X.

[00230] According to some embodiments, the material can be Si, Ge, SiGe, Ge on Si, III-V, II-VI, III-V on Si, polymer, glass, ceramic and any combination thereof. Examples of III-VI and II-VI are InP, GaAs, AlGaAs, AlAs, AlInAs, InGaAs, InGaAsP, InAs, InGaAsN, InN, GaN, InSb, ZnSe, ZnTe, HgTe, and CdS. Also III-V, II-VI and group IV material such as Ge can be embedded in Si microstructures using SAG, VLS, ELOG growth methods in MOCVD, CVD, MBE, reactors.

[00231] FIGs. 47-48 are cross sections showing microstructured pillar and hole arrays having varying lengths and depths, according to some embodiments. FIG. 47 shows a microstructured pillar array 4700 having different lengths, diameters and spacing. According to some embodiments, the pillar diameters range from 10 nm to 5000 nm and the pillar heights range from 0.1 to 10 microns. FIG. 48 shows a microstructured hole array 4800 having different depths, diameters and spacings. According to some embodiments, the holes have diameters ranging from 10 nm to 5000 nm and depths ranging from 0.1 to 10 microns. The variation in lengths and etched depths can be accomplished by additional lithographic masking steps where regions are masked for longer etch or shorter etch to vary the length of the pillars and the depth of the holes. The lengths and depths can be gradually or sharply varied. A patterned grating effect can be used to further optimize the optical path lengths and increase the enhancement factor for absorption coefficient. Other uses include forming a light trap by using constructive and destructive optical interference, generating a fresnel lens, matching the mode of the optical signal, forming a filter in wavelength selectivity in wavelength division multiplexing for example, or as a wavelength selector for spectroscopy and sensor applications. It should be noted that by varying the dimensions and spacing of the microstructured pillars and holes in an array can also result in constructive and destructive optical interferences that can also increase the enhancement factor of the absorption coefficient, improve light trapping, create fresnel lens, mode matching of radiation patterns of the optical signal.

[00232] FIG. 49 shows shows a microstructured surface having a combination of both pillars and holes, according to some embodiments. Microstructure array 4900 includes pillars and holes co-existing on the same microstructured surface either globally or locally. Both pillars and holes can exist in a single array (such as shown in FIG. 49) for the microstructured photodetector, or holes and pillars can exist on separate arrays for different microstructured photodetectors. In addition, hole(s) can exist in a pillar and pillar(s) can exist within a hole and these also can be global or local. The pillars, holes, hole(s) in pillar and pillar(s) in holes can have any shape, for example a rectangular pillar within a round hole, can have any mixture thereof to optimize enhancement of the absorption coefficient, light trapping, constructive and destructive optical interference, scattering, near field effects,

linear and non-linear optical effects, subwavelengths effects, fresnel lens, wavelength selection, optical mode matching, diffraction, high contrast grating, blazed grating, high Q resonator, highly reflective mirrors using high contrast grating.

[00233] The microstructured pillar and hole (and variations thereof) arrays can be fabricated in Si, Ge, Ge on Si, SiGe on Si, SiGe on Ge. The array structure can be any combination of Si, Ge and SiGe. The array can be entirely Si or Ge or SiGe, or Ge on Si, or Si on Ge, or Ge on Si with SiGe on both. The structure can also include III-V and II-VI material systems together with Si, Ge and SiGe and any combination of Si, Ge, and III-V, II-VI material systems. According to some embodiments, the array structure can also include polymer, glass, oxides, nitrides, sulfides and chlorides of transition metals, ceramics, quartz, SOI, IOS, organic conducting and non conducting polymers, carbon based material such as graphene to name a few.

[00234] The microstructures pillars, holes, voids, and any other shapes such as pyramids, microwires, nanowires, multiple materials, SAG microstructures, can have orientations that are not perpendicular to the surface of the substrate. They can have a single or multiple orientations that can be perpendicular and or off perpendicular to the surface. They can be random or pseudo random, single pattern or multiple pattern orientations at any angle where angle can range from 0 to 90 degrees with respect to the normal to the silicon substrate, and they can be on sidewalls and on all three dimensions. With the microstructures at certain orientations, the photosensor can have a higher sensitivity to certain direction of illumination. Conversely, with multiple orientations and or random or pseudo random orientations the photosensor can be mostly insensitive to direction of illumination.

[00235] Reducing the effective refractive index with buried voids in semiconductor has applications beyond PD/APD and PV devices. It also, for example, has applications in optical waveguides. FIG. 50 is a cross section of an optical ridge waveguide, according to some embodiments. Waveguide 5000 uses the density of voids to alter the effective refractive index of Si. According to some embodiments materials other than Si are used, for example other semiconductors such as Ge, SiGe, any of the III-V semiconductor family, or other material such as

ceramics, glass, polymer. In Si photonic optical waveguide 5000, the ridge 5002 and slab 5004 are made of Si on a BOX (buried oxide) Si substrate 5006. Due to the high refractive index of Si. 3.49 at 1100-1800 nm wavelengths, the dimensional tolerance of the solid Si waveguide is very critical. Known Si photonic components are difficult to manufacture and have low yield and are temperature sensitive. According to some embodiments, voids are buried in the Si layers. By varying the density of the voids, the refractive index of the composite Si-voids can be adjusted. In the schematic diagram of FIG. 50, a ridge waveguide 5000 has voids 5014 on slab 5004, as well as voids 5012 on ridge 5002. The density of voids 5012 in the ridge 5002 is less than the density of voids 5014 in the slab 5004. The refractive index in the ridge 5002 is therefore higher than the refractive index in the slab 5004 resulting in a ridge optical waveguide. The optical mode of the waveguide 5000 is indicated by the dotted oval 5022. The lower refractive index helps in reducing the dimensional tolerance and the optical waveguide can have a larger dimension. Thus, according to some embodiments, the refractive index can be varied by varying the void density making other components such as couplers easier to manufacture. The dimensions of the voids can be subwavelength ranging from 10nm to 1000nm depending on optical wavelengths.

[00236] According to some embodiments, voids are also buried in a silicon wafer (including BOX/SOI silicon wafers) to adjust the effective refractive index of the Si wafer. The Si wafer with buried voids can then be the starting platform for silicon photonic circuits. It can also be the platform for large area PV cells that allow mechanical flexibility but still retain the high quality of silicon and its electrical characteristics. This can also be the platform for flexible displays and other electronics that require mechanical flexibility and or light weight. According to some embodiments, burying or embedding voids is not limited to just Si, but can include Ge, GeSi, amorphous semiconductors, III-V, II-VI material families, polymers, glass, quartz, metal, alloys, ceramics and any other material that requires flexibility. In some embodiments, the voids can be filled with gas, liquid or solid for specific applications. Gel such as spin on glass that does not require anneal for example can be used for impact/crack situations where the integrity of the device is compromised such as a crack due to impact, to seal surfaces such as semiconductors or any surfaces sensitive to environment such as moisture, water,

oxygen to name a few to prevent further deterioration. Voids are also excellent in preventing crack propagation.

[00237] FIG. 51 is a cross section of a buried optical waveguide in silicon using voids, according to some embodiments. A composite waveguide 5100 is formed in Si substrate 5106 using Si-voids to selectively alter the effective refractive index in certain locations. The effective refractive index of Si can be adjusted precisely by adjusting the total volume of the voids in a given volume of Si. In the example shown in FIG. 51, the higher density voids 5114 surround a central region of lower density voids 5112. The optical mode of the waveguide 5100 is indicated by the dotted oval 5122.

[00238] According to some embodiments, the dimension and spacing of the voids are optimized to reduce scattering losses and to provide ease of manufacturing. Also, the void dimensions and spacing can be adjusted for certain applications. For example, in HCG the dimensions and spacings are selected to satisfy the near field regime where the dimensions and spacing lie approximately between the wavelength in the high refractive index material and the wavelength in the low refractive index material. In most cases, in the applications to reduce the effective refractive index, the void and the surrounding material dimensions and spacing are in the subwavelength regime where the microstructures containing the voids are less or much less than the wavelength in either the high or low index material. For coupling applications, the diffraction regime may be the microstructure (voids and material) dimensions and spacing. It can also be a mixture of two or more regimes to optimize a device performance.

[00239] Array patterns can include microstructure ensembles whose distribution of individual microstructures can be periodic, aperiodic, chirped, random, pseudo-random, uniform, or non-uniform in all three dimensions, orientations and spacings, (including overlapping). According to some embodiments, the patterns can include microstructures within microstructures. The terms “array” and “pattern” are used herein interchangeably.

[00240] The PD/APD are biased between the anode and cathode, to extract a broadband modulation signal greater than a gigabit per second (Gb/s) at a typical transmission line impedance is 25-50 ohms. According to some embodiments, the external bias is provided with a bias-tee connected to the transmission line to block

the RF signal from reaching the DC power supply and to block the DC from biasing the transmission line away from the PD/APD. The bias-tee basically consists of an inductor and capacitor, the inductor to block the RF and the capacitor to block the DC away from the PD/APD. External bias of -2 to -30 volts is applied depending on the application, PD or APD and performance desired.

[00241] In PV mode, no external bias is applied and the PV is basically a current generator. All the electrical connections are for DC current from the PV which then connects to a converter that converts the DC current/voltage to AC current/voltage.

[00242] PV devices are in DC mode whereas PD/APD for data and tele communication are all RF with modulation bandwidth ranging from 1 to 100 Gb/s. Transit time of carriers and capacitance are critical in PD and APD but not so much for PV.

[00243] The terms “modulation bandwidth” and “bandwidth” are interchangeable as used herein. Both terms refer to the modulation (e.g. of a laser or LED) where an RF signal is impressed on the light. When this modulated light (also referred to as “optical signal”) illuminates the PD/APD, the RF modulated signal is extracted and converted from light to electrical signal. For example, a bandwidth or modulation bandwidth of a PD/APD of 20 Gb/s means that an RF signal impressed on the laser light beam at a data rate at 20 Gb/s can be converted by the PD/APD from optical to electrical with good signal integrity or signal replication. The laser/LED is the transmitter and the PD/APD is the receiver where the electrical signal can be further processed by an amplifier such as a transimpedance amplifier and the signal sent for further analysis and processing in application specific integrated circuits (ASIC) computers (CPU central processing unit), routers, memories, to name a few.

[00244] According to some embodiments the applications for the microstructured pillars and or holes in Si and Ge and Si regrowth with Ge, Ge on Si, with and or without buried or embedded voids photodiodes and avalanche photodiodes, are in data and tele communications. According to some embodiments, these applications include: fiber to home, local area network, data center optical interconnects board to board, on the board, rack to rack, and chip to chip, between data centers, metro area network, and optical communication for distances from less than a centimeter to over 10 kilometers or more. The

applications in consumer space also includes: game box, personal computers, tablets, mobile devices such as smart phones, animations studios, and anywhere that benefits from a bandwidth of more than one gigabit per second. Other applications of the microstructured PDs and APDs, according to some embodiments, are in sensors where broadband communication is important, such as sensors for infrastructures, health, environment, oil exploration, where the sensors communicate with a remote receiver that is connected to data centers for data analysis.

[00245] Other applications of the microstructured PD and APD, according to some embodiments, are in analytical instruments and optical tests and measurement instruments where high sensitivity and bandwidth are important.

[00246] According to some embodiments, the microstructured PV have applications in energy harvesting for power generation all the way from gigawatts to watts, to power cities and homes to powering sensors. Since the microstructured PV is lightweight and high efficiency it can be used in mobile applications, space, solar transportation, recycling of photons in home, offices and factories. The PV can also be used on windows and can be semi-transparent.

[00247] The described microstructures in Si, Ge, Si regrowth with Ge, Ge on Si, pillars, holes, and voids can be any shape and form, and are not limited to the schematics shown. According to some embodiments, the dimensions range from 10-10000 nm (nanometers). The microstructures can be within each other such as pillar(s) in hole(s), hole(s) in pillar(s) and void(s) can be in the pillar, and buried and or embedded in any layer of the semiconductor heterogeneous or homogeneous. The material used includes semiconductors such as Si, Ge, GeSi, Ge on Si, and the III-V group material family of InP, GaN, InGaAsP, GaAs, and other semiconductors such as ZnO, CdTe, CuInGaSe (CIGS), amorphous Si, or any amorphous semiconductor and or microcrystalline and crystalline semiconductor. The material can be a combination of amorphous, microcrystalline, crystalline heterogeneous and or homogeneous. The material used is also not limited to semiconductors, but also include polymers, electrically conducting, semiconducting, non conducting polymers, organic and or inorganic polymers, glass, conducting, semiconducting, non conducting glass. Nanoparticles of semiconductors and or metal can also be buried in the polymer and glass.

Semiconductors, polymer and glass can exist within the same microstructure, separately or in any combination.

[00248] According to some embodiments, in silicon photonic circuit applications, optical waveguides such as shown in FIG. 50, *supra*, can be integrated with optical sources and optical detectors such as photodiodes, avalanche photodiodes and photoconductors. FIG. 52 is a cross section of a ridge waveguide integrated with a microstructured PD/APD, according to some embodiments. Device 5200 includes a ridge waveguide that is edge coupled to a microstructered Ge on Si photodiode or avalanche photodiode (with multiplication layers added). In the ridge wave guide portion, as shown in FIG. 50, a ridge 5202 has lower density voids 5212 and slab 5204 had higher density voids 5214. Ion implantation is used to increase the N doping (region 5224) for the PD and a coplanar transmission line is fabricated on the photodiode to extract the electrical signal as shown in FIG. 53, *infra*. Anode contact 5226 is made of P-Ge, according to some embodiments. The cathode contact is made to layer 5224 (cathode contact not shown for simplicity and clarity of drawing.)

[00249] FIG. 53 is a top view the integrated ridge waveguide and microstructured PD/APD shown in FIG. 52, according to some embodiments. The device 5200 is in a coplanar transmission line configuration. Ridge portion 5202 is 0.5 to 10 μm wide and 0.1 to 10 μm deep, according to some embodiments. Slab portion 5204 has higher density voids, as shown in FIG. 52, to vary the refractive index as a platform for silicon photonic circuits. Coplaner cathodes 5228 and 5230 are in contact with the N-Si ion implanted region 5224 shown in FIG. 52. According to some embodiments, the optical field can also be coupled evanescently by placing the PD/APD above the optical waveguide such that the optical field overlaps the absorbing I microstructures.

[00250] FIGs. 54A and 54B show a microwave transmission line on Si with voids, according to some embodiments. High bit rate transmission lines on silicon suffers from a multitude of effects, from slow wave to dispersion to loss. However by removing most of the silicon material with the addition of high-density voids according to some embodiments, the dispersion and loss can be alleviated and signal integrity restored. An advantage is that silicon can be the substrate for both microwave transmission line and for ICs without the use of intermediate ceramic

such as alumina for transmission line to connect various IC chips. FIG. 54A is a cross section showing high density voids 5314 buried in silicon 5304 which reduce the effective dielectric constant of the silicon, and disrupt lateral electrical conductivity which in turn can result in lower microwave loss and dispersion which are important as bit rate increases into the multi Gb/s range (e.g. 40-60 Gb/s). Coplanar microwave metallic transmission lines 5310 are provided as means to move the electrical signal to/from electronic devices (e.g. processors, storage devices, input-output devices, ASICs, CPUs, and memories) on the same substrate. FIG. 54B is a top view. Conventional techniques use multi chip carriers that need additional packaging. According to some embodiments, having many devices all on the same silicon substrate greatly reduces the cost since it can be all fabricated at once and requires no additional packaging for each chip. According to some embodiments, the voids 5314 are arranged in a fashion where the path length in silicon laterally is significantly increased in order to increase lateral resistivity. According to some embodiments, Ion implantation of protons and or oxygen can be used to further increase electrical resistivity. Although FIGs. 54A and 54B show a co-planar arrangement, according to some embodiments other microwave transmission line arrangements (e.g. microstrip, slotline, and stripline) are used with a semiconductor substrate having high-density buried voids. According to some embodiments, the positioning and/or other properties (e.g. size, shape, and filling material) of the high-density voids can be selected such that the slow wave effect can be manipulated or "tuned" in a way that is suitable for the application at hand.

[00251] FIG. 55 is a cross section of voids for thermal conduction and thermal isolation of heat producing ICs and light emitters, according to some embodiments. The buried voids in silicon 5404 can be filled with thermal conductors such as helium gas, metal such as copper, aluminum, tungsten, or ceramic such as boron nitride, or carbon, graphene, diamond like carbon, or heterogeneous material/ceramic doped with metal nanoparticles, carbon nanotubes. The voids 5414 underneath the heat producing elements such as ICs and CPUs 5422, and light emitters 5420 such as laser diodes and bipolar drivers, can be filled with enhanced thermal conductors to extract the heat from the hot components and direct it to a heat sink 5402. Voids 5412 between hot elements are kept at a low

thermal conducting state that are either in partial vacuum or filled with a gas such as nitrogen, argon, carbon dioxide, for example to prevent thermal cross talk between the hot components or to any other components where heat is not desirable. According to some embodiments, the voids are arranged in a fashion such that the path length in silicon is vastly increased to maintain low thermal crosstalk. According to some embodiments, the techniques of FIG. 55 are used to keep PVs cool when exposed to the sun. According to some embodiments, thermoelectric devices can be integrated together with the voids to generate electricity from the excess heat.

[00252] FIG. 56 is a cross section showing a distribution of voids to increase lateral path length for increasing lateral electrical resistivity and decrease lateral thermal conduction, according to some embodiments. The buried voids 5602 configured for microwave transmission lines and/or for thermal management can be arranged in a randomly, pseudo randomly, or in a pattern in areas where lateral electrical and thermal conductance is significantly reduced and vertical electrical and thermal conductance is significantly enhanced. There may be areas where lateral electrical and thermal conductance enhancement is desired, in which case the voids can overlap to form a conducting channel.

[00253] This patent application refers to certain theories in explaining the nature and operation of devices, but it should be clear that such theories are based on current understanding and do not affect the actual operation of the disclosed devices even if future developments prove the theories incorrect. This patent specification also refers to numerical ranges of paramaters, and it should be understood that insubstantial departures from such ranges are still within the spirit of the disclosed advancements.

[00254] Although the foregoing has been described in some detail for purposes of clarity, it will be apparent that certain changes and modifications may be made without departing from the principles thereof. It should be noted that there are many alternative ways of implementing both the processes and apparatuses described herein. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the body of work described herein is not to be limited to the details given herein, which may be modified within the scope and equivalents of the appended claims.

CLAIMS

What it claimed is:

1. A photodetector with microstructure-enhanced photoabsorption comprising:

a cathode region;

an anode region;

reverse biasing circuitry configured to apply a voltage between said cathode and anode regions such that said cathode region is driven to a more positive voltage than said anode region; and

a microstructure-enhanced photon absorbing semiconductor region operatively associated with the cathode and anode regions and configured to absorb photons from a source signal, said absorbing region including a plurality of microstructures configured to increase absorption of photons at a range of wavelengths that includes a wavelength of said source signal relative to an absorbing region that is not intentionally microstructure-enhanced.

2. A photodetector according to claim 1 wherein said microstructures are configured to increase absorption of photons at the range of wavelengths by being dimensioned and positioned to facilitate said increase of absorption.

3. A photodetector according to claim 2 wherein said microstructures have at least one dimension that is equal to or shorter than a longest wavelength in the range of wavelengths.

4. A photodetector according to claim 1 wherein said microstructures have one or more shapes selected from a group consisting of pillars, holes and voids.

5. A photodetector according to claim 1 wherein said microstructures are arranged into a periodically-spaced array.

6. A photodetector according to claim 1 wherein said microstructures are arranged into a non-periodically-spaced, randomly-spaced or multiperiodically-spaced array.

7. A photodetector according to claim 1 further including a substrate material and wherein said microstructures have a major longitudinal axis normal to an upper surface of the substrate material.

8. A photodetector according to claim 1 wherein said microstructures have major longitudinal axes that are not parallel to one another.

9. A photodetector according to claim 1 wherein said microstructures are oriented to reduce cross-talk in an application selected from a group consisting of: free space applications and coupling to multiple sources in an array, compared to an otherwise same photodetector.

10. A photodetector according to claim 1 wherein said microstructures are oriented to reduce sensitivity to any single direction of said source signal compared to an otherwise same photodetector.

11. A photodetector according to claim 1 wherein the microstructures increase absorption compared to an otherwise same photodetector at least in part by forming an absorbing mode high contrast grating.

12. A photodetector according to claim 11 wherein the microstructures increase absorption compared to an otherwise same photodetector at least in part due to one or more of the following effects: resonance effects, scattering effects, near field effects, sub-wavelength effects, and interference effects.

13. A photodetector according to claim 11 wherein said high contrast grating is in 2-dimensions or 3-dimensions.

14. A photodetector according to claim 11 wherein said high contrast grating is of one or more types selected from a group consisting of: periodic, aperodic, chirped, random, pseudo random.

15. A photodetector according to claim 11 wherein contrast for said high contrast grating is increased using a plurality of voids in one or more materials compared to an otherwise same photodetector.

16. A photodetector according to claim 1 wherein said microstructure-enhanced photon absorbing semiconductor region and said microstructures are formed of silicon.

17. A photodetector according to claim 16 wherein said photodetector is a silicon photodiode.

18. A photodetector according to claim 17 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 5 gigabits per second, at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 60%.

19. A photodetector according to claim 18 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 10 gigabits per second, at source signal wavelengths of 850 nanometers with a quantum efficiency of at least 60%.

20. A photodetector according to claim 17 wherein said photodetector is configured for quantum efficiency of greater than 60%.

21. A photodetector according to claim 16 wherein said photodetector is an avalanche photodiode.

22. A photodetector according to claim 21 wherein said avalanche photodiode is configured to detect said source signal at a data bandwidth of greater than 5 gigabits per second, at source signal wavelengths of 850 nanometers, and having a gain of greater than 2.

23. A photodetector according to claim 21 further comprising a multiplication region that includes a second plurality of microstructures.

24. A photodetector according to claim 23 wherein said second plurality of microstructures extends into one or more multiplication layers selected from a group consisting of: P multiplication layer, N multiplication layer and charge layer.

25. A photodetector according to claim 16 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 1 gigabit per second, at source signal wavelengths of 980 nanometers with a quantum efficiency of at least 40%.

26. A photodetector according to claim 16 wherein said photodetector is configured to detect said source signal at a data bandwidth of greater than 0.5 gigabits per second, at source signal wavelengths of 1000 nanometers with a quantum efficiency of at least 30%.

27. A photodetector according to claim 1 wherein said plurality of microstructures effectively reduces capacitance of the photodetector when compared to a microstructure-free device having a similar photon absorbing length.

28. A photodetector according to claim 1 wherein said microstructure-enhanced photon absorbing semiconductor region and said microstructures are formed of silicon and germanium.

29. A photodetector according to claim 28 wherein said microstructures are formed by etching away portions of silicon and using a selective area growth process to grow germanium in the etched away portions.

30. A photodetector according to claim 1 wherein said microstructure-enhanced photon absorbing semiconductor region and said microstructures are formed of germanium.

31. A photodetector according to claim 30 further including a substrate and wherein said cathode, absorbing and anode regions are formed above the substrate and said photodetector is configured to receive said source signal from a substrate-side of the photodetector.

32. A photodetector according to claim 31 wherein said anode region comprises a germanium P layer formed by an epitaxial lateral overgrowth process.

33. A photodetector according to claim 31 wherein the photodetector is configured for a portion of the source signal to pass through the absorbing region a first time, reflect from a surface and thereafter pass through the absorbing region a second time.

34. A photodetector according to claim 30 further including a substrate and wherein said cathode, absorbing and anode regions are formed above the substrate and said photodetector is configured to receive said source signal from directions facing a side of the photodetector opposite of said substrate.

35. A photodetector according to claim 34 wherein said anode region comprises a silicon P layer.

36. A photodetector according to claim 30 wherein said photodector is an avalanche photodiode and further comprises a multiplication region formed of silicon.

37. A photodetector according to claim 36 wherein said anode region comprises a germanium P layer formed by an epitaxial lateral overgrowth process.

38. A photodetector according to claim 36 wherein said avalanche photodiode is configured to detect said source signal at a data bandwidth of greater than 1 gigabit per second, at source signal wavelengths of 1750 nanometers or shorter, and having a gain of greater than 2.

39. A photodetector according to claim 36 wherein at least one germanium layer is grown epitaxiallly on a silicon layer.

40. A photodetector according to claim 1 wherein said microstructure-enhanced photon absorbing semiconductor region and said microstructures are at least partially formed of a III-V family material.

41. A photodetector according to claim 40 wherein said III-V family material is selected from a group consisting of: InP, GaAs, InGaAs, GaN, InGaN, InGaAsP, AlGaAs, AlGaN, GaP, InSb and InAs.

42. A photodetector according to claim 40 wherein said III-V family material is formed using a selective area growth process.

43. A photodetector according to claim 40 wherein said photodector is an avalanche photodiode and further comprises a multiplication region formed of silicon.

44. A photodetector according to claim 1 wherein said plurality of microstructures include voids buried within the absorbing semiconductor region.

45. A photodetector according to claim 44 wherein the absorbing semiconductor region is made of a material selected from a group consisting of silicon and germanium.

46. A photodetector according to claim 1 further comprising a plurality of voids buried in a layer of material effectively lowering a refractive index at said

range of wavelengths and lowering capacitance of said layer of material compared to the material when free of intentional voids.

47. A photodetector according to claim 46 wherein said layer of material is an N layer formed on a substrate material.

48. A photodetector according to claim 46 wherein said photodetector is an avalanche photodiode and said layer of material forms a multiplication layer of the avalanche photo diode.

49. A photodetector according to claim 46 wherein said plurality of voids are filed with a material selected from a group consisting: nitrogen, argon, polymer, amorphous semiconductor material, and glass.

50. A photovoltaic device comprising a semiconductor material having a plurality of voids buried therein, the semiconductor material configured to convert solar radiation into direct current electricity.

51. A device according to claim 50 wherein said plurality of voids are microstructured voids configured to enhance absorption of said semiconductor material to thereby increase conversion efficiency of the device compared with the material when free of intentional microstructured voids.

52. A device according to claim 50 wherein said plurality of voids are sized and/or spaced apart by less than 3 microns, and are configured to alter an effective refractive index of the semiconductor material near a surface of the semiconductor material to reduce reflection of incident sunlight from the device compared with an otherwise same device.

53. A device according to claim 50 wherein said plurality of microstructured voids are sized and/or spaced apart by less than 3 microns, and are configured to alter an effective refractive index of the semiconductor material

near a surface of the semiconductor material to increase internal reflection within the semiconductor material compared to an otherwise same device.

54. A glass material comprising a glass having a plurality of buried voids dimensioned between 0.01 microns to 1000 microns.

55. A glass material according to claim 54 wherein the material forms a part of a photovoltaic device.

56. A glass material according to claim 54 wherein said buried voids are filled with a material selected from a group consisting of: gel, polymer and gas.

57. A device according to claim 54 wherein said plurality of buried voids are configured to provide flexibility of the glass material.

58. A device according to claim 54 wherein said plurality of buried voids are configured to provide increased resistance of the glass material to physical damage and/or damage propagation compared to an otherwise same device.

59. A microwave transmission line structure comprising:
a semiconductor substrate material including a plurality of high-density dielectric-filled voids configured to reduce a dielectric constant of the semiconductor substrate material; and
a plurality of metallic microwave transmission lines, at least one of which is positioned above said semiconductor substrate material and is operatively associated therewith.

60. A structure according to claim 59 wherein said dielectric-filled voids are filled with one or more dielectric materials selected from a group consisting of: nitrogen, argon, vacuum, air, helium, polymer, metal oxides, silicon dioxide, silicon nitride, calcium fluoride, and zinc oxide.

61. A structure according to claim 59 wherein said voids are further configured to reduce dispersion and reduce loss associated with said microwave transmission lines at least in part by reducing current loop flow and/or eddy currents compared to an otherwise same structure.

62. A structure according to claim 59 wherein said plurality of metallic microwave transmission lines are arranged in a manner selected from a group consisting of: coplanar, microstrip, slotline, and stripline.

63. An optical waveguide structure comprising:
an optical mode region; and
a supporting semiconductor material adjacent to said optical mode region, wherein said supporting material includes a plurality of microstructured voids formed therein that are configured to alter an effective index of refraction of said supporting material.

64. An optical waveguide structure according to claim 63 wherein said effective index of refraction depends on a density of the plurality of microstructured voids.

65. An optical waveguide structure according to claim 63 wherein said optical mode region is formed into a ridge supported by said supporting semiconductor material.

66. An optical waveguide structure according to claim 63 wherein said optical mode region is surrounded by said supporting semiconductor material.

67. An optical waveguide structure according to claim 63 wherein said optical mode region includes a second plurality of microstructured voids formed therein that are configured to alter an effective index of refraction of said optical mode region.

68. A heat exchanger system comprising:

a heat generating device;

a heat sink configured to dissipate heat to a surrounding medium; and

an intermediate material mounted between said heat generating device and said heat sink, the intermediate material including a plurality of buried voids configured to alter thermal conductivity of said intermediate material.

69. A heat exchanger according to claim 68 wherein a first portion of said buried voids are filled with thermally conductive material and a second portion of said buried voids are filled with a thermally isolating material, the first and second portions being positioned to conduct heat from said heat generating device to said heat sink and to reduce thermal cross talk with other heat sensitive devices mounted on said intermediate material.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Attorney Docket Number:	309-0011USDIVCIP2

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY FILING FEE (ELECTRONIC FILING)	4011	1	80	80
UTILITY SEARCH FEE	2111	1	350	350
UTILITY EXAMINATION FEE	2311	1	400	400
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	2202	10	50	500
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	1330

PTO/AIA/15 (10-17)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	309-0011USDIVCIP2
First Named Inventor	Shih-Yuan WANG
Title	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
Priority Mail Express® Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [✔] **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. [✔] **Applicant asserts small entity status.** See 37 CFR 1.27
3. [ ] **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. [✔] **Specification** [*Total Pages* 92] Both the claims and abstract must start on a new page. *(See MPEP § 608.01(a) for information on the preferred arrangement)*
5. [✔] **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 47]
6. **Inventor's Oath or Declaration** [*Total Pages* 2] *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   - a. [ ] Newly executed (original or copy)
   - b. [✔] A copy from a prior application (37 CFR 1.63(d))
7. [✔] **Application Data Sheet** ** See note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R** in duplicate, large table, or Computer Program (*Appendix*)
   - [ ] Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** (*if applicable, items a. – c. are required*)
   - a. [ ] Computer Readable Form (CRF)
   - b. [ ] Specification Sequence Listing on:
     - i. [ ] CD-ROM or CD-R (2 copies); or
     - ii. [ ] Paper
   - c. [ ] Statements verifying identity of above copies

ADDRESS TO:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ACCOMPANYING APPLICATION PAPERS

10. [ ] **Assignment Papers** (cover sheet & document(s))
    Name of Assignee _____
11. [ ] **37 CFR 3.73(c) Statement** (*when there is an assignee*) [✔] **Power of Attorney**
12. [ ] **English Translation Document** (*if applicable*)
13. [ ] **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    - [ ] Copies of citations attached
14. [✔] **Preliminary Amendment**
15. [ ] **Return Receipt Postcard** (*MPEP § 503*) (*Should be specifically itemized*)
16. [ ] **Certified Copy of Priority Document(s)** (*if foreign priority is claimed*)
17. [ ] **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. [ ] **Other:** _____

*__Note__: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS

[✔] The address associated with Customer Number: 139982 **OR** [ ] Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone		Email	

Signature	/Ivan S. Kavrukov/	Date	March 29, 2022
Name (Print/Type)	Ivan S. Kavrukov	Registration No. (Attorney/Agent)	25,161

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/17 (10-20)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

FEE TRANSMITTAL

Complete if known	
Application Number	n/a
Filing Date	TBD
First Named Inventor	Shih-Yuan WANG
Examiner Name	n/a
Art Unit	n/a
Practitioner Docket No.	309-0011USDIVCIP2

☒ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

TOTAL AMOUNT OF PAYMENT ($) 1,330.00

METHOD OF PAYMENT (check all that apply)

☐ Check ☒ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 600125 Deposit Account Name: Wissing Miller LLP

For the above-identified deposit account, the Director is hereby authorized to (check all that apply):

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayment of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayment of fee(s)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES (U = undiscounted fee; S = small entity fee; M = micro entity fee)

	FILING FEES			SEARCH FEES			EXAMINATION FEES			
Application Type	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**U ($)**	**S ($)**	**M ($)**	**Fees Paid ($)**
Utility	320	160*	80	700	350	175	800	400	200	830.00
Design	220	110	55	160	80	40	640	320	160	
Plant	220	110	55	440	220	110	660	330	165	
Reissue	320	160	80	700	350	175	2,320	1,160	580	
Provisional	300	150	75	0	0	0	0	0	0	

* The $160 small entity status filing fee for a utility application is further reduced to $80 for a small entity status applicant who files the application via EFS-Web.

2. EXCESS CLAIM FEES

Fee Description	**Undiscounted Fee ($)**	**Small Entity Fee ($)**	**Micro Entity Fee ($)**
Each claim over 20 (including Reissues)	100	50	25
Each independent claim over 3 (including Reissues)	480	240	120
Multiple dependent claims	860	430	215

Total Claims		**Extra Claims**	**Fee ($)**		**Fee Paid ($)**
30	-20 or HP =	10	x 50.00	=	500.00

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		**Extra Claims**	**Fee ($)**		**Fee Paid ($)**
3	-3 or HP =	0	x 0	=	0

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	**Fee ($)**	**Fee Paid ($)**

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $420 ($210 for small entity) ($105 for micro entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		**Extra Sheets**		**Number of each additional 50 or fraction thereof**		**Fee ($)**		**Fee Paid ($)**
92	- 100 =	0	/ 50 =	0	(round **up** to a whole number) x	0	=	0

4. OTHER FEE(S) **Fees Paid ($)**

Non-English specification, $140 fee ($70 for small entity) ($35 for micro entity) _____

Non-electronic filing fee under 37 CFR 1.16(t) for a utility application, $400 fee ($200 small or micro entity) _____

Other (e.g., late filing surcharge): _____ _____

SUBMITTED BY

Signature	/Ivan S. Kavrukov/	Registration No. (Attorney/Agent) 25,161	Telephone 917-945-0121
Name (Print/Type)	Ivan S. Kavrukov		Date March 29, 2022

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	45346476
Application Number:	17707429
International Application Number:	
Confirmation Number:	1214
Title of Invention:	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
First Named Inventor/Applicant Name:	Shih-Yuan WANG
Customer Number:	139982
Filer:	Ivan Kavrukov/Mary Ellen Finnegan
Filer Authorized By:	Ivan Kavrukov
Attorney Docket Number:	309-0011USDIVCIP2
Receipt Date:	29-MAR-2022
Filing Date:	
Time Stamp:	16:35:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1330
RAM confirmation Number	E20223SG35460719
Deposit Account	600125
Authorized User	Mary Ellen Finnegan

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	309-0011USDIVCIP2_TransmittalPOA_Signed.pdf	603357 38391801fef2bc979678738021617b9fc909d1e3	no	2
Warnings:					
Information:					
2	Oath or Declaration filed	309-0011USDIVCIP2_Declaration_ShihYuanWang-signed.pdf	186616 85ee35e434cd05e0ceb23a12a1cb1b102f4e20f3	no	2
Warnings:					
Information:					
3	Oath or Declaration filed	309-0011USDIVCIP2_Declaration_SPBobWang-signed.pdf	406296 33b8b45774e0caa54890b3d09dacc8233f672d5c	no	1
Warnings:					
Information:					
4	Specification	309-0011USDIVCIP2_SpecificationFINAL-03-29-2022.pdf	852781 af05e665002904d5284e07eebb5bd0a9654d517a	no	92
Warnings:					
Information:					
5	Drawings-only black and white line drawings	309-0011USDIVCIP2_Figures.pdf	3390412 8872a39764be24131d29260f72388019c43e349b	no	47
Warnings:					
Information:					
6	Transmittal of New Application	309-0011USDIVCIP2_TransmittalForm_Signed.pdf	354334 b9d7be0ffecc66594b49adcc681339a0a59ac62a	no	2
Warnings:					
Information:					

7	Transmittal Letter	309-0011USDIVCIP2_FeeTransmittal_signed.pdf	243008 60795b51197b8a5ab247598429bb335db04338c5	no	2
Warnings:					
Information:					
8	Application Data Sheet	309-0011USDIVCIP2_ADS_FINAL.pdf	1819931 c847bd6c02ebb5e4e81eec0dd131f51db5a185be	no	8
Warnings:					
Information:					
9	Fee Worksheet (SB06)	fee-info.pdf	46561 80ce05c941c8723eb149850f923e44f481b0c9cd	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	7903296	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shih-Yuan		WANG	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Palo Alto	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	766 Encina Grande Dr.		
Address 2			
City	Palo Alto	State/Province	CA
Postal Code	94306	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Shih-Ping		WANG	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	Los Altos	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	38 3rd Street, Suite #307		
Address 2			
City	Los Altos	State/Province	CA
Postal Code	94022	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	23432		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES		
Attorney Docket Number	309-0011USDIVCIP2	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	47	**Suggested Figure for Publication (if any)**	5B

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	23432		

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the application number blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Division of	17532831	2021-11-22
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
17532831	Continuation in part of	17182954	2021-02-23
Prior Application Status	Patented		Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17182954	Division of	16528958	2019-08-01	11121271	2021-09-04

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16528958	Continuation in part of	15797821	2017-10-30	10446700	2019-10-15

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15797821	Continuation of	14947718	2015-11-20	10622498	2020-04-14

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
14947718	Continuation of	PCT/US14/39208	2014-05-22
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61826446	2013-05-05
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61834873	2013-06-13
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61834021	2013-07-04
Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
PCT/US14/39208	Claims benefit of provisional	61905109	2013-11-15

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	W&WSENS DEVICES, INC.		
Mailing Address Information For Applicant:			
Address 1	38 THIRD STREET		
Address 2	SUITE 307		
City	LOS ALTOS	**State/Province**	CA
Country	US	Postal Code	94022
Phone Number		Fax Number	

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

Email Address	

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication . An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/Ivan S. Kavrukov/			Date (YYYY-MM-DD)	2022-03-29
First Name	Ivan	Last Name	Kavrukov	Registration Number	25161

Additional Signature may be generated within this form by selecting the Add button. Add

PTO/AIA/14 (07-14)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	309-0011USDIVCIP2
	Application Number	
Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent C o o p eration Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/01 (06-12)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [■] The attached application, or
- [ ] United States application or PCT international application number _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Shih-Yuan Wang Date (Optional) : _____

Signature: Shih-Yuan Wang 11/22/2021

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

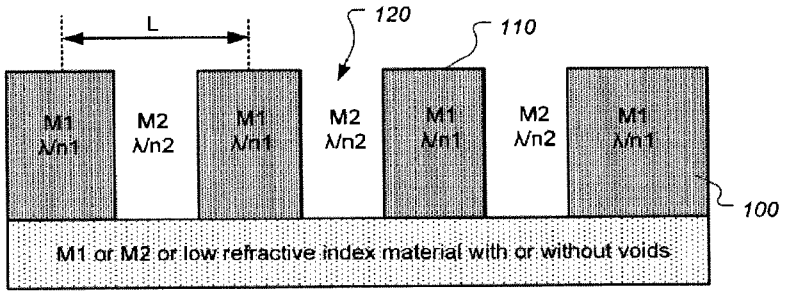


FIG. 1

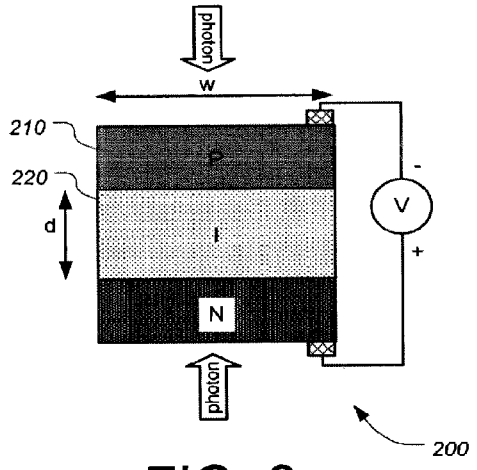


FIG. 2
(prior art)

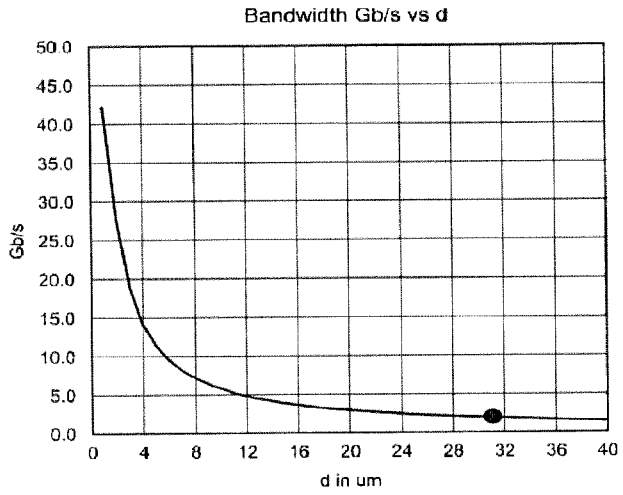


FIG. 3A
(prior art)

310

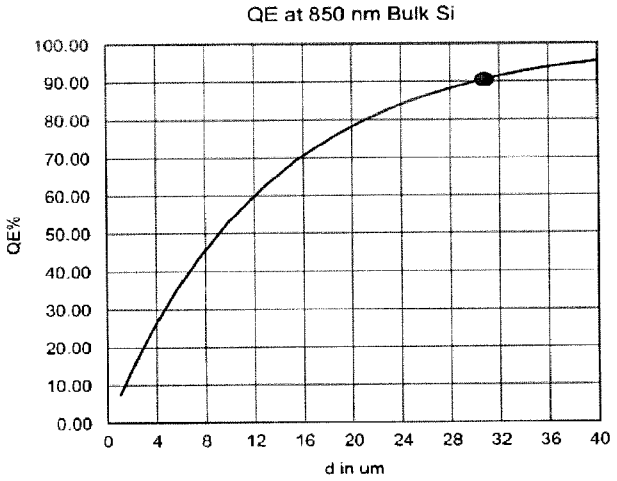


FIG. 3B
(prior art)

312

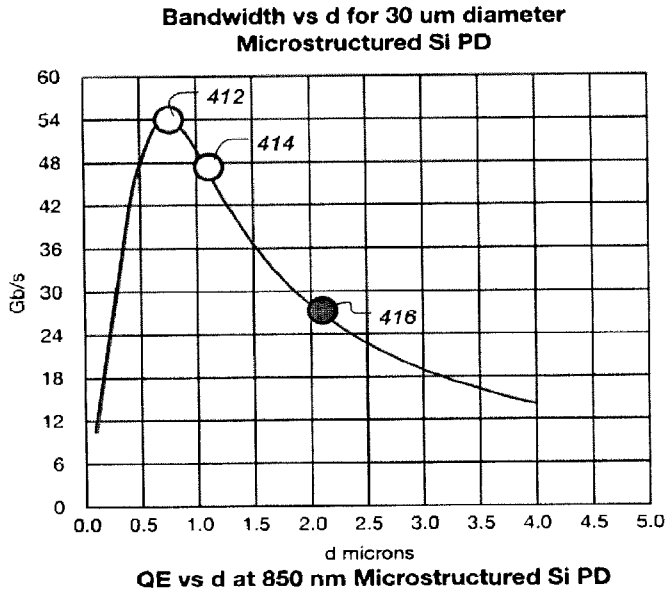


FIG. 4A

410

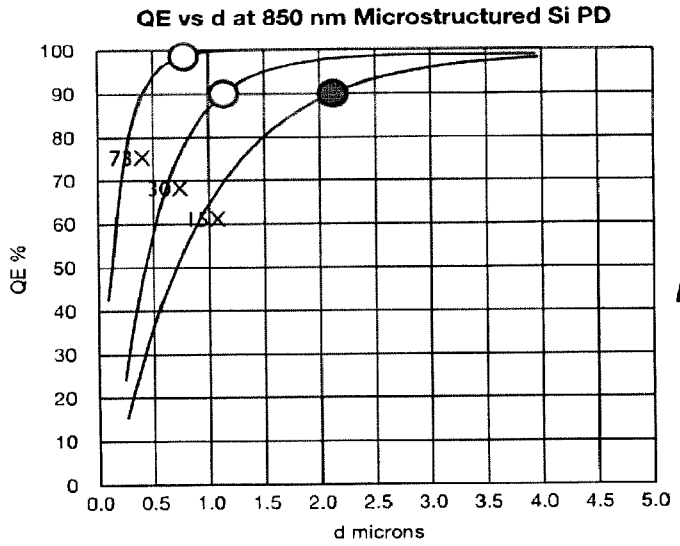


FIG. 4B

420

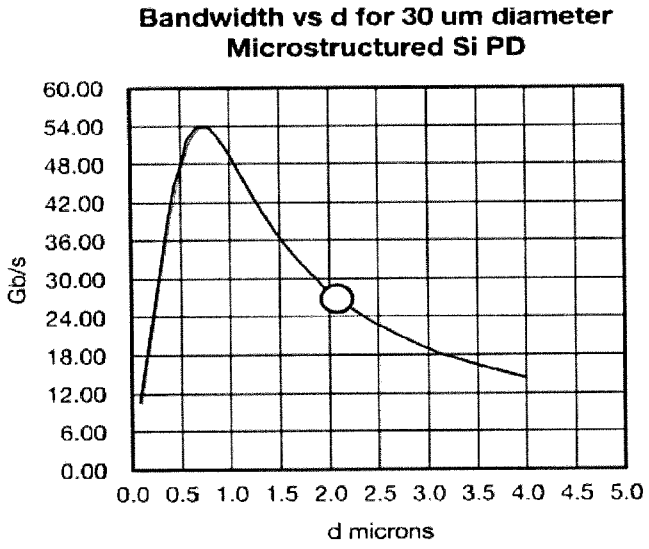


FIG. 4C

430

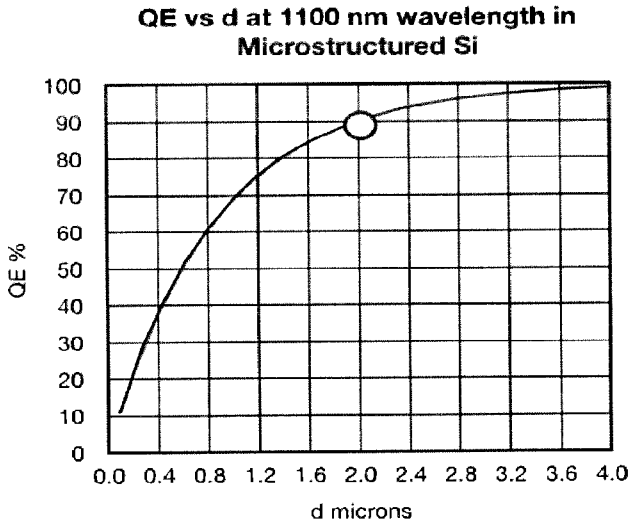


FIG. 4D

440

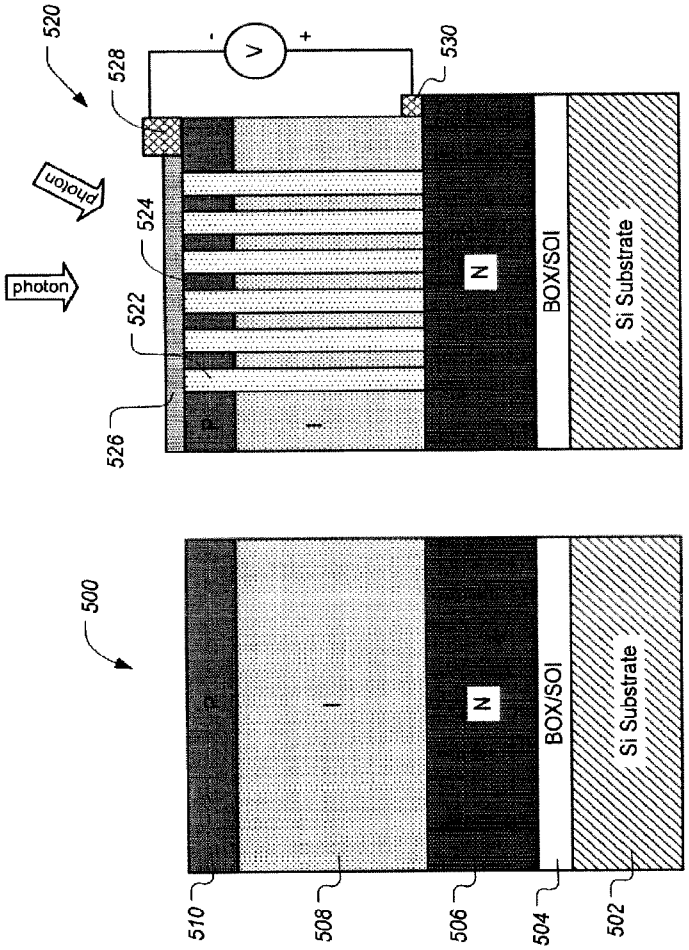

520
528
530
V
-
+
photon
photon
524
522
526
P
I
N
BOX/SOI
Si Substrate

FIG. 5B

500
P
I
N
BOX/SOI
Si Substrate
510
508
506
504
502

FIG. 5A

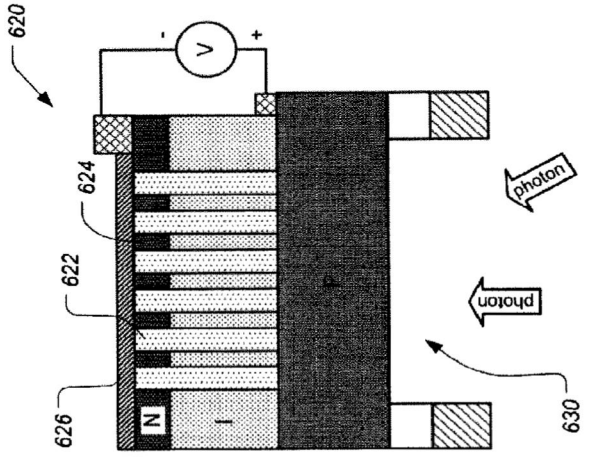

620
V
-
+
624
622
626
N
I
P
photon
photon
630

FIG. 6B

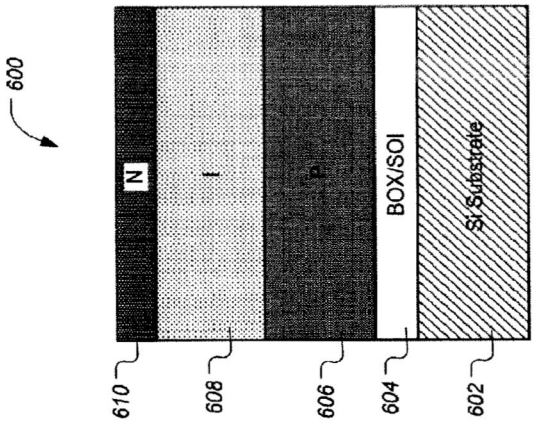

600
N
I
P
BOX/SOI
Si Substrate
610
608
606
604
602

FIG. 6A

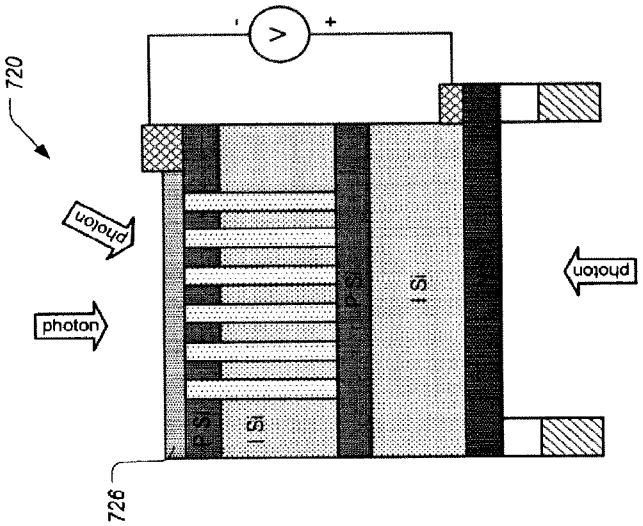

720
-
+
photon
photon
photon
p Si
i Si
n Si
726

FIG. 7B

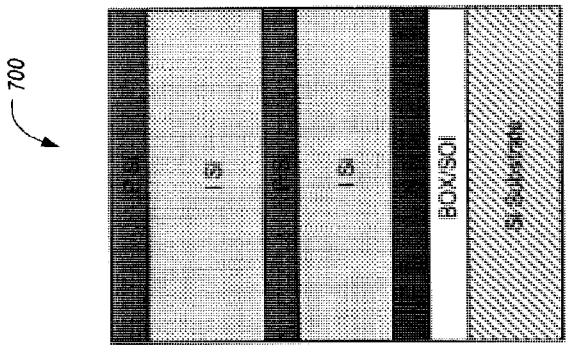

700
p Si
i Si
n Si
i Si
BOX/SOI
Si substrate

FIG. 7A

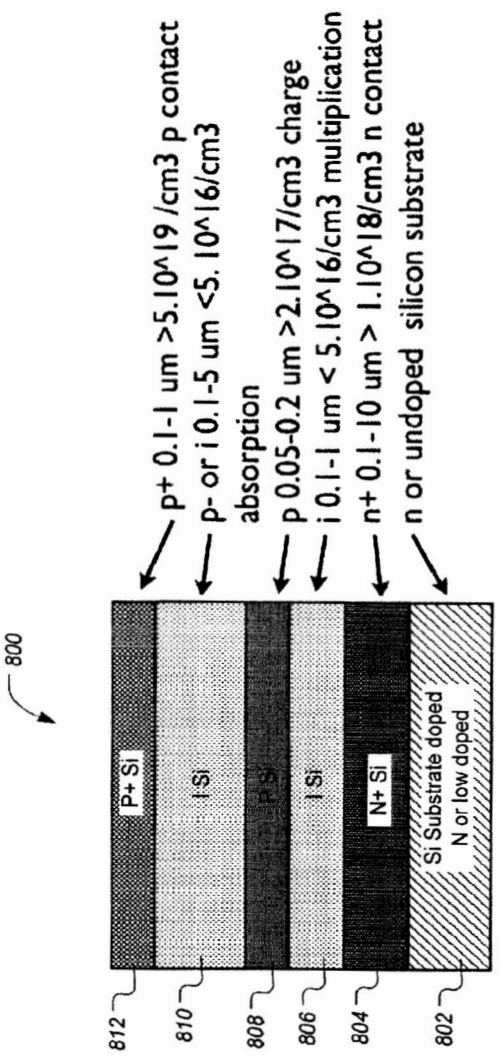

800
P+ Si
I Si
P Si
I Si
N+ Si
Si Substrate doped
N or low doped
812
810
808
806
804
802
p+ 0.1-1 um >5.10^19 /cm3 p contact
p- or i 0.1-5 um <5. 10^16/cm3
absorption
p 0.05-0.2 um >2.10^17/cm3 charge
i 0.1-1 um < 5.10^16/cm3 multiplication
n+ 0.1-10 um > 1.10^18/cm3 n contact
n or undoped silicon substrate

FIG. 8

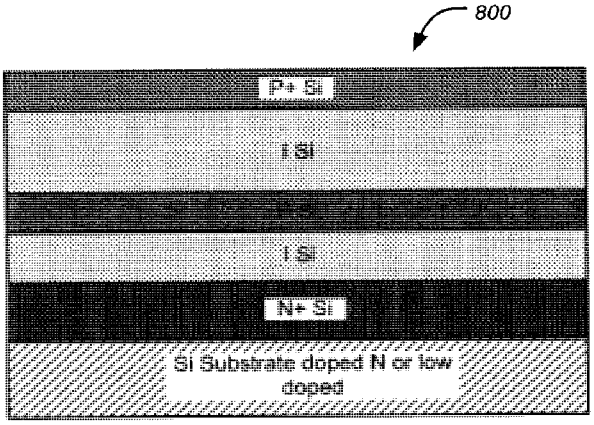

800
P+ Si
I Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9A

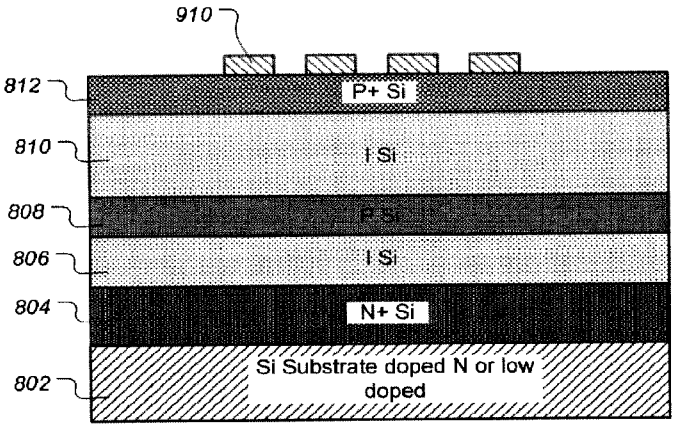

910
812
810
808
806
804
802
P+ Si
I Si
P Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9B

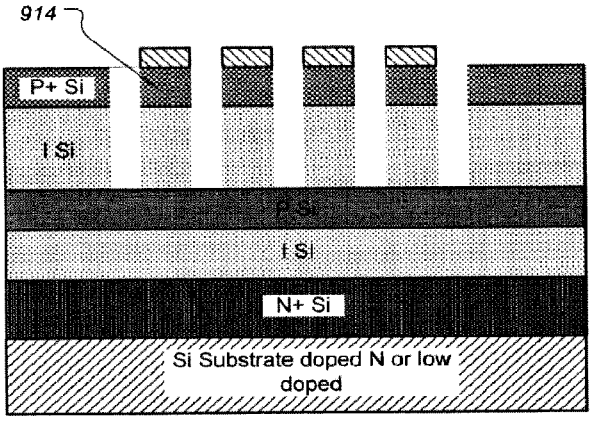

914
P+ Si
I Si
P Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9C

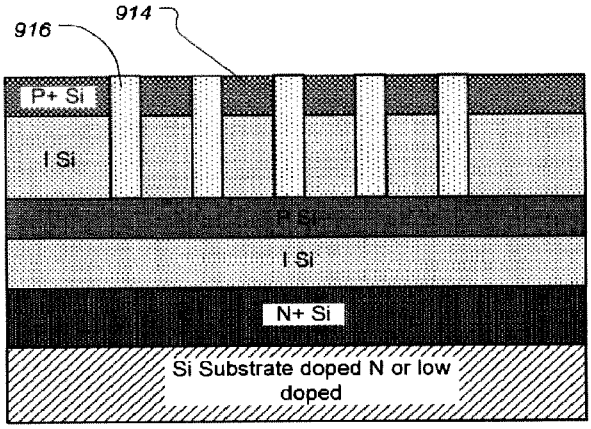

916
914
P+ Si
I Si
P Si
I Si
N+ Si
Si Substrate doped N or low doped

FIG. 9D

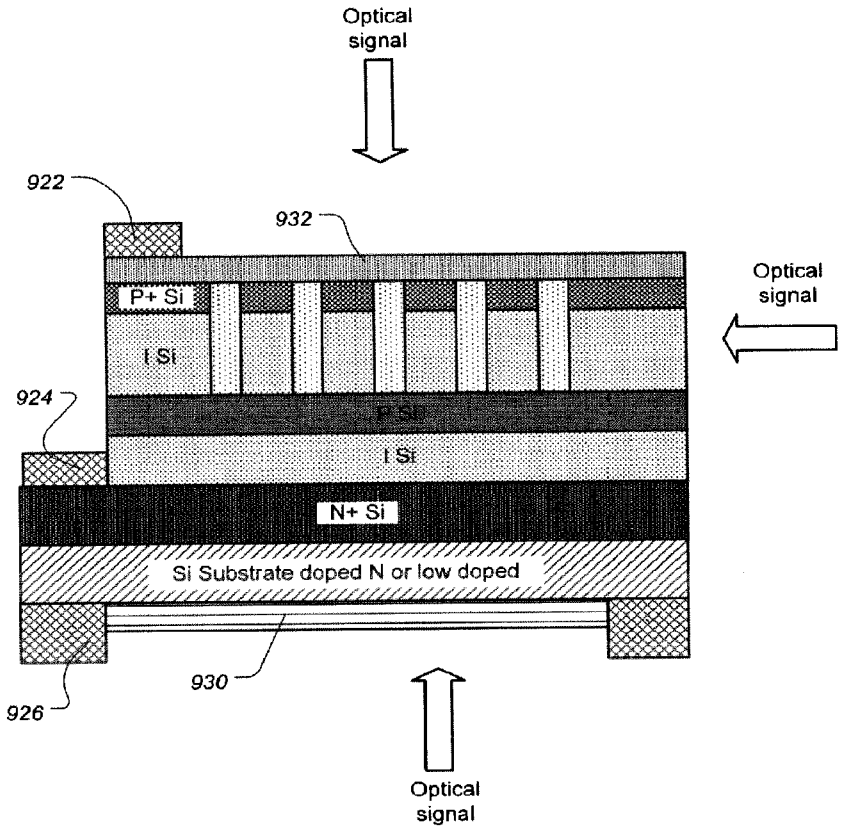

Optical signal
922
932
Optical signal
P+ Si
I Si
924
P Si
I Si
N+ Si
Si Substrate doped N or low doped
930
926
Optical signal

FIG. 9E

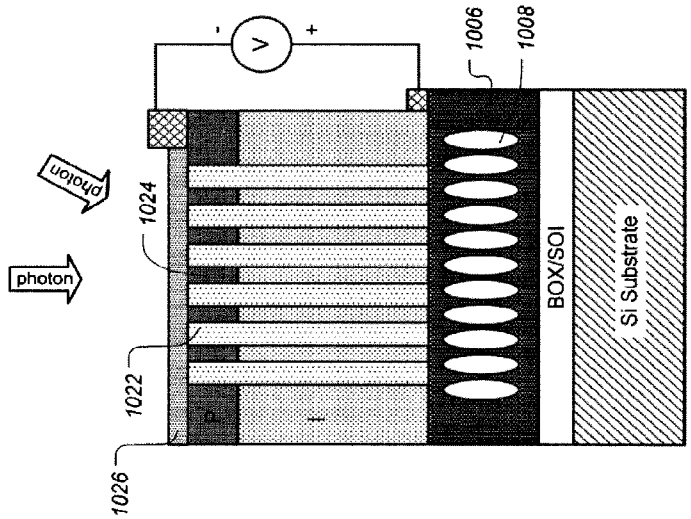


FIG. 10A

FIG. 10B

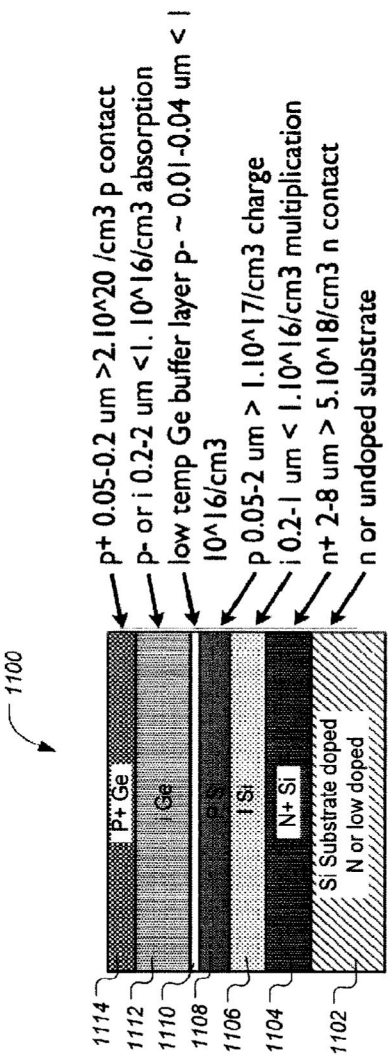

1100
P+ Ge
Ge
P Si
I Si
N+ Si
Si Substrate doped
N or low doped
p+ 0.05-0.2 um >2.10^20 /cm3 p contact
p- or i 0.2-2 um <1. 10^16/cm3 absorption
low temp Ge buffer layer p- ~ 0.01-0.04 um < 1
10^16/cm3
p 0.05-2 um > 1.10^17/cm3 charge
i 0.2-1 um < 1.10^16/cm3 multiplication
n+ 2-8 um > 5.10^18/cm3 n contact
n or undoped substrate
1114
1112
1110
1108
1106
1104
1102

FIG. 11A

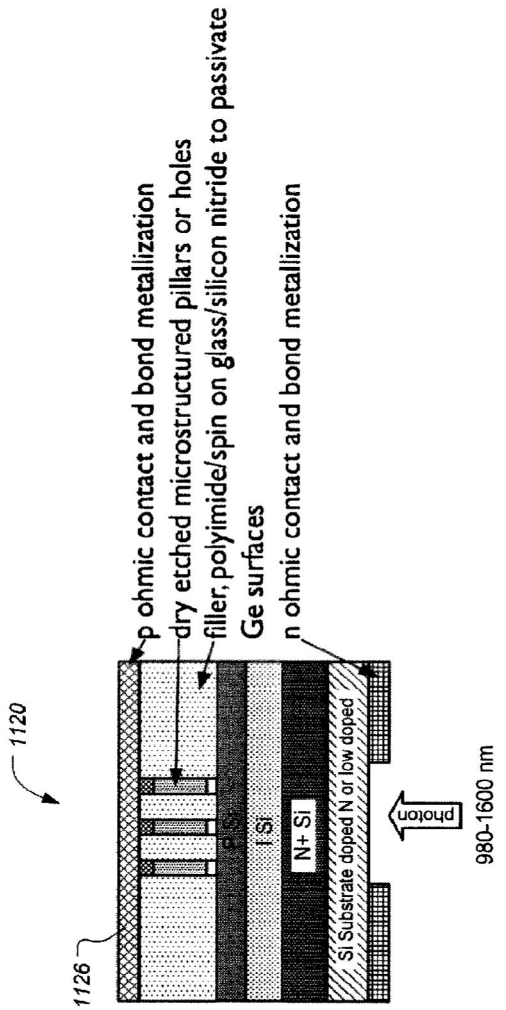

1120
1126
p ohmic contact and bond metallization
dry etched microstructured pillars or holes
filler, polyimide/spin on glass/silicon nitride to passivate
Ge surfaces
n ohmic contact and bond metallization
P+ Si
I Si
N+ Si
Si Substrate doped N or low doped
photon
980-1600 nm

FIG. 11B

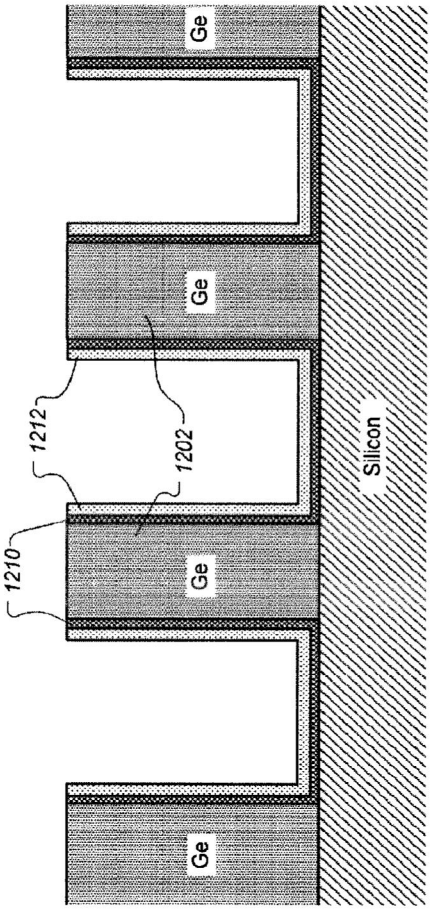


FIG. 12

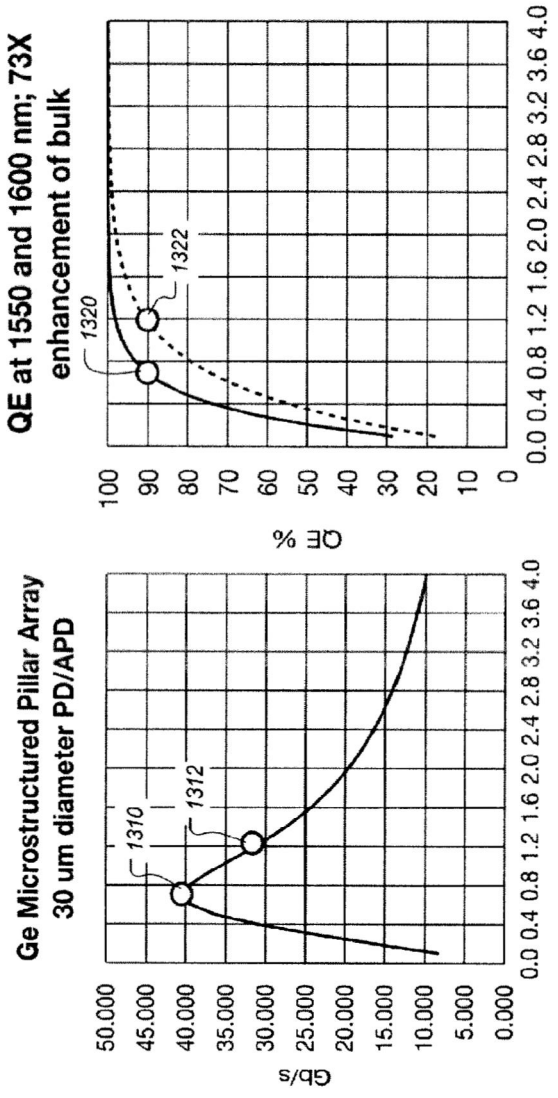


FIG. 13A

FIG. 13B

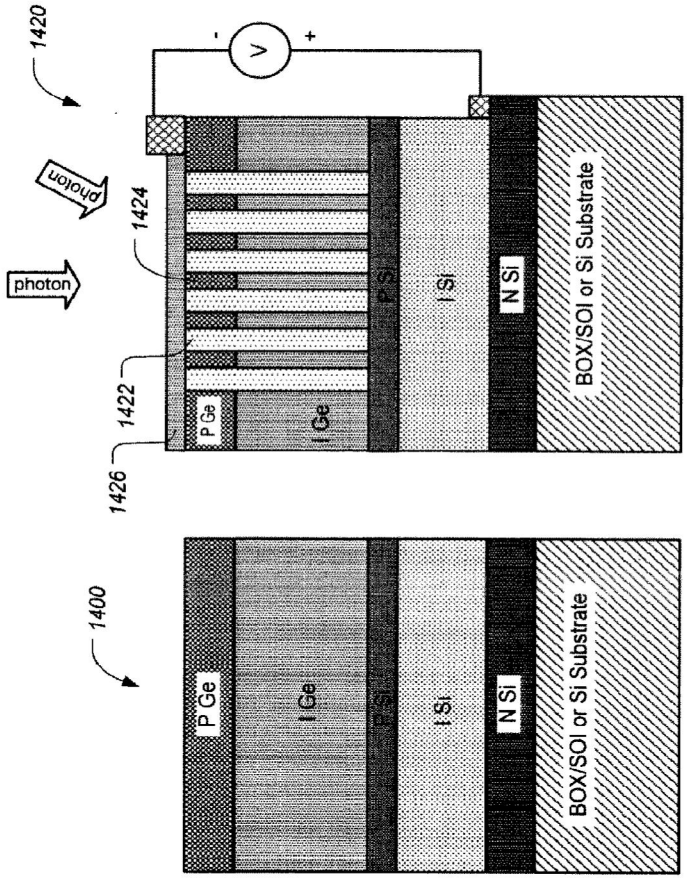


FIG. 14B

FIG. 14A

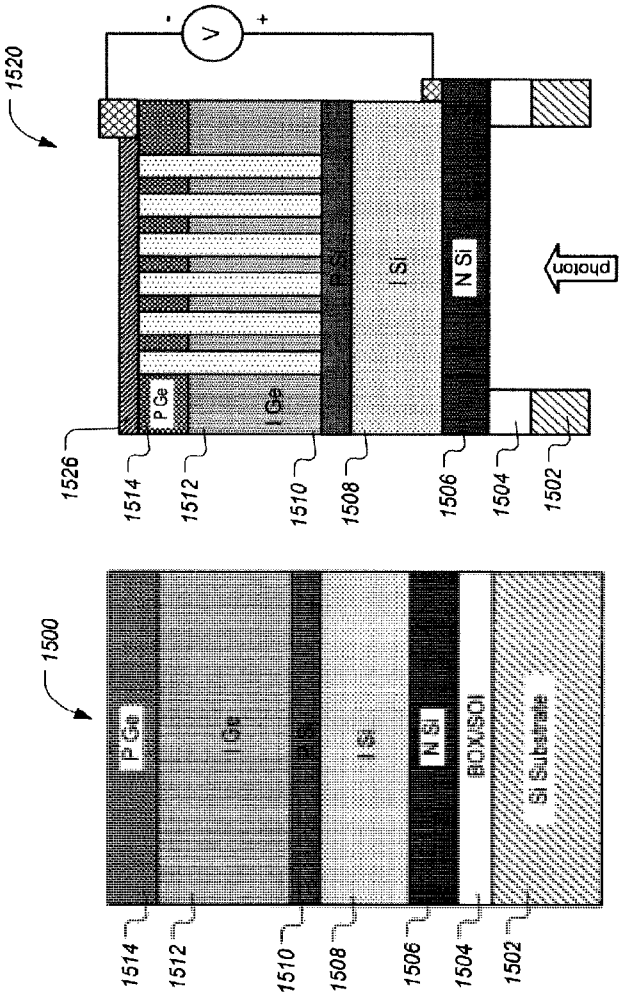


FIG. 15B

FIG. 15A

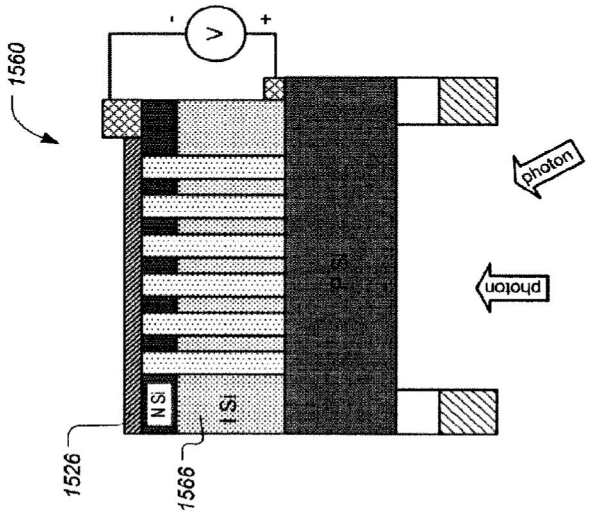


FIG. 15D

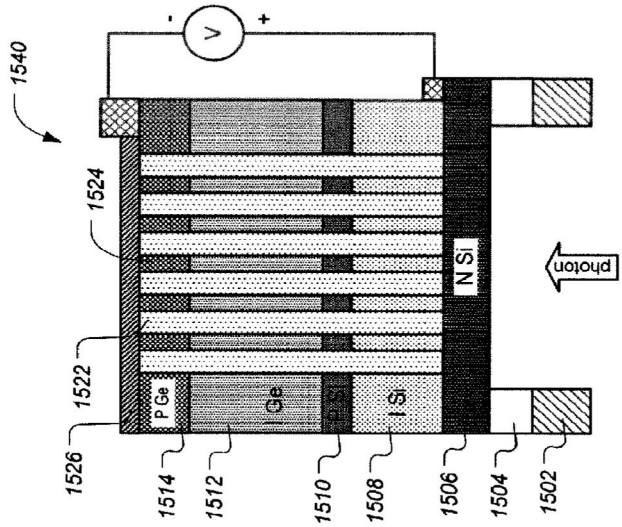


FIG. 15C

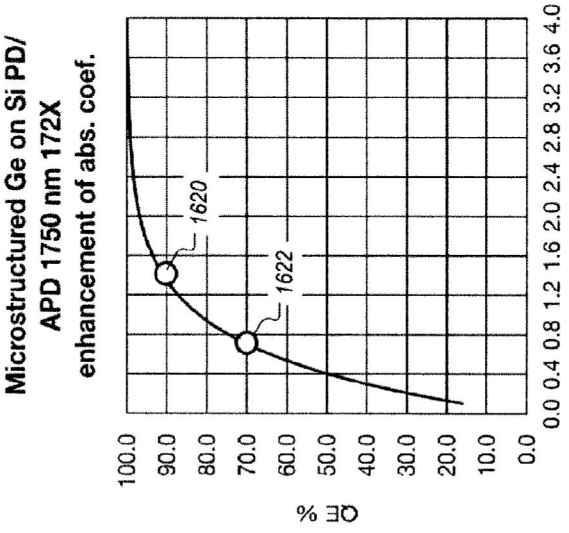


FIG. 16B

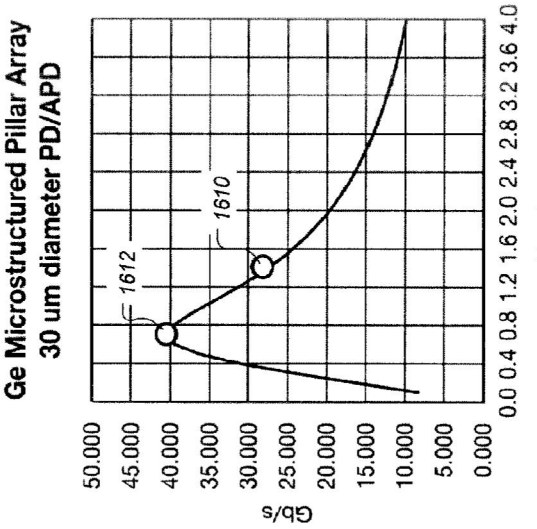


FIG. 16A

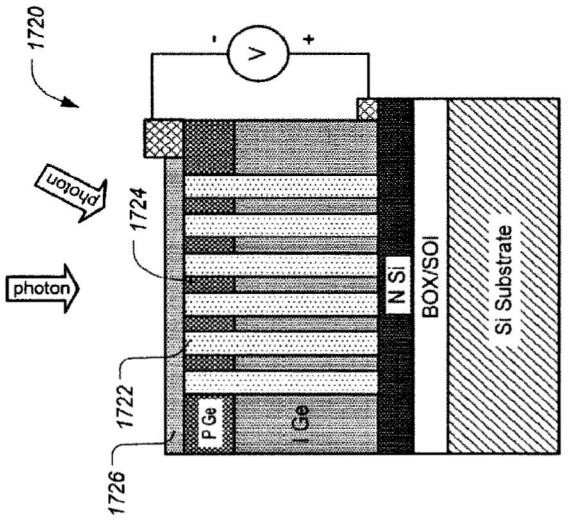


FIG. 17B

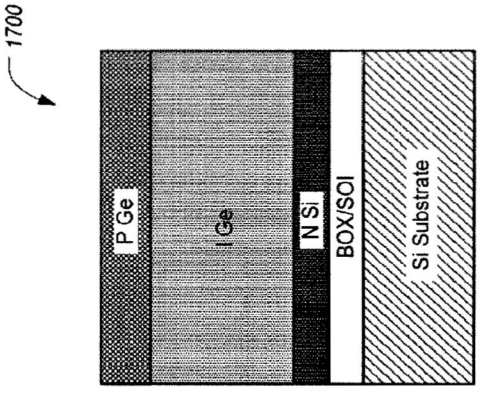


FIG. 17A

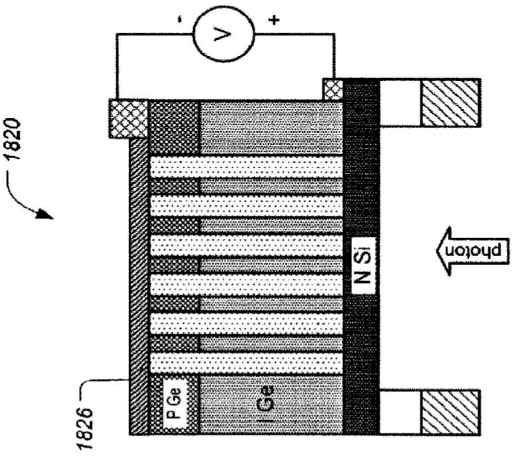


FIG. 18B

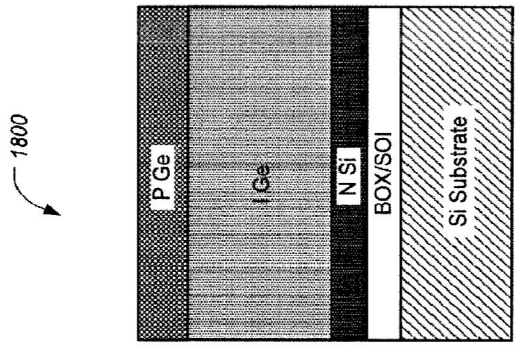


FIG. 18A

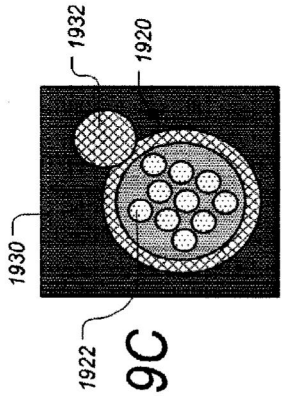


FIG. 19C

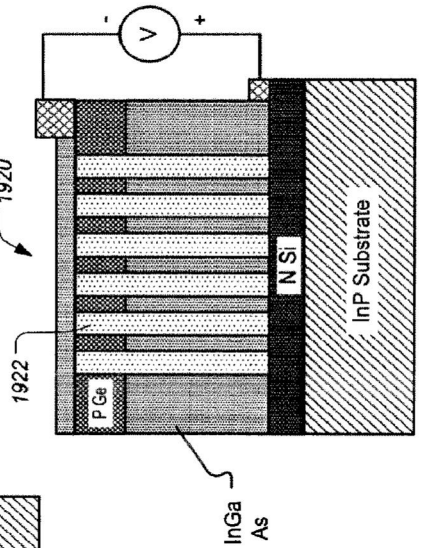


FIG. 19B

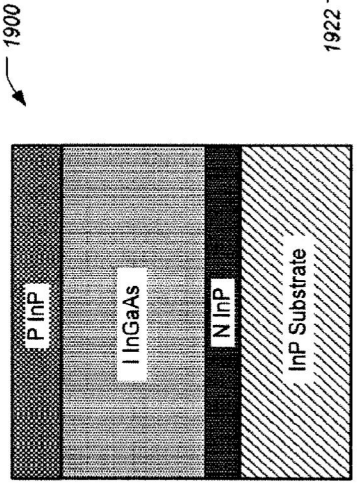


FIG. 19A

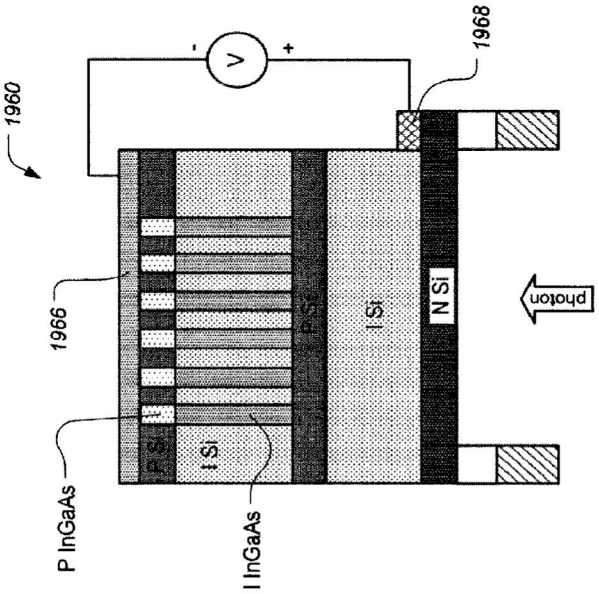


FIG. 19E

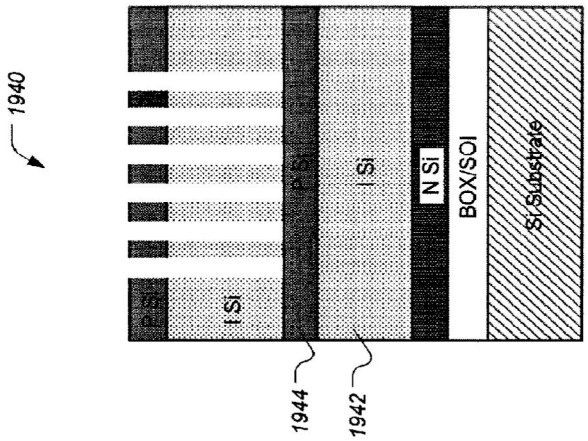


FIG. 19D

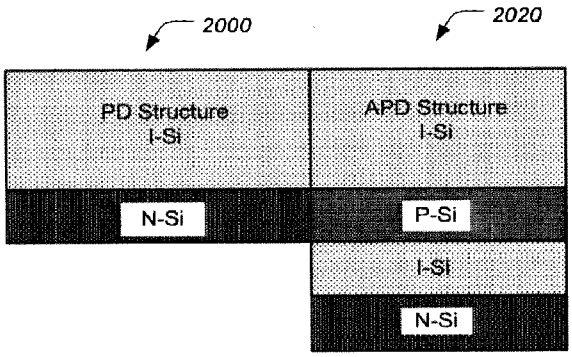

2000
2020
PD Structure
I-Si
APD Structure
I-Si
N-Si
P-Si
I-Si
N-Si

FIG. 20

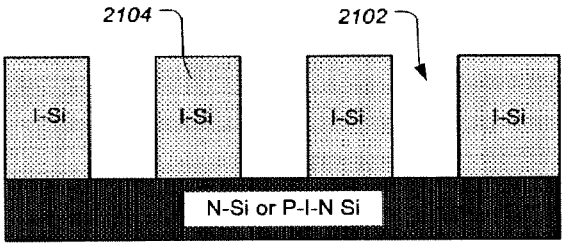

2104
2102
I-Si
I-Si
I-Si
I-Si
N-Si or P-I-N Si

FIG. 21

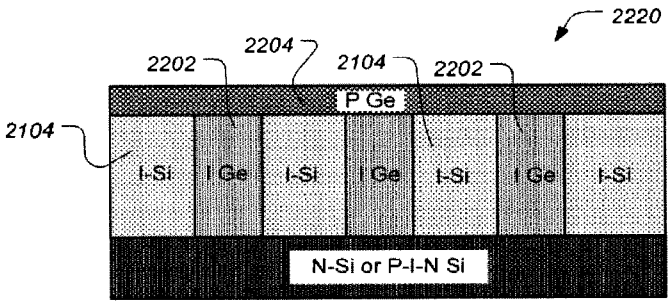

2220
2202
2204
2104
2202
P Ge
2104
I-Si
I Ge
I-Si
I Ge
I-Si
I Ge
I-Si
N-Si or P-I-N Si

FIG. 22

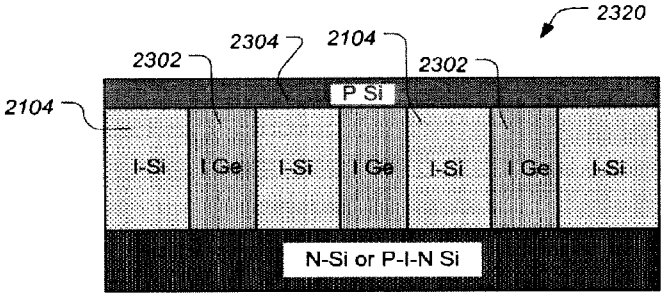

2320
2302
2304
2104
2302
P Si
2104
I-Si
I Ge
I-Si
I Ge
I-Si
I Ge
I-Si
N-Si or P-I-N Si

FIG. 23

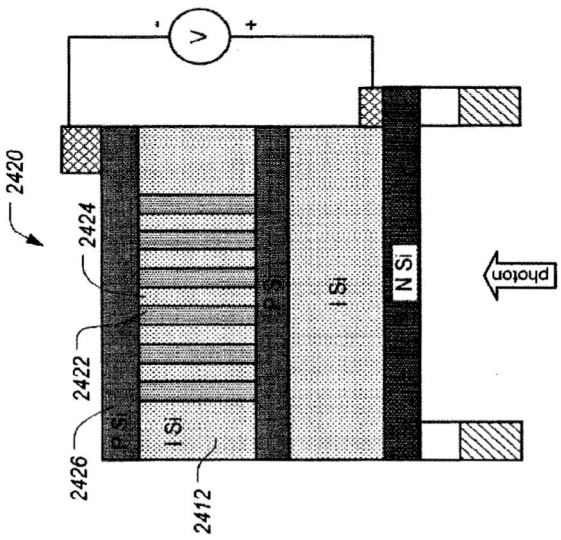


FIG. 24B

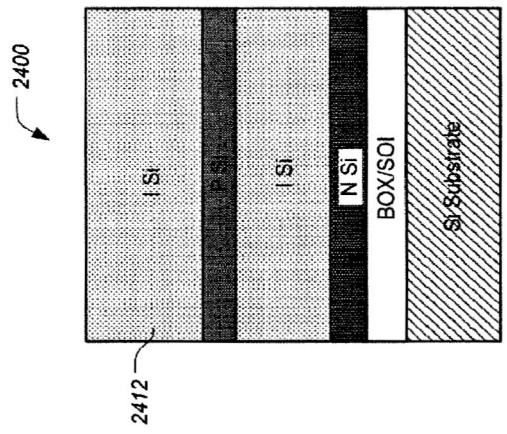


FIG. 24A

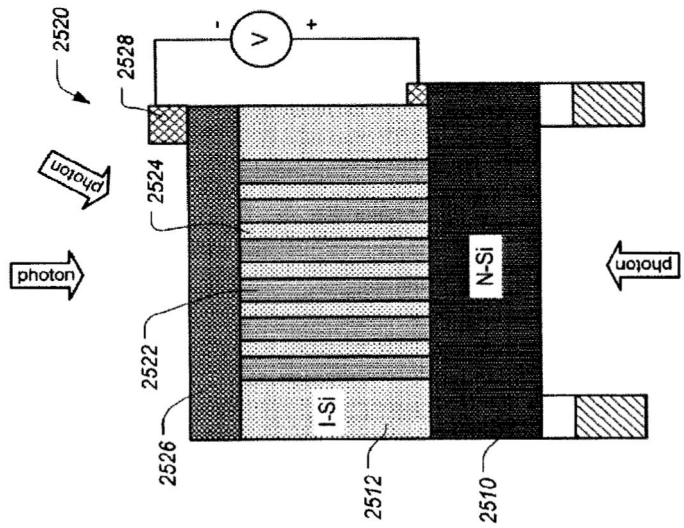


FIG. 25B

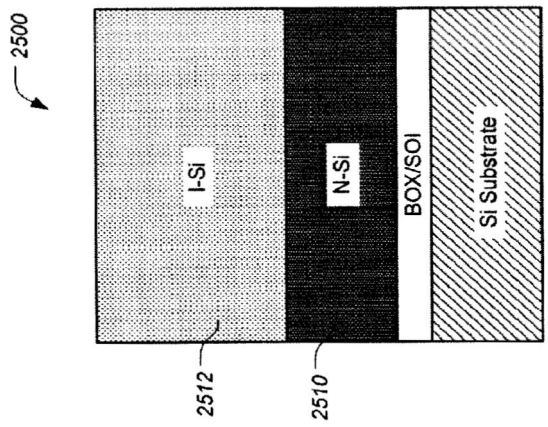


FIG. 25A

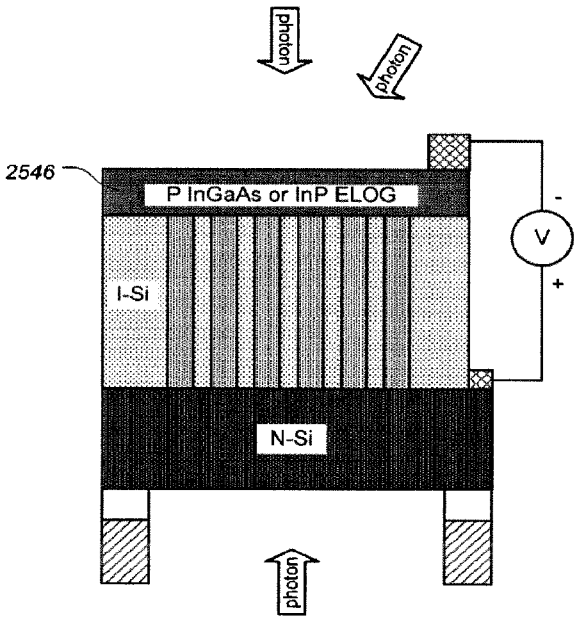


FIG. 25C

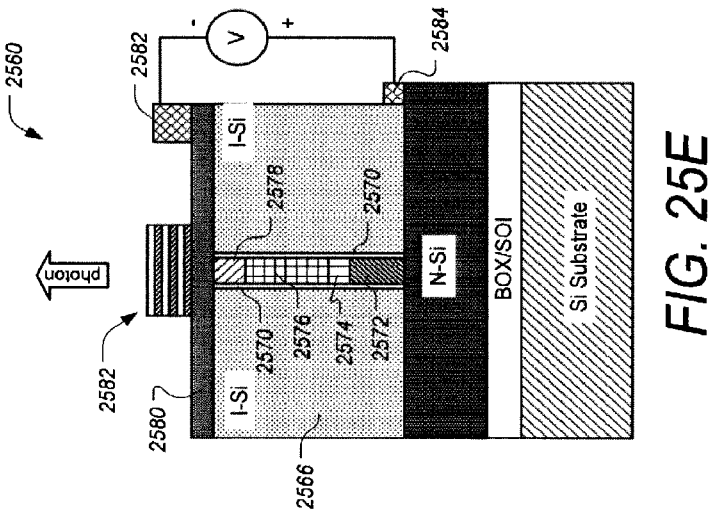


FIG. 25E

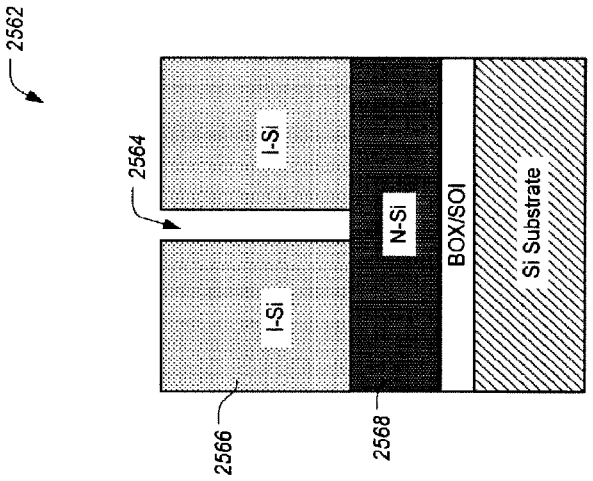


FIG. 25D

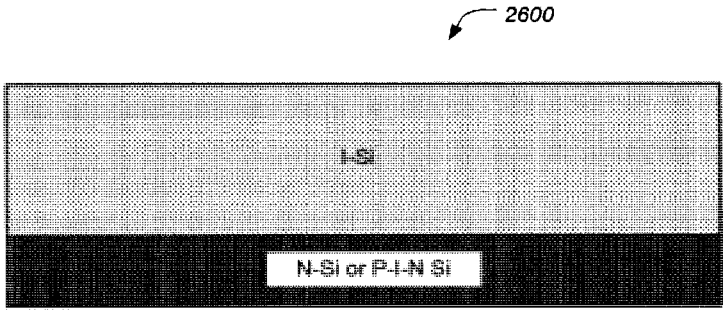


FIG. 26

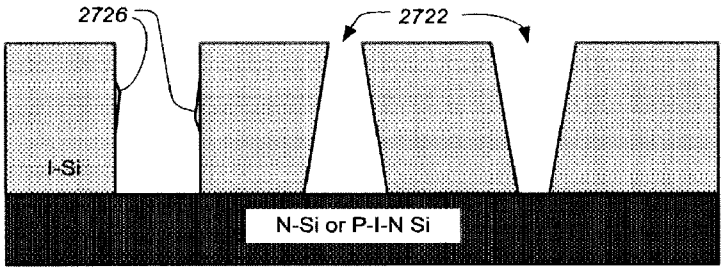


FIG. 27

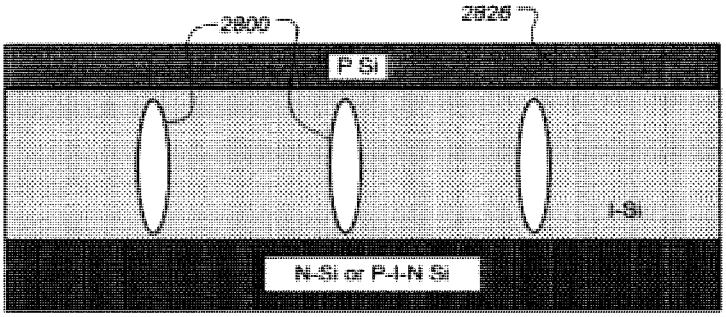

2800
2826
P Si
I-Si
N-Si or P-I-N Si

FIG. 28

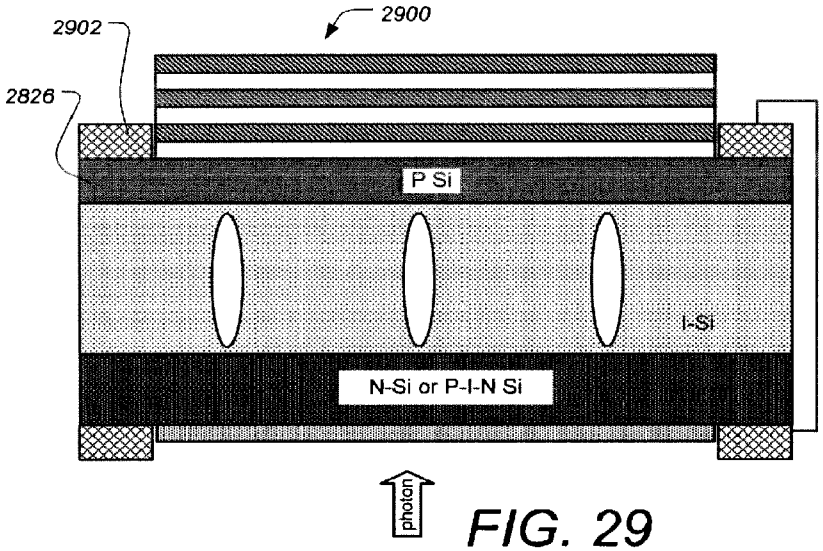

2902
2900
2826
P Si
I-Si
N-Si or P-I-N Si
photon

FIG. 29

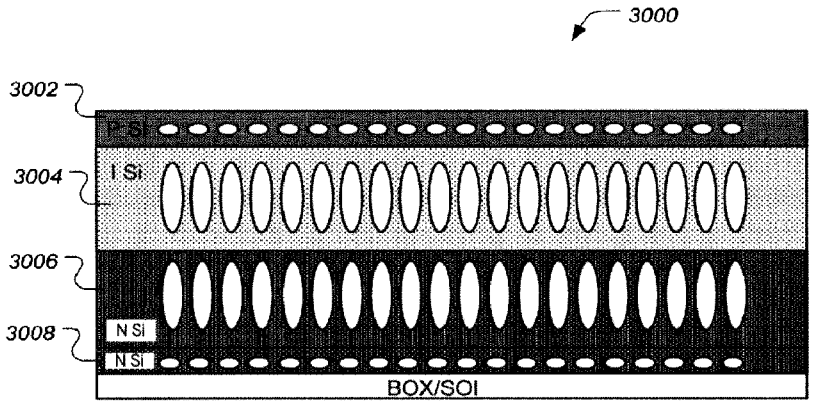

3000
3002
P Si
3004
I Si
3006
3008
N Si
N Si
BOX/SOI

FIG. 30

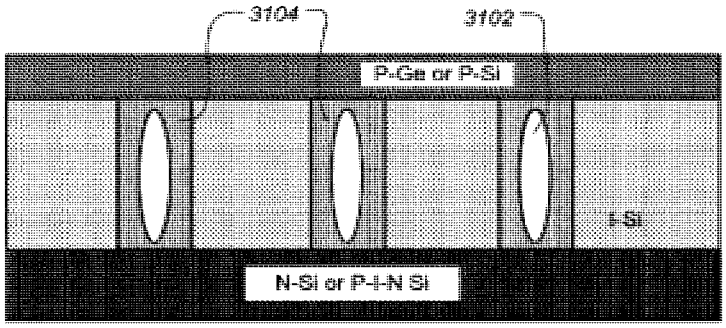

3104
3102
P-Ge or P-Si
I-Si
N-Si or P-I-N Si

FIG. 31

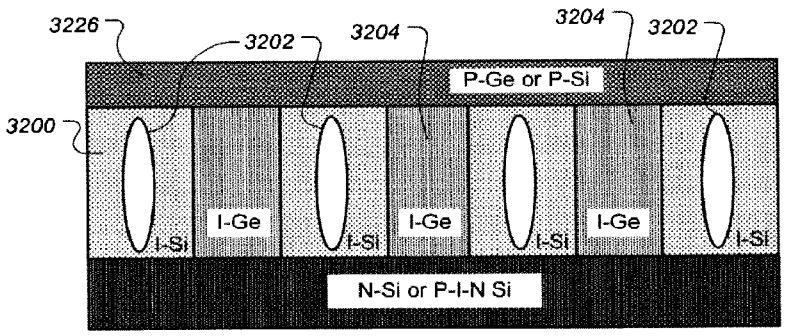

3226
3202
3204
3204
3202
3200
P-Ge or P-Si
I-Si
I-Ge
I-Si
I-Ge
I-Si
I-Ge
I-Si
N-Si or P-I-N Si

FIG. 32

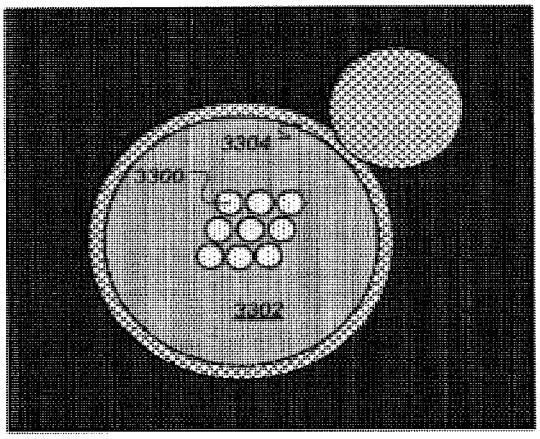

3204
3200
3202

FIG. 33

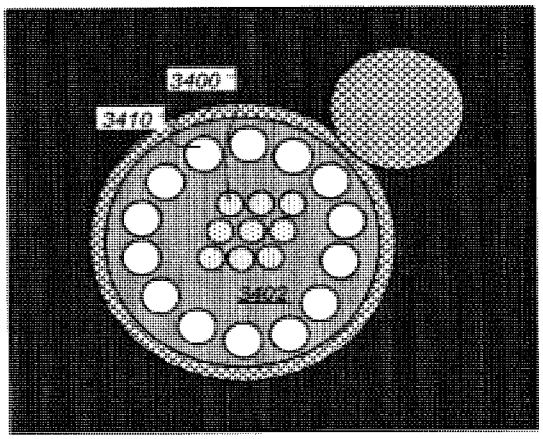


FIG. 34

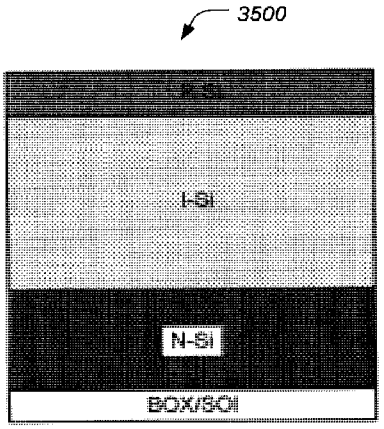


FIG. 35
(prior art)

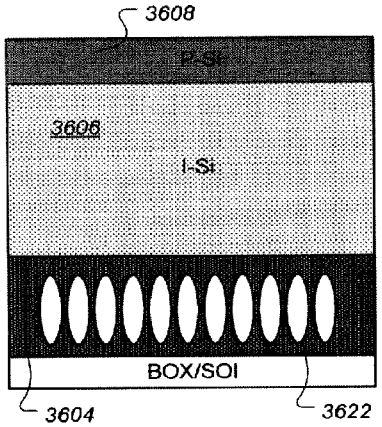


FIG. 36

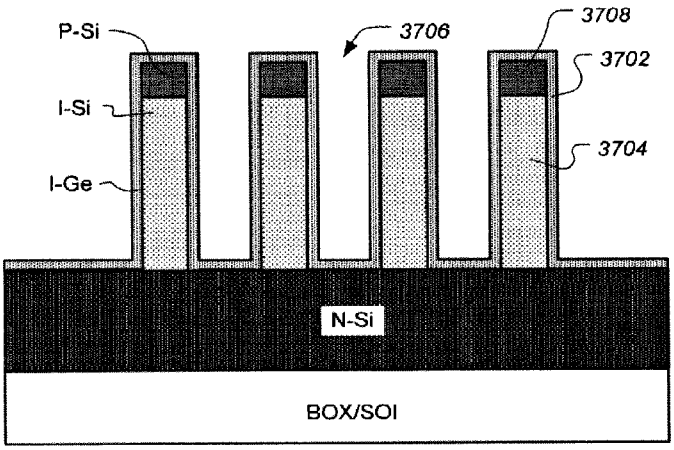

P-Si
3706
3708
3702
I-Si
3704
I-Ge
N-Si
BOX/SOI

FIG. 37

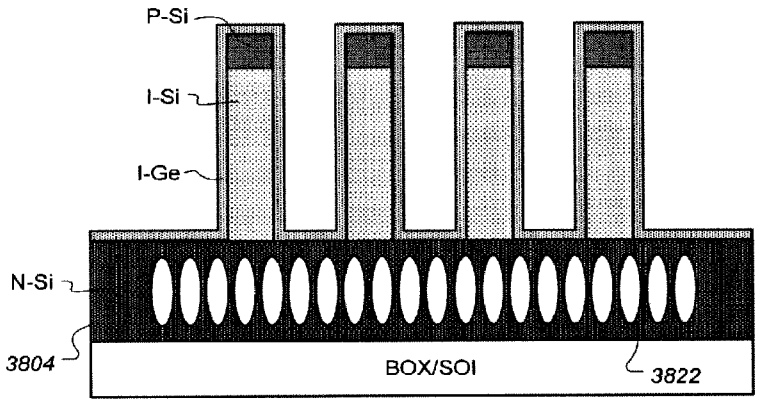

P-Si
I-Si
I-Ge
N-Si
3804
BOX/SOI
3822

FIG. 38

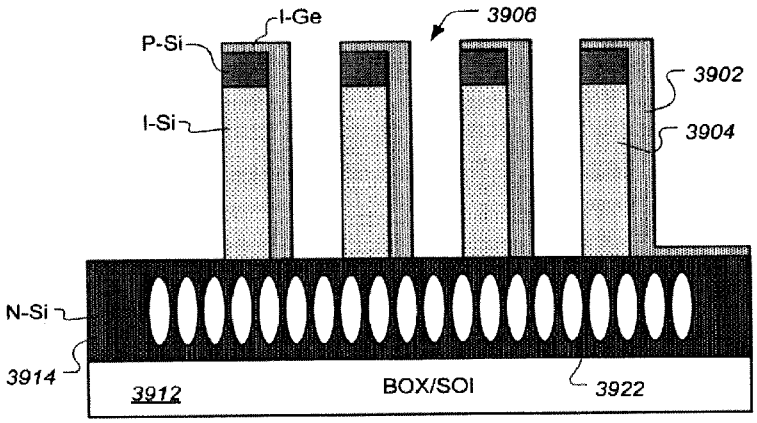

I-Ge
3906
P-Si
3902
I-Si
3904
N-Si
3914
3912
BOX/SOI
3922

FIG. 39

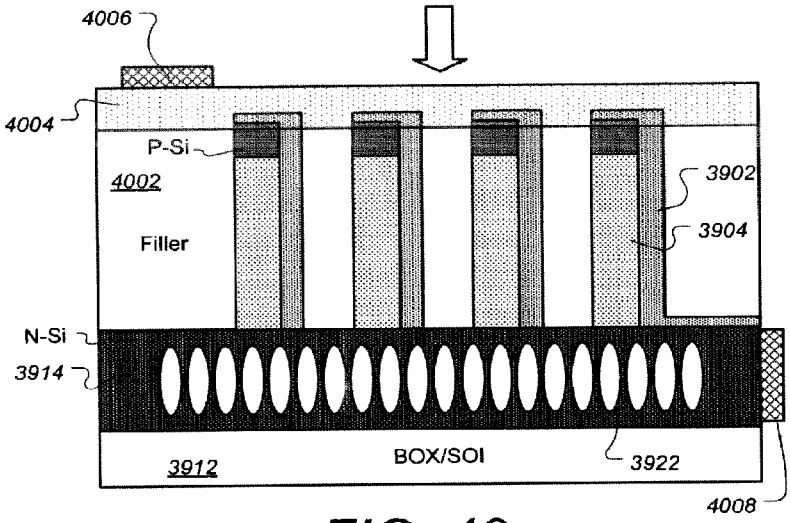

4006
4004
P-Si
4002
Filler
3902
3904
N-Si
3914
3912
BOX/SOI
3922
4008

FIG. 40

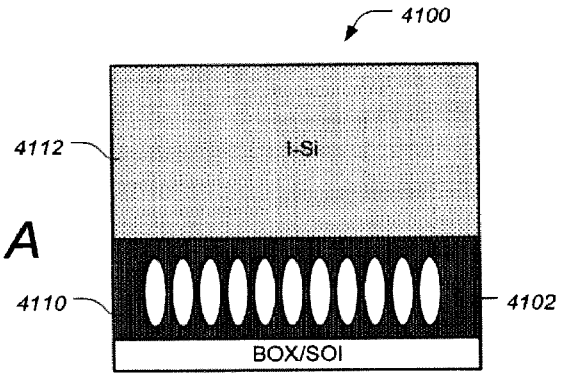


FIG. 41A

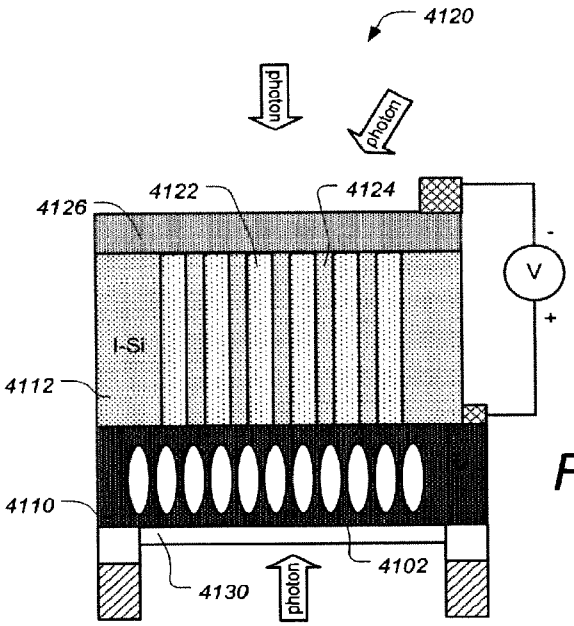
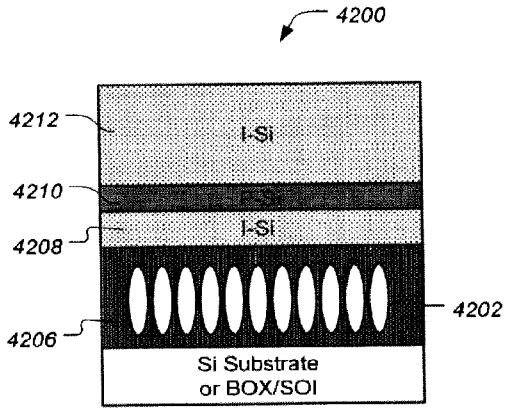


FIG. 41B

FIG. 42A



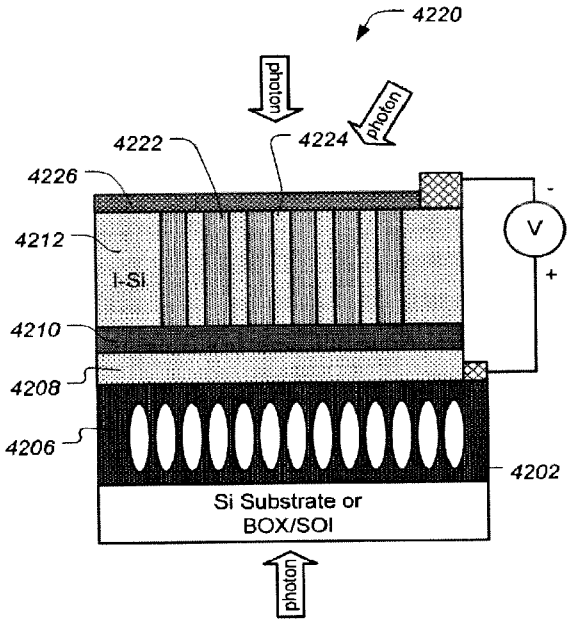


FIG. 42B

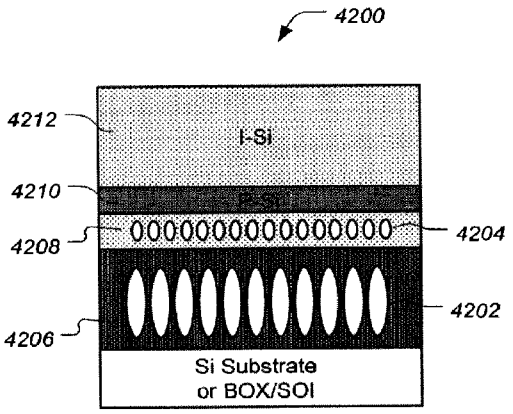


FIG. 42C

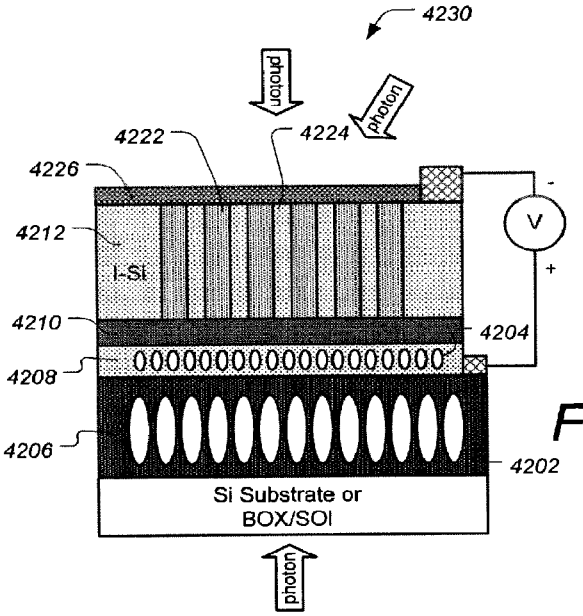


FIG. 42D

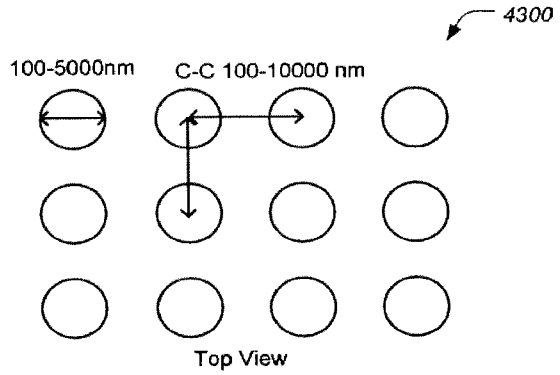

4300
100-5000nm
C-C 100-10000 nm
Top View

FIG. 43

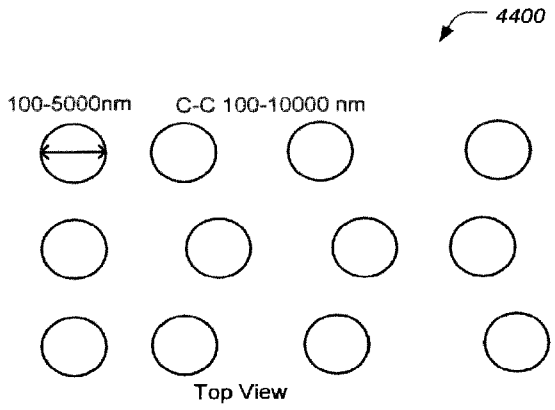

4400
100-5000nm
C-C 100-10000 nm
Top View

FIG. 44

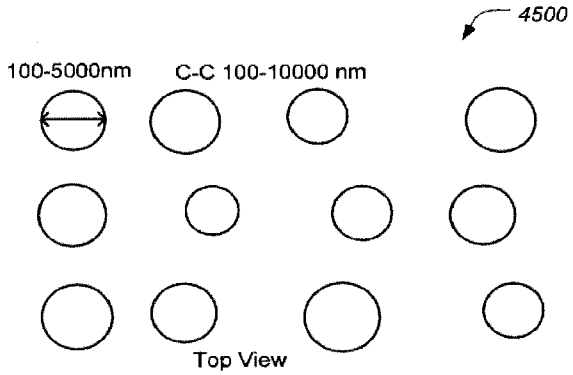

4500
100-5000nm
C-C 100-10000 nm
Top View

FIG. 45

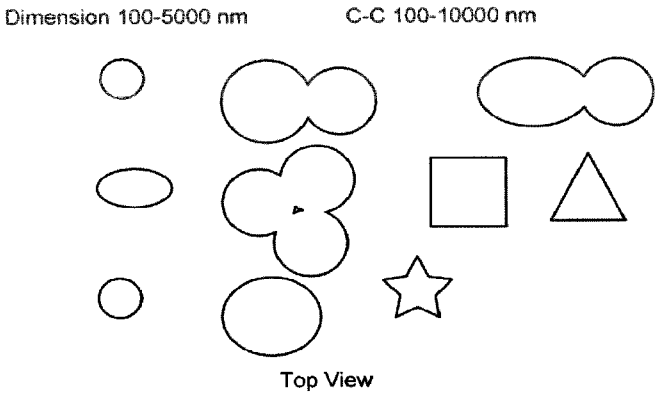

Dimension 100-5000 nm
C-C 100-10000 nm
Top View

FIG. 46

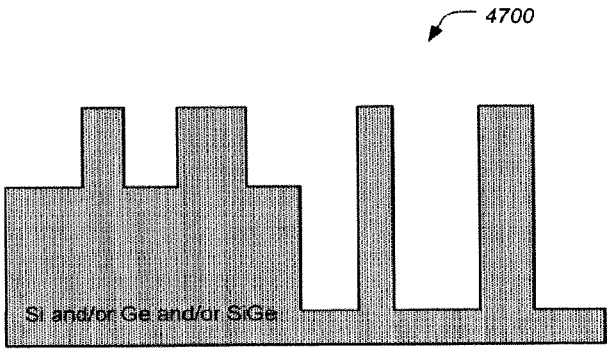


FIG. 47

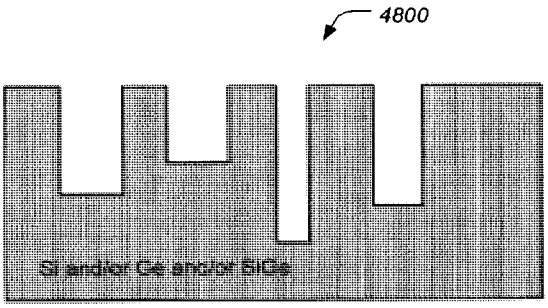


FIG. 48

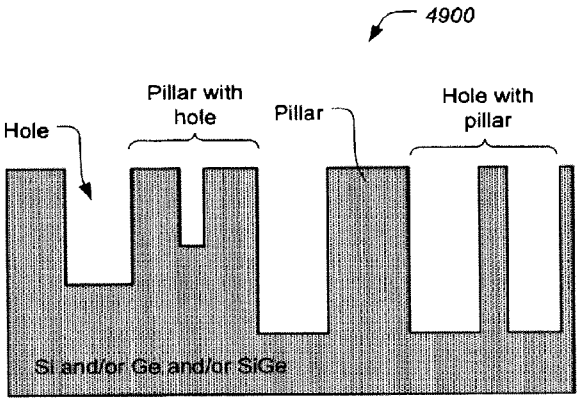

4900
Pillar with hole
Pillar
Hole with pillar
Hole
Si and/or Ge and/or SiGe

FIG. 49

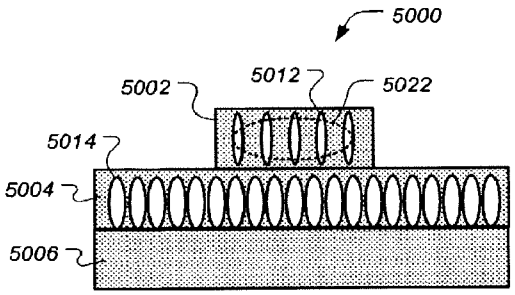

5000
5002
5012
5022
5014
5004
5006

FIG. 50

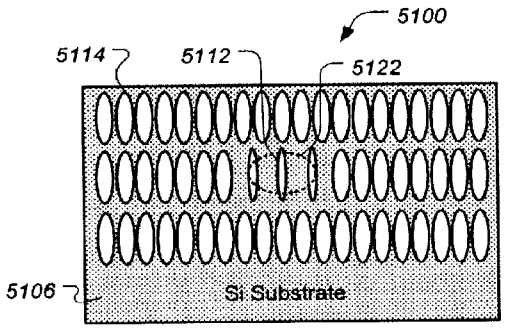

5100
5114
5112
5122
5106
Si Substrate

FIG. 51

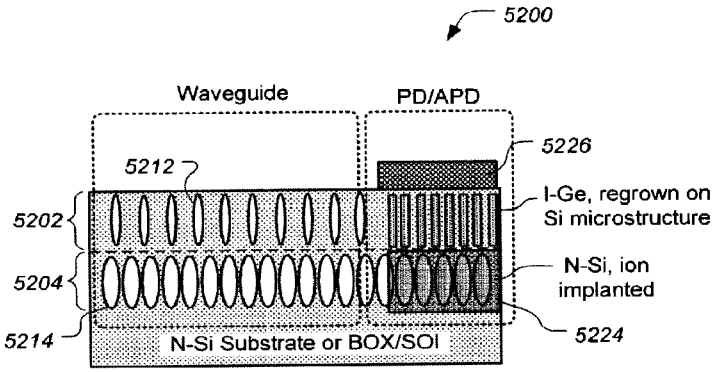

5200
Waveguide
PD/APD
5212
5226
I-Ge, regrown on
Si microstructure
5202
5204
N-Si, ion
implanted
5214
5224
N-Si Substrate or BOX/SOI

FIG. 52

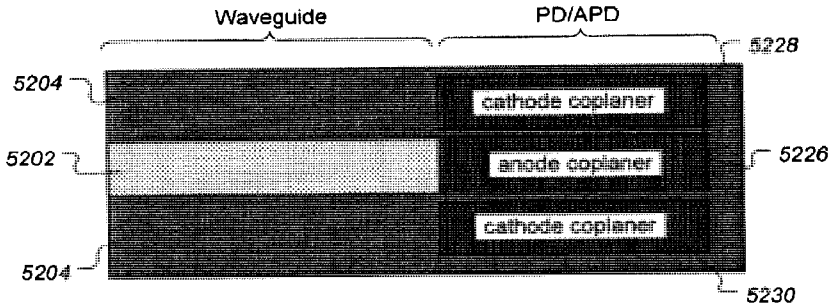


FIG. 53

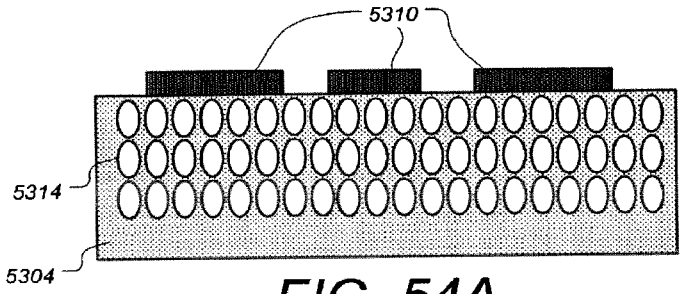


FIG. 54A

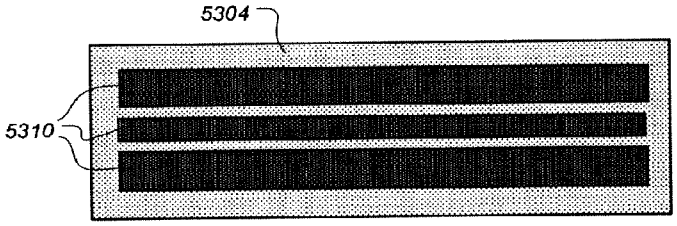


FIG. 54B

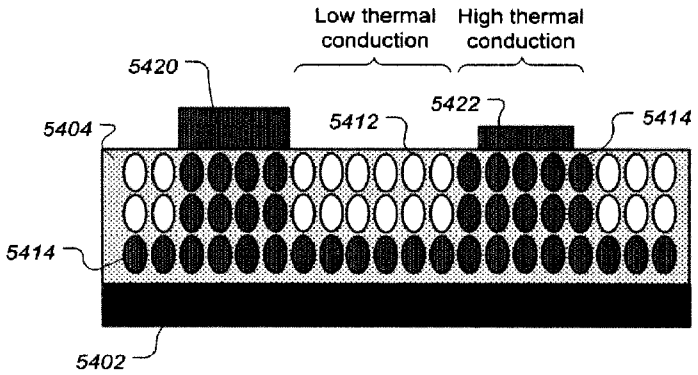

Low thermal conduction
High thermal conduction
5420
5422
5404
5412
5414
5414
5402

FIG. 55

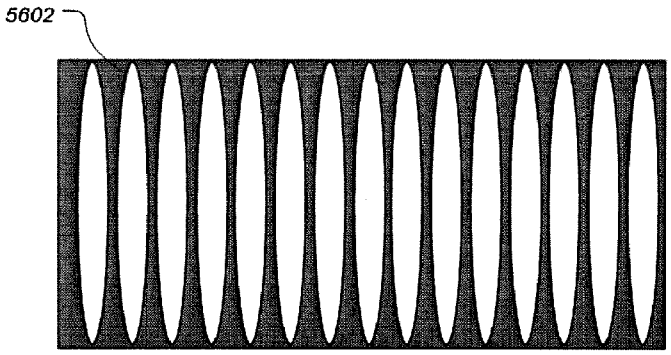

5602

FIG. 56

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	TBD
Filing Date	TBD
First Named Inventor	Shih-Yuan Wang
Title	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES
Art Unit	n/a
Examiner Name	n/a
Attorney Docket Number	309-0011USDIVCIP2

SIGNATURE of Applicant or Patent Practitioner

Signature	/Ivan S. Kavrukov/	Date (Optional)	
Name	Ivan S. Kavrukov	Registration Number	25,161
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 139982

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

W&WSens Devices, Inc.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	[signature]	Date (Optional)	Oct 20, 2020
Name	SHUPING WANG		
Title	PRESIDENT CEO		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/01 (06-12)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	MICROSTRUCTURE ENHANCED ABSORPTION PHOTOSENSITIVE DEVICES

As the below named inventor, I hereby declare that:

This declaration is directed to:

- [■] The attached application, or
- [ ] United States application or PCT international application number _____

filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Shih-Ping WANG Date (Optional): _____

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.