

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS
AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG
AUSTIN SEMICONDUCTOR LLC,

Petitioner,

v.

W&WSENS DEVICES INC.,

Patent Owner.

Case IPR2025-00994
Patent No. 11,621,360

PETITION FOR *INTER PARTES* REVIEW

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- a. [1pre]: “A photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar holes comprising:” 21
- b. [1a]: “a laterally extending array of pillars that have rectangular cross-sections in a horizontal plane;” 24
- c. [1b.1]: “wherein said array of pillars comprises: a first doped semiconductor material; an intermediate semiconductor material; and solid dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars;” 26
- d. [1b.2]: “a second doped semiconductor material; wherein:” 31
- e. [1c.1]: “the intermediate semiconductor material is between said first and second doped semiconductor materials;” 32
- f. [1c.2]: “the first and second doped semiconductor materials are doped to opposite semiconductor types;” 33
- g. [1c.3]: “the intermediate semiconductor material is less doped than at least one of the first and second doped semiconductor materials and the degree of doping is the same or different for different positions in the intermediate semiconductor material; and” 34
- h. [1c.4]: “each of the first and second doped semiconductor materials and said intermediate semiconductor material comprises Si;” 36
- i. [1d]: “one or more deliberately formed in-pillar holes with solid dielectric therein;” 37
- j. [1e]: “top and bottom electrical contacts electrically coupled with said array of pillars,

- wherein said photodetector device is configured to respond to light photons incident on said array of pillars by photo-generated charge carriers therein; and” 40
- k. [1f]: “a base dielectric region that is below the array of pillars and comprises substantially solid dielectric material;” 43
- l. [1g]: “wherein the pillars of said array of pillars: are laterally spaced center to center by no more than 10,000 nanometers; and have up-down lengths of said intermediate semiconductor material in the range of 100-5000 nanometers;” 47
- m. [1h]: “wherein at least said pillars, in-pillar holes, and solid dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars increase photon absorption of said device of incident light by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said one or more in-pillar holes;” 51
- n. [1i]: “wherein said array of pillars is monolithically integrated in or on said **semiconductor substrate** with electronic circuits that include active elements for signal processing and transmission.” 63
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PETITIONER’S EXHIBIT LIST

Exhibit	Description
Ex-1001	U.S. Patent No. 11,621,360 B2 to Wang et al. (“’360 Patent”)
Ex-1002	Declaration of Dr. Michael Lebby, Ph.D. (“Lebby”)
Ex-1003	Prosecution History of the ’360 Patent (downloaded from Patent Center)
Ex-1004	U.S. Patent Application Publication No. 2012/0049044 A1 to Kuboi (“ <i>Kuboi</i> ”)
Ex-1005	U.S. Patent Application Publication No. 2012/0033119 to Shinohara (“ <i>Shinohara</i> ”)
Ex-1006	European Patent Application EP 2172974 A1 to NXP B.V. (“ <i>NXP</i> ”)
Ex-1007	U.S. Patent Application Publication No. 2008/0259981 A1 to Wang et al. (“ <i>Wang</i> ”)
Ex-1008 to Ex-1009	Reserved
Ex-1010	Zhihong Huang et al., <i>Microstructured silicon photodetector</i> , Applied Physics Letter, Vol. 89 (2006), pp. 033506-1 to -3.
Ex-1011	Richard A. Myers et al., <i>Enhancing near-infrared avalanche photodiode performance by femtosecond laser microstructuring</i> , Applied Optics, Vol. 45, No. 35 (Dec. 2006), pp. 8825-31.
Ex-1012	Abbas El Gamal et al., <i>CMOS Image Sensors</i> , IEEE Circuits & Devices Magazine (2005), pp. 6-20.
Ex-1013	Eric R. Fossum, <i>CMOS Image Sensors: Electronic Camera-On-A-Chip</i> , IEEE Transactions on Electron Devices, Vol. 44, No. 10 (Oct. 1997), pp. 1689-98.
Ex-1014	Sunetra Mendis et al., <i>CMOS Active Pixel Image Sensor</i> , IEEE Transactions on Electron Devices, Vol. 41, No. 3 (Mar. 1994), pp. 452-53.
Ex-1015	Renato Turchetta et al., <i>Introduction to CMOS Image Sensors</i> , Molecular Expressions™ Optical Microscopy Primer: Digital Imaging in Optical Microscopy - Introduction to CMOS Image Sensors (July 16, 2004), pp. 1-9, available at

Exhibit	Description
	https://web.archive.org/web/20120508153832/https://micro.magnet.fsu.edu/primer/digitalimaging/cmosimagesensors.html
Ex-1016 to Ex-1019	Reserved
Ex-1020	John P. Uyemura, <i>CMOS Logic Circuit Design</i> (Kluwer Academic Publishers 2002), pp. 64, 74-102, 315-17, 458-60.
Ex-1021	Khalil Jumah Tawfiq Haram, Organic Solar Cells Based on High Dielectric Constant Materials: An Approach to Increase Efficiency (June 2013) (Ph.D. dissertation, Western Michigan University), pp. 1-122.
Ex-1022	P. Kalugasalam et al., <i>Dielectric and AC Conduction Studies of Lead Phthalocyanine Thin Film</i> , Chalcogenide Letters, Vol. 6, No. 9 (Sept. 2009), pp. 469-76.
Ex-1023 to Ex-1027	Reserved
Ex-1028	Leonard Rubin et al., <i>Ion Implantation in Silicon Technology</i> , Industrial Physicist, 9(3), (Jun/July 2003), pp. 12-15.
Ex-1029	Jurgen Michel et al., <i>Advances in fully CMOS integrated photonic devices</i> , Proceedings of SPIE, Vol. 6477 (2007), pp. 64770P-1 to -11 (“Michel”).
Ex-1030	Mark Beals et al., <i>Process Flow Innovations for Photonic Device Integration in CMOS</i> , Proceedings of SPIE, Vol. 6898 (2008), pp. 689804-1 to -14 (“Beals”).
Ex-1031 to Ex-1033	Reserved
Ex-1034	Matthew Saucedo, <i>Porphyrim Thin Film Dielectrics</i> , SUNFEST Technical Report TR-CST01NOV04, Center for Sensor Technologies, Univ. of Pennsylvania, Philadelphia, PA (2004), pp. 181-98.
Ex-1035	N. Venkatramaiah et al., <i>Spectroscopic and dielectric studies of meso-tetrakis(p-sulfonatophenyl) porphyrin doped hybrid borate glasses</i> , Journal of Alloys and Compounds, Vol. 509 (2011), pp. 2797-803.

Exhibit	Description
Ex-1036	Tom J. Savenije, <i>Photogeneration and transport of charge carriers in a porphyrin p/n heterojunction</i> , Physical Review B, Vol. 55, No. 15 (Apr. 1997), pp. 9685-92.
Ex-1037	Ümit Salan et al., <i>Synthesis, characterization, electrical and dielectric permittivity measurements of 2,9,16,23-tetra(4-ferrocenylimino-3-nitrophenoxy)phthalocyanines</i> , Journal of Porphyrins and Phthalocyanines, Vol. 10 (2006), pp. 1263-70.
Ex-1038	Teresa M. Figueira-Duarte et al., <i>Pyrene-Based Materials for Organic Electronics</i> , Chemical Reviews, Vol. 111 (2011), pp. 7260-314.
Ex-1039 to Ex-1049	Reserved
Ex-1050	U.S. Patent Application Publication No. 2012/0153124 A1 to Yu et al. (“ <i>Yu</i> ”)
Ex-1051	International Patent Publication No. WO 2011/085297 A1 to Han et al. (“ <i>Han</i> ”)
Ex-1052	Japanese Patent Publication No. JP 2007-129024A
Ex-1053	Certified English Language Translation of Japanese Patent Publication No. JP 2007-129024A to Hasegawa (“ <i>Hasegawa</i> ”)
Ex-1054	Reserved
Ex-1055	U.S. Patent No. 7,646,943 B1 to Wober (“‘943 Patent”)
Ex-1056	U. S. Patent No. 8,274,122 B2 to Shimotsusa
Ex-1057	U. S. Patent No. 8,378,339 B2 to Nomura et al.
Ex-1058	Richard Rhoad et al., <i>Geometry for Enjoyment and Challenge</i> (Houghton Mifflin 1997), pp. 236.
Ex-1059	U.S. Patent Application Publication No. 2008/0157141 A1 to Han
Ex-1060	U.S. Patent No. 8,390,036 B2 to Goto
Ex-1061	H. H. Li, <i>Refractive Index of Silicon and Germanium and Its Wavelength and Temperature Derivatives</i> , J. Phys. Chem. Ref. Data, Vol. 9, No. 3 (1980), pp. 561-658.

Exhibit	Description
Ex-1062	Rei Kitamura et al., <i>Optical constants of silica glass from extreme ultraviolet to far infrared at near room temperature</i> , Applied Optics, Vol. 46, No. 33 (November 20, 2007), pp. 8118-33.
Ex-1063	S.M. Sze et al., <i>Semiconductor Devices Physics and Technology</i> (John Wiley & Sons, Inc. 3d ed. 2012), pp. 6-9, 205-10, 325-30, 392-406, 416-17, 466-67.
Ex-1064 to Ex-1066	Reserved
Ex-1067	<i>Electrical Engineering Dictionary - CRCnetBase</i> (Phillip A. Laplante editor-in-chief, CRCPress LLC 2000), pp. 1-10.
Ex-1068	P.A. Lane et al., <i>Electroabsorption studies of phthalocynine/perylene solar cells</i> , Solar Energy Materials & Solar Cells, Vol. 63, (2000), pp. 3-13.
Ex-1069	Martin A. Green, <i>Self-consistent optical parameters of intrinsic silicon at 300K including temperature coefficients</i> , Solar Energy Materials & Solar Cells, Vol. 92, (2008), pp. 1305-10.
Ex-1070	Horst Zimmerman, <i>Integrated Silicon Optoelectronics</i> (Springer. 2d ed. 2010), pp. 1-7.
Ex-1071	M.M. El-Nahas et al., <i>Structural and optical properties of Ni (II) tetraphenyl porphyrin thin films</i> , Eur. Phys. J. Appl. Phys. (2012), Vol. 57, pp. 30201-p1 to 30201-p13.
Ex-1072	M.M. El-Nahas et al., <i>Structural and optical properties of thermally evaporated zinc phthalocyanine thin films</i> , Proc. 2 nd Saudi Sc. Conf. (March 2004), pp. 277-293.
Ex-1073	M.E. Azim-Araghi et al., <i>Electrical and optical properties of an organic semiconductor metal-free phthalocyanine (C₃₂H₁₈N₈)</i> , Eur. Phys. J. Appl. Phys. (2012), Vol. 58, pp. 30201-p1 to 30201-p6.
Ex-1074	<i>W&Wsens Devices Inc. v. Samsung Electronics Co. Ltd. et al.</i> , Case No. 2:24-cv-00854, Excerpts from Plaintiff's Infringement Contentions (Jan. 7, 2025)

I. Preliminary Statement

Petitioner Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor Inc.; and Samsung Austin Semiconductor LLC (collectively, “Samsung”), requests *inter partes* review of U.S. Patent No. 11,621,360 (Ex-1001), and cancellation of claims 1, 3, 5-6, and 8-9.

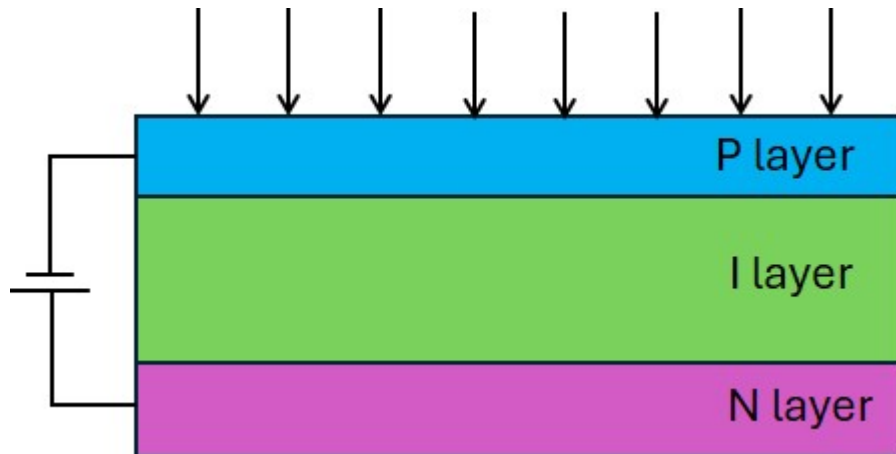
The challenged claims pertain to a photodetector that uses microstructures to enhance photon absorption in a semiconductor device, and recite specific microstructure dimensions that allegedly increase light absorption by 10% over a semiconductor that does not include such microstructures. The challenged claims also require a photodetector in which the image sensor and control circuitry are monolithically integrated on a single semiconductor substrate. These features, however, were all well known. For example, *Kuboi* and *Yu* disclose microstructured semiconductors with the claimed dimensions. And *Kuboi*, *Yu*, and *Shinohara* disclose monolithic integration.

As detailed below and in the supporting declaration of Michael Lebby, Ph.D., (“Lebby”) (Ex-1002), the challenged claims are unpatentable based on the grounds presented. Lebby, ¶¶3-5, 99-101. The Board should institute review and cancel all challenged claims.

II. State of the Art

A. Photodetectors

A photodetector is a semiconductor device that transforms photons into electrical signals, enabling electrical circuits to detect and measure incident light. Leeb, ¶51. Various types of photodetectors exist, including photodiodes. A PiN photodetector is a photodiode characterized by an **intrinsic (undoped) layer** positioned between highly doped **P-type** and **N-type** semiconductor layers (hence “**PiN**”):



Id. When light enters the photodetector, the intrinsic layer absorbs photons, generating electron-hole pairs. Applying a negative bias across the photodetector causes the separated electrons to move towards the N-type layer and the holes towards the P-type layer, producing a measurable photocurrent. Leeb, ¶52.

B. Microstructure-Enhanced Photodetectors

Conventional silicon photodetectors exhibit high responsivity at wavelengths of light less than about 850 nm. Ex-1010, 1. The prior art recognized that tailoring silicon's microstructure extends photodetector operability to longer wavelengths. For instance, etching a silicon photodetector surface to create micron-sized pillars was known to enhance a photodetector's responsiveness at longer wavelengths. Ex-1010, 1-2; Ex-1011, 1-6; Lebby, ¶53.

Photodetectors featuring microstructures enhanced by etched holes were widely known well before the purported invention date. For example, *NXP*'s (Ex-1006) single-chip device includes a silicon PiN photodiode integrated with CMOS signal processing circuitry on the same substrate 102.

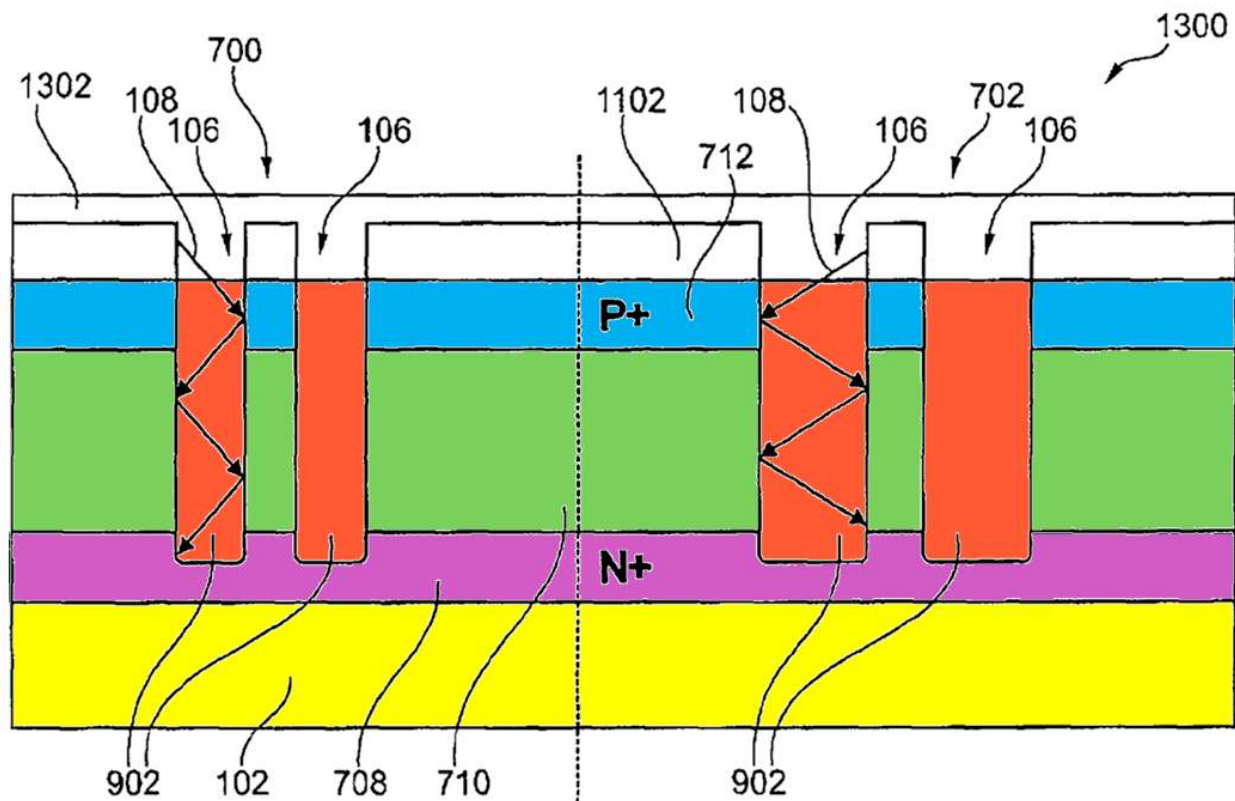


Fig. 13

NXP, Fig. 13.¹ The **PiN** photodiode's **intrinsic layer** 710 is disposed between **N⁺ layer** 708 and **P⁺ layer** 712 and holes or **pores** 106 formed on the **PiN** layers by etching. *NXP*, ¶¶[77]-[78]. **Pores** 106 increase the photodiode's quantum efficiency. *NXP*, ¶¶[13], [38]; Lebby, ¶¶53-56.

¹ All color and colored annotations in figures have been added.

III. The '360 Patent

A. Specification

The '360 Patent's photodetector includes microstructures to enhance photoabsorption. '360 Patent, 2:31-32, 2:58-62, 3:57-64, 17:13-19. The photodetectors include a silicon substrate with a first layer (P^+ layer), a very low doped N or P intermediate layer (or I layer), and a second layer (N^+ layer), with holes etched in one or more PIN layers. *Id.*, 15:45-47, 15:64-16:24, 17:35-40. The photodetector, which is illustrated below, operates in reverse-bias mode with negative voltage on the anode (P^+ layer) and positive voltage on the cathode (N^+ layer). *Id.*, 16:28-31, 11:32-38.

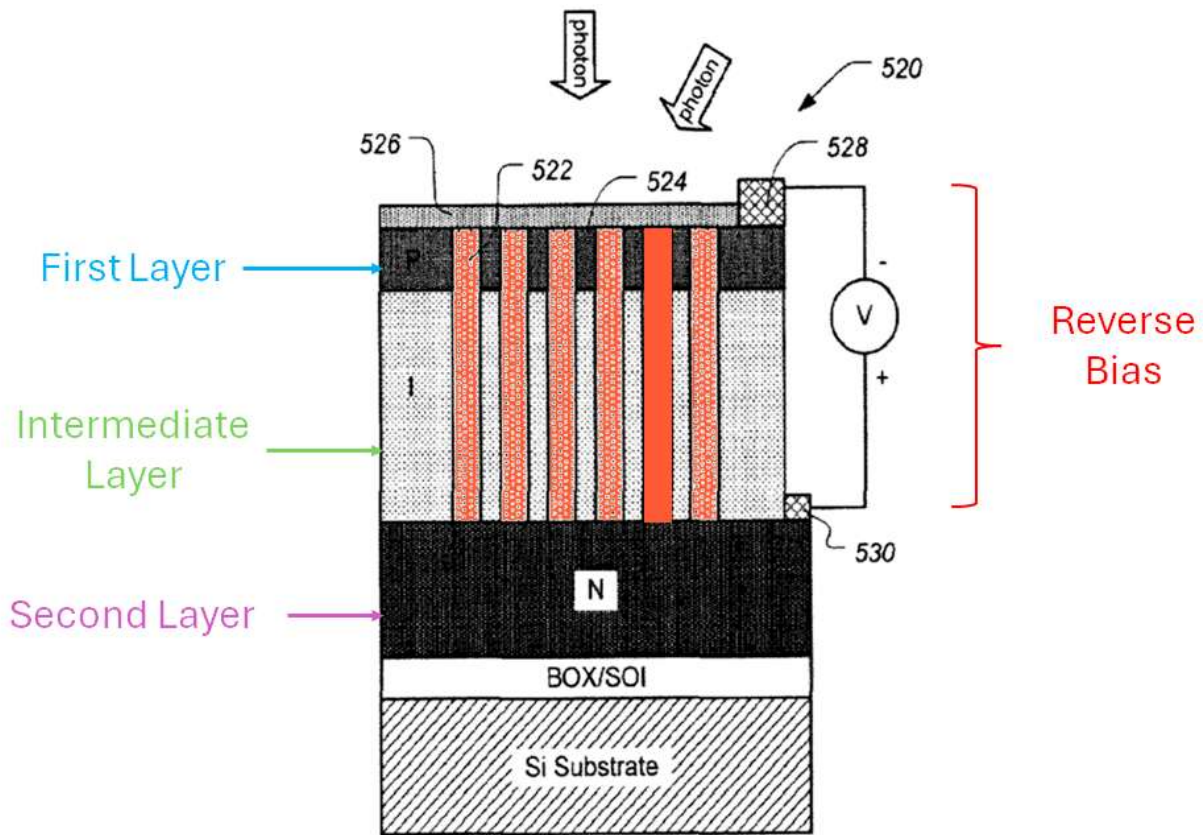


FIG. 5B

Id., Fig. 5B.

The '360 Patent discloses that optical signals can impinge normal to the light-receiving surface of the photodetector or at an angle off normal. *Id.*, 16:36-37. The '360 Patent discloses that one of the causes of enhancement of the absorption coefficient of the incident light includes high contrast grating (HCG) effects. *Id.*, 11:39-44. The '360 Patent explains that because of the HCG effect, the microstructured pillar-hole-void array can have an enhanced absorption coefficient over the bulk absorption coefficient by a factor of 1.1 to over 100. *Id.*, 12:36-42.

The photodetector can be integrated with ASIC (application-specific integrated circuits) for specific applications. *Id.*, 10:9-13; Lebbly, ¶¶66-69.

B. Claim Construction

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. §42.100(b). Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, no terms need construction to resolve the controversy.²

IV. Statement of Precise Relief Requested

A. Prior Art

The application that resulted in the '360 Patent was filed on March 29, 2022, claiming priority to multiple patent applications, the earliest of which was filed on May 22, 2013.³ Thus, the earliest claimed priority date is May 22, 2013.

- *Kuboi* (Ex-1004), U.S. Patent Publication No. 2012/0049044, which published on March 1, 2012, is prior art under 35 U.S.C. §102(a)(1), (a)(2).

² Petitioner retains the right to contend in another proceeding that certain limitations are indefinite.

³ Petitioner retains the right to dispute the claimed priority in another proceeding.

- *Shinohara* (Ex-1005), U.S. Patent Publication No. 2012/0033119, which published on February 9, 2012, is prior art under 35 U.S.C. §102(a)(1), (a)(2).
- *Yu* (Ex-1050), U.S. Patent Publication No. 2012/0153124, which published on June 21, 2012, is prior art under 35 U.S.C. §102(a)(1), (a)(2).

B. Challenges

Ground	Challenged Claims	Basis	Prior Art
1	1, 3, and 5-6	§103	<i>Kuboi and Shinohara</i>
2	1 and 8-9	§103	<i>Yu</i>
3	1 and 8-9	§103	<i>Yu and Shinohara</i>

V. Level of Ordinary Skill in the Art

A person of ordinary skill in the art (“POSITA”) would have had at least a master’s degree in electrical engineering or a similar field and at least two years of experience working with semiconductor systems and semiconductor devices.

Lebby, ¶¶96-97. Additional relevant work experience can compensate for less education, and *vice versa*. Lebby, ¶¶97-98.

VI. The Challenged Claims Are Unpatentable

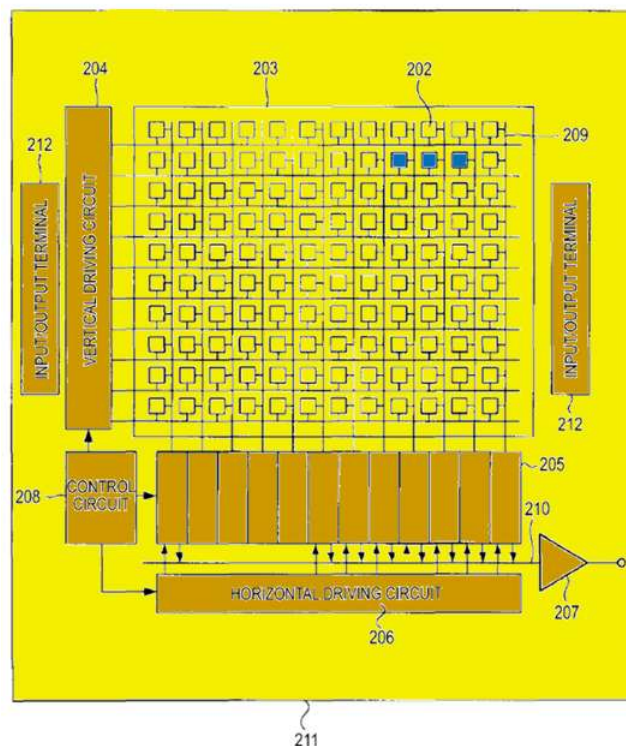
A. Claims 1, 3, and 5-6 are Obvious Over *Kuboi* and *Shinohara* (Ground 1)

1. Overview of *Kuboi*

Kuboi's CMOS imaging device 201 includes a pixel region 203 and a peripheral circuit portion on a single semiconductor substrate 211. *Kuboi*, ¶[48]; Lebby, ¶¶73-75.

FIG. 15

201



Kuboi, Fig. 15. Pixel region 203 of substrate 211 comprises a plurality of pixels 202 arranged in a two-dimensional array. *Kuboi*, ¶[48]. Each pixel 202 contains one photoelectric conversion portion (or a photodiode) and four pixel

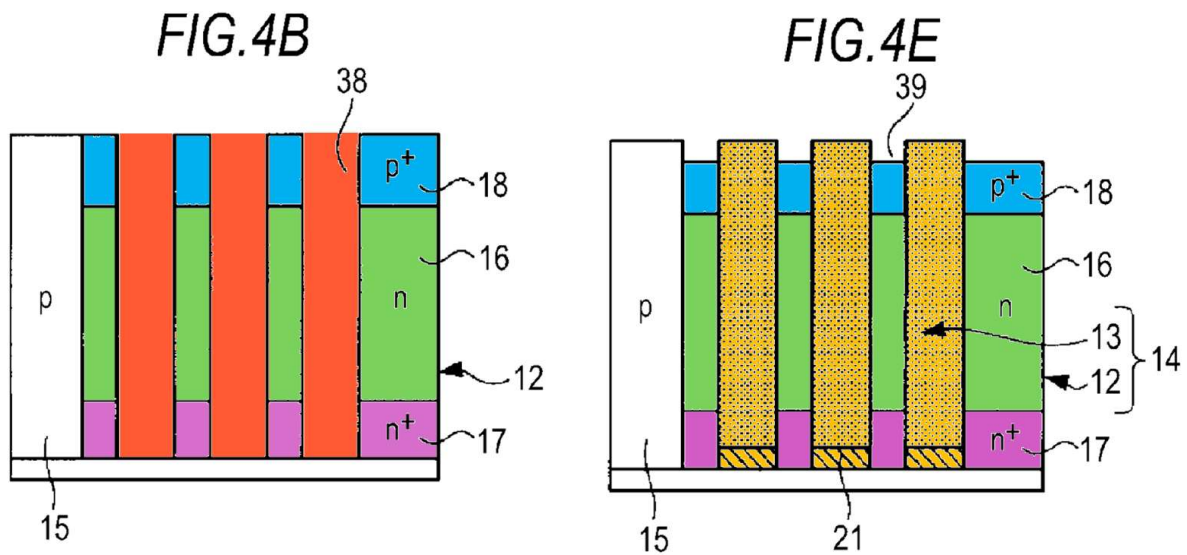
transistors. *Id.* The peripheral circuit portion includes “logic[] circuits” (e.g., circuits 204, 205, 206, 207, and 208), which process the pixel’s electrical output and then output it. *Kuboi*, ¶¶[49]-[54]. The pixels and peripheral circuit portion are fabricated on a single substrate, the pixel transistors are fabricated on another substrate, and the two substrates are bonded together. *Kuboi*, ¶[70].

Kuboi describes photoelectric conversion portions suitable for use in imaging device 201. *Kuboi*, ¶[48]. For example, *Kuboi* discloses a basic pixel configuration with reference to Figures 1A/1B. *Kuboi*, ¶[55]. *Kuboi* likewise discloses a pixel configuration in Figures 6A/6B, explaining that the disclosed red and green pixels 53R and 53G have a structure that is the same as the basic configuration of Figures 1A/1B. *Kuboi*, ¶¶[90], [95], [69]. *Kuboi* also discloses that Figure 13 includes pixels 53R, 53G, and 53B, having configurations that are the same as the pixels of Figures 1A/1B. *Kuboi*, ¶[181]. Similarly, *Kuboi* describes Figure 15 as applicable to all of *Kuboi*’s pixel configurations. *Kuboi*, ¶¶[34], [48]. Further, *Kuboi*’s Figures 4A-4F show a method of manufacturing the basic pixel configuration of Figures 1A/1B. *Kuboi*, ¶¶[69]-[76]. Thus, Figures 1A/1B, 6A/6B, 13, and 15 all disclose the pixel configuration of the same imaging device. And Figures 4A-4F of *Kuboi* disclose methods of manufacturing that same pixel configuration. Accordingly, this Petition relies on Figures 1A/1B, 4A-4F, 6A/6B,

13, and 15, and *Kuboi*'s associated disclosures as representative of the pixel configuration of the same imaging device. Lebbby, ¶¶76-77.

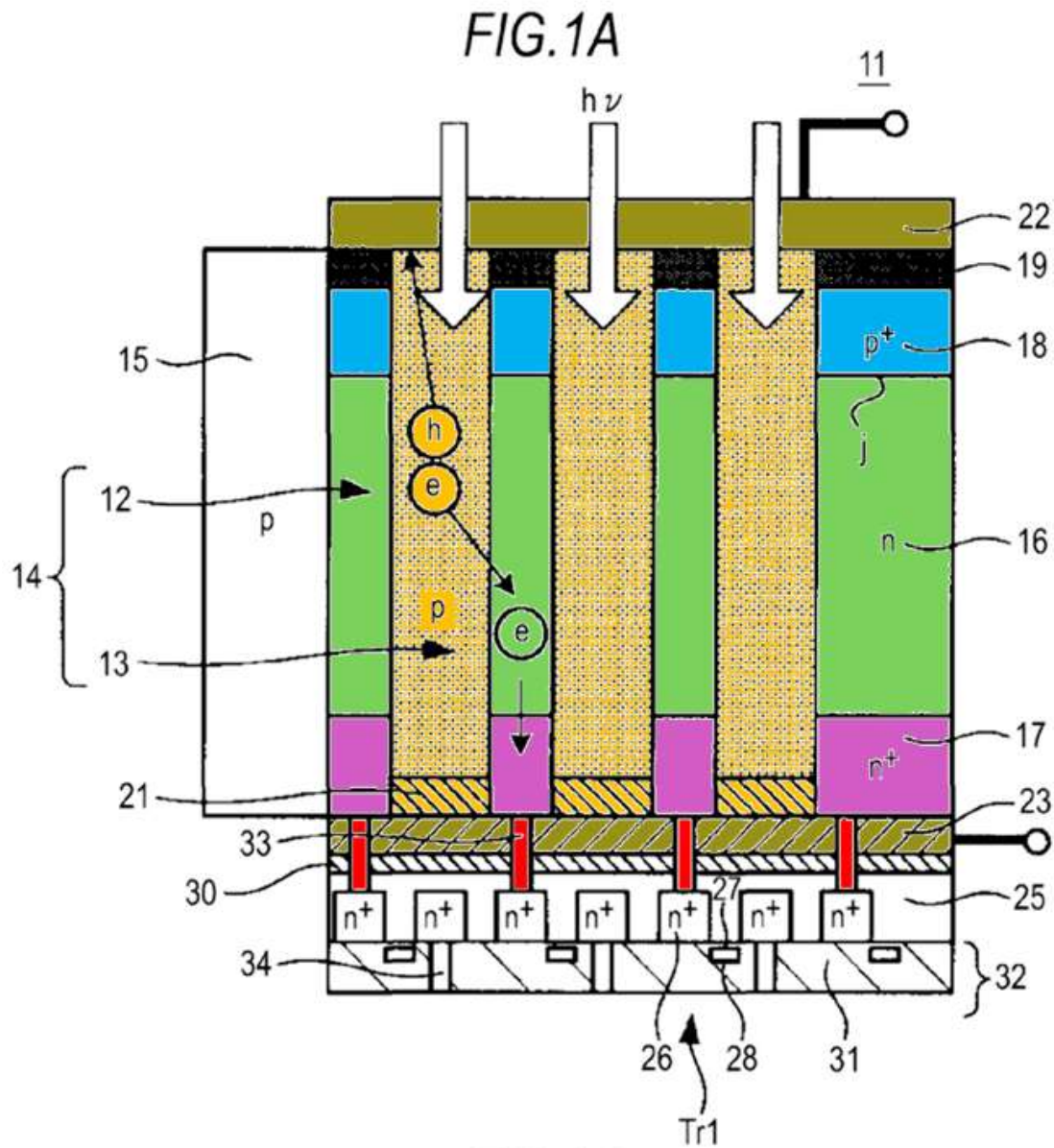
Figure 1A illustrates photoelectric conversion portion 14 in pixel 11. *Kuboi*, ¶¶[48], [55]-[56]. Pixel 11, including portion 14, can be utilized in imaging device 201. *Kuboi*, ¶¶[48], [55]. Portion 14 comprises a silicon semiconductor layer 12 that includes multiple embedded organic material layers 13. *Kuboi*, ¶[55]. Layer 12 is implanted with different impurities (doped) to form n-type semiconductor ("intermediate") region 16 with p⁺ type semiconductor region 18 on one side and n⁺-type semiconductor region 17 on the opposite side (stacked PIN regions). *Kuboi*, ¶¶[56], [71]. The doping of layer 12 is such that region 18 and region 17 have a higher concentration of impurities than region 16. *Kuboi*, ¶[56].

After forming regions 18, 16, and 17, holes 38 extending from p⁺ type region 17 to n⁺-type region 17 are etched into the PIN regions (below, left). *Kuboi*, ¶¶[71]-[72]. Then, the organic material that forms photoelectric conversion films 13 is deposited in holes 38 (below, right). *Kuboi*, ¶¶[72]-[73].



Kuboi, Figs. 4B (left), 4E (right).

Metal shielding film 19 is applied to the surface of **region 18** such that only **holes 38** containing **films 13** are exposed to incident light ($h\nu$). *Kuboi*, ¶[59]. An **upper electrode 22** and a **lower electrode 23** are formed on opposite sides of the **PIN** regions, and a reverse bias is applied. *Kuboi*, ¶¶[60], [64]. Photoelectric conversion of the incident light ($h\nu$) within **films 13** (inside **holes 38**) generates electron-hole pairs that pass through the depleted semiconductor layer 12 into a charge accumulation region 26 of the transfer transistor (Tr1) of the corresponding **pixel 11** (via **conductors 33**). *Kuboi*, ¶¶[62], [64], [73], Fig. 1A.



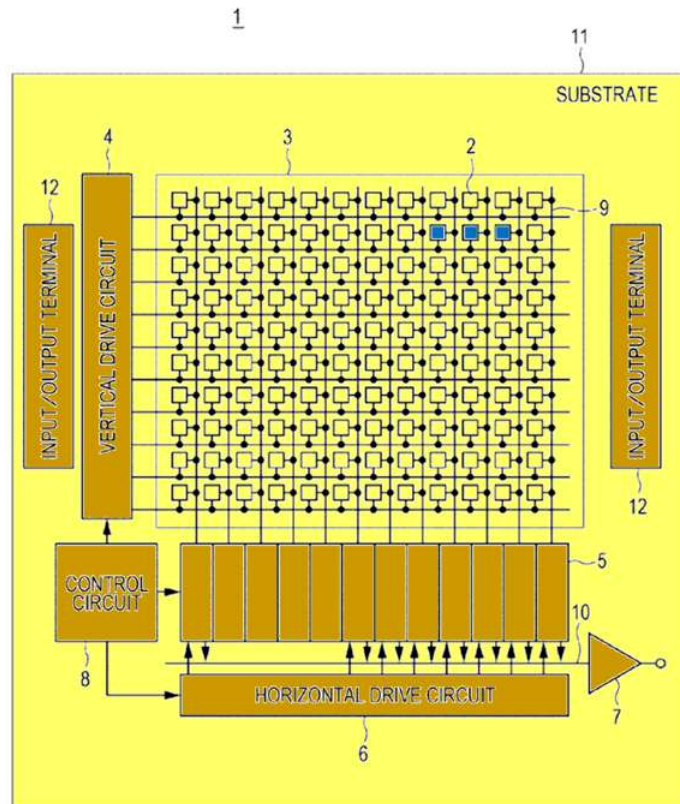
Kuboi, Fig. 1A.

After initial signal processing (e.g., amplification) by the pixel transistors, the electrical signals from the **pixel 11** are sent to the **peripheral circuit portions** for further processing. *Kuboi*, ¶¶[48]-[49], [61]-[62]; *Lebby*, ¶¶78-82.

2. Overview of *Shinohara*

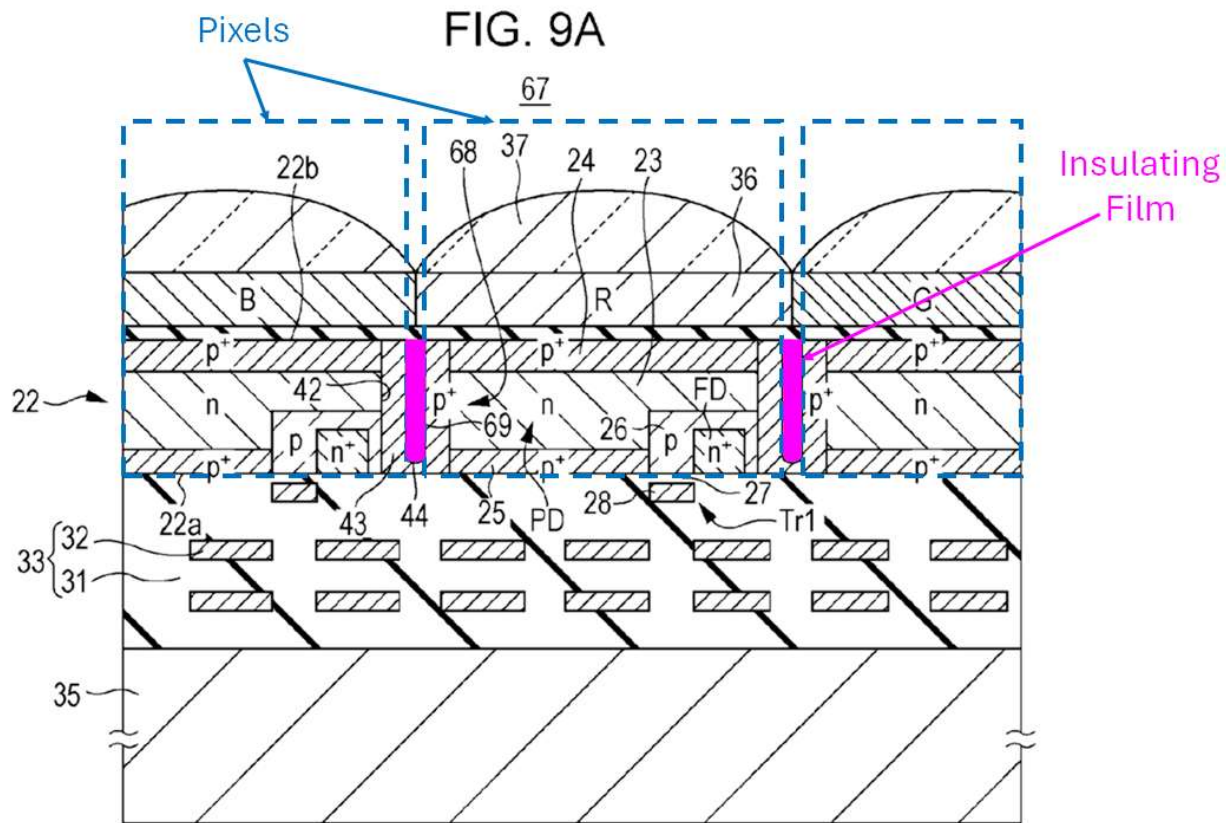
Shinohara's "solid-state imaging device ... suppresses the generation of white spots and dark current and the occurrence of color mixture and which improves the sensitivity." *Shinohara*, ¶[13]. *Shinohara* discloses "one example of a MOS solid-state imaging device." *Shinohara*, ¶[51]. Solid-state imaging device 1, illustrated below, "includes a pixel region (so-called imaging region) 3 in which a plurality of pixels 2 each having a photoelectric conversion portion is regularly arranged in a semiconductor substrate 11, such as a silicon substrate, in a two-dimensional matrix and a peripheral circuit portion." *Id.* "The peripheral circuit portion includes so-called logic circuits" (e.g., circuits 4, 5, 6, 7, and 8). *Shinohara*, ¶[52]; Leiby, ¶¶83-84.

FIG. 1



Shinohara, Fig. 1.

Shinohara's “photodiode PD” includes an n-type charge storage region 23 and p-type semiconductor regions 25 and 24. *Shinohara*, ¶[58]. *Shinohara's* imaging device includes “an element isolation region 68 for isolating pixels ... such that the p-type semiconductor layer 43 is provided in the trench 42 by an epitaxial growth, and an insulating film 69 is filled in the void 44 inside this p-type semiconductor layer 43.” *Shinohara*, ¶[90]. Insulating film 69 may include a silicon oxide film or silicon nitride film. *Shinohara*, ¶[91]; Lebbby, ¶¶85-89. These features are illustrated below:



Shinohara, Fig. 9A.

3. Motivation to modify *Kuboi*'s imaging device in view of *Shinohara*'s teaching of a solid dielectric insulating film

A POSITA would have been motivated to combine *Shinohara*'s solid dielectric insulating film with *Kuboi*'s pixel isolation region. Lebbby, ¶¶125-132.

Kuboi and *Shinohara* are analogous art to the '360 Patent because, like the '360 Patent, *Kuboi* and *Shinohara* also aim to improve the light absorption efficiency of their respective imaging devices. Lebbby, ¶126. The '360 Patent is directed to techniques for enhancing photon absorption. '360 Patent, Abstract. Similarly, *Kuboi* is directed to a solid-state imaging device in which light

absorption efficiency is increased to improve sensitivity. *Kuboi*, ¶[9]. Likewise, *Shinohara*'s solid-state imaging device improves sensitivity by improving a pixel's light absorption, thereby reducing charge leakage into an adjacent pixel. *Shinohara*, ¶¶[12]-[13].

Kuboi's adjacent pixels are separated by an element separation region formed of p-type semiconductor. *Kuboi*, ¶¶[55], [71], [91]. Like *Kuboi*, *Shinohara*'s adjacent pixels are separated by an isolation region made of p-type semiconductor. *Shinohara*, ¶[60]. The element isolation region may include a void. *Id.* *Shinohara* discloses that the void in the p-type element isolation region is filled with an insulating film made of solid dielectric material, such as silicon oxide or silicon nitride. *Shinohara*, ¶¶[90]-[91]; Lebbby, ¶127.

Shinohara teaches that “[s]ince the insulating film 69 is filled in the void 44, adjacent pixels are further electrically insulated from each other, thereby suppressing the leakage of photoelectrically converted charge into an adjacent pixel.” *Shinohara*, ¶[94]. Since the filled insulating film 69 has a refractive index different from that of p-type semiconductor layer 43, any “inclined incident light is reflected at the interface between the silicon and the insulating film and does not leak outside from the pixel,” preventing color mixture. *Id.* Thus, *Shinohara* outlines the benefits of using a solid dielectric material between adjacent pixels. Lebbby, ¶128.

A POSITA would have understood that including *Shinohara*'s solid dielectric insulating film in *Kuboi*'s element isolation region would improve electrical insulation between adjacent pixels in *Kuboi*'s modified imaging device. Lebbby, ¶129. Such insulation would ensure that light incident on a particular pixel did not inadvertently leak into and generate electrical charge in a neighboring pixel. *Id.* Further, a POSITA would have recognized that using *Shinohara*'s insulating film in *Kuboi*'s element isolation region would also help reflect light incident on a pixel at an angle back into that same pixel, thereby improving that pixel's light absorption and improving *Kuboi*'s device's efficiency. *Id.*

A POSITA would therefore have been motivated to implement *Shinohara*'s insulating film in *Kuboi* to improve *Kuboi*'s imaging device. Lebbby, ¶130. A POSITA would have found it obvious to modify *Kuboi*'s element separation region because it would have involved the use of a known technique—inserting an insulating film in the element separation region—to improve a similar device—*Kuboi*'s imaging device—in the same way, namely, by improving electrical insulation between adjacent pixels and minimizing light leakage between adjacent pixels. *Id.*

A POSITA would have had a reasonable expectation of success in implementing *Shinohara*'s teachings in *Kuboi*'s imaging device. Lebbby, ¶131. Because *Kuboi* and *Shinohara* disclose similar imaging devices with adjacent

pixels separated by an element separation or element isolation region, implementing *Shinohara*'s insulating film into *Kuboi*'s element separation region using *Shinohara*'s techniques would have been within a POSITA's skill. *Id.* A POSITA would have had a reasonable expectation of success for the combination because it requires combining well-known prior elements and *Shinohara*'s manufacturing methods. *Id.*

4. Motivation to modify *Kuboi*'s imaging device in view of *Shinohara*'s teaching of monolithic integration

Kuboi and *Shinohara* are analogous art to the '360 Patent. VI.A.3. A POSITA would have been motivated to implement *Shinohara*'s teaching of monolithic integration of the array of pillars (or pixels) with electronic circuits that include active elements for signal processing and transmission with *Kuboi*'s imaging device. Leiby, ¶¶222-227. Indeed, the integration of photodetectors and signal processing circuitry on a single substrate to form a single-chip device was known long before the purported invention date. Leiby, ¶¶57-65.

Kuboi discloses forming a pixel region and a peripheral circuit portion including logic circuits, input and output circuits, and a control circuit on a substrate. *Kuboi*, ¶¶[48]-[49], [69], [78]. This substrate "may be created in advance and be bonded to the semiconductor substrate on which the semiconductor region 25 having the pixel transistors, the multilayer wiring layer 32, the lower

electrode 23, and the like are formed.” *Kuboi*, ¶[78]. *Shinohara* discloses forming a pixel region, a peripheral circuit portion, pixel transistors, and a wiring layer on the same substrate. *Shinohara*, ¶¶[68]-[82].

Including the pixel region, peripheral circuit portion, pixel transistors, and wiring layer on the same substrate provides several advantages. Lebbby, ¶223. For example, monolithically integrating the pixel region and electronic circuits for signal processing and transmission on the same substrate reduces noise and attenuation of the photoelectric signal generated by the pixel region by shortening the signal travel path in the monolithically integrated imaging device. *Hasegawa*, ¶[9]; Lebbby, ¶223. Furthermore, such monolithic integration reduces manufacturing costs and package size. Lebbby, ¶224 (citing *Hasegawa*, ¶[9]; *Michel*, Abstract; *Beals*, 2; *NXP*, ¶¶[16], [32], [37]).

A POSITA therefore would have been motivated to use *Shinohara*’s monolithic integration method to manufacture and improve *Kuboi*’s imaging device. Lebbby, ¶225. The combination would have involved the use of a known technique—forming the pixel region and all associated electronic circuitry on the same substrate—to improve a similar device—*Kuboi*’s imaging device—in the same way, namely, by improving manufacturing reliability, reducing manufacturing cost and package size, reducing signal attenuation, reducing noise, and improving high-bandwidth performance of *Kuboi*’s device. *Id.*

A POSITA would have had a reasonable expectation of success in implementing *Shinohara*'s teachings for manufacturing *Kuboi*'s imaging device. Lebbby, ¶226. Given that both *Kuboi* and *Shinohara* disclose similar imaging devices that include a pixel region and a peripheral circuit portion, manufacturing *Kuboi*'s pixel region and associated electronic circuitry, including *Kuboi*'s pixel transistors, using *Shinohara*'s techniques would have been well within a POSITA's skill. *Id.* A POSITA would have had a reasonable expectation of success for the *Kuboi-Shinohara* combination because it merely requires combining well-known prior elements and manufacturing methods taught by *Shinohara*. *Id.*

5. Independent Claim 1

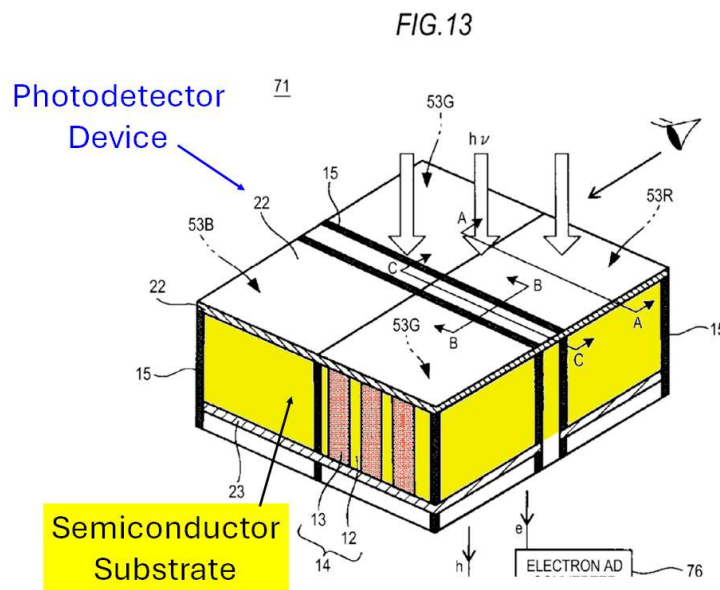
- a. [1pre]: “A photodetector device formed in or on a semiconductor substrate and provided with deliberately formed in-pillar holes comprising:”

To the extent the preamble is limiting, *Kuboi* discloses it. Lebbby, ¶¶102-105. *Kuboi*'s imaging device is a photodetector that includes photoelectric conversion portions formed on a silicon substrate. *Kuboi*, Abstract, ¶¶[11]-[13], [55], [181].

Kuboi's “imaging device includes: pixels each including a hybrid photoelectric conversion.” *Kuboi*, Abstract. Specifically, the “imaging device” includes “a pixel region in which a group of red, blue, green, and green pixels ... are arranged in a two-dimensional array.” *Kuboi*, ¶[181]. The “respective pixels 53R, 53G, and 53B include the hybrid photoelectric conversion portion 14.” *Id.*

Kuboi's imaging device is a photodetector device because it includes a photoelectric conversion portion that receives light and in response generates electron hole pairs. Lebbby, ¶103; *Kuboi*, ¶[64]. *Kuboi*'s "hybrid photoelectric conversion portion 14 includes a semiconductor layer 12 formed of silicon and a plurality of organic material layers 13 embedded in the semiconductor layer 12." *Kuboi*, ¶¶[55], [181]. Thus, *Kuboi*'s photodetector device is formed in or on a semiconductor substrate (i.e., Figure 13's layer 12 or Figure 15's layer 211).

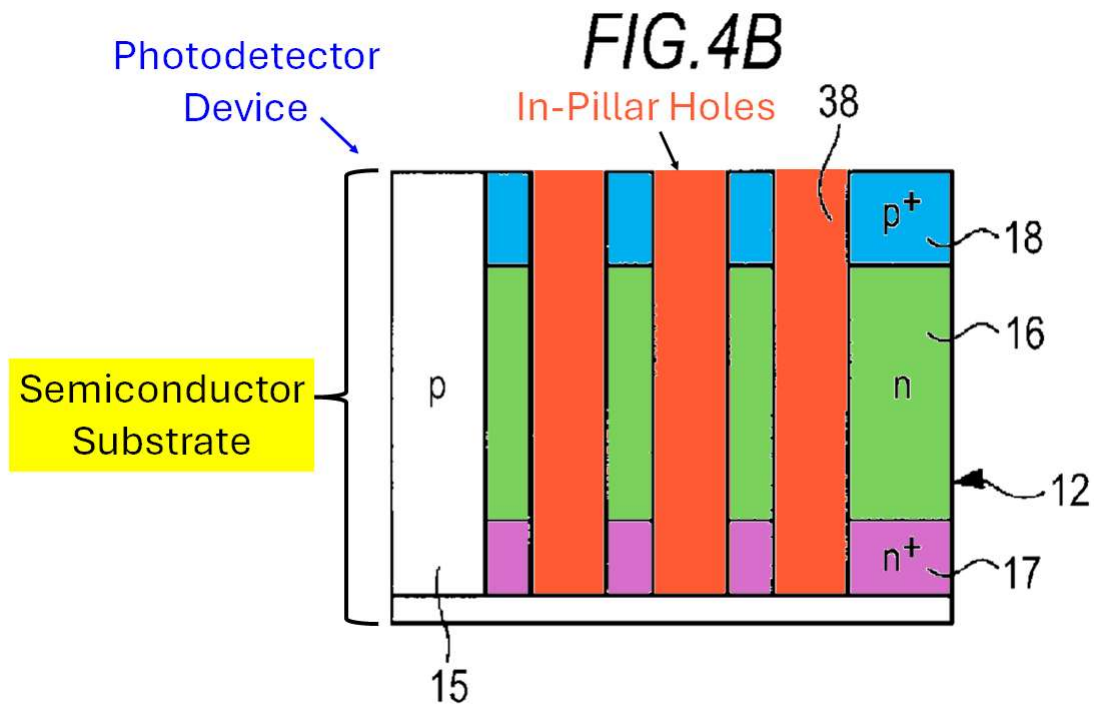
Lebbby, ¶104. *Kuboi*'s photodetector device is shown below:



Kuboi, Fig. 13.

Kuboi discloses an exemplary pixel manufacturing method in which a semiconductor substrate including "element separation region 15" and doped semiconductor regions, including " n^+ -type semiconductor region 17

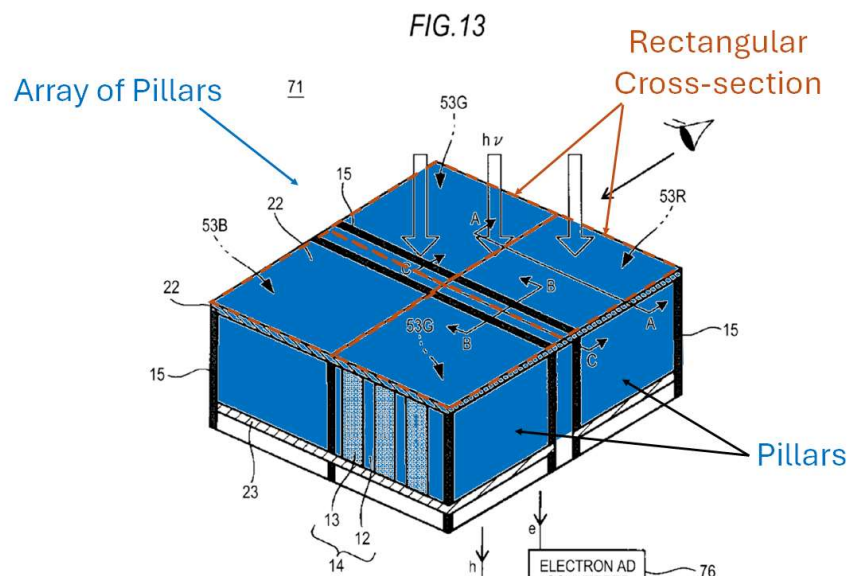
(corresponding to the front surface side), a **n-type semiconductor region 16** (corresponding to an intermediate region), and a **p⁺-type semiconductor region [18]** (corresponding to the rear surface side) are formed.” *Kuboi*, ¶[71]. “[H]oles 38 are formed at necessary intervals” where each “hole 38 such as a trench or a via extend[s] from the p⁺-type semiconductor region 18 to the n⁺-type semiconductor region.” *Kuboi*, ¶[72]. Thus, as shown below, *Kuboi*’s **photodetector device** includes deliberately formed **in-pillar holes**. VI.A.5.i ([1d]); Lebby, ¶105.



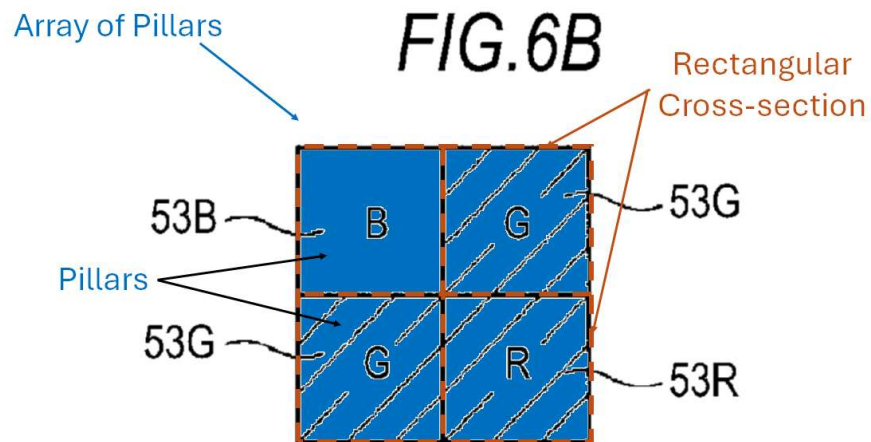
Kuboi, Fig. 4B.

- b. [1a]: “a laterally extending **array of pillars** that have **rectangular cross-sections** in a horizontal plane;”

Kuboi discloses [1a]. Leebby, ¶¶106-109. *Kuboi*’s “imaging device” includes “red, blue, green, and green **pixels** ... arranged in a two-dimensional array.” *Kuboi*, ¶¶[181], [90]. As illustrated below, each **pixel** constitutes a **pillar** (bounded by **sides of a rectangle**) in the two-dimensional **array of pillars** (“laterally extending ... in a horizontal plane”). Leebby, ¶107. Furthermore, each **pillar** has a **rectangular cross-section**. *Id.*

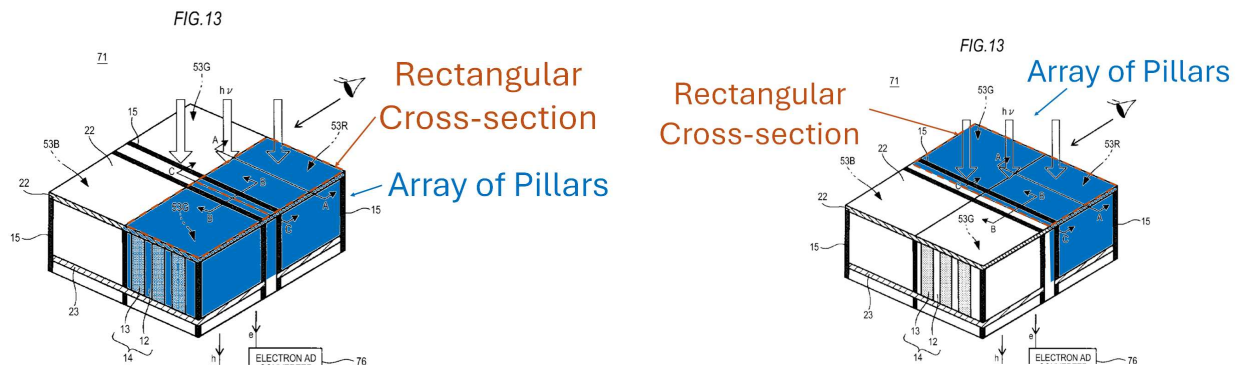


Kuboi, Fig. 13 (perspective view).

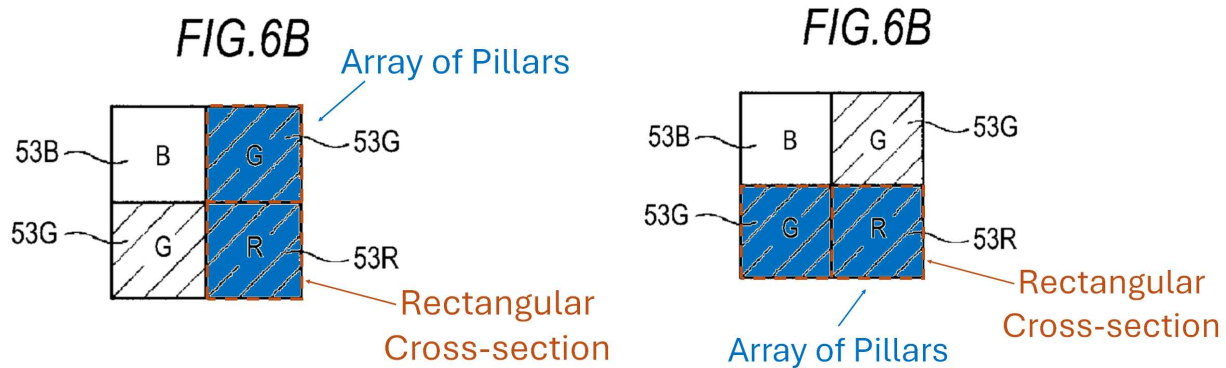


Kuboi, Fig. 6B (horizontal plane view).

Although pixels 53B/53G/53G/53R are illustrated as forming a 2-row by 2-column array of pillars, a subset of these pixels may also form a 2-row by 1-column or a 1-row by 2-column array. Lebbay, ¶108. This is shown below.



Kuboi, Fig. 13 (2x1 array, left; 1x2 array, right).



Kuboi, Fig. 6B (2x1 array, left; 1x2 array, right).

To the extent Patent Owner argues that *Kuboi*'s pixels have a square shape, a square is a rectangle that has sides of equal length. Lebbly, ¶109 (citing Ex-1058, 17, 23).

- c. [1b.1]: “wherein said **array of pillars** comprises: a **first doped semiconductor material**; an **intermediate semiconductor material**; and **solid dielectric** between at least portions of **sidewalls** of adjacent **pillars** of said **array of pillars**;

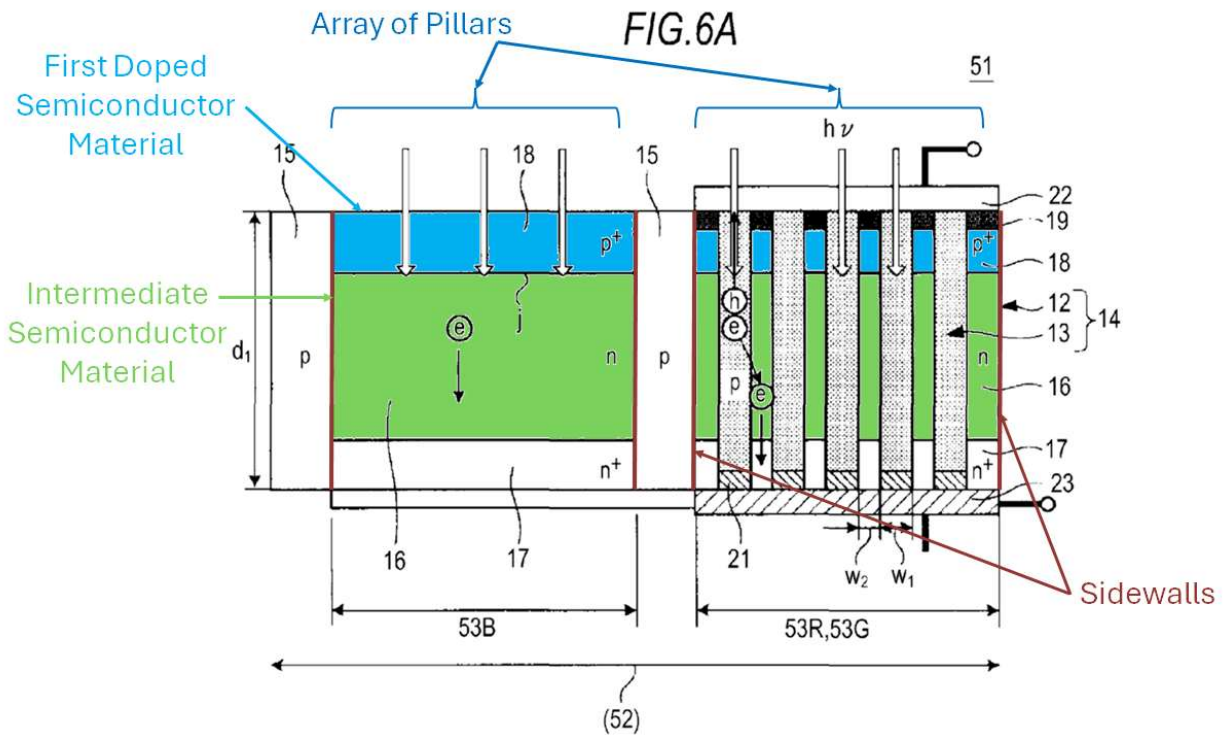
The *Kuboi-Shinohara* combination renders obvious [1b.1]. Lebbly, ¶¶110-132. *Kuboi*'s “imaging device” includes “pixel region 52 in which a **group of pixels** made up of a blue (B) pixel 53B, a red (R) pixel 53R, a green (G) pixel 53G, and a green (G) pixel 53G are arranged in a two-dimensional array.” *Kuboi*, ¶[90]. In blue pixel 53B (i.e., a **pillar**), “a **p⁺-type semiconductor region 18**, an **n-type semiconductor region 16**, and a **n⁺-type semiconductor region 17** are formed in that order from the light incident surface of the semiconductor layer 12 toward the opposite surface.” *Kuboi*, ¶[91]; *see also Kuboi*, ¶¶[71], [181]. In red pixel 53R and

green pixels 53G (i.e., pillars), “the same p⁺-type semiconductor region 18, n-type semiconductor region 16, and n⁺-type semiconductor region 17 are formed.”

Kuboi, ¶[91]; Lebbby, ¶111.

Kuboi’s silicon “semiconductor layer 12 is implanted with impurities ... [to form] a n⁺-type ... region 17 having higher concentration [of impurities] than the n-type ... region 16, and a semiconductor region 18 of second conductivity type (for example, p⁺ type) having higher concentration [of impurities] than the n-type ... region 16.” *Kuboi*, ¶¶[55]-[56]; see also *Kuboi*, ¶¶[111], [151], [7]. A POSITA would have understood that the process of implanting impurities into silicon material is known as “doping,” and as a result, region 18 is a “first doped semiconductor material.” Lebbby, ¶¶112-114 (citing Ex-1067, 4 (“doping”); Ex-1063, 37; Ex-1020, 4), 116.

Kuboi’s first doped semiconductor material (region 18), intermediate semiconductor material (region 16), and sidewalls are illustrated below:



Kuboi, Fig. 6A.

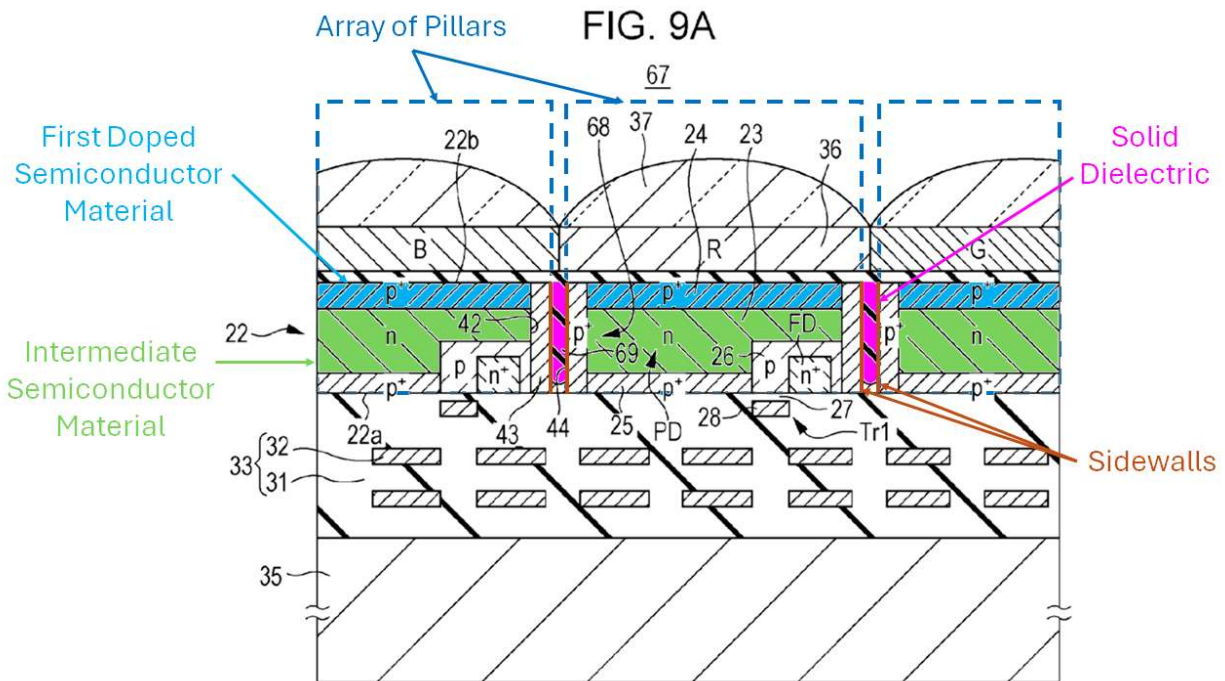
Kuboi's pixels are "separated by an element separation region 15" and in one example, "the element separation region 15 is formed by a p-type semiconductor region." Kuboi, ¶¶[55], [56], [71], [91], [182]. Thus, Kuboi contemplates region 15 formed of semiconductor or other materials such as a solid dielectric. Lebbby, ¶115. To the extent Patent Owner argues that Kuboi does not disclose or suggest a solid dielectric between at least portions of sidewalls of adjacent pillars, Shinohara discloses this. Lebbby, ¶117.

Shinohara's "imaging device" includes "a plurality of unit pixels each having a photodiode PD functioning as a photoelectric conversion portion and a plurality of pixel transistors ... regularly arranged in a two-dimensional matrix." *Shinohara*, ¶[58]. *Shinohara*'s photodiode PD includes "a first conductivity type functioning as both photoelectric conversion and charge storage, i.e., an n-type charge storage region 23," and "second conductivity types ..., i.e., p-type semiconductor regions 25 and 24." *Id.* *Shinohara*'s region 24 corresponds to the "first doped region" and region 23 corresponds to the "intermediate semiconductor material." Lebbby, ¶118.

Shinohara's imaging device includes "element isolation region 68 for isolating pixels [that] is formed such that the p-type semiconductor layer 43 is provided in the trench 42 by an epitaxial growth, and an insulating film 69 is filled in the void 44 inside this p-type semiconductor layer 43." *Shinohara*, ¶[90].

Insulating film 69 may include "a silicon oxide film or a silicon nitride film."

Shinohara, ¶[91]. A POSITA would have understood that silicon oxide and silicon nitride films are solid dielectric materials and therefore solid dielectrics. Lebbby, ¶¶119-123 (citing Ex-1020, 34-35; Ex-1063, 20-21, 23, 30, 33). These features are illustrated below:



Shinohara, Fig. 9A. *Shinohara*'s **solid dielectric** is disposed between portions (i.e., at least part of the height) of **sidewalls** of **adjacent pillars** (**adjacent pixels** B and R or **adjacent pixels** R and G).

As explained above, a POSITA would have found it obvious to implement *Shinohara*'s **solid dielectric** (**insulating film 69**) in *Kuboi*'s p-type isolation region. Lebbby, ¶¶124-132. This would have resulted in modifying *Kuboi*'s imaging device to include a “**solid dielectric** between at least **portions of sidewalls** of **adjacent pillars** of said **array of pillars**.” Lebbby, ¶124.

**d. [1b.2]: “a second doped semiconductor material;
wherein:”**

Kuboi discloses [1b.2]. Lebbby, ¶¶133-134. In blue pixel 53B, region 18, region 16, and region 17 “are formed in that order.” *Kuboi*, ¶¶[91], [71], [181]. Similarly, in red pixel 53R and green pixels 53G, “the same” region 18, region 16, and region 17 “are formed.” *Kuboi*, ¶¶[91], [71], [181]. As discussed above, region 17 is formed by implanting semiconductor layer 12 with impurities. *Kuboi*, ¶¶[55]-[56]; VI.A.5.c. Furthermore, “the process of introducing impurity atoms into pure silicon” results in a “doped ... material.” Ex-1067, 4 (“doping”); Ex-1063, 37; Ex-1020, 4; VI.A.5.c ([1b.1]). Thus, *Kuboi*’s region 17 (illustrated below) is the claimed “second doped semiconductor material.”



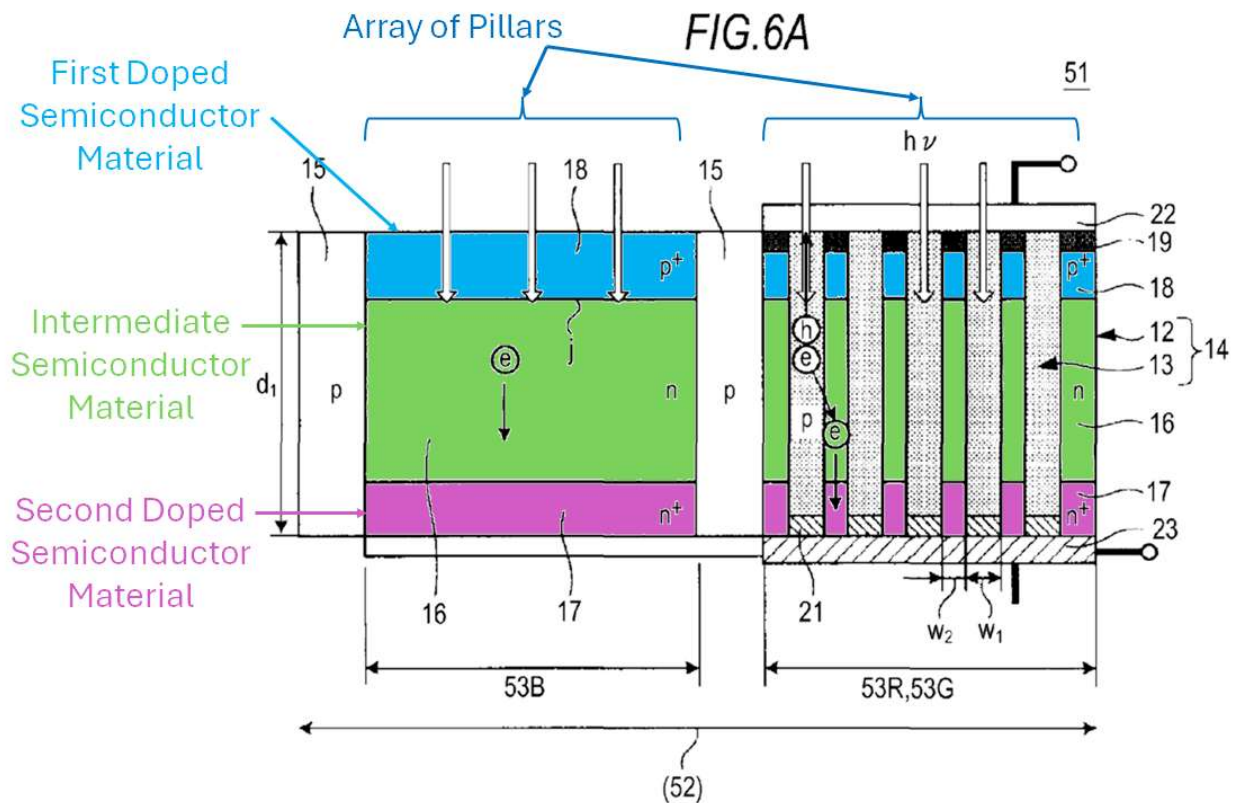
FIG. 6A

Second Doped Semiconductor Material

Kuboi, Fig. 6A.

- e. [1c.1]: “the **intermediate semiconductor material** is between said **first** and **second** doped semiconductor materials;”

Kuboi discloses [1c.1]. Lebby, ¶¶135-136. *Kuboi* discloses that region 18, region 16, and region 17 “are formed in that order from the light incident surface of the semiconductor layer 12 toward the opposite surface.” *Kuboi*, ¶¶[91], [55]-[56], [71], [181]; VI.A.5.d ([1b.2]). Because layers 18, 16, and 17 are formed “in that order,” *Kuboi*’s intermediate semiconductor material (region 16) is located between its first doped semiconductor material (region 18) and its second doped semiconductor material (region 17):



Kuboi, Fig. 6A.

- f. [1c.2]: “the **first** and **second** doped semiconductor materials are doped to opposite semiconductor types;”

Kuboi discloses [1c.2]. Leiby, ¶¶137-138. Kuboi’s **region 18**, **region 16**, and **region 17** are formed in semiconductor layer 12. Kuboi, ¶¶[91], [55]-[56], [71], [181]; VI.A.5.e ([1c.1]). Because the first doped semiconductor material is **p⁺-type semiconductor region 18** and the second doped semiconductor material is the oppositely doped **n⁺-type semiconductor region 17**, Kuboi discloses [1c.2]. Leiby, ¶138 (citing Yu, ¶[63]).

- g. [1c.3]: “the **intermediate semiconductor material** is less doped than at least one of the **first** and **second** doped semiconductor materials and the degree of doping is the same or different for different positions in the **intermediate semiconductor material**; and”

Kuboi discloses [1c.3]. Lebbby, ¶¶139-149. *Kuboi*’s “semiconductor layer 12 is implanted with impurities.” *Kuboi*, ¶[56]. Layer 12 includes “**region 17** having higher concentration than ... **region 16**.” *Id.* Layer 12 also includes “a **semiconductor region 18** of second conductivity type (for example, **p⁺ type**) having higher concentration than ... **region 16**.” *Id.*

Thus, *Kuboi* discloses that both the first and second doped semiconductor materials (**region 17** and **region 18**) have a higher doping concentration than the intermediate semiconductor material (**region 16**). Lebbby, ¶141. A POSITA would have understood this to mean that the intermediate semiconductor material (**region 16**) is doped less than *Kuboi*’s first and second doped semiconductor materials (**region 17** and **region 18**). *Id.*

A POSITA would have understood that the degree of doping in **region 16** (“**intermediate semiconductor material**”) could only be either the same or different at different positions, as no other possibilities exist. Lebbby, ¶¶142-148 (citing Ex-1063, 37-38; Ex-1020, 4; Ex-1028, 1). *Kuboi* uses “ion implantation” for implanting impurities in semiconductor layer 12. *Kuboi*, ¶¶[7], [134]. After ion

implantation, the dopant concentration varies with depth (x in the figure below) of the layer. Leiby, ¶¶145-148; Ex-1020, 4; Ex-1063, 37-38; Ex-1028, 1.

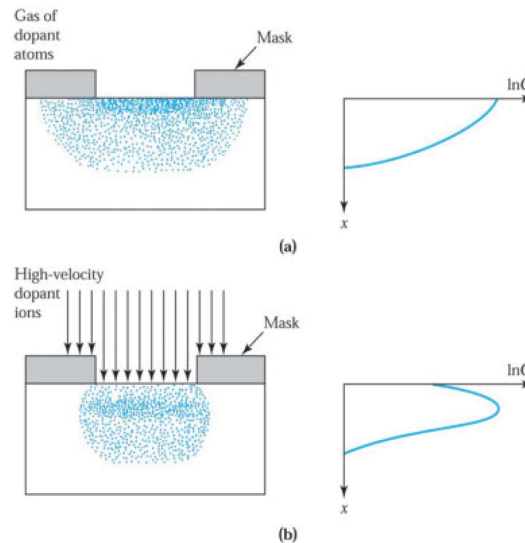
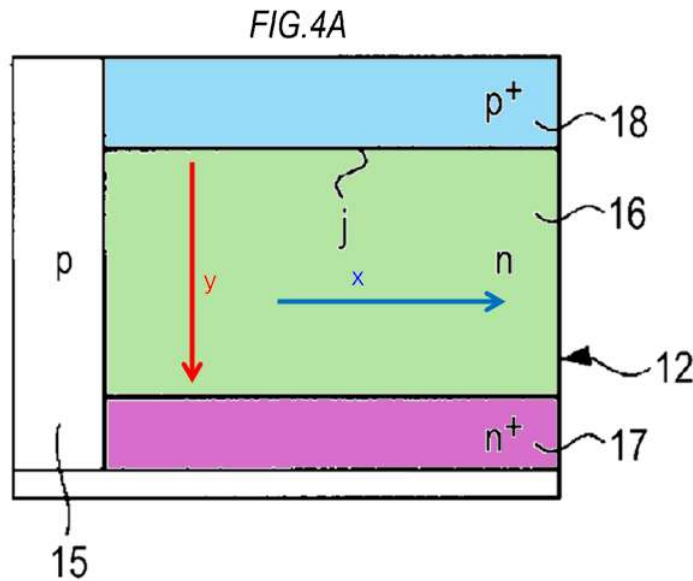


Fig. 1 Comparison of (a) diffusion and (b) ion-implantation techniques for selective introduction of dopants into the semiconductor substrate.

Ex-1063, 38. A POSITA would thus have recognized that the degree of doping in *Kuboi's* n-type region 16 will be different at different positions along the depth (along **line y** below) and the same for different positions along its width (along **line x** below). Leiby, ¶148.



Kuboi, Fig. 4A. *Kuboi* thus discloses that “the degree of doping is the same or different for different positions in the intermediate semiconductor material.”

Lebby, ¶149.

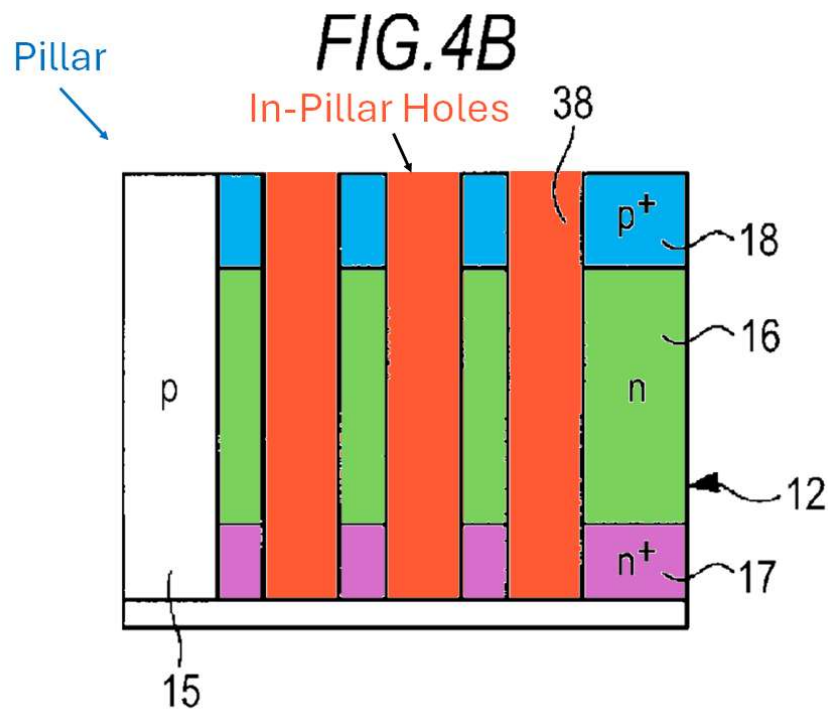
- h. [1c.4]: “each of the first and second doped semiconductor materials and said intermediate semiconductor material comprises Si;”

Kuboi discloses [1c.4]. Lebby, ¶¶150-153. *Kuboi*’s pixel 11 includes “semiconductor layer 12 formed of silicon.” *Kuboi*, ¶¶[55], [70]-[71], [91], [108], [181]. Layer 12 includes “region 17 having higher concentration than ... region 16” and “region 18 of second conductivity type (for example, p⁺ type) having higher concentration than ... region 16.” *Kuboi*, ¶[56]; VI.A.5.g ([1c.3]). Since these regions are created by implanting impurities into silicon, each region comprises silicon. Lebby, ¶¶150-153; *Kuboi*, ¶[3]; see also *Kuboi*, ¶¶[7], [56], [66].

i. [1d]: “one or more deliberately formed **in-pillar holes** with **solid dielectric** therein;”

Kuboi discloses [1d]. Lebby, ¶¶154-160. *Kuboi* discloses that “**hole 38** such as a trench or a via extending from the **p⁺-type semiconductor region 18** to the **n⁺-type semiconductor region** is formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching.” *Kuboi*, ¶¶[72], [13]-[14], [67], [95]. A “plurality of **vertical holes 38** are formed at necessary intervals” and “**holes 38** are formed in a stripe shape.” *Kuboi*, ¶[72]. *Kuboi*’s **holes 38** extend through the **PIN** regions and may be dry-etched using various etching apparatuses. *Kuboi*, ¶¶[72], [95]. Therefore, **holes 38** are deliberately formed. Lebby, ¶155.

Furthermore, each **pixel** of *Kuboi* is a **pillar**. VI.A.5.b ([1a]). **Holes 38** are thus **in-pillar holes** (shown below) because they are formed in a **pillar** (i.e., **pixel 11**). Lebby, ¶156.



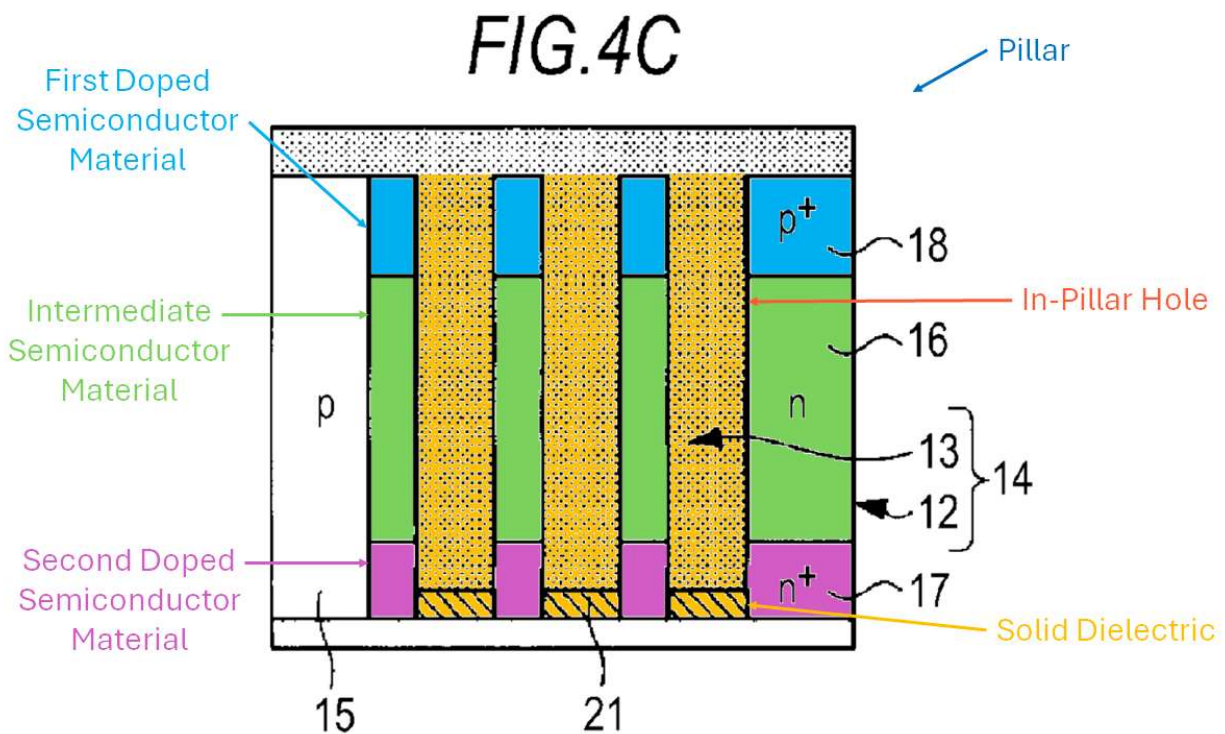
Kuboi, Fig. 4B.

Kuboi also discloses that “an **electron blocking film 21** ... is formed on the bottom portions of the vertical holes 38.” *Kuboi*, ¶¶[73], [91]. “[F]ilm 21 is formed by an insulating film such as, for example, a silicon nitride (Si₃N₄) film [or] a silicon [oxide] (SiO₂) film.” *Kuboi*, ¶[73]. Silicon nitride (Si₃N₄) and silicon oxide (SiO₂) are solid dielectrics. Lebbby, ¶157 (citing Ex-1020, 34-35; Ex-1063, 20-21, 23, 30, 33).

Like the organic material in the holes of the '360 patent, an organic material is deposited to fill the remaining portions of *Kuboi*'s **holes**, thereby forming organic **photoelectric conversion films 13** embedded within the hole. *Kuboi*, ¶¶[73], [58], [85], Fig. 4C; '360 Patent, 49:67-50:5. *Kuboi* discloses that “[a]s the

p-type organic material [is] sensitive to a visible light region, perylene-based compounds, phthalocyanine compounds, quinacridone compounds, porphyrin compounds, merocyanine compounds, and the like can be used.” *Kuboi*, ¶[58]. A POSITA would have understood that phthalocyanine, perylene-based, and porphyrin compounds are solid dielectrics. *Lebby*, ¶¶158-159 (citing Ex-1021; Ex-1022; Ex-1034–Ex-1038).

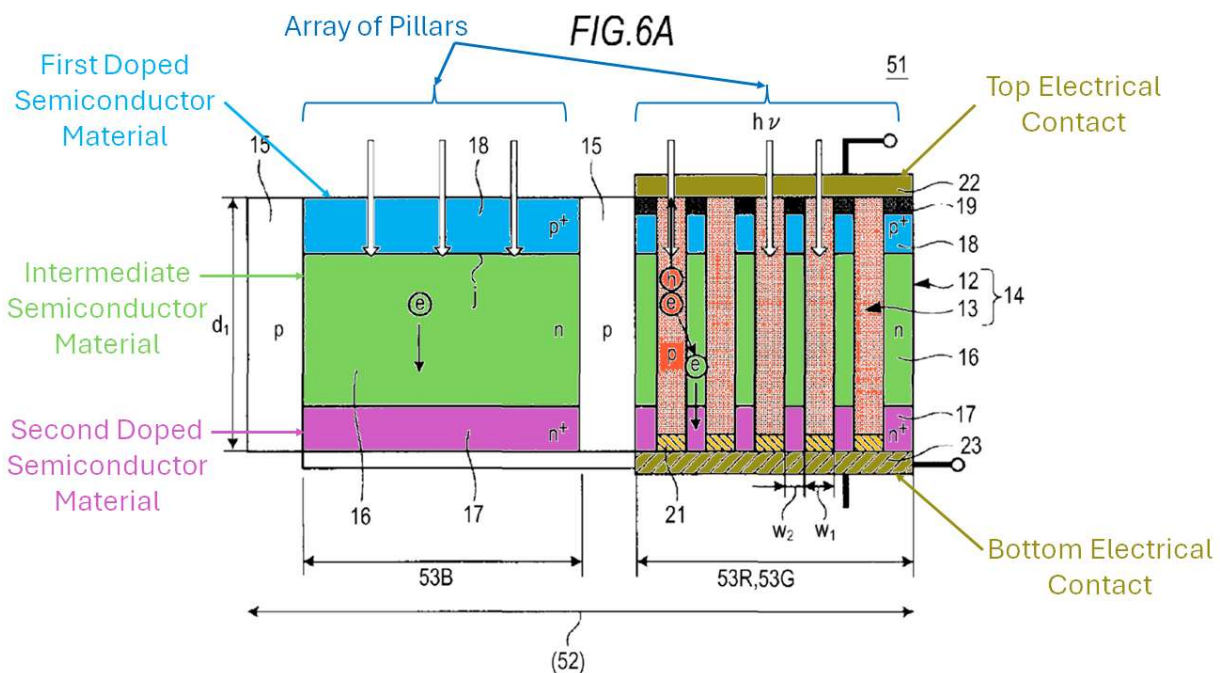
Thus, as illustrated below, **electron blocking film 21** and **photoelectric conversion film 13** together entirely fill **photoelectric conversion portion 14**’s **holes** and are **solid dielectrics**. *Lebby*, ¶160.



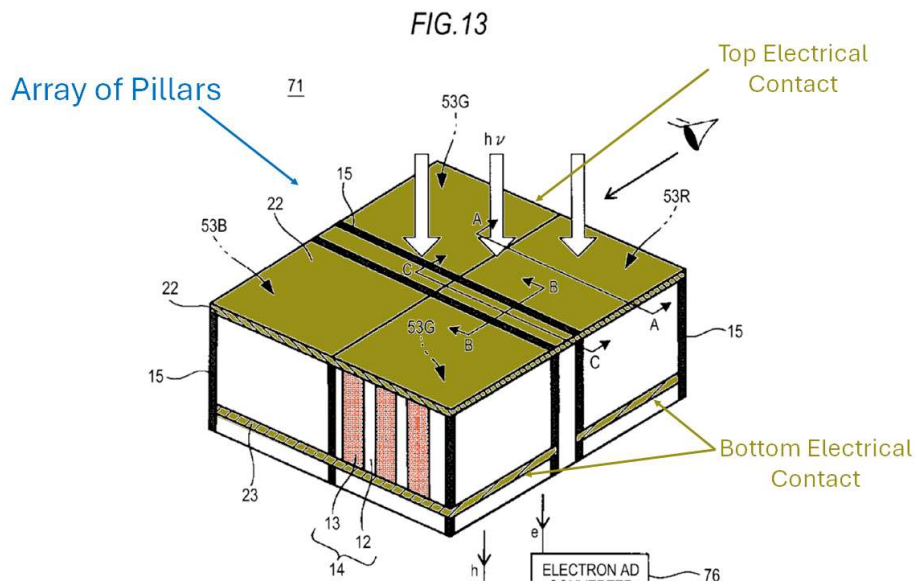
Kuboi, Fig. 4C.

- j. [1e]: “**top and bottom electrical contacts** electrically coupled with said **array of pillars**, wherein said **photodetector device** is configured to respond to **light photons** incident on said **array of pillars** by **photo-generated charge carriers** therein; and”

Kuboi discloses [1e]. Lebbby, ¶¶161-167. “[E]lectrodes 22 and 23 [are] formed on the entire rear and fro[nt] surfaces of the semiconductor layer 12.” *Kuboi*, ¶¶[60], [77], [93], [103]. “[U]pper electrode 22 on the rear surface side is formed by a transparent electrode formed of a transparent conductive film.” *Kuboi*, ¶[60]. And “lower electrode 23 is formed of metal exhibiting ohmic properties.” *Id.* *Kuboi*’s electrodes (“electrical contacts”) are illustrated below from different perspectives:



Kuboi, Fig. 6A.



Kuboi, Fig. 13; Lebbby, ¶¶162-163.

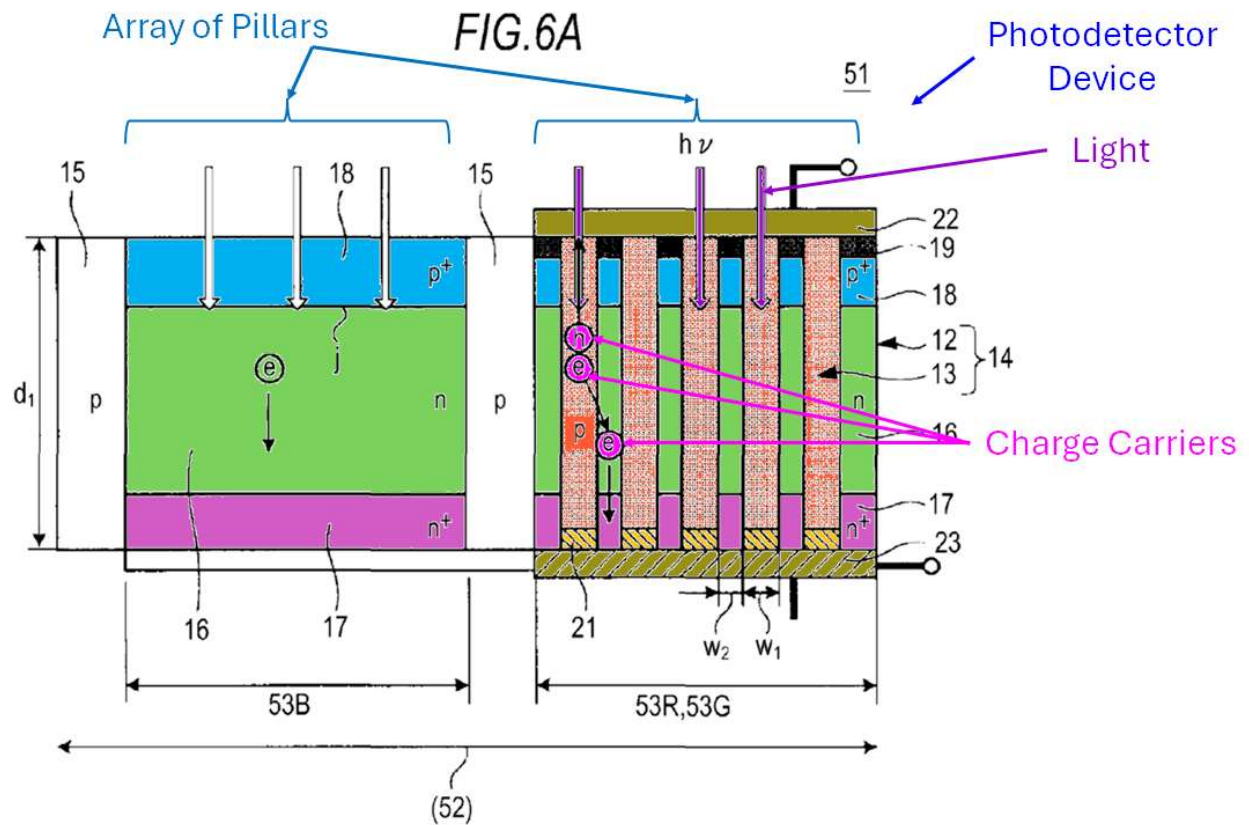
Kuboi's pixel 11 “is configured to include a hybrid photoelectric conversion portion 14 and a plurality of pixel transistors.” *Kuboi*, ¶[55]. “[H]ybrid photoelectric conversion portion 14 includes a semiconductor layer 12 formed of silicon and a plurality of organic material layers 13 embedded in the semiconductor layer 12.” *Kuboi*, ¶¶[55], [91], [181]. Specifically, *Kuboi* discloses that “an organic photoelectric conversion film 13 is deposited so as to be embedded in the vertical holes 38.” *Kuboi*, ¶¶[73], [91]. *Kuboi* explains that “[l]ight *hν* passes through the on-chip microlens to enter the p-type organic photoelectric conversion film 13, in which the light is subjected to photoelectric conversion, whereby *electron-hole pairs* are generated.” *Kuboi*, ¶[64]. Because the photoelectric conversion film 13 is embedded in *pixels 11* of the *imaging device*

(photodetector device), *Kuboi's* photodetector device is configured to generate electron-hole pairs (photo-generated charge carriers) when subjected to light $h\nu$ (light photons incident on said array of pillars). *Kuboi*, ¶¶[107], [64]; Lebby, ¶¶164-165. The generation of charge carriers is illustrated below:

electron-hole pairs (photo-generated charge carriers) when subjected to light

hv (light photons incident on said array of pillars). *Kuboi*, [107], [64]; *Lebby*,

¶¶164-165. The generation of charge carriers is illustrated below:



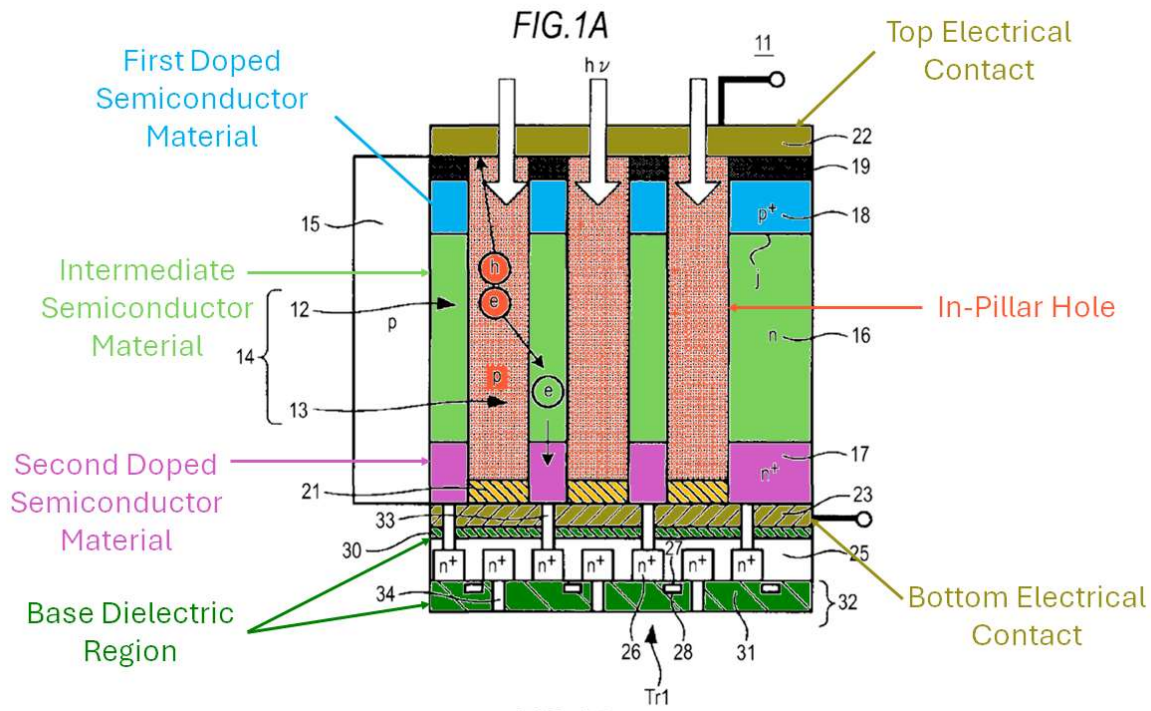
Kuboi, Fig. 6A.

Kuboi discloses that a “necessary voltage is applied between the upper electrode 22 and the lower electrode 23.” *Kuboi*, ¶[64]. “[E]lectrons e ... move from the organic photoelectric conversion film 13 ... toward the semiconductor layer 12 depleted by the applied bias voltage” and “hole h moves toward the upper

electrode 22 through the organic photoelectric conversion film 13 and is discharged through the upper electrode 22.” *Kuboi*, ¶[64]. Because the **holes** generated in *Kuboi*’s pixels (i.e., pillars) move through **electrodes 22**, and because electrons *e* move toward semiconductor layer 12 due to a bias voltage applied between **electrodes 22 and 23**, the **electrodes** are electrically coupled with *Kuboi*’s **array of pillars**. Lebbby, ¶¶166-167.

- k. [1f]: “a **base dielectric region** that is below the array of pillars and comprises substantially solid dielectric material;”

Kuboi alone or in combination with *Shinohara* renders obvious [1f]. Lebbby, ¶¶168-175. *Kuboi*’s “semiconductor region 25 formed of silicon [] is disposed on the front surface side of the semiconductor layer 12, namely under the lower electrode 23 with an insulating film 30 disposed therebetween.” *Kuboi*, ¶[61]. *Kuboi* discloses a semiconductor substrate on which the semiconductor region 25 having pixel transistors, the multilayer wiring layer 32, and the lower electrode 23 are formed. *Kuboi*, ¶[69]. *Kuboi*’s multilayer wiring layer 32 includes a plurality of layers of wiring with an interlayer insulating film 31 disposed therebetween. *Kuboi*, ¶[62]. **Insulating film 30** and/or **insulating interlayer film 31** constitutes the claimed **base dielectric region** because they are disposed below *Kuboi*’s **pillars**. Lebbby, ¶169. *Kuboi*’s **base dielectric region** (films 30 and/or 31) is illustrated below:



Kuboi, Fig. 1A. Although Figure 1A illustrates only one pixel, *Kuboi*'s imaging device includes a plurality of pixels (53R and 53G) arranged as an array of pixels.

VI.A.5.b ([1a]). Pixels 53R and 53G have structures similar to Figure 1A's pixel.

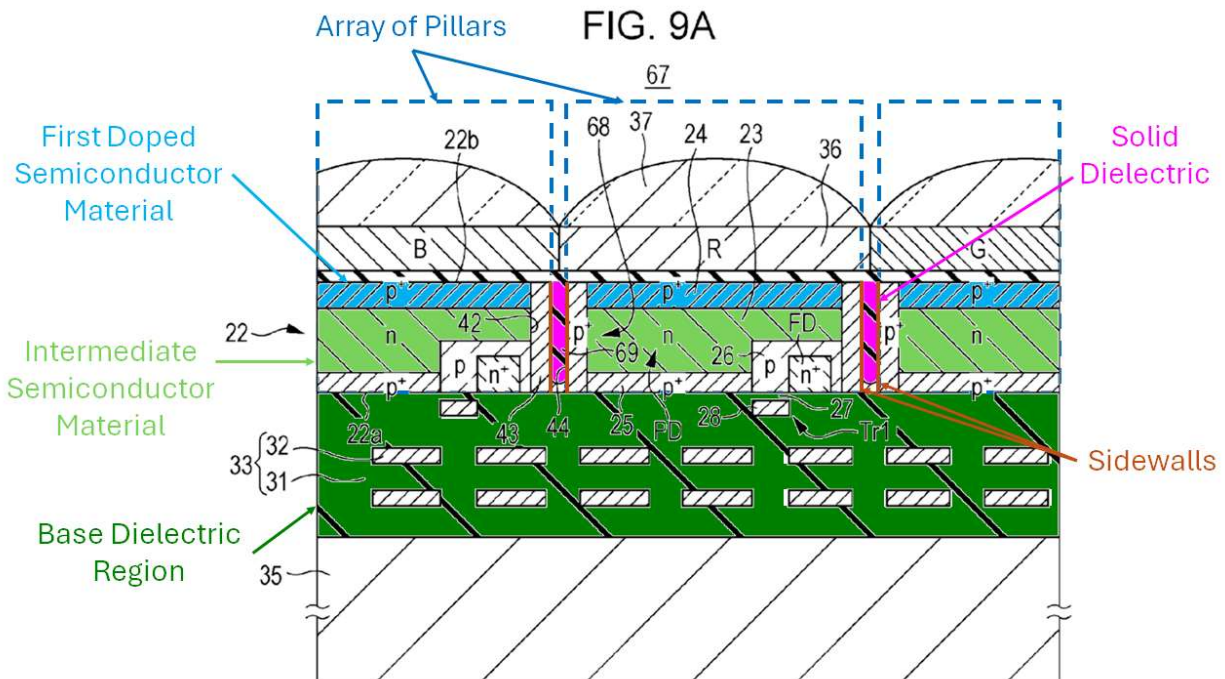
Kuboi ¶[90]. Thus, Figure 1A's base dielectric region is a base dielectric region for *Kuboi*'s array of pixels. Lebbby, ¶173.

Although *Kuboi* does not disclose the material used to make its semiconductor insulating films (30 and/or 31), a POSITA would have understood that such semiconductor insulating films are made of silicon oxide or silicon nitride, which are solid dielectric materials, because these materials can be fabricated using standard silicon fabrication processes and because these materials provide good barriers to impurity and moisture diffusion. Lebbby, ¶¶170-172 (citing

Ex-1020, 34-35; Ex-1059, ¶¶[13]-[14]; Ex-1060, 26:9-14; Ex-1063, 4-5, 20, 34).

Thus, a POSITA would have found it obvious to form *Kuboi*'s **insulating film 30** or **31** of a solid dielectric material like silicon oxide or silicon nitride. Lebbby, ¶171. A POSITA would also have a reasonable expectation of success in making *Kuboi*'s **insulating film 30** or **31** with a solid dielectric material because methods of formation with such materials in semiconductor fabrication were well known in the art before the '360 Patent. *Id.* (citing Ex-1020, 34-35; Ex-1060, 26:9-14; Ex-1063, 20-21, 23).

Shinohara discloses forming multilayer wiring layer 33 including wires 32 and interlayer insulating film 31 on the same substrate 22 on which pixels B, R, G are formed. *Shinohara*, ¶[82]; *see also Shinohara*, ¶¶[68]-[89]. *Shinohara* discloses a “solid-state imaging device.” *Shinohara*, Abstract, ¶[90]. As discussed, a POSITA would have found it obvious to make insulating films for separating wires 32, like *Shinohara*'s insulating film 31, with silicon oxide or silicon nitride, which are solid dielectric materials. Lebbby, ¶¶173-174 (citing Ex. 1020, 24-25; Ex. 1059, ¶¶[13], [14]; Ex. 1060, 26:9-14; Ex. 1063, 4-5). *Shinohara*'s **base dielectric region** is illustrated below.



Shinohara, Fig. 9A. A POSITA would have found it obvious to modify *Kuboi* in view of *Shinohara*, resulting in an imaging device in which the array of pillars (i.e., pixel region) is monolithically integrated with electronic circuits that include active elements for signal processing and transmission. VI.A.5.n ([1i]); VI.A.4. A POSITA would have also found it obvious that monolithically integrating *Kuboi*'s electronic circuits and active elements, as taught by *Shinohara*, would have resulted in a wiring layer having a **base dielectric region** and/or *Kuboi*'s **insulating layer 30** disposed below the array of pillars in *Kuboi*'s monolithically integrated imaging device. Lebbby, ¶175. A POSITA would have had a reasonable expectation of success because *Shinohara* already discloses a monolithically integrated

imaging device having a **base dielectric region (insulating film 30)** disposed below the **array of pillars**. *Id.*; *Shinohara*, Fig. 9A.

- I. **[1g]: “wherein the **pillars** of said **array of pillars**: are laterally spaced center to center by no more than 10,000 nanometers; and have up-down lengths of said **intermediate semiconductor material** in the range of 100-5000 nanometers;”**

Kuboi renders obvious [1g]. *Lebby*, ¶¶176-186. *Kuboi*’s **pixels 11** constitute the claimed **pillars** forming the **array of pillars**. VI.A.5.b ([1a]). Figures 6A/6B “show a solid-state imaging device according to a first embodiment.” *Kuboi*, ¶[90]. In this embodiment, “a blue (B) pixel 53B, a red (R) pixel 53R, a green (G) pixel 53G, and a green (G) pixel 53G are arranged in a two-dimensional array.” *Id.* *Kuboi* discloses that, “[i]n the present embodiment, one pixel has an area of 1.4 μm by 1.4 μm.” *Kuboi*, ¶[94]. *Kuboi* further discloses that “FIG. 13 is a perspective view showing a simplified configuration corresponding to the four pixels of red, blue, green, and green pixels” and that Figure 14B is cross-sectional view taken along line B-B. *Kuboi*, ¶[180]. Figures 13/14B are illustrated below.

FIG.13

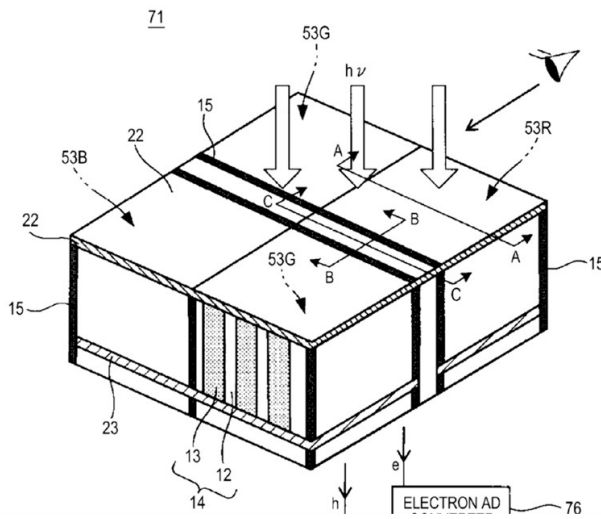
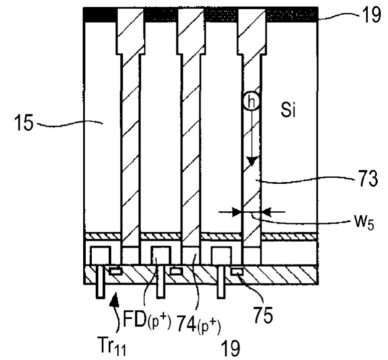


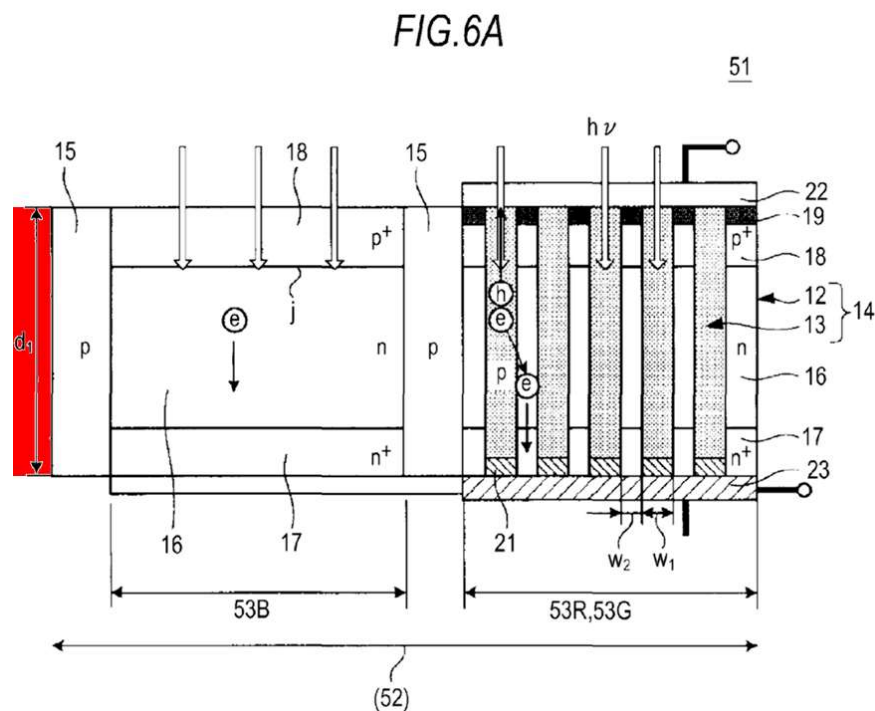
FIG.14B



Kuboi, Figs. 13, 14B. Referencing Figure 14B, *Kuboi* explains that “in the element separation region 15 between the pixels neighboring each other in the vertical direction of the pixel region, wiring layers 73 are formed ... for the movement of holes h of the electron-hole pairs.” *Kuboi*, ¶[182]. A POSITA would have understood from Figure 14B that the wiring layers are formed in the element separation region 15 between *Kuboi*’s pixels. Lebbly, ¶178. A POSITA would have also understood that inclusion of a dielectric region as taught by *Shinohara* in *Kuboi*’s element separation region 15 (VI.A.5.c) would still permit formation of the wiring layers in one or both of the dielectric region or the portions of the element separation region 15 adjacent to the dielectric region. Lebbly, ¶178.

Kuboi's "pixel including the wiring layer has an area of $1.65\text{ }\mu\text{m}$ by $1.65\text{ }\mu\text{m}$." *Kuboi*, ¶[185]. A POSITA would have understood that *Kuboi*'s pixel including the element separation region 15 with the wiring layers has a width of $1.65\text{ }\mu\text{m}$. Lebbby, ¶179. If adjoining pixels (i.e., pillars) each have a width of $1.65\text{ }\mu\text{m}$, then the pitch or center-to-center distance between adjacently located pillars would also be $1.65\text{ }\mu\text{m}$. *Id.* A center-to-center distance of $1.65\text{ }\mu\text{m}$ (or 1650 nm) is "no more than 10,000 nanometers." Lebbby, ¶180.

Thickness d_1 of *Kuboi*'s semiconductor layer 12, as shown below, "is set to about $1.4\text{ }\mu\text{m}$." *Kuboi*, ¶[94].



Kuboi, Fig. 6A. A POSITA would have understood that because region 16 (intermediate semiconductor material) occupies only a portion of thickness d_1 , the

up-down length of **region 16** would be less than 1400 nanometers to accommodate regions 17 and 18 within the thickness **d₁**. Lebbby, ¶¶181-182. And because **region 16** is formed in *Kuboi*'s substrate (*e.g.*, *Kuboi*, ¶[71]), **region 16**'s thickness would be greater than 0 nm. Lebbby, ¶182. Thus, **region 16** would have a thickness ranging between some number greater than 0 nm and a number less than 1400 nm. *Id.* A POSITA would have understood that a PiN diode, like *Kuboi*'s, is designed so that almost complete optical absorption occurs over the i-layer. Lebbby, ¶183 (citing Ex-1063, 17). A POSITA would have also understood that a thicker **region 16** (**intermediate semiconductor material**) is desirable to increase the quantity of absorbed photons. *Id.* A POSITA would, therefore, have found it obvious that *Kuboi*'s **region 16** (**intermediate semiconductor material**) would occupy a majority of the 1400 nm thickness of *Kuboi*'s pixel, placing the thickness of **region 16** (**intermediate semiconductor material**) well within the claimed 100-5,000 nm thickness range. *Id.*

Although *Kuboi*'s figures are not to scale, a POSITA would have understood from Fig. 6A that n-doped layer (**intermediate semiconductor material**) would be approximately 50%—if not more—of thickness **d₁** to maximize photon absorption. Lebbby, ¶184; *Collabo Innovations, Inc. v. Sony Corp.*, 778 F. App'x 954, 960 (Fed. Cir. 2019) (permitting reliance on patent figures directed to a semiconductor image sensing apparatus package where “the references are not ‘completely silent’ on the

relative dimensions”). Thus, a POSITA would have understood *Kuboi*’s intermediate semiconductor material to have a thickness of 700 nm or higher (within the 100-5,000 nm claimed range). Lebbby, ¶184.

The ’360 Patent fails to disclose that the claimed range is critical to the claimed photodetector device’s operation. Thus, at a minimum, because *Kuboi*’s thickness range for its **intermediate semiconductor material** overlaps with the claimed 100-5,000 nm range, *Kuboi* renders the claimed range obvious. Lebbby, ¶¶185-186; *In re Peterson*, 315 F.3d 1325, 1329 (Fed. Cir. 2003) (“[E]ven a slight overlap in range establishes a prima facie case of obviousness.”); *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990); *In re Geisler*, 116 F.3d 1465, 1469 (Fed. Cir. 1997).

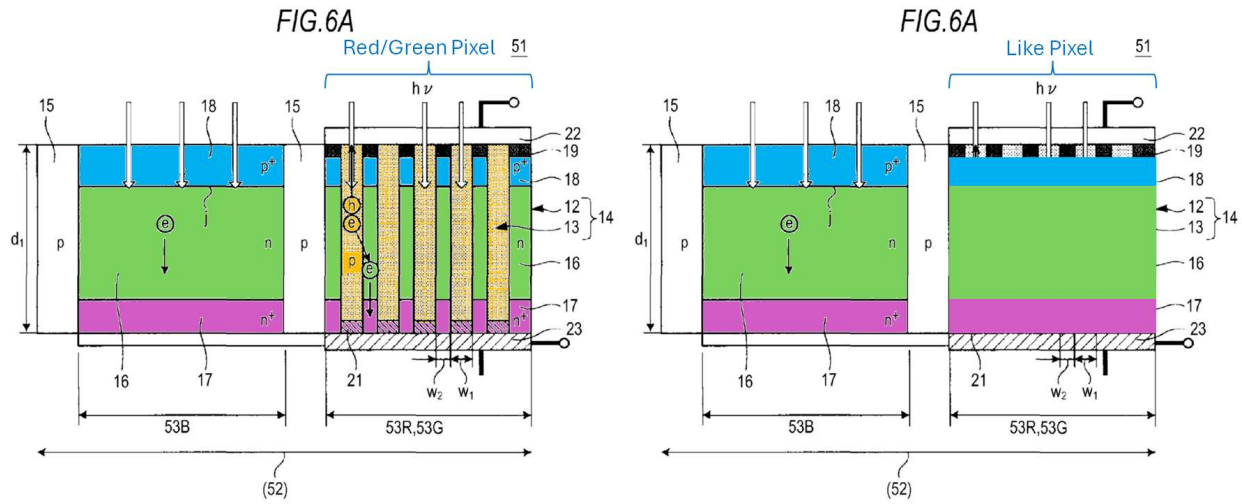
- m. [1h]: “wherein at least said pillars, in-pillar holes, and solid dielectric between at least portions of sidewalls of adjacent pillars of said array of pillars increase photon absorption of said device of incident light by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said one or more in-pillar holes;”

Kuboi discloses, or at a minimum, suggests [1h] based on a POSITA’s knowledge of the state of the art before the ’360 Patent’s priority date and Patent Owner’s statements in the ’360 Patent. Lebbby, ¶¶187-213.

A POSITA would have found *Kuboi* discloses [1h]. *Id.* A POSITA would have understood that the amount of light absorbed, P_{abs} , by a material of thickness

“d” can be determined using the Lambert-Beer formula: $I_0 (1 - e^{-\alpha d})$. Lebbby, ¶188. Here, I_0 is the incident light intensity, α is the material absorption coefficient, and A is the light incidence area. *Id.* (citing, Ex-1070, 23-25). *Kuboi*’s red and green pixels have 1.4 μm deep in-pillar holes filled with phthalocyanine and porphyrin compounds, respectively. *Kuboi*, ¶¶[92], [94]. Compared to silicon, the absorption coefficient of porphyrin compounds is higher in the green light wavelength range of 510-580 nm, and the absorption coefficient of phthalocyanine compounds is at least ten times larger for the red light wavelength range of 620-750 nm. Lebbby, ¶¶189-192. The higher absorption coefficient of *Kuboi*’s organic films increases light absorption by more than 10% over a comparable device lacking in-pillar holes. Lebbby, ¶189.

The figures below illustrate the structure of *Kuboi*’s red or green pixels 53R or 53G (left) and a *like* pixel (right) lacking the in-pillar holes. Lebbby, ¶192. Because both *Kuboi*’s 53R or 53G pixel and the *like* pixel include *Kuboi*’s light shielding film 19, both have the same area of light incidence, defined by the light shielding film openings. *Id.*



The figures below illustrate the structure of *Kuboi's* red or green pixels 53R or 53G (left) and a *hypothetical like* pixel (right) lacking the in-pillar holes and the light shielding film. Lebbly, ¶193. The light incidence area for *Kuboi's* red or green pixels (53R or 53G), as defined by the openings in the light shielding film is about 71% of the light incidence area for the *hypothetical like* pixel. Lebbly, ¶194.

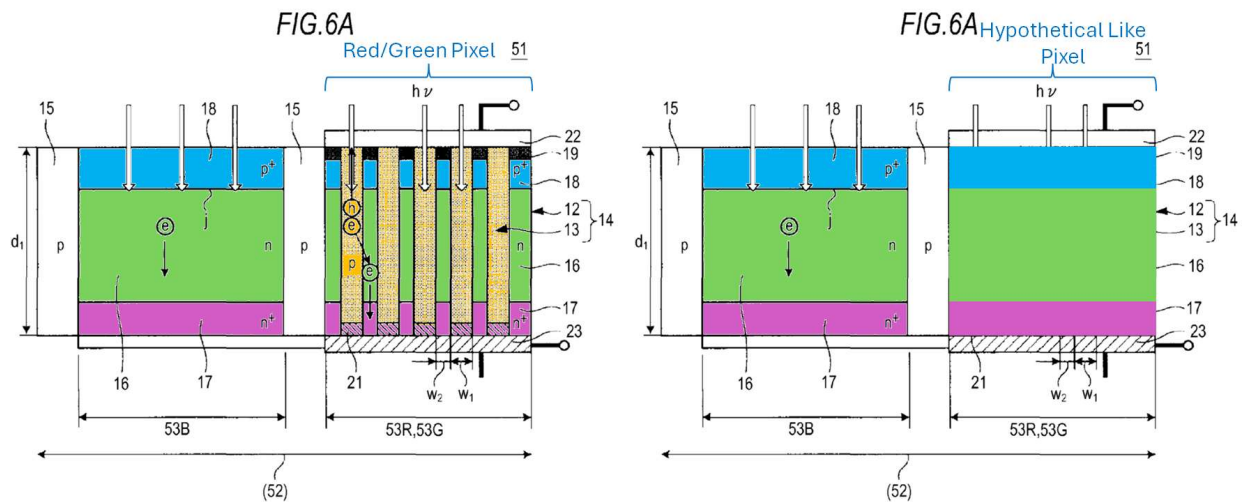


Figure A below illustrates the ratio, $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$, for the green light wavelength range of 490-580 nm (Yu, ¶[23]), where, $P_{\text{abs-organic}}$ represents the

amount of light absorbed by *Kuboi's* green pixel and $P_{\text{abs-silicon}}$ represents the amount of light absorbed by a pixel without in-pillar holes. Leiby, ¶¶195-196.

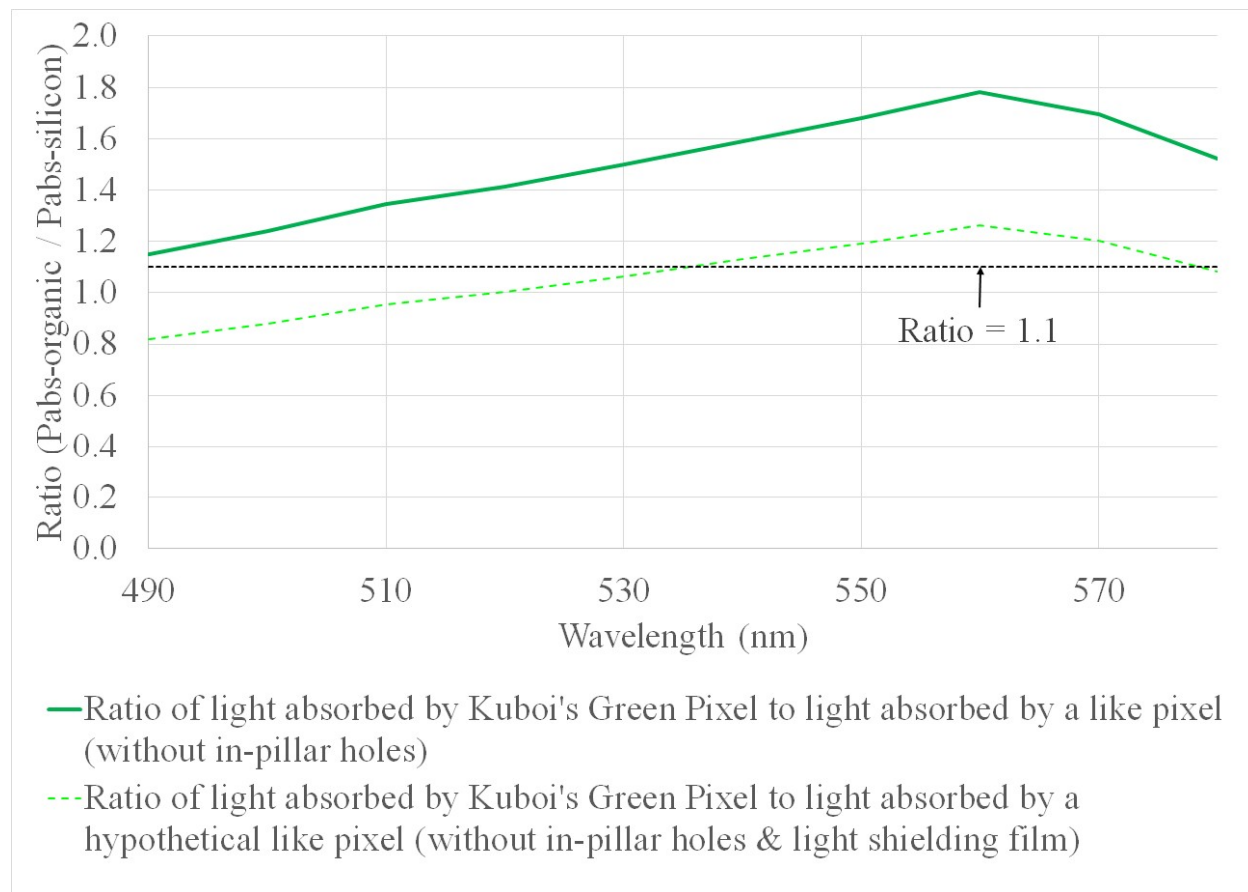


Figure A

In the above figure, the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ for the *hypothetical like* pixel is obtained by scaling the same ratio for the *like* pixel by 71%. Leiby, ¶195. As illustrated, the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ is greater than or equal to 1.1 (shown by the dashed black line) for the entire green light wavelength range for the *like* pixel and for the 540-570 nm wavelength range for the *hypothetical like* pixel. Leiby, ¶¶195-196.

Figure B below illustrates the ratio, $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$, for *Kuboi's* red pixels, in the red light wavelength range of 620-780 nm (Yu, ¶[23]). Leiby, ¶¶197-198.

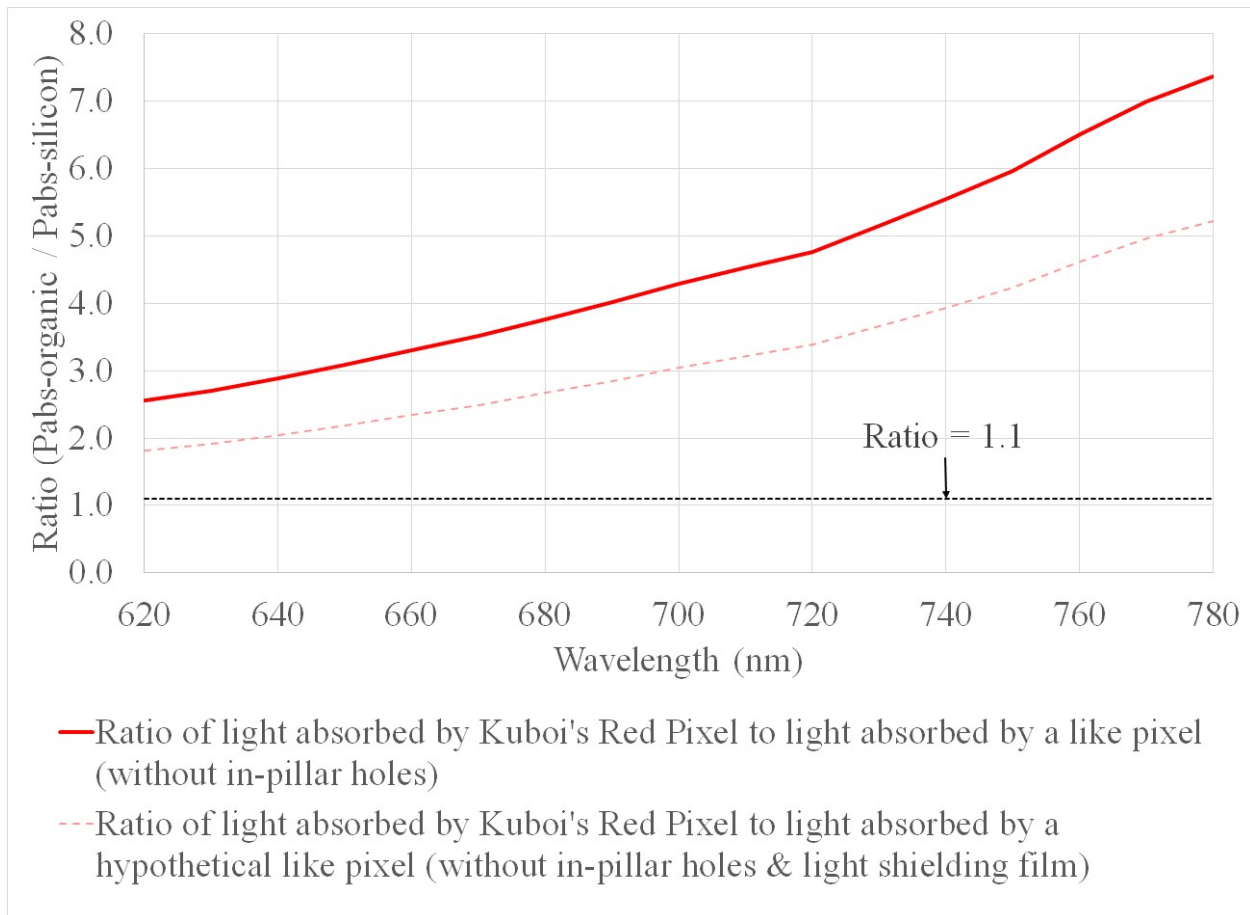


Figure B

As illustrated, the ratio $P_{\text{abs-organic}} / P_{\text{abs-silicon}}$ is greater than or equal to 1.1 for the entire red light wavelength range for both the *like* pixel and the *hypothetical like* pixel. Thus, a POSITA would have understood that *Kuboi's* photodetector device

with in-pillar holes filled with organic material absorbs at least 1.1 times more light relative to a like pixel having no in-pillar holes. Lebbby, ¶¶198-199.

A POSITA would also have found [1h] disclosed in view of Patent Owner's statements in the '360 Patent. Lebbby, ¶¶200-211. The '360 Patent details the cause or causes of the enhancement of the absorption coefficient, explaining:

The cause or causes of the enhancement of the absorption coefficient are believed to include one or more of the following: an increase in optical field concentration, resonance effects, constructive and destructive optical interferences (amplitude and phase) effects, scattering, and *high contrast grating (HCG) effects*. See, e.g. Chang-Hasnain et al, High contrast gratings for integrated optoelectronics, *Advances in Optics and Photonics* 4, 379-440 (2012), hereinafter "Chang-Hasnain." The HCG effects are at the near-wavelength regime (See, Chang-Hasnain) where the optical wavelength in the material of the grating and the optical wavelength in the surrounding material of the grating is the range of the period of the grating.

'360 Patent, 11:39-51 (emphasis added). "The period of the 3D pillar/hole microstructured array can be seen as a 3D high contrast grating, whose period Λ can lie between λ/n_1 where n_1 is the optical refractive index of material M_1 and

λ/n_2 where n_2 is the optical refractive index of material M_2 .” *Id.*, 12:1-5. Further, “[i]f $n_1 > n_2$ then $\lambda/n_1 < \Lambda < \lambda/n_2$.” *Id.*, 12:5-11.

The '360 Patent explains that the HCG effect may explain the high absorption coefficient of semiconductors with in-pillar holes that satisfy the relationship $\lambda/n_1 < \Lambda < \lambda/n_2$. For example, the '360 Patent states:

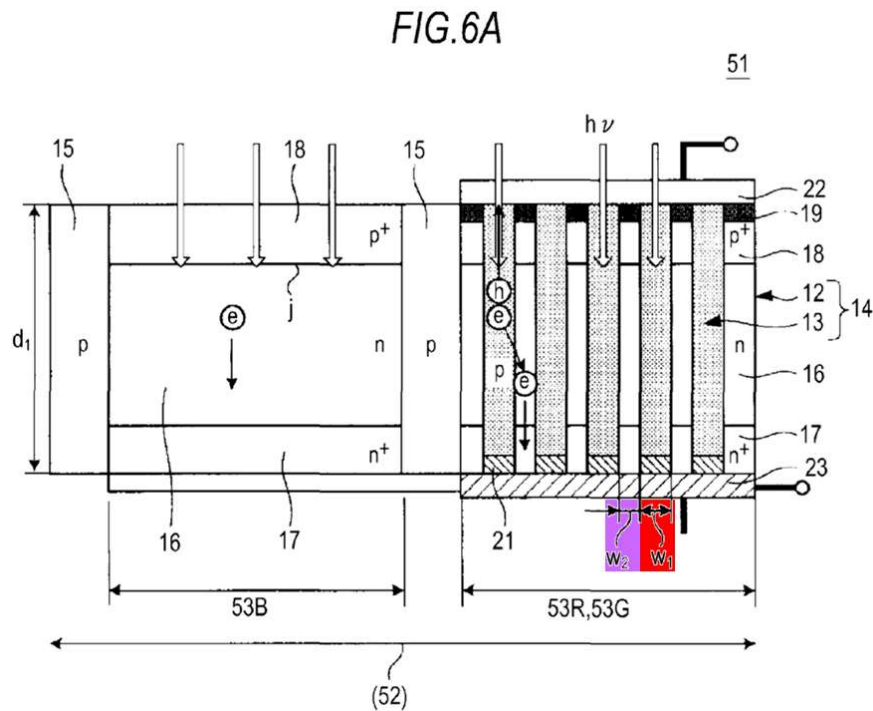
The HCG effect that may explain the high enhancement of the absorption coefficient of the bulk material is that a single or multiple HCG layer (or a single microstructured pillar/hole array layer) due to its resonance effects and/or due to a varying of the microstructured pillar/hole period spacing, the optical signal resonating in the HCG/microstructured pillar-hole array can be directed to propagate in the plane of the HCG/microstructured pillar-hole array rather than normal to the surface. Together with resonance and in-plane propagation this can greatly increase the absorption path length in the HCG/microstructured pillar-hole array.

Id., 12:22-32. Finally, “[u]sing the phenomenon of near-wavelength and also deep-wavelength where the HCG period is much less than the optical wavelength, and the diffraction regime where the HCG period is greater than the optical wavelength (See, Chang-Hasnain) the microstructured pillar-hole-void array can have

enhanced absorption coefficient over the bulk absorption coefficient by a factor of 1.1 to over 100.” *Id.*, 12:36-42.

Patent Owner thus represents in the '360 Patent that a microstructured pillar hole array having microstructure period Λ and satisfying the relationship $\lambda/n_1 < \Lambda < \lambda/n_2$ forms a high contrast grating (HCG). Leebby, ¶204. Patent Owner also represents that if the microstructure pillar hole array forms an HCG, then the physical phenomenon of near-wavelength and deep-wavelength result in an enhanced absorption coefficient of 1.1 to 100 times the bulk absorption coefficient. *Id.*

Applying these representations to *Kuboi*, as illustrated below, *Kuboi* discloses width w1 of photoelectric conversion films 13 is 200 nm and width w2 of semiconductor layer 12 between the photoelectric conversion films is about 50 nm. *Kuboi*, ¶[94].



Kuboi, Fig. 6A. The period Λ or center-to-center distance between holes for *Kuboi* is thus 250 nm. Lebbby, ¶205. Visible light has wavelength in the range 400-700 nm and infrared light has wavelength in the range 750 nm-1000 μm . Lebbby, ¶206 (citing Ex-1012, 4; *Yu*, ¶[23]). The refractive index n_1 of silicon varies from about 3.5 (wavelength 1000 nm) to 5.8 (wavelength 300 nm). Lebbby, ¶206 (citing Ex-1056, 9:43-46, Fig. 4; Ex-1061, 48). The refractive index n_2 of the organic material in *Kuboi*'s holes ranges between 1.5-3.0. Lebbby, ¶207 (citing Ex-1057, 86:35-48, 142:18-25; Ex-1071, 6, Fig. 5, Ex-1072, 13, Fig. 7; Ex-1073, Abstract).

Using the above values for wavelengths and refractive indices, Table A shows the calculated values of λ/n_1 and λ/n_2 for *Kuboi*'s green pixels with porphyrin. *Kuboi*'s 250 nm hole pitch falls in the range λ/n_1 to λ/n_2 for at least part

of the visible light spectrum (400-700 nm wavelengths) and at least part of the near infrared light spectrum (>700 nm wavelengths). Lebbby, ¶¶208. For example, for the 550 nm green light wavelength, λ/n_1 ($550/4.5 = 123$) $< \Lambda$ (250 nm) $< \lambda/n_2$ ($550/2.0 = 275$).

Table A				
λ (nm)	n_1 (Silicon)	n_2 (Porphyrin)	λ/n_1(nm)	λ/n_2 (nm)
400	5.8	1.7	68	235
550	4.5	2.0	123	275
700	3.8	1.6	186	438
750	3.7	1.8	203	417

Similarly, Table B shows the calculated values of λ/n_1 and λ/n_2 for *Kuboi*'s red pixels with phthalocyanine. *Kuboi*'s 250 nm hole pitch falls in the range λ/n_1 to λ/n_2 for at least part of the visible light spectrum (400-700 nm wavelengths) and at least part of the near infrared light spectrum (>700 nm wavelengths). Lebbby, ¶209. For example, for the 650 nm red light wavelength, λ/n_1 ($650/3.9 = 168$) $< \Lambda$ (250 nm) $< \lambda/n_2$ ($650/2.1 = 302$).

Table B				
λ (nm)	n_1 (Silicon)	n_2 (Phthalocyanine)	λ/n_1 (nm)	λ/n_2 (nm)
400	5.8	1.9	68	211
650	3.9	2.1	168	302
700	3.8	1.8	186	389
750	3.7	2.3	203	326

Thus, the stated period of *Kuboi*'s pillar hole array falls within the range λ/n_1 to λ/n_2 for "selected visible and infrared wavelength ranges." Leiby, ¶210.

As a result, based on Patent Owner's representations, *Kuboi*'s pillar hole array forms an HCG. Leiby, ¶211. And, under those same representations, such an HCG would produce an enhanced absorption coefficient of 1.1 to 100 times the bulk absorption coefficient based on the near-wavelength and deep-wavelength phenomena. *Id.* Thus, consistent with Patent Owner's representations, a POSITA would have understood that *Kuboi*'s in-pillar holes increase photon absorption in *Kuboi*'s device by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said one or more in-pillar holes. *Id.*

Patent Owner's representations were also consistent with those of other prior art teachings. Leiby, ¶¶212-213. For example, *Han* (Ex-1051) is consistent with Patent Owner's representations as to the impact of nanoholes on the ultimate

efficiency associated with photon absorption before the '360 Patent priority date.

Han, 7:19-8:5. According to *Han*, the ultimate efficiency for a device having a semiconductor thickness of about 1.4 μm without nanoholes is approximately 0.12, whereas the ultimate efficiency for a similar device having nanoholes is approximately 0.22. *Han*, Fig. 4; Lebbby, ¶212.

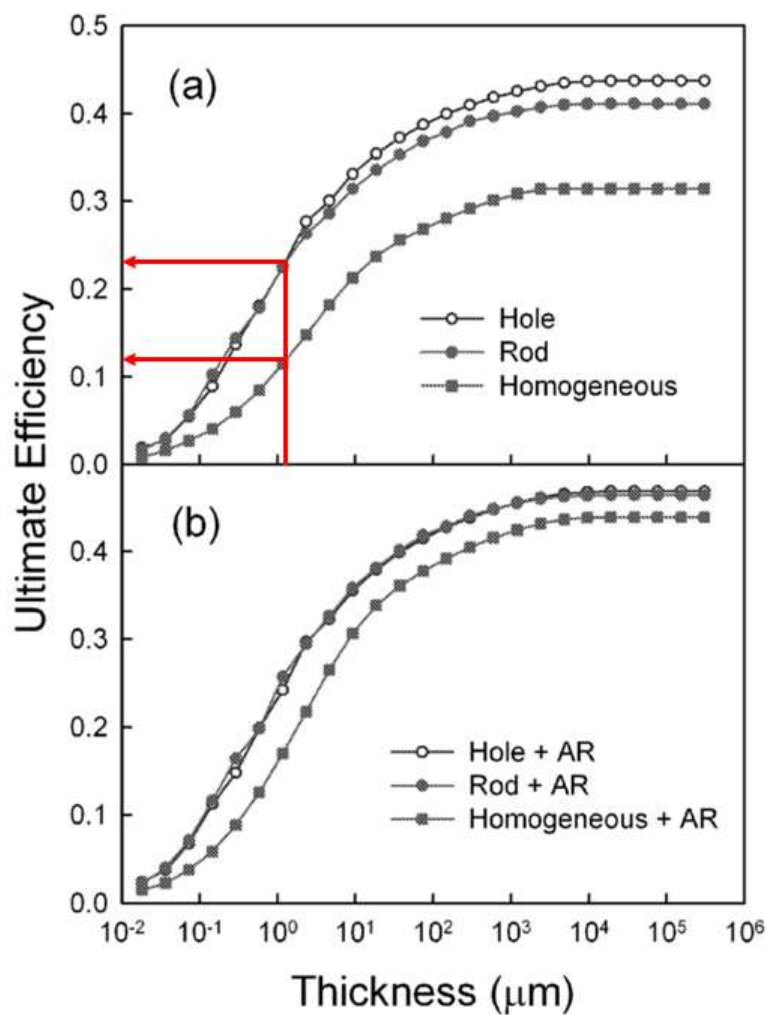


FIG. 4

Han, Fig. 4.

Thus, before the '360 Patent priority date, a POSITA would have understood that *Kuboi*'s 1.4 μm nanohole depth would increase light absorption by a factor of 1.8 ($0.22/0.12 = 1.8$), which is significantly higher than 1.1. Lebbby, ¶¶212-213; *Han*, Fig. 4. Accordingly, based on a POSITA's understanding of the state of the art before the '360 Patent's priority date, a POSITA would have understood that *Kuboi*'s in-pillar 1.4 μm hole depth would increase photon absorption in *Kuboi*'s device by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said one or more in-pillar holes, and even if not readily understood, a POSITA would have found such a result not only obvious but also one having a reasonable expectation of success in achieving this increase because *Kuboi* discloses forming nanoholes of 1.4 μm depth. Lebbby, ¶213.

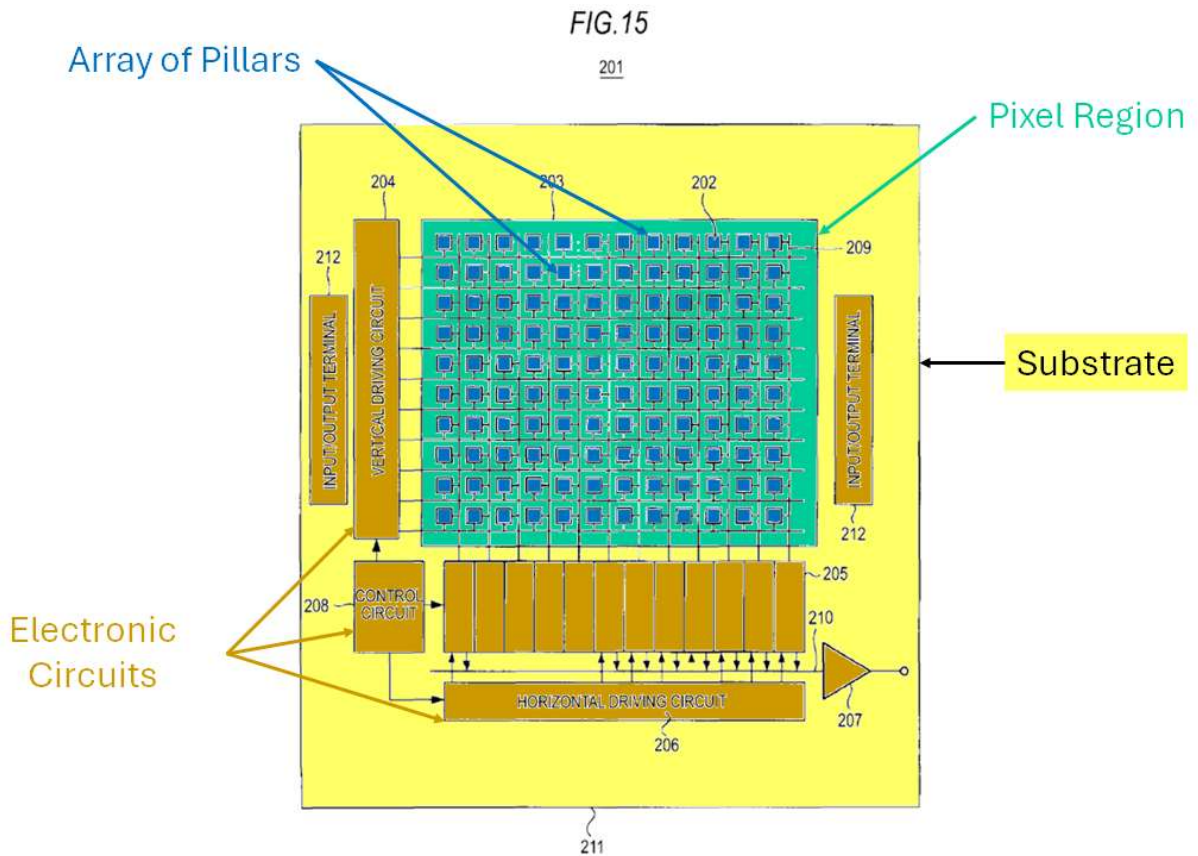
- n. [1i]: “wherein said **array of pillars** is monolithically integrated in or on said **semiconductor substrate** with **electronic circuits** that include active elements for signal processing and transmission.”

First, *Kuboi* discloses [1i]. Second, the *Kuboi-Shinohara* combination renders obvious [1i]. Lebbby, ¶¶214-227.

i. *Kuboi* discloses this limitation.

Kuboi discloses “a simplified exemplary configuration of a CMOS solid-state imaging device.” *Kuboi*, ¶[48]. *Kuboi*'s **imaging device 201** “include[s] a

pixel region (so-called ... imaging region) 203 and a peripheral circuit portion which are provided on a semiconductor substrate 211 (i.e., a silicon substrate).” *Id.* *Kuboi* “pixel [region] and logical circuit portion may be created in advance and be bonded to the semiconductor substrate on which the semiconductor region 25 having the pixel transistors, the multilayer wiring layer 32, the lower electrode 23, and the like are formed.” *Kuboi*, ¶[78] (emphasis added). Thus, *Kuboi* teaches forming the pixel region (i.e., array of pillars) and logical circuit portion (including vertical driving circuit 204, column signal processing circuits 205, horizontal driving circuit 206, output circuit 207, control circuit 208) in advance in or on the same substrate. *Kuboi*, ¶¶[48]-[49]; *Lebby*, ¶215. This single-chip device is shown below:



Kuboi, Fig. 15. *Kuboi*'s disclosure, including Fig. 15 and its method of fabrication, show that the pixels and the peripheral circuit portion are formed on a single substrate, substrate 211. *Kuboi*, ¶¶[70]-[78], [48]-[49]; Lebbby, ¶216. Because the pixel region (including an array of pillars) and logical circuits are formed in or on the same substrate, *Kuboi* discloses monolithically integrating the array of pillars (i.e., pixel region) with electronic circuits that include active elements for signal processing and transmission (control circuit 208 and output circuit 207). Lebbby, ¶216.

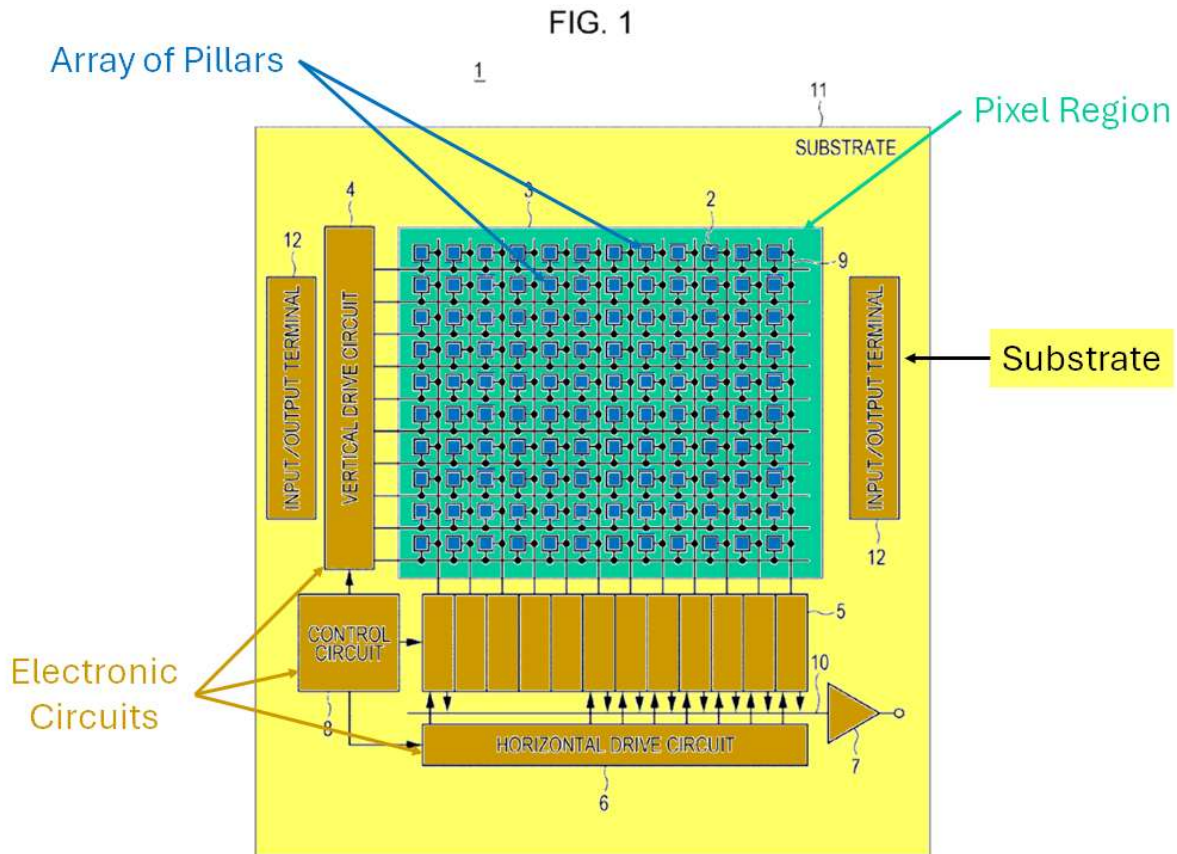
ii. The *Kuboi-Shinohara* combination renders this limitation obvious.

To the extent Patent Owner argues that *Kuboi* does not disclose monolithic integration, the *Kuboi-Shinohara* combination renders [1i] obvious. Lebbby, ¶¶217-227. Referring to its Figure 1, *Shinohara* discloses “one example of a MOS solid-state imaging device applied to each embodiment of the present disclosure.” *Shinohara*, ¶[51]. The imaging device “of this embodiment includes a pixel region (so-called imaging region) 3 in which a plurality of pixels 2 each having a photoelectric conversion portion is regularly arranged in a semiconductor substrate 11, such as a silicon substrate, in a two-dimensional matrix and a peripheral circuit portion.” *Id.* Like *Kuboi*, *Shinohara*’s “peripheral circuit portion includes so-called logic circuits, such as a vertical drive circuit 4, a column signal processing circuit 5, a horizontal drive circuit 6, an output circuit 7, and a control circuit 8.” *Shinohara*, ¶[52].

Shinohara discloses a method for manufacturing the imaging device on a “p-type silicon semiconductor substrate 22.” *Shinohara*, ¶[68]. *Shinohara* teaches forming the photodiodes and the separation regions between the photodiodes on the imaging device on a “p-type silicon semiconductor.” *Shinohara*, ¶¶[68]-[82]. According to *Shinohara*, “the floating diffusion portion,” “transfer gate electrode,” “transfer transistor,” “reset transistor,” “amplification transistor,” and “selection

transistor” are each “formed in the other part of the p-type semiconductor well region” of the substrate. *Shinohara*, ¶[81]. As a result, “the pixel region in which the pixels are arranged in a two-dimensional matrix is formed.” *Id.* *Shinohara* discloses that “the peripheral circuit portion (not shown) by CMOS transistors is formed in the periphery of the pixel region.” *Id.* And “the multilayer wiring layer 33 in which a plurality of layers of the wires 32 is disposed with at least one interlayer insulating film 31 provided therebetween is formed on the surface of the semiconductor substrate 22.” *Shinohara*, ¶[82]

Thus, *Shinohara* discloses forming the pixel region (i.e., including [array of pillars](#)), the peripheral circuit portion, and multilayer wiring layer 33 (i.e. [electronic circuits](#)) on the same substrate 22. *Lebby*, ¶¶218-220. These features are illustrated below.



Shinohara, Fig. 1.

Shinohara thus teaches an imaging device in which the array of pillars (i.e., pixel region) is monolithically integrated with electronic circuits that include active elements for signal processing and transmission (transistors, peripheral circuit portion, and multilayer wiring layer). Lebbby, ¶220.

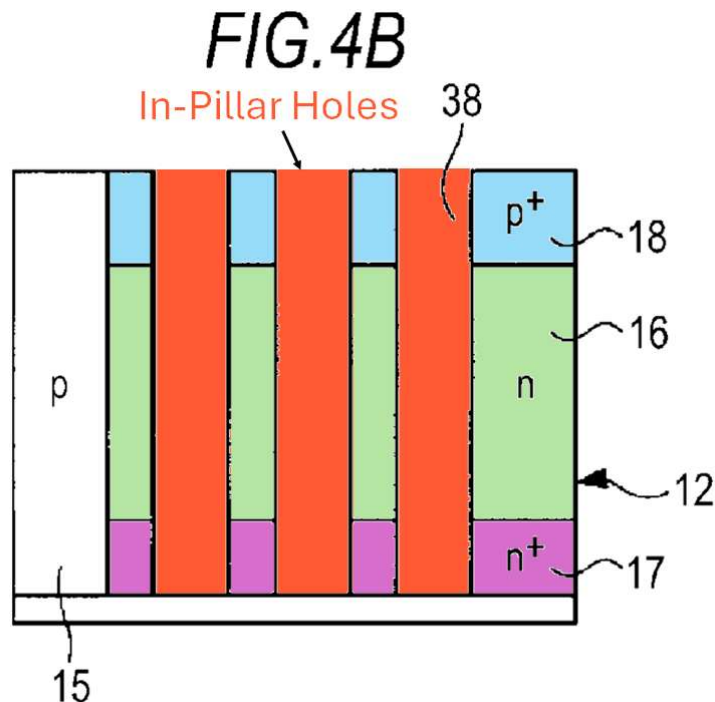
As explained above, a POSITA would have found it obvious to combine *Shinohara*'s teachings with *Kuboi*, resulting in an imaging device in which the array of pillars (i.e., pixel region) is monolithically integrated with electronic

circuits that include active elements for signal processing and transmission.

VI.A.4; Lebbby, ¶¶222-227.

6. **Claim 3: “The photodetector device of claim 1, in which each of said pillars has a plurality of said one or more in-pillar holes.”**

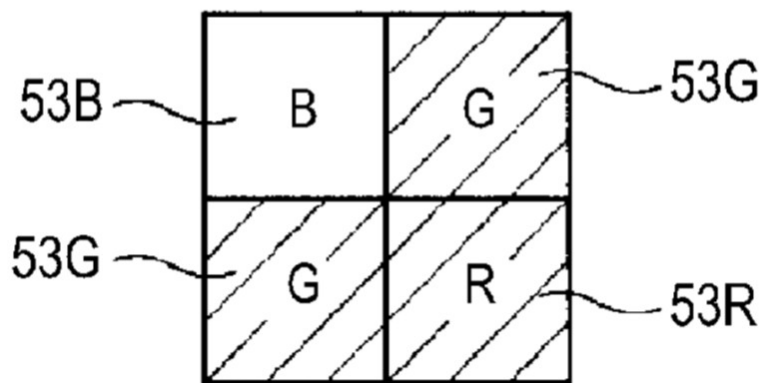
Kuboi discloses this additional limitation. Lebbby, ¶¶228-231. *Kuboi*’s holes 38 extending from region 18 to region 17 are “formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching.” *Kuboi*, ¶¶[72], [13]-[14], [67], [95]; VI.A.7.i ([1d]). “[H]oles 38 are formed at necessary intervals” and “in a stripe shape.” *Kuboi*, ¶[72]. The plurality of in-pillar holes are illustrated below:



Kuboi, Fig. 4B.

Although only one pillar (or pixel) is described above, *Kuboi* uses the same structure for a plurality of pixels. Lebbby, ¶230. For example, *Kuboi*’s “imaging device” includes “primary color filters ... and a pixel region 52 in which a group of pixels made up of a blue (B) pixel 53B, a red (R) pixel 53R, a green (G) pixel 53G, and a green (G) pixel 53G are arranged in a two-dimensional array,” as shown below. *Kuboi*, ¶[90].

FIG. 6B



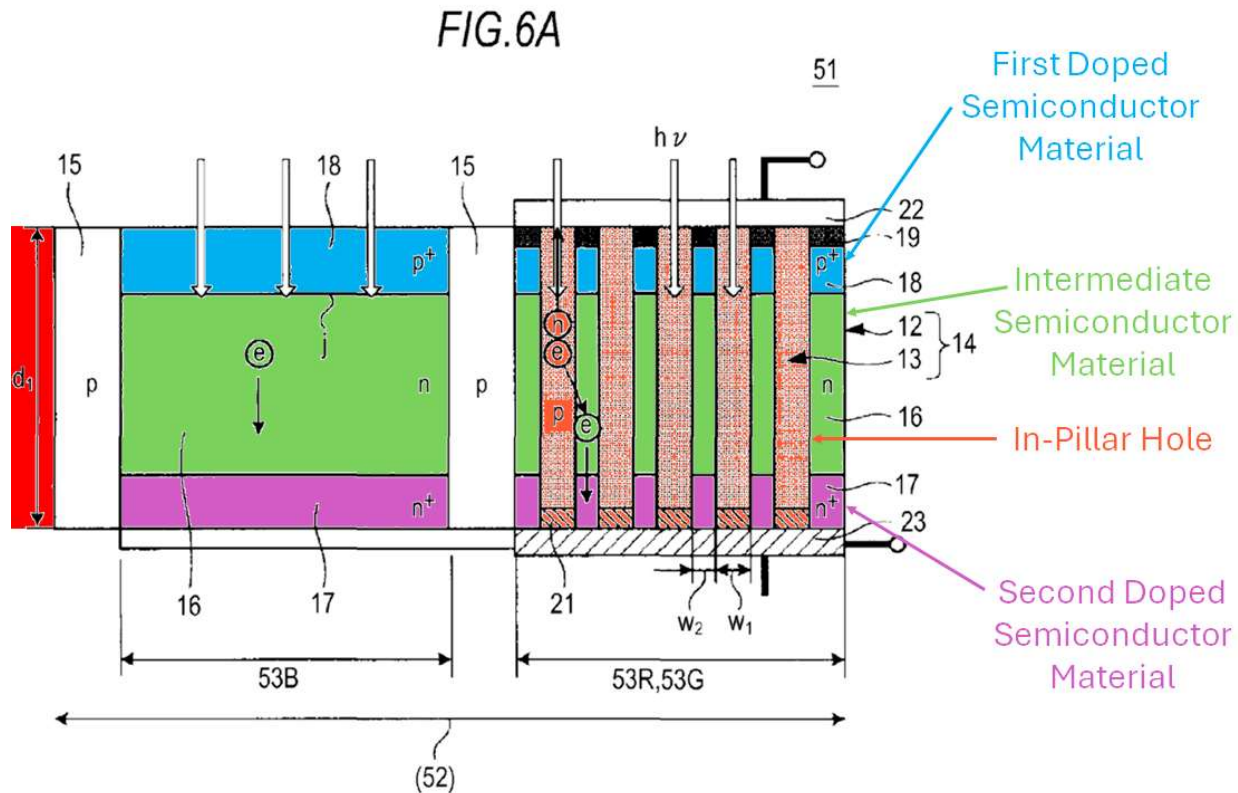
Kuboi, Fig. 6B.

Kuboi discloses that “[t]he processes of manufacturing the red and green pixels in the solid-state imaging device 51 of the first embodiment are the same as those illustrated in FIGS. 4A to 4F.” *Kuboi*, ¶[95]. *Kuboi*’s pillar arrays may include a 2-column, 1-row array; or a 1-column, 2-row array. VI.A.5.b ([1a]). *Kuboi* thus discloses a plurality of pixels (53G, 53R) forming an array of pillars

(2-column, 1-row; or 1-column, 2-row) and each pillar (pixels 53G, 53R) includes a plurality of in-pillar holes 38 (Figure 4B). Lebbby, ¶231.

7. Claim 5: “The photodetector device of claim 1, in which said one or more in-pillar holes extend to a depth in a range of 100-10,000 nanometers.”

Kuboi discloses this additional limitation. Lebbby, ¶¶232-234. *Kuboi* discloses that holes 38 extending from region 18 to region 17 “[are] formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching.” *Kuboi*, ¶¶[72], [13]-[14], [67], [95]. Furthermore, referencing Figures 6A/6B, *Kuboi* discloses that semiconductor layer 12’s thickness d_1 is “about 1.4 μm .” *Kuboi*, ¶[94]. These features are illustrated below:



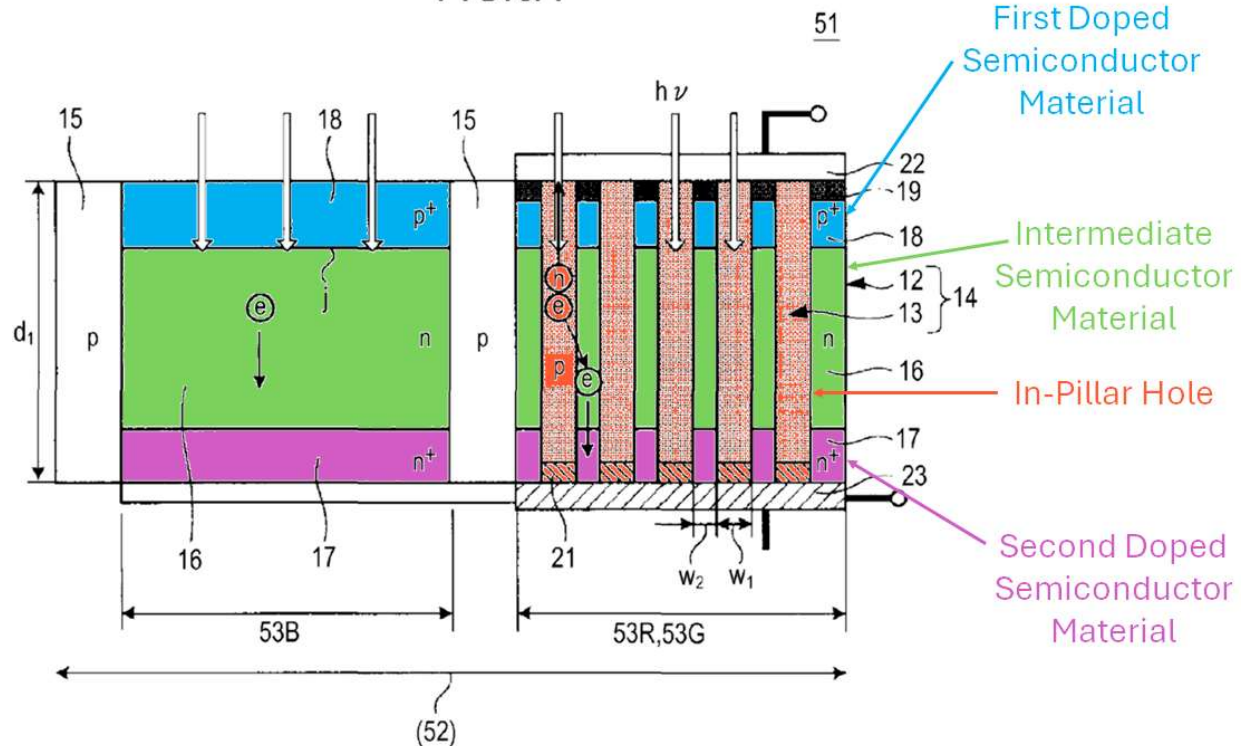
Kuboi, Fig. 6A. The height of each hole is d_1 , which is 1400 nm, and thus *Kuboi*'s one or more in-pillar holes extend to a depth in the claimed range of 100-10,000 nm. Lebbby, ¶234.

8. **Claim 6:** “The photodetector device of claim 1, in which said one or more in-pillar holes extend into said intermediate semiconductor material.”

Kuboi discloses this additional limitation. Lebbby, ¶¶235-236. *Kuboi*'s region 18, region 16, and region 17 “are formed in that order from the light incident surface of the semiconductor layer 12.” *Kuboi*, ¶¶[91], [55]-[56], [71], [181]; VI.A.5.d ([1b.2]). Further, holes 38 extending from region 18 to region 17 are “formed in a region of the semiconductor layer 12 corresponding to one pixel by

dry-etching.” *Kuboi*, ¶[72]. *Kuboi*’s intermediate semiconductor material (region 16) is disposed between region 18 and region 17. VI.A.5.e ([1c.1]). As a result, and because holes 38 extend from region 18 to region 17, *Kuboi*’s one or more in-pillar holes extend into intermediate semiconductor material. Lebbby, ¶236. This is illustrated below.

FIG. 6A



Kuboi, Fig. 6A.

B. Claims 1 and 8-9 are Obvious Over *Yu* (Ground 2) or *Yu* and *Shinohara* (Ground 3)

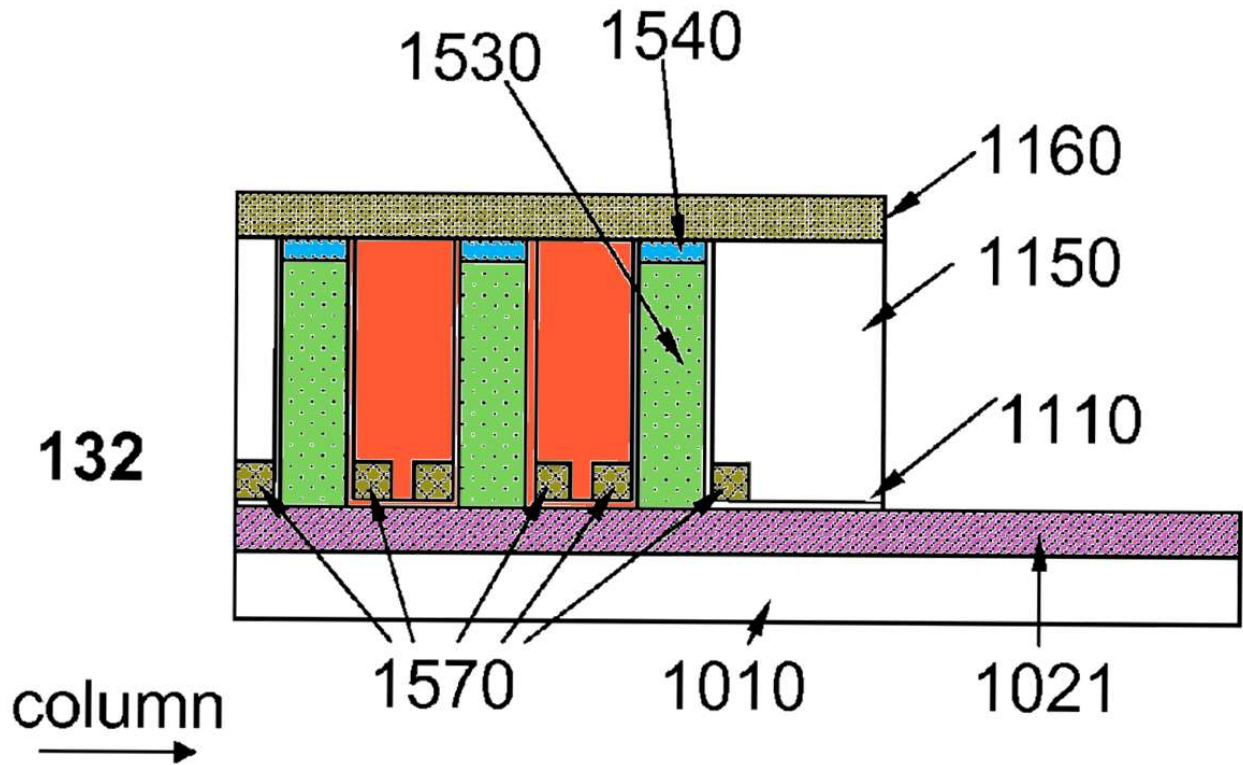
1. Overview of *Yu*

Yu's image sensor includes pixels having at least one nanopillar to convert light to electrical signals. *Yu*, Abstract, ¶[48]; Lebby, ¶¶90-95. *Yu*'s "image sensor and the control circuit can be formed as an integrated circuit or chip." *Yu*, ¶[115].

Yu's image sensor's pixels may include different size nanopillars, including a three-nanopillar pixel and a four-nanopillar pixel. *Yu*, ¶¶[130], [124], Figs. 7A-7B. "[T]he pixels are organized into a plurality of 'rows'" and the "pixels can be organized into a plurality of 'columns.'" *Yu*, ¶[51].

Yu's "nanopillars and the substrate can comprise suitable semiconductor materials and/or metals such as Si." *Yu*, ¶¶[55], [27]. The "substrate has an oxide layer 1010, a heavily doped layer (HDL) 1020 on the layer 1010 and an epi layer 1030 on the HDL layer 1020." *Yu*, ¶[62]. *Yu*'s "substrate can have the following doping profiles: (i) the HDL layer 1020 is p⁺ (i.e. heavily doped to p type), the epi layer 1030 is p⁻ (i.e. lightly doped to p type); [and] (ii) the HDL layer 1020 [is] p⁺, the epi layer 1030 is i (i.e., intrinsic)." *Id.* "[E]pi layer 1030 can be about 3000 to 10000 nm thick." *Id.* "[A] junction layer 1040 is formed on the epi layer 1030," and that "junction layer 1040 is of the opposite conduction type as the HDL layer 1020, i.e., if the HDL 1020 is p type, the junction layer 1040 is n

type.” *Yu*, ¶[63]. *Yu* discloses that “the exposed portion of the junction layer 1040 and the portion of the epi layer 1030 directly therebelow are deep etched until the HDL layer 1020 directly below the exposed portion of the junction layer 1040 is exposed, to form nanopillars 1500.” *Yu*, ¶¶[68], [76]. The deep etching produces holes between adjacent nanopillars. *Id.* *Yu* explains that the “portion of the metal layer 1140 deposited around the lower end of the nanopillars 1500 forms the gate electrodes and gate lines 1570.” *Yu*, ¶[85]. Further, “a transparent conductive layer (TCL) 1160, such as ITO or aluminum doped zinc oxide (AZO) is deposited by a suitable technique such sputtering.” *Yu*, ¶[89]. These features are illustrated below, including holes (orange).



Yu, Fig. 1, step 132. *Yu* also discloses “a silicon-on-insulator (SOI)-type substrate or silicon-on-glass (SG)-type substrate.” *Yu*, ¶[62].

2. Motivation to modify *Yu*'s image sensor in view of *Shinohara*'s teaching of monolithic integration

A POSITA would have been motivated to implement *Shinohara*'s teaching of the monolithic integration of the array of pillars (or pixels) with electronic circuits that include active elements for signal processing and transmission with *Yu*'s image sensor. Leebby, ¶¶297-300. Like the '360 Patent and *Shinohara*, *Yu*'s image sensor includes a plurality of pixels. *Yu*, Abstract, ¶¶[7], [17], [48], [52]. *Yu* is analogous art to the '360 Patent because, like the '360 Patent, *Yu*'s image sensor also includes features to improve light absorption. *Yu*, ¶[133]; Leebby, ¶297.

Shinohara discloses forming a pixel region, a peripheral circuit portion, pixel transistors, and a wiring layer on the same substrate (i.e., monolithic integration). *Shinohara*, ¶¶[68]-[82]; VI.A.4. *Shinohara*'s monolithic integration lowers manufacturing costs, allows high bandwidth operation, improves power efficiency, and enables high-frequency mixed-signal processing. VI.A.4. A POSITA therefore would have been motivated to use *Shinohara*'s monolithic integration teaching to manufacture *Yu*'s image sensor. Lebbby, ¶298. The combination would have involved the use of a known technique—forming the pixel region and all associated electronic circuitry on the same substrate—to improve a similar device—*Yu*'s imaging device—in the same way, namely, by improving manufacturing reliability, reducing manufacturing cost, signal attenuation, and noise, and improving high-bandwidth performance of *Yu*'s device. *Id.*

A POSITA would have had a reasonable expectation of success in implementing *Shinohara*'s teachings for manufacturing *Yu*'s image sensor. Lebbby, ¶299. Given that both references disclose similar imaging devices with pixels, manufacturing *Yu*'s pixels and associated electronic circuitry using *Shinohara*'s techniques would have been well within a POSITA's skill. *Id.* A POSITA would have had a reasonable expectation of success combining *Shinohara* with *Yu* because it requires combining well-known prior elements and manufacturing

methods already taught by both *Yu* and *Shinohara. Id.*; *Inland Steel*, 265 F.3d at 1364.

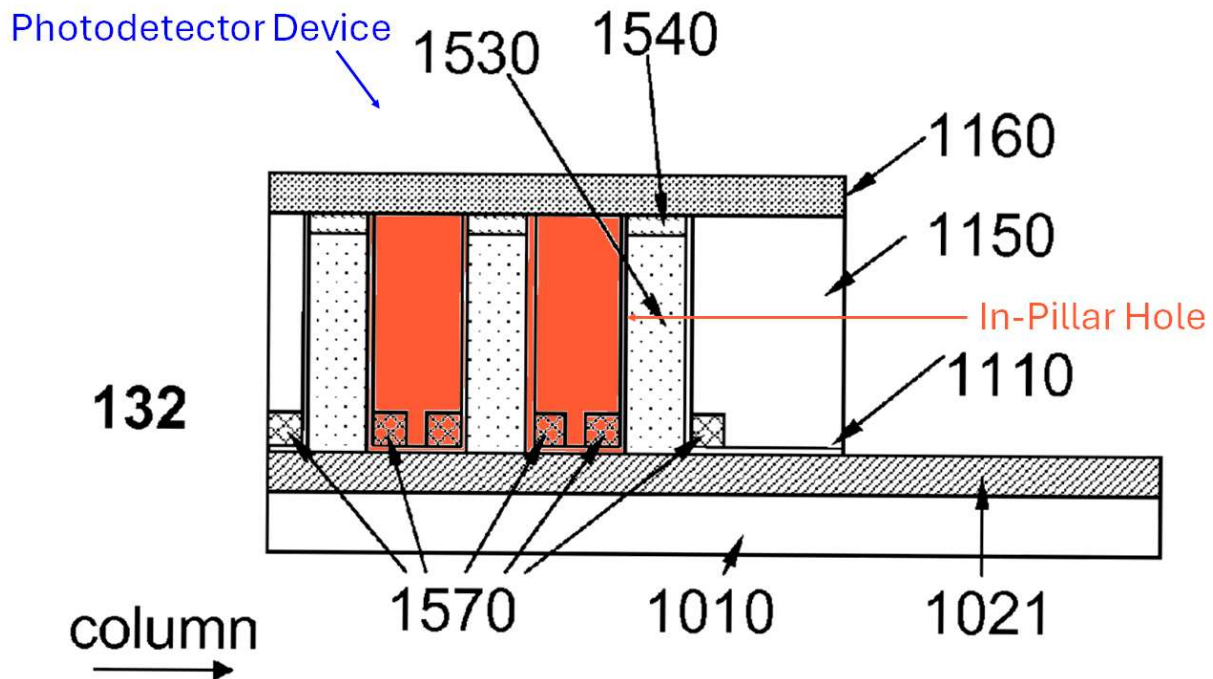
3. Independent Claim 1

a. [1pre]⁴

To the extent the preamble is limiting, *Yu* discloses it. Lebbby, ¶¶237-239. *Yu*’s image sensor is a photodetector device formed in or on a semiconductor substrate that includes nanopillars adapted to convert light impinging thereon to electrical signals. *Yu*, Abstract, ¶¶[7], [17], [48], [52]. *Yu* discloses starting with a silicon-on-insulator (SOI)-type substrate. *Yu*, ¶[62]; Lebbby, ¶238.

Yu’s “image sensor has pixels [that] include[] at least one nanopillar,” which “convert[s] light impinging thereon to electrical signals.” *Yu*, Abstract, ¶[48]. Because *Yu*’s nanopillars convert light to electrical signals, *Yu*’s image sensor is a photodetector device. Lebbby, ¶239. According to *Yu*, “the nanopillars and the substrate can comprise suitable semiconductor materials.” *Yu*, ¶[55]. As explained above (VI.B.3.i, [1d]), *Yu*’s image sensor includes deliberately formed in-pillar holes:

⁴ Petitioners’ mapping of the claims to *Yu*, including the terms “in-pillar holes” (and a plurality thereof) and “array of pillars,” is based on how Patent Owner maps the same claims to Petitioner’s accused products in litigation. Ex-1074.



Yu, Fig. 1, step 132.

b. [1a]

Yu discloses [1a]. Lebbby, ¶¶240-244. Yu’s image sensor’s pixels include at least one nanopillar. Yu, Abstract. “[T]he pixels are organized into a plurality of ‘rows’” and the “pixels can be organized into a plurality of ‘columns.’” Yu, ¶¶[51], [9], [17], [25], [48]. Each of Yu’s pixels is a [pillar](#). Lebbby, ¶241. Because the pixels can be organized into rows and columns, Yu discloses a laterally extending [array of pillars](#). *Id.*

According to Yu, “each pixel has at least one nanopillar, which comprises a p-n or p-i-n junction extending in the length direction of the nanopillar.” Yu, ¶[52].

Yu discloses “an exemplary three-nanopillar pixel and an exemplary four-nanopillar pixel” that “may be incorporated into the image sensor.” *Yu*, ¶¶[130]-[132], Figs. 7A-7B. Each of *Yu*’s pixels is a **pillar**, and each **pillar** has a **rectangular cross-section** in a horizontal plane. Leiby, ¶242. An exemplary pixel (i.e., pillar) with multiple nanopillars is illustrated below:

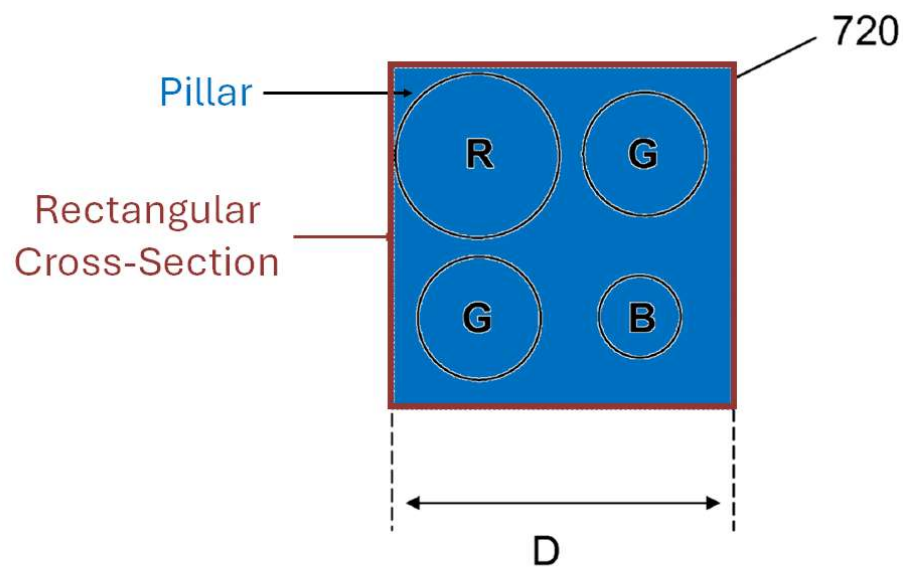


FIG. 7B

Yu, Fig. 7B.

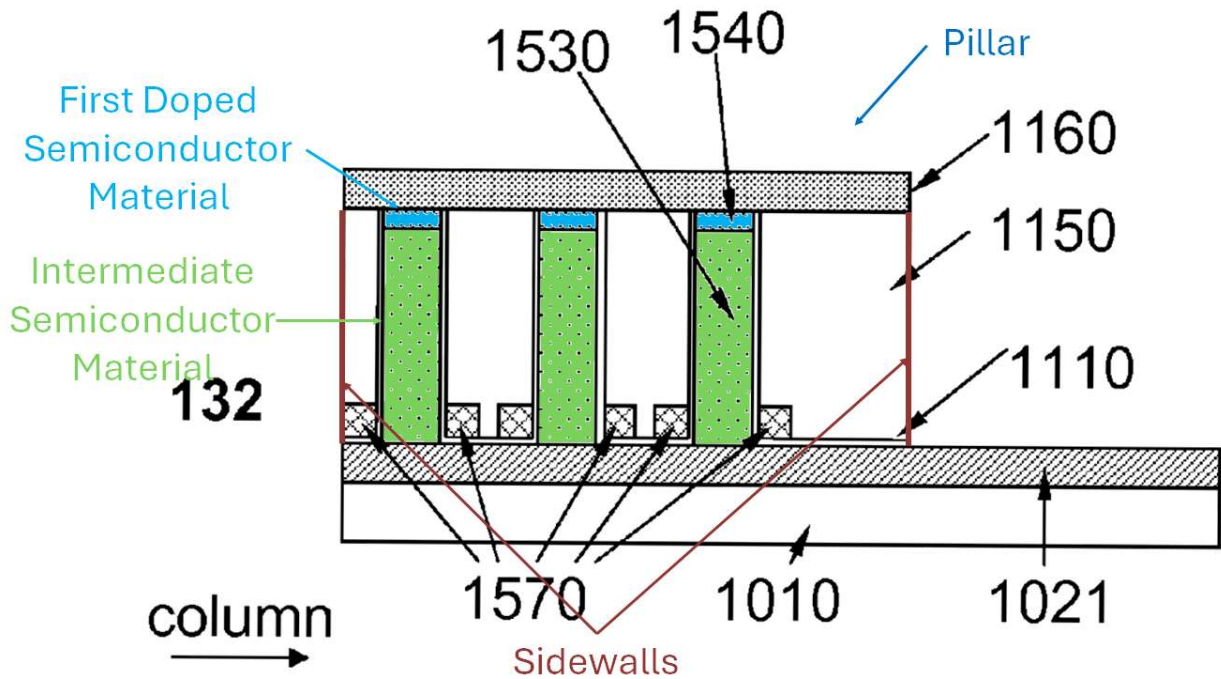
A POSITA would have understood that *Yu*’s “nanopillars” are not the claimed pillars. Leiby, ¶243. Rather, *Yu*’s pixel is the claimed pillar and each such pixel may have more than one nanopillars. *Id.* Thus, *Yu* discloses an array of **pixels** (i.e., **pillars**) arranged in an array of rows and columns and further that each such **pixel** or **pillar** has a **rectangular cross-section**. *Id.* To the extent Patent Owner

argues that *Yu*'s pixels are square, a square is a particular type of rectangle that has sides of equal length. Leebby, ¶244 (citing Ex. 1058, 17, 23).

c. [1b.1]

Yu discloses [1b.1]. Leebby, ¶¶245-247. *Yu* discloses an [array of pixels](#) (or [pillars](#)), each of which has multiple nanopillars. VI.B.3.b ([1a]); Leebby, ¶246.

Yu's "nanopillars and the substrate can comprise suitable semiconductor materials and/or metals such as Si." *Yu*, ¶¶[55], [27]; VI.B.3.a ([1pre]). The "substrate has an oxide layer 1010, a heavily doped layer (HDL) 1020 on the layer 1010 and an [epi layer 1030](#) on the HDL layer 1020." *Yu*, ¶[62]. *Yu*'s "[junction layer 1040](#) is formed on the epi layer 1030" and "is of the opposite conduction type as the HDL layer 1020, i.e.,] if the HDL 1020 is p type, the [junction layer 1040](#) is n type." *Yu*, ¶[63]. *Yu*'s [epi layer 1030](#) is the [intermediate semiconductor material](#) because *Yu*'s [epi layer 1030](#) is located between *Yu*'s [junction layer 1040](#) and *Yu*'s HDL 1020. The figure below illustrates [intrinsic epi layer 1530](#) ("[intermediate semiconductor material](#)"), [junction layer 1540](#), "which is part of the [junction layer 1040](#)" (*Yu*, ¶[68], "[first doped semiconductor material](#)"), and [sidewalls](#):

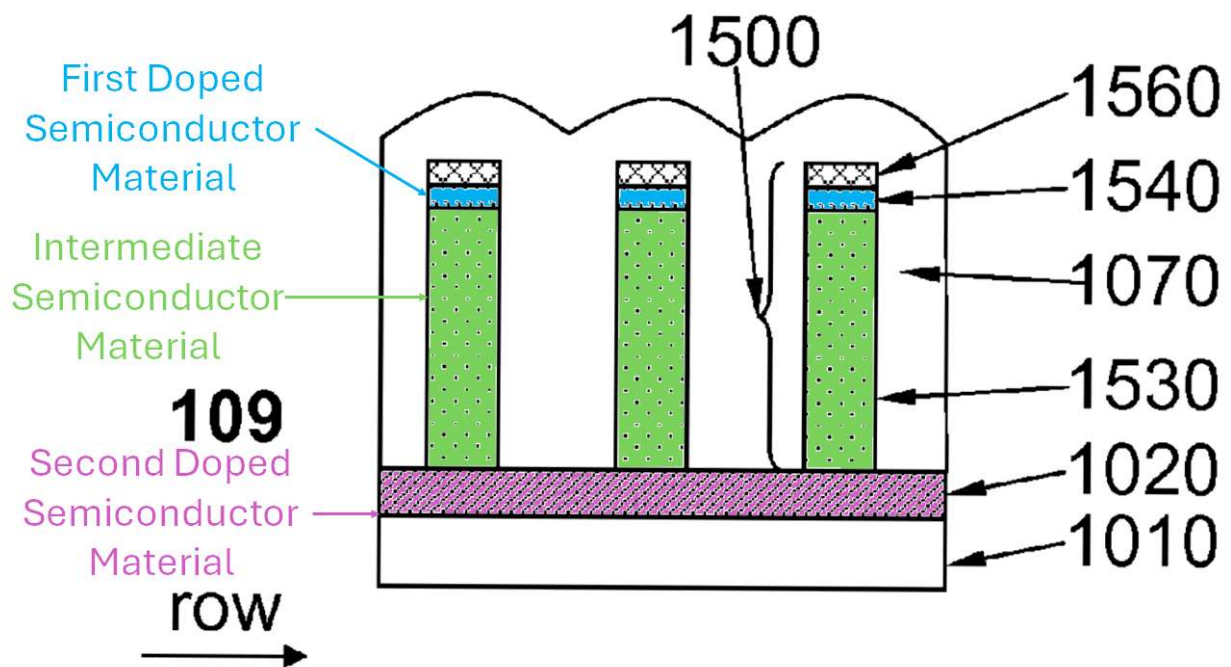


Yu, Fig. 1, step 132. A **cladding** may surround some or all image sensor **pixels**, and the **cladding** may be formed from **silicon nitride**. Yu, ¶[133]. A POSITA would have understood that the **silicon nitride cladding** on the **sidewalls** is a “**solid dielectric**.” Lebby, ¶247 (citing Ex-1063, 20, 33; Ex-1020, 35). Moreover, because the **cladding** is on the **sidewalls** of the **pixels** (or **pillars**), the **cladding** is positioned between **sidewalls** of adjacent **pixels**. Lebby, ¶247.

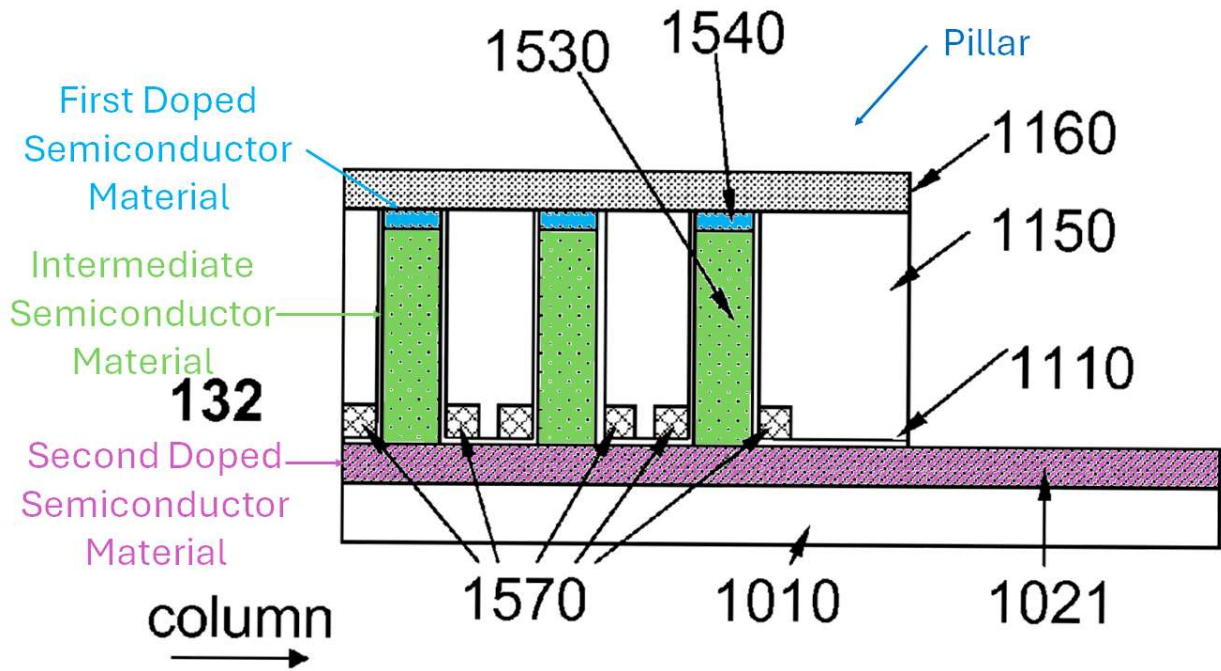
d. [1b.2]

Yu discloses [1b.2]. Lebby, ¶¶248-249. *Yu*’s “substrate has an oxide layer 1010, a heavily doped layer (HDL) 1020 on the layer 1010 and an epi layer 1030 on the HDL layer 1020.” *Yu*, ¶[62]; VI.B.3.c ([1b.1]). “[T]he HDL layer 1020 is p+

(i.e., heavily doped to p type).” Yu, ¶[62]. Yu’s HDL layer 1020 is segmented into readout lines 1021. Yu, ¶[76]. HDL layer 1020, segmented into readout lines 1021 and illustrated below, is the claimed “second doped semiconductor material.”



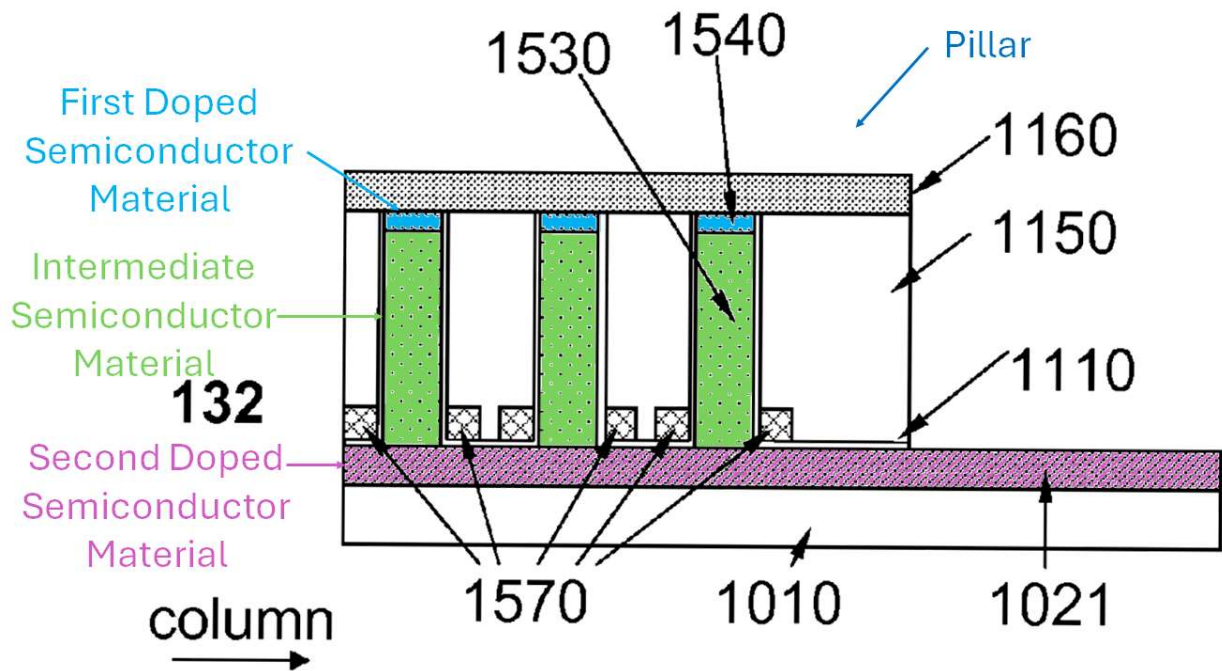
Yu, Fig. 1, step 109.



Yu, Fig. 1, step 132; Lebbby, ¶249.

e. [1c.1]

Yu discloses [1c.1]. Lebbby, ¶¶250-251. *Yu*’s “substrate has an oxide layer 1010, a heavily doped layer (HDL) 1020 on the layer 1010 and an epi layer 1030 on the HDL layer 1020.” *Yu*, ¶[62]. “[J]unction layer 1040 is formed on the epi layer 1030.” *Yu*, ¶[63]. Because the epi layer is formed on the HDL layer and because the junction layer is formed on the epi layer, *Yu*’s **epi layer (intermediate semiconductor material)** is between the **junction layer 1540**, “which is part of the **junction layer 1040**” (*Yu*, ¶[68], **first doped semiconductor material**) and the **HDL (second doped semiconductor material)**. Lebbby, ¶251. This is illustrated below.



Yu, Fig. 1, step 132.

f. [1c.2]

Yu discloses [1c.2]. Lebbby, ¶¶252-253. Yu’s “[junction layer 1040](#) is of the opposite conduction type as the HDL layer 1020, i.e.,] if the HDL 1020 is p type, the [junction layer 1040](#) is n type.” Yu, ¶[63]; see also Yu, ¶[62]. Because the [junction layer](#) ([first doped semiconductor material](#)) is a n type and because the [HDL layer](#) ([second doped semiconductor material](#)) is the oppositely doped p⁺-type semiconductor region, Yu discloses [1c.2]. Lebbby, ¶253.

g. [1c.3]

Yu discloses [1c.3]. Lebbby, ¶¶254-257. Yu’s “substrate can have the following doping profiles: (i) the [HDL layer](#) 1020 is p⁺ (i.e.,] heavily doped to p

type)”; and (ii) “the **epi layer** 1030 is p– (i.e. lightly doped to p type).” *Yu*, ¶[62].

Yu’s intermediate semiconductor material (**epi layer**) is doped less (lightly doped p type) than the second doped semiconductor material (**HDL layer**, highly doped p type). Lebbby, ¶255.

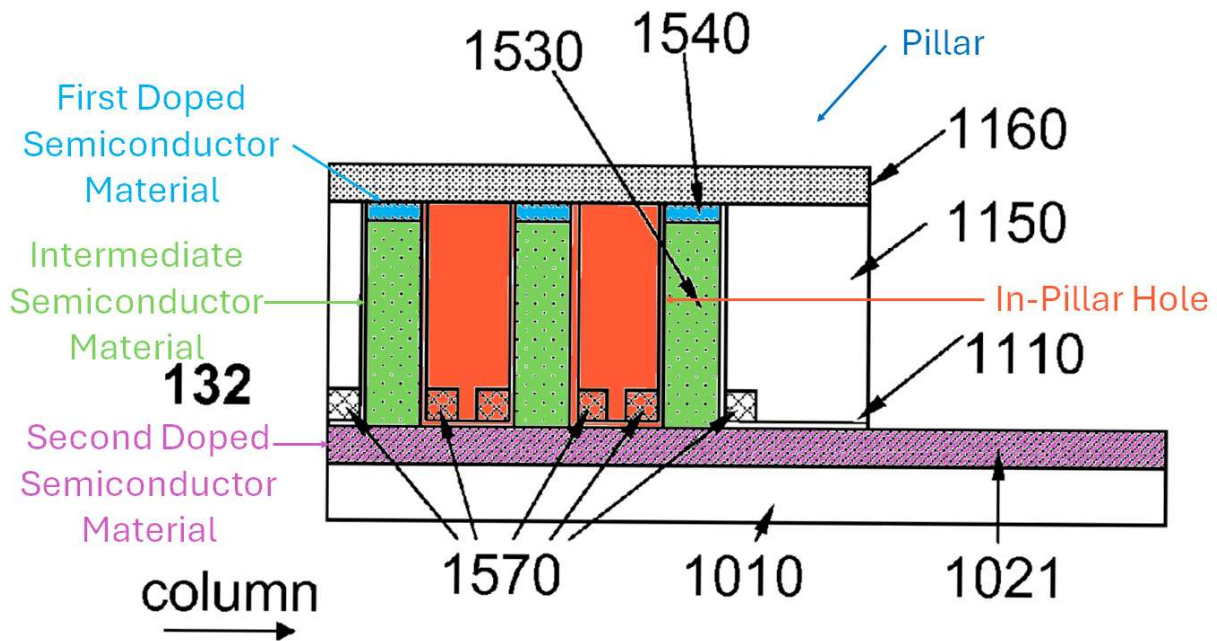
The degree of doping in the **epi layer** (“intermediate semiconductor material”) could only be either the same or different at different positions, as no other possibilities exist. Lebbby, ¶256. As discussed above, the dopant concentration varies with depth. VI.A.5.g; Lebbby, ¶257 (citing Ex-1063, 37-38; Ex-1020, 4; Ex-1028, 1). *Yu* thus discloses that “the degree of doping is the same or different for different positions in the intermediate semiconductor material.” Lebbby, ¶257.

h. [1c.4]

Yu discloses [1c.4]. Lebbby, ¶¶258-259. *Yu*’s “nanopillars and the substrate can comprise suitable semiconductor materials and/or metals such as Si.” *Yu*, ¶[55]; VI.B.3.a ([1pre]). *Yu* also discloses that “**junction layer** 1040, the **epi layer** 1030[,] and the **HDL layer** 1020 form a p-i-n, p-n, n-i-p, or n-p junction, depending on the doping profile.” *Yu*, ¶[63]. Since *Yu*’s first and second doped semiconductor materials and the intermediate semiconductor material are created in silicon nanopillars by doping, each region comprises silicon (Si). Lebbby, ¶259.

i. [1d]

Yu discloses [1d]. Lebbby, ¶¶260-262. *Yu* discloses starting with a silicon-on-insulator (SOI)-type substrate. *Yu*, ¶[62]. *Yu* discloses forming an oxide layer, a heavily doped layer (HDL) on the oxide layer, and forming an epi layer on the HDL layer. *Id.* *Yu* also discloses forming a junction layer on the epi layer. *Yu*, ¶[63]. “[T]he exposed portion of the junction layer 1040 and the portion of the epi layer 1030 directly therebelow are deep etched until the HDL layer 1020 directly below the exposed portion of the junction layer 1040 is exposed, to form nanopillars 1500.” *Yu*, ¶¶[68], [76]. The spaces between nanopillars are the **in-pillar holes**. Lebbby, ¶261. These **in-pillar holes**, shown below, are deliberately formed because they are formed by a purposeful deep-etch process. *Id.*



Yu, Fig. 1, step 132. There are a plurality of (i.e., two) **in-pillar holes** in each pixel.

Lebby, ¶261.

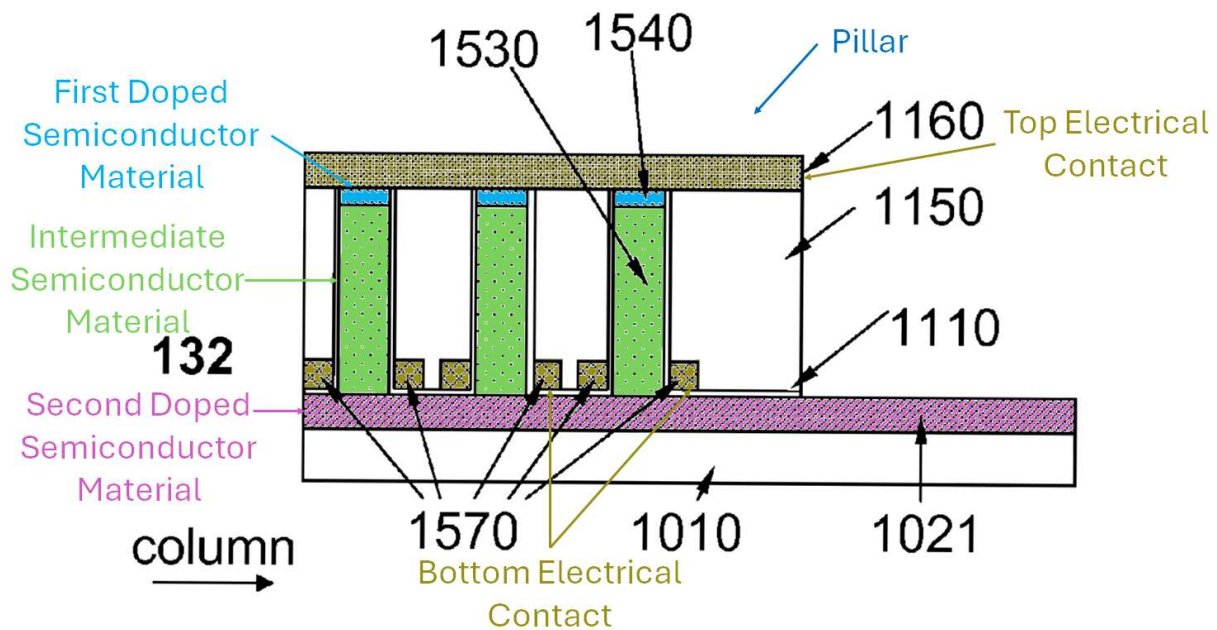
According to *Yu*, “space between the nanopillars 1500 is filled by **an oxide** or a polymer 1150 such as **silicon oxide** or polyimide.” *Yu*, ¶[87]. **Silicon oxide** is a **solid dielectric**. Lebby, ¶262 (citing Ex-1020, 34-35; Ex-1063, 20-21, 23). Thus, *Yu*’s **in-pillar holes** are filled with **solid dielectric**. Lebby, ¶262.

j. [1e]

Yu discloses [1e]. Lebby, ¶¶263-267. During formation of *Yu*’s image sensor, “**metal layer 1140** is deposited.” *Yu*, ¶[85]. The “portion of the **metal layer 1140** deposited around the lower end of the nanopillars 1500 forms the gate electrodes and gate lines 1570.” *Id.* This **metal layer 1140** forms the **bottom electrical contacts**. Lebby, ¶264. *Yu* also discloses “a first **gate line** electrically

connected to the gate electrodes of the first and third pixels and a second **gate line** electrically connected to the gate electrodes of the second and fourth pixels.” *Yu*, ¶¶[9], [25], [51]. Thus, *Yu*’s **bottom electrical contacts** (**gate lines**) are electrically connected to a plurality of **pixels** (or **pillars**) and therefore connected to *Yu*’s **array of pillars**.

Yu further discloses that “a **transparent conductive layer (TCL) 1160**, such as ITO or aluminum doped zinc oxide (AZO)[,] is deposited.” *Yu*, ¶¶[89], [27], [53]. The **TCL layer** is the image sensor’s **top electrical contact**. Lebbby, ¶265. *Yu*’s **electric contacts** are illustrated below. Because **layer 1160** is deposited on *Yu*’s image sensor including a plurality of **pixels** (or **pillars**), *Yu*’s **top electrical contact (TCL)** is electrically connected to *Yu*’s **array of pillars**.



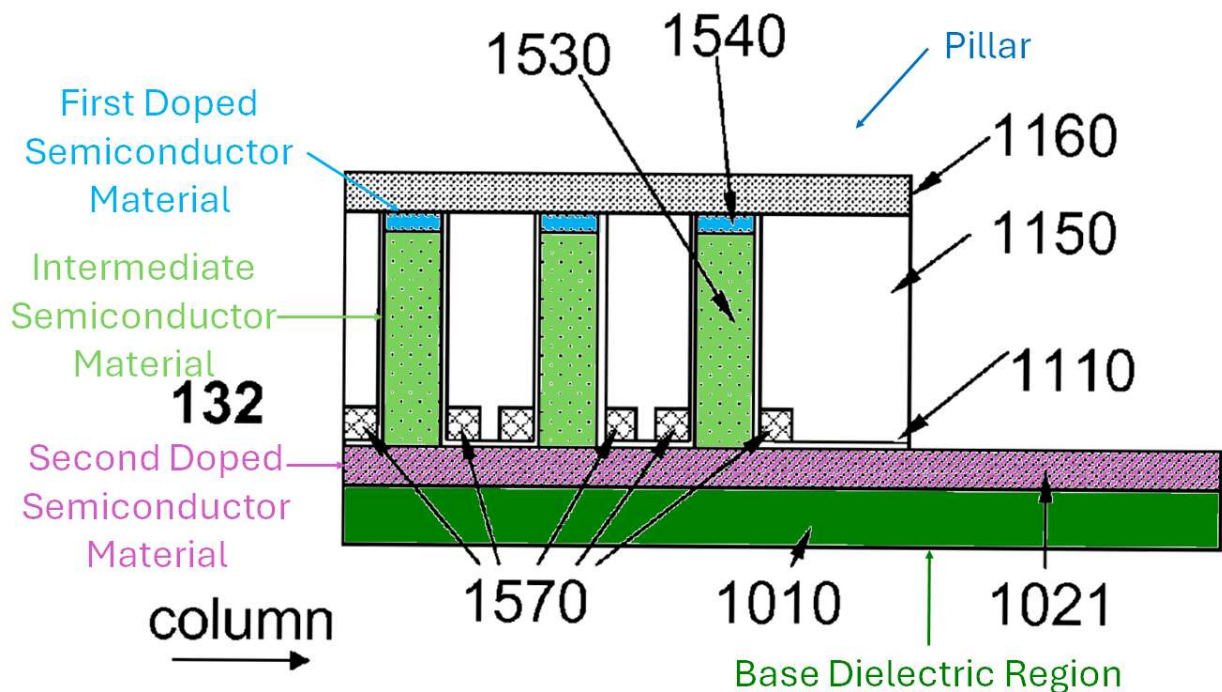
Yu, Fig. 1, step 132.

Yu’s image sensor pixels each “[have] at least a nanopillar that can convert light impinging thereon to electrical signals.” Yu, ¶¶[48], [17]. Thus, Yu’s **image sensor** (**photodetector device**) is configured to convert **light photons** (**impinging light**) incident on said **array of pillars** into **electrical signals** (**photo-generated charge carriers**). Lebbby, ¶267.

k. [1f]

Yu discloses [1f]. Lebbby, ¶¶268-270. Yu also discloses “a silicon-on-insulator (SOI)-type substrate or silicon-on-glass (SG)-type substrate is provided.” Yu, ¶¶[62], [15], [102]. The “substrate has an **oxide layer 1010**.” Yu, ¶¶[62], [102]. The substrate’s **oxide layer 1010** is the **base dielectric layer** because as shown in

the figure below, it is disposed below *Yu*'s pillars. Leiby, ¶269. And oxide layer 1010 is a solid dielectric material. Leiby, ¶270 (citing Ex-1020, 34; Ex-1063, 20-21); VI.A.5.k. *Yu*'s base dielectric layer is illustrated below.



Yu, Fig. 1, step 132.

I. [1g]

Yu renders obvious [1g]. Leiby, ¶¶271-279. *Yu* “is related to U.S. patent application Ser. No[. 12/204,686 (granted as U.S. Pat. No. 7,646,943)” (“’943 Patent,” Ex-1055), and the ’943 Patent and other applications are “incorporated by reference in their entirety.” *Yu*, ¶[1]. The ’943 Patent discloses that “each pixel containing an image sensor of the embodiments disclosed herein could be as small as 1 micron or less in pitch.” ’943 Patent, 10:50-54.

Yu's pixels constitute the claimed pillars forming the array of pillars.

VI.B.3.a ([1pre]), VI.B.3.b ([1a]). Further, because the '943 Patent is incorporated by reference, *Yu* also discloses a pixel pitch—which is the same as the pitch between *Yu*'s pillars—of 1 μm or less. *Advanced Display Sys., Inc. v. Kent State Univ.*, 212 F.3d 1272, 1282 (Fed. Cir. 2000) (incorporated material “is effectively part of the host document as if it were explicitly contained therein”). *Yu*'s 1 μm pixel pitch is equivalent to 1,000 nm, meaning that *Yu*'s pillars are “laterally spaced center to center by no more than 10,000 nanometers.” Lebbby, ¶277. Moreover, a POSITA would have found it obvious to implement the '943 patent's dimensions in *Yu*'s photodetector device as such pitch dimensions were well known in the art, and they would have had a reasonable expectation of success in doing so. Lebbby, ¶¶274-276; e.g., *Kuboi* (1.65 μm pixel pitch); Ex-1012, 2 (pixel size and therefore pitch of 2 μm).

Yu's epi layer is the claimed intermediate semiconductor material. VI.B.3.e ([1c.1]). “[E]pi layer 1030 can be about 3000 to 10000 nm thick.” *Yu*, ¶[62]. The '360 Patent fails to disclose that the claimed range is critical to the claimed photodetector device's operation. Therefore, *Yu* renders the claimed range obvious because *Yu*'s disclosed thickness range for its intermediate semiconductor material

overlaps with the claimed range of 100-5,000 nm. Lebbby, ¶¶278-279; *Peterson*, 315 F.3d at 1329; VI.A.5.1.

m. [1h]

Yu discloses, or at a minimum suggests [1h] based on Patent Owner's statements in the '360 Patent and a POSITA's knowledge of the state of the art before the '360 Patent's priority date. Lebbby, ¶¶280-291.

Yu discloses an embodiment in which the spacing between its nanopillars is approximately of 50 nm. *Yu*, ¶[65] (disclosing minimum feature size of 50 nm when etching the in-pillar holes). *Yu*'s nanopillars preferably have dimensions of 90-150 nm. *Yu*, ¶[57]. Thus, the period Λ or center-to-center distance between the in-pillar holes ranges between about 140-200 nm. Lebbby, ¶282. Silicon's refractive index n_1 varies from about 3.5 for light of wavelength 1000 nm to 5.8 for light of wavelength 300 nm (Lebbby, ¶283 (citing Ex-1056, 9:43-46, Fig. 4; Ex-1061, 49)). The refractive index n_2 of the silicon dioxide in *Yu*'s holes is about 1.5 over the wavelength range of 400-1000 nm. Lebbby, ¶283. (citing Ex-1062, 6, Fig. 1; Ex-1056, 9:43-46, Fig. 4).

Using the above values for wavelengths and refractive indices, Table C below shows the calculated values of λ/n_1 to λ/n_2 for n_2 of 1.5. *Yu*'s hole pitch of

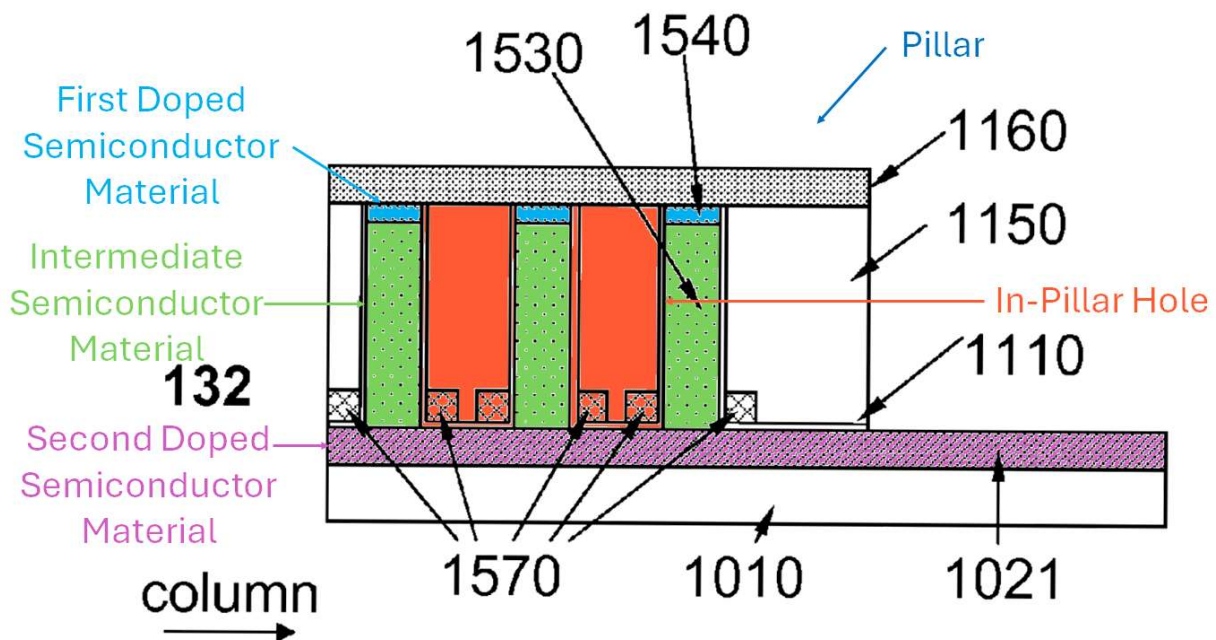
140-200 nm falls within the range λ/n_1 to λ/n_2 for at least a portion of the visible light spectrum. Lebbby, ¶¶284-285.

Table C				
λ (nm)	n_1 (Silicon)	n_2 (Dielectric)	λ/n_1 (nm)	λ/n_2 (nm)
400	5.8	1.5	68	267
550	4.5	1.5	123	367
650	3.9	1.5	168	433
700	3.8	1.5	184	467

Thus, the stated period of *Yu*'s in-pillar hole array falls within the range λ/n_1 to λ/n_2 for “selected visible and infrared wavelength ranges.” Lebbby, ¶286.

Further, based on Patent Owner's representations, *Yu*'s pillar hole array forms an HCG. *Id.*; VI.A.5.m (introducing Patent Owner's representations). And, under those same representations, such an HCG would produce an enhanced absorption coefficient of 1.1 to 100 times the bulk absorption coefficient based on the near-wavelength and deep-wavelength phenomena. Lebbby, ¶286. Thus, consistent with Patent Owner's representations, a POSITA would have understood that *Yu*'s in-pillar holes increase photon absorption in *Yu*'s device by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said one or more in-pillar holes. *Id.*

Patent Owner's representations, discussed above, were consistent with those of other prior art teachings that disclosed improvement in light absorption based on the depth of the **in-pillar holes**. Lebbby, ¶¶287-291. For example, Yu's pixel with **in-pillar holes** is illustrated below.



Yu, Fig. 1, step 132. Yu's "epi layer 1030 can be about 3000 to 10000 nm thick."

Yu, ¶[62]. "[T]he thickness of the junction layer 1040 is from 10 to 200 nm." Yu,

¶[63]. Thus, each **in-pillar hole** has a depth ranging between 3,010-10,200 nm.

Lebbby, ¶288.

According to Han, the ultimate efficiency for a device having a semiconductor thickness of about 3,010 nm (3.01 μm) without nanoholes is approximately 0.15, whereas the ultimate efficiency for a similar device having

nanoholes is approximately 0.27. *Han*, Fig. 4; Lebby, ¶289. Thus, before the earliest priority date of the '360 Patent, a POSITA would have understood that *Yu*'s nanohole depths of 3,010 nm (3.01 μ m) increase light absorption by a factor of 1.8 ($0.27/0.15 = 1.8$), which is significantly higher than a factor of 1.1. *Han*, Fig. 4; Lebby, ¶289.

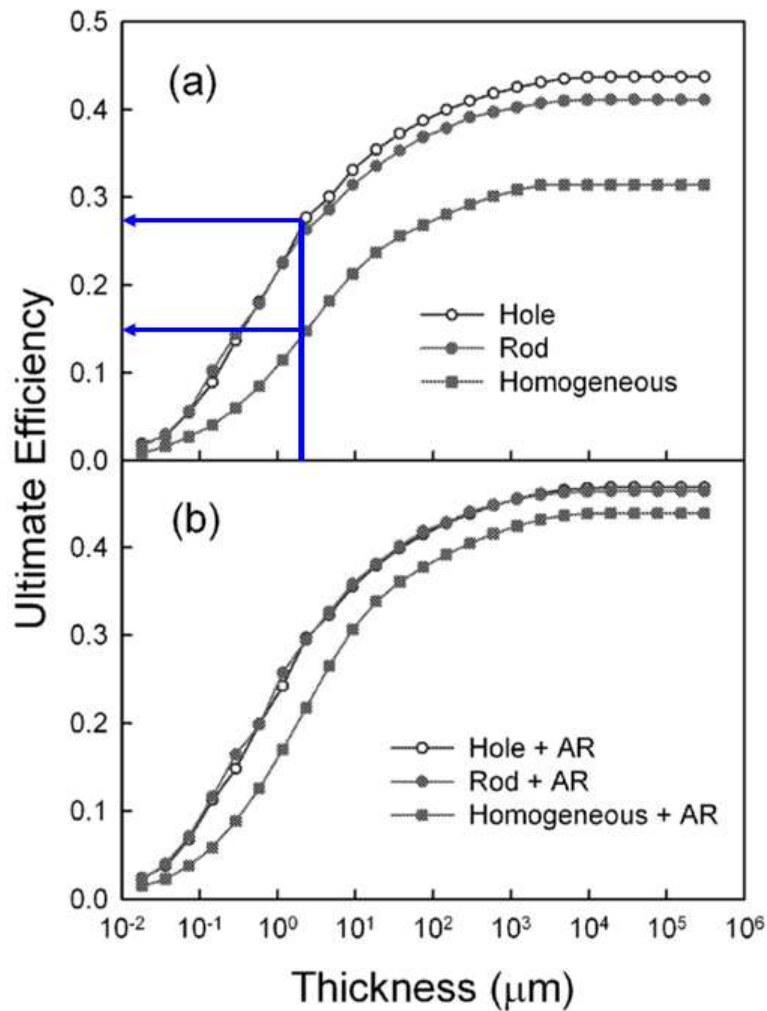


FIG. 4

Han, Fig. 4. As another example, *Han* discloses that the ultimate efficiency for a device having a semiconductor thickness of about 10,200 nm (10.2 μm) without nanoholes is approximately 0.22, whereas the ultimate efficiency for a similar device having nanoholes is approximately 0.33. *Han*, Fig. 4; Lebby, ¶290. Thus, before the '360 Patent priority date, a POSITA would have understood that *Yu*'s nanohole depths of 10,200 nm (10.21 μm) increase light absorption by a factor of

1.5 ($0.33/0.22 = 1.5$), which is significantly higher than a factor of 1.1. *Han*, Fig. 4; Lebbby, ¶290.

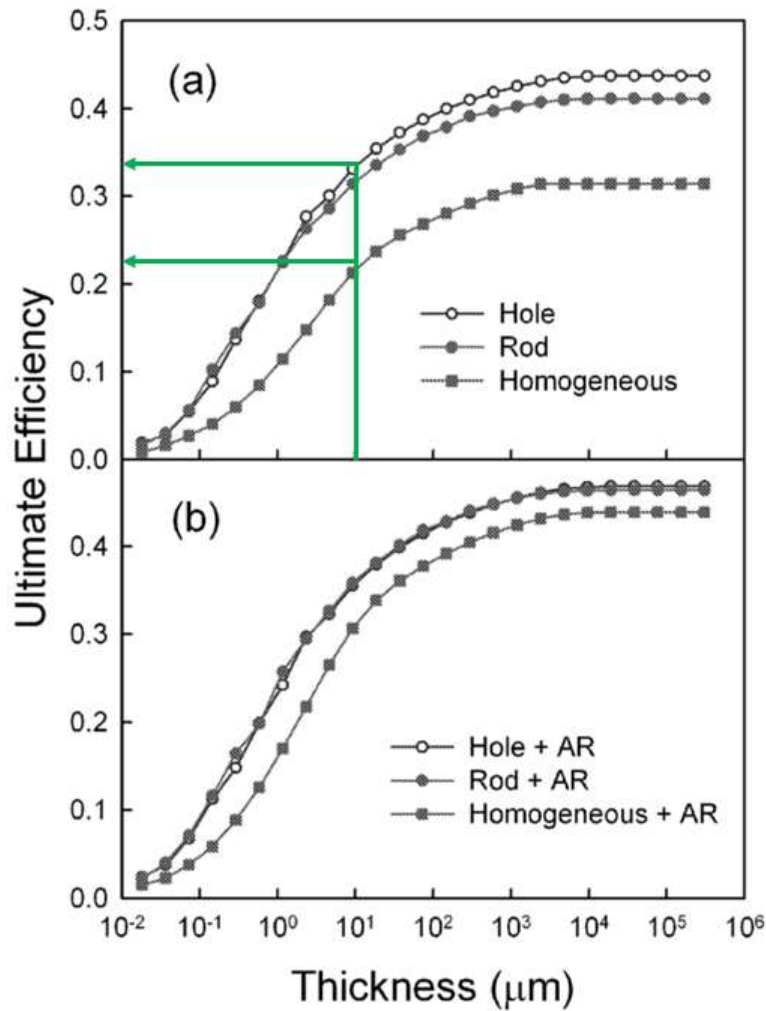


FIG. 4

Han, Fig. 4.

Accordingly, based on a POSITA's understanding of the state of the art before the '360 Patent's priority date, a POSITA would have understood that *Yu*'s in-pillar holes of depth 3,010-10,200 nm would increase photon absorption in *Yu*'s

image sensor by at least 1.1 times at selected visible and infrared wavelength ranges of said incident light compared to a like device lacking said one or more in-pillar holes, and even if not readily understood, a POSITA would have found such a result not only obvious but also one having a reasonable expectation of success in achieving this increase. Lebbby, ¶291.

n. [1i]

Yu discloses [1i]. Lebbby, ¶¶292-300. *Yu*'s apparatus comprises the image sensor and a control circuit that includes a decoder, a transimpedance amplifier, a multiplexer circuit, and other readout circuitry components. *Yu*, ¶[115]. The “image sensor and the control circuit can be formed as an integrated circuit or chip.” *Id.* Forming the image sensor and control circuit as an “integrated circuit” means that *Yu*'s pixels (part of the image sensor) are monolithically integrated with the control circuit on the same chip or substrate. Lebbby, ¶294 (citing Ex-1067, 6).

To the extent Patent Owner argues that *Yu* does not disclose monolithic integration, the *Yu-Shinohara* combination renders obvious [1i]. *Shinohara* discloses forming a pixel region, a peripheral circuit portion, pixel transistors, and a wiring layer on the same substrate. *Shinohara*, ¶¶[68]-[82]; VI.A.4; Lebbby, ¶¶295-296. The *Yu-Shinohara* combination renders obvious this limitation for reasons discussed above (VI.B.2) and for reasons similar to those discussed for the *Kuboi-Shinohara* combination (VI.A.4). Lebbby, ¶296.

4. **Claim 8: “The photodetector device of claim 1, in which each of said pillars has at least two of said one or more in-pillar holes that partly overlap.”**

Yu discloses this additional limitation. Lebbby, ¶¶301-307. “[T]he exposed portion of the junction layer 1040 and the portion of the epi layer 1030 directly therebelow are deep etched until the HDL layer 1020 directly below the exposed portion of the junction layer 1040 is exposed, to form nanopillars 1500.” *Yu*, ¶[68]. *Yu*’s “nanopillars can have any suitable cross-sectional shape such as a circle, a square, [or] a hexagon.” *Yu*, ¶[57]. Figure 2B illustrates a plan view where each nanopillar has a generally square or rectangular cross-sectional shape. *Yu*, ¶[57]; Lebbby, ¶302. The square or rectangular nanopillars are illustrated below.

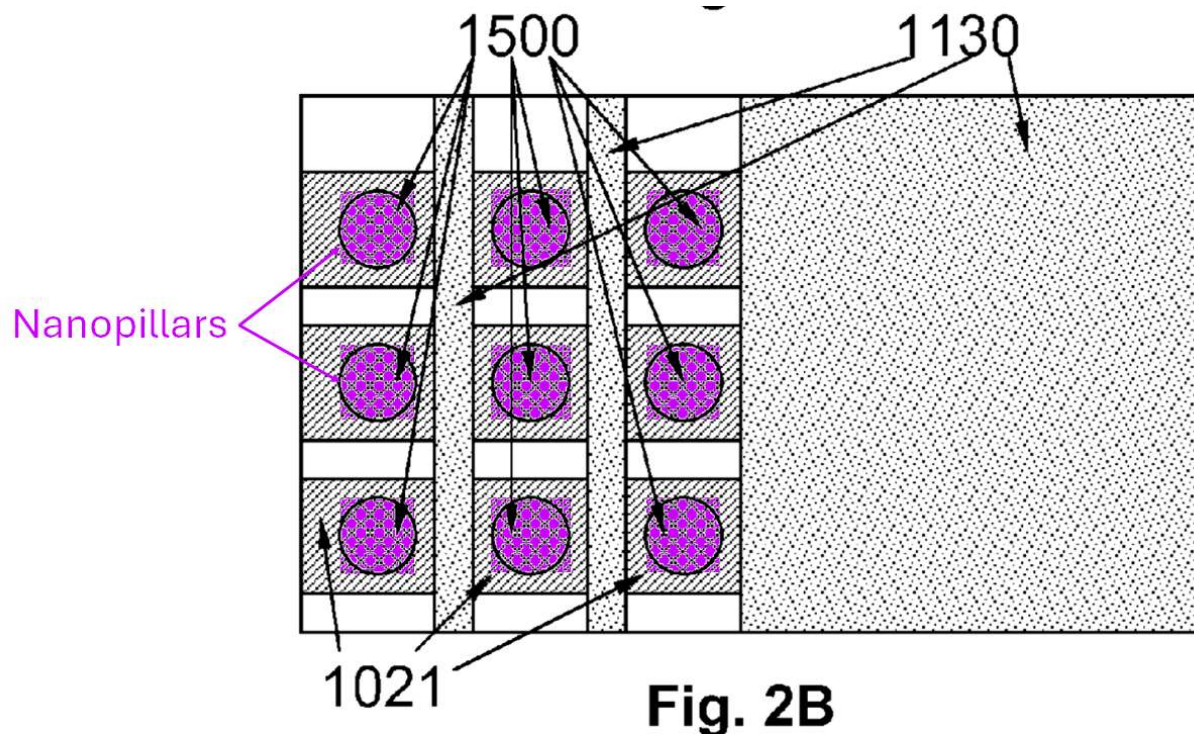
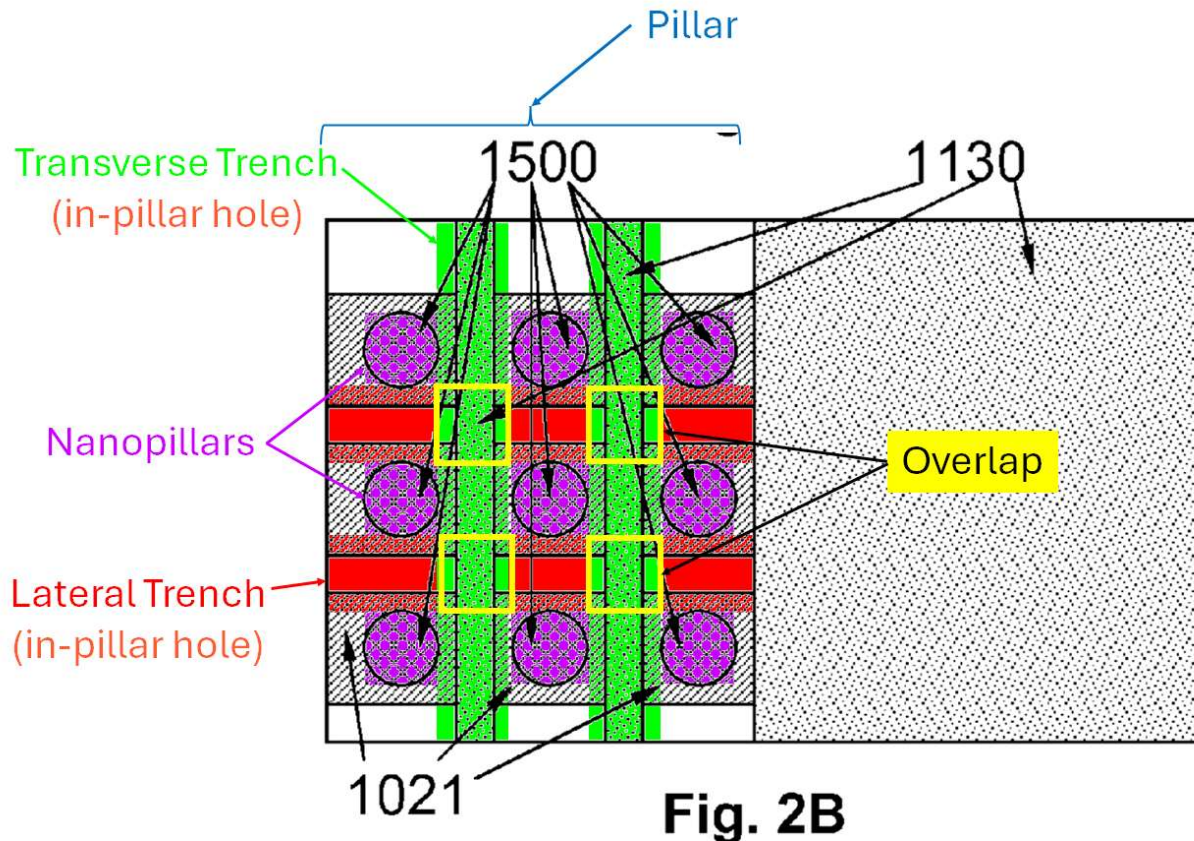


Fig. 2B

Yu, Fig. 2B. Yu's square- or rectangular -shaped nanopillars would have been formed by deep etching a substrate (Yu, ¶¶[68], [76]) to form trenches oriented generally perpendicular to each other. Lebbby, ¶¶303-306. These trenches (or in-pillar holes), including a plurality of trenches in a lateral direction and a plurality of trenches in a transverse direction, are shown below:



Yu, Fig. 2B. The yellow rectangles show that the trenches (or in-pillar holes) partly overlap with the trenches (or in-pillar holes) in a transverse direction. Leiby, ¶307.

5. **Claim 9:** “The photodetector device of claim 1, in which said second doped semiconductor material comprises a laterally continuous region coupled to a plurality of said pillars.”

Yu discloses this additional limitation. Leiby, ¶¶308-310. The HDL disposed on Yu’s substrate’s oxide layer constitutes the claimed second doped semiconductor material. VI.B.3.d ([1b.2]). “HDL layer 1020 is ... segmented into readout lines.” Yu, ¶[76]. And Yu’s “image sensor can comprise first, second, third[,] and fourth pixels, a first readout line electrically connected to the first and

second **pixels**, [and] a **second readout line** electrically connected to the third and fourth **pixels**.” *Yu*, ¶¶[9], [25], [51].

Each **pixel** in *Yu*’s image sensor corresponds to a claimed **pillar**. VI.B.3.b ([1a]). The **first readout line** must be continuous to connect two **pixels**. *Lebby*, ¶310. Similarly, the **second readout line** must be continuous to connect two **pixels**. *Id.* Moreover, because the **readout lines** are formed by segmenting the **HDL**, each **readout line** must extend laterally to connect two **pixels**. *Id.* Because the **first and second readout lines** are each connected to at least two **pixels**, *Yu*’s **first or second readout line** (**second doped semiconductor material**) is laterally continuous and is connected to more than one **pillar** (i.e., to more than one **pixel**). *Id.*

VII. Mandatory Notices

A. Real Parties-in-Interest

The real parties-in-interest are Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor LLC.

B. Related Matters

Patent Owner W&Wsens Devices Inc. asserted the ’360 Patent in *W&Wsens Devices Inc. v. Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor LLC*, Case No.

2:24-cv-00854-JRG (E.D. Tex.). Patent Owner also asserted U.S. Patent No. 12,087,871 (“’871 Patent”) in that case, which is related to the ’360 Patent.

C. Lead and Backup Counsel, and Service Information

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Please address all correspondence to counsel at the address above. Petitioner consents to electronic service by email at the above email addresses.

VIII. Grounds for Standing

Petitioner certifies that the '360 Patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified herein.

IX. Conclusion

For the reasons above, Petitioner requests institution of IPR and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Date: June 20, 2025

Respectfully submitted,

By: /Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, Petitioner certifies that the word count of Petitioner's Petition for *Inter Partes* Review (exclusive of any table of contents, table of authorities, mandatory notices under §42.8, certificates of service and word count, and list of exhibits or claim listing) as measured by Microsoft Word is 13,854.

Dated: June 20, 2025

By: /Joshua L. Goldberg/
Joshua L. Goldberg, Lead Counsel
Reg. No. 59,369

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§42.6(e) and 42.105(a), the undersigned certifies that on June 20, 2025, a copy of the foregoing **Petition for *Inter Partes* Review, the associated powers of attorney, and Exhibits 1001-1007, 1010-1015, 1020-1022, 1028-1030, 1034-1038, 1050-1053, 1055-1063, and 1067-1074** were served by FedEx Priority Overnight on the correspondence address of record indicated in the Patent Office's public Patent Center system for U.S. Patent No. 11,621,360:

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