

(incorporated herein by reference). According to some embodiments, chemical mechanical polishing (CMP) can be performed after the selective area growth to present a smooth flat surface for processing of the CMOS/BiCMOS and photodiode integration.

5 **[00409]** FIG. 63C shows an MSPD formed on the structure having selective area growth of Ge and/or GeSi on silicon. The Ge and/or GeSi 6310 top surface can be ion implanted and/or diffused with dopants of P type (can also be N type) to form a P (Ge and/or GeSi)- I(Ge and/or GeSi)-N(Si) structure 6384 and can include microstructured holes 6312 etched into the I Ge/GeSi 6310 partially and/or entirely
 10 using wet and/or dry etching. The Ge and/or GeSi layer 6310 thickness can range from 500 nm to 5000 nm and in some cases 500 nm to 2500 nm for data rate bandwidths of 10 to 50 Gb/s or more. Lateral dimension of the photosensitive area for high speed operation where a high electric field is externally applied via a reverse bias between the anode and cathode, can range from 10 micrometers to
 15 500 micrometers and in some cases from 25 micrometers to 80 micrometers and in some cases from 25 to 100 micrometers

[00410] For MSPD, MSAPD, MSOWPD, MSOWAPD, the hole dimension laterally can range from 100 nm to 5000 nm and in some cases from 350 nm to 2500 nm and spacing with adjacent holes can range from 50 nm to 5000 nm and in
 20 cases can range from 100 nm to 2000 nm and can be periodic and/or aperiodic and/or combination of periodic and aperiodic. The hole cross sections can be any combination of cross sectional shapes including funnel, inverted pyramid, cylindrical, trapezoidal, hourglass, ball shaped, rectangular, and polygonal. The surface shape of the holes can be circular, oval, hourglass, rectangular, polygon,
 25 amoeba, or combinations thereof. The holes can be periodic and/or aperiodic. Etch depth of the holes can range from 100 nm to 10000 nm and in some cases can partially etch into the top doped layer, and/or partially into the I layer or lightly doped layer and/or fully through the I or lightly doped layer and/or partially into the lower doped layer and/or through the lower doped layer. In some cases the
 30 microstructured holes can extend into the silicon regions vertically and/or laterally.

[00411] Operating wavelength can range from 800 nm to 2000 nm depending on the Ge fraction in the GeSi alloy. In some cases from 1250 nm to 1350 nm, and in some cases from 1550 nm to 1650 nm. In some cases from 840 nm to 960 nm and

in some cases from 900 nm to 1070 nm and in some cases from 840 nm to 1100 nm and in some cases from 900 nm to 1350 nm. Responsivity can range from 0.1A/W to 1A/W at at least one of the wavelength in the wavelength span. In some cases responsivity can be 0.1A/W or greater at at least one wavelength in the wavelength span, in some cases 0.3A/W or greater at at least one wavelength in the wavelength span, in some cases 0.5A/W or greater at at least one wavelength in the wavelength span, in some cases 0.8A/W or greater at at least one wavelength in the wavelength span, and in some cases 1A/W or greater at at least one wavelength in the wavelength span.

10 **[00412]** Data rates can range from 10-50 Gb/s or higher, in some cases 25 Gb/s or higher, in some cases 40 Gb/s or higher, and in some cases 50 Gb/s or higher.

[00413] Analog Devices, Inc. data sheet ADN3010-11 11.3 Gbps Optical Receiver (incorporated herein by reference), shows the integration of a SiGe PIN photodiode with TIA and LA with data rate bandwidth to 11.3 Gb/s. The bandwidth
15 can be limited by the thickness of the SiGe layer which was chosen to achieve a responsivity of 1A/W. This requires a thickness ranging from 3-4 micrometers with a saturation velocity of approximately 0.7×10^7 cm/s for electrons in Ge. The data rate is thus limited to approximately 9 GHz or less or approximately 10-13 Gb/s. According to some embodiments, to achieve higher data rates a thinner GeSi layer
20 can be provided, and to achieve high responsivity, microstructured holes can be provided to enhance the absorption and therefore the quantum efficiency and responsivity of a thinner GeSi layer. For example, a 2 micrometer or less thick Ge layer can achieve in excess of 22 Gb/s data rate bandwidth and microstructured holes can enhance the absorption of thinner Ge and/or GeSi layers to improve the
25 responsivity and therefore the system sensitivity.

[00414] In FIG. 63C, shallow P⁺ well 6384 can be implanted and/or diffused into the surface of the Ge/GeSi 6310 to a depth ranging from 50 nm to 300 nm and with resistivity less than 0.01 ohm-cm and in some cases a thin metal and/or transparent conducting metal oxide layer (not shown) can be deposited on the
30 Ge/GeSi prior to microstructure hole etch with thicknesses ranging from 1 nm to 300 nm. Buried N⁺ region 6304 can be formed using selective area ion implantation and/or diffusion, and/or epitaxially grown with resistivity of 0.01 ohm-cm or less and in some cases 0.001 ohm-cm or less and with thicknesses ranging from 100 nm to

500 nm or more, on N or P substrate. A buried O and/or N ion implant at selective areas 6334 can be implemented on the N or P substrate prior to N^{++} (or P^{++}) or undoped or intrinsic epitaxial growth of 0.5 to 5 microns with resistivity of 1 ohm-cm or greater and in some cases 10 ohm-cm or greater. In some cases a SOI substrate can be use.

[00415] N^+ connecting wells 6306 can be formed to connect the cathode to the buried N^+ layer 6304. The connecting wells 6306 can be post-like with the post around the perimeter of the photosensitive region defined by the P^+ doped layer 6384 and/or a continuous wall around the perimeter. The posts and/or walls can be approximately 2 times the depletion width, for example if the depletion width between the P^+ -I- N^+ is 2 microns, then the post and/or wall can be 4 microns or more distance from the P^+ region. Cathode metallization is formed on the N^+ well 6306 and can be ring shaped for circular shaped photosensitive areas and anode metallization can be formed on the P^+ region 6384. The anode can also be in the shape of a ring for a circular shaped photosensitive region (or it can be other shapes such as a polygonal). Transmission lines (not shown) connect the anode and cathode to the TIA and ASICs. CMOS/BiCMOS TIA and other ASICs can be fabricated on the low doped layer and other layer(s) may be provided if Ge/GeSi transistors are used and which are not shown in for simplicity. Electrical and/or optical isolation trench(es) 6360 can surround the entire MS-photodetector and in some cases partially surround the MS-photodetector. Many details are not shown, such as passivation, planarization, connecting metals, dielectric layers, antireflections, backside ohmic metallization if necessary, shallow trenches, and TSVs for solder bumps, for simplicity and clarity.

[00416] FIG. 64 is a cross section view showing aspects of a MSPD/MSAPD/MSOWPD/MSOWAPD having surface microstructures and is monolithically integrated with CMOS and/or BiCMOS ICs, according to some embodiments. The CMOS and/or BiCMOS ICs can include: TIAs, equalizers, limiting amplifiers, clock data recovery ICs, and other ASICs for optical data communication. In this example, microstructures are shown for both on top of the semiconductor surface and/or etched into the semiconductor surface. The microstructures 6414 on top of the surface can be a continuation of the semiconductor material above the photodetectors and/or deposited separately.

The upper microstructures 6414 can also be a non-semiconductor material such as dielectric, amorphous semiconductor, metal, a combination thereof, or a combination of semiconductor, non-semiconductor and/or other materials such as transparent conducting metal oxides. The above the surface microstructures 6414 can reduce reflection, and/or channel trapped photons to the photodetecting region and/or supplement the microstructures 6412 etched into the semiconductor to further enhance the absorption. The above surface microstructures 6414 can have any cross sectional shape, for example funnel, inverted pyramids, cylindrical, trapezoidal, V shaped, hourglass, ball shaped and/or a combination of shapes. The lateral shapes of microstructures 6414 can be grating-like, circular, rectangular, polygon, oval, hourglass, amoeba shaped, star shaped, chevron shaped, or combination of shape and sizes. The lateral dimensions of microstructures 6414 can range from 20-10000 nm and the thickness can range from 10-10000 nm. The spacing of microstructures 6414 can range from 10-5000 nm and can be periodic and/or aperiodic.

[00417] The monolithic integrated microstructure enhanced photodetectors and CMOS/BiCMOS electronics may not need further hermetic packaging since the entire chip can be passivated with native oxides and/or dielectrics. However in some cases the entire monolithically integrated MSPD/AMSPD with CMOS and/or BiCMOS electronics chip can be entirely and/or partially hermetically sealed with dielectrics such as silicon oxide, silicon nitride, aluminum oxide, aluminum nitride, polymers such as polyimide, and/or spin-on-glass.

[00418] Yashiki et al, 5 mW/Gbps hybrid-integrated Si-photonics-based optical I/O cores and their 25-Gbps/ch error-free operation with over 300-m MMF, OFC 2015 © OSA 2015 (incorporated herein by reference and referred to herein as "Yashiki") shows a hybrid packaging of photodetector with TIA using a glass and silicon platform. In contrast, according to some embodiments of this disclosure, a MSPD is monolithically integrated with CMOS/BiCMOS ASICs, which can reduce the entire 25 Gb/s optical receiver to a single chip. The single chip can include TSVs (through silicon vias) that can provide a hollow optical waveguide to the MSPD/MSAPD/MSOWPD/MSOWAPD. According to some embodiments, glass may be used to provide a TGV (through glass via) hollow optical waveguide to the MSPD/MSAPD/MSOWPD/MSOWAPD.

[00419] Also shown in FIG. 64, ion implanting and/or diffusion with dopants of P type (N type) can be used to form a P⁺ layer/region 6384. Also, N⁺ connecting wells 6406 can be formed to connect the cathode to a buried N⁺ layer 6404. These structures can be formed according the descriptions of similar structures shown

5 herein (e.g. FIG. 63C).

[00420] FIGs. 65, 66 and 67 are cross sectional views showing aspects of monolithically integrated MSPDs and CMOS/BiCMOS ICs with a through silicon via (TSV), according to some embodiments. As used herein the terms

MSPD/MSAPD/MSOWPD/MSOWAPD collectively can also be referred to as

10 Microstructured Photodetector, MS-PD, or MSPD. FIG. 65 shows a monolithically integrated MSPD such as one shown in FIG. 58 with an MSPD 6510 integrated with CMOS/BiCMOS circuitry 6502 on a silicon substrate. The CMOS/BiCMOS circuitry 6502 be ASICs with TIAs that also include equalizers, limiting amplifiers, clock data recovery, buffers, and/or electrical signal transmitters. In FIG. 65 a TSV
15 6530 is etched through the silicon substrate, which can range in thickness from 300 to 1000 micrometers. The sidewalls of TSV 6530 can be coated with metal and/or dielectrics to assist in guiding the optical signal to the MSPD. A BOX layer 6508 can be used as an etch stop layer for the TSV etching process. In some cases the optical fiber 6562, which can be single mode fiber (SMF) and/or
20 multimode fiber (MMF), is inserted partially into the TSV 6530. The monolithically integrated MSPD 6510 with CMOS and/or BiCMOS ASICs 6502 can be in the form of a single chip and can be solder bumped directly onto a printed circuit board in a flip chip manner. This significantly simplifies packaging when compared to FIG. 1 of Yashiki. The simplification can reduce the cost of the optical receiver by 25% or
25 more.

[00421] FIG. 66 show a integrated structure as in FIGs. 58-64, with the addition of a TSVs 6690 to provide electrical contacts between the CMOS/BiCMOS electronics 6602 to the printed circuit board with the aid of solder bumps that both fix the chip in place and provide electrical connectivity to external circuits. A glass
30 and/or polymer superstrate can be attached to the monolithically integrated chip to provide a light guide to the MSPD 6610 and can also provide an encapsulation for the chip to seal the chip against the environment. An example of such a superstrate is discussed in Yashiki.

[00422] In some cases, the glass and/or polymer superstrate may be attached at wafer level to simplify packaging and in some cases the glass and/or polymer superstrate may be 3D (dimension) printed at wafer level. A through glass via (TGV) 6630 is provided that may be coated with metal and/or dielectric to provide light guiding with minimal loss and in some cases SMF and/or MMF 6662 can be partially inserted into the TGV 6630.

[00423] FIG. 67 is similar to FIG. 66, except showing a 45 degree bend in a light pipe 6730 which allows SMF and/or MMF 6662 to be inserted and/or coupled to, parallel to the plane of the chip which in some cases may be desirable. The light pipe 6730 is a hollow optical waveguide that can be coated with metal and/or dielectric layers. In some cases, the superstrate can be glass and/or polymer and can be applied at the wafer level for example and in some cases can be 3D printed at the wafer level. See, e.g., Pyo et al, 3D Printed Nanophotonic Waveguides, <http://onlinelibrary.wiley.com/doi/10.1002/adom.201600220/abstract> (incorporated herein by reference). In some cases, the optical waveguide 6730 can be made of semiconductor. See, e.g., Miura et al, Modeling and Fabrication of Hollow Optical Waveguide for Photonic Integrated Circuits, Jpn. J. Appl. Phys. Vol. 41 (2002) pp. 4785–4789 (incorporated herein by reference).

[00424] FIG. 68A is a cross section showing a layer structure of Ge and/or GeSi on Si for monolithic integration of an MSPD with CMOS/BiCMOS ASICs, according to some embodiments. The Ge and/or GeSi layer 6802 is low doped and/or not intentionally doped layer with resistivity in the neighborhood of 1-10 ohm-cm or higher. N⁺⁺ and/or P⁺⁺ layer(s) can also be included on opposite sides of the Ge and/or GeSi layer 6802. Layer 6804 is one such layer, and another layer (not shown) could be diffused or grown on top of layer 6802. The doped layers can have a resistivity in the neighborhood of 0.005-0.001 ohm-cm or lower and thickness can range for the doped layers from 50 nm to 500 nm and in some cases from 100 nm to 300 nm. The N⁺ (or P⁺) doped layer 6804 can be buried by selective area ion implantation and/or diffusion of N type dopants in the N⁻ or P⁻ I Si layer, in some cases, the N⁺ layer 6804 can be epitaxially grown on the I Si layer 6806 and in some cases the N⁺ layer 6804 can be selectively etched away in areas where the CMOS/BiCMOS TIA/ASICs will be fabricated together with the Ge/GeSi layer 6802. In some cases, the ion implant and/or diffusion can be a blanket area

implant instead of selective area and the doped region can be etched off prior to CMOS/BiCMOS processing. Ge/GeSi can be grown on the buried N⁺ layer 6804 which is in and/or on top of the low doped Si layer 6806 as shown in FIG. 68A.

[00425] The undoped or low doped layer 6802 can range from 500 nm to 5000 nm and in some cases from 500 nm to 2000 nm. The Ge fraction in the GeSi alloy can range from 0.1 % to 100%, where 100% is all Ge. The Ge and/or GeSi layer 6802 can be grown on a Si layer 6806 that can have a resistivity in the neighborhood of 1-30 ohm-cm or more and a thickness ranging from 0.5 to 2 microns and in some cases approximately 1.1 microns. In some cases the Ge and/or GeSi layer 6802 can be grown on other layer(s) that may be needed for CMOS/BiCMOS electronics, which can include circuitry for: signal processing; conditioning; enhancements; storage; buffering; transmission; and other processes for specific applications such as data centers, high performance computing, and LIDAR. The thicknesses of the Ge/ GeSi layer for MSPD may be determined for desired specific applications, bandwidths, responsivity, voltages, for high bandwidth data rate optical communications for datacenters and/or for high sensitivity lower data rate bandwidth for LIDAR for example. Germanium resistivity verses doping is given by <http://www.ioffe.ru/SVA/NSM/Semicond/Ge/electric.html> (incorporated herein by reference).

[00426] FIG. 68B is a cross section showing some further aspects of a monolithically integrated CMOS/BiCMOS ASICs with a MSPD using a Ge and/or GeSi on Si, according to some embodiments. For simplicity conical cross sectional holes 6812 are shown which can also be inverted pyramids, funnels, cylindrical, hourglass, microstructured optical waveguides and/or any combinations thereof for example. Lateral dimensions of the microstructures holes and/or waveguides can range from 100 nm to 5000 nm and in some cases from 300 nm to 2500 nm, spacings between adjacent holes, waveguides can range from 50 nm to 2500 nm and in some cases from 100 nm to 1000 nm. Microstructure holes 6812 can be periodic and/or aperiodic and any combination of periodic and aperiodic. Vertical depth of the holes and/or waveguides can range from 100 nm to 5000 nm and in some cases from 300 nm to 2000 nm. The microstructured holes/waveguides 6812 can be etched pass the first doped layer 6884 on the surface, and/or into the low doped or undoped region 6802 and in some cases can be etched to the second

doped layer 6804 and in some cases can be etched past the second doped layer 6804.

[00427] FIG. 68B also shows a bottom N^{++} doped layer 6804 that can either be epitaxially grown on the I or low doped Si layer and/or it can be formed by selective area ion implantation and/or diffusion of N type dopants. The N^{++} (or P^{++}) region 6804 can be formed in the silicon I or low dope layer prior to Ge and/or GeSi layer growth. A P^{++} shallow well 6884 can be formed partially on the Ge and/or GeSi surface and on which an anode metallization and electrodes can be formed. A mesa etch to the N^{++} region and the N^{++} region, cathode metallization and electrodes can be formed to compete a P-I-N microstructure photodiode and/or microstructure avalanche photodiode with the addition of a charge and multiplication (avalanche) layers. Passivations are not shown and can be the same as Kang et al 2008 for example. The CMOS/BiCMOS integrated circuits are formed first by etching the Ge and/or GeSi away, and in some cases the etching may not be performed if CMOS and/or BiCMOS are formed on the GeSi. An electrical isolation trench (not shown) is optional. The optional trench can also provide optical isolation. A BOX layer can be included. A reverse bias voltage is applied between the anode and cathode and the high speed electrical signal is extracted from the anode and cathode via a transmission line that is connected to the inputs of electronics such as a transimpedance amplifier (TIA) and/or equalizer and/or other ASICs. Wavelength range can span from 800 nm to 2000 nm and in some cases to 2100 nm or longer if the Ge is not relaxed, and in some cases from 800 nm to 1100 nm, in some cases from 1250 nm to 1350 nm, in some cases from 1250 nm to 1550 nm, in some case from 1000 nm to 1650 nm, in some cases from 900 nm to 1700 nm, and in some cases from 900 nm to 1350 nm. Data bandwidth for a single channel can be 5 Gb/s, 10 Gb/s, 25 Gb/s, 30 Gb/s, 40 Gb/s, 40 and/or 50 Gb/s, 80 Gb/s, 100Gb/s or higher at the output of the electronics of the monolithically integrated chip at at least part of the wavelengths described above depending on the Ge fraction in the GeSi alloy. Responsivity can be 0.1A/W or higher at at least part of the wavelength spectrum, in some cases can be 0.3A/W or higher, in some case can be 0.5A/W or higher and in some case can be 0.8A/W or higher. Using amplification by avalanching process, the responsivity can be higher by 3dB, 6 dB, 9 dB and/or 12 dB, respectively.

[00428] Optical signals can impinge from the top surface as shown. The lateral dimension of the microstructure photodetector (MSPD, MSAPD, MSOWPD, MSOWAPD) can range from 20 to 500 micrometers. In some cases the microstructured (MS) photodetector is circular, and the diameter can range from 20
5 to 500 micrometers or more and in some cases from 30 to 80 micrometers. The MS photodetector can also be illuminated from the bottom through a via (not shown). TSV(s) can be used to solder bump the monolithically integrated chip to the printer circuit board either from the front or from the back as shown for example in FIGs. 65-67. Passivation and/or encapsulation can be used to avoid the use of
10 hermetic packaging.

[00429] The MSPD's large photosensitive area can be used for both single mode fiber and multimode fiber. Since the photosensitive area is large, the alignment of the optical fiber can be passively aligned with alignment tolerances of many micrometers and in some cases 10 or more micrometers which can greatly
15 reduce the cost of packaging. For comparison, with waveguide type detectors having dimensions of a few microns, single mode fiber alignment can have alignment tolerances less than a micrometer. Such tolerances are sometimes achieved using active alignment techniques where a fiber light is transmitted into the fiber during coupling to the waveguide photodiode while the output of the
20 photodiode is monitored. This active alignment can represent a significant portion of the packaging cost.

[00430] In addition, the monolithic integration of MSPDs with CMOS/BiCMOS ASICs can be single MSPD and/or multiple such as 4 MSPDs connected to CMOS/BiCMOS ASICs. In some cases 8, 16, 32 or more MSPDs can be integrated
25 for parallel optical and/or coarse wavelength division multiplexing (CWDM). In addition, for LIDAR applications, the lateral dimension of the MSPD/MSAPD can be 1000 microns and can be a square, rectangular or polygonal shaped MS-photodetector to provide high sensitivity at low reverse bias voltages in the range of -10 to -35V. The use of MS-holes allow the use of thin layers and therefore lower
30 voltages. Commercial Si APDs can have a reverse bias voltage as high as -100 volts for example.

[00431] FIG. 69A and 69B are cross section views showing some aspects of monolithic integration of a MSPD with CMOS/BiCMOS ASICs, according to some

embodiments. Note that some necessary CMOS/BiCMOS layers may not be shown for simplicity. A BOX layer can be included followed by a doped layer 6904 such as N^{++} (or P^{++}) implanted and/or diffused into the device layer of the SOI and/or grown on the device layer epitaxially with resistivity in the neighborhood of 0.01 ohm-cm or less and in some cases 0.001 ohm-cm or less. A low doped or undoped layer 6902 of Si and/or GeSi can be formed with resistivity in the neighborhood of 1-30 ohm-cm or more. Further layers used for the CMOS/BiCMOS ICs are not shown. Thickness of the low doped and/or undoped N^- (P^-) layer 6902 can range from 0.5 to 5 micrometers and in some cases from 0.5 to 2 micrometers. The doped layer 6904 thickness can range from 0.1 to 0.5 micrometers. The BOX layer, if included, can range from 0.2 to 4 micrometers or more. A device layer (not shown) can be formed between the BOX and layer 6904, that can range from 0.1 to 0.3 micrometers. A handle wafer and/or silicon substrate can range from 400 to 1000 micrometers.

15 **[00432]** The highly doped layer 6904 may be grown and/or implanted and/or diffused prior to the low doped and/or undoped layer of Si and/or GeSi 6902 where the Ge fraction is less than 100% and in some cases less than 50% and in some cases less than 40% and in some cases can be relaxed and/or not relaxed. Shown in FIG. 69B, a N^{++} connecting well 6906 can be diffused and/or implanted to make contact with the doped layer N^{++} (or P^{++}) 6904 and cathode metallization such as an ohmic contact and metal electrodes are formed on the doped N^{++} connecting well 6906 which can have a resistivity of 0.01 ohm-cm or less and in some cases 0.001 ohm-cm or less. A shallow trench can be etched around the photosensitive region defined by the P^+ or P^{++} doped region 6984 on the surface of the Si and/or GeSi, to reduce the distance of the diffusion and/or ion implantation to the doped N^{++} layer 6904. The doped N^{++} connecting well 6906 can form a continuous perimeter around the P^{++} region 6984 and/or the connecting N^{++} well 6906 can form a few points such as posts that is non-continuous around the P^{++} region 6984, which can reduce the contribution of capacitance to the over all P-I-N structure. The P^{++} layer 6984 can be formed on part of the surface of the Si and/or GeSi with a resistivity of 0.01 ohm-cm or less and in some cases 0.001 ohm-cm or less, and with an anode metallization to complete the P-I-N structure and microstructure holes 6912 (or waveguides) can be dry and/or wet etched as as

discussed in earlier monolithic integrated structures. The microstructure holes 6912 can be inverted pyramids, be funnel shaped, and/or have cylindrical, conical, or hourglass cross sections. The holes 6912 can be circular, oval, square, polygonal, hourglass, amoeba and/or any combination of shapes. Dimensions, spacings, doping, thicknesses, bandwidths are similar to those discussed earlier such as for example FIG. 68B. For example, the lateral dimensions of the microstructures holes can range from 100 nm to 5000 nm and in some cases from 500 nm to 2500 nm. The spacing between adjacent microstructures can range from 50 nm to 5000 nm, in some cases from 100 nm to 1500 nm and in some cases 20 nm to 2000 nm. The spacing can be periodic, aperiodic or a combination of periodic and/or aperiodic. The depth of the microstructure holes can range from 100 nm to 5000 nm. In some cases the holes can be etched past the first doped layer 6984 and partially into the low doped and/or undoped layer 6902, in some cases entirely through the low doped layer 6902 and partially into and/or past the second doped layer 6904. In some cases, the first doped layer 6984 can be formed after microstructure holes 6912 are etched partially into the low doped and/or undoped region 6902 by selective area ion implantation and/or selective area diffusion of dopants as in FIG. 42. The thickness of the doped layers 6984 and 6904 can range from 100 nm to 500 nm with resistivity in the neighborhood of 0.01 -0.001 ohm-cm or less. The low doped layer 6902 can have a thickness ranging from 0.5 to 5 micrometers and in some cases 0.5 to 2 micrometers. The low doped layer 6902 can have a resistivity in the neighborhood of 1-100 ohm-cm or higher. Data rates from the output of the monolithically integrated MS-photodetector with CMOS/BiCMOS ASICs chips can range from 2-50 Gb/s or higher, 10 to 50 Gb/s or higher, 25 Gb/s or higher, 30 Gb/s or higher, 40 Gb/s or higher, 50 Gb/s or higher, 80 Gb/s or higher, and in some cases 100 Gb/s or higher. Multiple MSPDs and CMOS/BiCMOS ASICs (application specific integrated circuits) can be monolithically integrated on a single silicon chip that can be solder bumped directly to a printed circuit board. The optical signal can enter from the top, the bottom and/or from the side as in FIGs. 65, 66 and 67. Arrays of MSPDs of 4 for example each operating at 25 Gb/s can achieve an aggregated bandwidth of 100 Gb/s and if each each MSPD and associated ASICs can operate at 50 Gb/s then the aggregated bandwidth can be 200 Gb/s. In some cases an array of 4x2 each at 50

Gb/s can achieve an aggregated bandwidth of 400 Gb/s. A 4x4 array can achieve 800 Gb/s. The array can keep increasing to $n \times m$ where n and m are whole numbers, and $n \times m \times BW$ (BW is the output bandwidth of the monolithic chip for each channel, where channel can be a single MS-PD with its associated ASICs) will give the aggregated bandwidth. The diameter, assuming a circular photosensitive area can range from 10 to 500 micrometers, in some cases 25 to 100 micrometers and in some cases 30 to 80 micrometers. The photosensitive area can have other shapes such as square, polygonal, or oval. The distance between multiple MSPDs is determined by applications. For example in parallel optics, the distance can be as much as 250 micrometers, while for other applications, such as imaging or LIDAR, the MSPD can be as closely spaced as a few micrometers. In some applications the spacing may be in a regular and/or irregular patterns,

[00433] MSPDs/MSOWPDs can be operated at a reverse bias voltage in the range of -1 to -5 V applied to the anode and cathode, in some cases at -3.3V. MSAPDs/MSOWAPDs can be operated at a reverse bias voltage in the range -5 to -30V applied to the anode and cathode. These ranges can be applied to monolithically integrated MSPDs/MSAPDs with CMOS/BiCMOS ASICs. described herein, *supra*.

[00434] The wavelength span can range from 800 nm to 1100 nm, in some cases 840 nm to 960 nm, in some cases 940 nm to 1100 nm, in some cases 1100 nm to 1250 nm, in some cases 1250 nm to 1350 nm, in some cases 1350 nm to 1550 nm, and in some cases 1550 to 2000 nm. Responsivity can be 0.1A/W or higher at at least part of the wavelength span, in some cases 0.2A/W or higher, in some cases 0.3A/W or higher, in some case 0.5A/W or higher, in some cases 0.8A/W or higher at at least part of the wavelength span. For MSAPD and/or MSOWAPD, the gain can range from 2-10 or higher, in some cases 2-100 or higher and the responsivity of the MSPD/MSOWPD can be multiplied by the gain factor of 2-10 and/or 2-20 or more. For example, a MSPD having responsivity of 0.5 A/W can correspond to a MSAPD having a responsivity of 5A/W with a gain of 10. In some cases, the gain times bandwidth product can be a constant, and the higher the gain the lower the data rate bandwidth. For LIDAR and some LiFi applications, high sensitivity can be a higher priority than bandwidth in which case

a high gain can be desirable and bandwidth can be in the high Mb/s to low Gb/s. Reverse bias voltage may range in the -20 to -50V. The different wavelength spans depends on the amount of Ge in GeSi alloy.

[00435] In all the monolithically integrated MSPDs with CMOS/BiCMOS ASICs
5 an electrical isolation trench (such as trench 6960) may be used to isolate the MSPD from the electronics. The trench can also isolate stray optical signals from interfering with the electronics.

[00436] In some cases, in all the monolithically integrated MSPDs with CMOS/BiCMOS electronics, transparent conduction metal oxides, semitransparent
10 metal of a few nm thickness, can be used on the top doped layer where the holes are etched through to help reduce series resistance.

[00437] As described herein *supra*, the optical signal can impinge from the top surface and a TSV can be used to contact the electrodes to the bottom of the substrate such that solder bump can be formed to solder bump the monolithic chip
15 directly to a printed circuit board. The optical signal can also be illuminated from the back(or bottom) through a via and the front (or top) side is solder bumped to the printed circuit board. As described herein *supra*, a reflective layer can be used on one surface to reflect back any stray optical signal back to the microstructures for further enhancement of the absorption and to reduce the thickness of the low
20 dope or undoped layer further to increase the bandwidth.

[00438] In some cases multiple MS-photodetectors are integrated with CMOS/BiCMOS electronics to increase the aggregated bandwidths to 100 Gb/s, to 200 Gb/s, 400 Gb/s, 800 Gb/s, 1200 Gb/s or more. In some cases a dense multiple MS-photodetector with CMOS/BiCMOS can be used for imaging such as
25 for LIDAR and/or other robotic applications where high data rates from each MSPD maybe a few Gb/s or less but the aggregated rate from the entire array of MSPDs may be high, such as 100 Gb/s or higher.

[00439] Microstructured holes and/or waveguides for photon trapping for the enhancement of absorption can be applied to single crystalline, poly crystalline,
30 micro crystalline, and amorphous material, and in some cases to polymers, semimetals, semiconductors, dielectrics, glass, and insulators. In the case of insulators, dielectrics and glass, those materials can be doped with photo active ions such as Yt, Er and other rare earth elements and F-center, other color centers,

for optical gain such as for fiber laser, optical disk amplifiers, or holographic image storage. Microstructured holes and/or waveguides for photon trapping for the enhancement of absorption can be applied to the detection of photons and/or the amplification of photons where the material can have gain for example, such as

5 optical amplifiers, light emitting diodes and lasers. In the detection of photons, an external reverse bias voltage is applied between the anode and cathode, in the amplification and/or generation of photons a forward bias voltage is applied between the anode and cathode. In some cases, such a fiber amplifiers, an optical source provides a pump to amplify the optical signal where the microstructure

10 holes can be used to photon trap both the pump source and the optical signal such that photon trapping or slowing can enhance their interaction time for more efficient amplification.

[00440] FIG. 70A is a cross section illustrating some aspects of integration of a MSPD with CMOS/BiCMOS ASICs, according to some embodiments. The MSPD

15 can be a MSAPD, MSOWPD, MSOWAPD, and the ASICs can include TIAs, Equalizers, Limiting Amplifiers, buffers, drivers, other signal processing circuitry, data transmission circuitry, and other computing/storage components using standard CMOS/BiCMOS processing. On a P⁺ Si wafer with resistivity in the neighborhood of 0.02 ohms-cm or less, a N⁻ layer 7002 is epitaxially grown. The

20 layer 7002 can have a thickness of 0.5-2 micrometer, in some cases approximately 1 micrometer, in some cases approximately 2 micrometers, and in some cases 1-5 micrometers or more. N⁻ layer 7002 can have resistivity in the neighborhood of 1-30 ohm-cm or more and in some cases 10 ohm-cm or higher. CMOS/BiCMOS ASICs are formed. In some cases additional layers such as GeSi may be provided

25 for the CMOS/BiCMOS components. The N⁺⁺ shallow well 7084 can be formed on part of the surface and the N⁺⁺ defines approximately the area of photosensitivity for high speed and/or high sensitivity applications. The cathode is formed on the well 7084. The N⁺⁺ well 7084 can be diffused and/or ion implanted with N type ions to a depth ranging from 100 nm to 300 nm and with resistivity in the neighborhood

30 of 0.01-0.001 ohm-cm or less. A multiple energy ion implantation process can be used to for a more uniform distribution of implanted ions. The P⁺⁺ connecting well 7006 to the P⁺ substrate can be formed and where the anode metallization can be formed on the P⁺⁺ well. In some cases the P⁺⁺ connecting well 7006 may not be

needed since the anode for the MSPD can be formed on the bottom of the P substrate such as shown in FIG. 70A. In some cases a metal connecting electrode can be formed from the surface to the P⁺ substrate via a trench (not shown) and in some cases a TSV (not shown) can be formed to the bottom anode metal. As

5 described herein *supra*, the connecting well 7006 can be at a few spots/posts or it can form a continuous perimeter around the photosensitive region defined mainly by the region under the N⁺⁺ layer 7084 where a high electric field can exist with a reverse bias between the cathode and anode with voltages in the range -1 to -4 volts and in some cases -3.3 volts. Microstructures such as holes 7012 and/or

10 waveguides can be etched past the first doped layer 7084 and partially (5% to 95% for example) into the low doped and/or undoped region 7002. In some cases the microstructures can be etched pasts the low doped and/or undoped region 7002 and to the P⁺ (or N⁺) substrate.

Shape, dimensions and spacing of the microstructures are as described herein

15 *supra*, and a combination of holes and/or microstructure optical waveguides can be provided as in FIG. 61. The lateral dimensions of the microstructures can range from 100 nm to 3000 nm and in some cases 300 nm to 3000 nm. The spacing can range from 50 nm to 3000 nm and can be periodic, aperiodic and/or a combination of periodic and aperiodic. The depth of the microstructures can range from 50 nm

20 to 10000 nm, in some cases 300 nm to 2000 nm and in some cases 300 nm to 5000 nm. The cross sectional shape of the microstructure holes can be funnel as shown, inverted pyramid, cylindrical, polygonal, ball like, oval, hourglass, conical, and/or any combination of shapes with multiple sidewall angles achieved by a combination of dry etchings and/or wet etchings. The microstructures can be

25 passivated with native thermal oxide, amorphous semiconductor, dielectric, crystalline semiconductor, micro and/or poly crystalline semiconductor, polymer, and/or any combination of passivations physical, chemical, hermetic and/or non hermetic sealing and/or packaging. Antireflection using dielectric, dielectric stacks, nanostructures, microstructures can be used to reduce reflection. In addition the

30 CMOS/BiCMOS ASICs can be covered with a light shield to minimize interference. An electrical and/or optical isolation trench 7060 may be etched for further electrical and/or optical isolation. As in earlier discussions the integrated MSPD(s)

with CMOS/BiCMOS ASICs can be solder bumped either on the front and/or back surface with appropriate paths for the optical signal to reach the MSPD.

[00441] Not shown for simplicity are the CMOS/BiCMOS structures and interconnect metals to form the ASICs nor the electrodes connecting the MS-PD to the ASICs.

[00442] Depending on the Ge fraction in the GeSi, the wavelength can span from 800 nm to 1600 nm, in some cases from 840 nm to 1100 nm, in some cases from 1250 nm to 1350 nm, in some cases 1500 nm to 1600 nm, in some cases 800 nm to 2000 nm, in some cases 800 nm to 880 nm, and in some cases 1000 nm to 1350 nm. Responsivity can be 100 mA/W or higher at at least a few wavelengths in the span, in some cases can be 200 mA/W or higher at at least a few wavelength in one of the wavelength spans, in some cases 300 mA/W or higher at at least a few wavelengths in one of the wavelength spans, in some cases 400 mA/W or higher at at least a few wavelengths in one of the wavelength spans, in some cases 500mA/W or higher at at least a few wavelengths in one of the wavelength spans, in some cases 600 mA/W or higher at at least a few wavelengths in one of the wavelength spans, and in some cases 700 mA/W or higher at at least a few wavelengths in one of the wavelength spans. Data rate bandwidth from the integrated MSPD(s) and ASICs can range from 10 to 100 Gb/s or higher for a single MS-PD –ASICs integration, in some cases 25Gb/s, in some cases 30 Gb/s, in some cases 40 Gb/s, in some cases 50 Gb/s, in some cases 80 Gb/s and in some cases 100 Gb/s. In a quad configuration where 4 MSPDs are integrated with ASICs, data rate from the integrated chip can be quadrupled to 40-400 Gb/s. With higher number of MSPDs in the array, the data rate can be further increased, approaching 1000 Gb/s or more.

[00443] For some applications such as LIDAR, where high data rate is less important, high sensitivity is more important and an MSAPD and/or MSOWAPD can improve system sensitivity significantly, a low voltage APD is desirable for integration with CMOS/BiCMOS. Using microstructures, the layer thicknesses can be reduced without sacrificing quantum efficiency and therefore the MSAPD and/or MSOWAPD can be operated at voltages less than -30V, in some cases less than -25 V, in some cases less than -20V, in some cases less than -15V, and in some cases less than -10V. Gain for the MSAPD can range from 2-10 and in some cases

2-100. The responsivity of the MSAPD/MSOWAPD can be 10x that of a MSPD/MSOWPD, and can be 20x or more than that of the MSPD/MSOWPD. For example, if the MSPD/MSOWPD responsivity is 0.3A/W and a MSAPD/MSOWAPD with 20x results in responsivity being 6A/W.

- 5 **[00444]** FIG. 70B is a plot showing absorption for an MSPD simulated using using finite difference time domain analysis (FDTD), according to some embodiments. Note that absorption is directly proportional to QE. The absorption is for 0.9 micrometer thick I or low doped region (which can also be the quantum efficiency). The horizontal axis is wavelength from 800 nm to 900 nm. At 850 nm
- 10 wavelength, the absorption coefficient of Si is 535/cm which results in a 5% absorption without microstructure holes. As shown in FIG. 70B, absorption as high as 37% with microstructured holes can be achieved with 0.9 micron thick I and/or undoped Si layer. This is an over 7x improvement over a similar structure without microstructured holes for photon trapping and absorption enhancements. The
- 15 microstructured holes used in this simulation has a hexagonal lattice, funnel cross section, with a diameter of 700 nm, a period of 900 nm, and an etched depth of 600 nm. The total thickness from the surface to the P⁺ substrate is 1.1 microns, referring to the structure of FIG. 70A, the N⁺ surface doped well 7084 is 200 nm thick, the P⁺ substrate thickness can range from 500 to 1000 microns.
- 20 **[00445]** FIG. 70C is a plot showing a FDTD simulation of the optical field in the microstructure holes, according to some embodiments. The simulation is for a 0.9 micron thick I or low doped layer and 0.2 micron N⁺ doped surface layer on P⁺ substrate as in FIG. 70B. The holes are square inverted pyramids using wet etch such as KOH and in a square lattice with a period of 1000 nm. The lateral
- 25 dimension of the microstructure hole is 900 nm per side. An enhanced absorption of 40%, equivalent to 40% quantum efficiency, is simulated which is over 7x a similar structure without microstructure holes. The wavelength span is 800 nm to 900 nm and almost constant 40% across the entire wavelength span.
- [00446]** FIG. 70D is a plot of a data rate bandwidth calculation, according to
- 30 some embodiments. Curve 7020 is for the MSPD simulated in FIGs. 70B and 70C, and curve 7022 is for similar photodiode without microstructure holes taking into account the transit time and RC time of the photodiode. The I or low doped layer is assumed to be 0.9 microns and fully depleted with a reverse bias voltage of

-2 to -3.3V and with a series resistance of 50 ohms. The bandwidth is given in GHz and can be converted to Gb/s by dividing GHz by 0.675 (0.675 is an approximate average, depending on the digital signal coding, NRZ-not return to zero or RZ-return to zero, in some cases it can be 0.5 and in other cases it can be 0.75

- 5 approximately). For example, 24.5 GHz can be 36.3 Gb/s. As can be seen from the curves 7022 for a PD without microstructure holes and curve 7020 solid for a MSPD, the data rate bandwidth can be significantly higher for the same diameter PD. For example at 50 microns diameter, a PD without microstructure holes has a - 3dB bandwidth of 13.6 GHz where as for the same diameter MSPD the - 3dB
- 10 bandwidth is 24.5 GHz or 1.8 times higher bandwidth.

[00447] The MSPD data rate, depending on diameter of the MSPD, can range from 72.6 Gb/s to 7.4 Gb/s with a structure such as FIG. 70A (and in some cases FIG. 69B) where the I or low doped layer is 0.9 microns thick. The material can be Si and/or GeSi and applies for wavelengths from 800 nm to 2000 nm depending on

15 the Ge fraction in the GeSi which can range from 0 to 1 where 0 is all Si and 1 is Ge.

[00448] FIG. 71 is cross section view similar to FIG. 70A with the addition of a BOX (buried oxide) layer. The BOX layer can improve the response of the MSPD by reducing the number of photogenerated carriers outside the high field region

20 between the top N⁺ layer 7084 and bottom P⁺ layer 7104. In addition, the BOX layer can provide a discontinuity in the optical refractive index that can reflect optical signal not trapped in the microstructures in the first pass and reflect the optical signal back toward the microstructures for further absorption enhancements for improved quantum efficiencies. In some cases, in place of a BOX (SOI) wafer, a

25 bulk wafer such as in FIG. 70A can be used with selective area and/or blanket ion implantation of oxygen and/or nitrogen ions into the P⁺ substrate to retard and/or to impede the diffusion of deep photogenerated carriers from diffusing back to the high field region that can cause a slow tail in the impulse response and can degrade the data rate bandwidth of the MS-photodetector. Doping levels of O and

30 N ions can range from 1E17 to 1E22 /cm³ and in some cases, other ions such as metal ions, isoelectronic ions such as H, He, Ar, Ne may be used to reduce the mobility and lifetime of the photogenerated carriers deep in the P⁺ substrate.

[00449] FIG. 72 is a cross section showing some aspects of a MSAPD monolithically integrated with CMOS/BiCMOS ICs, according to some embodiments. The structure is similar to that of FIG. 36 except instead of mesa etching and/or a trench etch to connect N⁺ layer, a connecting N⁺ well 7206 is used and in some cases a trench 7262 can be used between the connecting N⁺ well 7206 and the photosensitive P⁺ region 7284 for electrical isolation and in some cases such a trench 7262 may not be necessary. If an isolation trench 7262 is used, the etch depth can vary and in some cases it continues to the N⁺ layer/region 7204 and in some cases to the multiplication I layer and in some cases through the P charge layer. Such isolation trenches may also be used in MSPDs, MSOWPDs as described elsewhere herein if desirable for improvement in device performance. In addition, an isolation trench 7260 may be used between the MSAPD/MSOWADP and the CMOS/BiCMOS integrated circuits.

[00450] With a reverse bias applied between the anode and cathode of the MSAPD/MSOWAPD with voltages ranging from -8 to -35 volts, the gain can range from greater than 2 to 10 or more, in some cases the gain can range from 2 to 4, in some cases the gain can range from 2 to 8 or more, in some cases the gain can range from 2 to 20 and in some cases from 2 to 100. Gain bandwidth product can range from 20 to 300 Gb/s or more and in some cases 500 Gb/s or more. With gain the quantum efficiency can be 50% or greater, in some cases 80% or greater, in some cases 100% or greater, in some cases 200% or greater and in some cases 500% or greater. Responsivity can be 0.5A/W (amperes/watt) or greater, in some cases 1A/W or greater, in some cases 5 A/W or greater and in some cases 10A/w or greater. The responsivity is for some wavelengths in the range 800-1600 nm, in some cases 800nm to 990 nm, in some cases 800 nm to 1100 nm, in some cases 900 nm to 1250 nm, in some cases 1250 nm to 1350 nm, in some cases from 1300 nm to 1550 nm, in some case 1500 nm to 2000 nm and in some cases 1500 nm to 1600 nm depending on the Ge fraction in the GeSi ally which can range from 0 (all Si) to 1 (all Ge). A shallow P⁺ well 7284 is formed on the surface of the I layer by diffusion of P type dopants and/or by ion implantation of P type ions. The P⁺ well 7284 completes the P-I-P-I-N MSAPD structure, and can have a thickness ranging from 50 to 500 nm and in some cases 100 nm to 300 nm and can have a resistivity in the neighborhood of 0.01 to 0.001 ohm-cm or lower. In addition, a thin

semitransparent metal layer with thickness ranging from 10-100 nm and/or transparent conducting metal oxide (TCMO) such as ITO (not shown) with thickness ranging from 1nm to 500 nm can be deposited on the P shallow well prior to microstructure hole etch. The addition of metal and/or TCMO can assist in

- 5 reducing the series sheet resistance of the P⁺ shallow well 7284. In some cases, it is desirable to have thin P⁺ shallow wells to reduce the generation of photocarriers in the P⁺ well that can reduce the overall quantum efficiency and/or reduce the data rate bandwidth of the MSAPD due to photogenerated carriers in the P⁺ region diffusing to the high field region in the I layer that can result in a slow "tail" in the
- 10 impulse response.

[00451] The I or low doped layer Si and/or GeSi (N⁻) can have a thickness range from 0.5 to 5 microns with a resistivity in the range of 1-100 ohm-cm and in some cases 10 ohm-cm or greater. The P charge layer Si or GeSi can have a thickness in the range 0.05 to 0.2 microns with a resistivity in the range 0.05 to 0.2

15 ohm-cm approximately. The multiplication I Si or GeSi layer can have a thickness ranging from 0 nm to 0.5 microns and with resistivity ranging from 0.5 -1 ohm-cm or greater. The N⁺ layer of Si and/or GeSi can have a thickness range of 0.1-0.5 microns and in some cases 0.1 to 0.3 microns and with a resistivity in the range of 0.005 ohm-cm or less. The N or P Si device layer can be approximately 0.1 to 0.2

20 microns thick. The BOX layer can be a few microns thick on Si substrate. In some cases instead of a SOI wafer, a bulk silicon N⁺ wafer without a BOX can be used. In some cases O, N and other ions can be implanted into a N⁺ Si wafer prior to the growth of the avalanche photodiode layers. See, e.g., FIG. 1 of Kang et al 2008, which shows a Ge on Si avalanche photodiode. A similar structure can be

25 fabricated with microstructured holes and where the holes can be etched through the contact layer and into the absorption layer partially and/or entirely. In some cases the holes can be etched to the charge layer and in some cases through the multiplication layer and in some cases to the bottom contact layer. As in Kang et al 2008, passivation can be amorphous silicon (a-Si) and/or silicon nitride.

- 30 **[00452]** Microstructure holes 7212 can be circular, square, rectangular, polygon, star, amoeba, hourglass, dog bone, oval and/or any combination of shapes and the cross-sectional shapes can be inverted pyramids, funnel, tapered holes, conical, trapezoidal, hourglass, and any combination of shapes created by wet and/or dry

etching and/or electrochemical. Lateral dimensions at the surface of the microstructure holes can range from 200 nm to 5000 nm, in some cases 300 nm to 3000 nm and in some cases 500 nm to 2500 nm. The microstructured holes can be arranged in a random pattern, a periodic pattern, an aperiodic pattern, or a

5 combination of the foregoing. The hole lateral diameter can also be varied in any manner. The spacing between adjacent microstructure holes can range from 20 nm to 3000 nm, in some cases 30 nm to 1000 nm, in some cases 50 nm to 1000 nm, in some cases 100 nm to 1000 nm, and in some cases 100 nm to 600 nm. The microstructure holes can be etched to depths ranging from 50 nm to 5000 nm, in

10 some cases 300 nm to 2000 nm and in some cases 300 nm to 1500 nm. The microstructured holes can be etched first, followed by formation of the P⁺ region 7284 as in FIG. 42. Or the microstructure holes can be etched through the P⁺ region, an any other layers such a thin metal layer 1-20 nm, ITO layer, and/or partially into the I or low doped Si and/or GeSi layer. For example the holes can be

15 etched into 10% of the I or low doped layer thickness, in some cases 20% or less, in some cases 30% or less, in some cases 40% or less, in some cases 50% or less, in some cases 60% or less, in some cases 70% or less, in some cases 80% or less, and in some cases 90% or less. In some cases the microstructure holes can be etched through the I or low doped layer and partially into the charge layer

20 and/or partially into the multiplication layer and/or partially into the N⁺ layer 7204 and/or to the BOX layer and/or if there is no BOX layer, into the N⁺ Si Substrate.

[00453] The N⁺ connecting well 7206 connects the cathode metallization with the N⁺ layer 7204 and can be all along the perimeter of the P⁺ region separated by 2-10x the depletion distance. For example if the I layer is 2 microns then the

25 connecting well can be 4-20 microns or more from the P⁺ region. The connecting well can be a continuous wall and/or posts around the P⁺ region. In addition in some cases without a BOX the avalanche photodiode layers are grown on a N⁺ substrate of milli-ohm-cm range (e.g., 1-30 milli-ohm-cm). The cathode can also be formed on the bottom of the wafer and connecting N⁺ wells may or may not be

30 necessary depending on how the transmission line from the anode and cathode are connected to the CMOS/BiCMOS ASICs. A TSV may be used to connect the bottom cathode to the electrodes of the ASICs. In some cases surface cathodes and anodes are preferred for high speed transmission and the connecting wells are

desirable. In certain applications where high data rates may not be necessary, such as LIDAR applications, a bottom cathode may suffice. An optional light shield 7252 is also shown in FIG. 72.

[00454] FIG. 73 is a cross section view of a structure that is similar to that of FIG. 72 except that a buried N type device layer is included. The selective area buried ion implant and/or diffusion is made into the N type device layer of a SOI can have a thicknesses ranging from 0.2 to 0.5 microns with resistivity in the range 1-30 ohm-cm or more. The ion implanted and/or diffused N⁺ region 7304 can have a resistivity in the range of 6 milli-ohm-cm or less. The multiplication layer and the rest of the avalanche photodiode layers can be grown on the buried N⁺ layer 7304 and the CMOS/BiCMOS ASICs can be integrated on the I or low doped layer and may include extra BiCMOS layers if necessary.

[00455] As in FIG. 72, SOI can be replaced with a bulk N⁺ Si substrate and buried O, N and/or other ions into the N⁺ substrate can be implemented to reduce the diffusion of photogenerated carriers in the N⁺ substrate from diffusion back to the high field regions of the MSAPD.

[00456] FIGs. 74 and 75 are perspective views showing some aspects of a connecting wells for connecting surface electrodes to lower layers, according to some embodiments. The structures as shown in FIG. 73. Although an MSAPD is shown in FIG. 73, the description in FIGs. 74 and 75 apply as well to MSPDs. In FIG. 74, well N⁺ 7206 is wall-shaped and connects the surface cathode 7422 with the bottom N⁺ layer 7304. The P⁺ region 7384 is enclosed by the continuous wall of N⁺ connecting well. Ring-shaped cathode metallization 7422 on top the N⁺ connecting wall-shaped well 7206. A ring-shaped anode metallization 7420 is shown near the perimeter of the P⁺ region 7384. The microstructured holes 7212 are etched into the P⁺ region 7384. Shown in dotted outline is the optional isolation trench 7262. Not shown for simplicity are the monolithically integrated CMOS/BiCMOS ASICs.

[00457] FIG. 75 is similar to FIG. 74 except the connecting N⁺ wells are in the form of a series of post-shaped N⁺ wells 7506. The tops of each of N⁺ wells 7506 are connected by the ring of cathode metallization 7422 encircling the P⁺ region 7384 which has a ring anode metallization 7420. For simplicity, the depth of microstructure holes 7212 is not shown. Also not shown are the integrated

CMOS/BiCMOS ASICs. In some cases, for both the N⁺ connecting wall and the N⁺ connecting posts, the distance to the P⁺ region 7384 can be less and/or equal to the I layer or low doped layer thickness and/or the fully depleted region thickness and in some cases it can be equal to and/or greater than the I layer or low doped layer thickness. For example the distance between the connecting well 7206 or 7506 to the P⁺ 7384 (or N⁺ for N-I-P or N-I-P-I-P structures) can range approximately from 0.5- 10x or more of the I layer and/or low doped layer thickness.

[00458] FIGs. 76A to 76K are diagrams illustrating aspects of a basic process flow for fabricating MSPDs monolithically integrated with CMOS/BiCMOS ASICs, according to some embodiments. Note that the focus is on the MSPD process flow rather than the well-known ASICs processes flow.

[00459] In FIG. 76A shows a simple cross section of a possible CMOS/BiCMOS starting wafer, with a 1.1 microns N⁻ layer 7602 having resistivity in the neighborhood of 10 ohm-cm on a P⁺ silicon substrate 7600 with resistivity in the neighborhood of 20 milli ohm-cm. In some cases the N⁻ layer 7602 can be 2 microns thick or more. In some cases a SOI wafer (dotted BOX layer) can be used with a P⁺ device layer of thickness ranging from 0.2 to 0.5 microns and resistivity ranging from 10 milli ohm-cm to 1 milli ohm-cm or lower. The BOX layer can block the photogenerated carriers in the substrate from returning to the high field I region where they could be swept out and could contribute to a slow diffusion "tail" to the impulse response of the MSPD. Such a "tail" could degrade the bandwidth of the monolithic chip (MSPD integrated with ASICs). The BOX (buried oxide) layer can also provide a low-refractive optical index and can enhance the microstructure holes in higher enhanced absorption. The inverted pyramids microstructure holes (shown in FIG. 76E) have lateral dimension variations from greater than a wavelength (900 nm sides and wavelength at 850 nm for example) to approximately 0 nm at the apex of the inverted pyramid which is much less than the wavelength. In between the surface lateral dimension and the apex, there can be a range of lateral dimensions where the microstructure holes can vary from greater than a wavelength to subwavelength. In certain regions the microstructured holes of the inverted pyramid can behave similar to a lossy high contrast grating (HCG) when there is a large refractive index difference such as the addition of a

BOX layer. In some cases, front end of line (FEOL) processes can include an ion implantation into the P⁺ silicon substrate to a depth of 0.3 to 0.6 microns or more, and in some cases 0.1 to 0.3 microns, of O, N, metal ions, Ar, and/or Xe, with doping ranging from 1×10^{17} to 1×10^{22} ions/cm³. The doping reduces lifetime of photogenerated carriers, and in some cases P type dopants ions such as C, B, Al, Ga, and/or In ions can be implanted 0.01-0.6 microns or more and in some cases 0.1 nm to 300 nm or more, into the P⁺ substrate. This doping reduces lifetime of photogenerated carriers in the P⁺ silicon substrate. Similarly for an N⁺ substrate, N type dopant ions such as C, N, P, As, Sb, and/or Bi can be implanted to depths ranging from 0.1 nm to 600 nm or more and with doping concentration ranging from 1×10^{17} to 1×10^{22} ions/cm³ with doping ranging from 1×10^{18} to 1×10^{22} ions/cm³.

[00460] FIG. 76B shows a shallow surface well 7684 of N⁺ that can be implanted and/or diffused to a depth of 0.2 microns with a resistivity in the neighborhood of 1 milli ohm-cm and can have a range of 20 milliohm-cm or less. The well width can range from 20-80 microns wide in a circular and/or square and/or polygon shape and in this example is 30 microns wide in a circular shape and in selective area. In some cases a thin layer of metal such as Pt, Au, Cu, Al, Ni, Cr, V, or Ag can also be deposited on the N⁺ well of similar diameter and with thickness ranging from 1 to 200 nm prior to microstructure hole etch to assist in the reduction of series resistance. In some case transparent conducting metal oxide can also be use with similar thicknesses.

[00461] FIG. 76C is a cross section view adding P⁺ connecting wells 7606 to connect the surface to the P⁺ substrate 7600. The P⁺ connecting well 7606 can ion implanted and/or diffused and can be a ring (as in 7206 shown in FIG. 74) and/or posts/columns (as in 7506 shown in FIG. 75). In this example well 7606 is ring-shaped/wall-shaped. The P⁺ connecting well 7606 can have a width ranging from 5 to 50 microns and 1.1 microns deep or more and a resistivity in the neighborhood of 10 milli ohm-cm or less and in some cases 1 milli ohm-cm or less. FIG 76D shows anode 7620 and cathode 7622 ohmic metal and metallization on the P⁺ well 7060 and N⁺ region 7684 respectively. In some cases the P⁺ connecting well 7606 may not be necessary and the anode 7620 can be formed on bottom of the P⁺ substrate 7600 and a through silicon via (TSV) and/or deep trench can connect the bottom anode with a surface electrode connecting to the CMOS/BiCMOS ASICs.

[00462] FIG. 76E shows the MSPD with inverted pyramid holes 7612 etched using KOH solutions wet etch on a (100) Si wafer with the square microstructure hole aligned along the wafer flat and the etch is along the (111) lattice plane. This wet etch process can be a back end of line (BEOL) process after the bulk of the processing for the CMOS/BiCMOS integrated circuits are completed. Passivation of the holes can also be a BEOL process. The microstructure holes can be square and can have a side lateral dimension of 900 nm and a period of 1100-1200 nm in a square lattice. The side wall angle is approximately 54.7 degrees from the plane of the surface resulting in an etch depth of approximately 636 nm. In some cases the surface lateral dimension can range from 500 nm to 2000 nm and the spacing between adjacent microstructure holes can range from 100 nm to 500 nm. In some cases, as mentioned earlier, a BOX layer can be included to further enhance the absorption and therefore the quantum efficiency. FIG. 76F is a top view showing a square lattice of square holes 7612. In some cases, it can be aperiodic and in some cases can be arranged in a random manner with same and/or different hole lateral dimensions. In some cases, the microstructure holes can be arranged in a hexagonal lattice. In some cases the microstructure holes can be oriented not parallel to the wafer flat and in some cases different orientations of the wafer such as (111) and (110) can be used and the microstructure holes may or may not be inverted pyramids. See, e.g., Mavrokefalos et al, Efficient Light Trapping in Inverted Nanopyramid Thin Crystalline Silicon Membranes for Solar Cell Applications, Nano Lett. 2012, 12, 2792-2796 (incorporated herein by reference and referred to herein as "Mavrokefalos"), which discusses using inverted pyramids for solar cell applications. In some embodiments of the present disclosure, an external reverse bias is applied to the anode and cathode for high data rate bandwidth absorption enhanced photodiode (or avalanche photodiode) and for high sensitivity MSAPD (microstructure avalanche photodiode) with reduced avalanche reverse bias voltages for imaging, and LIDAR applications. Improvements in efficiency in Mavrokefalos for a solar cell with inverted nanopyramids and a solar cell without inverted nanopyramids is about 170% where as in some embodiments of the present disclosure, the improvement in quantum efficiency can range from 500% to 1000% or more for a photodiode with microstructure holes as compared with a photodiode without microstructure holes. In addition solar cells are not biased

where as MSPD/MSAPD and other microstructure photodetectors operate at a reverse bias with voltages ranging from -1 to -45 volts. In addition, solar cells are not limited by the thickness of the absorption layer since sun light is a constant source (CW constant wave) and no time is involved, in many cases nanostructured pillar and/or hole solar cells are only a few per cent better than a conventional Si solar cell with thick absorption layers and often times the nanostructured solar cells have worst efficiency than a conventional solar cell. In some embodiments of the present disclosure, the micro/nanostructured hole photodetectors have time scales ranging from a few picosecond to tens of nanoseconds, data rate bandwidths from 1 Gb/s to over 100 Gb/s and in some cases less than 1 Gb/s and in some cases from 25 Gb/s to 100 Gb/s or more. Micro and nano structure holes and/or waveguides allow a thinner I or low doped layer of Si and/or GeSi to achieve high data rate bandwidth and high quantum efficiency at the same time. For example, data rates greater than 20 Gb/s and quantum efficiency greater than 50% at 800-850 nm wavelength have not being achieved, to the inventors' knowledge, simultaneously in any known silicon photodiode with a usable wavelength spectrum of 50 nm or more and where the quantum efficiency does not vary by more than 50%, in some cases 30%, in some cases 20%, and in some cases 10% and is not a resonant photodiode where the QE is sharply peaked. In FIG. 4A of Gao et al, the quantum efficiency (QE) monotonically decrease from 60% at 800 nm to 40% at 900 nm and the data rate bandwidth can be maintained at greater than or equal to 20 Gb/s at all the wavelengths. In some cases nano/microstructure holes can be applied to GeSi and/or Ge photodiodes and can achieve high data rate bandwidths and high quantum efficiencies with I and/or low doped layers of less than or equal to 2 microns and in some cases 3 microns and in some cases 5 microns at wavelengths where the bulk absorption coefficient is weak. For example, in the neighborhood of 1000/cm or less, in some cases 2000/cm or less, in some cases 700/cm or less, and in some cases 500/cm or less, as compared to III-V direct bandgap material which can be 5000-10000/cm or more. Without the use nano/microstructure holes, a thick I and/or low doped layer may be used to achieve high QE but high data rate bandwidths at the same time cannot be achieved. In some applications such as for APD, a low avalanche voltage is desirable and with nano/microstructure holes the avalanche voltage can be

significantly less than a comparable APD without nano microstructure holes. A conventional Si APD requires a thick I or low doped region which requires a high reverse bias voltage to deplete the I and/or low doped region before the voltage can be dropped across the multiplication or avalanche region, voltages of -80 to -100 volts are common. Whereas with nano and/or microstructure holes APD, the I and/or low doped region can be thinner by 2 to 10 times or more resulting in a lower reverse bias voltage to deplete the I and/or low doped region before the voltage drop across the multiplication or avalanche region with reverse bias voltages ranging from -10 to -45 volts approximately. This is also another advantage of using nano and/or microstructure holes for MSAPD than cannot be achieved with conventional Si and/or GeSi and/or Ge APD. Applications include monolithically integrated MSAPD with CMOS/BiCMOS ASICs for LIDAR and imaging.

[00463] In addition, in some cases, the microstructure holes can be very complex, as for example in Berenschot et al, Fabrication of 3D fractal structures using nanoscale anisotropic etching of single crystalline silicon, J. Micromech. Microeng. 23 (2013) 055024 (10pp) (incorporated herein by reference) where the 3D structure can be applied to microstructure holes.

[00464] FIGs. 76G to 76K are top views showing some aspects of MSPDs/MSAPDs for integration with CMOS/BiCMOS ASICs on a single silicon chip. In some cases array of MSPD/MSAPD can be integrated with CMOS/BiCMOS ASICs on a single silicon chip. Only a basic masking and processing steps for the MSPD/MSAPD are shown for simplicity.

[00465] FIG. 76G shows the surface N^+ (can also be P^+) well 7684 with a diameter ranging from 10 to 150 microns and in some cases from 25 to 150 microns and in some cases 100 to 500 microns or more. The N^+ surface well 7684 defines approximately the N-i-P junction capacitance and also the photosensitive area for high data rate bandwidth applications. The N^+ well 7684 can be implanted and/or diffused with N type dopants. Other shapes other than circular are also possible, such as square, polygon, triangular, and rectangular. In this example, the N^+ well 7684 is formed on a N^- layer 7602.

[00466] FIG. 76H shows a concentric ring of P^+ connecting well 7606 formed around the N^+ surface well 7684. The connecting ring 7606 can have a width

ranging from 1 to 100 microns and can be spaced from the edge of the N⁺ well 7684 by 1 (and in some cases less than 1) to 50 times the depletion depth, if the depletion depth is 1 micron, then in the range from 1 to 50 microns and in some cases 0.5 to 50 microns. The depth of the connecting P⁺ well 7606 is to the P⁺ substrate 7600 (shown in FIGs. 76A-76E) and in some cases to the P⁺ device layer of a SOI wafer. In some cases, instead of a concentric ring, the connecting P⁺ (or N⁺) well can be a concentric series of posts/columns from the surface to the P⁺ layer (as in wells 7506 shown in FIG. 75). The number of post/column can range from 1 to 20 for example.

10 **[00467]** FIG. 76I shows N and P ohmic metal and electrode to form the cathode 7622 and anode 7620 metallization. The metal can be Al, SiAl, Ti, Pt, and/or Ni, and/or silicides. The width of the metal can range from 1 to 50 microns and the metal thicknesses can range from 50 nm to 5000 nm and in some cases to 10000 nm.

15 **[00468]** FIG. 76J shows coplanar transmission lines 7640 and 7642 attached to the anode and cathode respectively of the MSPD. The transmission lines 7640 and 7642 to the CMOS/BiCMOS ASIC 7604. Not shown are also dielectric and/or polymer layers for the cathode coplanar line to cross over the anode contacts and in some cases the anode and the connecting well can have a gap to allow the
20 coplanar transmission line to cross. In some cases, a dielectric insulating layer may be provided under the coplanar transmission lines.

[00469] FIG. 76K shows the square microstructure holes 7612 that are inverted pyramids as a result of wet KOH etch into the silicon. This can be a back end of line (BEOL) process after the completion of the CMOS/BiCMOS ASICs. The holes
25 are as described earlier and can be 900 nm to each side and a period of 1000nm to 1200nm in this example and in a square lattice. Passivations of the microstructure holes and surfaces are not shown for simplicity. The separation of the MSPD/MSAPD to the CMOS/BiCMOS electronics can range from a few microns to 100s of microns and in some cases from 10 to 500 microns and in some
30 cases from 5 to 1000 microns or more.

[00470] FIG. 77A is cross section view of an MSPD, according to some embodiments. The structure shown is similar to FIG. 76A. A 1.1 micron N⁻ Si layer 7702 epitaxially grown on a P⁺ Si substrate 7700. In this case, a FEOL (front end of

line) CMOS/BiCMOS process is carried out. The P⁺ substrate 7700 is first either blanket and/or selective area ion implanted with a P type dopant ion such as Al, Ga, In that has minimal diffusion during N⁻ growth for example. B ions may be used if the N⁻ layer is grown at a lower temperature. Similarly for an N⁺ Si substrate, N

5 type dopant ions as discussed earlier can be implanted. In this example, the P⁺⁺ ion implanted and/or diffused layer 7704 can be on the surface of the P⁺ substrate 7700 (as shown) or it can be buried beneath the surface and the depth can range from 0 nm to 600 nm for example, and the thickness of the layer can range from 10 nm to 1000 nm or more and with a resistivity ranging from 0.1 to 0.0001 ohm-cm or

10 less. The high doping levels can reduce the lifetime of photogenerated carriers in this P⁺⁺ region 7704 to a few ps approximately and in some cases to less than a few hundred ps and/or also to reduce mobility of photogenerated carriers. In some cases if the substrate 7700 is highly doped already, the addition of more P type ions (or N type ions for N substrate) may not be provided. Preventing the diffusion

15 of photogenerated carriers back to the high field I and/or low doped region under a reverse bias voltage, can reduce the effect of a "tail" in the impulse response of the microstructured PD when illuminated with a short pulse optical laser light. Any energy in the tail can reduce the data rate bandwidth of the microstructure PD. N⁺ surface well 7784 is also shown. The complete MSPD is not shown, the P⁺

20 connecting well and the anode and cathode as in FIGs. 76A-E are not shown for simplicity and for FDTD simulation purposes. The hole size of holes 7712 can range from 600 nm to 2000 nm and the period can range from 900 nm to 3000 nm and can be in a square, and/or hexagonal lattice and/or aperiodic arrangements.

[00471] In some cases the N⁻ layer 7702 can be I and/or P- layer with resistivity

25 equal to or greater than 10 ohm-cm approximately and with layer thicknesses ranging from 1 to 2 microns for I, N⁻ or P⁻ layers and in some cases 1-2.5 microns. In some cases the substrate can be N⁺ and in some cases the surface well can be P⁺ and in some cases the FEOL process of diffusion and/or ion implantation into the N⁺ substrate can be P and/or As ions to a depth ranging from 10 nm to 500 nm

30 and from the surface ranging from 0 nm to 500 nm or more below the surface. Resistivity of this layer can range from 0.01 to 0.0001 ohm-cm or less.

[00472] FIG. 77B is a plot showing a FDTD simulation of the optical field spanning wavelengths from 800 nm to 900 nm interacting with microstructure

holes, according to some embodiments. The holes are inverted pyramid cross sectional shapes in silicon and where the absorption and therefore the quantum efficiency in the I or low doped layer 7702 of 0.9 microns as shown in FIG. 77A as a function of incident wavelength with the optical signal impinging from the surface

5 where the microstructure holes are etched. The microstructure holes are etched with a KOH solution on (100) silicon plane, along (111) planes resulting in an inverted pyramid with 54.7 degree from the plane of the surface. See e.g., Sato, Basic 2 Anisotropic Wet-etching of Silicon: Characterization and Modeling of Changeable Anisotropy, <http://gcoe.mech.nagoya-u.ac.jp/basic/pdf/basic-02.pdf>

10 (incorporated herein by reference and referred to herein as "Sato") which discusses various anisotropic etches for silicon, and where KOH is one of the etchants. Passivation with HF dip and/or oxide, dielectric can be used on the microstructure holes to reduce leakage current. The quantum efficiency can be at and/or just below 40% in the wavelength span of 800-900 nm for square microstructure holes

15 with 900 nm and 1200 nm sides and a square lattice of 1500 nm period. The solid line 7720 is for the 900 nm microstructure hole and the dash line 7722 is for the 1200 nm microstructure holes. In some cases the QE is 30% or more for certain wavelengths in the wave length range 800-900 nm and in some cases the QE is 20% or more for certain wavelengths in the wavelength range 800-900 nm.

20 **[00473]** FIG. 78 is a cross section view of a structure similar to FIG. 76A with a BOX layer (or on a SOI wafer), according to some embodiments. The device layer 7704 is P⁺ and 0.3 microns thick and the BOX 7708 is about 2 microns thick (can have a range from 0.1 to 5 microns or more) and the device layer can be ion implanted as in FIG. 77A and/or diffused or doped during growth to a resistivity in

25 the range from 0.01 to 0.001 ohm-cm or less and an I or low doped N⁻ layer 7702 with resistivity of 10 ohm-cm or more epitaxially grown and/or wafer bonded on the P⁺ layer to a thickness of 1.1 microns. After the N⁺ layer 7884 is formed, square microstructure holes 7812 are etched using KOH solutions resulting in an inverted pyramid with the side wall (111) plane at a 54.7 angle from the plane of the

30 surface. The side of the microstructure holes 7812 are 900 nm in a square lattice with 1200 nm periods. The hole size can range from 600 nm to 2000 nm and the period can range from 900 nm to 3000 nm and can be in a square lattice and/or hexagonal lattice and/or aperiodic and/or random arrangements.

[00474] The complete MSPD is not shown, for example the P⁺ connecting well and the anode and cathode as in FIGs. 76A-C for simplicity and for FDTD simulation purposes.

- [00475]** FIG. 79 is a plot showing a FDTD simulation of the structure shown in
5 FIG. 78 of the optical field interacting with the microstructure holes in silicon. The absorption of the I or low doped N⁻ layer 7702 is 0.9 microns thick (also the quantum efficiency of the MSPD) as a function of the optical signal wavelength from 800 nm to 900 nm impinging on the top surface where the square holes are etched. The solid curve 7920 is for square holes with 900 nm sides in a square
10 lattice with a period of 1200 nm. The absorption and therefore the QE is mostly above 40% from 800 nm to 900 nm and in certain wavelengths it can be over 50%. In some cases, the QE is 30% or more at certain wavelengths in the range 800-900 nm. And in some cases the QE can be 20% or more at certain wavelengths in the wavelength range 800-900 nm.
- [00476]** In some cases, KOH may not be allowed in CMOS/BiCMOS fabrication laboratories due to the possibility of K contamination, in which case TMAH, EDP and other isotropic and/or anisotropic etchants may be used. See, e.g., Sato; Sato et al, Anisotropic etching rates of single-crystal silicon for TMAH water solution as a function of crystallographic orientation, Sensors and Actuators, 73(1999) 131-137
20 (incorporated herein by reference); Bassous, Fabrication of Novel Three Dimensinal Microstructures by the Anisotropic Etching of (100) and (110) Silicon, IEEE Transactions of Electron Devices, ED-25, 10, 1978 (incorporated herein by reference). In addition other combinations of wet etch and/or orientations, not necessary an inverted pyramid, are possible. The wet etched and/or dry etched
25 microstructure holes can be any cross sectional shapes and in addition, different cross sections, for example perpendicular cross sections can have same and/or different cross sectional shapes. See, e.g., Zubel, Anisotropic etching of silicon in solutions containing tensioactive compounds, Proc. of SPIE Vol. 10175 101750L-1 (incorporated herein by reference). In some cases, wet and dry etching can be
30 combined to produce cross sectional shapes that cannot be achieved by either wet or dry etching alone. In some cases wet etch can be used after dry etch to remove surface damage caused by dry etching plasmas.

[00477] In some applications as mentioned earlier, a superstrate can be attached with precision to the monolithically integrated microstructure photodetector and CMOS/BiCMOS ASICs and in some cases the microstructure photodetectors can be an array. The superstrate can be precision molds from three dimensional printing with built in bandpass filters and reflectors for CWDM, and/or precision silicon platforms such as MEMS with or without actuators for movement of mirrors, filters and in some cases the superstrate can be a passive silicon with 45 degree mirror etched to redirect the optical signal that can enter the monolithic chip in plane for example. See, e.g., Hsiao et al, Compact and passive-alignment 4-channel × 2.5- Gbps optical interconnect modules based on silicon optical benches with 45° micro-reflectors, 21 December 2009 / Vol. 17, No. 26 / OPTICS EXPRESS 24250 (incorporated herein by reference); and Rola et al, Triton Surfactant as an Additive to KOH Silicon Etchant, JOURNAL OF MICROELECTROMECHANICAL SYSTEMS, VOL. 22, NO. 6, DECEMBER 2013 (incorporated herein by reference). Rola, Anisotropic etching of silicon in KOH + Triton X-100 for 45° micromirror applications, Microsyst Technol (2017) 23:1463–1473 (incorporated herein by reference and referred to herein as “Rola”), in connection with FIG.1 of Rola an optical fiber is coupled to a silicon bench mirror etched 45 degree to re direct the optical beam perpendicular to the fiber.

[00478] FIG. 80 is a cross section illustrating some aspects of a MSAPD with microstructure holes, according to some embodiments. In this example the microstructure holes 8012 can be inverted pyramids. In some cases the holes are not inverted pyramids and can be more complex. The holes can be etched with wet anisotropic and/or isotropic wet and/or dry, and/or dry etching. Not shown for simplicity are the CMOS/BiCMOS ASICs that can be monolithically integrated with the MSAPD. An electrical isolation trench 8062 can be etched between the anode 8020 and cathode region 8022 as shown in a ring and/or perimeter fashion such that the N⁺ connecting well 8006 can be isolated from the depletion regions. This isolation trench 8062 between the anode and cathode can also be applied to earlier discussed MSPD with connecting wells to isolate the connecting wells from the depletion regions. In this example of a MSAPD, a SOI wafer is used with a BOX layer 8008 thickness ranging from 0.2 to 4 microns or more. A device layer (not shown) can be formed between layers 8008 and 8004 that has a thickness

ranging from 100 nm to 500 nm, and can be diffused and/or ion implanted with N type dopants to a resistivity of 0.01 ohm-cm or less. An epitaxial N⁺ layer 8004 can be grown with thicknesses ranging from 200 to 500 nm and with resistivity of 0.01 ohm-cm or less. A multiplication or avalanche layer 8026 can then be grown with

5 thickness ranging from 0 to 500 nm that can be intrinsic and/or low doped N and with a resistivity of 0.6 ohm-cm or higher and/or 2 ohm-cm for low doped P. A P type charge layer 8028 has a thickness ranging from 50 nm to 200 nm and resistivity in the neighborhood of 0.2 to 0.07 ohm-cm. The I and/or low doped N⁻ layer 8002 has thickness ranging from 0.5 to 5 microns and in some cases 0.8 to 2

10 microns, in some cases 0.8 to 1.2 microns and in some cases 1 microns, and has resistivity 1-10 ohm-cm or higher (in some cases it can be P- layer with resistivity ranging from 5-10 ohm-cm or higher). A P⁺ well 8084 can be diffused and/or implanted to a depth of 50-300 nm and in some cases 100 nm, and in some cases can have a thin layer of metal such as Al, Pt, Cu, Cr, Au, Ag, Ta, V, Zr, W, and/or

15 Fe with thickness ranging from 1 nm to 100 nm and/or transparent conducting metal oxide such as indium tin oxide with thickness ranging from 50 nm to 500 nm that can be deposited on the P⁺ surface prior to microstructure hole patterning and etching. Not discussed are thermal anneals for diffusion processes and for ion implant activation processes and these can be a part of or separate from the

20 CMOS/BiCMOS processes. Passivation is not shown for simplicity and clarity. A N⁺ connecting well 8006 can be diffused and/or implanted (multiple energy if necessary) to form a connection for the surface cathode 8022 to the N⁺ layer 8004. The depth of the well 8006 can be to the N⁺ layer 8004 and/or past the N⁺ layer. The width of well 8006 can range from 1 to 30 microns and the resistivity can be

25 0.1 ohm-cm or less. Cathode ohmic metallization ring 8022 and anode ohmic metallization ring 8020 can be formed as in FIG. 76I for example. An electrical isolation trench 8062 can be etched between the cathode ring 8022 and anode ring 8020. The trench 8062 can be formed to a depth of the N⁺ layer 8004 for example as shown in FIG. 80. Similarly such an electrical isolation ring between the cathode

30 and anode can also be etched for MSPD shown in FIG. 76E for example to a depth where it reaches and/or passes the P⁺ layer 8084. In addition, a second electrical isolation ring and/or perimeter (not shown) can be etched outside the MSAPD and/or the MSPD, and between the MSAPD and/or MSPD, and the

CMOS/BiCMOS ASICs if necessary. The width of the rings can range from 100 nm to 1000 nm or more and can be dry and/or wet etched. In some cases, multiple rings for between the anode and cathode and/or between the microstructure photodetectors and the ASICs can be etched to form a Bragg reflector to confine the light within the MSAPD/MSPD to further enhance absorption and therefore improve the quantum efficiency. Also not shown are the transmission lines connecting the anode and cathode to the ASICs and external power supply that power the ASICs and provide the reverse bias for the MSAPD and MSPD.

[00479] As discussed earlier, the microstructure holes 8012 lateral dimensions can range from 300 nm to 3000 nm or more, in some cases from 500 nm to 3000 nm, and in some cases from 600 nm to 2000 nm. The holes can have any shape, for example, circular, square, rectangle, polygonal, star, amoeba, or fractal. The cross-sectional shape of the holes can be inverted pyramids, fractal, cone, funnel, polygonal, hourglass, amoeba, or continuous curve. Different lattice directions can have different cross sectional shape, and any combinations of shapes by anisotropic, isotropic and/or dry etching. The spacing of adjacent microstructure holes can vary and/or be constant and can range from 50 nm to 500 nm or more and can be periodic such as square, hexagonal lattice, aperiodic, random and/or a combination of periodic and aperiodic. In this example, microstructure holes 8012 can be square with each side ranging from 900-1200 nm and a period ranging from 1000 nm to 1500 nm in a square lattice.

[00480] The layer thicknesses for the MSAPD is thinner than a conventional silicon APD without microstructure holes by a factor of 2 to over 10 with similar quantum efficiencies. Thinner layers of the MSAPD can result in significantly lower reverse bias voltages. For example, instead of -100V in a conventional APD, -45V or less can be achieved with similar gain, and in some cases -30V or less.

[00481] In some cases some or all of the layers, except for the substrate 8000, can be some composition of GeSi where the Ge fraction can vary from 0 to 1 for the MSAPD and MSPD.

[00482] FIG. 81 is a cross section similar to FIG. 80, and illustrating some aspects of a MSAPD with microstructure holes, according to some embodiments. In this case, instead of a BOX layer a N⁺ silicon substrate 8100 is used. A FEOL (front end of line) process of selective and/or blanket ion implantation and/or

diffusion of N^+ type ions into the N^+ substrate 8100 can be performed to form region 8104. The implantation and/or diffusion can be carried out prior to the growth of the multiplication/avalanche layer, charge layer, I or low doped layer. P type ions such as Al and/or Ga is attractive due to its larger size than B and may
5 diffuse less during epitaxial growth. Resistivity of 0.001 ohm-cm or less or a dopant density of $1E20$ or greater and a thickness ranging from 10 nm to 300 nm or more and with a depth ranging from 0 nm to 300 nm or more, can be desirable to reduce the photogenerated carrier lifetime in these regions away from the high electric field to minimize diffusion of the photogenerated carriers back to the high field region
10 that can degrade the high frequency response of the MSAPD. In certain applications where high bandwidth is not necessary. The BOX and/or high doping regions may also not be provided and the low avalanche voltage is the most important factor. Such applications may include LIDAR and image processing. In some cases, some or all of the epitaxial layers can be GeSi with Ge fraction
15 ranging from 0 to 1.

[00483] In some cases, the connecting well 8006, connecting the surface cathode and/or anode to N^+ and/or P^+ layers, can be metal for the MSAPD and MSPD and either a ring or post/columns can be used and the number of post/columns can range from 1 to 25 or more. Trench isolations as discussed
20 earlier may be used for electrical and/or optical isolation.

[00484] In some cases, for the highly doped layers, other atoms may be added to compensate for lattice strain. For example, in highly doped boron layers Ge may be added to compensate for lattice strain with approximately similar amount as the doping ions for example.

25 **[00485]** FIGs. 82A and 82B are cross sectional views of layer structures prior to integration of a MSPD with CMOS/BiCMOS ASICs, according to some embodiments. Shown are variations of structures shown in FIGs. 77A and 78 and prior to microstructure hole etching and connecting wells. In some cases, the I or N^- or P^- low doped layers of FIG. 76A, 77A, 78 can have a thickness ranging from 0.5
30 to 5 microns and in some cases from 1 to 2.5 microns. FIGs. 82A and 82B show further variations of the starting material for CMOS/BiCMOS integration with MSPD. In FIG. 82A the substrate is N^+ 8200 and/or the device layer is N^+ in a SOI. The BOX layer 8208 can have a range in thickness from 0.1 to 10 microns. FIG.

82A is on SOI and the device layer 8204 thickness can range from 100 nm to 500 nm with a resistivity of less than 10 ohm-cm and can be diffused and/or ion implanted with P and/or As ions to a resistivity of less than 0.01 ohm-cm and in some cases less than 0.001 ohm-cm. A P⁺ surface well 8284 can be diffused
5 and/or ion implanted with B and/or Al ions to a depth ranging from 10 nm to 500 nm and can include multiple energy ion implant such that the doping can be uniform to the surface. The width of the P⁺⁺ well 8284 can range from 20 to 100 microns and in some cases from 25 to 80 microns and in some case from 30 to 500 microns or more. In some cases a thin metal and/or transparent conducting
10 metal oxide layer can be added on the surface of the P⁺ region with thicknesses ranging from 1 nm to 500 nm to reduce series resistance, prior to etching of the microstructure holes. FIG. 82B shows a N⁺ substrate 8216 with a FEOL diffusion and/or ion implantation of P and/or As ions to a depth ranging from 10 to 500 nm from the surface of the substrate and can be 0 nm to 500 nm or more beneath the
15 surface after thermal annealing where the dopants may diffuse. The resistivity of the N⁺⁺ layer 8214 can range from 0.01 ohm-cm or less to 0.001 ohm-cm or less to 0.0001 ohm-cm or less. In some cases the addition of N⁺⁺ layer may not be provided if the substrate 8216 is highly doped and/or in some cases where the data rate bandwidth degradation due to diffusion current can be tolerated in certain
20 applications. Not shown in FIGs. 82A and 82B for clarity and simplicity are structures such as the connecting wells and/or electrodes, the cathode and anodes and its metallization and transmission lines connecting the MSPD to the ASICs, the microstructure holes which are similar to earlier figures, passivations, antireflection layers, planarization effects, and dielectric cross-overs for the electrodes. Optical
25 signals can impinge from the surface where the microstructure holes are etched and in some cases the optical signal can impinge from the bottom where a via can be etched.

[00486] In some cases, the monolithically integrated MSPD/MSAPD layer structures can have one or more GeSi layers with Ge fraction varying from 0 to 1
30 and where the layer(s) can have the same and/or different Ge fractions. This can apply to all earlier discussions and later discussions on microstructure photodetectors.

[00487] FIG. 83 is a cross section view showing aspects of a starting layer structure with N^+ surface well, according to some embodiments. The structure is similar to that of FIG. 76B, except with a FEOL (front end of line) ion implant of buried O and/or N ions in the P^+ substrate 8300. See, e.g., Izumi et al, C.M.O.S. 5 DEVICES FABRICATED ON BURIED SiO_2 LAYERS FORMED BY O_2 OXYGEN IMPLANTATION INTO SILICON, ELECTRONICS LETTERS 31st August 1978 Vol.14 No. 1 (incorporated herein by reference); Hauthan et al, Improvement in buried silicon nitride silicon-on-insulator structures by fluorine-ion implantation, J. Appl. Phys., Vol. 83, No. 7, 1 April 1998 (incorporated herein by reference). The 10 implantation energy can range from 50 to 200 KeV or more and the dose can range from 1×10^{14} to 8×10^{18} /cm² (1×10^{14} to 8×10^{18}) or more. B and/or Al can be diffused and/or ion implanted for a P substrate if necessary above the buried O/N region 8314 to from region 8304 having a thickness ranging from 50 to 300 nm and can be 0 to 300 nm below the surface of the P substrate and can have a resistivity 15 of 0.01 ohm-cm or less. For N substrate, P and/or As can be diffused and/or ion implanted similarly and with a resistivity of 0.01 ohm-cm or less. The width of the surface well 8384, N^+ in this case, can range from 20 to 500 microns and in some cases from 25 to 100 microns and in some cases 500 to 1000 microns and can be circular, square, or polygonal. Basic processing steps can be similar to FIGs. 76A 20 to 76F and can include depletion isolation trench ring/perimeter as in FIGs. 80 and 81.

[00488] In some cases, the buried O/N implant may not be provided. In some cases the additional P^+ and/or N^+ doping on the P or N substrate 8300 may not be provided. In some cases both buried O and/or N region 8314 and P^+ or N^+ doping 25 on the substrate 8300 can be provided.

[00489] The O/N buried ion implant can also applied FEOL to MSAPD for example in FIG. 81 a buried oxygen and/or nitrogen layer can be implanted with similar dose as for MSPD followed by P/As diffusion and/or ion implantation for an N^+ layer or region. In some cases, one or more of the layers can be GeSi with Ge 30 fraction ranging from 0 to 1.

[00490] FIGs. 84A and 84B are cross sectional views of a MSPD/MSAPD on SOI and/or a sacrificial layer, according to some embodiments. The structure in FIG. 84A is similar to that of FIG. 71. In this case, the BOX layer 8408 is etched

away selectively in the region 8490 below the microstructure holes 8412 and surrounding regions. An etching trench 8460 or via is dry etched to the BOX layer 8408 and wet etch can be introduced through the etch trench to the BOX or sacrificial layer to be etched mostly away and leaving mostly air beneath the

5 microstructure holes. The wet etch for silicon dioxide can be HF based for example. The etch pattern can be circular and these circular patterns can converge to remove most of the oxide and/or sacrificial layer. In FIG. 84A only the region under the microstructure holes are shown etched mostly away for simplicity. However, in practice the region 8490 may extend into a larger region of oxide

10 and/or sacrificial layer extending roughly equidistance from the etch trench 8460 in all lateral directions with the etch trench 8460 as the center. In some cases some silicon dioxide and/or sacrificial layer may remain as a spacer layer in the form of posts, islands and/or regions to provide separation between the bottom doped layer and the substrate. See, e.g., Judy, Microelectromechanical systems (MEMS):

15 fabrication, design and applications, Smart Mater. Struct. 10 (2001) 1115–1134 (incorporated herein by reference); and Smith et al, Embedded Micromechanical Devices for the Monolithic Integration of MEMS with CMOS, *Proc. 1995 IEDM*, pp. 609-612 (incorporated herein by reference). In some cases, the etch trench/via 8460 can be located in the same region as the microstructure holes 8412 and in

20 some cases can be located between the cathode and anode and in some cases in region outside the ohmic contact regions.

[00491] The removal of the BOX 8408 or sacrificial layer allows higher reflection from the semiconductor-air interface than from semiconductor-silicon dioxide interface. This higher reflection, as shown in FIG. 86 *infra*, can result in an

25 absorption and/or quantum efficiency of greater than 80% for a one micron thick I or low doped N or P layer of silicon at certain wavelengths in the range of 800 nm to 1000 nm. The BOX layer 8408 thickness can range from 0.5 to 10 microns or more and in some cases less than 0.5 microns. The P⁺ layer 8404 can range from 100 nm to 500 nm with resistivity of 0.01 ohm-cm or less. The I or low doped N or

30 P layer 8402 can have a thickness ranging from 0.5 to 5 microns and have a resistivity of 1 ohm-cm or more. The N⁺ surface well 8484 can have a thickness ranging from 50 nm to 500 nm and in some cases can have a thin metal and/or transparent conduction metal oxide layer with thickness ranging from 1 nm to 500

nm and the N⁺ well can have a resistivity of 0.01 ohm-cm or less. The width of the N⁺ well 8484 can range from 20-1000 microns and in some cases from 25 to 100 microns, and can be circular, polygonal, star shaped, and/or any combinations of shapes. The P⁺ connecting wells 8406, in ring/perimeter and/or post form, can be
5 diffused and/or ion implanted to form a connection to the P⁺ layer 8404 and the surface Anode 8420. In some cases, the connecting well 8406 can be formed by dry and/or wet etching holes to the P⁺ layer and filling with conducting material such as silicide and/or metal and/or high doped amorphous semiconductor. Also shown is an isolation trench 8462 between the anode and cathode region, which
10 can serve as a depletion isolation trench ring/perimeter to further reduce parasitic capacitance. In some cases such a depletion isolation ring may not be necessary. In some cases, the depletion isolation ring/perimeter can be etched partially into the I or low doped N or P layer and not entirely to the P⁺ layer. Not shown nor discussed are passivation, thermal anneals, chemical dips, hermetic sealing if
15 necessary, to reduce surface damage and to reduce leakage current.

[00492] The microstructure holes 8412 can have cross sectional shapes as inverted pyramids, funnel, cone, cylindrical, hourglass, keyhole, fractal and any combination of shapes that can be created with wet and/or dry etching and in some cases electrochemical etching. Etch depth of holes 8412 as discussed earlier, can
20 be partially into the I or low doped N or P layer, partially in the surface doped layer, through the I or low doped P or N layer, partially into the bottom doped P⁺ or N⁺ layer, through the P⁺ or N⁺ layer. In some cases if the microstructure holes are etched to the BOX layer, the silicon dioxide can be etched mostly away by using the microstructure holes as a conduit for the wet etch to remove the silicon dioxide
25 and an extra etch trench or via may not be necessary. In some cases, microstructure holes can be etched to the BOX layer and in some cases can be etched into the BOX layer and in some cases pass the BOX layer and into the Si substrate. Mixtures of HF solutions in liquid and/or vapor can be used to remove all and/or mostly all and/or partially the silicon dioxide of the BOX layer and in some
30 cases only dry etching into and/or through the BOX layer is necessary and HF solutions in liquid and/or vapor may not be used at all. In some cases, the microstructure holes 8412 can be used as a conduit for the HF and/or similar oxide etching solutions in liquid and/or vapor to etch all and/or mostly all and/or partially

the silicon dioxide of the BOX layer. In some cases dry etching alone can be used to remove the BOX layer partially and/or entirely by etching the BOX layer via the microstructure holes.

[00493] Microstructure hole lateral dimension can range from 300 nm to 3000 nm and in some cases from 100 nm to 5000 nm, and the spacing between microstructure holes can range from 50 nm to 3000 nm and can be periodic and/or aperiodic and/or any combination of periodic and aperiodic. The microstructure holes 8412 can be in a square and/or hexagonal lattice and/or in a random arrangement that can also have lateral dimension of the holes varying in a pattern and/or random within certain bounds for example within 500 to 1500 nm lateral dimension. The microstructure hole dimensions lateral and vertical and spacing can be optimize for certain wavelength ranges. The variation can be from subwavelength to about 2x wavelength in free space. For example for 1500-2000 nm wavelength the microstructure hole range may be 800 nm to 3500 nm. For wavelength ranges from 800 to 1350 nm the microstructure holes can have lateral dimensions from 500 nm to 2500 nm range, In some cases, one or more of the layers in FIGs. 84A and 84B can be GeSi with Ge fraction ranging from 0 to 1 where 0 is all Si and 1 is all Ge.

[00494] In some cases, mesa etching can be used instead of connecting wells/electrodes. A mesa can be etched and passivated with the connecting electrode in the passivation region and in some cases outside the passivation region. See, e.g., Figure 1 of Kang et al 2008. This can apply to FIG. 84B and all earlier discussions where connecting wells/electrodes were used.

[00495] Quantum efficiency can range from 30% to 90% for at least one or more wavelengths in the range of 800 nm to 1000 nm. With GeSi I and/or low doped layer, quantum efficiency can range from 30% to 90% for at least one or more wavelength in the range of 800 nm to 1350 nm, in some cases from 1000 nm to 1550 nm, and in some cases from 850 nm to 2000 nm. Note that quantum efficiency can be directly related to absorption if carriers are not lost to recombination and scattering in the I or low doped region.

[00496] Data rate bandwidth can range from 3 Gb/s to 10 Gb/s, in some cases 10 Gb/s to 40 Gb/s, in some cases 25Gb/s to 50 Gb/s, and in some cases 25 Gb/s to 100 Gb/s or higher when monolithically integrated with CMOS/BiCMOS ASICs.

[00497] The structure shown in FIG. 84A can also be used for photovoltaic application where there is no external bias voltage and used for converting light to electrical energy. The high efficiency and the inertness of silicon material can be a good candidate for implant under the skin to power electronics such as heart pacers for example. In addition, the structure in FIG. 84A can also be used for energy harvesting of solar energy and convert to electrical energy. The microstructure holes allow a greater angle of incidence and can efficiently convert sunlight over a more hours during the daylight than conventional silicon solar cells.

[00498] FIG. 84B is similar to FIG. 80 except for the etch trench or via 8460 as in FIG. 84A to etch mostly away the silicon dioxide layer beneath the microstructure holes. A depletion isolation trench 8462 can be included if necessary between the anode and cathode and in some cases the depletion isolation trench ring/perimeter can be partially etched through the I or low doped layer and/or through the I or low doped layer into the P charge layer 8428 and/or to the multiplication layer 8426 and/or to the N⁺ layer 8424. As mentioned earlier, some silicon dioxide may be allowed to remain to provide rigidity in the space left void when the silicon dioxide is removed. In a mesa can be etched and the connecting electrode can be outside the mesa area and supported by dielectric and/or poly/amorphous semiconductor that may or may not be a part of the passivation. In addition to the range of thicknesses and resistivity (or doping concentration) given in FIG. 80, the BOX layer 8408 can have a thickness ranging from 0.1 to 10 microns or more. The N device layer can have a thickness range of 100 nm to 500 nm and can have a resistivity of 1 ohm-cm or less and can be further doped by N type ions such as P and/or As in a FEOL process with resistivity of 0.01 ohm-cm or less, followed by epitaxial growth of N⁺ Si layer with resistivity of 0.01 ohm-cm or less and in some cases 0.001 ohm-cm or less with thickness ranging from 50 nm to 300 nm. A multiplication layer I or low doped N⁻ (or P⁻) 8426 with resistivity of 0.5 ohm-cm or more can have a thickness ranging from 0 to 600 nm. P charge P layer 8428 can have resistivity ranging from 0.3 to 0.06 ohm-cm with thickness ranging from 50 nm to 250 nm. I and/or low doped N⁻ (or P⁻) layer 8402 can have thickness ranging from 0.5 to 5 microns and in some cases 0.9 to 2 microns and in some cases 1.2 microns and in some cases 1 micron, with resistivity 1 ohm-cm or greater. A surface P⁺ well 8484 can be formed by diffusion

and/or ion implant of P type ions such as B, Al, Ga, In, and/or C, with resistivity of 0.04 ohm-cm or less. In some cases a thin metal and/or transparent conducting metal oxide such as indium tin oxide can be deposited in top of the P⁺ well with layer thickness ranging from 1 nm to 500 nm prior to microstructure hole etch. The thickness of the P⁺ well can range from 0 nm (Schottky contact) to 500 nm and in some cases from 50 nm to 300 nm. In some cases one or more of the layers can be GeSi alloy where the Ge fraction can range from 0 to 1.

[00499] Microstructure holes 8412 can be inverted pyramids etched with KOH and/or TMAH anisotropic etch with square microstructure holes with lateral dimensions ranging from 300 nm to 1200 nm and in some cases from 600 nm to 2500 nm with an etch sidewall angle of approximately 54.7 degrees. A period of 900 to 2700 nm. In some cases the side dimensions of the microstructure holes can range from 900 nm to 1200 nm and a period ranging from 1000 nm to 1500 nm with square and/or hexagonal lattices. The microstructure holes 8412 can have other cross sectional shapes such as funnel, cone, cylindrical, trapezoidal, fractal, polygonal, hourglass, keyhole, and any other shapes that can be generated with wet, dry, electrochemical etching. The microstructure holes can be circular, oval, rectangular, square, polygonal, star-shaped, string shaped, or amoeba shaped. In a microstructure-photodetector, dimension of the ms-holes (microstructure holes) can be approximately constant. For example, no changes in the lateral dimensions, depth and spacing, and/or any of the dimensions, lateral dimension, depth and/or spacing, can vary in a systematic manner and/or in a non-systematic manner. For example a random manner and any combination of systematic and non systematic. This can apply to all MSPD, MSAPD, and other ms-photodetectors.

[00500] The MSAPD can have a low reverse bias avalanche voltage of less than -30V and reach QE as much as 1300%, in some cases 1000%, in some cases 800%, in some cases 600%, and in some cases 400% at the avalanche voltage. See, e.g., Kang et al 2008. Data rate bandwidth can range from 3 Gb/s to 10 Gb/s, in some cases 10 Gb/s to 40 Gb/s, in some cases 25Gb/s to 50 Gb/s and in some cases 25 Gb/s to 100 Gb/s or higher when monolithically integrated with CMOS/BiCMOS ASICs.

[00501] In some cases, if the MSPD/MSAPD is released from the substrate in regions directly below the ms-holes, the application of an electrostatic voltage between the bottom doped layer (anode or cathode) with respect to the substrate can change the spacing of the air gap between the MSPD/MSAPD and the
5 substrate which can result in a tuning effect of the QE with respect to incident wavelength and may be used to further optimize the QE.

[00502] In some cases for LIDAR applications, in any of the MSPDs/MSAPDs described in this disclosure, the I or low doped layer for photon absorption and trapping can have a thickness ranging from 2 to 10 microns or more. In such
10 cases the microstructure holes can be partially etched into the I layer which in some cases can be GeSi with Ge fraction ranging from 0 to 1 and data rate bandwidth can be less than a few Gb/s. Sensitivity (QE or responsivity, gain) and avalanche voltage can be optimized with the addition of microstructure holes that can reduce the overall thickness of the APD structure while still maintaining desired
15 sensitivity as compared to a comparable APD without microstructure holes.

[00503] FIG. 85 is a top view of a MSPD/MSAPD integrated with CMOS/BiCMOS, according to some embodiments. In this example the MSPD/MSAPD can be as shown in FIGs. 84A and/or 84B. The inner ohmic contact ring and metallization 8422 and outer ring ohmic contact metallization 8420
20 are shown connected to transmission lines that are connected to CMOS/BiCMOS ASICs (not shown). A depletion isolation trench 8462 between the anode and cathode rings is also shown in dotted outline. Several examples of etch trench/vias 8460 are shown as outside the ms-photodetector. In some cases the etch trench/via can be inside the ms-photodetector as also shown in FIG. 85. In some
25 cases, the microstructure holes 8412 can be etched to the BOX layer, in which case, the microstructure holes can be used as a conduit for HP based wet etchant to etch mostly away the silicon dioxide material underneath the microstructure holes in which case etch trench/via may not be necessary in this case. The etch trench/vias 8460 can be any shape and dimension from circular to polygon to slice
30 of pie shape and dimensions can range from sub microns to multi microns and perhaps even 10 microns or more. Square microstructure holes 8412 are shown etched into the surface doped region 8484 that can be N⁺ or P⁺.

[00504] Many structures are not shown for simplicity, such as cross over dielectric isolation, thin metal and/or transparent conducting metal oxide layer, hermetic sealing, and planarization effects. The MSPD/MSAPD can be an array or 2D array that can be monolithically integrated on a single chip with CMOS/BiCMOS ASICs.

[00505] FIG. 86 is a plot showing the results of a FDTD simulation of the optical field on inverted pyramid holes on 1 micron thick silicon with air interfaces on both the top and bottom. The microstructure holes have the following dimensions for the simulations: square holes 900 nm on the side; in a square lattice with period 1000 nm (dash curve 8610); and 1200 nm (solid curve 8612) over a wavelength span from 800 nm to 1000 nm. The vertical axis is enhanced absorption in the 1 micron silicon with microstructure holes. Anisotropic wet etch with 54.7 degree (111) plane side walls on (100) silicon surface using KOH and/or TMAH based etchants.

[00506] Absorption as high as 90% at 920 nm can be seen in the dash plot 8610 and at 850 nm wavelength the absorption is close to 80%. In a similar structure without ms-holes, the absorption is approximately 5%. The enhancement is 1600%. Absorption without any recombination is directly proportional to QE, and in some cases absorption is equal to QE. Air-semiconductor interfaces for both top and bottom can greatly enhance the QE, and as in high contrast grating the lower the absorption the higher the Q which compensate for the low absorption and the high Q enhance the QE as the wavelength approach the silicon bandgap wavelength of 1100 nm at room temperature. Depending on the period, the QE can range from 20% to over 90% at certain wavelengths in the range 800 nm to 1000 nm. In Figure 2 of Kang et al 2008, at avalanche voltage, the Ge on Si APD can achieve a QE of 1400% and at lower voltage bias without avalanche gain the QE is approximately 30% which is approximately 46 times gain or approximately a 17 dB gain. With similar layer structure, and with an avalanche gain of 46, the QE of the MSAPD can range from approximately 900% to 4000% at certain wavelengths in the wavelength range 800 nm to 1000 nm for a silicon MSAPD.

[00507] This high sensitivity can be useful to LIDAR applications in addition to its low avalanche voltage and wide wavelength span and can be integrated with CMOS/BiCMOS ASICs in 1D or 2D arrays. The LIDAR chip can comprise the MSAPD CMOS/BiCMOS array and an array of VCSELs for generating short

pulses. Other applications include LIFI and other free space optical communications.

- [00508]** The MSPD/MSAPD can be used for both single and multimode fiber for short reach, reach gap (1250-1350 nm), long reach data center applications and
- 5 high performance computing applications. FTTH (fiber to the home) can also use MSPD/MSAPD integrated with CMOS/BiCMOS ASICs. With Si and GeSi and Ge on Si, all the wavelengths can be covered using MSPD and/or MSAPD with enhanced absorption, thinner layers, lower bias voltages, and higher data rate bandwidths.
- 10 **[00509]** A fully integrated MSPD with TIA and other ASICs may resemble structures discussed in Analog Devices Inc. product data sheet, for example, where a SiGe photodiode was integrated with CMOS TIA and other ASICs for 11.3 Gb/s at wavelengths ranging from 1300-1330 nm. With the addition of microstructured holes, the SiGe photodiode I or low doped layer can be made
- 15 thinner for higher data rate and also the wavelength range can be extended by 100 nm or more and in some cases by 200 nm or more. And in some cases to 1550 nm wavelength or longer. Responsivity can be 0.3A/W or higher at at least one wavelengths in the wavelength span from 1250 nm to 1550 nm, and in some cases 0.2 A/W or higher at at least one wavelength in the wavelength span from 1250 to
- 20 1550 nm. In some cases the SiGe or GeSi MSPD can have a bandwidth of 25 Gb/s and a responsivity of 0.2A/W or higher at 1550 nm and in some cases the responsivity can be 0.3 A/W or higher and in some cases 0.5 A/w or higher and in some cases 0.6A/W or higher.
- [00510]** At 1350 nm wavelength, the GeSi MSPD can have a data rate
- 25 bandwidth of 25 Gb/s or higher and a responsivity of 0.5 A/W or higher and in some cases 0.3A/W or higher and in some cases 0.6 A/W or higher and in some cases 0.7A/W or higher.
- [00511]** In some cases, isolation trenches can be filled with dielectrics such as silicon dioxide and/or silicon oxide. The etch via trenches can be filled in some
- 30 cases with silicon dioxide/oxide for passivation and hermetic and other purposes to improve performances and reliability. In some cases the entire MSPD/MSAPD can be covered with a dielectric layer such as silicon dioxide, or silicon nitride. In some

cases silicon dioxide may not be stoichiometric and the oxide may be silicon oxide and may be a mixture of silicon dioxide and silicon oxide.

[00512] FIG. 87 is a cross section view of a N-I-P photodiode structure on SOI with a BOX layer, according to some embodiments. Note that the N and P can be
5 interchanged. Not shown for simplicity are structures such as: anode, cathode contacts, mesas, connecting wells, and isolation trenches. For clarity and simplicity only the microstructure holes and the N-I-P layers (8710, 8702 and 8704, respectively) on BOX 8708 are shown. The microstructure holes 8712 can have a range of size and shapes and depth and spacing as discussed earlier, however for
10 purposes of the simulation shown FIG. 88, *infra*, the microstructure holes 8712 are circular, 900 nm in diameter with a cylindrical cross section and a period of 1200 nm. The holes 8712 are etched to the BOX layer 8708 and are filled with SiO₂ and/or SiO_x and have about 10 microns of silicon dioxide/oxide 8770 on the top surface. In some cases, the microstructure holes 8712 can be partially filled with
15 silicon dioxide/oxide and in some cases the microstructure holes can be partially etched into the I or low doped layer 8702. The BOX layer 8708 is 2 microns, the P⁺ layer 8704 is 0.3 microns, the I or low doped layer 8702 is 1 micron and the N⁺ layer 8710 is 0.2 microns. 10 microns of silicon dioxide 8770 is on top of the surface covering the microstructure holes for the FDTD simulation shown in FIG.
20 88, *infra*, of the optical field incident from the top surface. Other range of thickness can be used, the P⁺ can range from 0.1 to 0.5 microns, the I or low doped layer can range from 0.5 to 5 microns and the N⁺ layer can range from 0.1 to 0.5 microns. The dielectric in the hole and on the surface can be silicon oxide and/or dioxide, silicon nitride, and/or other insulating dielectrics that can be polymer for example
25 and the thickness can range from 0 to 20 microns. The microstructure holes can be fully and/or partially filled with dielectrics.

[00513] In some cases, the microstructure holes can be formed partially in and/or through the I or low doped layer and in some cases the microstructure holes can be in the top P or N layer. The holes can be trapezoidal and/or any other
30 shapes such as inverted pyramids and partially and/or fully filled with silicon oxide and/or dioxide.

[00514] In some cases, one or more of the layers can be GeSi where the Ge fraction can vary from 0 to 1 where 0 is pure silicon and 1 is pure germanium.

[00515] FIG. 88 is a plot showing a FDTD simulation of absorption of the incident photons in the I or low doped layer as a function of wavelength from 800-900 nm for the structure shown in FIG. 87. Absorption can be directly proportional to quantum efficiency if all the photogenerated carriers are converted to external
5 current. With an external reverse bias establishing a high electric field in the I or low doped region, most of the photogenerated carriers can be swept to the anode or cathode before the photogenerated carriers can recombine, therefore under these conditions absorption can be equated to quantum efficiency. Three plots are shown in FIG. 88 with periods of 1000 nm (curve 8810), 1200 nm (curve 8812) and
10 1300 nm (curve 8814). Absorption in the I or low doped layer or QE can be 50% at certain wavelength ranges for certain periods. For example, for 850 nm and with a period of 1000 nm with 900 nm diameter microstructure holes the QE can be 50% and at 880 nm wavelength the QE can be 50% with period of 1300 nm and with microstructure hole diameter of 900 nm. In an array of monolithically integrated
15 MSPD/MSAPD with CMOS/BiCMOS ASICs, each photodiode can be optimized for certain wavelengths by having different periods and/or hole diameter and/or hole etch depth.

[00516] According to some embodiments of the present disclosure, the use of micro/nano structure holes enables the enhancement of absorption where the
20 absorption of the material is weak, especially at wavelengths near the bandgap for indirect bandgap semiconductors such as silicon and germanium. By enhancing absorption, thinner layers can be used to achieve higher data rate bandwidth with good quantum efficiency and also lower bias voltages for microstructure avalanche photodiodes.

25 **[00517]** Usable wavelengths for Si MSPD can be extended to 1000 nm. See, e.g.; Gao et al, High Speed Surface Illuminated Si Photodiode Using Microstructured Holes for Absorption Enhancements at 900–1000 nm Wavelength, DOI: 10.1021/acsphotonics.7b00486 (incorporated herein by reference). This is a wider range than GaAs based photodiodes.

30 **[00518]** In some cases, a BOX layer is desirable when the wavelength is above bandgap wavelength of silicon since a BOX layer and/or other methods, as discussed earlier, disrupts the photogenerated carriers in the substrate from diffusing slowly back to the high field region in the I or low doped layer under

reverse bias. The phenomenon of the carriers diffusing back could result in a slow tail in the response of the MSPD/MSAPD that can degrade the data rate bandwidth of the MSPD/MSAPD. For optical signal wavelengths that are below the bandgap wavelength of silicon, the silicon can be mostly transparent and will not generate significant photocarriers in the substrate and the BOX and/or methods to disrupt the lifetime and/or diffusion of photogenerated carriers back to the high field region is less important and may not be provided. GeSi and/or Ge on Si I or low doped layers that absorb in the wavelength region near and/or below the bandgap wavelength of silicon will generate insignificant amount of photocarriers in the silicon substrate and therefore not cause a degradation of the data rate bandwidth of the MSPD/MSAPD.

[00519] However in both cases, above or below the bandgap wavelength of silicon, a BOX and/or where the BOX is etched mostly away under the microstructured holes, will provide a reflection at the semiconductor-dielectric and/or semiconductor-air interface to result in a higher quantum efficiency which is desirable for MSPD/MSAPD devices.

[00520] In some cases, a buried O or N ion implant such as for layer 8314 of FIG. 83 can be implemented in a FEOL process prior to MSPD/MSAPD layer structure growth to improve the QE. In some cases the buried oxide and/or nitride layer can be etched entirely and/or partially away in regions under the microstructure holes by either using the microstructure holes itself as a etching conduits and/or a separate etching trench as discussed earlier to remove fully and/or partially the buried oxide and/or nitride regions under the microstructure holes. Other buried layers can be formed using ion species other than O and/or N such that the buried region can be selectively etched away fully and/or partially to allow a semiconductor-air interface.

[00521] FIG. 89 is a cross section view of an MSPD, according to some embodiments. The structure is is similar to that shown in FIG. 84A except it is not formed on a SOI wafer. A FEOL process on a bulk silicon wafer 8900, P type in this example (but can be N type with P and N interchanged) implants buried O and/or N ions to create a buried mostly oxide and/or mostly nitride region 8934. This region 8934 can be used to provide a refractive index difference between the silicon and region 8934 that reflects light back to the microstructure holes for further absorption

enhancement. In addition, for above bandgap optical signal radiation, this region can also inhibit the diffusion of photogenerated carriers in the substrate from diffusing back to the high field region in the I or low doped region that has a reverse bias applied.

- 5 **[00522]** In some cases the mostly oxide and/or nitride region 8934 can be selectively etched by dry and/or wet and/or vapor mostly and/or entirely away so that the region below the microstructure holes can be mostly and/or entirely air such that the optical field impinging from the from surface travelling through the semiconductor sees a semiconductor-air interface at the bottom beneath the
- 10 microstructure holes 8912. This can provide a higher refractive index contrast and can result in a higher percentage of reflecting optical signal and/or light. The buried oxide and/or nitride 8934 can be etched through the microstructure holes 8912 if the microstructure holes are etched all the way to the buried oxide and/or nitride region. In some cases the holes 8912 can be etched past the buried region 8934.
- 15 As shown in FIG. 89, cylindrical microstructure holes 8912 are etched to the buried oxide and/or nitride region 8934. In some cases, as in FIG. 84A where the microstructure holes are not etched to the buried oxide and/or nitride region, etch trenches 8960 can be used to etch the buried oxide and/or nitride region as shown.
- [00523]** In some cases, instead of a highly doped connecting well, a deep trench
- 20 with oxide 8970 on its sidewalls and the center can have conducting silicide 8972 and/or metal as shown in FIG. 89 which is similar to Kang et al 2008.

- [00524]** The FEOL buried oxide and/or nitride can be formed by a selective area ion implantation. In some cases other species of ions can also be used to generate a buried region that can be selectively etched to create a buried cavity.
- 25 **[00525]** In FIGs. 84A/B and 89, the microstructure holes as in other MSPD/MSAPD structures can have cross sectional shapes such as cylindrical, funnel, cone, inverted pyramids, trapezoidal, hourglass, ball-like, or a combination of shapes. The holes can have a diameter ranging from 300 nm to 3000 nm with spacing ranging from 50 nm to 5000 nm. The spacing can be periodic, aperiodic,
- 30 random or a combination of periodic, aperiodic and random. The depth of the microstructure holes can range from 50 nm to 10000 nm. In some cases the microstructure holes can be on a superstrate and do not penetrate the photodetector structure. The superstrate can be a high K dielectric such as

hafnium oxide and in some cases not a high K dielectric. In some cases the superstrate can be another semiconductor, in some cases the superstrate can be transparent conducting metal oxide, in some cases can be a dielectric and in some cases it can be metal and/or conducting material. In some cases the superstrate
5 can be a combination of dielectric, semiconductor, a conducting material such as metal and/or metal like, polymer and/or conducting polymer. In some cases a superstrate with microstructure holes on top of photodiode and avalanche photodiode can be used without the microstructure holes penetrating the photodetector structure. And in some cases the microstructure holes can penetrate
10 both the superstrate and the photodetector structure and in some cases the holes in the superstrate and the photodetectors are not the same.

[00526] In some cases microstructure holes can be used to enhance the absorption of direct bandgap materials such as materials in the III-V family in cases where the absorbing layer is thin to the point where the absorption efficiency is
15 poor. For example, GaAs at 850 nm wavelength and with the absorbing I or low doped layer of 1 micron or less, the QE can be 40% or less. The addition of microstructure holes can increase the QE by a factor of 2 or more. The same principle can be applied to other material in the III-V family such as InGaAs, InP, InGaAsP, AlGaAs, GaN, InN, AlGaN, InGaN, and AlN. The thin I or low doped
20 layer is important for high bandwidth operation of the photodiode and/or avalanche photodiode. In addition, other material such as a-Si, polymers, CdS, can also benefit from the absorption enhancement of the microstructure holes for imaging, night vision scopes, and LIDAR. Wavelengths can range from 800 nm to 2000 nm depending on the material system. Enhancement of absorption and/or quantum
25 efficiency can be a factor of 1.1 or greater and in some cases factor of 2 or greater for structures with microstructure holes over devices without microstructure holes, for absorbing layer(s) that have QE of 50% or less, in some cases 40% or less and in some cases 20% or less. The low QE can be due to the absorbing layer being 1 micron or less in thickness, in some cases 2 microns or less in thickness, and in
30 some cases 5 microns or less in thickness.

[00527] According to some embodiments of this disclosure, using microstructure holes for enhancing absorption in a reverse biased photodiode can be applied to both indirect bandgap material and/or direct bandgap material and also other

materials such as a-Si, a-Ge, A-GeSi, graphene, photosensitive polymers, and semiconducting oxides.

- [00528]** In some cases, in a forward biased diode application, the microstructure holes can enhance the interaction of photons with the gain in a material. For
- 5 example, microstructure holes in a vertical cavity surface emitting laser can enhance the photon-gain interaction that can result in a more efficient laser and/or higher modulation bandwidth laser. In some cases, the microstructure holes can enhance the light output of a light emitting diode and/or the modulation rate of a light emitting diode.
- 10 **[00529]** As in the case of MSPD, microstructure holes can be etched through the P or N region and into or through the I or low doped region of a vertical cavity surface emitting laser and/or a light emitting diode. Applications include LIDAR laser arrays, detector arrays, lighting, LIFI, data centers, high performance computer, fiber to the home, and enterprise.
- 15 **[00530]** FIG. 90 is a cross section view of a MSPD PIN structure that can be monolithically integrated with CMOS/BiCMOS ASICs on a SOI wafer, according to some embodiments. Note that the CMOS/BiCMOS ASICs are not shown. In this example, the PIN layer thicknesses are approximately 0.2, 1.5 and 0.2 microns respectively and with resistivity of 0.1 ohm-cm or less for the P and N regions and
- 20 1 ohm-cm or greater for the I or low doped region 9002. The thicknesses of the P region 9010 and N region 9004 can vary from 0.05 to 0.5 microns and the thickness of the I or low doped region 9002 can vary from 0.4 to 5 microns. In this example for FDTD simulation of the optical field as it impinges from the top surface (shown in FIG. 91, *infra*), the microstructure holes 9012 are square with a side
- 25 dimension of 900 nm and with a period of 1200 and 1300 nm in a square lattice. The cross section of the holes are trapezoidal, with a side wall angle of approximately 70 degrees and are filled with silicon dioxide to a thickness of 10 microns above the surface. The microstructure holes are etched to 0.3 and 0.5 microns. The BOX layer 9008 is 1 micron. In some cases, the microstructure holes
- 30 9012 can have other cross sectional shapes such as cylindrical, funnel, cone, inverted pyramids, fractal, hourglass, square, polygonal, trapezoidal with side wall angle ranging from about 160 to 20 degrees, or a combination of shapes. The plan view shapes of the holes can shapes such as circular, oval, rectangular, square,

triangular, hexagonal, polygonal, hourglass-shaped, amoeba shaped, star shaped, or fractal shaped. The lateral dimensions at the surface can range from 300 nm to 3000 nm or more. Spacing can range from 50 nm to 5000 nm or more. The spacing can be random, periodic, aperiodic or a combination. The microstructure

5 hole depths can range from 50 nm to 10000 nm or more and in some cases microstructure holes are not etched in the PIN, NIP, PIPIN, PIPN, NINIP, NINP layer structures but rather on a superstrate above the photodetectors. The silicon dioxide can be other dielectrics such as silicon oxide, silicon nitride, hafnium oxide, polymer, and/or any combination of dielectrics and can be fully and/or partially

10 filling the microstructure holes and can be on the surface with thicknesses ranging from 0 to 10 microns or more, as depicted in FIG. 90 as layer 9070.

[00531] In some cases the microstructure holes 9012 are passivated and not filled with dielectric and in some cases the microstructure holes are passivated and filled fully and/or partially with dielectrics.

15 **[00532]** For simplicity, anode, cathode, connecting wells, connecting electrodes, passivation, anti reflection coatings, transmission lines to CMOS/BiCMOS ASICs and other components are not shown.

[00533] FIG. 91 is a plot showing a FDTD simulation of the optical field from 800-900 nm wavelength impinging on the top surface of a structure shown in FIG.

20 90. The vertical axis shows the absorption of the photons in the I or low doped region 9002 (shown in FIG. 90) that is directly proportional to QE and in some cases without recombination and/or scattering, equivalent to QE. The horizontal axis is the incoming optical signal or light wavelength from 800-900 nm. The microstructure holes are square with 900 nm sides in a square lattice with period of

25 1200 nm and 1300 nm and the ms-holes are etched to 0.3 and 0.5 microns deep and filled with SiO₂ and have SiO₂ above the surface to a thickness of 10 microns. Curves 9110, 9112 and 9114 represent the hole depth and periods according to inset legend. The absorption in the I or low doped layer and/or the QE of the MSPD can be 50% or greater at 850 nm for both 0.3 and 0.5 etch depth and with

30 period of 1200 nm. At 880-900 nm wavelengths the QE can be 60% or higher. The QE range from approximately 30 to 60% over the wavelength span and where at some wavelegnth the QE can be as high as 60% or higher. This can be a factor of

2-10 or more higher than a comparable PIN photodiode without microstructure holes.

[00534] FIG. 92 is a cross section view of a two-dimensional (2D) material photodetector that can have an absorption enhancement by employing micro and/or nano holes for photon trapping, according to some embodiments. In this example, the 2D material 9270 can be as discussed in Fiori et al, Electronics based on two-dimensional materials, PUBLISHED ONLINE: 6 OCTOBER 2014 | DOI: 10.1038/NNANO.2014.207 (incorporated herein by reference); Ref. Molle et al, Buckled two-dimensional Xene sheets, PUBLISHED ONLINE: 16 JANUARY 2017 | DOI: 10.1038/NMAT4802 (incorporated herein by reference); and Ref. Mak et al, Photonics and optoelectronics of 2D semiconductor transition metal dichalcogenides, PUBLISHED ONLINE: 31 MARCH 2016 | DOI: 10.1038/NPHOTON.2015.282 (incorporated herein by reference). The 2D material 9270 can be sandwiched between two structures 9272 and 9274 with micro and/or nano holes 9212 for photon trapping and where the material in 9272 and 9274 can be high K dielectrics such as hafnium oxide and in some cases can be non high K dielectrics. The photon trapping structure can enhance the quantum efficiency of the 2D material for detecting photons in the wavelength range of visible to infrared to far infrared. Contacts 9220 and 9222 are made to the 2D material and a voltage and/or current bias can be applied to the contacts for collecting the photogenerated carriers in the 2D material and in some cases no bias need to be applied when operating in a photovoltaic mode. In some cases the 2D material can be stacked with spacer layers of dielectric and contacts can be made to each layer to further improve the QE of the 2D material photodetector efficiency. The micro/nano structure holes 9212 can extend through the 2D material 9270 and/or in some cases not extend through the 2D material and only in the top and/or bottom dielectric and/or silicon 9202. The nano/micro structure holes 9212 can have lateral surface dimensions ranging from 30 nm to 5000 nm or more and spacing between the nano micro structure holes can range from 10 nm to 10000 nm or more. The holes can be shaped as a circle, oval, square, polygon, hourglass, fractal, amoeba, star or a combination of shapes. The cross section of the micro nanoholes can be cylindrical, funnel, cone, inverted pyramids, trapezoidal, fractal, and any other cross sections or combinations that can be achieved by dry, wet, electrochemical,

focused ion beam, vapor or any other etching and combination of etching methods. Other layers not shown can include thin metal, amorphous semiconductor, III-V semiconductor, conducting and/or insulating polymers, glass, doped glass. In some cases, the 2D photodetector arrays and/or stacked arrays can be monolithically
5 integrated with CMOS and/or BiCMOS electronics. In some cases the 2D material can be functionalize to detect chemical species where the QE can change with such detection such that the output voltage and/or current from the contacts can change under a constant illumination of light at certain wavelengths. A superstrate
10 9274 can be used where the micro/nano microstructure holes can be etched without penetrating the 2D material and where the superstrate can be a dielectric and/or semiconductor and/or conductor and any combination thereof. In some cases only the substrate 9200 have micro nano holes and the substrate can be conducting, dielectric, semiconducting and/or any combination thereof.

[00535] FIG. 93 is a cross section view of a MSPD PIN structure similar to that
15 shown in FIG. 90, according to some embodiments. The structure is also similar to those described elsewhere herein of microstructure holes on superstrates in contact with an MSPD/MSAPD. FIG. 93 shows a simple partial cross section schematic of a PIN photodiode structure on SOI wafer that can be monolithically integrated with CMOS and/or BiCMOS electronics. The electronics can include a
20 TIA(s) and/or other ASICs for applications in datacenters, LIDAR, HPC, other optical purposes and/or imaging purposes. The PIN thicknesses are shown for simulation purposes and can range from, N layer 0.05 to 0.5 microns, I layer 0.5 to 5 microns and P 0.05 to 0.5 microns. The N and P layer can have resistivities of 0.1 ohm-cm or less and the I or low doped layer can have resistivity of 1 ohm-cm or
25 more. The top P layer (or N layer if P and N are interchanged) can have a thin metal layer and/or transparent conducting metal oxide layer with thicknesses ranging from 1 nm to 100 nm or more. A dielectric layer 9370 can be deposited on the top surface and can be a high K dielectric layer(s) and/or silicon oxide and/or silicon nitride layer(s) and/or polymer layer(s) and/or spin on glass layer(s), with
30 thicknesses ranging from 0.1 to 10 microns or more. Microstructure holes (and/or nanostructure holes) 9312 can be etched into the dielectric partially (9314) and/or entirely (9316) and/or through the dielectric and into the semiconductor (9318). Etch depth of the microstructure holes can range from 50 nm to 6000 nm or more.

Microstructure hole lateral dimensions can range from 200 nm to 5000 nm and spacing between microstructure holes can range from 50 nm to 5000 nm. The spacing can be periodic, aperiodic, random or a combination thereof.

Microstructure holes 9312 can be circular, oval, cross, polygonal, square, or

- 5 amoeba shaped. The cross section can be shaped as a cylinder, funnel, cone, fishbowl, trapezoidal, box, inverted pyramid, or combination thereof. In some cases, the structure can be an avalanche diode of PIPIN or NINIP or PIPN or NINP. In some cases one or more of the layers can be GeSi with Ge fraction ranging from 0 to 1.

- 10 **[00536]** In some cases the BOX layer may not be necessary when the photon energy is below or near the bandgap energy of silicon where photogenerated carriers outside the high field region and in the silicon region can be less significant. In some cases the BOX layer can be etched partially and/or completely away in regions under the microstructure holes approximately and can extend
15 beyond the regions under the microstructure holes as discussed earlier for example. As discussed earlier, MSPD, MSAPD with BOX layers can have the BOX layer etched partially and/or entirely away in regions under the microstructure holes by using etch trenches for example. The BOX and/or semiconductor-air interface can provide a higher enhancement of the absorption due to reflection at the
20 semiconductor-dielectric and/or semiconductor-air interface.

- [00537]** The operational wavelength can range from 800-1000 nm, in some cases from 850 nm to 1250 nm, in some cases from 1250-1350 nm, in some cases from 1350 to 1550 nm, in some cases from 1350 nm to 2000 nm, in some cases from 950 nm to 1200 nm, in some cases 900 nm to 1350 nm and in some cases
25 from 840 nm to 1350 nm. QE can be 30% or higher at at least some wavelengths in the span. In some cases QE can be 50% or higher at at least some wavelengths in the span, and in some cases the QE can be 70% or higher at some wavelengths in the span. Data rate can range from 1 to 100 Gb/s, in some cases 10 to 25 Gb/s, in some cases from 25-50 Gb/s and in some cases 60 Gb/s or higher.

- 30 **[00538]** Not shown are the anode, cathodes, connecting electrodes/wells, transmission lines to the CMOS/BiCMOS electronics, passivations, antireflections, and other necessary elements to complete a working and operational photodetector integrated with silicon electronics. A reverse bias is applied between

the anode and cathode. The MSPD/MSAPD can be monolithically integrated with silicon electronics for applications in optical interconnects, LIDAR, image processing for example.

[00539] FIG. 94 is cross section showing a structure similar to FIG. 80 except with the addition of a superstrate as shown in FIG. 93. In some cases, a BOX etch trench can also be provided. The superstrate 9470 as in FIG. 93 can be a high K dielectric such as hafnium oxide and/or simply silicon oxide and/or silicon nitride and/or polymer with similar thickness ranges and microstructure hole ranges and parameters as in FIG. 93. In addition, as in FIG. 93, a thin metal and/or transparent conducting metal oxide can be added to the top surface of the P layer 8084. BOX etch trenches 9460 can be included for etching the BOX layer 9408 partially and/or entirely away in regions under the microstructure holes 9312 and vicinity. And in some cases the BOX layer 9408 may not be provided. In some cases, one or more layers can be GeSi where the Ge fraction can range from 0 (all silicon) to 1 (all germanium). Not shown are passivations, transmission lines to CMOS/BiCMOS electronics that can be monolithically integrated with the MSAPD.

[00540] The operational wavelength can range from 800-1000 nm, in some cases from 850 nm to 1250 nm, in some cases from 1250-1350 nm, in some cases from 1350 to 1550 nm, in some cases from 1350 nm to 2000 nm, in some cases from 950 nm to 1200 nm, in some cases 900 nm to 1350 nm, and in some cases from 840 nm to 1350 nm. QE can be 60% or higher at at least some wavelengths in the span, in some cases QE can be 90% or higher at at least some wavelengths in the span, and in some cases the QE can be 150% or higher at some wavelengths in the span. Avalanche gain can range from 2-20dB or more with reverse bias voltage applied to the anode and cathode ranging from -10 to -45 volts and in some cases to -50V.

[00541] Data rate can range from 1 to 100 Gb/s, in some cases 10 to 25 Gb/s, in some cases from 25-50 Gb/s, and in some cases 60 Gb/s or higher.

[00542] Not shown are the CMOS/BiCMOS ASICs. The MSPD/MSAPD can be monolithically integrated with CMOS/BiCMOS ASICs in arrays for parallel optical and/or for CWDM optical communication, for LIDAR, for imaging processing applications and/or other sensor applications. For LIDAR applications, see, e.g., Takai et al, Single-Photon Avalanche Diode with Enhanced NIR-Sensitivity for

Automotive LIDAR Systems, *Sensors* 2016, 16, 459; doi:10.3390/s16040459 (incorporated herein by reference).

[00543] In some cases, the superstrate 9484 can be crystalline and/or non-crystalline, can be epitaxially deposited on the MSPD/MSAPD structure and/or
5 deposited by other methods such as e-beam deposition, chemical vapor deposition, plasma enhanced chemical vapor deposition, and sputtering. The superstrate 9484 can be spun on such as spin-on-glass and/or polymer. The superstrate 9484 could also be bonded to the photodetector assembly by soldering, by Van Der Waals force such as lift-off epitaxy where thin layers are held
10 together by Van Der Waals force, and/or by wafer bonding where pressure and heat can be applied to bond the superstrate to the semiconductor comprising the photodetector. Other methods may include gluing the superstrate to the semiconductor. In addition to microstructure holes 9312 and/or pillars on the superstrate for absorption enhancement by providing some lateral propagating
15 and/or standing and/or leaky and/or evanescent and/or non propagating and/or radiating optical modes in the semiconductor for example can enhance the absorption at certain wavelengths. The dimension of the microstructure holes and/or pillars can range from 100 nm to 50000 nm and the spacing between the microstructure holes and/or pillars can range from 100 nm to 5000 nm depending
20 on the operational wavelengths which can range from 500 nm to 10000 nm. The depth of the microstructure holes and/or pillars can range from 30 nm to 10000 nm. The holes can have cross sections that are in the shapes of a funnel, cone, cylindrical, rectangle, polygon, inverted bell, inverted pyramid, hourglass, ball, or a combination thereof. In some cases, the superstrate can be a semiconductor
25 and/or an insulator that is transparent and/or mostly transparent to the incident optical signal.

[00544] Applications for enhancement of absorption of photons at certain wavelengths and/or wavelength ranges, can include: LIDAR; imaging such as for camera sensors; high speed optical communication; chemical sensors; and night
30 vision. For camera sensor applications, absorption of photons at at single and/or multiple wavelength ranges can be used where sensors are provided in an array and/or stacked where shorter wavelengths can be absorbed first and longer wavelengths absorbed last.

[00545] The microstructure holes and/or pillars can also be used for enhanced emission of photons such as for light emitting diodes and/or vertical cavity surface emitting lasers in cases where a forward bias can be applied to the anode and cathode of a PN or PIN semiconductor structure. In some cases, for LIDAR

5 applications, the I or low doped layer for photon absorption and trapping can have a thickness ranging from 2 to 10 microns or more and the microstructure holes can be partially etched into the I layer which in some cases can be GeSi with Ge fraction ranging from 0 to 1.

[00546] FIGs. 95A and 95B are plots showing a FDTD simulation of the optical
10 field absorption in the I or low doped layers of FIGs 93 and 94 for holes 9314 and 9318 in silicon dioxide and hafnium oxide superstrates with microstructure holes 9312 etched to certain depths as a function of incident optical wavelength from 800 to 1000 nm. In both FIGs. 95A and 95B the holes are square with a side dimension of 900 nm and a period of 1200 nm in a square lattice. In FIG. 95A, the holes are
15 etched to a depth of 1.5 microns and shows approximately an average of 30-35% absorption in the I or low doped layer for either the silicon dioxide or the hafnium oxide. Some of the resonance may be due to interferences between the dielectric layers at the bottom and top of the photodetector, as in the case of a resonant photodiode. In case FIG. 95C, the microstructure holes are etched to a depth of 3.3
20 microns, or approximately 0.3 microns into the semiconductor, shows an approximate average of 50-55% absorption in the I or low doped layer of FIG. 93 and 94. The resonance is less pronounced as in FIG. 95A, and may have lateral modes in the I or low doped region in addition to other optical modes resulting in higher absorption enhancements and therefore higher quantum efficiency and/or
25 responsivity.

[00547] FIG. 95C as in FIGs. 95A-95B are square holes in a square lattice with the same dimensions but etched to different depths in a 3 microns thick silicon dioxide superstrate that is deposited on the silicon photodetectors, the etched depths are 0.5 microns above the silicon surface (curve 9514), at the surface
30 (curve 9516) and 1 microns below the surface (curve 9518). The absorption is plotted as a function of wavelength from 800 -900 nm. In some cases the absorption and therefore the quantum efficiency can be as high as 70% at certain wavelengths but on average the enhanced absorption is between 40-50%. In

some cases, one or more layers can be replaced with GeSi where the Ge fraction can vary from 0 to 1.

[00548] FIG. 96 is a cross section view of a lateral P-I-N photodiode structure that is surface illuminated, according to some embodiments. Although the photodiode is shown in a P-I-N configuration some cases it can be a metal semiconductor metal (MSM) structure and in some cases it can be a N-I-N or P-I-P structure. The I layer 9602 can be intrinsic and/or have a resistivity of 10 to 100 ohm-cm or higher and in some cases 1 ohm-cm or higher. P⁺ well 9606 and N⁺ well 9604 can be implanted and/or diffused to depths of 0.5 to 5 microns for example, and in some cases 1 to 3 microns. Microstructure holes 9612 can be etched in the region of 9612 between the P⁺ and N⁺ region as shown, The P⁺ and N⁺ wells 9606 and 9604 can have a resistivity of 0.1 to 0.001 ohm-cm or less. The distance between the P⁺ and N⁺ wells 9606 and 9604 can range from 2-50 microns or more. A reverse bias can be applied on the anode and cathode with voltages ranging from -2 to -30 volts, and in some cases -3V and in some cases -2 to -10V. The photodetector structure can be grown on a SOI silicon wafer and in some cases on a silicon wafer without a BOX. Microstructure holes 9612 as in described herein *supra*, can have a variety of shapes and sizes, and cross sections, including circular, oval, square, polygonal, bowtie shaped, star shaped, and keyhole shaped. The cross sectional shapes can be any shape including: funnel, cone, inverted pyramid, cylindrical, ball, fractal, or combinations thereof. The holes 9612 can be formed by dry and/or wet etching. Lateral dimensions can range from 100 nm to 5000 nm, in some cases from 500 nm to 3000 nm, and in some cases from 400 nm to 2500 nm. Spacing between adjacent microstructure holes can range from 100 nm to 5000 nm and in some cases from 200 nm to 1000 nm. Depth of the holes can range from 100 nm to 10000 nm and in some cases superstrates can be used as discussed earlier. The electric field applied externally via a reverse bias between the anode and cathode can be predominately perpendicular and/or almost perpendicular to the optical incident ray direction. This is in contrast to many earlier configurations where the electric field between the anode 9620 can cathode 9622 can be predominately parallel and/or approximately parallel to the incident optical ray direction.

[00549] From FDTD simulations, the incident optical waves interact with the microstructure holes and can generate a very complex optical mode pattern with complex optical field directions. The directions can be parallel, perpendicular and/or at some other angle to the applied DC field as a result of the reverse bias voltage applied at the anode and cathode. This set of complex optical modes and fields can enhance the absorption of the incident photons in the semiconductor. Photons absorbed in the I or low doped region can contribute to the high data rate bandwidth response of the photodetector whereas photogenerated carriers outside the high electric field region of the I or low doped layer due to the reverse bias voltage, can result in a degradation of the high speed data rate bandwidth of the photodetector.

[00550] In some cases, one of more layers in FIG. 96 can be GeSi with the Ge fraction x ranging from 0 to 1 ($\text{Ge}_x\text{Si}_{1-x}$ where x can range from 0 to 1). This can be applied to all the photodetector structures described elsewhere herein.

[00551] According to some embodiments the structure shown in FIG. 96 can include multiple interleaving fingers of P^+ and N^+ regions to increase the area of the photodetector for example. The structure can be integrated with CMOS/BiCMOS ASICs into a single monolithic chip. The ASICs can include CDR, LA, TIA, and Equalizers. See, e.g., Ref. Kao et al.

[00552] FIG. 97 is a top view of the structure shown in FIG. 96, according to some embodiments. The structure includes an array of microstructure holes 9612 for absorption enhancement and therefore quantum efficiency enhancement. Also shown are integrated CMOS/BiCMOS ASICs 9770 for signal processing and enhancements and for further data analysis and/or transmission to other electronic circuits. An electrical isolation trench 9760 can be included to separate any potential electrical interference between the photodetector and the ASICs. Transmission lines 9780 and 9782 can be used to connect the photodetector to the ASICs. In addition, arrays of photodetectors can be fabricated and integrated with CMOS/BiCMOS ASICs into a single monolithic chip 9700. Optical signals illuminate the surface and in some cases superstrates can be used to redirect the optical signal whose rays are parallel to the photodetector to illuminate at an angle normal and/or almost normal to the surface of the photodetector. In some cases one or more layers can be replaced with GeSi where Ge fraction can vary from 0 to 1.

[00553] According to some embodiments, the structure shown in FIG. 97 can be repeated, where multiple anodes and multiple cathodes are “interleaved” with an array of microstructure holes between each anode and cathode. Such a structure can be thought of as an interleaved fingers pattern.

5 **[00554]** FIG. 98 is a top view of an integrated MSPD/MSAPD, according to some embodiments. The MSPD/MSAPDs 9810 can be formed with or without superstrates, as described herein *supra*. Monolithically integrated to CMOS/BiCMOS ASICs 9870 can include functionality such as transimpedance amplifier, clock data recovery, limiting amplifier, and equalizer. In the example
10 shown chip 9800 include the ASICs 9870 and MSPD/MSAPDs 9810 in a 1x4 configuration (i.e. one ASICs module paired with four MSPD/MSAPDs. Other configurations such as 1x10, 2x5, and 2x4 are also possible. In some examples, the 1x4 configuration shown can be 4x 25Gb/s for a total of 100 Gb/s or 4x 50Gb/s for a total of 200 Gb/s. The MSPDs/MSAPDs 9810 can be spaced by 250 microns
15 center to center with the diameter of the photodetectors ranging from 25 to 80 microns and in some cases 30 to 50 microns. An optional electrical isolation trench 9860 can be included that can be filled with dielectric and/or amorphous semiconductor. A number of bond pads 9806 can be provided. Not all elements are shown for simplicity. Examples of structure that could be included but are now
20 shown include: anti reflection coatings, passivations, planarization effects, transmission lines, mesas, and implanted wells. Also the correct number of bond pads may not be shown. The chip size can vary from 1.5 mm x 1.5 mm to 3 mm x 3 mm or more depending on the number of photodetectors and the ASICs.

[00555] In some cases one of more layers can be replaced with GeSi and where
25 the Ge fraction can vary from 0 to 1. In some cases, the MSPD/MSAPD with or without superstrates can have one or more of its layer made of a III-V family material. The substrate can be made of a III-V family material. The inclusion of microstructure holes in III-V material can enhance absorption and therefore the quantum efficiency of thin III-V material photon absorbing layer with thicknesses
30 less than 2000 nm for example and in some cases with thicknesses equal to or less than 1000 nm. When the III-V or II-VI material is thin for high speed or high data rate bandwidth operation the quantum efficiency and/or responsivity can suffer from the reduced thickness resulting in reduced absorption of photons. With

the addition of microstructure holes, the absorption can be enhanced and therefore the quantum efficiency by a factor ranging from 1.5 to 10 or greater as compared to a similar structure without microstructure holes.

- [00556]** FIG. 99A is a cross section schematic of a microstructure enhanced III-V photodiode, according to some embodiments. For further detail of III-V photodiodes, see, e.g., K.W. Carey et al, Characterization of InP/GaInAs/InP heterostructures grown by organometallic vapor phase epitaxy for high-speed pin photodiode, Journal of Crystal Growth 1986 (incorporated herein by reference). The light absorbing region 9902 is an I or low doped InGaAs and/or InGaAsP layer of 1500 nm thickness. The I layer 9902 is cladded by InP P and N type material (layers 9904 and 9906) The substrate 9900 is InP N or be semi insulating. The photodiode is used to detect photons at 1300 nm. To increase the data rate bandwidth of the photodiode, a thinner InGaAs photon absorption layer 9902 can be used to reduce the photogenerated carrier transit time under a reverse bias applied between the anode and cathode. The reduced thickness of the InGaAs layer can result in lower quantum efficiency and/or responsivity. Microstructure holes 9912 are etched into the P-I-N structure at depths ranging from 100 nm to 3000 nm. Microstructure holes can be shaped as discussed earlier (e.g. funnel, cone, cylindrical, inverted pyramids, etc.), and have lateral dimensions ranging from 300 nm to 5000 nm. The spacing of the microstructure holes can range from 100 nm to 3000 nm. The microstructure holes can be in a periodic array, aperiodic arrangement or random arrangements. The diameter of the photosensitive area can range from 10 to 100 microns or more. In some cases the diameter of the photosensitive area can range from 5 to 50 microns. In some applications where data rate may not be high, but the photon absorption region needs to be thin, the addition of microstructure holes can enhance the absorption and therefore the quantum efficiency and/or responsivity. In some cases a superstrate can be utilized as discussed earlier. And in some cases the substrate 9900 can be silicon.
- [00557]** In some cases, a III-V avalanche photodiode can be fabricated with microstructure holes in a P-I-P-I-N structure where the I layer between the P layers can be InGaAs and/or InGaAsP and microstructure holes can be etched partially into the top P layer and/or partially into the I absorption layer and/or entirely into

the I absorption layer. In some cases, a superstrate as discussed earlier can be implemented on the avalanche photodiode with microstructure holes. See, e.g., Chen et al, Optimization of InGaAs/InAlAs Avalanche Photodiodes, Nanoscale Research Letters (2017) 12:33 (incorporated herein by reference) which discusses

5 InP/InGaAs APDs without superstrate or holes. The microstructure holes with depth from the surface of the semiconductor ranging from 50 nm to 3000 nm and can have cross sectional shapes of funnel, cone, inverted pyramids, cylindrical, polygonal and/or any combinations of shapes, and the microstructure holes (applies to III-V photodiodes also) can be circular, square, polygonal, star, oval,

10 fractal, keyhole and/or any combination of shapes, with lateral dimensions ranging from 300 nm to 5000 nm and with spacing between the microstructure holes ranging from 100 nm to 3000 nm or more and can be periodic and/or aperiodic and/or random. Wavelength ranges can span from 800-1600 nm depending on the III-V material combination of binary, ternary and/or quaternary. Quantum efficiency

15 can range from 50% or higher at certain wavelengths and in some cases 70% or higher at certain wavelengths and in some cases 90% or higher at certain wavelengths and in some cases with avalanche gain due to a reverse bias between the anode and cathode can be 200% or higher and in some cases 400% or higher at certain wavelengths. Data rate bandwidth can range from 1 Gb/s to

20 100 Gb/s or higher depending on the thickness of the layers and size of the photodetector that can contribute to junction capacitance.

[00558] In some cases, a superstrate can be used with the III-V APD with microstructure holes. And in some cases one or more layers can be II-VI material family and in some cases the wafer can be silicon. In some cases one or more

25 layers can be non crystalline and applies to all the structures discussed.

[00559] Applications can include optical data communication, LIDAR, imaging, sensing, and other applications requiring high quantum efficiency optical detection that converts photons to electrons for further image processing or information processing. In some cases, the III-V photodetector can be a AlGaAs/GaAs

30 structure for wavelengths ranging from 800 to 900 nm

[00560] FIG. 99B is a plot showing an FDTD simulation of the the structure shown in FIG. 99A. The following parameters where used for the simulation: P-AlGaAs (30% Al) 1 micron thick; I GaAs 1 micron thick; N AlGaAs (30% Al) 1

micron thick; and GaAs semi insulating substrate. The Microstructure holes were funnel shaped etched 1.5 micron deep, diameter 700 nm with a period of 1000 nm in a square lattice. The vertical axis is absorption and the horizontal axis is wavelength in microns. Curve 9922 is for the structure without microstructure holes and curve 9920 is for the structure with microstructure holes. As can be seen, the absorption and therefore the quantum efficiency QE with microstructure holes on the III-V MSPD can be 2 times or greater than a similar III-V photodiode without microstructure holes at at least one or more wavelengths in the span from 800-900 nm for GaAs and 1200 nm to 1600 nm for InGaAs absorption layers. The reduction in thickness of the I layer can significantly increase the data rate bandwidth of the III-V MSPD to 40 Gb/s or higher, in some cases 50 Gb/s or higher, in some cases 80 Gb/s or higher and in some cases 100 Gb/s or higher. This is while maintaining a QE that is higher than a similar III-V photodiode without microstructure holes by a factor of 1.5 times or more at certain wavelengths. Optical signals impinge from the top surface and in some cases from the bottom surface and photons are absorbed in the I layer. The same principle can be applied to III-V MSAPDs with the addition of avalanche layer(s). The addition of microstructure holes in an APD (Si, GeSi or III-V) can increase the QE and sensitivity and responsivity due to photon trapping over a similar structure without microstructure holes. Other attributes for an APD can be lower avalanche voltages of an APD with microstructure holes as compared to a comparable APD without microstructure holes.

[00561] FIG. 100 is a cross section of a MSPD, according to some embodiments. A PINP photodetector structure is shown with an optional BOX layer. The structure could also be a MSAPD with added avalanche layers. The photodiode PIN layers 10006, 10002 and 10004 are grown on a P layer 10010 such that a second anode 10024 can provide a forward or reverse bias between anode 10024 and cathode 10020, while the photodiode PIN provides a reverse bias between the anode 10022 and cathode 10020. A reverse bias between anode 10024 and cathode 10020 can help reduce the effect of the slow diffusion of photogenerated carriers outside the high field I region. The forward biasing of the bottom PN layer provides a current injection at the interface between the bottom PN junction. In some cases, with a high enough current injection the P layer 10010 with resistivity ranging from 0.1 to 0.001 ohm-cm or less can change in its

refractive index and in some cases can become more metallic therefore reflecting more of any photons that were not trapped by the microstructures back toward the photon trapping microstructure holes and/or other microstructures. This extra reflection of photons at the bottom PN junction can further increase the QE of the MSPD/MSAPD. In some cases the bias between anode 10024 and cathode 10020 can be modulating. In some cases the bias can be forward, reverse either modulating, DC or both. Mixing, heterodyne, homodyne, of RF with detected optical signals may improve signal to noise ratio, RF transmission applications, and other applications requiring high fidelity of signal.

10 **[00562]** The material can be silicon and/or in some cases one or more layers can be GeSi with Ge fraction x ranging from 0 to 1. In some cases, the material can be a non-silicon material, such as one or more layers being a III-V family and/or II-VI family material.

15 **[00563]** Microstructure holes 10012 and/or other microstructures are formed as described herein *supra*. The lateral dimensions, spacing, cross sectional shapes, depth, and other parameters such as wavelength, data rates, monolithic integration, QE, responsivity are as in any of the MSPD/MSAPD structures described herein *supra*.

20 **[00564]** In some cases, the PINP MSPD can have gain such as a PNP bipolar transistor. Such MSPDs with gain can be advantageous due to the low voltage nature and having transistor like gain.

25 **[00565]** In some cases the P Si layer 10006 can be 0.2-0.3 microns thick with doping with boron to concentration greater than 1×10^{20} ions/cm³. The I layer 10002 can have thickness ranging from 1.0 to 2.0 microns with background doping concentration of less than 1.5×10^{15} ions/cm³. The N layer 10004 can have thickness ranging from 0.2-0.3 microns with doping concentration of arsenic greater than 1×10^{19} ions/cm³. The P device layer 10010 can have thickness ranging from 0.1 to 0.25 microns. The optional BOX (buried oxide) 10008 can have thickness ranging from 1 to 4 microns on silicon handle wafer 10000.

30 **[00566]** FIG. 101 is a cross section of a MSPD (or MSAPD) with a mesa and the regions under the microstructure holes selectively removed, according to some embodiments. In this example, the BOX layer 10108 is fully and/or partially removed to provide a higher refractive index contrast between the microstructure

hole semiconductor regions. Instead of silicon dioxide, region 10110 can be mostly air which has a refractive index of 1 instead of approximately 1.45 for silicon dioxide. This higher refractive index contrast can further improve the enhancement of absorption in the microstructures 10112 and therefore improve the QE and

5 responsivity. FIG. 101 shows cylindrical holes 10160 that are etched to the BOX layer 10108 with dimensions similar to the microstructures 10112. Microstructures 10112 are not etched all the way to the BOX layer 10108 and can be any shape such as inverted pyramids, funnels, cones, or combination of shapes that can be achieved with dry and/or wet etching.

10 **[00567]** The microstructured holes 10160 that are etched to the BOX layer can have lateral dimensions ranging from 300 nm to 3000 nm and can be an array spaced ranging from 1000 nm to 10000 nm. The shallower microstructure holes 10112 can have lateral dimensions ranging from 300 nm to 3000 nm and spacing ranging from 50 nm to 3000 nm. Microstructure holes 10112, as discussed earlier,

15 can have surface shapes such as circular, oval, square, polygonal, hourglass, star, amoeba, fractal, or combinations of shapes, and cross sectional shapes such as inverted pyramids, funnels, cones, cylindrical, polygonal, hourglasses, balls, fractals or combinations thereof.

[00568] In some cases all or mostly all of the microstructure holes can be etched

20 to the BOX layer. In some cases some of the microstructure holes can be etched to the BOX layer and in some cases the microstructure holes that are etched to the BOX layer can be in a periodic array and/or aperiodic ally arranged and/or arranged in a pattern such as circular for example to further assist confining the photons to regions for photon trapping with microstructures.

25 **[00569]** The material in FIG. 101 can be silicon or one or more layers can be GeSi with Ge fraction x ranging from 0 to 1. In some cases, one or more layers can be a III-V and/or a II-VI material. The MSPD/MSAPD can be operated with a reverse bias applied between the anode and cathode. Optical signals can impinge from the top surface and in some cases from the bottom surface.

30 **[00570]** Depending on the material, wavelength ranges can range from 800-1550 nm or longer, in some cases from 800 nm to 950 nm, in some cases from 800 nm to 1100 nm, in some cases from 1250 nm to 1350 nm, in some cases from 1250 nm to 1600 nm and in some cases 800 nm to 880 nm.

[00571] QE can range from 30% to 70% or higher at at least one wavelength in the wavelength span. The QE of MSPD and/or MSAPD can be higher than a comparable photodiode and/or avalanche photodiode without microstructure. Data rate bandwidth can range from 1 Gb/s to 100 Gb/s, in some cases 25 Gb/s to 50 Gb/s, and in some cases 50 Gb/s or higher.

[00572] In some cases the P Si layer 10106 can be 0.2-0.3 microns thick with doping with boron to concentration greater than 1×10^{20} ions/cm³. The I layer 10102 can have a thickness ranging from 1.0 to 2.0 microns with background doping concentration of less than 1.5×10^{15} ions/cm³. The N layer 10104 can have a thickness ranging from 0.2-0.3 microns with doping concentration of arsenic greater than 1×10^{19} ions/cm³. An N device layer (not shown) can exist between 10104 and 10108 having a thickness ranging from 0.1 to 0.25 microns. BOX (buried oxide) 10108 can have thickness ranging from 1 to 4 microns on silicon handle wafer 10100. In some cases, the BOX 10108 beneath the microstructure holes can be partially and/or fully etched away, and in some cases the BOX remain un-etched. The structures shown in Fig. 101 and other Si, GeSi and silicon based MSPDs/MSAPDs can all be monolithically integrated with CMOS and/or BiCMOS silicon electronics such as TIAs, CDRs, LAs, and/or equalizers. In some cases with heteroepitaxy, III-V MSPDs and/or III-V MSAPDs on silicon based material and substrates can also be monolithically integrated with CMOS/BiCMOS ASICs in silicon. Applications include optical communications, optical data communications, LIDAR, imaging, single photon detections, sensing, and biometrics. In some cases for LIDAR applications, the MSAPDs described in the present disclosure can be tailored for the LIDAR wavelengths, responsivity or QE, data rate bandwidth and avalanche voltage. In particular, the I or low doped region for photon absorption and trapping can have a thickness ranging from 2 to 10 microns or more and the photosensitive area can have a lateral dimension ranging from 50 to 5000 microns or more. Arrays of the MSAPDs can be monolithically integrated with CMOS/BiCMOS ASICs suitable for specific LIDAR applications such as automotive sensors and/or robotic sensors. Wavelengths can be tailored and optimized with the addition of GeSi with Ge fraction ranging from 0 to 1 to address wavelengths from 700 nm to 2000 nm. Low avalanche voltages can be achieved with the addition of microstructure holes to reach desired QE and responsivity with reduced

overall thickness of the APD structure for higher reliability in hostile environments. The microstructure holes and the MSAPD can be fully passivated for low dark current. Avalanche gain can take place in an Si I layer for reduced noise characteristics.

5 **[00573]** In some cases the wavelength used for LIDAR applications is 903 nm and in some cases the wavelength range is 800-950 nm. For these wavelengths a GeSi alloy I or low doped absorption layer with photon trapping microstructure holes can be used in an MSAPD. The microstructure holes can be used to improve the QE and/or responsivity over a comparable APD without microstructure
10 holes. The detection range can be extended from 100 meters to 250 meters in some cases. In some cases, the avalanche voltage can be reduced due to reduced layer thickness in a MSAPD as compared to a comparable APD without microstructure holes.

[00574] FIG. 102 is a plot showing an FDTD simulation of the optical field
15 absorption enhancement verses wavelength for a MSPD structure with PIPN, PP-N, PN-N, or PIPIN structure for a MSAPD device, according to some embodiments. The wavelength range is (800-980 nm). The device has microstructure holes in silicon with an I or low doped layer thickness of 5 micrometers (curve 10212) cladded by 0.2 and 0.4 microns of P and N layers on a BOX layer (SOI wafer) for a
20 MSPD structure and with either a PIPN or PIPIN structure for a MSAPD device. The hole diameter is 700 nm and the hole period is 1000 nm in a square lattice and the holes are cylindrical, etched to a depth of 1000 nm for this simulation. Enhanced absorption at some wavelengths in the range 800-980 nm, can be 80% or higher and at some wavelengths the enhanced absorption can be 60% or
25 higher. A comparable silicon photodetector absorption verses wavelength without microstructure holes with 10 micrometers of I or low doped layer and without a BOX layer, is shown in the dashed curve 10214. For a silicon photodetector to reach 80% absorption at some wavelengths in the range of about 800-980 nm, an I or low doped layer of thickness of approximately 30 microns may be necessary.
30 Such thick I layer would require a reverse bias voltage of 100 to 200 volts for APD operation. Even for photodiode operation, a high reverse bias voltage of 20 volts or higher may be necessary to achieve good quantum efficiency. Absorption can be directly proportional to quantum efficiency and in some cases can be the quantum

efficiency if recombination and scattering are negligible. With the addition of micro and or nano structure holes, a thinner I or low doped layer or region can be used to achieve a quantum efficiency that is approximately equivalent to a thicker micro/nanostructure hole-free I or low doped layer. Reverse bias voltages of

5 MSPDs can be less than 20 volts and for MSAPD less than 100 volts. In some cases the reverse bias voltages for MSPDs can be less than 10V and for MSAPDs less than 50V. In some cases the reverse bias voltages for MSAPDs can be less than 35V. In some cases, for single photon MSAPD devices where the MSAPD can be operated at the Geiger-counter mode or beyond the breakdown voltages, the
10 reverse bias voltage can be less than 25V, in some cases less than 15V, and in some cases less than 10V. The I or low doped layer or region for a single photon MSAPD detector can range from 0.3 to 5 microns for example. In some cases the I layer or region for MSAPDs and or MSPDs can range from 0.5 to 6 microns.

[00575] The thinner I layer or region of MSPDs, MSAPDs can be more
15 conducive for monolithic integration with CMOS/BiCMOS electronics and the lower reverse bias voltages can result in high device reliability.

[00576] For LIDAR and or LiFi applications the data rate can range from hundreds of Mb/s to tens of Gb/s. Monolithic integration with CMOS/BiCMOS ASICs of arrays of MSPDs can be suitable for such applications. MSAPDs and
20 MSAPD-single photon detectors can be implemented with significant cost reduction and improvement in performance due to low parasitics.

[00577] In some cases, wavelengths used for LIDAR can range from 780-980 nm, and in some cases from 800 nm to 2000 nm. MSPDs/MSAPDs can cover these wavelengths with Si and or GeSi I or low doped regions with microstructured
25 holes for photon trapping and enhanced absorption. Microstructure holes can be etched or formed in Si and or GeSi photodiodes, Si and or GeSi avalanche photodiodes, Si and/or GeSi single photon avalanche photodiodes, Si and/or GeSi photomultipliers for example. See, e.g., Hamamatsu data sheet for Si photodetectors for LIDAR,
30 https://www.hamamatsu.com/resources/pdf/ssd/Photodetector_lidar_kapd0005e.pdf, incorporated herein by reference.

[00578] In some cases, a thermal anneal and/or passivation can be performed after the etching and/or formation of the microstructure holes and structures and/or

any mesas and/or any trenches to remove any damage due to etching. In some cases, the lateral dimension of the photodetector for LIDAR can range from 30 microns to 3000 microns or more. In some cases an array of photodetectors can be made such as an array of Si and or GeSi I layer SPAD (Single photon avalanche photodiode) that can be fabricated for high sensitivity imaging. The use of microstructure holes can further improve the sensitivity and extend the wavelength of the Si and or GeSi photodetector as compared to a comparable photodetector without microstructures holes or microstructures for photon trapping to enhance the absorption and therefore the QE. QE of photodetectors with microstructure holes for absorption enhancement can be formed in the superstrate, in the first doped layer, into the low doped or I layer or region and/or in the second doped region. QE can thereby be enhancement by a factor of 1.5 or more at certain wavelengths in the range 800 to 1000 nm for silicon, 900 nm to 1400 nm for GeSi, and 1000 nm to 2000 nm for Ge. In some cases the QE enhancement factor can be 2 or more times at certain wavelengths and in some cases the enhancement factor can be 10 times or more at certain wavelengths.

[00579] FIG. 103 is a cross section of a MSPD or MSAPD having Ge and/or GeSi (with Ge fraction ranging from greater than 0 to 1 where 1 is all Ge, and in some cases from 0 to 1 where 0 is all silicon) layers grown on Si that is monolithically integrated with CMOS/BiCMOS ASICs, according to some embodiments. The ASICs can be configured for various applications such as high speed optical data communications using optical fibers, free space optical communications such as LIFI, light direction and ranging (LIDAR), and imaging. The layers/regions can be grown on SOI or bulk silicon substrates. Shown in FIG. 103, a BOX layer 10308 is used to provide higher refraction index contrast to confine the photon trapped light. As discussed earlier, the BOX layer 10308 can be partially and/or entirely removed beneath the photodetector to provide a higher refractive index contrast which can further improve the QE.

[00580] The N+ Si layer 10304 adjacent to the BOX layer 10308 can have a resistivity of 0.02 ohm-cm or less with thickness ranging from 100 nm to 1000 nm approximately. Si P layer 10303 can have resistivity of 1 ohm-cm or less with thickness ranging from 50 nm to 500 nm. Ge and/or GeSi alloy I and or low doped layer/region 10302 can have resistivity of 0.2 ohm-cm or greater with thickness

ranging from 100 nm to 5000 nm. Ge and/or GeSi P+ layer 10306 can have resistivity of 0.05 ohm-cm or less with thickness ranging from 50 nm to 1000 nm. In some cases a thin metal or transparent conducting metal oxide such as indium tin oxide (ITO) of thickness ranging from 5 nm to 1000 nm can be added to the top

5 layer to reduce the series resistances.

[00581] In some cases, the Ge and/or GeSi layers 10302 and/or 10306 can be grown by selective area growth where dielectric layers such as silicon oxide, nitride for example, 10364 can be used to cover areas on the silicon to prevent crystalline or mostly crystalline Ge or GeSi growth. An array of dielectric pattern of
10 rectangular, polygonal, circular, oval and/or any other shapes can be deposited or otherwise formed on the Si 10303 such that during selective area growth of Ge/GeSi, those areas with dielectric will be void and or mostly void of high quality Ge/GeSi such as crystalline or mostly crystalline. These voids can be called microstructure holes. The dielectric thin film pattern can be periodic and/or
15 aperiodic with nearest edge to edge spacing ranging from 50 nm to 3000 nm and with lateral dimensions ranging from 100 nm to 3500 nm or more.

[00582] The microstructure holes 10312 formed using selective area growth are shown as holes "C" in FIG. 103. The sidewalls of the holes "C" may not be vertical as shown but may have slope depending on the thickness of the Ge/GeSi and
20 growth conditions and crystal orientations. The C microstructure holes can be further etched to improve MSPD/MSAPD performances if necessary. In some cases, additional holes can be etched into the Ge/GeSi layers after selective area growth as shown in holes "A" and "B" where holes "A" can be an inverted pyramid and "B" can be cylindrical and or funnel or cone and/or any combination of shapes
25 using dry and/or wet etch. The microstructure holes can be etched to depths into the first doped layer (P+) 10306 and/or into the I or low doped Ge/GeSi layer/region 10302. As discussed elsewhere herein, thermal annealing and/or passivation can be used to reduce leakage current due to etching damages and/or exposed surfaces. The wavelength range of operation can be from 800 nm to 1650
30 nm or longer depending on the composition of GeSi alloy and/or Ge and whether the layers are strained or relaxed. Data rates can range from less than 1 Gb/s to 50 Gb/s or higher depending on photodetector layer structure and diameter.

[00583] In the case of MSAPDs, a reverse bias voltage ranging from -5 to -35 volts can be applied to the anode 10320 and cathode 10322 (shown formed in a mesa/trench etch 10360) and can operate in either the avalanche mode and/or the persistent avalanche mode. In the case of MSPDs, the Si P 10303 layer may not
5 be necessary and a reverse bias voltage of -2 to -10 volts can be applied to the anode 10320 and cathode 10322. In some cases, selective area growth may not be necessary and microstructure holes A and B can be etched into the first doped layer and or into the I or low doped region. The photodetectors with microstructure holes for photon trapping can have a QE (or external QE, EQE) greater than a
10 comparable photodetector without microstructure holes for photon trapping for certain wavelengths.

[00584] According to some embodiments, the temperature range of operation for the MSPDs described herein can range from -40 to 95 degrees centigrade, in some cases from -5 to 95 degrees, and in some cases from -40 to 100 degrees C.

15 **[00585]** According to some embodiments, the thickness of the BOX layer for MSPDs/MSAPDs described herein can range from 5 nm to 5000 nm or more and in some cases from 20 nm to 5000 nm or more. In some cases the BOX layer or region can be ion implanted.

[00586] According to some embodiments, the pitch between MSPDs/AMSPDs in
20 an array can range from 100 to 4000 micrometers.

[00587] According to some embodiments, high data rate bandwidth of the integrated chip comprising MSPD/AMSPD and CMOS and or BiCMOS ASICs with clean open eye diagrams can result in bit error rates (BER) of 1E-3 to 1E-12 or better for certain data rates in the range of less than 1 Gb/s to 25 Gb/s or higher, in
25 some cases for data rates of 50 Gb/s or higher, and in some cases for data rates of 100 Gb/s or higher. BER also depends on the bit pattern, and any error correcting algorithms and or forward error corrections.

[00588] Although the foregoing has been described in some detail for purposes of clarity, it will be apparent that certain changes and modifications may be made
30 without departing from the principles thereof. It should be noted that there are many alternative ways of implementing both the processes and apparatuses described herein. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the body of work described herein is not to be

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limited to the details given herein, which may be modified within the scope and equivalents of the appended claims.

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