UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG AUSTIN SEMICONDUCTOR LLC,

Petitioner,

v.

W&WSENS DEVICES INC.,

Patent Owner.

Case IPR2025-00996
Patent No. 10,446,700

PETITION FOR *INTER PARTES* REVIEW

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2. Independent Claim 1 14

a. [1pre(a)]: "A single-chip device comprising an integrated combination of a microstructure-enhanced photodetector (MSPD) configured for reverse-bias operation and an active electronic circuit," 14

b. [1pre(b)]: "both formed on or in a single substrate" 23

c. [1pre(c)]: "and configured to receive an optical input that in cross-section is substantially continuous, convert the optical input to an electrical output, and process the electrical output into a processed output, wherein:" 26

d. [1a]: "the MSPD on or in said single substrate comprises an intermediate layer, a first layer at one side of the intermediate layer, and a second layer at an opposite side of the intermediate layer, wherein:".....34

e. [1b]: "each of the layers comprises Silicon, Germanium, or an alloy thereof;".....35

f. [1c]: "at least one of said layers, or an overlying covering layer that may be present, has holes intentionally formed therein, extending in directions transverse to the layers;".....36

g. [1d]: "each of the first and second layers comprises a doped material;".....39

h. [1e]: "the intermediate layer comprises a material that is less doped than at least one of the first and second layers or is undoped, wherein the degree of doping is the same or different for different positions in the intermediate layer;".....40

i. [1f]: "an input portion configured to concurrently receive at a plurality of said holes said optical input that has said substantially continuous cross-section; and" 42

j. [1g]: "an output portion configured to provide said electrical output from the MSPD;".....45

k. [1h]: "the MSPD includes reverse-bias electrodes coupled therewith to establish an electrical field therein when energized to thereby sweep in a

selected direction electrical charges generated in the MSPD by said optical input;” 47

l. [1i]: “said reverse-bias electrodes being free of a pattern of openings that matches said holes; and” 51

m. [1j]: “the active electronic circuit on or in said single substrate is configured to process the electrical output from the MSPD by applying thereto:” 52

n. [1k]: “amplification to form said processed output from the single-chip device;” 54

o. [1l]: “processing other than or in addition to amplification to form said processed output from the single-chip device; and” 57

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4. Claim 3 67

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9. Claim 11 76

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a. [12]: “The single-chip device of claim 1, in which each of said first and second layers and said intermediate layer has a thickness and at least some of said holes extend through the entire thickness of said intermediate layer and of one of said first layer and second layer and through at least a part of the thickness of the other one of said first and second layers.” 76

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a. [16]: "The single-chip device of claim 1, in which at least some of said holes have sidewalls that slope in planes transverse to said layers." 79

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a. [20]: "The single-chip device of claim 1, in which the holes are at least partly filled with a dielectric material." 84

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a. [24]: "The single-chip device of claim 1, in which said MSPD further comprises ohmic contacts configured for reverse-biasing the MSPD." 88

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17. Claim 26 95

a. [26a]: "The single-chip device of claim 1, further comprising a light guide to said MSPD for directing said optical input thereto," 95

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a. [28a]: "The single-chip device of claim 1, further comprising one or more additional MSPD on or in the same substrate,"....99

b. [28b]: "and respective different optical bandpass filters coupled with at least two of the MSPDs on or in said single substrate, whereby at least two of said MSPDs are configured to respond to different wavelength ranges that are within said optical input."....102

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a. [29]: "The single-chip device of claim 1, further comprising one or more additional MSPDs on or in said single substrate, one or more additional active electronic circuits on or in the said single substrate, and one or more additional communication channels configured to supply electrical outputs from the MSPDs to the one or more of the active electronic circuits."....104

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PETITIONER'S EXHIBIT LIST

Exhibit	Description
Ex-1001	U.S. Patent No. 10,446,700 B2 to Wang et al. ("'700 Patent")
Ex-1002	Declaration of Dr. Michael Lebby, Ph.D. ("Lebby")
Ex-1003	Prosecution History of the '700 Patent (downloaded from Public PAIR)
Ex-1004	U.S. Patent Application Publication No. 2012/0049044 A1 to Kuboi ("*Kuboi*")
Ex-1005	U.S. Patent Application Publication No. 2012/0033119 A1 to Shinohara ("*Shinohara*")
Ex-1006	European Patent Application EP 2 172 974 A1 to NXP B.V. ("*NXP*")
Ex-1007	U.S. Patent Application Publication No. 2008/0259981 A1 to Wang et al. ("*Wang*")
Ex-1008	U.S. Patent Application Publication No. 2009/0133741 A1 to Higuchi et al. ("*Higuchi*")
Ex-1009	Tapan K. Gupta, *Copper Interconnect Technology*, (Springer Science+Business Media, LLC 2009), pp. 67-71.
Ex-1010	Zhihong Huang et al., *Microstructured silicon photodetector*, Applied Physics Letters, Vol. 89 (2006), pp. 033506-1 to -3.
Ex-1011	Richard A. Myers et al., *Enhancing near-infrared avalanche photodiode performance by femtosecond laser microstructuring*, Applied Optics, Vol. 45, No. 35 (Dec. 2006), pp. 8825-31.
Ex-1012	Abbas El Gamal et al., *CMOS Image Sensors*, IEEE Circuits & Devices Magazine (2005), pp. 6-20.
Ex-1013	Eric R. Fossum, *CMOS Image Sensors: Electronic Camera-On-A-Chip*, IEEE Transactions on Electron Devices, Vol. 44, No. 10 (Oct. 1997), pp. 1689-98.
Ex-1014	Sunetra Mendis et al., *CMOS Active Pixel Image Sensor*, IEEE Transactions on Electron Devices, Vol. 41, No. 3 (Mar. 1994), pp. 452-53.

Exhibit	Description
Ex-1015	Renato Turchetta et al., *Introduction to CMOS Image Sensors*, Molecular Expressions™ Optical Microscopy Primer: Digital Imaging in Optical Microscopy - Introduction to CMOS Image Sensors (July 16, 2004), pp. 1-9, *available at* https://web.archive.org/web/20120508153832/https://micro.magnet.fsu.edu/primer/digitalimaging/cmosimagesensors.html
Ex-1016	Ming-Dou Ker et al., *Investigation on Device Characteristics of MOSFET Transistor Placed Under Bond Pad for High-Pin-Count SOC Applications*, IEEE Transactions on Components and Packaging Technologies, Vol. 27, No. 3 (Sept. 2004), pp. 452-60.
Ex-1017	Paul Horowitz et al., *The Art of Electronics* (Cambridge University Press, New York 3d ed. 2016), pp. 1, 11, 52, 71.
Ex-1018	*Electrical Engineering Dictionary* - CRC*netBase* (Phillip A. Laplante editor-in-chief, CRC Press LLC 2000), pp. 1-6.
Ex-1019	S.M. Sze et al., *Semiconductor Devices Physics and Technology*, (John Wiley & Sons, Inc. 3d ed. 2012), pp. 205-10, 325-26, 392-400, 416-417, 466-67.
Ex-1020	John P. Uyemura, *CMOS Logic Circuit Design* (Kluwer Academic Publishers 2002), pp. 64, 74-102, 315-17, 458-60.
Ex-1021	Khalil Jumah Tawfiq Hamam, Organic Solar Cells Based on High Dielectric Constant Materials: An Approach to Increase Efficiency (June 2013) (Ph.D. dissertation, Western Michigan University), pp. 1-122.
Ex-1022	P. Kalugasalam et al., *Dielectric and AC Conduction Studies of Lead Phthalocyanine Thin Film*, Chalcogenide Letters, Vol. 6, No. 9 (Sept. 2009), pp. 469-76.
Ex-1023	Gopal G. Pethuraja et al., *Current-Voltage Characteristics of ITO/p-Si and ITO/n-Si Contact Interfaces*, Advances in Materials Physics and Chemistry, Vol. 2 (2012), pp. 59-62.
Ex-1024	Giampiero de Cesare et al., *Electrical Properties of ITO/Crystalline-Silicon Contact at Different Deposition Temperatures*, IEEE Electron Device Letters, Vol. 33, No. 3 (Mar. 2012), pp. 327-29.

Exhibit	Description
Ex-1025	Wen-Jang Jiang et al., *The effect of indium tin oxide as an ohmic contact for the 850 nm GaAs oxide-confined VCSELs*, Solid-State Electronics, Vol. 46 (2002), pp. 1945-48.
Ex-1026	*IEEE 100 - The Authoritative Dictionary of IEEE Standards Terms*, IEEE (7th ed. 2000), pp. 333, 1205.
Ex-1027	Christian C. Fesenmaier et al., *Optical confinement methods for continued scaling of CMOS image sensor pixels*, Optics Express, Vol. 16, No. 25 (Dec. 2008), pp. 20457-70.
Ex-1028	Leonard Rubin et al., *Ion Implantation in Silicon Technology*, Industrial Physicist, 9(3), (Jun/July 2003), pp. 12-15.
Ex-1029	Jurgen Michel et al., *Advances in fully CMOS integrated photonic devices*, Proceedings of SPIE, Vol. 6477 (2007), pp. 64770P-1 to -11.
Ex-1030	Mark Beals et al., *Process Flow Innovations for Photonic Device Integration in CMOS*, Proceedings of SPIE, Vol. 6898 (2008), pp. 689804-1 to -14.
Ex-1031	Donald A. Neaman, *Semiconductor Physics and Devices – Basic Principles* (McGraw Hill 3d ed. 2003), pp. 247-50, 260-61.
Ex-1032	Adel S. Sedra et al., *Microelectronic Circuits* (Oxford University Press 7th ed. 2015), pp. 155-56.
Ex-1033	Chung-Wei Chang et al., *High Sensitivity of Dielectric films Structure for Advanced CMOS Image Sensor Technology*, 2007 International Image Sensor Workshop, IEEE Electron Devices Society (2007), pp. 207-10.
Ex-1034	Matthew Sauceda, *Porphyrin Thin Film Dielectrics*, SUNFEST Technical Report TR-CST01NOV04, Center for Sensor Technologies, Univ. of Pennsylvania, Philadelphia, PA (2004), pp. 181-98.
Ex-1035	N. Venkatramaiah et al., *Spectroscopic and dielectric studies of meso-tetrakis(p-sulfonatophenyl) porphyrin doped hybrid borate glasses*, Journal of Alloys and Compounds, Vol. 509 (2011), pp. 2797-803.

Exhibit	Description
Ex-1036	Tom J. Savenije, *Photogeneration and transport of charge carriers in a porphyrin p/n heterojunction*, Physical Review B, Vol. 55, No. 15 (Apr. 1997), pp. 9685-92.
Ex-1037	Ümit Salan et al., *Synthesis, characterization, electrical and dielectric permittivity measurements of 2,9,16,23-tetra(4-ferrocenylimino-3-nitrophenoxy)phthalocyanines*, Journal of Porphyrins and Phthalocyanines, Vol. 10 (2006), pp. 1263-70.
Ex-1038	Teresa M. Figueira-Duarte et al., *Pyrene-Based Materials for Organic Electronics*, Chemical Reviews, Vol. 111 (2011), pp. 7260-314.
Ex-1039	*Handbook of Wafer Bonding* (Peter Ramm et al. eds., Wiley-VCH Verlag & Co. KGaA 2012), pp. 52-54, 63-64, 112-15.
Ex-1040	*W&Wsens Devices Inc. v. Samsung Electronics Co. Ltd. et al.*, Case No. 2:24-cv-00854, Plaintiff's Infringement Contentions, Appendix D-1 (Jan. 7, 2025)
Ex-1041	*W&Wsens Devices Inc. v. Samsung Electronics Co. Ltd. et al.*, Case No. 2:24-cv-00854, Plaintiff's Infringement Contentions, Appendix D-2 (Jan. 7, 2025)

I. Preliminary Statement

Petitioner Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor LLC (collectively, "Samsung") requests *inter partes* review of U.S. Patent No. 10,446,700 (Ex-1001) and cancellation of claims 1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35.

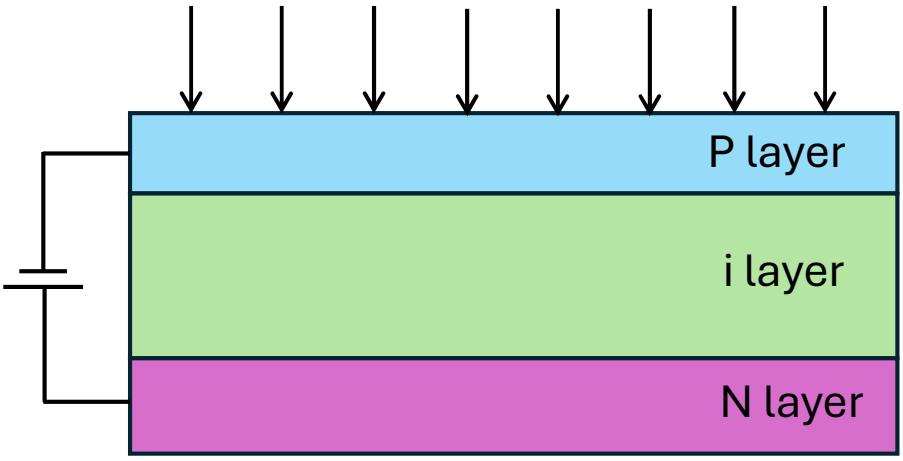
The challenged claims pertain to a single-chip device with a photodetector with CMOS signal processing circuitry on a single substrate. This photodetector, called a microstructure-enhanced photodetector (alternatively, "MSPD") in the '700 Patent, features etched holes to increase light absorption. However, integration of photodetectors (even MSPDs) with CMOS signal processing circuitry on the same substrate was widely known and was a common characteristic of CMOS image sensors well before the alleged invention date. For example, *Kuboi* (Ex-1004), which was not considered by the Examiner, discloses and renders obvious all recited features of the claimed single-chip device.

As detailed below and in the supporting declaration of Dr. Michael Lebby, Ph.D. ("Lebby") (Ex-1002), the challenged claims are unpatentable over *Kuboi*. Lebby, ¶¶1-244. The Board should institute review and cancel all challenged claims.

II. State of the Art

A. Photodetectors

A photodetector is a semiconductor device that transforms photons into electrical signals, enabling electrical circuits to detect and measure incident light. Lebby, ¶51. As illustrated below, a PIN photodetector is a specific type of photodiode characterized by an intrinsic (undoped) layer positioned between highly doped P-type and N-type semiconductor layers (hence the name "PiN"):



Lebby, ¶51. When light enters the photodetector, photons are absorbed in the intrinsic layer, generating electron-hole pairs. Lebby, ¶52. Applying a negative bias across the photodetector causes the separated electrons to move towards the N-type layer and the holes towards the P-type layer, producing a measurable photocurrent. Lebby, ¶52.

B. Microstructure-Enhanced Photodetectors

Conventional silicon photodetectors exhibit high responsivity at wavelengths of light less than about 850 nm. Ex-1010, 1; Lebby, ¶53. The prior art recognized that tailoring the microstructure of silicon can extend the operability of these photodetectors to longer wavelengths, such as infrared. Lebby, ¶53. For instance, etching the surface of a silicon photodetector to create micron-sized pillars/grooves was known to enhance a photodetector's responsiveness at longer wavelengths. Ex-1010, 1-2; Ex-1011, 1-6; Lebby, ¶¶53-56. The images below illustrate photodiodes with laser-etched microstructures designed to enhance their responsiveness at longer wavelengths. Lebby, ¶53.

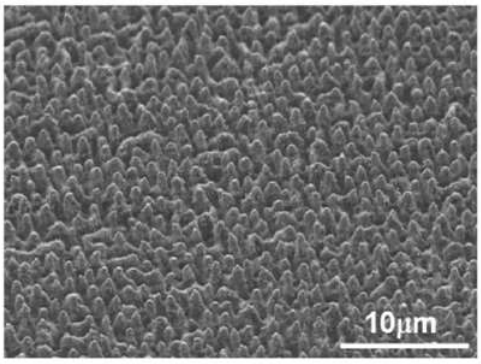


FIG. 1. Scanning electron micrographs of microstructured Si surface.

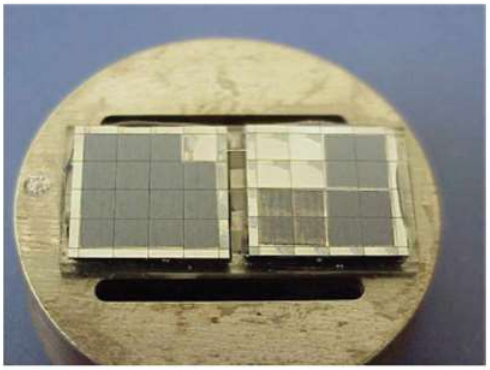


Fig. 1. (Color online) Picture of two microstructured APD arrays prior to packaging. Structuring was performed with an 800 nm fs laser operating at a fluence of 3.5 kJ/m^2 in an atmosphere of SF_6. The array on the right had four different structured regions with a pulse number ranging from 0 to 300. The shiny area is the bare silicon.

Ex-1010, 1 (left); Ex-1011, 2 (right).

Photodetectors featuring microstructures enhanced by etched holes were widely known and utilized well before the purported invention. Lebby, ¶54. For

example, *NXP* (Ex-1006) discloses a single-chip device 1300 where a silicon PIN photodiode is integrated with CMOS signal processing circuitry (not shown in Figure 13 below) on the same substrate 102. *NXP*, ¶¶[15], [32], [42], [85].

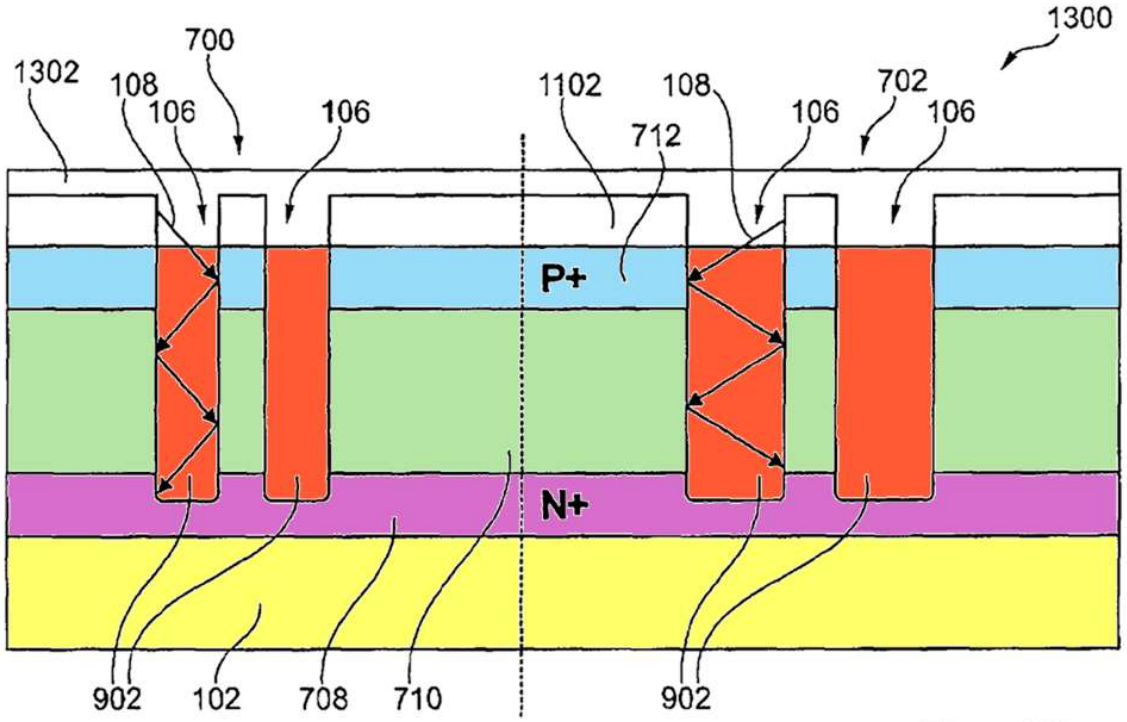


Fig. 13

NXP, Fig. 13.[1] The PiN photodiode above includes an intrinsic layer 710 disposed between an N^+ layer 708 and a P^+ layer 712 and holes or pores 106 formed on the PiN layers by etching. *NXP*, ¶¶[77]-[78]. *NXP* discloses that the presence of pores 106 increases the quantum efficiency of the photodiode. *NXP*, ¶¶[13], [15], [38]; Lebby, ¶55.

[1] All color and colored annotations in figures have been added.

The integration of photodetectors and signal processing circuitry on a single substrate to form a single-chip device was also known long before the purported invention date of the '543 Patent. Lebby, ¶¶57-65; Ex-1012, 1-14; Ex-1013, 1-8; Ex-1014, 1-2; Ex-1015, 1-5; *NXP*, ¶¶[16], [32]-[37].

III. The '700 Patent

A. Specification

The '700 Patent details a single-chip device that integrates photodetectors (referred to as MSPDs and MSAPDs) with CMOS active electronic circuits on a single substrate. '700 Patent, 2:58-61, 4:60-67, 6:17-22; Lebby, ¶66.

The disclosed photodetectors include a silicon substrate with a first layer (a P layer), a very low doped N or P layer called the intermediate layer (or I layer), and a second layer (an N layer) with holes etched in one or more of the PIN layers. '700 Patent, 22:1-33, 16:30-34, 26:33-62. Optical signals impinge on the top and/or bottom surfaces of the photodetectors. '700 Patent, 16:15-19. According to the '700 Patent, because of the holes, light interacts with the absorbing layer(s) for a longer length of time, resulting in enhanced light absorption and a larger external quantum efficiency over a similar structure without holes. '700 Patent, 15:41-49, Abstract; Lebby, ¶67.

Figure 14, reproduced below, illustrates the disclosed photodetector:

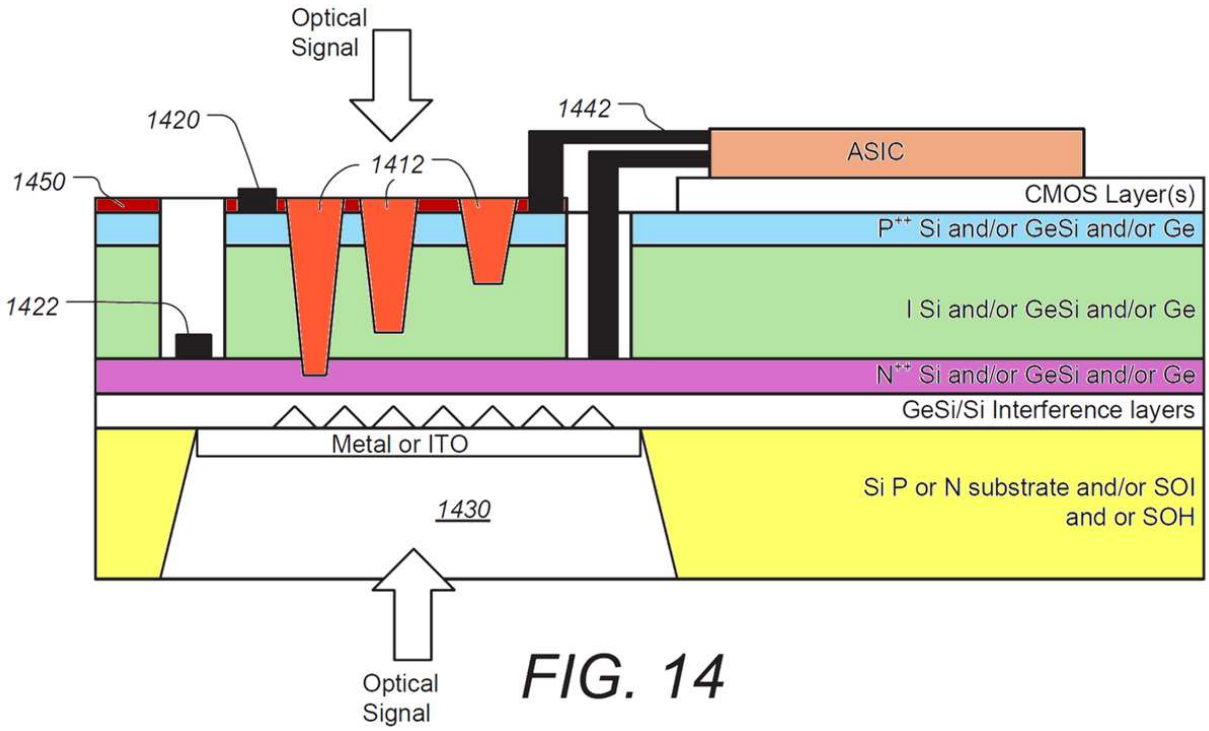


FIG. 14

'700 Patent, Fig. 14, 10:57-59, 26:33-35. The photodetector is monolithically integrated with signal processing circuits (such as ASIC) on the same substrate to form a single-chip device. '700 Patent, 18:61-65, 23:35-38, 26:33-35. Notably, the '700 Patent acknowledges that it was well known to integrate photodetectors with signal processing circuits on a single silicon substrate to reduce cost and improve performance. '700 Patent, 28:50-62, 32:44-61, 47:7-18; Lebby, ¶68.

B. Prosecution History

The Examiner allowed the application that resulted in the '700 Patent, stating that while "the prior art teaches a similar microstructure enhanced photodetector device, [it] fails to disclose the specific characteristic recited in the claims of the instant invention[,] e.g.[,] the single[-]chip device with combination

of photodetector as detailed in communication with active electronic unit which processes the information gathered by the photodetector, in conjunction with the details of the electrodes do not have the pattern of openings." Ex-1003, 124. However, the Examiner did not consider *Kuboi*, which teaches all these features and renders the challenged claims unpatentable. Lebby, ¶69.

C. Claim Construction

The Board construes claims per *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). 37 C.F.R. §42.100(b). Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, no terms need construction to resolve the controversy.[2]

IV. Statement of Precise Relief Requested

A. Prior Art

The application that resulted in the '700 Patent was filed on October 30, 2017, claiming priority to multiple patent applications, the earliest of which was filed on May 22, 2013.[3] Thus, the earliest claimed priority date is May 22, 2013.

[2] Petitioner retains the right to contend in another proceeding that certain limitations are indefinite.

[3] Petitioner retains the right to dispute the claimed priority in another proceeding.

- *Kuboi* (Ex-1004), U.S. Patent Publication No. 2012/0049044, which published on March 1, 2012, is prior art under 35 U.S.C. §102(a)(1) and §102(a)(2).

B. Challenges

Ground	Challenged Claims	Basis	Prior Art
1A	1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35	§ 102	*Kuboi*
1B	1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35	§ 103	*Kuboi*

V. Level of Ordinary Skill in the Art

A person of ordinary skill in the art ("POSITA") would have had at least a master's degree in electrical engineering or a similar field and at least five years of experience working with semiconductor systems and semiconductor devices. Lebby, ¶¶82-84. Additional relevant work experience can compensate for less education and vice versa. Lebby, ¶83.

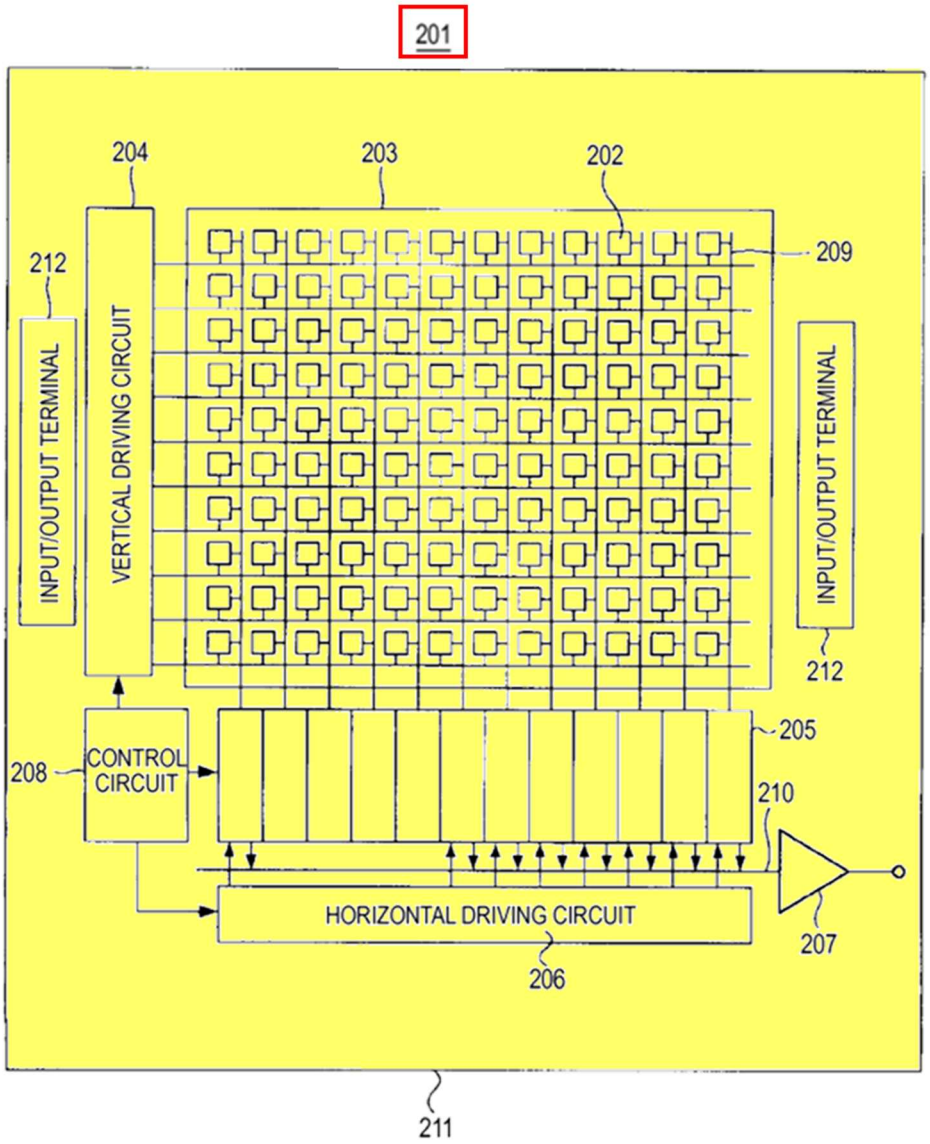
VI. The Challenged Claims Are Unpatentable

A. Grounds 1A/1B: Claims 1-4, 7, 9-12, 16-17, 20-21, 24-26, 28-30, 32, and 35 Are Anticipated by *Kuboi* (Ground 1A) and Obvious over *Kuboi* (Ground 1B)

1. Overview of *Kuboi*

Kuboi discloses a CMOS solid-state imaging device 201 that includes a pixel region 203 and a peripheral circuit portion on a single semiconductor substrate 211. *Kuboi*, ¶[48], Fig. 15.

FIG.15



Kuboi, Fig. 15. Pixel region 203 of substrate 211 comprises a plurality of pixels 202 arranged in a two-dimensional array. *Kuboi*, ¶[48]. Each pixel 202 contains one photoelectric conversion portion (or a photodiode) and four pixel transistors. *Kuboi*, ¶[48]. The peripheral circuit portion includes "logic[] circuits" (such as a vertical driving circuit 204, column signal processing circuits 205, horizontal

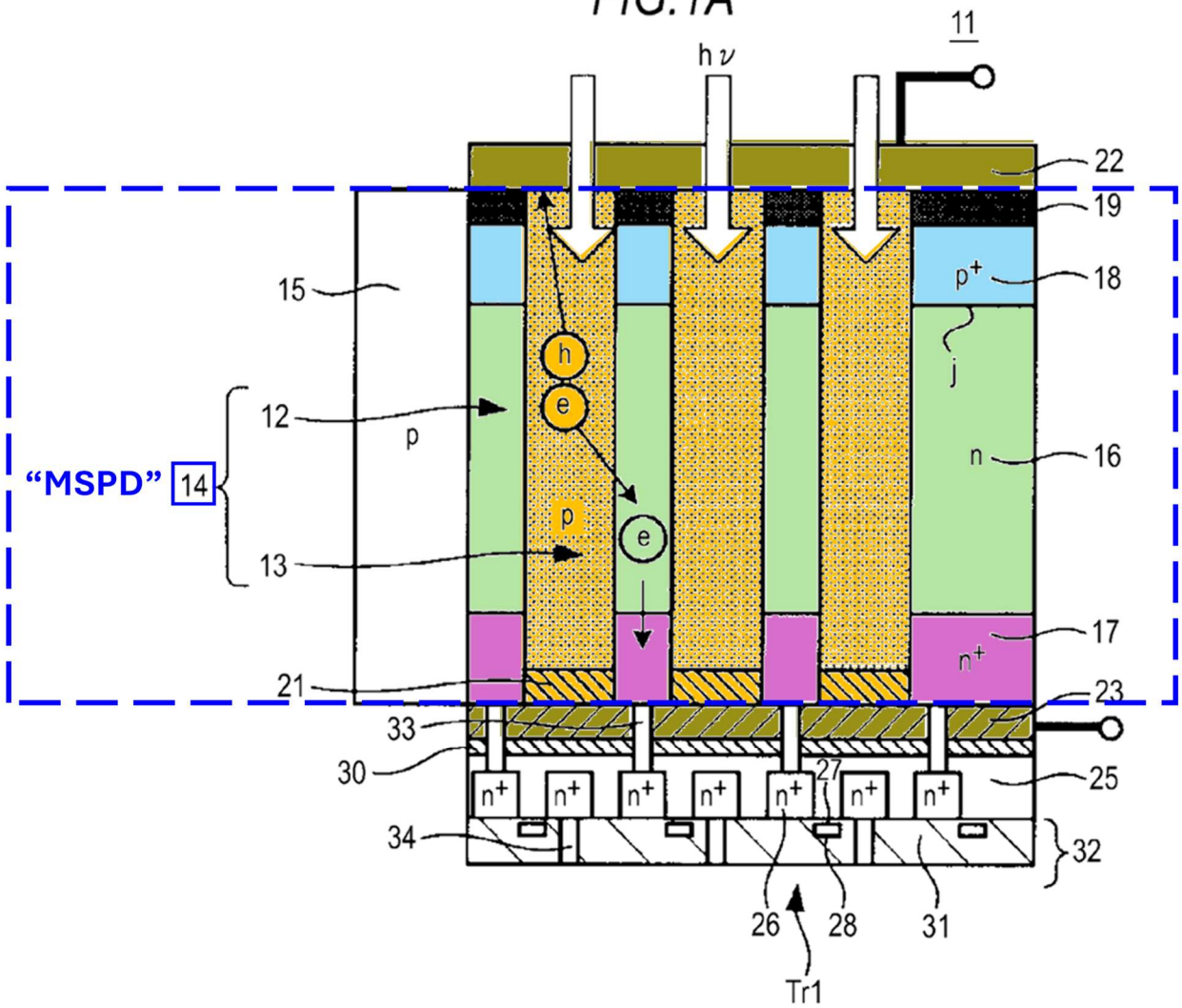
driving circuit 206, output circuit 207, and control circuit 208), which process the electrical output of the pixels and then output it. *Kuboi*, ¶¶[49]-[54]; Lebby, ¶75. The pixels and the peripheral circuit portion are fabricated on a single substrate, and the pixel transistors are fabricated on another substrate and the two substrates are bonded together. *Kuboi*, ¶¶[62], [70], [78]; Lebby, ¶75.

Kuboi describes photoelectric conversion portions suitable for use in imaging device 201. *Kuboi*, ¶[48]; Lebby, ¶76. For example, *Kuboi* discloses a basic pixel configuration with reference to Figures 1A/1B. *Kuboi*, ¶[55]. *Kuboi* likewise discloses a pixel configuration in Figures 6A/6B, explaining that the disclosed red and green pixels 53R and 53G have a structure that is the same as the basic configuration of Figures 1A/1B. *Kuboi*, ¶¶[90], [95], [69]. *Kuboi* also discloses that Figure 13 includes pixels 53R, 53G, and 53B, having configurations that are the same as the pixels of Figures 1A/1B. *Kuboi*, ¶[181]. Similarly, *Kuboi* describes Figure 15 as applicable to all of *Kuboi*'s embodiments. *Kuboi*, ¶¶[35], [48]. Further, *Kuboi*'s Figures 4A-4F show a method of manufacturing the basic pixel configuration of Figures 1A/1B. *Kuboi*, ¶¶[69]-[76]. Thus, Figures 1A/1B, 6A/6B, 13, and 15 all disclose the pixel configuration of the same imaging device, and Figures 4A-4F disclose methods of manufacturing that same pixel configuration. Lebby, ¶76. Accordingly, this Petition relies on *Kuboi*'s Figures

1A/1B, 4A-4F, 6A/6B, 13, and 15, and associated disclosures as representative of the pixel configuration of the same imaging device 201. Lebby, ¶76.

Figure 1A (below) illustrates a photoelectric conversion portion 14 in a pixel 11 that may be used in imaging device 201. *Kuboi*, ¶¶[48], [55]-[56]. *Kuboi* explains that pixel 11, including photoelectric conversion portion 14, can be utilized in imaging device 201. *Kuboi*, ¶¶[48], [55]; Lebby, ¶77.

FIG.1A



Kuboi, Fig. 1A. Photoelectric conversion portion 14 comprises a silicon semiconductor layer 12 that includes multiple embedded organic material layers 13. *Kuboi*, ¶[55]; Lebby, ¶78. Silicon semiconductor layer 12 is implanted with different impurities (or doped) to form an n-type semiconductor (or "intermediate") region 16 with a p^+-type semiconductor region 18 on one side and an n^+-type semiconductor region 17 on the opposite side (i.e., stacked PiN regions). *Kuboi*, ¶¶[56], [71]; Lebby, ¶78. The doping of layer 12 is such that p^+-type region 18 and n^+-type region 17 have a higher concentration of impurities than n-type region 16. *Kuboi*, ¶[56].

After forming regions 18, 16, and 17, vertical holes 38 extending from the p^+-type region 18 to n^+-type region 17 are etched into the PiN regions (below left). *Kuboi*, ¶¶[71]-[72]; Lebby, ¶¶79-80.

FIG.4B

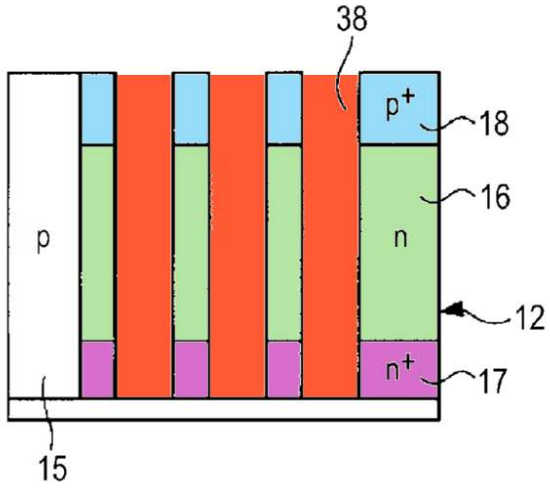
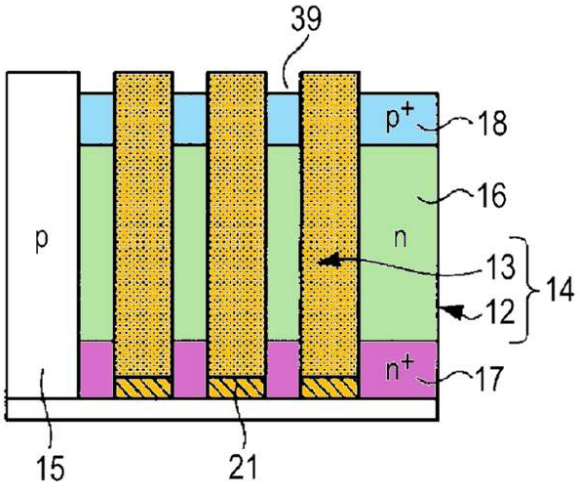


FIG.4E



Kuboi, Figs. 4B, 4E. Then, the organic material that forms photoelectric conversion film 13 is deposited in these holes 38 (above right). *Kuboi*, ¶¶[72]-[73].

A metal light shielding film 19 is then applied to the surface of p^+-type region 18 such that only holes 38 containing films 13 are exposed to incident light (hν), *Kuboi*, ¶¶[59], [76], Figs. 1A, 4F; Lebby, ¶81. An upper electrode 22 and a lower electrode 23 are formed on opposite sides of the PiN regions, and a reverse bias is applied. *Kuboi*, ¶¶[60], [64]. Photoelectric conversion of the incident light (hν) within films 13 (inside holes 38) generates electron-hole pairs that pass through the depleted semiconductor layer 12 into a charge accumulation region 26 of the transfer transistor (Tr1) of the corresponding pixel 11 (via conductors 33). *Kuboi*, ¶¶[62], [64]; Lebby, ¶81. After initial signal processing (e.g., amplification) by the pixel transistors, the electrical signals from pixel 11 are sent to the peripheral circuits for further processing. *Kuboi*, ¶¶[48]-[49], [61]-[62].

2. Independent Claim 1

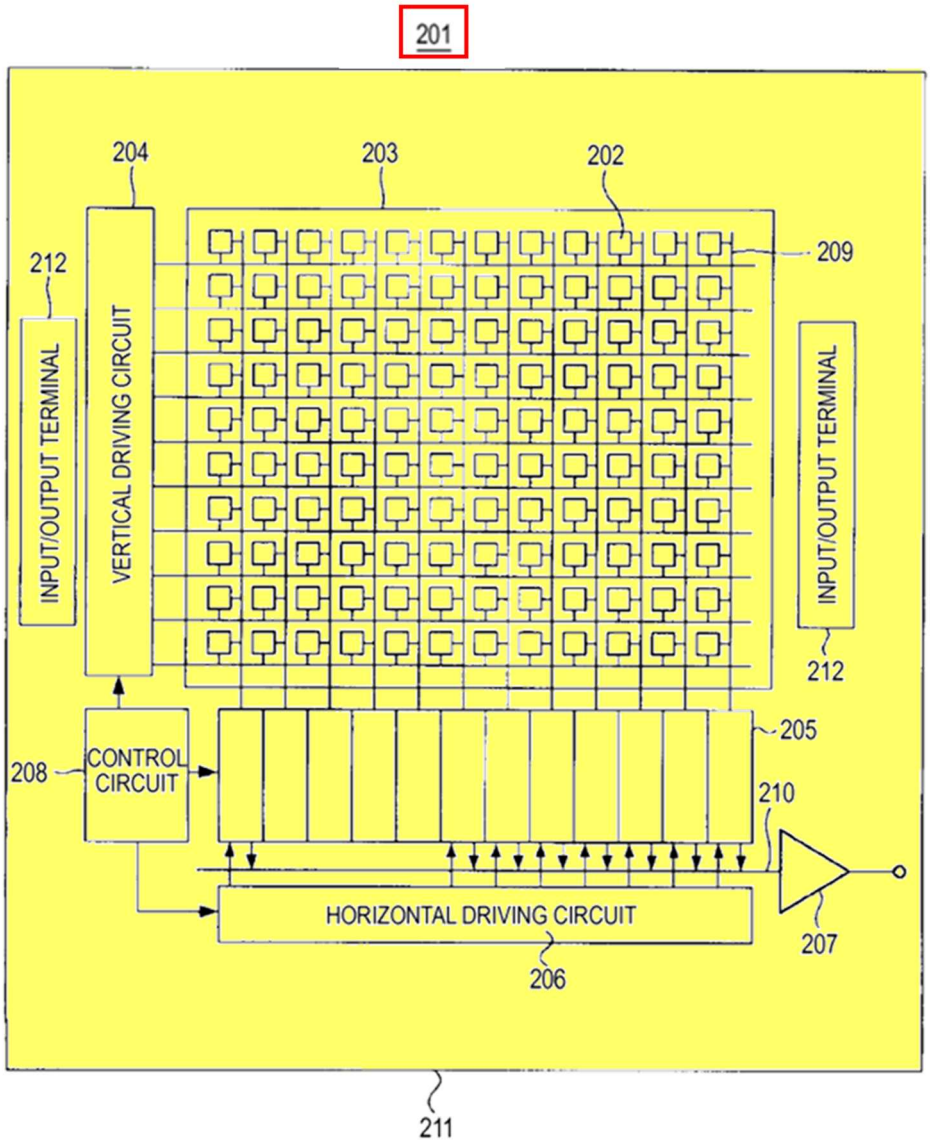
a. [1pre(a)]: "A single-chip device comprising an integrated combination of a microstructure-enhanced photodetector (MSPD) configured for reverse-bias operation and an active electronic circuit,"

To the extent the preamble is limiting, *Kuboi* discloses this portion of it because its CMOS solid-state imaging device ("single-chip device") is a single chip that includes multiple pixels, with hybrid microstructure-enhanced

photoelectric conversion portions ("MSPD") configured for reverse-bias operation, integrated with an active electronic circuit on a single semiconductor substrate 211. *Kuboi*, ¶¶[48], [64], Fig. 15; Lebby, ¶88.

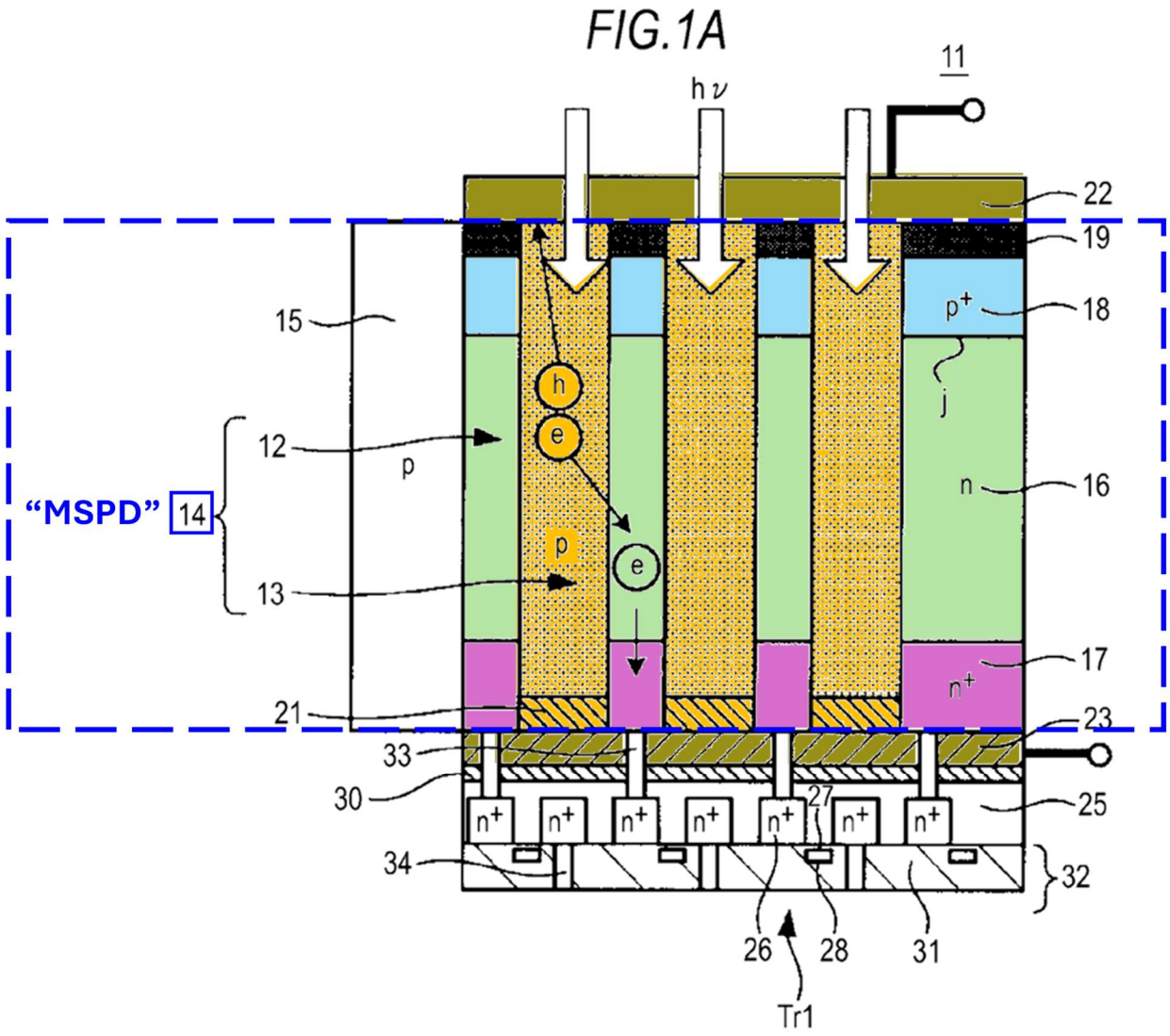
Kuboi discloses the claimed "single-chip device" and "microstructure-enhanced photodetector (MSPD)." Lebby, ¶89. *Kuboi*'s imaging device 201 "include[s] a pixel region (so-called an imaging region) 203 and a peripheral circuit portion which are provided on a semiconductor substrate 211 (e.g., a silicon substrate)." *Kuboi*, ¶[48]. This "single-chip device" is shown below:

FIG.15



Kuboi, Fig. 15. Pixel portion 203 includes a plurality of pixels 202 (elsewhere designated "pixel 11"), each of which includes a microstructure enhanced photodetector in the form of photoelectric conversion portion 14 ("MSPD"), regularly arranged in a two-dimensional array. *Kuboi*, ¶¶[48], [55]; Lebby, ¶90.

Figure 1A, reproduced below, illustrates an exemplary pixel 11, including photoelectric conversion portion 14, that may be used in imaging device 201. *Kuboi*, ¶¶[48], [55]; Lebby, ¶91.



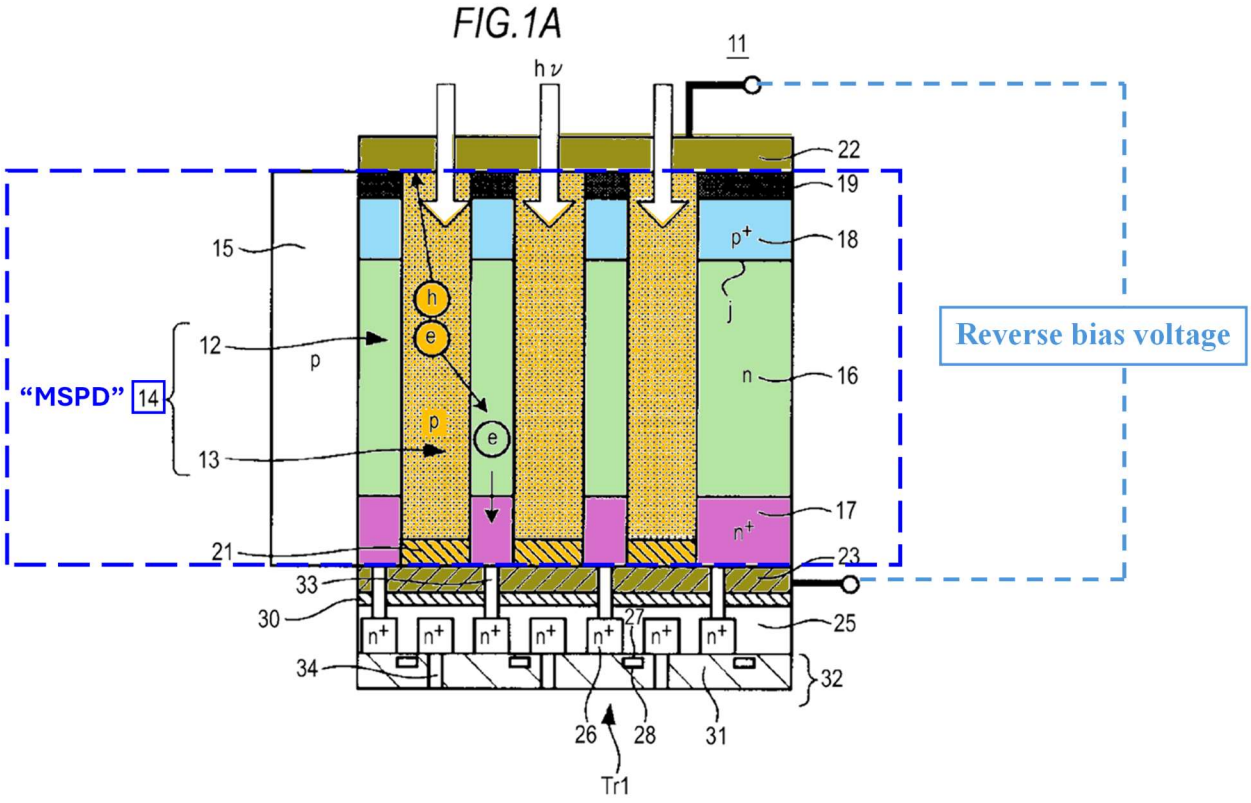
Kuboi, Fig. 1A. Photoelectric conversion portion 14 comprises a semiconductor layer 12 made of silicon and doped with different concentrations of impurities to form a p^+-type region 18 and an n^+-type region 17 on opposite sides of an n-type

region 16 creating a PiN photodiode. *Kuboi*, ¶¶[55]-[56], [71], Fig. 4A; Lebby, ¶92.

Etching vertical holes 38 and embedding photoelectric conversion films 13 in photoelectric conversion portion 14 enhances the microstructure and improves light absorption of the pixel's photoelectric conversion portion. Lebby, ¶93; *Kuboi*, ¶¶[72], [80]-[84], [107]-[108]. Vertical holes 38 extending from p^+-type region 18 to n^+-type region 17 are dry-etched into the semiconductor layer 12, and organic photoelectric conversion films 13 are embedded in holes 38. *Kuboi*, ¶¶[57]-[58], [71]-[75], Figs. 4A-4E. A metal light shielding film 19 is arranged on the surface of p^+-type region 18 such that only the embedded photoelectric conversion films 13 are exposed to incident light (hν). *Kuboi*, ¶¶[57]-[59], [72]-[76]; Lebby, ¶93. Incident light enters photoelectric conversion films 13 and undergoes photoelectric conversion to generate electric charges corresponding to the amount of light received. *Kuboi*, ¶¶[51], [64]. *Kuboi* notes that embedding photoelectric conversion films 13 in holes in the PiN regions increases light absorption compared to photoelectric conversion portions without embedded films 13. *Kuboi*, ¶¶[12], [71]-[75], [80]-[82], [107].

Photoelectric conversion portion 14 is configured for "reverse-bias operation," as claimed. *Kuboi*, ¶¶[64], [87], [149], [171], [186], Fig. 1A; Lebby, ¶¶94-96. As shown below, an upper electrode 22 formed on top of metal film 19 of

photoelectric conversion portion 14 makes electrical contact with p^+-type region 18, and a lower electrode 23 is coupled to—and makes electrical contact with—the surface of n^+-type region 17. *Kuboi*, ¶¶[59]-[60], [77], Fig. 1A; Lebby, ¶94.

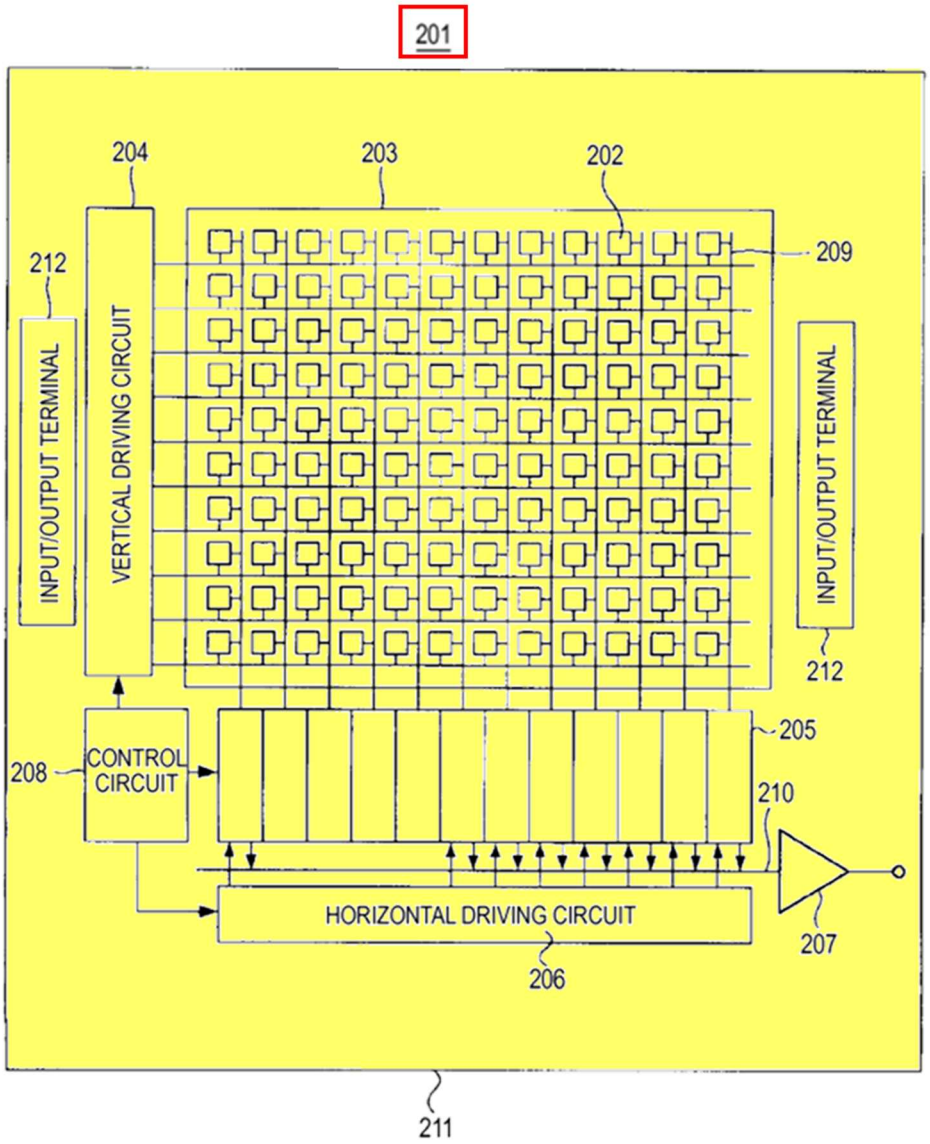


Kuboi, Fig. 1A. A voltage bias is applied between these electrodes, causing upper electrode 22 to have a negative potential and lower electrode 23 to have a positive potential. *Kuboi*, ¶¶[64], [87]. This creates a depletion layer in semiconductor layer 12. *Kuboi*, ¶¶[64], [87]. A POSITA would have understood that applying a voltage bias with a negative potential to p^+-type region 18 and a positive potential to n^+-type region 17 constitutes a reverse bias. Lebby, ¶¶95-96; *see also* Ex-1031, 3-5, 8 (explaining that reverse bias is "[t]he condition in which a positive voltage is

applied to the n region with respect to the p region of a pn junction"); Ex-1032, 3-4.

Kuboi also discloses the claimed "active electronic circuit," which is integrated with photoelectric conversion portion 14. Lebby, ¶¶97-99. Imaging device 201 includes a peripheral circuit portion with "logical circuits" (logic circuits). *Kuboi*, ¶¶[48]-[49], [78], Fig. 15; Lebby, ¶97. The "logic[] circuits" of the peripheral circuit portion include a vertical driving circuit 204, multiple column signal processing circuits 205, a horizontal driving circuit 206, an output circuit 207, and a control circuit 208. *Kuboi*, ¶[49]; Lebby, ¶97. Each can be seen below.

FIG.15

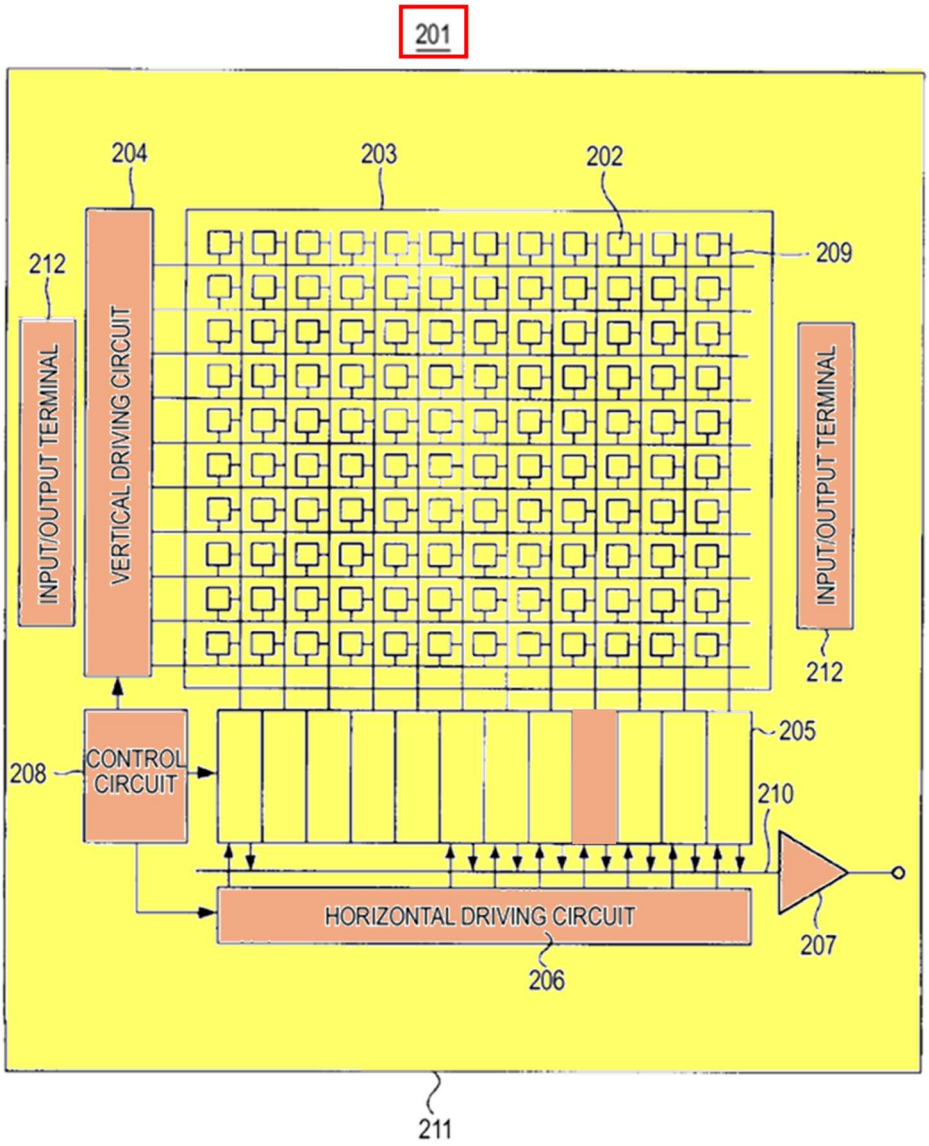


Kuboi, Fig. 15. Vertical driving circuit 204 supplies pulses for activating the pixels in a selected row and channels pixel signals from each pixel to a corresponding column signal processing circuit 205, which performs signal processing tasks such as, e.g., signal amplification. *Kuboi*, ¶¶[51]-[52]. Horizontal driving circuit 206 sequentially selects a column signal processing circuit 205 and routes the

processed pixel signals from that circuit 205 to output circuit 207, which further processes the received signals and outputs the processed signals. *Kuboi*, ¶¶[53]-[54]. Meanwhile, control circuit 208 controls the other circuits of the peripheral circuit portion. *Kuboi*, ¶[50].

Each of these CMOS "logic[] circuits" of the peripheral circuit portion includes active components such as transistors, which activate circuits and amplify signals, thereby making them an active electronic circuit. Lebby, ¶¶99-100; *Kuboi*, ¶[49]; Ex-1019, 4 ("Complementary MOS (CMOS) refers to a complementary *p*-channel and *n*-channel MOSFET pair."); Ex-1017, 6 (describing amplifiers and logic circuits as "active circuits"), 7, 9 (describing transistors as the most important example of an "'active' component[]"), 8 (describing circuits with transistors as "active circuits"); Ex-1019, 4 (describing logic circuits as including transistors); Ex-1018, 4, 5; *see* Ex-1026, 4. Thus, the logic circuits (vertical driving circuit 204, a column signal processing circuit 205, horizontal driving circuit 206, output circuit 207, and control circuit 208) of *Kuboi*'s peripheral circuit portion that process the signals from a pixel (pixel 11) and output it are the claimed active electronic circuit. Lebby, ¶100. The active electronic circuit is highlighted in the figure of imaging device 201 below.

FIG.15



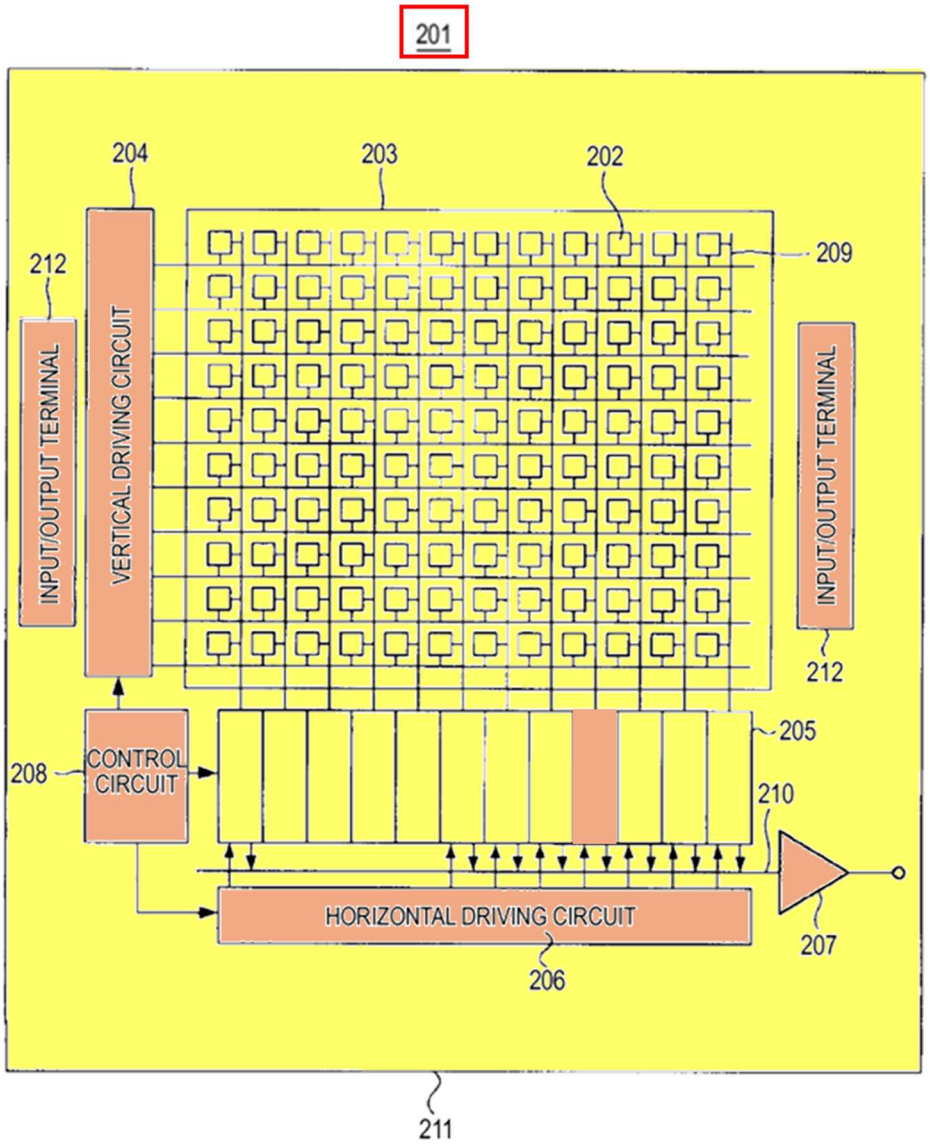
Kuboi, Fig. 15 (identifying an active electronic circuit).

b. [1pre(b)]: "both formed on or in a single substrate"

To the extent the preamble is limiting, *Kuboi* discloses this portion of it because imaging device 201's photoelectric conversion portions 14 and active electronic circuit are both formed on or in a single substrate. Lebby, ¶¶101-103.

In imaging device 201, pixels 11 (including photoelectric conversion portions 14) and the peripheral circuit portion (which includes an active electronic circuit) "are provided on … semiconductor substrate 211." *Kuboi*, ¶¶[48], [78]-[79]; *see Kuboi*, Fig. 15; Lebby, ¶102. As shown below, the pixel region (including pixels 11) and the peripheral circuit portion (including circuits 204-208) "are provided on a semiconductor substrate 211." *Kuboi*, ¶¶[48]-[49].

FIG.15



Kuboi, Fig. 15. Indeed, consistent with the above figure's disclosure of a single substrate, *Kuboi* specifically outlines a method for fabricating the imaging device in which the "pixel and logical circuit portion … [are] created in advance" and bonded to another substrate on which the pixel transistors are formed. *Kuboi*, ¶[78]; Lebby, ¶103. As Dr. Lebby explains, *Kuboi*'s disclosure, including Figure

15 and its method of fabrication, show that the pixels (including microstructure-enhanced photodetectors) and the peripheral circuit portion (which includes the active electronic circuit, VI.A.2.a [**1pre(a)]**) are formed on a single substrate, substrate 211.[4] Lebby, ¶103.

c. [1pre(c)]: "and configured to receive an optical input that in cross-section is substantially continuous, convert the optical input to an electrical output, and process the electrical output into a processed output, wherein:"

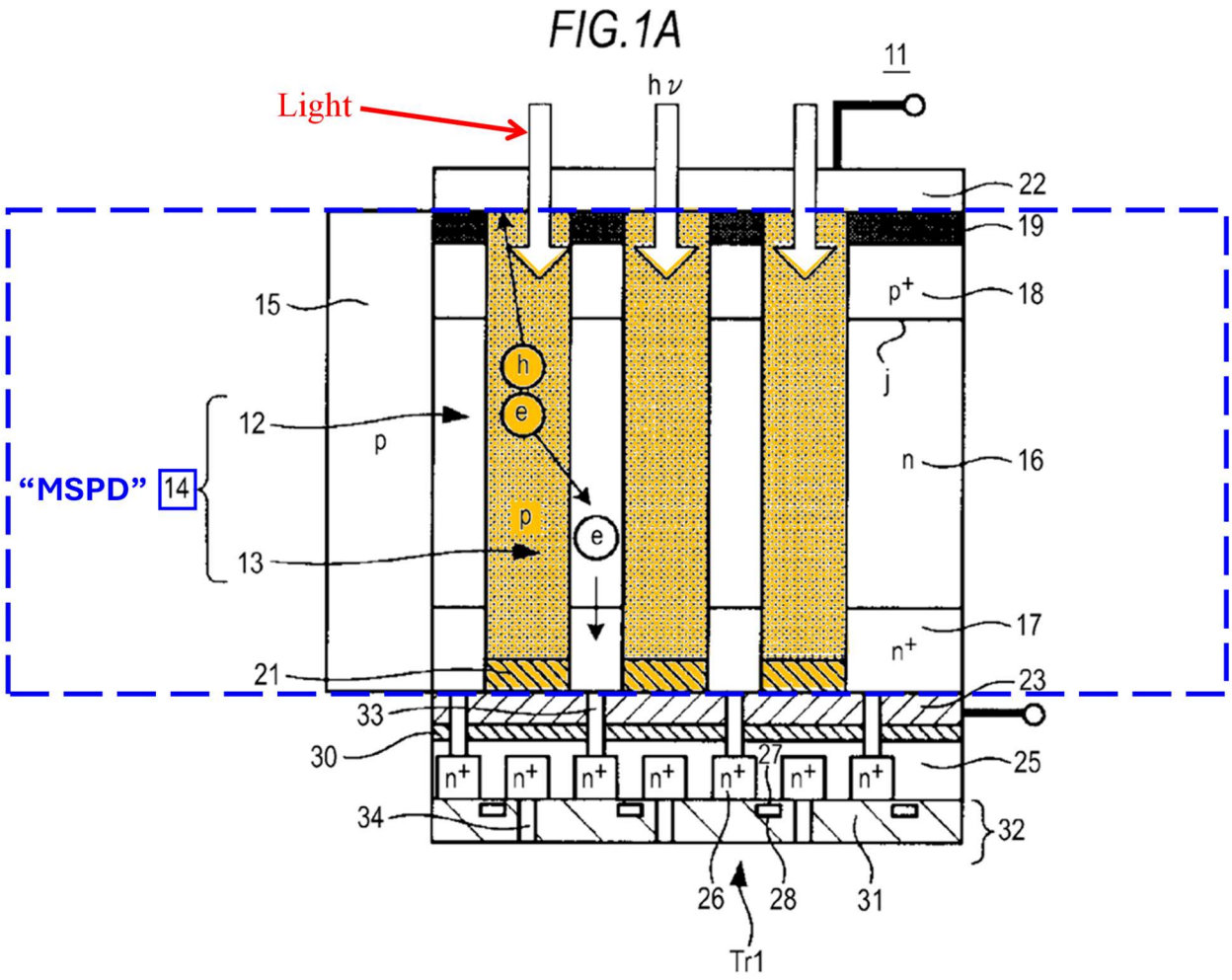
To the extent the preamble is limiting, *Kuboi* discloses and renders obvious this portion of it because imaging device 201 and pixels 11 are configured to receive light (hγ) (the "optical input") that is substantially continuous in cross-section,[5] convert the received light to electrical charges, and process these electrical charges into a processed output. Lebby, ¶¶104-113.

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[4] A drawing teaches all that it reasonably discloses and suggests to a POSITA. *In re Aslanian*, 590 F.2d 911, 914 (CCPA 1979); *see also Current Lighting Sols. LLC v. Jiaxing Super Lighting Elec. Appliance Co.*, IPR2023-00269, Paper 18, 22-26 (PTAB Aug. 16, 2023).

[5] During prosecution, the Examiner indicated that "optical input that in cross-section is substantially continuous" means that the received optical input is substantially continuous in cross-section spatially. Ex-1003, 385; Lebby, ¶105.

Pixel 11 includes an on-chip microlens (not shown in the drawings) formed on transparent upper electrode 22. *Kuboi*, ¶¶[63]-[64]. A color filter is disposed between upper electrode 22 and the on-chip microlens. *Kuboi*, ¶¶[63]-[64], [90], Figs. 6A-6B. As illustrated below, light that passes through the on-chip microlens and the color filter passes through transparent upper electrode 22 and enters photoelectric conversion film 13 of photoelectric conversion portion 14 for photoelectric conversion. *Kuboi*, ¶¶[63]-[64], Fig. 1A; Lebby, ¶106.



Kuboi, Fig. 1A.

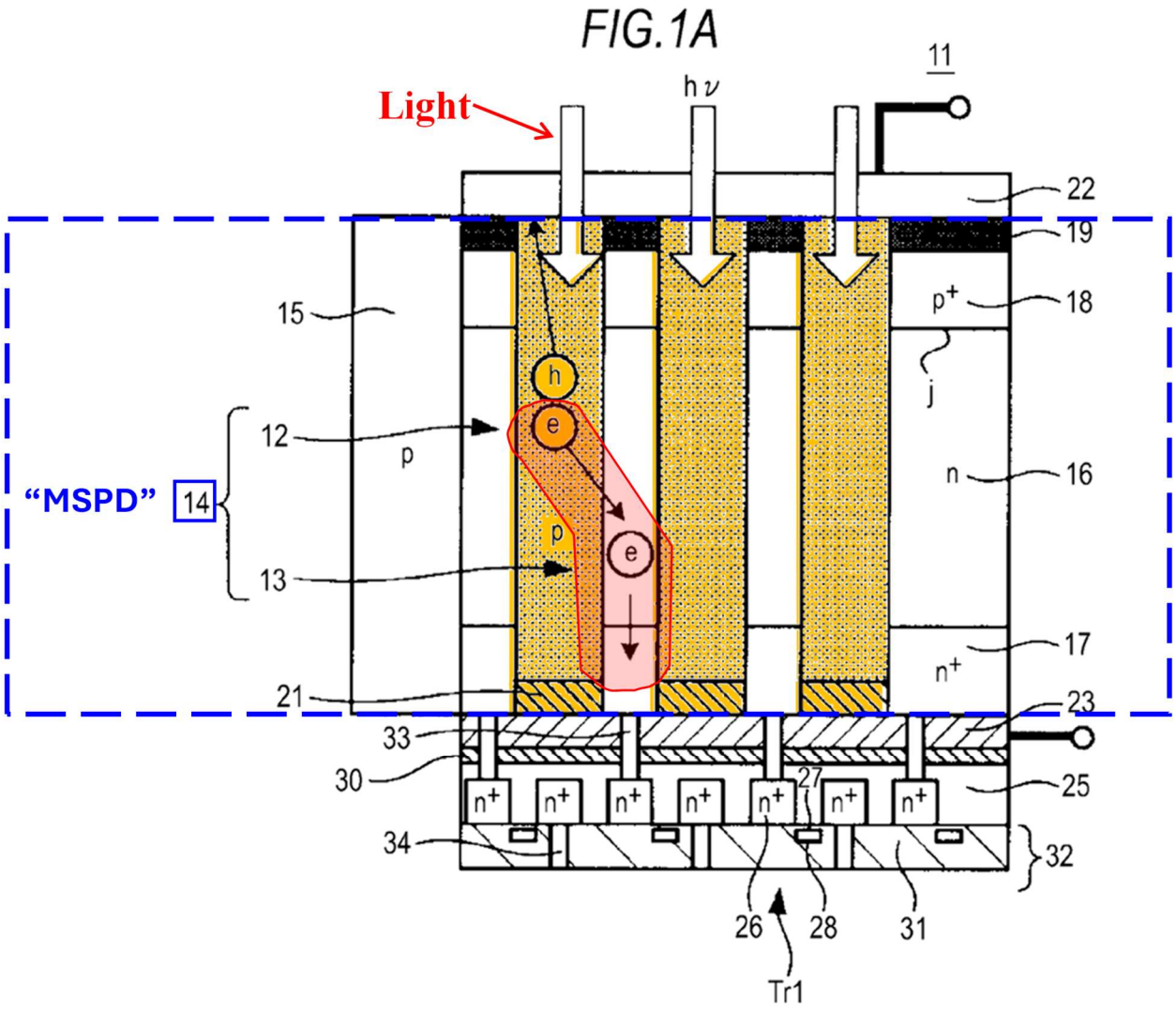
The light that passes through upper electrode 22 after passing through a color filter will have the same color (or wavelength) as the color filter. *Kuboi*, ¶¶[63]-[64], [90], Figs. 6A-6B; Lebby, ¶107. For instance, if a red filter is used, the wavelength of incident light will be about 650 nm; if a green filter is used, the wavelength will be about 540 nm, and so on. Lebby, ¶107; *see Kuboi*, ¶¶[6], [90].

Thus, the wavelength of light received by photoelectric conversion portion 14 is "substantially continuous" in cross-section, as claimed. Lebby, ¶107; *see Kuboi*, Fig. 1A. Moreover, based on the structure of pixel 11, a POSITA would have understood that light is uniformly received across the surface of photoelectric conversion portion 14 beneath upper electrode 22, rather than being limited to specific locations. Lebby, ¶107. Furthermore, based at least on the size of the arrows that illustrate incident light on the pixels, a POSITA would have recognized that the magnitude of the light received by photoelectric conversion portions 14 is substantially continuous in cross-section. Lebby, ¶107; *see Kuboi*, Figs. 1A, 3, 5A, 6A, 8A, 9, 10A, 13.

To the extent that *Kuboi* does not expressly disclose that light received by pixel 11 is substantially continuous in cross-section, this would have been obvious to a POSITA based on *Kuboi*. Lebby, ¶108. Imaging device 201 may be used in an imaging apparatus where light reflected from an object is guided to the pixels (including pixel 11) to capture an image of the object. *Kuboi*, ¶¶[48], [191]-[192], Fig. 16; Lebby, ¶108. A POSITA would have understood that each pixel receiving light that is substantially uniform in cross-section would assist in preserving the integrity of color reproduction and would enable the image sensor to produce sharper and more vivid images with reduced distortions. Lebby, ¶108; Ex-1015, 4-6 (discussing the impact of color variations and illumination levels on the pixels of

an image sensor on the resulting image). A POSITA would thus have been motivated to configure imaging device 201 such that the light received by pixel 11 is substantially uniform in cross-section, ensuring that the images produced by imaging device 201 are sharp and vivid. Lebby, ¶109. For example, a POSITA would have recognized that an optical system that guides light to the pixels can be configured such that the light received by pixel 11 is substantially uniform in cross-section. Lebby, ¶109. Given that this is a well-understood image sensor feature, the results would have been entirely predictable and a POSITA would have had a reasonable expectation of success in carrying out this modification. Lebby, ¶109.

Photoelectric conversion portion 14 converts the received light into electrical charges ("convert the optical input to an electrical output") and outputs it. Lebby, ¶¶110-111. As illustrated below, light that enters photoelectric conversion films 13 undergoes photoelectric conversion and generates electron-hole pairs. *Kuboi*, ¶[64].

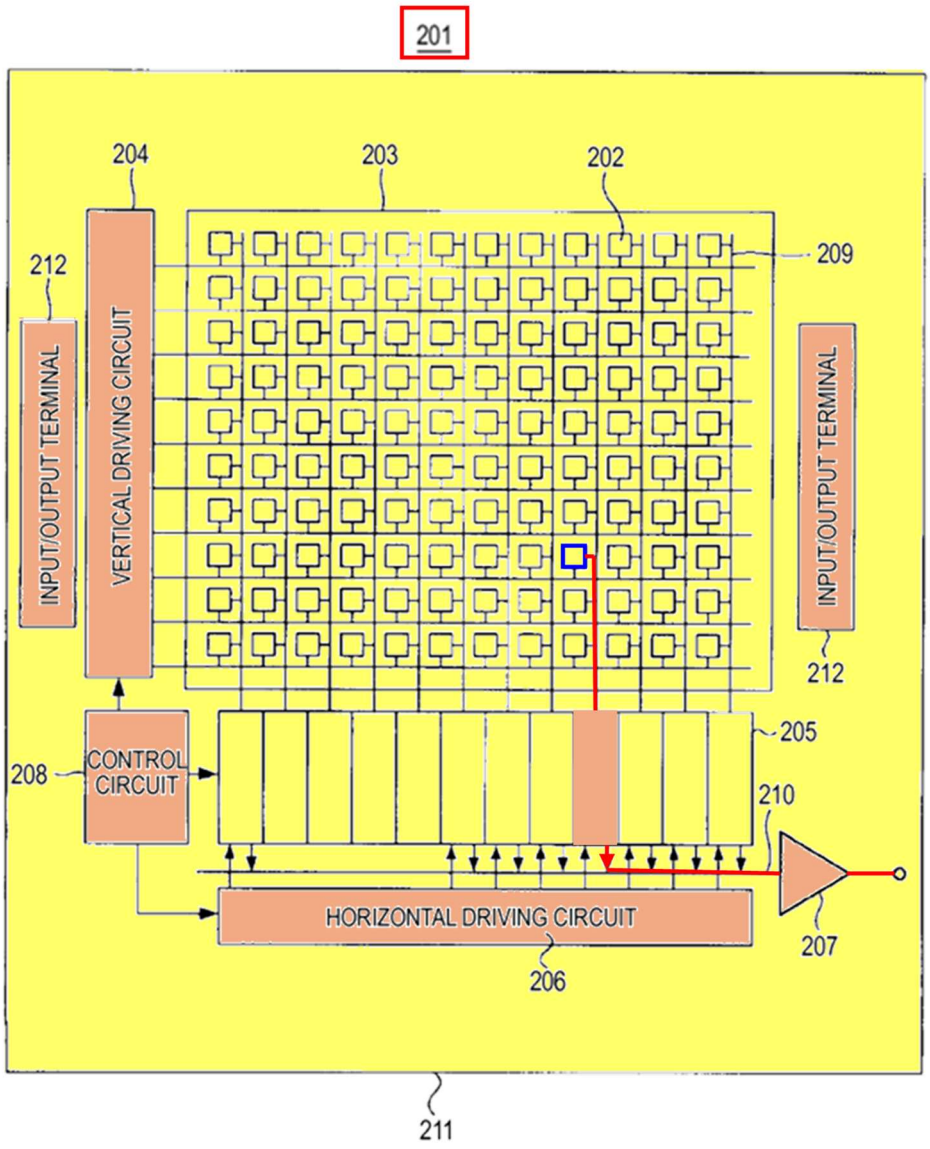


Kuboi, Fig. 1A. The highlighted arrows above show how the separated electrons (e), which serve as signal charges, move from photoelectric conversion films 13 through the interface and semiconductor layer 12, and are output from photoelectric conversion portion 14 to a charge accumulation region 26 of the pixel transistors via conductors 33. *Kuboi*, ¶¶[61], [62], [64], Fig. 1A; Lebby, ¶111.

Meanwhile, the holes (h) are discharged through upper electrode 22. *Kuboi*, ¶[64]. The signal charges that are generated based on the amount of light received by photoelectric conversion portion 14 are pixel 11's electrical output. *Kuboi*, ¶¶[51], [62]-[64]; Lebby, ¶111.

The peripheral circuit portion's logic circuits (that include circuits 204-208) process pixel 11's electrical output into a processed output. Lebby, ¶¶112-113. As indicated by the annotated red line below, vertical driving circuit 204 transfers the accumulated electrical output (via signal line 209) to the corresponding column signal processing circuit 205. *Kuboi*, ¶¶[51]-[52].

FIG.15

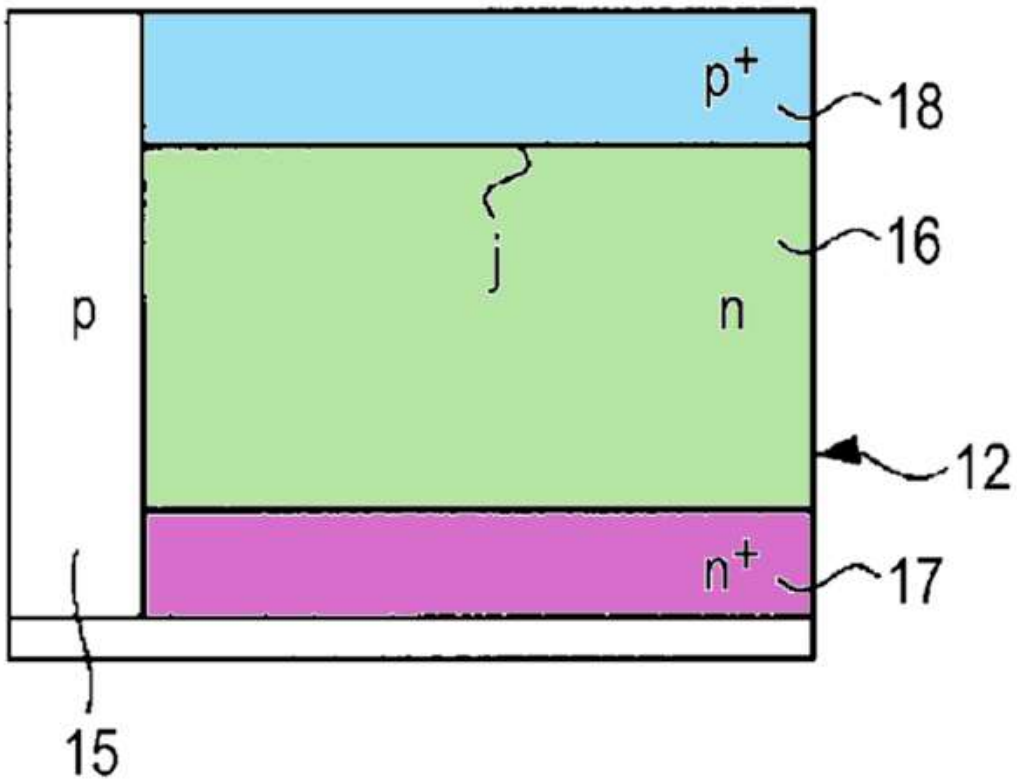


Kuboi, Fig. 15. This circuit performs signal processing tasks such as signal amplification and then outputs the amplified signals (via signal line 210) to output circuit 207, which conducts further signal processing and outputs the processed signals. *Kuboi*, ¶¶[52]-[54]; VI.A.2.n (**[1k]**), VI.A.2.o (**[1l]**); Lebby, ¶113.

d. [1a]: "the MSPD on or in said single substrate comprises an intermediate layer, a first layer at one side of the intermediate layer, and a second layer at an opposite side of the intermediate layer, wherein:"

Kuboi discloses this limitation because semiconductor layer 12 of photoelectric conversion portion 14 ("MSPD") comprises an n-type region 16 ("intermediate layer"), a p^+-type region 18 ("first layer") on one side of n-type region 16, and an n^+-type region 17 ("second layer") on the opposite side of n-type region 16. *Kuboi*, ¶¶[55]-[56], [71], Figs. 3, 4A; Lebby, ¶¶114-116. These layers are illustrated below:

FIG.4A



Kuboi, Fig. 4A. Silicon semiconductor layer 12 is implanted with impurities to form an "n^+-type semiconductor region 17 (corresponding to the front surface side), a n-type semiconductor region 16 (corresponding to an intermediate region), and a p^+-type semiconductor region [18] (corresponding to the rear surface side) … in that order from the lower region of the drawing [of Figure 4A] in a region corresponding to one pixel." *Kuboi*, ¶¶[55]-[56], [71]; Lebby, ¶115.

As discussed for **[1pre(b)]**, photoelectric conversion portion 14 ("MSPD") (including semiconductor layer 12 and the layers discussed above) is formed on substrate 211 (the "single substrate"). VI.A.2.b; Lebby, ¶116.

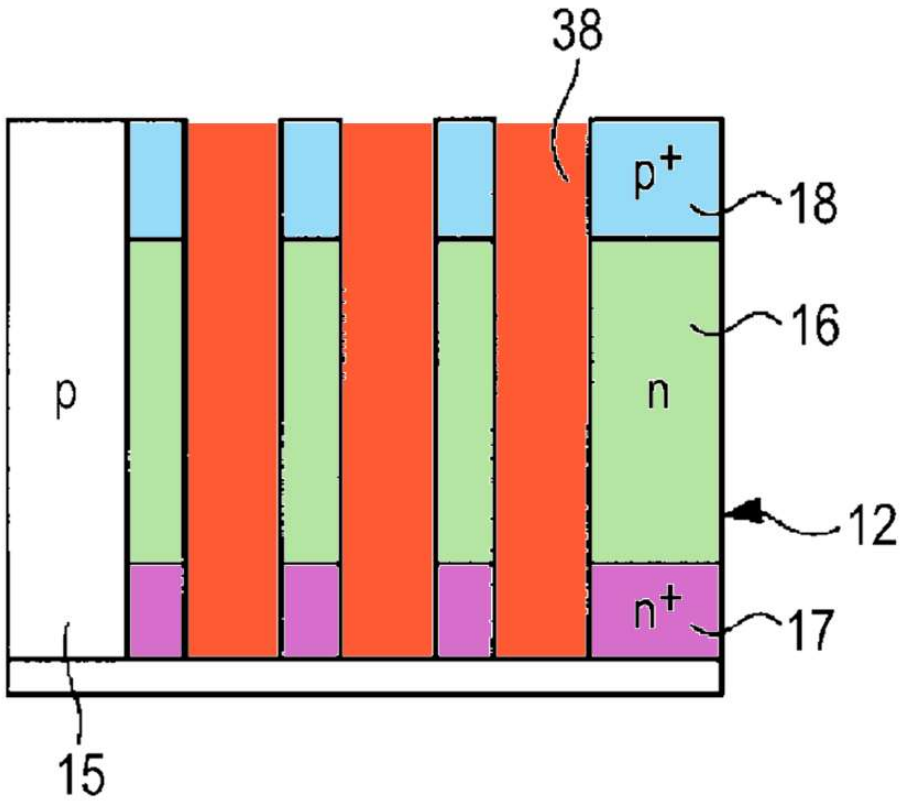
e. [1b]: "each of the layers comprises Silicon, Germanium, or an alloy thereof;"

Kuboi discloses this limitation because n^+-type semiconductor region 17 ("second layer"), n-type semiconductor region 16 ("intermediate layer"), and p^+-type semiconductor region 18 ("first layer") are each formed by implanting "semiconductor layer 12 formed of silicon" with impurities. Lebby, ¶117; *Kuboi*, ¶¶[55]-[56], [71]. Since these regions are created by implanting impurities into silicon, each region will comprise silicon. Lebby, ¶117; *Kuboi*, ¶[3] ("an impurity-implanted crystalline silicon layer"); *see also Kuboi*, ¶¶[6], [66], [110]-[111].

f. [1c]: "at least one of said layers, or an overlying covering layer that may be present, has holes intentionally formed therein, extending in directions transverse to the layers;"

Kuboi discloses this limitation because multiple vertical holes 38 ("holes intentionally formed") are dry-etched through the three regions ("layers") of pixel 11's semiconductor layer 12: n^+-type region 17, n-type region 16, and p^+-type region 18. Lebby, ¶¶118-122; *Kuboi*, ¶¶[71]-[72], Fig. 4B. These holes 38 are illustrated below:

FIG.4B



Kuboi, Fig. 4B. After regions 16, 17, and 18 are formed on semiconductor layer 12, "vertical hole[s] 38" "extending from the p^+-type … region 18 to the n^+-type … region [17] [are] formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching." *Kuboi*, ¶¶[71]-[72]; Lebby, ¶119. These holes can be cylindrically shaped or may extend into the page to form a stripe shape in a plan view. *Kuboi*, ¶[57]; *see Kuboi*, Fig. 1B.

A light shielding film 19 ("an overlying covering layer"), which is formed on (and overlies) the light incident surface of p^+-type region 18, also contains holes that align with the holes in the underlying PiN regions. *Kuboi*, ¶¶[76], [91], Fig. 1A; Lebby, ¶120.

FIG.4E

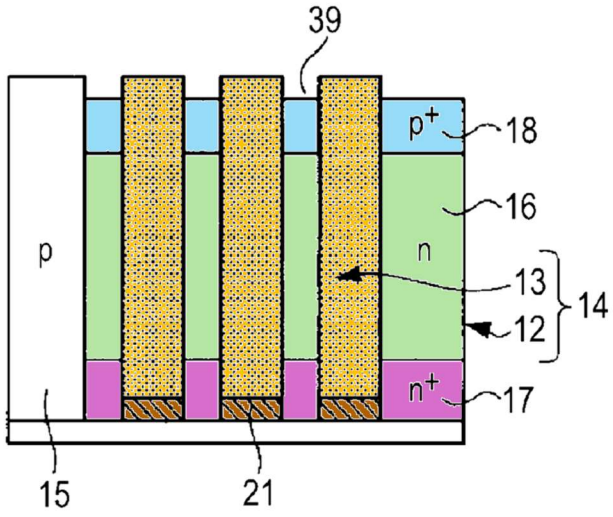
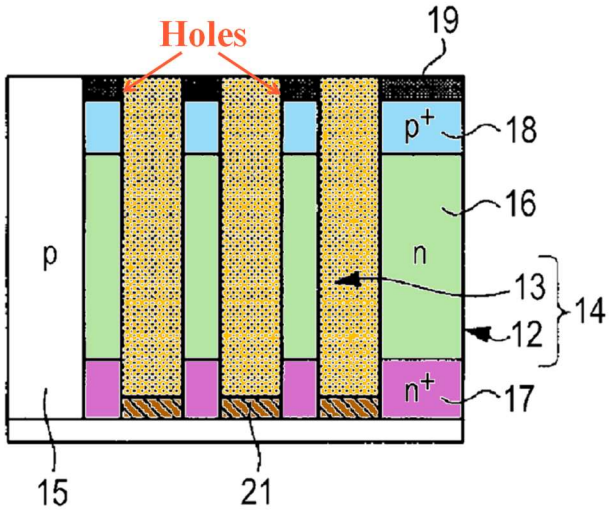


FIG.4F



Kuboi, Figs. 4E, 4F. After depositing photoelectric conversion films 13 into holes 38 formed through regions 16, 17, and 18, the surfaces of films 13 are covered

using a resist mask (not shown). *Kuboi*, ¶¶[73]-[75]; Lebby, ¶121. The exposed surface of p^+-type region 18 is then etched back, causing the embedded films 13 to protrude from the surface of p^+-type region 18. *Kuboi*, ¶[75], Fig. 4E. Then, a light shielding film 19 is applied on the etched surface of p^+-type region 18 around protruding films 13 so that incident light only enters exposed films 13 (and not p^+-type region 18). *Kuboi*, ¶¶[[59], [76]. Applying light shielding film 19 around protruding films 13 results in holes being formed in light shielding film 19 around films 13. Lebby, ¶121.

Kuboi discloses that vertical holes 38 extending through the PiN regions may be dry-etched "using a CCP (Capacitive Coupled Plasma) etching apparatus" or other apparatuses. *Kuboi*, ¶¶[72], [95]. Therefore, a POSITA would have understood that these holes 38 are intentionally created. Lebby, ¶122. Since the holes in the overlying light shielding film 19 are formed by etching back p^+-type region 18 around films 13 and forming light shielding film 19 around the protruding films 13, holes in the light shielding film 19 are also intentionally created. *Kuboi*, ¶¶[72], [75]-[76]; Lebby, ¶122. Furthermore, since the holes extend perpendicularly through the PiN regions, they extend transversely through these regions. Lebby, ¶122; *Kuboi*, ¶¶[72], [75]-[76], Figs. 1A, 4A-4F.

g. [1d]: "each of the first and second layers comprises a doped material;"

Kuboi discloses this limitation because p^+-type region 18 ("first layer") and n^+-type region 17 ("second layer") of semiconductor layer 12 are formed by "implant[ing] … impurities" in silicon semiconductor layer 12. *Kuboi*, ¶¶[55]-[56]; Lebby, ¶¶123-124.

According to *Kuboi*, "semiconductor layer 12 [formed of silicon] is implanted with impurities … [to form] a[n] n^+-type … region 17 having higher concentration [of impurities] than the n-type … region 16, and a semiconductor region 18 of second conductivity type (for example, p^+ type) having higher concentration [of impurities] than the n-type … region 16." *Kuboi*, ¶¶[55]-[56]; *see also Kuboi*, ¶¶[7], [111], [151]. A POSITA would have understood that the process of implanting impurities into silicon material is known as "doping" the silicon material and the result is a "doped material," as claimed. Lebby, ¶124; Ex-1018, 3 (defining "doping" as "the process of introducing impurity atoms into pure silicon to change its electrical properties"); Ex-1019, 23 ("Impurity doping is the introduction of controlled amounts of impurity dopants into semiconductor materials."); Ex-1020, 4 ("A doped region is simply a section of the silicon into which impurity atoms have been purposely added to alter the electrical

properties."); *see* Ex-1026, 3. Therefore, *Kuboi*'s first and second layers comprise doped silicon. Lebby, ¶124.

h. [1e]: "the intermediate layer comprises a material that is less doped than at least one of the first and second layers or is undoped, wherein the degree of doping is the same or different for different positions in the intermediate layer;"

Kuboi discloses this limitation because its n-type region 16 ("intermediate layer") comprises silicon that is less doped than both p^+-type region 18 ("first layer") and n^+-type region 17 ("second layer"). *Kuboi*, ¶[56]; Lebby, ¶¶125-132. And, in addition, the degree of doping is the same or different at different positions in n-type region 16. *Kuboi*, ¶[56]; Lebby, ¶¶125-132.

According to *Kuboi*, "semiconductor layer 12 [formed of silicon] is implanted with impurities … [to form] a semiconductor region 16 of first conductivity type (for example, n type), a[n] n^+-type semiconductor region 17 having higher concentration [of impurities] than the n-type semiconductor region 16, and a semiconductor region 18 of second conductivity type (for example, p^+ type) having higher concentration [of impurities] than the n-type semiconductor region 16." *Kuboi*, ¶¶[55]-[56]; *see also Kuboi*, ¶¶[7], [111], [151]. As explained for **[1d]**, "the process of introducing impurity atoms into pure silicon" is doping the silicon material and results in a "doped material." Ex-1018, 3; Ex-1020, 4; VI.A.2.g. Thus, n-type region 16 comprises doped silicon with a concentration of

impurities (or degree of doping) less than that in p^+-type region 18 and n^+-type region 17. Lebby, ¶126.

A POSITA would have understood that the degree of doping in n-type region 16 ("intermediate region") would either be the same or different at different positions, as no other possibilities exist. Lebby, ¶¶127-132. *Kuboi* uses "ion implantation" for implanting impurities in semiconductor layer 12. *Kuboi*, ¶¶[7], [134]. After ion implantation, the dopant concentration varies with depth (*x* in the figure below) of the layer. Lebby, ¶¶127-131; Ex-1020, 4; Ex-1019, 23-24; Ex-1028, 1.

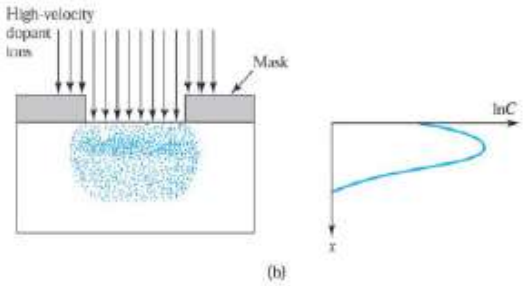
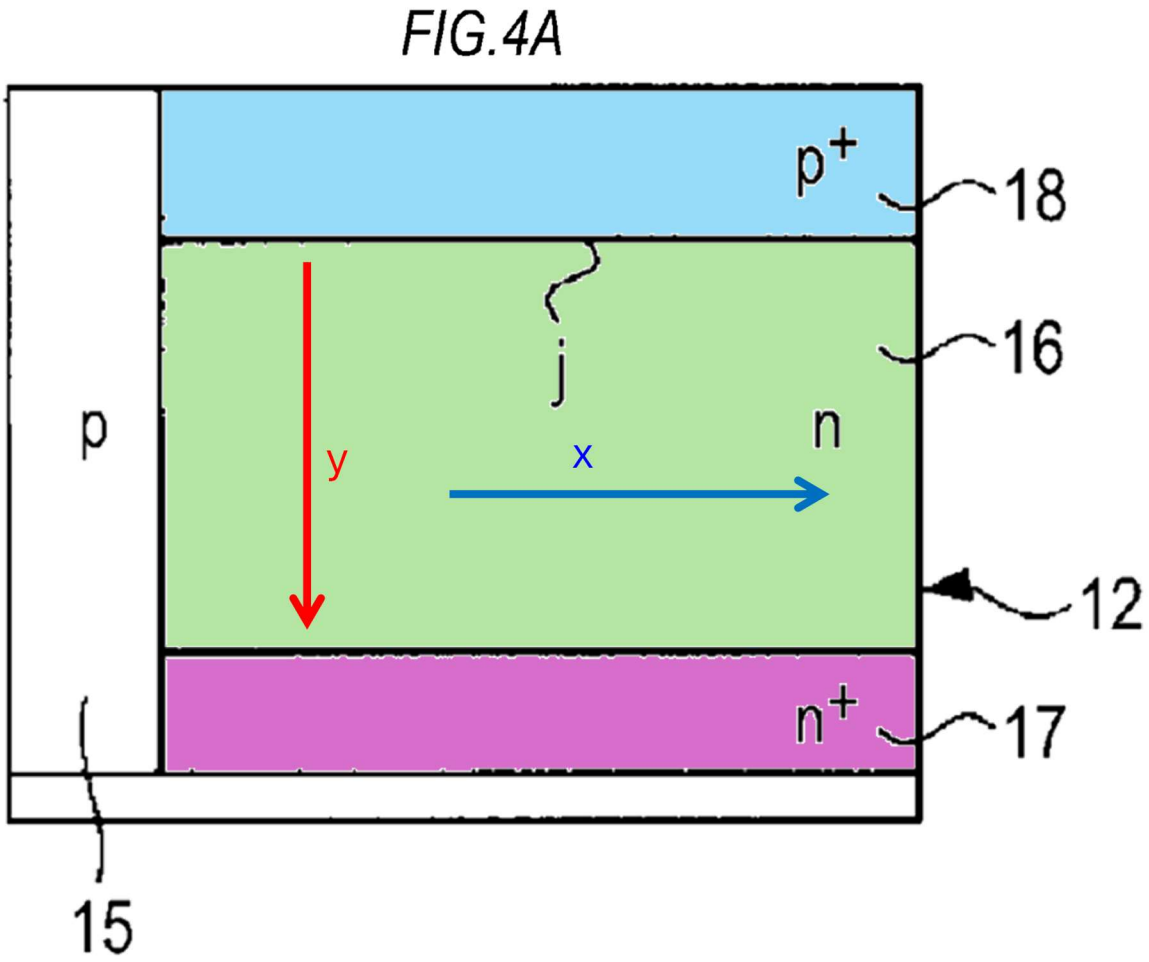


Fig. 1 **Comparison of (*a*) diffusion and (*b*) ion-implantation techniques for selective introduction of dopants into the semiconductor substrate.**

Ex-1019, 24 (Fig. 1 cropped). A POSITA would thus have recognized that the degree of doping in n-type region 16 will be different at different positions along the depth (along line y in the figure below) and the same for different positions along its width (along line x in the figure below). Lebby, ¶132.



Kuboi, Fig. 4A. Therefore, in *Kuboi*, " the degree of doping is the same or different for different positions in the intermediate layer," as claimed. Lebby, ¶132.

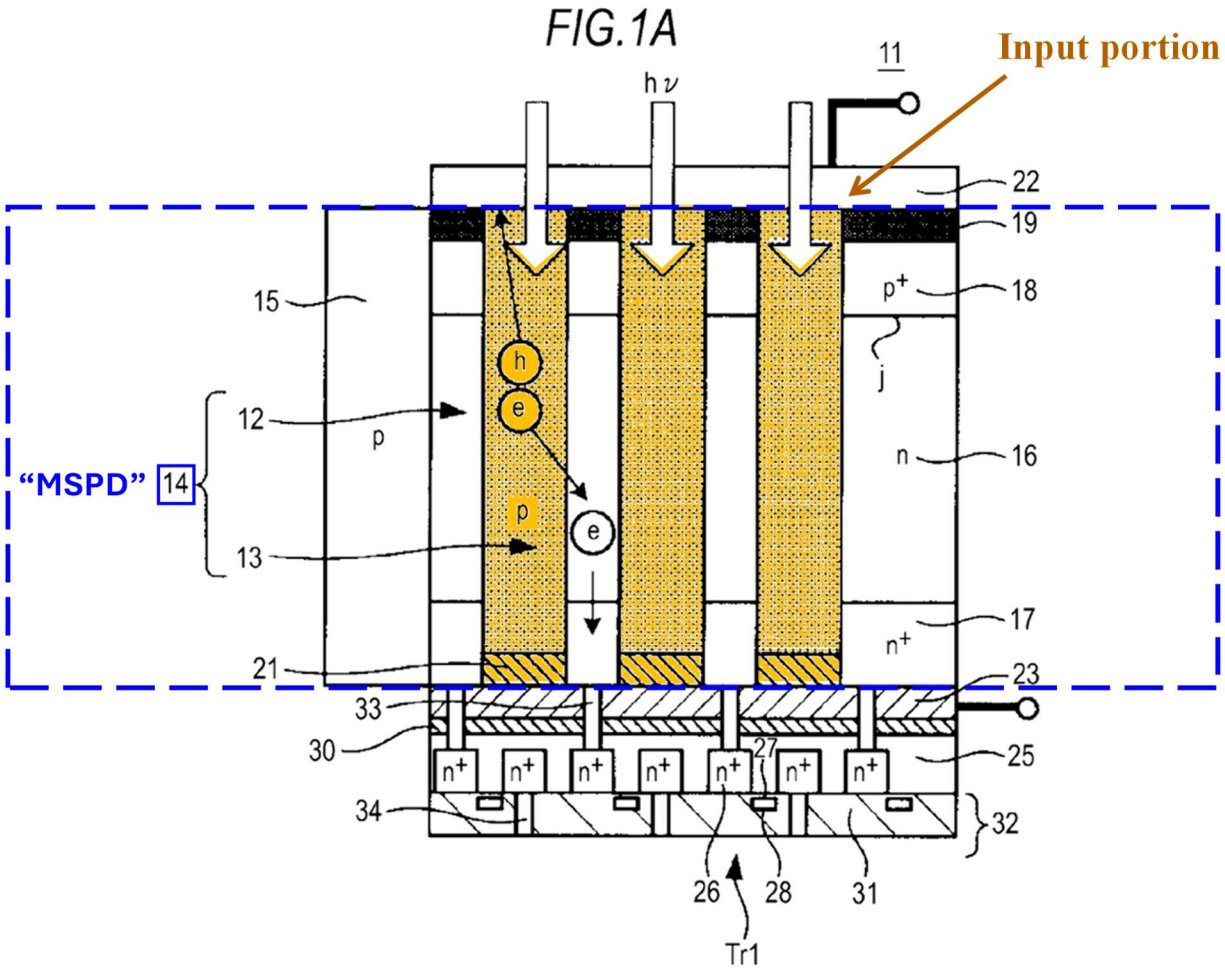
i. [1f]: "an input portion configured to concurrently receive at a plurality of said holes said optical input that has said substantially continuous cross-section; and"

Kuboi discloses and renders obvious this limitation because, as explained for **[1pre(c)]**, light ("optical input") that passes through transparent upper electrode 22 of pixel 11 is substantially continuous in cross-section (or this would have been

obvious), VI.A.2.c, and since light enters photoelectric conversion films 13 (extending through holes in semiconductor layer 12) through upper electrode 22, the holes are configured to concurrently receive light having substantially continuous cross-section. Lebby, ¶¶133-137.

Pixel 11 includes an on-chip microlens (not shown in the drawings) formed on transparent upper electrode 22 with a color filter therebetween. *Kuboi*, ¶¶[63]-[64], [90]. Light from the on-chip microlens passes through the color filter and upper electrode 22 and enters photoelectric conversion film 13 exposed through the light shielding film 19 of photoelectric conversion portion 14. *Kuboi*, ¶¶[63]-[64], Fig. 1A; VI.A.2.c (**[1pre(c)]**), VI.A.2.f (**[1c]**); Lebby, ¶¶134-135. According to *Kuboi*, the plurality of organic photoelectric conversion films 13 may be formed in a cylindrical hollow shape or a stripe shape as viewed from the upper surface of photoelectric conversion portion 14. *Kuboi*, ¶[57], Fig. 1B.

As illustrated below, the upper surface of photoelectric conversion portion 14 (where films 13 are exposed through light shielding film 19) serves as an "input portion" through which light enters photoelectric conversion portion 14. Lebby, ¶135.



Kuboi, Fig. 1A. As explained for **[1c]**, photoelectric conversion films 13 are embedded in holes that extend vertically through the PiN regions of photoelectric conversion portion 14. VI.A.2.f; Lebby, ¶136. Thus, photoelectric conversion portion 14 has an input portion that is configured to receive, at a plurality of holes, light having a substantially continuous cross-section. Lebby, ¶136.

A POSITA would have recognized that all photoelectric conversion films 13 exposed at the input portion would receive light concurrently. Lebby, ¶137. *Kuboi* discloses that its imaging device may be used in a camera where an optical system

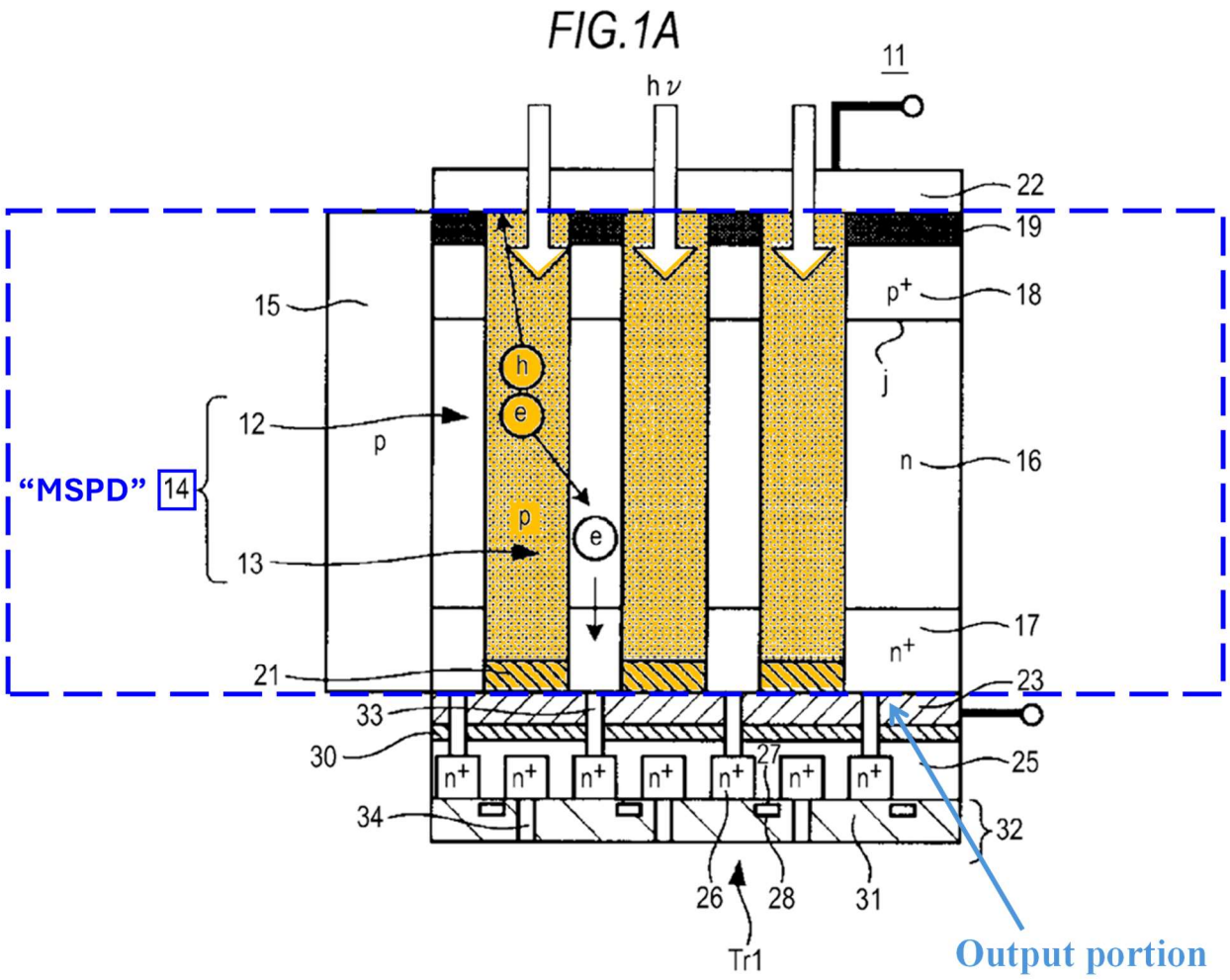
guides incident light (e.g., light reflected from an object) to the pixel portion of the imaging device. *Kuboi*, ¶¶[191]-[192], Fig. 16; Lebby, ¶137. A POSITA would have understood that pixel 11 (including films 13 exposed at the input portion) receives the light reflected from the object concurrently so that the image of the object can be accurately recorded. Lebby, ¶137.

j. [1g]: "an output portion configured to provide said electrical output from the MSPD;"

Kuboi discloses this limitation because the electric charge carriers generated from the photoelectric conversion of light in photoelectric conversion films 13 are output through multiple conductors 33 exposed at the lower surface of photoelectric conversion portion 14. Lebby, ¶¶138-140; *Kuboi*, ¶¶[62], [64], Fig. 1A. The lower surface functions as an "output portion," providing electrical output from photoelectric conversion portion 14. Lebby, ¶¶138-139.

Kuboi discloses that incident light that enters films 13 in photoelectric conversion portion 14 undergoes photoelectric conversion, generating electron-hole pairs. *Kuboi*, ¶[64]; VI.A.2.c (**[1pre(c)]**). As indicated by arrows in Figure 1A below, the separated electrons (e), which act as signal charges, travel from films 13 through the interface and semiconductor layer 12, exiting photoelectric conversion

portion 14 via conductors 33. *Kuboi*, ¶¶[62], [64]; Lebby, ¶139.



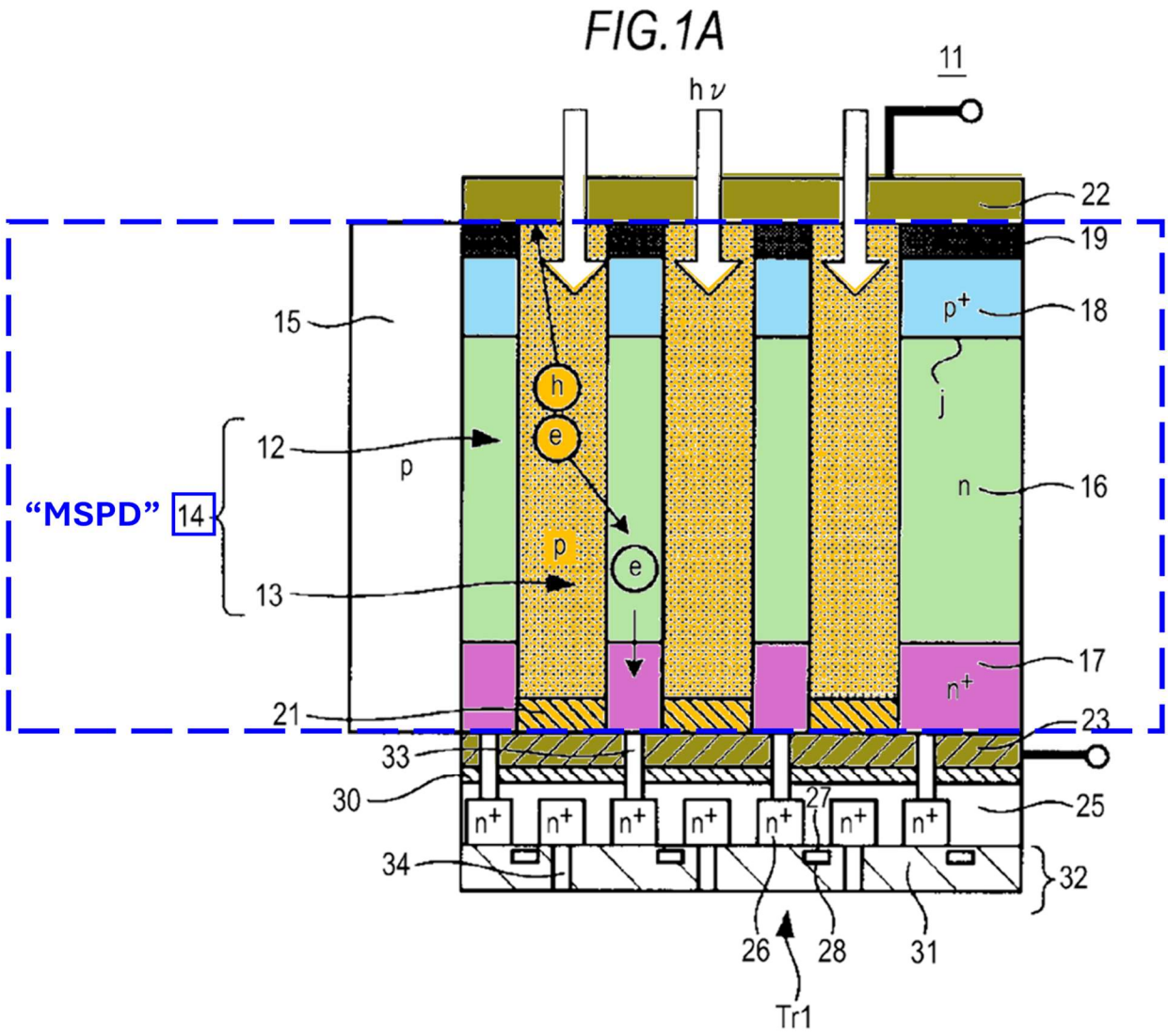
Kuboi, Fig. 1A. The signal charges, determined by the amount of light received by photoelectric conversion portion 14, form the photoelectric conversion portion 14's electrical output. *Kuboi*, ¶[51]; VI.A.2.c (**[1pre(c)]**); Lebby, ¶¶139-140. The signal charges are delivered from photoelectric conversion portion 14 to a charge accumulation region 26 of the pixel transistors via electrically isolated conductors 33 that are exposed at the lower surface of photoelectric conversion

portion 14. *Kuboi*, ¶¶[62], [64]. The lower surface thus functions as an "output portion," as claimed, for providing electrical output from photoelectric conversion portion 14. Lebby, ¶140.

k. [1h]: "the MSPD includes reverse-bias electrodes coupled therewith to establish an electrical field therein when energized to thereby sweep in a selected direction electrical charges generated in the MSPD by said optical input;"

Kuboi discloses this limitation because photoelectric conversion portion 14 ("MSPD") includes reverse-bias upper and lower electrodes 22, 23 to establish an electric field in photoelectric conversion portion 14 to sweep the signal charges generated by photoelectric conversion of received light towards lower electrode 23 and conductors 33. Lebby, ¶¶141-147; *Kuboi*, ¶¶[62], [64].

Transparent upper electrode 22 is formed on light shielding film 19, covering the entire upper surface of photoelectric conversion portion 14 through which light enters. *Kuboi*, ¶¶[60], [77], Fig. 1A; Lebby, ¶142. Lower electrode 23 is formed on the entire lower surface of photoelectric conversion portion 14 on n^+-type region 17. *Kuboi*, ¶¶[60], [77], Fig. 1A; Lebby, ¶142. Both electrodes are depicted below:



Kuboi, Fig. 1A. Upper electrode 22 is in electrical contact with p^+-type region 18 (of semiconductor layer 12) through light shielding film 19, which is made of electrically conductive tungsten. Lebby, ¶¶142-143; *Kuboi*, ¶¶[59]-[60]; Ex-1019, 21-22 (discussing the use of tungsten as the first level metal and contact plugs of IC devices); Ex-1020, 14 (discussing using tungsten plugs in electrically conductive vias between different metal layers of a CMOS chip), 15.

Kuboi discloses that a sufficient voltage is applied between upper and lower electrodes 22, 23 so that p^+-type region 18 is at a negative potential and n^+-type region 17 is at a positive potential. *Kuboi*, ¶¶[64], [87], Fig. 1A; Lebby, ¶144. The applied bias voltage creates a depletion layer in n-type region 16 between regions 17 and 18. *Kuboi*, ¶¶[64], [87]; Lebby, ¶144. As explained for **[1pre(a)]**, a POSITA would have understood that applying a voltage bias with a negative potential to p^+-type region 18 and a positive potential to n^+-type region 17 constitutes a reverse bias. VI.A.2.a; Lebby, ¶144. Thus, upper electrode 22 and lower electrode 23 are reverse-bias electrodes that are coupled to photoelectric conversion portion 14. Lebby, ¶144.

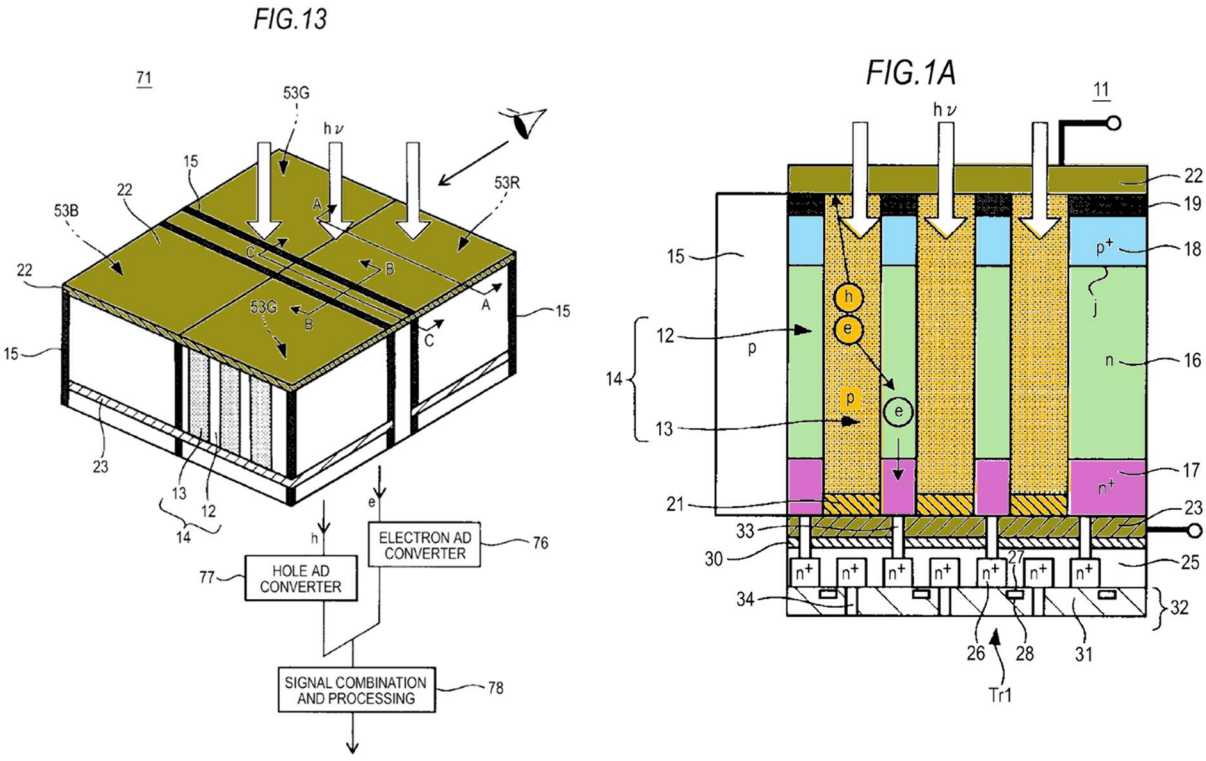
Kuboi discloses that when a reverse bias is applied and incident light (hγ) enters photoelectric conversion films 13, electrons (e) in the electron-hole pairs generated by photoelectric conversion of the light move from films 13 through the interface and semiconductor layer 12, which is depleted by the applied bias voltage, toward lower electrode 23 and exit photoelectric conversion portion 14 through conductors 33. *Kuboi*, ¶¶[62], [64], Fig. 1A; Lebby, ¶145. Meanwhile, the generated holes (h) move toward upper electrode 22 through photoelectric conversion films 13 and are discharged through upper electrode 22. *Kuboi*, ¶[64]; Lebby, ¶145.

A POSITA would have understood that when a reverse bias is applied to photoelectric conversion portion 14, the electrodes establish an "electrical field," as claimed, in photoelectric conversion portion 14. Lebby, ¶146. This electrical field encourages the electron-hole pairs created by the photoelectric conversion of the light to separate and move towards respective electrodes. Lebby, ¶146; Ex-1019, 10-11 (detailing how an electric field generated by electrodes in a reverse-bias arrangement separates electron-hole pairs and causes them to drift towards the electrodes).

Kuboi explains that "[t]he hybrid photoelectric conversion portion is configured so that charges generated in the organic material layers through photoelectric conversion move inside the semiconductor layer so as to be guided to a charge accumulation region." *Kuboi*, ¶[11], claim 1. Thus, when a reverse bias is applied to upper and lower electrodes 22 and 23, the electrons generated in photoelectric conversion films 13 by the incident light are driven toward lower electrode 23 and conductors 33 ("to thereby sweep in a selected direction electrical charges generated in the MSPD by said optical input"), while the holes are swept toward upper electrode 22. Lebby, ¶147.

l. [1i]: "said reverse-bias electrodes being free of a pattern of openings that matches said holes; and"

Kuboi discloses this limitation because, as shown below, upper and lower electrodes 22, 23 do not have openings that match the holes of photoelectric conversion portion 14. Lebby, ¶¶148-149; *Kuboi*, ¶[60], Figs. 1A, 13.



Kuboi, Figs. 13 (left), 1A (right). Upper electrode 22 is transparent, allowing incident light to pass through and enter photoelectric conversion portion 14. Lebby, ¶149. It does not have any openings, much less openings that align with the holes in the photoelectric conversion portion 14. Lebby, ¶149. Meanwhile, lower electrode 23 has openings for conductors 33, but these openings are not in the same

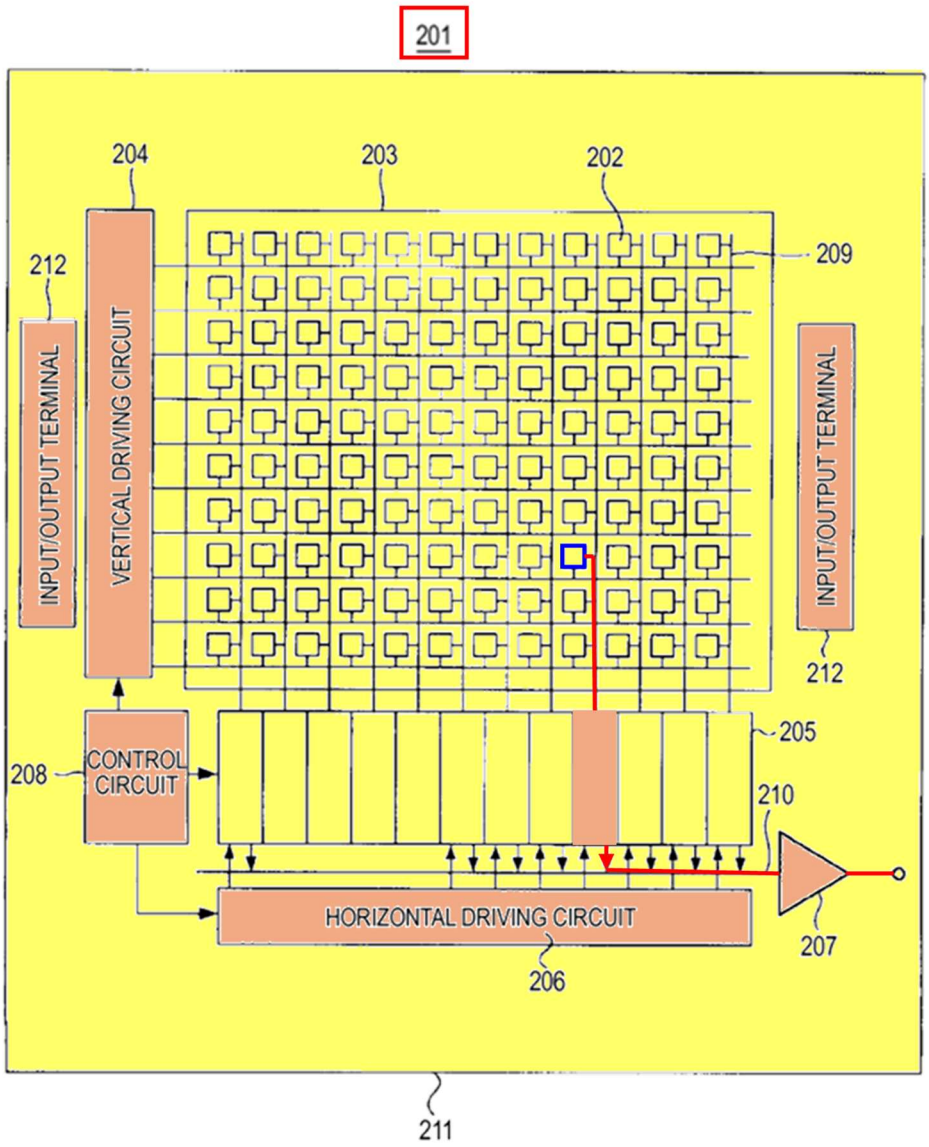
position as the holes of photoelectric conversion portion 14. Lebby, ¶149; *Kuboi*, ¶[62], Fig. 1A.

m. [1j]: "the active electronic circuit on or in said single substrate is configured to process the electrical output from the MSPD by applying thereto:"

Kuboi discloses this limitation because the logic circuits of the active electronic circuit (vertical driving circuit 204, a column signal processing circuit 205, horizontal driving circuit 206, output circuit 207, and control circuit 208) perform signal processing of the electrical signals output from photoelectric conversion portion 14 ("MSPD") of pixel 11. Lebby, ¶¶150-152; *Kuboi*, ¶¶[49]-[52], Fig. 15. As discussed for **[1pre(b)]**, all logic circuits of the peripheral circuit portion (including the active electronic circuit) are formed on or in substrate 211 along with the pixels. VI.A.2.b.

Kuboi's active electronic circuit processes the electrical output from photoelectric conversion portions 14. Lebby, ¶151. For instance, column signal processing circuit 205 "perform[s] signal processing such as noise removal" for each pixel 202 (such as pixel 11 with photoelectric conversion portion 14) in a column. *Kuboi*, ¶[52]. According to *Kuboi*, "column signal processing circuits 205 perform signal processing such as [correlated double sampling] CDS for removing fixed pattern noise inherent in the pixels 202, signal amplification, or AD conversion." *Kuboi*, ¶[52]. This is illustrated below:

FIG.15

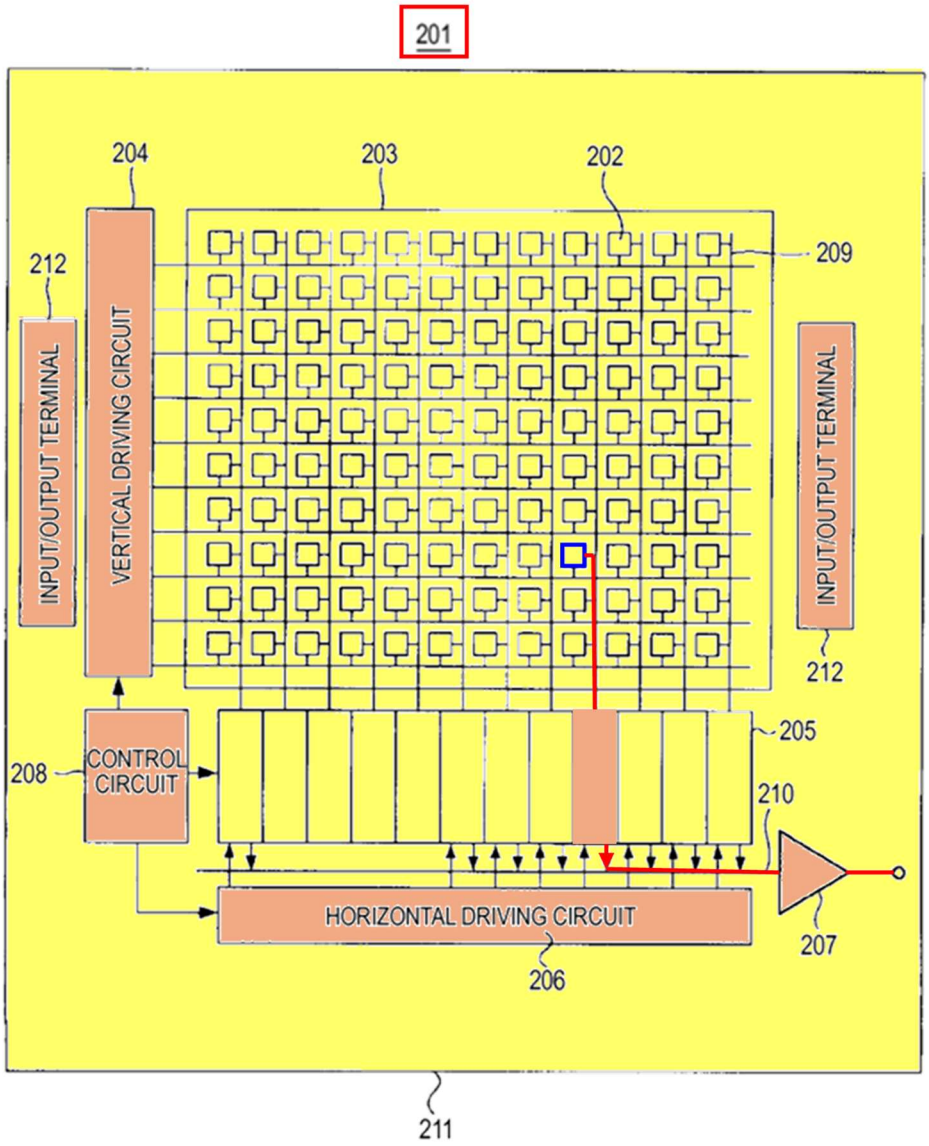


Kuboi, Fig. 15. Thus, *Kuboi*'s "active electronic circuit" (circuits 204-208) processes the electrical output from photoelectric conversion portions 14. Lebby, ¶152; *Kuboi*, ¶¶[49], [52].

n. [1k]: "amplification to form said processed output from the single-chip device;"

Kuboi discloses this limitation. Lebby, ¶¶153-156. The logic circuits of *Kuboi*'s active electronic circuit amplify the electrical output of pixel 11 and outputs it from imaging device 201. Lebby, ¶153; *Kuboi*, ¶¶[48]-[49], [52]-[54]. Specifically, "column signal processing circuit[] 205 perform[s] signal processing such as … signal amplification" of the electrical output from a pixel (pixel 11 with photoelectric conversion portion 14). *Kuboi*, ¶[52]; Lebby, ¶153. Horizontal driving circuit 206 sequentially selects and outputs the processed signals from column signal processing circuit 205 to output circuit 207, which then outputs the processed signals from imaging device 201. *Kuboi*, ¶¶[52]-[54]; Lebby, ¶153. This is illustrated below:

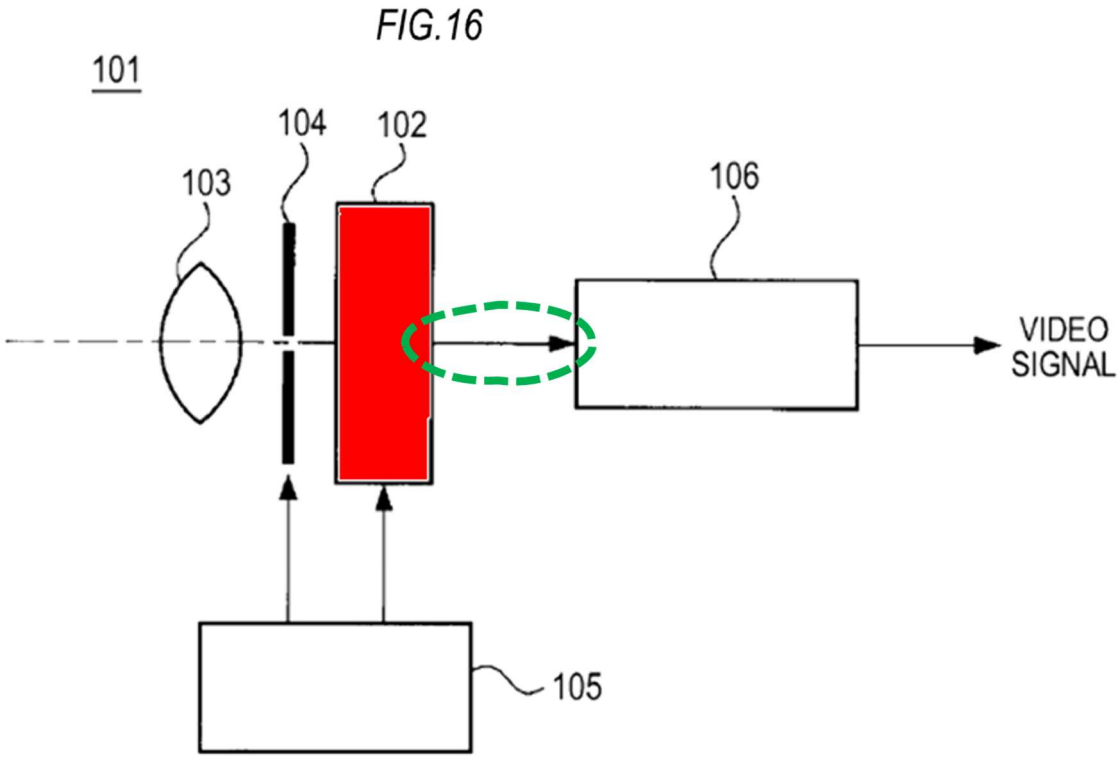
FIG.15



Kuboi, Fig. 15. Thus, column signal processing circuit 205 amplifies the electrical output from photoelectric conversion portion 14, and the processed signal is output through output circuit 207. Lebby, ¶154.

Output circuit 207 outputs the processed electrical output of photoelectric conversion portion 14 from imaging device 102. Lebby, ¶¶155-156; *Kuboi*, ¶¶[54],

[191]-[193]. For example, as illustrated below, imaging device 102 can be applied in an apparatus having an external signal processing circuit. *Kuboi*, ¶¶[191]-[193], Fig. 16.

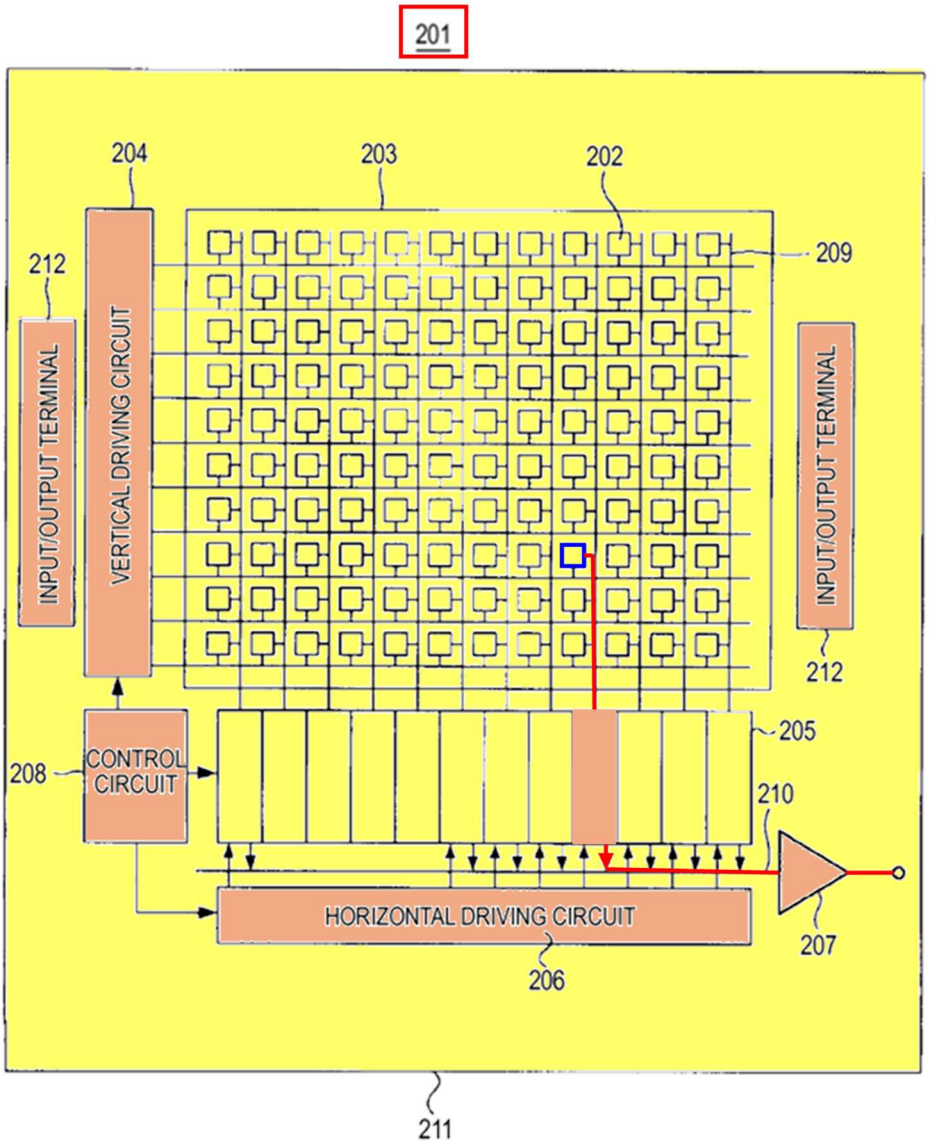


Kuboi, Fig. 16. In this application, output circuit 207 of imaging device 102 outputs the processed output of photoelectric conversion portion 14 to external signal processing circuit 106 as shown in the figure above. *Kuboi*, ¶¶[54], [192], Fig. 16; Lebby, ¶156; VI.A.17.b (**[26b]**).

o. [1l]: "processing other than or in addition to amplification to form said processed output from the single-chip device; and"

Kuboi discloses this limitation. Lebby, ¶¶157-158. In addition to amplifying the electrical output received from pixels 11, VI.A.2.n (**[1k]**), the logic circuits of the active electronic circuit perform additional signal processing of the received signals before outputting the processed output. Lebby, ¶157; *Kuboi* ¶¶[49], [54]. Specifically, "output circuit 207," which is part of the active electronic circuit, "performs signal processing on signals which are sequentially supplied from each of the column signal processing circuits 205 through the horizontal signal line 210 and outputs the processed signals." *Kuboi*, ¶[54]. For example, according to *Kuboi*, "output circuit 207 may perform only buffering and may perform black level adjustment, column fluctuation correction, various digital signal processings, and the like." *Kuboi*, ¶[54]. Hence, as shown in the figure below, output circuit 207 conducts further signal processing on the processed signals from column signal processing circuit 205 before outputting the processed output. Lebby, ¶¶157-158.

FIG.15



Kuboi, Fig. 15.

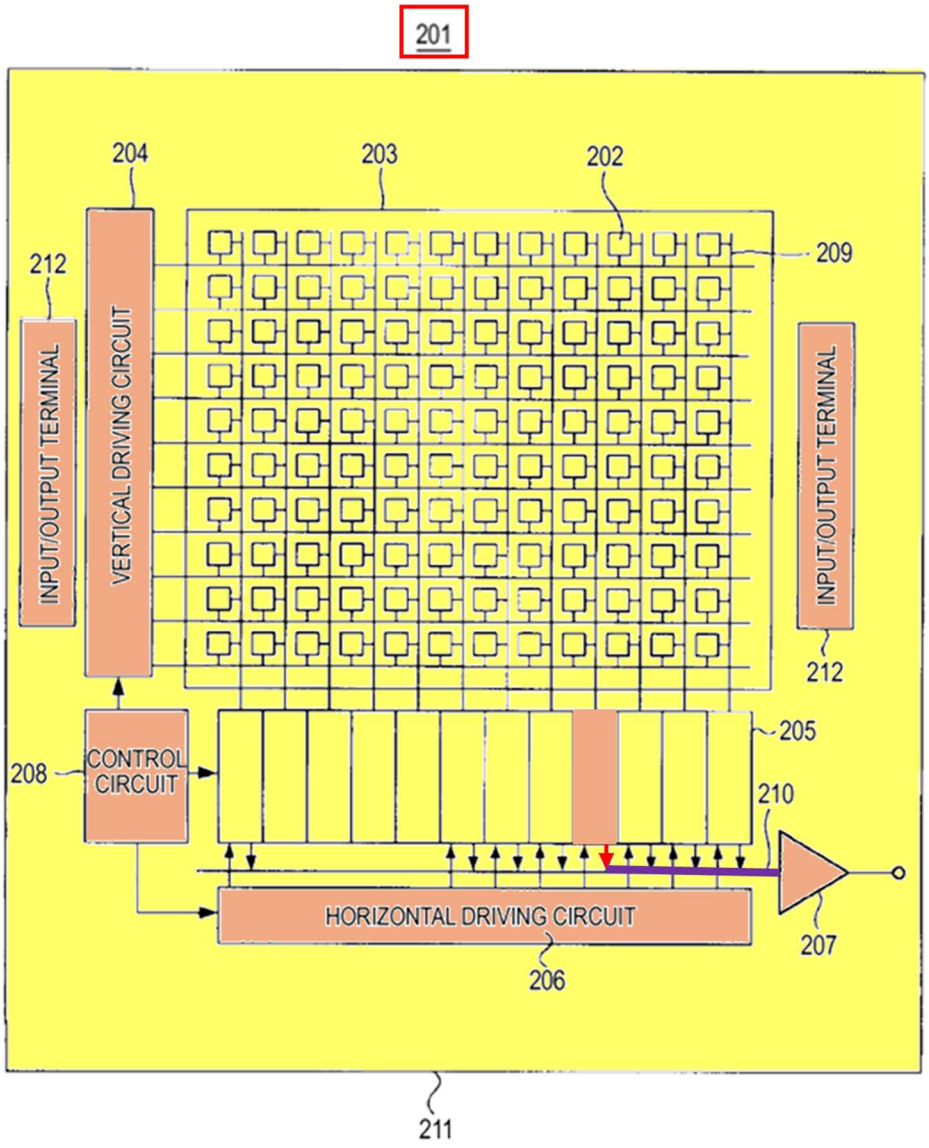
p. [1m]: "routing to one or more selected destinations; and"

Kuboi discloses this limitation. Lebby, ¶¶159-162. Horizontal driving circuit 206 of the active electronic circuit sequentially selects and outputs the processed signals from each column signal processing circuit 205 (including column signal

processing circuit 205) to output circuit 207 through horizontal signal line 210. VI.A.2.o (**[1l]**); *Kuboi*, ¶¶[53]-[54].

To the extent that the term "routing" refers to the physical connection to a destination, horizontal signal line 210, which delivers processed signals from column signal processing circuit 205 to output circuit 207, performs "routing." Lebby, ¶160; *see* Ex-1020, 38 (describing "metal routing" that connects devices in a CMOS circuit). This routing is illustrated below:

FIG.15

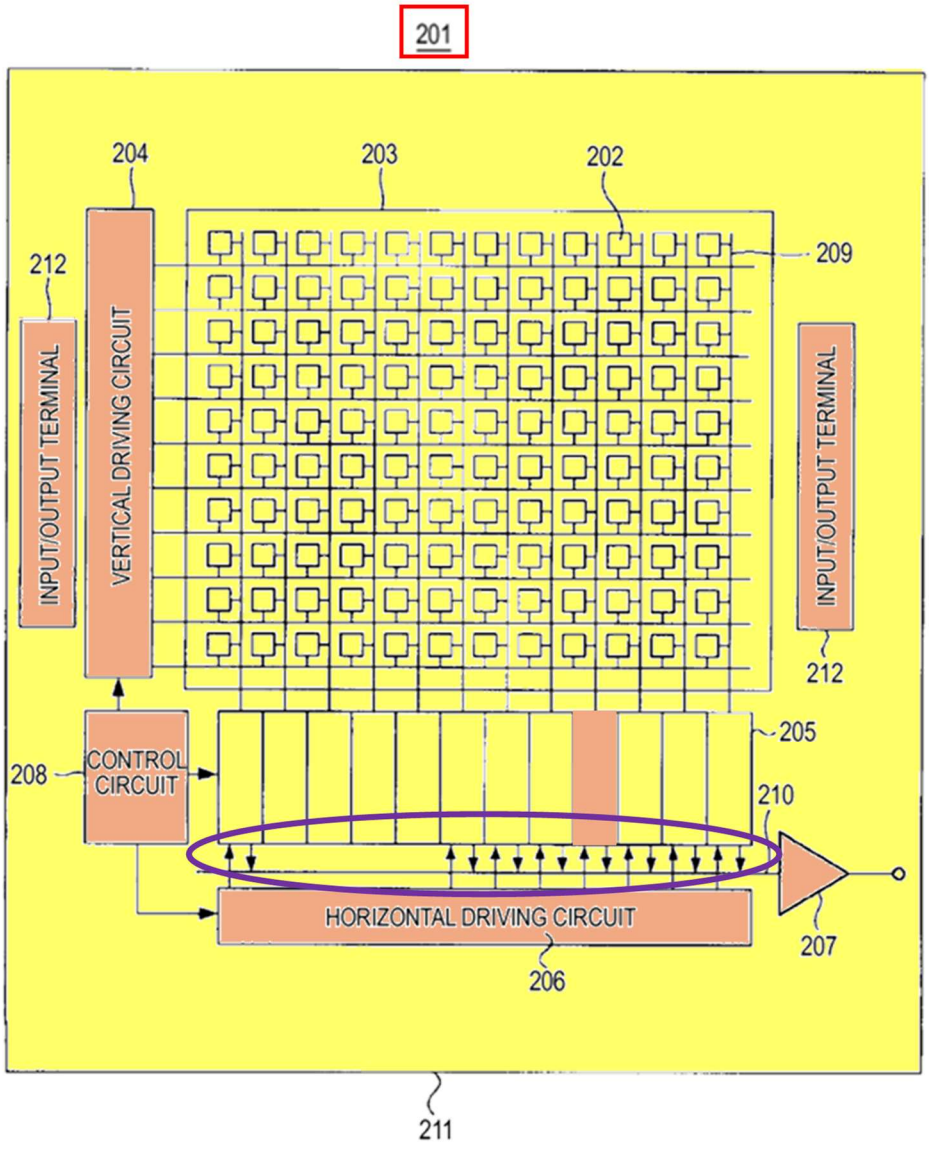


Kuboi, Fig. 15.

To the extent that the term "routing" refers to the process of delivering signals to a destination, *see* Ex-1018, 6, horizontal driving circuit 206 sequentially selects each of column signal processing circuits 205 by sequentially outputting horizontal scanning pulses and delivers the processed signals from each of column

signal processing circuits 205 to horizontal signal line 210. *Kuboi*, ¶[53]; Lebby, ¶161. Output circuit 207 then performs signal processing on the signals sequentially supplied from each column signal processing circuit 205 through horizontal signal line 210. *Kuboi*, ¶[54]. This process is illustrated below:

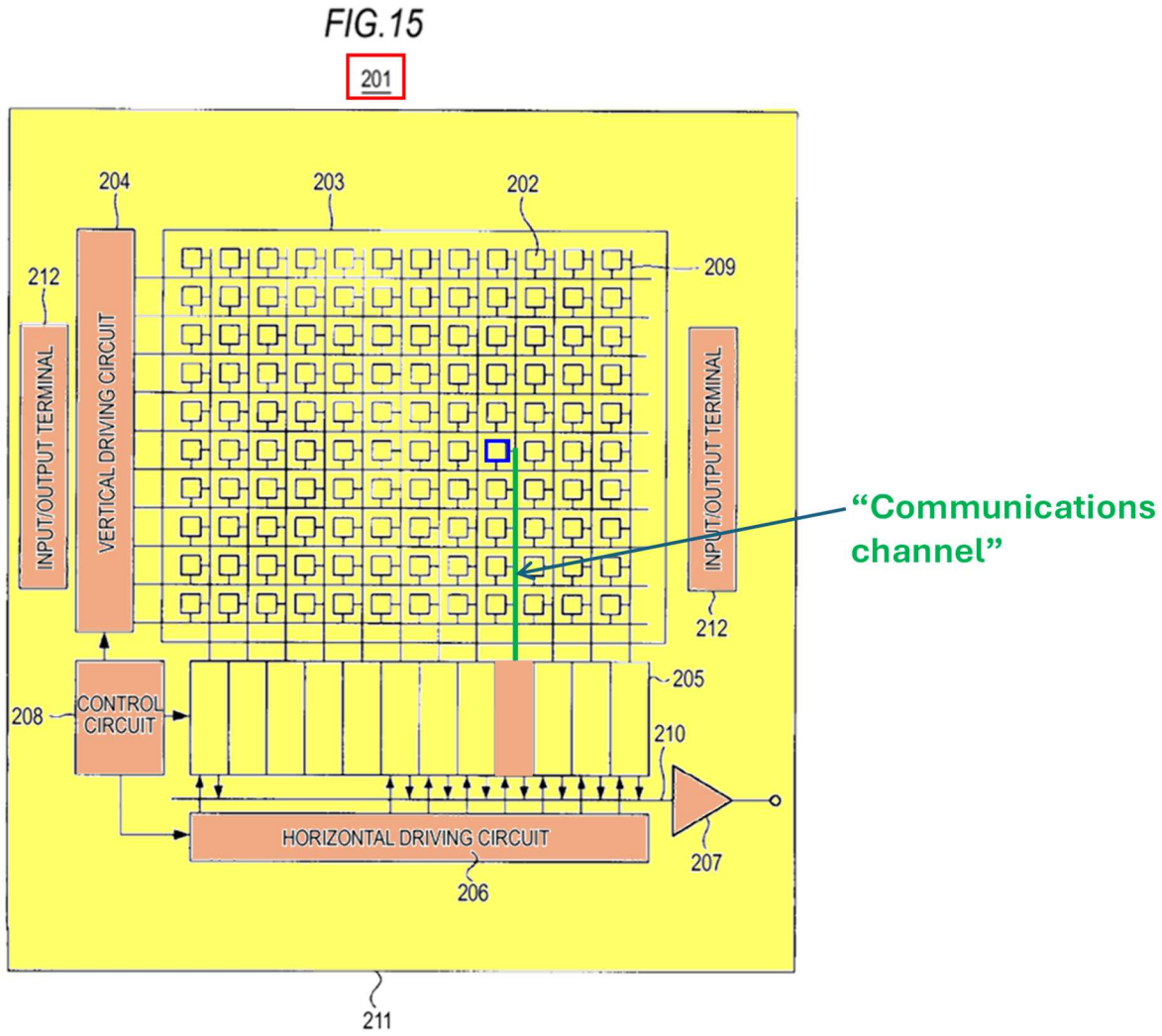
FIG.15



Kuboi, Fig. 15. The process of sequentially selecting each column signal processing circuit 205 by applying scanning pulses (from horizontal driving circuit 206) to a column signal processing circuit 205 to deliver the processed signals from that column signal processing circuit 205 to output circuit 207 constitutes "routing" the processed signals to the output circuit. Lebby, ¶¶161-162.

q. [1n]: "a communication channel on or in said single-chip device, configured to deliver the electrical output from the MSPD to the active electronic circuit."

Kuboi discloses this limitation. Lebby, ¶¶163-164. In particular, the electrical output from photoelectric conversion portion 14 is supplied to column signal processing circuit 205 of the active electronic circuit through a vertical signal line 209 that is on or in imaging device 201. *Kuboi*, ¶[51], Fig. 15; Lebby, ¶163. This is illustrated below:



Kuboi, Fig. 15. Since both photoelectric conversion portions 14 of pixel 11 and column signal processing circuit 205 are on substrate 211 of imaging device 201, a POSITA would have recognized that vertical signal lines 209 (for transmitting signals between the aforementioned components) would also be on or in imaging device 201. Lebby, ¶164; *Kuboi*, ¶¶[48]-[49], [51]. Moreover, as Dr. Lebby

explains, Figure 15 shows vertical signal lines 209 as being on substrate 211. Lebby, ¶164; *supra* FN 4.

3. Claim 2

a. [2]: "The single-chip device of claim 1, in which said active electronic circuit at least partly extends beyond said substrate."

Kuboi discloses or renders obvious this additional limitation. Lebby, ¶¶165-168. As explained for **[1pre(a)]**, in imaging device 201, the claimed "active electronic circuit" (including logic circuits 204-208) include transistor connected together. VI.A.2.a; *Kuboi*, ¶[49]; Ex-1019, 4.

A POSITA would have known that the multiple transistors of the logic circuits of imaging device 201 are connected together using metal interconnects that route signals to and from the transistors. Lebby, ¶166; VI.A.2.a (**[1pre(a)]**); Ex-1020, 9-14, Fig. 2.22. A POSITA would have found it obvious that, although the transistors themselves are formed partly within the substrate, VI.A.4.a, the metal interconnects are formed above the substrate using "above-wafer" steps. Ex-1020, 10-12, 13 (Fig. 2.20 illustrates the "above-wafer" steps in the processing sequence); Ex-1016, 1-3; Lebby, ¶166. For example, in the figure below, metal interconnects (Metal 1, Metal 2, etc.) are formed above the substrate surface. Lebby, ¶166; Ex-1020, 10, 13-14, 25-26.

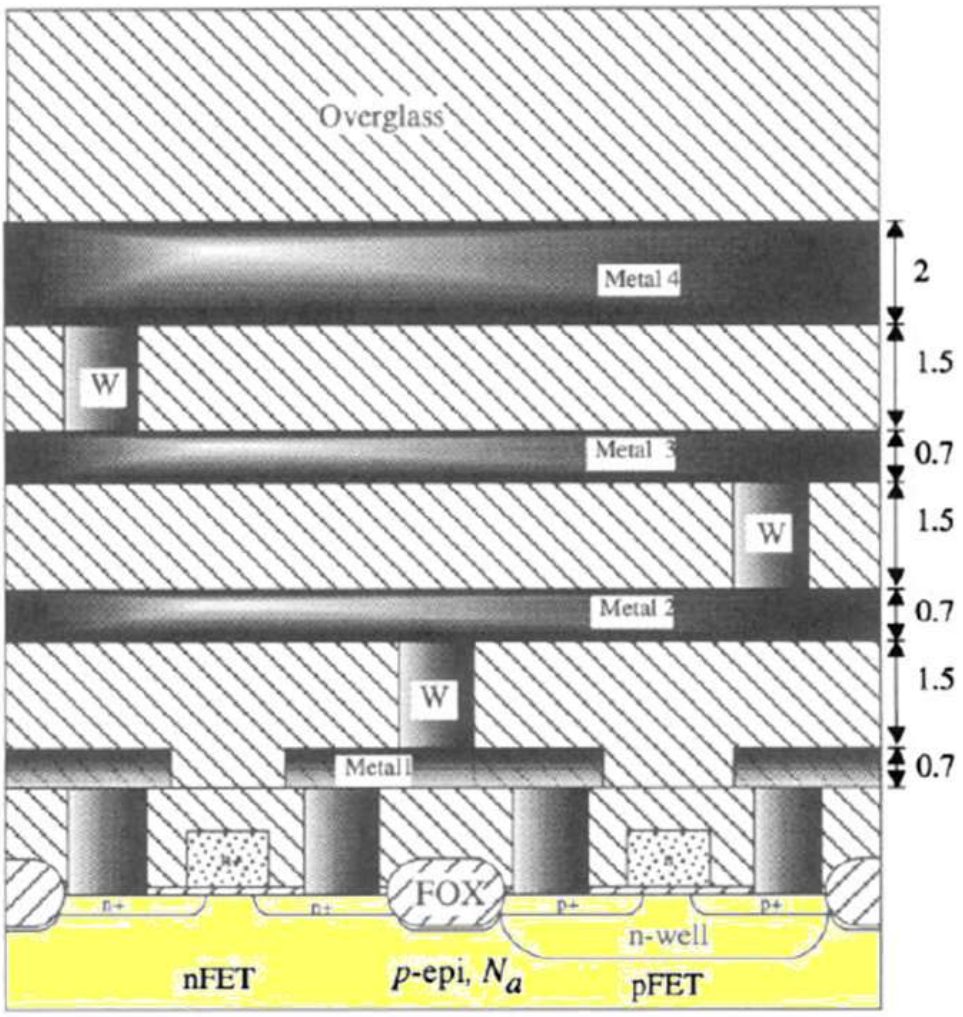


Figure 2.22 Visualization of 4-metal interconnect structure

Ex-1020, 14. It would have been obvious that *Kuboi*'s CMOS logic circuits (of the active electronic circuit) would use interconnects (or wiring) formed above the substrate surface to connect to the transistors of these circuits. Lebby, ¶167. For example, a POSITA would have known that CMOS logic circuits have "many [such] interconnect layers … to ease the layout and signal distribution problems."

Ex-1020, 10. Thus, a POSITA would have found it obvious that wiring that connects to the transistors of the active electronic circuit would at least partly extend beyond substrate 211. Lebby, ¶167.

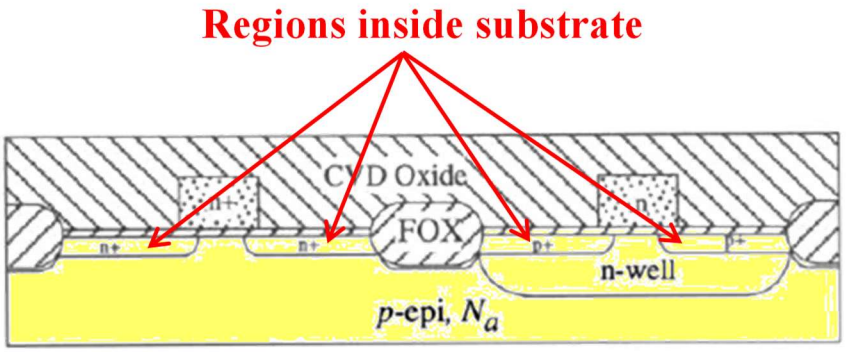
A POSITA would have been motivated to incorporate wiring formed above substrate 211 to form electrical connections to the transistors of *Kuboi*'s logic circuits so that these logic circuits can be formed using conventional CMOS processes. Lebby, ¶168; *see* Ex-1020, 10-14, 25-26. Imaging device 201 already incorporates such above-the-substrate wiring layers. Lebby, ¶168; *see Kuboi*, ¶[62]. For instance, a multilayer wiring layer 32, comprising multiple wiring layers separated by an insulating film 31, is formed on the substrate surface containing pixel transistors. *Kuboi*, ¶[62]. Given the widespread use of wiring layers above the substrate in CMOS logic circuits and *Kuboi*'s existing implementation of such wiring layers, a POSITA would have reasonably expected success in forming above- substrate 211 wiring layers to provide electrical connections to transistors of the active electronic circuit within substrate 211. Lebby, ¶168. Therefore, it would have been obvious to a POSITA that portions of *Kuboi*'s active electronic circuit, including above-the-substrate wiring layers, would at least partly extend beyond substrate 211. Lebby, ¶168.

4. Claim 3

a. [3]: "The single-chip device of claim 1, in which said active electronic circuit is at least partly inside said substrate."

Kuboi discloses this additional limitation. Lebby, ¶¶169-171. As explained for **[1pre(a)]**, in CMOS imaging device 201, the logic circuits of vertical driving circuit 204, column signal processing circuit 205, horizontal driving circuit 206, output circuit 207, and control circuit 208 are the claimed "active electronic circuit." VI.A.2.a; *Kuboi*, ¶[49].

As explained for **[1pre(a)]** and **[2]**, a POSITA would have known that CMOS logic circuits include transistors. Lebby, ¶170; VI.A.2.a, VI.A.3.a; Ex-1020, 9-14; Ex-1019, 4. A POSITA would also have understood that transistors are formed by doping regions of the substrate with selected impurities to create the sources and drains of the transistors. Lebby, ¶¶170-171; Ex-1020, 9-14; Ex-1019, 4-9. This is further illustrated below:



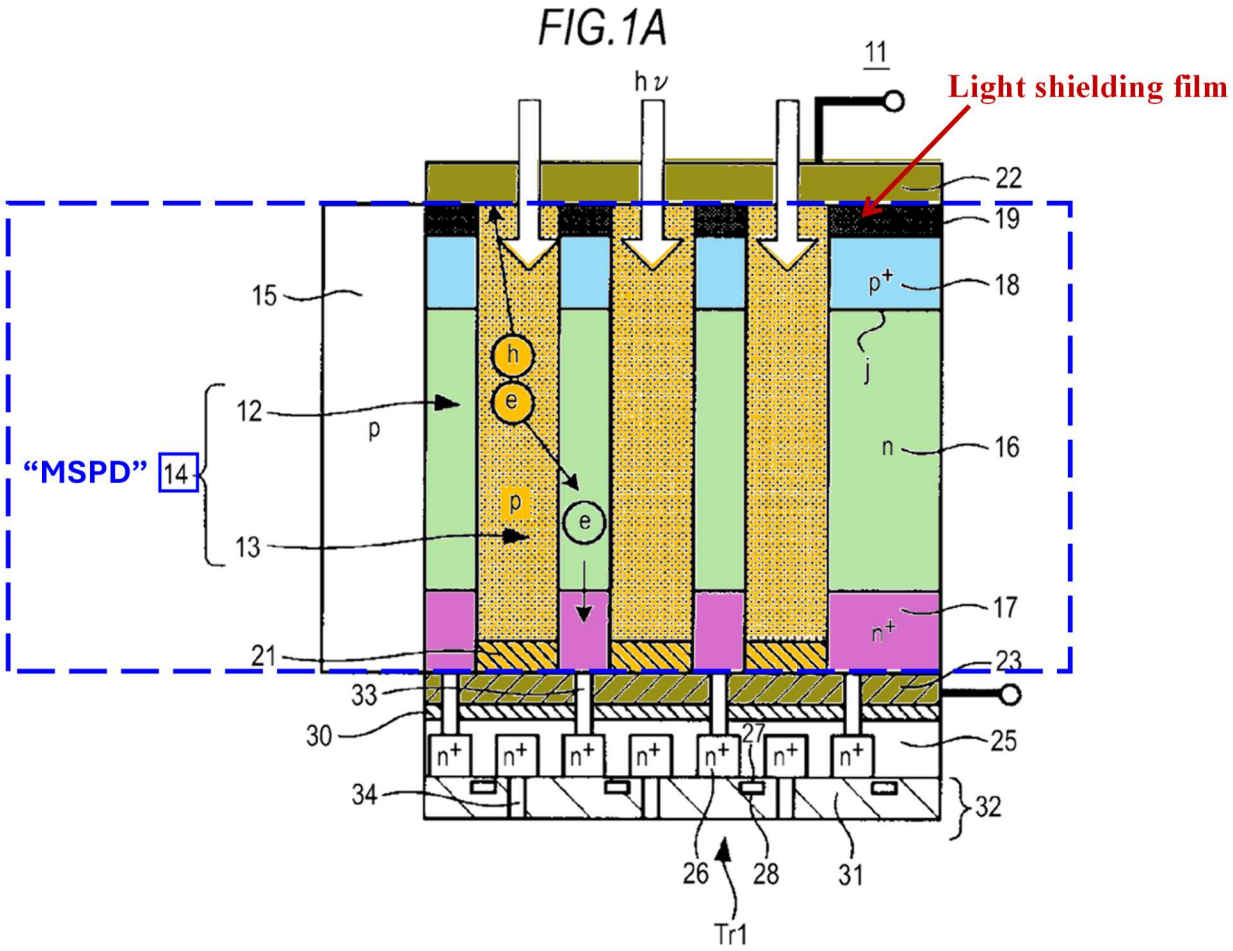
(a) CVD oxide and planarization

Ex-1020, 13. For example, an "n-well is created using a deep ion implant that is diffused deeper into the substrate," and "transistors … are formed by ion implants using the self-aligned scheme. pFETs are created using a p-type boron implant in which nFET locations are blocked …. Similarly, nFETs require an n-type implant for drain and source regions." Ex-1020, 10; Lebby, ¶171. As Dr. Lebby explains, the doped regions of the transistors in *Kuboi*'s active electronic circuit are thus at least partly inside substrate 211. Lebby, ¶171.

5. Claim 4

a. [4]: "The single-chip device of claim 1, in which said overlying layer is present as a superstrate at one side of said first, intermediate, and second layers, and contains said holes."

Kuboi discloses this additional limitation. Lebby, ¶¶172-173. As explained for **[1c]**, *Kuboi* discloses light shielding film 19 formed on the light incident surface of the semiconductor layer 12 that contains holes that align with the holes in p^+-type region 18 ("first layer"), n-type region 16 ("intermediate layer"), and n^+-type region 17 ("second layer"). VI.A.2.f; *Kuboi*, ¶¶[59], [75]-[76], Fig. 1A. As illustrated below, light shielding film 19 is formed on top of the stacked p^+-type region 18 (P), n-type region 16 (i), and n^+-type region 17 (N), and is therefore a superstrate of the stacked PiN regions. Lebby, ¶172; *Kuboi*, ¶¶[59], [75]-[76], Fig. 1A.



Kuboi, Fig. 1A. Moreover, light shielding film 19 is formed on the light receiving side of semiconductor layer 12, and as discussed for **[1c]**, it contains holes. VI.A.2.f; Lebby, ¶173; *Kuboi*, ¶¶[59], [75]-[76]; Fig. 1A.

6. Claim 7

a. [7]: "The single-chip device of claim 1, further including a layer of a dielectric material that covers the holes and is in the propagation path of said optical input."

Kuboi discloses this additional limitation. Lebby, ¶¶174-178. *Kuboi* refers to dielectric films ("dielectric material") as "insulating films." Lebby, ¶174; *Kuboi*,

¶[59] ("an insulating film such as, for example, a silicon nitride (Si_3N_4) film, a silicon oxide (SiO_2) film, and the like"). A POSITA would have understood that silicon nitride and silicon oxide (SiO_2) are dielectric materials. Lebby, ¶174; Ex-1020, 34-35; Ex-1019, 9, 12; Ex-1009, 5. *Kuboi* discloses that, "an on-chip microlens is formed on the upper electrode 22 which is a transparent electrode with or without color filters disposed therebetween. The color filters are formed on the upper electrode 22 with or without an insulating film disposed therebetween." *Kuboi*, ¶¶[63], [73], [146].

In addition, a POSITA would have understood that an "insulating film" disposed between the microlens and the color filter of a CMOS image sensor would be made of a dielectric material to provide a suitable surface for microlens formation. Lebby, ¶175. For example, as shown below, Ex-1027 describes a CMOS image sensor with a color filter and microlens formed over each photodiode on a substrate. Ex-1027, 2-3.

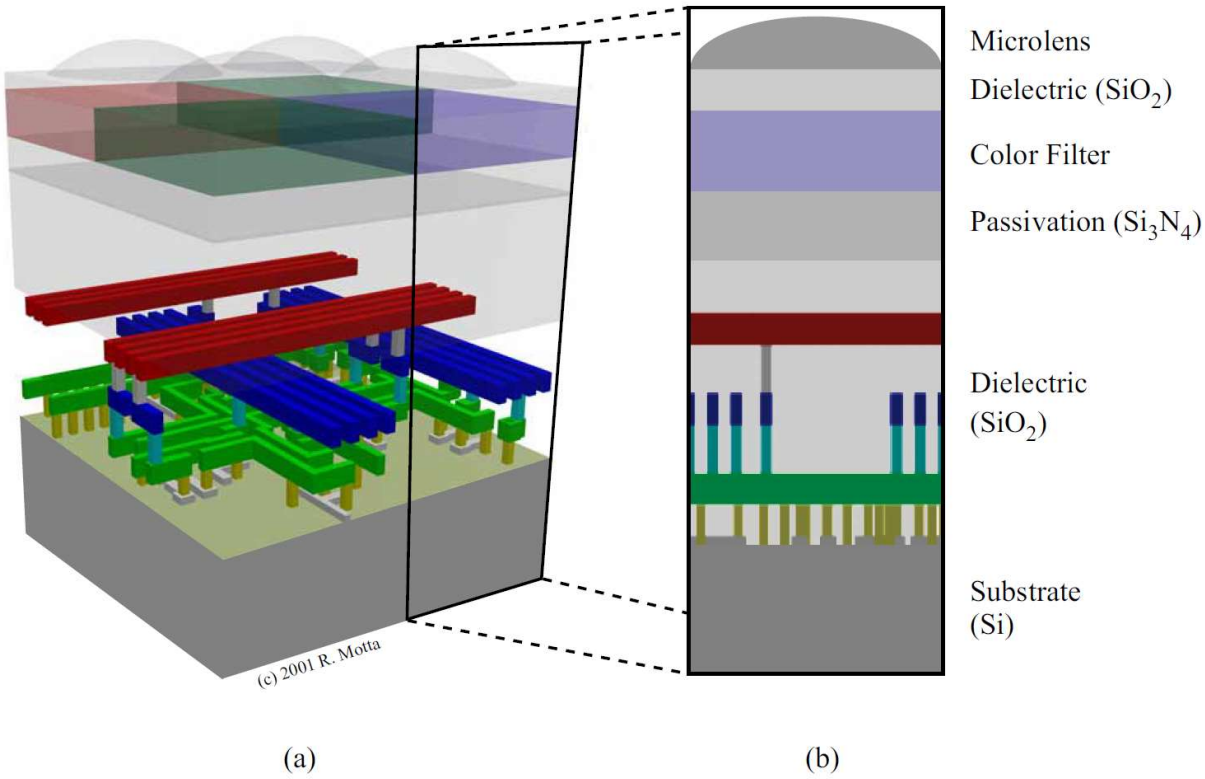
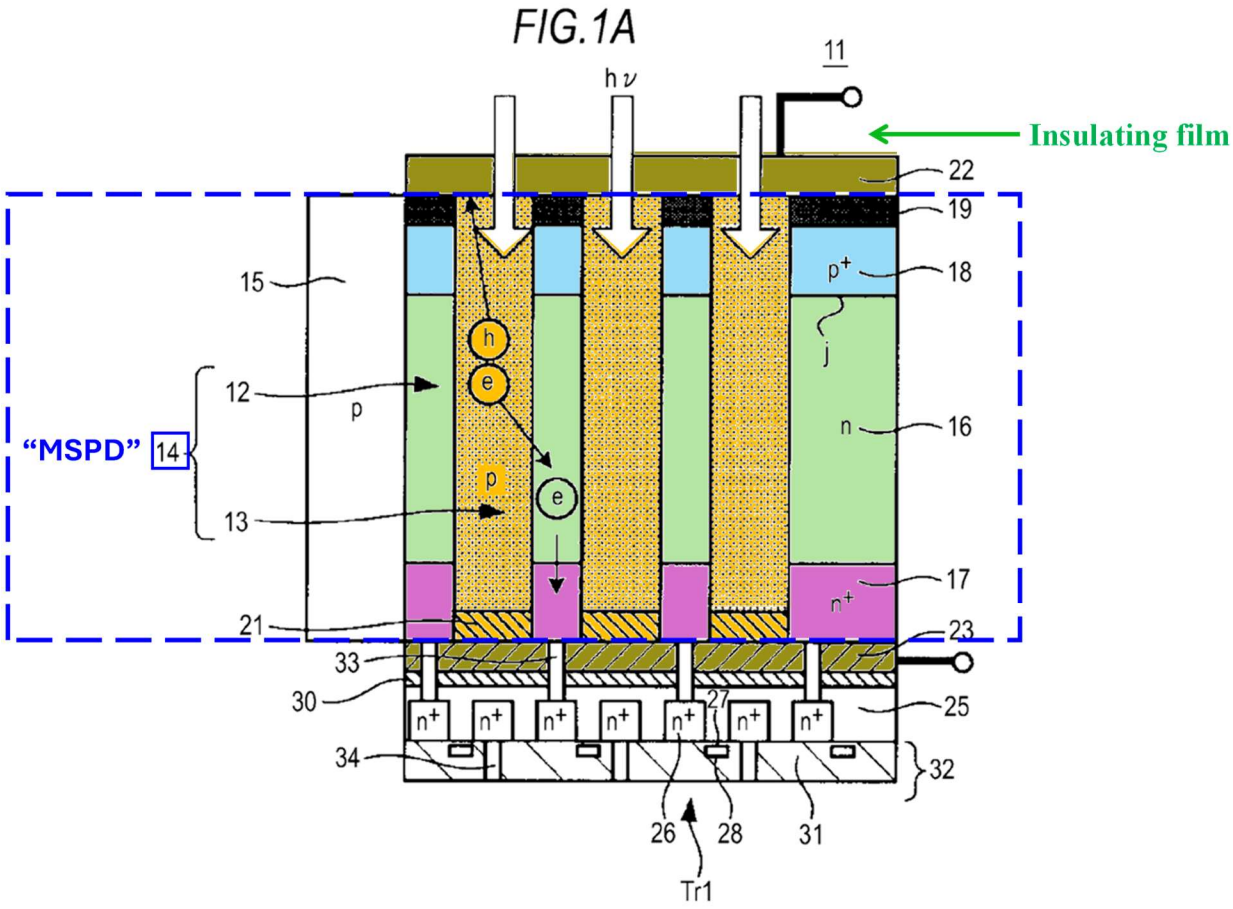


Fig. 1. (a). Three-dimensional (3D) structure of a typical four-pixel unit cell of a CMOS image sensor with a red-green-green-blue Bayer color filter array. (b) Single pixel side view, including the microlens, color filter, passivation layer, dielectric layers, metal interconnects, and silicon substrate.

Ex-1027, 3. A dielectric layer of silicon oxide is formed between the color filter and the microlens to "provide[] a suitable surface for microlens formation." Ex-1027, 4; Lebby, ¶176. Thus, in addition to *Kuboi*'s express disclosure, a POSITA would have understood that *Kuboi*'s insulating film positioned between the color filter and on-chip microlens is an insulating film made of a "dielectric material," as claimed. Lebby, ¶176; Ex-1012, 4 (describes a dielectric tunnel positioned between the microlens and the photodetector and illustrates this

dielectric tunnel in Figure 4); Ex-1033, 2-5 (explains that the microlens is typically constructed on a dielectric layer to ensure signal integrity).

Since light ("optical input") passing through the on-chip microlens to enter photoelectric conversion films 13 of pixel 11 would traverse the dielectric insulating film (positioned between the color filter and upper electrode 22), this insulating film "is in the propagation path of said optical input." Lebby, ¶177; *Kuboi*, ¶[64]. This is illustrated below:



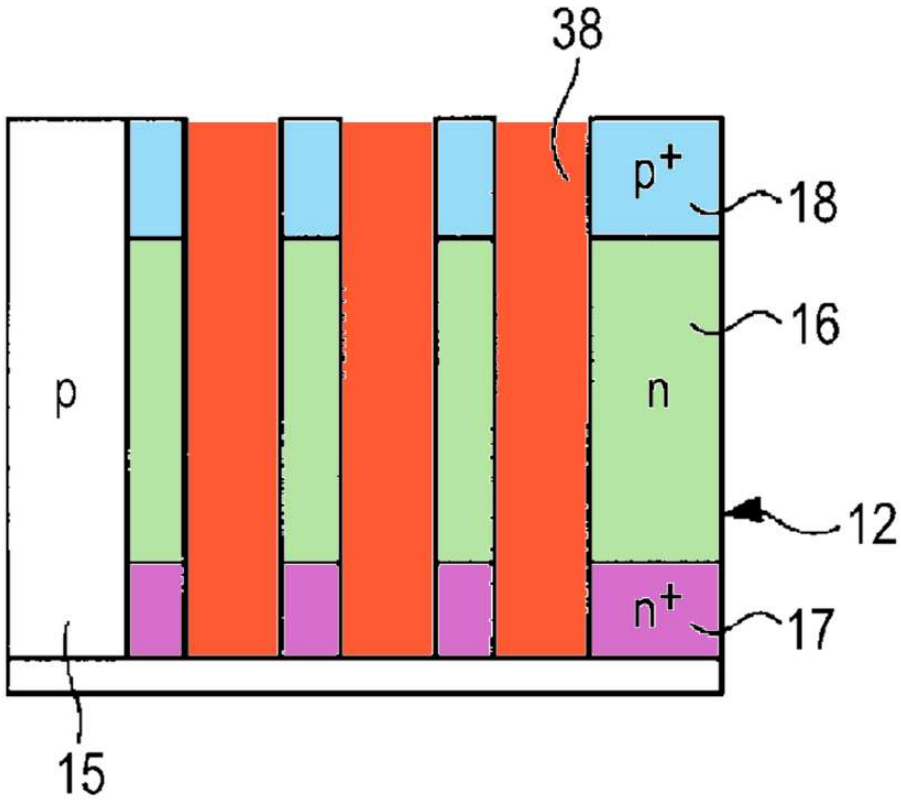
Kuboi, Fig. 1A. A POSITA would have recognized that an insulating film positioned in such a location would cover the holes in semiconductor substrate 12 through which films 13 extend. Lebby, ¶178.

7. Claim 9

a. [9]: "The single-chip device of claim 1, in which said holes are present in said intermediate layer."

Kuboi discloses this additional limitation. Lebby, ¶¶179-180. As explained for **[1c]**, after n^+-type region 17, n-type region 16, and p^+-type region 18 are formed on the semiconductor layer 12, "vertical hole[s] 38" "extending from the p^+-type … region 18 to the n^+-type … region [17] [are] formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching." *Kuboi*, ¶¶[71]-[72]; VI.A.2.f; Lebby, ¶179. Vertical holes 38 are shown below:

FIG.4B



Kuboi, Fig. 4B. Accordingly, in *Kuboi*, holes 38 are present in n-type region 16, which is the claimed "intermediate layer." Lebby, ¶180; VI.A.2.d (**[1a]**); *Kuboi*, ¶¶[71]-[72], Fig. 4B.

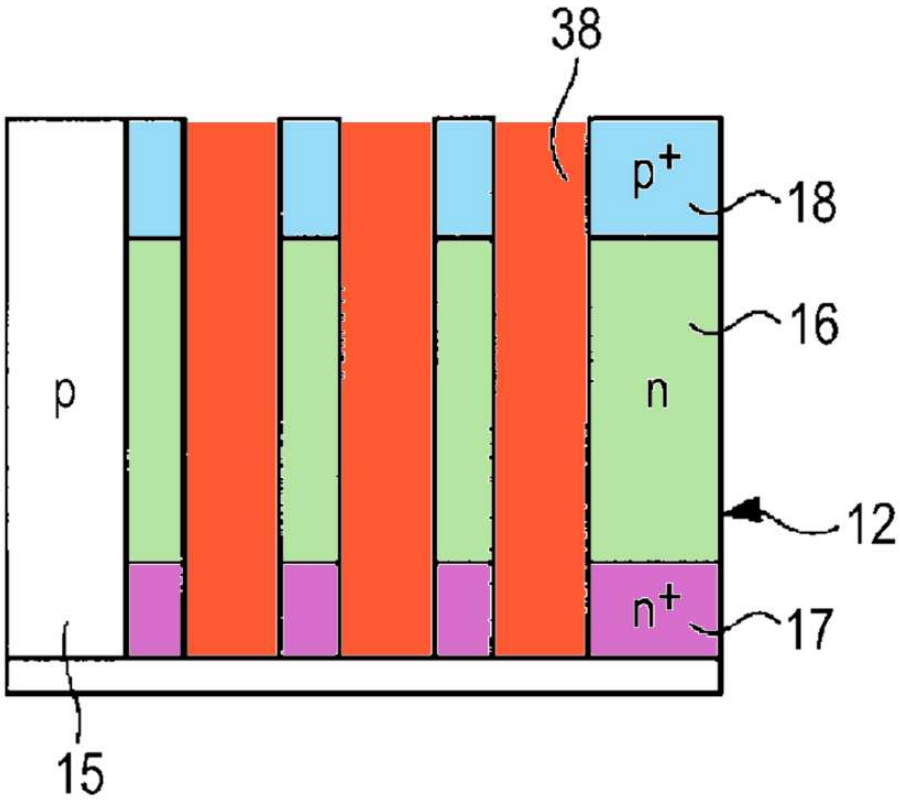
8. Claim 10

a. [10]: "The single-chip device of claim 1, in which said holes are present in said intermediate layer as well as in at least one of the first and second layers."

Kuboi discloses this additional limitation. Lebby, ¶¶181-182. As explained for **[1c]** and **[9]**, "vertical hole[s] 38" "extending from the p^+-type … region 18 to

the n^+-type … region [17] [are] formed in a region of the semiconductor layer 12." *Kuboi*, ¶¶[71]-[72]; VI.A.2.f, VI.A.7.a; Lebby, ¶181. These vertical holes 38 are shown below:

FIG.4B



Kuboi, Fig. 4B. Accordingly, holes 38 are present in n-type region 16 ("intermediate layer"), p^+-type region 18 ("first layer"), and n^+-type region 17 ("second layer"). Lebby, ¶182; VI.A.2.d **[1a]**), VI.A.2.f (**[1c]**); *Kuboi*, ¶¶[71]-[72], Fig. 4B.

9. Claim 11

a. [11]: "The single-chip device of claim 1, in which said holes are present in each of the first, second, and intermediate layer."

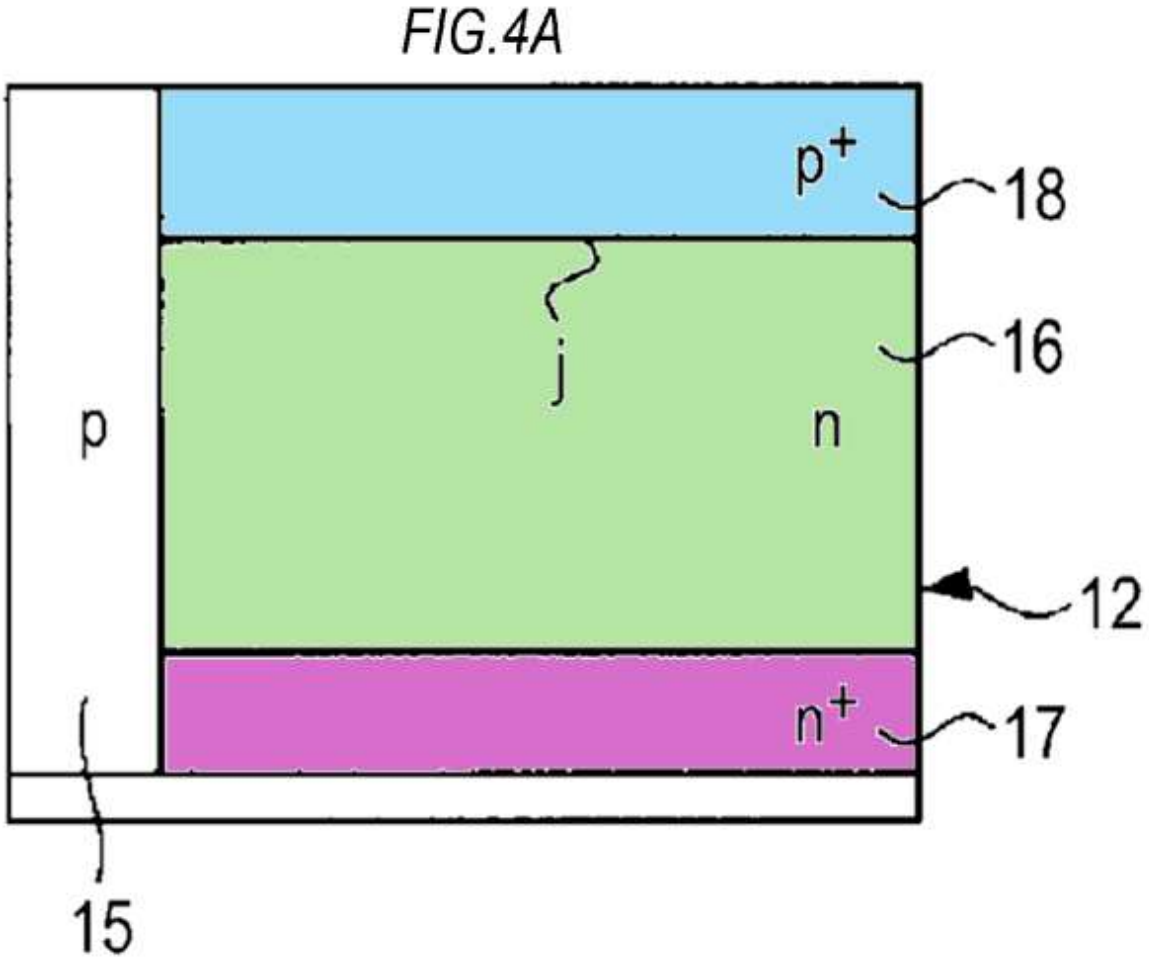
Kuboi discloses this additional limitation. Lebby, ¶183. As explained for **[10]**, *Kuboi*'s holes 38 are present in n-type region 16 ("intermediate layer"), p^+-type region 18 ("first layer"), and n^+-type region 17 ("second layer"). Lebby, ¶183; VI.A.2.d (**[1a]**), VI.A.2.f (**[1c]**), VI.A.8.a (**[10]**); *Kuboi*, ¶¶[71]-[72], Fig. 4B.

10. Claim 12

a. [12]: "The single-chip device of claim 1, in which each of said first and second layers and said intermediate layer has a thickness and at least some of said holes extend through the entire thickness of said intermediate layer and of one of said first layer and second layer and through at least a part of the thickness of the other one of said first and second layers."

Kuboi discloses this additional limitation. Lebby, ¶¶184-188. *Kuboi* discloses that, during manufacturing, semiconductor layer 12 is implanted with impurities to form (in order) n^+-type region 17 ("first layer"), n-type region 16 ("intermediate layer"), and p^+-type region 18 ("second layer"). *Kuboi*, ¶¶[55]-[56],

[71]; VI.A.2.d (**[1a]**); Lebby, ¶184. *Kuboi* illustrates all three regions in Figure 4A:



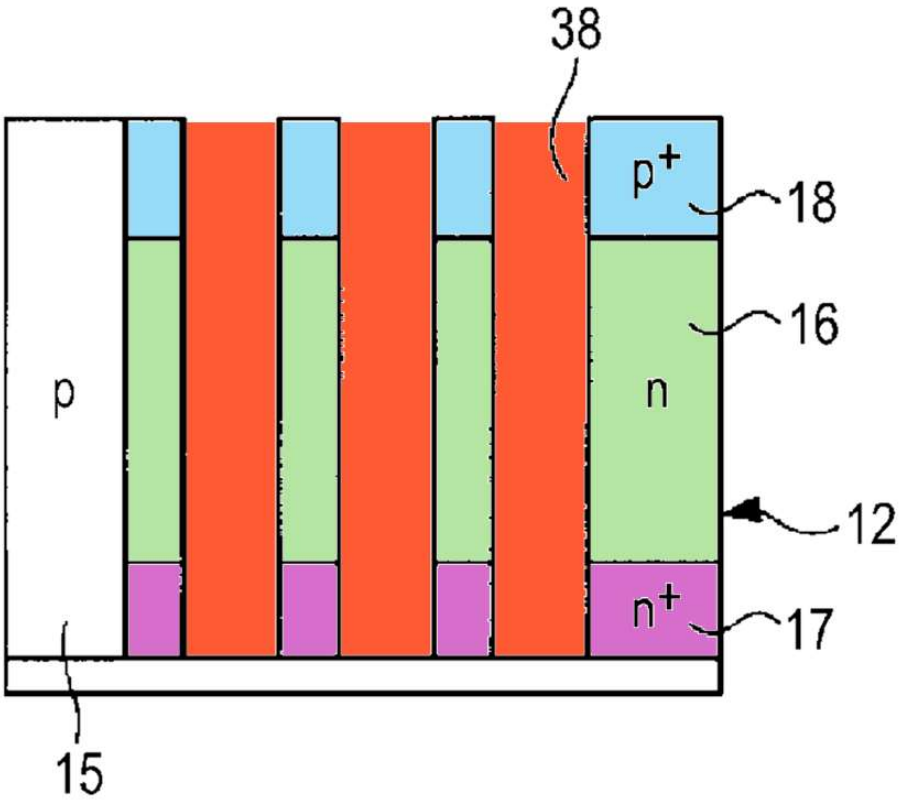
Kuboi, Fig. 4A. As Dr. Lebby explains, a POSITA would have understood that each region has a thickness. Lebby, ¶185; *Kuboi*, Figs. 1A, 4A-4F. This is evident from the figures. Lebby, ¶185.

In addition, *Kuboi* discloses that, in one example, the total thickness (d1) of the semiconductor layer 12 is about 1.4 microns (μm). *Kuboi*, ¶[94]; Lebby, ¶186. A POSITA would have understood that this example makes clear that the regions in the figure would have at least some thickness, even if the figures themselves do

not disclose specific dimensions. Lebby, ¶186. A POSITA would have further understood that when the 1.4-micron thick semiconductor layer 12 is implanted with impurities to form a stacked PiN structure, each of the component regions will have a thickness that together sum to 1.4 microns. Lebby, ¶186.

Kuboi further discloses that, after forming the stacked PiN structure, vertical holes 38 "extending from the p^+-type … region 18 to the n^+-type … region [17]" are dry-etched in semiconductor layer 12. *Kuboi*, ¶¶[71]-[72]; VI.A.2.f (**[1c]**), VI.A.7.a-VI.A.9.a (**[9]-[11]**); Lebby, ¶187. These are shown below:

FIG.4B



Kuboi, Fig. 4B. Accordingly, holes 38 extend through the entire thickness of n-type region 16 ("intermediate layer") and p^+-type region 18 ("first layer") and through at least a part of the thickness of n^+-type region 17 ("second layer"). Lebby, ¶188; VI.A.2.d (**[1a]**), VI.A.2.f (**[1c]**); *Kuboi*, ¶¶[71]-[72], Fig. 4B.

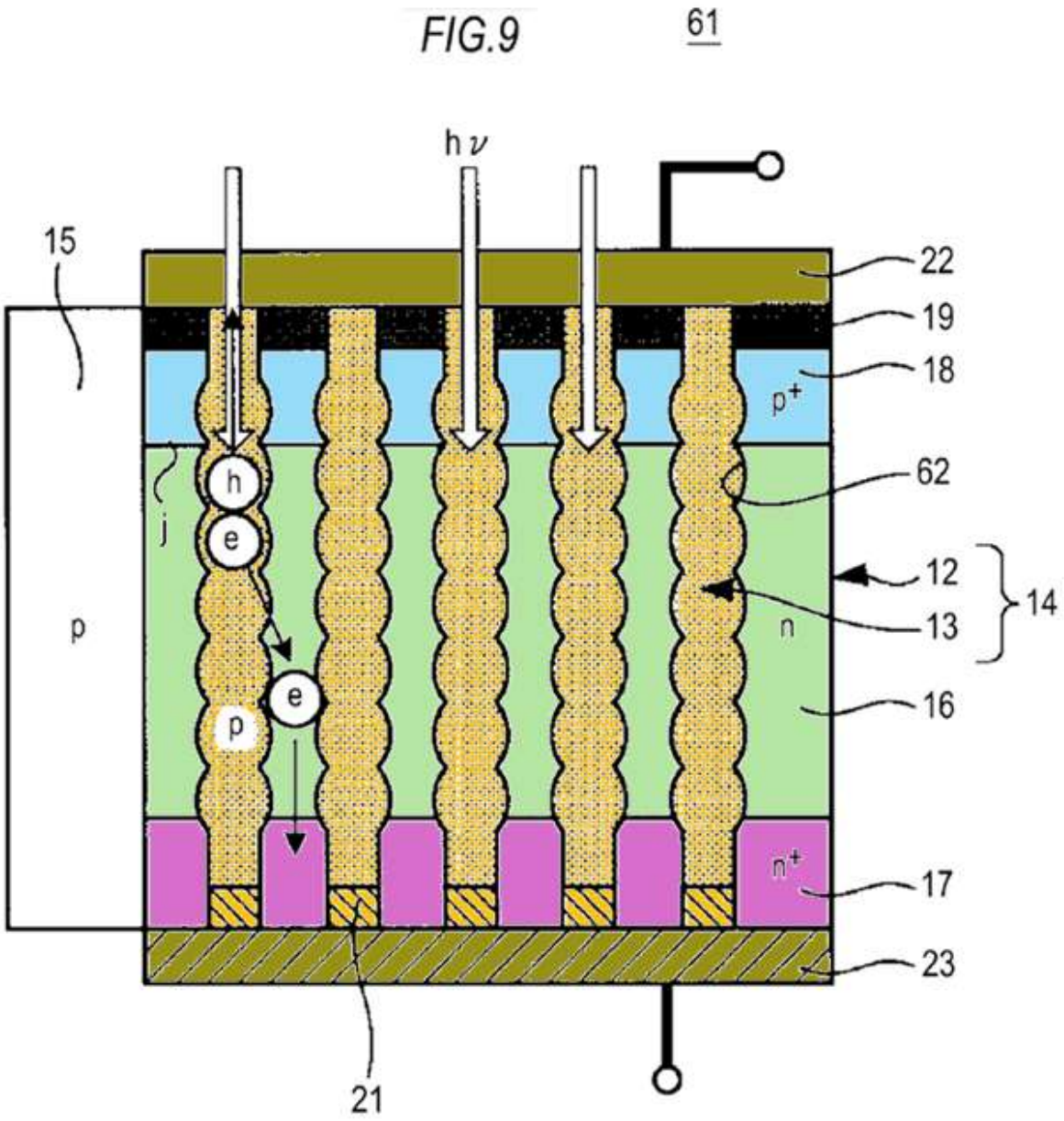
11. Claim 16

a. [16]: "The single-chip device of claim 1, in which at least some of said holes have sidewalls that slope in planes transverse to said layers."

Kuboi renders obvious this additional limitation. Lebby, ¶¶189-193. As explained for **[1c]**, "vertical hole[s] 38" "extending from the p^+-type … region 18 to the n^+-type … region [17] [are] formed in a region of the semiconductor layer 12 corresponding to one pixel by dry-etching." *Kuboi*, ¶¶[71]-[72]; VI.A.2.f; Lebby, ¶189. *Kuboi* further discloses that, by using "the Bosch process" for dry-etching the holes, "it is possible to form a concavo-convex shape on the lateral walls of the vertical holes 38." *Kuboi*, ¶[72], Fig. 9. These concavo-convex-shaped holes meet the requirements of claim 16. Lebby, ¶189.

Kuboi explains that "[b]y forming the concavo-convex shape, it is possible to increase the area of the interface with the organic photoelectric conversion film formed in a subsequent step and to accelerate the movement of electrons (charges)," which increases light absorption efficiency and improves sensitivity.

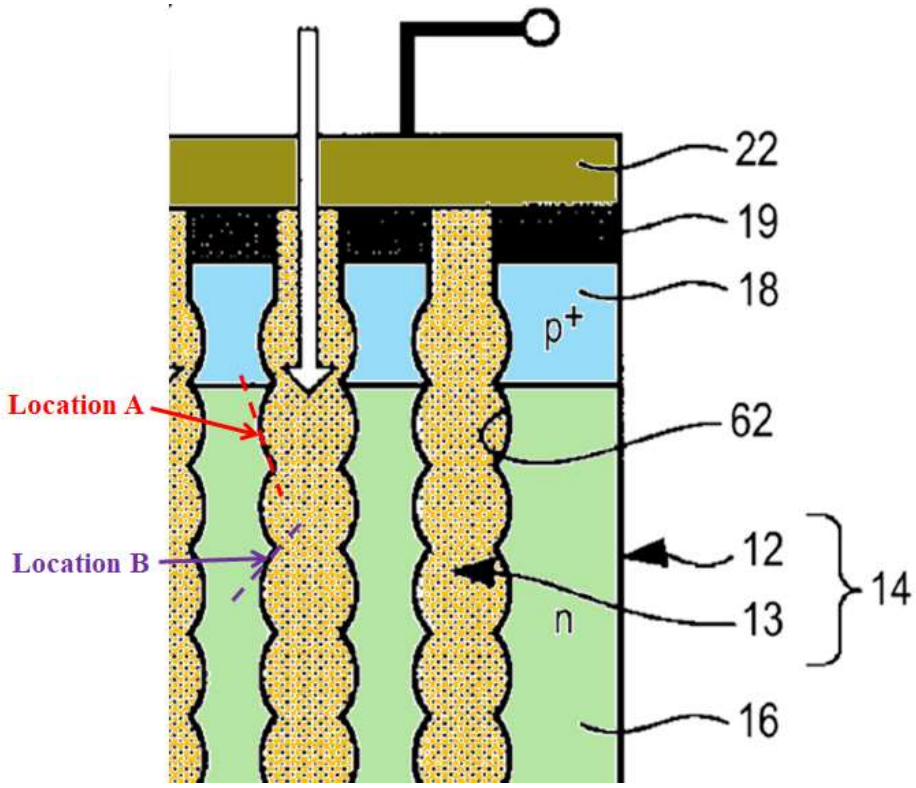
Kuboi, ¶¶[72], [80]; Lebby, ¶190. This concavo-convex shape on the lateral walls of vertical holes 38 is illustrated below:



Kuboi, Fig. 9. Figure 9 depicts photoelectric conversion portion 14, where the Bosch process is employed to create holes 62 with a "concavo-convex shape … at the interface between the semiconductor layer 12 and the organic photoelectric

conversion film 13." *Kuboi*, ¶[137]. The size of the concavo-convex shape can be adjusted in the Bosch process. *Kuboi*, ¶¶[139]-[140]. Organic photoelectric conversion films 13 are subsequently embedded into these holes. *Kuboi*, ¶[139]. According to *Kuboi*, the fabrication process in Figure 9, which includes concavo-convex holes 62, is "basically the same" as that for photoelectric conversion portion 14 in Figure 1A, except that the Bosch process is used to form the holes. *Kuboi*, ¶¶[137], [139]; Lebby, ¶191.

Concavo-convex holes 62 feature sidewalls that slope in planes transverse to the stacked n^+-type region 17, n-type region 16, and p^+-type region 18. Lebby, ¶192. For example, the sidewalls of holes 62 at the locations marked A and B, illustrated below, are sloped in planes parallel to the plane of this paper, which is oriented transversely to the stacked layers. Lebby, ¶192.



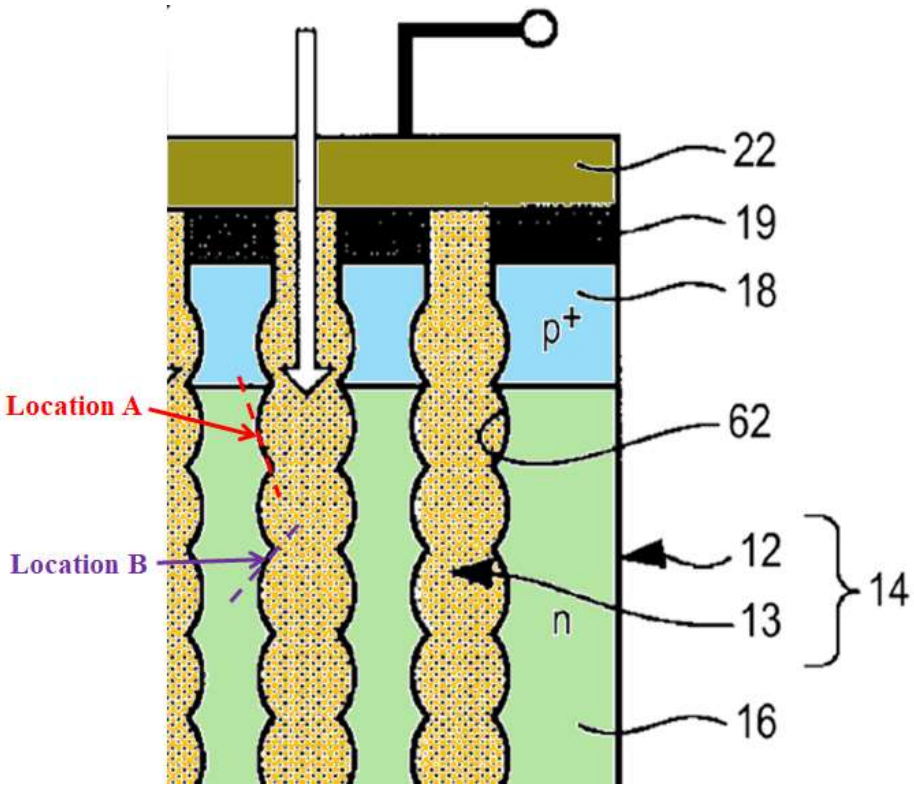
Kuboi, Fig. 9 (cropped).

A POSITA would have been motivated to incorporate concavo-convex holes 62 in photoelectric conversion portion 14 of Figure 1A to enhance electron mobility and thus improve light absorption efficiency and sensitivity of photoelectric conversion portion 14. Lebby, ¶193; *Kuboi*, ¶¶[72], [80], [137], [139]. Since *Kuboi* explicitly states that the Bosch process can be used to create holes with concavo-convex walls in photoelectric conversion portion 14 of Figure 1A, the results would have been entirely predictable and a POSITA would have had a reasonable expectation of success in carrying out this modification. Lebby, ¶193; *Kuboi*, ¶[72].

12. Claim 17

a. [17]: "The single-chip device of claim 1, in which at least some of said holes have sidewalls with plural different slopes along the inside walls of the holes."

Kuboi renders obvious this additional limitation. Lebby, ¶¶194-195. As outlined for [16], a POSITA would have been motivated to integrate concavo-convex holes 62 into photoelectric conversion portion 14 to boost electron mobility, light absorption efficiency, and sensitivity. Lebby, ¶194; VI.A.11.a; *Kuboi*, ¶¶[72], [80], [137], [139]. The same analysis applies here. As shown below, concavo-convex holes 62 feature sidewalls with varying slopes along the inner walls. Lebby, ¶¶194-195.



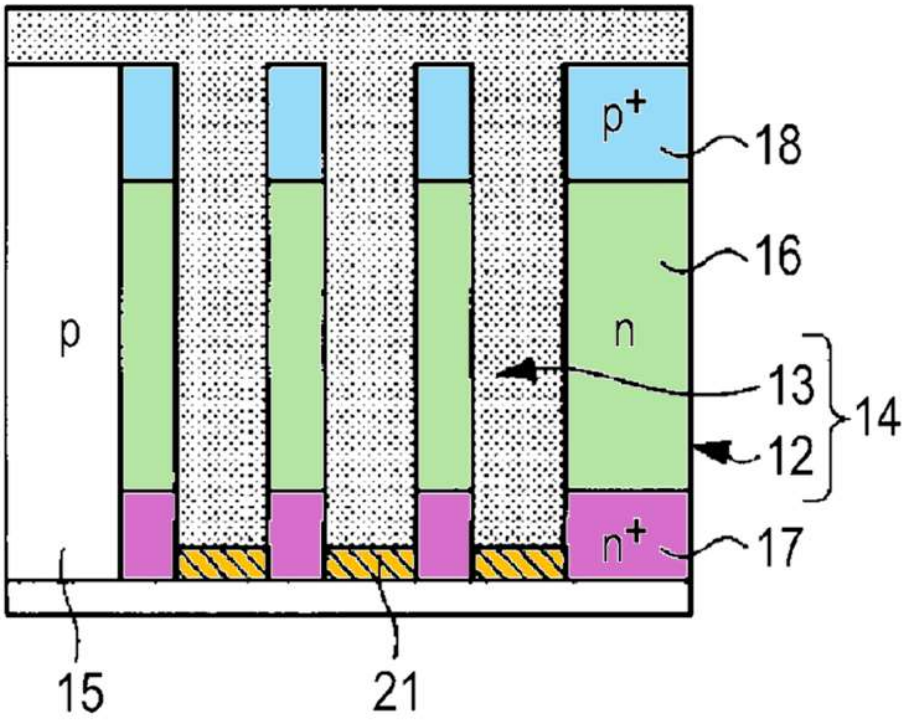
Kuboi, Fig. 9 (cropped). A POSITA would have understood that the sidewalls at locations A and B have different slopes, as required by the claim. Lebby, ¶195.

13. Claim 20

a. [20]: "The single-chip device of claim 1, in which the holes are at least partly filled with a dielectric material."

Kuboi discloses this additional limitation. Lebby, ¶¶196-197. During the manufacturing of *Kuboi*'s pixel, vertical holes 38 extending from the p^+-type region 18 to the n^+-type region 17 are first formed in a region of the semiconductor layer 12. *Kuboi*, ¶¶[71]-[72]; Lebby, ¶196. Then, "an electron blocking film 21 having a thickness of several tens of nm, for example[,] is formed on the bottom portions of the vertical holes 38" by chemical vapor deposition. *Kuboi*, ¶[73], Fig. 4C. Electron blocking film 21 is annotated in the figure below:

FIG.4C



Kuboi, Fig. 4C. Electron blocking film 21 is composed of an insulating material, such as silicon nitride (Si_3N_4) or silicon dioxide (SiO_2). *Kuboi*, ¶[59]. A POSITA would have understood that silicon nitride and silicon dioxide are dielectric materials. Lebby, ¶197; Ex-1020, 34-35; Ex-1019, 9, 12. Thus, the holes of the photoelectric conversion portion 14 "are at least partly filled with a dielectric material," as claimed. Lebby, ¶197.

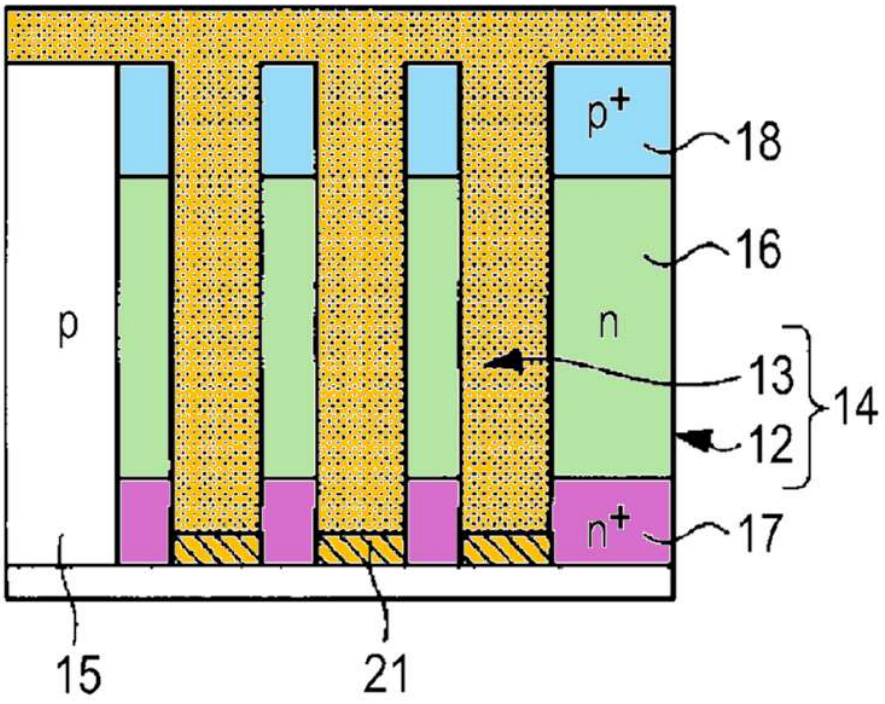
14. Claim 21

a. [21]: "The single-chip device of claim 1, in which the holes are entirely filled with a dielectric material."

Kuboi discloses this additional limitation. Lebby, ¶¶198-203. As detailed for **[20]**, after formation of holes 38, electron blocking film 21 composed of a dielectric material such as silicon nitride (Si_3N_4) or silicon dioxide (SiO_2) is deposited at the bottom portions of holes 38. *Supra* VI.A.13.a; *Kuboi*, ¶¶[71]-[73]; Lebby, ¶198.

As part of the next step of the manufacturing process and as shown below, an organic material is deposited to fill the remaining portions of the holes, thereby forming organic photoelectric conversion films 13 embedded within the hole. *Kuboi*, ¶¶[73], [58], [85], Fig. 4C; Lebby, ¶199.

FIG.4C



Kuboi, Fig. 4C. *Kuboi* discloses that "[a]s the p-type organic material sensitive to a visible light region, perylene-based compounds, phthalocyanine compounds, quinacridone compounds, porphyrin compounds, merocyanine compounds, and the like can be used, for example." *Kuboi*, ¶[58].

A POSITA would have recognized that phthalocyanine compounds, perylene-based compounds, and porphyrin compounds are dielectric materials. Lebby, ¶¶200-201. Multiple prior art references discuss the dielectric properties and behavior of these materials in various optoelectronic devices. Lebby, ¶201 (citing Ex-1021; Ex-1022; Ex-1028; Ex-1034–Ex-1038). For instance, Ex-1021

discusses the dielectric behavior of metal-phthalocyanine (MePc) films used as photoelectric conversion materials in organic solar cells, noting that the "dielectric constant was high at low frequencies and decreas[ed] as the frequency increase[d]." Ex-1021, 3. Thus, both electron blocking film 21 and photoelectric conversion film 13 that together entirely fill the holes of photoelectric conversion portion 14 are dielectric materials.[6] Lebby, ¶¶202-203.

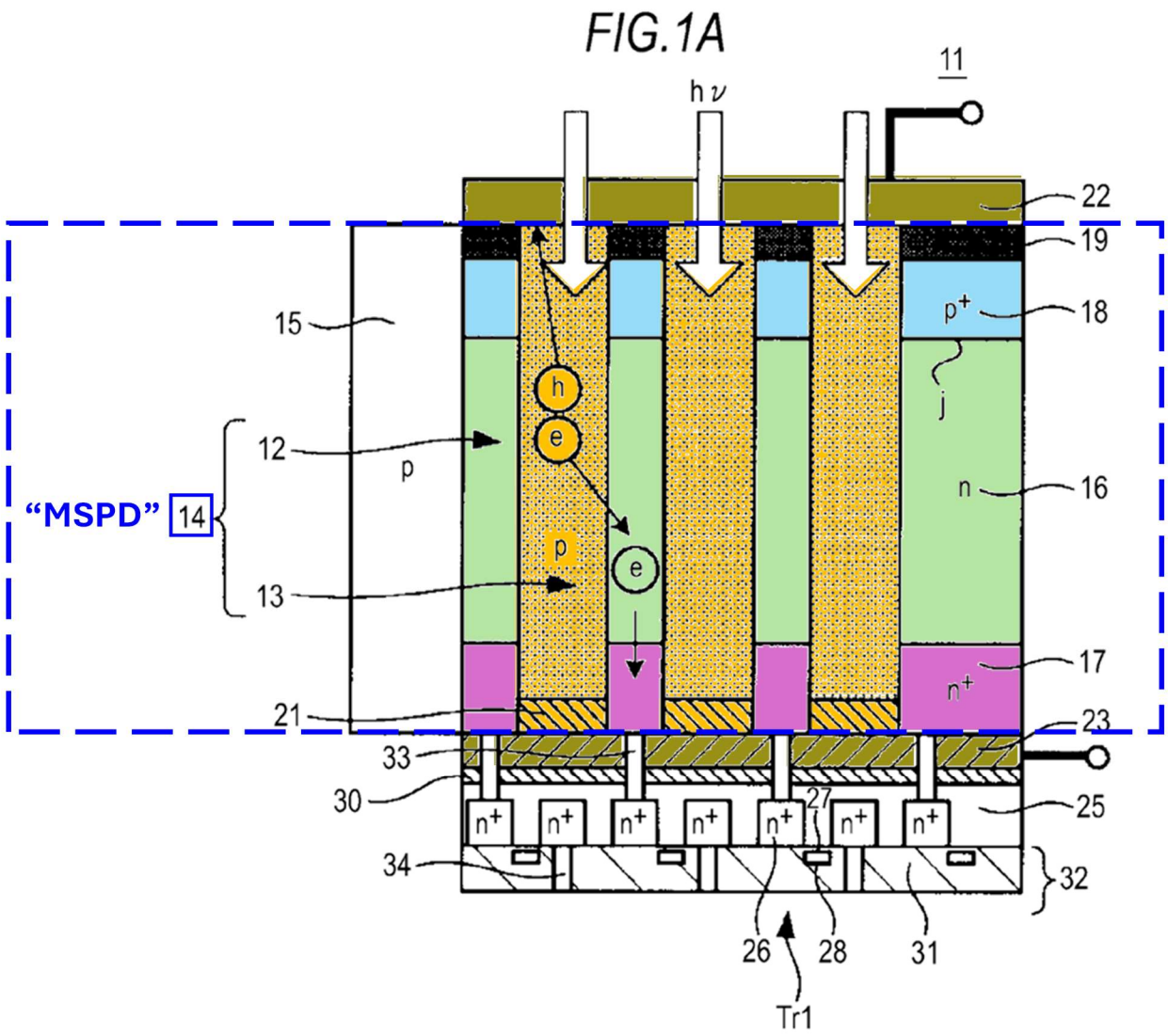
15. Claim 24

a. [24]: "The single-chip device of claim 1, in which said MSPD further comprises ohmic contacts configured for reverse-biasing the MSPD."

Kuboi discloses this additional limitation. Lebby, ¶¶204-207. As detailed for **[1h]**, photoelectric conversion portion 14 includes upper electrode 22 on its upper surface and lower electrode 23 on its lower surface that are configured for reverse-

[6] The '700 Patent acknowledges that a hole filled with a dielectric material can be filled with multiple dielectric materials. '700 Patent, 30:58-61 (disclosing that "holes 1916 can be partially filled, and/or completely filled with another dielectric(s) and/or amorphous semiconductor and can be multiple layers"), 104:40-43 (disclosing that "microstructure holes are passivated and filled fully and/or partially with dielectrics").

biasing photoelectric conversion portion 14. VI.A.2.k; *Kuboi*, ¶¶[60], [64], [77], Fig. 1A; Lebby, ¶204. These electrodes are shown below:



Kuboi, Fig. 1A. Lower electrode 23 "is formed of metal exhibiting ohmic properties." *Kuboi*, ¶[60]. Meanwhile, an indium tin oxide (ITO) film serves as upper electrode 22. *Kuboi*, ¶[60]; Lebby, ¶205.

As Dr. Lebby explains, a POSITA would have understood that an electrode made of ITO establishes ohmic contact and thus comprises ohmic contacts.[7] Lebby, ¶¶206-207; Ex-1023, Abstract ("ITO contact with p-type silicon semiconductor is a robust ohmic contact for Si[-]based optoelectronic devices."); Ex-1024, 3; Ex-1025, 1. As a result, both upper electrode 22 and lower electrode 23 are ohmic contacts, as claimed. Lebby, ¶207.

16. Claim 25

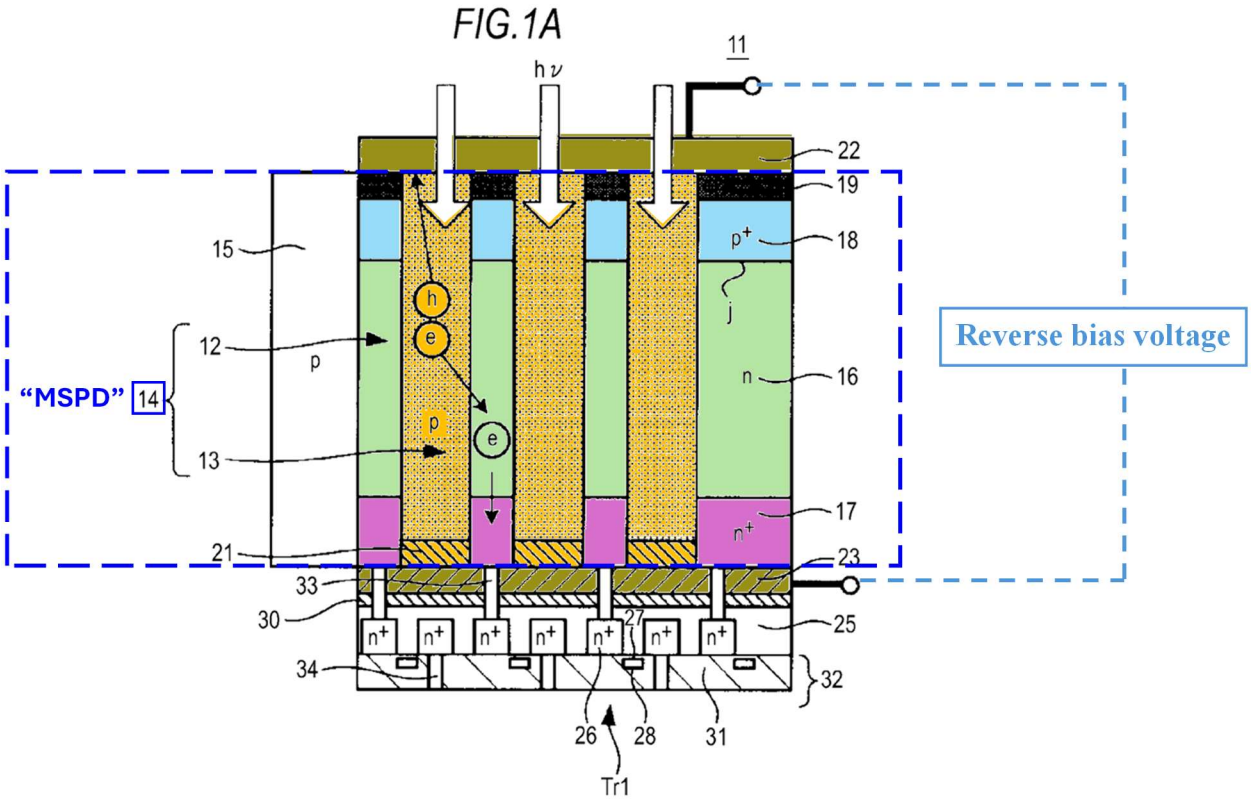
a. [25]: "The single-chip device of claim 1, in which the MSPD further includes ohmic contacts to said first and second layers, at least one of said ohmic contact[s] being through a via in said substrate."

Kuboi renders obvious this additional limitation. Lebby, ¶¶208-216. As explained for **[24]**, upper electrode 22 and lower electrode 23 are ohmic contacts. VI.A.15.a; Lebby, ¶208. These ohmic contacts meet each limitation of claim 25. Lebby, ¶208.

Electrodes 22, 23 make contact with each of the "first and second layers," as claimed. Lebby, ¶209. Upper electrode 22 is formed over the entire upper surface

[7] The '700 Patent acknowledges that ITO makes ohmic contact. '700 Patent, 39:15-21 (explaining that an "ohmic contact" can include a "transparent conducting metal oxide such as indium tin oxide (ITO)").

of photoelectric conversion portion 14 on top of light shielding film 19, which is made of tungsten. *Kuboi*, ¶¶[59]-[60], [77]; Lebby, ¶209.



Kuboi, Fig. 1A. A POSITA would have understood that tungsten is an electrically conductive material. Lebby, ¶210; Ex-1019, 21-22 (discussing the use of tungsten as the first level metal and contact plugs of IC devices); Ex-1020, 14-15.

Consequently, upper electrode 22 makes ohmic contact with p^+-type region 18. Lebby, ¶210. Lower electrode 23 is formed over the entire lower surface of photoelectric conversion portion 14, covering the back surface of n^+-type region 17. *Kuboi*, ¶¶[59]-[60], [77], Fig. 1A; Lebby, ¶210. Therefore, lower electrode 23 makes ohmic contact with n^+-type region 17. Lebby, ¶210.

Kuboi further teaches and renders obvious that "at least one of said ohmic contact[s] [is] through a via in said substrate," as claimed. Lebby, ¶¶211-216. In imaging device 201, pixels 11 (with photoelectric conversion portion 14) and the peripheral circuit portion are formed on substrate 211. *Kuboi*, ¶¶[48], [78]; VI.A.2.b (**[1pre(b)]**). Subsequently, a different substrate with pixel transistors Tr1 and lower electrode 23 formed on its top surface is bonded to the lower surface of substrate 211. *Kuboi*, ¶¶[70], [78]; *see Kuboi*, Fig. 15. These two substrates are bonded such that the photoelectric conversion portions 14 on substrate 211 connect to the n-type charge accumulation regions 26 of corresponding pixel transistors Tr1 via conductors 33 that penetrate through lower electrode 23. *Kuboi*, ¶¶[48], [62]; Lebby, ¶211.

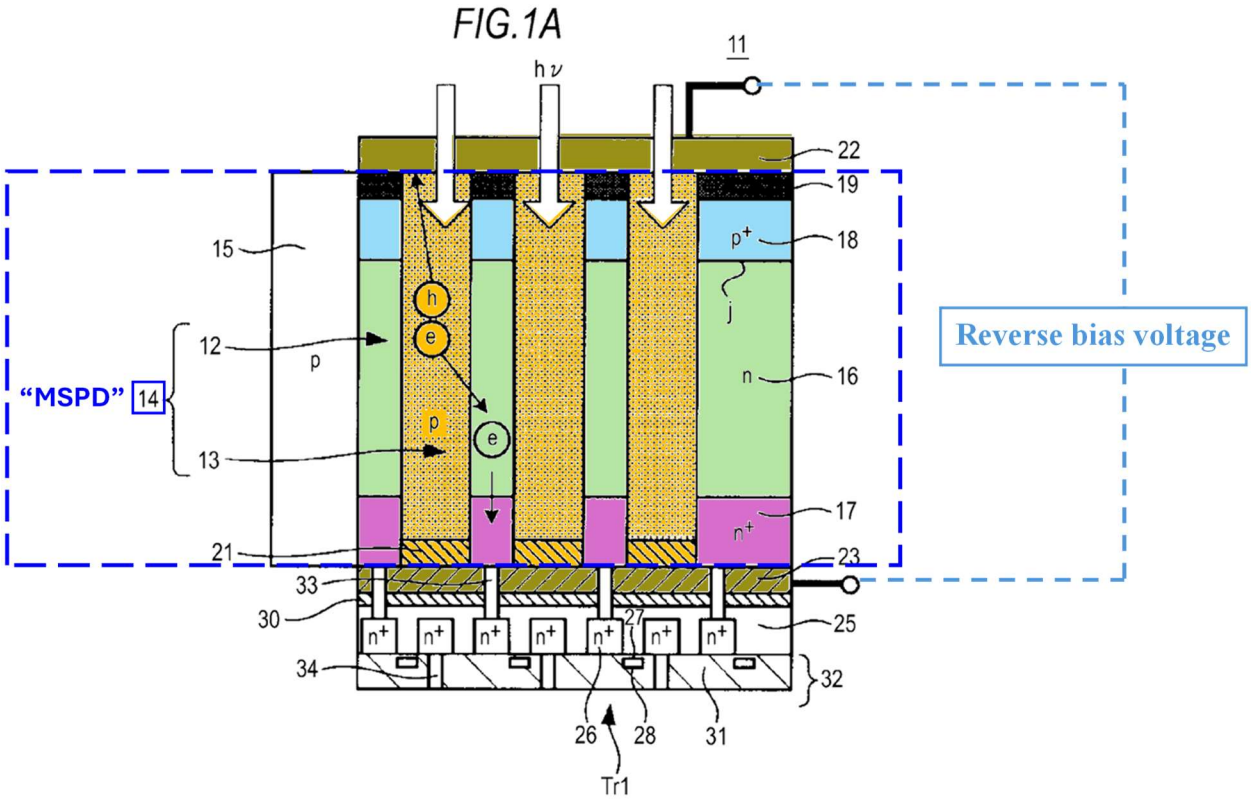
A POSITA would have been motivated to fabricate photoelectric conversion portions 14 and pixel transistors on substrate 211. Lebby, ¶212. Given *Kuboi*'s approximately 1.4 μm x 1.4 μm pixel size, *e.g.*, *Kuboi*, ¶¶[94], [122], [145], a POSITA would have recognized that challenges in spatially aligning conductors 33 with photoelectric conversion portions 14 during substrate bonding would reduce the yield of the bonding process. Lebby, ¶212; *see* Ex-1039, 5-6, 8-9, 11-13. A POSITA would have understood that fabricating photoelectric conversion portions 14 and pixel transistors on the same substrate 211 would eliminate the need for

aligning electrodes 33 and thereby increase yield. Lebby, ¶212; *see, e.g.*, *Shinohara*, ¶¶[58], [81].

As Dr. Lebby explains, integrating signal processing circuits on the same substrate as photodetectors was well known and beneficial to lower cost and improve fabrication reliability. Lebby, ¶213; Ex-1029, 1; Ex-1030, 1-2. Consequently, a POSITA would have found it obvious to fabricate photoelectric conversion portions 14 and pixel transistors Tr1 on substrate 211 to simplify fabrication and reduce costs. Lebby, ¶213. Additionally, methods for fabricating photoelectric conversion portions and pixel transistors on the same substrate were well established.[8] *See Shinohara*, ¶¶[68]-[89]. Thus, a POSITA would have had the motivation, requisite skill, and reasonable expectation of success in fabricating photoelectric conversion portions 14 and pixel transistors on substrate 211. Lebby, ¶213.

When the pixel transistors Tr1 are fabricated on substrate 211, as illustrated below, lower electrode 23 is positioned within substrate 211. Lebby, ¶214.

[8] The ’700 Patent acknowledges that integrating photodetectors with signal processing circuits on the same substrate was a common practice to reduce costs and enhance performance. ’700 Patent, 28:50-62, 32:44-61 47:7-18; Lebby, ¶213.



Kuboi, Fig. 1A.

As explained for **[1h]**, a reverse bias is applied to photoelectric conversion portion 14 via upper and lower electrodes 22, 23. VI.A.2.k. A POSITA would have understood that an electrical connection (to apply the "necessary voltage" for biasing, *see Kuboi*, ¶[64]) to lower electrode 23 positioned within substrate 211 is made using "vias." Lebby, ¶215; *see* Ex-1020, 13 (Fig. 2.21), 18; Ex-1018, 7 (defining "via" as "a hole in the insulator between two metal layers on a multilayer integrated circuit that is etched and filled with a conducting material so that the two metal layers are electrically connected").

In addition, a POSITA would have also been motivated to implement vias in substrate 211 for electrical connection to lower electrode 23 so that a "necessary voltage" can be applied to this electrode for biasing photoelectric conversion portion 14. Lebby, ¶216; *see Kuboi*, ¶[64]. In *Kuboi*, conductors 33 extend through vias on semiconductor region 25 of the substrate to interconnect the pixel transistors to photoelectric conversion portions 14. Lebby, ¶216; *see Kuboi*, ¶[62], Fig. 1A. Given that "vias" are conventional components commonly used in similar devices for electrical connections through substrates and that *Kuboi* already incorporates electrical connections through the substrate, a POSITA would have also had a reasonable expectation of success in using "vias" through substrate 211 to provide electrical connection to lower electrode 23. Lebby, ¶216. Therefore, it would have been obvious to a POSITA that, in *Kuboi*, electrical contact to lower electrode 23 will be made through a "via," as claimed. Lebby, ¶216.

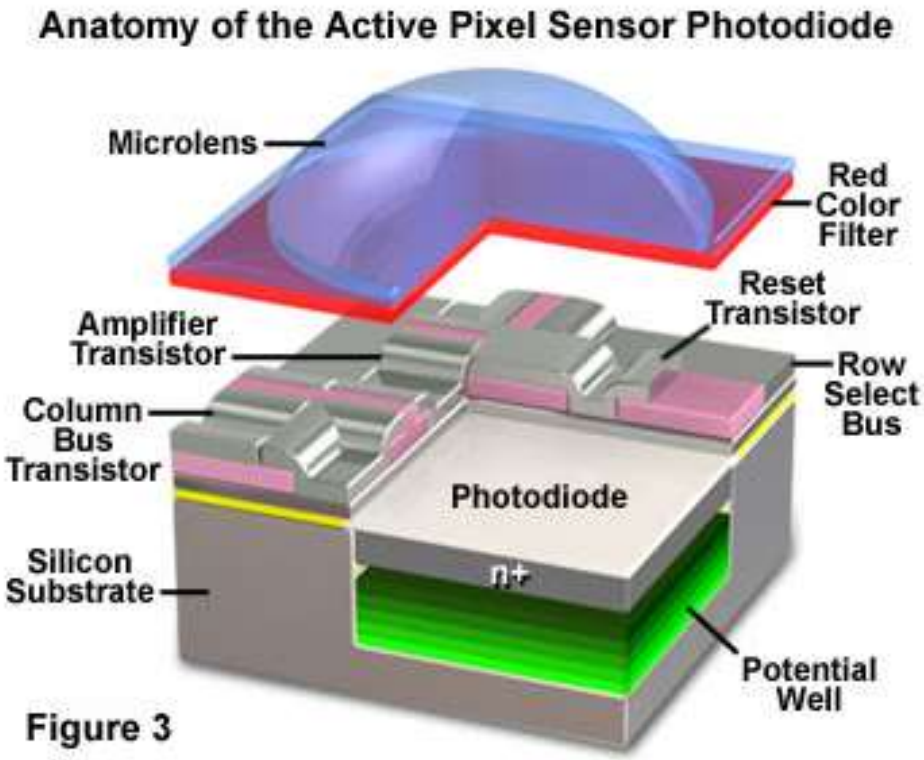
17. Claim 26

a. [26a]: "The single-chip device of claim 1, further comprising a light guide to said MSPD for directing said optical input thereto,"

Kuboi discloses this additional limitation. Lebby, ¶¶217-221. *Kuboi* discloses that, although not depicted in the drawings, "an on-chip microlens" ("light guide") is formed on upper electrode 22, allowing light to pass through this

microlens to reach photoelectric conversion films 13 of photoelectric conversion portion 14, where the light undergoes photoelectric conversion. *Kuboi*, ¶¶[63]-[64].

A POSITA would recognize that the on-chip microlens is a light guide, directing light to the photoelectric conversion portion 14. Lebby, ¶218. For instance, Ex-1015 describes a CMOS image sensor with a two-dimensional array of photodiodes (or pixels) with a microlens formed over each photodiode. Ex-1015, 2-4. This is illustrated below:

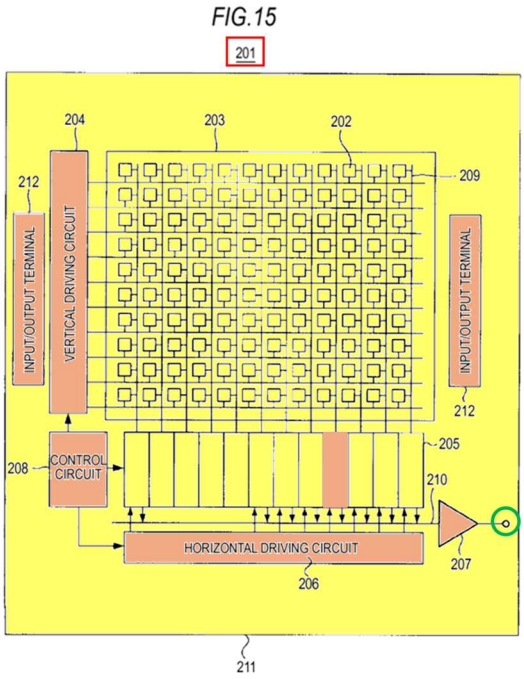


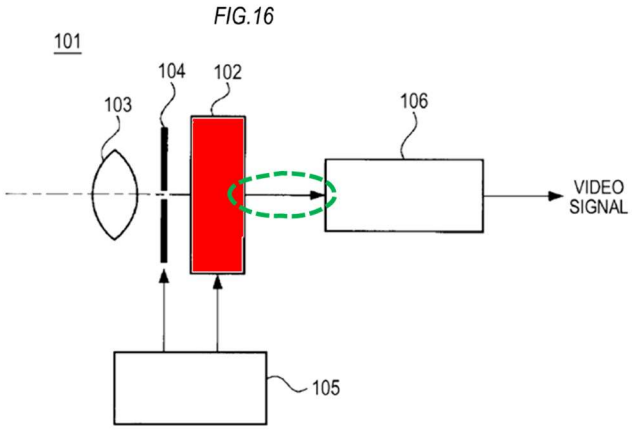
Ex-1015, Fig. 3. The microlens "serves to focus incident light directly into the photosensitive area of the photodiode." Ex-1015, 3. As Dr. Lebby explains, this is

consistent with other prior art and Patent Owner's infringement contentions in the parallel litigation. Lebby, ¶¶219-221 (citing Ex-1027; Ex-1040; Ex-1041). As a result, a POSITA would have understood that *Kuboi*'s on-chip microlens operates as a light guide that directs light to photoelectric conversion portion 14. Lebby, ¶220.

b. [26b]: "and electrical contacts from the active electronic circuit configured to carry said processed output out of the single-chip device."

Kuboi discloses and renders obvious this additional limitation. Lebby, ¶¶222-224. As explained for **[1pre(a)]**, the "active electronic circuit" of imaging device 201 includes circuits 204-208. VI.A.2.a; *Kuboi*, ¶¶[48]-[49]. Output circuit 207 "outputs the processed signals" from imaging device 201. *Kuboi*, ¶[54]. *Kuboi* discloses that its imaging device (labelled 102 in Figure 16) can be integrated into various apparatuses (e.g., cameras, mobile phones) with an external signal processing circuit 106, as illustrated below:





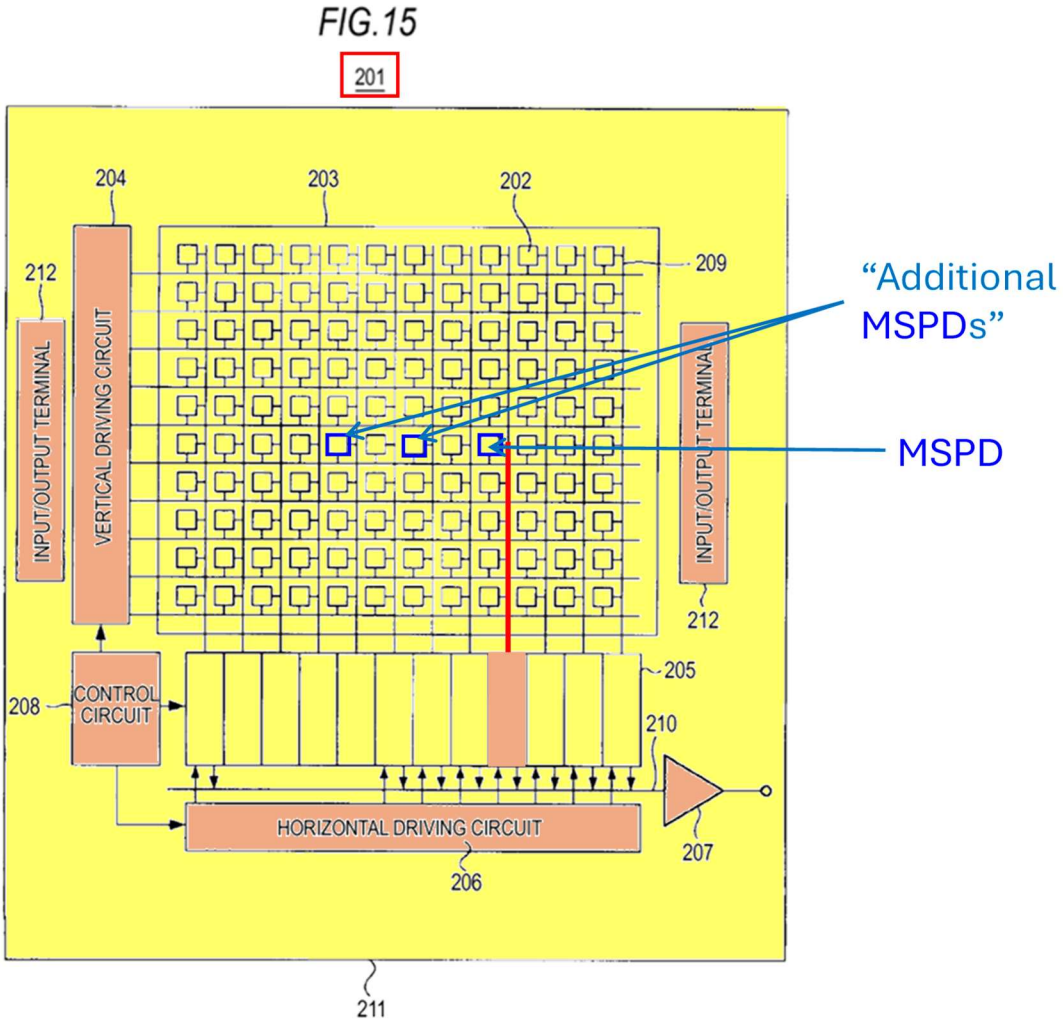
Kuboi, Figs. 15, 16; *Kuboi*, ¶¶[191]-[193]; Lebby, ¶222. When used in an apparatus above, output circuit 207 sends the processed signals to the external signal processing circuit 106. *Kuboi*, Fig. 16; Lebby, ¶223. A POSITA would have understood that output circuit 207 would require electrical contacts to interconnect it with external signal processing circuit 106, allowing the processed signals to be transferred from imaging device 201 to external processing circuit 106. Lebby, ¶¶222-223; *Kuboi*, ¶[192]. Additionally, *Kuboi* discloses that imaging device 201 includes "[a]n input/output terminal 212 [to] exchange[] signals with an external device." *Kuboi*, ¶[54]. *Kuboi* thus discloses this limitation. Lebby, ¶223.

A POSITA would have also found it obvious to incorporate electrical contacts in imaging device 201 to transfer processed signals from output circuit 207 to external signal processing circuitry, given that the use of such contacts was well known in CMOS solid-state integrated circuit devices. Lebby, ¶224; Ex-1016, 1-3. Since the use of electrical contacts to output signals from CMOS devices was well known and *Kuboi* discloses exchanging signals with an external device, a POSITA would have been motivated to include electrical contacts in imaging device 201 and would have had a reasonable expectation of success in implementing this modification. Lebby, ¶224.

18. Claim 28

a. [28a]: "The single-chip device of claim 1, further comprising one or more additional MSPD on or in the same substrate,"

Kuboi discloses this additional limitation. Lebby, ¶¶225-228. Imaging device 201 ("single-chip device") includes a plurality of pixels 202, each with a photoelectric conversion portion 14, arranged in a two-dimensional array on the same substrate 211 (addressing how each MSPD is formed on or in substrate 211). *Kuboi*, ¶[48], Fig. 15; Lebby, ¶225; VI.A.2.b (**[1pre(b)]**).



Kuboi, Fig. 15. Imaging device 201 includes multiple pixels 11 with photoelectric conversion portions 14 ("MSPD" of claim 1 and "additional MSPD[s]" of this claim). Lebby, ¶226; *Kuboi*, ¶¶[48],[55].

For instance, as illustrated below, *Kuboi* describes an embodiment where four pixels—blue pixel 53B, red pixel 53R, and two green pixels 53G—are arranged in a two-dimensional Bayer pattern:

FIG.6A

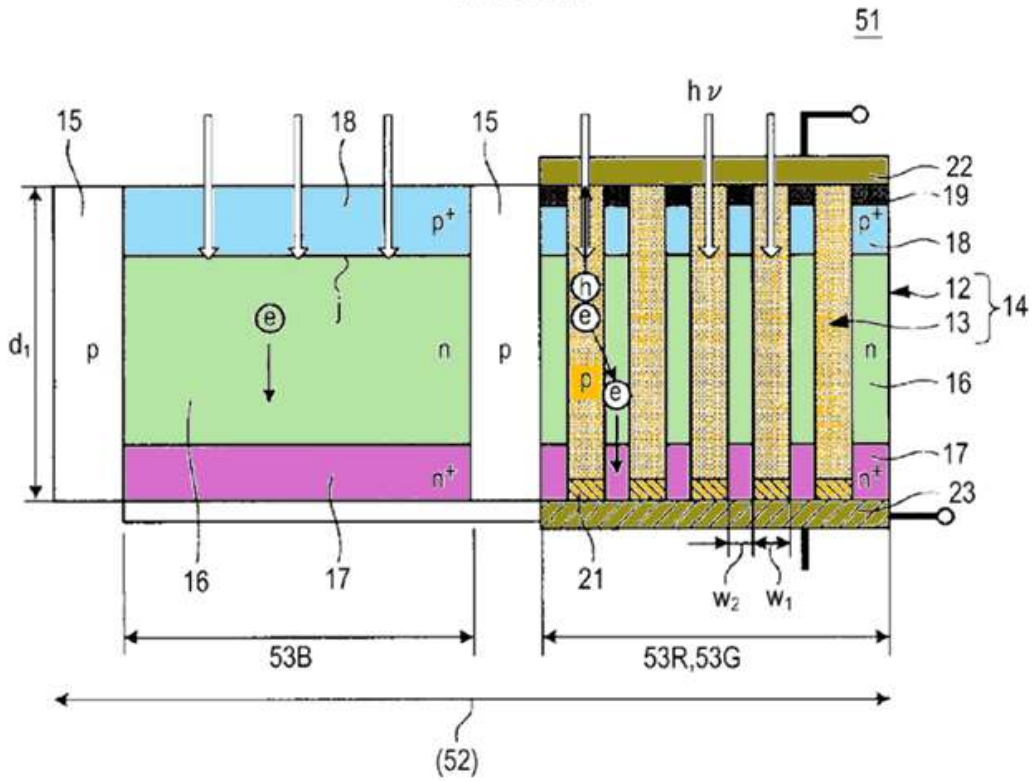
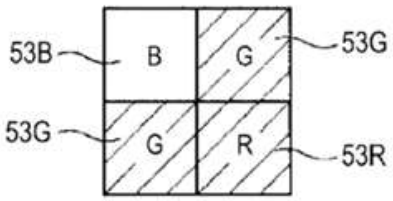


FIG.6B

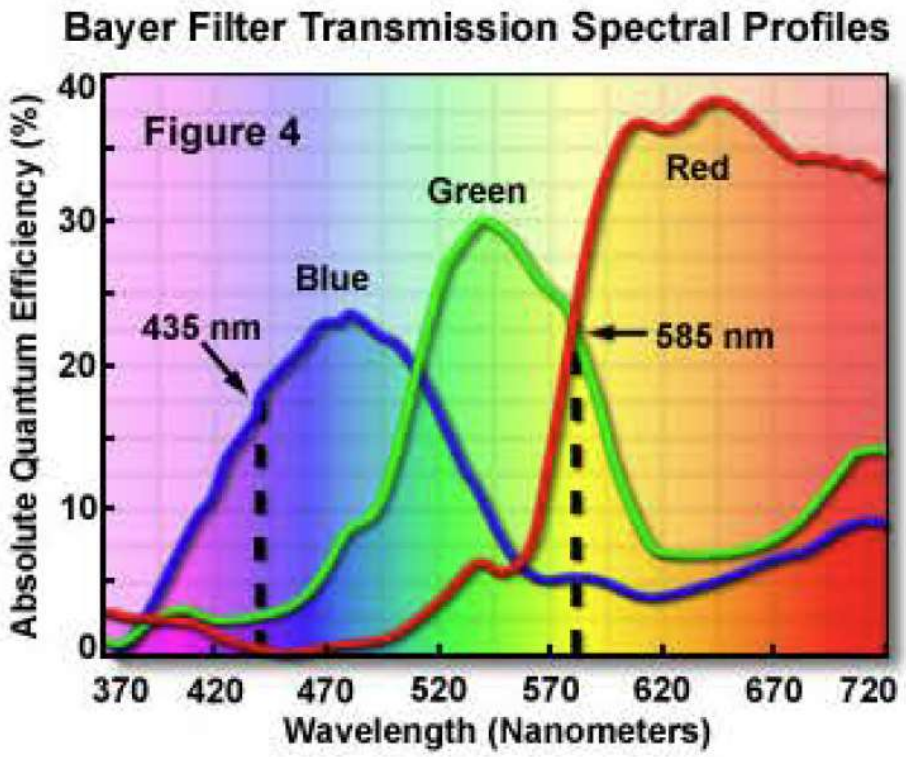


Kuboi, Figs. 6A-6B, ¶[90]. Red pixel 53R and green pixels 53G "are formed by the hybrid photoelectric conversion portion 14 shown in FIGS. 1A and 1B." *Kuboi*, ¶[90]. *Kuboi* teaches incorporating this pixel grouping into imaging device 201. Lebby, ¶¶227-228; *Kuboi*, ¶¶[48], [90]. Thus, imaging device 201 includes

multiple pixels 11 (e.g., one red pixel 53R and two green pixels 53G) with photoelectric conversion portions 14 (MSPD) on or in substrate 211. Lebby, ¶228.

b. [28b]: "and respective different optical bandpass filters coupled with at least two of the MSPDs on or in said single substrate, whereby at least two of said MSPDs are configured to respond to different wavelength ranges that are within said optical input."

Kuboi discloses this additional limitation. Lebby, ¶¶229-231. The four pixels (blue pixel 53B, red pixel 53R, and two green pixels 53G), which each include their own MSPD, also include corresponding color filters and on-chip microlenses in a Bayer arrangement formed over the pixels' upper electrodes 22. *Kuboi*, ¶¶[90], [93]; Lebby, ¶229. Each color filter is an optical bandpass filter that allows light at a specific band of wavelengths (or "wavelength band") corresponding to the filter color to pass through (while blocking other wavelengths). Lebby, ¶229; *Kuboi*, ¶[92] ("red wavelength band," "green wavelength band"); Ex-1015, 4-5. For example, as shown below, red, green, and blue color filters each have different wavelength bands:



Ex-1015, 4. Thus, photoelectric conversion portions 14 of red pixel 53R and green pixels 53G are coupled to different optical bandpass filters. Lebby, ¶230.

Red pixel 53R and green pixels 53G are designed to respond to different wavelength ranges within the incident light ("optical input"). Lebby, ¶231. For instance, photoelectric conversion films 13 of red pixel 53R are composed of a material "sensitive to [the] red wavelength band," while films 13 of green pixels 53G are made of a material "sensitive to [the] green wavelength band." *Kuboi*, ¶[92]. The red and green wavelength bands represent different wavelength ranges. Lebby, ¶231; *see* Ex-1015, 4. Thus, films 13 of red pixel 53R convert the red wavelength range in the incident light into electrical output, while films 13 of

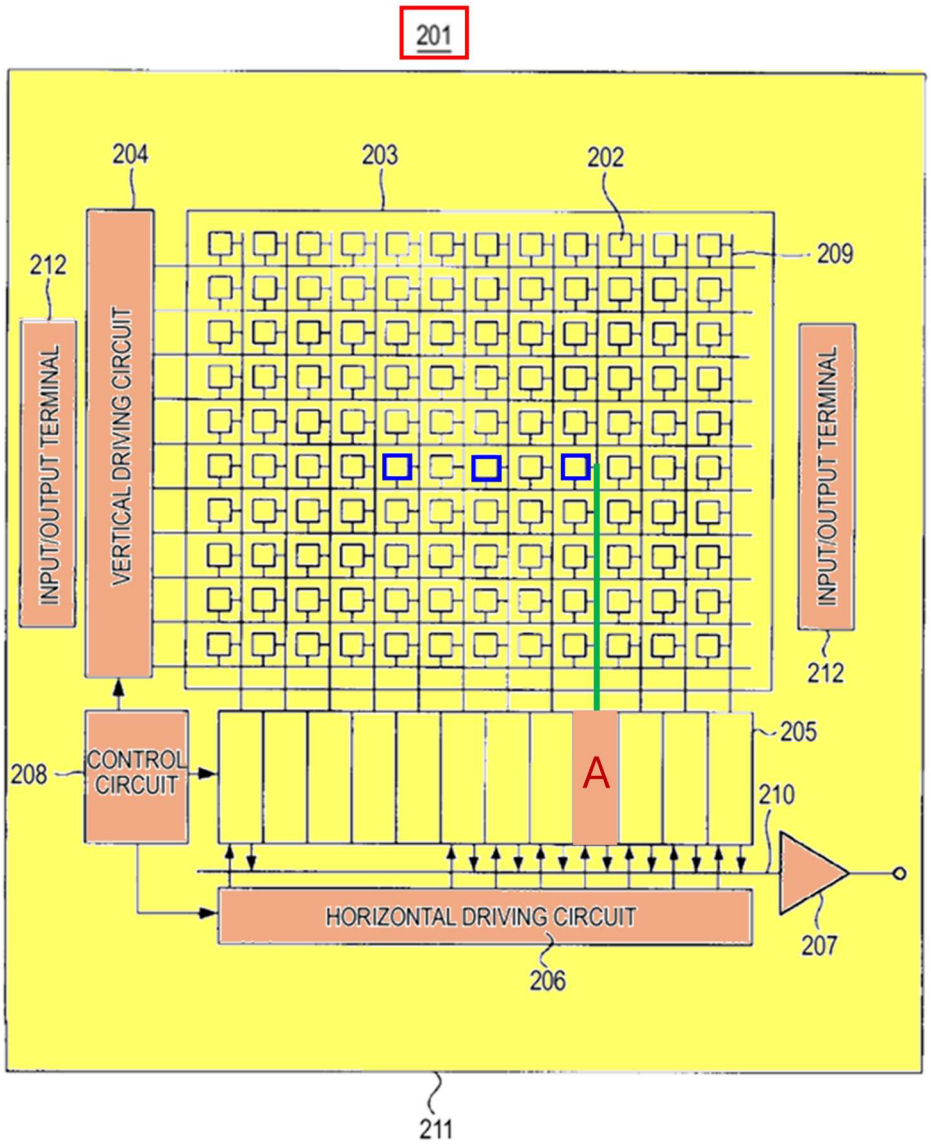
green pixels 53G convert the green wavelength range in the incident light into electrical output. Lebby, ¶231.

19. Claim 29

a. [29]: "The single-chip device of claim 1, further comprising one or more additional MSPDs on or in said single substrate, one or more additional active electronic circuits on or in the said single substrate, and one or more additional communication channels configured to supply electrical outputs from the MSPDs to the one or more of the active electronic circuits."

Kuboi discloses this additional limitation. Lebby, ¶¶232-235. As detailed for **[28a]**, imaging device 201 comprises multiple MSPDs on or in substrate 211. VI.A.18.a; Lebby, ¶232. As also explained for **[1pre(a)]** and **[1pre(b)]**, *Kuboi*'s active electronic circuit (which includes circuits 204-208) is on or in substrate 211. VI.A.2.a, VI.A.2.b; *Kuboi*, ¶¶[48]-[49], [78], Fig. 15. As explained for **[1n]**, imaging device 201 includes a communication channel (vertical signal line 209) that supplies the electrical output from a pixel 11 to a column signal processing circuit 205. VI.A.2.q. These components are shown below:

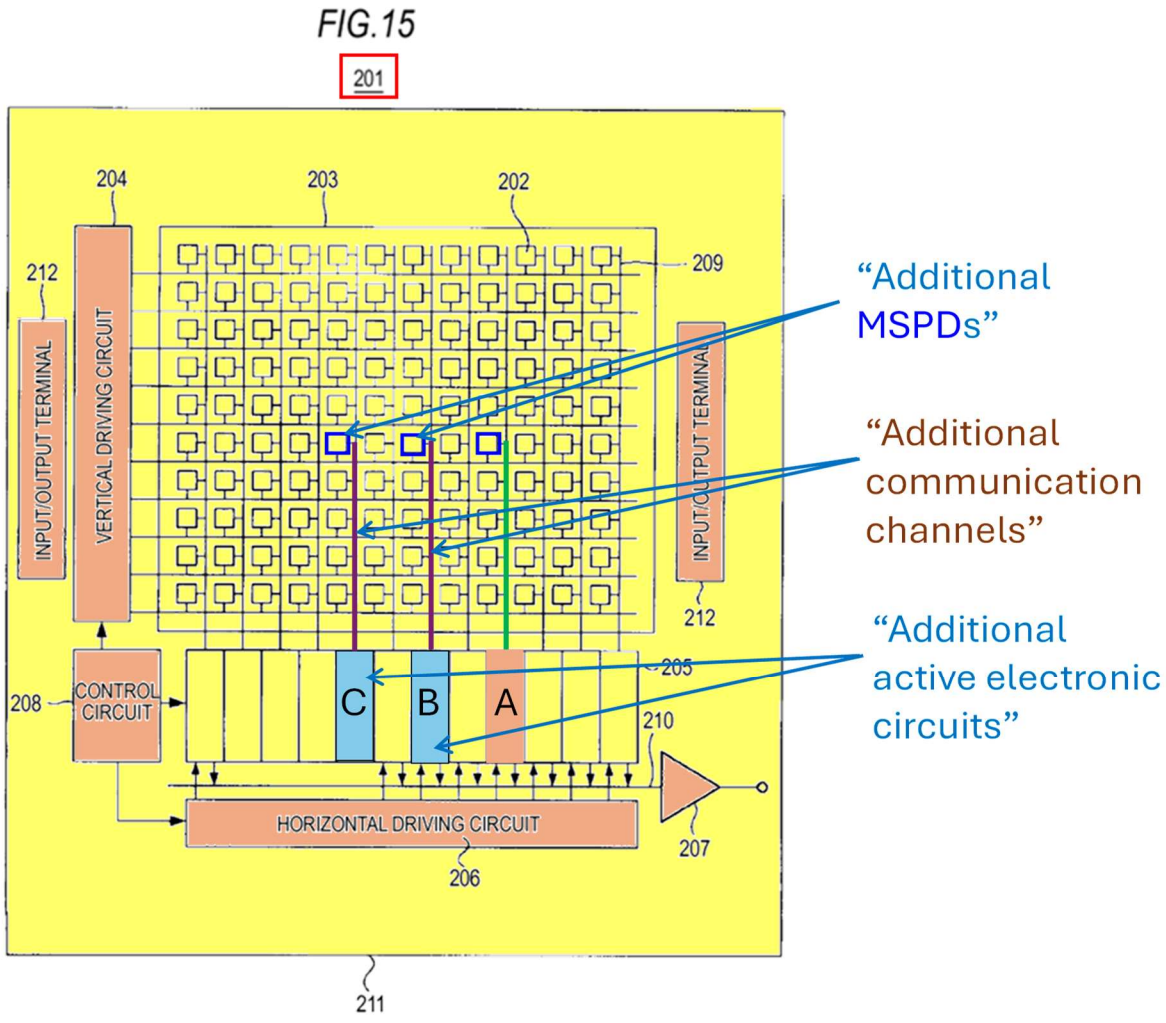
FIG.15



Kuboi, Fig. 15.

In addition to column signal processing circuit 205 of the claimed active electronic circuit (marked A in the figure above), the peripheral circuit portion includes multiple column signal processing circuits 205 provided "for each column of the pixels 202 and perform signal processing such as noise removal for each

pixel column on signals output from pixels 202 of one row." *Kuboi*, ¶[52]; Lebby, ¶¶232-233. Vertical driving circuit 204 activates pixels in a selected row and supplies the electrical output from each pixel (including pixels 11) to a corresponding column signal processing circuit 205 through a vertical signal line 209. *Kuboi*, ¶¶[51]-[52]; VI.A.2.c (**[1pre(c)]**); Lebby, ¶233. This is shown below:



Kuboi, Fig. 15. Thus, the electrical output from the first pixel 11 (and MSPD) is directed to a first signal processing circuit 205 (marked A) via a signal line 209, the electrical output from a second pixel 11 is routed to a second signal processing circuit 205 (marked B) via a second signal line 209, the electrical output from a third MSPD is conveyed to a third signal processing circuit 205 (marked C) via a third signal line 209, and so on. Lebby, ¶234; *Kuboi*, ¶¶[51]-[52].

The MSPD associated with the first pixel 11 is the "MSPD" of claim 1, while the MSPDs associated with the second and third pixels 11 are the "additional MSPDs" of this claim. Lebby, ¶235. The first signal processing circuit 205 (A) constitutes part of the "active electronic circuit" of claim 1, whereas the second and third signal processing circuits 205 (B and C) are the "additional active electronic circuits" of this claim. Lebby, ¶235. Similarly, signal line 209 is the "communication channel" of claim 1, and the signal lines 209 are the "additional communication channels" of this claim. Lebby, ¶235. As explained for **[1pre(a)]** and **[1pre(b)]**, all logic circuits of the peripheral circuit portion (including signal processing circuits B and C) are "active" electronic circuits comprising transistors, and all pixels and logic circuits of the peripheral circuit portion of imaging device 201 are formed on or in substrate 211. VI.A.2.a, VI.A.2.b; Lebby, ¶235.

20. Claim 30

a. [30]: "The single-chip device of claim 1, further comprising one or more additional active electronic circuits that are formed on or in the said single substrate."

Kuboi discloses this additional limitation. Lebby, ¶236. As explained for [29], the one or more additional active electronic circuits (signal processing circuits 205 B and C) are formed on or in substrate 211 of imaging device 201. VI.A.2.a (**[1pre(a)]**), VI.A.2.b (**[1pre(b)]**, VI.A.19.a (**[29]**); *Kuboi*, ¶[52]; Lebby, ¶236.

21. Claim 32

a. [32]: "The single-chip device of claim 1, further comprising one or more additional active electronic circuits that are formed on or in the said single substrate and comprise one or more of CMOS, BiCMOS, and bipolar active devices."

Kuboi discloses this additional limitation. Lebby, ¶¶237-238. As explained for **[29]**, the one or more additional active electronic circuits (signal processing circuits 205 B and C) are formed on or in substrate 211. VI.A.2.a (**[1pre(a)]**), VI.A.2.b (**[1pre(b)]**, VI.A.19.a (**[29]**); *Kuboi*, ¶[52]; Lebby, ¶237.

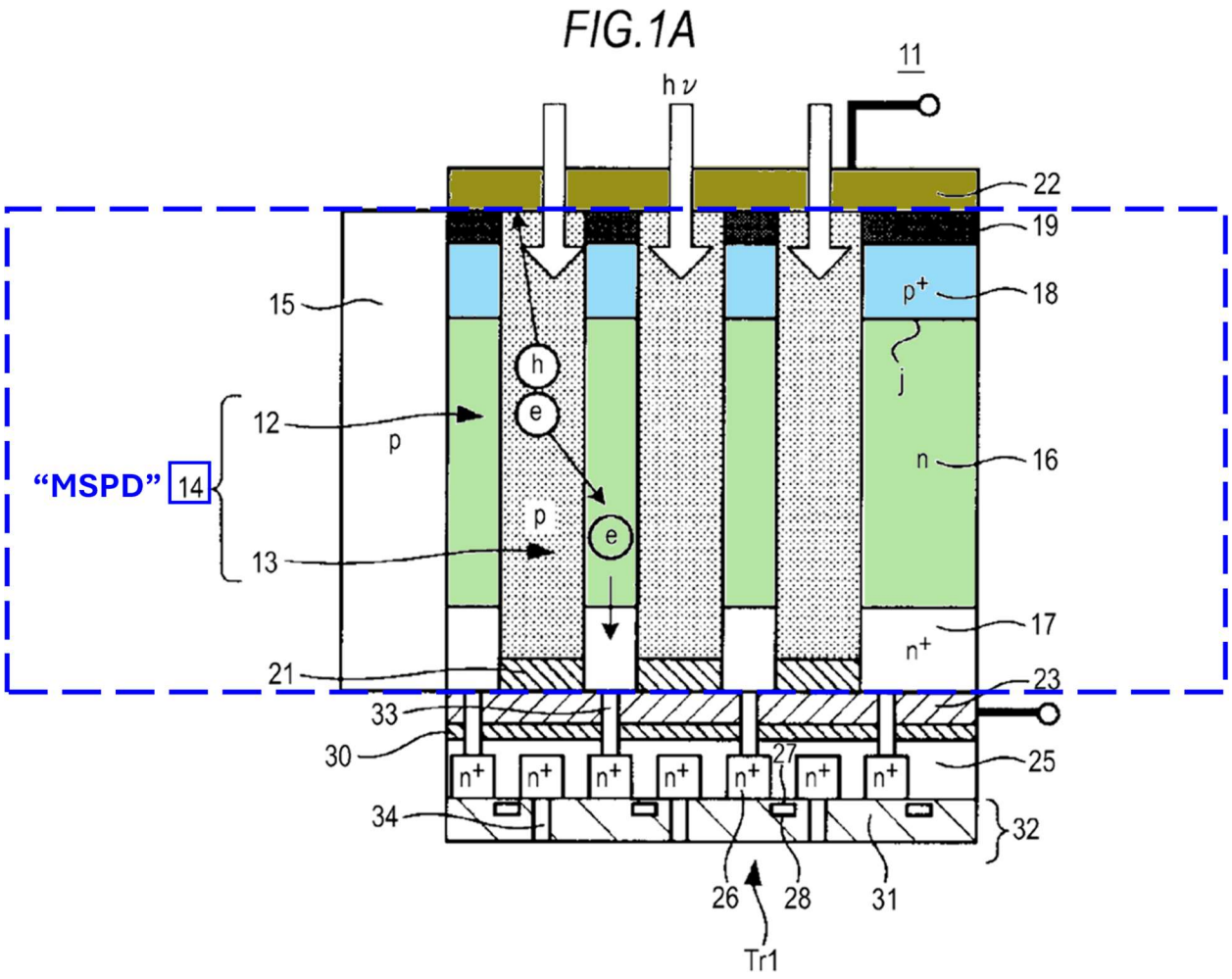
Kuboi further discloses that imaging device 201 is a "CMOS solid-state imaging device" fabricated using "existing CMOS techniques." *Kuboi*, ¶¶[3], [7], [48], [55]. A POSITA would have understood that, in a CMOS solid-state device

fabricated using existing CMOS fabrication techniques, all logic circuits of the peripheral circuit portion (including the active electronic circuit and the additional active electronic circuits) would be CMOS active devices. Lebby, ¶238.

22. Claim 35

a. [35]: "The single-chip device of claim 1, further including a layer of selected material that is over a side of one of the first and second layers facing away from the intermediate layer and is configured to reduce sheet resistance."

Kuboi discloses this additional limitation. Lebby, ¶¶239-241. As shown below, a transparent upper electrode 22, which is made of indium tin oxide (ITO), covers the entire light incident side of pixel 11's photoelectric conversion portion 14. *Kuboi*, ¶¶[60], [93], Fig. 1A; Lebby, ¶239.



Kuboi, Fig. 1A. Light enters photoelectric conversion portion 14 through transparent upper electrode 22. *Kuboi*, ¶¶[60], [64]; Lebby, ¶240. A POSITA would have understood that upper electrode 22 is formed over a side (the light incident side) of p^+-type region 18 ("first layer"), which faces away from n-type region 16 ("intermediate layer"). *See Kuboi*, Fig. 1A; Lebby, ¶240.

A POSITA would also have understood that an ITO film reduces sheet resistance.[9] Lebby, ¶241; *Higuchi*, ¶¶[16]-[17] (explaining that an ITO film on a photoelectric conversion device decreases the sheet resistance of the device due to the low sheet resistance of ITO). Upper electrode 22 is thus "configured to reduce sheet resistance," as claimed. Lebby, ¶241.

VII. Mandatory Notices

A. Real Parties-in-Interest

The real parties-in-interest are Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; Samsung Semiconductor, Inc.; and Samsung Austin Semiconductor LLC.

B. Related Matters

Patent Owner W&Wsens Devices Inc. asserted the '700 Patent in *W&Wsens Devices Inc. v. Samsung Electronics Co., Ltd., Samsung Electronics America, Inc.,*

[9] The '700 Patent acknowledges that an ITO layer on a photodiode reduces sheet resistance. '700 Patent, 27:48-51 ("Layer 1450 is a thin ITO like material … that can be deposited on the P and/or N layer(s) to reduce the sheet resistance of these layers."), 29:36-39 ("transparent conducting metal oxide may be used to reduce the sheet resistance").

Samsung Semiconductor, Inc., and Samsung Austin Semiconductor LLC, Case No. 2:24-cv-00854-JRG (E.D. Tex.). Patent Owner also asserted U.S. Patent No. 10,468,543 ("'543 Patent"), 12,087,871, 11,621,360, 9,525,084, and 12,243,948 in that case, which are related to the '700 Patent. Petitioner is simultaneously challenging the '543 Patent in IPR2025-00995.

C. Lead and Backup Counsel, and Service Information

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Please address all correspondence to counsel at the address above. Petitioner consents to electronic service by email at the above email addresses.

VIII. Grounds for Standing

Petitioner certifies that the ’700 Patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified herein.

IX. Conclusion

For the reasons above, Petitioner requests institution of IPR and cancellation of each challenged claim. The Office may charge any required fees to Deposit Account No. 06-0916.

Date: May 20, 2025

Respectfully submitted,

By: /Joshua L. Goldberg/
Joshua L. Goldberg
Lead Counsel
Reg. No. 59,369

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. §42.24, Petitioner certifies that the word count of Petitioner's Petition for *Inter Partes* Review (exclusive of any table of contents, table of authorities, mandatory notices under §42.8, certificates of service and word count, and list of exhibits or claim listing) as measured by Microsoft Word is 13,855.

Dated: May 20, 2025

By: /Joshua L. Goldberg/
Joshua L. Goldberg
Lead Counsel
Reg. No. 59,369

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§42.6(e) and 42.105(a), the undersigned certifies that on May 20, 2025, a copy of the foregoing **Petition for *Inter Partes* Review**, **the associated powers of attorney**, and **Exhibits 1001-1041** were served by FedEx Priority Overnight on the correspondence address of record indicated in the Patent Office's public Patent Center system for U.S. Patent No. 10,446,700:

Mr. Gerald M. Wissing
Wissing Miller LLP
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31 Hudson Yards, 11th Floor
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Date: May 20, 2025

By: /William Esper/
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